User's Manual

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RA6M5 Group

User's Manual: Hardware

32-bit MCU
Renesas Advanced (RA) Family
Renesas RA6 Series

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瑞萨电子高级(RA)系列32位MCU

Renesas RA6 Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. 防止静电放电(ESD)
   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。脚步
   必须采取措施，尽可能停止静电的产生，并在出现时迅速消散。环境控制必须
   足够的。干燥时，应使用加湿器。建议避免使用容易产生静电的绝缘体。
   半导体器件必须在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和
   包括工作台和地板在内的测量工具必须接地。操作员还必须使用腕带接地。半导体
   不得赤手触摸设备。对于安装有半导体器件的印刷电路板，必须采取类似的预防措施。
2. 上电处理
   通电时产品的状态是不确定的。LSI内部电路的状态是不确定的，
   通电时寄存器设置和引脚未定义。在将复位信号施加到外部复位的成品中
   管脚，从通电到复位过程完成，管脚的状态不能保证。以类似的方式，引脚的状态
   在通过片内上电复位功能复位的产品中，从供电时间到供电达到
   指定重置的级别。
3. 断电状态下的信号输入
   请勿在设备断电时输入信号或IO上拉电源。输入此类信号或IO导致的电流注入
   上拉电源可能会导致故障，此时通过设备的异常电流可能会导致内部退化
   元素。请按照产品文档中所述的电源关闭状态下的输入信号指南进行操作。
4. 处理未使用的引脚
   按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚是
   一般处于高阻状态。在开路状态下使用未使用的引脚操作时，会在附近感应出额外的电磁噪声
   LSI，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障
   成为可能。
5. 时钟信号
   应用复位后，只有在工作时钟信号稳定后才释放复位线。在程序中切换时钟信号时
   执行，等待目标时钟信号稳定。当时钟信号由外部谐振器或外部振荡器产生时
   在复位期间，确保只有在时钟信号完全稳定后才释放复位线。此外，当切换到时钟信号时
   在程序执行过程中由外部谐振器或外部振荡器产生，等待目标时钟信号稳定。
6. 输入引脚的电压施加波形
   由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在VIL之间的区域
   (Max.)和VIH(Min.)由于噪音，例如，设备可能发生故障。小心，以防止颤动的噪音进入设备时，
   输入电平是固定的，并且在输入电平通过VIL(Max.)和VIH(Min.)之间的区域时的过渡期间也是如此。
7. 禁止访问保留地址
   禁止访问保留地址。保留地址是为将来可能的功能扩展提供的。不要访问这些
   不能保证LSI的正确操作。
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   在从一种产品更改为另一种产品之前，例如更改为具有不同部件号的产品，请确认更改不会导致问题。
   同一组中的微处理单元或微控制器单元产品的特性，但具有不同的部件号，其特性可能会有所不同
   内部存储器容量，布局模式和其他因素，这些因素会影响电气特性的范围，例如特性值，
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RA生态工作室

Preface

1. About this document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using the Renesas Microcontroller. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

3. Renesas Publications

Renesas provides the following documents. Before using any of these documents, visit www.renesas.com for the most up-to-date version of the document.

Component	Document Type	Description
Microcontrollers	Data sheet	Features, overview, and electrical characteristics of the MCU
	User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
	Application Notes	Technical notes, board design guidelines, and software migration information
	Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata
Software	User's Manual: Software	API reference and programming information
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications
Tools & Kits, Solutions	User's Manual: Development Tools	User's manual and quick start guide for developing embedded software applications with Development Kits (DK), Starter Kits (SK), Promotion Kits (PK), Product Examples (PE), and Application Examples (AE)
	User's Manual: Software	
	Quick Start Guide	
	Application Notes	Project files, guidelines for software programming, and application examples to develop embedded software applications

Preface

1. 关于本文档

本手册一般由产品概述、CPU说明、系统控制功能、外围功能、电气特性和使用说明组成。本手册描述了微控制器(MCU)超集的产品规格。根据您的产品，某些引脚、寄存器或功能可能不存在。保留存储不可用寄存器的地址空间。

2. Audience

本手册是为使用瑞萨微控制器设计和编程应用程序的系统设计人员编写的。要求用户具备电路、逻辑电路和MCU的基本知识。

3. Renesas Publications

瑞萨电子提供以下文件。在使用任何这些文档之前，请访问www.renesas.com以获取该文档的最新版本。

Component	文件类型	Description
Microcontrollers	数据表	MCU的特性、概述和电气特性
	User's Manual: Hardware	MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述
	应用笔记	技术说明、电路板设计指南和软件迁移信息
	技术更新(TU)	限制、勘误等产品规格的初步报告
Software	User's Manual: Software	API参考和编程信息
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例
工具和套件 解决方案	用户手册：开发工具	使用开发套件(DK)、入门套件(SK)、促销套件(PK)、产品示例(PE)和应用程序开发嵌入式软件应用程序的用户手册和快速入门指南
	User's Manual: Software	
	快速入门指南	Examples (AE)
	应用笔记	用于开发嵌入式软件应用程序的项目文件、软件编程指南和应用程序示例

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4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
0x1F	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 0x1F. In some cases, a hexadecimal number is shown with the suffix "h".
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
WDT.WDTRCR.RSTIRQS	Periods separated a function module symbol (WDT), register symbol (WDTRCR), and bit field symbol (RSTIRQS).
WDT.WDTRCR	A period separated a function module symbol (WDT) and register symbol (WDTRCR).
WDTRCR.RSTIRQS	A period separated a register symbol (WDTRCR) and bit field symbol (RSTIRQS).
CKS[3:0]	Numbers in brackets expresses a bit number. For example, CKS[3:0] occupies bits 3 to 0 of the WDT Control Register (WDTCR) register.

6. Unit and Unit Prefix

The following units and unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Symbol	Name	Description
b	Binary Digit	Single 0 or 1
B	Byte	This unit is generally used for memory specification of the MCU and address space.
k	kilo-	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	Kilo-	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings.

Term	Description
NC	Not connected pin. NC means that pin is not connected to the MCU.
Hi-Z	High impedance.

4. 编号符号

本手册通篇使用以下编号符号：

Example	Description
011b	二进制数。例如，数字3的二进制等价物是011b。
0x1F	十六进制数。例如，数字31的十六进制等效项被描述为0x1F。在某些情况下，显示的十六进制数带有后缀“h”。
1234	十进制数。仅当存在混淆的可能性时，才在十进制数后面加上此符号。十进制数字通常不带后缀。

5. 排版符号

本手册通篇使用以下印刷符号：

Example	Description
WDT.WDTRCR.RSTIRQS	句点分隔功能模块符号(WDT)、寄存器符号(WDTRCR)和位域符号(RSTIRQS)。
WDT.WDTRCR	句点分隔功能模块符号(WDT)和寄存器符号(WDTRCR)。
WDTRCR.RSTIRQS	一个句点分隔寄存器符号(WDTRCR)和位域符号(RSTIRQS)。
CKS[3:0]	括号中的数字表示一个位数。例如，CKS[3:0]占用WDT的3到0位 控制寄存器(WDTCR)寄存器。

6. 单位和单位前缀

以下单位和单位前缀有时会产生误导。这些单位前缀在本手册中进行了描述，含义如下：

Symbol	Name	Description
b	二进制数字	单个0或1
B	Byte	该单元一般用于MCU的内存规范和地址空间。
k	kilo-	1000=103。k也用于表示1024(210)，但在本手册中，此单位前缀用于表示1 000(103)。
K	Kilo-	1024=210。在本手册中，该单位前缀用于表示1024(210)而不是1000(103)。

7. 特别条款

以下术语具有特殊含义。

Term	Description
NC	未连接引脚。NC表示该引脚未连接到MCU。
Hi-Z	高阻抗。

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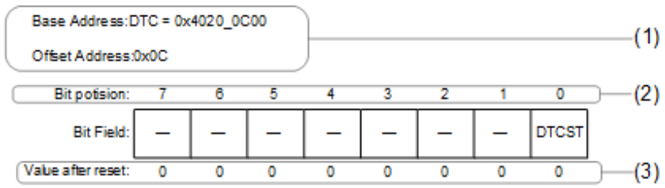
8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. Base Address and Offset Address mean DTC Module Start Register (DTCST) of Data Transfer Controller (DTC) is assigned to address 0x4020_0C00.

(2) Bit number

This number indicates the bit number. This bits are shown in order from bits 31 to 0 for 32-bit register, from bits 15 to 0 for 16-bit register, and from bits 7 to 0 for 8-bit register.

(3) Value after reset

This symbol or number indicate the value of each bit after a hard reset. The value is shown in binary unless specified otherwise.

0: Indicates that the value is 0 after a reset.

1: Indicates that the value is 1 after a reset.

x: Indicates that the value is undefined after a reset.

(4) Symbol

Symbol indicates the short name of bit field. Reserved bit is expressed with a —.

(5) Function

Function indicates the full name of the bit field and enumerated values.

(6) R/W

The R/W column indicates access type whether the bit field is readable or writable.

R/W: The bit field is readable and writable.

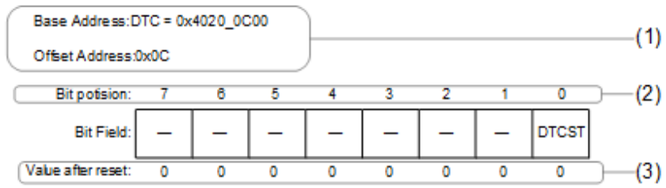
R: The bit field is readable only. Writing to this bit field has no effect.

W: The bit field is writable only. The read value is the same as after a reset unless specified otherwise.

8. 注册说明

每个寄存器描述都包括显示位分配的寄存器图和描述每个位内容的寄存器位表。这些表中使用的符号示例将在以下部分中描述。以下是寄存器描述和相关位字段定义的示例。

XXXX DTCST : DTC Module Start Register



(4) (5) (6)

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0:DTC module stop 1:DTC module start	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

(1)功能模块符号、寄存器符号、地址分配

一般表示该寄存器的功能模块符号、寄存器符号、地址分配。基地址和偏移地址意味着数据传输控制器(DTC)的DTC模块起始寄存器(DTCST)分配到地址0x4020_0C00。

(2)位号

该数字表示位数。对于32位寄存器，这些位按位31到0、16位寄存器从位15到0、8位寄存器从位7到0的顺序显示。

(3)复位后的值

该符号或数字表示硬复位后每个位的值。除非另有说明，否则该值以二进制显示。

0：表示复位后值为0。

1：表示复位后值为1。

x：表示复位后该值未定义。

(4) Symbol

符号表示位域的简称。保留位用—表示。

(5) Function

函数表示位域的全称和枚举值。

(6) R/W

RW列指示位字段是可读还是可写的访问类型。

RW：位域可读可写。

R：位域是只读的。写入该位域无效。

W：位域只可写。除非另有说明，否则读取的值与复位后的值相同。

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9. Abbreviations

Abbreviations used in this document are shown in the following table.

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating Point Unit
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-on reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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9. Abbreviations

本文档中使用的缩写如下表所示。

Abbreviation	Description
AES	高级加密标准
AHB	先进的高性能总线
AHB-AP	AHB访问端口
APB	先进的外围总线
ARC	Alleged RC
ATB	高级跟踪总线
BCD	二进制编码的十进制
BSDL	边界扫描描述语言
DES	数据加密标准
DSA	数字签名算法
ETB	嵌入式跟踪缓冲区
ETM	嵌入式跟踪宏单元
FLL	锁频环
FPU	浮点单元
HMI	人机接口
IrDA	红外数据协会
LSB	最低有效位
MSB	最高有效位
NVIC	嵌套向量中断控制器
PC	程序计数器
PFS	端口功能选择
PLL	锁相环
POR	Power-on reset
PWM	脉冲宽度调制
RSA	Rivest Shamir Adleman
SHA	安全哈希算法
S/H	采样和保持
SP	堆栈指针
SWD	串口线调试
SW-DP	串行线调试端口
TRNG	真随机数发生器
UART	通用异步收发器
VCO	压控振荡器

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RA生态工作室

High-performance 200 MHz Arm Cortex-M33 core, up to 2 MB code flash memory with Dual-bank, background and SWAP operation, 8 KB Data flash memory, and 512 KB SRAM with Parity/ECC. High-integration with Ethernet MAC controller, USB 2.0 High-Speed, CAN FD, SDHI, Quad and Octa SPI, and advanced analog. Integrated Secure Crypto Engine with cryptography accelerators, key management support, tamper detection and power analysis resistance in concert with Arm TrustZone for integrated secure element functionality.

Features

■ Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 200 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

■ Memory

- Up to 2-MB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 512-KB SRAM

■ Connectivity

- Serial Communications Interface (SCI) × 10
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding (SCI3, SCI4)
- I²C bus interface (IIC) × 3
- Serial Peripheral Interface (SPI) × 2
- Quad Serial Peripheral Interface (QSPI)
- Octa Serial Peripheral Interface (OSPI)
- USB 2.0 Full-Speed Module (USBFS)
- USB 2.0 High-Speed Module (USBHS)
- CAN with Flexible Data-rate (CANFD) × 2
- Ethernet MAC/DMA Controller (ETHERC/EDMAC)
- SD/MMC Host Interface (SDHI)
- Serial Sound Interface Enhanced (SSIE)
- Consumer Electronics Control (CEC)

■ Analog

- 12-bit A/D Converter (ADC12) × 2
  - 5 Msps at interleaving
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-bit (GPT32) × 4
- General PWM Timer 16-bit (GPT16) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 6

■ Security and Encryption

- Secure Crypto Engine 9
  - Symmetric algorithms: AES
  - Asymmetric algorithms: RSA, ECC, and DSA
  - Hash-value generation: SHA224, SHA256, GHASH
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to three or six regions for the code flash, depending on the bank mode
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- Device lifecyle management
- Pin function
  - Up to three tamper pins
  - Secure pin multiplexing

■ System and Power Management

- Low power modes
- Battery backup function (VBATT)
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

■ Human Machine Interface (HMI)

- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL/PLL2
- Clock out support

■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating Voltage

- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
- Ta = -40°C to +85°C
  - 176-pin BGA (13 mm × 13 mm, 0.8 mm pitch)

高性能200MHzArmCortex-M33内核，高达2MB的代码闪存，具有双存储区、后台和SWAP操作、8KB数据闪存和512KBSRAM，具有奇偶校验ECC。与以太网MAC控制器、USB2.0高速、CANFD、SDHI、Quad和OctaSPI以及高级模拟高度集成。具有加密加速器的集成安全加密引擎、密钥管理支持、篡改检测和电源分析抗性与ArmTrustZone相结合，可实现集成安全元件功能。

Features

■Arm®Cortex®-M33内核

●带有主扩展的Armv8-M架构●最大工作频率：200MHz●Arm内存保护单元（ArmMPU）

受保护的内存系统架构(PMSAv8) 安全MPU(MPU_S)：8个区域 非安全MPU(MPU_NS)：8个区域●SysTick计时器

嵌入两个Systick计时器：安全和非安全实例 由LOCO或系统时钟驱动●CoreSight ETM-M33

■ Memory

●高达2-MB代码闪存●8-KB数据闪存（100 000次程序擦除(PE)周期）●512-KBSRAM

■ Connectivity

●串行通信接口(SCI)×10-异步接口-8位时钟同步接口-智能卡接口-简单IIC-简单SPI-曼彻斯特编码(SCI3 SCI4)●I2C总线接口(IIC)×3●串行外设接口(SPI)×2●四路串行外设接口(QSPI)●八路串行外设接口(OSPI)●USB2.0全速模块(USBFS)●USB2.0高速模块(USBHS)●具有灵活数据速率的CAN(CANFD)×2●以太网MACDMA控制器(ETHERCEDMAC)●SDMMC主机接口(SDHI)●增强型串行声音接口(SSIE)●消费电子控制(CEC)

■ Analog

●12位AD转换器(ADC12)×25Msps交错●12位DA转换器(DAC12)×2●温度传感器(TSN)

■ Timers

●通用PWM定时器32位(GPT32)×4●通用PWM定时器16位(GPT16)×6●低功耗异步通用定时器(AGT)×6

■安全和加密●安全加密引擎9

对称算法：AES 非对称算法：RSA、ECC和DSA 哈希值生成：SHA224、SHA256、GHASH 128位唯一ID●Arm®TrustZone®

代码闪存最多三个或六个区域，具体取决于存储区模式 数据闪存最多两个区域 SRAM最多三个区域 每个外围设备的单独安全或非安全安全属性●设备生命周期管理●引脚功能

最多三个防篡改引脚
安全引脚复用

■系统和电源管理●低功耗模式●电池备份功能（VBATT）

●支持日历和VBATT的实时时钟(RTC)●事件链接控制器(ELC)●数据传输控制器(DTC)●DMA控制器(DMAC)×8●上电复位●具有电压设置的低电压检测(LVD)●看门狗定时器（WDT）●独立看门狗定时器（IWDT）

■人机界面(HMI)●电容式触摸感应单元(CTSU)

■多个时钟源

●主时钟振荡器（MOSC）（8至24MHz）●副时钟振荡器（SOSC）（32.768kHz）●高速片上振荡器（HOCO）（161820MHz）●中速片上振荡器(MOCO)(8MHz)●低速片上振荡器(LOCO)(32.768kHz)●IWDT专用片上振荡器(15kHz)●HOCOMOCOLOCO的时钟微调功能●PLLPLL2●时钟输出支持

■ General-Purpose I/O Ports

●5V容差、开漏、输入上拉、可切换驱动能力

■工作电压●VCC：2.7至3.6V

■工作温度和封装●Ta=-40℃to+105℃

176引脚LQFP（24mm×24mm，0.5mm间距） 144引脚LQFP（20mm×20mm，0.5mm间距） 100引脚LQFP（14mm×14mm，0.5mm间距）●Ta=-40℃至+85℃

176-pin BGA (13 mm × 13 mm, 0.8 mm pitch)

RA生态工作室

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 200 MHz with the following features:

- Up to 2 MB code flash memory
- 512 KB SRAM
- Quad Serial Peripheral Interface (QSPI), Octa Serial Peripheral Interface (OSPI)
- Ethernet MAC Controller (ETHERC), USBFS, USBHS, SD/MMC Host Interface
- Capacitive Touch Sensing Unit (CTSU)
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 200 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 2 MB of code flash memory. See section 50, Flash Memory.
Data flash memory	8 KB of data flash memory. See section 50, Flash Memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 48, SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/USB boot mode See section 3, Operating Modes.
Resets	The MCU provides 14 resets. See section 5, Resets.

1. Overview

MCU集成了多个系列的软件和基于Arm®引脚兼容的32位内核，这些内核共享一组通用的瑞萨外围设备可促进设计可扩展性和高效的基于平台的产品开发。

该系列中的MCU包含一个运行频率高达200MHz的高性能ArmCortex®-M33内核，具有以下特性：

●高达2MB的代码闪存
- 512 KB SRAM
●四路串行外设接口（QSPI）、八路串行外设接口（OSPI）
●以太网MAC控制器(ETHERC)、USBFS、USBHS、SDMMC主机接口
●电容式触控感应单元(CTSU)
●模拟外设
●安全和安全功能

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M33内核	• 最大工作频率：高达200MHz • Arm Cortex-M33 core: – 带有安全扩展的Armv8-M架构 – Revision: r0p4-00rel0 • Arm内存保护单元（ArmMPU） – 受保护的内存系统架构(PMSAv8) – 安全MPU(MPU_S)：8个区域 – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – 嵌入两个Systick计时器：安全和非安全实例 – 由SysTick定时器时钟(SYSTICCLK)或系统时钟(ICLK)驱动 • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	功能说明
代码闪存	最大2MB代码闪存。 请参阅第50节，闪存。
数据闪存	8KB数据闪存。请参阅第50节 ，闪存。
Option-setting memory	选项设置存储器确定复位后MCU的状态。 请参阅第6节，选项设置内存。
SRAM	具有奇偶校验位或纠错码(ECC)的片上高速SRAM。 参见第48节，SRAM。

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种操作模式：● • SCIUSB启动模式 请参阅第3节，操作模式。
Resets	MCU提供14次复位。 请参阅第5节，重置。

RA生态工作室

Table 1.3 System (2 of 2)

Feature	Functional description
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds. See section 7, Low Voltage Detection (LVD).
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL/PLL2 • Clock out support See section 8, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts. See section 13, Interrupt Controller Unit (ICU).
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 11, Battery Backup Function.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR). See section 12, Register Write Protection.
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU). See section 15, Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention. See section 18, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 17, Data Transfer Controller (DTC).
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 16, DMA Controller (DMAC).

Table 1.3 系统(2之2)

Feature	功能说明
低电压检测(LVD)	低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。请参见第7节，低电压检测(LVD)。
Clocks	• 主时钟振荡器(MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL/PLL2 • 打卡支持 请参见第8节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在被选为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。请参见第9节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。请参阅第13节，中断控制器单元(ICU)。
低功耗模式	可以通过多种方式降低功耗，包括设置时钟分频器、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参阅第10节，低功耗模式。
电池备份功能	提供电池备份功能，由电池部分供电。电池供电区域包括RTC、SOSC、备份存储器以及VCC和VBATT之间的切换。请参阅第11节，电池备份功能。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。请参见第12节，寄存器写保护。
内存保护单元(MPU)	MCU有一个内存保护单元(MPU)。 请参阅第15节，内存保护单元(MPU)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。请参阅第18节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅第17节，数据传输控制器(DTC)。
DMA Controller (DMAC)	MCU包括一个8通道直接内存访问控制器(DMAC)，无需CPU干预即可传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。请参见第16节，DMA控制器(DMAC)。

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Table 1.6 External bus interface

Feature	Functional description
External buses	● CS area (ECBIU): Connected to the external devices (external memory interface) ● QSPI area (EQBIU): Connected to the QSPI (external device interface) ● OSPI area (EOBIU): Connected to the OSPI (external device interface)

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 4 channels and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 21, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state See section 20, Port Output Enable for GPT (POEG).
Low power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register. See section 22, Low Power Asynchronous General Purpose Timer (AGT).
Realtime Clock (RTC)	The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 23, Realtime Clock (RTC).
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. See section 24, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDT).

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 10 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface ● Extended Serial interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3 to 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 30, Serial Communications Interface (SCI).
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 3 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 31, I2C Bus Interface (IIC).

Table 1.6 外部总线接口

Feature	功能说明
外部总线	● CS区（ECBIU）：连接外部设备（外部存储器接口） ● QSPI区（EQBIU）：连接到QSPI（外部设备接口） ● OSPI区（EOBIU）：连接到OSPI（外部设备接口）

Table 1.7 Timers

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有GPT32×4通道的32位定时器和一个具有GPT16×6通道。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参见第21节，通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	端口输出启用(POEG)功能可以将通用PWM定时器(GPT)输出引脚置于输出禁用状态，请参见第20节，GPT端口输出启用(POEG)。
低功耗异步通用 目的定时器(AGT)	低功耗异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参见第22节，低功耗异步通用定时器(AGT)。
实时时钟(RTC)	实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。请参阅第23节，实时时钟(RTC)。
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。请参见第24节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。请参见第25节，独立看门狗定时器(IWDT)。

Table 1.8 通信接口（2个中的1个）

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)×10通道具有异步和同步串行接口：● 异步接口（UART和异步通信接口适配器(ACIA)） ● 8位时钟同步接口 ● Simple IIC (master-only) ● 简单的SPI ● 智能卡接口 ● 曼彻斯特界面 ● 扩展串行接口 智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0 3to9)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。参见第30节，串行通信接口(SCI)。
I2C总线接口(IIC)	I2C总线接口(IIC)有3个通道。IIC模块符合并提供NXPI2C（内部集成电路）总线接口功能的子集。请参见第31节，I2C总线接口(IIC)。

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 34, Serial Peripheral Interface (SPI).
Control Area Network with Flexible Data-Rate Module (CAN-FD)	The CAN with Flexible Data-Rate (CAN-FD) module can handle classical CAN frames and CAN-FD frames complied with ISO 11898-1 standard. The module supports 16 transmit buffers per channel and 16 receive buffer per channel. See section 32, CAN-FD.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 28, USB 2.0 Full-Speed Module (USBFS).
USB 2.0 High-speed Module (USBHS)	The USB 2.0 High-Speed Module (USBHS) that operates as a host or a device controller compliant with the Universal Serial Bus (USB) Specification revision 2.0. The host controller supports USB 2.0 high-speed, fullspeed, and low-speed transfers, and the device controller supports USB 2.0 high-speed and full-speed transfers. The USBHS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification. The USBHS has FIFO buffer for data transfers, providing a maximum of 10 pipes. See section 29, USB 2.0 High-Speed Module (USBHS).
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 35, Quad Serial Peripheral Interface (QSPI).
Octa Serial Peripheral Interface (OSPI)	The Octa Serial Peripheral Interface (OSPI) module is a memory controller for connecting OctaFlash and OctaRAM. See section 36, Octa Serial Peripheral Interface (OSPI).
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I^2S/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 38, Serial Sound Interface Enhanced (SSIE).
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 39, SD/MMC Host Interface (SDHI).
Ethernet MAC (ETHERC)	One-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. See section 26, Ethernet MAC Controller (ETHERC).
Consumer Electronics Control module (CEC)	The CEC transmission/reception module can generate and receive CEC signals complied with the High-Definition Multimedia Interface (HDMI) Ver.1.4b. And the module can automaticall detect communication states. See section 37, CEC Transmission/Reception Circuit (CEC).

Table 1.8 通信接口（2个中的2个）

Feature	功能说明
串行外设接口(SPI)	串行外围接口(SPI)提供与多个处理器和外围设备的高速全双工同步串行通信。请参阅第34节，串行外设接口(SPI)。
灵活的控制局域网 Data-Rate Module (CAN-FD)	具有灵活数据速率(CAN-FD)模块的CAN可以处理经典CAN帧和CAN FD框架符合ISO11898-1标准。 该模块支持每个通道16个发送缓冲器和每个通道16个接收缓冲器。 参见第32节，CAN-FD。
USB2.0全速模块(USBFS)	USB2.0全速模块(USBFS)可以作为主机控制器或设备控制器运行。 该模块支持全速和低速（仅限主机控制器）传输，如通用串行总线规范2.0。该模块有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，最多可提供10个管道。可以根据用于通信的外围设备或根据您的系统为管道1到9分配任何端点编号。请参阅第28节，USB2.0全速模块(USBFS)。
USB2.0高速模块(USBHS)	作为主机或设备控制器运行的USB2.0高速模块(USBHS)，符合通用串行总线(USB)规范修订版2.0。主机控制器支持USB2.0高速、全速和低速传输，设备控制器支持USB2.0高速和全速传输。USBHS有一个内部USB收发器，并支持在 USB2.0规范。 USBHS具有用于数据传输的FIFO缓冲区，最多提供10个管道。 请参阅第29节，USB2.0高速模块(USBHS)。
四路串行外设接口(QSPI)	QuadSerialPeripheralInterface(QSPI)是一种存储器控制器，用于连接具有SPI兼容接口的串行ROM（非易失性存储器，例如串行闪存、串行EEPROM或串行FeRAM）。请参见第35节，四通道串行外设接口(QSPI)。
Octa串行外设接口(OSPI)	Octa串行外设接口(OSPI)模块是用于连接的内存控制器 OctaFlash and OctaRAM. 请参阅第36节，八进制串行外设接口(OSPI)。
增强型串行声音接口(SSIE)增强型串行声音接口(SSIE)外设提供与数字音频设备接口的功能，用于通过串行总线传输I2S单声道TDM音频数据。SSIE支持高达50MHz的音频时钟频率，并可作为从属或主接收器、发送器或收发器运行，以适应各种应用。SSIE在接收器和发送器中包含32级FIFO缓冲区，并支持中断和DMA驱动的数据接收和发送。请参阅第38节，增强的串行声音接口(SSIE)。	
SDMMC主机接口(SDHI)	SDHI和多媒体卡(MMC)接口模块提供将各种外部存储卡连接到MCU所需的功能。SDHI支持1位和4位总线，用于连接支持SD、SDHC和SDXC格式的存储卡。在开发符合SD规范的主机设备时，您必须遵守SD主机辅助产品许可协议(SDHALA)。MMC接口支持提供eMMC4.51（JEDEC标准JESD84-B451）器件访问的1位、4位和8位MMC总线。该接口还提供向后兼容性并支持高速SDR传输模式。请参阅第39节，SDMMC主机接口(SDHI)。
以太网MAC(ETHERC)	符合以太网IEEE802.3媒体访问控制(MAC)层协议的单通道以太网MAC控制器(ETHERC)。ETHERC通道提供一个MAC层接口通道，将MCU连接到允许发送和接收符合以太网和IEEE802.3标准的帧的物理层LSI(PHY-LSI)。ETHERC连接到以太网DMA控制器(EDMAC)，因此可以在不使用CPU的情况下传输数据。请参阅第26节，以太网MAC控制器(ETHERC)。
消费电子控制模块(CEC)	CEC发射接收模块可以产生和接收符合高清多媒体接口(HDMI)Ver.1.4b的CEC信号。并且模块可以自动检测通讯状态。 请参见第37节，CEC发送接收电路(CEC)。

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 29 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. See section 43, 12-Bit A/D Converter (ADC12).
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided. See section 44, 12-Bit D/A Converter (DAC12).
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application. See section 45, Temperature Sensor (TSN).

Table 1.10 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode. See section 46, Capacitive Touch Sensing Unit (CTSU).

Table 1.11 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. See section 40, Cyclic Redundancy Check (CRC).
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. See section 47, Data Operation Circuit (DOC).

Table 1.12 Security

Feature	Functional description
Securty function	• ARMv8-M TrustZone security • Device lifecycle management • Debug access level • Key injection • Secure pin multiplexing
Secure Crypto Engine 9 (SCE9)	• Symmetric algorithms: AES • Asymmetric algorithms: RSA, ECC, and DSA • Hash-value generation: SHA224, SHA256, GHASH • 128-bit unique ID. See section 42, Secure Cryptographic Engine (SCE9).

Table 1.9 Analog

Feature	功能说明
12-bit A/D Converter (ADC12)	提供了一个12位逐次逼近模数转换器。最多可选择29个模拟输入通道。可选择温度传感器输出和内部参考电压进行转换。请参阅第43节，12位AD转换器(ADC12)。
12-bit D/A Converter (DAC12)	提供了一个12位DA转换器(DAC12)。 请参阅第44节，12位DA转换器(DAC12)。
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压被提供给ADC12进行转换，并且可以被最终应用进一步使用。请参见第45节，温度传感器(TSN)。

Table 1.10 人机界面

Feature	功能说明
电容式触控感应单元(CTSU)	电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，该软件使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电导体包围，因此手指不会直接接触电极。请参阅第46节，电容式触摸传感单元(CTSU)。

Table 1.11 数据处理

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。请参阅第40节，循环冗余校验(CRC)。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，比较16位数据并可以生成中断。参见第47节，数据操作电路(DOC)。

Table 1.12 Security

Feature	功能说明
安全功能	• ARMv8-M TrustZone security • 设备生命周期管理 • 调试访问级别 • 密钥注入 • 安全引脚复用
安全加密引擎9(SCE9)	• Symmetric algorithms: AES • 非对称算法：RSA、ECC和DSA • Hash-value generation: SHA224, SHA256, GHASH ●128位唯一标识。请参阅第42节，安全加密引擎(SCE9)。

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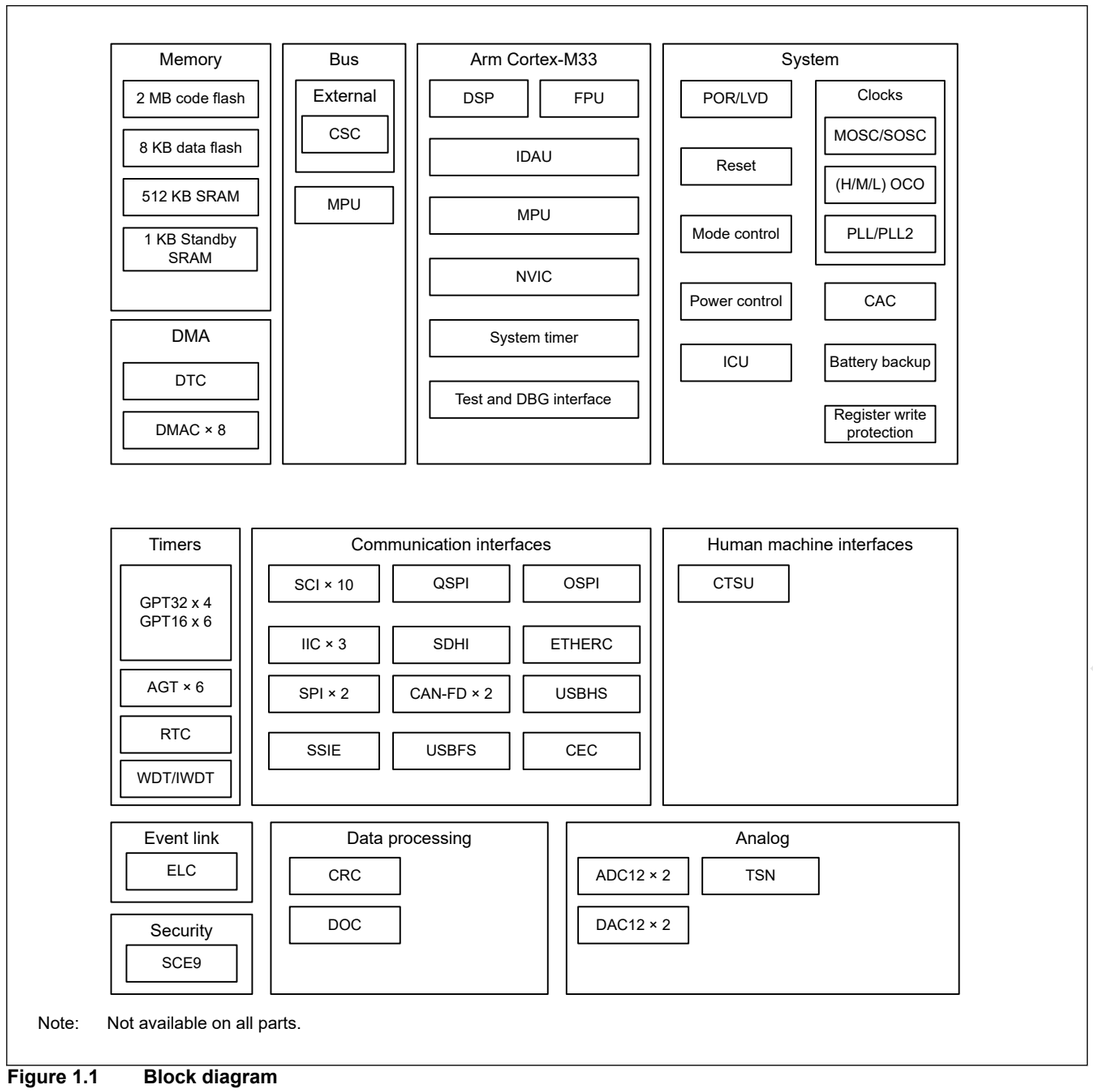
1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.



Note: Not available on all parts.

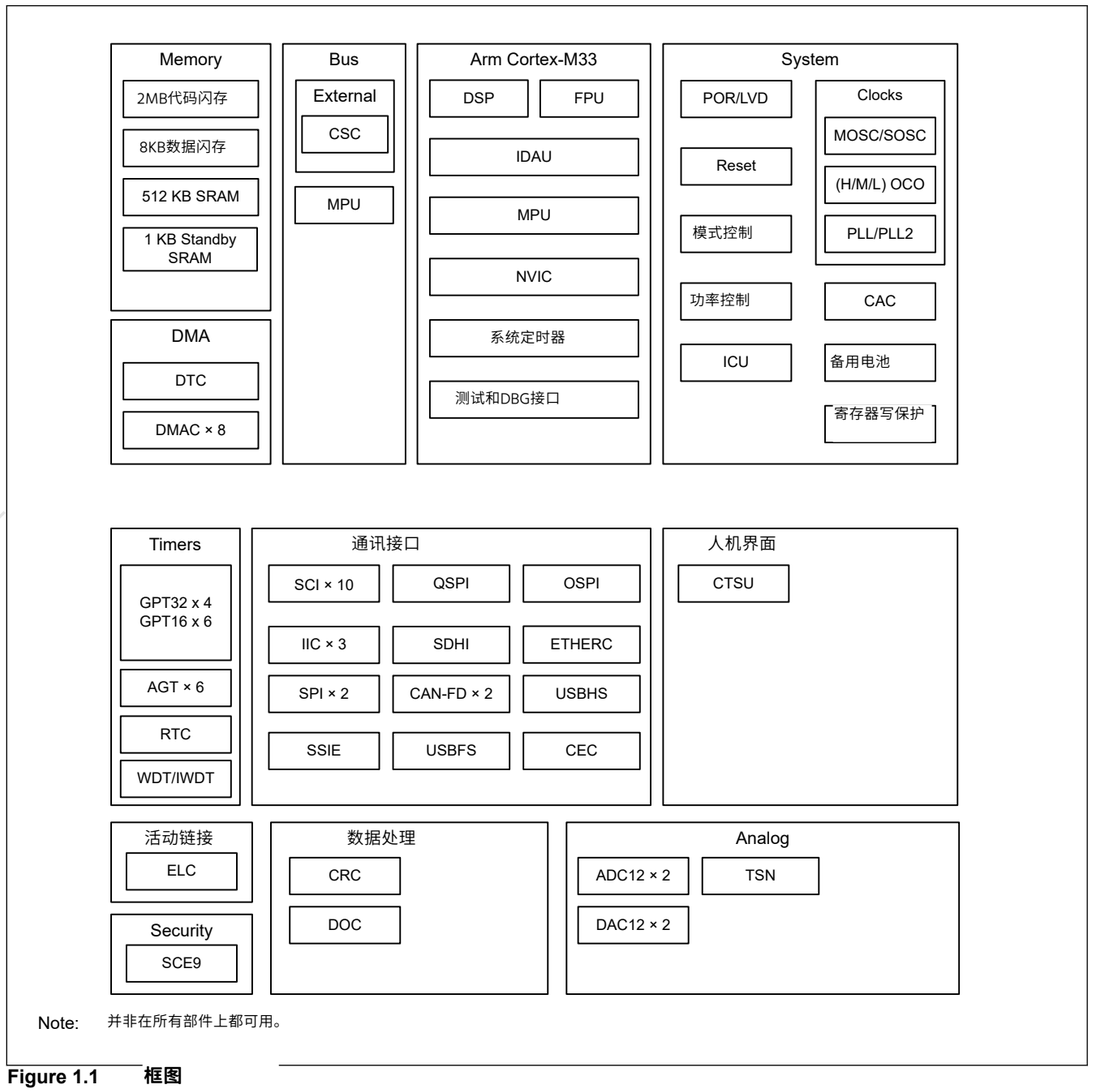
Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.13 shows a list of products.

1.2 框图

图1.1显示了MCU超集的框图。组内的某些单独设备具有部分功能。



Note: 并非在所有部件上都可用。

Figure 1.1 框图

1.3 零件编号

图1.2显示了产品部件号信息，包括内存容量和封装类型。表1.13显示了产品列表。

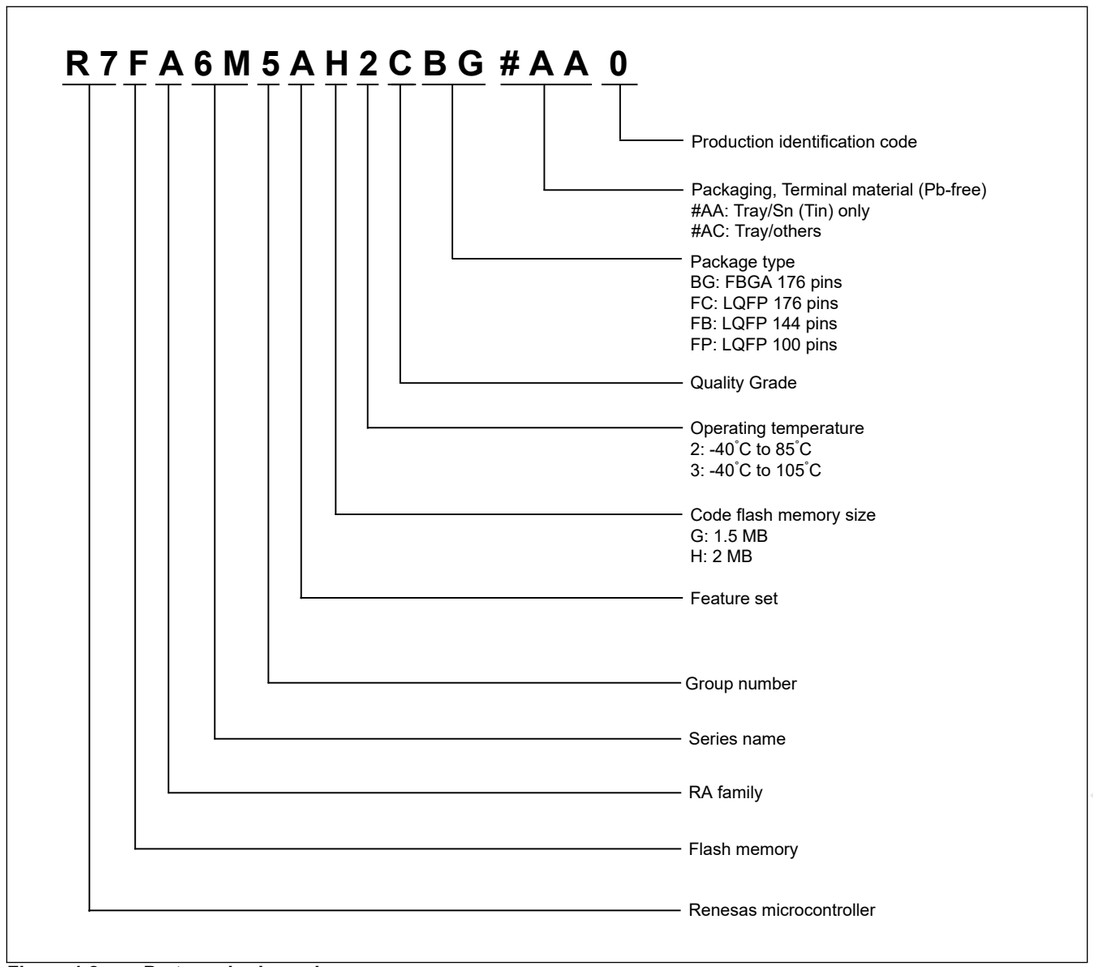


Figure 1.2 Part numbering scheme

Table 1.13 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6M5AH2CBG	PLBG0176GF-A	2 MB	8 KB	512 KB	-40 to +85°C
R7FA6M5AH3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5AH3CFB	PLQP0144KA-B				
R7FA6M5AH3CFP	PLQP0100KB-B				
R7FA6M5AG2CBG	PLBG0176GF-A	1.5 MB			-40 to +85°C
R7FA6M5AG3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5AG3CFB	PLQP0144KA-B				
R7FA6M5AG3CFP	PLQP0100KB-B				

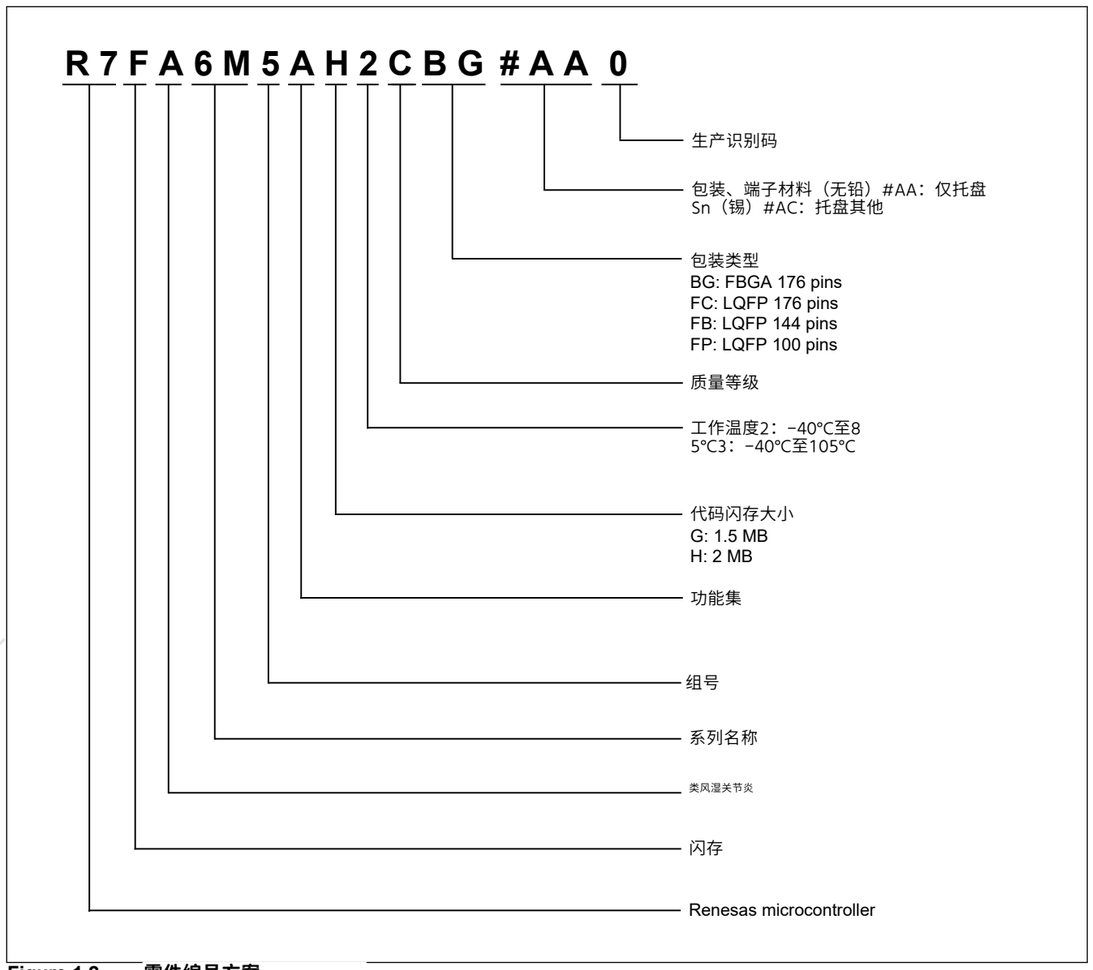


Figure 1.2 零件编号方案

Table 1.13 产品列表

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA6M5AH2CBG	PLBG0176GF-A	2 MB	8 KB	512 KB	-40 to +85°C
R7FA6M5AH3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5AH3CFB	PLQP0144KA-B				
R7FA6M5AH3CFP	PLQP0100KB-B				
R7FA6M5AG2CBG	PLBG0176GF-A	1.5 MB			-40 to +85°C
R7FA6M5AG3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5AG3CFB	PLQP0144KA-B				
R7FA6M5AG3CFP	PLQP0100KB-B				

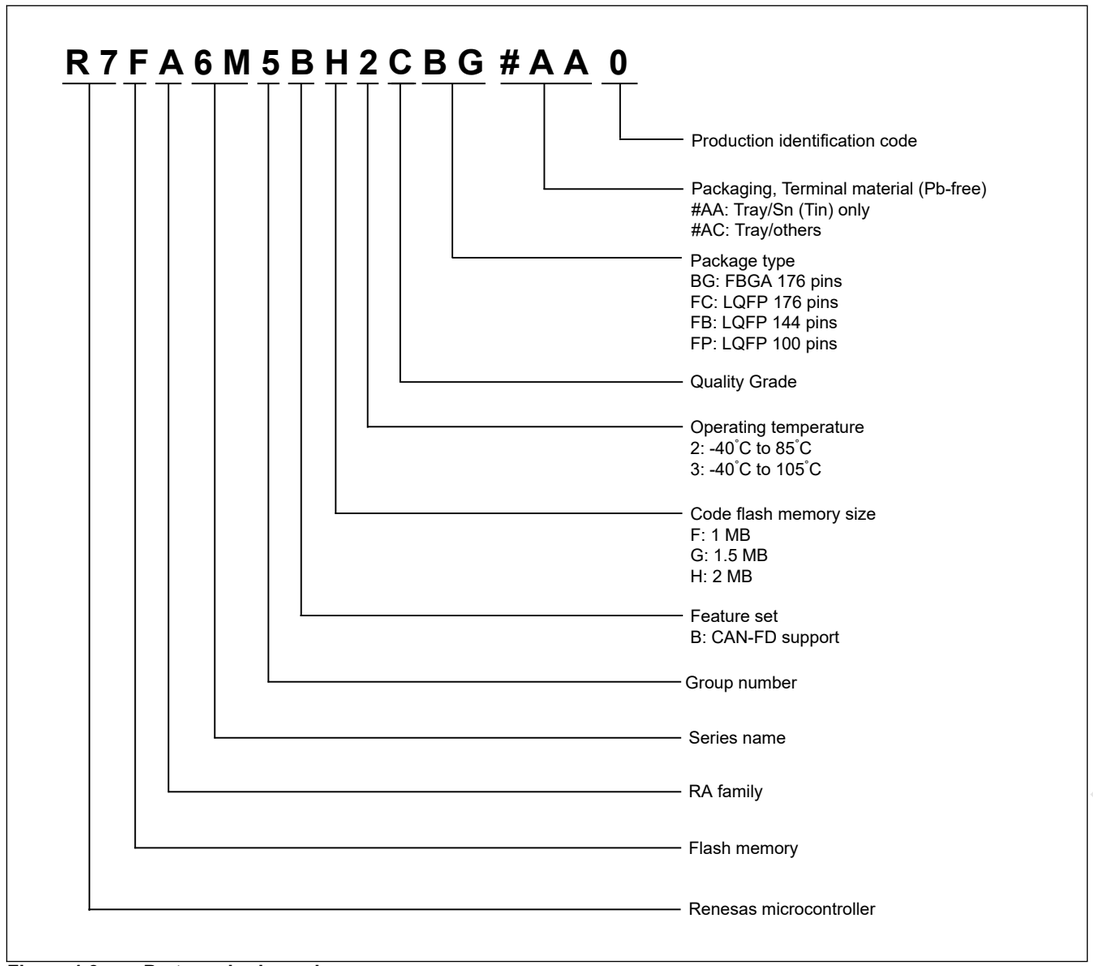


Figure 1.3 Part numbering scheme

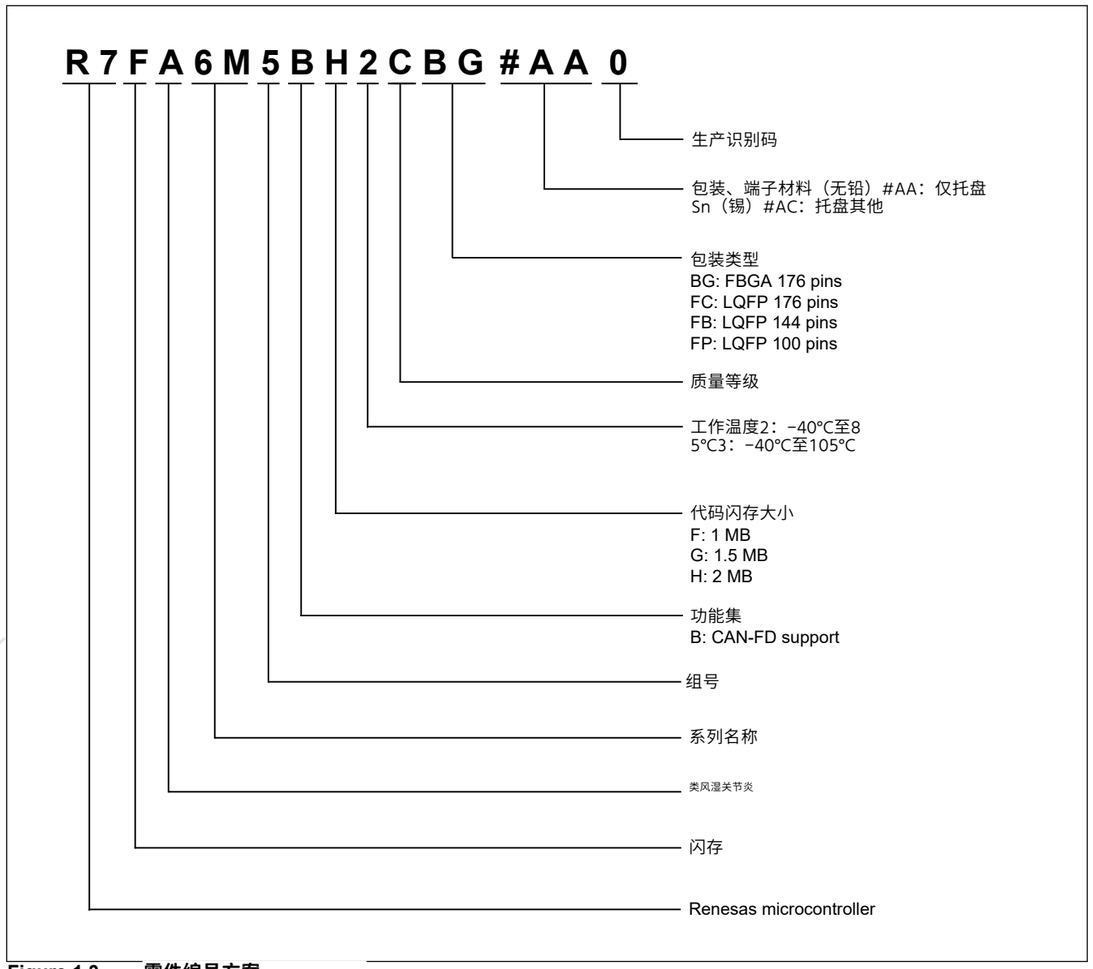


Figure 1.3 零件编号方案

Table 1.14 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6M5BH2CBG	PLBG0176GE-A	2 MB	8 KB	512 KB	-40 to +85°C
R7FA6M5BH3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5BH3CFB	PLQP0144KA-B				
R7FA6M5BH3CFP	PLQP0100KB-B				
R7FA6M5BG2CBG	PLBG0176GE-A	1.5 MB			-40 to +85°C
R7FA6M5BG3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5BG3CFB	PLQP0144KA-B				
R7FA6M5BG3CFP	PLQP0100KB-B				
R7FA6M5BF2CBG	PLBG0176GE-A	1 MB			-40 to +85°C
R7FA6M5BF3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5BF3CFB	PLQP0144KA-B				
R7FA6M5BF3CFP	PLQP0100KB-B				

Table 1.14 产品列表

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA6M5BH2CBG	PLBG0176GE-A	2 MB	8 KB	512 KB	-40 to +85°C
R7FA6M5BH3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5BH3CFB	PLQP0144KA-B				
R7FA6M5BH3CFP	PLQP0100KB-B				
R7FA6M5BG2CBG	PLBG0176GE-A	1.5 MB			-40 to +85°C
R7FA6M5BG3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5BG3CFB	PLQP0144KA-B				
R7FA6M5BG3CFP	PLQP0100KB-B				
R7FA6M5BF2CBG	PLBG0176GE-A	1 MB			-40 to +85°C
R7FA6M5BF3CFC	PLQP0176KB-C				-40 to +105°C
R7FA6M5BF3CFB	PLQP0144KA-B				
R7FA6M5BF3CFP	PLQP0100KB-B				

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1.4 Function Comparison

Table 1.15 Function Comparison

Parts number		R7FA6M5XX2CBG	R7FA6M5XX3CFC	R7FA6M5XX3CFB	R7FA6M5XX3CFP
Pin count		176		144	100
Package		BGA	LQFP		
Code flash memory		2 MB, 1.5 MB, 1 MB			
Data flash memory		8 KB			
SRAM		512 KB			
	Parity	448 KB			
	ECC	64 KB			
Standby SRAM		1 KB			
DMA	DTC	Yes			
	DMAC	8			
BUS	External bus	16-bit bus			8-bit bus
System	CPU clock	200 MHz (max.)			
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL			
	CAC	Yes			
	WDT/IWDT	Yes			
	Backup register	128 B			
Communication	SCI	10		10	10
	IIC	3			
	SPI	2			
	CAN or CANFD	2			
	USBFS	Yes			
	USBHS	Yes		No	
	QSPI	Yes			
	OSPI	Yes			
	SSIE	Yes			
	SDHI/MMC	Yes			
	ETHERC	Yes			
	CEC	Yes			
Timers	GPT32*1	4			
	GPT16*1	6			
	AGT*1	6			
	RTC	Yes			
Analog	ADC12	Unit 0: 13, Unit 1: 16		Unit 0: 12, Unit 1: 13	Unit 0: 11, Unit 1: 9
	DAC12	2			
	TSN	Yes			
HMI	CTSU	20			12
Data processing	CRC	Yes			
	DOC	Yes			
Event control	ELC	Yes			
Security		SCE9, TrustZone, and Lifecycle management			

1.4 功能比较

Table 1.15 功能比较

零件编号		R7FA6M5XX2CBG	R7FA6M5XX3CFC	R7FA6M5XX3CFB	R7FA6M5XX3CFP
针数		176		144	100
Package		BGA	LQFP		
代码闪存		2 MB, 1.5 MB, 1 MB			
数据闪存		8 KB			
SRAM		512 KB			
	Parity	448 KB			
	ECC	64 KB			
Standby SRAM		1 KB			
DMA	DTC	Yes			
	DMAC	8			
BUS	外部总线	16-bit bus			8-bit bus
System	中央处理器时钟	200 MHz (max.)			
	CPU时钟源	MOSC, SOSC, HOCO, MOCO, LOCO, PLL			
	CAC	Yes			
	WDT/IWDT	Yes			
	备份寄存器	128 B			
Communication	SCI	10		10	10
	IIC	3			
	SPI	2			
	CAN或CANFD	2			
	USBFS	Yes			
	USBHS	Yes		No	
	QSPI	Yes			
	OSPI	Yes			
	SSIE	Yes			
	SDHI/MMC	Yes			
	ETHERC	Yes			
	CEC	Yes			
Timers	GPT32*1	4			
	GPT16*1	6			
	AGT*1	6			
	RTC	Yes			
Analog	ADC12	Unit 0: 13, Unit 1: 16		Unit 0: 12, Unit 1: 13	Unit 0: 11, Unit 1: 9
	DAC12	2			
	TSN	Yes			
HMI	CTSU	20			12
数据处理	CRC	Yes			
	DOC	Yes			
事件控制	ELC	Yes			
Security		SCE9、TrustZone和生命周期管理			

Note: The product name differs depend on the memory size and whether CAN or CANFD is supported. see section 1.3. Part Numbering
Note 1. Available pins depend on the Pin count, about details see section 1.7. Pin Lists.

Note: 产品名称因内存大小以及是否支持CAN或CANFD而异。见第1.3节。零件编号
注1.可用管脚取决于管脚数，详情见1.7节。引脚列表。

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1.5 Pin Functions

Table 1.16 Pin functions (1 of 7)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL/VCL0	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VBATT	Input	Battery Backup power pin
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	Output clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWO	Output	Serial wire trace output pin
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode

1.5 引脚功能

Table 1.16 引脚功能(1of7)

Function	Signal	I/O	Description
电源	VCC	Input	电源引脚。将其连接到系统电源。通过一个0.1μF电容将此引脚连接到VSS。电容应靠近引脚放置。
	VCL/VCL0	I/O	通过用于稳定内部电源的平滑电容器将此引脚连接到VSS引脚。将电容器靠近引脚放置。
	VBATT	Input	电池备用电源引脚
	VSS	Input	接地引脚。将其连接到系统电源(0V)。
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过EXTAL引脚输入。
	EXTAL	Input	
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
On-chip emulator	TMS	I/O	片上仿真器或边界扫描引脚
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	用于与跟踪数据同步的输出时钟
	TDATA0 to TDATA3	Output	跟踪数据输出
	SWO	Output	串行线迹输出引脚
	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQn	Input	可屏蔽中断请求引脚
	IRQn-DS	Input	可屏蔽中断请求引脚，也可用于Deep软件待机模式

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Table 1.16 Pin functions (2 of 7)

Function	Signal	I/O	Description
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active-low
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low
	WRn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active-low
	BCn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active-low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active-low
	CSn	Output	Select signals for CS areas, active-low
	A00 to A23	Output	Address bus
	D00 to D15	I/O	Data bus
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCICn	Input	Time capture event input pins

Table 1.16 引脚功能(2of7)

Function	Signal	I/O	Description
外部总线接口	RD	Output	指示正在从外部总线接口空间读取的选通信号，低电平有效
	WR	Output	Strobe信号指示正在写入外部总线接口空间，在1-writestrobe模式下，低电平有效
	WRn	Output	选通信号指示任一组数据总线引脚（D07到D00或D15到D08）在写入外部总线接口空间时有效，在字节选通模式下，低电平有效
	BCn	Output	选通信号指示任一组数据总线引脚（D07到D00或D15到D08）在访问外部总线接口空间时有效，在1写选通模式下，低电平有效
	ALE	Output	选择地址数据复用总线时的地址锁存信号
	WAIT	Input	用于访问外部空间的等待请求信号的输入引脚，低电平有效
	CSn	Output	CS区域的选择信号，低电平有效
	A00 to A23	Output	地址总线
	D00 to D15	I/O	数据总线
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	外部触发输入引脚
	GTIOCnA, GTIOCnB	I/O	输入捕捉、输出比较或PWM输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEEn	Input	外部事件输入使能信号
	AGTIOn	I/O	外部事件输入和脉冲输出引脚
	AGTOn	Output	脉冲输出引脚
	AGTOAn	Output	输出比较匹配A输出引脚
	AGTOBn	Output	输出比较匹配B输出引脚
RTC	RTCOUT	Output	用于1Hz或64Hz时钟的输出引脚
	RTCICn	Input	时间捕捉事件输入引脚

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Table 1.16 Pin functions (3 of 7)

Function	Signal	I/O	Description
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	RXDXn	Input	Input pins for received data (Extended Serial Mode)
	TXDXn	Output	Output pins for transmitted data (Extended Serial Mode)
	SIOXn	I/O	Input/output pins for receivde or tramsmitted data (Extended Serial Mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CAN or CANFD	CRXn	Input	Receive data
	CTXn	Output	Transmit data

Table 1.16 引脚功能(3of7)

Function	Signal	I/O	Description
SCI	SCKn	I/O	时钟输入输出引脚（时钟同步模式）
	RXDn	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXDn	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTSn_RTSn	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效。
	CTSn	Input	开始传输的输入。
	SCLn	I/O	IIC时钟的输入输出引脚（简单IIC模式）
	SDAn	I/O	IIC数据的输入输出引脚（简单IIC模式）
	SCKn	I/O	时钟输入输出引脚（简单SPI模式）
	MISOn	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSIn	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	RXDXn	Input	接收数据的输入引脚（扩展串行模式）
	TXDXn	Output	传输数据的输出引脚（扩展串行模式）
	SIOXn	I/O	用于接收或传输数据的输入输出引脚（扩展串行Mode)
	SSn	Input	片选输入引脚（简单SPI模式），低电平有效
IIC	SCLn	I/O	时钟的输入输出引脚
	SDAn	I/O	数据输入输出引脚
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	用于从主机输出数据的输入或输出引脚
	MISOA, MISOB	I/O	从机数据输出的输入或输出引脚
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	从机选择的输出引脚
CAN或CANFD	CRXn	Input	接收数据
	CTXn	Output	传输数据

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Table 1.16 Pin functions (4 of 7)

Function	Signal	I/O	Description
USBFS	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_OVRCURA-DS, USB_OVRCURB-DS	Input	Overcurrent pins for USBFS that can also be used in Deep Software Standby mode. Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
USBHS	VCC_USBHS	Input	Power supply pin
	VSS1_USBHS, VSS2_USBHS	Input	Ground pin
	AVCC_USBHS	Input	Analog power supply
	AVSS_USBHS	Input	Analog ground pin Must be shorted to the PVSS_USBHS pin
	PVSS_USBHS	Input	PLL circuit ground pin for the USBHS Must be shorted to the AVSS_USBHS pin.
	USBHS_RREF	I/O	Reference current source pin for the USBHS Must be connected to the AVSS_USBHS pin through a 2.2-kΩ (±1%) resistor.
	USBHS_DP	I/O	Input/output pin for the D+ data line of the USB bus
	USBHS_DM	I/O	Input/output pin for the D- data line of the USB bus
	USBHS_EXICEN	Output	Must be connected to the OTG power supply IC
	USBHS_ID	input	Must be connected to the OTG power supply IC
	USBHS_VBUSEN	Output	VBUS power supply enable pin for the USBHS
	USBHS_OVRCURA, USBHS_OVRCURB	Input	Overcurrent pin for the USBHS
	USBHS_VBUS	Input	USB cable connection monitor input pin
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3

Table 1.16 引脚功能（4个，共7个）

Function	Signal	I/O	Description
USBFS	VCC_USB	Input	电源引脚
	VSS_USB	Input	接地引脚
	USB_DP	I/O	USB片上收发器的D+引脚。将此引脚连接到USB总线的D+引脚。
	USB_DM	I/O	USB片上收发器的Dpin。将此引脚连接到USB总线的Dpin。
	USB_VBUS	Input	USB电缆连接监视器引脚。将此引脚连接到USB总线的VBUS。当USB模块作为功能控制器运行时，可以检测VBUS引脚状态（连接或断开）。
	USB_EXICEN	Output	用于外部电源(OTG)芯片的低功耗控制信号
	USB_VBUSEN	Output	VBUS(5V)为外部供电芯片供电使能信号
	USB_OVRCURA, USB_OVRCURB	Input	将外部过电流检测信号连接到这些引脚。 连接OTG电源芯片时，将VBUS比较器信号连接到这些引脚。
	USB_OVRCURA-DS, USB_OVRCURB-DS	Input	也可在DeepSoftware中使用的USBFS过流引脚 待机模式。 将外部过电流检测信号连接到这些引脚。 连接OTG电源芯片时，将VBUS比较器信号连接到这些引脚。
	USB_ID	Input	在OTG模式下运行期间，将MicroAB连接器ID输入信号连接到此引脚
USBHS	VCC_USBHS	Input	电源引脚
	VSS1_USBHS, VSS2_USBHS	Input	接地引脚
	AVCC_USBHS	Input	模拟电源
	AVSS_USBHS	Input	模拟接地引脚 必须短接到PVSS_USBHS引脚
	PVSS_USBHS	Input	USBHS的PLL电路接地引脚 必须短接到AVSS_USBHS引脚。
	USBHS_RREF	I/O	USBHS的参考电流源引脚 必须通过2.2-kΩ(±1%)电阻连接到AVSS_USBHS引脚。
	USBHS_DP	I/O	USB总线D+数据线的输入输出引脚
	USBHS_DM	I/O	USB总线Ddata线的输入输出引脚
	USBHS_EXICEN	Output	必须接OTG电源IC
	USBHS_ID	input	必须接OTG电源IC
	USBHS_VBUSEN	Output	USBHS的VBUS电源使能引脚
	USBHS_OVRCURA, USBHS_OVRCURB	Input	USBHS的过流引脚
	USBHS_VBUS	Input	USB线连接显示器输入引脚
QSPI	QSPCLK	Output	QSPI时钟输出引脚
	QSSL	Output	QSPI从机输出引脚
	QIO0 to QIO3	I/O	Data0 to Data3

Table 1.16 Pin functions (5 of 7)

Function	Signal	I/O	Description
OSPI	OM_SCLK	Output	Clock output (OCTACLK divided by 2)
	OM_CSn	Output	Chip select signal for an OctaFlash device, active-low
	OM_DQS	I/O	Read data strobe/write data mask signal
	OM_SIOn	I/O	Data input/output
	OM_RESET	Output	Reset signal for both OctaFlash and OctaRAM devices, active-low
	OM_ECS	Input	ECC error detection signal from the external memory, active-low
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	SSIDATA0	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)
SDHI/MMC	SD0CLK	Output	SD clock output pins
	SD0CMD	I/O	Command output pin and response input signal pins
	SD0DAT0 to SD0DAT7	I/O	SD and MMC data bus pins
	SD0CD	Input	SD card detection pins
	SD0WP	Input	SD write-protect signals

Table 1.16 引脚功能（5个，共7个）

Function	Signal	I/O	Description
OSPI	OM_SCLK	Output	时钟输出（OCTACLK除以2）
	OM_CSn	Output	OctaFlash器件的片选信号，低电平有效
	OM_DQS	I/O	读数据选通写数据屏蔽信号
	OM_SIOn	I/O	Data input/output
	OM_RESET	Output	OctaFlash和OctaRAM器件的复位信号，低电平有效
	OM_ECS	Input	来自外部存储器的ECC错误检测信号，低电平有效
SSIE	SSIBCK0	I/O	SSIE串行位时钟引脚
	SSILRCK0/SSIFS0	I/O	LR时钟帧同步管脚
	SSITXD0	Output	串行数据输出引脚
	SSIRXD0	Input	串行数据输入引脚
	SSIDATA0	I/O	串行数据输入输出引脚
	AUDIO_CLK	Input	音频外部时钟引脚（输入过采样时钟）
SDHI/MMC	SD0CLK	Output	SD时钟输出引脚
	SD0CMD	I/O	命令输出引脚和响应输入信号引脚
	SD0DAT0 to SD0DAT7	I/O	SD和MMC数据总线引脚
	SD0CD	Input	SD卡检测引脚
	SD0WP	Input	SD write-protect signals

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Table 1.16 Pin functions (6 of 7)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode .
	RMII0_TXDn	Output	2-bit transmit data in RMII mode
	RMII0_RXDn	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode
	ET0_CRS	Input	Carrier detection/data reception enable signal
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0
	ET0_EXOUT	Output	General-purpose external output pin
	ET0_LINKSTA	Input	Input link status from the PHY-LSI
	ET0_ETXDn	Output	4 bits of MII transmit data
	ET0_ERXDn	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0.
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission.
	ET0_RX_ER	Output	Receive error pin. Functions as signal to recognize an error during reception.
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER.
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.
	ET0_COL	Input	Input collision detection signal
	ET0_WOL	Output	Receive Magic packets
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO
	ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to AVCC0 when not using the ADC12 (unit 1) and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to AVSS0 when not using the ADC12 (unit 1) and D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to AVCC0 when not using the ADC12 (unit 0).
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12 (unit 0).

Table 1.16 引脚功能（6个，共7个）

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50MHz参考时钟。该引脚输入RMII模式下发送接收时序的参考信号。
	RMII0_CRS_DV	Input	指示载波检测信号和有效的接收数据 RMII模式下的RMII0_RXD1和RMII0_RXD0 .
	RMII0_TXDn	Output	RMII模式下的2位发送数据
	RMII0_RXDn	Input	RMII模式下的2位接收数据
	RMII0_TXD_EN	Output	RMII模式下数据发送使能信号的输出引脚
	RMII0_RX_ER	Input	表示在RMII模式下接收数据时发生错误
	ET0_CRS	Input	载波检测数据接收使能信号
	ET0_RX_DV	Input	指示ET0_ERXD3到ET0_ERXD0上的有效接收数据
	ET0_EXOUT	Output	通用外部输出引脚
	ET0_LINKSTA	Input	从PHY-LSI输入链路状态
	ET0_ETXDn	Output	4位MII传输数据
	ET0_ERXDn	Input	4位MII接收数据
	ET0_TX_EN	Output	发送使能信号。用作指示在ET0_ETXD3到ET0_ETXD0上传输数据已准备好的信号。
	ET0_TX_ER	Output	发送错误引脚。用作在传输过程中向PHY_LSI通知错误的信号。
	ET0_RX_ER	Output	接收错误引脚。用作在接收期间识别错误的信号。
	ET0_TX_CLK	Input	发送时钟引脚。该引脚输入参考信号，用于从ET0_TX_EN、ET0_ETXD3到ET0_ETXD0和ET0_TX_ER的输出时序。
	ET0_RX_CLK	Input	接收时钟引脚。该引脚输入用于输入时序的参考信号 ET0_RX_DV、ET0_ERXD3到ET0_ERXD0和ET0_RX_ER。
	ET0_COL	Input	输入碰撞检测信号
	ET0_WOL	Output	接收魔术包
	ET0_MDC	Output	输出参考时钟信号用于信息传输 ET0_MDIO
	ET0_MDIO	I/O	用于与PHY-LSI交换管理数据的输入或输出双向信号
模拟电源	AVCC0	Input	模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。
	AVSS0	Input	模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。
	VREFH	Input	ADC12（单元1）和DA的模拟参考电压电源引脚 转换器。不使用ADC12（单元1）和DA转换器时，将此引脚连接到AVCC0。
	VREFL	Input	ADC12和DA转换器的模拟参考接地引脚。 不使用ADC12（单元1）时将此引脚连接到AVSS0，并且 D/A Converter.
	VREFH0	Input	ADC12（单元0）的模拟参考电压电源引脚。不使用ADC12（单元0）时，将此引脚连接到AVCC0。
	VREFL0	Input	ADC12的模拟参考接地引脚。将此引脚连接到 不使用ADC12（单元0）时的AVSS0。

Table 1.16 Pin functions (7 of 7)

Function	Signal	I/O	Description
ADC12	ANmn	Input	Input pins for the analog signals to be processed by the A/D converter. (m: ADC unit number, n: pin number)
	ADTRGm	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
CTSU	TSn	Input	Capacitive touch detection pins (touch pins)
	TSCAP	I/O	Secondary power supply pin for the touch driver
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin
CEC	CECIO	I/O	CEC data communication

Table 1.16 引脚功能（7之7）

Function	Signal	I/O	Description
ADC12	ANmn	Input	AD转换器要处理的模拟信号的输入引脚。（m：ADC单元编号，n：引脚编号）
	ADTRGm	Input	用于启动AD转换的外部触发信号的输入引脚，低电平有效。
DAC12	DAn	Output	由数模转换器处理的模拟信号的输出引脚。
CTSU	TSn	Input	电容式触摸检测引脚（触摸引脚）
	TSCAP	I/O	触摸驱动器的辅助电源引脚
I/O ports	Pmn	I/O	通用输入输出引脚（m：端口号，n：引脚号）
	P200	Input	通用输入引脚
CEC	CECIO	I/O	CEC数据通信

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1.6 Pin Assignments

The following figures show the pin assignments from the top view.

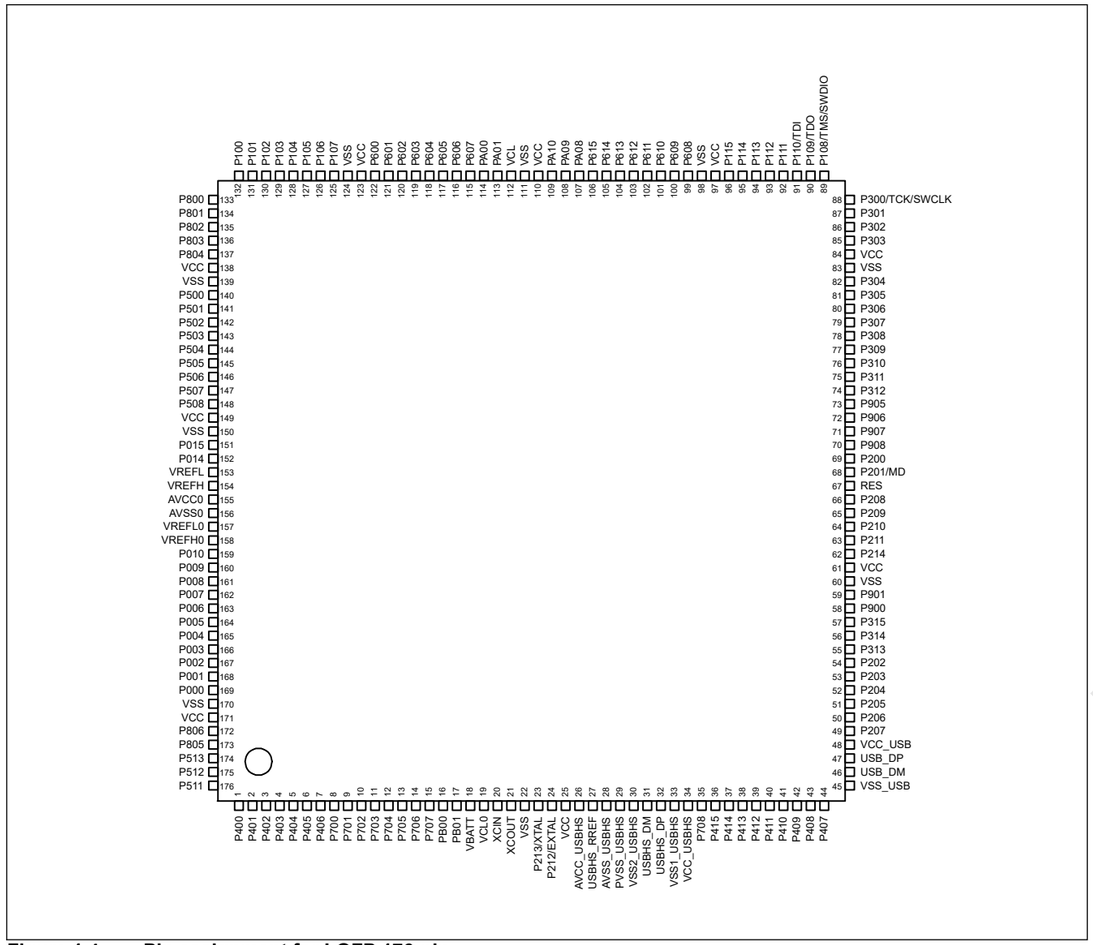

Figure 1.4 Pin assignment for LQFP 176-pin

1.6 引脚分配

下图从顶视图显示了引脚分配。

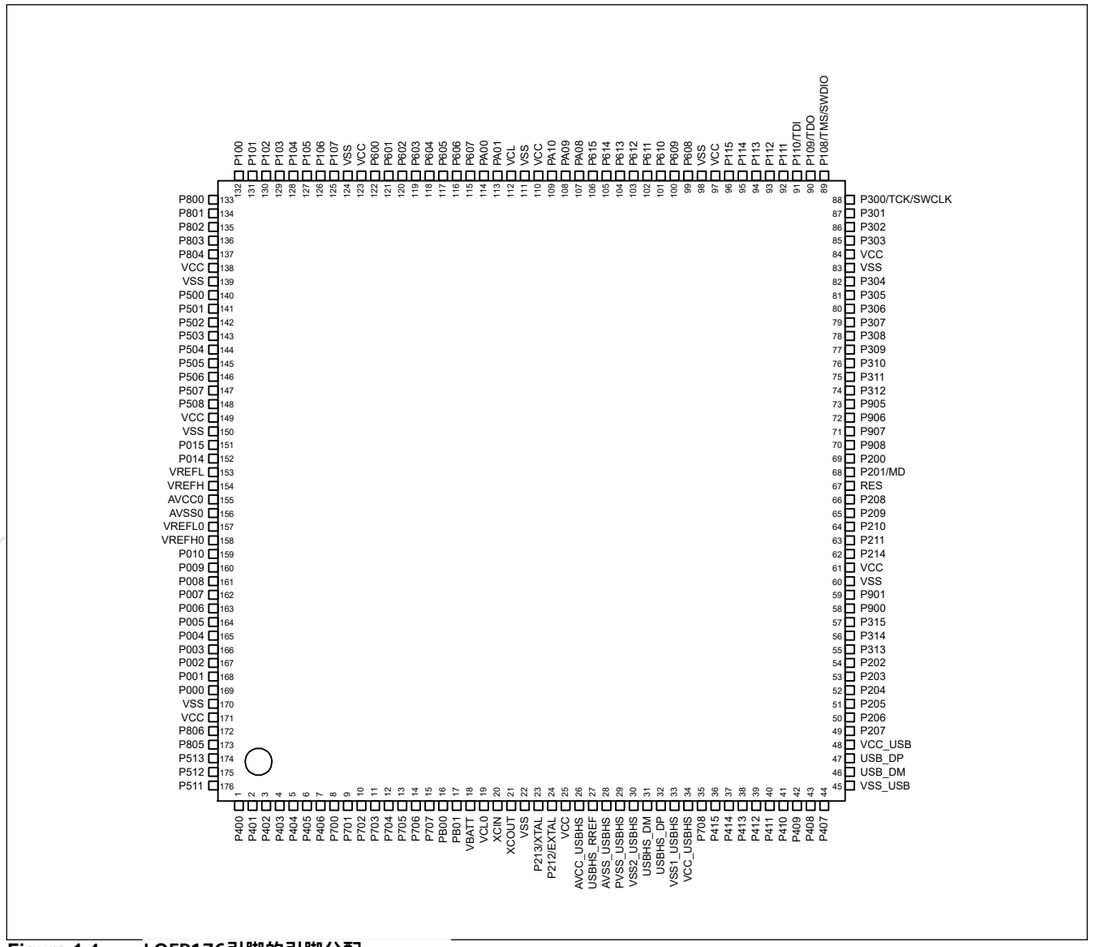

Figure 1.4 LQFP176引脚的引脚分配

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212/EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213/XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK/SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS/SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.5 Pin assignment for BGA 176-pin

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212/EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213/XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK/SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS/SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.5 BGA176引脚的引脚分配

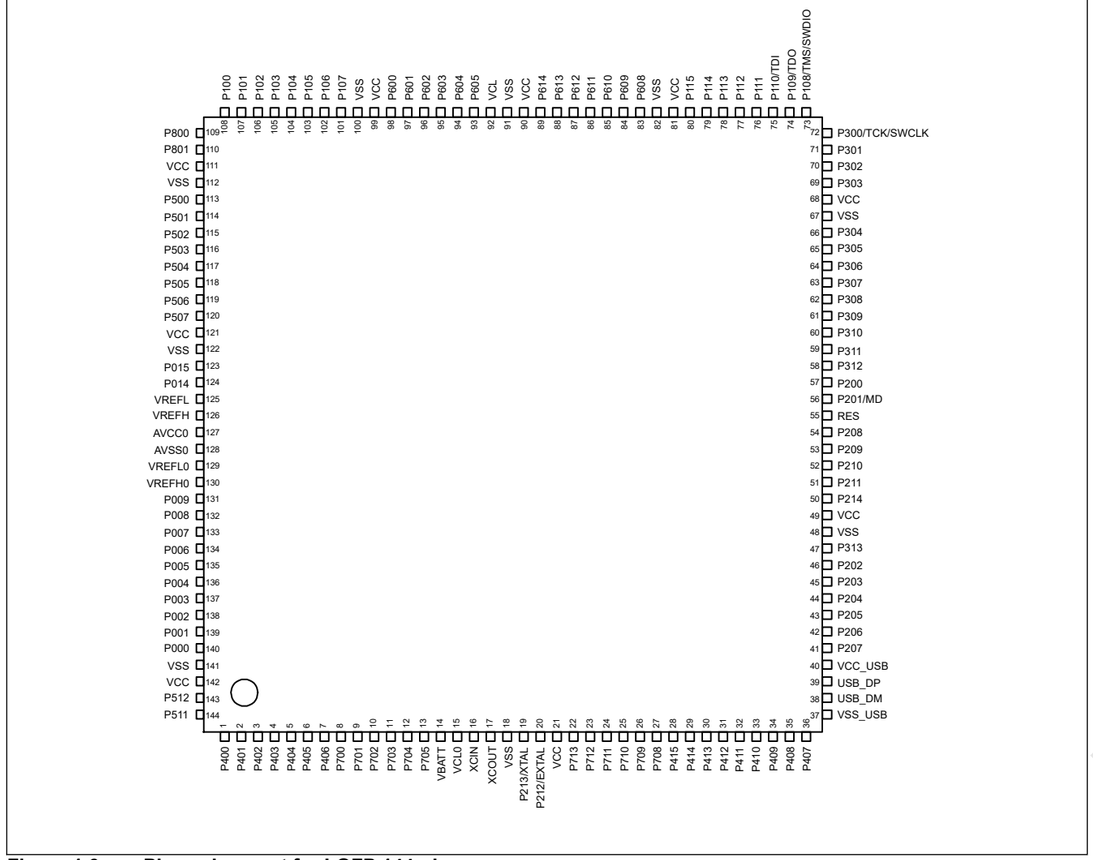

Figure 1.6 Pin assignment for LQFP 144-pin

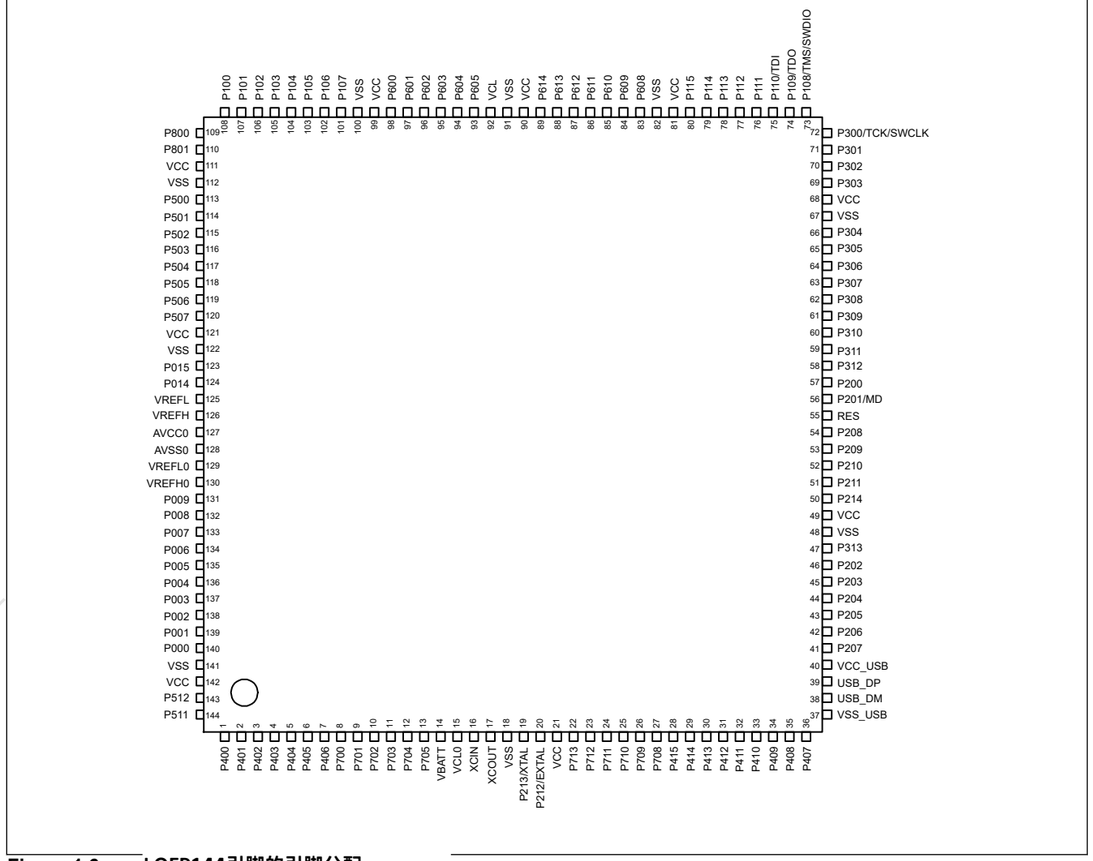

Figure 1.6 LQFP144引脚的引脚分配

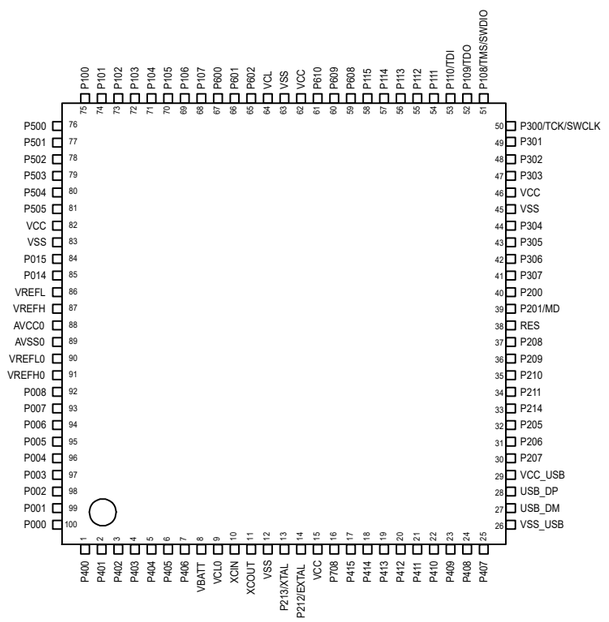

Figure 1.7 Pin assignment for LQFP 100-pin

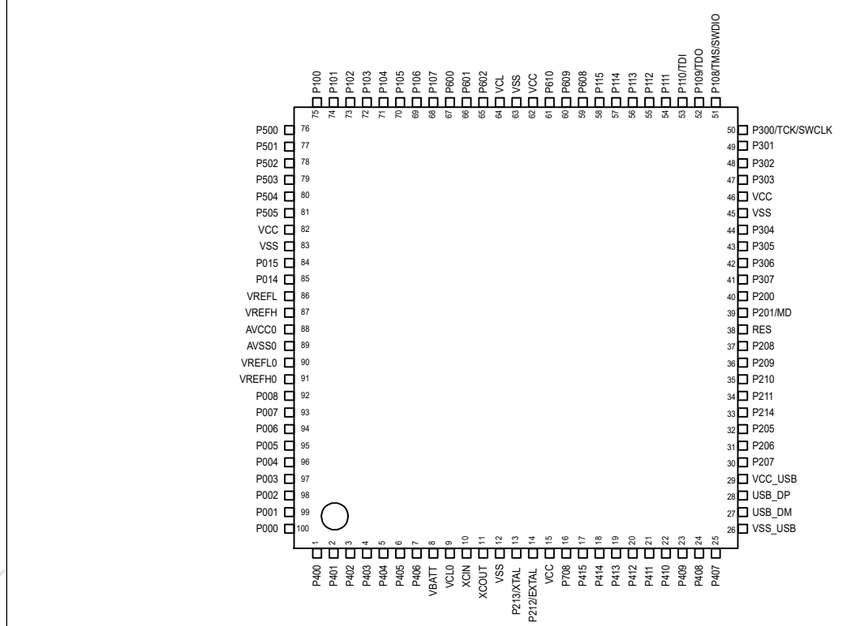

Figure 1.7 LQFP100引脚的引脚分配

1.7 Pin Lists

Table 1.17 Pin list (1 of 4)

LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus	Ex. Interrupt	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/ SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
1	1	1	—	P400	—	IRQ0	SCK4/SCK7/SCL0_A/AUDIO_CLK/ET0_WOL/ ET0_WOL	GTIOC6A/AGTIO1	ADTRG1	—
2	2	2	—	P401	—	IRQ5-DS	CTS4_RTS4/TXD7/SDA0_A/CTX0/ET0_MDC/ ET0_MDC	GTETRGA/GTIOC6B	—	—
3	3	3	CACREF	P402	—	IRQ4-DS	CTS4/RXD7/CRX0/AUDIO_CLK/ET0_MDIO/ ET0_MDIO	AGTIO0/AGTIO1/AGTIO2/ AGTIO3/RTCIC0	—	—
4	4	4	—	P403	—	IRQ14-DS	CTS7_RTS7/SSIBCK0_A/ET0_LINKSTA/ ET0_LINKSTA	GTIOC3A/AGTIO0/AGTIO1/ AGTIO2/AGTIO3/RTCIC1	—	—
5	5	5	—	P404	—	IRQ15-DS	CTS7/SSILRCK0_A/ET0_EXOUT/ET0_EXOUT	GTIOC3B/AGTIO0_G/AGTIO1/ AGTIO2/AGTIO3/RTCIC2	—	—
6	6	6	—	P405	—	—	SSITXD0_A/ET0_TX_EN/RMII0_TXD_EN_B	GTIOC1A	—	—
7	7	7	—	P406	—	—	SSLA3_C/SSIRXD0_A/ET0_RX_ER/RMII0_TXD1_B	GTIOC1B/AGTO5	—	—
8	8	—	—	P700	—	—	MISOA_C/ET0_ETXD1/RMII0_TXD0_B	GTIOC5A/AGTO4	—	—
9	9	—	—	P701	—	—	MOSIA_C/ET0_ETXD0/REF50CK0_B	GTIOC5B/AGTO3	—	—
10	10	—	—	P702	—	—	RSPCKA_C/ET0_ERXD1/RMII0_RXD0_B	GTIOC6A/AGTO2	—	—
11	11	—	—	P703	—	—	SSLA0_C/ET0_ERXD0/RMII0_RXD1_B	GTIOC6B/AGTO1	—	—
12	12	—	—	P704	—	—	SSLA1_C/CTX0/ET0_RX_CLK/RMII0_RX_ER_B	AGTO0	—	—
13	13	—	—	P705	—	—	CTS3/SSLA2_C/CRX0/ET0_CRS/RMII0_CRS_DV_B	AGTIO0	—	—
14	—	—	—	P706	—	IRQ7	USBHS_OVRCURB/RXD3_B	—	—	—
15	—	—	—	P707	—	IRQ8	USBHS_OVRCURA/TXD3_B	—	—	—
16	—	—	—	PB00	—	—	USBHS_VBUSEN/SCK3_B	—	—	—
17	—	—	—	PB01	—	—	USBHS_VBUS/CTS_RTS3_B	—	—	—
18	14	8	VBATT	—	—	—	—	—	—	—
19	15	9	VCL0	—	—	—	—	—	—	—
20	16	10	XCIN	—	—	—	—	—	—	—
21	17	11	XCOUT	—	—	—	—	—	—	—
22	18	12	VSS	—	—	—	—	—	—	—
23	19	13	XTAL	P213	—	IRQ2	TXD1	GTETRGC/GTIOC0A/AGTEE2	ADTRG1	—
24	20	14	EXTAL	P212	—	IRQ3	RXD1	GTETRGD/GTIOC0B/AGTEE1	—	—
25	21	15	VCC	—	—	—	—	—	—	—
26	—	—	AVCC_USBHS	—	—	—	—	—	—	—
27	—	—	USBHS_RREF	—	—	—	—	—	—	—
28	—	—	AVSS_USBHS	—	—	—	—	—	—	—
29	—	—	VSS_USBHS	—	—	—	—	—	—	—
30	—	—	VSS_USBHS	—	—	—	—	—	—	—
31	—	—	USBHS_DM	—	—	—	—	—	—	—
32	—	—	USBHS_DP	—	—	—	—	—	—	—
33	—	—	VSS_USBHS	—	—	—	—	—	—	—
34	—	—	VCC_USBHS	—	—	—	—	—	—	—
—	22	—	—	P713	—	—	—	GTIOC2A/AGTOA0	—	TS17
—	23	—	—	P712	—	—	—	GTIOC2B/AGTOB0	—	TS16
—	24	—	—	P711	—	—	CTS1_RTS1/ET0_TX_CLK	AGTEE0	—	TS15
—	25	—	—	P710	—	—	SCK1/ET0_TX_ER	—	—	TS14
—	26	—	—	P709	—	IRQ10	TXD1/ET0_ETXD2	—	—	TS13
35	27	16	CACREF	P708	—	IRQ11	RXD1/SSLB3_B/AUDIO_CLK/ET0_ETXD3/CECIO	—	—	TS12
36	28	17	—	P415	—	IRQ8	SCL2/SSLB2_B/USB_VBUSEN/SD0CD/ET0_TX_EN/ RMII0_TXD_EN_A	GTIOC0A/AGTIO4	—	TS11
37	29	18	—	P414	—	IRQ9	SDA2/CTS0/SSLB1_B/SD0WP/ET0_RX_ER/ RMII0_TXD1_A	GTIOC0B/AGTIO5	—	TS10
38	30	19	—	P413	—	—	CTS0_RTS0/SSLB0_B/SD0CLK_A/ET0_ETXD1/ RMII0_TXD0_A	GTOUUP/AGTEE3	—	TS09

1.7 引脚列表

Table 1.17 引脚列表（4个中的1个）

LQFP176	LQFP144	LQFP100	电源、系统、时钟、调试、CAC	I/O ports	前任。公共汽车	前任。打断	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/ SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
1	1	1	—	P400	—	IRQ0	SCK4/SCK7/SCL0_A/AUDIO_CLK/ET0_WOL/ ET0_WOL	GTIOC6A/AGTIO1	ADTRG1	—
2	2	2	—	P401	—	IRQ5-DS	CTS4_RTS4/TXD7/SDA0_A/CTX0/ET0_MDC/ ET0_MDC	GTETRGA/GTIOC6B	—	—
3	3	3	CACREF	P402	—	IRQ4-DS	CTS4/RXD7/CRX0/AUDIO_CLK/ET0_MDIO/ ET0_MDIO	AGTIO0/AGTIO1/AGTIO2/ AGTIO3/RTCIC0	—	—
4	4	4	—	P403	—	IRQ14-DS	CTS7_RTS7/SSIBCK0_A/ET0_LINKSTA/ ET0_LINKSTA	GTIOC3A/AGTIO0/AGTIO1/ AGTIO2/AGTIO3/RTCIC1	—	—
5	5	5	—	P404	—	IRQ15-DS	CTS7/SSILRCK0_A/ET0_EXOUT/ET0_EXOUT	GTIOC3B/AGTIO0_G/AGTIO1/ AGTIO2/AGTIO3/RTCIC2	—	—
6	6	6	—	P405	—	—	SSITXD0_A/ET0_TX_EN/RMII0_TXD_EN_B	GTIOC1A	—	—
7	7	7	—	P406	—	—	SSLA3_C/SSIRXD0_A/ET0_RX_ER/RMII0_TXD1_B	GTIOC1B/AGTO5	—	—
8	8	—	—	P700	—	—	MISOA_C/ET0_ETXD1/RMII0_TXD0_B	GTIOC5A/AGTO4	—	—
9	9	—	—	P701	—	—	MOSIA_C/ET0_ETXD0/REF50CK0_B	GTIOC5B/AGTO3	—	—
10	10	—	—	P702	—	—	RSPCKA_C/ET0_ERXD1/RMII0_RXD0_B	GTIOC6A/AGTO2	—	—
11	11	—	—	P703	—	—	SSLA0_C/ET0_ERXD0/RMII0_RXD1_B	GTIOC6B/AGTO1	—	—
12	12	—	—	P704	—	—	SSLA1_C/CTX0/ET0_RX_CLK/RMII0_RX_ER_B	AGTO0	—	—
13	13	—	—	P705	—	—	CTS3/SSLA2_C/CRX0/ET0_CRS/RMII0_CRS_DV_B	AGTIO0	—	—
14	—	—	—	P706	—	IRQ7	USBHS_OVRCURB/RXD3_B	—	—	—
15	—	—	—	P707	—	IRQ8	USBHS_OVRCURA/TXD3_B	—	—	—
16	—	—	—	PB00	—	—	USBHS_VBUSEN/SCK3_B	—	—	—
17	—	—	—	PB01	—	—	USBHS_VBUS/CTS_RTS3_B	—	—	—
18	14	8	VBATT	—	—	—	—	—	—	—
19	15	9	VCL0	—	—	—	—	—	—	—
20	16	10	XCIN	—	—	—	—	—	—	—
21	17	11	XCOUT	—	—	—	—	—	—	—
22	18	12	VSS	—	—	—	—	—	—	—
23	19	13	XTAL	P213	—	IRQ2	TXD1	GTETRGC/GTIOC0A/AGTEE2	ADTRG1	—
24	20	14	EXTAL	P212	—	IRQ3	RXD1	GTETRGD/GTIOC0B/AGTEE1	—	—
25	21	15	VCC	—	—	—	—	—	—	—
26	—	—	AVCC_USBHS	—	—	—	—	—	—	—
27	—	—	USBHS_RREF	—	—	—	—	—	—	—
28	—	—	AVSS_USBHS	—	—	—	—	—	—	—
29	—	—	VSS_USBHS	—	—	—	—	—	—	—
30	—	—	VSS_USBHS	—	—	—	—	—	—	—
31	—	—	USBHS_DM	—	—	—	—	—	—	—
32	—	—	USBHS_DP	—	—	—	—	—	—	—
33	—	—	VSS_USBHS	—	—	—	—	—	—	—
34	—	—	VCC_USBHS	—	—	—	—	—	—	—
—	22	—	—	P713	—	—	—	GTIOC2A/AGTOA0	—	TS17
—	23	—	—	P712	—	—	—	GTIOC2B/AGTOB0	—	TS16
—	24	—	—	P711	—	—	CTS1_RTS1/ET0_TX_CLK	AGTEE0	—	TS15
—	25	—	—	P710	—	—	SCK1/ET0_TX_ER	—	—	TS14
—	26	—	—	P709	—	IRQ10	TXD1/ET0_ETXD2	—	—	TS13
35	27	16	CACREF	P708	—	IRQ11	RXD1/SSLB3_B/AUDIO_CLK/ET0_ETXD3/CECIO	—	—	TS12
36	28	17	—	P415	—	IRQ8	SCL2/SSLB2_B/USB_VBUSEN/SD0CD/ET0_TX_EN/ RMII0_TXD_EN_A	GTIOC0A/AGTIO4	—	TS11
37	29	18	—	P414	—	IRQ9	SDA2/CTS0/SSLB1_B/SD0WP/ET0_RX_ER/ RMII0_TXD1_A	GTIOC0B/AGTIO5	—	TS10
38	30	19	—	P413	—	—	CTS0_RTS0/SSLB0_B/SD0CLK_A/ET0_ETXD1/ RMII0_TXD0_A	GTOUUP/AGTEE3	—	TS09

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Table 1.17 Pin list (2 of 4)

LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus	Ex. Interrupt	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/ SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
39	31	20	—	P412	—	—	SCK0/CTS3/RSPCKB_B/SD0CMD_A/ET0_ETXD0/ REF50CK0_A	GTOULO/AGTEE1	—	TS08
40	32	21	—	P411	—	IRQ4	TXD0/CTS3_RTS3/MOSIB_B/SD0DAT0_A/ ET0_ERXD1/RMII0_RXD0_A	GTOVUP/GTIOC9A/AGTOA1	—	TS07
41	33	22	—	P410	—	IRQ5	RXD0/SCL2/SCK3/MISOB_B/SD0DAT1_A/ ET0_ERXD0/RMII0_RXD1_A	GTOVLO/GTIOC9B/AGTOB1	—	TS06
42	34	23	—	P409	—	IRQ6	TXD3/SDA2/USB_EXICEN/USBHS_EXICEN/ ET0_RX_CLK/RMII0_RX_ER_A	GTOWUP/AGTOA2	—	TS05
43	35	24	—	P408	—	IRQ7	CTS4/RXD3/SCL0_B/USB_ID/USBHS_ID/ET0_CRS/ RMII0_CRS_DV_A	GTOWLO/GTIOC6B/AGTOB2	—	TS04
44	36	25	—	P407	—	—	CTS4_RTS4/SDA0_B/SSLA3_A/USB_VBUS/ ET0_EXOUT/ET0_EXOUT	GTIOC6A/AGTIO0/RTCOUT	ADTRG0	TS03
45	37	26	VSS_USB	—	—	—	—	—	—	—
46	38	27	USB_DM	—	—	—	—	—	—	—
47	39	28	USB_DP	—	—	—	—	—	—	—
48	40	29	VCC_USB	—	—	—	—	—	—	—
49	41	30	—	P207	A17	—	TXD4/SSLA2_A/QSSL	—	—	TSCAP
50	42	31	—	P206	WAIT	IRQ0-DS	RXD4/CTS9/SDA1_B/SSLA1_A/USB_VBUSEN/ SD0DAT2_A/ET0_LINKSTA/ET0_LINKSTA/CECIO/ SSIDATA0_C	GTIU	—	TS02
51	43	32	CLKOUT	P205	A16	IRQ1-DS	TXD4/CTS9_RTS9/SCL1_B/SSLA0_A/ USB_OVRCURA-DS/SSILRCK0_C/SD0DAT3_A/ ET0_WOL/ET0_WOL	GTIV/GTIOC4A/AGTO1	—	TS01
52	44	—	CACREF	P204	A18	—	SCK4/SCK9/RSPCKA_A/USB_OVRCURB-DS/ SSIBCK0_C/SD0DAT4_A/ET0_RX_DV	GTIW/GTIOC4B/AGTIO1	—	TS00
53	45	—	—	P203	A19	IRQ2-DS	CTS2_RTS2/TXD9/MOSIA_A/CTX0/SD0DAT5_A/ ET0_COL	GTIOC5A/AGTOA3	—	TS18
54	46	—	—	P202	WR1/BC1	IRQ3-DS	SCK2/RXD9/MISOA_A/CRX0/SD0DAT6_A/ ET0_ERXD2	GTIOC5B/AGTOB3	—	TS19
55	47	—	—	P313	A20	—	SD0DAT7_A/ET0_ERXD3	—	—	—
56	—	—	—	P314	A21	—	—	—	ADTRG0	—
57	—	—	—	P315	A22	—	RXD4_C	—	—	—
58	—	—	—	P900	A23	—	TXD4_C	—	—	—
59	—	—	—	P901	—	—	SCK4_C	AGTIO1_E	—	—
60	48	—	VSS	—	—	—	—	—	—	—
61	49	—	VCC	—	—	—	—	—	—	—
62	50	33	TCLK	P214	—	—	QSPCLK/SD0CLK_B/ET0_MDC/ET0_MDC	GTIU/AGTO5	—	—
63	51	34	TDATA0	P211	CS7	—	QIO0/SD0CMD_B/ET0_MDIO/ET0_MDIO	GTIV/AGTOA5	—	—
64	52	35	TDATA1	P210	CS6	—	QIO1/SD0CD/ET0_WOL/ET0_WOL	GTIW/AGTOB5	—	—
65	53	36	TDATA2	P209	CS5	—	QIO2/SD0WP/ET0_EXOUT/ET0_EXOUT	GTOVUP/AGTEE5	—	—
66	54	37	TDATA3	P208	CS4	—	QIO3/SD0DAT0_B/ET0_LINKSTA/ET0_LINKSTA	GTOVLO	—	—
67	55	38	RES	—	—	—	—	—	—	—
68	56	39	MD	P201	—	—	—	—	—	—
69	57	40	—	P200	—	NMI	—	—	—	—
70	—	—	—	P908	—	IRQ11	USBHS_EXICEN	—	—	—
71	—	—	—	P907	—	IRQ10	USBHS_ID	—	—	—
72	—	—	—	P906	—	IRQ9	USB_EXICEN_C	—	—	—
73	—	—	—	P905	—	IRQ8	USB_ID_C	—	—	—
74	58	—	—	P312	CS3	—	CTS3_RTS3	AGTOA1	—	—
75	59	—	—	P311	CS2	—	SCK3	AGTOB1	—	—
76	60	—	—	P310	A15	—	TXD3/QIO3	AGTEE1	—	—
77	61	—	—	P309	A14	—	RXD3/QIO2	AGTOA4	—	—
78	62	—	—	P308	A13	—	CTS6/CTS3/QIO1	AGTOB4	—	—
79	63	41	—	P307	A12	—	CTS6_RTS6/QIO0	GTOUUP_D/AGTEE4	—	—
80	64	42	—	P306	A11	—	SCK6/QSSL	GTOULO_D/AGTOA2	—	—

Table 1.17 引脚列表（2个，共4个）

LQFP176	LQFP144	LQFP100	电源、系统、时钟、调试、CAC	I/O ports	前任。公共汽车	前任。打断	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/ SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
39	31	20	—	P412	—	—	SCK0/CTS3/RSPCKB_B/SD0CMD_A/ET0_ETXD0/ REF50CK0_A	GTOULO/AGTEE1	—	TS08
40	32	21	—	P411	—	IRQ4	TXD0/CTS3_RTS3/MOSIB_B/SD0DAT0_A/ ET0_ERXD1/RMII0_RXD0_A	GTOVUP/GTIOC9A/AGTOA1	—	TS07
41	33	22	—	P410	—	IRQ5	RXD0/SCL2/SCK3/MISOB_B/SD0DAT1_A/ ET0_ERXD0/RMII0_RXD1_A	GTOVLO/GTIOC9B/AGTOB1	—	TS06
42	34	23	—	P409	—	IRQ6	TXD3/SDA2/USB_EXICEN/USBHS_EXICEN/ ET0_RX_CLK/RMII0_RX_ER_A	GTOWUP/AGTOA2	—	TS05
43	35	24	—	P408	—	IRQ7	CTS4/RXD3/SCL0_B/USB_ID/USBHS_ID/ET0_CRS/ RMII0_CRS_DV_A	GTOWLO/GTIOC6B/AGTOB2	—	TS04
44	36	25	—	P407	—	—	CTS4_RTS4/SDA0_B/SSLA3_A/USB_VBUS/ ET0_EXOUT/ET0_EXOUT	GTIOC6A/AGTIO0/RTCOUT	ADTRG0	TS03
45	37	26	VSS_USB	—	—	—	—	—	—	—
46	38	27	USB_DM	—	—	—	—	—	—	—
47	39	28	USB_DP	—	—	—	—	—	—	—
48	40	29	VCC_USB	—	—	—	—	—	—	—
49	41	30	—	P207	A17	—	TXD4/SSLA2_A/QSSL	—	—	TSCAP
50	42	31	—	P206	WAIT	IRQ0-DS	RXD4/CTS9/SDA1_B/SSLA1_A/USB_VBUSEN/ SD0DAT2_A/ET0_LINKSTA/ET0_LINKSTA/CECIO/ SSIDATA0_C	GTIU	—	TS02
51	43	32	CLKOUT	P205	A16	IRQ1-DS	TXD4/CTS9_RTS9/SCL1_B/SSLA0_A/ USB_OVRCURA-DS/SSILRCK0_C/SD0DAT3_A/ ET0_WOL/ET0_WOL	GTIV/GTIOC4A/AGTO1	—	TS01
52	44	—	CACREF	P204	A18	—	SCK4/SCK9/RSPCKA_A/USB_OVRCURB-DS/ SSIBCK0_C/SD0DAT4_A/ET0_RX_DV	GTIW/GTIOC4B/AGTIO1	—	TS00
53	45	—	—	P203	A19	IRQ2-DS	CTS2_RTS2/TXD9/MOSIA_A/CTX0/SD0DAT5_A/ ET0_COL	GTIOC5A/AGTOA3	—	TS18
54	46	—	—	P202	WR1/BC1	IRQ3-DS	SCK2/RXD9/MISOA_A/CRX0/SD0DAT6_A/ ET0_ERXD2	GTIOC5B/AGTOB3	—	TS19
55	47	—	—	P313	A20	—	SD0DAT7_A/ET0_ERXD3	—	—	—
56	—	—	—	P314	A21	—	—	—	ADTRG0	—
57	—	—	—	P315	A22	—	RXD4_C	—	—	—
58	—	—	—	P900	A23	—	TXD4_C	—	—	—
59	—	—	—	P901	—	—	SCK4_C	AGTIO1_E	—	—
60	48	—	VSS	—	—	—	—	—	—	—
61	49	—	VCC	—	—	—	—	—	—	—
62	50	33	TCLK	P214	—	—	QSPCLK/SD0CLK_B/ET0_MDC/ET0_MDC	GTIU/AGTO5	—	—
63	51	34	TDATA0	P211	CS7	—	QIO0/SD0CMD_B/ET0_MDIO/ET0_MDIO	GTIV/AGTOA5	—	—
64	52	35	TDATA1	P210	CS6	—	QIO1/SD0CD/ET0_WOL/ET0_WOL	GTIW/AGTOB5	—	—
65	53	36	TDATA2	P209	CS5	—	QIO2/SD0WP/ET0_EXOUT/ET0_EXOUT	GTOVUP/AGTEE5	—	—
66	54	37	TDATA3	P208	CS4	—	QIO3/SD0DAT0_B/ET0_LINKSTA/ET0_LINKSTA	GTOVLO	—	—
67	55	38	RES	—	—	—	—	—	—	—
68	56	39	MD	P201	—	—	—	—	—	—
69	57	40	—	P200	—	NMI	—	—	—	—
70	—	—	—	P908	—	IRQ11	USBHS_EXICEN	—	—	—
71	—	—	—	P907	—	IRQ10	USBHS_ID	—	—	—
72	—	—	—	P906	—	IRQ9	USB_EXICEN_C	—	—	—
73	—	—	—	P905	—	IRQ8	USB_ID_C	—	—	—
74	58	—	—	P312	CS3	—	CTS3_RTS3	AGTOA1	—	—
75	59	—	—	P311	CS2	—	SCK3	AGTOB1	—	—
76	60	—	—	P310	A15	—	TXD3/QIO3	AGTEE1	—	—
77	61	—	—	P309	A14	—	RXD3/QIO2	AGTOA4	—	—
78	62	—	—	P308	A13	—	CTS6/CTS3/QIO1	AGTOB4	—	—
79	63	41	—	P307	A12	—	CTS6_RTS6/QIO0	GTOUUP_D/AGTEE4	—	—
80	64	42	—	P306	A11	—	SCK6/QSSL	GTOULO_D/AGTOA2	—	—

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Table 1.17 Pin list (3 of 4)

LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus	Ex. Interrupt	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
81	65	43	—	P305	A10	IRQ8	TXD6/QSPCLK	GTOWUP/AGTOB2	—	—
82	66	44	—	P304	A9	IRQ9	RXD6	GTOWLO/GTIOC7A/AGTEE2	—	—
83	67	45	VSS	—	—	—	—	—	—	—
84	68	46	VCC	—	—	—	—	—	—	—
85	69	47	—	P303	A8	—	CTS9	GTIOC7B	—	—
86	70	48	—	P302	A7	IRQ5	TXD2/SSLA3_B	GTOUUP/GTIOC4A	—	—
87	71	49	—	P301	A6	IRQ6	RXD2/CTS9_RTS9/SSLA2_B	GTOULO/GTIOC4B/AGTIO0	—	—
88	72	50	TCK/SWCLK	P300	—	—	SSLA1_B	GTOUUP/GTIOC0A	—	—
89	73	51	TMS/SWDIO	P108	—	—	CTS9_RTS9/SSLA0_B	GTOULO/GTIOC0B/AGTOA3	—	—
90	74	52	TDO/SWO/CLKOUT	P109	—	—	TXD9/MOSIA_B/CTX1	GTOVUP/GTIOC1A/AGTOB3	—	—
91	75	53	TDI	P110	—	IRQ3	CTS2_RTS2/RXD9/MISOA_B/CRX1	GTOVLO/GTIOC1B/AGTEE3	—	—
92	76	54	—	P111	A5	IRQ4	SCK2/SCK9/RSPCKA_B	GTIOC3A/AGTOA5	—	—
93	77	55	—	P112	A4	—	TXD2/SCK1/SSLA0_B/QSSL/OM_CS1/SSISCK0_B	GTIOC3B/AGTOB5	—	—
94	78	56	—	P113	A3	—	RXD2/SSILRCK0_B	GTIOC2A/AGTEE5	—	—
95	79	57	—	P114	A2	—	CTS9/SSIRXD0_B	GTIOC2B/AGTIO5	—	—
96	80	58	—	P115	A1	—	SSITXD0_B	GTIOC4A	—	—
97	81	—	VCC	—	—	—	—	—	—	—
98	82	—	VSS	—	—	—	—	—	—	—
99	83	59	—	P608	A0/BC0	—	—	GTIOC4B	—	—
100	84	60	—	P609	CS1	—	CTX1/OM_ECS	GTIOC5A/AGTO5	—	—
101	85	61	—	P610	CS0	—	CTS7/CRX1/OM_CS0	GTIOC5B/AGTO4	—	—
102	86	—	CACREF/CLKOUT	P611	—	—	CTS7_RTS7	AGTO3	—	—
103	87	—	—	P612	D8	—	SCK7	AGTO2	—	—
104	88	—	—	P613	D9	—	TXD7	AGTO1	—	—
105	89	—	—	P614	D10	—	RXD7	AGTO0	—	—
106	—	—	—	P615	—	IRQ7	USB_VBUSEN_D	—	—	—
107	—	—	—	PA08	—	IRQ6	USB_OVRCURA_C	—	—	—
108	—	—	—	PA09	—	IRQ5	USB_OVRCURB_C	—	—	—
109	—	—	—	PA10	—	IRQ4	—	—	—	—
110	90	62	VCC	—	—	—	—	—	—	—
111	91	63	VSS	—	—	—	—	—	—	—
112	92	64	VCL	—	—	—	—	—	—	—
113	—	—	—	PA01	—	—	SCK8_C	—	—	—
114	—	—	—	PA00	—	—	TXD8_C	—	—	—
115	—	—	—	P607	—	—	RXD8_C	—	—	—
116	—	—	—	P606	—	—	CTS_RTS8_C	RTCOUT_B	—	—
117	93	—	—	P605	D11	—	CTS8	GTIOC8A/AGTO4	—	—
118	94	—	—	P604	D12	—	CTS9	GTIOC8B/AGTEE4	—	—
119	95	—	—	P603	D13	—	CTS9_RTS9	GTIOC7A/AGTIO4	—	—
120	96	65	—	P602	BCLK	—	TXD9/OM_CS1	GTIOC7B/AGTO3	—	—
121	97	66	—	P601	WR/WR0	—	RXD9/OM_SIO2	GTIOC6A/AGTEE3	—	—
122	98	67	CACREF/CLKOUT	P600	RD	—	SCK9/OM_SIO4	GTIOC6B/AGTIO3	—	—
123	99	—	VCC	—	—	—	—	—	—	—
124	100	—	VSS	—	—	—	—	—	—	—
125	101	68	—	P107	D7	—	CTS8_RTS8/OM_SIO3	GTIOC8A/AGTOA0	—	—
126	102	69	—	P106	D6	—	SCK8/SSLB3_A/OM_SIO0	GTIOC8B/AGTOB0	—	—
127	103	70	—	P105	D5	IRQ0	TXD8/SSLB2_A/OM_SIO5	GTETRGA/GTIOC1A/AGTO2	—	—
128	104	71	—	P104	D4	IRQ1	RXD8/SSLB1_A/QIO2/OM_DQS	GTETRGB/GTIOC1B/AGTEE2	—	—
129	105	72	—	P103	D3	—	CTS0_RTS0/SSLB0_A/CTX0/QIO3/OM_SIO6	GTOWUP/GTIOC2A/AGTIO2	—	—

Table 1.17 引脚列表（4个中的3个）

LQFP176	LQFP144	LQFP100	电源、系统、时钟、调试、CAC	I/O ports	前任。公共汽车	前任。打断	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
81	65	43	—	P305	A10	IRQ8	TXD6/QSPCLK	GTOWUP/AGTOB2	—	—
82	66	44	—	P304	A9	IRQ9	RXD6	GTOWLO/GTIOC7A/AGTEE2	—	—
83	67	45	VSS	—	—	—	—	—	—	—
84	68	46	VCC	—	—	—	—	—	—	—
85	69	47	—	P303	A8	—	CTS9	GTIOC7B	—	—
86	70	48	—	P302	A7	IRQ5	TXD2/SSLA3_B	GTOUUP/GTIOC4A	—	—
87	71	49	—	P301	A6	IRQ6	RXD2/CTS9_RTS9/SSLA2_B	GTOULO/GTIOC4B/AGTIO0	—	—
88	72	50	TCK/SWCLK	P300	—	—	SSLA1_B	GTOUUP/GTIOC0A	—	—
89	73	51	TMS/SWDIO	P108	—	—	CTS9_RTS9/SSLA0_B	GTOULO/GTIOC0B/AGTOA3	—	—
90	74	52	TDO/SWO/CLKOUT	P109	—	—	TXD9/MOSIA_B/CTX1	GTOVUP/GTIOC1A/AGTOB3	—	—
91	75	53	TDI	P110	—	IRQ3	CTS2_RTS2/RXD9/MISOA_B/CRX1	GTOVLO/GTIOC1B/AGTEE3	—	—
92	76	54	—	P111	A5	IRQ4	SCK2/SCK9/RSPCKA_B	GTIOC3A/AGTOA5	—	—
93	77	55	—	P112	A4	—	TXD2/SCK1/SSLA0_B/QSSL/OM_CS1/SSISCK0_B	GTIOC3B/AGTOB5	—	—
94	78	56	—	P113	A3	—	RXD2/SSILRCK0_B	GTIOC2A/AGTEE5	—	—
95	79	57	—	P114	A2	—	CTS9/SSIRXD0_B	GTIOC2B/AGTIO5	—	—
96	80	58	—	P115	A1	—	SSITXD0_B	GTIOC4A	—	—
97	81	—	VCC	—	—	—	—	—	—	—
98	82	—	VSS	—	—	—	—	—	—	—
99	83	59	—	P608	A0/BC0	—	—	GTIOC4B	—	—
100	84	60	—	P609	CS1	—	CTX1/OM_ECS	GTIOC5A/AGTO5	—	—
101	85	61	—	P610	CS0	—	CTS7/CRX1/OM_CS0	GTIOC5B/AGTO4	—	—
102	86	—	CACREF/CLKOUT	P611	—	—	CTS7_RTS7	AGTO3	—	—
103	87	—	—	P612	D8	—	SCK7	AGTO2	—	—
104	88	—	—	P613	D9	—	TXD7	AGTO1	—	—
105	89	—	—	P614	D10	—	RXD7	AGTO0	—	—
106	—	—	—	P615	—	IRQ7	USB_VBUSEN_D	—	—	—
107	—	—	—	PA08	—	IRQ6	USB_OVRCURA_C	—	—	—
108	—	—	—	PA09	—	IRQ5	USB_OVRCURB_C	—	—	—
109	—	—	—	PA10	—	IRQ4	—	—	—	—
110	90	62	VCC	—	—	—	—	—	—	—
111	91	63	VSS	—	—	—	—	—	—	—
112	92	64	VCL	—	—	—	—	—	—	—
113	—	—	—	PA01	—	—	SCK8_C	—	—	—
114	—	—	—	PA00	—	—	TXD8_C	—	—	—
115	—	—	—	P607	—	—	RXD8_C	—	—	—
116	—	—	—	P606	—	—	CTS_RTS8_C	RTCOUT_B	—	—
117	93	—	—	P605	D11	—	CTS8	GTIOC8A/AGTO4	—	—
118	94	—	—	P604	D12	—	CTS9	GTIOC8B/AGTEE4	—	—
119	95	—	—	P603	D13	—	CTS9_RTS9	GTIOC7A/AGTIO4	—	—
120	96	65	—	P602	BCLK	—	TXD9/OM_CS1	GTIOC7B/AGTO3	—	—
121	97	66	—	P601	WR/WR0	—	RXD9/OM_SIO2	GTIOC6A/AGTEE3	—	—
122	98	67	CACREF/CLKOUT	P600	RD	—	SCK9/OM_SIO4	GTIOC6B/AGTIO3	—	—
123	99	—	VCC	—	—	—	—	—	—	—
124	100	—	VSS	—	—	—	—	—	—	—
125	101	68	—	P107	D7	—	CTS8_RTS8/OM_SIO3	GTIOC8A/AGTOA0	—	—
126	102	69	—	P106	D6	—	SCK8/SSLB3_A/OM_SIO0	GTIOC8B/AGTOB0	—	—
127	103	70	—	P105	D5	IRQ0	TXD8/SSLB2_A/OM_SIO5	GTETRGA/GTIOC1A/AGTO2	—	—
128	104	71	—	P104	D4	IRQ1	RXD8/SSLB1_A/QIO2/OM_DQS	GTETRGB/GTIOC1B/AGTEE2	—	—
129	105	72	—	P103	D3	—	CTS0_RTS0/SSLB0_A/CTX0/QIO3/OM_SIO6	GTOWUP/GTIOC2A/AGTIO2	—	—

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Table 1.17 Pin list (4 of 4)

LQFP176	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	I/O ports	Ex. Bus	Ex. Interrupt	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/ SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
130	106	73	—	P102	D2	—	SCK0/RSPCKB_A/CRX0/QIO0/OM_SIO1	GTOWLO/GTIOC2B/AGTO0	ADTRG0	—
131	107	74	—	P101	D1	IRQ1	TXD0/CTS1_RTS1/MOSIB_A/QIO1/OM_SIO7	GTETRGB/GTIOC5A/AGTEE0	—	—
132	108	75	—	P100	D0	IRQ2	RXD0/SCK1/MISOB_A/QSPCLK/OM_SCLK	GTETRGA/GTIOC5B/AGTIO0	—	—
133	109	—	—	P800	D14	—	CTS0	AGTOA4	AN125	—
134	110	—	—	P801	D15	—	CTS8	AGTOB4	AN126	—
135	—	—	—	P802	—	IRQ3	—	—	AN127	—
136	—	—	—	P803	—	IRQ2	—	—	AN128	—
137	—	—	—	P804	—	IRQ1	—	—	—	—
138	111	—	VCC	—	—	—	—	—	—	—
139	112	—	VSS	—	—	—	—	—	—	—
140	113	76	CACREF	P500	—	—	CTS5/USB_VBUSEN/QSPCLK	GTIU/AGTOA0	AN116	—
141	114	77	—	P501	—	IRQ11	TXD5/USB_OVRCURA/QSSL	GTIV/AGTOB0	AN117	—
142	115	78	—	P502	—	IRQ12	CTS6/RXD5/USB_OVRCURB/QIO0	GTIW/AGTOA2	AN118	—
143	116	79	—	P503	—	—	CTS6_RTS6/SCK5/USB_EXICEN/QIO1	GTETRGC/AGTOB2	AN119	—
144	117	80	—	P504	ALE	—	SCK6/CTS5_RTS5/USB_ID/QIO2	GTETRGD/AGTOA3	AN120	—
145	118	81	—	P505	—	IRQ14	RXD6/QIO3	AGTOB3	AN121	—
146	119	—	—	P506	—	IRQ15	TXD6	—	AN122	—
147	120	—	—	P507	—	—	SCK6/SCK5	—	AN123	—
148	—	—	—	P508	—	—	CTS_RTS5_B	—	AN124	—
149	121	82	VCC	—	—	—	—	—	—	—
150	122	83	VSS	—	—	—	—	—	—	—
151	123	84	—	P015	—	IRQ13	—	—	AN013/DA1	—
152	124	85	—	P014	—	—	—	—	AN012/DA0	—
153	125	86	VREFL	—	—	—	—	—	—	—
154	126	87	VREFH	—	—	—	—	—	—	—
155	127	88	AVCC0	—	—	—	—	—	—	—
156	128	89	AVSS0	—	—	—	—	—	—	—
157	129	90	VREFL0	—	—	—	—	—	—	—
158	130	91	VREFH0	—	—	—	—	—	—	—
159	—	—	—	P010	—	IRQ14	—	—	AN010	—
160	131	—	—	P009	—	IRQ13-DS	—	—	AN009	—
161	132	92	—	P008	—	IRQ12-DS	—	—	AN008	—
162	133	93	—	P007	—	—	—	—	AN007	—
163	134	94	—	P006	—	IRQ11-DS	—	—	AN006	—
164	135	95	—	P005	—	IRQ10-DS	—	—	AN005	—
165	136	96	—	P004	—	IRQ9-DS	—	—	AN004	—
166	137	97	—	P003	—	—	—	—	AN003	—
167	138	98	—	P002	—	IRQ8-DS	—	—	AN002/AN102	—
168	139	99	—	P001	—	IRQ7-DS	—	—	AN001/AN101	—
169	140	100	—	P000	—	IRQ6-DS	—	—	AN000/AN100	—
170	141	—	VSS	—	—	—	—	—	—	—
171	142	—	VCC	—	—	—	—	—	—	—
172	—	—	—	P806	—	IRQ0	—	—	—	—
173	—	—	—	P805	—	—	TXD5_B	—	—	—
174	—	—	—	P513	—	—	RXD5_B	—	—	—
175	143	—	—	P512	—	IRQ14	TXD4/SCL1_A/CTX1	GTIOC0A	—	—
176	144	—	—	P511	—	IRQ15	RXD4/SDA1_A/CRX1	GTIOC0B	—	—

Note: Several pin names have the added suffix of _A, _B, and _C. The suffix can be ignored when assigning functionality.

Table 1.17 引脚列表（4个，共4个）

LQFP176	LQFP144	LQFP100	电源、系统、时钟、调试、CAC	I/O ports	前任。公共汽车	前任。打断	SCI/IIC/SPI/CAN/USBFS/USBHS/QSPI/OSPI/ SSIE/SDHI/MMC/EHTERC(MII,RMII)/CEC	GPT/AGT/RTC	ADC12/DAC12	CTSU
130	106	73	—	P102	D2	—	SCK0/RSPCKB_A/CRX0/QIO0/OM_SIO1	GTOWLO/GTIOC2B/AGTO0	ADTRG0	—
131	107	74	—	P101	D1	IRQ1	TXD0/CTS1_RTS1/MOSIB_A/QIO1/OM_SIO7	GTETRGB/GTIOC5A/AGTEE0	—	—
132	108	75	—	P100	D0	IRQ2	RXD0/SCK1/MISOB_A/QSPCLK/OM_SCLK	GTETRGA/GTIOC5B/AGTIO0	—	—
133	109	—	—	P800	D14	—	CTS0	AGTOA4	AN125	—
134	110	—	—	P801	D15	—	CTS8	AGTOB4	AN126	—
135	—	—	—	P802	—	IRQ3	—	—	AN127	—
136	—	—	—	P803	—	IRQ2	—	—	AN128	—
137	—	—	—	P804	—	IRQ1	—	—	—	—
138	111	—	VCC	—	—	—	—	—	—	—
139	112	—	VSS	—	—	—	—	—	—	—
140	113	76	CACREF	P500	—	—	CTS5/USB_VBUSEN/QSPCLK	GTIU/AGTOA0	AN116	—
141	114	77	—	P501	—	IRQ11	TXD5/USB_OVRCURA/QSSL	GTIV/AGTOB0	AN117	—
142	115	78	—	P502	—	IRQ12	CTS6/RXD5/USB_OVRCURB/QIO0	GTIW/AGTOA2	AN118	—
143	116	79	—	P503	—	—	CTS6_RTS6/SCK5/USB_EXICEN/QIO1	GTETRGC/AGTOB2	AN119	—
144	117	80	—	P504	ALE	—	SCK6/CTS5_RTS5/USB_ID/QIO2	GTETRGD/AGTOA3	AN120	—
145	118	81	—	P505	—	IRQ14	RXD6/QIO3	AGTOB3	AN121	—
146	119	—	—	P506	—	IRQ15	TXD6	—	AN122	—
147	120	—	—	P507	—	—	SCK6/SCK5	—	AN123	—
148	—	—	—	P508	—	—	CTS_RTS5_B	—	AN124	—
149	121	82	VCC	—	—	—	—	—	—	—
150	122	83	VSS	—	—	—	—	—	—	—
151	123	84	—	P015	—	IRQ13	—	—	AN013/DA1	—
152	124	85	—	P014	—	—	—	—	AN012/DA0	—
153	125	86	VREFL	—	—	—	—	—	—	—
154	126	87	VREFH	—	—	—	—	—	—	—
155	127	88	AVCC0	—	—	—	—	—	—	—
156	128	89	AVSS0	—	—	—	—	—	—	—
157	129	90	VREFL0	—	—	—	—	—	—	—
158	130	91	VREFH0	—	—	—	—	—	—	—
159	—	—	—	P010	—	IRQ14	—	—	AN010	—
160	131	—	—	P009	—	IRQ13-DS	—	—	AN009	—
161	132	92	—	P008	—	IRQ12-DS	—	—	AN008	—
162	133	93	—	P007	—	—	—	—	AN007	—
163	134	94	—	P006	—	IRQ11-DS	—	—	AN006	—
164	135	95	—	P005	—	IRQ10-DS	—	—	AN005	—
165	136	96	—	P004	—	IRQ9-DS	—	—	AN004	—
166	137	97	—	P003	—	—	—	—	AN003	—
167	138	98	—	P002	—	IRQ8-DS	—	—	AN002/AN102	—
168	139	99	—	P001	—	IRQ7-DS	—	—	AN001/AN101	—
169	140	100	—	P000	—	IRQ6-DS	—	—	AN000/AN100	—
170	141	—	VSS	—	—	—	—	—	—	—
171	142	—	VCC	—	—	—	—	—	—	—
172	—	—	—	P806	—	IRQ0	—	—	—	—
173	—	—	—	P805	—	—	TXD5_B	—	—	—
174	—	—	—	P513	—	—	RXD5_B	—	—	—
175	143	—	—	P512	—	IRQ14	TXD4/SCL1_A/CTX1	GTIOC0A	—	—
176	144	—	—	P511	—	IRQ15	RXD4/SDA1_A/CRX1	GTIOC0B	—	—

Note: 几个引脚名称添加了_A、_B和_C的后缀。分配功能时可以忽略后缀。

2. CPU

The MCU is based on the Arm® Cortex®-M33 core.

2.1 Overview

2.1.1 CPU

- Arm Cortex-M33
  - Revision: r0p4-00rel1
  - Armv8-M architecture profile
  - Single Precision Floating-Point Unit compliant with the ANSI/IEEE Std 754-2008
- SAU (Security Attribution Unit): 0 region
- IDAU (Implementation Defined Attribution Unit): 8 regions
  - Code flash (secure/non-secure callable/non-secure)
  - Data Flash (secure/non-secure)
  - SRAM0 (secure/non-secure callable/non-secure)
- Memory Protection Unit (MPU)
  - Armv8 Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Two Systick timers: Secure and Non-secure instance
  - Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK)

See reference 1. and reference 2. in section 2.14. References for details.

2.1.2 Debug

- Arm® CoreSight™ ETM-M33
  - Revision: r0p2-00rel0
  - ARM ETM Architecture version 4.2
- Instrumentation Trace Macrocell (ITM)
- Data Watchpoint and Trace Unit (DWT)
  - 4 comparators for watchpoints and triggers
- Breakpoint Unit (BPU)
  - Breakpoint function is available.
    - 8 instruction comparators
    - 0 literal comparators
- Time Stamp Generator (TSG)
  - Time stamp for ETM and ITM
  - Driven by CPU clock
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control
- Debug Access Port (DAP)

2. CPU

MCU基于Arm®Cortex®-M33内核。

2.1 Overview

2.1.1 CPU

- Arm Cortex-M33
  - Revision: r0p4-00rel1
    Armv8-M架构配置文件
    符合ANSIIEEEStd754-2008的单精度浮点单元
●SAU（安全归属单元）：0地区
●IDAU（实施定义的归因单元）：8个地区
    代码闪存（安全非安全可调用非安全）
    数据闪存（安全非安全）
  - SRAM0 (secure/non-secure callable/non-secure)
●内存保护单元（MPU）
    Armv8保护内存系统架构(PMSAv8)
    安全MPU(MPU_S)：8个区域
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
    两个Systick计时器：安全和非安全实例
    由SysTick定时器时钟(SYSTICCLK)或系统时钟(ICLK)驱动

请参阅第2.14节中的参考1.和参考2.。详情参考。

2.1.2 Debug

- Arm® CoreSight™ ETM-M33
  - Revision: r0p2-00rel0
    ARMETM架构版本4.2
●仪器跟踪宏单元(ITM)
●数据观察点和跟踪单元(DWT)
    4个用于观察点和触发器的比较器
- Breakpoint Unit (BPU)
    断点功能可用。
    - 8 instruction comparators
    - 0 literal comparators
●时间戳生成器(TSG)
    ETM和ITM的时间戳
    由CPU时钟驱动
●调试寄存器模块（DBGREG）
    重置控制
    停止控制
●调试访问端口(DAP)

- JTAG Debug Port (JTAG-DP)
- Serial Wire Debug Port (SW-DP)

- Cortex-M33 Trace Port Interface Unit (TPIU)
  - 4 bits TPIU formatter output
  - Serial Wire Output
- Cross Trigger Interface (CTI)
- Embedded Trace Buffer (ETB)
  - CoreSight Trace Memory Controller with ETB configuration
  - Buffer size: 2 KB

See reference 1. and reference 2. in section 2.14. References for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU: maximum 200 MHz
- 4-bit TPIU trace interface: maximum 50 MHz
- Serial Write Output (SWO) trace interface: maximum 50 MHz
- Joint Test Action Group (JTAG) interface: maximum 25 MHz
- Serial Wire Data (SWD) interface: maximum 25 MHz

2.1.4 Block Diagram

Figure 2.1 shows a block diagram of the Cortex-M33 core.

JTAG调试端口(JTAG-DP)
串行线调试端口(SW-DP)

●Cortex-M33跟踪端口接口单元(TPIU)
4位TPIU格式化输出
串行线输出

●交叉触发接口(CTI)

●嵌入式跟踪缓冲区(ETB)
具有ETB配置的CoreSight跟踪内存控制器
- Buffer size: 2 KB

请参阅第2.14节中的参考1.和参考2.。详情参考。

2.1.3 工作频率

MCU的工作频率如下：

- CPU: maximum 200 MHz

●4位TPIU跟踪接口：最大50MHz
●串行写输出(SWO)跟踪接口：最大50MHz
●联合测试行动组(JTAG)接口：最大25MHz
●串行线数据(SWD)接口：最大25MHz

2.1.4 框图

图2.1显示了Cortex-M33内核的框图。

RA生态工作室

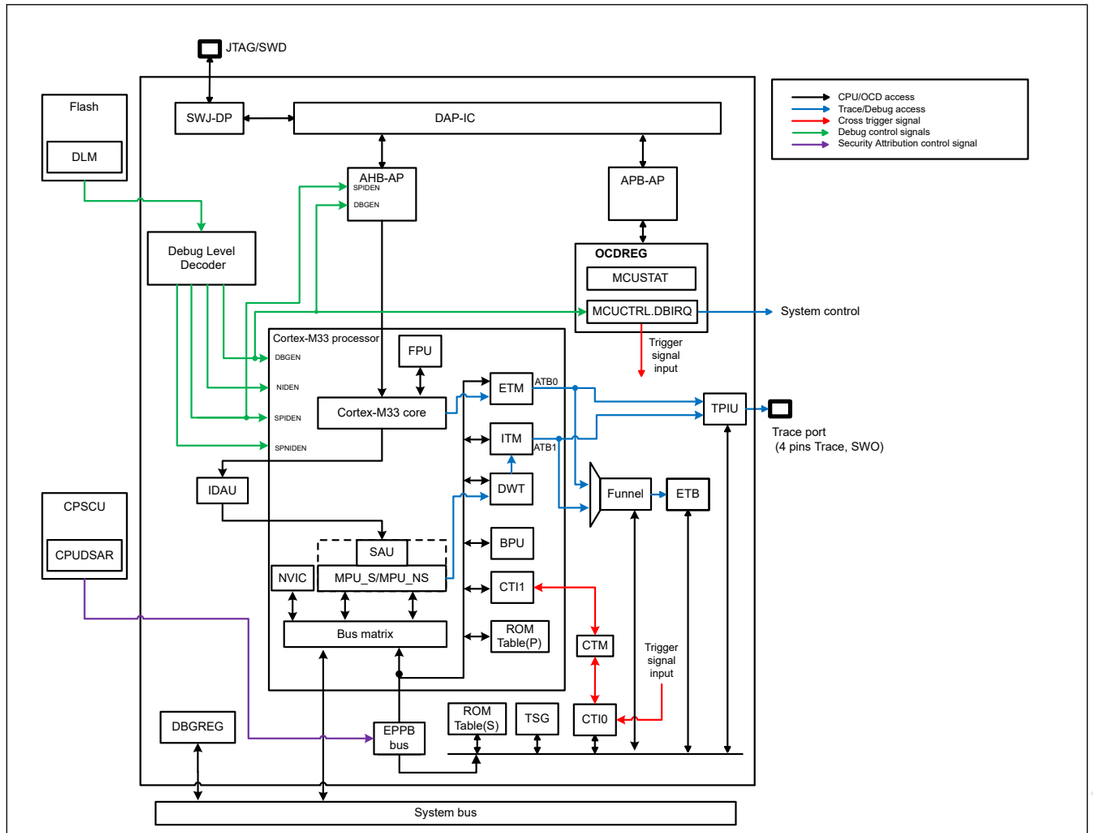

Figure 2.1 Cortex-M33 block diagram

2.2 Implementation Options

Table 2.1 shows the implementation options of the MCU.

Table 2.1 Implementation options (1 of 2)

Option	Implementation
SAU	Not included
IDAU	Included, 8 regions
MPU	Included, 8 regions for Secure and 8 regions for Non-secure
BPU	Included
Cross Trigger Interface (CTI)	Included
DWT	Included
Number of Wakeup Interrupt Controllers (WIC)	Not included ICU can wake up CPU instead of WIC. See section 13, Interrupt Controller Unit (ICU) for details.
TPIU	Included ● 4 bits TPIU formatter output ● Serial Wire Output
FPU	Included
DSP	Included

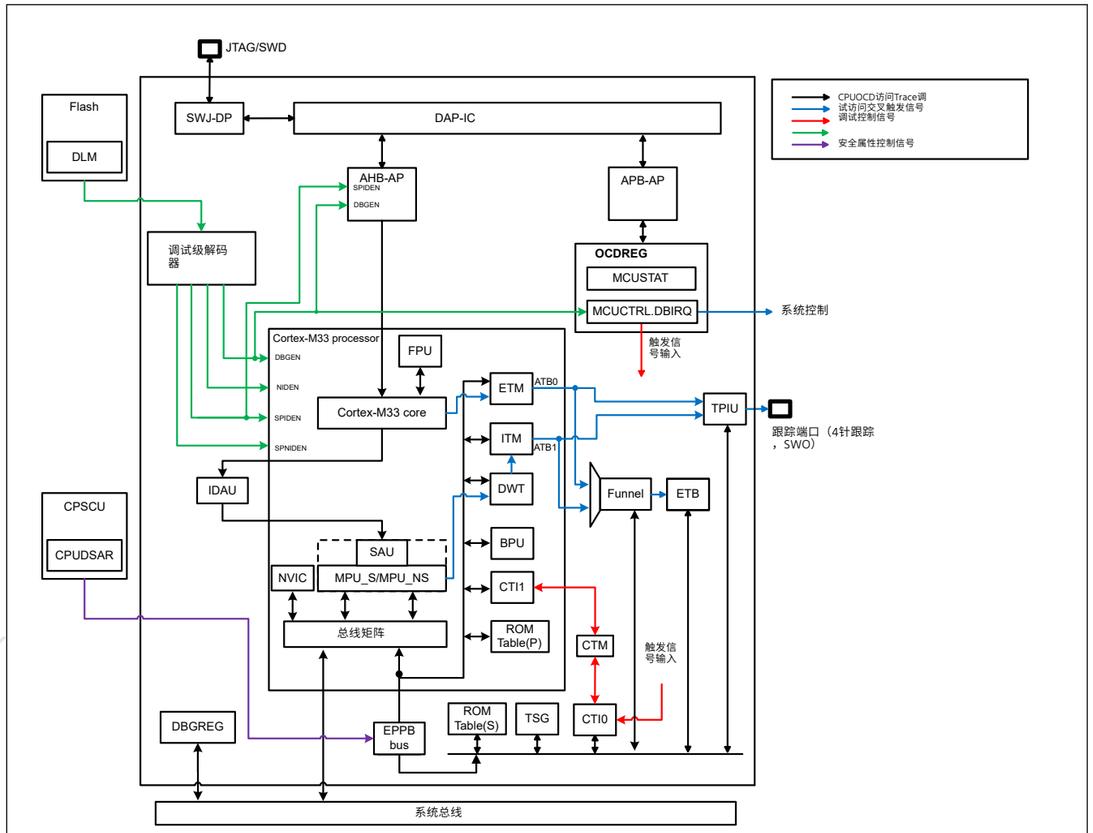

Figure 2.1 Cortex-M33框图

2.2 实施选项

表2.1显示了MCU的实现选项。

Table 2.1 实施选项（2个中的1个）

Option	Implementation
SAU	不包含
IDAU	包括，8个地区
MPU	包括，8个安全区域和8个非安全区域
BPU	Included
交叉触发接口(CTI)	Included
DWT	Included
唤醒中断控制器(WIC)的数量	不包含 ICU可以唤醒CPU而不是WIC。有关详细信息，请参见第13节，中断控制器单元(ICU)。
TPIU	Included ● 4位TPIU格式化输出 ● 串行线输出
FPU	Included
DSP	Included

RA生态工作室

Table 2.1 Implementation options (2 of 2)

Option	Implementation
Embedded Trace Macrocell (ETM)	Included
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 10, Low Power Modes. Note: SCB.SCR.SLEEPDEEP is ignored.
Interrupts	98
Priority bits	4 bits (16 levels)
Endianness	Little-endian
Memory features	Cacheable attribute is utilized in the MCU. See section 14, Buses for the detail.
SysTick	Included
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 Reference clock provided Bit [30] = 1 TERMS value is inexact Bits [29:24] = 0x00 Reserved Bits [23:0] = 0x000147 TERM: (32768 × 10 ms) - 1/32.768 kHz = 326.66 decimal = 327 with skew = 0x000147
Event input/output	Not implemented
Global exclusive monitor	Not implemented
System reset request output	The SYSRESETREQ bit in Application Interrupt and Reset Control Register causes a CPU reset

2.3 Trace Interface

A Trace Port Interface Unit (TPIU) and Serial Wire Output (SWO) provide trace output. Table 2.2 shows the MCU pins for the function. These pins are multiplexed with other functions.

Table 2.2 Trace function pins

Name	I/O	Function	When not in use
TCLK	Output	Trace clock	Open
TDATA0	Output	Trace data output 0	Open
TDATA1	Output	Trace data output 1	Open
TDATA2	Output	Trace data output 2	Open
TDATA3	Output	Trace data output 3	Open
TDO/SWO	Output	Serial wire output multiplexed with JTAG TDO pin	Open

2.4 JTAG/SWD Interface

Table 2.3 shows the JTAG/SWD pins.

Table 2.3 JTAG/SWD pins

Name	I/O	Function	When not in use
TDI	Input	JTAG TDI pin	Pull-up
TDO/SWO	Output	JTAG TDO pin multiplexed with serial wire output	Open
TCK/SWCLK	Input	JTAG clock pin Serial wire clock pin	Pull-up
TMS/SWDIO	I/O	JTAG TMS pin Serial wire data I/O pin	Pull-up

Table 2.1 实施选项（2个中的2个）

Option	Implementation
嵌入式跟踪宏单元(ETM)	Included
睡眠模式省电	支持睡眠模式和其他低功耗模式。有关详细信息，请参阅第10节，低电源模式。 Note: SCB.SCR.SLEEPDEEP被忽略。
Interrupts	98
优先位	4 bits (16 levels)
Endianness	Little-endian
记忆功能	可缓存属性在MCU中使用。有关详细信息，请参阅第14节，总线。
SysTick	Included
SYST_CALIB register (0x4000_0147)	Bit [31] = 0 提供参考时钟 Bit [30] = 1 TERMS值不准确 Bits [29:24] = 0x00 Reserved Bits [23:0] = 0x000147 TERM:(32768×10ms)132.768kHz=326.66十进制=327withskew=0x000147
Event input/output	未实现
全球独家监控	未实现
系统复位请求输出	应用程序中断和复位控制寄存器中的SYSRESETREQ位导致CPU复位

2.3 跟踪接口

跟踪端口接口单元(TPIU)和串行线输出(SWO)提供跟踪输出。表2.2显示了该功能的MCU引脚。这些引脚与其他功能复用。

Table 2.2 跟踪功能引脚

Name	I/O	Function	不使用时
TCLK	Output	跟踪时钟	Open
TDATA0	Output	跟踪数据输出0	Open
TDATA1	Output	跟踪数据输出1	Open
TDATA2	Output	跟踪数据输出2	Open
TDATA3	Output	跟踪数据输出3	Open
TDO/SWO	Output	串行线输出与JTAGTDO引脚复用	Open

2.4 JTAG/SWD Interface

表2.3显示了JTAGSWD引脚。

Table 2.3 JTAG/SWD pins

Name	I/O	Function	不使用时
TDI	Input	JTAG TDI pin	Pull-up
TDO/SWO	Output	JTAGTDO引脚与串行线输出复用	Open
TCK/SWCLK	Input	JTAG时钟引脚 串行线时钟引脚	Pull-up
TMS/SWDIO	I/O	JTAG TMS pin 串行线数据IO引脚	Pull-up

2.5 Security Attribution for Memory

In this MCU, SAU is not implemented and IDAU performs region definition for memory. IDAU divides the memory into 8 different areas as shown in Figure 2.2.

The code flash, the data flash, and the SRAM are divided into Secure (S), Non-secure (NS) and Non-secure callable (NSC) regions. These memory security attributions are set into the nonvolatile memory by the serial programming command when the device lifecycle is in SSD state. These memory security attributions are loaded into the IDAU and the memory controller before application execution. These memory security attributions cannot be updated by application but can read through the dedicated registers.

Note: When configuring, the memory regions should satisfy the setting condition of minimum address unit shown in Table 2.4.

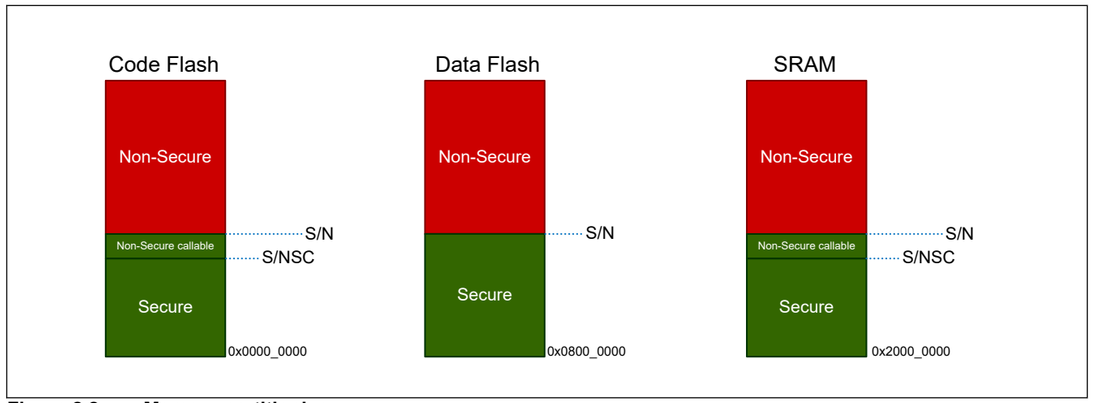

Figure 2.2 Memory partitioning

Table 2.4 S/NS and S/NSC boundary list

Boundary	Code flash	Data flash	SRAM
S/NS	32 KB	1 KB	8 KB
S/NSC	1 KB	—	1 KB

Each region has its dedicated ID as follows. The code flash is banked in dual mode. For more details, see section 2.14. References.

IREGION (IDAU region number)	Description
0x0D	Non-secure SRAM
0x0E	Non-secure callable SRAM
0x0F	Secure SRAM
0x09	Non-secure data flash
0x0B	Secure data flash
0x05	Non-secure code flash
0x06	Non-secure callable code flash
0x07	Secure code flash

2.6 Debug Function

2.6.1 Debugger connectivity

In this MCU, debug function is considered in three levels, DBG0, DBG1, DBG2. At DBG0, no debug function is available. DBG1 level is defined as non-secure debug in ARMv-8 and the debugger can only access defined non-secure debug

2.5 内存安全归属

在这个MCU中，没有实现SAU，而IDAU为内存执行区域定义。IDAU将内存划分为8个不同的区域，如图2.2所示。

代码闪存、数据闪存和SRAM分为安全(S)、非安全(NS)和非安全可调用(NSC)区域。当设备生命周期处于SSD状态时，这些内存安全属性由串行编程命令设置到非易失性内存中。这些内存安全属性在应用程序执行之前被加载到IDAU和内存控制器中。这些内存安全属性不能由应用程序更新，但可以通过专用寄存器读取。

Note: 配置时，内存区域应满足表2.4所示的最小地址单元设置条件。

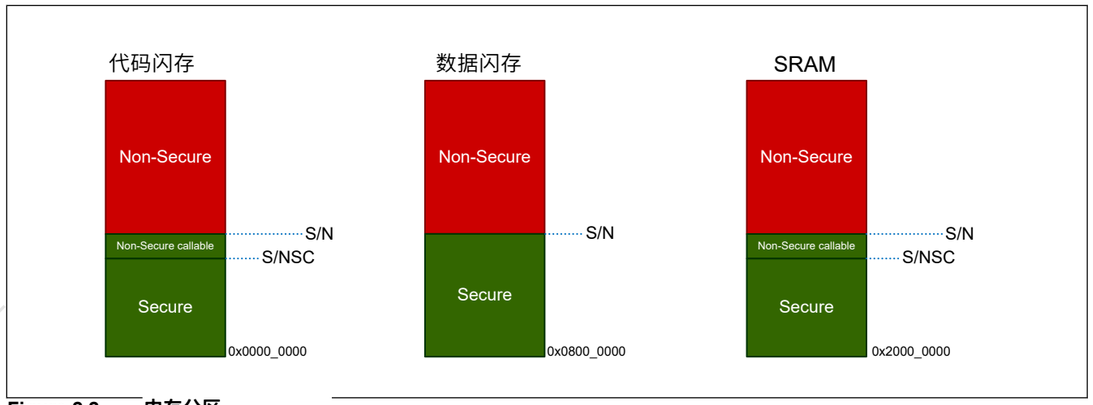

Figure 2.2 内存分区

Table 2.4 SNS和SNSC边界列表

Boundary	代码闪存	数据闪存	SRAM
S/NS	32 KB	1 KB	8 KB
S/NSC	1 KB	—	1 KB

每个区域都有其专用ID，如下所示。代码闪存以双模式存储。有关详细信息，请参阅第2.14节。References.

IREGION (IDAU region number)	Description
0x0D	Non-secure SRAM
0x0E	Non-secure callable SRAM
0x0F	Secure SRAM
0x09	非安全数据闪存
0x0B	安全数据闪存
0x05	非安全代码闪存
0x06	非安全可调用代码闪存
0x07	安全代码闪存

2.6 调试功能

2.6.1 调试器连接

在本单片机中，调试功能分为三个层次，DBG0、DBG1、DBG2。在DBG0，没有调试功能可用。
DBG1级别在ARMv-8中定义为非安全调试，调试器只能访问定义的非安全调试

accessible regions. DBG2 level is defined as secure debug in ARMv-8 and at this level, nonsecure and secure debug function is enabled and can be accessible from the debugger.

Debug level is determined by the Device Lifecycle Management (DLM) state of the product.

See Figure 2.1 for debugger accessible regions.

Table 2.5 shows the CPU debug function and conditions.

Table 2.5 CPU debug function and conditions

Condition			Permitted debug function
OCD connect*1	DLM State	Debug level	Description
Connected	CM	DBG2	All debug functions are available
Connected	SSD	DBG2	All debug functions are available
Connected	NSECSD	DBG1	Only Non-secure debug function is available
Connected	DPL	DBG0	Debugger connection is not available
Connected	LCK_DBG	DBG0	Debugger connection is not available
Connected	LCK_BOOT	DBG0	Debugger connection is not available
Connected	RMA_REQ	DBG0	Debugger connection is not available
Connected	RMA_ACK	DBG2	All debug functions are available

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.

2.6.2 Emulator Connection

Renesas provides the emulator which supports both debugging using SWD or JTAG communication and serial programming using SCI communication. This emulator makes it easy to switch between debug-ging and serial programming.

Table 2.6 shows the pinout of 10 pin or 20 pin socket pinouts when using this emulator. The pinout of SWD and JTAG is ARM standard, and MD, TXD, RXD pins are added for the serial programming using SCI communication.

The serial programming interface must be used to program the TrustZone IDAU boundary register settings.

It is recommended to connect P300/SWCLK/TCK and P201/MD pins using wired OR circuit on the board to use both debugging and serial programming.

Table 2.6 Pin assign for emulator (1 of 2)

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	P108/SWDIO	P108/TMS	NC
4	P300/SWCLK Wired OR with P201/MD	P300/TCK Wired OR with P201/MD	P201/MD
6	P109/SWO/TXD9	P109/SWO/TXD9	P109/TXD9
8	P110/RXD9	P110/TDI/RXD9	P110/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	P214/TCLK	P214/TCLK	NC
14	P211/TDATA[0]	P211/TDATA[0]	NC
16	P210/TDATA[1]	P210/TDATA[1]	NC
18	P209/TDATA[2]	P209/TDATA[2]	NC
20	P208/TDATA[3]	P208/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND

可访问的地区。DBG2级别在ARMv-8中定义为安全调试，在此级别，启用了非安全和安全调试功能，并且可以从调试器访问。

调试级别由产品的设备生命周期管理(DLM)状态确定。

有关调试器可访问区域，请参见图2.1。

表2.5显示了CPU调试功能和条件。

Table 2.5 CPU调试功能及条件

Condition			允许的调试功能
强迫症连接*1	DLM State	调试级别	Description
Connected	CM	DBG2	所有调试功能均可用
Connected	SSD	DBG2	所有调试功能均可用
Connected	NSECSD	DBG1	只有非安全调试功能可用
Connected	DPL	DBG0	调试器连接不可用
Connected	LCK_DBG	DBG0	调试器连接不可用
Connected	LCK_BOOT	DBG0	调试器连接不可用
Connected	RMA_REQ	DBG0	调试器连接不可用
Connected	RMA_ACK	DBG2	所有调试功能均可用

注1.OCD连接由SWJ-DP寄存器中的CDBGPWUPREQ位输出决定。该位只能由OCD写入。但是，可以通过读取DBGSTR.CDBGPWUPREQ位来确认该位的电平。

2.6.2 仿真器连接

瑞萨电子提供的仿真器支持使用SWD或JTAG通信进行调试和使用SCI通信进行串行编程。该仿真器可以轻松地在调试和串行编程之间切换。

表2.6显示了使用该仿真器时10针或20针插座的引脚排列。SWD和JTAG的管脚是ARM标准，并增加了MD、TXD、RXD引脚用于使用SCI通信的串行编程。

必须使用串行编程接口对TrustZoneIDAU边界寄存器设置进行编程。

建议使用板上的有线或电路连接P300SWCLKTCK和P201MD引脚，以同时使用调试和串行编程。

Table 2.6 模拟器的引脚分配（2个中的1个）

针号	SWD	JTAG	使用SCI进行串行编程
1	VCC	VCC	VCC
2	P108/SWDIO	P108/TMS	NC
4	P300/SWCLK 有线或带P201MD	P300/TCK 有线或带P201MD	P201/MD
6	P109/SWO/TXD9	P109/SWO/TXD9	P109/TXD9
8	P110/RXD9	P110/TDI/RXD9	P110/RXD9
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	P214/TCLK	P214/TCLK	NC
14	P211/TDATA[0]	P211/TDATA[0]	NC
16	P210/TDATA[1]	P210/TDATA[1]	NC
18	P209/TDATA[2]	P209/TDATA[2]	NC
20	P208/TDATA[3]	P208/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND

Table 2.6 Pin assign for emulator (2 of 2)

Pin No.	SWD	JTAG	Serial Programming using SCI
7	NC	NC	NC
11, 13	NC	NC	NC

2.6.3 Self-Hosted Debug Function

As described in section 2.7.6. CPUDSAR : CPU Debug Security Attribution Register, at the initial setting access from the CPU in non-secure state to CoreSight debug components is protected, that is, the non-secure access to Coresight debug components from the self-hosted debugger is not allowed when the debug level is DBG2 at the initial setting. Therfore, you must set CPUDSAR.CPUDSA0 to 1 to enable the full self-hosted debug function.

Note: There is no restriction for the self-hosted debug function while the CPU is in the secure state.

2.6.4 Effect of Debug Function

The debug function effects inside and outside of CPU.

2.6.4.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby, Snooze or Deep Software Standby mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.7.5.2. MCUCTRL : MCU Control Register.

2.6.4.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR register setting.

Table 2.7 Reset or interrupt and mode setting

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting
Voltage monitor 0 reset	Depends on DBGSTOPCR setting	
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting	
Voltage monitor 2 reset/interrupt	Depends on DBGSTOPCR setting	
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting	
SRAM ECC error reset/interrupt	Depends on DBGSTOPCR setting	
Cache parity error reset/interrupt	Depends on DBGSTOPCR setting	
Bus master MPU error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.

Table 2.6 仿真器的引脚分配（2个中的2个）

针号	SWD	JTAG	使用SCI进行串行编程
7	NC	NC	NC
11, 13	NC	NC	NC

2.6.3 自托管调试功能

如第2.7.6节所述。CPUDSAR：CPUDebugSecurityAttributionRegister，在初始设置时从
对CoreSight调试组件处于非安全状态的CPU受到保护，即当初始设置的调试级别为DBG2时，不允许自托管调试器对Coresight调试组件的非安全访问。因此，您必须将CPUDSAR.CPUDSA0设置为1以启用完全自托管调试功能。

Note: 当CPU处于安全状态时，自托管调试功能没有限制。

2.6.4 调试功能的效果

调试功能影响CPU内部和外部。

2.6.4.1 低功耗模式

即使CPU进入软件待机、贪睡或深度软件待机模式，所有CoreSight调试组件都可以存储寄存器设置。但是，AHB-AP在这些低功耗模式下无法响应片上调试(OCD)访问。OCD必须等待取消低功耗模式才能访问CoreSight调试组件。要请求取消低功耗模式，OCD可以设置MCUCTRL寄存器中的DBIRQ位。详见2.7.5.2节。MCUCTRL：MCU控制寄存器。

2.6.4.2 Reset

在OCD模式下，一些复位取决于CPU状态和DBGSTOPCR寄存器设置。

Table 2.7 复位或中断和模式设置

重置或中断名称	片上调试(OCD)模式下的控制	
	强迫症休息模式	强迫症运行模式
RES引脚复位	与用户模式相同	
Power-on reset	与用户模式相同	
独立看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置
看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置
电压监控器0复位	取决于DBGSTOPCR设置	
电压监视器1复位中断	取决于DBGSTOPCR设置	
电压监视器2复位中断	取决于DBGSTOPCR设置	
SRAM奇偶校验错误复位中断	取决于DBGSTOPCR设置	
SRAM ECC error reset/interrupt	取决于DBGSTOPCR设置	
缓存奇偶校验错误复位中断	取决于DBGSTOPCR设置	
总线主控MPU错误复位中断	与用户模式相同	
深度软件待机复位	与用户模式相同	
软件复位	与用户模式相同	

Note: 在OCD中断模式下，CPU停止。在OCD运行模式下，CPU处于OCD模式并且CPU不会停止。
注1.IWDT和WDT在此模式下始终停止。

2.7 Programmers Model

2.7.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCDREG registers.

Figure 2.3 shows a block diagram of the AP connection and address spaces.

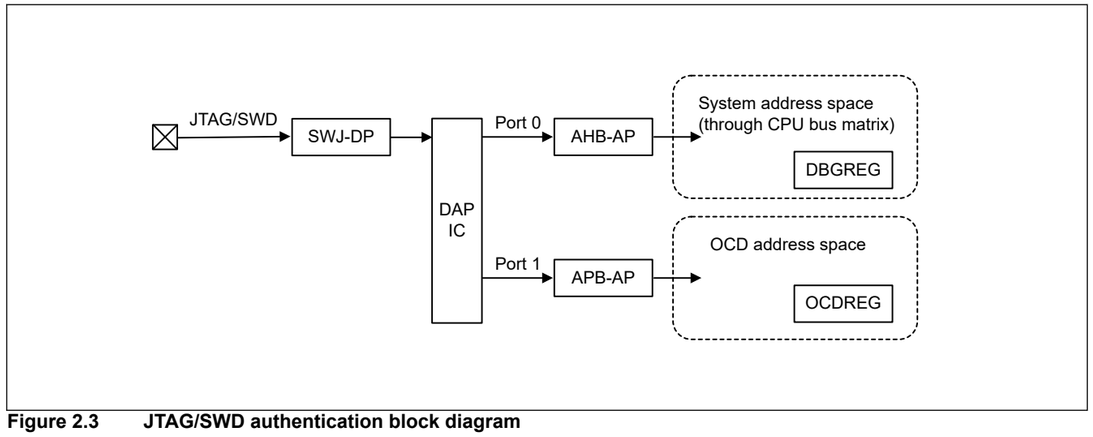

Figure 2.3 JTAG/SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space and can be accessed from the OCD emulator, the CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access OCDREG.

2.7.2 Peripheral Address Map

In system address space, the Cortex-M33 core has a Private Peripheral Bus (PPB) which can be accessed only from CPU and OCD emulator. The PPB is expanded from the original implementation of the Cortex-M33 core for this MCU. Table 2.8 shows the address map of the MCU.

Table 2.8 Peripheral address map (1 of 2)

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.14. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.14. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.14. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.14. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.14. References
TPIU	0xE004_0000	0xE004_0FFF	See reference 3. in section 2.14. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.14. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.14. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.14. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.9. CoreSight ATB Funnel and reference 4. in section 2.14. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.14. References

2.7 程序员模型

2.7.1 地址空间

MCU调试系统包括两个CoreSight访问端口(AP)：

●AHB-AP，与CPU总线矩阵相连，与CPU具有相同的系统地址空间访问权限

●APB-AP，具有专用的地址空间（OCD地址空间）并连接到OCDREG寄存器。

图2.3显示了AP连接和地址空间的框图。

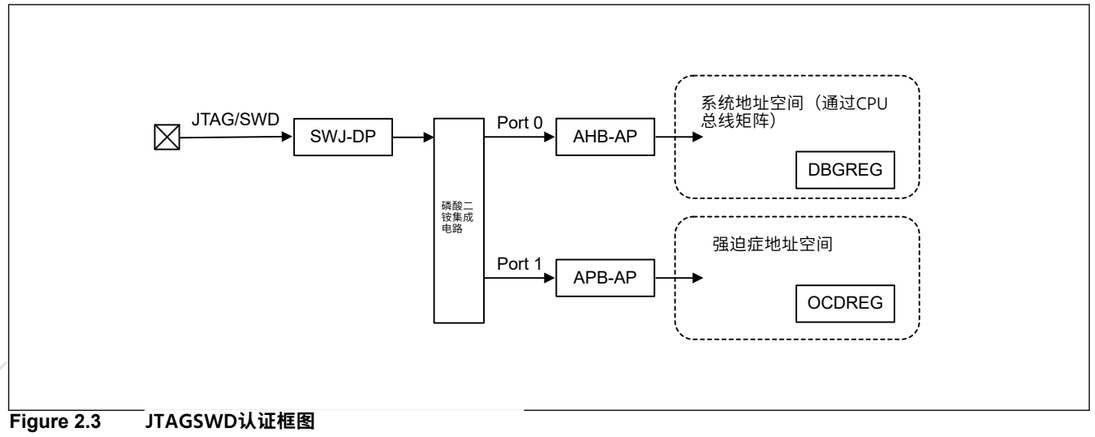

Figure 2.3 JTAGSWD认证框图

出于调试目的，有两个寄存器模块，DBGREG和OCDREG。DBGREG位于系统地址空间中，可以从OCD仿真器、CPU和MCU中的其他总线主控器访问。OCDREG位于OCD地址空间，只能从OCD工具访问。CPU和其他总线主机无法访问OCDREG。

2.7.2 外设地址映射

在系统地址空间中，Cortex-M33内核有一个专用外设总线(PPB)，只能从CPU和OCD仿真器访问。PPB是从该MCU的Cortex-M33内核的原始实现扩展而来的。表2.8显示了MCU的地址映射。

Table 2.8 外设地址映射(1of2)

组件名称	起始地址	结束地址	Note
ITM	0xE000_0000	0xE000_0FFF	请参阅第2.14节中的参考2。参考
DWT	0xE000_1000	0xE000_1FFF	请参阅第2.14节中的参考2。参考
BPU	0xE000_2000	0xE000_2FFF	请参阅第2.14节中的参考2。参考
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	请参阅第2.14节中的参考1。参考
Non-Secure SCS	0xE002_E000	0xE002_EFFF	请参阅第2.14节中的参考2。参考
TPIU	0xE004_0000	0xE004_0FFF	请参见第2.14节中的参考3。参考
ETM	0xE004_1000	0xE004_1FFF	请参阅第2.14节中的参考1。参考
CTI1	0xE004_2000	0xE004_2FFF	请参阅第2.14节中的参考2。参考
CTI0	0xE004_4000	0xE004_4FFF	参见第2.14节中的参考4。参考
ATB Funnel	0xE004_7000	0xE004_7FFF	请参阅第2.9节。CoreSightATB漏斗和参考4.在第2.14节中。References
ETB	0xE004_8000	0xE004_8FFF	参见第2.14节中的参考4。参考

Table 2.8 Peripheral address map (2 of 2)

Component name	Start address	End address	Note
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.11. CoreSight Time Stamp Generator and reference 4. in section 2.14. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.14. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.14. References

2.7.3 CoreSight ROM Table

The MCU contains two CoreSight ROM Tables, the processor and system ROM Tables. The Processor ROM Table contains entries which hold a list of debug components inside the processor. The System ROM Table contains entries of Processor ROM Table and others debug components outside the processor.

2.7.3.1 ROM entries

ROM entries hold a list of components in the system. OCD emulator can use the ROM entries to determine which components are implemented in a system.

Table 2.9 and Table 2.10 show the System ROM entries and Processor ROM entries. See reference 5. in section 2.14. References for details.

Table 2.9 System ROM entries

#	Address	Access size	R/W	Value	Target module pointer
0	0xE00F_E000	32 bits	R	0xFFF46003	CTI0
1	0xE00F_E004	32 bits	R	0xFFF49003	Funnel
2	0xE00F_E008	32 bits	R	0xFFF4A003	ETB
3	0xE00F_E00C	32 bits	R	0xFFF4B003	TSG
4	0xE00F_E010	32 bits	R	0xFFF42003	TPIU
5	0xE00F_E014	32 bits	R	0x00001003	Processor ROM table
6	0xE00F_E018	32 bits	R	0x00000000	End of entries

Table 2.10 Processor ROM Entries

#	Address	Access size	R/W	Value	Target module pointer
0	0xE00F_F000	32 bits	R	0xFFF0F003	SCS
1	0xE00F_F004	32 bits	R	0xFFF02003	DWT
2	0xE00F_F008	32 bits	R	0xFFF03003	BPU
3	0xE00F_F00C	32 bits	R	0xFFF01003	ITM
4	0xE00F_F014	32 bits	R	0xFFF42003	ETM
5	0xE00F_F018	32 bits	R	0xFFF43003	CTI1
6	0xE00F_F020	32 bits	R	0x00000000	End of entries

2.7.3.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.11 shows the registers. See reference 5. in section 2.14. References for details of each register.

Table 2.11 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
PID4	0xE00F_EFD0	32 bits	R	0x00000004
PID5	0xE00F_EFD4	32 bits	R	0x00000000
PID6	0xE00F_EFD8	32 bits	R	0x00000000

Table 2.8 外设地址映射(2of2)

组件名称	起始地址	结束地址	Note
时间戳生成器	0xE004_9000	0xE004_9FFF	请参阅第2.11节。CoreSight时间戳生成器和第2.14节中的参考4。参考
系统ROM表	0xE00F_E000	0xE00F_EFFF	请参见第2.14节中的参考3。参考
处理器ROM表	0xE00F_F000	0xE00F_FFFF	请参阅第2.14节中的参考2。参考

2.7.3 CoreSightROM表

MCU包含两个CoreSightROM表，即处理器和系统ROM表。处理器ROM表包含保存处理器内部调试组件列表的条目。系统ROM表包含处理器ROM表和处理器外部的其他调试组件的条目。

2.7.3.1 ROM条目

ROM条目保存系统中的组件列表。OCD仿真器可以使用ROM条目来确定系统中实现了哪些组件。

表2.9和表2.10显示了系统ROM条目和处理器ROM条目。请参阅第2.14节中的参考5。
详情参考。

Table 2.9 系统ROM条目

#	Address	访问大小	R/W	Value	目标模块指针
0	0xE00F_E000	32 bits	R	0xFFF46003	CTI0
1	0xE00F_E004	32 bits	R	0xFFF49003	Funnel
2	0xE00F_E008	32 bits	R	0xFFF4A003	ETB
3	0xE00F_E00C	32 bits	R	0xFFF4B003	TSG
4	0xE00F_E010	32 bits	R	0xFFF42003	TPIU
5	0xE00F_E014	32 bits	R	0x00001003	处理器ROM表
6	0xE00F_E018	32 bits	R	0x00000000	条目结束

Table 2.10 处理器ROM条目

#	Address	访问大小	R/W	Value	目标模块指针
0	0xE00F_F000	32 bits	R	0xFFF0F003	SCS
1	0xE00F_F004	32 bits	R	0xFFF02003	DWT
2	0xE00F_F008	32 bits	R	0xFFF03003	BPU
3	0xE00F_F00C	32 bits	R	0xFFF01003	ITM
4	0xE00F_F014	32 bits	R	0xFFF42003	ETM
5	0xE00F_F018	32 bits	R	0xFFF43003	CTI1
6	0xE00F_F020	32 bits	R	0x00000000	条目结束

2.7.3.2 CoreSight组件寄存器

CoreSightROM表列出了ArmCoreSight架构中定义的CoreSight组件寄存器。
表2.11显示了寄存器。请参阅第2.14节中的参考5。每个寄存器的详细信息参考。

Table 2.11 CoreSightROM表中的CoreSight组件寄存器(1of2)

Name	Address	访问大小	R/W	初始值
PID4	0xE00F_EFD0	32 bits	R	0x00000004
PID5	0xE00F_EFD4	32 bits	R	0x00000000
PID6	0xE00F_EFD8	32 bits	R	0x00000000

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Table 2.11 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	0xE00F_EFDC	32 bits	R	0x00000000
PID0	0xE00F_EFE0	32 bits	R	0x00000036
PID1	0xE00F_EFE4	32 bits	R	0x00000030
PID2	0xE00F_EFE8	32 bits	R	0x0000000A
PID3	0xE00F_EFEC	32 bits	R	0x00000000
CID0	0xE00F_EFF0	32 bits	R	0x0000000D
CID1	0xE00F_EFF4	32 bits	R	0x00000010
CID2	0xE00F_EFF8	32 bits	R	0x00000005
CID3	0xE00F_EFFC	32 bits	R	0x000000B1

2.7.4 DBGREG Module

The DBGREG module controls the debug functionalities and is implemented as a CoreSight-compliant component.

Table 2.12 shows the DBGREG registers other than the CoreSight component registers.

Table 2.12 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	0x4001_B000	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

2.7.4.1 DBGSTR : Debug Status Register

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	These bits are read as 0.	R
28	CDBGPWRUPREQ	Debug power-up request 0: OCD is not requesting debug power up 1: OCD is requesting debug power up	R
29	CDBGPWRUPACK	Debug power-up acknowledge 0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged	R
31:30	—	These bits are read as 0.	R

The DBGSTR register is a status register which indicates the state of the debug power-up request to the MCU from the emulator.

Table 2.11 CoreSightROM表中的CoreSight组件寄存器(2of2)

Name	Address	访问大小	R/W	初始值
PID7	0xE00F_EFDC	32 bits	R	0x00000000
PID0	0xE00F_EFE0	32 bits	R	0x00000036
PID1	0xE00F_EFE4	32 bits	R	0x00000030
PID2	0xE00F_EFE8	32 bits	R	0x0000000A
PID3	0xE00F_EFEC	32 bits	R	0x00000000
CID0	0xE00F_EFF0	32 bits	R	0x0000000D
CID1	0xE00F_EFF4	32 bits	R	0x00000010
CID2	0xE00F_EFF8	32 bits	R	0x00000005
CID3	0xE00F_EFFC	32 bits	R	0x000000B1

2.7.4 DBGREG Module

DBGREG模块控制调试功能并被实现为符合CoreSight的组件。

表2.12显示了除CoreSight组件寄存器之外的DBGREG寄存器。

Table 2.12 Non-CoreSight DBGREG registers

Name		端口	Address	访问大小	R/W
调试状态寄存器	DBGSTR	Port 0	0x4001_B000	32 bits	R
调试停止控制寄存器	DBGSTOPCR	Port 0	0x4001_B010	32 bits	R/W

2.7.4.1 DBGSTR：调试状态寄存器

Base address: DBG = 0x4001_B000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	这些位读为0。	R
28	CDBGPWRUPREQ	调试上电请求 0：OCD不请求调试上电1：OCD请求调试上电	R
29	CDBGPWRUPACK	调试上电确认 0：未确认调试上电请求1：确认调试上电请求	R
31:30	—	这些位读为0。	R

DBGSTR寄存器是一个状态寄存器，它指示从仿真器到MCU的调试上电请求的状态。

2.7.4.2 DBGSTOPCR : Debug Stop Control Register

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DBGSTOP_CPER	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	Mask bit for IWDT reset/interrupt in the OCD run mode In the OCD break mode, the reset/interrupt is masked and IWDT counter is stopped, regardless of this bit value. 0: Enable IWDT reset/interrupt 1: Mask IWDT reset/interrupt and stop IWDT counter	R/W
1	DBGSTOP_WDT	Mask bit for WDT reset/interrupt in the OCD run mode In the OCD break mode, the reset/interrupt is masked and WDT counter is stopped, regardless of this bit value. 0: Enable WDT reset/interrupt 1: Mask WDT reset/interrupt and stop WDT counter	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
16	DBGSTOP_LVD0	Mask bit for LVD0 reset 0: Enable LVD0 reset 1: Mask LVD0 reset	R/W
17	DBGSTOP_LVD1	Mask bit for LVD1 reset/interrupt 0: Enable LVD1 reset/interrupt 1: Mask LVD1 reset/interrupt	R/W
18	DBGSTOP_LVD2	Mask bit for LVD2 reset/interrupt 0: Enable LVD2 reset/interrupt 1: Mask LVD2 reset/interrupt	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
24	DBGSTOP_RPER	Mask bit for SRAM parity error reset/interrupt 0: Enable SRAM parity error reset/interrupt 1: Mask SRAM parity error reset/interrupt	R/W
25	DBGSTOP_RECCR	Mask bit for SRAM ECC error reset/interrupt 0: Enable SRAM ECC error reset/interrupt 1: Mask SRAM ECC error reset/interrupt	R/W
30:26	—	These bits are read as 0. The write value should be 0.	R/W
31	DBGSTOP_CPER	Mask bit for Cache SRAM parity error reset/interrupt 0: Enable Cache SRAM parity error reset/interrupt 1: Mask Cache SRAM parity error reset/interrupt	R/W

The Debug Stop Control Register (DBGSTOPCR) specifies the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.7.4.3 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.13 shows the registers. See reference 4. in section 2.14. References for details of each register.

2.7.4.2 DBGSTOPCR:调试停止控制寄存器

Base address: DBG = 0x4001_B000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DBGSTOP_CPER	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD2	DBGSTOP_LVD1	DBGSTOP_LVD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	DBGSTOP_IWDT	OCD运行模式下IWDT复位中断的屏蔽位 在OCD中断模式下，复位中断被屏蔽，IWDT计数器停止，无论该位值如何。 0：使能IWDT复位中断1：屏蔽IWDT复位中断并停止IWDT计数器	R/W
1	DBGSTOP_WDT	OCD运行模式下WDT复位中断的屏蔽位 在OCD中断模式下，复位中断被屏蔽并且WDT计数器停止，无论该位值如何。 0：使能WDT复位中断1：屏蔽WDT复位中断并停止WDT计数器	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
16	DBGSTOP_LVD0	LVD0复位屏蔽位 0：启用LVD0复位1：屏蔽LVD0复位	R/W
17	DBGSTOP_LVD1	LVD1复位中断的屏蔽位 0：使能LVD1复位中断1：屏蔽LVD1复位中断	R/W
18	DBGSTOP_LVD2	LVD2复位中断的屏蔽位 0：使能LVD2复位中断1：屏蔽LVD2复位中断	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
24	DBGSTOP_RPER	SRAM奇偶校验错误复位中断的屏蔽位 0：使能SRAM奇偶校验错误复位中断1：屏蔽SRAM奇偶校验错误复位中断	R/W
25	DBGSTOP_RECCR	SRAMECC错误复位中断的屏蔽位 0：使能SRAMECC错误复位中断1：屏蔽SRAMECC错误复位中断	R/W
30:26	—	这些位被读取为0。写入值应为0。	R/W
31	DBGSTOP_CPER	CacheSRAM奇偶校验错误复位中断的屏蔽位 0：使能CacheSRAM奇偶校验错误复位中断1：屏蔽CacheSRAM奇偶校验错误复位中断	R/W

调试停止控制寄存器(DBGSTOPCR)指定OCD模式下的功能停止。当MCU不处于OCD模式时，寄存器中的所有位都被视为0。

2.7.4.3 DBGREGCoreSight组件寄存器

DBGREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.13显示了寄存器。参见第2.14节中的参考4。每个寄存器的详细信息参考。

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Table 2.13 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000000A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.7.5 OCDREG Module

The OCDREG module are only accessible by the On-Chip Debug (OCD) emulator. OCDREG is implemented as a CoreSight-compliant component.

Table 2.14 lists the OCDREG registers.

Table 2.14 OCDREG registers

Name		DAP port	Address	Access size	R/W
MCU Status Register	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU Control Register	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map.

2.7.5.1 MCUSTAT : MCU Status Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	SECDBG	DBGFUNCEN	BOOTMD	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	—
Value after reset:	0	0	1/0*1	1/0*1	1/0*1	0	0	1	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Function	R/W
0	—	These bits are read as 0.	R
1	CPUSLEEP	Sleep mode status This bit is unpredictable when the MCU is in Software Standby mode, Snooze mode, or Deep Software Standby mode. 0: CPU is not in Sleep mode 1: CPU in Sleep mode	R

Table 2.13 DBGREGCoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	0x4001_BFD0	32 bits	R	0x00000004
PID5	0x4001_BFD4	32 bits	R	0x00000000
PID6	0x4001_BFD8	32 bits	R	0x00000000
PID7	0x4001_BFDC	32 bits	R	0x00000000
PID0	0x4001_BFE0	32 bits	R	0x00000005
PID1	0x4001_BFE4	32 bits	R	0x00000030
PID2	0x4001_BFE8	32 bits	R	0x0000000A
PID3	0x4001_BFEC	32 bits	R	0x00000000
CID0	0x4001_BFF0	32 bits	R	0x0000000D
CID1	0x4001_BFF4	32 bits	R	0x000000F0
CID2	0x4001_BFF8	32 bits	R	0x00000005
CID3	0x4001_BFFC	32 bits	R	0x000000B1

2.7.5 OCDREG Module

OCDREG模块只能由片上调试(OCD)仿真器访问。OCDREG被实现为CoreSight-compliant component.

表2.14列出了OCDREG寄存器。

Table 2.14 OCDREG registers

Name		端口	Address	访问大小	R/W
MCU状态寄存器	MCUSTAT	Port 1	0x8000_0400	32 bits	R
MCU控制寄存器	MCUCTRL	Port 1	0x8000_0410	32 bits	R/W

Note: OCDREG位于专用的OCD地址空间中。该地址映射独立于系统地址映射。

2.7.5.1 MCUSTAT：MCU状态寄存器

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	SECDBG	DBGFUNCEN	BOOTMD	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	—
重置后的值：	0	0	1/0*1	1/0*1	1/0*1	0	0	1	0	0	0	0	0	1/0*1	1/0*1	0

Bit	Symbol	Function	R/W
0	—	这些位读为0。	R
1	CPUSLEEP	睡眠模式状态 当MCU处于软件待机模式、贪睡模式或深度软件待机模式。 0：CPU不处于休眠模式1：CPU处于休眠模式	R

Bit	Symbol	Function	R/W
2	CPUSTOPCLK	CPU clock status This bit is unpredictable when the MCU is in Deep Software Standby mode. 0: CPU clock is not stopped. 1: CPU clock is stopped.	R
7:3	—	These bits are read as 0.	R
8	—	These bits are read as 1.	R
10:9	—	These bits are read as 0.	R
11	BOOTMD	Boot mode status 0: Device is not in Boot mode 1: Device is in Boot mode	R
12	DBGFUNCEN	Debugger status 0: Debugger connection is not available 1: Debugger function is enabled	R
13	SECDBG	Secure Debug status 0: Secure Debug is not available 1: Secure Debug is available	R
31:14	—	These bits are read as 0.	R

Note 1. Depends on the MCU status.

2.7.5.2 MCUCTRL : MCU Control Register

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUWAIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	DBIRQ*2	Debug Interrupt Request Writing 1 to the bit wakes up the MCU from low power mode. The condition can be cleared by writing 0 to the DBIRQ bit. 0: Debug interrupt not requested 1: Debug interrupt requested	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	CPUWAIT*2	CPU Wait Setting Write 1 to assert CPUWAIT, write 0 to dessert CPUWAIT*1. 0: Clear CPUWAIT to low 1: Set CPUWAIT to high	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. CPUWAIT is used to prevent the processor from executing code immediately after reset.
Note 2. Access (R/W) to bit is valid only when Debug Level is DBG1 or DBG2.

2.7.5.3 OCDREG CoreSight component registers

The OCDREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.15 shows the registers. See reference 4. in section 2.14. References for details of each register.

Bit	Symbol	Function	R/W
2	CPUSTOPCLK	CPU时钟状态 当MCU处于深度软件待机模式时，该位是不可预测的。 0：CPU时钟不停止。1：CPU时钟停止。	R
7:3	—	这些位读为0。	R
8	—	这些位读为1。	R
10:9	—	这些位读为0。	R
11	BOOTMD	引导模式状态 0：设备未处于引导模式1：设备处于引导模式	R
12	DBGFUNCEN	调试器状态 0：调试器连接不可用1：调试器功能启用	R
13	SECDBG	安全调试状态 0：安全调试不可用1：安全调试可用	R
31:14	—	这些位读为0。	R

注1.取决于MCU状态。

2.7.5.2 MCUCTRL:MCU控制寄存器

Base address: CPU_OCD = 0x8000_0000

Offset address: 0x410

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUWAIT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
8	DBIRQ*2	调试中断请求 向该位写入1将MCU从低功耗模式唤醒。可以通过将0写入DBIRQ位来清除该条件。 0：未请求调试中断1：请求调试中断	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	CPUWAIT*2	CPU等待设置 写1来断言CPUWAIT，写0到甜点CPUWAIT*1。 0：清除CPUWAIT为低1：设置CPUWAIT为高	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

注1.CPUWAIT用于防止处理器在复位后立即执行代码。
注2.只有当DebugLevel为DBG1或DBG2时，对位的访问(RW)才有效。

2.7.5.3 OCDREGCoreSight组件寄存器

OCDREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.15显示了寄存器。参见第2.14节中的参考4。每个寄存器的详细信息参考。

Table 2.15 OCDREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.7.6 CPUDSAR : CPU Debug Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUDSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	CPUDSA0	CPU Debug Security Attribution 0 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, and no TrustZone access error is generated.

Note: This register is write-protected by PRCR register.

When Debug level of the MCU is DBG2, by guarding entire EPPB bus, the non-secure access from CPU to debug related components is completely controlled by the current value of the CPUDSA0 bit. Since this bit is modifiable only when CPU is in secure state, user must be aware of the CPUDSAR register before using Coresight debug components.

CPUDSA0 bit (CPU Debug Security Attribution 0)

Security attributes of register for accessing the debug component of the CPU.

0: Debug component can only be accessed with secure access.

1: There is no restriction on accessing the debug component.

2.7.7 Processing on Error response generated by CPU access

In addition to the specific-error detection specification of the Arm Cortex-M33 processor, this MCU also provides additional error information which is described in section 14, Buses.

Table 2.15 OCDREGCoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	0x8000_0FD0	32 bits	R	0x00000004
PID5	0x8000_0FD4	32 bits	R	0x00000000
PID6	0x8000_0FD8	32 bits	R	0x00000000
PID7	0x8000_0FDC	32 bits	R	0x00000000
PID0	0x8000_0FE0	32 bits	R	0x00000004
PID1	0x8000_0FE4	32 bits	R	0x00000030
PID2	0x8000_0FE8	32 bits	R	0x0000000A
PID3	0x8000_0FEC	32 bits	R	0x00000000
CID0	0x8000_0FF0	32 bits	R	0x0000000D
CID1	0x8000_0FF4	32 bits	R	0x000000F0
CID2	0x8000_0FF8	32 bits	R	0x00000005
CID3	0x8000_0FFC	32 bits	R	0x000000B1

2.7.6 CPUDSAR:CPU调试安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUDSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	CPUDSA0	CPU调试安全属性0 0: Secure 1: Non-secure	R/W
31:1	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问。拒绝非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

当MCU的Debug级别为DBG2时，通过保护整个EPPB总线，CPU对调试相关组件的非安全访问完全由CPUDSA0位的当前值控制。由于该位仅在CPU处于安全状态时才可修改，因此用户在使用Coresight调试组件之前必须了解CPUDSAR寄存器。

CPUDSA0位（CPU调试安全属性0）

用于访问CPU调试组件的寄存器的安全属性。

0：只能通过安全访问访问调试组件。

1：对调试组件的访问没有限制。

2.7.7 CPU访问产生的错误响应的处理

除了ArmCortex-M33处理器的特定错误检测规范外，此MCU还提供第14节“总线”中描述的其他错误信息。

This section describes how to handle the additional error information with no conflict to that of the Arm Cortex-M33 processor.

Table 2.16 shows error detection modules, which are also described in section 14, Buses. These error detection modules not only provide error information on the bus module, but also notify the processor to trigger the exception handler.

Table 2.16

	NMI/RESET request	Interrupt	Bus error status register	Error address register Error RW register
Slave TZF	NMISR.TZFST	Bus Fault*1 (Hard Fault)	BUS.BUSnERRSTAT. STERRSTAT	BUS.BTZFnERRADD BUS.BTZFnERRRW
Slave bus error	—	Bus Fault	BUS.BUSnERRSTAT. SLERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW
Illegal address access error	—	Bus Fault	BUS.BUSnERRSTAT.ILERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW

Note 1. A Bus Fault can be treated as HardFault. *ARM® Cortex®-M33 Device Generic User Guide* in the References section 2.14. References

To prevent unexpected operation, when handling the exception, additional operation should be added into exception routing.

BusFault when occurred by error detected as shown in Table 2.16:

- See section 14, Buses for the error information in the corresponding register
- Clear the data in cache for the error address
- Clear the Error Status register in the bus module
- Service exception handling with Arm-guided operation

For a Bus Fault that is not detected in the Renesas-specific error detection module (occurred inside the Arm Cortex-M33 core), see the *ARM® Cortex®-M33 Device Generic User Guide* to handle this case.

In the system bus specification, there is a specific case for Slave TrustZone Filter, that is, if an error is selected to generate an NMI, then before the processor handles the Bus Fault exception, NMI with higher priority takes the exception first. Therefore, use the BusFault handler and not NMI handler to handle this error. In other words, the NMI status should be cleared but the error status bit should not be cleared to ensure that BusFault captures all the error information.

Figure 2.4 and Figure 2.5 show the recommended flows for NMI handler and BusFault handler for the errors described in Table 2.16.

本节介绍如何处理与ArmCortex-M33处理器不冲突的附加错误信息。

表2.16显示了错误检测模块，这些模块也在第14节"总线"中进行了描述。这些错误检测模块不仅提供总线模块上的错误信息，还通知处理器触发异常处理程序。

Table 2.16

	NMI/RESET request	Interrupt	总线错误状态寄存器	错误地址寄存器 错误RW寄存器
Slave TZF	NMISR.TZFST	总线故障*1 (Hard Fault)	BUS.BUSnERRSTAT. STERRSTAT	BUS.BTZFnERRADD BUS.BTZFnERRRW
从站总线错误	—	总线故障	BUS.BUSnERRSTAT. SLERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW
非法地址访问错误	—	总线故障	BUS.BUSnERRSTAT.ILERRSTAT	BUS.BUSnERRADD BUS.BUSnERRRW

注1.总线故障可被视为硬故障。参考第2.14节中的ARM®Cortex®-M33设备通用用户指南。
References

为防止意外操作，在处理异常时，应在异常路由中增加额外的操作。

检测到错误发生时的BusFault，如表2.16所示：

- ●相应寄存器中的错误信息见第14节，总线
- ●清除缓存中错误地址的数据
- ●清除总线模块中的错误状态寄存器
- ●服务异常处理，手臂引导操作

对于未在Renesas特定错误检测模块中检测到的总线故障（发生在ArmCortex-M33内核中），请参阅ARM®Cortex®-M33DeviceGenericUserGuide来处理这种情况。

在系统总线规范中，SlaveTrustZoneFilter有一个特定的情况，即如果选择了错误产生NMI，那么在处理器处理BusFault异常之前，优先级较高的NMI先处理该异常。因此，使用BusFault处理程序而不是NMI处理程序来处理此错误。换言之，应清除NMI状态但不应清除错误状态位，以确保BusFault捕获所有错误信息。

图2.4和图2.5显示了NMI处理程序和BusFault处理程序的推荐流程，用于处理中描述的错误
Table 2.16.

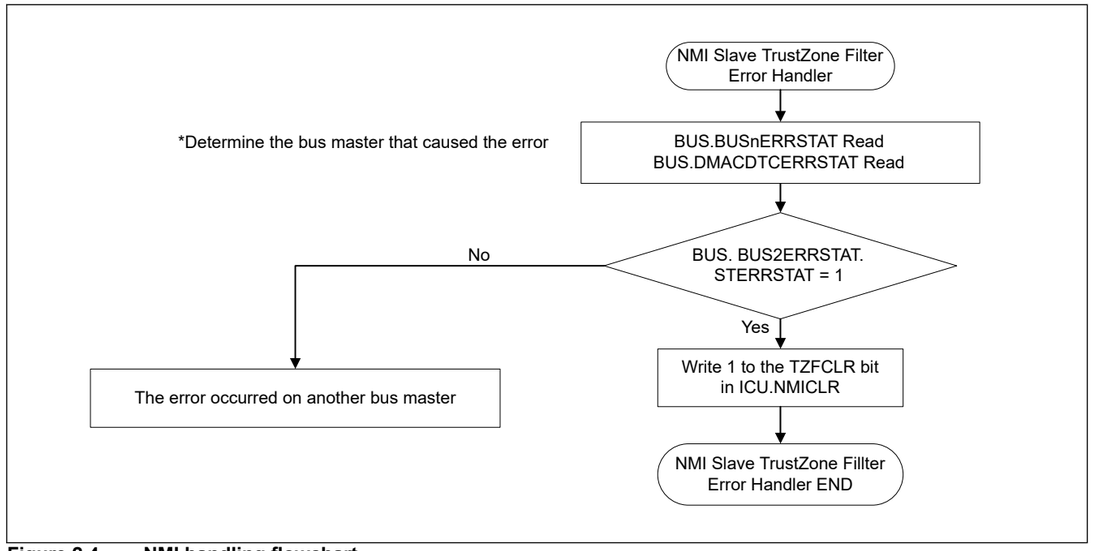


Figure 2.4 NMI handling flowchart

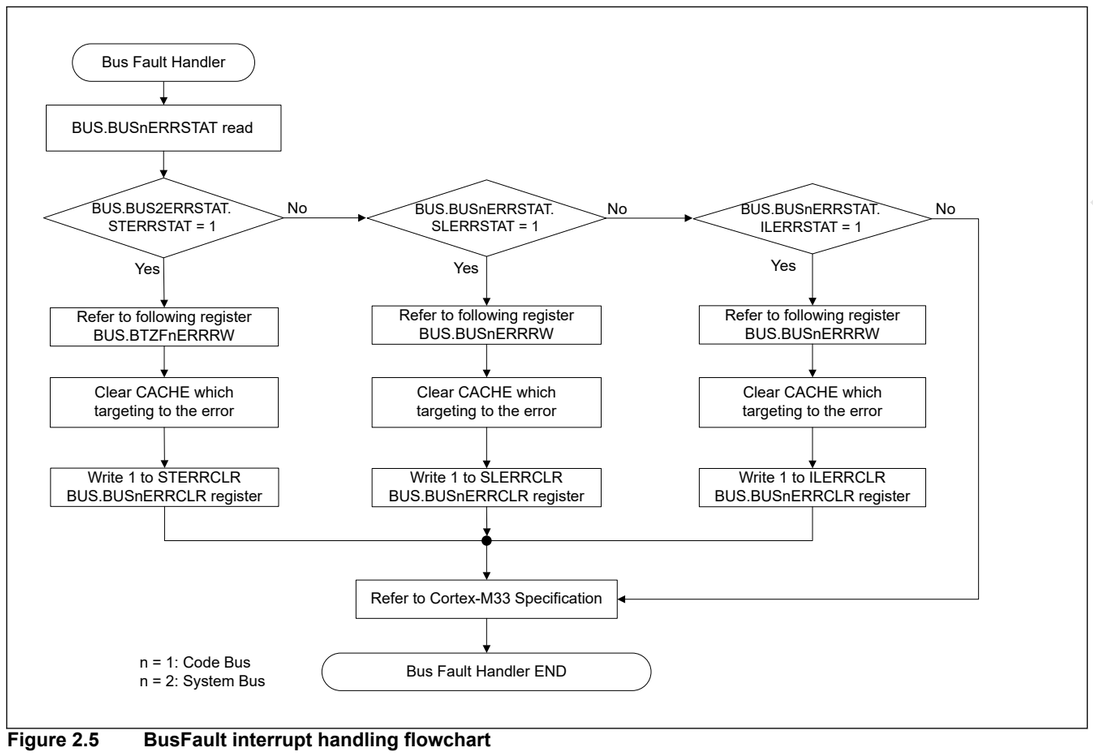


Figure 2.5 BusFault interrupt handling flowchart

2.8 CoreSight Cross Trigger Interface (CTI)

As shown in Figure 2.6, the input and output of a Cross Trigger Interface (CTI) interact with each other through four CTM channels. Input of a CTI can be used to trigger the output of another CTI using the four CTM channels.

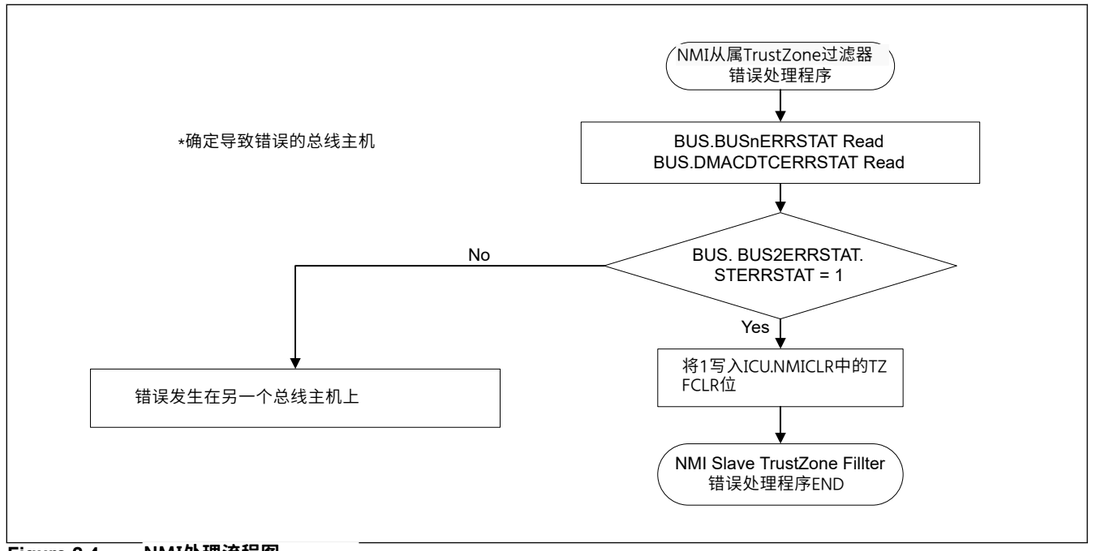


Figure 2.4 NMI处理流程图

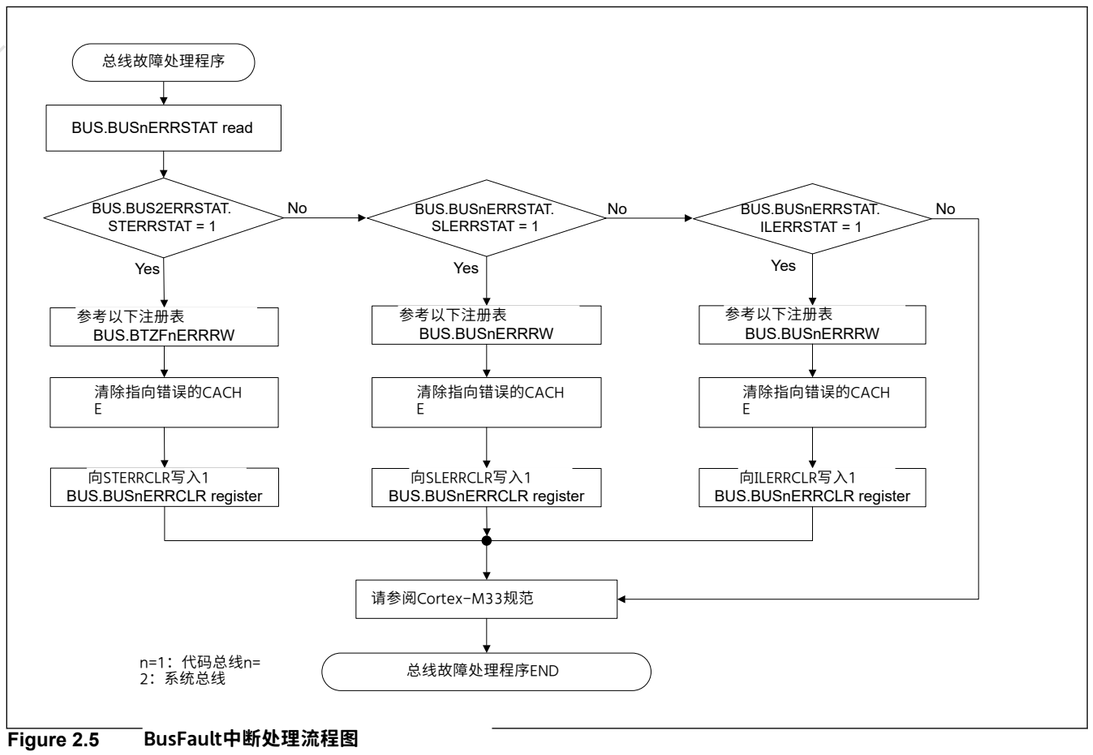


Figure 2.5 BusFault中断处理流程图

2.8 CoreSight交叉触发接口(CTI)

如图2.6所示，交叉触发接口（CTI）的输入和输出通过四个CTM通道相互交互。一个CTI的输入可用于使用四个CTM通道触发另一个CTI的输出。

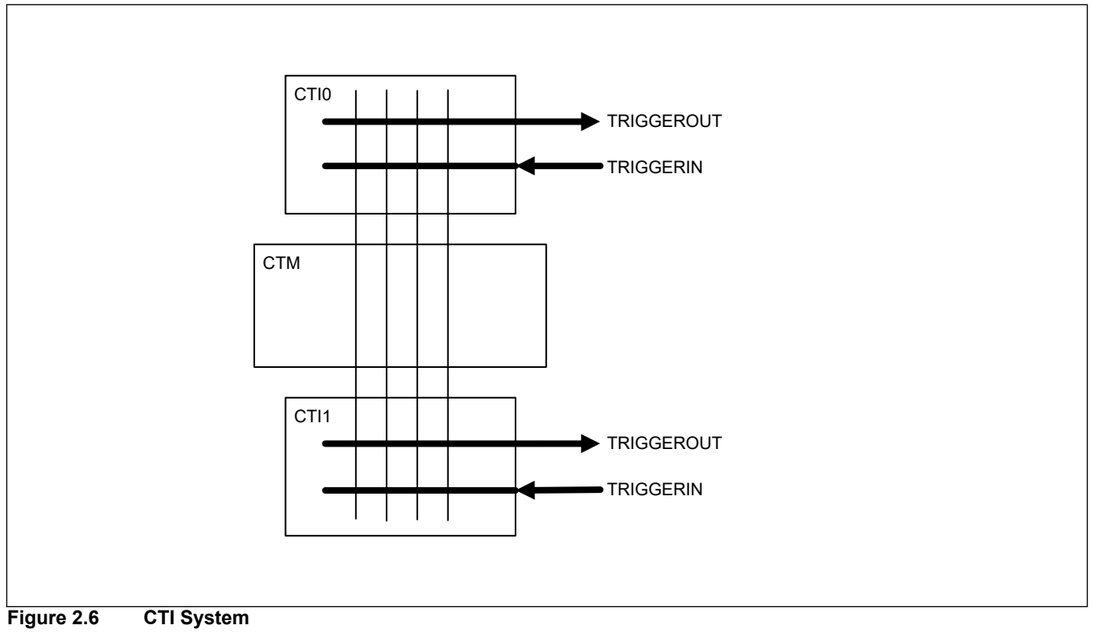


Figure 2.6 CTI System

Debug Interrupt Request (DBGIRQ) is controlled by MCUCTRL register in OCDREG module.

Table 2.17 CTI Trigger signals

Number of CTI channel	CTITRIGIN		CTITRIGOUT	
CTI0 (Debug common)	0	ACQCOMP	0	—
	1	FULL	1	—
	2	DBIRQ	2	ETB FLUSHIN
	3	—	3	ETB TRIGIN
	4	—	4	—
	5	—	5	—
	6	—	6	—
	7	—	7	—
CTI1 (CPU)	0	Processor Halted	0	Processor debug request
	1	DWT Comparator Output 0	1	Processor Restart
	2	DWT Comparator Output 1	2	CTIIRQ[0] (Connected to IRQ96)
	3	DWT Comparator Output 2	3	CTIIRQ[1] (Connected to IRQ97)
	4	ETM Event Output 0	4	ETM Event Input 0
	5	ETM Event Output 1	5	ETM Event Input 1
	6	—	6	ETM Event Input 2
	7	—	7	ETM Event Input 3

2.9 CoreSight ATB Funnel

There is one CoreSight ATB funnel in the MCU. The funnel has two ATB slaves and one ATB master, and it selects the debug trace source from ETM and ITM to ETB. Figure 2.7 shows the CoreSight ATB connection in the MCU.

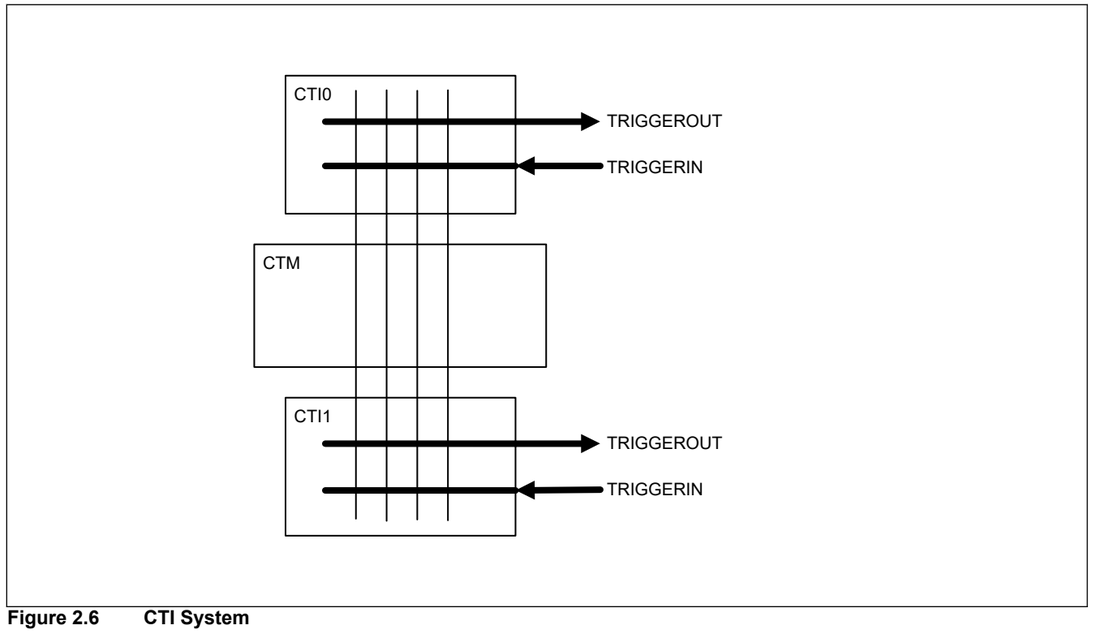


Figure 2.6 CTI System

调试中断请求(DBGIRQ)由OCDREG模块中的MCUCTRL寄存器控制。

Table 2.17 CTI触发信号

CTI通道数	CTITRIGIN		CTITRIGOUT	
CTI0 (Debug common)	0	ACQCOMP	0	—
	1	FULL	1	—
	2	DBIRQ	2	ETB FLUSHIN
	3	—	3	ETB TRIGIN
	4	—	4	—
	5	—	5	—
	6	—	6	—
	7	—	7	—
CTI1 (CPU)	0	处理器停止	0	处理器调试请求
	1	DWT比较器输出0	1	处理器重启
	2	DWT比较器输出1	2	CTIIRQ[0] (Connected to IRQ96)
	3	DWT比较器输出2	3	CTIIRQ[1] (Connected to IRQ97)
	4	ETM事件输出0	4	ETM事件输入0
	5	ETM事件输出1	5	ETM事件输入1
	6	—	6	ETM事件输入2
	7	—	7	ETM事件输入3

2.9 CoreSight ATB Funnel

MCU中有一个CoreSightATB漏斗。漏斗有两个ATB从站和一个ATB主站，它选择从ETM和ITM到ETB的调试跟踪源。图2.7显示了MCU中的CoreSightATB连接。

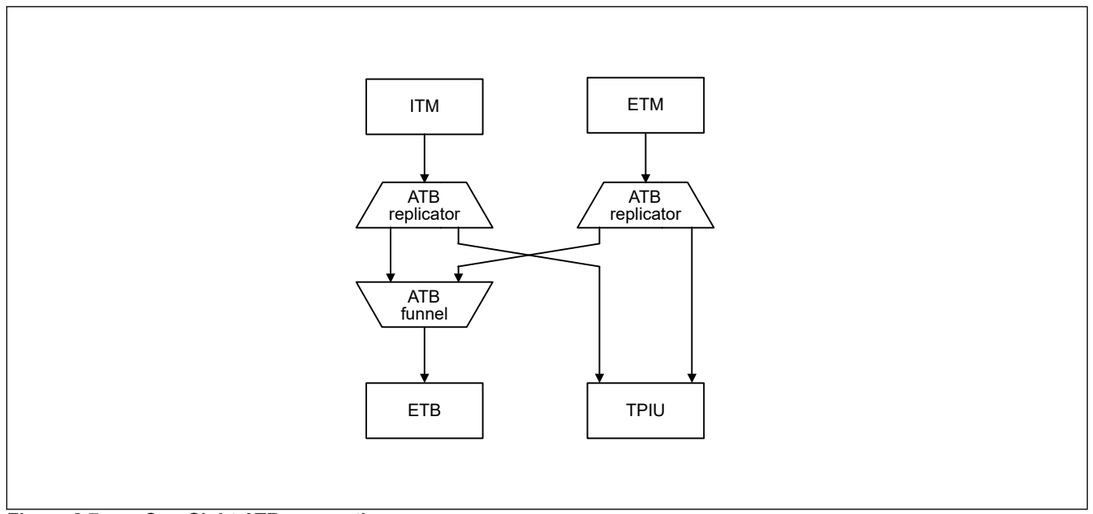


Figure 2.7 CoreSight ATB connection

Table 2.18 shows the ATB slave connection for the funnel.

Table 2.18 ATB slave connection

ATB slave number	Connected trace source
#0	ITM
#1	ETM

See reference 4. in section 2.14. References for details of the ATB and funnel.

2.10 Break Point Unit

The MCU has Break Point Unit. See BreakPoint unit chapter of reference 1. in section 2.14. References for details about register description of this module.

2.11 CoreSight Time Stamp Generator

A CoreSight Time Stamp Generator provides a CPU clock-based timestamp to ITM and ETM.The timestamp is generated by a 64-bit counter. See reference 4. in section 2.14. References for details.

2.12 SysTick Timer

The MCU has SysTick timer that provides two 24-bit down counters, non-secure and secure counters. The timer can select SysTick timer clock (SYSTICCLK) or System clock (ICLK).

See section 8, Clock Generation Circuit and reference 1. in section 2.14. References for details.

Note: SysTick timer counter operation is enabled by signal synchronized with CPU clock. Therefore, the counter might not operate correctly if the CPU clock is slower than the SysTick timer clock. In other words, clock setting must satisfy the following: CPU clock ≥ Systick clock (LOCO: 32.768 kHz).

2.13 OCD Emulator Connection

In this product, the MCU confirms the access permission for Non-secure debug and Non-secure chip resources by checking Debug level is DBG1 or higher. For full access permission for debug and chip resources, Secure debug level DBG2 is required.

Figure 2.8 shows a block diagram of SWD authentication mechanism.

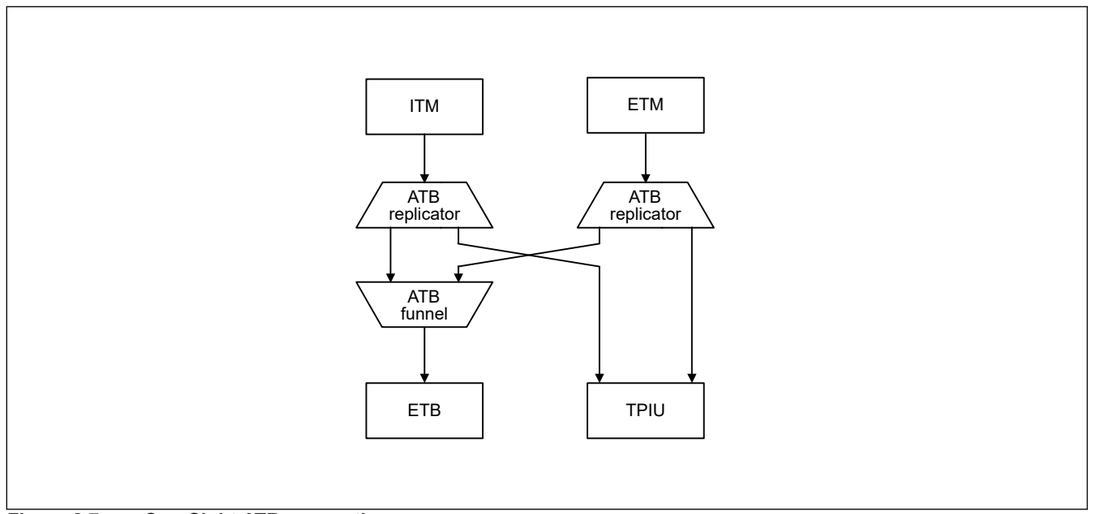


Figure 2.7 CoreSight ATB connection

表2.18显示了漏斗的ATB从属连接。

Table 2.18 ATB从机连接

ATB从机号	连接的跟踪源
#0	ITM
#1	ETM

参见第2.14节中的参考4。有关ATB和漏斗详细信息的参考资料。

2.10 断点单元

MCU有断点单元。请参阅第2.14节中参考文献1.的断点单元章节。关于该模块的寄存器描述的详细信息参考。

2.11 CoreSight时间戳生成器

CoreSight时间戳生成器为ITM和ETM提供基于CPU时钟的时间戳。时间戳由64位计数器生成。参见第2.14节中的参考4。详情参考。

2.12 SysTick Timer

MCU具有SysTick定时器，提供两个24位递减计数器、非安全计数器和安全计数器。定时器可以选择SysTick定时器时钟(SYSTICCLK)或系统时钟(ICLK)。

请参见第8节，时钟生成电路和第2.14节中的参考1。详情参考。

Note: SysTick定时器计数器操作由与CPU时钟同步的信号启用。因此，如果CPU时钟比SysTick定时器时钟慢，计数器可能无法正确运行。换言之，时钟设置必须满足以下条件：CPU时钟≥Systick时钟（LOCO：32.768kHz）。

2.13 OCD模拟器连接

本产品中，MCU通过勾选确认非安全调试和非安全芯片资源的访问权限
调试级别为DBG1或更高。对于调试和芯片资源的完全访问权限，需要安全调试级别DBG2。

图2.8显示了SWD认证机制的框图。

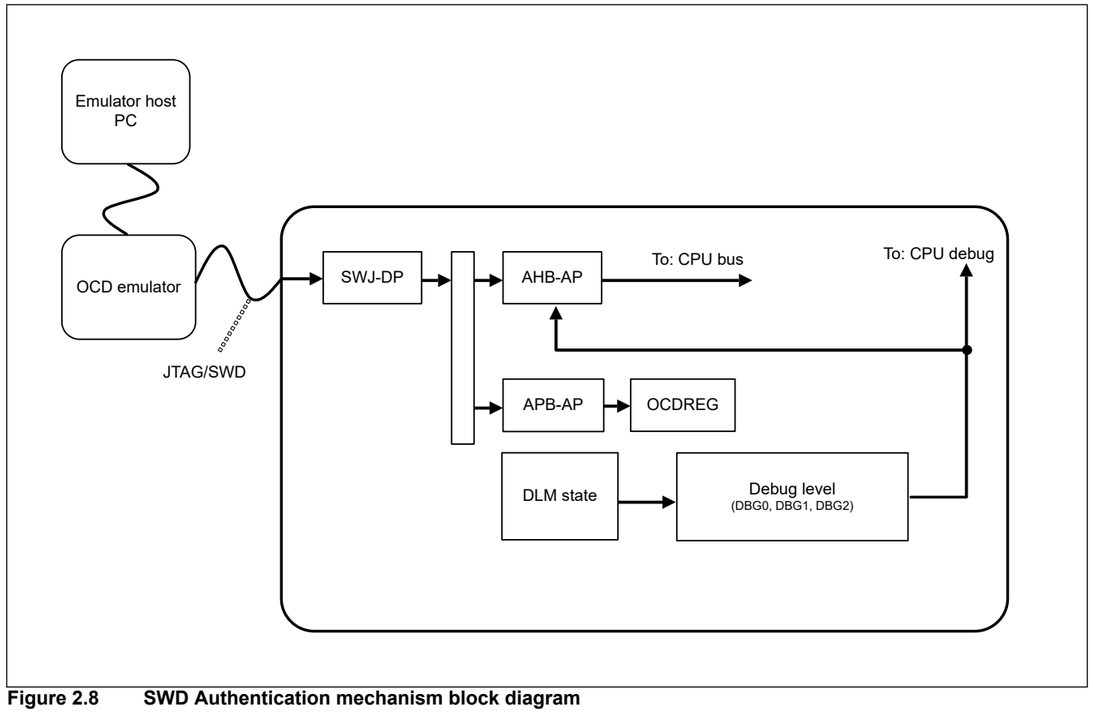


Figure 2.8 SWD Authentication mechanism block diagram

Three levels of debug capability are available, DBG0, DBG1, and DBG2, which correspond to the Device Level Management (DLM) states. When debug level is DBG0, access to debug components and system bus from OCD emulator is not permitted. When debug level is DBG1 or DBG2, the corresponding non-secure or secure debug components and system bus can be accessed from the OCD emulator. See Table 2.5 for more information about debug levels.

2.13.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 10, Low Power Modes for details.

2.13.2 Restrictions on Connecting an OCD emulator

This section describes the restrictions on emulator access.

2.13.2.1 Starting connection while in low power mode

When starting a JTAG/SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby, Snooze, or Deep Software Standby mode, the OCD emulator can cause the MCU to hang.

2.13.2.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby, Snooze or Deep Software Standby mode. Only SWJ-DP, APB-AP, and OCDREG can be accessed from the OCD emulator in these modes. Table 2.19 shows the restrictions.

Table 2.19 Restrictions by mode (1 of 2)

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes

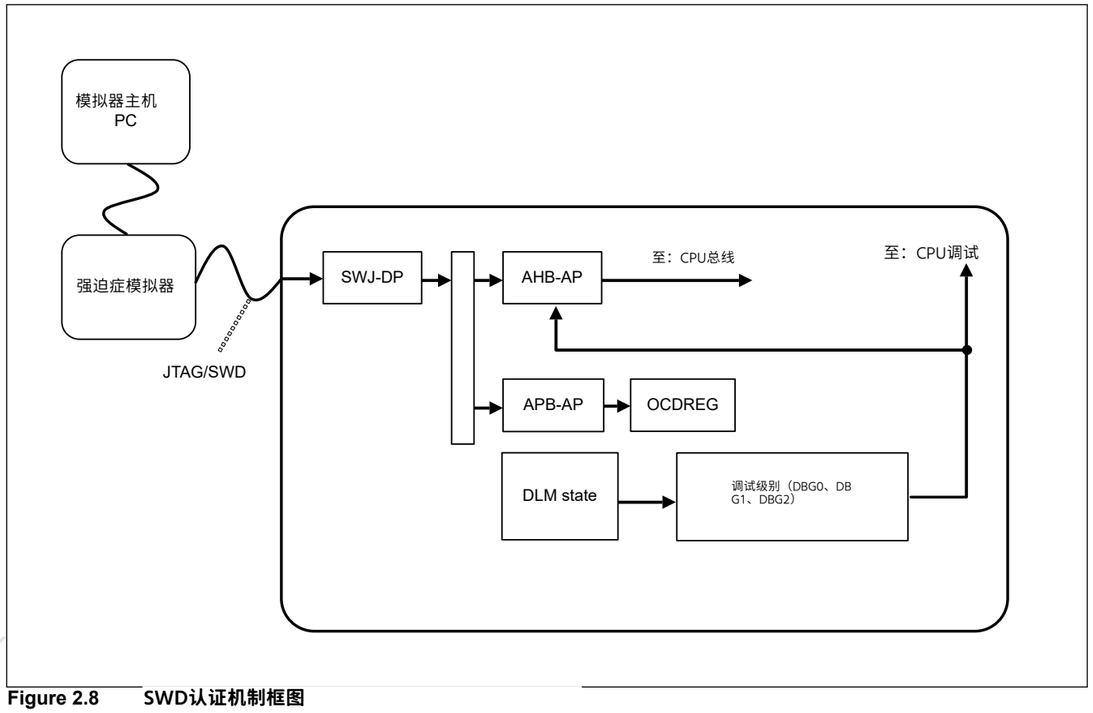


Figure 2.8 SWD认证机制框图

提供三个级别的调试能力，DBG0、DBG1和DBG2，它们对应于DeviceLevel管理(DLM)状态。当调试级别为DBG0时，不允许从OCD仿真器访问调试组件和系统总线。当调试级别为DBG1或DBG2时，可以从OCD仿真器访问相应的非安全或安全调试组件和系统总线。有关调试级别的更多信息，请参见表2.5。

2.13.1 DBGEN

OCD模拟器获得访问权限后，OCD模拟器必须设置SystemControlOCD中的DBGEN位控制寄存器(SYOCDCR)。此外，OCD仿真器必须在断开连接之前清除DBGEN位。有关详细信息，请参见第10节，低功耗模式。

2.13.2 连接强迫症模拟器的限制

本节介绍对仿真器访问的限制。

2.13.2.1 在低功耗模式下开始连接

从OCD仿真器启动JTAGSWD连接时，MCU必须处于正常或睡眠模式。如果MCU处于软件待机、贪睡或深度软件待机模式，OCD仿真器可能会导致MCU挂起。

2.13.2.2 在OCD模式下更改低功耗模式

当MCU处于OCD模式时，可以更改低功耗模式。但是，在软件待机、贪睡或深度软件待机模式下，禁止从AHB-AP访问系统总线。在这些模式下，只能从OCD仿真器访问SWJ-DP、APB-AP和OCDREG。表2.19显示了这些限制。

Table 2.19 模式限制(1of2)

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Normal	Yes	Yes	Yes	Yes

Table 2.19 Restrictions by mode (2 of 2)

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
Deep Software Standby	No	Yes	No	Yes

If system bus access is required in Software Standby, Snooze, or Deep Software Standby mode, set the MCUCTRL.DBIRQ bit in OCDREG to wake up the MCU from the low power modes. Simultaneously, by asserting the MCUCTRL.DBIRQ bit in OCDREG, the OCD emulator can wake up the MCU without starting CPU execution by using a CPU break.

2.13.2.3 Connecting sequence and JTAG/SWD authentication

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access DAP bus.
   In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP.
   Control Status Register, and then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. This APB-AP is connected to DAP bus port 1.
4. Set MCUCTRL.CPUWAIT = 1.
5. Confirm the debug capability of device by reading MCUSTAT:
   - If Debug function is prohibited, this device is not able to debug.
   - If Debug function is enabled and secure debug is not available, only non-secure debug is available.
   - If Debug function is enabled and secure debug is available, full debug functions are available.

   If Debug function is available, set debug-related register then clear MCUCTRL.CPUWAIT = 0.
6. Set up the AHB-AP to access the system address space. The AHB-AP is connected to DAP bus port 0.
7. Set SYOCDCR.DBGEN to 1.
8. Start accessing the CPU debug resources using the AHB-AP.

Note: Debug level is determined by the current DLM state of product.

2.14 References

1. *ARM®v8-M Architecture Reference Manual* (ARM DDI 0553B.a)
2. *ARM® Cortex®-M33 Processor Technical Reference Manual* (ARM 100230)
3. *ARM® Cortex®-M33 Device Generic User Guide* (ARM 100235)
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480G)
5. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029E)

Table 2.19 模式限制(2of2)

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Sleep	Yes	Yes	Yes	Yes
软件待机	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
深度软件待机	No	Yes	No	Yes

如果在软件待机、贪睡或深度软件待机模式下需要系统总线访问，则设置OCDREG中的MCUCTRL.DBIRQ位以将MCU从低功耗模式中唤醒。同时，通过置位OCDREG中的MCUCTRL.DBIRQ位，OCD仿真器可以在不使用CPU中断启动CPU执行的情况下唤醒MCU。

2.13.2.3 连接顺序和JTAGSWD认证

1.通过JTAG或SWD接口将OCD调试器连接到MCU。

2.设置SWJ-DP访问DAP总线。
在设置中，OCD仿真器必须在SWJDP中声明CDBGPWRUPREQ。
控制状态寄存器，然后等待同一寄存器中的CSDBGPWRUPACK被断言。

3.将APB-AP设置为访问OCDREG。此APB-AP连接到DAP总线端口1。

4. Set MCUCTRL.CPUWAIT = 1.

5.通过读取MCUSTAT确认设备的调试能力：
●如果Debug功能被禁止，则本设备无法调试。
●如果启用了Debug功能且没有安全调试，则只能进行非安全调试。
●如果启用了Debug功能并且可以使用安全调试，则可以使用完整的调试功能。

如果Debug功能可用，设置调试相关寄存器然后清除MCUCTRL.CPUWAIT=0。

6.设置AHB-AP访问系统地址空间。AHB-AP连接到DAP总线端口0。

7.将SOOCDCR.DBGEN设置为1。

8.开始使用AHB-AP访问CPU调试资源。

Note: 调试级别由产品的当前DLM状态决定。

2.14 References

1.ARM®v8-M架构参考手册（ARMDDI0553B.a）

2.ARM®Cortex®-M33处理器技术参考手册（ARM100230）

3.ARM®Cortex®-M33设备通用用户指南(ARM100235)

4.ARM®CoreSight SoC-400技术参考手册（ARMDDI0480G）

5.ARM®CoreSight 架构规范（ARMIHI0029E）

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2. Details of Operating Modes. Operation starts with the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin (MD)	Operating mode	On-chip Flash	External bus
1	Single-chip mode	Enable	Disable
0	SCI / USB boot mode	Enable	Disable

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs.

When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI. For details, see section 50, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.2.3 USB Boot Mode

In this mode, the on-chip flash memory programming routine (USB boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using USB. For details, see section 50, Flash Memory. The MCU starts in USB boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Modes Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the MD pin settings.

3. 操作模式

3.1 Overview

表3.1显示了通过模式设置引脚选择的工作模式。有关详细信息，请参阅第3.2节。经营详情模式。无论操作以何种模式开始，操作都会从启用片上闪存开始。

Table 3.1 通过模式设置引脚选择工作模式

Mode-setting pin (MD)	操作模式	On-chip Flash	外部总线
1	Single-chip mode	Enable	Disable
0	SCIUSB启动模式	Enable	Disable

3.2 操作模式的详细信息

3.2.1 Single-Chip Mode

在单片机模式下，所有IO引脚都可用作输入或输出端口、外围功能的输入或输出，或用作中断输入。

当MD引脚为高电平时释放复位时，MCU以单芯片模式启动，并启用片上闪存。

3.2.2 SCI启动模式

在这种模式下，使用存储在MCU引导区域中的片上闪存编程例程（SCI引导程序）。片上闪存，包括代码闪存和数据闪存，可以通过使用通用异步接收发送器(UART)SCI从MCU外部进行修改。有关详细信息，请参阅第50节，闪存。如果MD引脚在从复位状态释放时保持低电平，则MCU以SCI启动模式启动。

3.2.3 USB启动模式

在这种模式下，使用存储在MCU引导区域中的片上闪存编程例程（USB引导程序）。片上闪存，包括代码闪存和数据闪存，可以通过USB从MCU外部进行修改。有关详细信息，请参阅第50节，闪存。如果MD引脚在从复位状态释放时保持低电平，则MCU在USB引导模式下启动。

3.3 操作模式转换

3.3.1 由模式设置引脚确定的操作模式转换

图3.1显示了由MD引脚设置确定的操作模式转换。

RA生态工作室

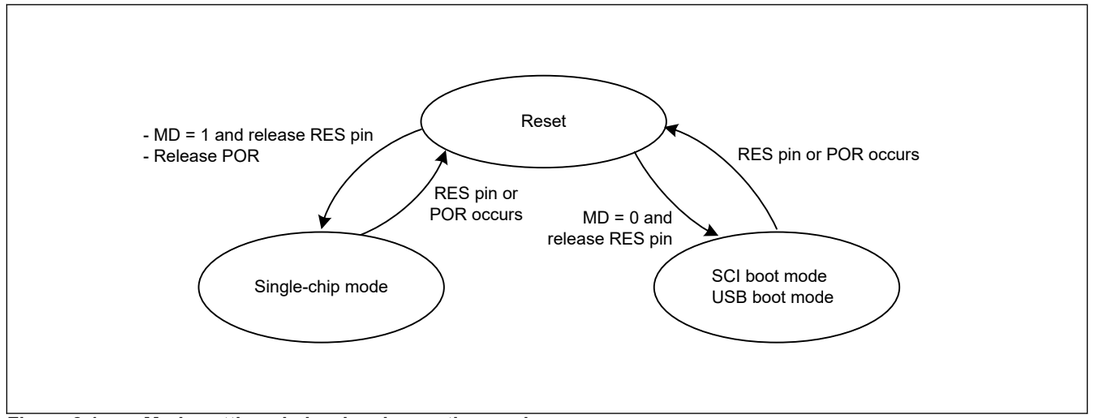


Figure 3.1 Mode-setting pin level and operating mode

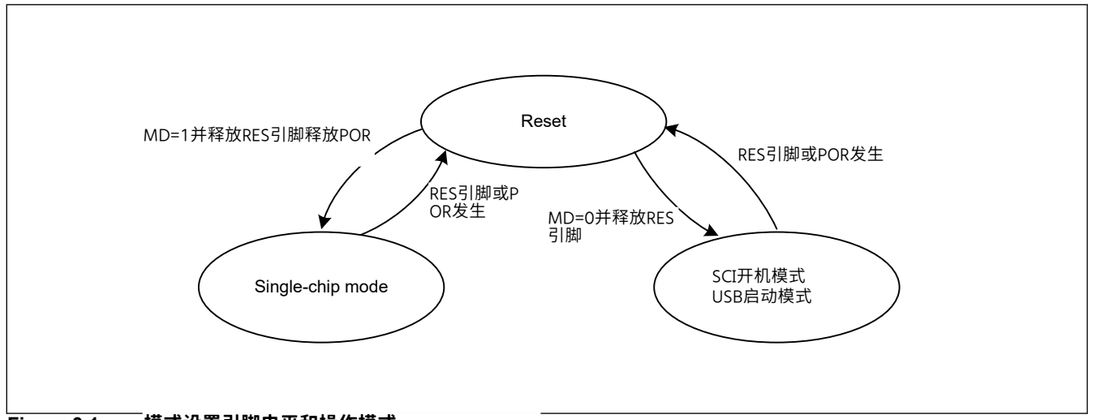


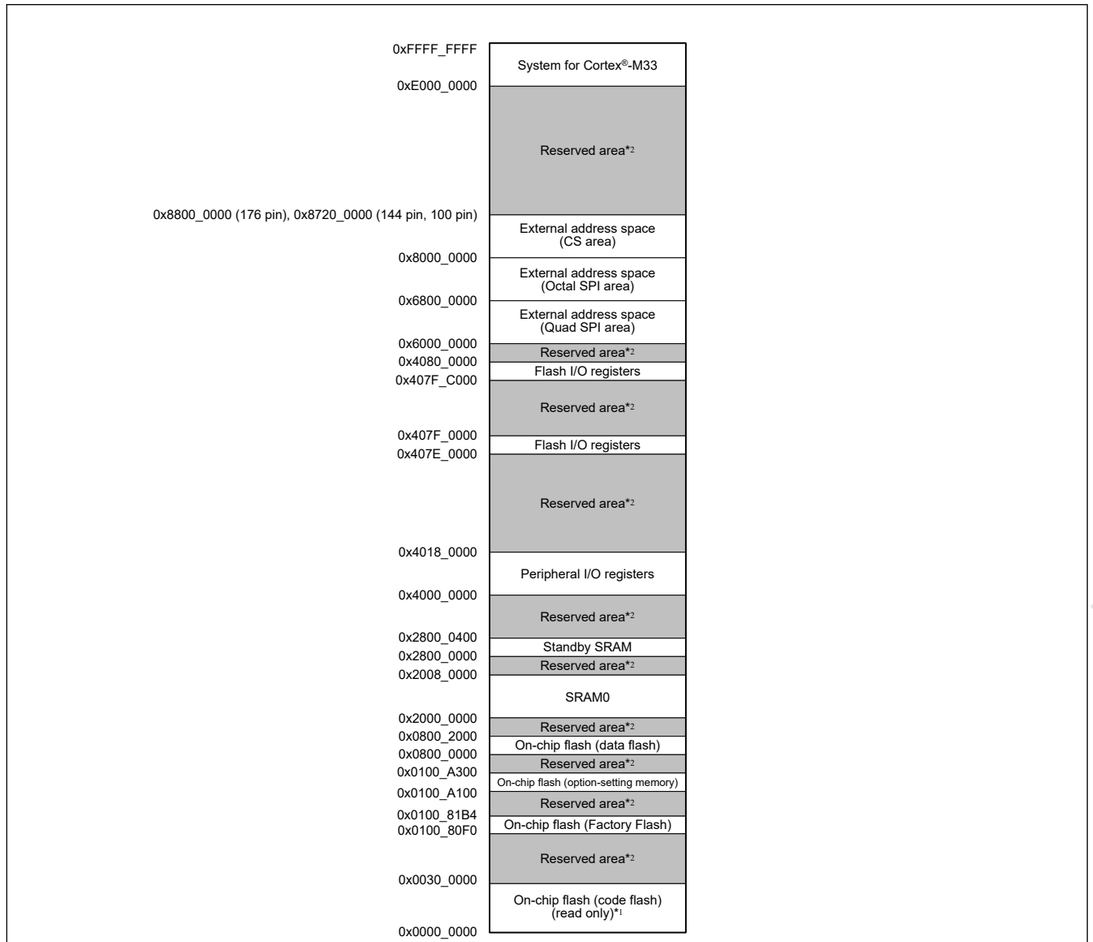
Figure 3.1 模式设置引脚电平和操作模式

RA生态工作室

4. Address Space

4.1 Address Space

The MCU supports a 4-GB linear address space ranging from 0x0000_0000 to 0xFFFF_FFFF that can contain both program and data. Figure 4.1 shows the memory map.



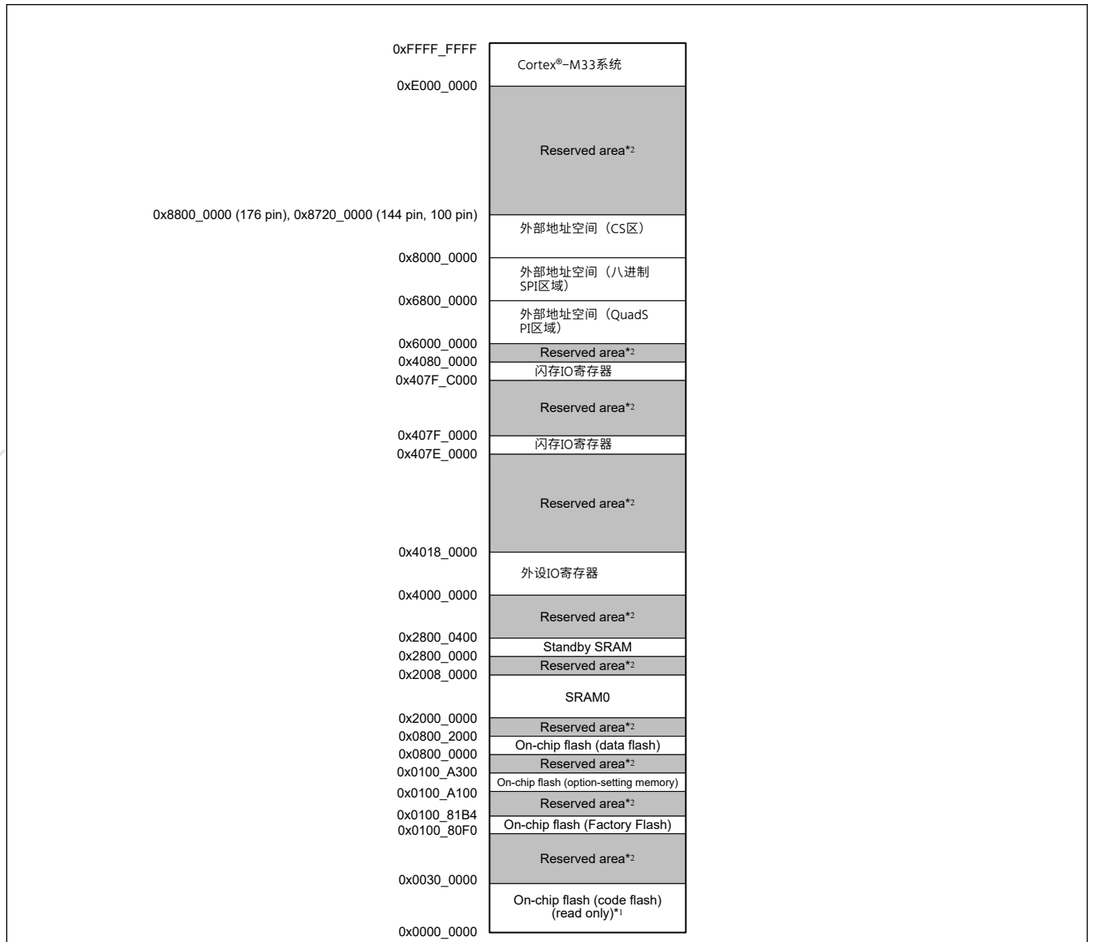
Note 1. See Table 4.1. The capacity of the flash differs depending on the product.
Note 2. Do not access reserved areas.

Figure 4.1 Memory map

4. 地址空间

4.1 地址空间

MCU支持4-GB线性地址空间，范围从0x0000_0000到0xFFFF_FFFF，可以同时包含程序和数据。图4.1显示了内存映射。



注1.见表4.1。闪光灯的容量因产品而异。
注2.请勿进入保留区域。

Figure 4.1 内存映射

Table 4.1 Capacity of the code flash memory, data flash memory, and SRAM0

Code flash memory			Data flash memory		SRAM0	
Capacity	Address		Capacity	Address	Capacity	Address
	Linear mode	Dual mode (BANKSEL.BANKSWP[2:0] = 111b)				
2 MB	0x0000_0000 - 0x001F_FFFF	Upper side bank: 0x0020_0000 - 0x002F_FFFF	8 KB	0x0800_0000 - 0x0800_1FFF	512 KB	0x2000_0000 - 0x2007_FFFF
		Lower side bank: 0x0000_0000 - 0x000F_FFFF				
1 MB	0x0000_0000 - 0x000F_FFFF	Upper side bank: 0x0020_0000 - 0x0027_FFFF				
		Lower side bank: 0x0000_0000 - 0x0007_FFFF				

4.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7), Octal SPI area (CS0 and CS1), and Quad SPI area. The eight CS areas (CS0 to CS7) each correspond to the CSn signal output from a CSn (n = 0 to 7) pin. The two Octal SPI areas (CS0 and CS1) each correspond to the OM_CSn signal output from a OM_CSn (n = 0, 1) pin. The Quad SPI area is divided into two areas, QSPI I/O registers and external SPI device space.

Figure 4.2 shows the address ranges associated with the individual CS areas (CS0 to CS7), Octal SPI area (CS0 and CS1), and Quad SPI area.

Table 4.1 代码闪存、数据闪存和SRAM0的容量

代码闪存			数据闪存		SRAM0	
Capacity	Address		Capacity	Address	Capacity	Address
	线性模式	双模式（BANKSEL.BANKSWP[2:0]=111b）				
2 MB	0x0000_0000 - 0x001F_FFFF	上侧银行：0x0020_00000x002F_FFFF	8 KB	0x0800_0000 - 0x0800_1FFF	512 KB	0x2000_0000 - 0x2007_FFFF
		下侧银行：0x0000_00000x000F_FFFF				
1 MB	0x0000_0000 - 0x000F_FFFF	上边银行：0x0020_00000x0027_FFFF				
		下侧银行：0x0000_00000x0007_FFFF				

4.2 外部地址空间

外部地址空间分为CS区（CS0到CS7）、八进制SPI区（CS0和CS1）和四线SPI区。8个CS区域（CS0至CS7）分别对应于从CSn（n=0至7）引脚输出的CSn信号。两个八进制SPI区域（CS0和CS1）分别对应于从OM_CSn(n=0 1）引脚输出的OM_CSn信号。QuadSPI区域分为两个区域，QSPIIO寄存器和外部SPI设备空间。

图4.2显示了与各个CS区域（CS0到CS7）、八进制SPI区域（CS0和CS1）和四路SPI区域相关的地址范围。

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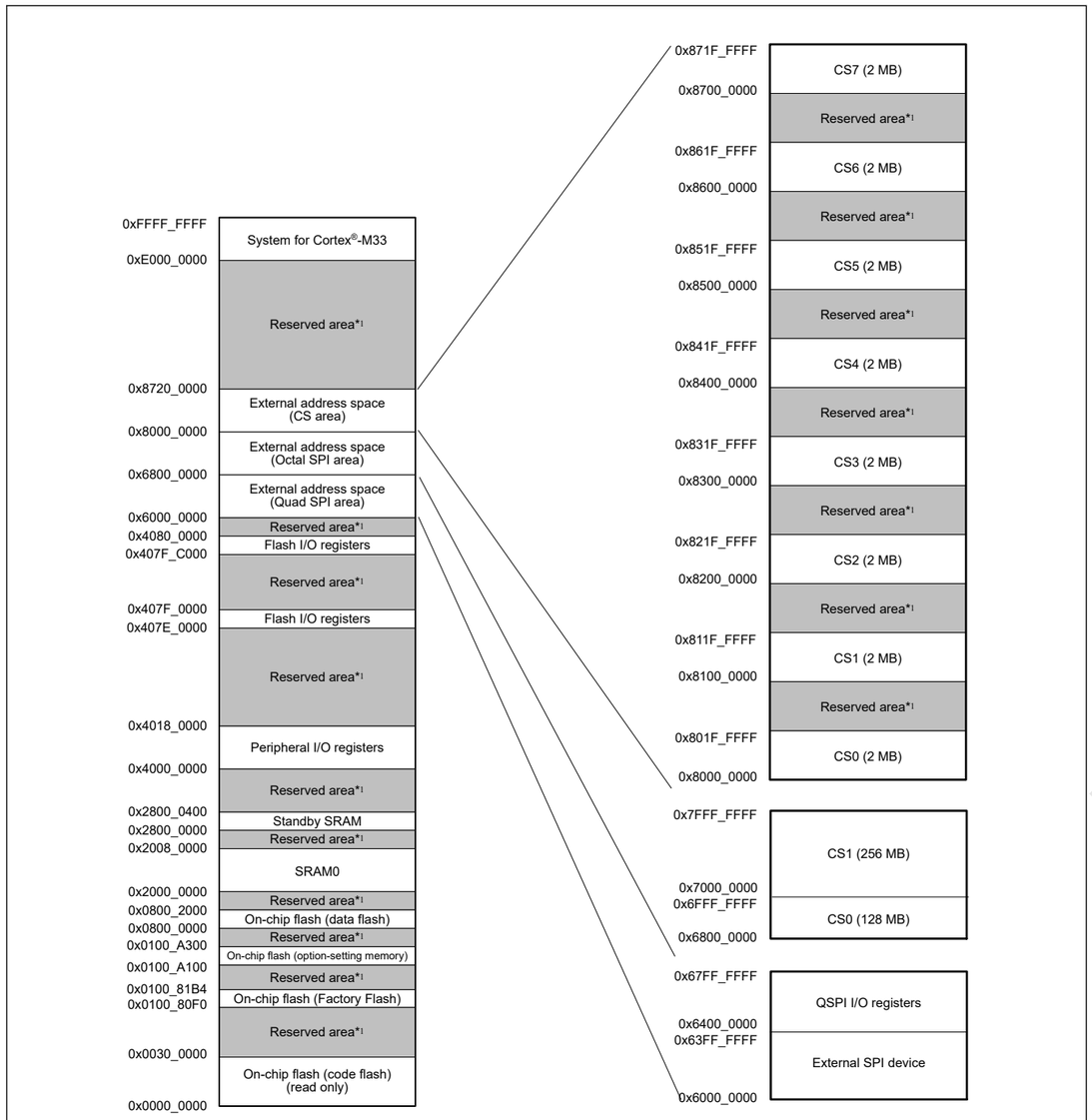
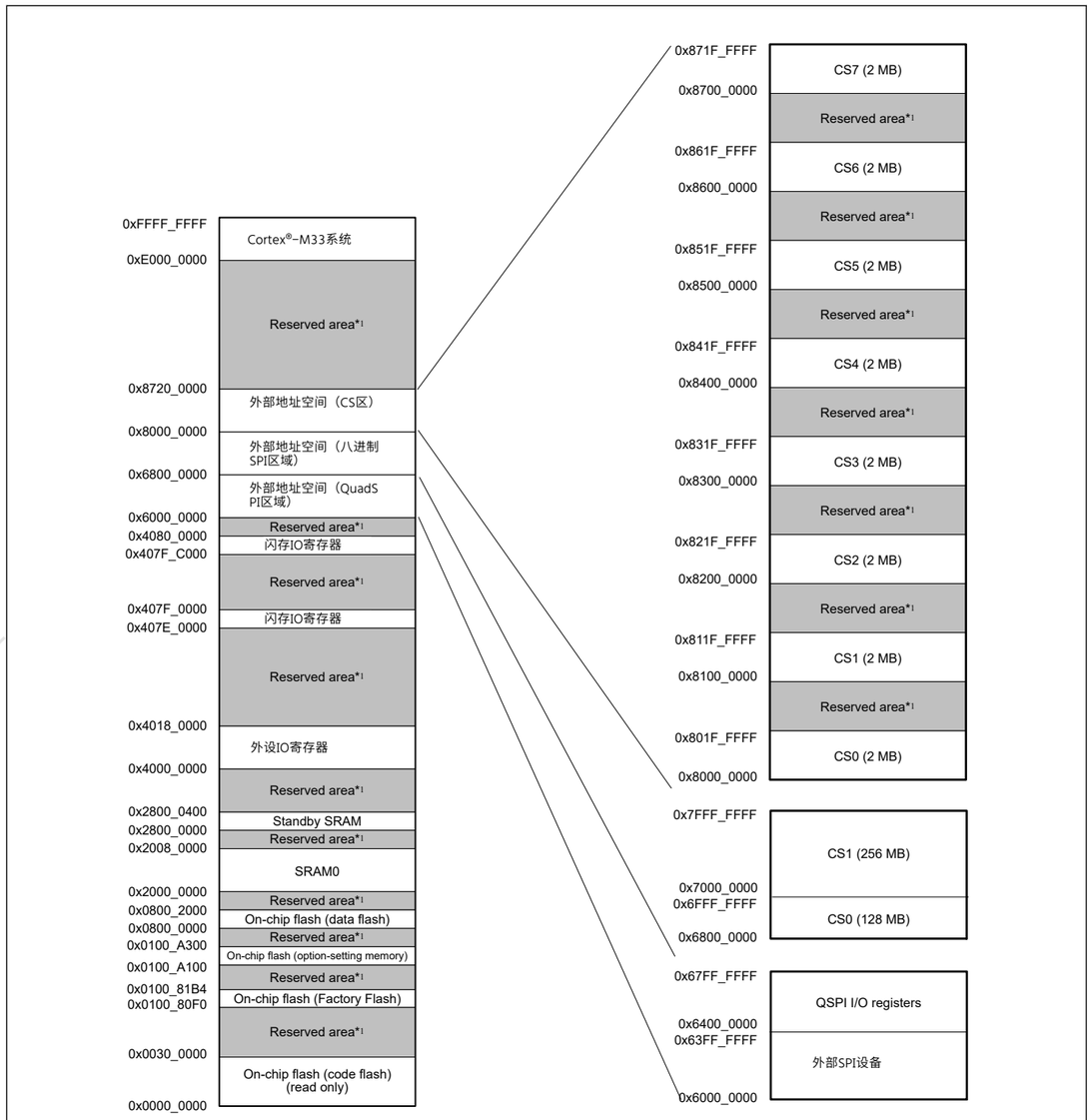


Note 1. Do not access reserved areas.

Figure 4.2 Association between external address spaces (144 pin, 100 pin)



注1.请勿进入保留区域。

Figure 4.2 外部地址空间之间的关联（144针、100针）

RA生态工作室

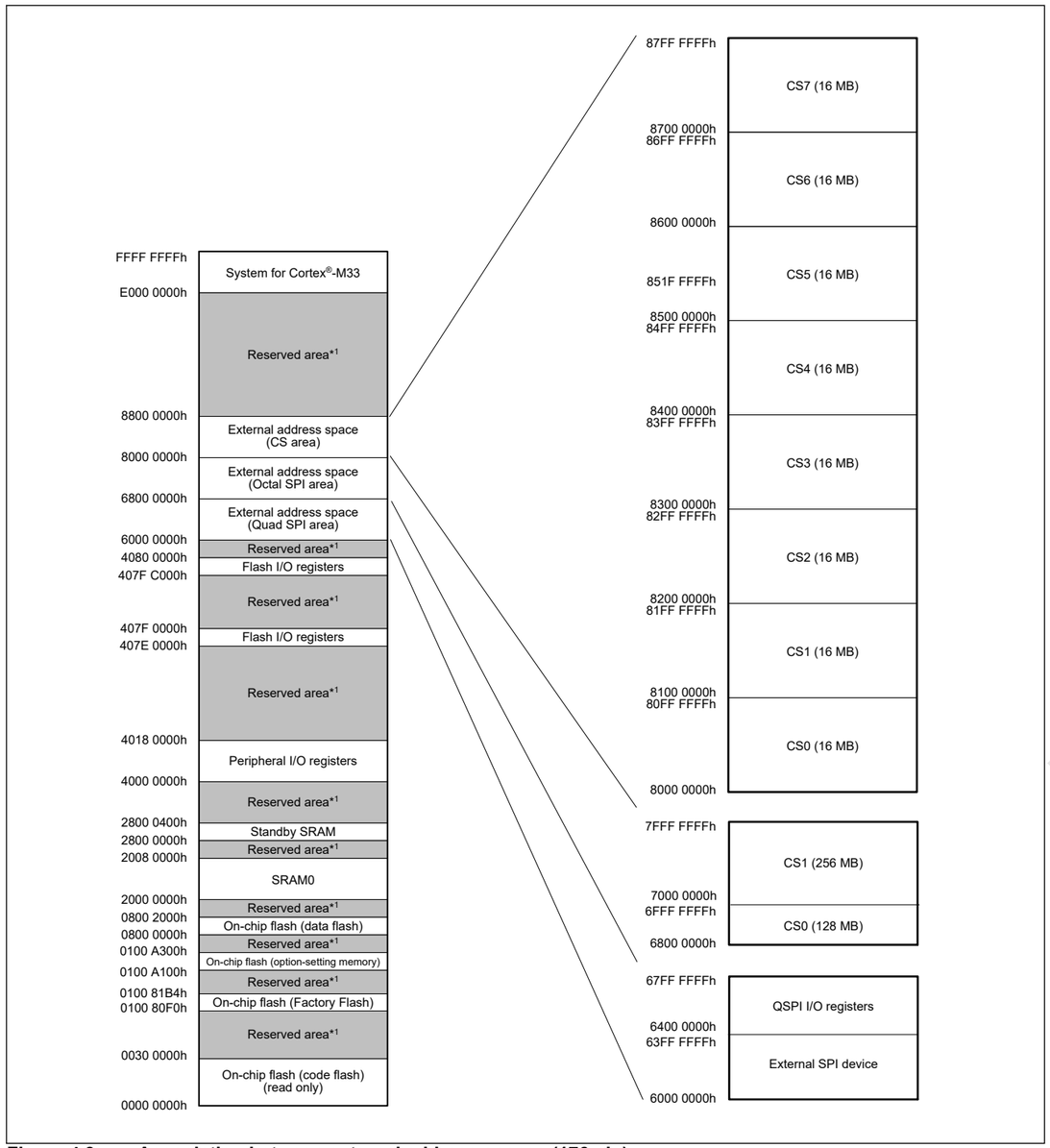


Figure 4.3 Association between external address spaces (176 pin)

RA生态工作室

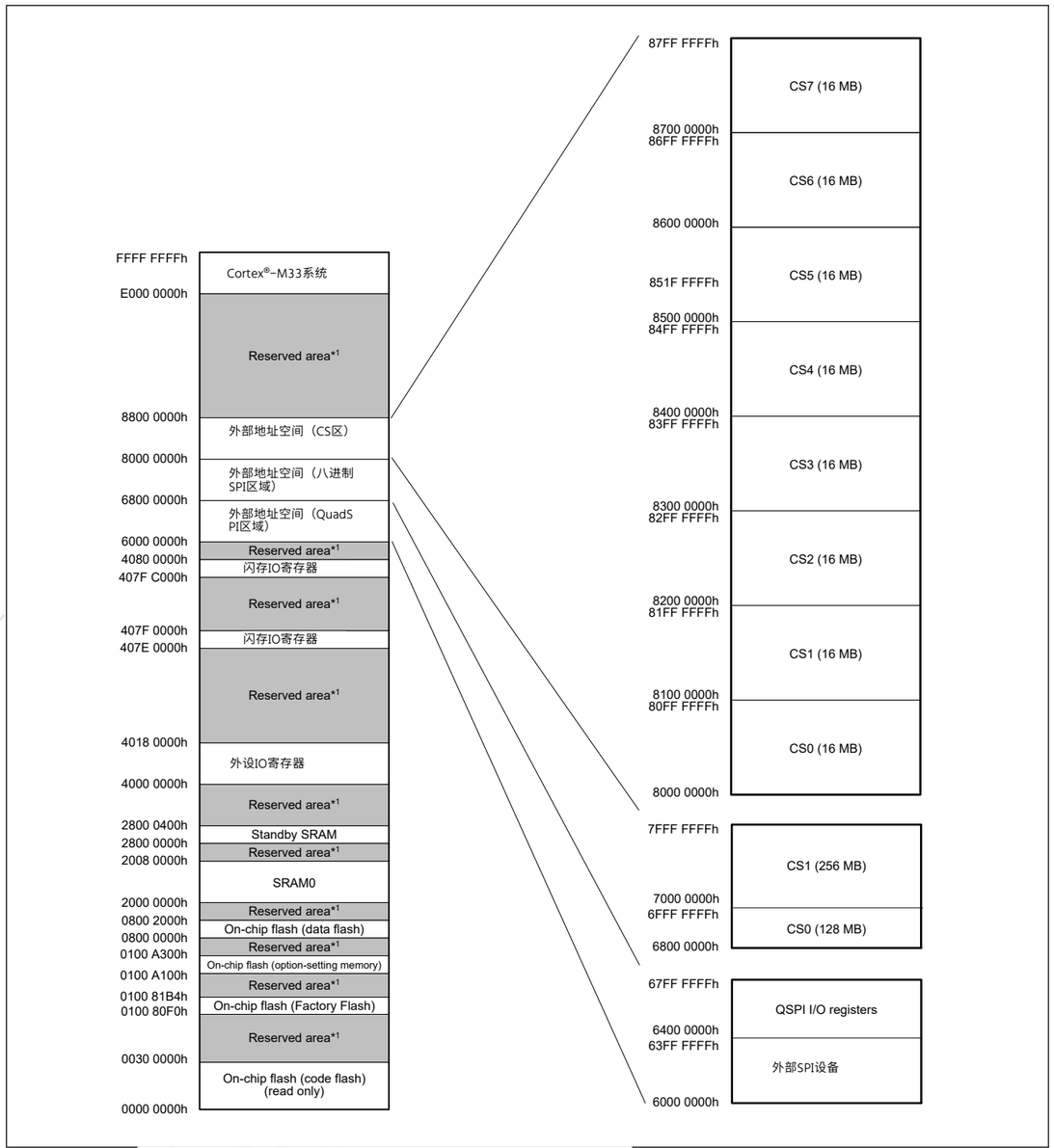


Figure 4.3 外部地址空间之间的关联（176针）

5. Resets

5.1 Overview

The MCU provides 14 resets.

Table 5.1 lists the reset names and sources.

Table 5.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
SRAM ECC error reset	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection
TrustZone error reset	TrustZone error detection
Cache Parity error reset	Cache Parity error detection
Deep software standby reset	Deep software standby mode is canceled by an interrupt
Software reset	Register setting (use the software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 7, Low Voltage Detection (LVD) and section 53, Electrical Characteristics.

The internal state and pins are initialized by a reset. Table 5.2 and Table 5.3 list the targets initialized by resets.

Table 5.2 Reset detect flags initialized by each reset source (1 of 4)

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	—	—	—	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	—	—	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	—	—	—	—	—
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	—	—	—	—	—
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	—	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	—	—	—	—	—

5. Resets

5.1 Overview

MCU提供14次复位。

表5.1列出了复位名称和来源。

Table 5.1 重置名称和来源

重设名称	Source
RES引脚复位	输入到RES引脚的电压被驱动为低电平
Power-on reset	VCC上升（电压检测VPOR）*1
独立看门狗定时器复位	IWDT下溢或刷新错误
看门狗定时器复位	WDT下溢或刷新错误
电压监控器0复位	VCC下降（电压检测Vdet0）*1
电压监视器1复位	VCC下降（电压检测Vdet1）*1
电压监视器2复位	VCC下降（电压检测Vdet2）*1
SRAM奇偶校验错误复位	SRAM奇偶校验错误检测
SRAMECC错误复位	SRAMECC错误检测
总线主控MPU错误复位	总线主控MPU错误检测
TrustZone错误重置	TrustZone错误检测
缓存奇偶校验错误重置	缓存奇偶校验错误检测
深度软件待机复位	深度软件待机模式被中断取消
软件复位	寄存器设置（使用软件复位位AIRCR.SYSRESETREQ）

注1.有关要监控的电压（VPOR、Vdet0、Vdet1和Vdet2）的详细信息，请参见第7节，低电压检测(LVD)和第53节，电气特性。

内部状态和引脚由复位初始化。表5.2和表5.3列出了由复位初始化的目标。

Table 5.2 由每个复位源初始化的复位检测标志（4个中的1个）

要初始化的标志	重置源							
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
上电复位检测标志(RSTSR0.PORF)	✓	—	—	—	—	—	—	—
电压监视器0复位检测标志(RSTSR0.LVD0RF)	✓	✓	—	—	—	—	—	—
Independent 看门狗定时器 复位检测标志(RSTSR1.IWDTRF)	✓	✓	✓	—	—	—	—	—
看门狗定时器 复位检测标志(RSTSR1.WDTRF)	✓	✓	✓	—	—	—	—	—
电压监视器1复位检测标志(RSTSR0.LVD1RF)	✓	✓	✓	—	—	—	—	—
电压监视器2复位检测标志(RSTSR0.LVD2RF)	✓	✓	✓	—	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (2 of 4)

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	—	—	—	—	—
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	—	—	—	—	—
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	✓	✓	✓	—	—	—	—	—
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	—	—	—	—	—
TrustZone Error Reset Detect Flag (RSTSR1.TZERF)	✓	✓	✓	—	—	—	—	—
Cache Parity Reset Detect Flag (RSTSR1.CPERF)	✓	✓	✓	—	—	—	—	—
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	✓	✓	✓	—	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	✓	—	—	—	—	—	—

Table 5.2 Reset detect flags initialized by each reset source (3 of 4)

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone reset error	Cache Parity error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
Power-On Reset Detect Flag (RSTSR0.PORF)	—	—	—	—	—	—	—
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	—	—	—	—	—	—	—
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	—	—	—	—	—	✓	✓
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	—	—	—	—	—	✓	✓
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	—	—	—	—	—	—	—
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	—	—	—	—	—	—	—
Software Reset Detect Flag (RSTSR1.SWRF)	—	—	—	—	—	✓	✓
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	—	—	—	—	—	✓	✓
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	—	—	—	—	—	✓	✓

Table 5.2 由每个复位源初始化的复位检测标志（4个中的2个）

要初始化的标志	重置源							
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
软件复位检测标志(RSTSR1.SWRF)	✓	✓	✓	—	—	—	—	—
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	✓	✓	✓	—	—	—	—	—
SRAMECC错误复位检测标志(RSTSR1.REERF)	✓	✓	✓	—	—	—	—	—
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	✓	✓	✓	—	—	—	—	—
TrustZone错误重置检测标志(RSTSR1.TZERF)	✓	✓	✓	—	—	—	—	—
高速缓存奇偶校验复位检测标志(RSTSR1.CPERF)	✓	✓	✓	—	—	—	—	—
深度软件待机复位检测标志(RSTSR0.DPRSTF)	✓	✓	✓	—	—	—	—	—
冷启动热启动确定标志(RSTSR2.CWSF)	—	✓	—	—	—	—	—	—

Table 5.2 由每个复位源初始化的复位检测标志（4个中的3个）

要初始化的标志	重置源						
	SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	TrustZone重置错误	缓存奇偶校验错误重置	深度软件待机复位	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
上电复位检测标志(RSTSR0.PORF)	—	—	—	—	—	—	—
电压监控器0复位检测Flag (RSTSR0.LVD0RF)	—	—	—	—	—	—	—
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	—	—	—	—	—	✓	✓
看门狗定时器复位检测Flag (RSTSR1.WDTRF)	—	—	—	—	—	✓	✓
电压监视器1复位检测Flag (RSTSR0.LVD1RF)	—	—	—	—	—	—	—
电压监视器2复位检测Flag (RSTSR0.LVD2RF)	—	—	—	—	—	—	—
软件复位检测标志(RSTSR1.SWRF)	—	—	—	—	—	✓	✓
SRAM奇偶校验错误复位检测Flag (RSTSR1.RPERF)	—	—	—	—	—	✓	✓
SRAMECC错误复位检测Flag (RSTSR1.REERF)	—	—	—	—	—	✓	✓

Table 5.2 Reset detect flags initialized by each reset source (4 of 4)

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone reset error	Cache Parity error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	—	—	—	—	—	✓	✓
TrustZone Error Reset Detect Flag (RSTSR1.TZERF)	—	—	—	—	—	✓	✓
Cache Parity Reset Detect Flag (RSTSR1.CPERF)	—	—	—	—	—	✓	✓
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	—	—	—	—	—	—	—
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	—	—	—	—	—	—	—

Note: ✓ : Initialized to 0
— : Not initialized

Table 5.3 Module-related registers initialized by each reset source (1 of 4)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Independent watchdog timer registers	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓	✓
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0,LVD1CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	—	—	—
Voltage monitor function 2 registers	LVD2CR0, LVD2CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	—	—	—
SOSC register	SOSCCR	—	✓*1	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—	—
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—	✓	✓	—
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
Realtime Clock (RTC) register*2		—	—	—	—	—	—	—	—
AGTn registers (n = 0 to 3)		—	✓	✓	—	—	✓	✓	—
AGTn registers (n = 4, 5)		✓	✓	✓	✓	✓	✓	✓	✓
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓

Table 5.2 由每个复位源初始化的复位检测标志（4个中的4个）

要初始化的标志	重置源						
	SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	TrustZone重置错误	缓存奇偶校验错误重置	深度软件待机复位	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	—	—	—	—	—	✓	✓
TrustZone错误复位检测标志(RSTSR1.TZERF)	—	—	—	—	—	✓	✓
高速缓存奇偶校验复位检测标志(RSTSR1.CPERF)	—	—	—	—	—	✓	✓
深度软件待机复位检测标志(RSTSR0.DPRSTF)	—	—	—	—	—	—	—
冷启动热启动确定标志(RSTSR2.CWSF)	—	—	—	—	—	—	—

Note: :初始化为0—:未初始化

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的1个）

待初始化的寄存器		重置源							
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
独立的看门狗定时器寄存器	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓	✓
看门狗定时器寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
电压监控功能1个寄存器	LVD1CR0,LVD1CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	—	—	—
电压监控功能2个寄存器	LVD2CR0, LVD2CMPCR	✓	✓	✓	✓	✓	—	—	—
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	—	—	—
SOSC register	SOSCCR	—	✓*1	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—	—
LOCO寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	✓	✓	—	—	✓	✓	—
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
实时时钟(RTC)寄存器*2		—	—	—	—	—	—	—	—
AGTn寄存器（n=0到3）		—	✓	✓	—	—	✓	✓	—
AGTn registers (n = 4, 5)		✓	✓	✓	✓	✓	✓	✓	✓
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓

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Table 5.3 Module-related registers initialized by each reset source (2 of 4)

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
Bus, MPU and TrustZone error registers*4	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	✓	✓	✓	✓	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓	✓	✓
Pin states (XCIN/XCOUT pin)		—	—	—	—	—	—	—	—
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
	SYOCDCR	—	✓	—	—	—	—	—	—
Security Attribute Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, BBFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, ELCSARC, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*5	✓	✓*5	✓*5	✓*5	✓*5	✓*5	✓*5
Battery backup register	VBTBKRn,VBTICTLR	—	—	—	—	—	—	—	—
	VBTBER	—	✓	—	—	—	—	—	—
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓	✓

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的2个）

待初始化的寄存器		重置源							
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
总线、MPU和TrustZone错误寄存器*4	BUS_ERROR_ADDRESS寄存器BUS_ERROR_STAT 美国注册	✓	✓	✓	✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚）		—	—	—	—	—	—	—	—
低功耗功能寄存器	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
	SYOCDCR	—	✓	—	—	—	—	—	—
安全属性 Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, BBFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, ELCSARC, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*5	✓	✓*5	✓*5	✓*5	✓*5	✓*5	✓*5
电池备份寄存器	VBTBKRn,VBTICTLR	—	—	—	—	—	—	—	—
	VBTBER	—	✓	—	—	—	—	—	—
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓	✓	✓	✓

Table 5.3 Module-related registers initialized by each reset source (3 of 4)

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone error reset	Cache Parity error reset	Deep Software Standby reset	
							DEEPCU T[0] = 0	DEEPCU T[0] = 1
Independent watchdog timer registers	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0,LVD1CMPCR	—	—	—	—	—	—	—
	LVD1CR1 / LVD1SR	—	—	—	—	—	✓	✓
Voltage monitor function 2 registers	LVD2CR0, LVD2CMPCR	—	—	—	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—	—	✓	✓
SOSC register	SOSCCR	—	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	—	—	—	—	—	✓
MOSC register	MOMCR	✓	✓	✓	✓	✓	—	—
Realtime Clock (RTC) register*2		—	—	—	—	—	—	—
AGTn registers (n = 0 to 3)		—	—	—	—	—	—	✓
AGTn registers (n = 4,5)		✓	✓	✓	✓	✓	✓	✓
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	—	✓
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	—	✓
Bus, MPU and TrustZone error registers*4	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	—	—	—	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	*3	*3
Pin states (XCIN/XCOUT pin)		—	—	—	—	—	—	—
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	—	—
	SYOCDCR	—	—	—	—	—	—	—

Table 5.3 由每个复位源初始化的模块相关寄存器（4个中的3个）

待初始化的寄存器		重置源						
		SRAM奇偶校验错误复位	SRAMECC错误复位	总线主控MPU错误复位	TrustZone错误重置	缓存奇偶校验错误重置	深度软件待机复位	
							DEEPCU T[0] = 0	DEEPCU T[0] = 1
独立的看门狗定时器寄存器	IWDTRR, IWDTSR	✓	✓	✓	✓	✓	✓	✓
看门狗定时器寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
电压监控功能1个寄存器	LVD1CR0,LVD1CMPCR	—	—	—	—	—	—	—
	LVD1CR1 / LVD1SR	—	—	—	—	—	✓	✓
电压监控功能2个寄存器	LVD2CR0, LVD2CMPCR	—	—	—	—	—	—	—
	LVD2CR1/LVD2SR	—	—	—	—	—	✓	✓
SOSC register	SOSCCR	—	—	—	—	—	—	—
	SOMCR	—	—	—	—	—	—	—
LOCO寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	—	—	—	—	—	—	✓
MOSC register	MOMCR	✓	✓	✓	✓	✓	—	—
实时时钟(RTC)寄存器*2		—	—	—	—	—	—	—
AGTn寄存器（n=0到3）		—	—	—	—	—	—	✓
AGTn registers (n = 4,5)		✓	✓	✓	✓	✓	✓	✓
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	—	✓
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	—	✓
总线、MPU和TrustZone错误寄存器*4	BUS_ERROR_ADDRESS Register BUS_ERROR_STATUS Register	✓	✓	—	—	—	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓	*3	*3
引脚状态（XCINXCOUT引脚）		—	—	—	—	—	—	—
低功耗功能寄存器	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	—	—
	SYOCDCR	—	—	—	—	—	—	—

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Table 5.3 Module-related registers initialized by each reset source (4 of 4)

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	TrustZone error reset	Cache Parity error reset	Deep Software Standby reset	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
Security Attribute Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, BBFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, ELCSARC, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*5	✓*5	✓*5	✓*5	✓*5	✓*6	✓*6
Battery backup register	VBTBKRn,VBTICTLR	—	—	—	—	—	—	—
	VBTBER	—	—	—	—	—	—	—
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓

Note: ✓ : Initialized
— : Not initialized
Note 1. For the initial value of each register, see section 8, Clock Generation Circuit.
Note 2. The RTC has a software reset. Some control bits are not initialized by all types of resets. For details on the target bits, see section 23, Realtime Clock (RTC).
Note 3. Depends on the setting of DPSBYCR.IOKEEP.
Note 4. Some control bits are not initialized by all types of resets. For details on the target bits, see section 14, Buses
Note 5. Reset does not occur while the debugger is connected (DBGSTR.CDBGPWRUPREQ = 1) even if On-chip debugger is disabled (SYOCDCR.DBGEN = 0).
Note 6. Reset does not occur while On-chip debugger is enabled (SYOCDCR.DBGEN = 1).

The RTC is not initialized by any reset source. SOSC and LOCO can be selected as the clock sources of the RTC.

Table 5.4 and Table 5.5 show the states of SOSC and LOCO when a reset occurs.

Table 5.4 States of SOSC when a reset occurs

		Reset source	
		POR	Other
SOSC	Enable or disable	Initialized to enable	Continue with the state that was selected before the reset occurred
	Drive capability	Continue with the state that was selected before the reset occurred	

Table 5.5 States of LOCO when a reset occurs

		Reset source	
		POR, LVD0, LVD1, LVD2, Deep Software Standby (DEEPCUT[0] = 1)	Other
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by power-on (accuracy: ± 10%)	Continue with the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, LVD2, and Deep Software Standby (DEEPCUT[0] = 1) resets, returning the LOCO to the default oscillation accuracy. This can affect RTC accuracy if the RTC uses the LOCO (with a user trimming value in LOCOUTCR) as the RTC source clock. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

When a reset is released, reset exception handling starts.

Table 5.3 由每个复位源初始化的模块相关寄存器（4个，共4个）

待初始化的寄存器		重置源						
		SRAM奇偶校验错误复位	SRAMECC错误复位	总线主控MPU错误复位	TrustZone错误重置	缓存奇偶校验错误重置	深度软件待机复位	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
安全属性Registers	CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, BBFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, ELCSARC, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR	✓*5	✓*5	✓*5	✓*5	✓*5	✓*6	✓*6
电池备份寄存器	VBTBKRn,VBTICTLR	—	—	—	—	—	—	—
	VBTBER	—	—	—	—	—	—	—
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓	✓	✓

Note: :已初始化—:未初始化
注1.关于各寄存器的初始值，请参阅第8节"时钟生成电路"。
注2.RTC具有软件复位功能。某些控制位并非由所有类型的复位初始化。有关目标位的详细信息，请参见第23节，实时时钟(RTC)。
注3.取决于DPSBYCR.IOKEEP的设置。
注4.并非所有类型的复位都会初始化一些控制位。有关目标位的详细信息，请参阅第14节，总线
注5.连接调试器(DBGSTR.CDBGPWRUPREQ=1)时不会发生复位，即使禁用片上调试器(SYOCDCR.DBGEN=0)。
注6.启用片上调试器(SYOCDCR.DBGEN=1)时不会发生复位。

RTC不会被任何复位源初始化。可选择SOSC和LOCO作为RTC的时钟源。

表5.4和表5.5显示了复位发生时SOSC和LOCO的状态。

Table 5.4 发生复位时SOSC的状态

		重置源	
		POR	Other
SOSC	启用或禁用	初始化为启用	继续使用重置发生之前选择的状态
	驱动能力	继续使用重置发生之前选择的状态	

Table 5.5 发生复位时的LOCO状态

		重置源	
		POR、LVD0、LVD1、LVD2、深软件待机（DEEPCUT[0]=1）	Other
LOCO	启用或禁用	初始化为启用	
	振荡精度*1	上电微调前初始化为精度（精度：±10%）	继续使用被修剪的精度LOCOUTCR

注1.LOCO用户微调控制寄存器(LOCOUTCR)由POR、LVD0、LVD1、LVD2和深度软件待机复位(DEEPCUT[0]=1)复位，将LOCO返回到默认振荡精度。如果RTC使用LOCO（在LOCOUTCR中具有用户修整值）作为RTC源时钟，这可能会影响RTC精度。要恢复预复位的LOCO振荡精度，请在任何这些复位后将所需的微调值重新加载到LOCOUTCR。

当一个复位被释放时，复位异常处理开始。

Table 5.6 lists the pin related to the reset function.

Table 5.6 Pin related to reset

Pin name	I/O	Function
RES	Input	Reset pin

5.2 Register Descriptions

5.2.1 RSTSAR : Reset Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: Reset Status Register 0 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: Reset Status Register 1 0: Secure 1: Non Secure	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: Reset Status Register 2 0: Secure 1: Non Secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of RSTSR0.

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of RSTSR1.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of RSTSR2.

表5.6列出了与复位功能相关的引脚。

Table 5.6 复位相关引脚

引脚名称	I/O	Function
RES	Input	复位引脚

5.2 注册说明

5.2.1 RSTSAR：重置安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3C4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	非安全属性位0 目标寄存器：复位状态寄存器0 0：安全1：不安全	R/W
1	NONSEC1	非安全属性位1 目标寄存器：复位状态寄存器1 0：安全1：不安全	R/W
2	NONSEC2	非安全属性位2 目标寄存器：复位状态寄存器2 0：安全1：不安全	R/W
31:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

NONSEC0位（非安全属性位0）

该位控制RSTSR0的安全属性。

NONSEC1位（非安全属性位1）

该位控制RSTSR1的安全属性。

NONSEC2位（非安全属性位2）

该位控制RSTSR2的安全属性。

5.2.2 RSTSR0 : Reset Status Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	x*1	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	PORF	Power-On Reset Detect Flag 0: Power-on reset not detected 1: Power-on reset detected	R/W*2
1	LVD0RF	Voltage Monitor 0 Reset Detect Flag 0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected	R/W*2
2	LVD1RF	Voltage Monitor 1 Reset Detect Flag 0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected	R/W*2
3	LVD2RF	Voltage Monitor 2 Reset Detect Flag 0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected	R/W*2
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	DPSRSTF	Deep Software Standby Reset Flag 0: Deep software standby mode cancellation not requested by an interrupt. 1: Deep software standby mode cancellation requested by an interrupt.	R/W*2

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.

Note 2. The register is cleared when a reset source listed in Table 5.2 occurs or when 0 is written to clear a flag. Bits other than the flag that is cleared should be set to 1.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When PORF is read as 1 and then 0 is written to PORF

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

5.2.2 RSTSR0：复位状态寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x410

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
重置后的值：	x*1	0	0	0	x*1	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	PORF	上电复位检测标志 0：未检测到上电复位1：检测到上电复位	R/W*2
1	LVD0RF	电压监视器0复位检测标志 0：未检测到电压监控器0复位1：检测到电压监控器0复位	R/W*2
2	LVD1RF	电压监视器1复位检测标志 0：未检测到电压监控器1复位1：检测到电压监控器1复位	R/W*2
3	LVD2RF	电压监视器2复位检测标志 0：未检测到电压监控器2复位1：检测到电压监控器2复位	R/W*2
6:4	—	这些位被读取为0。写入值应为0。	R/W
7	DPSRSTF	深度软件待机复位标志 0：中断未请求深度软件待机模式取消。1：中断请求的深度软件待机模式取消。	R/W*2

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后的值取决于复位源。

注2.当表5.2中列出的复位源发生或写入0以清除标志时，该寄存器被清除。清除标志以外的位应设置为1。

PORF标志（上电复位检测标志）

PORF标志表示发生了上电复位。

[Setting condition]

●发生上电复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当PORF读为1，然后将0写入PORF

LVD0RF标志（电压监视器0复位检测标志）

LVD0RF标志表示VCC电压低于Vdet0。

[Setting condition]

●发生电压监视器0复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当LVD0RF被读为1，然后0被写入LVD0RF。

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD1RF is read as 1 and then 0 is written to LVD1RF

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that the VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When LVD2RF is read as 1 and then 0 is written to LVD2RF

DPSRSTF flag (Deep Software Standby Reset Flag)

The DPSRSTF flag indicates that deep software standby mode has been canceled by an external or internal interrupt and that an internal reset (deep software standby reset) occurred when the exception from Deep Software Standby Mode occur.

[Setting condition]

- When deep software standby mode is cancelled by an external or an internal interrupt. For details, see section 10, Low Power Modes.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs.
- When DPSRSTF is read as 1 and then 0 is written to DPSRSTF

5.2.3 RSTSR1 : Reset Status Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPERF	—	TZERF	—	BUSMRF	—	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	x*1	0	x*1	0	x*1	0	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	Independent Watchdog Timer Reset Detect Flag 0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected	R/W*2
1	WDTRF	Watchdog Timer Reset Detect Flag 0: Watchdog timer reset not detected 1: Watchdog timer reset detected	R/W*2
2	SWRF	Software Reset Detect Flag 0: Software reset not detected 1: Software reset detected	R/W*2
7:3	—	These bits are read as 0. The write value should be 0.	R/W

LVD1RF标志（电压监视器1复位检测标志）

LVD1RF标志表示VCC电压低于Vdet1。

[Setting condition]

●发生电压监视器1复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当LVD1RF被读为1，然后0被写入LVD1RF

LVD2RF标志（电压监视器2复位检测标志）

LVD2RF标志表示VCC电压低于Vdet2。

[Setting condition]

●发生电压监视器2复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当LVD2RF被读为1，然后0被写入LVD2RF

DPRSTF标志（深度软件待机复位标志）

DPSRSTF标志表示深度软件待机模式已被外部或内部中断取消，并且当深度软件待机模式发生异常时发生内部复位（深度软件待机复位）。

[Setting condition]

●当深度软件待机模式被外部或内部中断取消时。有关详细信息，请参阅第10节，低功耗模式。

[Clearing conditions]

●发生表5.2中列出的复位时。

●DPSRSTF被读为1，然后0被写入DPSRSTF

5.2.3 RSTSR1：复位状态寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x0C0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPERF	—	TZERF	—	BUSMRF	—	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
重置后的值：	x*1	0	x*1	0	x*1	0	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Function	R/W
0	IWDTRF	独立看门狗定时器复位检测标志 0：未检测到独立看门狗定时器复位1：检测到独立看门狗定时器复位	R/W*2
1	WDTRF	看门狗定时器复位检测标志 0：未检测到看门狗定时器复位1：检测到看门狗定时器复位	R/W*2
2	SWRF	软件复位检测标志 0：未检测到软件复位1：检测到软件复位	R/W*2
7:3	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
8	RPERF	SRAM Parity Error Reset Detect Flag 0: SRAM parity error reset not detected 1: SRAM parity error reset detected	R/W*2
9	REERF	SRAM ECC Error Reset Detect Flag 0: SRAM ECC error reset not detected 1: SRAM ECC error reset detected	R/W*2
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMRF	Bus Master MPU Error Reset Detect Flag 0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected	R/W*2
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZERF	TrustZone Error Reset Detect Flag 0: TrustZone error reset not detected. 1: TrustZone error reset detected.	R/W*2
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPERF	Cache Parity Error Reset Detect Flag 0: Cache Parity error reset not detected. 1: Cache Parity error reset detected.	R/W*2

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurs.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurs.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurs.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs

Bit	Symbol	Function	R/W
8	RPERF	SRAM奇偶校验错误复位检测标志 0：未检测到SRAM奇偶校验错误复位1： 检测到SRAM奇偶校验错误复位	R/W*2
9	REERF	SRAMECC错误复位检测标志 0：未检测到SRAMECC错误复位1：检 测到SRAMECC错误复位	R/W*2
10	—	该位读取为0。写入值应为0。	R/W
11	BUSMRF	总线主控MPU错误复位检测标志 0：未检测到总线主控MPU错误复位1：检测 到总线主控MPU错误复位	R/W*2
12	—	该位读取为0。写入值应为0。	R/W
13	TZERF	TrustZone错误复位检测标志 0：未检测到TrustZone错误复位。1： 检测到TrustZone错误复位。	R/W*2
14	—	该位读取为0。写入值应为0。	R/W
15	CPERF	高速缓存奇偶校验错误复位检测标志 0：未检测到缓存奇偶校验错误复位。1： 检测到缓存奇偶校验错误复位。	R/W*2

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后的值取决于复位源。
注2.只能写入0来清除标志。该标志必须在读取1后写入0来清除。

IWDTRF标志（独立看门狗定时器复位检测标志）

IWDTRF标志指示发生了独立的看门狗定时器复位。

[Setting condition]

●发生独立看门狗定时器复位时。

[Clearing conditions]

●发生表5.2中列出的复位时
●读取1，然后将0写入IWDTRF。

WDTRF标志（看门狗定时器复位检测标志）

WDTRF标志指示发生了看门狗定时器复位。

[Setting condition]

●发生看门狗定时器复位时。

[Clearing conditions]

●发生表5.2中列出的复位时
●读取1后写入0时WDTRF。

SWRF标志（软件复位检测标志）

SWRF标志表示发生了软件复位。

[Setting condition]

●发生软件复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

- When 1 is read and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that an SRAM parity error reset occurs.

[Setting condition]

- When an SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to RPERF.

REERF flag (SRAM ECC Error Reset Detect Flag)

The REERF flag indicates that an SRAM ECC error reset occurs.

[Setting condition]

- When an SRAM ECC error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read as 1 and then 0 is written to REERF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurs.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read and then 0 is written to BUSMRF.

TZERF flag (TrustZone Error Reset Detect Flag)

The TZERF flag indicates that a TrustZone error reset has occurred.

[Setting condition]

- When a TrustZone error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to TZERF.

CPERF flag (Cache Parity Error Reset Detect Flag)

The CPERF flag indicates that a Cache Parity error reset has occurred.

[Setting condition]

- When a Cache Parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 5.2 occurs
- When 1 is read then and 0 is written to CPERF.

●读取1，然后将0写入SWRF。

RPERF标志（SRAM奇偶校验错误复位检测标志）

RPERF标志表示发生SRAM奇偶校验错误复位。

[Setting condition]

●SRAM奇偶校验错误复位发生时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当1被读为1，然后0被写入RPERF。

REERF标志（SRAMECC错误复位检测标志）

REERF标志表示发生了SRAMECC错误复位。

[Setting condition]

●SRAMECC错误复位发生时。

[Clearing conditions]

●发生表5.2中列出的复位时

●当1被读为1，然后0被写入REERF。

BUSMRF标志（总线主控MPU错误复位检测标志）

BUSMRF标志指示发生总线主控MPU错误复位。

[Setting condition]

●发生总线主控MPU错误复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1，然后将0写入BUSMRF。

TZERF标志（TrustZone错误复位检测标志）

TZERF标志指示发生了TrustZone错误重置。

[Setting condition]

●发生TrustZone错误重置时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1并将0写入TZERF。

CPERF标志（高速缓存奇偶校验错误复位检测标志）

CPERF标志表示发生了缓存奇偶校验错误重置。

[Setting condition]

●发生CacheParity错误复位时。

[Clearing conditions]

●发生表5.2中列出的复位时

●读取1并将0写入CPERF。

5.2.4 RSTSR2 : Reset Status Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	Cold/Warm Start Determination Flag 0: Cold start 1: Warm start	R/W*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start). CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written by software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in Table 5.2 occurs.

5.3 Operation

5.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 53, Electrical Characteristics.

5.3.2 Power-On Reset

The power-on reset (POR) is an internal reset generated by the power-on reset circuit. A power-on reset is generated under the following conditions.

1. If the RES pin is in a high level state when power is supplied
2. If the RES pin is in a high level state when VCC is below V_{POR}

After VCC exceeds V_{POR} and the specified power-on reset time (t_{POR}) elapses, the CPU starts the reset exception handling. The power-on reset time is a stabilization period of the external power supply and the MCU circuit.

5.2.4 RSTSR2：复位状态寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x411

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CWSF
重置后的值：	0	0	0	0	0	0	0	x*1

Bit	Symbol	Function	R/W
0	CWSF	冷暖启动确定标志 0：冷启动1： 热启动	R/W*2
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后的值取决于复位源。
注2.只能写入1来设置标志。

RSTSR2判断是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

CWSF标志（冷暖启动确定标志）

CWSF标志指示复位处理的类型，冷启动或热启动。确定是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。CWSF标志由上电复位初始化。它不会被RES引脚产生的复位信号初始化。

[Setting condition]

●软件写入1时。将0写入CWSF不会将其设置为0。

[Clearing condition]

●发生表5.2中列出的复位时。

5.3 Operation

5.3.1 RES引脚复位

RES引脚产生此复位。当RES引脚被驱动为低电平时，所有正在进行的处理都被中止，MCU进入复位状态。要成功复位MCU，RES引脚必须在上电时指定的电源稳定时间内保持低电平。

当RES引脚从低电平驱动为高电平时，内部复位会在RES取消后等待时间(tRESWT)过去后取消。CPU然后开始复位异常处理。

有关详细信息，请参阅第53节，电气特性。

5.3.2 Power-On Reset

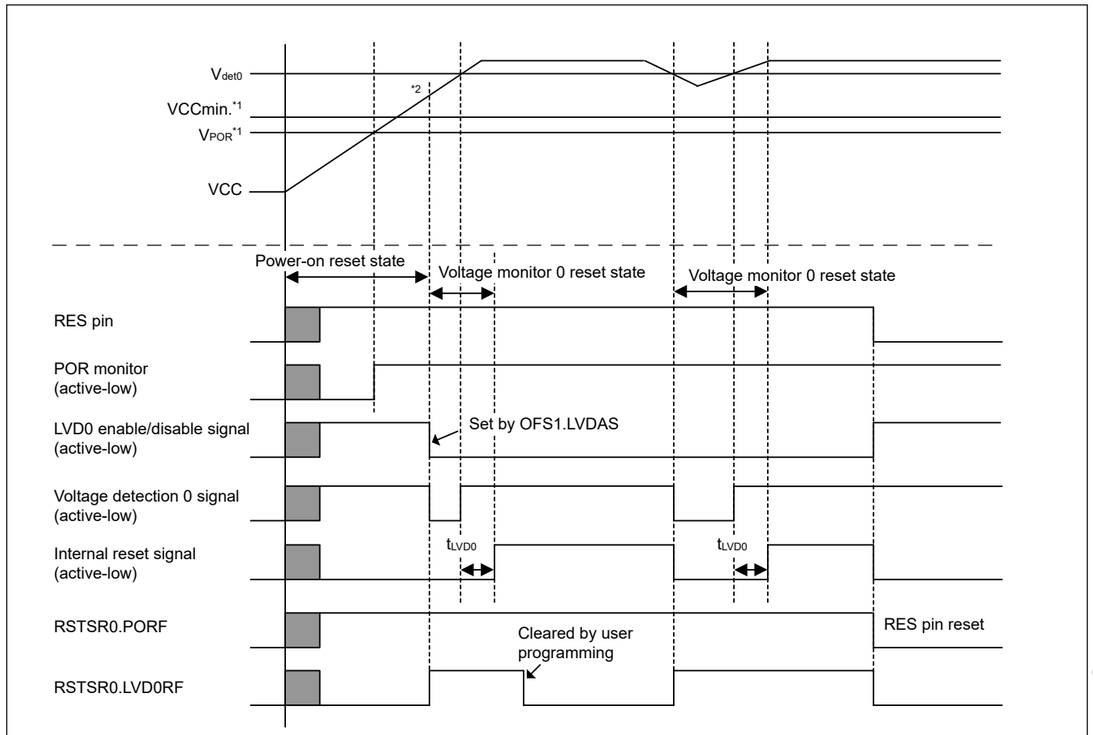
上电复位（POR）是由上电复位电路产生的内部复位。在以下条件下会产生上电复位。

1.如果RES引脚在供电时处于高电平状态
2.如果VCC低于VPOR时RES管脚处于高电平状态

在VCC超过VPOR并且经过指定的上电复位时间(tPOR)后，CPU开始复位异常处理。
上电复位时间是外部电源和MCU电路的稳定期。

After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset. When VCC falls below V_{POR}, a power-on reset state is occurred.

Figure 5.1 shows example of operations during a power-on reset.



Note: For details on the electrical characteristics, see section 53, Electrical Characteristics.
Note 1. V_{POR} shows a power-on reset detection level, and VCCmin shows the minimum guaranteed voltage of MCU.
Note 2. At power-on, VCC should rise to the minimum guaranteed voltage before the power-on reset is released.

Figure 5.1 Example of operations during a power-on reset

5.3.3 Voltage Monitor Reset

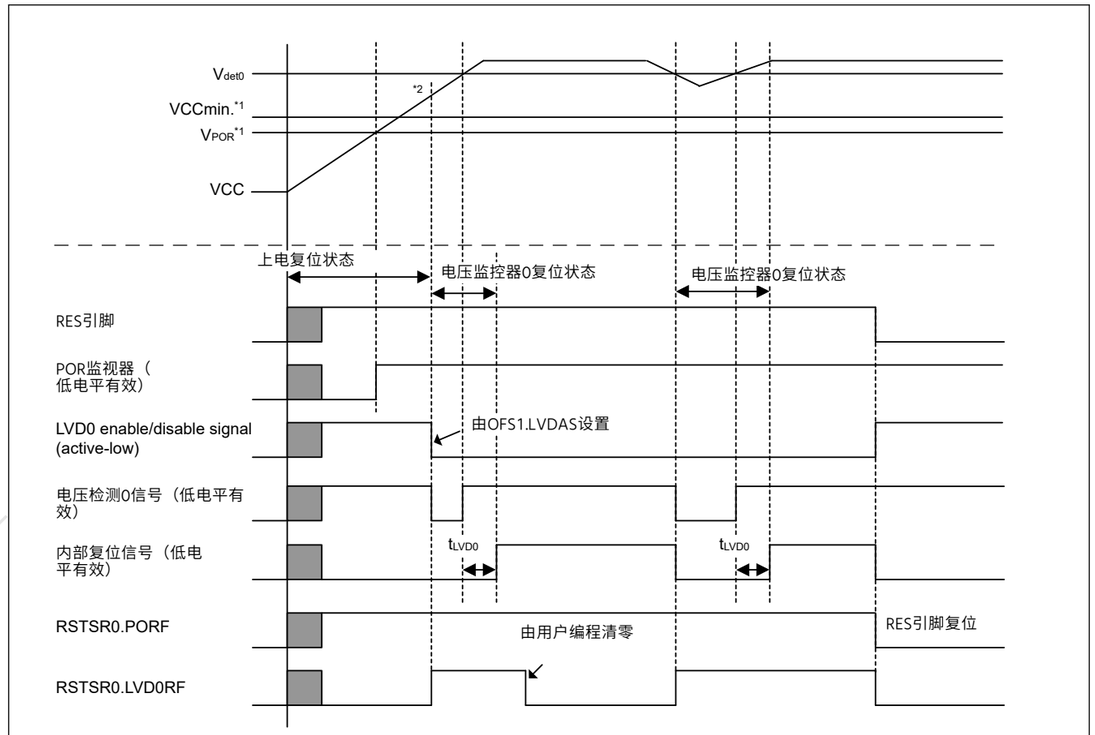
The voltage monitor i (i = 0, 1, 2) reset is an internal reset generated by the voltage monitor i circuit. If the Voltage Detection 0 Circuit Start (LVDAS) bit in the Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (t_{LVD0}) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 1 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

上电复位产生后，RSTSR0中的PORF标志设置为1。PORF标志由RES引脚复位初始化。当VCC低于VPOR时，会发生上电复位状态。

图5.1显示了上电复位期间的操作示例。



Note: 有关电气特性的详细信息，请参见第53节，电气特性。
注1.VPOR表示上电复位检测电平，VCCmin表示MCU的最低保证电压。
注2.上电时，VCC应上升到上电复位解除前的最低保证电压。

Figure 5.1 上电复位时的动作示例

5.3.3 电压监视器复位

电压监视器i(i=0 1 2)复位是由电压监视器i电路产生的内部复位。如果电压选项功能选择寄存器1(OFS1)中的检测0电路启动(LVDAS)位为0（复位后使能电压监视器0复位）且VCC低于Vdet0时，RSTSR0.LVD0RF标志变为1，电压检测电路生成电压监视器0复位。如果要使用电压监视器0复位，则将OFS1.LVDAS位清零。在VCC超过Vdet0并且经过电压监视器0复位时间(tLVD0)后，内部复位被取消，CPU开始复位异常处理。

当电压监控器1中断复位允许位(RIE)设置为1（允许电压检测电路产生复位或中断）且电压监控器1电路模式选择位(RI)设置为1（选择产生电压监控器1电路控制寄存器0(LVD1CR0)中的低电压检测复位响应，RSTSR0.LVD1RF标志设置为1，如果VCC降至或低于V，电压检测电路将产生电压监控器1复位det1。

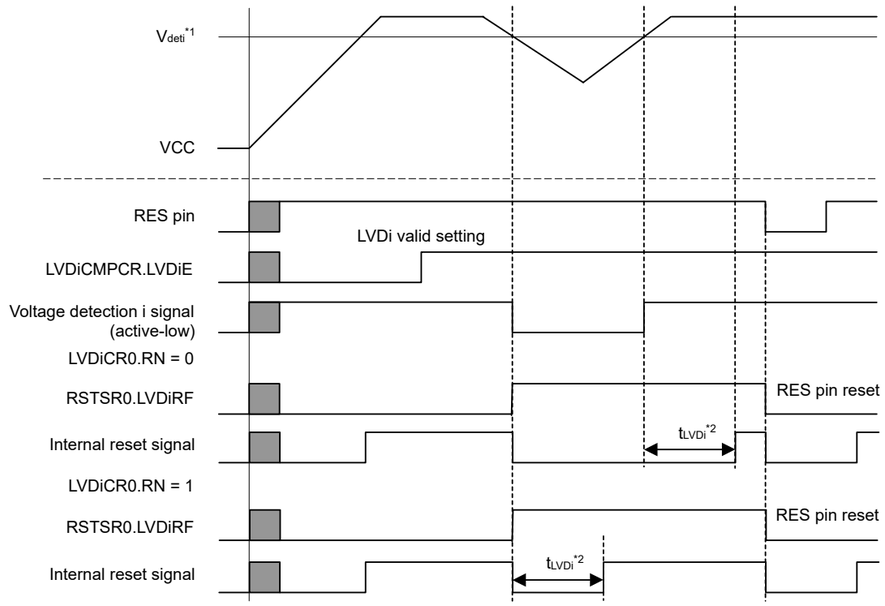
同样，当电压监视器2中断复位使能位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监视器2电路模式选择位(RI)设置为1（选择在电压监控器2电路控制寄存器0(LVD2CR0)中响应检测到低电压产生复位），RSTSR0.LVD2RF标志设置为1，如果VCC下降到或电压检测电路产生电压监控器2复位低于Vdet2。

Similarly, timing for release from the voltage monitor 1 reset state is selectable with the Voltage Monitor 1 Reset Negate Select bit (RN) in the LVD1CR0. When the LVD1CR0.RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (t_{LVD1}) elapses.

Likewise, timing for release from the voltage monitor 2 reset state is selectable by setting the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Monitoring Comparator Control Register (LVD1CMPCR/ LVD2CMPCR).

Figure 5.2 shows example of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 7, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 53, Electrical Characteristics.
Note 1. V_{deti} indicates the detection level of a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).
Note 2. t_{LVDi} indicates the time for a voltage monitor 1 reset and a voltage monitor 2 reset (i = 1, 2).

Figure 5.2 Example of operations during voltage monitor 1 and voltage monitor 2 resets

5.3.4 Deep Software Standby Reset

This is an internal reset generated when deep software standby mode is canceled by an interrupt.

When a deep software standby mode cancelation source is generated, a deep software standby reset is generated. The deep software standby reset is canceled after t_{DSBY} (return time after deep software standby mode cancelation) has elapsed. At the same time, deep software standby mode is also canceled.

When t_{DSBYWT} (wait time after deep software standby mode cancelation) has elapsed after deep software standby mode has been canceled, the internal reset is canceled and the CPU starts the reset exception handling.

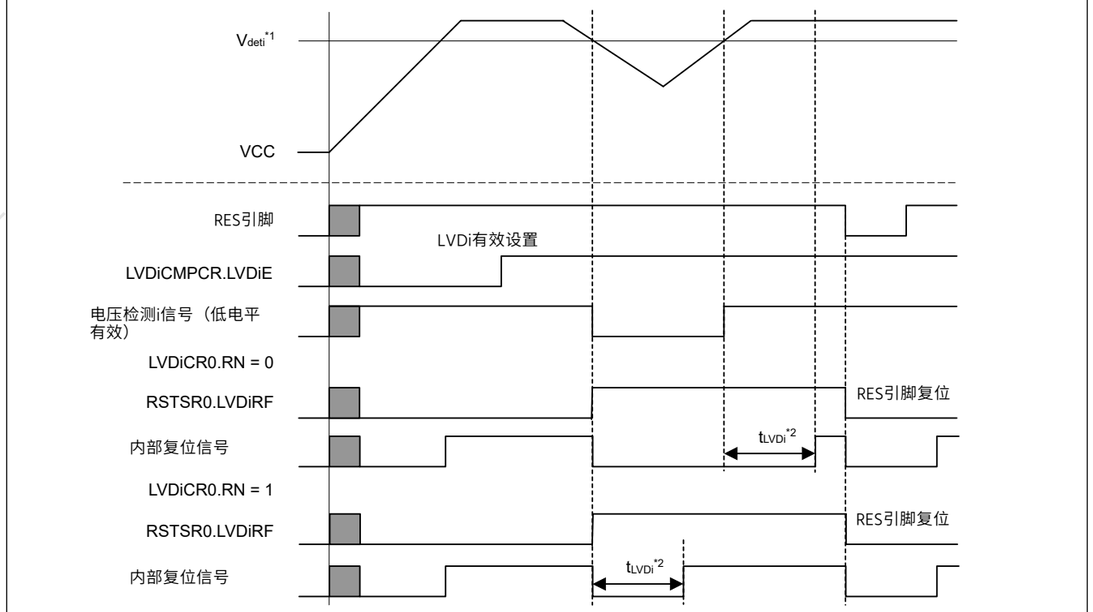
For details of the deep software standby reset, see section 10, Low Power Modes.

类似地，从电压监视器1复位状态释放的时间可以通过LVD1CR0中的电压监视器1复位否定选择位(RN)来选择。当LVD1CR0.RN位为0且VCC下降到或低于Vdet1时，CPU从内部复位状态中释放并在VCC上升到Vdet1以上后经过LVD1复位时间(tLVD1)时开始复位异常处理。当LVD1CR0.RN位为1且VCC下降到或低于Vdet1时，CPU会从内部复位状态中释放，并在LVD1复位时间(tLVD1)过去后开始复位异常处理。

同样，从电压监视器2复位状态释放的时间可通过设置电压监视器2复位来选择LDV2CR0寄存器中的取反选择位(RN)。

检测电平Vdet1和Vdet2可以在电压监控比较器控制寄存器(LVD1CMPCR LVD2CMPCR).

图5.2显示了电压监视器1和2复位期间的操作示例。有关电压监视器1复位和电压监视器2复位的详细信息，请参见第7节，低电压检测(LVD)。



Note: 有关电气特性的详细信息，请参见第53节，电气特性。
注1.Vdeti表示电压监视器1复位和电压监视器2复位(i=1 2)的检测电平。
注2.tLVDi表示电压监视器1复位和电压监视器2复位(i=1 2)的时间。

Figure 5.2 电压监控器1和电压监控器2复位期间的操作示例

5.3.4 深度软件待机复位

这是当深度软件待机模式被中断取消时产生的内部复位。

当产生深度软件待机模式取消源时，将产生深度软件待机复位。在经过tDSBY（深度软件待机模式取消后的返回时间）后，深度软件待机复位被取消。同时，深度软件待机模式也被取消。

在深度软件待机模式取消后经过tDSBYWT（深度软件待机模式取消后的等待时间）时，内部复位被取消，CPU开始复位异常处理。

有关深度软件待机复位的详细信息，请参见第10节，低功耗模式。

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5.3.5 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 25, Independent Watchdog Timer (IWDT).

5.3.6 Watchdog Timer Reset

The watchdog timer reset is an internal reset generated from the Watchdog Timer (WDT). Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select register 0 (OFS0).

When output of the watchdog timer reset is selected, a watchdog timer reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (t_{RESW2}) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 24, Watchdog Timer (WDT).

5.3.7 Software Reset

The software reset is an internal reset generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (t_{RESW2}) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M33 Technical Reference Manual*.

5.3.8 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. This flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The CWSF flag is set to 0 when a power-on reset occurs (cold start), otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 5.3 shows an example of cold/warm start determination operation.

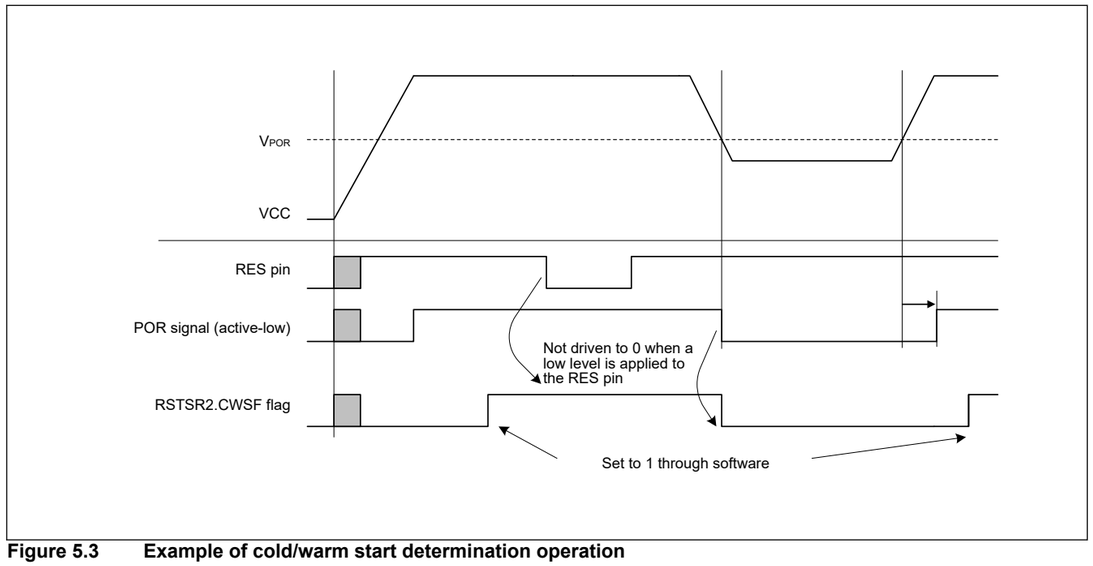


Figure 5.3 Example of cold/warm start determination operation

5.3.5 独立看门狗定时器复位

独立看门狗定时器复位是由独立看门狗定时器（IWDT）产生的内部复位。可以在选项功能选择寄存器0(OFS0)中选择IWDT的复位输出。

Whenoutputoftheindependentwatchdogtimerresetisselected theresetisgeneratediftheIWDTunderflows orifdataiswrittenwhenrefreshoperationisdisabled.当独立看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关独立看门狗定时器复位的详细信息，请参见第25节，独立看门狗定时器(IWDT)。

5.3.6 看门狗定时器复位

看门狗定时器复位是由看门狗定时器(WDT)产生的内部复位。WDT的复位输出可以在WDT复位控制寄存器(WDTRCR)或选项功能选择寄存器0(OFS0)中选择。

选择看门狗定时器复位输出时，如果WDT下溢，或者在禁止刷新操作时写入数据，则会产生看门狗定时器复位。在产生看门狗定时器复位后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关看门狗定时器复位的详细信息，请参见第24节，看门狗定时器(WDT)。

5.3.7 软件复位

软件复位是通过软件设置Arm内核的AIRCR寄存器中的SYSRESETREQ位产生的内部复位。当SYSRESETREQ位设置为1时，会产生软件复位。当软件复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关SYSRESETREQ位的详细信息，请参阅ARM®Cortex®-M33技术参考手册。

5.3.8 冷暖启动的测定

读取RSTSR2中的CWSF标志以确定复位处理的原因。该标志指示是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

当发生上电复位（冷启动）时，CWSF标志设置为0，否则该标志不设置为0。当通过软件向其写入1时，该标志设置为1。即使向其写入0，它也不会设置为0。

图5.3显示了冷暖启动确定操作的示例。

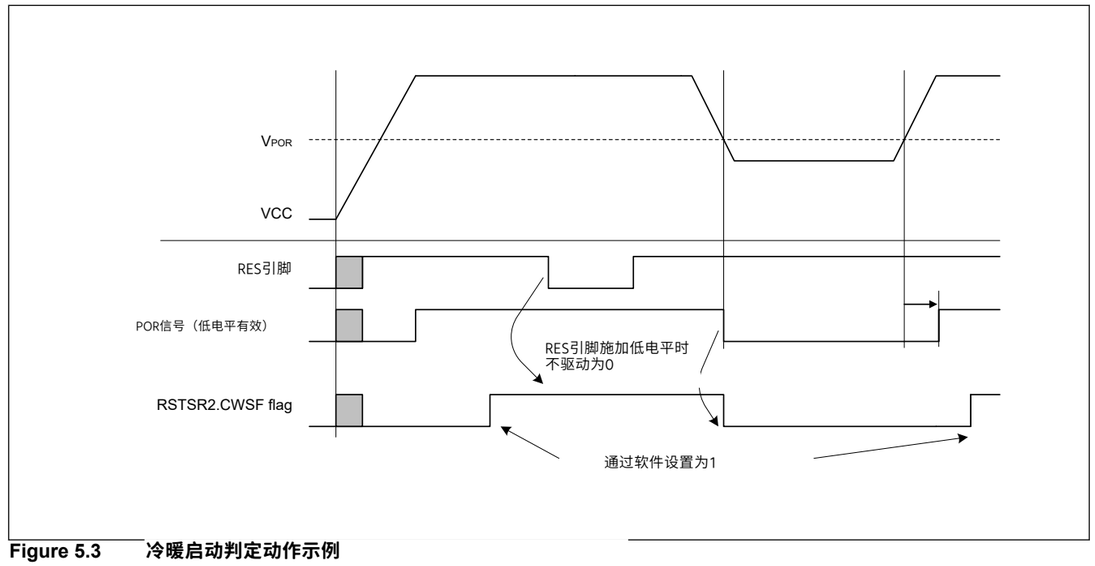
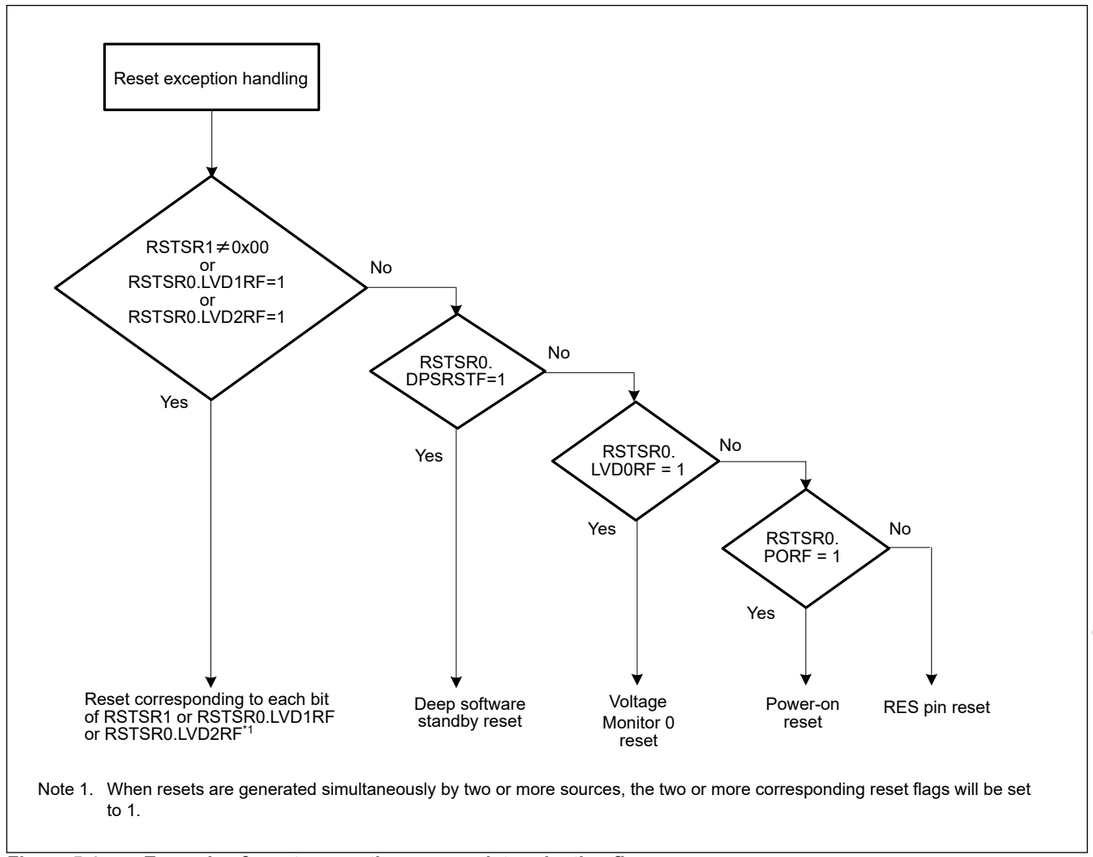


Figure 5.3 冷暖启动判定动作示例

5.3.9 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset executes the reset exception handling.

Figure 5.4 shows an example of the flow to identify a reset generation source. The reset flag must be written with 0 after it is read as 1.



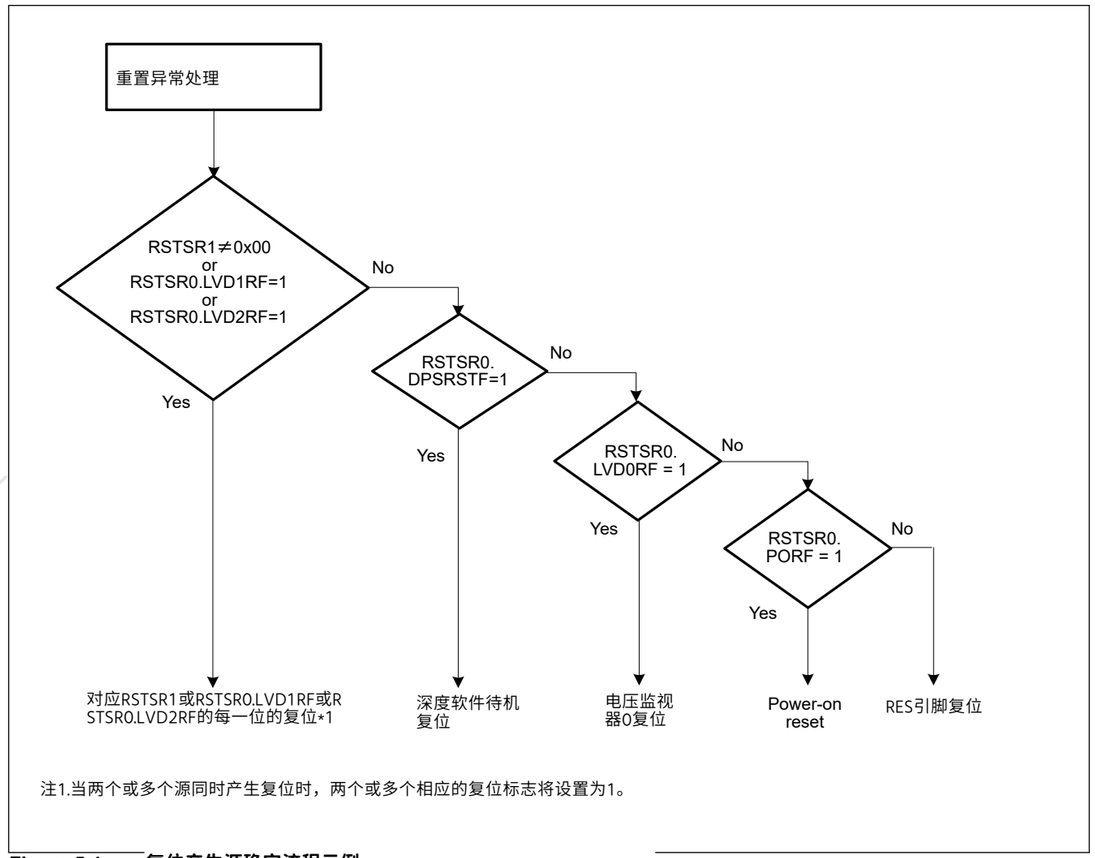
Note 1. When resets are generated simultaneously by two or more sources, the two or more corresponding reset flags will be set to 1.

Figure 5.4 Example of reset generation source determination flow

5.3.9 复位产生源的确定

读取RSTSR0和RSTSR1以确定哪个复位执行复位异常处理。

图5.4显示了识别复位产生源的流程示例。复位标志读为1后必须写为0。



注1.当两个或多个源同时产生复位时，两个或多个相应的复位标志将设置为1。

Figure 5.4 复位产生源确定流程示例

6. Option-Setting Memory

6.1 Overview

The option-setting memory determines the state of the MCU after a reset. The option-setting memory is allocated to the configuration setting area of the flash memory.

Figure 6.1 shows the option-setting memory area. The option-setting memory area has secure region. Table 6.1 shows the programming condition of the option-setting memory area.

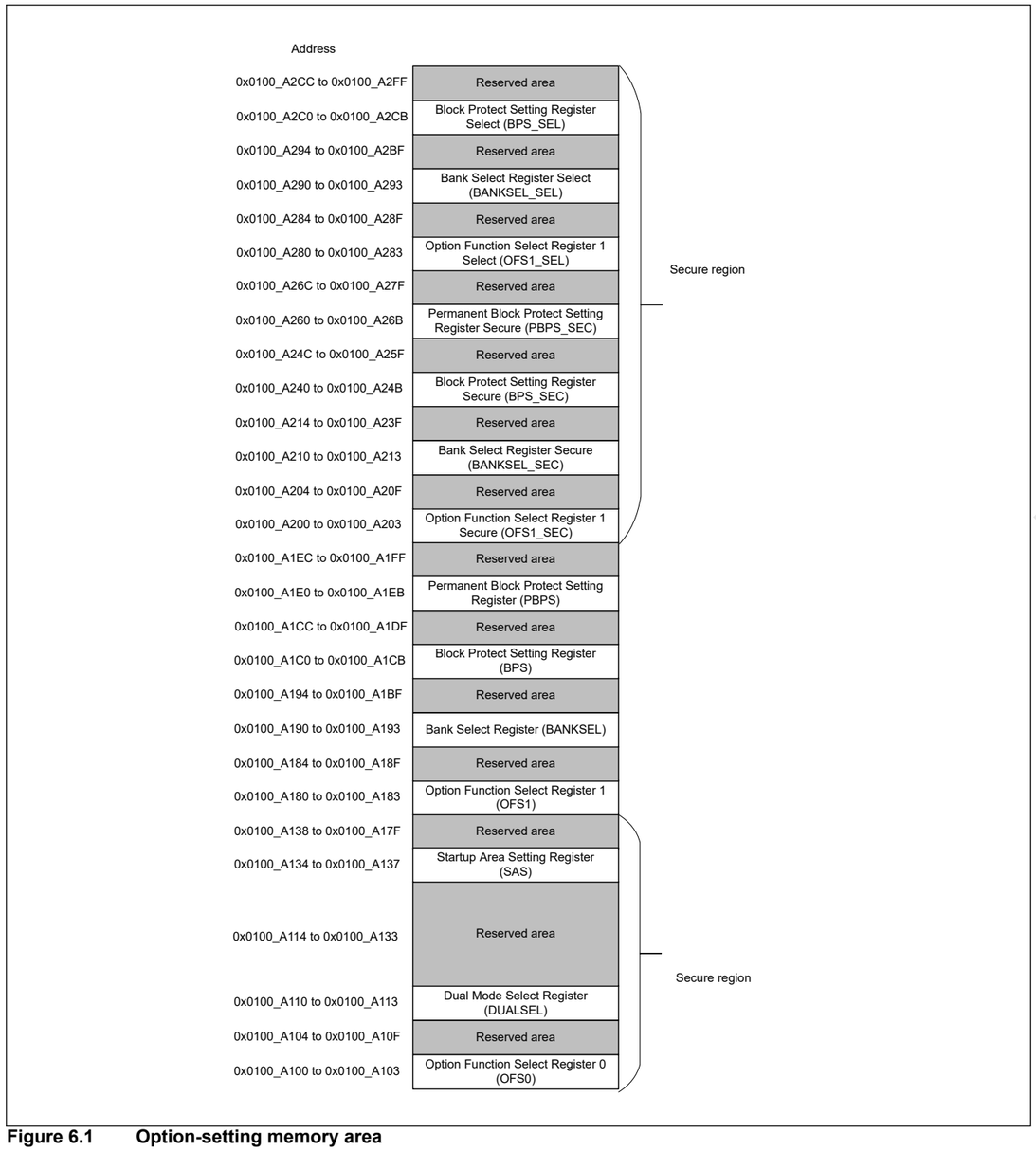


Figure 6.1 Option-setting memory area

6. Option-Setting Memory

6.1 Overview

选项设置存储器确定复位后MCU的状态。选项设置内存分配给闪存的配置设置区域。

图6.1显示了选项设置存储区。选项设置内存区域具有安全区域。表6.1显示了选项设置存储区的编程条件。

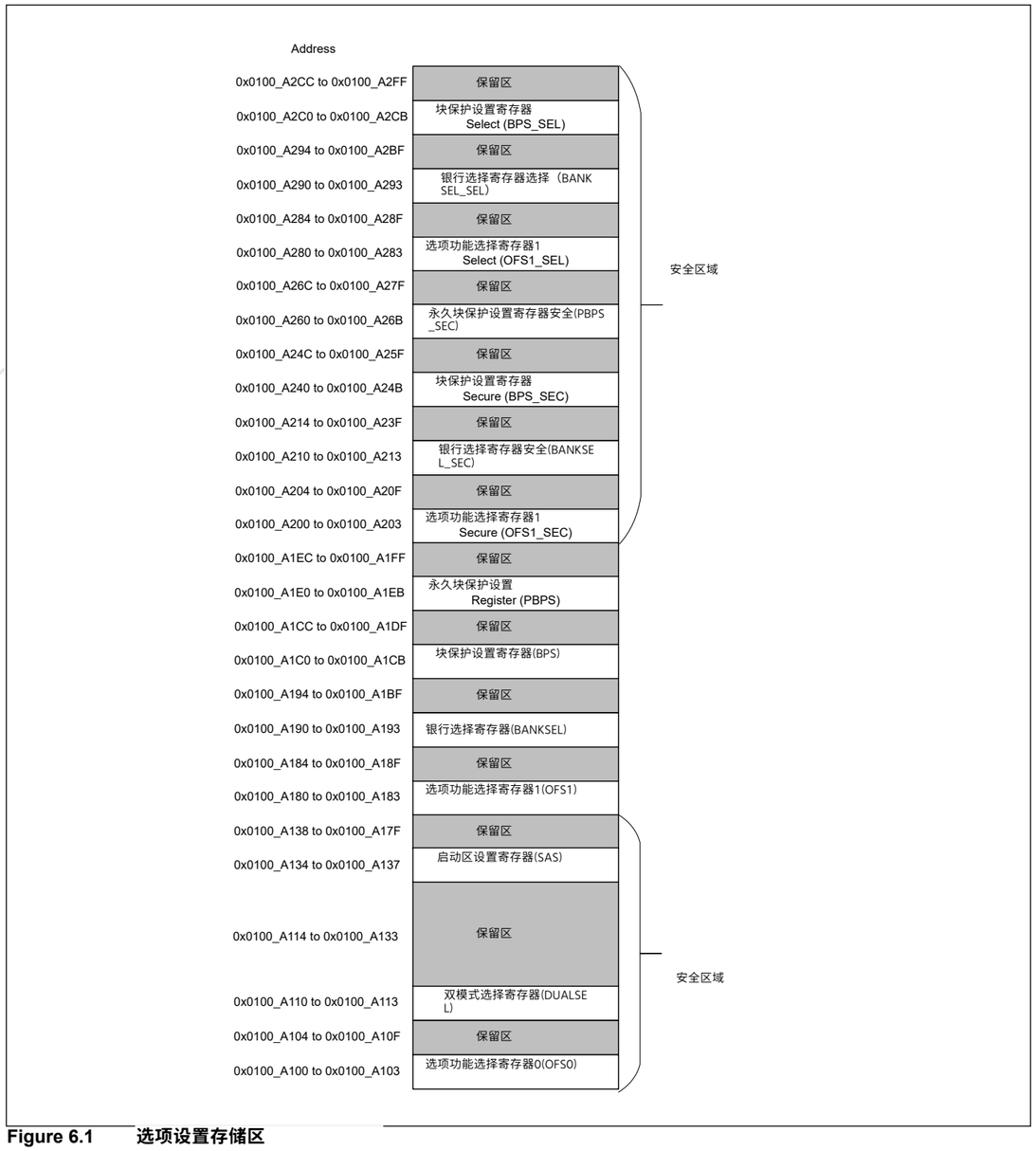


Figure 6.1 选项设置存储区

Table 6.1 The programming condition of the option-setting memory area

	Self programming	Serial programming	Programming by the on-chip debugger
Secure region	Programming commands issued by secure access.	Programming commands issued when the device life cycle is SSD.	Programming commands issued when the debug level is DBG2.
Other region	Programming commands issued by secure or non-secure access.	Programming commands issued when the devise life cycle is SSD or NSECSD.	Programming commands issued when the debug level is DBG2 or DBG1.

6.2 Register Descriptions

6.2.1 OFS0 : Option Function Select Register 0

Address: 0x0100_A100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
Value after reset:	User setting*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
Value after reset:	User setting*1															

Bit	Symbol	Function	R/W
0	—	When read, this bit returns the written value. The write value should be 1.	R
1	IWDTSTRT	IWDT Start Mode Select 0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT after a reset	R
3:2	IWDTTOPS[1:0]	IWDT Timeout Period Select 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: Setting prohibited	R
9:8	IWDTRPES[1:0]	IWDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
11:10	IWDTRPSS[1:0]	IWDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request 1: Enable reset	R

Table 6.1 选项设置存储区的编程条件

	自编程	串行编程	通过片上调试器进行编程
安全区域	安全访问发出的编程命令。	设备生命周期为SSD时发出的编程命令。	调试级别为DBG2时发出的编程命令。
其他地区	通过安全或非安全访问发出的编程命令。	设备生命周期为SSD或NSECSD时发出的编程命令。	调试级别为DBG2或DBG1时发出的编程命令。

6.2 注册说明

6.2.1 OFS0：选项功能选择寄存器0

Address: 0x0100_A100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	WDTSTPCTL	—	WDTRSTIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTSTRT	—
重置后的值：	用户设置*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	IWDTSTPCTL	—	IWDTRSTIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTSTRT	—
重置后的值：	用户设置*1															

Bit	Symbol	Function	R/W
0	—	读取时，该位返回写入的值。写入值应为1。	R
1	IWDTSTRT	IWDT启动模式选择 0：复位后自动激活IWDT（自动启动模式）1：复位后禁用IWDT	R
3:2	IWDTTOPS[1:0]	IWDT超时周期选择 0 0: 128 cycles (0x007F) 0 1: 512 cycles (0x01FF) 1 0: 1024 cycles (0x03FF) 1 1: 2048 cycles (0x07FF)	R
7:4	IWDTCKS[3:0]	IWDT-专用时钟分频比选择 0x0: × 1 0x2: × 1/16 0x3: × 1/32 0x4: × 1/64 0xF: × 1/128 0x5: × 1/256 Others: 禁止设定	R
9:8	IWDTRPES[1:0]	IWDT窗口结束位置选择 00：75%01：50%10：25%11：0%（无窗口结束位置设置）	R
11:10	IWDTRPSS[1:0]	IWDT窗口起始位置选择 00：25%01：50%10：75%11：100%（无窗口起始位置设置）	R
12	IWDTRSTIRQS	IWDT复位中断请求选择 0：使能不可屏蔽中断请求或中断请求1：使能复位	R

Bit	Symbol	Function	R/W
13	—	When read, this bit returns the written value. The write value should be 1.	R
14	IWDTSTPCTL	IWDT Stop Control 0: Continue counting 1: Stop counting when in Sleep, Snooze, or Software Standby mode	R
16:15	—	When read, these bits return the written value. The write value should be 1.	R
17	WDTSTRT	WDT Start Mode Select 0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode)	R
19:18	WDTTOPS[1:0]	WDT Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select 0x1: PCLKB divided by 4 0x4: PCLKB divided by 64 0xF: PCLKB divided by 128 0x6: PCLKB divided by 512 0x7: PCLKB divided by 2048 0x8: PCLKB divided by 8192 Others: Setting prohibited	R
25:24	WDTRPES[1:0]	WDT Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting)	R
27:26	WDTRPSS[1:0]	WDT Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting)	R
28	WDTRSTIRQS	WDT Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request 1: Reset	R
29	—	When read, these bits return the written value. The write value should be 1.	R
30	WDTSTPCTL	WDT Stop Control 0: Continue counting 1: Stop counting when entering Sleep mode	R
31	—	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the IWDT takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256. Using this setting combined with the IWDTTOPS[1:0] bits setting, the IWDT counting period can be set from 128 to 524288 IWDT clock cycles.

Bit	Symbol	Function	R/W
13	—	读取时，该位返回写入的值。写入值应为1。	R
14	IWDTSTPCTL	IWDT停止控制 0：继续计数1：在休眠、贪睡或软件待机模式下停止计数	R
16:15	—	读取时，这些位返回写入的值。写入值应为1。	R
17	WDTSTRT	WDT启动模式选择 0：复位后自动激活WDT（自动启动模式）1：复位后停止WDT（寄存器启动模式）	R
19:18	WDTTOPS[1:0]	WDT超时周期选择 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R
23:20	WDTCKS[3:0]	WDT时钟分频比选择 0x1：PCLKB4分频0x4：PCLKB64分频0xF：PCLKB128分频 0x6：PCLKB512分频0x7：PCLKB2048分频0x8：PCLKB8192分频 Others: 禁止设定	R
25:24	WDTRPES[1:0]	WDT窗口结束位置选择 00：75%01：50%10：25%11：0%（无窗口结束位置设置）	R
27:26	WDTRPSS[1:0]	WDT窗口起始位置选择 00：25%01：50%10：75%11：100%（无窗口起始位置设置）	R
28	WDTRSTIRQS	WDT复位中断请求选择 0：使能不可屏蔽中断请求或中断请求1：复位	R
29	—	读取时，这些位返回写入的值。写入值应为1。	R
30	WDTSTPCTL	WDT停止控制 0：继续计数1：进入休眠模式时停止计数	R
31	—	读取时，这些位返回写入的值。写入值应为1。	R

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

IWDTSTRT位（IWDT启动模式选择）

IWDTSTRT位选择复位后激活IWDT的模式（停止状态或激活状态）。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位指定超时周期，即递减计数器下溢所需的时间，为IWDTCKS[3中设置的分频时钟的128、512、1024或2048个周期：0]位。刷新操作后IWDT下溢所需的时钟周期数由IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于将IWDT的时钟频率分频为11、116、132、164、1128和1256的预分频器的分频比。将此设置与IWDTTOPS[1:0]位设置，IWDT计数周期可以设置为128到524288个IWDT时钟周期。

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window starts and ends positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The operation is selectable to an independent watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 25, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep mode, Snooze mode, or Software Standby mode.

For details, see section 25, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto start mode). When WDT is activated in auto start mode, the OFS0 register setting for the WDT is valid.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, that is, the time it takes for the down counter to underflow as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 24, Watchdog Timer (WDT).

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of PCLKB as 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192. Using this setting combined with the WDTTOPS[1:0] bits setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 24, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window on the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position, otherwise only the value for the window start position is valid.

The counter values associated with the settings for the start and end positions of the window in the WDTRPSS[1:0] and WDTRPES[1:0] bits vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 24, Watchdog Timer (WDT).

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值，否则只有窗口开始位置的值有效。

与IWDTRPSS[1:0]中窗口的开始和结束位置的设置相关的计数器值和IWDTRPES[1:0]位随IWDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始位置和结束位置之间的间隔成为可以刷新的时间段。在此期间之外无法刷新。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择独立看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位指定在进入休眠模式、贪睡模式或软件待机模式时是否停止计数。

有关详细信息，请参见第25节，独立看门狗定时器(IWDT)。

WDTSTRT位（WDT启动模式选择）

WDTSTRT位选择WDT在复位后激活的模式（停止状态或在自动启动模式下激活）。当WDT在自动启动模式下激活时，WDT的OFS0寄存器设置有效。

WDTOPS[1:0]位（WDT超时周期选择）

WDTTOPS[1:0]位指定超时周期，即在WDTCKS[3:0中设置的分频时钟的1024、4096、8192或16384个周期时，递减计数器下溢所需的时间。]位。刷新操作后下溢的PCLKB周期数由WDTCKS[3:0]和WDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTCKS[3:0]位（WDT时钟分频比选择）

WDTCKS[3:0]位指定用于分频PCLKB频率的预分频器的分频比为14、164、1128、1512、12048和18192。将此设置与WDTOPS[1:0]位设置，WDT计数周期可以设置为4096到134217728个PCLKB周期。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTRPES[1:0]位（WDT窗口结束位置选择）

WDTRPES[1:0]位指定递减计数器上窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值，否则只有窗口开始位置的值有效。

与WDTRPSS[1:0]中窗口的开始和结束位置设置相关的计数器值和WDTRPES[1:0]位随WDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the positions where the window starts and ends becomes the period in which a refresh is possible.

Refresh is not possible outside this period.

For details, see section 24, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down-counter or generation of a refresh error. The operation is selectable to a watchdog timer reset, a non-maskable interrupt request, or an interrupt request.

For details, see section 24, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode.

For details, see section 24, Watchdog Timer (WDT).

6.2.2 DUALSEL : Dual Mode Select Register

address: 0x0100_A110

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	BANKMD[2:0]		
Value after reset:	User setting*1															

Bit	Symbol	Function	R/W
2:0	BANKMD[2:0]	Bank Mode Select 0 0 0: Dual mode 1 1 1: Linear mode Others: Setting prohibited	R
31:3	—	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is 0xFFFF_FFFF. It is set to the value written by your application

BANKMD[2:0] bit (Bank Mode Select)

The BANKMD[2:0] bits select bank mode of the dual bank function of the code flash memory

6.2.3 SAS : Startup Area Setting Register

Address: 0x0100_A134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	User setting															

WDTRPSS[1:0]位（WDT窗口起始位置选择）

WDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始和结束位置之间的间隔成为可以刷新的时间段。

在此期间之外无法刷新。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTRSTIRQS位（WDT复位中断请求选择）

WDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。该操作可选择看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

WDTSTPCTL位（WDT停止控制）

WDTSTPCTL位指定进入休眠模式时是否停止计数。

有关详细信息，请参见第24节，看门狗定时器(WDT)。

6.2.2 DUALSEL:双模式选择寄存器

address: 0x0100_A110

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	用户设置*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	BANKMD[2:0]		
重置后的值:	用户设置*1															

Bit	Symbol	Function	R/W
2:0	BANKMD[2:0]	银行模式选择 000：双模式111： 线性模式 其他：禁止设置	R
31:3	—	读取时，这些位返回写入的值。写入值应为1。	R

注1.空白产品中的值为0xFFFF_FFFF。它设置为您的应用程序写入的值

BANKMD[2:0]位（组模式选择）

BANKMD[2:0]位选择代码闪存双组功能的组模式

6.2.3 SAS：启动区设置寄存器

Address: 0x0100_A134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	用户设置															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	用户设置															

Bit	Symbol	Function	R/W
14:0	—	When read, these bits return the written value. The write value should be 1.	R
15	FSPR	Protection of Startup Area Select Function This bit controls the programming of the write/erase protection for the Startup Area Select flag (SAS.BTFLG), and the temporary boot swap control. When this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the Startup Area Select flag (SAS.BTFLG) is invalid. 1: Executing the configuration setting command for programming the Startup Area Select flag (SAS.BTFLG) is valid.	R
30:16	—	When read, these bits return the written value. The write value should be 1.	R
31	BTFLG	Startup Area Select Flag This bit specifies whether the address of the startup area is exchanged for the boot swap function or not. In dual mode (the DUALSEL.BANKMD[2:0] bits are 000b), set 1 to this bit. 0: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are exchanged. 1: First 8-KB area (0x0000_0000 to 0x0000_1FFF) and second 8-KB area (0x0000_2000 to 0x0000_3FFF) are not exchanged.	R

6.2.4 OFS1, OFS1_SEC, OFS1_SEL : Option Function Select Register 1

Address: OFS1: 0x0100_A180
OFS1_SEC: 0x0100_A200
OFS1_SEL: 0x0100_A280

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	The value set by the user*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
Value after reset:	The value set by the user*1															

Bit	Symbol	Function	R/W
1:0	VDSEL[1:0]	Voltage Detection 0 Level Select 0 0: Setting prohibited 0 1: Select 2.94 V 1 0: Select 2.87 V 1 1: Select 2.80 V	R
2	LVDAS	Voltage Detection 0 Circuit Start 0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset	R
7:3	—	When read, these bits return the written value. The write value should be 1.	R
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset	R
10:9	HOCOFRQ0[1:0]	HOCO Frequency Setting 0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1: Setting prohibited	R
31:11	—	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

Bit	Symbol	Function	R/W
14:0	—	读取时，这些位返回写入的值。写入值应为1。	R
15	FSPR	保护启动区选择功能 该位控制启动区域选择标志(SAS.BTFLG)的写擦除保护的编程，以及临时引导交换控制。当该位设置为0时，不能更改为1。 0：执行用于编程启动区域选择标志（SAS.BTFLG）的配置设置命令无效。 1：执行用于编程启动区域选择标志（SAS.BTFLG）的配置设置命令有效。	R
30:16	—	读取时，这些位返回写入的值。写入值应为1。	R
31	BTFLG	启动区选择标志 该位指定是否将启动区域的地址交换为引导交换功能。在双模式下（DUALSEL.BANKMD[2:0]位为000b），将此位设置为1。 0：交换第一个8-KB区域（0x0000_0000到0x0000_1FFF）和第二个8-KB区域（0x0000_2000到0x0000_3FFF）。 1：第一个8-KB区域（0x0000_0000到0x0000_1FFF）和第二个8-KB区域（0x0000_2000到0x0000_3FFF）不交换。	R

6.2.4 OFS1、OFS1_SEC、OFS1_SEL：选项功能选择寄存器1

Address: OFS1: 0x0100_A180
OFS1_SEC: 0x0100_A200
OFS1_SEL: 0x0100_A280

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	用户设置的值*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL[1:0]	
重置后的值：	用户设置的值*1															

Bit	Symbol	Function	R/W
1:0	VDSEL[1:0]	电压检测0电平选择 00：禁止设置01：选择2.94V10：选择2.87V11：选择2.80V	R
2	LVDAS	电压检测0电路启动 0：启用电压监控0复位后复位1：禁用电压监控0复位后复位	R
7:3	—	读取时，这些位返回写入的值。写入值应为1。	R
8	HOCOEN	HOCO振荡使能 0：复位后启用HOCO振荡1：复位后禁用HOCO振荡	R
10:9	HOCOFRQ0[1:0]	HOCO频率设定0 00：16MHz01：18MHz10：20MHz11：禁止设置	R
31:11	—	读取时，这些位返回写入的值。写入值应为1。	R

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

Only secure developer can program OFS1_SEC and OFS1_SEL registers. OFS1_SEC register is for secure developer, and OFS1 register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in OFS1_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory.

VDSEL[1:0] bits (Voltage Detection 0 Level Select)

The VDSEL[1:0] bits select the voltage detection level of the voltage detection 0 circuit.

LVDAS bits (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enabled or disabled after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the Clock Source Select bits (SCKSCR.CKSEL[2:0]). To use the HOCO clock, you must set the OFS1.HOCOFRQ0 bit to an optimum value.

HOCOFRQ0[1:0] bits (HOCO Frequency Setting 0)

The HOCOFRQ0[1:0] bits specify the HOCO frequency after a reset as 16, 18, or 20 MHz.

6.2.5 BANKSEL, BANKSEL_SEC, BANKSEL_SEL : Bank Select Register

Address: BANKSEL: 0x0100_A190
BANKSEL_SEC: 0x0100_A210
BANKSEL_SEL: 0x0100_A290

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	BLCKSWP[7:0]							
Value after reset:	User setting*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	BANKSWP[2:0]		
Value after reset:	User setting*1															

Bit	Symbol	Function	R/W
2:0	BANKSWP[2:0]	Startup Bank Switch This setting is valid in dual mode. 0 0 0: Start address of Bank0 is 0x0020_0000 and Bnak1 is 0x0000_0000 in dual mode 1 1 1: Start address of Bank0 is 0x0000_0000 and Bnak1 is 0x0020_0000 in dual mode Others: Setting prohibited	R/W
15:3	—	When read, these bits return the written value. The write value should be 1.	R/W
23:16	BLCKSWP[7:0]	Block Swap Select When all bits are set to 1, the block swap is disabled. When at least one bit is set to 0, block swap is enabled and the corresponding blocks of code flash memory are swapped.	R/W
31:24	—	When read, these bits return the written value. The write value should be 1.	R/W

Note 1. The value in a blank product is 0xFFFF_FFFF. It is set to the value written by your application.

Only secure developer can program BANKSEL_SEC and BANK_SEL registers. BANKSEL_SEC register is for secure developer, and BANKSEL register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in BANKSEL_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory.

BANKSWP[2:0] bits (Startup Bank Switch)

The BANKSWP[2:0] bits select the start address of the bank0 and bank1 of code flash memory in dual mode. For details of the startup bank selection, see section 50.11.4.2. Selecting the Startup Bank.

只有安全的开发人员才能对OFS1_SEC和OFS1_SEL寄存器进行编程。OFS1_SEC寄存器用于安全开发者，OFS1寄存器用于非安全开发者。应用的设置值由OFS1_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。

VDSEL[1:0]位（电压检测0电平选择）

VDSEL[1:0]位选择电压检测0电路的电压检测电平。

LVDAS位（电压检测0电路启动）

LVDAS位选择在复位后是启用还是禁用电压监视器0复位。

HOCOEN位（HOCO振荡使能）

HOCOEN位选择在复位后是启用还是禁用HOCO振荡。将此位设置为0允许在CPU开始运行之前启动HOCO振荡，减少了振荡稳定的等待时间。

Note: 当HOCOEN位设置为0时，系统时钟源不切换到HOCO。系统时钟源只能通过设置时钟源选择位(SCKSCR.CKSEL[2:0])切换到HOCO。要使用HOCO时钟，您必须将OFS1.HOCOFRQ0位设置为最佳值。

HOCOFRQ0[1:0]位（HOCO频率设置0）

HOCOFRQ0[1:0]位指定复位后的HOCO频率为16、18或20MHz。

6.2.5 BANKSEL，BANKSEL_SEC，BANKSEL_SEL：银行选择寄存器

Address: BANKSEL: 0x0100_A190
BANKSEL_SEC: 0x0100_A210
BANKSEL_SEL: 0x0100_A290

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	BLCKSWP[7:0]							
重置后的值：	用户设置*1															

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	BANKSWP[2:0]		
重置后的值：	用户设置*1															

Bit	Symbol	Function	R/W
2:0	BANKSWP[2:0]	启动银行开关 此设置在双模式下有效。 000：双模式下Bank0起始地址为0x0020_0000，Bnak1为0x0000_0000111：双模式下Bank0起始地址为0x0000_0000，Bnak1为0x0020_0000 其他：禁止设置	R/W
15:3	—	读取时，这些位返回写入的值。写入值应为1。	R/W
23:16	BLCKSWP[7:0]	块交换选择 当所有位都设置为1时，禁用块交换。当至少一位设置为0时，启用块交换并交换相应的代码闪存块。	R/W
31:24	—	读取时，这些位返回写入的值。写入值应为1。	R/W

注1.空白产品中的值为0xFFFF_FFFF。它设置为您的应用程序写入的值。

只有安全的开发人员才能对BANKSEL_SEC和BANK_SEL寄存器进行编程。BANKSEL_SEC寄存器用于安全开发者，BANKSEL寄存器用于非安全开发者。应用的设置值由BANKSEL_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。

BANKSWP[2:0]位（启动组开关）

BANKSWP[2:0]位选择双模式下代码闪存的bank0和bank1的起始地址。关于启动银行选择的详细信息，请参见第50.11.4.2节。选择启动银行。

BLCKSWP[7:0] bit (Block Swap Select)

The BLCKSWP[7:0] bits enable the block swap and select the valid blocks of the code flash memory. Figure 6.2 shows the mapping of the flash memory. Table 6.2 shows the specification of BLCKSWP bits for each product. Unused bits are reserved and should be set to 1. For details of block swap, see section 50.11.5. Block Swap Function.

BLCKSWP[7:0]位（块交换选择）

BLCKSWP[7:0]位启用块交换并选择代码闪存的有效块。图6.2显示了闪存的映射。表6.2显示了每个产品的BLCKSWP位规格。未使用的位保留，应设置为1。有关块交换的详细信息，请参阅第50.11.5节。块交换功能。

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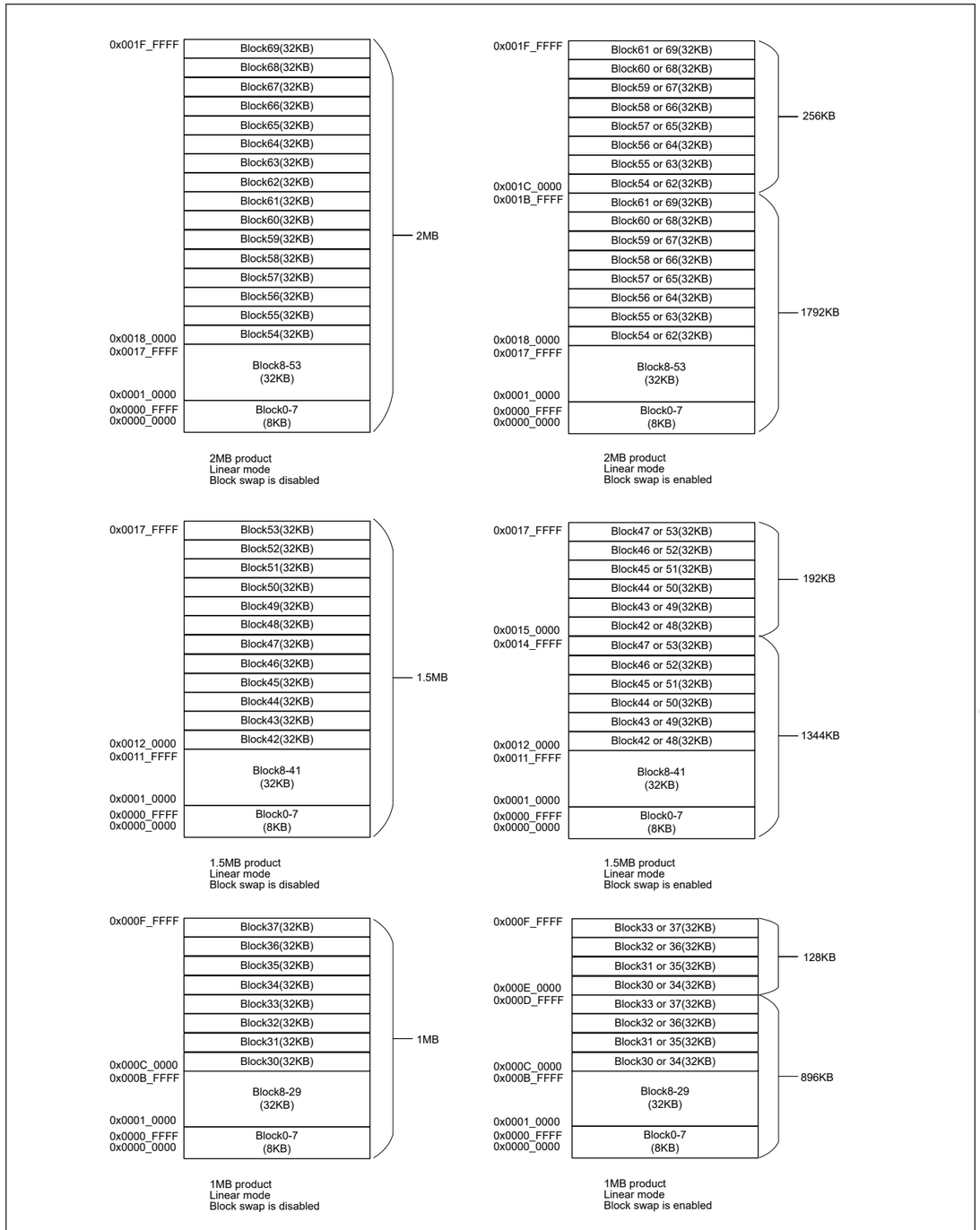

Figure 6.2 Mapping of the flash memory

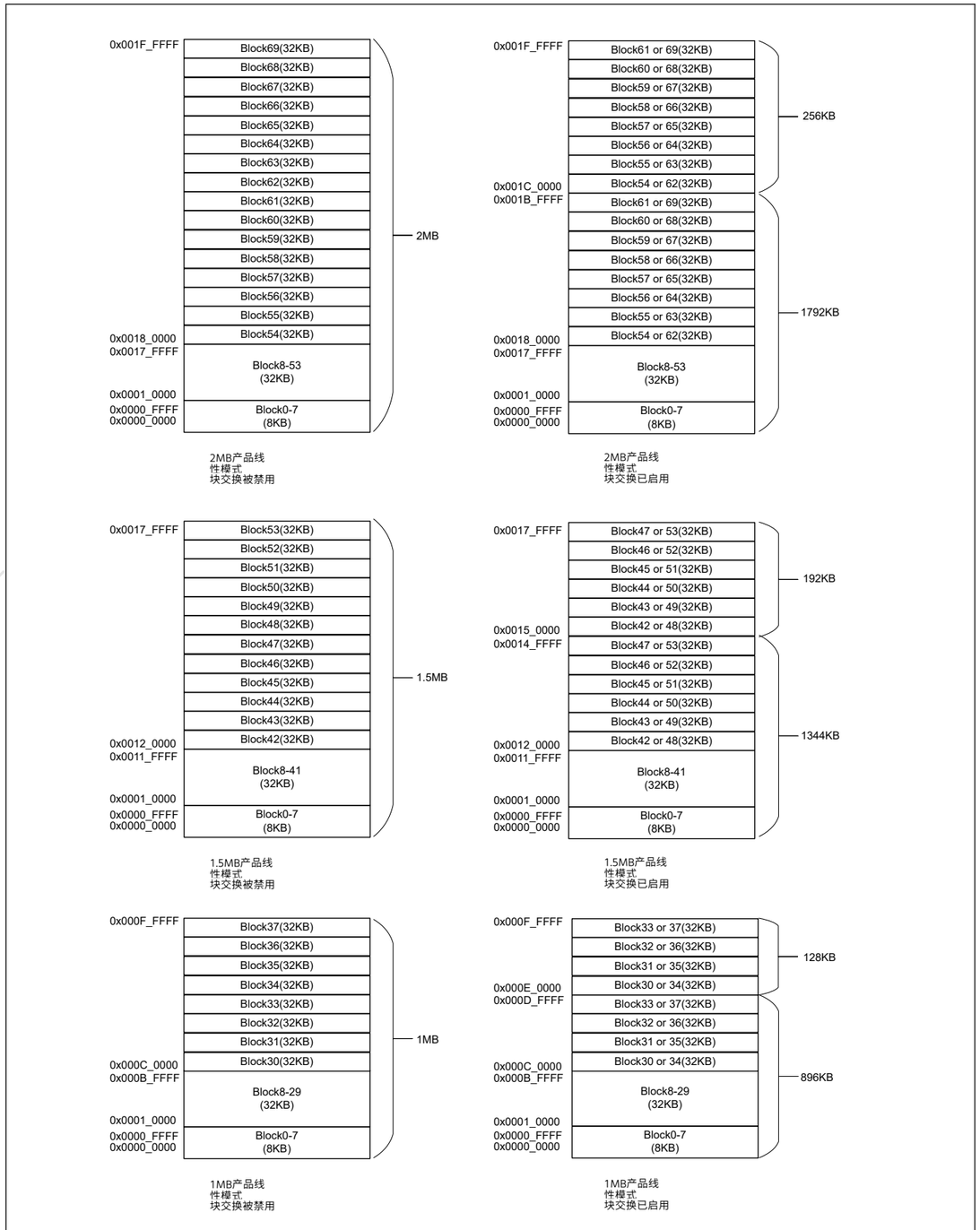

Figure 6.2 闪存映射

Table 6.2 Specification of BLCKSWP bits for each product

	BLCKSWP bits	Select 0 / 1
2 MB product	BLCKSWP[0]	1 : Block54 start address is 0x0018 0000. Block62 start address is 0x001C 0000. 0 : Block54 start address is 0x001C 0000. Block62 start address is 0x0018 0000.
	BLCKSWP[1]	1 : Block55 start address is 0x0018 8000. Block63 start address is 0x001C 8000. 0 : Block55 start address is 0x001C 8000. Block63 start address is 0x0018 8000.
	BLCKSWP[2]	1 : Block56 start address is 0x0019 0000. Block64 start address is 0x001D 0000. 0 : Block56 start address is 0x001D 0000. Block64 start address is 0x0019 0000.
	BLCKSWP[3]	1 : Block57 start address is 0x0019 8000. Block65 start address is 0x001D 8000. 0 : Block57 start address is 0x001D 8000. Block65 start address is 0x0019 8000.
	BLCKSWP[4]	1 : Block58 start address is 0x001A 0000. Block66 start address is 0x001E 0000. 0 : Block58 start address is 0x001E 0000. Block66 start address is 0x001A 0000.
	BLCKSWP[5]	1 : Block59 start address is 0x001A 8000. Block67 start address is 0x001E 8000. 0 : Block59 start address is 0x001E 8000. Block67 start address is 0x001A 8000.
	BLCKSWP[6]	1 : Block60 start address is 0x001B 0000. Block68 start address is 0x001F 0000. 0 : Block60 start address is 0x001F 0000. Block68 start address is 0x001B 0000.
	BLCKSWP[7]	1 : Block61 start address is 0x001B 8000. Block69 start address is 0x001F 8000. 0 : Block61 start address is 0x001F 8000. Block69 start address is 0x001B 8000.
1.5 MB product	BLCKSWP[0]	1 : Block42 start address is 0x0012 0000. Block48 start address is 0x0015 0000. 0 : Block42 start address is 0x0015 0000. Block48 start address is 0x0012 0000.
	BLCKSWP[1]	1 : Block43 start address is 0x0012 8000. Block49 start address is 0x0015 8000. 0 : Block43 start address is 0x0015 8000. Block49 start address is 0x0012 8000.
	BLCKSWP[2]	1 : Block44 start address is 0x0013 0000. Block50 start address is 0x0016 0000. 0 : Block44 start address is 0x0016 0000. Block50 start address is 0x0013 0000.
	BLCKSWP[3]	1 : Block45 start address is 0x0013 8000. Block51 start address is 0x0016 8000. 0 : Block45 start address is 0x0016 8000. Block51 start address is 0x0013 8000.
	BLCKSWP[4]	1 : Block46 start address is 0x0014 0000. Block52 start address is 0x0017 0000. 0 : Block46 start address is 0x0017 0000. Block52 start address is 0x0014 0000.
	BLCKSWP[5]	1 : Block47 start address is 0x0014 8000. Block53 start address is 0x0017 8000. 0 : Block47 start address is 0x0017 8000. Block53 start address is 0x0014 8000.
1 MB product	BLCKSWP[0]	1 : Block30 start address is 0x000C 0000. Block34 start address is 0x000E 0000. 0 : Block30 start address is 0x000E 0000. Block34 start address is 0x000C 0000.
	BLCKSWP[1]	1 : Block31 start address is 0x000C 8000. Block35 start address is 0x000E 8000. 0 : Block31 start address is 0x000E 8000. Block35 start address is 0x000C 8000.
	BLCKSWP[2]	1 : Block32 start address is 0x000D 0000. Block36 start address is 0x000F 0000. 0 : Block32 start address is 0x000F 0000. Block36 start address is 0x000D 0000.
	BLCKSWP[3]	1 : Block33 start address is 0x000D 8000. Block37 start address is 0x000F 8000. 0 : Block33 start address is 0x000F 8000. Block37 start address is 0x000D 8000.

6.2.6 BPS, BPS_SEC, BPS_SEL : Block Protect Setting Register

address:

BPS: 0x0100_A1C0, 0x0100_A1C4, 0x0100_A1C8
BPS_SEC: 0x0100_A240, 0x0100_A244, 0x0100_A248
BPS_SEL: 0x0100_A2C0, 0x0100_A2C4, 0x0100_A2C8

Bit position:	31	0
Bit field:		
Value after reset:	User setting*1	

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

Only secure developer can program BPS_SEC and BPS_SEL registers. BPS_SEC register is for secure developer, and BPS register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in BPS_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory.

Table 6.2 各产品的BLCKSWP位规格

	BLCKSWP bits	Select 0 / 1
2 MB product	BLCKSWP[0]	1：Block54起始地址为0x00180000。Block62起始地址为0x001C0000。0：Block54起始地址为0x001C0000。Block62起始地址为0x00180000。
	BLCKSWP[1]	1：Block55起始地址为0x00188000。Block63起始地址为0x001C8000。0：Block55起始地址为0x001C8000。Block63起始地址为0x00188000。
	BLCKSWP[2]	1：Block56起始地址为0x00190000。Block64起始地址为0x001D0000。0：Block56起始地址为0x001D0000。Block64起始地址为0x00190000。
	BLCKSWP[3]	1：Block57起始地址为0x00198000。Block65起始地址为0x001D8000。0：Block57起始地址为0x001D8000。Block65起始地址为0x00198000。
	BLCKSWP[4]	1：Block58起始地址为0x001A0000。Block66起始地址为0x001E0000。0：Block58起始地址为0x001E0000。Block66起始地址为0x001A0000。
	BLCKSWP[5]	1：Block59起始地址为0x001A8000。Block67起始地址为0x001E8000。0：Block59起始地址为0x001E8000。Block67起始地址为0x001A8000。
	BLCKSWP[6]	1：Block60起始地址为0x001B0000。Block68起始地址为0x001F0000。0：Block60起始地址为0x001F0000。Block68起始地址为0x001B0000。
	BLCKSWP[7]	1：Block61起始地址为0x001B8000。Block69起始地址为0x001F8000。0：Block61起始地址为0x001F8000。Block69起始地址为0x001B8000。
1.5 MB product	BLCKSWP[0]	1：Block42起始地址为0x00120000。Block48起始地址为0x00150000。0：Block42起始地址为0x00150000。Block48起始地址为0x00120000。
	BLCKSWP[1]	1：Block43起始地址为0x00128000。Block49起始地址为0x00158000。0：Block43起始地址为0x00158000。Block49起始地址为0x00128000。
	BLCKSWP[2]	1：Block44起始地址为0x00130000。Block50起始地址为0x00160000。0：Block44起始地址为0x00160000。Block50起始地址为0x00130000。
	BLCKSWP[3]	1：Block45起始地址为0x00138000。Block51起始地址为0x00168000。0：Block45起始地址为0x00168000。Block51起始地址为0x00138000。
	BLCKSWP[4]	1：Block46起始地址为0x00140000。Block52起始地址为0x00170000。0：Block46起始地址为0x00170000。Block52起始地址为0x00140000。
	BLCKSWP[5]	1：Block47起始地址为0x00148000。Block53起始地址为0x00178000。0：Block47起始地址为0x00178000。Block53起始地址为0x00148000。
1 MB product	BLCKSWP[0]	1：Block30起始地址为0x000C0000。Block34起始地址为0x000E0000。0：Block30起始地址为0x000E0000。Block34起始地址为0x000C0000。
	BLCKSWP[1]	1：Block31起始地址为0x000C8000。Block35起始地址为0x000E8000。0：Block31起始地址为0x000E8000。Block35起始地址为0x000C8000。
	BLCKSWP[2]	1：Block32起始地址为0x000D0000。Block36起始地址为0x000F0000。0：Block32起始地址为0x000F0000。Block36起始地址为0x000D0000。
	BLCKSWP[3]	1：Block33起始地址为0x000D8000。Block37起始地址为0x000F8000。0：Block33起始地址为0x000F8000。Block37起始地址为0x000D8000。

6.2.6 BPS、BPS_SEC、BPS_SEL：块保护设置寄存器

address:

BPS: 0x0100_A1C0, 0x0100_A1C4, 0x0100_A1C8
BPS_SEC: 0x0100_A240, 0x0100_A244, 0x0100_A248
BPS_SEL: 0x0100_A2C0, 0x0100_A2C4, 0x0100_A2C8

Bit position:	31	0
Bit field:		
重置后的值：	用户设置*1	

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

只有安全的开发人员才能对BPS_SEC和BPS_SEL寄存器进行编程。BPS_SEC寄存器用于安全开发者，BPS寄存器用于非安全开发者。应用的设置值由BPS_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。

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The BPS and BPS_SEC registers invalidate the programming and erasure to the code flash memory. When the bit of this register is set to 0, the programming and erasure to the corresponding block are invalid. Figure 6.3 shows the code flash block structure of each product. Figure 6.4 shows the relationship between the bit of register and the block number. Unused bits are reserved and should be set to 1.

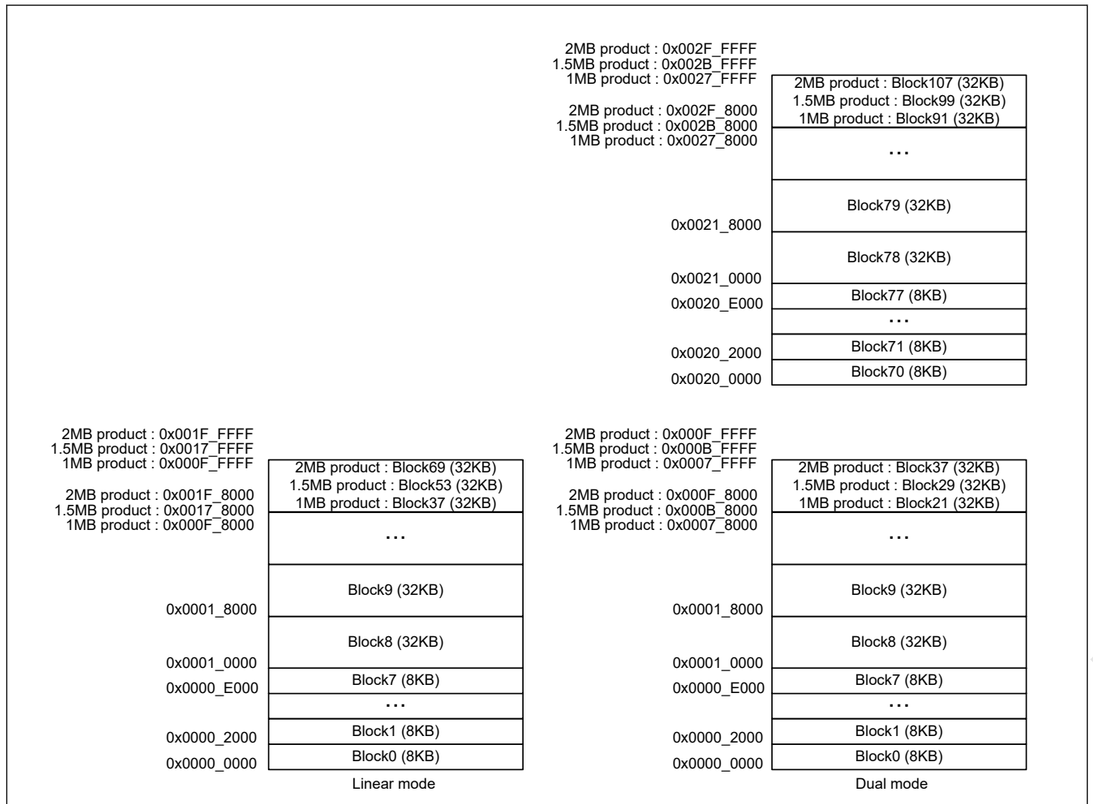

Figure 6.3 Code Flash block structure

Regiser	Address	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+ 9	+ 8	+ 7	+ 6	+ 5	+ 4	+ 3	+ 2	+ 1	+ 0
BPS_SEL	0x0100_A2C8					91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70						
	0x0100_A2C4																											37	36	35	34	33	32
	0x0100_A2C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS_SEC	0x0100_A248					91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70						
	0x0100_A244																											37	36	35	34	33	32
	0x0100_A240	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS	0x0100_A1C8					91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70						
	0x0100_A1C4																											37	36	35	34	33	32
	0x0100_A1C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6.4 The relationship between the bit of register and the block number

BPS和BPS_SEC寄存器使对代码闪存的编程和擦除无效。当该寄存器的位设置为0时，对相应块的编程和擦除无效。图6.3显示了每个产品的代码闪存块结构。图6.4显示了寄存器的位和块号之间的关系。未使用的位被保留，应设置为1。

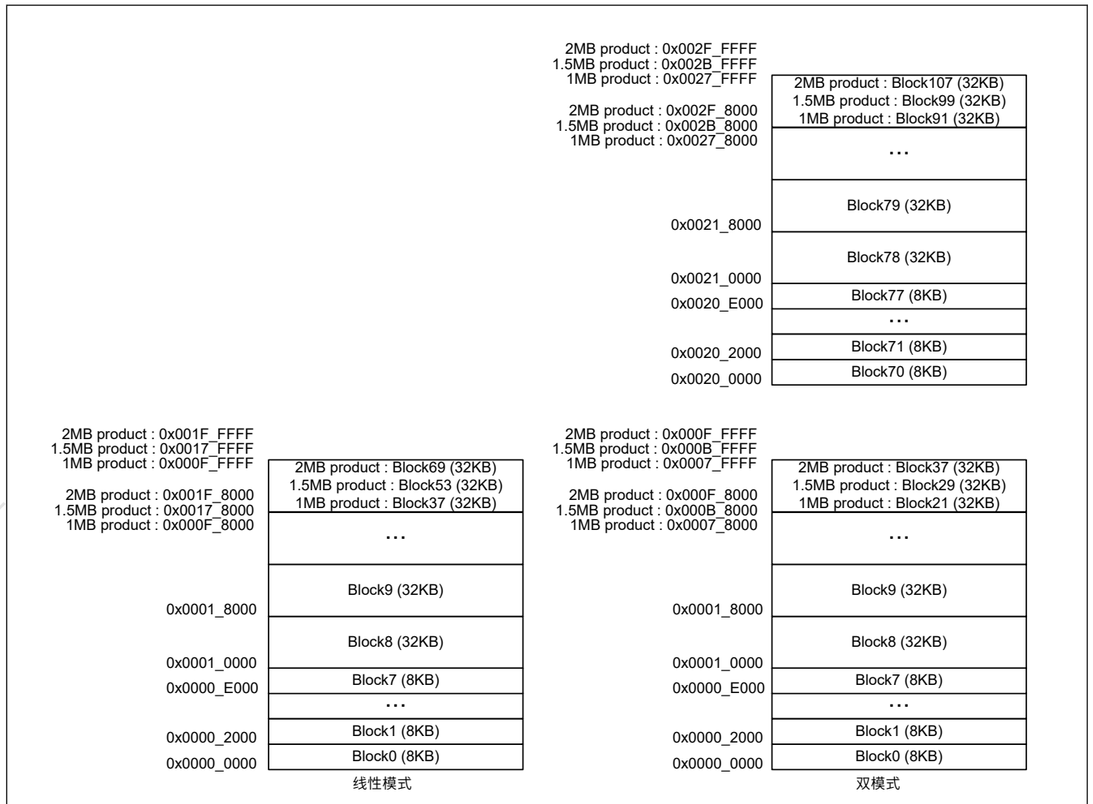

Figure 6.3 代码Flash块结构

Regiser	Address	+31	+30	+29	+28	+27	+26	+25	+24	+23	+22	+21	+20	+19	+18	+17	+16	+15	+14	+13	+12	+11	+10	+ 9	+ 8	+ 7	+ 6	+ 5	+ 4	+ 3	+ 2	+ 1	+ 0
BPS_SEL	0x0100_A2C8					91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70						
	0x0100_A2C4																											37	36	35	34	33	32
	0x0100_A2C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS_SEC	0x0100_A248					91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70						
	0x0100_A244																											37	36	35	34	33	32
	0x0100_A240	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	⋮																																
BPS	0x0100_A1C8					91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70						
	0x0100_A1C4																											37	36	35	34	33	32
	0x0100_A1C0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6.4 寄存器位与块号的关系

6.2.7 PBPS, PBPS_SEC : Permanent Block Protect Setting Register

Address: PBPS: 0x0100_A1E0, 0x0100_A1E4, 0x0100_A1E8
PBPS_SEC: 0x0100_A260, 0x0100_A264, 0x0100_A268

Bit position:	31	0
Bit field:		
Value after reset:	User setting*1	

Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

Only secure developer can program PBPS_SEC register. PBPS_SEC register is for secure developer, and PBPS register is for non-secure developer. The applied setting value is determined by the setting value of the corresponding bit in BPS_SEL register. For details, see section 6.3.3. Security attribution of option-setting memory. The security attribution register is same BPS_SEL register between the block protection and permanent block protection.

The PBPS and PBPS_SEC registers invalidate writes to bits of BPS and BPS_SEC. The bit of this register can be set to 0 when corresponding bit of BPS and BPS_SEC is set to 0. When the bit of this register is set to 0, writing the corresponding bit of BPS and BPS_SEC register is invalid. Once the bit of this register is set to 0, it is impossible to change the bit to 1. Table 6.3 shows the relationship between the bit of applied PBPS and bit of applied BPS.

The relationship between the bit of this register and the block number is same as BPS and BPS_SEC registers (section 6.2.6. BPS, BPS_SEC, BPS_SEL : Block Protect Setting Register). Unused bits are reserved and should be set to 1.

Table 6.3 The relationship between the bit of PBPS, PBPS_SEC and bit of BPS, BPS_SEC

The bit of applied PBPS	The bit of applied BPS	Content
1	1	Programming and erasure to the corresponding block is valid.
1	0	Programming and erasure to the corresponding block is invalid. This protection can be canceled by FBPROT0 or FBPROT1 registers.
0	1	Can not set this condition
0	0	Programming and erasure to the corresponding block is invalid permanently

6.3 Setting Option-Setting Memory

6.3.1 Allocation of Data in Option-Setting Memory

Programming data is allocated to the addresses in the option-setting memory shown in Figure 6.1. The allocated data is used by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

6.3.2 Setting Data for Programming Option-Setting Memory

Allocating data according to the procedure described in section 6.3.1. Allocation of Data in Option-Setting Memory, alone does not actually write the data to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

Use the configuration setting command to write data to the option-setting memory in the configuration setting area.

The option-setting memory does not support background operations (BGO). When write the option-setting memory, jump to SRAM after copying writing softwere to SRAM.

For details of the configuration setting command, see section 50, Flash Memory.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, see the tool manual for details.

The MCU provides two setting procedures:

6.2.7 PBPS PBPS_SEC:永久块保护设置寄存器

Address: PBPS: 0x0100_A1E0, 0x0100_A1E4, 0x0100_A1E8
PBPS_SEC: 0x0100_A260, 0x0100_A264, 0x0100_A268

Bit position:	31	0
Bit field:		
重置后的值:	用户设置*1	

注1.空白产品中的值为0xFFFFFFFF。它设置为您的应用程序写入的值。

只有安全的开发人员才能对PBPS_SEC寄存器进行编程。PBPS_SEC寄存器用于安全开发者，PBPS寄存器用于非安全开发者。应用的设置值由BPS_SEL寄存器中相应位的设置值决定。详见6.3.3节。选项设置内存的安全属性。安全属性寄存器与块保护和永久块保护之间的BPS_SEL寄存器相同。

PBPS和PBPS_SEC寄存器使对BPS和BPS_SEC位的写入无效。当BPS和BPS_SEC的对应位设置为0时，该寄存器的位可以设置为0。当该寄存器的位设置为0时，写入BPS和BPS_SEC寄存器的对应位无效。一旦该寄存器的位设置为0，就无法将该位更改为1。表6.3显示了应用PBPS的位和应用的BPS位之间的关系。

该寄存器的位与块号的关系与BPS和BPS_SEC寄存器相同（第6.2.6节）。
BPS、BPS_SEC、BPS_SEL：块保护设置寄存器）。未使用的位被保留，应设置为1。

Table 6.3 PBPS、PBPS_SEC的位与BPS、BPS_SEC的位的关系

应用PBPS的位	应用BPS的点滴	Content
1	1	对相应块的编程和擦除是有效的。
1	0	对相应块的编程和擦除无效。该保护可以通过FBPROT0或FBPROT1寄存器取消。
0	1	不能设置这个条件
0	0	对相应块的编程和擦除永久无效

6.3 设置选项设置内存

6.3.1 选项设置内存中的数据分配

编程数据被分配到图6.1所示的选项设置存储器中的地址。分配的数据由闪存编程软件或片上调试器等工具使用。

Note: 编程格式因编译器而异。有关详细信息，请参阅编译器手册。

6.3.2 编程选项设置存储器的设置数据

根据第6.3.1节中描述的程序分配数据。选项设置内存中的数据分配，单独并不实际将数据写入选项设置内存。您还必须遵循本节中描述的操作之一。

(1) 通过自编程更改选项设置存储器

使用配置设置命令将数据写入配置设置区的选项设置内存。

选项设置内存不支持后台操作(BGO)。写入选项设置内存时，跳转到
将写入软件复制到SRAM后的SRAM。

有关配置设置命令的详细信息，请参阅第50节，闪存。

(2) 通过OCD进行调试或通过闪存写入器进行编程

此过程取决于所使用的工具，详细信息请参见工具手册。

MCU提供两种设置程序：

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- Read the data allocated as described in section 6.3.1. Allocation of Data in Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data as allocated in section 6.3.1. Allocation of Data in Option-Setting Memory.

6.3.3 Security attribution of option-setting memory

Some functionality has 3 registers for non-secure (FUNC NAME), and secure (FUNC NAME_SEC), and security attribution (FUNC NAME_SEL). Only secure developer can set the registers for secure and security attribution. As shown in Figure 6.5, when the bit of security attribution register is set to 0, the corresponding bit of secure register is applied. When the bit of security attribution register is set to 1, the corresponding bit of non-secure register is applied.

For example, if the secure developer wants to configure LVD of OFS1 as secure, HOCO of OFS1 as non-secure, the secure developer needs to set OFS1_SEL as follows.

OFS1_SEL = 0xFFFF_FFF8

By this setting, LVDAS and VDSEL[1:0] values of OFS1_SEC and HOCOFRQ0[1:0] and HOCOEN values of OFS1 are applied to MCU. The reserved bits of the security attribution register (FUNC NAME_SEL) should be set to 1.

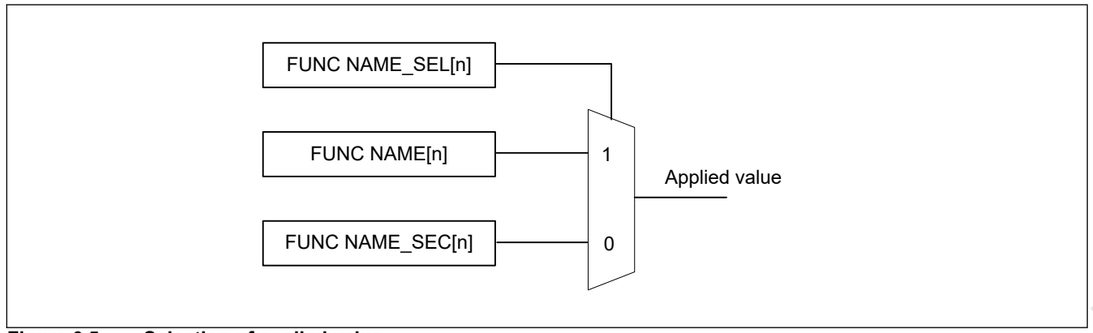

Figure 6.5 Selection of applied value

6.3.4 Timing of the Setting Value

For SAS, BPS, BPS_SEC, PBPS, and PBPS_SEC registers, the setting value of the related startup area and block protection is applied immediately after programming. For other registers, the setting value is applied after the MCU is reset.

In case the programming using the serial programming mode in customer's factory, be careful that the block protection for secure user is applied after MCU is reset. Because initial value of the security attribution registers of block protection (BPS_SEL) is 1 (non-secure), the block protection setting for secure developer (BPS_SEC/PBPS_SEC) is not applied until MCU is reset even if the corresponding bit of BPS_SEL is programmed to 0 (secure).

6.4 Usage Notes

6.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits of reserved areas and all reserved bits. If 0 is written to these bits, normal operation cannot be guaranteed.

●读取第6.3.1节所述分配的数据。在选项设置内存中分配数据，从编译器生成的目标文件或摩托罗拉S格式文件，并将数据写入MCU

●使用工具的GUI界面对6.3.1节分配的相同数据进行编程。OptionSetting内存中的数据分配。

6.3.3 选项设置内存的安全属性

某些功能具有3个用于非安全(FUNCNAME)、安全(FUNCNAME_SEC)和安全属性(FUNCNAME_SEL)的寄存器。只有安全的开发人员才能设置安全和安全属性的寄存器。如图6.5所示，当安全属性寄存器的位设置为0时，应用安全寄存器的相应位。当安全属性寄存器的位设置为1时，应用非安全寄存器的相应位。

例如，如果安全开发者要将OFS1的LVD配置为安全，将OFS1的HOCO配置为非安全，则安全开发者需要如下设置OFS1_SEL。

OFS1_SEL = 0xFFFF_FFF8

通过此设置，OFS1_SEC和HOCOFRQ0[1:0]的LVDAS和VDSEL[1:0]值以及OFS1的HOCOEN值将应用于MCU。安全属性寄存器(FUNCNAME_SEL)的保留位应设置为1。

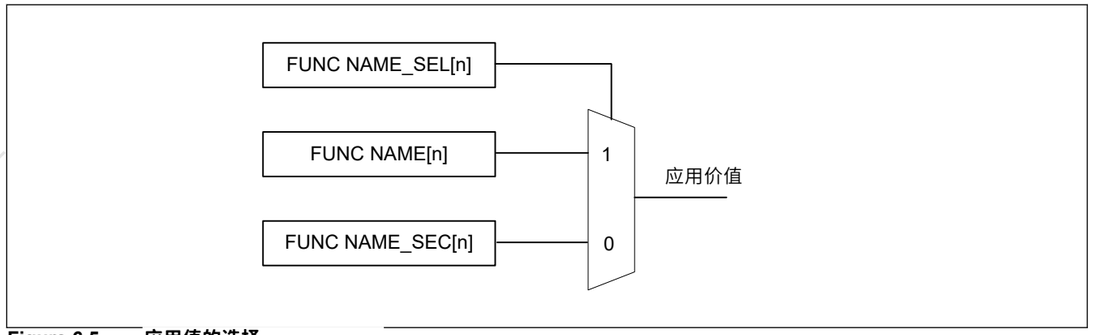

Figure 6.5 应用值的选择

6.3.4 设定值的时机

对于SAS、BPS、BPS_SEC、PBPS和PBPS_SEC寄存器，编程后立即应用相关启动区域和块保护的设置值。对于其他寄存器，设置值在MCU复位后应用。

如果在客户工厂使用串行编程模式进行编程，请注意在MCU复位后应用安全用户的块保护。由于块保护(BPS_SEL)的安全属性寄存器的初始值为1（非安全），因此即使BPS_SEL的相应位被编程为0（安全）。

6.4 使用说明

6.4.1 用于编程选项设置中的保留区域和保留位的数据 Memory

当期权设置内存中的保留区域和保留位在编程范围内时，将1写入保留区域和所有保留位的所有位。如果将0写入这些位，则无法保证正常操作。

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7. Low Voltage Detection (LVD)

7.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 7.1 lists the LVD specifications. Figure 7.1 shows a block diagram of the voltage monitor 0 reset generation circuit. Figure 7.2 shows a block diagram of the voltage monitor 1 interrupt and reset circuit, and Figure 7.3 shows a block diagram of the voltage monitor 2 interrupt and reset circuit.

Table 7.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1	Voltage monitor 2
Means for setting up operation		OFS1 register	Registers	Registers
Target for monitoring		VCC pin input voltage	VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det0}	V_{det1}	V_{det2}
Detected event		Voltage falls past V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
Detection voltage		Selectable from 3 different levels in the OFS1.VDSEL[1:0] bits	Selectable from 3 different levels in the LVD1CMPCR.LVD1LVL[4:0] bits	Selectable from 3 different levels in the LVD2CMPCR.LVD2LVL[2:0] bits
Monitoring flag		None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with either VCC > V_{det2} or V_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable interrupt selectable	Non-maskable or maskable interrupt selectable
			Interrupt request issued when V_{det1} > VCC and VCC > V_{det1} or either	Interrupt request issued when V_{det2} > VCC and VCC > V_{det2} or either
Digital filter	Switching between enable and disable	No digital filter function	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings
TrustZone Filter		—	Security attribution can be set for each registers	

7. 低电压检测(LVD)

7.1 Overview

低电压检测(LVD)模块监控输入到VCC引脚的电压电平。检测等级可以通过寄存器设置来选择。LVD模块由三个独立的电压电平检测器（LVD0、LVD1、LVD2）组成。LVD0、LVD1和LVD2测量输入到VCC引脚的电压电平。LVD寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。

电压监控寄存器用于配置LVD，以在超过阈值时触发中断、事件链接输出或复位。

表7.1列出了LVD规格。图7.1显示了电压监视器0复位产生电路的框图。
图7.2显示了电压监视器1中断和复位电路的框图，图7.3显示了电压监视器2中断和复位电路的框图。

Table 7.1 LVD specifications

Parameter		电压监视器0	电压监视器1	电压监测器2
设置操作的方法		OFS1 register	Registers	Registers
监测目标		VCC引脚输入电压	VCC引脚输入电压	VCC引脚输入电压
监控电压		V_{det0}	V_{det1}	V_{det2}
检测到的事件		电压下降超过Vdet0	电压上升或下降超过Vdet1	电压上升或下降超过Vdet2
检测电压		可从OFS1.VDSEL[1:0]位的3个不同级别中选择	可从LVD1CMPCR.LVD1LVL[4:0]位中的3个不同级别中选择	可从LVD2CMPCR.LVD2LVL[2:0]位中的3个不同级别中选择
监控标志		None	LVD1SR.MON标志：监控电压是高于还是低于Vdet1	LVD2SR.MON标志：监控电压是高于还是低于Vdet2
			LVD1SR.DET标志：Vdet1通过检测	LVD2SR.DET标志：Vdet2通过检测
电压检测流程	Reset	电压监控器0复位	电压监视器1复位	电压监视器2复位
		当Vdet0>VCC时复位 CPU在VCC>Vdet0指定时间后重启	当Vdet1>VCC时复位 CPU重启时间可选：在VCC>Vdet1或Vdet1>VCC的指定时间后	当Vdet2>VCC时复位 CPU重启时间可选：在VCC>Vdet2或Vdet2>VCC的指定时间后
	Interrupt	无中断	电压监视器1中断	电压监视器2中断
			可选择不可屏蔽或可屏蔽中断	可选择不可屏蔽或可屏蔽中断
			当Vdet1>时发出中断请求 VCC和VCC>Vdet1或	当Vdet2>VCC和VCC>Vdet2或任一时发出中断请求
数字滤波器	在启用和禁用之间切换	无数字滤波功能	Available	Available
	采样时间	—	1nLOCO频率×2(n:2 4 8 16)	1nLOCO频率×2(n:2 4 8 16)
事件链接功能		None	Available 在检测到Vdet1交叉点时输出事件信号	Available 在检测到Vdet2交叉点时输出事件信号
TrustZone Filter		—	可以为每个寄存器设置安全属性	

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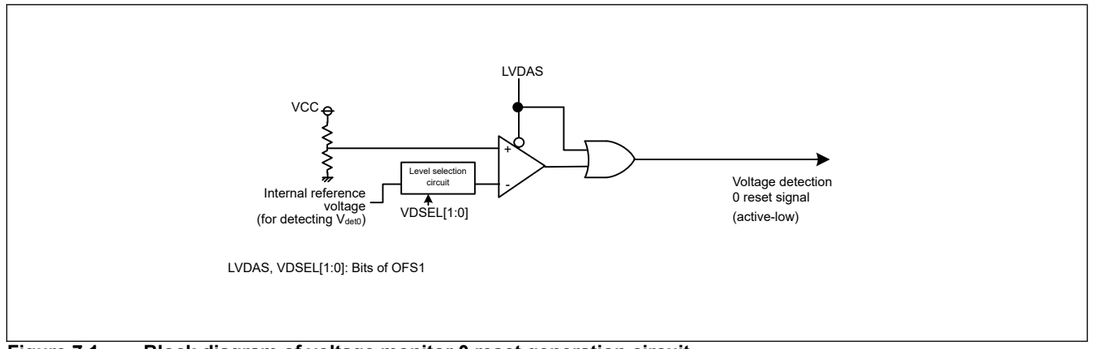


Figure 7.1 Block diagram of voltage monitor 0 reset generation circuit

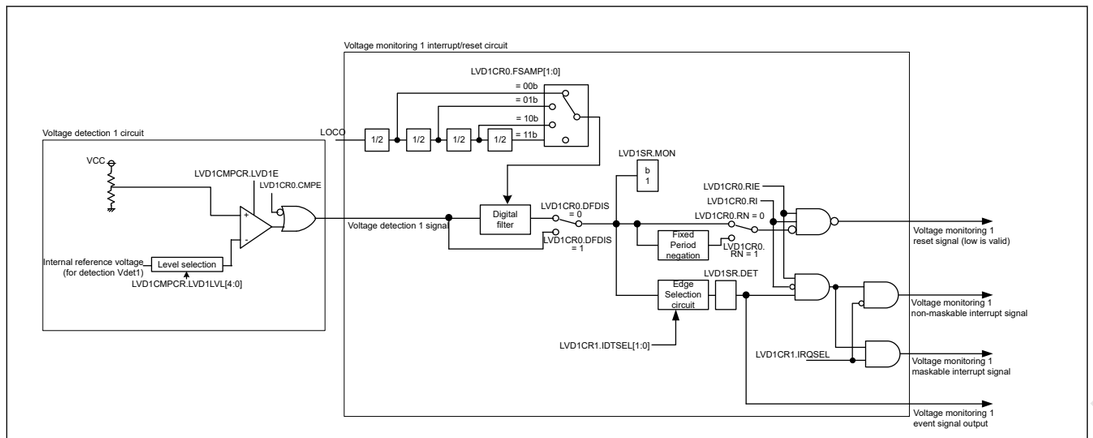


Figure 7.2 Block diagram of voltage monitor 1 interrupt and reset circuit

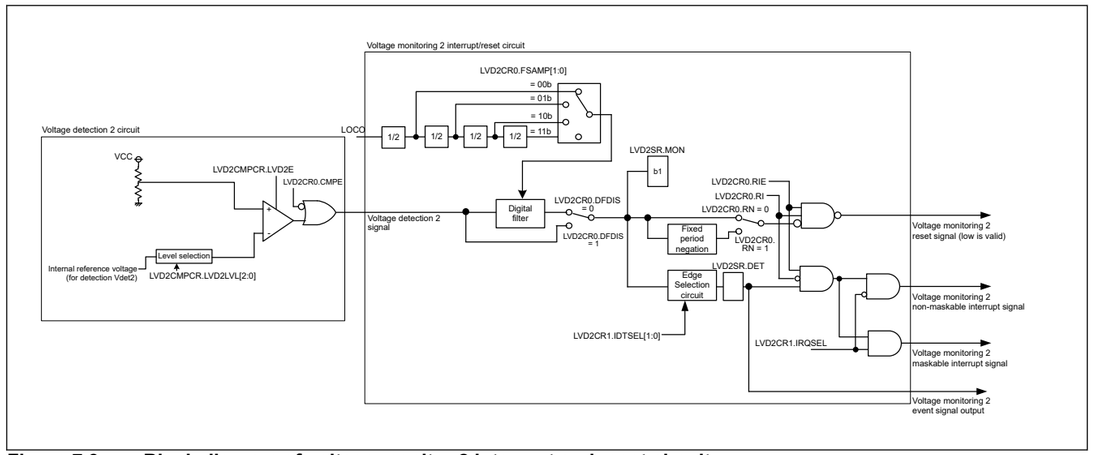


Figure 7.3 Block diagram of voltage monitor 2 interrupt and reset circuit

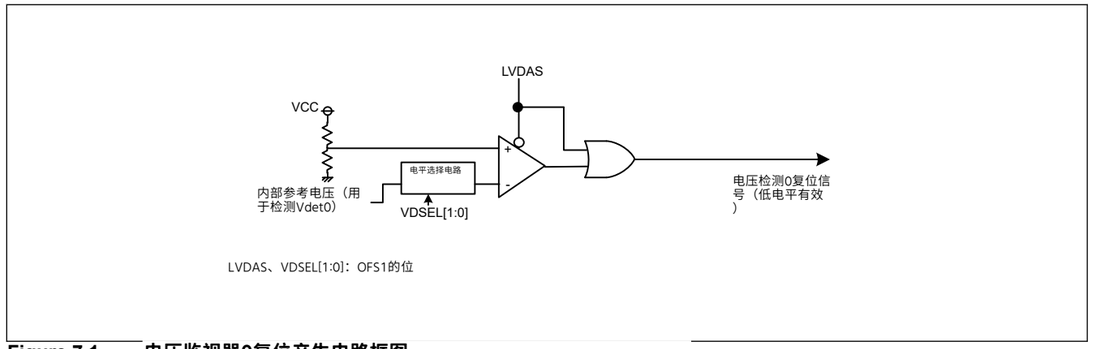


Figure 7.1 电压监视器0复位产生电路框图

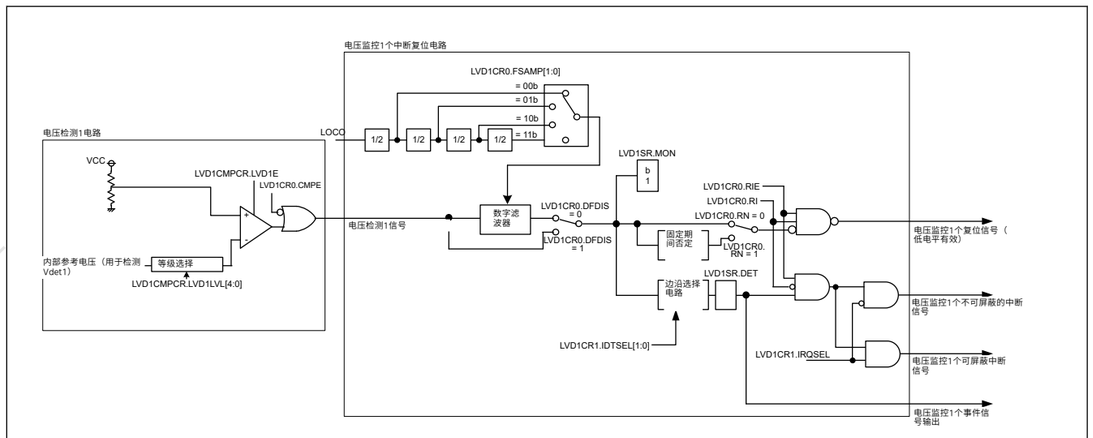


Figure 7.2 电压监测器1中断和复位电路框图

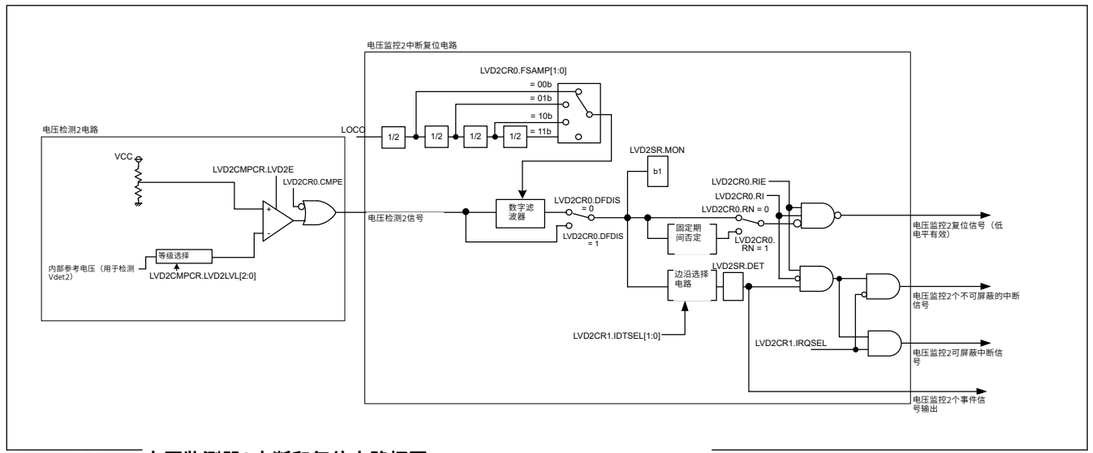


Figure 7.3 电压监测器2中断和复位电路框图

7.2 Register Descriptions

7.2.1 LVDSAR : Low Voltage Detection Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: registers for LVD1 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: registers for LVD2 0: Secure 1: Non Secure	R/W
31:2	—	These bits are read as 1. The write value must be 1 when it is possible to write.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

The LVDSAR register controls the secure attribute of LVD registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of LVD1CMPCR, LVD1CR0, LVD1CR1, LVD1SR.

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of LVD2CMPCR, LVD2CR0, LVD2CR1, LVD2SR.

7.2.2 LVD1CMPCR : Voltage Monitoring 1 Comparator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD1E	—	—	LVD1LVL[4:0]				
Value after reset:	0	0	0	1	0	0	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage) 0x11: 2.99 V (Vdet1_11) 0x12: 2.92 V (Vdet1_12) 0x13: 2.85 V (Vdet1_13) Others: Setting prohibited	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W

7.2 注册说明

7.2.1 LVDSAR：低电压检测安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC1	NONSEC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	非安全属性位0 目标寄存器：LVD1的寄存器 0：安全1：不 安全	R/W
1	NONSEC1	非安全属性位1 目标寄存器：LVD2的寄存器 0：安全1：不 安全	R/W
31:2	—	这些位被读取为1。当可以写入时，写入值必须为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

LVDSAR寄存器控制LVD寄存器的安全属性。

NONSEC0位（非安全属性位0）

该位控制LVD1CMPCR、LVD1CR0、LVD1CR1、LVD1SR的安全属性。

NONSEC1位（非安全属性位1）

该位控制LVD2CMPCR、LVD2CR0、LVD2CR1、LVD2SR的安全属性。

7.2.2 LVD1CMPCR:电压监测1比较器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x417

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD1E	—	—	LVD1LVL[4:0]				
重置后的值：	0	0	0	1	0	0	1	1

Bit	Symbol	Function	R/W
4:0	LVD1LVL[4:0]	电压检测1电平选择（电压下降时的标准电压） 0x11: 2.99 V (Vdet1_11) 0x12: 2.92 V (Vdet1_12) 0x13: 2.85 V (Vdet1_13) 其他：禁止设置	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	LVD1E	Voltage Detection 1 Enable 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The LVD1CMPCR.LVD1LVL can be changed only if the LVD1CMPCR.LVD1E and LVD2CMPCR.LVD2E bits are both 0. The voltage detection circuits 1 and 2 should not be set at the same voltage detection level.

Please do not change LVD1CMPCR.LVD1LVL and LVD1CMPCR.LVD1E at the same time.

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts once td(E-A) passes after the LVD1E bit value is changed from 0 to 1. When using the voltage detection 1 circuit in deep software standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

7.2.3 LVD2CMPCR : Voltage Monitoring 2 Comparator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2E	—	—	—	—	LVD2LVL[2:0]		
Value after reset:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	LVD2LVL[2:0]	Voltage Detection 2 Level Select (Standard voltage during drop in voltage) 1 0 1: 2.99 V (Vdet2_5) 1 1 0: 2.92 V (Vdet2_6) 1 1 1: 2.85 V (Vdet2_7) Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LVD2E	Voltage Detection 2 Enable 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The LVD2CMPCR.LVD2LVL can be changed only if the LVD1CMPCR.LVD1E and LVD2CMPCR.LVD2E bits are both 0. The voltage detection circuits 1 and 2 should not be set at the same voltage detection level.

Do not change LVD2CMPCR.LVD2LVL and LVD2CMPCR.LVD2E at the same time.

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON bit, set the LVD2E bit to 1. The voltage detection 2 circuit starts once td(E-A) passes after the LVD2E bit value is changed from 0 to 1. When using the voltage detection 2 circuit in deep software standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

Bit	Symbol	Function	R/W
7	LVD1E	电压检测1使能 0：电压检测1电路无效1：电压检测1电路有效	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVD1CMPCR.LVD1LVL只有在LVD1CMPCR.LVD1E和LVD2CMPCR.LVD2E位均为0时才能更改。电压检测电路1和2不应设置为相同的电压检测电平。

请不要同时更改LVD1CMPCR.LVD1LVL和LVD1CMPCR.LVD1E。

LVD1E位（电压检测1使能）

使用电压检测1中断复位或LVD1SR.MON位时，将LVD1E位设置为1。LVD1E位值从0变为1后，一旦经过td(E-A)，电压检测1电路就会启动。使用电压检测时1电路处于深度软件待机模式，请勿将DPSBYCR.DEEPCUT[1:0]位设置为11b。

7.2.3 LVD2CMPCR:电压监测2比较器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x418

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LVD2E	—	—	—	—	LVD2LVL[2:0]		
重置后的值:	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	LVD2LVL[2:0]	电压检测2电平选择（电压下降时的标准电压） 1 0 1: 2.99 V (Vdet2_5) 1 1 0: 2.92 V (Vdet2_6) 1 1 1: 2.85 V (Vdet2_7) 其他：禁止设置	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	LVD2E	电压检测2使能 0：电压检测2电路无效1：电压检测2电路有效	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVD2CMPCR.LVD2LVL只有在LVD1CMPCR.LVD1E和LVD2CMPCR.LVD2E位均为0时才能更改。电压检测电路1和2不应设置为相同的电压检测电平。

不要同时更改LVD2CMPCR.LVD2LVL和LVD2CMPCR.LVD2E。

LVD2E位（电压检测2使能）

使用电压检测2中断复位或LVD2SR.MON位时，将LVD2E位设置为1。LVD2E位值从0变为1后，一旦经过td(E-A)，电压检测2电路就会启动。使用电压检测时2电路处于深度软件待机模式，请勿将DPSBYCR.DEEPCUT[1:0]位设置为11b。

7.2.4 LVD1CR0 : Voltage Monitor 1 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 1 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	DFDIS	Voltage monitor 1 Digital Filter Disabled Mode Select 0: Enable the digital filter 1: Disable the digital filter	R/W
2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable 0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	FSAMP[1:0]	Sampling Clock Select 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency	R/W
6	RI	Voltage Monitor 1 Circuit Mode Select 0: Generate voltage monitor 1 interrupt on V_{det1} crossing 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}	R/W
7	RN	Voltage Monitor 1 Reset Negate Select 0: Negate after a stabilization time (t_{LVD1}) when VCC > V_{det1} is detected 1: Negate after a stabilization time (t_{LVD1}) on assertion of the LVD1 reset	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 1 interrupt/reset. Ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage monitor 1 Digital Filter Disabled Mode Select)

The DFDIS bit disables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) when this bit is 0(enabled). Set this bit to 1 (disabled) when using the voltage monitor 1 circuit in Software Standby mode or in Deep Software Standby mode.

CMPE bit (Voltage Monitor 1 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 1 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 1 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 1 circut, disable the voltage detection 1 circuit after setting the CMPE bit is 0.

FSAMP[1:0] bits (Sampling Clock Select)

The FSAMP[1:0] bits can be rewritten only when the LVD1CR0.DFDIS bit is 1 (digital filter circuit disabled). Do not rewrite these bits if the LVD1CR0.DFDIS bit is 0 (digital filter circuit enabled).

7.2.4 LVD1CR0：电压监视器1电路控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x41A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值：	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	电压监视器1中断复位使能 0：禁用1 ：启用	R/W
1	DFDIS	电压监视器1数字滤波器禁用模式选择 0：启用数字滤波器1：禁用数字滤波器	R/W
2	CMPE	电压监视器1电路比较结果输出使能 0：禁止电压监视1电路比较结果输出1：使能电压监视1电路比较结果输出	R/W
3	—	读取值未定义。写入值应为1。	R/W
5:4	FSAMP[1:0]	采样时钟选择 00:12LOCO频率01:14LOCO频率10:18LOCO频率11:116LOCO频率	R/W
6	RI	电压监视器1电路模式选择 0：在Vdet1交叉时产生电压监视器1中断1：当电压下降到或低于Vdet1时使能电压监视器1复位	R/W
7	RN	电压监视器1复位否定选择 0：在检测到VCC>Vdet1时在稳定时间(tLVD1)后取反1：在LVD1复位有效时在稳定时间(tLVD1)后取反	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器1中断复位使能）

RIE位启用或禁用电压监视器1中断复位。确保在对闪存进行编程或擦除期间，既不会产生电压监视器1中断，也不会产生电压监视器1复位。

DFDIS位（电压监视器1数字滤波器禁用模式选择）

DFDIS位禁用数字滤波器电路。当该位为0（启用）时，将LOCOCR.LCSTP位设置为0（LOCO运行）。在软件待机模式或深度软件待机模式下使用电压监视器1电路时，将此位设置为1（禁用）。

CMPE位（电压监视器1电路比较结果输出使能）

CMPE位启用或禁用电压监视器1电路比较结果输出。在电压检测1电路使能并经过稳定时间(td(E-A))后，将CMPE位设置为1。停止电压检测1电路时，将CMPE位设置为0后禁用电压检测1电路。

FSAMP[1:0]位（采样时钟选择）

只有当LVD1CR0.DFDIS位为1（数字滤波器电路禁用）时，FSAMP[1:0]位才能被重写。如果LVD1CR0.DFDIS位为0（启用数字滤波器电路），请勿重写这些位。

RA生态工作室

RI bit (Voltage Monitor 1 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 1 reset selected), transition to Deep Software Standby mode cannot be made. In this case, transition to Software Standby mode is made. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 1 interrupt selected).

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is set to 1 (negation follows a stabilization time on assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). In addition, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows stabilization time when VCC > V_{det1} is detected). Do not set the RN bit to 1 when this is the case.

7.2.5 LVD2CR0 : Voltage Monitor 2 Circuit Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	Voltage Monitor 2 Interrupt/Reset Enable 0: Disable 1: Enable	R/W
1	DFDIS	Voltage monitor 2 Digital Filter Disabled Mode Select 0: Enable the digital filter 1: Disable the digital filter	R/W
2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable 0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output	R/W
3	—	The read value is undefined. The write value should be 1.	R/W
5:4	FSAMP[1:0]	Sampling Clock Select 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency	R/W
6	RI	Voltage Monitor 2 Circuit Mode Select 0: Generate voltage monitor 2 interrupt on V_{det2} crossing 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}	R/W
7	RN	Voltage Monitor 2 Reset Negate Select 0: Negate after a stabilization time (t_{LVD2}) when VCC > V_{det2} is detected 1: Negate after a stabilization time (t_{LVD2}) on assertion of the LVD2 reset	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables the voltage monitor 2 interrupt/reset. Ensure that neither a voltage monitor 2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

RI位（电压监视器1电路模式选择）

当RI位为1（选择电压监视器1复位）时，无法转换到深度软件待机模式。在这种情况下，将转换到软件待机模式。要进入深度软件待机模式，请将RI位设置为0（选择电压监视器1中断）。

RN位（电压监视器1复位否定选择）

如果RN位设置为1（否定遵循LVD1复位信号断言的稳定时间），设置LOCOCR.LCSTP位为0（LOCO运行）。此外，为了转换到软件待机或深度软件待机模式，RN位的唯一可能值为0（当检测到VCC>Vdet1时，取反跟随稳定时间）。在这种情况下，请勿将RN位设置为1。

7.2.5 LVD2CR0：电压监视器2电路控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x41B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值：	1	0	0	0	x	0	1	0

Bit	Symbol	Function	R/W
0	RIE	电压监视器2中断复位使能 0：禁用1 ：启用	R/W
1	DFDIS	电压监视器2数字滤波器禁用模式选择 0：启用数字滤波器1：禁用数字滤波器	R/W
2	CMPE	电压监视器2电路比较结果输出使能 0：禁止电压监视2电路比较结果输出1：使能电压监视2电路比较结果输出	R/W
3	—	读取值未定义。写入值应为1。	R/W
5:4	FSAMP[1:0]	采样时钟选择 00:12LOCO频率01:14LOCO频率10:18LOCO频率11:116LOCO频率	R/W
6	RI	电压监视器2电路模式选择 0：在Vdet2交叉时产生电压监视器2中断1：当电压下降到或低于Vdet2时使能电压监视器2复位	R/W
7	RN	电压监视器2复位否定选择 0：在检测到VCC>Vdet2时在稳定时间(tLVD2)后取反1：在LVD2复位有效时在稳定时间(tLVD2)后取反	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

RIE位（电压监视器2中断复位使能）

RIE位启用或禁用电压监视器2中断复位。确保在对闪存进行编程或擦除期间，既不会产生电压监视器2中断，也不会产生电压监视器2复位。

RA生态工作室

DFDIS bit (Voltage monitor 2 Digital Filter Disabled Mode Select)

The DFDIS bit disables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) when this bit is 0 (digital filter enabled). Set this bit to 1 (digital filter disabled) when using the voltage monitor 2 circuit in Software Standby mode or in Deep Software Standby mode.

CMPE bit (Voltage Monitor 2 Circuit Comparison Result Output Enable)

The CMPE bit enables or disables voltage monitor 2 circuit comparison result output. Set the CMPE bit to 1 after the voltage detection 2 circuit enables and stabilization time ($t_{d(E-A)}$) elapses. When stopping the voltage detection 2 circut, disable the voltage detection 2 circuit after setting the CMPE bit is 0.

FSAMP[1:0] bits (Sampling Clock Select)

The FSAMP[1:0] bits can be rewritten only when the LVD2CR0.DFDIS bit is 1 (digital filter circuit disabled). Do not rewrite these bits if the LVD2CR0.DFDIS bit is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 2 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 2 reset selected), transition to Deep Software Standby mode cannot be made. In this case, transition to Software Standby mode is made. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 2 interrupt selected).

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is set to 1 (negating LVD2 reset in a specified time after its assertion), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, for a transition to Software Standby or Deep Software Standby mode, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det2} is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD2 reset signal) when this is the case.

7.2.6 LVD1CR1 : Voltage Monitor 1 Circuit Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 1 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.

Note 1. When enabling maskable interrupts, do not change the NMIER.LVD1EN bit value in the ICU from the reset state.

DFDIS位（电压监视器2数字滤波器禁用模式选择）

DFDIS位禁用数字滤波器电路。当该位为0（启用数字滤波器）时，将LOCOCR.LCSTP位设置为0（LOCO运行）。在软件待机模式或深度软件待机模式下使用电压监视器2电路时，将此位设置为1（禁用数字滤波器）。

CMPE位（电压监视器2电路比较结果输出使能）

CMPE位启用或禁用电压监视器2电路比较结果输出。在电压检测2电路使能且稳定时间(td(E-A))过后，将CMPE位设置为1。停止电压检测2电路时，将CMPE位设置为0后禁用电压检测2电路。

FSAMP[1:0]位（采样时钟选择）

只有当LVD2CR0.DFDIS位为1（数字滤波器电路禁用）时，FSAMP[1:0]位才能被重写。如果LVD2CR0.DFDIS位为0（启用数字滤波器电路），请勿重写这些位。

RI位（电压监视器2电路模式选择）

当RI位为1（选择电压监视器2复位）时，无法转换到深度软件待机模式。在这种情况下，将转换到软件待机模式。要进入深度软件待机模式，请将RI位设置为0（选择电压监视器2中断）。

RN位（电压监视器2复位否定选择）

如果RN位设置为1（在其断言后的指定时间内否定LVD2复位），则将LOCOCR.LCSTP位设置为0（LOCO运行）。此外，为了转换到软件待机或深度软件待机模式，RN位的唯一可能值是0（当检测到VCC>Vdet2时，取反遵循稳定时间）。在这种情况下，请勿将RN位设置为1（在LVD2复位信号置位后的稳定时间之后取反）。

7.2.6 LVD1CR1：电压监视器1电路控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	电压监视器1中断发生条件选择 00：检测到VCC≥Vdet1（上升）时01：检测到VCC<Vdet1（下降）时10：检测到下降和上升时11：禁止设置	R/W
2	IRQSEL	电压监视器1中断类型选择 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

注1.当使能可屏蔽中断时，不要从复位状态更改ICU中的NMIER.LVD1EN位值。

7.2.7 LVD1SR : Voltage Monitor 1 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 1 Voltage Variation Detection Flag 0: Not detected 1: V_{det1} crossing is detected	R/W*1
1	MON	Voltage Monitor 1 Signal Monitor Flag 0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Variation Detection Flag)

The DET flag is enabled when the LVD1CMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

When detecting V_{det1}, set the DET flag to 0 after setting LVD1CR0.RIE is 0 (disabled). When setting LVD1CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVD1CMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

7.2.8 LVD2CR1 : Voltage Monitor 2 Circuit Control Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	Voltage Monitor 2 Interrupt Generation Condition Select 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited	R/W
2	IRQSEL	Voltage Monitor 2 Interrupt Type Select 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W

7.2.7 LVD1SR:电压监视器1电路状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	电压监视器1电压变化检测标志 0：未检测到1：检测到Vdet 1交叉	R/W*1
1	MON	电压监视器1信号监视器标志 0：VCC<Vdet11：VCC≥Vdet1或M ON被禁用	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

注1.该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器1电压变化检测标志）

当LVD1CMPCR.LVD1E位为1（使能电压检测1电路）且LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

检测Vdet1时，将LVD1CR0.RIE设置为0（禁用）后，将DET标志设置为0。在将LVD1CR0.RIE位设置为0后将其设置为1（启用）时，等待2个或更多PCLKB周期已过去。

MON标志（电压监控1信号监控标志）

当LVD1CMPCR.LVD1E位为1（使能电压检测1电路）且LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

7.2.8 LVD2CR1：电压监视器2电路控制寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x0E2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	IDTSEL[1:0]	电压监视器2中断发生条件选择 00：检测到VCC≥Vdet2（上升）时01： 检测到VCC<Vdet2（下降）时10：检测到 下降和上升时11：禁止设置	R/W
2	IRQSEL	电压监视器2中断类型选择 0: Non-maskable interrupt 1: Maskable interrupt*1	R/W

Bit	Symbol	Function	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (writing enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the NMIER.LVD2EN bit value in the ICU from the reset state.

7.2.9 LVD2SR : Voltage Monitor 2 Circuit Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	Voltage Monitor 2 Voltage Variation Detection Flag 0: Not detected 1: V_{det2} crossing is detected	R/W*1
1	MON	Voltage Monitor 2 Signal Monitor Flag 0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Variation Detection Flag)

The DET flag is enabled when the LVD2CMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

Set the DET flag to 0 after setting LVD2CR0.RIE is 0 (disabled). When setting LVD2CR0.RIE bit to 1 (enabled) after setting it to 0, wait for 2 or more PCLKB cycles which have elapsed.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVD2CMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

7.3 VCC Input Voltage Monitor

7.3.1 Monitoring V_{det0}

The comparison results from voltage monitor 0 are not available for reading.

7.3.2 Monitoring V_{det1}

Table 7.2 shows the procedures to set up monitoring against V_{det1}. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

Bit	Symbol	Function	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.当启用可屏蔽中断时，不要从复位状态更改ICU中的NMIER.LVD2EN位值。

7.2.9 LVD2SR：电压监视器2电路状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0E3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MON	DET
重置后的值：	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
0	DET	电压监视器2电压变化检测标志 0：未检测到1：检测到Vdet2交叉	R/W*1
1	MON	电压监视器2信号监视器标志 0：VCC<Vdet21：VCC≥Vdet2或MON被禁用	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
注1.该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器2电压变化检测标志）

当LVD2CMPCR.LVD2E位为1（使能电压检测2电路）且LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

设置LVD2CR0.RIE为0（禁用）后，将DET标志设置为0。在将LVD2CR0.RIE位设置为0后将其设置为1（启用）时，等待2个或更多PCLKB周期已过去。

MON标志（电压监控2信号监控标志）

当LVD2CMPCR.LVD2E位为1（电压检测2电路使能）且LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

7.3 VCC输入电压监视器

7.3.1 Monitoring V_{det0}

电压监视器0的比较结果不可读取。

7.3.2 Monitoring V_{det1}

表7.2显示了针对Vdet1设置监控的程序。设置完成后，电压监视器1的比较结果可以通过LVD1SR.MON标志进行监视。

Table 7.2 Procedures to set up monitoring against V_{det1}

Step		Monitoring the comparison results from voltage monitor 1
Setting up the voltage detection 1 circuit	1	Set LVD1CMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVD1CMPCR.LVD1LVL[4:0] bits.
	2	Select the detection voltage in the LVD1CMPCR.LVD1LVL[4:0] bits.
	3	Set LVD1CMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

Note 1. Steps 5 to 7 can be performed during the wait time of step 4. For details of $t_{d(E-A)}$, see section 53, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

7.3.3 Monitoring V_{det2}

Table 7.3 shows the procedures to set up monitoring against V_{det2}. After the settings are complete, the comparison results from voltage monitor 2 can be monitored in the LVD2SR.MON flag.

Table 7.3 Procedures to set up monitoring against V_{det2}

Step		Monitoring the results of comparison by voltage monitor 2
Setting up the voltage detection 2 circuit	1	Set LVD2CMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVD2CMPCR.LVD2LVL[2:0] bits.
	2	Select the detection voltage in the LVD2CMPCR.LVD2LVL[2:0] bits.
	3	Set LVD2CMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1
Setting the digital filter*2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.

Note 1. Steps 5 to 7 can be performed during the wait time of step 4. For details of $t_{d(E-A)}$, see section 53, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

7.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Figure 7.4 shows an example of operations for a voltage monitor 0 reset.

Table 7.2 针对Vdet1设置监控的程序

Step		从电压监视器1监视比较结果
设置电压检测1电路	1	设置LVD1CMPCR.LVD1E=0以在写入之前禁用电压检测1 LVD1CMPCR.LVD1LVL[4:0] bits.
	2	在LVD1CMPCR.LVD1LVL[4:0]位中选择检测电压。
	3	设置LVD1CMPCR.LVD1E=1以启用电压检测1电路。
	4	启用LVD1后，至少等待td(E-A)的LVD1操作稳定时间。*1
设置数字滤波器*2	5	在LVD1CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。
	6	设置LVD1CR0.DFDIS=0以启用数字滤波器。
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。
启用输出	8	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。

注1.可以在步骤4的等待时间内执行步骤5至7。有关td(E-A)的详细信息，请参阅第53节，电气特性。
注2.如果不使用数字滤波器，则不需要步骤5至7。

7.3.3 Monitoring V_{det2}

表7.3显示了针对Vdet2设置监控的程序。设置完成后，可以在LVD2SR.MON标志中监控电压监视器2的比较结果。

Table 7.3 针对Vdet2设置监控的程序

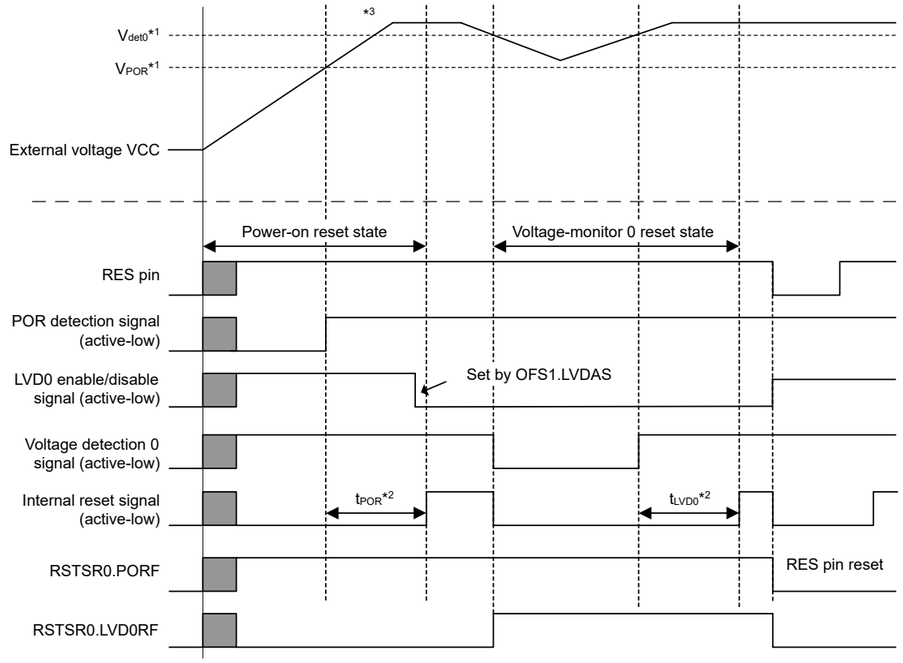
Step		通过电压监视器2监视比较结果
设置电压检测2电路	1	设置LVD2CMPCR.LVD2E=0以在写入之前禁用电压检测2 LVD2CMPCR.LVD2LVL[2:0] bits.
	2	在LVD2CMPCR.LVD2LVL[2:0]位中选择检测电压。
	3	设置LVD2CMPCR.LVD2E=1以启用电压检测2电路。
	4	启用LVD2后，至少等待td(E-A)的LVD2操作稳定时间。*1
设置数字滤波器*2	5	在LVD2CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。
	6	设置LVD2CR0.DFDIS=0以启用数字滤波器。
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。
启用输出	8	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。

注1.可以在步骤4的等待时间内执行步骤5至7。有关td(E-A)的详细信息，请参阅第53节，电气特性。
注2.如果不使用数字滤波器，则不需要步骤5至7。

7.4 从电压监视器复位0

使用电压监控器0复位时，将OFS1.LVDAS位清零以在复位后启用电压监控器0复位。但是，在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。

图7.4显示了电压监视器0复位的操作示例。



Note: For details of the electrical characteristics, see section 53, Electrical Characteristics.
Note 1. V_{POR} indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. t_{POR}: the period of a power-on reset.
t_{LVD0}: the period of a voltage monitor 0 reset.
Note 3. At power-on, the POR reset is released after VCC has reached the minimum guaranteed voltage.

Figure 7.4 Example of voltage monitor 0 reset operation

7.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 1 circuit.

Table 7.4 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring occurs. Table 7.5 shows the procedures for setting bits related to the voltage monitor 1 interrupt/reset so that voltage monitoring stops. Figure 7.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 5.2 in section 5, Resets.

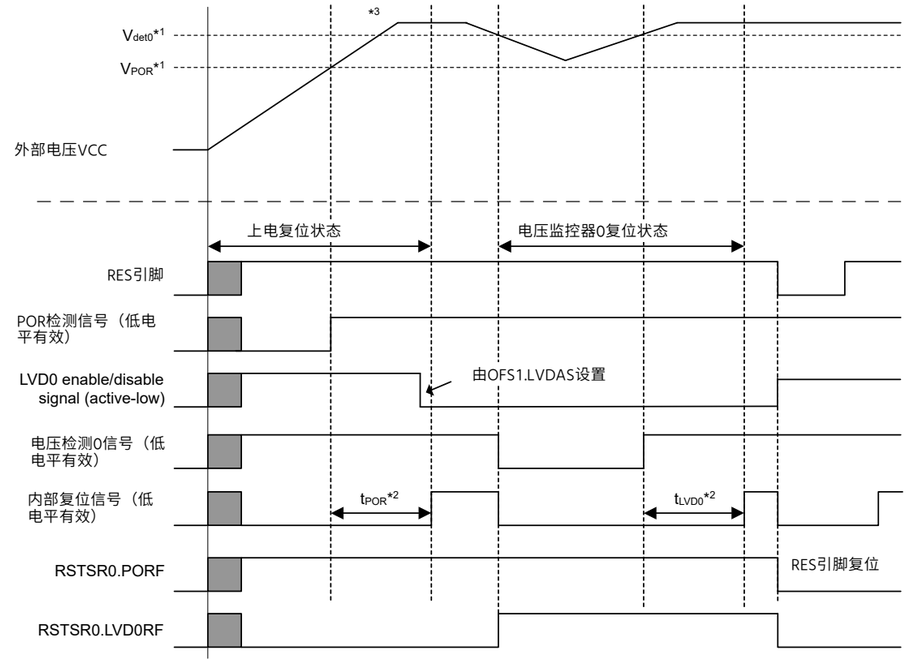
When using the voltage monitor 1 circuit in Software Standby mode or Deep Software Standby mode, set up the circuit using the procedures in this section.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1).
- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1).



Note: 有关电气特性的详细信息，请参阅第53节，电气特性。
注1.VPOR表示上电复位的检测电平，Vdet0表示电压监视器0复位的检测电平。

注2.tPOR：上电复位周期。
tLVD0:电压监视器0复位的周期。
注3.上电时，当VCC达到最低保证电压后，POR复位被释放。

Figure 7.4 电压监视器0复位操作示例

7.5 电压监视器1的中断和复位

响应电压监视器1电路的比较结果，可以产生中断或复位。

表7.4显示了设置与电压监控1中断复位相关的位以进行电压监控的过程。表7.5显示了设置与电压监控1中断复位相关的位以停止电压监控的步骤。图7.5显示了电压监视器1中断的操作示例。有关电压监视器1复位的操作，请参见第5节“复位”中的图5.2。

在软件待机模式或深度软件待机模式下使用电压监视器1电路时，请使用本节中的步骤设置电路。

(1) 在软件待机模式下设置

●禁用数字滤波器（LVD1CR0.DFDIS=1）。
●当检测到VCC>Vdet1时，在经过一段稳定时间后将电压监视器1复位信号(LVD1CR0.RN=0)取反。

(2) 深度软件待机模式中的设置

●禁用数字滤波器（LVD1CR0.DFDIS=1）。

- Enable the voltage monitor 1 interrupt (LVD1CR0.RI = 0). If the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 1 circuit stops. To use the voltage monitor 1 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 7.4 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring occurs

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting up the voltage detection 1 circuit	1	Set LVD1CMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVD1CMPCR register.	
	2	Select the detection voltage in the LVD1CMPCR.LVD1LVL[4:0] bits.	
	3	Set LVD1CMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD1 operation stabilization time after LVD1 is enabled.*1	
Setting the digital filter*3	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.	
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 1 interrupt or reset	8	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset. • Select the type of reset negation in the LVD1CR0.RN bit.
	9	• Select the interrupt request condition in the LVD1CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD1CR1.IRQSEL bit.	—
Enabling output	10	Set LVD1SR.DET = 0.	
	11	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*2	
	12	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d\ (E-A)}$, see section 53, Electrical Characteristics.
Note 2. Step 11 is not required if only the ELC event signal is to be output.
Note 3. Steps 5 to 7 are not required if the digital filter is not in use.
Note 4. Steps 8 to 11 can be performed during the wait time of step 7.

Table 7.5 Procedures for setting bits related to voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Stopping the enabling output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 1.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*2
	3	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*1
Stopping the digital filter	4	Set LVD1CR0.DFDIS = 1 to disable the digital filter.*2 *3
Stopping the voltage detection 1 circuit	5	Set LVD1CMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Step 3 is not required if only the ELC event signal is to be output.
Note 2. Steps 2 and 4 are not required if the digital filter is not in use.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 1 circuit is not required if the settings for the circuit do not change.

●启用电压监视器1中断(LVD1CR0.RI=0)。如果使能电压监视器1复位(LVD1CR0.RI=1)，则无法转换到深度软件待机模式，而是将操作转换到软件待机模式。

●当DPSBYCR.DEEPCUT[1:0]位为11b时，电压监视器1电路停止。要在深度软件待机模式下使用电压监视器1电路，请将DPSBYCR.DEEPCUT[1:0]位设置为11b以外的值。

Table 7.4 设置与电压监控器1中断和电压监控器1相关的位以进行电压监控的步骤

Step		电压监视器1中断（电压监视器1 ELC event output)	电压监视器1复位
设置电压检测1电路	1	设置LVD1CMPCR.LVD1E=0以在写入LVD1CMPCR寄存器之前禁用电压检测1。	
	2	在LVD1CMPCR.LVD1LVL[4:0]位中选择检测电压。	
	3	设置LVD1CMPCR.LVD1E=1以启用电压检测1电路。	
	4	启用LVD1后，至少等待td(E-A)的LVD1操作稳定时间。*1	
设置数字滤波器*3	5	在LVD1CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。	
	6	设置LVD1CR0.DFDIS=0以启用数字滤波器。	
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，并且数字滤波器的采样时钟是LOCO频率除以n。*4	
设置电压监视器1中断或复位	8	设置LVD1CR0.RI=0以选择电压监视器1中断。	• 设置LVD1CR0.RI=1以选择电压监视器1复位。 • 选择复位否定的类型 LVD1CR0.RN bit.
	9	• 选择中断请求条件 LVD1CR1.IDTSEL[1:0] bits. • 选择中断类型 LVD1CR1.IRQSEL bit.	—
启用输出	10	Set LVD1SR.DET = 0.	
	11	设置LVD1CR0.RIE=1以启用电压监视器1中断或复位。*2	
	12	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。	

注1.步骤5到11可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参阅第53节，电气特性。
注2.如果只输出ELC事件信号，则不需要步骤11。
注3.如果不使用数字滤波器，则不需要步骤5至7。
注4.步骤7的等待时间内可以执行步骤8至11。

Table 7.5 设置与电压监控1中断和电压监控1相关的位以使电压监控停止的步骤

Step		电压监视器1中断（电压监视器1ELC事件输出），电压监视器1复位
停止使能输出	1	设置LVD1CR0.CMPE=0以禁用电压监视器1的比较结果输出。
	2	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。*2
	3	设置LVD1CR0.RIE=0以禁用电压监视器1中断或复位。*1
停止数字滤波器	4	设置LVD1CR0.DFDIS=1以禁用数字滤波器。*2*3
停止电压检测1电路	5	设置LVD1CMPCR.LVD1E=0以禁用电压检测1电路。

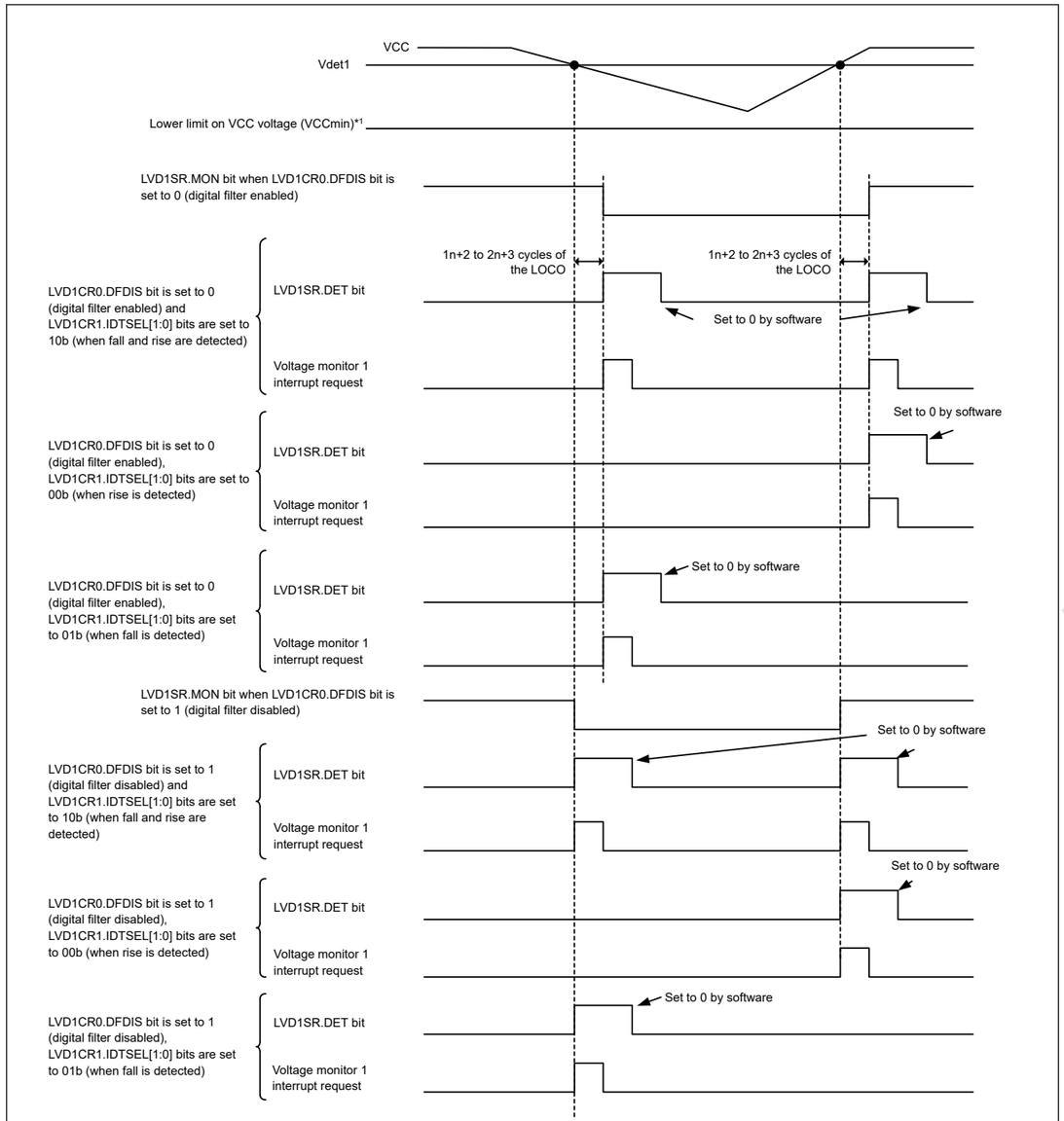
注1.如果只输出ELC事件信号，则不需要步骤3。
注2.如果不使用数字滤波器，则不需要步骤2和4。
注3.要从启用状态禁用数字滤波器然后重新启用它，请禁用它并等待至少2个LOCO时钟周期，然后再重新启用它。

如果电压监测器1在使用和停止一次后再次进行中断或复位设置，可根据情况省略停止和设置过程中的以下步骤：

●如果电路的设置不变，则不需要设置电压检测1电路。

- Setting the digital filter is not required if the settings for the circuit do not change.
- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or voltage monitor 1 reset do not change.

Figure 7.5 shows an example of the voltage monitor 1 interrupt operation.

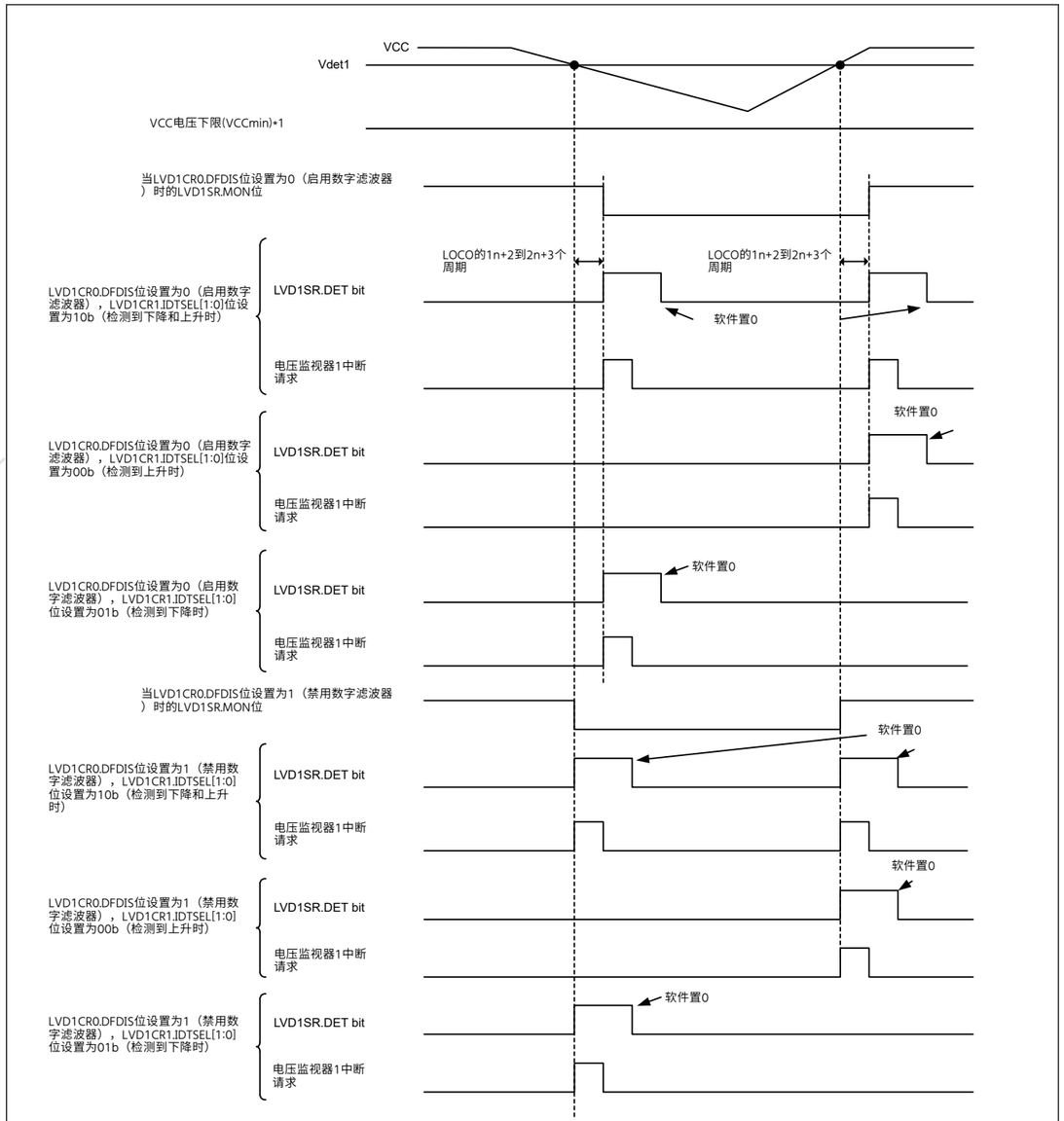


Note: n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n
Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

Figure 7.5 Example of voltage monitor 1 interrupt operation

●如果电路的设置不变，则不需要设置数字滤波器。
●如果电压监视器1中断或电压监视器1复位的设置没有改变，则不需要设置电压监视器1中断或复位。

图7.5显示了电压监视器1中断操作的示例。



Note: n：数字滤波器的采样时钟频率是LOCO频率除以n
注1.不使用电压监视器0复位时，请在VCC≥VCCmin时使用。

Figure 7.5 电压监视器1中断操作示例

7.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 2 circuit.

Table 7.6 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring occurs. Table 7.7 shows the procedures for setting bits related to the voltage monitor 2 interrupt/reset so that voltage monitoring stops. Figure 7.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 5.2 in section 5, Resets.

When using the voltage monitor 2 circuit in Software Standby mode or Deep Software Standby mode, set up the circuit with the following procedures.

(1) Setting in Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- When VCC > V_{det2} is detected, negate the voltage monitor 2 reset signal (LVD2CR0.RN = 0) following a LVD2 stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1).
- Enable the voltage monitor 2 interrupt (LVD2CR0.RI = 0). If the voltage monitor 2 reset is enabled (LVD2CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 2 circuit stops. To use the voltage monitor 2 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 7.6 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring occurs

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
2 circuit	1	Set LVD2CMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVD2CMPCR register.	
	2	Select the detection voltage in the LVD2CMPCR.LVD2LVL[2:0] bits.	
	3	Set LVD2CMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least $t_{d\ (E-A)}$ for the LVD2 operation stabilization time after LVD2 is enabled.*1	
Setting the digital filter*3	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.	
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO cycles, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 2 interrupt or reset	8	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset. • Select the type of reset negation in the LVD2CR0.RN bit.
	9	• Select the interrupt request condition in the LVD2CR1.IDTSEL[1:0] bits. • Select the interrupt type in the LVD2CR1.IRQSEL bit.	—
Enabling output	10	Set LVD2SR.DET = 0.	
	11	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*2	
	12	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on $t_{d(E-A)}$, see section 53, Electrical Characteristics.
Note 2. Step 11 is not required if only the ELC event signal is to be output.
Note 3. Steps 5 to 7 are not required if the digital filter is not in use.
Note 4. Steps 8 to 11 can be performed during the wait time of step 7.

7.6 电压监视器2的中断和复位

响应电压监视器2电路的比较结果，可以产生中断或复位。

表7.6显示了设置与电压监视器2中断复位相关的位以进行电压监视的过程。表7.7显示了设置与电压监控2中断复位相关的位以停止电压监控的步骤。图7.6显示了电压监视器2中断的操作示例。有关电压监视器2复位的操作，请参见第5节“复位”中的图5.2。

在软件待机模式或深度软件待机模式下使用电压监视器2电路时，请按照以下步骤设置电路。

(1) 在软件待机模式下设置

●禁用数字滤波器(LVD2CR0.DFDIS=1)

●当检测到VCC>Vdet2时，在LVD2稳定时间后取消电压监视器2复位信号(LVD2CR0.RN=0)。

(2) 深度软件待机模式中的设置

●禁用数字滤波器（LVD2CR0.DFDIS=1）。

●启用电压监视器2中断(LVD2CR0.RI=0)。如果启用电压监视器2复位(LVD2CR0.RI=1)，则无法转换到深度软件待机模式，而是将操作转换到软件待机模式。

●当DPSBYCR.DEEPCUT[1:0]位为11b时，电压监视器2电路停止。要在深度软件待机模式下使用电压监视器2电路，请将DPSBYCR.DEEPCUT[1:0]位设置为11b以外的值。

Table 7.6 设置与电压监控器2中断和电压监控器2相关的位以进行电压监控的步骤

Step		电压监视器2中断（电压监视器2 ELC event output)	电压监视器2复位
2 circuit	1	在写入LVD2CMPCR寄存器之前，设置LVD2CMPCR.LVD2E=0以禁用电压检测2。	
	2	在LVD2CMPCR.LVD2LVL[2:0]位中选择检测电压。	
	3	设置LVD2CMPCR.LVD2E=1以启用电压检测2电路。	
	4	启用LVD2后，至少等待td(E-A)的LVD2操作稳定时间。*1	
设置数字滤波器*3	5	在LVD2CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。	
	6	设置LVD2CR0.DFDIS=0以启用数字滤波器。	
	7	等待至少2n+3个LOCO周期，其中n=2、4、8或16，并且数字滤波器的采样时钟是LOCO频率除以n。*4	
设置电压监视器2中断或复位	8	设置LVD2CR0.RI=0以选择电压监视器2中断。	• 设置LVD2CR0.RI=1以选择电压监视器2复位。 • 选择复位否定的类型 LVD2CR0.RN bit.
	9	• 选择中断请求条件 LVD2CR1.IDTSEL[1:0] bits. • 选择中断类型 LVD2CR1.IRQSEL bit.	—
启用输出	10	Set LVD2SR.DET = 0.	
	11	设置LVD2CR0.RIE=1以启用电压监视器2中断或复位。*2	
	12	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。	

注1.步骤5至11可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参阅第53节，电气特性。
注2.如果只输出ELC事件信号，则不需要步骤11。
注3.如果不使用数字滤波器，则不需要步骤5至7。
注4.步骤7的等待时间内可以执行步骤8至11。

Table 7.7 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Settings to stop enabling output	1	Set LVD2CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 2.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, or 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*2
	3	Set LVD2CR0.RIE = 0 to disable the voltage monitor 2 interrupt or reset.*1
Stopping the digital filter	4	Set LVD2CR0.DFDIS = 1 to disable the digital filter. *2 *3
Stopping the voltage detection 2 circuit	5	Set LVD2CMPCR.LVD2E = 0 to disable the voltage detection 2 circuit.

Note 1. Step 3 is not required if only the ELC event signal is to be output.
Note 2. Steps 2 and 4 are not required if the digital filter is not in use.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, you can omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting the voltage detection 2 is not required if the settings for the circuit do not change.
- Setting the digital filter is not required if the settings for the circuit do not change.
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt or voltage monitor 2 reset do not change.

Table 7.7 设置与电压监控器2中断和电压监控器2相关的位以使电压监控器停止的步骤

Step		电压监控器2中断（电压监控器2ELC事件输出），电压监控器2复位
停止启用输出的设置	1	设置LVD2CR0.CMPE=0以禁用电压监视器2的比较结果输出。
	2	等待至少2n+3个LOCO周期，其中n=2、4、8或16，数字滤波器的采样时钟是LOCO分频的n。*2
	3	设置LVD2CR0.RIE=0以禁用电压监视器2中断或复位。*1
停止数字滤波器	4	设置LVD2CR0.DFDIS=1以禁用数字滤波器。*2*3
停止电压检测2电路	5	设置LVD2CMPCR.LVD2E=0以禁用电压检测2电路。

注1.如果只输出ELC事件信号，则不需要步骤3。
注2.如果不使用数字滤波器，则不需要步骤2和4。
注3.要从启用状态禁用数字滤波器然后重新启用它，请禁用它并等待至少2个LOCO时钟周期，然后再重新启用它。

如果电压监测器2的中断或复位设置在使用和停止一次后再次进行，可以根据情况省略停止和设置过程中的以下步骤：

- 如果电路的设置不变，则不需要设置电压检测2。
- 如果电路的设置不变，则不需要设置数字滤波器。
- 如果电压监视器2中断或电压监视器2复位的设置没有改变，则不需要设置电压监视器2中断或复位。

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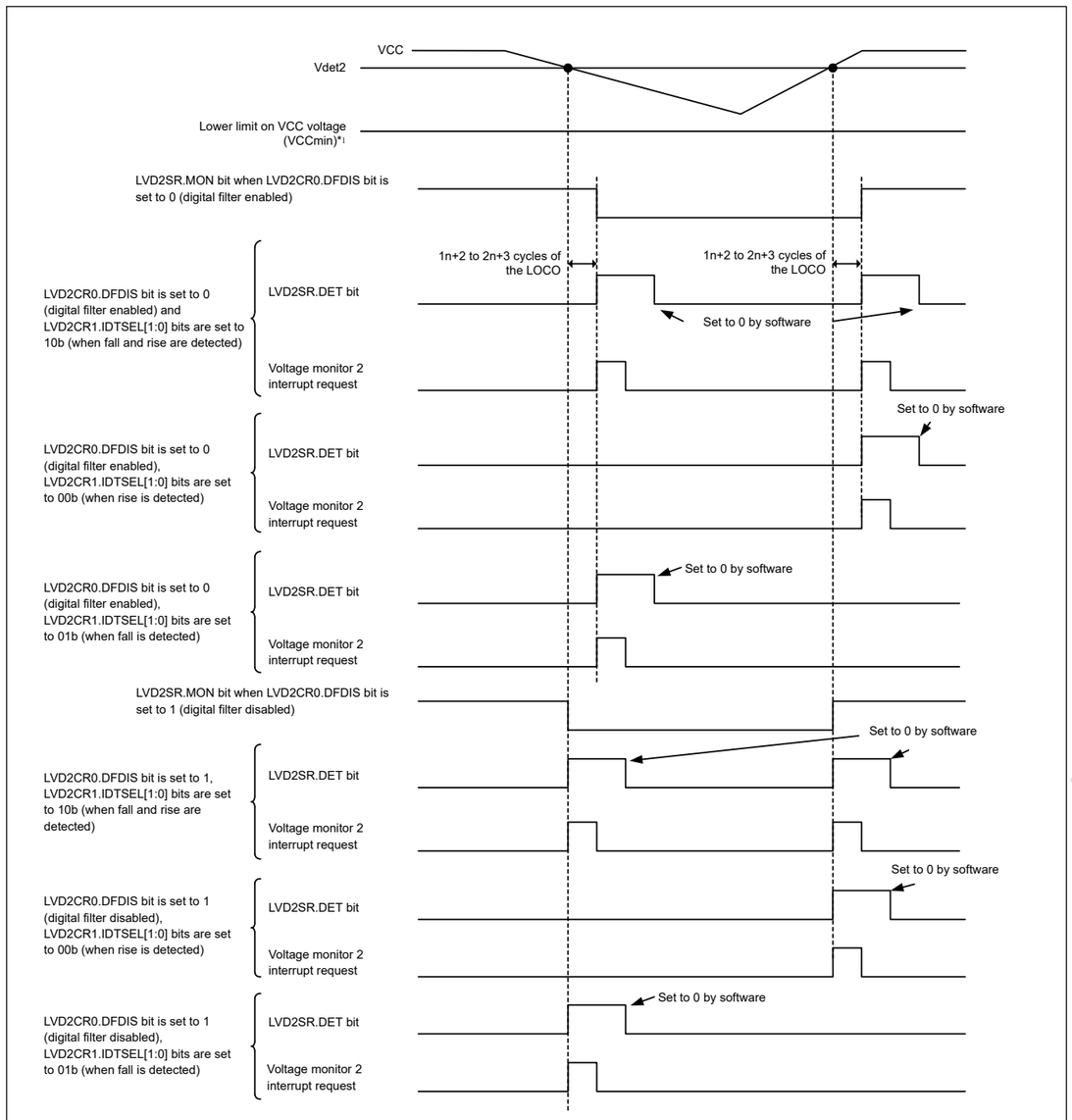


Note: n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n
Note 1. When the voltage monitor 0 reset is not in use, use at VCC ≥ VCCmin.

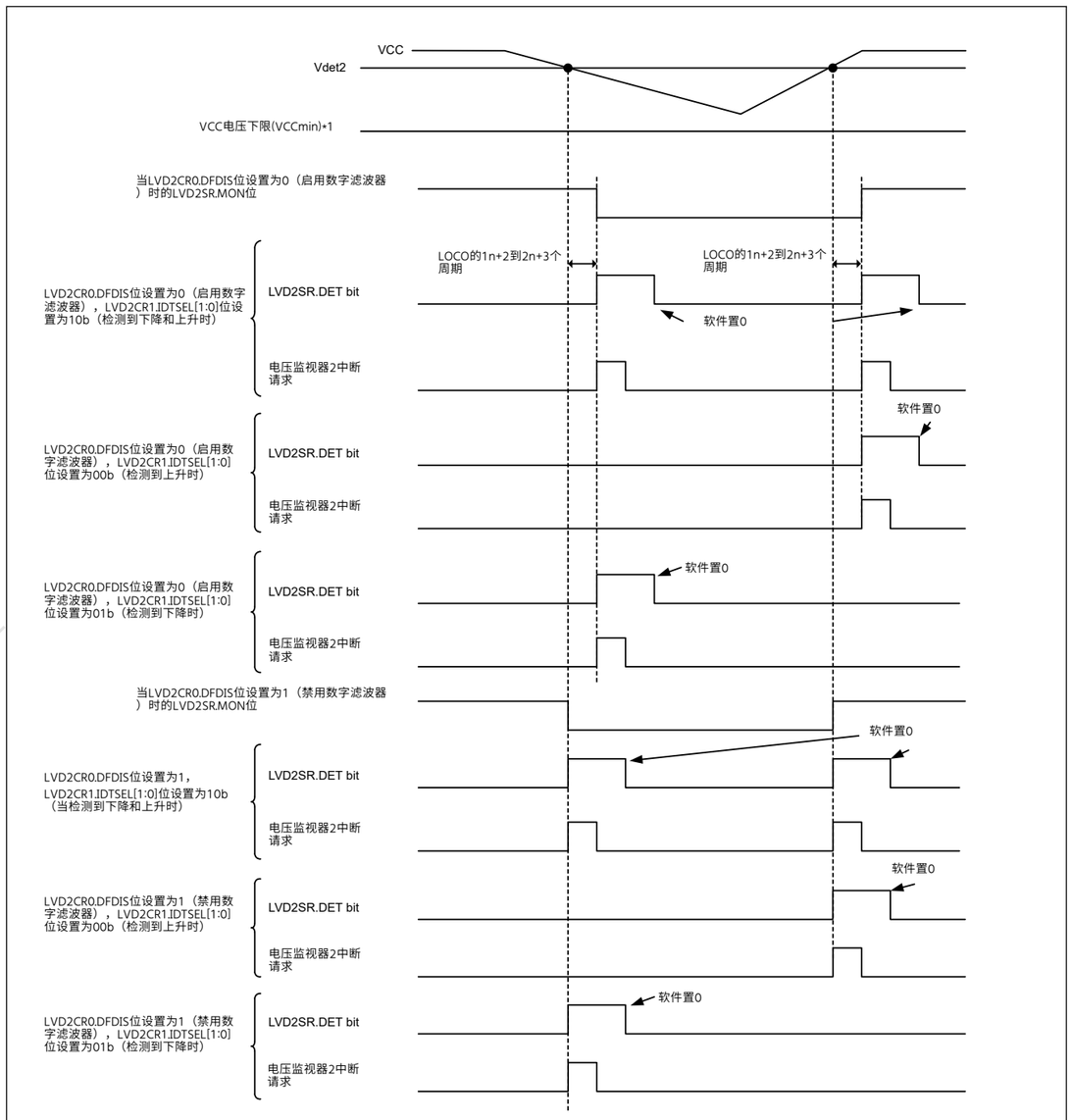
Figure 7.6 Example of voltage monitor 2 interrupt operation

7.7 Event Link Controller (ELC) Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) V_{det1} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.



Note: n：数字滤波器的采样时钟频率是LOCO频率除以n
注1.不使用电压监视器0复位时，请在VCC≥VCCmin时使用。

Figure 7.6 电压监视器2中断操作示例

7.7 事件链接控制器(ELC)输出

LVD可以将事件信号输出到事件链接控制器(ELC)。

(1) Vdet1交叉检测事件

当电压检测1电路和电压监视器1电路比较结果输出都启用时，LVD检测到电压已超过Vdet1电压时输出事件信号。

(2) V_{det2} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD before disabling the LVD event link function of the ELC.

7.7.1 Interrupt Handling and Event Linking

The LVD provides bits to separately enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal is output to the CPU.

In contrast, as soon as an interrupt source is generated, an event link signal is output as the event signal to the other module through the ELC, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby and Deep Software Standby modes. The event signals for the ELC in Software Standby and Deep Software Standby modes are output as follows:

- When a V_{det1} or V_{det2} passage events is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} and V_{det2} passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} and V_{det2} detection flags.
- When a Vdet1 or Vdet2 passage events are detected in Deep Software Standby mode, event signals are not generated for the ELC.

(2) Vdet2交叉检测事件

当电压检测2电路和电压监测器2电路比较结果输出都启用时，LVD检测到电压已超过Vdet2电压时输出事件信号。

使能LVD的事件链接输出功能时，必须先使能LVD，再使能ELC的LVD事件链接功能。要停止LVD的事件链接输出功能，必须先停止LVD，然后再禁用ELC的LVD事件链接功能。

7.7.1 中断处理和事件链接

LVD提供位来分别启用或禁用电压监视器1和2中断。当产生中断源并通过中断使能位使能中断时，将中断信号输出到CPU。

相反，一旦产生中断源，无论中断使能位的状态如何，都会通过ELC将事件链接信号作为事件信号输出到其他模块。

在软件待机和深度软件待机模式下，可以输出电压监视器1和2中断。软件待机和深度软件待机模式下ELC的事件信号输出如下：

- 当在软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC，因为在软件待机模式下不提供时钟。因为保存了Vdet1和Vdet2通过检测标志，所以当从软件待机模式恢复后时钟供应恢复时，ELC的事件信号将根据Vdet1和Vdet2检测标志的状态输出。
- 当在深度软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC生成事件信号。

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8. Clock Generation Circuit

8.1 Overview

The MCU provides a clock generation circuit. Table 8.1 and Table 8.2 list the clock generation circuit specifications. Figure 8.1 show a block diagram, and Table 8.3 lists the I/O pins.

Table 8.1 Clock generation circuit specifications for the clock sources

Clock source	Description	Specification
Main clock oscillator (MOSC)	Resonator frequency	8 MHz to 24 MHz 8, 10, 16, 20, 24 MHz (USB boot mode)
	External clock input frequency	Up to 24 MHz
	External resonator or additional circuit	ceramic resonator, crystal
	Connection pins	EXTAL, XTAL
	Drive capability switching	Available
	Oscillation stop detection function	Available
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit	crystal resonator
	Connection pins	XCIN, XCOUT
	Drive capability switching	Available
PLL circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)
	Output pulse frequency division ratio	Unavailable
	PLL Output frequency	120 MHz to 200 MHz
PLL2 circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)
	Output pulse frequency division ratio	Unavailable
	PLL Output frequency	120 MHz to 240 MHz
	PLL2-LDO stop function	Unavailable
High-speed on-chip oscillator (HOCO)	Oscillation frequency	16/18/20 MHz
	FLL function	Available
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
	User trimming	Unavailable
External clock input for JTAG (TCK)	Input clock frequency	Up to 25 MHz
External clock input for SWD (SWCLK)	Input clock frequency	Up to 25 MHz

8. 时钟产生电路

8.1 Overview

MCU提供时钟生成电路。表8.1和表8.2列出了时钟生成电路规格。图8.1显示了框图，表8.3列出了IO引脚。

Table 8.1 时钟源的时钟生成电路规格

时钟源	Description	Specification
主时钟振荡器(MOSC)	谐振器频率	8MHz至24MHz8、10、16、20、24MHz（USB引导模式）
	外部时钟输入频率	高达24MHz
	外部谐振器或附加电路	陶瓷谐振器，晶体
	连接引脚	EXTAL, XTAL
	驱动能力切换	Available
	振荡停止检测功能	Available
Sub-clock oscillator (SOSC)	谐振器频率	32.768 kHz
	外部谐振器或附加电路	晶体谐振器
	连接引脚	XCIN, XCOUT
	驱动能力切换	Available
PLL circuit	输入时钟源	MOSC, HOCO
	输入脉冲分频比	可从1、2和3中选择
	输入频率	8 MHz to 24 MHz
	倍频比	可选择10至30（0.5步）
	输出脉冲分频比	Unavailable
	锁相环输出频率	120 MHz to 200 MHz
PLL2 circuit	输入时钟源	MOSC, HOCO
	输入脉冲分频比	可从1、2和3中选择
	输入频率	8 MHz to 24 MHz
	倍频比	可选择10至30（0.5步）
	输出脉冲分频比	Unavailable
	锁相环输出频率	120 MHz to 240 MHz
	PLL2-LDO停止功能	Unavailable
High-speed on-chip oscillator (HOCO)	振荡频率	16/18/20 MHz
	FLL function	Available
	用户修剪	Available
Middle-speed on-chip oscillator (MOCO)	振荡频率	8 MHz
	用户修剪	Available
Low-speed on-chip oscillator (LOCO)	振荡频率	32.768 kHz
	用户修剪	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	振荡频率	15 kHz
	用户修剪	Unavailable
JTAG(TCK)的外部时钟输入	输入时钟频率	高达25MHz
SWD的外部时钟输入(SWCLK)	输入时钟频率	高达25MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	CPU, DTC, DMAC, Flash, RAM	Up to 200 MHz Division ratios: 1/2/4/8/16/32/64
Peripheral module clock A (PCLKA)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	Peripheral modules (ETHERC, EDMAC, USBHS, QSPI, SCI, CAN-RAM, SPI, CRC, DOC, ADC12, DAC12, SCE9, GPT bus clock)	Up to 100 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	Peripheral modules (CAC, ELC, I/O ports, POEG, RTC, WDT, IWDT, AGT, IIC, CAN, USBFS, SSIE, SDHI, CEC, TSN, CTSU, Standby SRAM, Octal-SPI bus clock)	Up to 50 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock C (PCLKC)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	Peripheral module (ADC12 conversion clock)	Up to 50 MHz Division ratio: 1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	Peripheral module(GPT count clock)	Up to 100 MHz Division ratio: 1/2/4/8/16/32/64
FlashIF clock (FCLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	FlashIF	4 MHz to 50 MHz(P/E) Up to 50 MHz(read) Division ratio: 1/2/4/8/16/32/64
External bus clock (BCLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	External bus	Up to 100 MHz Division ratio: 1/2/4/8/16/32/64
EBCLK pin output (EBCLK)	BCLK or 1/2 BCLK	EBCLK pin	Up to 50 MHz Division ratio: 1 or 2
USB clock (USBCLK)	PLL/PLL2	USBFS, USBHS	48 MHz Division ratio: 3/4/5
USB clock (USB60CLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL/PLL2	USBHS	60 MHz Division ratio: 1/2/3/4/5/6/8
USBHS-PHY clock (USBMCLK)	MOSC	USBHS-PHY	12 M/20 M/24 MHz
Octal-SPI clock (OCTACLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL/PLL2	Octal-SPI	Up to 200 MHz Division ratio: 1/2/4/6/8
CANFD clock (CANFDCLK)	PLL/PLL2	CANFD	Up to 40 MHz Division ratio: 1/2/4/6/8
CAN clock (CANMCLK)	MOSC	CAN	8 MHz to 24 MHz
CEC clock (CECCLK)	MOSC/SOSC	CEC	Up to 20 MHz (MOSC) Division ratio: 1/2 32.768kHz (SOSC)
AGT clock (AGTSCLK)	SOSC	AGT	32.768 kHz
AGT clock (AGTLCLK)	LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 24 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	16/18/20 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCCLK)	SOSC/LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz

Table 8.2 内部时钟的时钟生成电路规格（1of2）

Item	时钟源	时钟电源	Specification
系统时钟(ICLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	CPU、DTC、DMAC、闪存、RAM	高达200兆赫兹 Division ratios: 1/2/4/8/16/32/64
外设模块时钟A(PCLKA)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	外围模块（ETHERC、EDMAC、USB HS、QSPI、SCI、CAN RAM、SPI、CRC、DOC、ADC12、DAC12、SCE9、GPT总线时钟）	高达100MHz Division ratio: 1/2/4/8/16/32/64
外设模块时钟B(PCLKB)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	外围模块（CAC、ELC、IO端口、POEG、RTC、WDT、IWDT、AGT、IIC、CAN、USBFS、SSIE、SDHI, CEC, TSN, CTSU, Standby SRAM, Octal-SPI bus clock)	高达50MHz Division ratio: 1/2/4/8/16/32/64
外设模块时钟C(PCLKC)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	外设模块（ADC12转换时钟）	高达50MHz Division ratio: 1/2/4/8/16/32/64
外设模块时钟D(PCLKD)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	外设模块（GPT计数时钟）	高达100MHz Division ratio: 1/2/4/8/16/32/64
FlashIF clock (FCLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	FlashIF	4MHz至50MHz(PE)高达50MHz（读取） Division ratio: 1/2/4/8/16/32/64
外部总线时钟(BCLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL	外部总线	高达100MHz Division ratio: 1/2/4/8/16/32/64
EBCLK引脚输出(EBCLK)	BCLK or 1/2 BCLK	EBCLK pin	高达50MHz 分频比：1或2
USB时钟(USBCLK)	PLL/PLL2	USBFS, USBHS	48 MHz Division ratio: 3/4/5
USB时钟(USB60CLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL/PLL2	USBHS	60 MHz Division ratio: 1/2/3/4/5/6/8
USBHS-PHY clock (USBMCLK)	MOSC	USBHS-PHY	12 M/20 M/24 MHz
Octal-SPI clock (OCTACLK)	MOSC/SOSC/HOCO/MOCO/LOCO/PLL/PLL2	Octal-SPI	高达200兆赫兹 Division ratio: 1/2/4/6/8
CANFD clock (CANFDCLK)	PLL/PLL2	CANFD	高达40MHz Division ratio: 1/2/4/6/8
CAN时钟(CANMCLK)	MOSC	CAN	8 MHz to 24 MHz
CEC clock (CECCLK)	MOSC/SOSC	CEC	高达20MHz(MOSC) Division ratio: 1/2 32.768kHz (SOSC)
AGT clock (AGTSCLK)	SOSC	AGT	32.768 kHz
AGT clock (AGTLCLK)	LOCO	AGT	32.768 kHz
CAC主时钟(CACMCLK)	MOSC	CAC	高达24MHz
CAC副时钟(CACSCLK)	SOSC	CAC	32.768 kHz
CACLOCO时钟(CACLCLK)	LOCO	CAC	32.768 kHz
CACMOCO时钟(CACMOCLK)	MOCO	CAC	8 MHz
CACHOCO时钟(CACHCLK)	HOCO	CAC	16/18/20 MHz
CACIWDTLOCO时钟(CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCCLK)	SOSC/LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick定时器时钟(SYSTICCLK)	LOCO	SysTick timer	32.768 kHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
JTAG clock (JTAGTCK)	TCK	JTAG	Up to 25 MHz
Serial wire clock (SWCLK)	SWCLK	OCD	Up to 25 MHz
Trace clock (TRCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU-OCD	Up to 100 MHz, Division ratio: 1/2/4
TCLK pin output (TCLK)	1/2 TRCLK	TCLK pin	Up to 50 MHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	Up to 60 MHz Division ratios: 1/2/4/8/16/32/64/128

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB
ICLK ≥ FCLK, ICLK ≥ BCLK
Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:FCLK = N:1, ICLK:BCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1, ICLK:PCLKC = N:1 or 1:N , ICLK:PCLKD= N:1 or 1:N, ICLK:TRCLK= N:1 or 1:N
If the A/D converter is enabled, the clock frequency ratio is constrained as follows:
PCLKA:PCLKC = 1:1 or 2:1 or 4:1 or 8:1 or 1:2 or 1:4
If the CAN-FD is used, clock frequency ratio is constrained to be PCLKA:PCLKB = 2:1.

Note: Restrictions on the minimum FCLK frequency 4MHz when P/E.

Note: The multiplication of PLL and PLL2 should be set to be within the output frequency range of PLL and PLL2, taking the frequency of HOCO into consideration when not using the FLL function.

Note: Clocks have a permissible frequency range (See Table 8.2).
Flash memory and SRAM also have a permissible operating frequency range in each wait cycle setting. (See section 48, SRAM, section 50, Flash Memory)
Those clock frequency ranges must be satisfied even if the HOCO has its maximum or minimum frequency when not using FLL function. (See section 53, Electrical Characteristics).

Note: When using ETHERC, the PCLKA frequency is as follows:.
12.5 MHz ≤ PCLKA ≤ 100 MHz

Table 8.2 内部时钟的时钟生成电路规格(2of2)

Item	时钟源	时钟电源	Specification
JTAG clock (JTAGTCK)	TCK	JTAG	高达25MHz
串行线时钟(SWCLK)	SWCLK	OCD	高达25MHz
跟踪时钟(TRCLK)	MOSC/SOSC/HOCO/MOCO/ LOCO/PLL	CPU-OCD	高达100MHz，分频比：124
TCLK引脚输出(TCLK)	1/2 TRCLK	TCLK pin	高达50MHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/ HOCO	CLKOUT pin	高达60MHz Division ratios: 1/2/4/8/16/32/64/128

Note: 设置时钟频率的限制：ICLK≥PCLKA≥PCLKB，PCLKD≥PCLKA≥PCLKB
ICLK ≥ FCLK, ICLK ≥ BCLK
时钟频率比的限制：（N：整数，最大为64）
ICLK:FCLK=N:1 ICLK:BCLK=N:1 ICLK:PCLKA=N:1 ICLK:PCLKB=N:1 ICLK:PCLKC=N:1或1:N ICLK:PCLKD=N:1或1:N，ICLK:TRCLK=N:1或1:N如果AD转换器使能，时钟频率比受到如下约束：

PCLKA:PCLKC = 1:1 or 2:1 or 4:1 or 8:1 or 1:2 or 1:4
如果使用CAN-FD，时钟频率比被限制为PCLKA:PCLKB=2:1。

Note: PE时对最小FCLK频率4MHz的限制。

Note: PLL和PLL2的倍频应设置在PLL和PLL2的输出频率范围内，取频率为
不使用FLL功能时考虑HOCO。

Note: 时钟有一个允许的频率范围（见表8.2）。
闪存和SRAM在每个等待周期设置中也有一个允许的工作频率范围。（参见第48节，SRAM，第50节，闪存）即使HOCO在不使用FLL功能时具有其最大或最小频率，也必须满足这些时钟频率范围。（参见第53节，电气特性）。

Note: 使用ETHERC时，PCLKA频率如下：12.5MHz≤PCLKA≤100MHz

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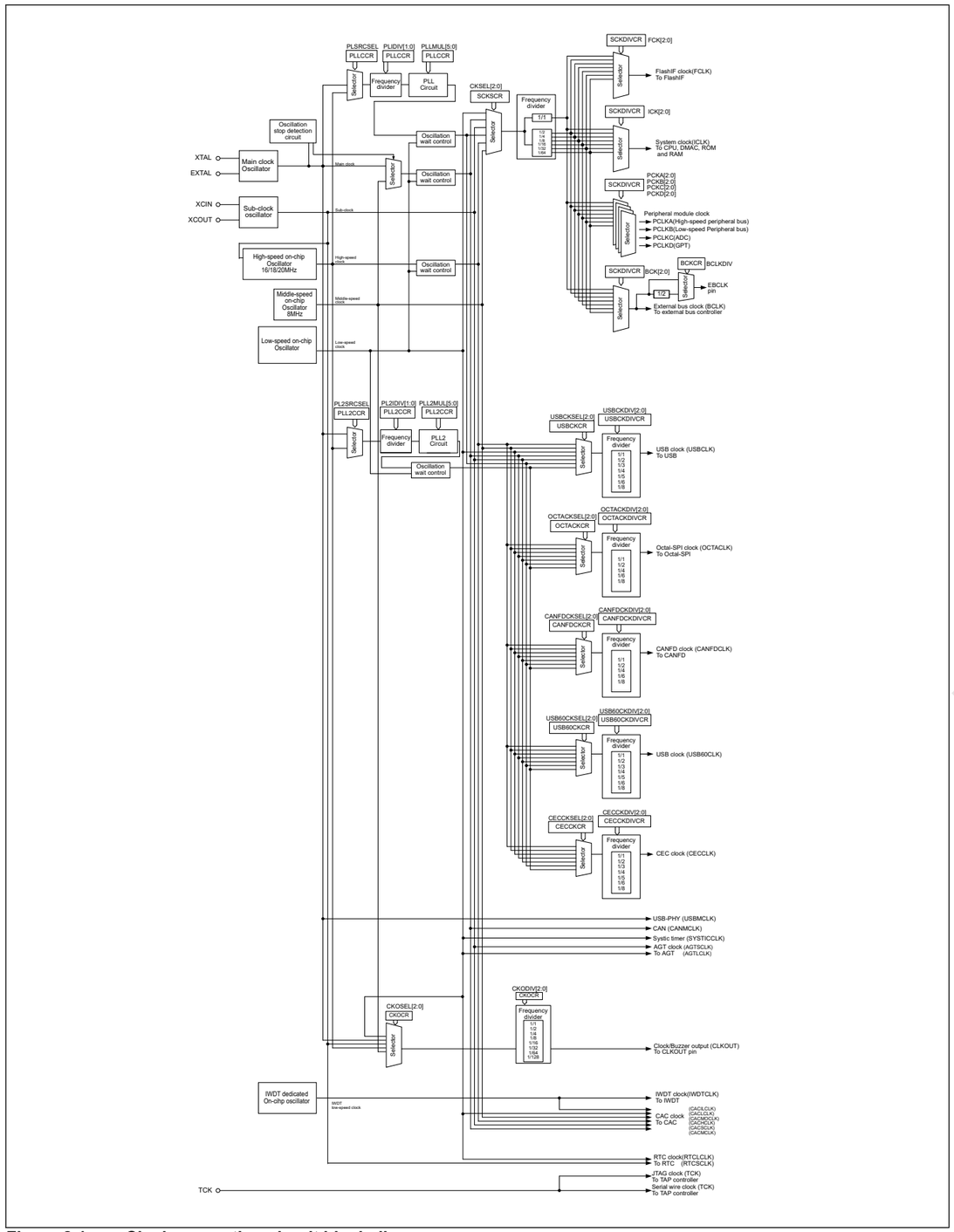

Figure 8.1 Clock generation circuit block diagram

Table 8.3 lists the input/output pins of the clock generation circuit.

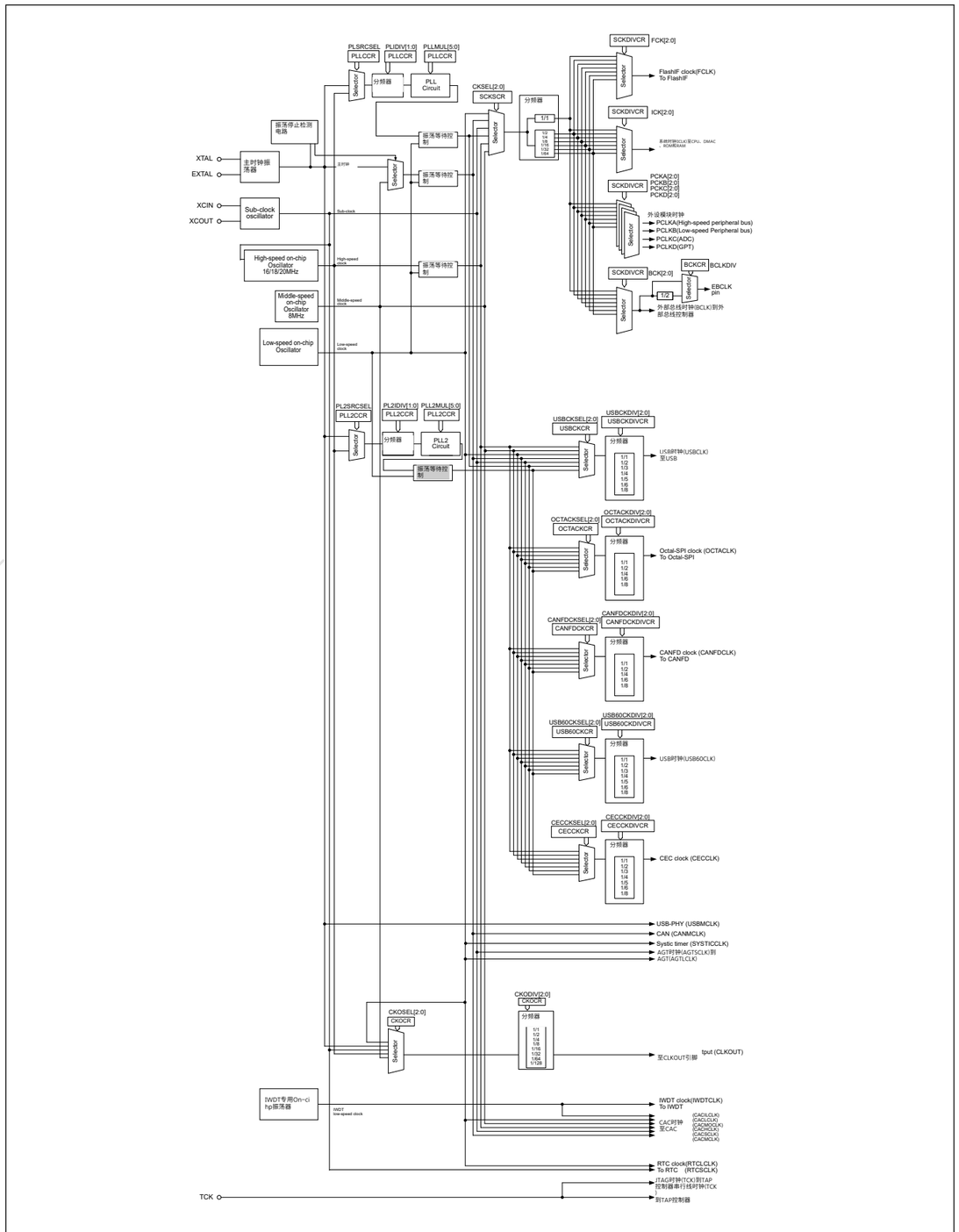

Figure 8.1 时钟产生电路框图

表8.3列出了时钟生成电路的输入输出引脚。

Table 8.3 Input/Output Pins of Clock Generation Circuit

Pin name	I/O	Description
XTAL	Output	These pins are used to connect a ceramic resonator or crystal resonator. The EXTAL pin can also be used to input an external clock. For details, see section 8.3.2. External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect a 32.768-kHz crystal resonator
XCOUT	Output	
TCK/SWCLK	Input	This pin is used to input the clock for the JTAG/SWD
EBCLK	Output	This pin is used to supply external devices with the external bus clock (EBCLK)
CLKOUT	Output	This pin is used to output the CLKOUT/BUZZER clock

8.2 Register Descriptions

8.2.1 CGFSAR : Clock Generation Function Security Attribute Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	NONSEC20	NONSEC19	NONSEC18	NONSEC17	NONSEC16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	NONSEC12	NONSEC11	—	NONSEC09	NONSEC08	NONSEC07	NONSEC06	NONSEC05	NONSEC04	NONSEC03	NONSEC02	—	NONSEC00
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC00*1	Non Secure Attribute bit 00 Target register: SCKDIVCR, SCKSCR Target factor: system clock control 0: Secure 1: Non Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	NONSEC02*1	Non Secure Attribute bit 02 Target register: HOCOCR, FLLCR1, FLLCR2, HOCOUTCR Target factor: HOCO 0: Secure 1: Non Secure	R/W
3	NONSEC03*1	Non Secure Attribute bit 03 Target register: MOCOCR, MOCOUTCR Target factor: MOCO 0: Secure 1: Non Secure	R/W
4	NONSEC04	Non Secure Attribute bit 04 Target register: LOCOCR, LOCOUTCR Target factor: LOCO 0: Secure 1: Non Secure	R/W
5	NONSEC05	Non Secure Attribute bit 05 Target register: MOSCCR, MOSCWTCR, MOMCR Target factor: MOSC 0: Secure 1: Non Secure	R/W

Table 8.3 时钟产生电路的输入输出引脚

引脚名称	I/O	Description
XTAL	Output	这些引脚用于连接陶瓷谐振器或晶体谐振器。EXTAL引脚也可用于输入外部时钟。详见8.3.2节。外部时钟输入。
EXTAL	Input	
XCIN	Input	这些引脚用于连接32.768-kHz晶体谐振器
XCOUT	Output	
TCK/SWCLK	Input	该引脚用于输入JTAGSWD的时钟
EBCLK	Output	该引脚用于为外部设备提供外部总线时钟(EBCLK)
CLKOUT	Output	该引脚用于输出CLKOUTBUZZER时钟

8.2 注册说明

8.2.1 CGFSAR:时钟生成功能安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	NONSEC20	NONSEC19	NONSEC18	NONSEC17	NONSEC16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	NONSEC12	NONSEC11	—	NONSEC09	NONSEC08	NONSEC07	NONSEC06	NONSEC05	NONSEC04	NONSEC03	NONSEC02	—	NONSEC00
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC00*1	非安全属性位00 Target register: SCKDIVCR, SCKSCR 目标因素：系统时钟控制 0：安全1：不安全	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	NONSEC02*1	非安全属性位02 Target register: HOCOCR, FLLCR1, FLLCR2, HOCOUTCR Target factor: HOCO 0：安全1：不安全	R/W
3	NONSEC03*1	非安全属性位03 Target register: MOCOCR, MOCOUTCR Target factor: MOCO 0：安全1：不安全	R/W
4	NONSEC04	非安全属性位04 Target register: LOCOCR, LOCOUTCR 目标因素：LOCO 0：安全1：不安全	R/W
5	NONSEC05	非安全属性位05 Target register: MOSCCR, MOSCWTCR, MOMCR Target factor: MOSC 0：安全1：不安全	R/W

Bit	Symbol	Function	R/W
6	NONSEC06	Non Secure Attribute bit 06 Target register: OSTDCR, OSTDSR Target factor: oscillation stop detection control 0: Secure 1: Non Secure	R/W
7	NONSEC07	Non Secure Attribute bit 07 Target register: SOSCCR, SOMCR Target factor: SOSC 0: Secure 1: Non Secure	R/W
8	NONSEC08*1	Non Secure Attribute bit 08 Target register: PLLCCR, PLLCR Target factor: PLL 0: Secure 1: Non Secure	R/W
9	NONSEC09	Non Secure Attribute bit 09 Target register: PLL2CCR, PLL2CR Target factor: PLL2 0: Secure 1: Non Secure	R/W
10	—	This bit is read as 1. The write value should be 1.	R/W
11	NONSEC11	Non Secure Attribute bit 11 Target register: CKOCR Target factor: CLKOUT control 0: Secure 1: Non Secure	R/W
12	NONSEC12	Non Secure Attribute bit 12 Target register: BCKCR, EBCKOCR Target factor: EBCLK 0: Secure 1: Non Secure	R/W
15:13	—	These bits are read as 1. The write value should be 1.	R/W
16	NONSEC16	Non Secure Attribute bit 16 Target register: USBCKDIVCR, USBCKCR Target factor: USBCLK 0: Secure 1: Non Secure	R/W
17	NONSEC17	Non Secure Attribute bit 17 Target register: OCTACKDIVCR, OCTACKCR Target factor: OCTACLK 0: Secure 1: Non Secure	R/W
18	NONSEC18	Non Secure Attribute bit 18 Target register: CANFDCKDIVCR, CANFDCKCR Target factor: CANFDCLK 0: Secure 1: Non Secure	R/W
19	NONSEC19	Non Secure Attribute bit 19 Target register: USB60CKDIVCR, USB60CKCR Target factor:USB60CK 0: Secure 1: Non Secure	R/W
20	NONSEC20	Non Secure Attribute bit 20 Target register: CECCKDIVCR, CECCKCR Target factor: CECCK 0: Secure 1: Non Secure	R/W
31:21	—	These bits are read as 1. The write value should be 1.	R/W

Bit	Symbol	Function	R/W
6	NONSEC06	非安全属性位06 Target register: OSTDCR, OSTDSR 目标因素：振荡停止检测控制 0：安全1：不安全	R/W
7	NONSEC07	非安全属性位07 Target register: SOSCCR, SOMCR Target factor: SOSC 0：安全1：不安全	R/W
8	NONSEC08*1	非安全属性位08 Target register: PLLCCR, PLLCR Target factor: PLL 0：安全1：不安全	R/W
9	NONSEC09	非安全属性位09 Target register: PLL2CCR, PLL2CR Target factor: PLL2 0：安全1：不安全	R/W
10	—	该位读取为1。写入值应为1。	R/W
11	NONSEC11	非安全属性位11 Target register: CKOCR 目标因素：CLKOUT控制 0：安全1：不安全	R/W
12	NONSEC12	非安全属性位12 Target register: BCKCR, EBCKOCR Target factor: EBCLK 0：安全1：不安全	R/W
15:13	—	这些位被读取为1。写入值应为1。	R/W
16	NONSEC16	非安全属性位16 Target register: USBCKDIVCR, USBCKCR Target factor: USBCLK 0：安全1：不安全	R/W
17	NONSEC17	非安全属性位17 Target register: OCTACKDIVCR, OCTACKCR Target factor: OCTACLK 0：安全1：不安全	R/W
18	NONSEC18	非安全属性位18目标寄存器：CANFDCKDIVCR、CANFDCKCR Target factor: CANFDCLK 0：安全1：不安全	R/W
19	NONSEC19	非安全属性位19 Target register: USB60CKDIVCR, USB60CKCR Target factor:USB60CK 0：安全1：不安全	R/W
20	NONSEC20	非安全属性位20 Target register: CECCKDIVCR, CECCKCR Target factor: CECCK 0：安全1：不安全	R/W
31:21	—	这些位被读取为1。写入值应为1。	R/W

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Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. It is recommended that these bits are configured as Non Secure when the device life cycle is NSECSD (DLMMON.DLMMON[3:0] = 0011b). See section 52.7.1. Restrictions on setting the security attribution for the details.

CGFSAR register controls the secure attribute of Clock Generation Function registers.

NONSEC00 bit (Non Secure Attribute bit 00)

This bit controls the security attribute of SCKDIVCR, SCKSCR.

NONSEC02 bit (Non Secure Attribute bit 02)

This bit controls the security attribute of HOCOCR, FLLCR1, FLLCR2, HOCOUTCR.

NONSEC03 bit (Non Secure Attribute bit 03)

This bit controls the security attribute of MOCOCR, MOCOUTCR.

NONSEC04 bit (Non Secure Attribute bit 04)

This bit controls the security attribute of LOCOCR, LOCOUTCR.

NONSEC05 bit (Non Secure Attribute bit 05)

This bit controls the security attribute of MOSCCR, MOSCWTCR, MOMCR.

NONSEC06 bit (Non Secure Attribute bit 06)

This bit controls the security attribute of OSTDCR, OSTDSR.

NONSEC07 bit (Non Secure Attribute bit 07)

This bit controls the security attribute of SOSCCR, SOMCR.

NONSEC08 bit (Non Secure Attribute bit 08)

This bit controls the security attribute of PLLCCR, PLLCR.

NONSEC09 bit (Non Secure Attribute bit 09)

This bit controls the security attribute of PLL2CCR, PLL2CR.

NONSEC11 bit (Non Secure Attribute bit 11)

This bit controls the security attribute of CKOCR.

NONSEC12 bit (Non Secure Attribute bit 12)

This bit controls the security attribute of BCKCR, EBCKOCR.

NONSEC16 bit (Non Secure Attribute bit 16)

This bit controls the security attribute of USBCKDIVCR, USBCKCR.

NONSEC17 bit (Non Secure Attribute bit 17)

This bit controls the security attribute of OCTACKDIVCR, OCTACKCR.

NONSEC18 bit (Non Secure Attribute bit 18)

This bit controls the security attribute of CANFDCKDIVCR, CANFDCKCR.

NONSEC19 bit (Non Secure Attribute bit 19)

This bit controls the security attribute of USB60CKDIVCR, USB60CKCR.

NONSEC20 bit (Non Secure Attribute bit 20)

This bit controls the security attribute of CECCKDIVCR, CECCKCR.

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
注1.当器件生命周期为NSECSD(DLMMON.DLMMON[3:0]=0011b)时，建议将这些位配置为非安全。请参阅第52.7.1节。设置详细信息的安全属性的限制。

CGFSAR寄存器控制时钟生成功能寄存器的安全属性。

NONSEC00位（非安全属性位00）

该位控制SCKDIVCR、SCKSCR的安全属性。

NONSEC02位（非安全属性位02）

该位控制HOCOCR、FLLCR1、FLLCR2、HOCOUTCR的安全属性。

NONSEC03位（非安全属性位03）

该位控制MOCOCR、MOCOUTCR的安全属性。

NONSEC04位（非安全属性位04）

该位控制LOCOCR、LOCOUTCR的安全属性。

NONSEC05位（非安全属性位05）

该位控制MOSCCR、MOSCWTCR、MOMCR的安全属性。

NONSEC06位（非安全属性位06）

该位控制OSTDCR、OSTDSR的安全属性。

NONSEC07位（非安全属性位07）

该位控制SOSCCR、SOMCR的安全属性。

NONSEC08位（非安全属性位08）

该位控制PLLCCR、PLLCR的安全属性。

NONSEC09位（非安全属性位09）

该位控制PLL2CCR、PLL2CR的安全属性。

NONSEC11位（非安全属性位11）

该位控制CKOCR的安全属性。

NONSEC12位（非安全属性位12）

该位控制BCKCR、EBCKOCR的安全属性。

NONSEC16位（非安全属性位16）

该位控制USBCKDIVCR、USBCKCR的安全属性。

NONSEC17位（非安全属性位17）

该位控制OCTACKDIVCR、OCTACKCR的安全属性。

NONSEC18位（非安全属性位18）

该位控制CANFDCKDIVCR、CANFDCKCR的安全属性。

NONSEC19位（非安全属性位19）

该位控制USB60CKDIVCR、USB60CKCR的安全属性。

NONSEC20位（非安全属性位20）

该位控制CECCKDIVCR、CECCKCR的安全属性。

8.2.2 SCKDIVCR : System Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	BCK[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]*4	Peripheral Module Clock D (PCLKD) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	PCKC[2:0]*4	Peripheral Module Clock C (PCLKC) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	PCKB[2:0]*3	Peripheral Module Clock B (PCLKB) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
14:12	PCKA[2:0]*3	Peripheral Module Clock A (PCLKA) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W

8.2.2 SCKDIVCR:系统时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	BCK[2:0]		
重置后的值:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
重置后的值:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Function	R/W
2:0	PCKD[2:0]*4	外设模块时钟D(PCLKD)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	PCKC[2:0]*4	外设模块时钟C(PCLKC)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	PCKB[2:0]*3	外设模块时钟B(PCLKB)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
11	—	该位读取为0。写入值应为0。	R/W
14:12	PCKA[2:0]*3	外设模块时钟A(PCLKA)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
15	—	该位读取为0。写入值应为0。	R/W

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Bit	Symbol	Function	R/W
18:16	BCK[2:0]*2	External Bus Clock (BCLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Settings prohibited	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
26:24	ICK[2:0]*1*2*3*4*5	System Clock (ICLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	FCK[2:0]*1	FlashIF Clock (FCLK) Select 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 Others: Setting prohibited.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. The following relation is required between the frequencies of the system clock (ICLK) and the FlashIF clock (FCLK).
ICLK:FCLK=N:1 (N: integer)

Note 2. The following relation is required between the frequencies of the system clock (ICLK) and the external bus clock (BCLK).
ICLK:BCLK=N:1 (N: integer)

Note 3. The following relation is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB)
ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)

Note 4. The following relation is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKC, PCLKD):
ICLK:PCLKC,PCLKD = N:1or1:N (N: integer)

Note 5. The frequency of the system clock (ICLK) is limited to the flash wait cycle register (FLWT). See section 50, Flash Memory.

SCKDIVCR selects the frequencies of the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), FlashIF clock (FCLK), and external bus clock (BCLK).

When the PLL is selected as the clock source, you must enter the following modules in module-stop state before changing the value of this register: USBHS, SCE9.

In addition, when changing any value in SCKDIVCR from a lower division ratio to a higher division ratio, wait at least 750 ns before changing the value.

When changing any value from a higher division ratio to a lower division ratio, wait at least 250 ns after changing the value, before starting subsequent processing.

The recommended method to measure the wait time is through software.

Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Bit	Symbol	Function	R/W
18:16	BCK[2:0]*2	外部总线时钟(BCLK)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
26:24	ICK[2:0]*1*2*3*4*5	系统时钟(ICLK)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
27	—	该位读取为0。写入值应为0。	R/W
30:28	FCK[2:0]*1	FlashIF时钟(FCLK)选择 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 其他：禁止设置。	R/W
31	—	该位读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

注1.系统时钟(ICLK)和FlashIF时钟(FCLK)的频率之间需要以下关系。
ICLK:FCLK=N:1 (N: integer)

注2.系统时钟(ICLK)和外部总线时钟(BCLK)的频率之间需要以下关系。
ICLK:BCLK=N:1 (N: integer)

注3.系统时钟(ICLK)和外围模块时钟(PCLKA
PCLKB)
ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)

注4.系统时钟(ICLK)和外围模块时钟(PCLKC
PCLKD):
ICLK:PCLKC,PCLKD = N:1or1:N (N: integer)

注5.系统时钟(ICLK)的频率仅限于闪存等待周期寄存器(FLWT)。请参阅第50节，闪存。

SCKDIVCR选择系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD)、FlashIF时钟(FCLK)和外部总线时钟(BCLK)。

WhenthePLLisselectedastheclocksource youmustenterthefollowingmodulesinmodule-stopstatebeforechangingthevalueofthisregister:USBHS SCE9.

此外，将SCKDIVCR中的任何值从较低的分频比更改为较高的分频比时，在更改该值之前至少等待750ns。

将任何值从较高的分频比更改为较低的分频比时，在更改该值后至少等待250ns，然后再开始后续处理。

测量等待时间的推荐方法是通过软件。

请务必考虑最坏情况，以确保经过所需的等待时间。

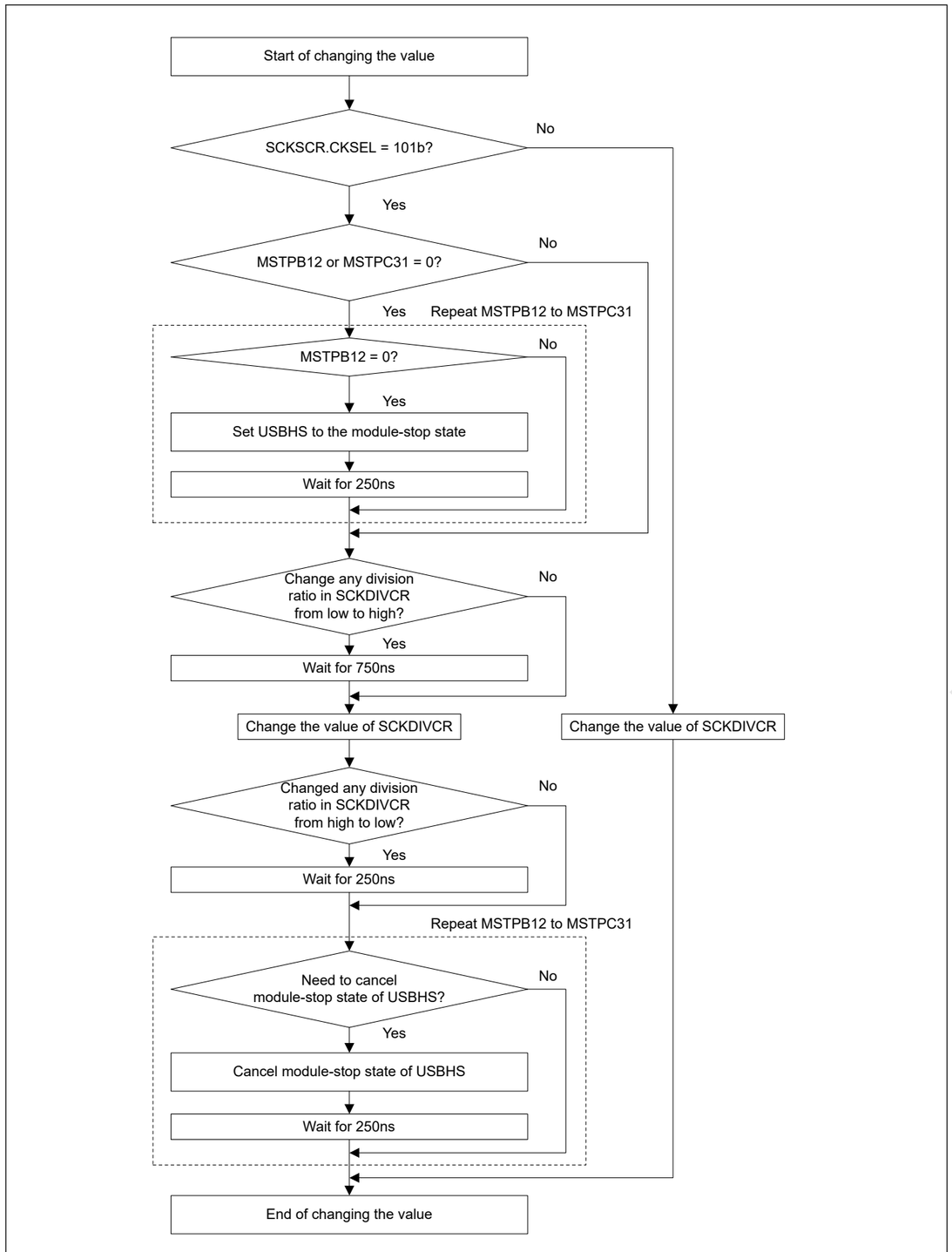

Figure 8.2 Example flow for changing the value of SCKDIVCR

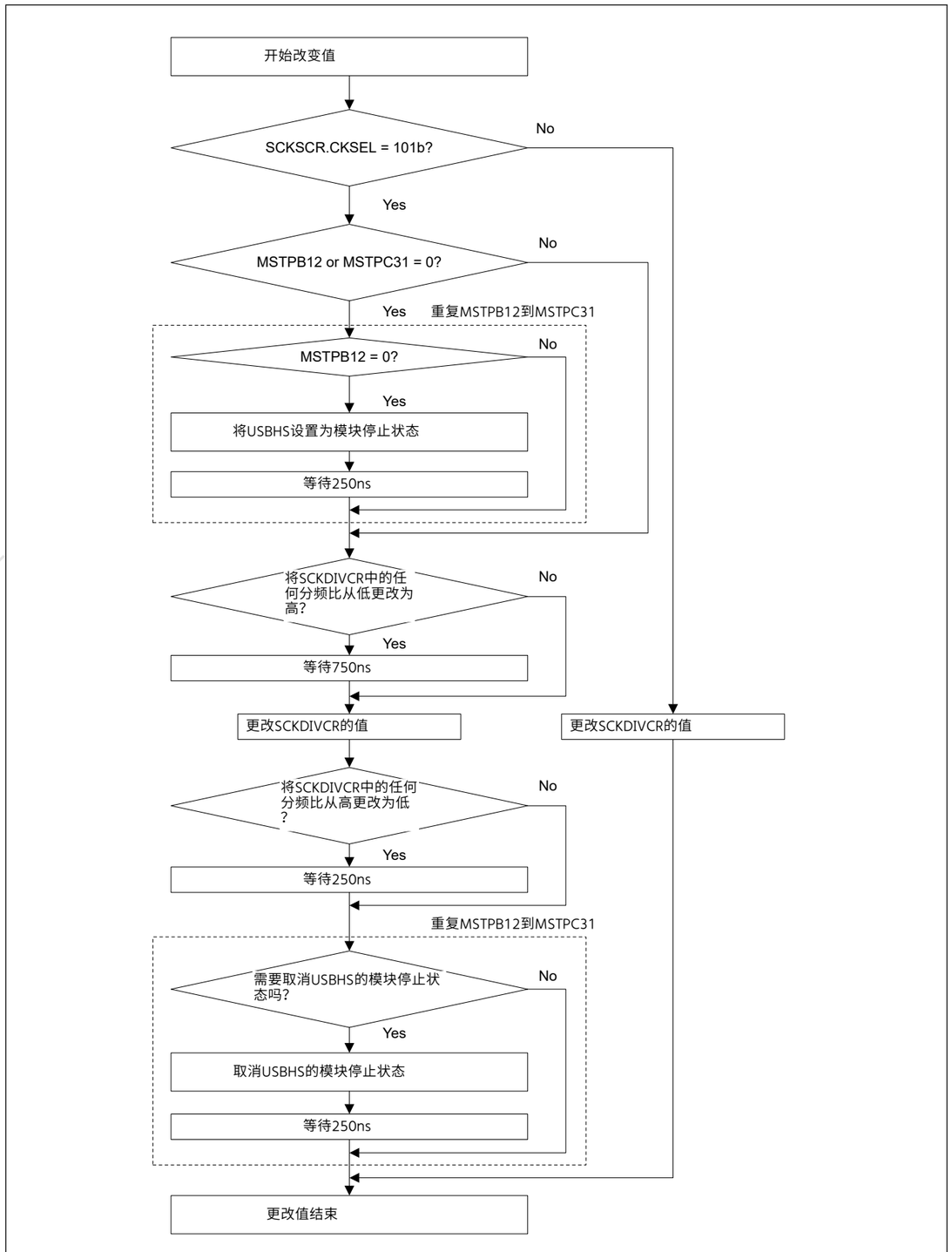

Figure 8.2 更改SCKDIVCR值的示例流程

8.2.3 SCKSCR : System Clock Source Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	Clock Source Select 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator (MOSC) 1 0 0: Sub-clock oscillator (SOSC) 1 0 1: PLL 1 1 0: Setting prohibited 1 1 1: Setting prohibited	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

The SCKSCR register selects the clock source for the system clock.

When changing the value of SCKSCR to either select or diselect the PLL, set the following modules to the module-stop state before changing the SCKSCR value: USBHS, SCE9.

In addition, when changing the value of SCKSCR from the PLL to a different clock source, wait at least 750 ns before changing the value.

When changing the value from a non-PLL clock source to the PLL, wait at least 250 ns after changing the value, before starting subsequent processing.

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

8.2.3 SCKSCR:系统时钟源控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x026

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CKSEL[2:0]	时钟源选择 000：HOCO001：MOCO010：LOCO011：主时钟振荡器（MOSC）100：副时钟振荡器（SOSC）101：PLL 110：禁止设置111:禁止设定	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

SCKSCR寄存器选择系统时钟的时钟源。

当更改SCKSCR的值以选择或取消选择PLL时，在更改SCKSCR值之前将以下模块设置为模块停止状态：USBHS、SCE9。

此外，当将SCKSCR的值从PLL更改为不同的时钟源时，在更改值之前至少等待750ns。

将值从非PLL时钟源更改为PLL时，更改值后至少等待250ns，然后再开始后续处理。

测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

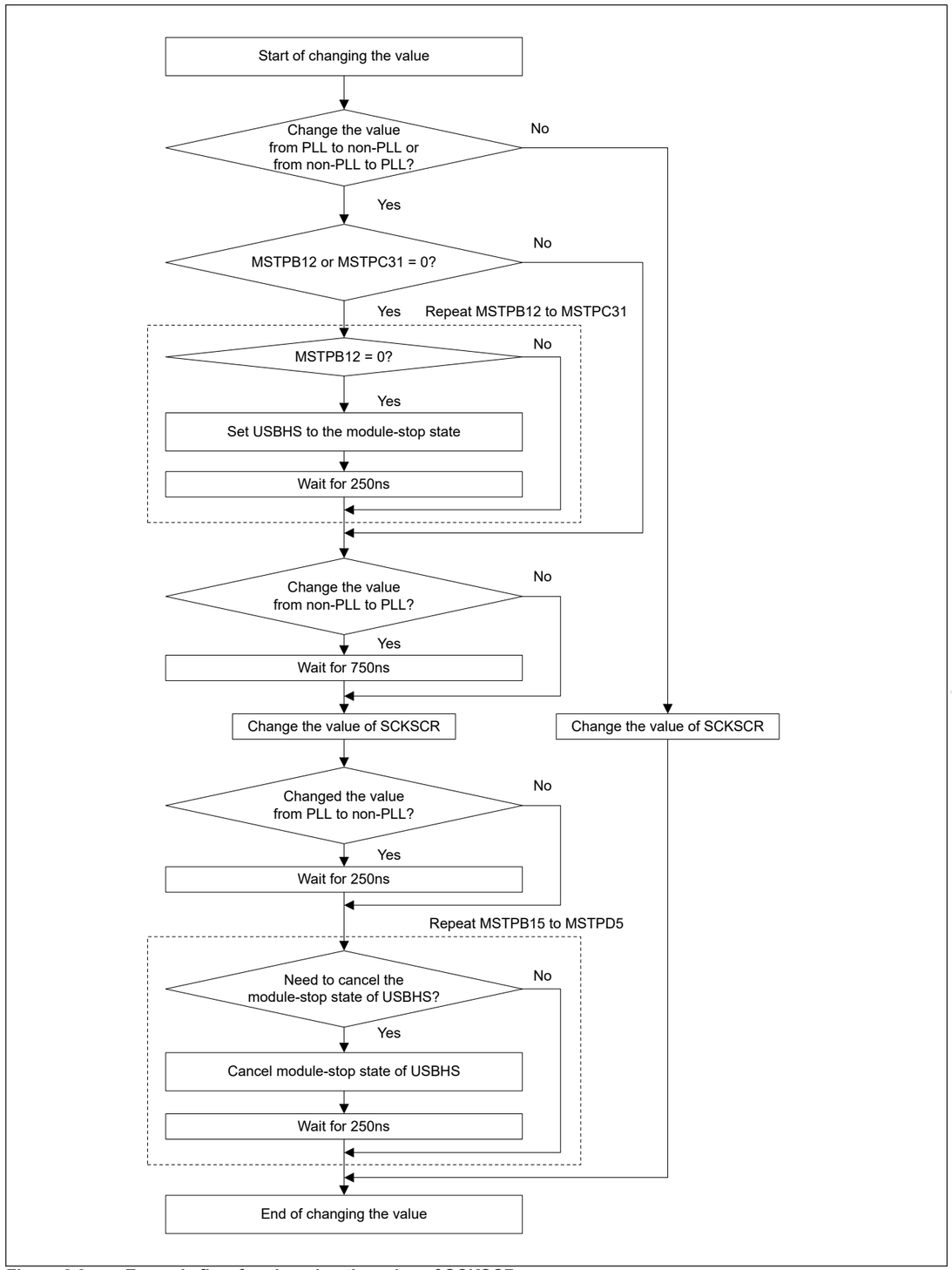

Figure 8.3 Example flow for changing the value of SCKSCR

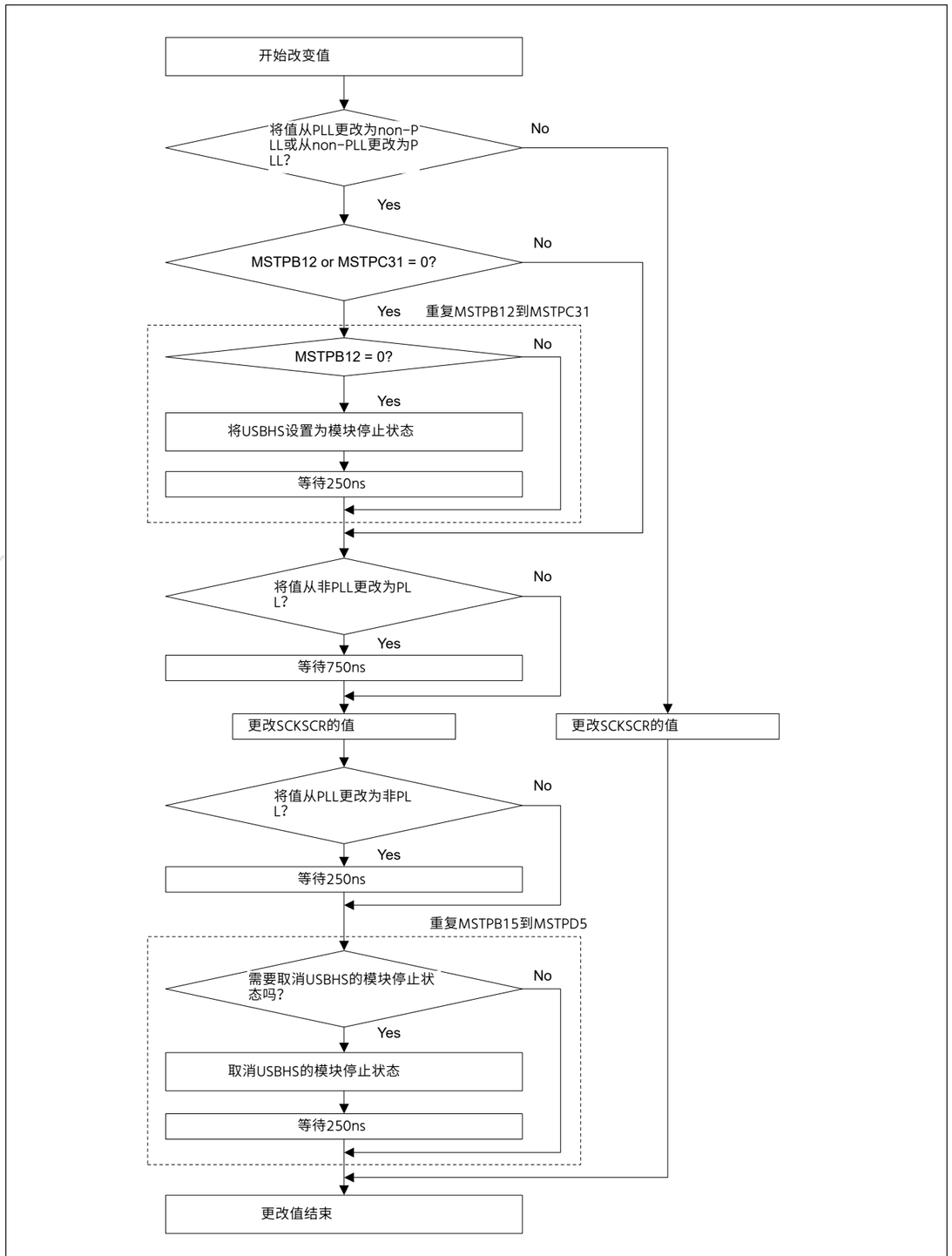

Figure 8.3 更改SCKSCR值的示例流程

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- FlashIF clock (FCLK)
- external bus clock (BCLK)

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator (MOSC)
- Sub-clock oscillator (SOSC)
- PLL

The operating state of each clock source is controlled not only by the clock oscillation enable settings but also by the operating modes of the product. Some clock sources might be forcibly stopped depending on the product operating mode being used.

Check the operation state of clock sources in each product operating mode, and do not select the clock source to be stopped in SCKSCR. The clock sources should be switched when there are no occurring internal asynchronous interrupt. For details, see section 10, Low Power Modes.

8.2.4 PLLCCR : PLL Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x028

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLLMUL[5:0]						—	—	—	PLSRCSEL	—	—	PLIDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PLIDIV[1:0]*1	PLL Input Frequency Division Ratio Select 0 0: /1 0 1: /2 1 0: /3 Others: Setting prohibited.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	PLSRCSEL	PLL Clock Source Select 0: Main clock oscillator 1: HOCO*3	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

CKSEL[2:0]位（时钟源选择）

CKSEL[2:0]位选择以下模块的源：

●系统时钟（ICLK）

●外设模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）

- FlashIF clock (FCLK)

●外部总线时钟（BCLK）

这些位从以下来源之一中选择：

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)

●主时钟振荡器（MOSC）

- Sub-clock oscillator (SOSC)
- PLL

每个时钟源的工作状态不仅由时钟振荡使能设置控制，还由产品的工作模式控制。根据所使用的产品操作模式，某些时钟源可能会被强制停止。

检查各产品工作模式下时钟源的运行状态，不要在SCKSCR中选择要停止的时钟源。当没有发生内部异步中断时，应切换时钟源。有关详细信息，请参阅第10节，低功耗模式。

8.2.4 PLLCCR:PLL时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x028

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLLMUL[5:0]						—	—	—	PLSRCSEL	—	—	PLIDIV[1:0]	
重置后的值：	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PLIDIV[1:0]*1	PLL输入分频比选择 0 0: /1 0 1: /2 1 0: /3 其他：禁止设置。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	PLSRCSEL	PLL时钟源选择 0：主时钟振荡器1：HOCO*3	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13:8	PLLMUL[5:0]*2	PLL Frequency Multiplication Factor Select 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 Others: Setting prohibited.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. PLIDIV[1:0] should be set so that the frequency of PLL input signal is within the range of section 8.1. Overview.
Note 2. PLLMUL[5:0] should be set so that the frequency of PLL output signal is within the range of section 8.1. Overview.
Note 3. The FLL function must be enabled when using USBCLK.

The PLLCCR register sets the operation of the PLL circuit.

Writing to the PLLCCR is prohibited when the PLLCR.PLLSTP bit is 0 (the PLL operates).

PLIDIV[1:0] bits (PLL Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL clock source.

PLSRCSEL bit (PLL Clock Source Select)

This bit selects the clock source for the PLL.

PLLMUL[5:0] bits (PLL Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL circuit.

8.2.5 PLLCR : PLL Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x02A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLLSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLLSTP	PLL Stop Control 0: PLL is operating 1: PLL is stopped.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The PLLCR register controls the operation of the PLL circuit.

Bit	Symbol	Function	R/W
13:8	PLLMUL[5:0]*2	PLL倍频因子选择 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 其他：禁止设置。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.应设置PLIDIV[1:0]，使PLL输入信号的频率在8.1节的范围内。概述。
注2.PLLMUL[5:0]应设置为使PLL输出信号的频率在8.1节的范围内。概述。
注3.使用USBCLK时必须使能FLL功能。

PLLCCR寄存器设置PLL电路的操作。

当PLLCR.PLLSTP位为0（PLL工作）时，禁止写入PLLCCR。

PLIDIV[1:0]位（PLL输入分频比选择）

这些位选择PLL时钟源的分频比。

PLSRCSEL位（PLL时钟源选择）

该位选择PLL的时钟源。

PLLMUL[5:0]位（PLL倍频因子选择）

这些位选择PLL电路的倍频因子。

8.2.5 PLLCR:PLL控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x02A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLLSTP
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLLSTP	PLL停止控制 0：PLL正在运行1： PLL停止。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

PLLCR寄存器控制PLL电路的操作。

PLLSTP bit (PLL Stop Control)

This bit runs or stops the PLL circuit.

If the main clock oscillator is to be selected as the clock source for the PLL by the PLLCCR.PLSRCSEL bit, the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set.

After the PLLSTP bit setting is changed to run the PLL, only use the PLL clock after confirming that the OSCSF.PLLSF bit is set to 1. That is, a fixed time for stabilization is required after starting the PLL operation. A fixed time is also required for oscillation to stop after stopping the PLL operation. Additionally, apply the following limitations when starting and stopping the PLL operation by the PLLSTP bit:

- After stopping the PLL, confirm that the OSCSF.PLLSF bit is 0 before restarting the PLL.
- Confirm that the PLL is operating and that the OSCSF.PLLSF bit is 1 before stopping the PLL.
- Regardless of whether the PLL clock is selected as the system clock, confirm that the OSCSF.PLLSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after operating the PLL.
- When transitioning to Software Standby or Deep Software Standby mode after stopping the PLL, confirm that the OSCSF.PLLSF bit is cleared to 0 before executing a WFI instruction.

Writing 1 to the PLLSTP bit is prohibited when SCKSCR.CKSEL[2:0] = 101 (system clock source = PLL).

Confirm the following conditions before writing 0 to PLLSTP:

- When PLL source clock = MOSC: MOSCCR.MOSTP = 0 (MOSC is enabled)
- When PLL source clock = HOCO: HOCOCR.HCSTP = 0 (HOCO is enabled).

8.2.6 PLL2CCR : PLL2 Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x048

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLL2MUL[5:0]						—	—	—	PL2SRCSEL	—	—	PL2IDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PL2IDIV[1:0]*1	PLL2 Input Frequency Division Ratio Select 0 0: /1 (value after reset) 0 1: /2 1 0: /3 Others: Setting prohibited.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	PL2SRCSEL	PLL2 Clock Source Select 0: Main clock oscillator 1: HOCO*3	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
13:8	PLL2MUL[5:0]*2	PLL2 Frequency Multiplication Factor Select 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 Others: Setting prohibited.	R/W

PLLSTP位（PLL停止控制）

该位运行或停止PLL电路。

如果要通过PLLCCR.PLSRCSEL位选择主时钟振荡器作为PLL的时钟源，则Main
必须设置时钟振荡器等待控制寄存器(MOSCWTCR)。

更改PLLSTP位设置以运行PLL后，只有在确认OSCSF.PLLSF位设置为1后才能使用PLL时钟。即，启动PLL操作后需要固定的稳定时间。在停止PLL操作后，振荡停止也需要一段固定的时间。此外，在通过PLLSTP位启动和停止PLL操作时应用以下限制：

●停止PLL后，请确认OSCSF.PLLSF位为0，然后再重新启动PLL。

●在停止PLL之前，确认PLL正在运行并且OSCSF.PLLSF位为1。

●无论是否选择PLL时钟作为系统时钟，在执行WFI指令之前，请确认OSCSF.PLLSF设置为1，以便在操作PLL后将MCU置于软件待机或深度软件待机模式。

●在停止PLL后转换到软件待机或深度软件待机模式时，请确认OSCSF.PLLSF位在执行WFI指令之前被清除为0。

当SCKSCR.CKSEL[2:0]=101（系统时钟源=PLL）时，禁止向PLLSTP位写入1。

在将0写入PLLSTP之前，请确认以下条件：

●当PLL源时钟=MOSC时：MOSCCR.MOSTP=0（启用MOSC）

●当PLL源时钟=HOCO时：HOCOCR.HCSTP=0（启用HOCO）。

8.2.6 PLL2CCR:PLL2时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x048

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PLL2MUL[5:0]						—	—	—	PL2SRCSEL	—	—	PL2IDIV[1:0]	
重置后的值:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PL2IDIV[1:0]*1	PLL2输入分频比选择 0 0: /1 (value after reset) 0 1: /2 1 0: /3 其他：禁止设置。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	PL2SRCSEL	PLL2时钟源选择 0：主时钟振荡器1：HOCO*3	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
13:8	PLL2MUL[5:0]*2	PLL2倍频因子选择 0x13: × 10.0 (value after reset) 0x14: × 10.5 0x15: × 11.0 ⋮ 0x1C: × 14.5 0x1D: × 15.0 0x1E: × 15.5 ⋮ 0x3A: × 29.5 0x3B: × 30.0 其他：禁止设置。	R/W

Bit	Symbol	Function	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note 1. PL2IDIV[1:0] should be set so that the frequency of PLL2 input signal is within the range of section 8.1. Overview.
Note 2. PLL2MUL[5:0] should be set so that the frequency of PLL2 output signal is within the range of section 8.1. Overview.
Note 3. The FLL function must be enabled when using USBCLK.

The PLL2CCR register sets the operation of the PLL2 circuit.

Writing to the PLL2CCR register is prohibited when the PLL2CR.PLL2STP bit is 0 (the PLL2 operates).

PL2IDIV[1:0] bits (PLL2 Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL2 clock source.

PL2SRCSEL bit (PLL2 Clock Source Select)

This bit selects the clock source for the PLL2.

PLL2MUL[5:0] bits (PLL2 Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL2 circuit.

8.2.7 PLL2CR : PLL2 Control Register

Base address: SYSC = 0x4001_E000
Offset address: 0x04A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLL2STP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLL2STP	PLL2 Stop Control 0: PLL2 is operating 1: PLL2 is stopped.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The PLL2CR register controls the operation of the PLL2 circuit.

PLL2STP bit (PLL2 Stop Control)

This bit runs or stops the PLL2 circuit.

If the main clock oscillator is to be selected as the clock source for the PLL2 by the PLL2CCR.PL2SRCSEL bit, the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set.

After the PLL2STP bit setting is changed to run the PLL2, only use the PLL2 clock after confirming that the OSCSF.PLL2SF bit is set to 1. That is, a fixed time for stabilization is required after starting the PLL2 operation. A fixed time is also required for oscillation to stop after stopping the PLL2 operation. Additionally, apply the following limitations when starting and stopping the PLL2 operation by the PLL2STP bit:

- After stopping the PLL2, confirm that the OSCSF.PLL2SF bit is 0 before restarting the PLL2.

Bit	Symbol	Function	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
注1.应设置PL2IDIV[1:0]，使PLL2输入信号的频率在8.1节的范围内。概述。
注2.PLL2MUL[5:0]应设置为使PLL2输出信号的频率在8.1节的范围内。概述。
注3.使用USBCLK时必须使能FLL功能。

PLL2CCR寄存器设置PLL2电路的操作。

当PLL2CR.PLL2STP位为0（PLL2工作）时，禁止写入PLL2CCR寄存器。

PL2IDIV[1:0]位（PLL2输入分频比选择）

这些位选择PLL2时钟源的分频比。

PL2SRCSEL位（PLL2时钟源选择）

该位选择PLL2的时钟源。

PLL2MUL[5:0]位（PLL2倍频因子选择）

这些位选择PLL2电路的倍频因子。

8.2.7 PLL2CR：PLL2控制寄存器

Base address: SYSC = 0x4001_E000
Offset address: 0x04A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	PLL2STP
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	PLL2STP	PLL2停止控制 0：PLL2正在运行1： PLL2停止。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

PLL2CR寄存器控制PLL2电路的操作。

PLL2STP位（PLL2停止控制）

该位运行或停止PLL2电路。

如果要通过PLL2CCR.PL2SRCSEL位选择主时钟振荡器作为PLL2的时钟源，则Main
必须设置时钟振荡器等待控制寄存器(MOSCWTCR)。

更改PLL2STP位设置运行PLL2后，确认
OSCSF.PLL2SF位设置为1。也就是说，在启动PLL2操作后需要一个固定的稳定时间。在停止PLL2操作后，振荡停止也需要一个固定的时间。此外，在通过PLL2STP位启动和停止PLL2操作时应用以下限制：

●停止PLL2后，确认OSCSF.PLL2SF位为0，再重启PLL2。

- Confirm that the PLL2 is operating and that the OSCSF.PLL2SF bit is 1 before stopping the PLL2.
- Confirm that the OSCSF.PLL2SF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after operating the PLL2.
- When transitioning to Software Standby or Deep Software Standby mode after stopping the PLL2, confirm that the OSCSF.PLL2SF bit is cleared to 0 before executing a WFI instruction.

Confirm the following conditions before writing 0 to PLL2STP:

- When the PLL2 source clock = MOSC: MOSCCR.MOSTP = 0 (MOSC is enabled)
- When the PLL2 source clock = HOCO: HOCOCR.HCSTP = 0 (HOCO is enabled).

8.2.8 BCKCR : External Bus Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x030

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCLKDIV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCLKDIV	BCLK Pin Output Select 0: BCLK 1: BCLK/2.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The BCKCR register controls the external bus clock.

BCLKDIV bit (BCLK Pin Output Select)

This bit selects the clock signal for output from the BCLK pin.

Either the BCLK clock with the frequency selected by the BCK[2:0] bits in SCKDIVCR or the BCLK clock divided by 2 can be selected.

8.2.9 MOSCCR : Main Clock Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	Main Clock Oscillator Stop 0: Operate the main clock oscillator*1 1: Stop the main clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

●在停止PLL2之前，确认PLL2正在运行并且OSCSF.PLL2SF位为1。

●在操作PLL2后，在执行WFI指令以将MCU置于软件待机或深度软件待机模式之前，确认OSCSF.PLL2SF位设置为1。

●在停止PLL2后转换到软件待机或深度软件待机模式时，请确认OSCSF.PLL2SF位在执行WFI指令之前被清除为0。

在将0写入PLL2STP之前，请确认以下条件：

●当PLL2源时钟=MOSC时：MOSCCR.MOSTP=0（启用MOSC）

●当PLL2源时钟=HOCO时：HOCOCR.HCSTP=0（启用HOCO）。

8.2.8 BCKCR:外部总线时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x030

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCLKDIV
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCLKDIV	BCLK引脚输出选择 0: BCLK 1: BCLK/2.	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

BCKCR寄存器控制外部总线时钟。

BCLKDIV位（BCLK引脚输出选择）

该位选择从BCLK引脚输出的时钟信号。

可以选择频率由SCKDIVCR中的BCK[2:0]位选择的BCLK时钟或除以2的BCLK时钟。

8.2.9 MOSCCR:主时钟振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x032

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MOSTP
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	MOSTP	主时钟振荡器停止 0:运行主时钟振荡器*1 1：停止主时钟振荡器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator.

When changing the value of the MOSTP bit, execute subsequent instructions only after reading the bit to check that the value is updated.

When using the main clock, the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) must be set before setting MOSTP to 0. After setting the MOSTP bit to 0, confirm that the OSCSF.MOSCSF bit is set to 1 before using the main clock oscillator.

A fixed stabilization wait time is required after setting the main clock oscillator to start operation. A fixed wait time is also required for oscillation to stop after stopping the main clock oscillator.

The following restrictions apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator operates and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode.
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is set to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and PLLCR.PLLSTP = 0 (PLL is operating)
- PLL2CCR.PL2SRCSEL = 0 (PLL2 source clock = MOSC) and PLL2CR.PLL2STP = 0 (PLL2 is operating)

8.2.10 SOSCCR : Sub-Clock Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x480

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOSTP	Sub Clock Oscillator Stop 0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.在将MOSTP设置为0之前，必须设置MOMCR寄存器。

MOSCCR寄存器控制主时钟振荡器。

MOSTP位（主时钟振荡器停止）

MOSTP位启动或停止主时钟振荡器。

更改MOSTP位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。

使用主时钟时，必须先设置主时钟振荡器模式振荡控制寄存器(MOMCR)和主时钟振荡器等待控制寄存器(MOSCWTCR)，然后再将MOSTP设置为0。将MOSTP位设置为0后，确认OSCSF。MOSCSF位在使用主时钟振荡器之前设置为1。

设置主时钟振荡器开始工作后，需要一个固定的稳定等待时间。停止主时钟振荡器后，振荡停止也需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止主时钟振荡器后，请确认OSCSF.MOSCSF位为0，然后再重新启动主时钟振荡器

●在停止主时钟振荡器之前，确认主时钟振荡器工作并且OSCSF.MOSCSF位为1

●无论是否选择主时钟振荡器作为系统时钟，在执行WFI指令之前确认OSCSF.MOSCSF位设置为1，将MCU置于软件待机或深度软件待机模式。

●当转换到软件待机或深度软件待机模式是按照设置停止主时钟振荡器时，在执行WFI指令之前确认OSCSF.MOSCSF位设置为0。

在以下情况下禁止向MOSTP写入1：

●SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

●PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）

●PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和PLLCR.PLLSTP=0（PLL正在运行）

●PLL2CCR.PL2SRCSEL=0（PLL2源时钟=MOSC）和PLL2CR.PLL2STP=0（PLL2正在运行）

8.2.10 SOSCCR：副时钟振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x480

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SOSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOSTP	副时钟振荡器停止 0：运行副时钟振荡器*1 1：停止副时钟振荡器	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The SOMCR register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

SOSTP bit (Sub Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator. When changing the value of the SOSTP bit, only execute subsequent instructions after reading the bit to check that the value is updated. Use the SOSTP bit when using the sub-clock oscillator as the source for a peripheral module, for example the RTC. When using the sub-clock oscillator, set the Sub-Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0.

The following restrictions apply when starting and stopping the operation:

- After stopping the sub-clock oscillator, allow a stop interval of at least 5 SOSC clock cycles before restarting it
- After setting the SOSTP bit to 0, use the sub-clock only after the sub-clock oscillation stabilization time ($t_{SUBOSCWT}$) has elapsed.
- Regardless of whether the sub-clock oscillator is selected as the system clock, confirm that the sub-clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least 3 SOSC clock cycles before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

8.2.11 LOCOCR : Low-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	LOCO Stop 0: Operate the LOCO clock 1: Stop the LOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The LOCOCR register controls the LOCO clock.

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO clock.

After setting the LCSTP bit to 0 to start the LOCO clock, only use the clock after the LOCO clock-oscillation stabilization wait time (t_{LOCOWT}) elapses. A fixed stabilization wait time is required after setting the LOCO clock to start operation. A fixed wait time is also required after setting the LOCO clock to stop.

The following restrictions apply when starting and stopping operation:

- After stopping the LOCO clock, allow a stop interval of at least 5 LOCO clock cycles before restarting it
- Confirm that LOCO oscillation is stable before stopping the LOCO clock

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.在将SOSTP设置为0之前，必须设置SOMCR寄存器。

SOSCCR寄存器控制副时钟振荡器。

SONTP位（副时钟振荡器停止）

SONTP位启动或停止副时钟振荡器。更改SOTP位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。当使用副时钟振荡器作为外围模块（例如RTC）的源时，使用SOTP位。使用副时钟振荡器时，请先设置副时钟振荡器模式控制寄存器(SOMCR)，然后再将SOSTP设置为0。

启动和停止操作时适用以下限制：

●子时钟振荡器停止后，在重新启动之前允许至少5个SOSC时钟周期的停止间隔

●将SOSTP位设置为0后，仅在副时钟振荡稳定时间(tSUBOSCWT)过去后使用副时钟。

●无论是否选择副时钟振荡器作为系统时钟，在执行WFI指令之前确认副时钟振荡稳定，将MCU置于软件待机或深度软件待机模式

●当根据设置转换到软件待机或深度软件待机模式以停止副时钟振荡器时，请等待至少3个SOSC时钟周期，然后再执行WFI指令。

在以下情况下禁止向SOTP写入1：

●SCKSCR.CKSEL[2:0]=100b（系统时钟源=SOSC）。

8.2.11 LOCOCR：低速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x490

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	LCSTP	机车站 0：运行LOCO时钟1：停止LOCO时钟	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

LOCOCR寄存器控制LOCO时钟。

LCSTP bit (LOCO Stop)

LCSTP位启动或停止LOCO时钟。

将LCSTP位设置为0以启动LOCO时钟后，仅在LOCO时钟振荡稳定等待时间(tLOCOWT)过去后使用时钟。设置LOCO时钟开始运行后，需要一个固定的稳定等待时间。将LOCO时钟设置为停止后，还需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止LOCO时钟后，在重新启动之前允许至少5个LOCO时钟周期的停止间隔

●在停止LOCO时钟之前确认LOCO振荡稳定

- Regardless of whether the LOCO is selected as the system clock, confirm that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the LOCO clock, wait for at least 3 LOCO cycles before executing the WFI instruction.

Writing 1 to LCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

Because the LOCO clock measures the wait time for other oscillators, it continues to oscillate while measuring this time, regardless of the setting in LOCOCR.LCSTP. As a result, the LOCO clock might be unintentionally supplied even when the LCSTP is set to stop.

8.2.12 HOCOCR : High-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0: Operate the HOCO clock *2 1: Stop the HOCO clock	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If you are using the HOCO (HCSTP = 0), set the OFS1.HOCOFRQ0[1:0] bit to an optimum value.

The HOCOCR register controls the HOCO clock.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO clock.

After setting the HCSTP bit to 0 to start the HOCO clock, confirm that the OSCSF.HOCOSF is set to 1 before using the clock. When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is also set to 1 before using the HOCO clock. A fixed stabilization wait time is required after setting the HOCO clock to start operation. A fixed wait time is also required after setting the HOCO clock to stop.

The following limitations apply when starting and stopping operation:

- After stopping the HOCO clock, confirm that the OSCSF.HOCOSF is 0 before restarting the HOCO clock.
- Confirm that the HOCO clock operates and that the OSCSF.HOCOSF is 1 before stopping the HOCO clock.
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOCOSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode after setting HOCO operation with the HCSTP bit.
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting of the HOCO clock to stop, confirm that the OSCSF.HOCOSF is set to 0 after setting the HOCO clock and before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following conditions:

●无论是否选择LOCO作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认LOCO振荡稳定

●当转换到软件待机或深度软件待机模式是按照设置停止LOCO时钟时，在执行WFI指令之前至少等待3个LOCO周期。

在以下情况下禁止向LCSTP写入1：

●SCKSCR.CKSEL[2:0]=010b（系统时钟源=LOCO）。

因为LOCO时钟测量其他振荡器的等待时间，所以无论LOCOCR.LCSTP中的设置如何，它都会在测量该时间时继续振荡。因此，即使LCSTP设置为停止，也可能会无意中提供LOCO时钟。

8.2.12 HOCOCR:高速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x036

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	HCSTP
重置后的值:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HCSTP	HOCO Stop 0：运行HOCO时钟*2 1：停止HOCO时钟	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.OFS1.HOCOEN位为0时复位后的HCSTP位值为0。OFS1.HOCOEN位为1时为1。
注2.如果您使用HOCO(HCSTP=0)，请将OFS1.HOCOFRQ0[1:0]位设置为最佳值。

HOCOCR寄存器控制HOCO时钟。

HCSTP bit (HOCO Stop)

HCSTP位启动或停止HOCO时钟。

将HCSTP位设置为0以启动HOCO时钟后，在使用时钟之前确认OSCSF.HOCOSF设置为1。当OFS1.HOCOEN设置为0时，请在使用HOCO时钟之前确认OSCSF.HOCOSF也设置为1。设置HOCO时钟开始运行后，需要一个固定的稳定等待时间。将HOCO时钟设置为停止后，还需要一个固定的等待时间。

启动和停止操作时适用以下限制：

●停止HOCO时钟后，确认OSCSF.HOCOSF为0，再重新启动HOCO时钟。

●在停止HOCO时钟之前，请确认HOCO时钟运行并且OSCSF.HOCOSF为1。

●无论是否选择HOCO时钟作为系统时钟，确认OSCSF.HOCOSF设置为1
在使用HCSTP位设置HOCO操作后，执行WFI指令以将MCU置于软件待机或深度软件待机模式之前。

●当转换到软件待机或深度软件待机模式是跟随HOCO时钟的设置停止时，在设置HOCO时钟之后和执行WFI指令之前确认OSCSF.HOCOSF设置为0。

在以下情况下禁止向HCSTP写入1：

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO).
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and PLLCR.PLLSTP = 0 (PLL is operating)
- PLL2CCR.PL2SRCSEL = 1 (PLL2 source clock = HOCO) and PLL2CR.PLL2STP = 0 (PLL2 is operating)

8.2.13 MOCOCR : Middle-Speed On-Chip Oscillator Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0: MOCO clock is operating 1: MOCO clock is stopped	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The MOCOCR register controls the MOCO clock.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO clock.

After setting MCSTP to 0, use the MOCO clock only after the MOCO clock oscillation stabilization time (t_{MOCOWT}) elapses. A fixed stabilization wait time is required after setting the MOCO clock to start operation. A fixed wait time is also required for oscillation to stop after setting the MOCO clock to stop operation.

The following restrictions apply when starting and stopping the oscillator:
- After stopping the MOCO clock, allow a stop interval of at least 5 MOCO clock cycles before restarting it
- Confirm that MOCO clock oscillation is stable before stopping the MOCO clock
- Regardless of whether the MOCO clock is selected as the system clock, confirm that MOCO clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow the setting to stop the MOCO clock, wait for at least 3 MOCO clock cycles before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:
- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Control Register (OSTDCR.OSTDE).

●SCKSCR.CKSEL[2:0]=000b（系统时钟源=HOCO）。

●PLLCCR.PLSRCSEL=1（PLL源时钟=HOCO）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）

●PLLCCR.PLSRCSEL=1（PLL源时钟=HOCO）和PLLCR.PLLSTP=0（PLL正在运行）

●PLL2CCR.PL2SRCSEL=1（PLL2源时钟=HOCO）和PLL2CR.PLL2STP=0（PLL2正在运行）

8.2.13 MOCOCR:中速片上振荡器控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x038

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MCSTP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MCSTP	MOCO Stop 0：MOCO时钟运行1：MOCO时钟停止	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

MOCOCR寄存器控制MOCO时钟。

MCSTP bit (MOCO Stop)

MCSTP位启动或停止MOCO时钟。

将MCSTP设置为0后，仅在MOCO时钟振荡稳定时间(tMOCOWT)过去后使用MOCO时钟。设置MOCO时钟开始运行后，需要一个固定的稳定等待时间。在将MOCO时钟设置为停止操作后，振荡停止也需要一个固定的等待时间。

启动和停止振荡器时适用以下限制：

●停止MOCO时钟后，在重新启动之前允许至少5个MOCO时钟周期的停止间隔

●确认MOCO时钟振荡稳定后再停止MOCO时钟

●无论是否选择MOCO时钟作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认MOCO时钟振荡稳定

●当按照设置转换到软件待机或深度软件待机模式以停止MOCO时钟时，请等待至少3个MOCO时钟周期，然后再执行WFI指令。

在以下情况下禁止向MCSTP写入1：

●SCKSCR.CKSEL[2:0]=001b（系统时钟源=MOCO）。

如果在Oscillation中使能了振荡停止检测，则禁止向MCSTP位写入1（停止MOCO）停止检测控制寄存器(OSTDCR.OSTDE)。

8.2.14 FLLCR1 : FLL Control Register1

Base address: SYSC = 0x4001_E000

Offset address: 0x039

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FLLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FLLEN	FLL Enable 0: FLL function is disabled 1: FLL function is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: HOCO must be stopped (HOCOCR.HCSTP = 1) before FLLCR1.FLLEN is modified.
Note: SOSC must be operating with stabilization while FLL is enabled (FLLCR1.FLLEN = 1).
Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The FLLCR1 register controls the FLL function of the HOCO.

FLLEN bit (FLL Enable)

This bit enables or disables the FLL function of the HOCO.

If FLL is enabled, the frequency accuracy is guaranteed after FLL is stabilized. The FLL stabilization can be checked by the CAC frequency measurement, but it must be executed after HOCO stabilization.

In addition, you must disable FLL by setting the FLLEN bit to 0 before transitioning to Software Standby mode.

Table 8.4 show an example flow of the FLL setting for each case.

Table 8.4 FLL setting flow (1 of 2)

Step		Operation
After reset release/deep software standby cancellation	1	Start (After reset release / deep software standby cancellation)
	2	FLL setting (FLLCR2.FLLCNTL)
	3	Enable FLL (FLLCR1.FLLEN = 1) Note: SOSC must be running with the oscillation stabilization.
	4	Enable HOCO (HOCOCR.HCSTP = 0)
	5	Wait for the FLL stabilization (t_{FLLWT})
	6	Check the HOCO stabilization (OSCSF.HOCOSF = 1)
	7	End (HOCO can be used.)

8.2.14 FLLCR1 : FLL Control Register1

Base address: SYSC = 0x4001_E000

Offset address: 0x039

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FLLEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FLLEN	FLL Enable 0：禁用FLL功能1：启用FLL功能。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在修改FLLCR1.FLLEN之前，必须停止HOCO（HOCOCR.HCSTP=1）。
Note: SOSC必须在启用FLL时稳定运行(FLLCR1.FLLEN=1)。
Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

FLLCR1寄存器控制HOCO的FLL功能。

FLLEN bit (FLL Enable)

该位启用或禁用HOCO的FLL功能。

如果启用FLL，则在FLL稳定后，频率精度得到保证。FLL稳定性可以通过CAC频率测量，但必须在HOCO稳定后执行。

此外，在转换到软件待机模式之前，您必须通过将FLLEN位设置为0来禁用FLL。

表8.4显示了每种情况下FLL设置的示例流程。

Table 8.4 FLL设置流程(1of2)

Step		Operation
复位后释放深度软件待机取消	1	启动（复位后释放深度软件待机取消）
	2	FLL setting (FLLCR2.FLLCNTL)
	3	Enable FLL (FLLCR1.FLLEN = 1) Note: SOSC必须在振荡稳定的情况下运行。
	4	Enable HOCO (HOCOCR.HCSTP = 0)
	5	等待FLL稳定(tFLLWT)
	6	检查HOCO稳定性(OSCSF.HOCOSF=1)
	7	结束（可以使用HOCO。）

Table 8.4 FLL setting flow (2 of 2)

Step		Operation
Software standby transition/ cancellation	1	Start (FLL is being used.)
	2	Stop HOCO (HOCOCR.HCSTP = 1) Note: If HOCO is used as the system clock or the PLL reference clock, these clock source must be changed to another clock before HOCO is stopped.
	3	Disable FLL (FLLCR1.FLLEN = 0)
	4	WFI instruction
	5	Software standby mode
	6	Software standby cancellation
	7	Enable FLL (FLLCR1.FLLEN = 1)
	8	Enable HOCO (HOCOCR.HCSTP = 0)
	9	Wait for the FLL stabilization (t_{FLLWT})
	10	Check the HOCO stabilization (OSCSF.HOCOSF = 1)
	11	End (HOCO can be used.)

8.2.15 FLLCR2 : FLL Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLLCNTL[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FLLCNTL[10:0]	FLL Multiplication Control When OFS1.HOCOFRQ[1:0] is 00b (16MHz), these bits must be set to 0x1E9. When OFS1.HOCOFRQ[1:0] is 01b (18MHz), these bits must be set to 0x226. When OFS1.HOCOFRQ[1:0] is 10b (20MHz), these bits must be set to 0x263. Other settings are prohibited.	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The FLLCR2 register controls the FLL function of the HOCO.

FLLCNTL[10:0] bits (FLL Multiplication Control)

These bits select the multiplication ratio of the FLL reference clock.

These bits must be set before FLL is enabled (FLLCR1.FLLEN=1).

Table 8.4 FLL设置流程(2of2)

Step		Operation
软件待机转换取消	1	开始（正在使用FLL。）
	2	Stop HOCO (HOCOCR.HCSTP = 1) Note: 如果HOCO用作系统时钟或PLL参考时钟，则这些时钟源必须在HOCO停止之前更改为另一个时钟。
	3	Disable FLL (FLLCR1.FLLEN = 0)
	4	WFI instruction
	5	软件待机模式
	6	软件待机取消
	7	Enable FLL (FLLCR1.FLLEN = 1)
	8	Enable HOCO (HOCOCR.HCSTP = 0)
	9	等待FLL稳定(tFLLWT)
	10	检查HOCO稳定性(OSCSF.HOCOSF=1)
	11	结束（可以使用HOCO。）

8.2.15 FLLCR2 : FLL Control Register2

Base address: SYSC = 0x4001_E000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLLCNTL[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FLLCNTL[10:0]	FLL乘法控制 当OFS1.HOCOFRQ[1:0]为00b(16MHz)时，这些位必须设置为0x1E9。当OFS1.HOCOFRQ[1:0]为01b(18MHz)时，这些位必须设置为0x226。当OFS1.HOCOFRQ[1:0]为10b(20MHz)时，这些位必须设置为0x263。 禁止其他设置。	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

FLLCR2寄存器控制HOCO的FLL功能。

FLLCNTL[10:0]位（FLL乘法控制）

这些位选择FLL参考时钟的倍频比。

这些位必须在启用FLL之前设置(FLLCR1.FLLEN=1)。

8.2.16 OSCSF : Oscillation Stabilization Flag Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PLL2SF	PLLSF	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO Clock Oscillation Stabilization Flag 0: The HOCO clock is stopped or is not yet stable 1: The HOCO clock is stable, so is available for use as the system clock	R
2:1	—	These bits are read as 0.	R
3	MOSCSF	Main Clock Oscillation Stabilization Flag 0: The main clock oscillator is stopped (MOSTP = 1) or is not yet stable*2 1: The main clock oscillator is stable, so is available for use as the system clock	R
4	—	This bit is read as 0.	R
5	PLLSF	PLL Clock Oscillation Stabilization Flag 0: The PLL clock is stopped, or oscillation of the PLL clock is not stable yet 1: The PLL clock is stable, so is available for use as the system clock	R
6	PLL2SF	PLL2 Clock Oscillation Stabilization Flag 0: The PLL2 clock is stopped, or oscillation of the PLL2 clock is not stable yet 1: The PLL2 clock is stable	R
7	—	These bits are read as 0.	R

Note 1. The value after reset depends on the OFS1.HOCOEN setting.
When OFS1.HOCOEN = 1 (disable HOCO), the value after reset of HOCOSF is 0.
When OFS1.HOCOEN = 0 (enable HOCO), the HOCOSF value is set to 0 immediately after reset is released, and the HOCOSF value is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. This is true when an appropriate value is set in the Wait Control register for the main clock oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation is stable.

This register is not controlled by CGFSAR register.

The OSCSF register contains flags to indicate the operating status of the counters in the oscillation stabilization wait circuits for the individual oscillators. After oscillation starts, these counters measure the wait time until each oscillator output clock is supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that OSCSF.HOCOSF is set to 1 before using the HOCO clock.

[Setting condition]

- When the HOCO clock is stopped and the HOCOCR.HCSTP bit is set to 0, and then the HOCO oscillation stabilization time is counted by the LOCO clock and supply of the HOCO clock within the MCU is started. For the HOCO oscillation stabilization time, see section 53, Electrical Characteristics.

[Clearing condition]

- When the HOCO clock is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating status of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

8.2.16 OSCSF:振荡稳定标志寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PLL2SF	PLLSF	—	MOSCSF	—	—	HOCOSF
重置后的值:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Function	R/W
0	HOCOSF	HOCO时钟振荡稳定标志 0：HOCO时钟停止或尚未稳定1：HOCO时钟稳定，可用作系统时钟	R
2:1	—	这些位读为0。	R
3	MOSCSF	主时钟振荡稳定标志 0：主时钟振荡器停止（MOSTP=1）或尚未稳定*2 1：主时钟振荡器稳定，可作为系统时钟使用	R
4	—	该位读为0。	R
5	PLLSF	PLL时钟振荡稳定标志 0：PLL时钟停止，或PLL时钟振荡尚未稳定1：PLL时钟稳定，可用作系统时钟	R
6	PLL2SF	PLL2时钟振荡稳定标志 0：PLL2时钟停止，或PLL2时钟振荡尚未稳定1：PLL2时钟稳定	R
7	—	这些位读为0。	R

注1.复位后的值取决于OFS1.HOCOEN的设置。
当OFS1.HOCOEN=1（禁用HOCO）时，HOCOSF复位后的值为0。
当OFS1.HOCOEN=0（启用HOCO）时，释放复位后立即将HOCOSF值设置为0，并在经过HOCO振荡稳定等待时间后将HOCOSF值设置为1。

注2.当主时钟振荡器的等待控制寄存器中设置了适当的值时，这是正确的。如果等待时间值不够，则将振荡稳定标志设置为1，并在振荡稳定之前开始向内部电路提供时钟信号。

该寄存器不受CGFSAR寄存器控制。

OSCSF寄存器包含用于指示各个振荡器的振荡稳定等待电路中的计数器的操作状态的标志。振荡开始后，这些计数器测量等待时间，直到每个振荡器输出时钟被提供给内部电路。计数器溢出表明时钟供应稳定并可用于相关电路。

HOCOSF标志（HOCO时钟振荡稳定标志）

HOCOSF标志指示测量高速时钟振荡器(HOCO)等待时间的计数器的操作状态。当OFS1.HOCOEN设置为0时，请在使用HOCO时钟之前确认OSCSF.HOCOSF设置为1。

[Setting condition]

●当HOCO时钟停止并且HOCOCR.HCSTP位设置为0时，然后通过LOCO时钟计算HOCO振荡稳定时间并开始提供MCU内的HOCO时钟。关于HOCO振荡稳定时间，请参见第53节，电气特性。

[Clearing condition]

●HOCO时钟正在运行，然后由于HOCOCR.HCSTP位设置为1而被停用。

MOSCSF标志（主时钟振荡稳定标志）

MOSCSF标志指示测量主时钟振荡器等待时间的计数器的操作状态。

[Setting condition]

- When the main clock oscillator is stopped and the MOSCCR.MOSTP bit is set to 0, and then the number of LOCO clock cycles corresponding to the setting of the MOSCWTCR register is counted and supply of the main clock within the MCU is started.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

PLLSF flag (PLL Clock Oscillation Stabilization Flag)

The PLLSF flag indicates the operating state of the counter that measures the wait time of the PLL.

[Setting condition]

- When the PLL is stopped and the PLLCR.PLLSTP bit is set to 0, and then the PLL oscillation stabilization time is counted by the LOCO clock and supply of the PLL clock within the MCU is started. If oscillation by the PLL clock source is not stable when the PLLCR.PLLSTP bit is set to 0, counting of the LOCO cycles continues even after the PLL clock source oscillation is stabilized. For the PLL oscillation stabilization time, see section 53, Electrical Characteristics.

[Clearing condition]

- When the PLL is operating and then is deactivated because the PLLCR.PLLSTP bit is set to 1.

PLL2SF flag (PLL2 Clock Oscillation Stabilization Flag)

The PLL2SF flag indicates the operating state of the counter that measures the wait time of the PLL2.

[Setting condition]

- When the PLL2 is stopped and the PLL2CR.PLL2STP bit is set to 0, and then the PLL2 oscillation stabilization time is counted by the LOCO clock and supply of the PLL2 clock within the MCU is started. If oscillation by the PLL2 clock source is not stable when the PLL2CR.PLL2STP bit is set to 0, counting of the LOCO cycles continues even after the PLL2 clock source oscillation is stabilized. For the PLL2 oscillation stabilization time, see section 53, Electrical Characteristics.

[Clearing condition]

- When the PLL2 is operating and then is deactivated because the PLL2CR.PLL2STP bit is set to 1.

8.2.17 OSTDCR : Oscillation Stop Detection Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	Oscillation Stop Detection Interrupt Enable 0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG)	R/W
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	OSTDE	Oscillation Stop Detection Function Enable 0: Disable oscillation stop detection function 1: Enable oscillation stop detection function	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

●当主时钟振荡器停止并且MOSCCR.MOSTP位设置为0，然后LOCO的个数与MOSCWTCR寄存器的设置相对应的时钟周期被计数，并开始提供MCU内的主时钟。

[Clearing condition]

●当主时钟振荡器正在运行，然后因为MOSCCR.MOSTP位被设置为1而被禁用时。

PLLSF标志（PLL时钟振荡稳定标志）

PLLSF标志指示测量PLL等待时间的计数器的操作状态。

[Setting condition]

●当PLL停止并且PLLCR.PLLSTP位设置为0时，然后PLL振荡稳定时间由LOCO时钟计数并开始提供MCU内的PLL时钟。如果当PLLCR.PLLSTP位设置为0时PLL时钟源的振荡不稳定，即使PLL时钟源振荡稳定后，LOCO周期的计数也会继续。关于PLL振荡稳定时间，请参见第53节，电气特性。

[Clearing condition]

●当PLL正在运行然后因为PLLCR.PLLSTP位设置为1而被停用时。

PLL2SF标志（PLL2时钟振荡稳定标志）

PLL2SF标志指示测量PLL2等待时间的计数器的操作状态。

[Setting condition]

●当PLL2停止并且PLL2CR.PLL2STP位设置为0时，然后PLL2振荡稳定时间由LOCO时钟计数并开始提供MCU内的PLL2时钟。如果当PLL2CR.PLL2STP位设置为0时PLL2时钟源的振荡不稳定，即使在PLL2时钟源振荡稳定后，LOCO周期的计数也会继续。有关PLL2振荡稳定时间，请参见第53节，电气

Characteristics.

[Clearing condition]

●当PLL2正在运行，然后因为PLL2CR.PLL2STP位设置为1而被停用时。

8.2.17 OSTDCR:振荡停止检测控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x040

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OSTDE	—	—	—	—	—	—	OSTDIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDIE	振荡停止检测中断使能 0：禁止振荡停止检测中断（不通知POEG）1：使能振荡停止检测中断（通知POEG）	R/W
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	OSTDE	振荡停止检测功能启用 0：禁用振荡停止检测功能1：启用振荡停止检测功能	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is reported to the POEG.

If the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, set the OSTDIE bit to 0 before clearing OSTDF. Wait for at least 2 PCLKB cycles before setting the OSTDIE bit to 1. By reading the I/O register whose access cycle number is defined by PCLKB, it is possible to secure waiting time of 2 or more cycles of PCLKB.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function.

When the OSTDE bit is 1 (enabled), the MOCO stop bit (MOCOCR.MCSTP) is set to 0 and the MOCO operation starts. The MOCO clock cannot be stopped while the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the Oscillation Stop Detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

The OSTDE bit must be set to 0 before transitioning to Software Standby or Deep Software Standby mode. To transition to Software Standby or Deep Software Standby mode, first set the OSTDE bit to 0, then execute the WFI instruction.

The following restrictions apply when using the oscillation stop detection function:
In low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD is prohibited.

8.2.18 OSTDSR : Oscillation Stop Detection Status Register

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	Oscillation Stop Detection Flag 0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. This bit can only be set to 0. This bit is cleared to 0 by writing 0 after reading it as 1.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When this flag is 1, it indicates that the main clock oscillation stop was detected. After this stop is detected, the OSTDF flag is not set to 0 even when the main clock oscillation is restarted. The OSTDF bit is cleared to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading it as 0. If the OSTDF flag is set to 0 when the main clock oscillation is stopped, the OSTDF flag becomes 0 then returns to 1.

The OSTDF flag cannot be set to 0 under the following conditions:

OSTDCR寄存器控制振荡停止检测功能。

OSTDIE位（振荡停止检测中断使能）

OSTDIE位使能振荡停止检测功能中断。它还控制是否将振荡停止检测报告给POEG。

如果振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志需要清零，则在清零OSTDF之前将OSTDIE位设置为0。在将OSTDIE位设置为1之前等待至少2个PCLKB周期。通过读取访问周期数由PCLKB定义的IO寄存器，可以确保2个或更多PCLKB周期的等待时间。

OSTDE位（振荡停止检测功能使能）

OSTDE位使能振荡停止检测功能。

当OSTDE位为1（使能）时，MOCO停止位（MOCOCR.MCSTP）设置为0，MOCO操作开始。
MOCO时钟在振荡停止检测功能启用时不能停止。将1写入
MOCOCR.MCSTP位（MOCO停止）无效。

当振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志为1（检测到主时钟振荡停止）时，向OSTDE位写入0无效。

在转换到软件待机或深度软件待机模式之前，必须将OSTDE位设置为0。过渡到
软件待机或深度软件待机模式，首先将OSTDE位设置为0，然后执行WFI指令。

使用振荡停止检测功能时有以下限制：
在低速模式下，禁止为ICLK、FCLK、BCLK、PCLKA、PCLKB、PCLKC和PCLKD选择1、2、4、8分频。

8.2.18 OSTDSR：振荡停止检测状态寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x041

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OSTDF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OSTDF	振荡停止检测标志 0：未检测到主时钟振荡停止1：检测到主时钟振荡停止	R/W*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.该位只能设置为0。读为1后写入0清除该位为0。

OSTDSR寄存器指示主时钟振荡器的停止检测状态。

OSTDF标志（振荡停止检测标志）

OSTDF标志指示主时钟振荡器状态。该标志为1时，表示检测到主时钟振荡停止。检测到此停止后，即使重新启动主时钟振荡，OSTDF标志也不会设置为0。OSTDF位在读为1后写入0清零。

从向OSTDF写入0到将其读取为0之间至少需要3个ICLK周期的等待时间。如果在主时钟振荡停止时将OSTDF标志设置为0，则OSTDF标志变为0然后返回1。

在以下情况下，OSTDF标志不能设置为0：

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC).
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (System clock source = PLL)

The OSTDF flag must be set to 0 after switching the clock source to sources other than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillator is stopped when OSTDCR.OSTDE = 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are neither 011b (system clock is MOSC) nor 101b (system clock is PLL) and PLLCCR.PLSRCSEL bit is not 0 (PLL source clock is MOSC).

8.2.19 MOSCWTCR : Main Clock Oscillator Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting 0x0: Wait time = 3 cycles (11.4 µs) 0x1: Wait time = 35 cycles (133.5 µs) 0x2: Wait time = 67 cycles (255.6 µs) 0x3: Wait time = 131 cycles (499.7 µs) 0x4: Wait time = 259 cycles (988.0 µs) 0x5: Wait time = 547 cycles (2086.6 µs) 0x6: Wait time = 1059 cycles (4039.8 µs) 0x7: Wait time = 2147 cycles (8190.2 µs) 0x8: Wait time = 4291 cycles (16368.9 µs) 0x9: Wait time = 8163 cycles (31139.4 µs) Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

The MSTS[3:0] bits specify the oscillation stabilization wait time for the main clock oscillator.

Set the main clock oscillation stabilization time to a period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0x0 because the oscillation stabilization time is not required.

The wait time set in these bits is counted using: 1 cycle (µs) = 1/(fLOCO[MHz] × 8) = 1/(0.032768 × 8) = 3.81 (µs) (min.) The LOCO clock automatically oscillates when necessary, regardless of the value of the LOCO.LCSTP bit. After the specified wait time elapses, supply of the main clock starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the specified wait time is short, supply of the main clock starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

●SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）。

●PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）

将时钟源切换到主时钟振荡器和PLL以外的源后，必须将OSTDF标志设置为0。

[Setting condition]

●当OSTDCR.OSTDE=1（振荡停止检测功能使能）时，主时钟振荡器停止。

[Clearing condition]

●当SCKSCR.CKSEL[2:0]位既不是011b（系统时钟为MOSC）也不是101b（系统时钟为PLL）且PLLCCR.PLSRCSEL位不为0（PLL源时钟为MOSC）。

8.2.19 MOSCWTCR:主时钟振荡器等待控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	MSTS[3:0]			
重置后的值:	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
3:0	MSTS[3:0]	主时钟振荡器等待时间设置 0x0：等待时间=3个周期(11.4µs)0x1：等待时间=35个周期(133.5µs)0x2：等待时间=67个周期(255.6µs)0x3：等待时间=131个周期(499.7µs)0x4：等待时间=259周期(988.0µs)0x5：等待时间=547个周期(2086.6µs)0x6：等待时间=1059个周期(4039.8µs)0x7：等待时间=2147个周期(8190.2µs)0x8：等待时间=4291个周期(16368.9µs)0x9:等待时间=8163个周期(31139.4µs) 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

MSTS[3:0]位（主时钟振荡器等待时间设置）

MSTS[3:0]位指定主时钟振荡器的振荡稳定等待时间。

将主时钟振荡稳定时间设置为大于或等于振荡器制造商推荐的稳定时间。当主时钟从外部输入时，将这些位设置为0x0，因为不需要振荡稳定时间。

这些位中设置的等待时间使用以下公式计算：1个周期(µs)=1(fLOCO[MHz]×8)=1(0.032768×8)=3.81(µs)(min.)
无论LOCO.LCSTP位的值如何，LOCO时钟都会在必要时自动振荡。经过指定的等待时间后，MCU内部开始提供主时钟，并将OSCSF.MOSCSF标志设置为1。如果指定的等待时间短，则在时钟振荡稳定之前开始提供主时钟.

仅当MOSCCR.MOSTP位为1且OSCSF.MOSCSF标志为0时才重写MOSCWTCR寄存器。在任何其他情况下请勿重写此寄存器。

RA生态工作室

8.2.20 MOMCR : Main Clock Oscillator Mode Oscillation Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	MODRV[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
5:4	MODRV[1:0]	Main Clock Oscillator Drive Capability 0 Switching 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz	R/W
6	MOSEL	Main Clock Oscillator Switching 0: Resonator 1: External clock input	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: The EXTAL/XTAL pins are also used as ports. In the initial state, the pin is set as a port.

Note: The MOSTP bit must be 1 (MOSC is stopped) before changing this register.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

MODRV[1:0] bit (Main Clock Oscillator Drive Capability 0 Switching)

The MODRV[1:0] bit switches the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

8.2.21 SOMCR : Sub-Clock Oscillator Mode Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x481

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SODRV	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	These bits are read as 0. The write value should be 0.	R/W
1	SODRV	Sub-Clock Oscillator Drive Capability Switching 0: Standard 1: Low	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

8.2.20 MOMCR：主时钟振荡器模式振荡控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x413

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MOSEL	MODRV[1:0]		—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
5:4	MODRV[1:0]	主时钟振荡器驱动能力0开关 0 0: 20 MHz to 24 MHz 0 1: 16 MHz to 20 MHz 1 0: 8 MHz to 16 MHz 1 1: 8 MHz	R/W
6	MOSEL	主时钟振荡器切换 0：谐振器1：外部时钟输入	R/W
7	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: EXTALXTAL引脚也用作端口。在初始状态下，该引脚被设置为一个端口。

Note: 在更改此寄存器之前，MOSTP位必须为1（MOSC停止）。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MODRV[1:0]位（主时钟振荡器驱动能力0切换）

MODRV[1:0]位切换主时钟振荡器的驱动能力。

MOSEL位（主时钟振荡器切换）

MOSEL位切换主时钟振荡器的源。

8.2.21 SOMCR：副时钟振荡器模式控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x481

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SODRV	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	这些位被读取为0。写入值应为0。	R/W
1	SODRV	副时钟振荡器驱动能力切换 0：标准1：低	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The SOMCR register must be modified when SOSCCR.SOSTP is 1 (SOSC is stopped).

SODRV bits (Sub-Clock Oscillator Drive Capability Switching)

The SODRV bits switch the drive capability of the sub-clock oscillator. SODRV is undefined at the first Power up, but value after reset of SOSCCR.SOSTP is 0 (SOSC is operated). And therefore, please set the SOSC as follows when the first Power up:

1. Set the SOSCCR.SOSTP to 1 (SOSC is stopped)
2. Set this bit to a value corresponding to the using capacitor.
3. Clear the SOSCCR.SOSTP to 0 (SOSC is operated)

8.2.22 CKOCR : Clock Out Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	Clock Out Source Select 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: MOSC 1 0 0: SOSC 1 0 1: Setting prohibited Others: Setting prohibited	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	CKODIV[2:0]	Clock Output Frequency Division Ratio 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W
7	CKOEN	Clock Out Enable 0: Disable clock out 1: Enable clock out	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits select the source of the clock to be output from the CLKOUT pin. When changing the clock source, set the CKOEN bit to 0.

CKODIV[2:0] bits (Clock Output Frequency Division Ratio)

The CKODIV[2:0] bits specify the clock division ratio. Set the CKOEN bit to 0 when changing the division ratio.

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

当SOSCCR.SOSTP为1（SOSC停止）时，必须修改SOMCR寄存器。

SODRV位（副时钟振荡器驱动能力切换）

SODRV位切换副时钟振荡器的驱动能力。首次上电时SODRV未定义，但SOSCCR.SOSTP复位后的值为0（SOSC运行）。因此，请在第一次上电时将SOSC设置如下：

1.将SOSCCR.SOSTP设置为1（SOSC停止）

2.将此位设置为与使用电容相对应的值。

3.清除SOSCCR.SOSTP为0（SOSC操作）

8.2.22 CKOCR：时钟输出控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKOSEL[2:0]	时钟输出源选择 000：HOCO001：MOC O010：LOCO011：MOS C100：SOSC101：禁止 设置 其他：禁止设置	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	CKODIV[2:0]	时钟输出分频比 0 0 0: × 1/1 0 0 1: × 1/2 0 1 0: × 1/4 0 1 1: × 1/8 1 0 0: × 1/16 1 0 1: × 1/32 1 1 0: × 1/64 1 1 1: × 1/128	R/W
7	CKOEN	时钟输出使能 0：禁用时钟输出1 ：启用时钟输出	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

CKOSEL[2:0]位（时钟输出源选择）

CKOSEL[2:0]位选择从CLKOUT引脚输出的时钟源。更改时钟源时，将CKOEN位设置为0。

CKODIV[2:0]位（时钟输出分频比）

CKODIV[2:0]位指定时钟分频比。更改分频比时将CKOEN位设置为0。

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CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

Clear this bit before entering Software Standby or Deep Software Standby mode if the selecting clock out source clock is stopped in that mode.

8.2.23 EBCKOCR : External Bus Clock Output Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x052

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EBCKOEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EBCKOEN	EBCLK Pin Output Control 0: EBCLK pin output is disabled (fixed high) 1: EBCLK pin output is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

8.2.24 LOCOUTCR : LOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

CKOEN位（时钟输出使能）

CKOEN位使能CLKOUT引脚的输出。

当该位设置为1时，输出选定的时钟。当该位设置为0时，输出低电平。更改此位时，请确认CKOSEL[2:0]位中选择的时钟输出源时钟稳定。否则，可能会在输出中产生故障。

如果选择时钟输出源时钟在该模式下停止，则在进入软件待机或深度软件待机模式之前清零该位。

8.2.23 EBCKOCR:外部总线时钟输出控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x052

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EBCKOEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EBCKOEN	EBCLK引脚输出控制 0：禁止EBCLK引脚输出（固定为高电平）1 ：使能EBCLK引脚输出。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

8.2.24 LOCOUTCR:LOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x492

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	LOCOUTRM[7:0]	LOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

The LOCOUTCR register is added to the original LOCO trimming data.

MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range. When LOCOUTCR is modified, the frequency stabilization time corresponds to the frequency stabilization time at the start of MCU operation. When the ratio of the LOCO frequency and the other oscillation frequency is an integer value, changing the LOCOUTCR value is prohibited.

Changing LOCOUTCR during RTC operation is prohibited.

8.2.25 MOCOUTCR : MOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The MOCOUTCR register is added to the original MOCO trimming data.

MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range. When MOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation. When the ratio of the MOCO frequency and the other oscillation frequency is an integer value, changing the MOCOUTCR value is prohibited.

8.2.26 HOCOUTCR : HOCO User Trimming Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

LOCOUTCR寄存器被添加到原始LOCO修整数据中。

当LOCOUTCR设置为导致LOCO频率超出规范范围的值时，MCU操作无法保证。修改LOCOUTCR时，频率稳定时间对应于MCU工作开始时的频率稳定时间。当LOCO频率与其他振荡频率之比为整数值时，禁止更改LOCOUTCR值。

禁止在RTC操作期间更改LOCOUTCR。

8.2.25 MOCOUTCR:MOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x061

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MOCOUTRM[7:0]	MOCO用户修整 0x80：-1280x81： -127 0xFF：-10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

MOCOUTCR寄存器被添加到原始MOCO修整数据中。

当MOCOUTCR设置为导致MOCO频率超出规格范围的值时，无法保证MCU操作。修改MOCOUTCR时，稳频等待时间对应MCU开始工作时的稳频等待时间。当MOCO频率与其他振荡频率之比为整数值时，禁止更改MOCOUTCR值。

8.2.26 HOCOUTCR:HOCO用户微调控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x062

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO User Trimming 0x80: -128 0x81: -127 ⋮ 0xFF: -1 0x00: Center Code 0x01: +1 ⋮ 0x7E: +126 0x7F: +127	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The HOCOUTCR register is added to the original HOCO trimming data.

MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range. When HOCOUTCR is modified, the frequency stabilization wait time corresponds to the frequency stabilization wait time at the start of the MCU operation.

These bits must be 0x00 when FLL is enabled (FLLCR1.FLLEN = 1).

8.2.27 USBCKDIVCR : USB Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	USBCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	USBCKDIV[2:0]	USB Clock (USBCLK) Division Select 0 1 0: /4 1 0 1: /3 1 1 0: /5 Others: Setting prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The USBCKDIVCR register controls the USB clock.

USBCKDIV[2:0] bits (USB Clock (USBCLK) Division Select)

These bits select the frequency of the USB clock (USBCLK) and must be modified when USBCKCR.USBCKSRDY = 1.

Bit	Symbol	Function	R/W
7:0	HOCOUTRM[7:0]	HOCO用户修整 0x80：−1280x81： −127 0xFF：−10x00 ：中心代码0x01：+ 1 0x7E：+1260x7F ：+127	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

HOCOUTCR寄存器被添加到原始HOCO修整数据中。

当HOCOUTCR设置为导致HOCO频率超出规范范围的值时，MCU操作无法保证。修改HOCOUTCR时，稳频等待时间对应MCU运行开始时的稳频等待时间。

当FLL使能时（FLLCR1.FLLEN=1），这些位必须为0x00。

8.2.27 USBCKDIVCR:USB时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	USBCKDIV[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	USBCKDIV[2:0]	USB时钟(USBCLK)分频选择 0 1 0: /4 1 0 1: /3 1 1 0: /5 其他：禁止设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

USBCKDIVCR寄存器控制USB时钟。

USBCKDIV[2:0]位（USB时钟(USBCLK)分频选择）

这些位选择USB时钟(USBCLK)的频率，并且必须在USBCKCR.USBCKSRDY=1时进行修改。

8.2.28 OCTACKDIVCR : Octal-SPI Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OCTACKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	OCTACKDIV[2:0]	Octal-SPI Clock (OCTACLK) Division Select 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 Others: Setting prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

OCTACKDIVCR controls the Octal-SPI clock.

OCTACKDIV[2:0] bits (Octal-SPI Clock (OCTACLK) Division Select)

These bits select the frequency of the Octal-SPI clock (OCTACLK) and must be modified when OCTACKCR.OCTACKSRDY = 1.

8.2.29 CANFDCKDIVCR : CANFD Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CANFDCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CANFDCKDIV[2:0]	CANFD clock (CANFDCLK) Division Select 0 0 0: 1 0 0 1: 2 0 1 0: 4 0 1 1: 6 Settings other than above are prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

8.2.28 OCTACKDIVCR:Octal-SPI时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OCTACKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	OCTACKDIV[2:0]	八进制SPI时钟(OCTACLK)分频选择 0 0 0: /1 (value after reset) 0 0 1: /2 0 1 0: /4 0 1 1: /6 1 0 0: /8 其他：禁止设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

OCTACKDIVCR控制八进制SPI时钟。

OCTACKDIV[2:0]位（八进制SPI时钟(OCTACLK)分频选择）

这些位选择八进制SPI时钟(OCTACLK)的频率，并且必须在OCTACKCR.OCTACKSRDY = 1.

8.2.29 CANFDCKDIVCR:CANFD时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CANFDCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CANFDCKDIV[2:0]	CANFD时钟(CANFDCLK)分频选择 0 0 0: 1 0 0 1: 2 0 1 0: 4 0 1 1: 6 禁止上述以外的设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

CANFDCKDIVCR controls the CANFD clock (CANFDCLK).

CANFDCKDIV[2:0] bit (CANFD clock (CANFDCLK) Division Select)

These bits select the frequency of the CANFD clock (CANFDCLK).

These bits must change when CANFDCKCR.CANFDCKSRDY = 1.

8.2.30 USB60CKDIVCR : USB60 Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x06F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	USB60CKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	USB60CKDIV[2:0]	USB clock (USB60CLK) Division Select 000: /1 (value after reset) 001: /2 010: /4 011: /6 100: /8 101: /3 110: /5 Settings other than above are prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

USB60CKDIVCR controls the USB clock (USB60CLK).

USB60CKDIV[2:0] bit (USB clock (USB60CLK) Division Select)

These bits select the frequency of the USB clock (USB60CLK).

These bits must change when USB60CKCR.USB60CKCRSRDY = 1.

8.2.31 CECCKDIVCR : CEC Clock Division Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x070

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CECCKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

CANFDCKDIVCR控制CANFD时钟(CANFDCLK)。

CANFDCKDIV[2:0]位（CANFD时钟(CANFDCLK)分频选择）

这些位选择CANFD时钟(CANFDCLK)的频率。

当CANFDCKCR.CANFDCKSRDY=1时，这些位必须改变。

8.2.30 USB60CKDIVCR:USB60时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x06F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	USB60CKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	USB60CKDIV[2:0]	USB时钟(USB60CLK)分频选择 000: /1 (value after reset) 001: /2 010: /4 011: /6 100: /8 101: /3 110: /5 禁止上述以外的设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

USB60CKDIVCR控制USB时钟(USB60CLK)。

USB60CKDIV[2:0]位（USB时钟(USB60CLK)分频选择）

这些位选择USB时钟(USB60CLK)的频率。

当USB60CKCR.USB60CKCRSRDY=1时，这些位必须改变。

8.2.31 CECCKDIVCR:CEC时钟分频控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x070

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CECCKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CECCKDIV[2:0]	CEC clock (CECCLK) Division Select 000: /1 (value after reset) 001: /2 010: /4 011: /6 100: /8 101: /3 110: /5 Settings other than above are prohibited.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.
CECCKDIVCR controls the CEC clock (CECCLK).

CECCKDIV[2:0] bit (CEC clock (CECCLK) Division Select)

These bits select the frequency of the CEC clock (CECCLK).

These bits must change when CECCKCR.CECCKSRDY = 1.

8.2.32 USBCKCR : USB Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x074

Bit position:	7	6	5	4	3	2	1	0
Bit field:	USBCKSRDY	USBCKSREQ	—	—	—	USBCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	USBCKSEL[2:0]	USB Clock (USBCLK) Source Select 1 0 1: PLL 1 1 0: PLL2 Others: Setting prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	USBCKSREQ	USB Clock (USBCLK) Switching Request 0: No request 1: Request switching.	R/W
7	USBCKSRDY	USB Clock (USBCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The USBCKCR register controls the USB clock.

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of USBCKDIVCR.USBCKDIV[2:0] and USBCKSEL[2:0], use the following procedure:

Bit	Symbol	Function	R/W
2:0	CECCKDIV[2:0]	CEC时钟(CECCLK)分频选择 000: /1 (value after reset) 001: /2 010: /4 011: /6 100: /8 101: /3 110: /5 禁止上述以外的设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。
CECCKDIVCR控制CEC时钟(CECCLK)。

CECCKDIV[2:0]位（CEC时钟(CECCLK)分频选择）

这些位选择CEC时钟(CECCLK)的频率。

当CECCKCR.CECCKSRDY=1时，这些位必须改变。

8.2.32 USBCKCR:USB时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x074

Bit position:	7	6	5	4	3	2	1	0
Bit field:	USBCKSRDY	USBCKSREQ	—	—	—	USBCKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	USBCKSEL[2:0]	USB时钟(USBCLK)源选择 1 0 1: PLL 1 1 0: PLL2 其他：禁止设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	USBCKSREQ	USB时钟(USBCLK)切换请求 0：无请求1：请求切换。	R/W
7	USBCKSRDY	USB时钟(USBCLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

USBCKCR寄存器控制USB时钟。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改USBCKDIVCR.USBCKDIV[2:0]和USBCKSEL[2:0]的设置值，请使用以下过程：

1. Write 1 to USBCKSREQ.
2. Poll until USBCKSRDY is read as 1. While USBCKSRDY = 1, no clock is output to USBCLK.
3. Write to USBCKDIVCR.USBCKDIV[2:0] and USBCKSEL[2:0].
4. Write 0 to USBCKSREQ.
5. Poll until USBCKSRDY is read as 0.
6. When USBCKSRDY becomes 0, USBCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when USBCKSREQ = 1 and USBCKSRDY = 0, or when USBCKSREQ = 0 and USBCKSRDY = 1.

USBCKSEL[2:0] bits (USB Clock (USBCLK) Source Select)

These bits select the clock source of the USB clock (USBCLK) and must be modified when USBCKCR.USBCKSRDY = 1.

USBCKSREQ bit (USB Clock (USBCLK) Switching Request)

This bit selects the USBCLK switching request.

USBCKSRDY flag (USB Clock (USBCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the USBCLK. When USBCKSRDY = 1, no clock is output to USBCLK.

8.2.33 OCTACKCR : Octal-SPI Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x075

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OCTACKSRDY	OCTACKSREQ	—	—	—	OCTACKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	OCTACKSEL[2:0]	Octal-SPI Clock (OCTACLK) Source Select 0 0 0: HOCO 0 0 1: MOCO (value after reset) 0 1 0: LOCO 0 1 1: Main clock oscillator 1 0 0: Sub-clock oscillator 1 0 1: PLL 1 1 0: PLL2 Others: Setting prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	OCTACKSREQ	Octal-SPI Clock (OCTACLK) Switching Request 0: No request 1: Request switching.	R/W
7	OCTACKSRDY	Octal-SPI Clock (OCTACLK) Switching Ready state flag 0: Switching not possible 1: Switching possible.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The OCTACKCR register controls the Octal-SPI clock.

1.将1写入USBCKSREQ。

2.轮询直到USBCKSRDY被读取为1。当USBCKSRDY=1时，没有时钟输出到USBCLK。

3.写入USBCKDIVCR.USBCKDIV[2:0]和USBCKSEL[2:0]。

4.将0写入USBCKSREQ。

5.轮询直到USBCKSRDY被读取为0。

6.当USBCKSRDY变为0时，USBCLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即USBCKSREQ=1且USBCKSRDY=0时，或USBCKSREQ=0且USBCKSRDY=1时不执行WFI指令。

USBCKSEL[2:0]位（USB时钟(USBCLK)源选择）

这些位选择USB时钟(USBCLK)的时钟源，并且必须在USBCKCR.USBCKSRDY=1时进行修改。

USBCKSREQ位（USB时钟(USBCLK)切换请求）

该位选择USBCLK切换请求。

USBCKSRDY标志（USB时钟(USBCLK)切换就绪状态标志）

该标志指示USBCLK的切换就绪状态。当USBCKSRDY=1时，没有时钟输出到USBCLK。

8.2.33 OCTACKCR:八进制SPI时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x075

Bit position:	7	6	5	4	3	2	1	0
Bit field:	OCTACKSRDY	OCTACKSREQ	—	—	—	OCTACKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	OCTACKSEL[2:0]	八路SPI时钟(OCTACLK)源选择 000：HOCO001：MOCO（复位后的值）010：LOCO011：主时钟振荡器100：副时钟振荡器101：PLL110：PLL2 其他：禁止设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	OCTACKSREQ	八路SPI时钟(OCTACLK)切换请求 0：无请求1：请求切换。	R/W
7	OCTACKSRDY	八进制SPI时钟(OCTACLK)切换就绪状态标志 0：不能切换1：可以切换。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

OCTACKCR寄存器控制八进制SPI时钟。

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output.

To change the set value of OCTACKDIVCR.OCTACKDIV[2:0] and OCTACKSEL[2:0], use the following procedure:

1. Write 1 to OCTACKSREQ.
2. Poll until OCTACKSRDY is read as 1. While OCTACKSRDY = 1, no clock is output to OCTACLK.
3. Write to OCTACKDIVCR.OCTACKDIV[2:0] and OCTACKSEL[2:0].
4. Write 0 to OCTACKSREQ.
5. Poll until OCTACKSRDY is read as 0.
6. When OCTACKSRDY becomes 0, OCTACLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when OCTACKSREQ = 1 and OCTACKSRDY = 0, or when OCTACKSREQ = 0 and OCTACKSRDY = 1.

OCTACKSEL[2:0] bits (Octal-SPI Clock (OCTACLK) Source Select)

These bits select the clock source of the Octal-SPI clock (OCTACLK) and must be modified when OCTACKCR.OCTACKSRDY = 1.

OCTACKSREQ bit (Octal-SPI Clock (OCTACLK) Switching Request)

This bit selects the OCTACLK switching request.

OCTACKSRDY flag (Octal-SPI Clock (OCTACLK) Switching Ready state flag)

This flag indicates the state of switching ready for the OCTACLK. When OCTACKSRDY = 1, no clock is output to OCTACLK.

8.2.34 CANFDCKCR : CANFD Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CANFDCKSRDY	CANFDCKSREQ	—	—	—	CANFDCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CANFDCKSEL[2:0]	CANFD clock (CANFDCLK) Source Select 1 0 1: PLL 1 1 0: PLL2 Settings other than above are prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	CANFDCKSREQ	CANFD clock (CANFDCLK) Switching Request 0: No request 1: Request switching	R/W
7	CANFDCKSRDY	CANFD clock (CANFDCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。

要更改OCTACKDIVCR.OCTACKDIV[2:0]和OCTACKSEL[2:0]的设置值，请使用以下过程：

1.将1写入OCTACKSREQ。

2.轮询直到OCTACKSRDY被读取为1。当OCTACKSRDY=1时，没有时钟输出到OCTACLK。

3.写入OCTACKDIVCR.OCTACKDIV[2:0]和OCTACKSEL[2:0]。

4.将0写入OCTACKSREQ。

5.轮询直到OCTACKSRDY被读取为0。

6.当OCTACKSRDY变为0时，OCTACLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即，当OCTACKSREQ=1且OCTACKSRDY=0或OCTACKSREQ=0且OCTACKSRDY=1时，不执行WFI指令。

OCTACKSEL[2:0]位（八进制SPI时钟(OCTACLK)源选择）

这些位选择八进制SPI时钟(OCTACLK)的时钟源，并且必须在OCTACKCR.OCTACKSRDY = 1.

OCTACKSREQ位（八进制SPI时钟(OCTACLK)切换请求）

该位选择OCTACLK切换请求。

OCTACKSRDY标志（八进制SPI时钟(OCTACLK)切换就绪状态标志）

该标志指示OCTACLK的切换就绪状态。当OCTACKSRDY=1时，没有时钟输出到OCTACLK.

8.2.34 CANFDCKCR:CANFD时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CANFDCKSRDY	CANFDCKSREQ	—	—	—	CANFDCKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CANFDCKSEL[2:0]	CANFD时钟(CANFDCLK)源选择 1 0 1: PLL 1 1 0: PLL2 禁止上述以外的设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	CANFDCKSREQ	CANFD时钟(CANFDCLK)切换请求 0：无请求1：请求切换	R/W
7	CANFDCKSRDY	CANFD时钟(CANFDCLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The CANFDCKCR register controls the CANFD clock (CANFDCLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of CANFDCKDIVCR.CANFDCKDIV[2:0] and CANFDCKSEL[2:0], use the following procedure:

1. Write 1 to CANFDCKSREQ.
2. Poll until CANFDCKSRDY is read as 1. While CANFDCKSRDY = 1, no clock is output to CANFDCLK.
3. Write to CANFDCKDIVCR.CANFDCKDIV[2:0] and CANFDCKSEL[2:0].
4. Write 0 to CANFDCKSREQ.
5. Poll until CANFDCKSRDY is read as 0.
6. When CANFDCKSRDY becomes 0, CANFDCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when CANFDCKSREQ = 1 and CANFDCKSRDY = 0, or when CANFDCKSREQ = 0 and CANFDCKSRDY = 1.

CANFDCKSEL[2:0] bits (CANFD clock (CANFDCLK) Source Select)

These bits select the clock source of the CANFD clock (CANFDCLK) and must be modified when CANFDCKCR.CANFDCKSRDY = 1.

CANFDCKSREQ bit (CANFD clock (CANFDCLK) Switching Request)

This bit selects the CANFDCLK switching request.

CANFDCKSRDY flag (CANFD clock (CANFDCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the CANFDCLK. When CANFDCKSRDY = 1, no clock is output to CANFDCLK.

8.2.35 USB60CKCR : USB60 Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x077

Bit position:	7	6	5	4	3	2	1	0
Bit field:	USB60CKSRDY	USB60CKSREQ	—	—	—	USB60CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	USB60CKSEL[2:0]	USB clock (USB60CLK) Source Select 101: PLL 110: PLL2 Settings other than above are prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	USB60CKSREQ	USB clock (USB60CLK) Switching Request 0: No request 1: Request switching	R/W
7	USB60CKSRDY	USB clock (USB60CLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

CANFDCKCR寄存器控制CANFD时钟(CANFDCLK)。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改CANFDCKDIVCR.CANFDCKDIV[2:0]和CANFDCKSEL[2:0]的设置值，请使用以下过程：

1.将1写入CANFDCKSREQ。

2.轮询直到CANFDCKSRDY被读取为1。当CANFDCKSRDY=1时，没有时钟输出到CANFDCLK。

3.写入CANFDCKDIVCR.CANFDCKDIV[2:0]和CANFDCKSEL[2:0]。

4.将0写入CANFDCKSREQ。

5.轮询直到CANFDCKSRDY被读取为0。

6.当CANFDCKSRDY变为0时，CANFDCLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即CANFDCKSREQ=1且CANFDCKSRDY=0时，或CANFDCKSREQ=0且CANFDCKSRDY=1时不执行WFI指令。

CANFDCKSEL[2:0]位（CANFD时钟(CANFDCLK)源选择）

这些位选择CANFD时钟(CANFDCLK)的时钟源，并且必须在CANFDCKCR.CANFDCKSRDY = 1.

CANFDCKSREQ位（CANFD时钟(CANFDCLK)切换请求）

该位选择CANFDCLK切换请求。

CANFDCKSRDY标志（CANFD时钟(CANFDCLK)切换就绪状态标志）

该标志指示CANFDCLK的切换就绪状态。当CANFDCKSRDY=1时，没有时钟输出到CANFDCLK.

8.2.35 USB60CKCR:USB60时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x077

Bit position:	7	6	5	4	3	2	1	0
Bit field:	USB60CKSRDY	USB60CKSREQ	—	—	—	USB60CKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	USB60CKSEL[2:0]	USB时钟(USB60CLK)源选择 101: PLL 110: PLL2 禁止上述以外的设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	USB60CKSREQ	USB时钟(USB60CLK)切换请求 0：无请求1：请求切换	R/W
7	USB60CKSRDY	USB时钟(USB60CLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The USB60CKCR register controls the USB clock (USB60CLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of USB60CKDIVCR.USB60CKDIV[2:0] and USB60CKSEL[2:0], use the following procedure:

1. Write 1 to USB60CKSREQ.
2. Poll until USB60CKSRDY is read as 1. While USB60CKSRDY = 1, no clock is output to USB60CLK.
3. Write to USB60CKDIVCR.USB60CKDIV[2:0] and USB60CKSEL[2:0].
4. Write 0 to USB60CKSREQ.
5. Poll until USB60CKSRDY is read as 0.
6. When USB60CKSRDY becomes 0, USB60CLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when USB60CKSREQ = 1 and USB60CKSRDY = 0, or when USB60CKSREQ = 0 and USB60CKSRDY = 1.

USB60CKSEL[2:0] bits (USB clock (USB60CLK) Source Select)

These bits select the clock source of the USB clock (USB60CLK) and must be modified when USB60CKCR.USB60CKSRDY = 1.

USB60CKSREQ bit (USB clock (USB60CLK) Switching Request)

This bit selects the USB60CLK switching request.

USB60CKSRDY flag (USB clock (USB60CLK) Switching Ready state flag)

This flag indicates the state of switching ready for the USB60CLK. When USB60CKSRDY = 1, no clock is output to USB60CLK.

8.2.36 CECCKCR : CEC Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CECCKSRDY	CECCKSREQ	—	—	—	CECCKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CECCKSEL[2:0]	CEC clock (CECCLK) Source Select 011: Main clock oscillator 100: Sub-clock oscillator Settings other than above are prohibited.	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	CECCKSREQ	CEC clock (CECCLK) Switching Request 0: No request 1: Request switching	R/W
7	CECCKSRDY	CEC clock (CECCLK) Switching Ready state flag 0: Impossible to Switch 1: Possible to Switch	R

Note: If the security attribution is configured as secure:

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

USB60CKCR寄存器控制USB时钟(USB60CLK)。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改USB60CKDIVCR.USB60CKDIV[2:0]和USB60CKSEL[2:0]的设置值，请使用以下步骤：

1.将1写入USB60CKSREQ。

2.轮询直到USB60CKSRDY被读取为1。当USB60CKSRDY=1时，没有时钟输出到USB60CLK。

3.写入USB60CKDIVCR.USB60CKDIV[2:0]和USB60CKSEL[2:0]。

4.将0写入USB60CKSREQ。

5.轮询直到USB60CKSRDY被读取为0。

6.当USB60CKSRDY变为0时，USB60CLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即当USB60CKSREQ=1且USB60CKSRDY=0时，或USB60CKSREQ=0且USB60CKSRDY=1时不执行WFI指令。

USB60CKSEL[2:0]位（USB时钟(USB60CLK)源选择）

这些位选择USB时钟(USB60CLK)的时钟源，并且必须在USB60CKCR.USB60CKSRDY = 1.

USB60CKSREQ位（USB时钟(USB60CLK)切换请求）

该位选择USB60CLK切换请求。

USB60CKSRDY标志（USB时钟(USB60CLK)切换就绪状态标志）

该标志指示USB60CLK的切换就绪状态。当USB60CKSRDY=1时，没有时钟输出到USB60CLK.

8.2.36 CECCKCR:CEC时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x076

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CECCKSRDY	CECCKSREQ	—	—	—	CECCKSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
2:0	CECCKSEL[2:0]	CEC时钟(CECCLK)源选择 011：主时钟振荡器100：副时钟振荡器 禁止上述以外的设置。	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	CECCKSREQ	CEC时钟(CECCLK)切换请求 0：无请求1：请求切换	R/W
7	CECCKSRDY	CEC时钟(CECCLK)切换就绪状态标志 0：不能切换1：可以切换	R

Note: 如果安全属性配置为安全：

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The CECCKCR register controls the CEC clock (CECCLK).

When switching the clock source, ensure that the clock before the switch and the clock after the switch generate stable output. To change the set value of CECCKDIVCR.CECCKDIV[2:0] and CECCKSEL[2:0], use the following procedure:

1. Write 1 to CECCKSREQ.
2. Poll until CECCKSRDY is read as 1. While CECCKSRDY = 1, no clock is output to CECCLK.
3. Write to CECCKDIVCR.CECCKDIV[2:0] and CECCKSEL[2:0].
4. Write 0 to CECCKSREQ.
5. Poll until CECCKSRDY is read as 0.
6. When CECCKSRDY becomes 0, CECCLK starts to output. Clock switching is complete.

When transitioning to Software Standby or Deep Software Standby mode, do not execute the WFI instruction while performing clock switching. That is, do not execute the WFI instruction when CECCKSREQ = 1 and CECCKSRDY = 0, or when CECCKSREQ = 0 and CECCKSRDY = 1.

CECCKSEL[2:0] bits (CEC clock (CECCLK) Source Select)

These bits select the clock source of the CEC clock (CECCLK) and must be modified when CECCKCR.CECCKSRDY = 1.

CECCKSREQ bit (CEC clock (CECCLK) Switching Request)

This bit selects the CECCLK switching request.

CECCKSRDY flag (CEC clock (CECCLK) Switching Ready state flag)

This flag indicates the state of switching ready for the CECCLK. When CECCKSRDY = 1, no clock is output to CECCLK.

8.2.37 TRCKCR : Trace Clock Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x03F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TRCKEN	—	—	—	TRCK[3:0]			
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
3:0	TRCK[3:0]	Trace Clock operating frequency select 0x0: /1 0x1: /2 (value after reset) 0x2: /4 Others: Setting prohibited	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	TRCKEN	Trace Clock operating Enable 0: Stop 1: Operation enable	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Trace Clock Control Register controls switching the trace clock.

TRCKCR can be written only when the debugger is connected (DBGSTR.CDBGPWRUPREQ = 1).

- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

CECCKCR寄存器控制CEC时钟(CECCLK)。

切换时钟源时，确保切换前的时钟和切换后的时钟产生稳定的输出。要更改CECCKDIVCR.CECCKDIV[2:0]和CECCKSEL[2:0]的设置值，请使用以下过程：

1.将1写入CECCKSREQ。

2.轮询直到CECCKSRDY被读取为1。当CECCKSRDY=1时，没有时钟输出到CECCLK。

3.写入CECCKDIVCR.CECCKDIV[2:0]和CECCKSEL[2:0]。

4.将0写入CECCKSREQ。

5.轮询直到CECCKSRDY被读取为0。

6.当CECCKSRDY变为0时，CECCLK开始输出。时钟切换完成。

当转换到软件待机或深度软件待机模式时，不要在执行时钟切换时执行WFI指令。即，当CECCKSREQ=1且CECCKSRDY=0时，或者当CECCKSREQ=0且CECCKSRDY=1时，不执行WFI指令。

CECCKSEL[2:0]位（CEC时钟(CECCLK)源选择）

这些位选择CEC时钟(CECCLK)的时钟源，并且必须在CECCKCR.CECCKSRDY=1时进行修改。

CECCKSREQ位（CEC时钟(CECCLK)切换请求）

该位选择CECCLK切换请求。

CECCKSRDY标志（CEC时钟(CECCLK)切换就绪状态标志）

该标志指示CECCLK的切换就绪状态。当CECCKSRDY=1时，没有时钟输出到CECCLK。

8.2.37 TRCKCR：跟踪时钟控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x03F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TRCKEN	—	—	—	TRCK[3:0]			
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
3:0	TRCK[3:0]	跟踪时钟工作频率选择 0x0: /1 0x1: /2 (value after reset) 0x2: /4 其他：禁止设置	R/W
6:4	—	这些位被读取为0。写入值应为0。	R/W
7	TRCKEN	跟踪时钟操作使能 0：停止1：运行使能	R/W

Note: 在重写此寄存器之前将PRCR.PRC0位设置为1（允许写入）。

跟踪时钟控制寄存器控制跟踪时钟的切换。

TRCKCR只能在调试器连接时写入(DBGSTR.CDBGPWRUPREQ=1)。

Change the TRCLK frequency in the state of TRCKEN = 0.

Factor of the initialization of TRCKCR register is all resets.

8.3 Main Clock Oscillator

To supply the clock signal to the main clock oscillator, use one of the following ways:

- Connect an oscillator
- Connect the input of an external clock signal.

8.3.1 Connecting a Crystal Resonator

Figure 8.4 shows an example of connecting a crystal resonator. A damping resistor (Rd) can be added, if required.

Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 8.1.

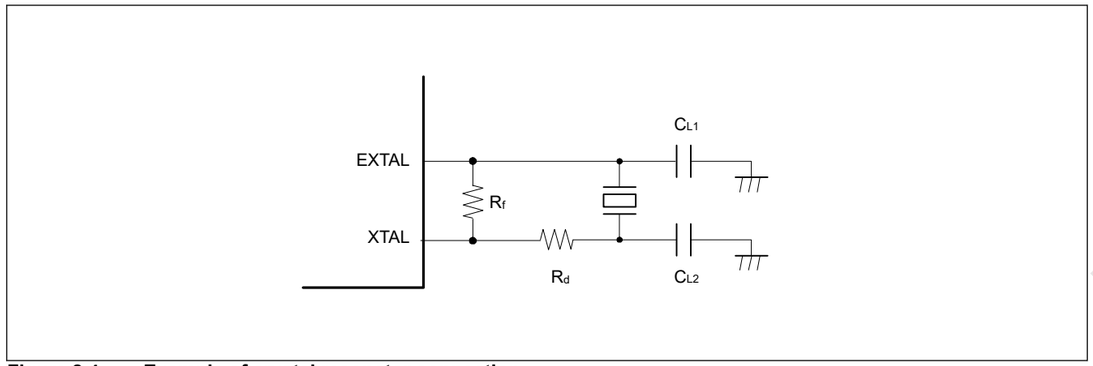

Figure 8.4 Example of crystal resonator connection

Figure 8.5 shows an equivalent circuit of the crystal resonator.

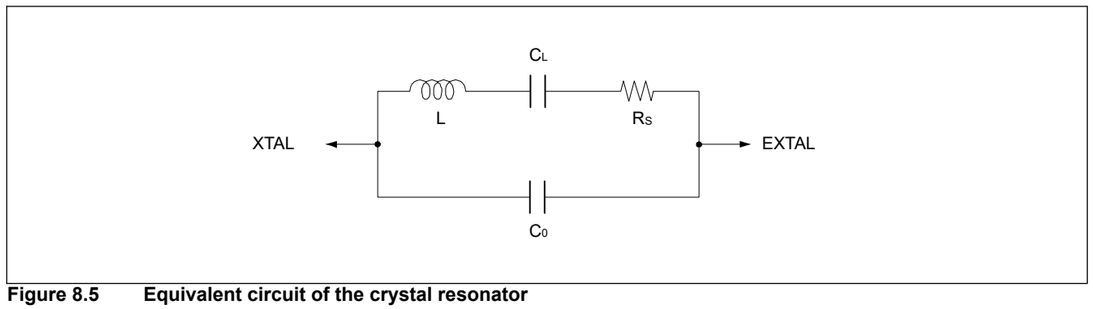

Figure 8.5 Equivalent circuit of the crystal resonator

8.3.2 External Clock Input

Figure 8.6 shows an example of connecting an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin becomes high impedance.

在TRCKEN=0的状态下改变TRCLK频率。

TRCKCR寄存器初始化的因素是所有的复位。

8.3 主时钟振荡器

要将时钟信号提供给主时钟振荡器，请使用以下方法之一：

●连接振荡器

●连接外部时钟信号的输入。

8.3.1 连接晶体谐振器

图8.4显示了连接晶体谐振器的示例。如果需要，可以添加一个阻尼电阻器(Rd)。

由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器(Rf)，请按照说明在EXTAL和XTAL之间插入一个Rf。

连接谐振器以提供时钟时，谐振器的频率必须在表8.1中所述的主时钟振荡器的谐振器频率范围内。

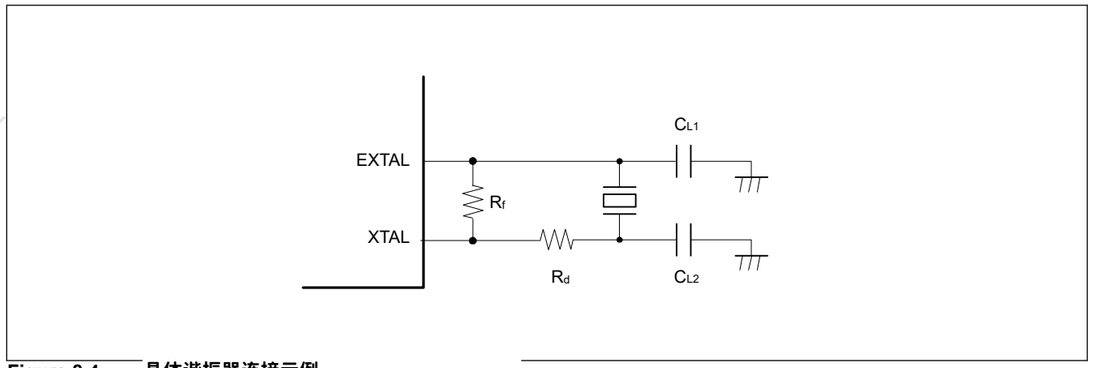

Figure 8.4 晶体谐振器连接示例

图8.5显示了晶体谐振器的等效电路。

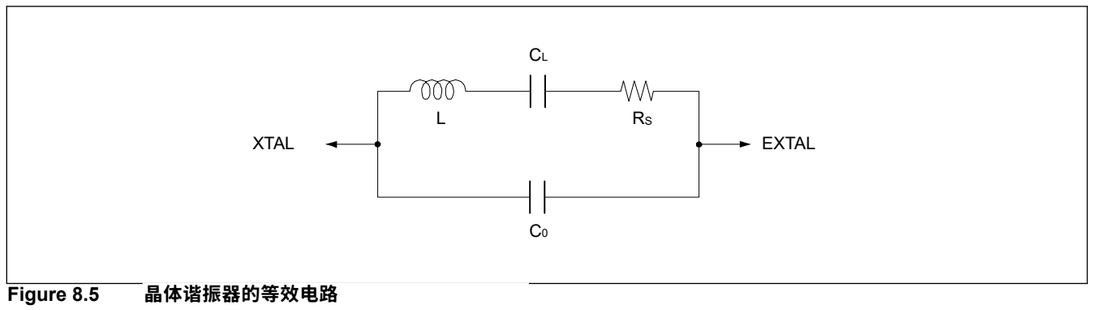

Figure 8.5 晶体谐振器的等效电路

8.3.2 外部时钟输入

图8.6显示了连接外部时钟输入的示例。要使用外部时钟信号操作振荡器，请将MOMCR.MOSEL位设置为1。XTAL引脚变为高阻抗。

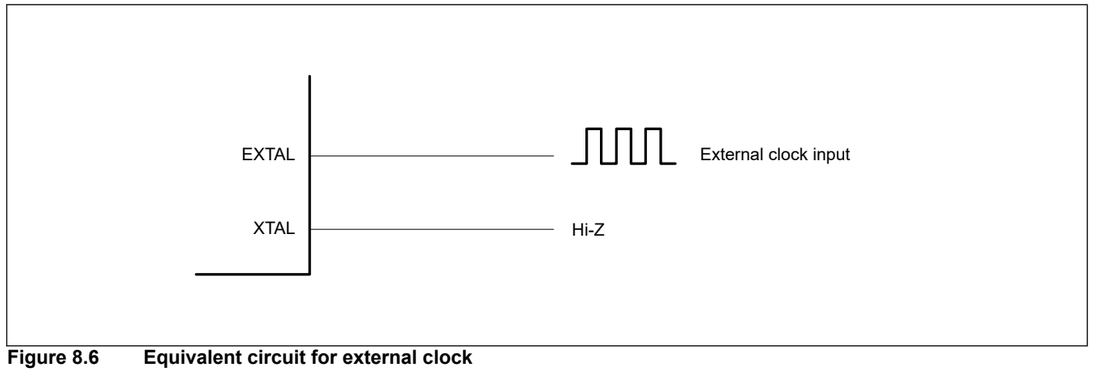

Figure 8.6 Equivalent circuit for external clock

8.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed when the main clock oscillator is stopped. Do not change the frequency of the external clock input when the setting of the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is 0.

8.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

8.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator as shown in Figure 8.7. A damping resistor (Rd) can be added, if necessary. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the resonator manufacturer recommends the use of an external feedback resistor (Rf), insert an Rf between XCIN and XCOUT by following the instructions. When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 8.1.

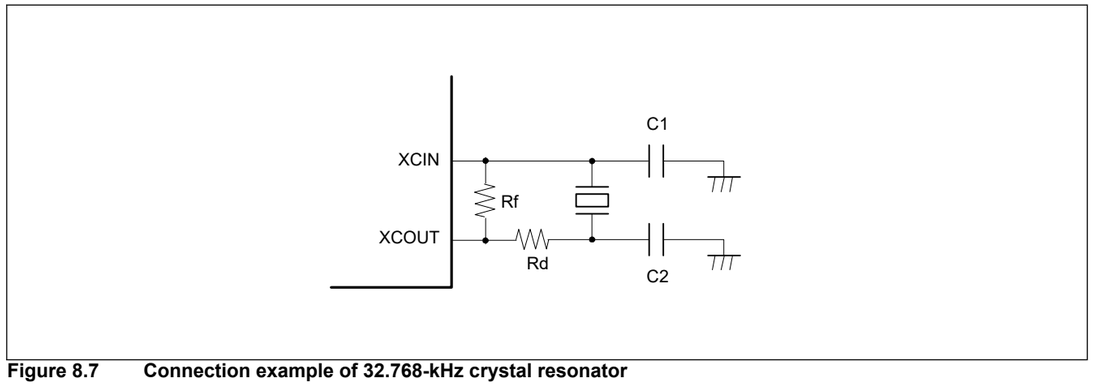

Figure 8.7 Connection example of 32.768-kHz crystal resonator

Figure 8.8 shows an equivalent circuit for the 32.768-kHz crystal resonator.

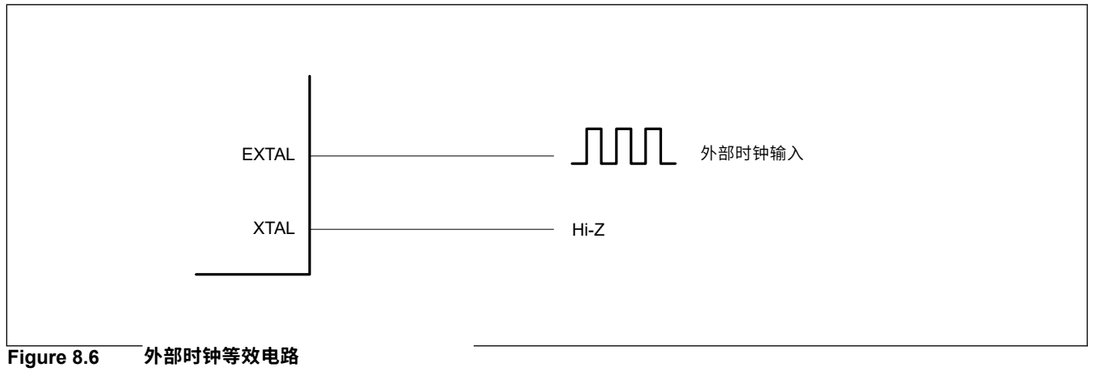

Figure 8.6 外部时钟等效电路

8.3.3 外部时钟输入注意事项

外部时钟输入的频率只有在主时钟振荡器停止时才能改变。当主时钟振荡器停止位(MOSCCR.MOSTP)设置为0时，请勿更改外部时钟输入的频率。

8.4 Sub-Clock Oscillator

向副时钟振荡器提供时钟信号的唯一方法是连接晶体振荡器。

8.4.1 连接32.768kHz晶体谐振器

要为副时钟振荡器提供时钟，请连接一个32.768-kHz晶体谐振器，如图8.7所示。如有必要，可以添加阻尼电阻器(Rd)。由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果谐振器制造商建议使用外部反馈电阻器(Rf)，请按照说明在XCIN和XCOUT之间插入一个Rf。连接谐振器以提供时钟时，谐振器的频率必须在表8.1中所述的副时钟振荡器的谐振器频率范围内。

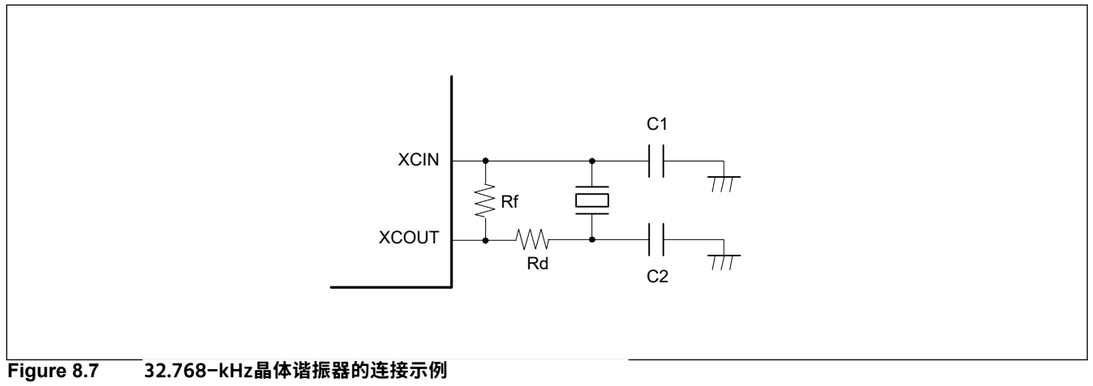

Figure 8.7 32.768-kHz晶体谐振器的连接示例

图8.8显示了32.768kHz晶体谐振器的等效电路。

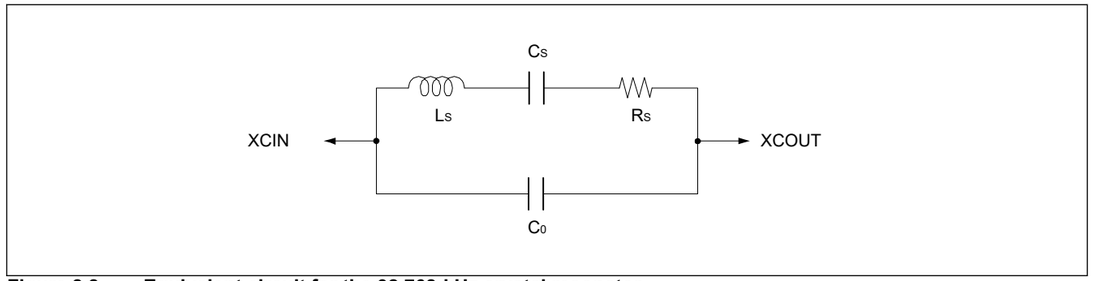

Figure 8.8 Equivalent circuit for the 32.768-kHz crystal resonator

8.4.2 Pin Handling When the Sub-Clock Oscillator Is Not Used

When the sub-clock oscillator is not in use, connect the XCIN pin to VSS through a resistor (to pull VSS down) and leave the XCOUT pin open as shown in Figure 8.9. In addition, if an oscillator is not connected, set the Sub-Clock Oscillator Stop bit (SOSCCR.SOSTP) to 1 to stop the oscillator.

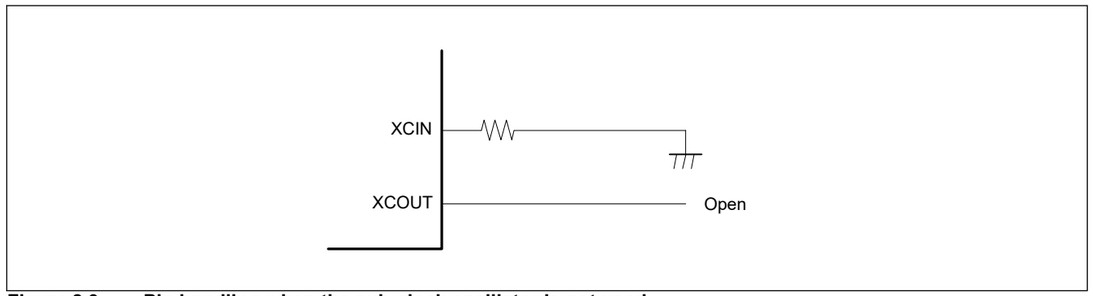

Figure 8.9 Pin handling when the sub-clock oscillator is not used

8.5 Oscillation Stop Detection Function

8.5.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop. When oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock.
- If an oscillation stop is detected with PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL), PLL clock remains the system clock source. However, the frequency becomes a free-running oscillation frequency.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 53, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock or between the PLL clock and PLL free-running clock is controlled by the Oscillation Stop Detection Flag (OSTDSR.OSTDF).

OSTDF controls the switched clock as follows:

- When SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  - When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock.
  - When OSTDF changes from 1 to 0, the clock source switches back to MOSC.

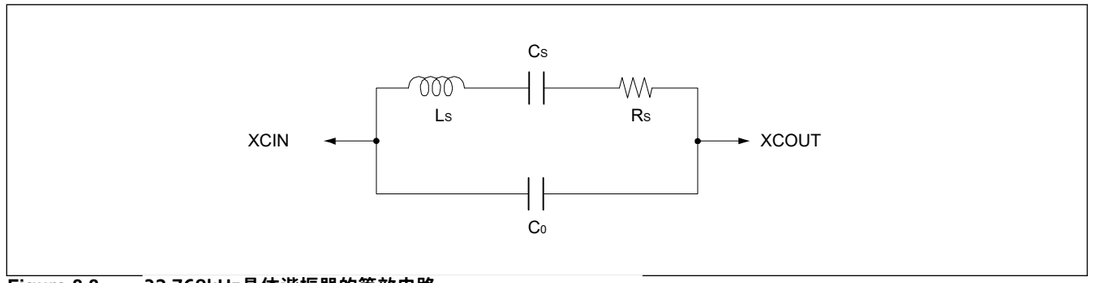

Figure 8.8 32.768kHz晶体谐振器的等效电路

8.4.2 不使用副时钟振荡器时的引脚处理

不使用副时钟振荡器时，通过一个电阻将XCIN引脚连接到VSS（将VSS下拉）并使XCOUT引脚保持开路，如图8.9所示。此外，如果未连接振荡器，请将副时钟振荡器停止位(SOSCCR.SOSTP)设置为1以停止振荡器。

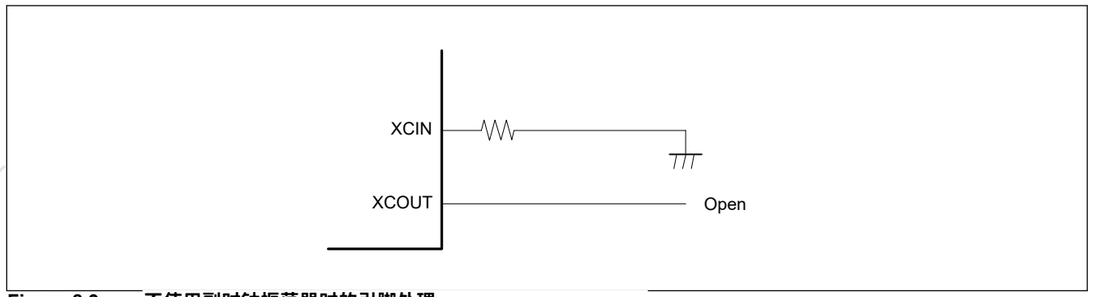

Figure 8.9 不使用副时钟振荡器时的引脚处理

8.5 振荡停止检测功能

8.5.1 振荡停止检测和检测后操作

振荡停止检测功能检测主时钟振荡器停止。当检测到振荡停止时，系统时钟切换如下：

●如果通过SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）检测到振荡停止，则系统时钟源切换到MOCO时钟。

●如果在PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）的情况下检测到振荡停止并且SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL），PLL时钟仍然是系统时钟源。然而，该频率变为自由运行的振荡频率。

当检测到振荡停止时，可以产生一个振荡停止检测中断请求。此外，一般PWM定时器(GPT)输出可在检测时强制为高阻抗状态。

当输入时钟保持在0或1一段时间，例如，当主时钟振荡器发生故障时，检测到主时钟振荡停止。参见第53节，电气特性。

主时钟振荡器和MOCO时钟之间或PLL时钟和PLL自由运行时钟之间的切换由振荡停止检测标志(OSTDSR.OSTDF)控制。

OSTDF控制切换时钟如下：

●当SCKSCR.CKSEL[2:0]=011b时（系统时钟源=MOSC）：

当OSTDF从0变为1时，时钟源切换到MOCO时钟。

当OSTDF从1变为0时，时钟源切换回MOSC。

- When PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (System clock source = PLL):
  - When OSTDF changes 0 to 1, the clock source switches to the PLL free-running oscillation clock.
  - When OSTDF changes 1 to 0, the clock source switches back to PLL.

To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock is stopped by an external cause. Therefore, the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or a transition is made to Software Standby or Deep Software Standby mode.

The oscillation stop detection function switches all clocks that can be selected as the MOSC clock except CLKOUT to the MOCO (when system clock is MOSC) or PLL free-running (when system clock is PLL).

The system clock (ICLK) frequency during the MOCO(when system clock is MOSC) or PLL free-running (when system clock is PLL) operation is specified by the MOCO oscillation frequency and the division ratio set by the system clock select bits (SCKDIVCR.ICK[2:0])

●当PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）且SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）时：

当OSTDF由0变为1时，时钟源切换到PLL自由运行振荡时钟。

当OSTDF由1变为0时，时钟源切换回PLL。

要在检测到振荡停止后再次将时钟源切换为主时钟或PLL时钟，请将CKSEL[2:0]位设置为主时钟或PLL时钟以外的时钟源，并将OSTDF标志清零。另外，检查OSTDF标志不为1，然后在指定的振荡稳定时间过去后将CKSEL[2:0]位设置为主时钟或PLL时钟。

复位释放后，主时钟振荡器停止，振荡停止检测功能被禁用。要启用振荡停止检测功能，激活主时钟振荡器并在经过指定的振荡稳定时间后将1写入振荡停止检测功能使能位(OSTDCR.OSTDE)。

振荡停止检测功能检测主时钟何时因外部原因停止。因此，必须在软件停止主时钟振荡器或转换到软件待机或深度软件待机模式之前禁用振荡停止检测功能。

振荡停止检测功能将除CLKOUT之外的所有可选择作为MOSC时钟的时钟切换到
MOCO（系统时钟为MOSC时）或PLL自由运行（系统时钟为PLL时）。

MOCO（系统时钟为MOSC时）或PLL自由运行（系统时钟为PLL时）操作期间的系统时钟（ICLK）频率由MOCO振荡频率和系统时钟选择位（SCKDIVCR）设置的分频比指定.ICK[2:0])

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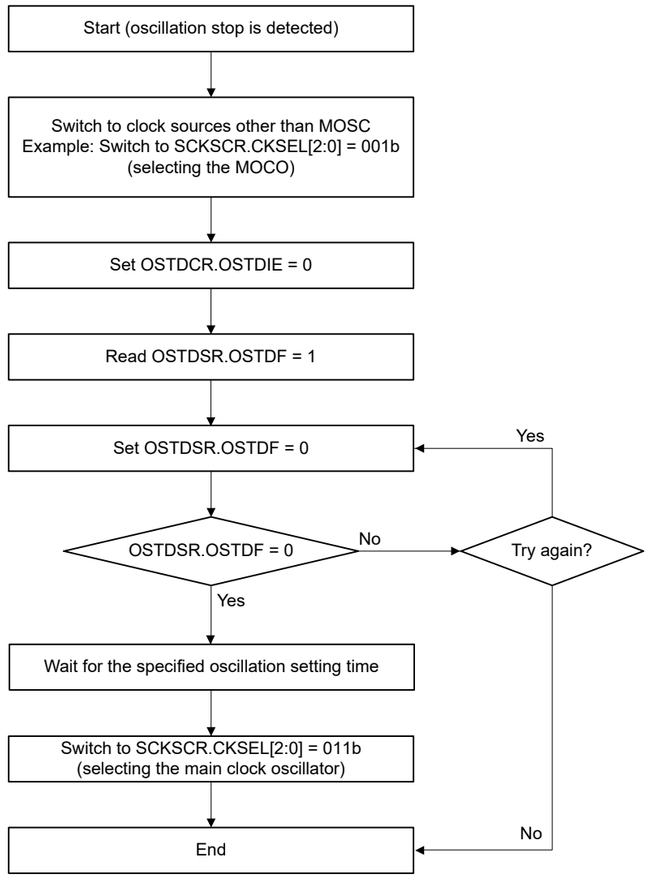
Example of returning when CKSEL[2:0] = 011b (selecting the main clock oscillator) after an oscillation stop is detected



Note: On return from the oscillation-stopped state, the factor responsible for stopping the main clock oscillation circuit must be removed from the system to allow oscillation to resume.

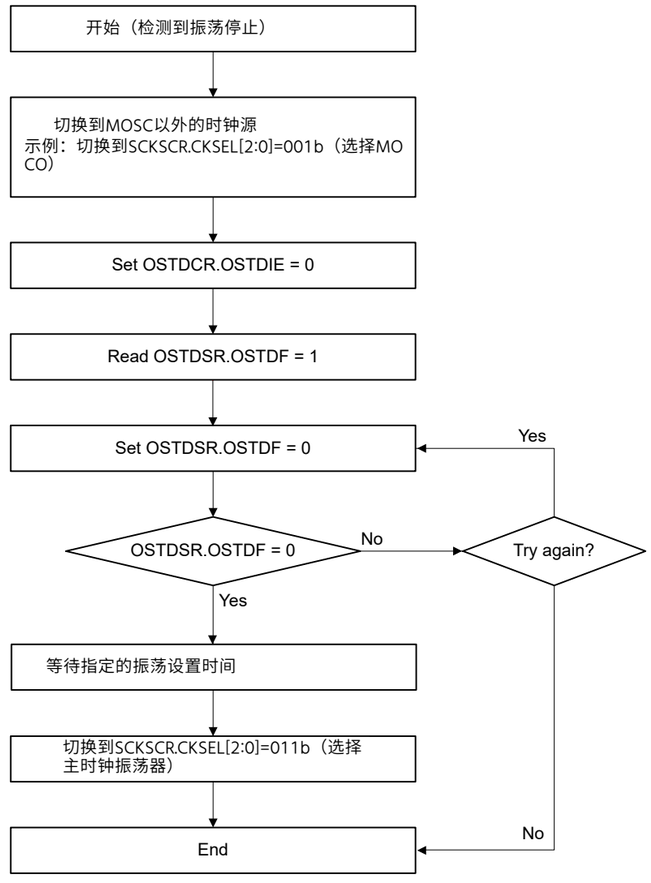
Figure 8.10 Flow of recovery on detection of oscillator stop

8.5.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the Oscillation Stop Detection Flag (OSTDSR.OSTDF) is 1 and the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B, C, D).

After the oscillation stop is detected, wait at least 10 PCLKB clock cycles before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the Oscillation Stop Detection Interrupt Enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait at least 2 PCLKB clock cycles before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

检测到振荡停止后CKSEL[2:0]=011b（选择主时钟振荡器）时返回的示例



Note: 在从振荡停止状态返回时，必须从系统中移除负责停止主时钟振荡电路的因素以允许振荡恢复。

Figure 8.10 检测到振荡器停止时的恢复流程

8.5.2 振荡停止检测中断

当振荡停止检测标志(OSTDSR.OSTDF)为1且振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位为1（使能）时，将产生一个振荡停止检测中断(MOSC_STOP)。GPT端口输出使能(POEG)被通知主时钟振荡器停止。收到通知后，POEG将POEG组n设置寄存器(POEGGn.OSTPF)中的振荡停止检测标志设置为1(n=A B C D)。

检测到振荡停止后，至少等待10个PCLKB时钟周期，然后再写入POEGGn.OSTPF标志。
当需要清除OSTDSR.OSTDF标志时，请在清除振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位后执行此操作。至少等待2个PCLKB时钟周期，然后再将OSTDCR.OSTDIE位设置为1。可能需要更长的PCLKB等待时间，具体取决于读取给定IO寄存器所需的周期数。

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable non-maskable interrupts through software before using oscillation stop detection interrupts. For details, see section 13, Interrupt Controller Unit (ICU).

8.6 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

8.7 Internal Clock

Clock sources for the internal clock signals include:

- Main clock
- Sub-clock
- HOCO clock
- MOCO clock
- LOCO clock
- PLL clock
- PLL2 clock
- IWDT-dedicated clock
- JTAG clock

The following internal clocks are produced from these sources.

- Operating clock of the CPU, DMAC, DTC, Flash, and RAM: System clock (ICLK)
- Operating clocks of peripheral modules: Peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD)
- Operating clock of the FlashIF: FlashIF clock (FCLK)
- Clock for the external bus controller and external pin output: External bus clock (BCLK)
- Operating clock for the USBFS and USBHS clock (USBCLK)
- Operating clock for the USBHS-PHY: USBHS-PHY clock (USBMCLK)
- Operating clock for the USBHS : USB clock (USB60CLK)
- Operating clock for the Octal-SPI: Octal-SPI clock (OCTACLK)
- Operating clock for the CANFD: CANFD clock (CANFDCLK)
- Operating clock for the CAN: CAN clock (CANMCLK)
- Operating clocks for the CEC: CEC clock (CECCLK)
- Operating clocks for the CAC: CAC clock (CACCLK)
- Operating clock for the RTC: RTC-dedicated LOCO clock (RTCLCLK)
- Operating clock for the RTC: RTC-dedicated sub clock (RTCSCLK)
- Operating clock for the IWDT: IWDT-dedicated clock (IWDTCLK)
- Operating clock for the AGT: AGT-dedicated LOCO clock (AGTLCLK)
- Operating clock for the AGT: AGT-dedicated sub clock (AGTSCLK)
- Operating clock for the Systick Timer: Systick Timer-dedicated clock (SYSTICCLK)
- Clock for external pin output: Clock/Buzzer output clock(CLKOUT)
- Operating clock for the JTAG: JTAG clock (JTAGTCK)

For details on the registers used to set the frequencies of the internal clocks, see section 8.7.1. System Clock (ICLK) to section 8.7.18. JTAG Clock (JTAGTCK)

If the value of any of these bits is changed, subsequent operation is at the frequency determined by the new value.

振荡停止检测中断是一个不可屏蔽的中断。由于不可屏蔽中断在复位释放后的初始状态下被禁用，因此在使用振荡停止检测中断之前，请通过软件启用不可屏蔽中断。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

8.6 PLL Circuit

PLL电路具有倍增振荡器频率的功能。

8.7 内部时钟

内部时钟信号的时钟源包括：

●主时钟

- Sub-clock
- HOCO clock
- MOCO clock

●LOCO时钟

- PLL clock
- PLL2 clock
- IWDT-dedicated clock
- JTAG clock

以下内部时钟由这些源产生。

●CPU、DMAC、DTC、Flash、RAM的工作时钟：系统时钟（ICLK）
●外设模块工作时钟：外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）
●FlashIF的工作时钟：FlashIF时钟（FCLK）
●外部总线控制器和外部引脚输出的时钟：外部总线时钟（BCLK）
●USBFS和USBHS时钟(USBCLK)的工作时钟
●USBHS-PHY的工作时钟：USBHS-PHY时钟（USBMCLK）
●USBHS的工作时钟：USB时钟(USB60CLK)
●Octal-SPI的工作时钟：Octal-SPI时钟(OCTACLK)
●CANFD的工作时钟：CANFD时钟(CANFDCLK)
●CAN的工作时钟：CAN时钟(CANMCLK)
●CEC的工作时钟：CEC时钟(CECCLK)
●CAC的工作时钟：CAC时钟(CACCLK)
●RTC的工作时钟：RTC专用的LOCO时钟(RTCLCLK)
●RTC的工作时钟：RTC专用子时钟(RTCSCLK)
●IWDT的工作时钟：IWDT专用时钟（IWDTCLK）
●AGT的工作时钟：AGT专用的LOCO时钟(AGTLCLK)
●AGT的工作时钟：AGT专用子时钟(AGTSCLK)
●SystickTimer的工作时钟：SystickTimer专用时钟(SYSTICCLK)
●外部引脚输出时钟：时钟蜂鸣器输出时钟（CLKOUT）
●JTAG的工作时钟：JTAG时钟（JTAGTCK）

有关用于设置内部时钟频率的寄存器的详细信息，请参见第8.7.1节。系统时钟(ICLK)参见第8.7.18节。JTAG时钟(JTAGTCK)

如果这些位中的任何一个的值发生变化，则后续操作将以新值确定的频率进行。

8.7.1 System Clock (ICLK)

The system clock (ICLK) is the operating clock of the CPU, DMAC, DTC, Flash, and SRAM.

The ICLK frequency is specified by the ICK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ0[1:0] bits in OFS1.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 8.11 and Figure 8.12.

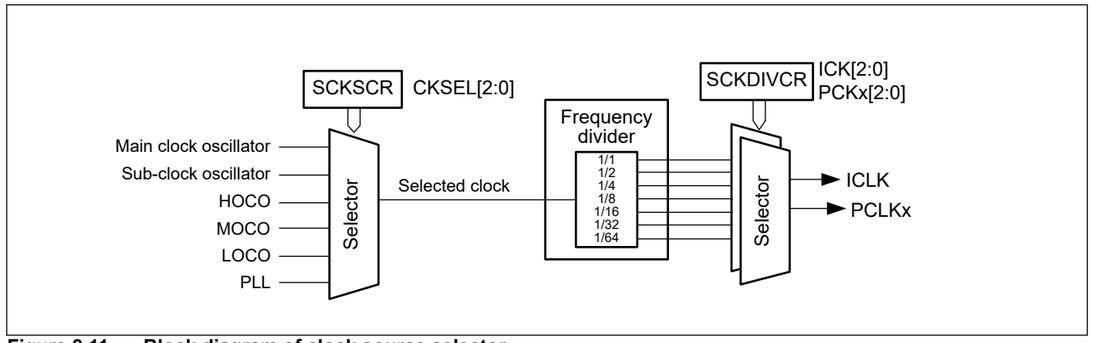


Figure 8.11 Block diagram of clock source selector

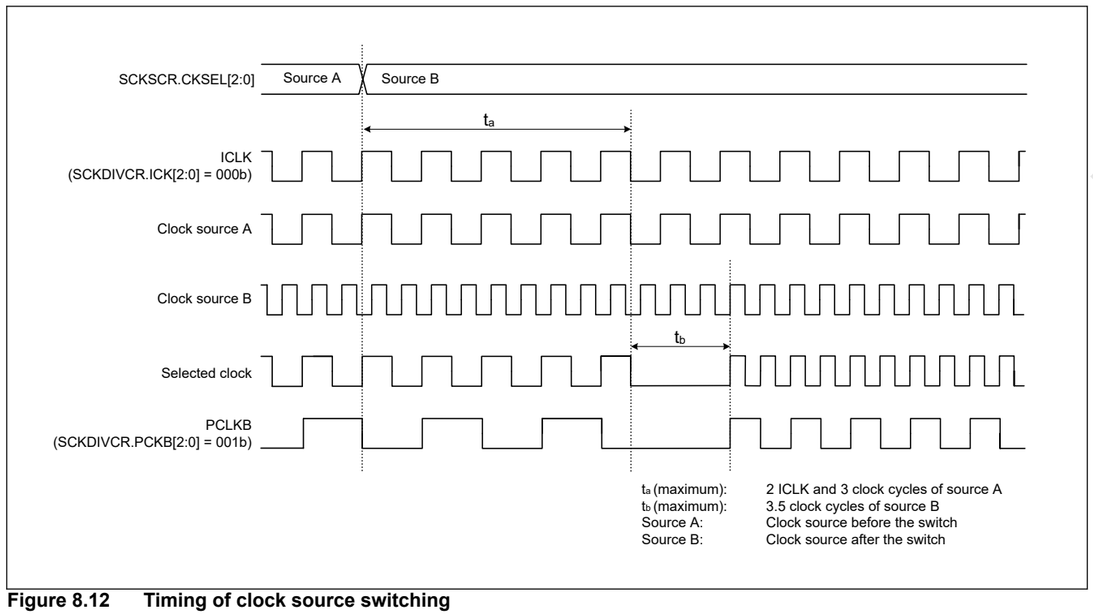


Figure 8.12 Timing of clock source switching

8.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

The peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD) are the operating clocks for the peripheral modules.

The frequency of the given clock is specified in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

8.7.1 系统时钟(ICLK)

系统时钟(ICLK)是CPU、DMAC、DTC、Flash和SRAM的工作时钟。

ICLK频率由SCKDIVCR中的ICK[2:0]位、SCKSCR中的CKSEL[2:0]位、PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位以及HOCOFRQ0指定OFS1中的[1:0]位。

当ICLK时钟源切换时，ICLK时钟周期的持续时间在时钟源转换期间变长。请参见图8.11和图8.12。

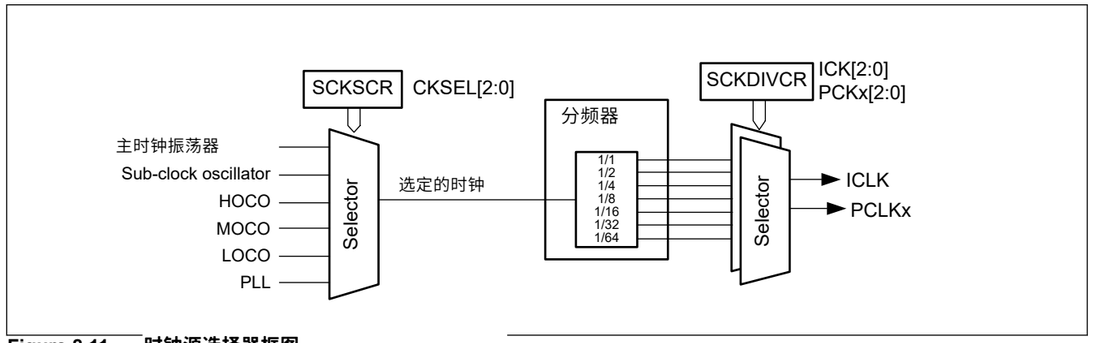


Figure 8.11 时钟源选择器框图

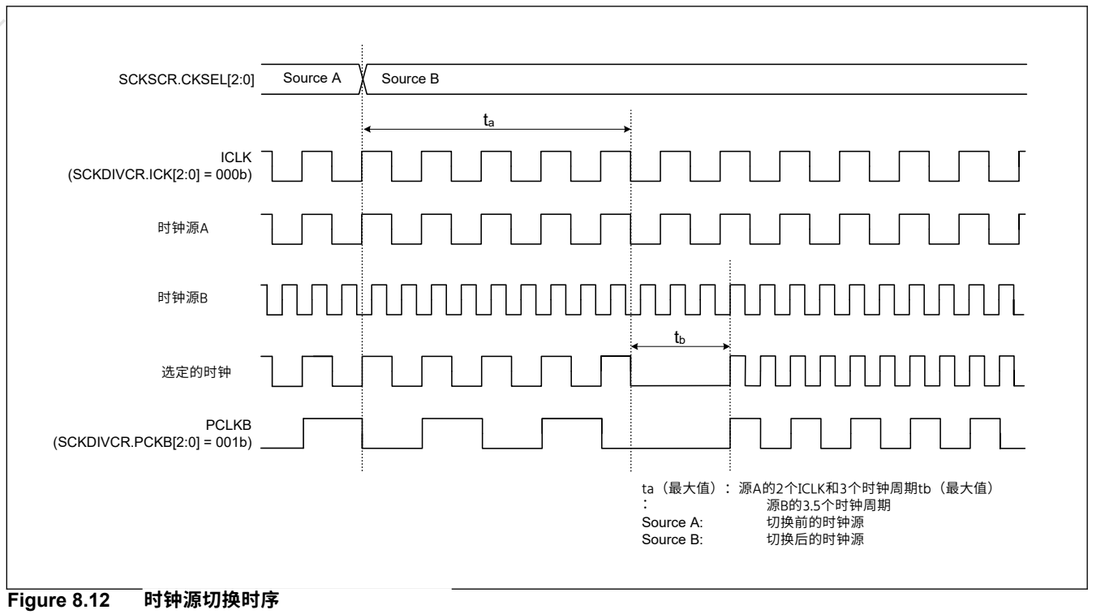


Figure 8.12 时钟源切换时序

8.7.2 外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）

外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）是外围模块的工作时钟。

给定时钟的频率在以下位中指定：

- SCKDIVCR中的PCKA[2:0]、PCKB[2:0]、PCKC[2:0]、PCKD[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 8.11 and Figure 8.12.

8.7.3 FlashIF Clock (FCLK)

The flash interface clock (FCLK) is the operating clock for the flash memory interface. In addition to reading from the data flash, FCLK is used for the programming and erasure of the code flash and data flash.

The FCLK frequency is specified in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

8.7.4 External Bus Clock (BCLK)

The external bus clock (BCLK) is an operating clock for the external bus controller. It is also output externally from the BCLK pin for the external connection bus.

BCLK can be output from the BCLK pin by setting the EBCKOCR.EBCKOEN bit to 1 and setting the PmnPFS.PSEL[4:0] to 01011b. Make sure that modification of the PmnPFS.PSEL[4:0] to 01011b must always be performed while the EBCKOCR.EBCKOEN bit is 0.

When the BCKCR.BCLKDIV bit is set to 1, the BCLK clock divided by 2 is output from the BCLK pin.

The BCLK frequency is specified by the BCK[2:0] bits in SCKDIVCR, the CKSEL[2:0] bits in SCKSCR, and the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR, and the HOCOFRQ[1:0] bits in OFS1.

A frequency higher than the system clock (ICLK) should not be set for the BCLK.

8.7.5 USB Clock (USBCLK)

The USB clock (USBCLK) is the operating clock for the USBFS and USBHS module.

A 48-MHz clock must be supplied to the USB module. When the USB module is used, setting must be made so that USBCLK is 48 MHz.

The USBCLK frequency is specified in the following bits:

- USBCKSEL[2:0] bits in USBCKCR
- USBCKDIV[2:0] bits in USBCKDIVCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- PLL2MUL[5:0] and PL2IDIV[1:0] bits in PLL2CCR.

8.7.6 USB-PHY Clock (USBMCLK)

The USB-PHY clock (USBMCLK) is the operating clock for the USBHS-PHY.

The USBMCLK frequency is 12 MHz or 20 MHz or 24 MHz supplied from the main clock oscillator.

8.7.7 USB Clock (USB60CLK)

The USB clock (USB60CLK) is the operating clock for the USBHS module.

A 60-MHz clock must be supplied to the USB module. When the USB module is used, setting must be made so that USB60CLK is 60 MHz.

The USB60CLK frequency is specified in the following bits:

- USB60CKSEL[2:0] bits in USB60CKCR
- USB60CKDIV[2:0] bits in USB60CKDIVCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR

当外围模块时钟的时钟源切换时，外围模块时钟周期的持续时间在时钟源转换期间会变长。请参见图8.11和图8.12。

8.7.3 FlashIF Clock (FCLK)

闪存接口时钟(FCLK)是闪存接口的工作时钟。除了从数据闪存读取外，FCLK还用于代码闪存和数据闪存的编程和擦除。

FCLK频率在以下位中指定：

- SCKDIVCR中的FCK[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

8.7.4 外部总线时钟(BCLK)

外部总线时钟(BCLK)是外部总线控制器的工作时钟。它也从外部输出BCLK引脚用于外部连接总线。

通过将EBCKOCR.EBCKOEN位设置为1并将PmnPFS.PSEL[4:0]设置为01011b，可以从BCLK引脚输出BCLK。确保必须始终在EBCKOCR.EBCKOEN位为0时将PmnPFS.PSEL[4:0]修改为01011b。

当BCKCR.BCLKDIV位设置为1时，从BCLK引脚输出除以2的BCLK时钟。

BCLK频率由SCKDIVCR中的BCK[2:0]位、SCKSCR中的CKSEL[2:0]位和PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位，以及OFS1中的HOCOFRQ[1:0]位。

不应为BCLK设置高于系统时钟(ICLK)的频率。

8.7.5 USB时钟(USBCLK)

USB时钟(USBCLK)是USBFS和USBHS模块的工作时钟。

必须为USB模块提供48-MHz时钟。使用USB模块时，必须进行设置，以便USBCLK is 48 MHz.

USBCLK频率在以下位中指定：

- USBCKCR中的USBCKSEL[2:0]位
- USBCKDIVCR中的USBCKDIV[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位。

8.7.6 USB-PHY Clock (USBMCLK)

USB-PHY时钟(USBMCLK)是USBHS-PHY的工作时钟。

USBMCLK频率为12MHz或20MHz或24MHz，由主时钟振荡器提供。

8.7.7 USB时钟(USB60CLK)

USB时钟(USB60CLK)是USBHS模块的工作时钟。

必须为USB模块提供60MHz时钟。使用USB模块时，必须进行设置，以便USB60CLK is 60 MHz.

USB60CLK频率在以下位中指定：

- USB60CKCR中的USB60CKSEL[2:0]位
- USB60CKDIVCR中的USB60CKDIV[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位

- PLL2MUL[5:0] and PL2IDIV[1:0] bits in PLL2CCR.

8.7.8 Octal-SPI clock (OCTACLK)

The Octal-SPI clock (OCTACLK) is the operating clock for the Octal-SPI module.

The OCTACLK frequency is specified by the OCTACKSEL[2:0] bits in OCTACKCR, the OCTACKDIV[2:0] bits in OCTACKDIVCR, the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR, the PLL2MUL[5:0], and PL2IDIV[1:0] bits in PLL2CCR.

8.7.9 CAN Clock (CANMCLK)

The CAN clock, CANMCLK, is the operating clock for the CAN module. CANMCLK is generated by the main clock oscillator.

8.7.10 CANFD clock (CANFDCLK)

The CANFD clock (CANFDCLK) is the operating clock for the CANFD module.

The CANFDCLK frequency is specified in the following bits:

- CANFDCKSEL[2:0] bits in CANFDCKCR
- CANFDCKDIV[2:0] bits in CANFDCKDIVCR
- PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR
- PLL2MUL[5:0], and PL2IDIV[1:0] bits in PLL2CCR.

8.7.11 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC. CACCLK is generated by the following oscillators:

- Main clock oscillator
- Sub-clock oscillator
- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

8.7.12 CEC clock (CECCLK)

The CEC clock (CECCLK) is the operating clock for the CEC module.

CECCLK is generated by the the main clock oscillator and sub clock oscillator.

8.7.13 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

The RTC-dedicated clock (RTCSCLK, RTCLCLK) is the operating clock for the RTC.

RTCSCLK is generated by the sub-clock oscillator, and RTCLCLK is generated by the LOCO clock.

8.7.14 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock (IWDTCLK) is the operating clock for the IWDT. IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

8.7.15 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clocks (AGTSCLK and AGTLCLK) are the operating clocks for the AGT. AGTSCLK is generated by the sub-clock oscillator, and AGTLCLK is generated by the LOCO clock.

●PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位。

8.7.8 Octal-SPI clock (OCTACLK)

Octal-SPI时钟(OCTACLK)是Octal-SPI模块的工作时钟。

OCTACLK频率由OCTACKCR中的OCTACKSEL[2:0]位、OCTACKDIV[2:0]位指定
PLLCCR中的OCTACKDIVCR、PLLMUL[5:0]和PLIDIV[1:0]位、PLL2MUL[5:0]和PL2IDIV[1:0]位
PLL2CCR.

8.7.9 CAN时钟(CANMCLK)

CAN时钟CANMCLK是CAN模块的工作时钟。CANMCLK由主时钟振荡器产生。

8.7.10 CANFD clock (CANFDCLK)

CANFD时钟(CANFDCLK)是CANFD模块的工作时钟。

CANFDCLK频率在以下位中指定：

●CANFDCKCR中的CANFDCKSEL[2:0]位
●CANFDCKDIVCR中的CANFDCKDIV[2:0]位
●PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
●PLL2CCR中的PLL2MUL[5:0]和PL2IDIV[1:0]位。

8.7.11 CAC时钟(CACCLK)

CAC时钟CACCLK是CAC的工作时钟。CACCLK由以下振荡器产生：

●主时钟振荡器
- Sub-clock oscillator
●高速时钟振荡器（HOCO）
●中速时钟振荡器（MOCO）
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator. (IWDTLOCO)

8.7.12 CEC clock (CECCLK)

CEC时钟(CECCLK)是CEC模块的工作时钟。

CECCLK由主时钟振荡器和副时钟振荡器产生。

8.7.13 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

RTC专用时钟（RTCSCLK、RTCLCLK）是RTC的工作时钟。

RTCSCLK由副时钟振荡器产生，RTCLCLK由LOCO时钟产生。

8.7.14 IWDT-Dedicated Clock (IWDTCLK)

IWDT专用时钟(IWDTCLK)是IWDT的工作时钟。IWDTCLK由内部产生
IWDT-dedicated on-chip oscillator.

8.7.15 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

AGT专用时钟（AGTSCLK和AGTLCLK）是AGT的工作时钟。AGTSCLK由副时钟振荡器产生，AGTLCLK由LOCO时钟产生。

8.7.16 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SYSTICCLK. SYSTICCLK is generated by the LOCO clock.

8.7.17 External Pin Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. Only change the value in the CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0.

The CLKOUT clock frequency is specified in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] in CKOCR
- HOCOFRQ0[1:0] bit in OFS1

8.7.18 JTAG Clock (JTAGTCK)

The JTAG clock (JTAGTCK) is the clock for the JTAG.

JTAGTCK is generated by the JTAG external clock (TCK).

8.8 Usage Notes

8.8.1 Notes on Clock Generation Circuit

The frequency of the following clocks supplied to each module changes according to the setting of the SCKDIVCR register:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- FlashIF clock (FCLK)
- external bus clock (BCLK)

Each frequency must meet the following conditions:

- Each frequency must be selected within the operation-guaranteed range of the operating frequency (f) specified in the AC characteristics. See section 53, Electrical Characteristics.
- The system clock, peripheral module clock must be set according to Table 8.2.
- Do not change the clock frequency during external bus access. Furthermore, when access via the external bus is to start after a change to the clock frequency, only start access via the bus after confirming that the change to the frequencies has been completed.

To ensure correct processing after the clock frequency changes, first write to the relevant Clock Control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

8.8.2 Notes on Resonator

Because various resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 8.7. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

8.8.3 Notes on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 8.13 to prevent electromagnetic induction from interfering with correct oscillation. Figure 8.13 shows the case which the main clock oscillator is used. In case of sub-clock oscillator, it is also same as Figure 8.13.

8.7.16 SysTick Timer-Dedicated Clock (SYSTICCLK)

SysTick定时器专用时钟SYSTICCLK是SYSTICCLK的工作时钟。SYSTICCLK由LOCO时钟生成。

8.7.17 外部引脚输出时钟(CLKOUT)

CLKOUT从CLKOUT引脚外部输出，用于时钟或蜂鸣器输出。CLKOUT被输出到CKOCR.CKOEN设置为1时的CLKOUT引脚。仅更改CKODIV[2:0]或CKOSEL[2:0]位中的值CKOCR.CKOEN位为0时的CKOCR。

CLKOUT时钟频率在以下位中指定：

●CKOCR中的CKODIV[2:0]或CKOSEL[2:0]

●OFS1中的HOCOFRQ0[1:0]位

8.7.18 JTAG Clock (JTAGTCK)

JTAG时钟(JTAGTCK)是JTAG的时钟。

JTAGTCK由JTAG外部时钟(TCK)生成。

8.8 使用说明

8.8.1 时钟产生电路注意事项

提供给每个模块的以下时钟的频率根据SCKDIVCR寄存器的设置而变化：

●系统时钟（ICLK）

●外设模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）

●FlashIF clock (FCLK)

●外部总线时钟（BCLK）

每个频率必须满足以下条件：

●各频率必须在交流特性规定的工作频率(f)的工作保证范围内选择。参见第53节，电气特性。

●系统时钟、外围模块时钟必须按照表8.2设置。

●在外部总线访问期间不要改变时钟频率。另外，在时钟频率变更后开始经由外部总线访问的情况下，仅在确认频率变更完成后才开始经由总线访问。

为保证时钟频率变化后的正确处理，首先写入相关的ClockControl寄存器改变频率，然后从寄存器中读取值，最后进行后续处理。

8.8.2 谐振器注意事项

由于各种谐振器特性与您的电路板设计密切相关，因此在使用前需要进行充分评估。请参见图8.7中的谐振器连接示例。谐振器的电路常数取决于要使用的谐振器和安装电路的杂散电容。因此，在确定电路常数时，请咨询谐振器制造商。施加在谐振器引脚之间的电压必须在绝对最大额定值范围内。

8.8.3 电路板设计注意事项

使用晶体谐振器时，将谐振器及其负载电容尽可能靠近XTAL和EXTAL引脚。其他信号线应远离振荡电路，如图8.13所示，以防止电磁感应干扰正确的振荡。图8.13显示了使用主时钟振荡器的情况。如果是副时钟振荡器，也与图8.13相同。

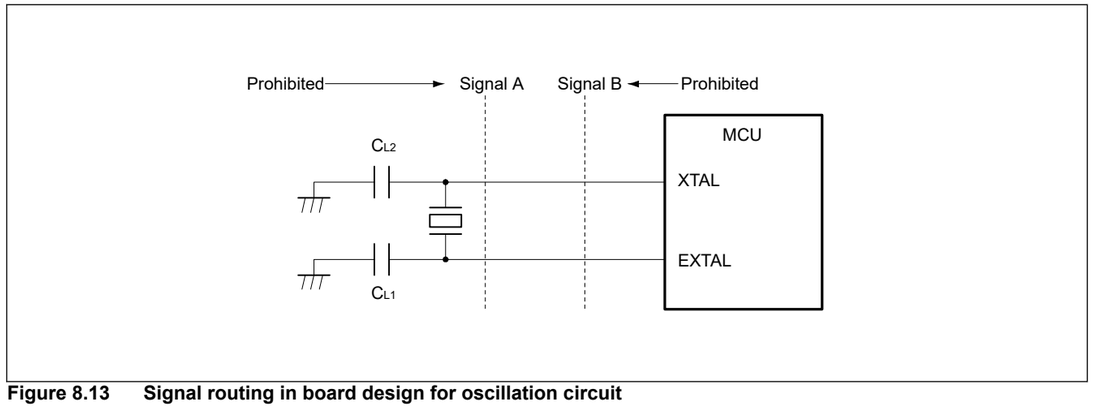


Figure 8.13 Signal routing in board design for oscillation circuit

8.8.4 Notes on Resonator Connect Pin

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports. When these pins are used as general ports, the main clock must be stopped (MOSCCR.MOSTP bit should be set to 1).

8.8.5 Notes on Using Sub-Clock Oscillator

The output of the P212 (EXTAL), P213 (XTAL), and PB01 pins may affect the oscillation by the sub-clock oscillator.

If the sub-clock oscillator is used, implement board design so as not to affect the oscillation. Renesas strongly recommends setting the DSCR[1:0] bits to 00b or 01b when using the P212 (EXTAL), P213 (XTAL), and PB01 as output pins and using the sub-clock oscillator.

In addition, when using the sub-clock oscillator in middle drive capability (SOMCR.SODRV1 = 1), Renesas recommecds setting the DSCR[1:0] bits to 00b when using the P212 (EXTAL), P213 (XTAL), and PB01 as output pins and using the sub-clock oscillator.

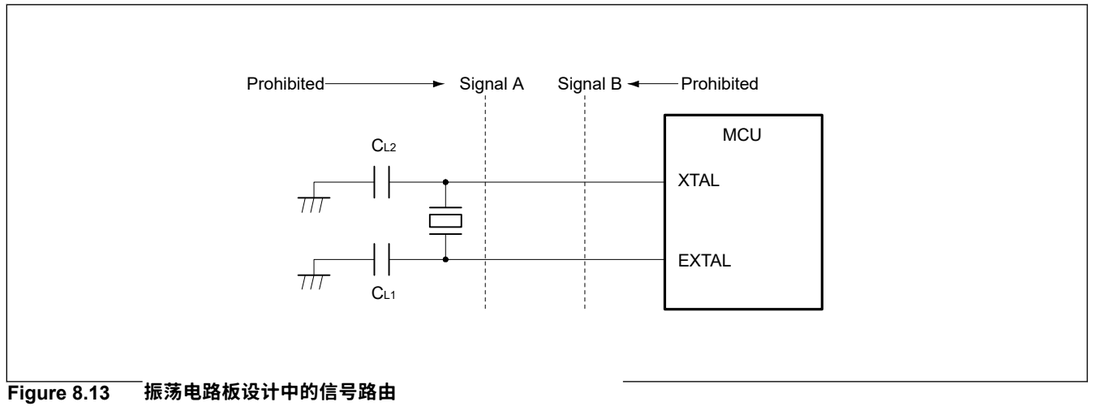


Figure 8.13 振荡电路板设计中的信号路由

8.8.4 谐振器连接引脚注意事项

当不使用主时钟时，EXTAL和XTAL引脚可用作通用端口。当这些引脚用作通用端口时，必须停止主时钟（MOSCCR.MOSTP位应设置为1）。

8.8.5 使用副时钟振荡器的注意事项

P212(EXTAL)、P213(XTAL)和PB01引脚的输出可能会影响副时钟振荡器的振荡。

如果使用副时钟振荡器，请在不影响振荡的情况下进行板卡设计。当使用P212(EXTAL)、P213(XTAL)和PB01作为输出引脚并使用副时钟振荡器时，瑞萨强烈建议将DSCR[1:0]位设置为00b或01b。

此外，当在中间驱动能力中使用副时钟振荡器（SOMCR.SODRV1=1）时，瑞萨建议在使用P212（EXTAL）、P213（XTAL）和PB01时将DSCR[1:0]位设置为00b作为输出引脚并使用副时钟振荡器。

9. Clock Frequency Accuracy Measurement Circuit (CAC)

9.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 9.1 lists the CAC specifications, Figure 9.1 shows the CAC block diagram, and Table 9.2 lists the CAC I/O pin.

Table 9.1 CAC specifications

Parameter	Specifications
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • Peripheral module clock B (PCLKB) • IWDT-dedicated clock
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set

9. 时钟频率精度测量电路(CAC)

9.1 Overview

时钟频率精度测量电路(CAC)在被选为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲数在允许范围内。当测量完成或测量参考时钟产生的时间内的脉冲数不在允许范围内时，将产生中断请求。

表9.1列出了CAC规格，图9.1显示了CAC框图，表9.2列出了CACIO引脚。

Table 9.1 CAC规格

Parameter	Specifications
测量目标时钟	可以测量频率：● 主时钟振荡器 • Sub-clock oscillator • HOCO clock • MOCO clock • 机车时钟 • 外设模块时钟B(PCLKB) • IWDT-dedicated clock
测量参考时钟	频率可参考：● CACREF引脚的外部时钟输入 • 主时钟振荡器 • Sub-clock oscillator • HOCO clock • MOCO clock • 机车时钟 • 外设模块时钟B(PCLKB) • IWDT-dedicated clock
可选择的功能	数字滤波器
中断源	• 测量结束 • 频率误差 • Overflow
Module-stop function	可设置模块停止状态以降低功耗
TrustZone Filter	可设置安全属性

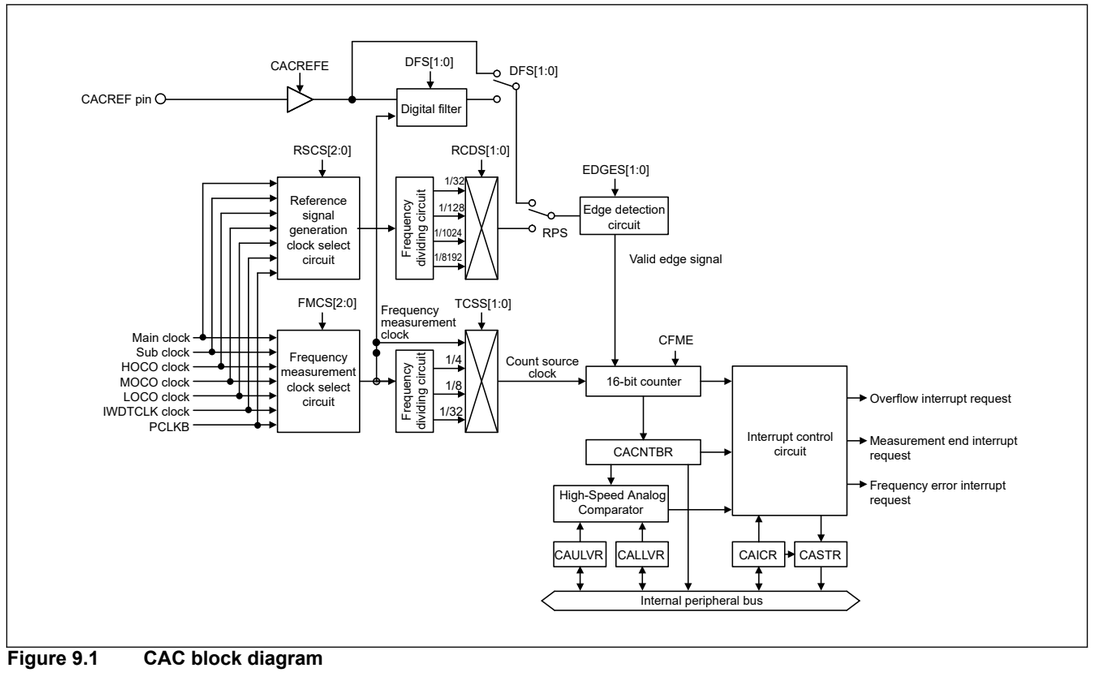


Figure 9.1 CAC block diagram

Table 9.2 CAC I/O pin

Function	Pin name	I/O	Description
CAC	CACREF	Input	Measurement reference clock input pin

9.2 Register Descriptions

9.2.1 CACR0 : CAC Control Register 0

Base address: CAC = 0x4008_3600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	Clock Frequency Measurement Enable 0: Disable 1: Enable	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables clock frequency measurement. Changes made to this bit are not immediately reflected to the internal circuit. Read the bit to confirm that the change has been reflected.

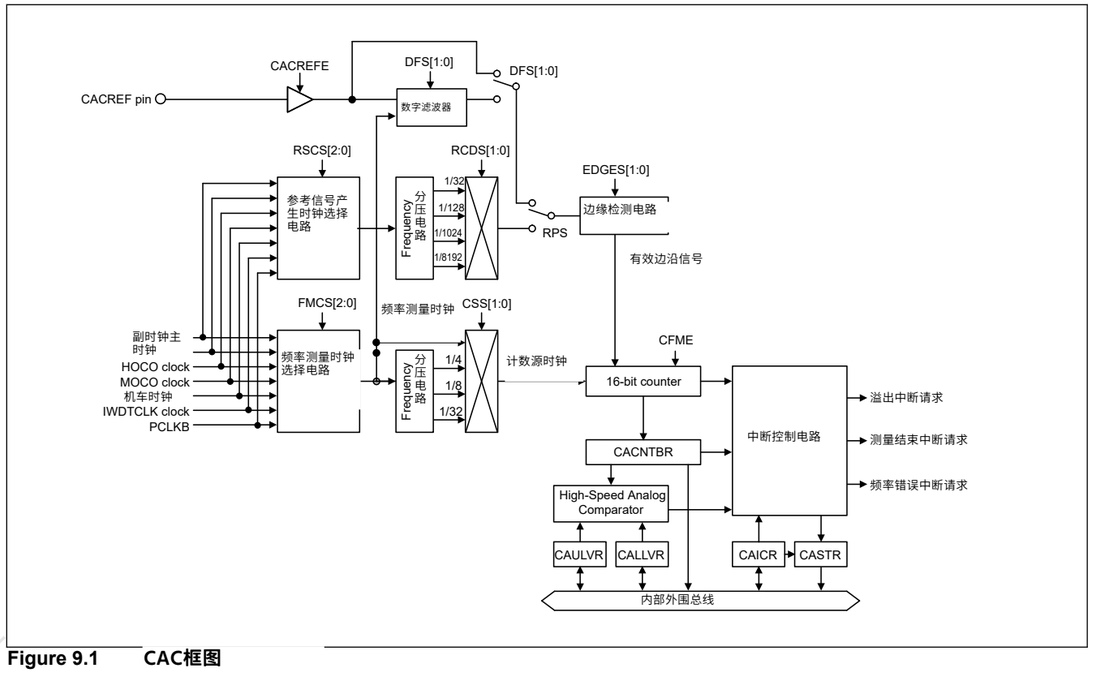


Figure 9.1 CAC框图

Table 9.2 CACIO引脚

Function	引脚名称	I/O	Description
CAC	CACREF	Input	测量参考时钟输入引脚

9.2 注册说明

9.2.1 CACR0:CAC控制寄存器0

Base address: CAC = 0x4008_3600

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFME
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFME	时钟频率测量启用 0：禁用1 ：启用	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

CFME位（时钟频率测量使能）

CFME位使能时钟频率测量。对该位所做的更改不会立即反映到内部电路。读取该位以确认更改已反映。

9.2.2 CACR1 : CAC Control Register 1

Base address: CAC = 0x4008_3600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF Pin Input Enable 0: Disable 1: Enable	R/W
3:1	FMCS[2:0]	Measurement Target Clock Select 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	TCSS[1:0]	Timer Count Clock Source Select 0 0: No division 0 1: × 1/4 clock 1 0: × 1/8 clock 1 1: × 1/32 clock	R/W
7:6	EDGES[1:0]	Valid Edge Select 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] bits (Timer Count Clock Source Select)

The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

9.2.3 CACR2 : CAC Control Register 2

Base address: CAC = 0x4008_3600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
Value after reset:	0	0	0	0	0	0	0	0

9.2.2 CACR1：CAC控制寄存器1

Base address: CAC = 0x4008_3600

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	EDGES[1:0]		TCSS[1:0]		FMCS[2:0]			CACREFE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CACREFE	CACREF引脚输入使能 0：禁用1 ：启用	R/W
3:1	FMCS[2:0]	测量目标时钟选择 000：主时钟振荡器001：副时钟振荡器01 0：HOCO时钟011：MOCO时钟100：LOC O时钟101：外设模块时钟B(PCLKB)110：I WDT-专用时钟111：禁止设置	R/W
5:4	TCSS[1:0]	定时器计数时钟源选择 00：不分频01： ×14个时钟10：× 18个时钟11：×1 32个时钟	R/W
7:6	EDGES[1:0]	有效边选择 00：上升沿01：下降沿10：上升 沿和下降沿11：禁止设置	R/W

Note: 当CACR0.CFME位为0时设置CACR1寄存器。

CACREFE位（CACREF引脚输入使能）

CACREFE位使能CACREF引脚输入。

FMCS[2:0]位（测量目标时钟选择）

FMCS[2:0]位选择要测量其频率的测量目标时钟。

TCSS[1:0]位（定时器计数时钟源选择）

TCSS[1:0]位选择测量目标时钟的分频比。

EDGES[1:0]位（有效边沿选择）

EDGES[1:0]位选择参考信号的有效边沿。

9.2.3 CACR2：CAC控制寄存器2

Base address: CAC = 0x4008_3600

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DFS[1:0]		RCDS[1:0]		RSCS[2:0]			RPS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPS	Reference Signal Select 0: CACREF pin input 1: Internal clock (internally generated signal)	R/W
3:1	RSCS[2:0]	Measurement Reference Clock Select 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock B (PCLKB) 1 1 0: IWDT-dedicated clock 1 1 1: Setting prohibited	R/W
5:4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	Digital Filter Select 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the reference clock for measurement.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

The RCDS[1:0] bits select the frequency-divisor of the reference clock for measurement when an internal reference clock is selected. When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The DFS[1:0] bits enable or disable the digital filter and selects its sampling clock.

9.2.4 CAICR : CAC Interrupt Control Register

Base address: CAC = 0x4008_3600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	Frequency Error Interrupt Request Enable 0: Disable 1: Enable	R/W

Bit	Symbol	Function	R/W
0	RPS	参考信号选择 0：CACREF引脚输入1：内部时钟（内部产生的信号）	R/W
3:1	RSCS[2:0]	测量参考时钟选择 000：主时钟振荡器001：副时钟振荡器01 0：HOCO时钟011：MOCO时钟100：LOC O时钟101：外设模块时钟B(PCLKB)110：I WDT-专用时钟111：禁止设置	R/W
5:4	RCDS[1:0]	测量参考时钟分频比选择 0 0: × 1/32 clock 0 1: × 1/128 clock 1 0: × 1/1024 clock 1 1: × 1/8192 clock	R/W
7:6	DFS[1:0]	数字滤波器选择 00：关闭数字滤波01：使用数字滤波器的采样时钟作为测频时钟10：使用数字滤波器的采样时钟作为测频时钟的4分频 11：使用数字滤波器的采样时钟作为频率测量时钟除以16。	R/W

Note: 当CACR0.CFME位为0时设置CACR2寄存器。

RPS位（参考信号选择）

RPS位选择是使用CACREF引脚输入还是使用内部时钟（内部产生的信号）作为参考信号。

RSCS[2:0]位（测量参考时钟选择）

RSCS[2:0]位选择用于测量的参考时钟。

RCDS[1:0]位（测量参考时钟分频比选择）

TheRCDS[1:0]bitsselectthefrequency-divisorofthereferenceclockformeasurementwhenaninternalreferenceclocki sselected.当RPS=0（CACREF引脚用作参考时钟源）时，参考时钟不分频。

DFS[1:0]位（数字滤波器选择）

DFS[1:0]位启用或禁用数字滤波器并选择其采样时钟。

9.2.4 CAICR:CAC中断控制寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRIE	频率错误中断请求使能 0：禁用1 ：启用	R/W

Bit	Symbol	Function	R/W
1	MENDIE	Measurement End Interrupt Request Enable 0: Disable 1: Enable	R/W
2	OVFIE	Overflow Interrupt Request Enable 0: Disable 1: Enable	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	FERRFCL	FERRF Clear 0: No effect 1: The CASTR.FERRF flag is cleared	W
5	MENDFCL	MENDF Clear 0: No effect 1: The CASTR.MENDF flag is cleared	W
6	OVFFCL	OVFF Clear 0: No effect 1: The CASTR.OVFF flag is cleared.	W
7	—	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables or disables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables or disables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables or disables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag.

MENDFCL bit (MENDF Clear)

Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag.

OVFFCL bit (OVFF Clear)

Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag.

9.2.5 CASTR : CAC Status Register

Base address: CAC = 0x4008_3600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	Frequency Error Flag 0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
1	MENDF	Measurement End Flag 0: Measurement is in progress 1: Measurement ended	R

Bit	Symbol	Function	R/W
1	MENDIE	测量结束中断请求使能 0：禁用1 ：启用	R/W
2	OVFIE	溢出中断请求使能 0：禁用1 ：启用	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	FERRFCL	FERRF Clear 0：无效1：清除CASTR.FERRF标志	W
5	MENDFCL	MENDF Clear 0：无效1：清除CASTR.MENDF标志	W
6	OVFFCL	OVFF Clear 0：无效1：清除CASTR.OVFF标志。	W
7	—	该位读取为0。写入值应为0。	R/W

FERRIE位（频率错误中断请求使能）

FERRIE位启用或禁用频率错误中断请求。

MENDIE位（测量结束中断请求使能）

MENDIE位启用或禁用测量结束中断请求。

OVFIE位（溢出中断请求使能）

OVFIE位启用或禁用溢出中断请求。

FERRFCL bit (FERRF Clear)

将FERRFCL位设置为1会清除CASTR.FERRF标志。

MENDFCL bit (MENDF Clear)

将MENDFCL位设置为1会清除CASTR.MENDF标志。

OVFFCL bit (OVFF Clear)

将OVFFCL位设置为1会清除CASTR.OVFF标志。

9.2.5 CASTR:CAC状态寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	OVFF	MENDF	FERRF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FERRF	频率错误标志 0：时钟频率在允许范围内1：时钟频率偏离允许范围（频率误差）。	R
1	MENDF	测量结束标志 0：测量中1：测量结束	R

Bit	Symbol	Function	R/W
2	OVFF	Overflow Flag 0: Counter has not overflowed 1: Counter overflowed	R
7:3	—	These bits are read as 0.	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement ends.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflows.

[Clearing condition]

- 1 is written to the CAICR.OVFFCL bit.

9.2.6 CAULVR : CAC Upper-Limit Value Setting Register

Base address: CAC = 0x4008_3600

Offset address: 0x06

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Upper Value of the Allowable Range The CAULVR register is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value exceeds the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

Bit	Symbol	Function	R/W
2	OVFF	溢出标志 0：计数器未溢出1：计数器溢出	R
7:3	—	这些位读为0。	R

FERRF标志（频率错误标志）

FERRF标志表示时钟频率与设定值的偏差（频率误差）。

[Setting condition]

●时钟频率超出CAULVR和CALLVR寄存器中定义的允许范围。

[Clearing condition]

●1写入FERRFCL位。

MENDF标志（测量结束标志）

MENDF标志表示测量结束。

[Setting condition]

●测量结束。

[Clearing condition]

●1写入MENDFCL位。

OVFF flag (Overflow Flag)

OVFF标志表示计数器溢出。

[Setting condition]

●计数器溢出。

[Clearing condition]

●1写入CAICR.OVFFCL位。

9.2.6 CAULVR:CAC上限值设置寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x06

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	允许范围的上限值 CAULVR寄存器是一个16位读写寄存器，用于指定允许范围的上限值。当计数器值超过此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。	R/W

9.2.7 CALLVR : CAC Lower-Limit Value Setting Register

Base address: CAC = 0x4008_3600

Offset address: 0x08

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Lower Value of the Allowable Range The CALLVR register is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0. The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit, and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.	R/W

9.2.8 CACNTBR : CAC Counter Buffer Register

Base address: CAC = 0x4008_3600

Offset address: 0x0A

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	The Measurement Result The CACNTBR register is a 16-bit read-only register that stores the measurement result.	R

9.3 Operation

9.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or an internal clock as a reference. Figure 9.2 shows an operating example of the CAC.

9.2.7 CALLVR:CAC下限值设置寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x08

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	允许范围的下限值 CALLVR寄存器是一个16位读写寄存器，用于指定允许范围的下限值。当计数器值低于此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位差以及CACREF引脚上的信号而变化。确保此设置允许有足够的余量。	R/W

9.2.8 CACNTBR:CAC计数器缓冲寄存器

Base address: CAC = 0x4008_3600

Offset address: 0x0A

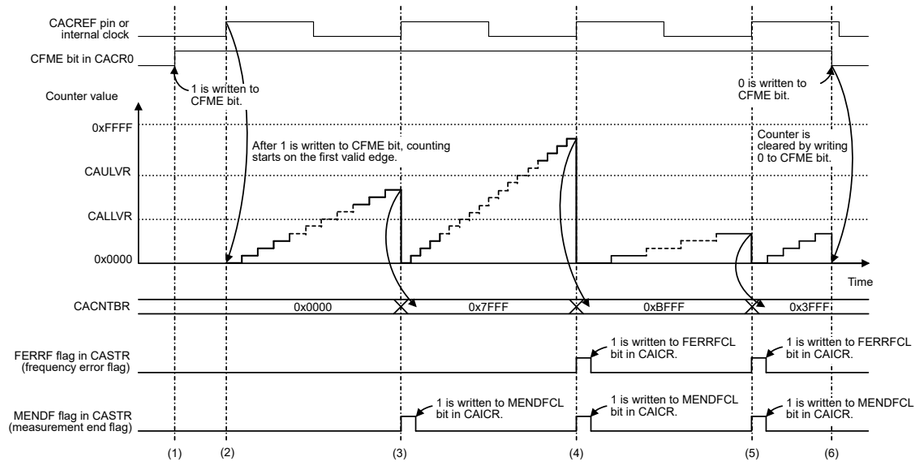
Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	测量结果 CACNTBR寄存器是一个16位只读寄存器，用于存储测量结果。	R

9.3 Operation

9.3.1 测量时钟频率

CAC使用CACREF引脚输入或内部时钟作为参考来测量时钟频率。图9.2显示了CAC的操作示例。

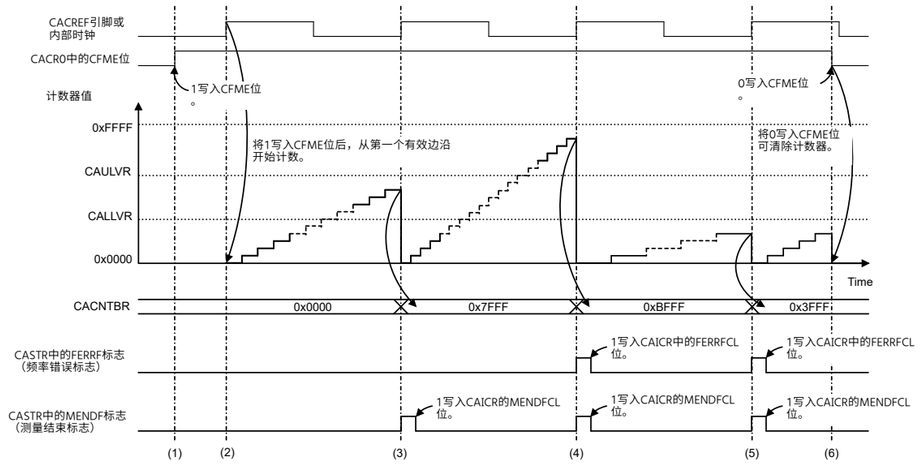


When the CACREF pin input is used as a reference:
In CACR1: CACREFE bit = 1, EDGES[1:0] bits = 00b
CAULVR register = 0xAAAA, CALLVR register = 0x5555
When the internal clock is used as a reference:
In CACR1: CACREFE bit = 0, EDGES[1:0] bits = 00b
CAULVR register = 0xAAAA, CALLVR register = 0x5555

Figure 9.2 CAC operating example

The events in Figure 9.2 are:

1. When the CACREF pin input is used as reference (CACR1.CACREFE = 1), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 0 and the CACR1.CACREFE bit is set to 1. When the internal clock is used as reference (CACR1.CACREFE = 0), frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is set to 1.
2. When the CACREF pin input is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2)is input from the CACREF pin. When the internal clock is used as reference, after 1 is written to the CFME bit, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits (rising edge (CACR1.EDGES[1:0] = 00b) in Figure 9.2) is input based on the clock source selected by the CACR2.RSCS[2:0] bits.
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1, because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.



当CACREF引脚输入用作参考时：在CACR1中：CACREFE位=1，EDGES[1:0]位=00b
CAULVR register = 0xAAAA, CALLVR register = 0x5555
当内部时钟用作参考时：
在CACR1中：CACREFE位=0，EDGES[1:0]位=00b
CAULVR register = 0xAAAA, CALLVR register = 0x5555

Figure 9.2 CAC操作示例

图9.2中的事件是：

1.当CACREF引脚输入用作参考时（CACR1.CACREFE=1），频率测量通过以下方式启用
将1写入CACR0.CFME位，同时将CACR2.RPS位设置为0，并将CACR1.CACREFE位设置为1。当内部时钟用作参考时(CACR1.CACREFE=0)，频率测量通过以下方式启用将1写入CACR0.CFME位，同时CACR2.RPS位设置为1。

2.当CACREF引脚输入用作参考时，向CFME位写入1后，如果CACR1.EDGES[1:0]位选择的有效沿（上升沿（CACR1.EDGES图9.2中的[1:0]=00b)从CACREF引脚输入。当内部时钟用作参考时，CFME位写入1后，如果CACR1.EDGES[1:0]位选择的有效沿（上升沿（CACR1.EDGES[1:图9.2中的0]=00b))根据CACR2.RSCS[2:0]位选择的时钟源输入。

3.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR≤CAULVR和CACNTBR≥CALLVR都为真，则只有MENDF标志CASTR设置为1，因为时钟频率正确。如果CAICR中的MENDIE位为1，则产生测量结束中断。

4.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR>CAULVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。

5.当输入下一个有效边沿时，计数器值被传送到CACNTBR并与中的值进行比较
CAULVR和CALLVR。如果CACNTBR<CALLVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。

6.当CACR0中的CFME位为1时，每次输入有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。向CACR0中的CFME位写入0将清除计数器并停止向上计数。

9.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are selectable.

The counter value transferred to CACNTBR might be in error by up to 1 cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained using the following formula:

Counter value error = (1 cycle of the count source clock) / (1 cycle of the sampling clock)

9.4 Interrupt Requests

The CAC generates three types of interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt

When an interrupt source is generated, the associated status flag is set to 1. Table 9.3 provides information on the CAC interrupt requests.

Table 9.3 CAC interrupt requests

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	Counter overflows

9.5 Usage Notes

9.5.1 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable CAC operation. The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

9.3.2 CACREF引脚上的信号数字滤波

CACREF引脚有一个数字滤波器，CACREF引脚上的电平在选定的采样间隔内连续三个匹配后传输到内部电路。同一电平继续在内部传输，直到引脚上的电平再次连续匹配三个。可选择启用或禁用数字滤波器及其采样时钟。

由于数字滤波器的相位和输入到CACREF引脚的信号之间的差异，传输到CACNTBR的计数器值可能会出现最多1个采样时钟周期的错误。Whenafrequencydividingclockisselectedasacountsourceclock thecountervalueerrorisobtainedusingthefollowingformula:

计数器值误差=（计数源时钟的1个周期）（采样时钟的1个周期）

9.4 中断请求

CAC产生三种类型的中断请求：

●频率错误中断

●测量结束中断

●溢出中断

产生中断源时，相关状态标志设置为1。表9.3提供了有关CAC中断请求的信息。

Table 9.3 CAC中断请求

中断请求	中断使能位	状态标志	中断源
频率错误中断	CAICR.FERRIE	CASTR.FERRF	CACNTBR与CAULVR和CALLVR比较的结果是CACNTBR>CAULVR或CACNTBR<CALLVR
测量结束中断	CAICR.MENDIE	CASTR.MENDF	• 有效边沿从CACREF引脚或内部时钟输入 • 将1写入CACR0.CFME位后，在第一个有效边沿不发生测量结束中断
溢出中断	CAICR.OVFIE	CASTR.OVFF	计数器溢出

9.5 使用说明

9.5.1 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CAC操作。CAC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

10. Low Power Modes

10.1 Overview

The MCU has several functions for reducing power consumption, such as setting clock dividers, EBCLK output control, stopping modules, selecting power control mode in Normal mode, and transitioning to low power modes.

Table 10.1 lists the specifications of the low power mode functions. Table 10.2 lists the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DTC, DMAC and SRAM operate.

Table 10.1 Specifications of the low power mode functions

Item	Specification
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK). *1
EBCLK output control	BCLK output or high-level output can be selected.
Module stop	Functions can be stopped independently for each peripheral module
Low-power modes	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode
Power control modes	• Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency. • Three operating power control modes are available: High-speed mode Low-speed mode Subosc-speed mode
TrustZone Filter	Security attribution can be set for each registers

Note 1. For details, see section 8, Clock Generation Circuit

Table 10.2 Operating conditions of each low power mode (1 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	Snooze request trigger in Software Standby mode. SNZCR.SNZE=1.	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.	Interrupts shown in Table 10.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Reset state
State after cancellation by a reset	Reset state	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*6	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*9
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1	Selectable*1	Stop
PLL	Selectable	Stop	Selectable*6	Stop
PLL2	Selectable	Stop	Selectable*6	Stop
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*2	Selectable	Stop (Undefined)

10. 低功耗模式

10.1 Overview

MCU具有多种降低功耗的功能，例如设置时钟分频器、EBCLK输出控制、停止模块、在正常模式下选择电源控制模式以及转换到低功耗模式。

表10.1列出了低功耗模式功能的规格。表10.2列出了转换到低功耗模式的条件、CPU和外围模块的状态以及取消每种模式的方法。复位后，MCU进入程序执行状态，但只有DTC、DMAC和SRAM运行。

Table 10.1 低功耗模式功能的规格

Item	Specification
通过切换时钟信号降低功耗	分频比可以为系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）、外部总线时钟（BCLK）和闪存接口时钟（FCLK）独立选择。*1
EBCLK输出控制	可选择BCLK输出或高电平输出。
模块停止	每个外围模块可以独立停止功能
Low-power modes	• 睡眠模式 • 软件待机模式 • 贪睡模式 • 深度软件待机模式
电源控制模式	• 根据工作频率选择合适的工作功率控制模式，可以降低正常和睡眠模式下的功耗。 • 提供三种工作功率控制模式： High-speed mode Low-speed mode Subosc-speed mode
TrustZone Filter	可以为每个寄存器设置安全属性

注1.详见第8节，时钟产生电路

Table 10.2 每种低功耗模式的运行条件（2个中的1个）

Item	睡眠模式	软件待机模式	贪睡模式	深度软件待机模式
过渡条件	WFI指令同时 SBYCR.SSBY = 0	WFI指令同时 SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	软件待机模式下的贪睡请求触发。 SNZCR.SNZE=1.	WFI指令同时 SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
取消方法	所有中断。 该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。	中断如表10.3所示。该模式下可用的任何复位。	中断如表10.3所示。 该模式下可用的任何复位。
中断取消后的状态	程序执行状态（中断处理）	程序执行状态（中断处理）	程序执行状态（中断处理）	重置状态
通过复位取消后的状态	重置状态	重置状态	重置状态	重置状态
主时钟振荡器	Selectable	Stop	Selectable*6	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*9
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1	Selectable*1	Stop
PLL	Selectable	Stop	Selectable*6	Stop
PLL2	Selectable	Stop	Selectable*6	Stop
振荡停止检测功能	Selectable	禁止操作	禁止操作	禁止操作
时钟蜂鸣器输出功能	Selectable	Selectable*2	Selectable	Stop (Undefined)

Table 10.2 Operating conditions of each low power mode (2 of 2)

Item	Sleep mode	Software Standby mode	Snooze mode	Deep Software Standby mode
External Bus (EBCLK)	Selectable	Stop (Retained)	Operation prohibited	Stop (Retained)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Standby SRAM	Selectable	Stop (Retained)	Selectable	Stop (Retained/Undefined)*10
Flash memory	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
USB 2.0 Full-Speed (USBFSn, n = 0)	Selectable	Stop (Retained). Detection of USB resumption is possible.	Operation prohibited. Detection of USB resumption is possible.	Stop (Retained/Undefined) Detection of USB resumption is possible.*11
USB 2.0 High-Speed Module (USBHS)	Selectable	Stop (Retained). Detection of USB resumption is possible.	Operation prohibited. Detection of USB resumption is possible.	Stop (Retained/Undefined) Detection of USB resumption is possible.*11
Watchdog Timer (WDT)	Selectable*1	Stop (Retained)	Stop (Retained)	Stop (Undefined)
Independent Watchdog Timer (IWDT)	Selectable*1	Selectable*1	Selectable*1	Stop (Undefined)
Realtime clock (RTC)	Selectable	Selectable	Selectable	Selectable*12
Asynchronous General Purpose Timer (AGTn (n = 0 to 3))	Selectable	Selectable*3	Selectable*3	Selectable*3
Asynchronous General Purpose Timer (AGTn (n = 4 to 5))	Selectable	Selectable*15	Selectable*15	Stop (Undefined)
12-Bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*16	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Capacitive Touch Sensing Unit (CTSU)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable (RXD0 falling edge is available, to enter snooze mode) (only in asynchronous mode).*7	Stop (Undefined)
Serial Communications Interface (SCIn (n = 1 to 9))	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I2C Bus Interface (IIC0)	Selectable	Selectable*4	Selectable*4 Only wakeup interrupt is available.	Stop (Undefined)
I2C Bus Interface (IIC1)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I2C Bus Interface (IIC2)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*8	Stop (Undefined)
IRQn (n = 0 to 15) pin interrupt	Selectable	Selectable	Selectable	Stop (Undefined)
NMI, IRQn-DS (n = 0 to 15) pin interrupt	Selectable	Selectable	Selectable	Selectable
Low voltage detection (LVD)	Selectable	Selectable	Selectable	Selectable*13
Power-on reset circuit	Operating	Operating	Operating	Operating*14
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I/O Ports	Operating	Retained*5	Operating EBCLK pin: Stop (Retained).	Retained*5

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.

Table 10.2 每种低功耗模式的操作条件（2个中的2个）

Item	睡眠模式	软件待机模式	贪睡模式	深度软件待机模式
外部总线(EBCLK)	Selectable	Stop (Retained)	禁止操作	Stop (Retained)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Standby SRAM	Selectable	Stop (Retained)	Selectable	Stop (Retained/Undefined)*10
闪存	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
数据传输控制器(DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
USB 2.0 Full-Speed (USBFSn, n = 0)	Selectable	Stop (Retained). 可以检测USB恢复。	禁止操作。 可以检测USB恢复。	Stop (Retained/Undefined) 可以检测USB恢复。*11
USB 2.0 High-Speed Module (USBHS)	Selectable	Stop (Retained). 可以检测USB恢复。	禁止操作。 可以检测USB恢复。	Stop (Retained/Undefined) 可以检测USB恢复。*11
看门狗定时器(WDT)	Selectable*1	Stop (Retained)	Stop (Retained)	Stop (Undefined)
独立看门狗 Timer (IWDT)	Selectable*1	Selectable*1	Selectable*1	Stop (Undefined)
实时时钟(RTC)	Selectable	Selectable	Selectable	Selectable*12
异步通用 定时器（AGTn（n =0到3））	Selectable	Selectable*3	Selectable*3	Selectable*3
异步通用 定时器（AGTn（n =4到5））	Selectable	Selectable*15	Selectable*15	Stop (Undefined)
12-Bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*16	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
电容式触控感应单元(CTSU)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
数据运算电路(DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
串行通信接口(SCI0)	Selectable	Stop (Retained)	可选（RXD0下降沿可用，进入贪睡模式）（仅在异步模式下）。*7	Stop (Undefined)
串行通信接口(SCIn(n=1to9))	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I2C总线接口(IIC0)	Selectable	Selectable*4	Selectable*4 只有唤醒中断可用。	Stop (Undefined)
I2C总线接口(IIC1)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I2C总线接口(IIC2)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
事件链接控制器(ELC)	Selectable	Stop (Retained)	Selectable*8	Stop (Undefined)
IRQn(n=0to15)引脚中断	Selectable	Selectable	Selectable	Stop (Undefined)
NMI IRQn-DS(n=0to15)引脚中断	Selectable	Selectable	Selectable	Selectable
低电压检测(LVD)	Selectable	Selectable	Selectable	Selectable*13
上电复位电路	Operating	Operating	Operating	Operating*14
其他外围模块	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I/O Ports	Operating	Retained*5	Operating EBCLK pin: Stop (Retained).	Retained*5

Note: 可选择的意思是可以通过控制寄存器来选择操作或不操作。
停止（Retained）表示内部寄存器的内容被保留但操作被暂停。
禁止操作意味着在进入软件待机模式之前必须停止该功能。

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Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.
All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. In order to avoid increase in power consumption in Snooze mode, module-stop bit of modules which are unnecessary in Snooze mode must be set to 1 before entering Software Standby mode.

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select Register 0 (OFS0) in WDT auto start mode.Power consumption can be reduced in Normal and Sleep modes by selecting an appropriate operating power control mode according to the operating frequency.

Note 2. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).

Note 3. AGT0/AGT2 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected by the AGT0/2.AGTMR1.TCK[2:0] bits. AGT1/AGT3 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK) or 101b (Underflow event signal from AGT0/AGT2) is selected by the AGT1/3.AGTMR1.TCK[2:0] bits.
When 100b (AGTLCLK) is selected by AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1, 2, 3), the DPSBYCR.DEEPCUT[1:0] bits must set to 00b before entering Deep Software Standby mode.

Note 4. IIC0 wakeup interrupt is available.

Note 5. For the address bus and bus control signals (CS0 to CS7, RD, WR0 to WR1, WR, BC0 to BC1, and ALE), keeping the output state or changing to the high-impedance state can be selected by SBYCR.OPE bit.In case there is a possibility of transferring from Software Standby mode to Snooze mode by any trigger, wakeup interrupt must be disabled.

Note 6. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP and PLL2CR.PLL2STP bits must be 1.

Note 7. Serial communication modes of SCI0 is only in asynchronous mode.

Note 8. Event lists the restrictions described in section 10.10.14. ELC Events in Snooze Mode.

Note 9. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.

Note 10. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, data in the Standby SRAM is retained in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, data in the Standby SRAM is undefined in Deep Software Standby mode.

Note 11. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the values of the USB resume detection circuit registers are retained and detection of USB resumption is enabled, and the values of other registers are undefined in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the values of all registers are undefined in Deep Software Standby mode.

Note 12. When the RCR4.RCKSEL bit set to 1 (LOCO), the DPSBYCR.DEEPCUT[1:0] bits must set to 00b before entering Deep Software Standby mode.

Note 13. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep Software Standby mode.

Note 14. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.

Note 15. AGT4 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected by the AGT4.AGTMR1.TCK[2:0] bits. AGT5 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK) or 101 (Underflow event signal from AGT4) is selected by the AGT5.AGTMR1.TCK[2:0] bits.

Note 16. When using the 12-bit A/D Converter in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits must be 1.

Table 10.3 Interrupt Source for canceling Snooze, Software Standby and Deep Software Standby Modes (1 of 2)

Interrupt source	Name	Software Standby Mode	Snooze Mode	Deep Software Standby Mode
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes	No
	PORT_IRQn-DS (n = 0 to 15)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
USBFS0	USBFS0_USBR	Yes	Yes	Yes
USBHS	USBHS_USBIR	Yes	Yes	Yes
RTC	RTC_ALM	Yes	Yes	Yes
	RTC_PRD	Yes	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No

停止（未定义）表示内部寄存器的内容未定义，内部电路的电源被切断。
进入贪睡模式后，一旦提供PCLK，所有模块停止位为0的模块都会启动。为了避免贪睡模式下的功耗增加，在进入软件待机模式之前，必须将在贪睡模式下不需要的模块的模块停止位设置为1。

注1.在IWDT专用内部振荡器和IWDT中，通过设置IWDT停止控制位来选择操作或停止
(IWDTSTPCTL)在IWDT自动启动模式下选项功能选择寄存器0(OFS0)。在WDT中，通过在WDT自动启动模式下设置选项功能选择寄存器0(OFS0)中的WDT停止控制位(WDTSTPCTL)来选择操作或停止。通过选择适当的操作功率控制，可以在正常和睡眠模式下降低功耗模式根据工作频率。

注2.当时钟输出源选择位(CKOCR.CKOSEL[2:0])设置为010b(LOCO)和100b(SOSC)以外的值时停止。

注3.当AGT02.AGTMR1.TCK[2:0]位选择100b(AGTLCLK)或110b(AGTSCLK)时，AGT0可以进行AGT2操作。
当AGT13.AGTMR1.TCK[2:0]位选择100b(AGTLCLK)、110b(AGTSCLK)或101b（来自AGT0AGT2的下溢事件信号）时，AGT1AGT3操作是可能的。当AGTn.AGTMR1.TCK[2:0]位(n=0 1 2 3)选择100b(AGTLCLK)时，DPSBYCR.DEEPCUT[1:0]位必须在进入深度软件待机之前设置为00b模式。

注4.IIC0唤醒中断可用。
注5.对于地址总线和总线控制信号（CS0至CS7、RD、WR0至WR1、WR、BC0至BC1和ALE），可以通过SBYCR选择保持输出状态或变为高阻抗状态。OPE位。如果有可能通过任何触发从软件待机模式转换到贪睡模式，则必须禁用唤醒中断。

注6.在贪睡模式下使用SCI0时，MOSCCR.MOSTP和PLLCR.PLLSTP和PLL2CR.PLL2STP位必须为1。
注7.SCI0的串行通信模式仅在异步模式下。
注8.事件列出了第10.10.14节中描述的限制。贪睡模式下的ELC事件。
注9.如果DPSBYCR.DEEPCUT[1:0]位为00b，则振荡器状态与进入深度软件待机模式前相同。
当DPSBYCR.DEEPCUT[1:0]位不为00b时，当MCU进入深度软件待机模式时振荡器停止。
注10.如果DPSBYCR.DEEPCUT[1:0]位为00b，则待机SRAM中的数据在深度软件待机模式下保留。当。。。的时候
DPSBYCR.DEEPCUT[1:0]位不是00b，在深度软件待机模式下，待机SRAM中的数据未定义。
注11.如果DPSBYCR.DEEPCUT[1:0]位为00b，则USB恢复检测电路寄存器的值被保留并检测
USB恢复使能，并且在深度软件待机模式下其他寄存器的值未定义。当。。。的时候
DPSBYCR.DEEPCUT[1:0]位不是00b，在深度软件待机模式下所有寄存器的值都是未定义的。
注12.当RCR4.RCKSEL位设置为1(LOCO)时，DPSBYCR.DEEPCUT[1:0]位必须在进入深度软件之前设置为00b
待机模式。
注13.在深度软件待机模式下使用LVD时，DPSBYCR.DEEPCUT[1:0]位必须为00b或01b才能进入深度软件
软件待机模式。
注14.当MCU进入深度软件待机模式且DPSBYCR.DEEPCUT[1:0]位设置为11b时，LVD电路停止并启用上电复位电路的低功耗功能。

注15.当AGT4.AGTMR1.TCK[2:0]位选择100b(AGTLCLK)或110b(AGTSCLK)时，可以进行AGT4操作。当AGT5.AGTMR1.TCK[2:0]位选择100b(AGTLCLK)、110b(AGTSCLK)或101（来自AGT4的下溢事件信号）时，可以进行AGT5操作。

注16.在贪睡模式下使用12位AD转换器时，ADCMPCR.CMPAE和ADCMPCR.CMPBE位必须为1。

Table 10.3 用于取消贪睡、软件待机和深度软件待机模式的中断源（1of2）

中断源	Name	软件待机模式	贪睡模式	深度软件待机模式
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes	No
	PORT_IRQn-DS (n = 0 to 15)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
USBFS0	USBFS0_USBR	Yes	Yes	Yes
USBHS	USBHS_USBIR	Yes	Yes	Yes
RTC	RTC_ALM	Yes	Yes	Yes
	RTC_PRD	Yes	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No

Table 10.3 Interrupt Source for canceling Snooze, Software Standby and Deep Software Standby Modes (2 of 2)

Interrupt source	Name	Software Standby Mode	Snooze Mode	Deep Software Standby Mode
AGT3	AGT3_AGTI	Yes	Yes*3	Yes
	AGT3_AGTCMAI	Yes	Yes	No
	AGT3_AGTCMBI	Yes	Yes	No
IIC0	IIC0_WUI	Yes	Yes	No
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	Yes with SELSR0*1 *3	No
	ADC12n_WCMPUM	No	Yes with SELSR0*1 *3	No
SCI0	SCI0_AM	No	Yes with SELSR0*1 *2	No
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1 *2	No
DTC	DTC_COMPLETE	No	Yes with SELSR0*1 *3	No
DOC	DOC_DOPCI	No	Yes with SELSR0 *1	No
CTSU	CTSU_CTSUFN	No	Yes with SELSR0*1	No

Note 1. To use the interrupt request as a trigger for exiting the Snooze mode, the request must be selected in SELSR0 . See section 13, Interrupt Controller Unit (ICU) for the setting of SELSR0. When a trigger selected in SELSR0 occurs after executing WFI instruction and during the transition from Normal mode to Software Standby mode, the request might or might not be accepted, depending on the timing of the occurrence.
Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be set.
Note 3. The event which is enabled by the SNZEDCRn must not be used.

Table 10.3 用于取消贪睡、软件待机和深度软件待机模式的中断源(2of2)

中断源	Name	软件待机模式	贪睡模式	深度软件待机模式
AGT3	AGT3_AGTI	Yes	Yes*3	Yes
	AGT3_AGTCMAI	Yes	Yes	No
	AGT3_AGTCMBI	Yes	Yes	No
IIC0	IIC0_WUI	Yes	Yes	No
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	是SELSR0*1*3	No
	ADC12n_WCMPUM	No	是SELSR0*1*3	No
SCI0	SCI0_AM	No	是SELSR0*1*2	No
	SCI0_RXI_OR_ERI	No	是SELSR0*1*2	No
DTC	DTC_COMPLETE	No	是SELSR0*1*3	No
DOC	DOC_DOPCI	No	是SELSR0*1	No
CTSU	CTSU_CTSUFN	No	是SELSR0*1	No

注1.要将中断请求用作退出贪睡模式的触发器，必须在SELSR0中选择该请求。见第13节，
用于设置SELSR0的中断控制器单元(ICU)。当SELSR0中选择的触发发生在执行WFI指令之后以及从正常模式到软件待机模式的转换期间，请求可能会或可能不会被接受，具体取决于发生的时间。

注2.只能设置SCI0_AM或SCI0_RXI_OR_ERI之一。
注3.不得使用由SNZEDCRn启用的事件。

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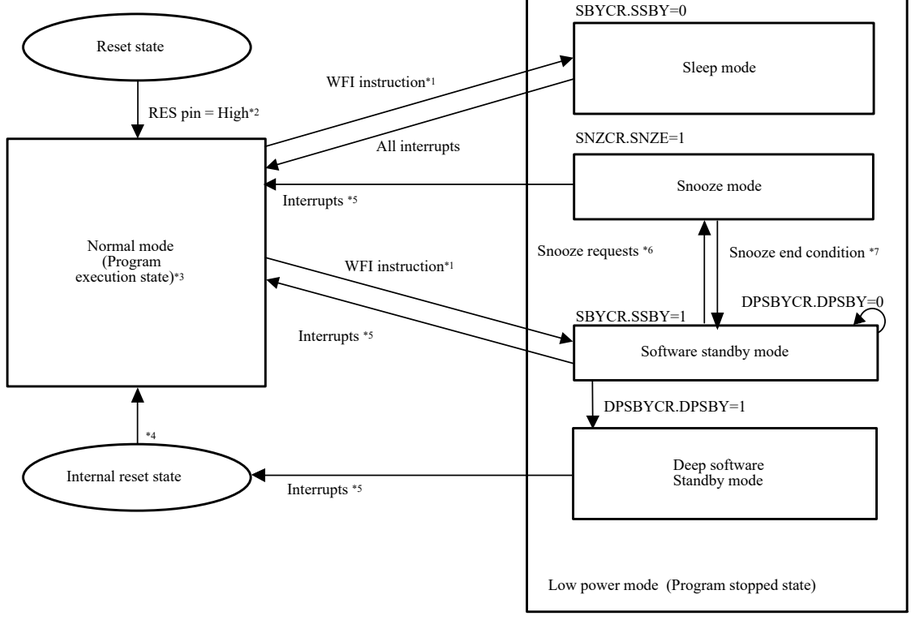
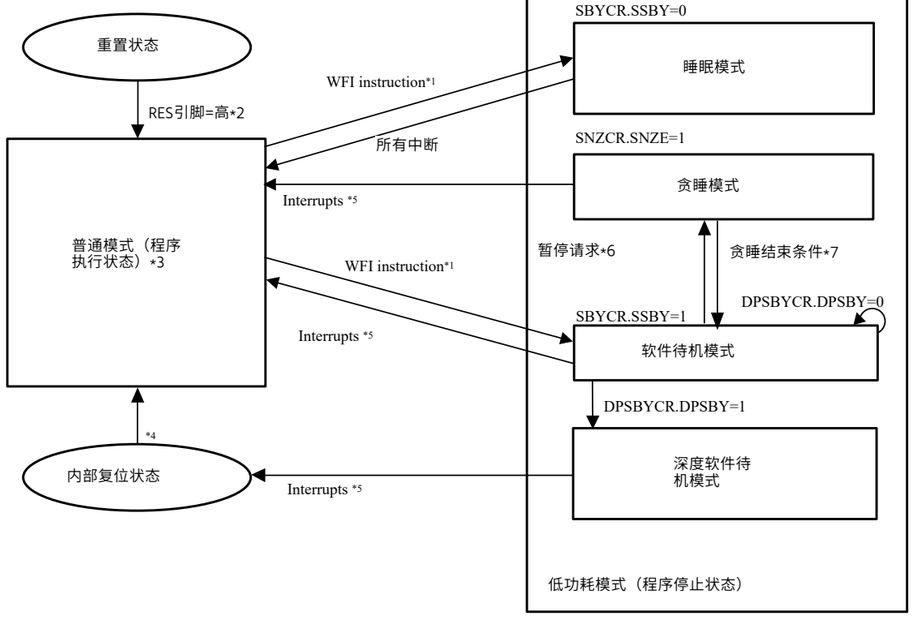


Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program-stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of transitioning to low power mode.
Note 2. The MOCO clock is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made because of an interrupt from Sleep mode, Snooze mode, or Software Standby mode. The clock source is the same as before entering the low power mode.
Note 4. When an available interrupt request is generated, an internal reset (Deep Software Standby reset) is generated over a fixed period. Canceling of Deep Software Standby mode accompanies release from the internal reset state, and then the MCU transitions to Normal mode and executes reset exception processing with the MOCO clock as the source of the operating clock.
Note 5. See Table 10.3
Note 6. See Table 10.7
Note 7. See Table 10.9

Figure 10.1 Mode Transitions



注1.在WFI指令执行后转换到程序停止状态期间，如果接收到用作取消触发的中断，MCU将执行中断异常处理，而不是转换到低功耗模式。

注2.MOCO时钟是从复位状态转换到正常模式后的工作时钟源。
注3.由于休眠模式、贪睡模式或软件待机模式的中断，会转换到正常模式。时钟源与进入低功耗模式前相同。

注4.当产生可用中断请求时，会在固定周期内产生内部复位（深度软件待机复位）。深度软件待机模式的取消伴随着内部复位状态的释放，然后MCU转换到正常模式并以MOCO时钟作为工作时钟源执行复位异常处理。

注5.见表10.3注6.见表10
.7注7.见表10.9

Figure 10.1 模式转换

10.2 Register Descriptions

10.2.1 LPMSAR : Low Power Mode Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	NONSEC9	NONSEC8	—	—	—	NONSEC4	—	NONSEC2	—	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0*1	Non Secure Attribute bit 0 Target register: OPCCR, SOPCCR 0: Secure 1: Non Secure	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: SBYCR 0: Secure 1: Non Secure	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	NONSEC4	Non Secure Attribute bit 4 Target register: SNZCR, SNZEDCRn, SNZREQCRn 0: Secure 1: Non Secure	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W
8	NONSEC8	Non Secure Attribute bit 8 Target register: DPSBYCR 0: Secure 1: Non Secure	R/W
9	NONSEC9	Non Secure Attribute bit 9 Target register: DPSWCR 0: Secure 1: Non Secure	R/W
31:10	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. It is recommended that these bits are configured as Non Secure when the device life cycle is NSECSD (DLMMON.DLMMON[3:0]=0011b). See section 52.7.1. Restrictions on setting the security attribution for the details.

The LPMSAR register controls the secure attribute of Low Power Mode registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of OPCCR, SOPCCR.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of SBYCR.

NONSEC4 bit (Non Secure Attribute bit 4)

This bit controls the security attribute of SNZCR, SNZEDCRn, SNZREQCRn

10.2 注册说明

10.2.1 LPMSAR：低功耗模式安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3C8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	NONSEC9	NONSEC8	—	—	—	NONSEC4	—	NONSEC2	—	NONSEC0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0*1	非安全属性位0 Target register: OPCCR, SOPCCR 0：安全1：不安全	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	NONSEC2	非安全属性位2 Target register: SBYCR 0：安全1：不安全	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	NONSEC4	非安全属性位4 Target register: SNZCR, SNZEDCRn, SNZREQCRn 0：安全1：不安全	R/W
7:5	—	这些位被读取为1。写入值应为1。	R/W
8	NONSEC8	非安全属性位8目标寄存器：DPSBYCR 0：安全1：不安全	R/W
9	NONSEC9	非安全属性位9目标寄存器：DPSWCR 0：安全1：不安全	R/W
31:10	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
注1.当设备生命周期为NSECSD时，建议将这些位配置为非安全(DLMMON.DLMMON[3:0]=0011b)。请参阅第52.7.1节。设置详细信息的安全属性的限制。

LPMSAR寄存器控制低功耗模式寄存器的安全属性。

NONSEC0位（非安全属性位0）

该位控制OPCCR、SOPCCR的安全属性。

NONSEC2位（非安全属性位2）

该位控制SBYCR的安全属性。

NONSEC4位（非安全属性位4）

该位控制SNZCR、SNZEDCRn、SNZREQCRn的安全属性

NONSEC8 bit (Non Secure Attribute bit 8)

This bit controls the security attribute of DPSBYCR.

NONSEC9 bit (Non Secure Attribute bit 9)

This bit controls the security attribute of DPSWCR.

10.2.2 DPFSAR : Deep Standby Interrupt Factor Security Attribution Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3E0

Bit position:	31																													0
Bit field:	DPFSAn (n = 0 to 31)																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	DPFSA0 to DPFSA7	Deep Standby Interrupt Factor Security Attribute bit n (n = 0 to 7) Target register: DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 0 to 7) Target factor : IRQn-DS Pin (n = 0 to 7) 0: Secure 1: Non Secure	R/W
15:8	DPFSA8 to DPFSA15	Deep Standby Interrupt Factor Security Attribute bit n (n = 8 to 15) Target register: DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 0 to 7) Target factor : IRQn-DS Pin (n = 8 to 15) 0: Secure 1: Non Secure	R/W
16	DPFSA16	Deep Standby Interrupt Factor Security Attribute bit 16 Target register: DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 Target factor : LVD1 0: Secure 1: Non Secure	R/W
17	DPFSA17	Deep Standby Interrupt Factor Security Attribute bit 17 Target register: DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1 Target factor : LVD2 0: Secure 1: Non Secure	R/W
18	DPFSA18	Deep Standby Interrupt Factor Security Attribute bit 18 Target register: DPSIER2.b2, DPSIFR2.b2 Target factor : RTC Interval 0: Secure 1: Non Secure	R/W
19	DPFSA19	Deep Standby Interrupt Factor Security Attribute bit 19 Target register: DPSIER2.b3, DPSIFR2.b3 Target factor : RTC Alarm 0: Secure 1: Non Secure	R/W
20	DPFSA20	Deep Standby Interrupt Factor Security Attribute bit 20 Target register: DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4 Target factor : NMI Pin 0: Secure 1: Non Secure	R/W
23:21	—	These bits are read as 1. The write value should be 1.	R/W
24	DPFSA24	Deep Standby Interrupt Factor Security Attribute bit 24 Target register: DPSIER3.b0, DPSIFR3.b0 Target factor : USBFS0 Suspend/Resume 0: Secure 1: Non Secure	R/W

NONSEC8位（非安全属性位8）

该位控制DPSBYCR的安全属性。

NONSEC9位（非安全属性位9）

该位控制DPSWCR的安全属性。

10.2.2 DPFSAR：深度待机中断因素安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3E0

Bit position:	31																													0
Bit field:	DPFSAn (n = 0 to 31)																													
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	DPFSA0 to DPFSA7	深度待机中断因素安全属性位n（n=0到7） 目标寄存器：DPSIER0.bn、DPSIFR0.bn、DPSIEGR0.bn（n=0到7） 目标因素：IRQn-DS引脚（n=0至7） 0：安全1：不安全	R/W
15:8	DPFSA8 to DPFSA15	深度待机中断因素安全属性位n（n=8到15） 目标寄存器：DPSIER1.bn、DPSIFR1.bn、DPSIEGR1.bn（n=0到7） 目标因素：IRQn-DS引脚（n=8至15） 0：安全1：不安全	R/W
16	DPFSA16	深度待机中断因素安全属性位16 Target register: DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 目标因素：LVD1 0：安全1：不安全	R/W
17	DPFSA17	深度待机中断因素安全属性位17 Target register: DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1 目标因素：LVD2 0：安全1：不安全	R/W
18	DPFSA18	深度待机中断因素安全属性位18 Target register: DPSIER2.b2, DPSIFR2.b2 目标因素：RTC间隔 0：安全1：不安全	R/W
19	DPFSA19	深度待机中断因素安全属性位19 Target register: DPSIER2.b3, DPSIFR2.b3 目标因素：RTC警报 0：安全1：不安全	R/W
20	DPFSA20	深度待机中断因素安全属性位20 Target register: DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4 目标因素:NMIPin 0：安全1：不安全	R/W
23:21	—	这些位被读取为1。写入值应为1。	R/W
24	DPFSA24	深度待机中断因素安全属性位24 目标寄存器：DPSIER3.b0、DPSIFR3.b0目标因子：USBFS0暂停恢复 0：安全1：不安全	R/W

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Bit	Symbol	Function	R/W
25	DPFSA25	Deep Standby Interrupt Factor Security Attribute bit 25 Target register: DPSIER3.b1, DPSIFR3.b1 Target factor : USBHS Suspend/Resume 0: Secure 1: Non Secure	R/W
26	DPFSA26	Deep Standby Interrupt Factor Security Attribute bit 26 Target register: DPSIER3.b2, DPSIFR3.b2 Target factor : AGT1 Underflow 0: Secure 1: Non Secure	R/W
27	DPFSA27	Deep Standby Interrupt Factor Security Attribute bit 27 Target register: DPSIER3.b3, DPSIFR3.b3 Target factor : AGT3 Underflow 0: Secure 1: Non Secure	R/W
31:28	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The DPFSAR register controls the secure attribute of Deep Standby Interrupt Factor control registers.

DPFSA0 to DPFSA7 bit (Deep Standby Interrupt Factor Security Attribute bit n (n = 0 to 7))

This bit controls the security attribute of DPSIER0.bn, DPSIFR0.bn, DPSIEGR0.bn (n = 0 to 7) .

Target factor is IRQn-DS Pin (n = 0 to 7).

DPFSA8 to DPFSA15 bit (Deep Standby Interrupt Factor Security Attribute bit n (n = 8 to 15))

This bit controls the security attribute of DPSIER1.bn, DPSIFR1.bn, DPSIEGR1.bn (n = 0 to 7) .

Target factor is IRQn-DS Pin (n = 8 to 15)

DPFSA16 bit (Deep Standby Interrupt Factor Security Attribute bit 16)

This bit controls the security attribute of DPSIER2.b0, DPSIFR2.b0, DPSIEGR2.b0 .

Target factor is LVD1.

DPFSA17 bits (Deep Standby Interrupt Factor Security Attribute bit 17)

This bit controls the security attribute of DPSIER2.b1, DPSIFR2.b1, DPSIEGR2.b1.

Target factor is LVD2.

DPFSA18 bit (Deep Standby Interrupt Factor Security Attribute bit 18)

This bit controls the security attribute of DPSIER2.b2, DPSIFR2.b2.

Target factor is RTC Interval.

DPFSA19 bit (Deep Standby Interrupt Factor Security Attribute bit 19)

This bit controls the security attribute of DPSIER2.b3, DPSIFR2.b3.

Target factor is RTC Alarm.

DPFSA20 bit (Deep Standby Interrupt Factor Security Attribute bit 20)

This bit controls the security attribute of DPSIER2.b4, DPSIFR2.b4, DPSIEGR2.b4.

Target factor is NMI Pin.

DPFSA24 bit (Deep Standby Interrupt Factor Security Attribute bit 24)

This bit controls the security attribute of DPSIER3.b0, DPSIFR3.b0.

Target factor is USBFS0 Suspend/Resume.

Bit	Symbol	Function	R/W
25	DPFSA25	深度待机中断因素安全属性位25 Target register: DPSIER3.b1, DPSIFR3.b1 目标因素：USBHS暂停恢复 0：安全1：不安全	R/W
26	DPFSA26	深度待机中断因素安全属性位26 Target register: DPSIER3.b2, DPSIFR3.b2 目标因素：AGT1下溢 0：安全1：不安全	R/W
27	DPFSA27	深度待机中断因素安全属性位27 Target register: DPSIER3.b3, DPSIFR3.b3 目标因素：AGT3下溢 0：安全1：不安全	R/W
31:28	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

DPFSAR寄存器控制深度待机中断因子控制寄存器的安全属性。

DPFSA0至DPFSA7位（深度待机中断因素安全属性位n（n=0至7））

该位控制DPSIER0.bn DPSIFR0.bn DPSIEGR0.bn(n=0to7)的安全属性。

目标因子是IRQn-DS引脚（n=0到7）。

DPFSA8至DPFSA15位（深度待机中断因素安全属性位n（n=8至15））

该位控制DPSIER1.bn DPSIFR1.bn DPSIEGR1.bn(n=0to7)的安全属性。

目标因子是IRQn-DS引脚（n=8到15）

DPFSA16位（深度待机中断因素安全属性位16）

该位控制DPSIER2.b0、DPSIFR2.b0、DPSIEGR2.b0的安全属性。

目标因子是LVD1。

DPFSA17位（深度待机中断因素安全属性位17）

该位控制DPSIER2.b1、DPSIFR2.b1、DPSIEGR2.b1的安全属性。

目标因子是LVD2。

DPFSA18位（深度待机中断因素安全属性位18）

该位控制DPSIER2.b2、DPSIFR2.b2的安全属性。

目标因素是RTC间隔。

DPFSA19位（深度待机中断因素安全属性位19）

该位控制DPSIER2.b3、DPSIFR2.b3的安全属性。

目标因素是RTC警报。

DPFSA20位（深度待机中断因素安全属性位20）

该位控制DPSIER2.b4、DPSIFR2.b4、DPSIEGR2.b4的安全属性。

目标因素是NMI引脚。

DPFSA24位（深度待机中断因素安全属性位24）

该位控制DPSIER3.b0、DPSIFR3.b0的安全属性。

目标因素是USBFS0暂停恢复。

DPFSA25 bit (Deep Standby Interrupt Factor Security Attribute bit 25)

This bit controls the security attribute of DPSIER3.b1, DPSIFR3.b1.

Target factor is USBHS Suspend/Resume.

DPFSA26 bit (Deep Standby Interrupt Factor Security Attribute bit 26)

This bit controls the security attribute of DPSIER3.b2, DPSIFR3.b2.

Target factor is AGT1 Underflow.

DPFSA27 bit (Deep Standby Interrupt Factor Security Attribute bit 27)

This bit controls the security attribute of DPSIER3.b3, DPSIFR3.b3.

Target factor is AGT3 Underflow.

10.2.3 SBYCR : Standby Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	—	These bits are read as reset value.The write value should be reset value	R/W
14	OPE	Output Port Enable 0: In Software Standby mode or Deep Software Standby mode, set the address bus and other bus control signal to the high-impedance state. In snooze mode, the status of the address bus and bus control signals are same as before entering Software Standby mode. 1: In Software Standby mode or Deep Software Standby mode, address bus and other bus control signal retain the output state.	R/W
15	SSBY	Software Standby Mode Select 0: Sleep mode 1: Software Standby mode.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

OPE bit (Output Port Enable)

The OPE bit specifies whether to set to the high-impedance state or to retain the output of the address bus and bus control signals (CS0 to CS7, RD, WR0 to WR1, WR, BC0 to BC1, and ALE) in Software Standby mode or Deep Software Standby mode. when DPSBYCR.DPSBY = 0 and Deep Software Standby mode when DPSBYCR.DPSBY = 1

SSBY bit (Software Standby Mode Select)

The SSBY bit specifies the transition destination after a WFI instruction is executed.

When the SSBY bit is set to 1, the MCU enters Software Standby mode after execution of a WFI instruction. When the MCU returns to Normal mode from Software Standby mode by an interrupt, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to it.

While the OSTDCR.OSTDE bit is 1, setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

While the FENTRYR.FENTRY0 bit is 1 setting of the SSBY bit is ignored. Even if SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

DPFSA25位（深度待机中断因素安全属性位25）

该位控制DPSIER3.b1、DPSIFR3.b1的安全属性。

目标因素是USBHS暂停恢复。

DPFSA26位（深度待机中断因素安全属性位26）

该位控制DPSIER3.b2、DPSIFR3.b2的安全属性。

目标因子是AGT1下溢。

DPFSA27位（深度待机中断因素安全属性位27）

该位控制DPSIER3.b3、DPSIFR3.b3的安全属性。

目标因子是AGT3下溢。

10.2.3 SBYCR：待机控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	—	这些位被读取为复位值。写入值应为复位值	R/W
14	OPE	输出端口使能 0：在软件待机模式或深度软件待机模式下，将地址总线和其他总线控制信号设置为高阻状态。在贪睡模式下，地址总线和总线控制信号的状态与进入软件待机模式前相同。 1：在软件待机模式或深度软件待机模式下，地址总线和其他总线控制信号保持输出状态。	R/W
15	SSBY	软件待机模式选择 0：休眠模式1：软件待机模式。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

OPE位（输出端口使能）

OPE位指定在软件待机模式下是设置为高阻抗状态还是保留地址总线和总线控制信号（CS0到CS7、RD、WR0到WR1、WR、BC0到BC1和ALE）的输出或深度软件待机模式。当DPSBYCR.DPSBY=0和深度软件待机模式时DPSBYCR.DPSBY=1

SSBY位（软件待机模式选择）

SSBY位指定执行WFI指令后的转移目标。

当SSBY位设置为1时，MCU在执行WFI指令后进入软件待机模式。当。。。的时候
MCU通过中断从软件待机模式返回到正常模式，SSBY位保持为1。SSBY位可以通过向其写入0来清除。

当OSTDCR.OSTDE位为1时，忽略SSBY位的设置。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

当FENTRYR.FENTRY0位为1时，SSBY位的设置被忽略。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

10.2.4 MSTPCRA : Module Stop Control Register A

Base address: MSTP = 0x4008_4000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MSTPA7	—	—	—	—	—	—	MSTPA0
Value after reset:	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	MSTPA0	SRAM0 Module Stop Target module: SRAM0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
6:1	—	These bits are read as 1. The write value should be 1.	R/W
7	MSTPA7	Standby SRAM Module Stop Target module: Standby SRAM 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:8	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPA22	DMA Controller/Data Transfer Controller Module Stop*1 Target module: DTC, DMAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:23	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When rewriting the MSTPA22 bit from 0 to 1, disable the DMAC and DTC before setting the MSTPA22 bit.

10.2.5 MSTPCRB : Module Stop Control Register B

Base address: MSTP = 0x4008_4000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	MSTPB26	MSTPB25	MSTPB24	MSTPB23	MSTPB22	—	—	MSTPB19	MSTPB18	—	MSTPB16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MSTPB15	—	—	MSTPB12	MSTPB11	—	MSTPB9	MSTPB8	MSTPB7	MSTPB6	—	—	MSTPB3	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	—	This bit is read as 1. The write value should be 1.	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W

10.2.4 MSTPCRA:模块停止控制寄存器A

Base address: MSTP = 0x4008_4000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MSTPA7	—	—	—	—	—	—	MSTPA0
重置后的值:	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	MSTPA0	SRAM0模块停止 Target module: SRAM0 0：取消模块停止状态1：进入模块停止状态	R/W
6:1	—	这些位被读取为1。写入值应为1。	R/W
7	MSTPA7	待机SRAM模块停止 目标模块：备用SRAM 0：取消模块停止状态1：进入模块停止状态	R/W
21:8	—	这些位被读取为1。写入值应为1。	R/W
22	MSTPA22	DMA控制器数据传输控制器模块停止*1 Target module: DTC, DMAC 0：取消模块停止状态1：进入模块停止状态	R/W
31:23	—	这些位被读取为1。写入值应为1。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.将MSTPA22位从0改写为1时，在设置MSTPA22位之前禁用DMAC和DTC。

10.2.5 MSTPCRB:模块停止控制寄存器B

Base address: MSTP = 0x4008_4000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	MSTPB26	MSTPB25	MSTPB24	MSTPB23	MSTPB22	—	—	MSTPB19	MSTPB18	—	MSTPB16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MSTPB15	—	—	MSTPB12	MSTPB11	—	MSTPB9	MSTPB8	MSTPB7	MSTPB6	—	—	MSTPB3	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	—	该位读取为1。写入值应为1。	R/W
1	—	该位读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	MSTPB3	CEC Module Stop*1 Target module: CEC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
5:4	—	These bits are read as 1. The write value should be 1.	R/W
6	MSTPB6	Quad Serial Peripheral Interface Module Stop Target module: QSPI 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
7	MSTPB7	I2C Bus Interface 2 Module Stop Target module: IIC2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
8	MSTPB8	I2C Bus Interface 1 Module Stop Target module: IIC1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
9	MSTPB9	I2C Bus Interface 0 Module Stop Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
10	—	This bit is read as 1. The write value should be 1.	R/W
11	MSTPB11	Universal Serial Bus 2.0 FS Interface 0 Module Stop*2 Target module: USBFS0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
12	MSTPB12	Universal Serial Bus 2.0 HS Interface Module Stop*3 Target module: USBHS 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14:13	—	These bits are read as 1. The write value should be 1.	R/W
15	MSTPB15	ETHERC0 and EDMAC0 Module Stop Target module: ETHERC0 and EDMAC0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
16	MSTPB16	OSPI Module Stop*4 Target module: OSPI 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
17	—	This bit is read as 1. The write value should be 1.	R/W
18	MSTPB18	Serial Peripheral Interface 1 Module Stop Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19	MSTPB19	Serial Peripheral Interface 0 Module Stop Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPB22	Serial Communication Interface 9 Module Stop Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Bit	Symbol	Function	R/W
2	—	该位读取为1。写入值应为1。	R/W
3	MSTPB3	CEC模块停止*1 Target module: CEC 0：取消模块停止状态1：进入模块停止状态	R/W
5:4	—	这些位被读取为1。写入值应为1。	R/W
6	MSTPB6	四路串行外围接口模块停止 Target module: QSPI 0：取消模块停止状态1：进入模块停止状态	R/W
7	MSTPB7	I2C总线接口2模块停止 Target module: IIC2 0：取消模块停止状态1：进入模块停止状态	R/W
8	MSTPB8	I2C总线接口1模块停止 Target module: IIC1 0：取消模块停止状态1：进入模块停止状态	R/W
9	MSTPB9	I2C总线接口0模块停止 Target module: IIC0 0：取消模块停止状态1：进入模块停止状态	R/W
10	—	该位读取为1。写入值应为1。	R/W
11	MSTPB11	通用串行总线2.0FS接口0模块停止*2 Target module: USBFS0 0：取消模块停止状态1：进入模块停止状态	R/W
12	MSTPB12	通用串行总线2.0HS接口模块停止*3 Target module: USBHS 0：取消模块停止状态1：进入模块停止状态	R/W
14:13	—	这些位被读取为1。写入值应为1。	R/W
15	MSTPB15	ETHERC0和EDMAC0模块停止 目标模块：ETHERC0和EDMAC0 0：取消模块停止状态1：进入模块停止状态	R/W
16	MSTPB16	OSPI模块停止*4 Target module: OSPI 0：取消模块停止状态1：进入模块停止状态	R/W
17	—	该位读取为1。写入值应为1。	R/W
18	MSTPB18	串行外设接口1模块停止 Target module: SPI1 0：取消模块停止状态1：进入模块停止状态	R/W
19	MSTPB19	串行外设接口0模块停止 Target module: SPI0 0：取消模块停止状态1：进入模块停止状态	R/W
21:20	—	这些位被读取为1。写入值应为1。	R/W
22	MSTPB22	串行通讯接口9模块停止 Target module: SCI9 0：取消模块停止状态1：进入模块停止状态	R/W

Bit	Symbol	Function	R/W
23	MSTPB23	Serial Communication Interface 8 Module Stop Target module: SCI8 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
24	MSTPB24	Serial Communication Interface 7 Module Stop Target module: SCI7 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
25	MSTPB25	Serial Communication Interface 6 Module Stop Target module: SCI6 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26	MSTPB26	Serial Communication Interface 5 Module Stop Target module: SCI5 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
27	MSTPB27	Serial Communication Interface 4 Module Stop Target module: SCI4 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28	MSTPB28	Serial Communication Interface 3 Module Stop Target module: SCI3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
29	MSTPB29	Serial Communication Interface 2 Module Stop Target module: SCI2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30	MSTPB30	Serial Communication Interface 1 Module Stop Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31	MSTPB31	Serial Communication Interface 0 Module Stop Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPBi bit, wait for CEC clock (CECMCLK) cycle after writing, and then execute a WFI instruction (i = 3).

Note 2. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPBi bit, wait for two USB clock (USBCLK) cycles after writing, and then execute a WFI instruction (i = 11).

Note 3. The MSTPBi bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPBi bit, wait for two USBCLK and USB60CLK cycles after writing, and then execute a WFI instruction (i = 12).

Note 4. The MSTPB16 bit must be written while the oscillation of the clock controlled by this bit is stabilized. For entering Software Standby mode after writing the MSTPB16 bit, wait for two Octal-SPI clock (OCTACLK) cycles after writing, and then execute a WFI instruction.

Bit	Symbol	Function	R/W
23	MSTPB23	串行通讯接口8模块停止 Target module: SCI8 0：取消模块停止状态1：进入模块停止状态	R/W
24	MSTPB24	串行通讯接口7模块停止 Target module: SCI7 0：取消模块停止状态1：进入模块停止状态	R/W
25	MSTPB25	串行通讯接口6模块停止 Target module: SCI6 0：取消模块停止状态1：进入模块停止状态	R/W
26	MSTPB26	串行通讯接口5模块停止 Target module: SCI5 0：取消模块停止状态1：进入模块停止状态	R/W
27	MSTPB27	串行通讯接口4模块停止 Target module: SCI4 0：取消模块停止状态1：进入模块停止状态	R/W
28	MSTPB28	串行通讯接口3模块停止 Target module: SCI3 0：取消模块停止状态1：进入模块停止状态	R/W
29	MSTPB29	串行通讯接口2模块停止 Target module: SCI2 0：取消模块停止状态1：进入模块停止状态	R/W
30	MSTPB30	串行通讯接口1模块停止 Target module: SCI1 0：取消模块停止状态1：进入模块停止状态	R/W
31	MSTPB31	串行通讯接口0模块停止 Target module: SCI0 0：取消模块停止状态1：进入模块停止状态	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.MSTPBi位必须在由该位控制的时钟振荡稳定时写入。要在写入MSTPBi位后进入软件待机模式，写入后等待CEC时钟(CECMCLK)周期，然后执行WFI指令(i=3)。

注2.MSTPBi位必须在由该位控制的时钟振荡稳定时写入。要在写入MSTPBi位后进入软件待机模式，写入后等待两个USB时钟(USBCLK)周期，然后执行WFI指令(i=11)。

注3.MSTPBi位必须在由该位控制的时钟振荡稳定时写入。进入软件待机
模式写入MSTPBi位后，写入后等待两个USBCLK和USB60CLK周期，然后执行WFI指令（i=12）。

注4.MSTPB16位必须在由该位控制的时钟振荡稳定时写入。要在写入MSTPB16位后进入软件待机模式，写入后等待两个八进制SPI时钟(OCTACLK)周期，然后执行WFI指令。

10.2.6 MSTPCRC : Module Stop Control Register C

Base address: MSTP = 0x4008_4000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	—	MSTPC27	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	MSTPC12	—	—	—	MSTPC8	—	—	—	—	MSTPC3	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	Clock Frequency Accuracy Measurement Circuit Module Stop*1 Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	MSTPC3	Capacitive Touch Sensing Unit Module Stop Target module: CTSU 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
7:4	—	These bits are read as 1. The write value should be 1.	R/W
8	MSTPC8	Serial Sound Interface Enhanced Module Stop Target module: SSIE 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
11:9	—	These bits are read as 1. The write value should be 1.	R/W
12	MSTPC12	Secure Digital HOST IF / Multi Media Card 0 Module Stop Target module: SDHI/MMC0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
13	MSTPC13	Data Operation Circuit Module Stop Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPC14	Event Link Controller Module Stop Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26:15	—	These bits are read as 1. The write value should be 1.	R/W
27	MSTPC27	CANFD Module Stop Target module: CANFD 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30:28	—	These bits are read as 1. The write value should be 1.	R/W
31	MSTPC31	SCE9 Module Stop Target module: SCE9 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

10.2.6 MSTPCRC:模块停止控制寄存器C

Base address: MSTP = 0x4008_4000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	—	MSTPC27	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	MSTPC12	—	—	—	MSTPC8	—	—	—	—	MSTPC3	—	MSTPC1	MSTPC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPC0	时钟频率精度测量电路模块停止*1 目标模块：CAC 0：取消模块停止状态1：进入模块停止状态	R/W
1	MSTPC1	循环冗余校验计算器模块停止 Target module: CRC 0：取消模块停止状态1：进入模块停止状态	R/W
2	—	该位读取为1。写入值应为1。	R/W
3	MSTPC3	电容式触摸感应单元模块停止 Target module: CTSU 0：取消模块停止状态1：进入模块停止状态	R/W
7:4	—	这些位被读取为1。写入值应为1。	R/W
8	MSTPC8	串行声音接口增强模块停止 Target module: SSIE 0：取消模块停止状态1：进入模块停止状态	R/W
11:9	—	这些位被读取为1。写入值应为1。	R/W
12	MSTPC12	SecureDigitalHOSTIF多媒体卡0模块停止 Target module: SDHI/MMC0 0：取消模块停止状态1：进入模块停止状态	R/W
13	MSTPC13	数据运算电路模块停止 目标模块：DOC 0：取消模块停止状态1：进入模块停止状态	R/W
14	MSTPC14	事件链接控制器模块停止 Target module: ELC 0：取消模块停止状态1：进入模块停止状态	R/W
26:15	—	这些位被读取为1。写入值应为1。	R/W
27	MSTPC27	CANFD模块停止 Target module: CANFD 0：取消模块停止状态1：进入模块停止状态	R/W
30:28	—	这些位被读取为1。写入值应为1。	R/W
31	MSTPC31	SCE9模块停止 Target module: SCE9 0：取消模块停止状态1：进入模块停止状态	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. The MSTPC0 bit must be written while the oscillation of the clock to be controlled by this bit is stable. To enter Software Standby mode after writing this bit, wait for 2 cycles of the slowest clock from the clocks output by the oscillators, then execute a WFI instruction.

10.2.7 MSTPCRD : Module Stop Control Register D

Base address: MSTP = 0x4008_4000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MSTPD15	MSTPD14	MSTPD13	MSTPD12	MSTPD11	—	—	—	—	—	—	—	MSTPD3	MSTPD2	MSTPD1	MSTPD0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPD0	Low Power Asynchronous General Purpose Timer 3 Module Stop*3 Target module: AGT3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
1	MSTPD1	Low Power Asynchronous General Purpose Timer 2 Module Stop*4 Target module: AGT2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
2	MSTPD2	Low Power Asynchronous General Purpose Timer 1 Module Stop*1 Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
3	MSTPD3	Low Power Asynchronous General Purpose Timer 0 Module Stop*2 Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
10:4	—	These bits are read as 1. The write value should be 1.	R/W
11	MSTPD11	Port Output Enable for GPT 3 Module Stop Target module: POEG3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
12	MSTPD12	Port Output Enable for GPT 2 Module Stop Target module:POEG2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
13	MSTPD13	Port Output Enable for GPT 1 Module Stop Target module: POEG1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
14	MSTPD14	Port Output Enable for GPT 0 Module Stop Target module: POEG0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.MSTPC0位必须在该位控制的时钟振荡稳定时写入。要在写入该位后进入软件待机模式，请等待振荡器输出时钟中最慢时钟的2个周期，然后执行WFI指令。

10.2.7 MSTPCRD:模块停止控制寄存器D

Base address: MSTP = 0x4008_4000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MSTPD15	MSTPD14	MSTPD13	MSTPD12	MSTPD11	—	—	—	—	—	—	—	MSTPD3	MSTPD2	MSTPD1	MSTPD0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSTPD0	低功耗异步通用定时器3模块停止*3 Target module: AGT3 0：取消模块停止状态1：进入模块停止状态	R/W
1	MSTPD1	低功耗异步通用定时器2模块停止*4 Target module: AGT2 0：取消模块停止状态1：进入模块停止状态	R/W
2	MSTPD2	低功耗异步通用定时器1模块停止*1 Target module: AGT1 0：取消模块停止状态1：进入模块停止状态	R/W
3	MSTPD3	低功耗异步通用定时器0模块停止*2 Target module: AGT0 0：取消模块停止状态1：进入模块停止状态	R/W
10:4	—	这些位被读取为1。写入值应为1。	R/W
11	MSTPD11	GPT3模块停止的端口输出启用 Target module: POEG3 0：取消模块停止状态1：进入模块停止状态	R/W
12	MSTPD12	GPT2模块停止的端口输出启用 Target module:POEG2 0：取消模块停止状态1：进入模块停止状态	R/W
13	MSTPD13	GPT1模块停止的端口输出使能 Target module: POEG1 0：取消模块停止状态1：进入模块停止状态	R/W
14	MSTPD14	GPT0模块停止的端口输出使能 Target module: POEG0 0：取消模块停止状态1：进入模块停止状态	R/W

Bit	Symbol	Function	R/W
15	MSTPD15	12-bit A/D Converter 1 Module Stop Target module: ADC121 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
16	MSTPD16	12-bit A/D Converter 0 Module Stop Target module: ADC120 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
19:17	—	These bits are read as 1. The write value should be 1.	R/W
20	MSTPD20	12-bit D/A Converter Module Stop Target module: DAC12 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
22	MSTPD22	Temperature Sensor Module Stop Target module: Temperature Sensor 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31:23	—	These bits are read as 1. The write value should be 1.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.

Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

Note 3. When the count source is sub-clock oscillator or LOCO, AGT3 counting doesn't stop even if MSTPD0 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT3 registers.

Note 4. When the count source is sub-clock oscillator or LOCO, AGT2 counting doesn't stop even if MSTPD1 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT2 registers.

10.2.8 MSTPCRE : Module Stop Control Register E

Base address: MSTP = 0x4008_4000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPE31	MSTPE30	MSTPE29	MSTPE28	MSTPE27	MSTPE26	MSTPE25	MSTPE24	MSTPE23	MSTPE22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MSTPE15	MSTPE14	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
13:0	—	These bits are read as 1. The write value should be 1.	R/W
14	MSTPE14	Low Power Asynchronous General Purpose Timer 5 Module Stop*1 Target module: AGT5 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Bit	Symbol	Function	R/W
15	MSTPD15	12位AD转换器1模块停止目标模块 ：ADC121 0：取消模块停止状态1：进入模块停止状态	R/W
16	MSTPD16	12位AD转换器0模块停止目标模块 ：ADC120 0：取消模块停止状态1：进入模块停止状态	R/W
19:17	—	这些位被读取为1。写入值应为1。	R/W
20	MSTPD20	12位DA转换器模块停止目标模块 ：DAC12 0：取消模块停止状态1：进入模块停止状态	R/W
21	—	该位读取为1。写入值应为1。	R/W
22	MSTPD22	温度传感器模块停止 目标模块：温度传感器 0：取消模块停止状态1：进入模块停止状态	R/W
31:23	—	这些位被读取为1。写入值应为1。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.当计数源为副时钟振荡器或LOCO时，即使MSTPD2设置为1，AGT1计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非当访问AGT1寄存器。

注2.当计数源为副时钟振荡器或LOCO时，即使MSTPD3设置为1，AGT0计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非当访问AGT0寄存器。

注3.当计数源为副时钟振荡器或LOCO时，即使MSTPD0设置为1，AGT3计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非访问AGT3寄存器时。

注4.当计数源为副时钟振荡器或LOCO时，即使MSTPD1设置为1，AGT2计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非访问AGT2寄存器时。

10.2.8 MSPCRE:模块停止控制寄存器E

Base address: MSTP = 0x4008_4000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPE31	MSTPE30	MSTPE29	MSTPE28	MSTPE27	MSTPE26	MSTPE25	MSTPE24	MSTPE23	MSTPE22	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MSTPE15	MSTPE14	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
13:0	—	这些位被读取为1。写入值应为1。	R/W
14	MSTPE14	低功耗异步通用定时器5模块停止*1 Target module: AGT5 0：取消模块停止状态1：进入模块停止状态	R/W

Bit	Symbol	Function	R/W
15	MSTPE15	Low Power Asynchronous General Purpose Timer 4 Module Stop*2 Target module: AGT4 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
21:16	—	These bits are read as 1. The write value should be 1.	R/W
22	MSTPE22	GPT9 Module Stop Target module: GPT9 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
23	MSTPE23	GPT8 Module Stop Target module: GPT8 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
24	MSTPE24	GPT7 Module Stop Target module: GPT7 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
25	MSTPE25	GPT6 Module Stop Target module: GPT6 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
26	MSTPE26	GPT5 Module Stop Target module: GPT5 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
27	MSTPE27	GPT4 Module Stop Target module: GPT4 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
28	MSTPE28	GPT3 Module Stop Target module: GPT3 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
29	MSTPE29	GPT2 Module Stop Target module: GPT2 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
30	MSTPE30	GPT1 Module Stop Target module: GPT1 0: Cancel the module-stop state 1: Enter the module-stop state	R/W
31	MSTPE31	GPT0 Module Stop Target module: GPT0 0: Cancel the module-stop state 1: Enter the module-stop state	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. When the count source is sub-clock oscillator or LOCO, AGT5 counting does not stop even if MSTPE14 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT5 registers.

Note 2. When the count source is sub-clock oscillator or LOCO, AGT4 counting does not stop even if MSTPE15 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT4 registers.

Bit	Symbol	Function	R/W
15	MSTPE15	低功耗异步通用定时器4模块停止*2 Target module: AGT4 0：取消模块停止状态1：进入模块停止状态	R/W
21:16	—	这些位被读取为1。写入值应为1。	R/W
22	MSTPE22	GPT9模块停止 Target module: GPT9 0：取消模块停止状态1：进入模块停止状态	R/W
23	MSTPE23	GPT8模块停止 Target module: GPT8 0：取消模块停止状态1：进入模块停止状态	R/W
24	MSTPE24	GPT7模块停止 Target module: GPT7 0：取消模块停止状态1：进入模块停止状态	R/W
25	MSTPE25	GPT6模块停止 Target module: GPT6 0：取消模块停止状态1：进入模块停止状态	R/W
26	MSTPE26	GPT5模块停止 Target module: GPT5 0：取消模块停止状态1：进入模块停止状态	R/W
27	MSTPE27	GPT4模块停止 Target module: GPT4 0：取消模块停止状态1：进入模块停止状态	R/W
28	MSTPE28	GPT3模块停止 Target module: GPT3 0：取消模块停止状态1：进入模块停止状态	R/W
29	MSTPE29	GPT2模块停止 Target module: GPT2 0：取消模块停止状态1：进入模块停止状态	R/W
30	MSTPE30	GPT1模块停止 Target module: GPT1 0：取消模块停止状态1：进入模块停止状态	R/W
31	MSTPE31	GPT0模块停止 Target module: GPT0 0：取消模块停止状态1：进入模块停止状态	R/W

Note: 如果安全属性配置为安全：
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：
- 允许安全和非安全访问。

注1.当计数源为副时钟振荡器或LOCO时，即使MSTPE14设置为1，AGT5计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非当访问AGT5寄存器。

注2.当计数源为副时钟振荡器或LOCO时，即使MSTPE15设置为1，AGT4计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非当访问AGT4寄存器。

RA生态工作室

10.2.9 OPCCR : Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	Operating Power Control Mode Select 0 0: High-speed mode 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Low-speed mode	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	OPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The OPCCR register is used to reduce power consumption in Normal and Sleep modes by specifying a lower operating frequency. For the procedure to change the operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

When transitioning from Software Standby mode to Normal or Snooze mode, the settings in the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction is executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal and Sleep modes. section 10.2.9. OPCCR : Operating Power Control Register shows the relationship between the operating power control modes and the OPCM[1:0] and SOPCM settings.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. This flag becomes 1 when the OPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

10.2.9 OPCCR:工作电源控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0A0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OPCM[1:0]	工作电源控制模式选择 00：高速模式01：禁止设定10：禁止设定1 1：低速模式	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	OPCMTSF	工作电源控制模式转换状态标志 0：转换完成1：转换中	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

OPCCR寄存器用于通过指定较低的工作频率来降低 正常和休眠模式下的功耗。有关更改运行功率控制模式的步骤，请参阅第10.5节。降低运行功耗的功能。

当从软件待机模式转换到正常或贪睡模式时，OPCCR.OPCM[1:0]中的设置和SOPCCR.SOPCM位如下，无论它们在进入软件待机模式之前的设置如何：

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

如果在转换到软件待机完成之前取消软件待机模式，则OPCCR.OPCM[1:0]和SOPCCR.SOPCM位保留其在执行WFI指令之前的设置。如果这导致任何问题，请设置取消软件待机模式时，MCU在异常处理过程中进入高速模式。

OPCM[1:0]位（工作电源控制模式选择）

OPCM[1:0]位选择正常和休眠模式下的工作功率控制模式。第10.2.9节。OPCCR：工作功率控制寄存器显示工作功率控制模式与OPCM[1:0]和SOPCM设置之间的关系。

OPCMTSF标志（工作电源控制模式转换状态标志）

OPCMTSF标志指示切换操作功率控制模式时的切换控制状态。该标志在OPCM位被写入时变为1，在模式转换完成时变为0。阅读此标志并确认其为0，然后再继续。

10.2.10 SOPCCR : Sub Operating Power Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x0AA

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOPCM	Sub Operating Power Control Mode Select 0: Other than Subosc-speed mode 1: Subosc-speed mode	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	SOPCMTSF	Operating Power Control Mode Transition Status Flag 0: Transition completed 1: During transition	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SOPCCR register is used to reduce power consumption in Normal mode and Sleep mode. Setting this register initiates entry to and exit from Subosc-speed mode. Subosc-speed mode is available only when using the sub-clock oscillator or LOCO without dividing the frequency.

For the procedure to change operating power control modes, see section 10.5. Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal and Sleep modes. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (operating mode set by OPCCR.OPCM[1:0]) that was active before the transition to Subosc-speed mode.

When transitioning from Software Standby mode to Normal mode or Snooze mode, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM settings are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode)

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction is executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

Table 10.4 shows the relationship between the operating power control modes, the OPCM[1:0], and SOPCM bits settings.

SOPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched to or from Subosc-speed mode. This flag becomes 1 when the SOPCM bit is written, and 0 when mode transition completes. Read this flag and confirm that it is 0 before proceeding.

Table 10.4 shows each operating power control mode.

10.2.10 SOPCCR:副操作功率控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x0AA

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SOPCMTSF	—	—	—	SOPCM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SOPCM	副工作功率控制模式选择 0：Subosc速度模式以外1：Subosc速度模式	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	SOPCMTSF	工作电源控制模式转换状态标志 0：转换完成1：转换中	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SOPCCR寄存器用于降低正常模式和休眠模式下的功耗。设置该寄存器启动进入和退出Subosc速度模式。Subosc速度模式仅在使用副时钟振荡器或LOCO而不分频时可用。

有关更改操作功率控制模式的步骤，请参阅第10.5节。降低操作功率的功能
Consumption.

SOPCM位（副工作功率控制模式选择）

SOPCM位选择正常和休眠模式下的工作功率控制模式。将此位设置为1允许转换到Subosc速度模式。将此位设置为0允许返回到转换到Subosc速度模式之前处于活动状态的操作模式（由OPCCR.OCM[1:0]设置的操作模式）。

当从软件待机模式转换到正常模式或贪睡模式时，OPCCR.OCM[1:0]和
SOPCCR.SOPCM设置如下，无论其进入软件待机模式前的设置如何：

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode)

如果在转换到软件待机完成之前取消软件待机模式，则OPCCR.OPCM[1:0]和
SOPCCR.SOPCM位保留其在执行WFI指令之前的设置。如果这导致任何问题，请设置
取消软件待机模式时，MCU在异常处理过程中进入高速模式。

表10.4显示了工作功率控制模式、OPCM[1:0]和SOPCM位设置之间的关系。

SOPCMTSF标志（工作电源控制模式转换状态标志）

SOPCMTSF标志指示当操作功率控制模式切换到或从切换控制状态
Subosc速度模式。写入SOPCM位时该标志变为1，模式转换完成时变为0。阅读此标志并确认其为0，然后再继续
。

表10.4显示了每种工作功率控制模式。

Table 10.4 Operating power control mode

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High
Low-speed mode	11b	0	↓
Subosc-speed mode	xxb	1	Low

For details about the operating frequency range, see section 53, Electrical Characteristics.

Each operating power control mode is described below.

- High-speed mode
  After a reset cancellation, the MCU is activated in this mode.
- Low-speed mode
  The following constraints apply in low-speed mode:
  – Programming and erasure operations for the flash memory are prohibited
  – Using the PLL or PLL2 is prohibited. See section 10.10.1. Register Access

  In this mode, lower power consumption is possible than in High-speed mode when the same operation is performed under the same conditions, such as operating frequency.
- Subosc-speed mode
  The following constraints apply in Subosc-speed mode:
  – Programming and erasure operations for the flash memory are prohibited
  – Reading of the data flash is prohibited
  – Using MOSC, PLL, PLL2, MOCO, or HOCO is prohibited. See section 10.10.1. Register Access
  – Using the divided clock for ICK or FCK is prohibited. See section 10.10.1. Register Access
  – Using the oscillation stop detection function of the main clock oscillator is prohibited.

  In this mode, lower power consumption is possible than in low-speed mode when the same operation is performed under the same conditions, such as operating frequency.

10.2.11 SNZCR : Snooze Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0 Snooze Request Enable 0: Ignore RXD0 falling edge in Software Standby mode 1: Detect RXD0 falling edge in Software Standby mode	R/W
1	SNZDTCEN	DTC Enable in Snooze mode 0: Disable DTC operation 1: Enable DTC operation	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W
7	SNZE	Snooze mode Enable 0: Disable Snooze mode 1: Enable Snooze mode	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

Table 10.4 工作功率控制方式

工作功率控制方式	OPCM[1:0] bits	SOPCM bit	能量消耗
High-speed mode	00b	0	High
Low-speed mode	11b	0	↓
Subosc-speed mode	xxb	1	Low

有关工作频率范围的详细信息，请参阅第53节，电气特性。

下面描述每种操作功率控制模式。

- High-speed mode
  复位取消后，MCU在此模式下激活。
- Low-speed mode
  以下约束适用于低速模式：
  禁止对闪存进行编程和擦除操作
  禁止使用PLL或PLL2。请参阅第10.10.1节。注册访问

  在这种模式下，如果在相同的条件下（例如工作频率）执行相同的操作，则可能比高速模式下的功耗更低。
- Subosc-speed mode
  以下约束适用于Subosc速度模式：
  禁止对闪存进行编程和擦除操作
  禁止读取数据闪存
  禁止使用MOSC、PLL、PLL2、MOCO或HOCO。请参阅第10.10.1节。注册访问
  禁止将分频时钟用于ICK或FCK。请参阅第10.10.1节。注册访问
  禁止使用主时钟振荡器的振荡停止检测功能。

  在这种模式下，当在相同的条件下（例如工作频率）执行相同的操作时，可以比低速模式更低的功耗。

10.2.11 SNZCR:贪睡控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RXDREQEN	RXD0贪睡请求启用 0：在软件待机模式下忽略RXD0下降沿1：在软件待机模式下检测RXD0下降沿	R/W
1	SNZDTCEN	在贪睡模式下启用DTC 0：禁用DTC操作1：启用DTC操作	R/W
6:2	—	这些位被读取为0。写入值应为0。	R/W
7	SNZE	贪睡模式启用 0：禁用贪睡模式1：启用贪睡模式	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit can be used only when SCI0 is operating in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn register.

SNZE bit (Snooze mode Enable)

The SNZE bit specifies whether to enable a transition from Software Standby mode to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, a trigger as shown in Table 10.7 in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby mode or Snooze mode to Normal mode, set 0 to the SNZE bit once then set it before re-entering Software Standby mode. For details, see section 10.8. Snooze Mode.

10.2.12 SNZEDCR0 : Snooze End Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	AD1UMTED	AD1MATED	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1 Underflow Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
1	DTCZRED	Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
3	AD0MATED	ADC120 Compare Match Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
4	AD0UMTED	ADC120 Compare Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
5	AD1MATED	ADC121 Compare Match Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
6	AD1UMTED	ADC121 Compare Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W
7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable 0: Disable the snooze end request 1: Enable the snooze end request	R/W

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

RXDREQEN位（RXD0贪睡请求使能）

RXDREQEN位指定在软件待机模式下是否检测RXD0引脚的下降沿。该位只能在SCI0工作在异步模式时使用。要检测RXD0引脚的下降沿，请在进入软件待机模式之前设置该位。当该位设置为1时，软件待机模式下RXD0引脚的下降沿会导致MCU进入贪睡模式。

SNZDTCEN位（在贪睡模式下启用DTC）

SNZDTCEN位指定是否在贪睡模式下使用DTC和SRAM。要在贪睡模式下使用DTC和SRAM，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，可以通过设置IELSRn寄存器来激活DTC。

SNZE位（贪睡模式启用）

SNZE位指定是否启用从软件待机模式到贪睡模式的转换。要使用贪睡模式，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，软件待机模式下如表10.7所示的触发会导致MCU进入贪睡模式。在MCU从软件待机模式或贪睡模式转换到正常模式后，将SNZE位设置为0一次，然后在重新进入软件待机模式之前将其设置。有关详细信息，请参阅第10.8节。贪睡模式。

10.2.12 SNZEDCR0：贪睡结束控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x094

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SCI0UMTED	AD1UMTED	AD1MATED	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGTUNFED	AGT1下溢贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
1	DTCZRED	上次DTC传输完成贪睡结束启用 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
2	DTCNZRED	不是最后一个DTC传输完成贪睡结束启用 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
3	AD0MATED	ADC120比较匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
4	AD0UMTED	ADC120比较失配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
5	AD1MATED	ADC121比较匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
6	AD1UMTED	ADC121比较失配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
7	SCI0UMTED	SCI0地址不匹配贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZEDCR0 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bitin the SNZEDCR0 register must be set to 1.

The event that is used to return from snooze mode to normal mode as shown in Table 10.3 must not be enabled in the SNZEDCR0 register.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 22, Low Power Asynchronous General Purpose Timer (AGT).

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of the last DTC transmission, that is, when CRA or CRB registers in the DTC is 0. For details on the trigger conditions, see section 17, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on completion of each DTC transmission, that is, when CRA or CRB registers in the DTC is not 0. For details on the trigger conditions, see section 17, Data Transfer Controller (DTC).

AD0MATED bit (ADC120 Compare Match Snooze End Enable)

The AD0MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD0 event when a conversion result matches the expected data. For details on the trigger conditions, see section 43, 12-Bit A/D Converter (ADC12).

AD0UMTED bit (ADC120 Compare Mismatch Snooze End Enable)

The AD0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an AD0 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 43, 12-Bit A/D Converter (ADC12).

AD1MATED bit (ADC121 Compare Match Snooze End Enable)

The AD1MATED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC121 event when a conversion result matches the expected data. For details on the trigger conditions, see section 43, 12-Bit A/D Converter (ADC12).

AD1UMTED bit (ADC121 Compare Mismatch Snooze End Enable)

The AD1UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an ADC121 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 43, 12-Bit A/D Converter (ADC12).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit specifies whether to enable a transition from Snooze mode to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 30, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 operates in asynchronous mode.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SNZEDCR0寄存器控制从贪睡模式切换到软件待机模式的条件。为了使用表10.8中所示的触发作为从贪睡模式切换到软件待机模式的条件，必须将SNZEDCR0寄存器中的相应位设置为1。

如表10.3所示用于从贪睡模式返回正常模式的事件不得在
SNZEDCR0 register.

AGTUNFED位（AGT1下溢贪睡结束使能）

AGTUNFED位指定是否在AGT1下溢时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第22节，低功耗异步通用定时器(AGT)。

DTCZRED位（最后一个DTC传输完成贪睡结束使能）

DTCZRED位指定是否在最后一次DTC传输完成时，即当DTC中的CRA或CRB寄存器为0时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第17节，数据传输控制器(DTC)。

DTCNZRED位（非最后一个DTC传输完成贪睡结束使能）

DTCNZRED位指定是否在每次DTC传输完成时启用从贪睡模式到软件待机模式的转换，即当DTC中的CRA或CRB寄存器不为0时。有关触发条件的详细信息，请参见第17节，数据传输控制器(DTC)。

AD0MATED位（ADC120比较匹配暂停结束使能）

AD0MATED位指定当转换结果与预期数据匹配时，是否在发生AD0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第43节，12位AD转换器(ADC12)。

AD0UMTED位（ADC120比较不匹配贪睡结束使能）

AD0UMTED位指定当转换结果与预期数据不匹配时，是否在发生AD0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第43节，12BitADConverter(ADC12)。

AD1MATED位（ADC121比较匹配暂停结束使能）

AD1MATED位指定当转换结果与预期数据匹配时，是否在发生ADC121事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第43节，12位AD转换器(ADC12)。

AD1UMTED位（ADC121比较不匹配贪睡结束使能）

AD1UMTED位指定当转换结果与预期数据不匹配时，是否在发生ADC121事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第43节，12BitADConverter(ADC12)。

SCI0UMTED位（SCI0地址不匹配贪睡结束使能）

SCI0UMTED位指定当在软件待机模式下接收到的地址与预期数据不匹配时，是否在发生SCI0事件时启用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第30节，串行通信接口(SCI)。仅当SCI0在异步模式下工作时将该位设置为1。

10.2.13 SNZEDCR1 : Snooze End Control Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x095

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AGT3UNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGT3UNFED	AGT3 underflow Snooze End Enable 0: Disable the Snooze End request 1: Enable the Snooze End request	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZEDCR1 register controls the condition of switching from Snooze mode to Software Standby mode. In order to use a trigger shown in Table 10.8 as a condition to switch from Snooze mode to Software Standby mode, the corresponding bit in the SNZEDCR1 register must be set to 1.

The event that is used to return from Snooze mode to normal operating mode as shown in Table 10.3 must not be enabled in the SNZEDCR1 register.

AGT3UNFED bit (AGT3 underflow Snooze End Enable)

The AGT3UNFED bit specifies whether to enable a transition from Snooze mode to Software Standby mode by an underflow of the AGT3. For the detail of the condition of the trigger, see section 22, Low Power Asynchronous General Purpose Timer (AGT).

10.2.14 SNZREQCR0 : Snooze Request Control Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SNZREQEN15	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	Enable IRQ0 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
1	SNZREQEN1	Enable IRQ1 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W

10.2.13 SNZEDCR1：贪睡结束控制寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x095

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AGT3UNFED
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGT3UNFED	AGT3下溢贪睡结束使能 0：禁用贪睡结束请求1：启用贪睡结束请求	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SNZEDCR1寄存器控制从贪睡模式切换到软件待机模式的条件。为了使用表10.8中所示的触发作为从贪睡模式切换到软件待机模式的条件，必须将SNZEDCR1寄存器中的相应位设置为1。

不得在SNZEDCR1寄存器中启用用于从贪睡模式返回到正常操作模式的事件，如表10.3所示。

AGT3UNFED位（AGT3下溢贪睡结束使能）

AGT3UNFED位指定是否通过AGT3的下溢来使能从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参见第22节，低功耗异步通用定时器(AGT)。

10.2.14 SNZREQCR0:贪睡请求控制寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SNZREQEN15	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	启用IRQ0引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
1	SNZREQEN1	启用IRQ1引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W

Bit	Symbol	Function	R/W
2	SNZREQEN2	Enable IRQ2 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
3	SNZREQEN3	Enable IRQ3 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
4	SNZREQEN4	Enable IRQ4 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
5	SNZREQEN5	Enable IRQ5 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
6	SNZREQEN6	Enable IRQ6 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
7	SNZREQEN7	Enable IRQ7 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
8	SNZREQEN8	Enable IRQ8 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
9	SNZREQEN9	Enable IRQ9 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
10	SNZREQEN10	Enable IRQ10 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
11	SNZREQEN11	Enable IRQ11 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
12	SNZREQEN12	Enable IRQ12 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
13	SNZREQEN13	Enable IRQ13 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
14	SNZREQEN14	Enable IRQ14 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
15	SNZREQEN15	Enable IRQ15 pin snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
23:16	—	These bits are read as 0. The write value should be 0.	R/W
24	SNZREQEN24	Enable RTC alarm snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
25	SNZREQEN25	Enable RTC period snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
27:26	—	These bits are read as 0. The write value should be 0.	R/W
28	SNZREQEN28	Enable AGT1 underflow snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W

Bit	Symbol	Function	R/W
2	SNZREQEN2	启用IRQ2引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
3	SNZREQEN3	启用IRQ3引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
4	SNZREQEN4	启用IRQ4引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
5	SNZREQEN5	启用IRQ5引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
6	SNZREQEN6	启用IRQ6引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
7	SNZREQEN7	启用IRQ7引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
8	SNZREQEN8	启用IRQ8引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
9	SNZREQEN9	启用IRQ9引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
10	SNZREQEN10	启用IRQ10引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
11	SNZREQEN11	启用IRQ11引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
12	SNZREQEN12	启用IRQ12引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
13	SNZREQEN13	启用IRQ13引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
14	SNZREQEN14	启用IRQ14引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
15	SNZREQEN15	启用IRQ15引脚贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
23:16	—	这些位被读取为0。写入值应为0。	R/W
24	SNZREQEN24	启用RTC闹钟暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
25	SNZREQEN25	启用RTC周期暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
27:26	—	这些位被读取为0。写入值应为0。	R/W
28	SNZREQEN28	启用AGT1下溢暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W

Bit	Symbol	Function	R/W
29	SNZREQEN29	Enable AGT1 compare match A snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
30	SNZREQEN30	Enable AGT1 compare match B snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZREQCR0 register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPENn register, see section 13, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the SNZREQCR0 is 1. The setting of the WUPENn register always has higher priority than the setting of the SNZREQCR0 register. For details, see section 10.8. Snooze Mode and section 13, Interrupt Controller Unit (ICU).

10.2.15 SNZREQCR1 : Snooze Request Control Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	Enable AGT3 underflow snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
1	SNZREQEN1	Enable AGT3 compare match A snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
2	SNZREQEN2	Enable AGT3 compare match B snooze request 0: Disable the snooze request 1: Enable the snooze request	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The SNZREQCR1 register controls which trigger causes the MCU to switch from Software Standby mode to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode by setting the WUPENn register, see section 13, Interrupt Controller Unit (ICU), the MCU enters Normal mode when the trigger is generated while the associated bit of the

Bit	Symbol	Function	R/W
29	SNZREQEN29	启用AGT1比较匹配贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
30	SNZREQEN30	启用AGT1比较匹配B贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
31	—	该位读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SNZREQCR0寄存器控制哪个触发器导致MCU从软件待机模式切换到贪睡模式。如果通过设置WUPENn寄存器选择触发作为取消软件待机模式的请求，请参见第13节，
中断控制器单元（ICU），当触发产生时MCU进入正常模式，而相关位
SNZREQCR0为1。WUPENn寄存器的设置总是比SNZREQCR0寄存器的设置具有更高的优先级。有关详细信息，请参阅第10.8节。贪睡模式和第13节，中断控制器单元(ICU)。

10.2.15 SNZREQCR1：贪睡请求控制寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SNZREQEN0	启用AGT3下溢暂停请求 0：禁用贪睡请求1：启用贪睡请求	R/W
1	SNZREQEN1	启用AGT3比较匹配贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
2	SNZREQEN2	启用AGT3比较匹配B贪睡请求 0：禁用贪睡请求1：启用贪睡请求	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

SNZREQCR1寄存器控制哪个触发器导致MCU从软件待机模式切换到贪睡模式。如果通过设置WUPENn寄存器选择触发作为取消软件待机模式的请求，请参见第13节，
中断控制器单元（ICU），当触发产生时MCU进入正常模式，而相关位

SNZREQCR1 is 1. The setting of the WUPENn register always has higher priority than the setting of the SNZREQCR1 register. For details, see section 10.8. Snooze Mode and section 13, Interrupt Controller Unit (ICU).

10.2.16 DPSBYCR : Deep Standby Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x400

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	DEEPCUT[1:0]	Power-Supply Control 0 0: Power to the standby RAM, Low-speed on-chip oscillator, AGTn (n = 0 to 3), and USBFS/USBHS resume detecting unit is supplied in Deep Software Standby mode. 0 1: Power to the standby RAM, Low-speed on-chip oscillator, AGT, and USBFS/ USBHS resume detecting unit is not supplied in Deep Software Standby mode. 1 0: Setting prohibited 1 1: Power to the standby RAM, Low-speed on-chip oscillator, AGT, and USBFS/ USBHS resume detecting unit is not supplied in Deep Software Standby mode. In addition, LVD is disabled and the low power function in a power-on reset circuit is enabled.	R/W
5:2	—	These bits are read as 0. The write value should be 0.	R/W
6	IOKEEP	I/O Port Rentention 0: When the Deep Software Standby mode is canceled, the I/O ports are in the reset state. 1: When the Deep Software Standby mode is canceled, the I/O ports are in the same state as in the Deep Software Standby mode.	R/W
7	DPSBY	Deep Software Standby 0: Sleep mode (SBYCR.SSBY=0) / Software Standby mode (SBYCR.SSBY=1) 1: Sleep mode (SBYCR.SSBY=0) / Deep Software Standby mode (SBYCR.SSBY=1)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The DPSBYCR register controls the Deep Software Standby mode.

DPSBYCR is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

DEEPCUT[1:0] bit (Power-Supply Control)

The DEEPCUT[1:0] bits control the internal power supply to the standby RAM, Low-speed on-chip oscillator, AGT, and USBFS/USBHS resume detecting unit in Deep Software Standby mode. In addition, these bits control the state of LVD and power-on reset circuit in Deep Software Standby mode.

When a USBFS/USBHS suspend/resume interrupt is used as a Deep Software Standby mode Cancelling source, the DEEPCUT[1:0] bits must be set to 00b.

When an LVD interrupt is used in Deep Software Standby mode, the DEEPCUT[1:0] bits must be set to 00b or 01b.

For lower power consumption, set the DEEPCUT[1:0] bits to 11b so that the LVD is stopped and the low power consumption function of the power-on reset circuit is enabled.

Regardless of the DEEPCUT [1: 0] bit setting, during deep software standby mode, internal power supply to SRAM other than standby SRAM is stopped.

SNZREQCR1为1。WUPENn寄存器的设置总是比SNZREQCR1寄存器的设置具有更高的优先级。有关详细信息，请参阅第10.8节。贪睡模式和第13节，中断控制器单元(ICU)。

10.2.16 DPSBYCR：深度待机控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x400

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	DEEPCUT[1:0]	Power-Supply Control 00：为待机RAM、低速片上振荡器、AGTn（n=0至3）和USBFS供电USBHS恢复检测单元在深度软件待机模式下供电。 01：为待机RAM、低速片上振荡器、AGT和USBFS供电USBHS恢复检测单元在深度软件待机模式下不供电。 10：禁止设置11：给待机RAM、低速内部振荡器、AGT和USBFS供电 在深度软件待机模式下不提供USBHS恢复检测单元。此外，LVD被禁用，上电复位电路中的低功耗功能被启用。	R/W
5:2	—	这些位被读取为0。写入值应为0。	R/W
6	IOKEEP	I/O Port Rentention 0：取消深度软件待机模式时，IO口处于复位状态。 1：当深度软件待机模式取消时，IO端口处于与深度软件待机模式相同的状态。	R/W
7	DPSBY	深度软件待机 0：休眠模式（SBYCR.SSBY=0）软件待机模式(SBYCR.SSBY=1) 1：休眠模式（SBYCR.SSBY=0）深度软件待机模式(SBYCR.SSBY=1)	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSBYCR寄存器控制深度软件待机模式。

DPSBYCR不会由作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

DEEPCUT[1:0] bit (Power-Supply Control)

DEEPCUT[1:0]位控制待机RAM、低速片上振荡器、AGT和USBFSUSBHS在深度软件待机模式下恢复检测单元。此外，这些位在深度软件待机模式下控制LVD和上电复位电路的状态。

当USBFSUSBHS挂起恢复中断用作深度软件待机模式取消源时，DEEPCUT[1:0]位必须设置为00b。

在深度软件待机模式下使用LVD中断时，DEEPCUT[1:0]位必须设置为00b或01b。

为降低功耗，将DEEPCUT[1:0]位设置为11b，使LVD停止并启用上电复位电路的低功耗功能。

无论DEEPCUT[1:0]位设置如何，在深度软件待机模式下，除待机SRAM之外的SRAM内部电源都会停止。

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When a deep standby mode is used, set DPSWCR.WTSTS bits depending on the value of DEEPCUT[1] before entering Deep Software Standby mode.

IOKEEP bit (I/O Port Rentention)

In Deep Software Standby mode, I/O ports keep the same states as in the Software Standby mode. The IOKEEP bit specifies whether to reset the state of the I/O ports or not when the Deep Software Standby mode is canceled.

DPSBY bit (Deep Software Standby)

The DPSBY bit controls transitions to Deep Software Standby mode.

When the WFI instruction is executed while SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both 1, the MCU enters Deep Software Standby mode through Software Standby mode.

The DPSBY bit remains 1 when Deep Software Standby mode is canceled by certain pins which are sources of external pin interrupts (NMI, IRQ0-DS to IRQ15-DS) or a peripheral interrupt (RTC alarm, RTC interval, USB suspend/resume, voltage monitor 1, or voltage monitor 2). Write 0 to this bit to clear it.

The DPSBY bit setting is invalid when OFS0.IWDTSTPCTL bit is 0 (counting continues) regardless of the setting in OFS0.IWDTSTRT bit. In that case, even when SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WFI instruction is to Software Standby mode.

The setting of the DPSBY bit is invalid when voltage monitor 1 reset is enabled (LVD1CR0.RI = 1) or when a voltage monitor 2 reset is enabled (LVD2CR0.RI = 1). In this case, even when the SBYCR.SSBY bit is 1 and the DPSBY bit is 1, the transition after the execution of a WFI instruction is to Software Standby mode.

10.2.17 DPSWCR : Deep Standby Wait Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x401

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	WTSTS[5:0]					
Value after reset:	0	0	0	1	1	0	0	1

Bit	Symbol	Function	R/W
5:0	WTSTS[5:0]	Deep Software Wait Standby Time Setting Bit 0x0E: Wait cycle for fast recovery 0x19: Wait cycle for slow recovery Others: Setting prohibited	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The DPSWCR register sets the wait stabilization time when a Deep Software Standby mode is canceled by certain pins that are the sources of external pin interrupts or a peripheral interrupt such as RTC alarm, RTC interval, and USB suspend/resume.

During a wait stabilization period set in this register, a Deep Software Standby reset occurs, and the MCU is initialized.

The DPSWCR register is not initialized with the internal reset signal by the cancellation of the Deep Software Standby mode. For details, see section 5, Resets.

When a deep standby mode is used, set DPSWCR.WTSTS bits according to the value of DPSBYCR.DEEPCUT[1] before entering Deep Software Standby mode.

When DPSBYCR.DEEPCUT[1]=0, you can set DPSWCR.WTSTS to the wait cycle for fast recovery.

When DPSBYCR.DEEPCUT[1]=1, you must set DPSWCR.WTSTS to the wait cycle for slow recovery.

当使用深度待机模式时，在进入之前根据DEEPCUT[1]的值设置DPSWCR.WTSTS位
深度软件待机模式。

IOKEEP位（IO端口保留）

在深度软件待机模式下，IO端口保持与软件待机模式相同的状态。IOKEEP位指定当深度软件待机模式被取消时是否复位IO端口的状态。

DPSBY位（深度软件待机）

DPSBY位控制向深度软件待机模式的转换。

当SBYCR.SSBY位和DPSBYCR.DPSBY位均为1时执行WFI指令，MCU进入
深度软件待机模式到软件待机模式。

当某些引脚取消深度软件待机模式时，DPSBY位保持为1，这些引脚是外部引脚中断（NMI、IRQ0-DS至IRQ15-DS）或外设中断（RTC警报、RTC间隔、USB暂停恢复、电压监控器）的来源1，或电压监视器2)。向该位写入0以清除它。

无论OFS0.IWDTSTRT位的设置如何，当OFS0.IWDTSTPCL位为0（继续计数）时，DPSBY位设置无效。在这种情况下，即使SBYCR.SSBY位为1且DPSBY位为1，在执行WFI指令后转换为软件待机模式。

当使能电压监视器1复位(LVD1CR0.RI=1)或使能电压监视器2复位(LVD2CR0.RI=1)时，DPSBY位的设置无效。在这种情况下，即使SBYCR.SSBY位为1且DPSBY位为1，在执行WFI指令后转换为软件待机模式。

10.2.17 DPSWCR：深度待机等待控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x401

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	WTSTS[5:0]					
重置后的值：	0	0	0	1	1	0	0	1

Bit	Symbol	Function	R/W
5:0	WTSTS[5:0]	深度软件等待待机时间设置位 0x0E：快速恢复的等待周期0x19： 慢速恢复的等待周期 其他：禁止设置	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSWCR寄存器设置当某个引脚取消深度软件待机模式时的等待稳定时间，这些引脚是外部引脚中断或外设中断（如RTC警报、RTC间隔和USB挂起恢复）的源。

在此寄存器中设置的等待稳定期间，会发生深度软件待机复位，并且初始化MCU。

通过取消深度软件待机模式，DPSWCR寄存器不会使用内部复位信号进行初始化。有关详细信息，请参阅第5节，重置。

当使用深度待机模式时，在进入深度软件待机模式之前，根据DPSBYCR.DEEPCUT[1]的值设置DPSWCR.WTSTS位。

当DPSBYCR.DEEPCUT[1]=0时，可以设置DPSWCR.WTSTS为等待周期，以便快速恢复。

当DPSBYCR.DEEPCUT[1]=1时，必须将DPSWCR.WTSTS设置为等待周期，以便缓慢恢复。

10.2.18 DPSIER0 : Deep Standby Interrupt Enable Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x402

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0E	IRQ0-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DIRQ1E	IRQ1-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
2	DIRQ2E	IRQ2-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3	DIRQ3E	IRQ3-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
4	DIRQ4E	IRQ4-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
5	DIRQ5E	IRQ5-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
6	DIRQ6E	IRQ6-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
7	DIRQ7E	IRQ7-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER0 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER0 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR0 being set to 1. Therefore, DPSIFR0 should be cleared to 0 before entering Deep Software Standby mode.

10.2.19 DPSIER1 : Deep Standby Interrupt Enable Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x403

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15E	DIRQ14E	DIRQ13E	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
Value after reset:	0	0	0	0	0	0	0	0

10.2.18 DPSIER0：深度待机中断使能寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x402

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0E	IRQ0-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
1	DIRQ1E	IRQ1-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
2	DIRQ2E	IRQ2-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
3	DIRQ3E	IRQ3-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
4	DIRQ4E	IRQ4-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
5	DIRQ5E	IRQ5-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
6	DIRQ6E	IRQ6-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
7	DIRQ7E	IRQ7-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIER0未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER0的设置后，可能会在内部产生一个边沿，具体取决于引脚的状态，导致DPSIFR0被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR0清零。

10.2.19 DPSIER1：深度待机中断使能寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x403

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15E	DIRQ14E	DIRQ13E	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8E	IRQ8-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DIRQ9E	IRQ9-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
2	DIRQ10E	IRQ10-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
3	DIRQ11E	IRQ11-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
4	DIRQ12E	IRQ12-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
5	DIRQ13E	IRQ13-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
6	DIRQ14E	IRQ14-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
7	DIRQ15E	IRQ15-DS Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER1 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER1 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR1 being set to 1. Therefore, DPSIFR1 should be cleared to 0 before entering Deep Software Standby mode.

10.2.20 DPSIER2 : Deep Standby Interrupt Enable Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x404

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIE	DRTCAIE	DRTCIIE	DLVD2IE	DLVD1IE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IE	LVD1 Deep Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
1	DLVD2IE	LVD2 Deep Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
2	DRTCIIE	RTC Interval interrupt Deep Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W

Bit	Symbol	Function	R/W
0	DIRQ8E	IRQ8-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
1	DIRQ9E	IRQ9-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
2	DIRQ10E	IRQ10-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
3	DIRQ11E	IRQ11-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
4	DIRQ12E	IRQ12-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
5	DIRQ13E	IRQ13-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
6	DIRQ14E	IRQ14-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
7	DIRQ15E	IRQ15-DS引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIER1未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER1的设置后，可能会在内部产生一个边沿，具体取决于引脚的状态，导致DPSIFR1被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR1清零。

10.2.20 DPSIER2：深度待机中断使能寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x404

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIE	DRTCAIE	DRTCIIE	DLVD2IE	DLVD1IE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IE	LVD1深度待机取消信号使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
1	DLVD2IE	LVD2深度待机取消信号使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
2	DRTCIIE	RTC间隔中断深度待机取消信号使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W

Bit	Symbol	Function	R/W
3	DRTCAIE	RTC Alarm interrupt Deep Standby Cancel Signal Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W
4	DNMIE	NMI Pin Enable 0: Cancelling Deep Software Standby mode is disabled 1: Cancelling Deep Software Standby mode is enabled	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. 1 can be written only once. Once 1 is written to this bit, subsequent write accesses are disabled.

DPSIER2 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER2 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR2 being set to 1. Therefore, DPSIFR2 should be cleared to 0 before entering Deep Software Standby mode.

10.2.21 DPSIER3 : Deep Standby Interrupt Enable Register 3

Base address: SYSC = 0x4001_E000

Offset address: 0x405

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DAGT3IE	DAGT1IE	DUSBHSIE	DUSBFS0IE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DUSBFS0IE	USBFS0 Suspend/Resume Deep Standby Cancel Signal Enable 0: Cancelling deep standby mode is disabled 1: Cancelling deep standby mode is enabled	R/W
1	DUSBHSIE	USBHS Suspend/Resume Deep Standby Cancel Signal Enable 0: Cancelling deep standby mode is disabled 1: Cancelling deep standby mode is enabled	R/W
2	DAGT1IE	AGT1 Underflow Deep Standby Cancel Signal Enable 0: Cancelling deep standby mode is disabled 1: Cancelling deep standby mode is enabled	R/W
3	DAGT3IE	AGT3 Underflow Deep Standby Cancel Signal Enable 0: Cancelling deep standby mode is disabled 1: Cancelling deep standby mode is enabled	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIER3 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

After the setting of DPSIER3 is modified, an edge may be internally generated depending on the state of the pin, resulting in DPSIFR3 being set to 1. Therefore, DPSIFR3 should be cleared to 0 before entering Deep Software Standby mode.

Bit	Symbol	Function	R/W
3	DRTCAIE	RTC闹钟中断深度待机取消信号使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W
4	DNMIE	NMI引脚使能 0：禁用取消深度软件待机模式1：启用取消深度软件待机模式	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。
注1.1只能写一次。一旦向该位写入1，随后的写访问将被禁用。

DPSIER2未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER2的设置后，可能会根据引脚的状态在内部产生一个边沿，从而导致DPSIFR2被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR2清除为0。

10.2.21 DPSIER3：深度待机中断使能寄存器3

Base address: SYSC = 0x4001_E000

Offset address: 0x405

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DAGT3IE	DAGT1IE	DUSBHSIE	DUSBFS0IE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DUSBFS0IE	USBFS0暂停恢复深度待机取消信号使能 0：禁用取消深度待机模式1：启用取消深度待机模式	R/W
1	DUSBHSIE	USBHS暂停恢复深度待机取消信号使能 0：禁用取消深度待机模式1：启用取消深度待机模式	R/W
2	DAGT1IE	AGT1下溢深度待机取消信号使能 0：禁用取消深度待机模式1：启用取消深度待机模式	R/W
3	DAGT3IE	AGT3下溢深度待机取消信号使能 0：禁用取消深度待机模式1：启用取消深度待机模式	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIER3未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

修改DPSIER3的设置后，根据引脚的状态，可能会在内部产生一个边沿，导致DPSIFR3被设置为1。因此，在进入深度软件待机模式之前，应将DPSIFR3清零。

10.2.22 DPSIFR0 : Deep Standby Interrupt Flag Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x406

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0F	IRQ0-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DIRQ1F	IRQ1-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DIRQ2F	IRQ2-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3	DIRQ3F	IRQ3-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
4	DIRQ4F	IRQ4-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
5	DIRQ5F	IRQ5-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
6	DIRQ6F	IRQ6-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7	DIRQ7F	IRQ7-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR0 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER0 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR0 is cleared to 0x00.

To clear DPSIFR0 to 0x00 after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0.

DPSIFR0 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. To clear DPSIFR0 to 0x00 after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. Six or more PCLKB cycles can be secured, for example, by reading DPSIER0. For details, see section 5, Resets.

DIRQnF flag (IRQn-DS Pin Deep Standby Cancel Flag) (n = 0 to 7)

The DIRQnF flag indicates that a cancel request by the IRQn-DS pin has been generated.

[Setting condition]

10.2.22 DPSIFR0：深度待机中断标志寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x406

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0F	IRQ0-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
1	DIRQ1F	IRQ1-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
2	DIRQ2F	IRQ2-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
3	DIRQ3F	IRQ3-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
4	DIRQ4F	IRQ4-DS引脚深度待机取消标志 0：不产生取消请求 1：生成取消请求	R/W
5	DIRQ5F	IRQ5-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
6	DIRQ6F	IRQ6-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
7	DIRQ7F	IRQ7-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成由DPSIEGR0指定的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER0的设置时，每个标志都可以设置为1。因此，应在DPSIFR0清零后转换到深度软件待机模式。

要在修改DPSIER0后将DPSIFR0清为0x00，请等待至少6个PCLKB周期，读取DPSIFR0，然后将0写入DPSIFR0。例如，可以通过读取DPSIER0来确保六个或更多PCLKB周期。

DPSIFR0不被用作深度软件待机模式取消源的内部复位信号初始化。清除修改DPSIER0后DPSIFR0到0x00，等待至少6个PCLKB周期，读取DPSIFR0，然后写入0到DPSIFR0。例如，可以通过读取DPSIER0来确保六个或更多PCLKB周期。有关详细信息，请参阅第5节，重置。

DIRQnF标志（IRQn-DS引脚深度待机取消标志）（n=0至7）

DIRQnF标志表示已生成IRQn-DS引脚的取消请求。

[Setting condition]

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A cancel request by the IRQn-DS pin specified by DPSIEGR0 is generated.

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.23 DPSIFR1 : Deep Standby Interrupt Flag Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x407

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15F	DIRQ14F	DIRQ13F	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8F	IRQ8-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DIRQ9F	IRQ9-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DIRQ10F	IRQ10-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3	DIRQ11F	IRQ11-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
4	DIRQ12F	IRQ12-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
5	DIRQ13F	IRQ13-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
6	DIRQ14F	IRQ14-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7	DIRQ15F	IRQ15-DS Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR1 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER1 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR1 is cleared to 0x00.

To clear DPSIFR1 to 0x00 after modifying DPSIER1, wait for at least 6 PCLKB cycles, read DPSIFR1, and then write 0 to DPSIFR1. Six or more PCLKB cycles can be secured, for example, by reading DPSIER1.

DPSIFR1 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

由DPSIEGR0指定的IRQn-DS引脚产生一个取消请求。

[Clearing condition]

读取1后将0写入每个标志。

10.2.23 DPSIFR1：深度待机中断标志寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x407

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15F	DIRQ14F	DIRQ13F	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8F	IRQ8-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
1	DIRQ9F	IRQ9-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
2	DIRQ10F	IRQ10-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
3	DIRQ11F	IRQ11-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
4	DIRQ12F	IRQ12-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
5	DIRQ13F	IRQ13-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
6	DIRQ14F	IRQ14-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
7	DIRQ15F	IRQ15-DS引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成由DPSIEGR1指定的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER1的设置时，每个标志都可以设置为1。因此，应在DPSIFR1被清除为0x00后转换到深度软件待机模式。

修改DPSIER1后要清除DPSIFR1为0x00，至少等待6个PCLKB周期，读取DPSIFR1，然后将0写入DPSIFR1。例如，可以通过读取DPSIER1来确保六个或更多PCLKB周期。

DPSIFR1未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

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DIRQnF flag (IRQn-DS Pin Deep Standby Cancel Flag) (n = 8 to 15)

The DIRQnF flag indicates that a cancel request by the IRQn-DS pin has been generated.

[Setting condition]

A cancel request by the IRQn-DS pin specified by DPSIEGR1 is generated.

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.24 DPSIFR2 : Deep Standby Interrupt Flag Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x408

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIF	DRTCAIF	DRTCIIF	DLVD2IF	DLVD1IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IF	LVD1 Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
1	DLVD2IF	LVD2 Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DRTCIIF	RTC Interval Interrupt Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
3	DRTCAIF	RTC Alarm Interrupt Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
4	DNMIF	NMI Pin Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when a cancel request specified by DPSIEGR2 is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER2 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR2 is cleared to 0x00.

To clear DPSIFR2 to 0x00 after modifying DPSIER2, wait for at least 6 PCLKB cycles, read DPSIFR2, and then write 0 to DPSIFR2. Six or more PCLKB cycles can be secured, for example, by reading DPSIER2.

DPSIFR2 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

DLVDmIF flag (LVDm Deep Standby Cancel Flag) (m = 1 to 2)

The DLVDmIF flag indicates that a cancel request by the voltage monitor m signal has been generated.

[Setting condition]

DIRQnF标志（IRQn-DS引脚深度待机取消标志）（n=8到15）

DIRQnF标志表示已生成IRQn-DS引脚的取消请求。

[Setting condition]

由DPSIEGR1指定的IRQn-DS引脚产生取消请求。

[Clearing condition]

读取1后将0写入每个标志。

10.2.24 DPSIFR2：深度待机中断标志寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x408

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIF	DRTCAIF	DRTCIIF	DLVD2IF	DLVD1IF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1IF	LVD1深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
1	DLVD2IF	LVD2深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
2	DRTCIIF	RTC间隔中断深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
3	DRTCAIF	RTC警报中断深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
4	DNMIF	NMI引脚深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成由DPSIEGR2指定的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER2的设置时，每个标志都可以设置为1。因此，应在DPSIFR2清零为0x00后转换到深度软件待机模式。

要在修改DPSIER2后将DPSIFR2清为0x00，请等待至少6个PCLKB周期，读取DPSIFR2，然后将0写入DPSIFR2。例如，可以通过读取DPSIER2来确保六个或更多PCLKB周期。

DPSIFR2未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

DLVDmIF标志（LVDm深度待机取消标志）（m=1到2）

DLVDmIF标志表示电压监视器m信号的取消请求已经产生。

[Setting condition]

A cancel request is generated by the voltage monitor m signal that is selected in DPSIEGR2.

[Clearing condition]

Writing 0 to each flag after 1 is read.

DRTCIIF flag (RTC Interval Interrupt Deep Standby Cancel Flag)

This flag indicates that a cancel request by the RTC interval interrupt signal has been generated.

[Setting condition]

A cancel request by the RTC interval interrupt signal is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

DRTCAIF flag (RTC Alarm Interrupt Deep Standby Cancel Flag)

This flag indicates that a cancel request by the RTC alarm interrupt signal has been generated.

[Setting condition]

A cancel request by the RTC alarm interrupt signal is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

DNMIF flag (NMI Pin Deep Standby Cancel Flag)

This flag indicates that a cancel request by the NMI pin has been generated.

[Setting condition]

A cancel request by the NMI pin specified by DPSIEGR2 is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

10.2.25 DPSIFR3 : Deep Standby Interrupt Flag Register 3

Base address: SYSC = 0x4001_E000

Offset address: 0x409

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DAGT 3IF	DAGT 1IF	DUSB HSIF	DUSB FS0IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DUSBFS0IF	USBFS0 Suspend/Resume Deep Standby Cancel Flag 0: The cancel request is not generated. 1: The cancel request is generated.	R/W
1	DUSBHSIF	USBHS Suspend/Resume Deep Standby Cancel Flag 0: The cancel request is not generated 1: The cancel request is generated	R/W
2	DAGT1IF	AGT1 Underflow Deep Standby Cancel Flag 0: The cancel request is not generated. 1: The cancel request is generated.	R/W
3	DAGT3IF	AGT3 Underflow Deep Standby Cancel Flag 0: The cancel request is not generated. 1: The cancel request is generated.	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed

取消请求由DPSIEGR2中选择的电压监视器m信号生成。

[Clearing condition]

读取1后将0写入每个标志。

DRTCIIF标志（RTC间隔中断深度待机取消标志）

该标志表示已经产生了RTC间隔中断信号的取消请求。

[Setting condition]

由RTC间隔中断信号产生一个取消请求

[Clearing condition]

读取1后将0写入每个标志。

DRTCAIF标志（RTC警报中断深度待机取消标志）

该标志表示已经产生了RTC警报中断信号的取消请求。

[Setting condition]

由RTC报警中断信号产生一个取消请求

[Clearing condition]

读取1后将0写入每个标志。

DNMIF标志（NMI引脚深度待机取消标志）

该标志表示已生成NMI引脚的取消请求。

[Setting condition]

由DPSIEGR2指定的NMI引脚生成取消请求

[Clearing condition]

读取1后将0写入每个标志。

10.2.25 DPSIFR3：深度待机中断标志寄存器3

Base address: SYSC = 0x4001_E000

Offset address: 0x409

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	DAGT 3IF	DAGT 1IF	DUSB HSIF	DUSB FS0IF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DUSBFS0IF	USBFS0暂停恢复深度待机取消标志 0：不产生取消请求。1：产生取消请求 。	R/W
1	DUSBHSIF	USBHS暂停恢复深度待机取消标志 0：不产生取消请求1：产生取消请求	R/W
2	DAGT1IF	AGT1下溢深度待机取消标志 0：不产生取消请求。1：产生取消请求 。	R/W
3	DAGT3IF	AGT3下溢深度待机取消标志 0：不产生取消请求。1：产生取消请求 。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问

- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note: Writing 0 clears the flag. Writing 1 is ignored.
Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Each flag is set to 1 when the corresponding cancel request is generated.

Each flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode) or when the setting of DPSIER3 is modified. Therefore, a transition to Deep Software Standby mode should be made after DPSIFR3 is cleared to 0x00.

To clear DPSIFR3 to 0x00 after modifying DPSIER3, wait for at least 6 PCLKB cycles, read DPSIFR3, and then write 0 to DPSIFR3. Six or more PCLKB cycles can be secured, for example, by reading DPSIER3.

DPSIFR3 is not initialized by the internal reset signal used as Deep Software Standby mode Cancelling source. For details, see section 5, Resets.

DUSBFS0IF flag (USBFS0 Suspend/Resume Deep Standby Cancel Flag)

The DUSBFS0IF flag is the flag for USBFS0 that indicates that a cancel request by the USBFS0 suspend/resume has been generated.

[Setting condition]

A cancel request by the USBFS0 suspend/resume is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

DUSBHSIF bit (USBHS Suspend/Resume Deep Standby Cancel Flag)

This flag indicates that a cancel request by the USBHS suspend/resume has been generated.

[Setting condition]

A cancel request by the USBHS suspend/resume is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

DAGT1IF flag (AGT1 Underflow Deep Standby Cancel Flag)

This flag indicates that a cancel request by the AGT1 underflow has been generated.

[Setting condition]

A cancel request by the AGT1 underflow is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

DAGT3IF flag (AGT3 Underflow Deep Standby Cancel Flag)

This flag indicates that a cancel request by the AGT3 underflow has been generated.

[Setting condition]

A cancel request by the AGT3 underflow is generated

[Clearing condition]

Writing 0 to each flag after 1 is read.

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 写入0清除标志。写入1被忽略。
Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

当生成相应的取消请求时，每个标志都设置为1。

当在任何模式下（不仅在深度软件待机模式下）生成取消请求或修改DPSIER3的设置时，每个标志都可以设置为1。因此，应在DPSIFR3被清除为0x00后转换到深度软件待机模式。

修改DPSIER3后要清除DPSIFR3为0x00，等待至少6个PCLKB周期，读取DPSIFR3，然后将0写入DPSIFR3.例如，可以通过读取DPSIER3来确保六个或更多PCLKB周期。

DPSIFR3未被用作深度软件待机模式取消源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

DUSBFS0IF标志（USBFS0暂停恢复深度待机取消标志）

DUSBFS0IF标志是USBFS0的标志，指示USBFS0暂停恢复的取消请求已生成。

[Setting condition]

USBFS0暂停恢复的取消请求产生

[Clearing condition]

读取1后将0写入每个标志。

DUSBHSIF位（USBHS暂停恢复深度待机取消标志）

该标志表示已生成USBHS暂停恢复的取消请求。

[Setting condition]

USBHS暂停恢复的取消请求产生

[Clearing condition]

读取1后将0写入每个标志。

DAGT1IF标志（AGT1下溢深度待机取消标志）

该标志表示已经产生了AGT1下溢的取消请求。

[Setting condition]

产生AGT1下溢的取消请求

[Clearing condition]

读取1后将0写入每个标志。

DAGT3IF标志（AGT3下溢深度待机取消标志）

该标志表示已经产生了AGT3下溢的取消请求。

[Setting condition]

生成AGT3下溢的取消请求

[Clearing condition]

读取1后将0写入每个标志。

10.2.26 DPSIEGR0 : Deep Standby Interrupt Edge Register 0

Base address: SYSC = 0x4001_E000

Offset address: 0x40A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0EG	IRQ0-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
1	DIRQ1EG	IRQ1-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
2	DIRQ2EG	IRQ2-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
3	DIRQ3EG	IRQ3-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
4	DIRQ4EG	IRQ4-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
5	DIRQ5EG	IRQ5-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
6	DIRQ6EG	IRQ6-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W
7	DIRQ7EG	IRQ7-DS Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR0 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.27 DPSIEGR1 : Deep Standby Interrupt Edge Register 1

Base address: SYSC = 0x4001_E000

Offset address: 0x40B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15EG	DIRQ14EG	DIRQ13EG	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
Value after reset:	0	0	0	0	0	0	0	0

10.2.26 DPSIEGR0：深度待机中断边沿寄存器0

Base address: SYSC = 0x4001_E000

Offset address: 0x40A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ0EG	IRQ0-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
1	DIRQ1EG	IRQ1-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
2	DIRQ2EG	IRQ2-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
3	DIRQ3EG	IRQ3-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
4	DIRQ4EG	IRQ4-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
5	DIRQ5EG	IRQ5-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
6	DIRQ6EG	IRQ6-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W
7	DIRQ7EG	IRQ7-DS引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIEGR0不会被作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

10.2.27 DPSIEGR1：深度待机中断边沿寄存器1

Base address: SYSC = 0x4001_E000

Offset address: 0x40B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DIRQ15EG	DIRQ14EG	DIRQ13EG	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DIRQ8EG	IRQ8-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
1	DIRQ9EG	IRQ9-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
2	DIRQ10EG	IRQ10-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge	R/W
3	DIRQ11EG	IRQ11-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
4	DIRQ12EG	IRQ12-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
5	DIRQ13EG	IRQ13-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
6	DIRQ14EG	IRQ14-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W
7	DIRQ15EG	IRQ15-DS Pin Edge Select 0: A cancel request is generated at a falling edge. 1: A cancel request is generated at a rising edge.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR1 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.28 DPSIEGR2 : Deep Standby Interrupt Edge Register 2

Base address: SYSC = 0x4001_E000

Offset address: 0x40C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1EG	LVD1 Edge Select 0: A cancel request is generated when VCC < V_{det1} (fall) is detected 1: A cancel request is generated when VCC ≥ V_{det1} (rise) is detected	R/W
1	DLVD2EG	LVD2 Edge Select 0: A cancel request is generated when VCC < V_{det2} (fall) is detected 1: A cancel request is generated when VCC ≥ V_{det2} (rise) is detected	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DNMIEG	NMI Pin Edge Select 0: A cancel request is generated at a falling edge 1: A cancel request is generated at a rising edge	R/W

Bit	Symbol	Function	R/W
0	DIRQ8EG	IRQ8-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
1	DIRQ9EG	IRQ9-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
2	DIRQ10EG	IRQ10-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求	R/W
3	DIRQ11EG	IRQ11-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
4	DIRQ12EG	IRQ12-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
5	DIRQ13EG	IRQ13-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
6	DIRQ14EG	IRQ14-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W
7	DIRQ15EG	IRQ15-DS引脚边沿选择 0：在下降沿产生取消请求。1：在上升沿产生取消请求。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIEGR1不会被作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

10.2.28 DPSIEGR2：深度待机中断边沿寄存器2

Base address: SYSC = 0x4001_E000

Offset address: 0x40C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DLVD1EG	LVD1边沿选择 0：检测到VCC<Vdet1（下降）时产生取消请求1：检测到VCC≥Vdet1（上升）时产生取消请求	R/W
1	DLVD2EG	LVD2边沿选择 0：检测到VCC<Vdet2（下降）时产生取消请求1：检测到VCC≥Vdet2（上升）时产生取消请求	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	DNMIEG	NMI引脚边沿选择 0：下降沿产生取消请求1：上升沿产生取消请求	R/W

Bit	Symbol	Function	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

DPSIEGR2 is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode. For details, see section 5, Resets.

10.2.29 SYOCDCR : System Control OCD Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	DOCDF
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	DOCDF	Deep Software Standby OCD flag 0: DBIRQ is not generated 1: DBIRQ is generated	R/W*1
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	DBGEN	Debugger Enable bit Set to 1 first in on-chip debug mode. 0: On-chip debugger is disabled 1: On-chip debugger is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.
Note 1. Writing 0 clears the flag. Writing 1 is ignored

This register is not controlled by any security attribute register (eg. LPMSAR, DPFSAR).

SYOCDCR can be written when DBGSTR.CDBGPWRUPREQ = 1 (the debugger is connected).

SYOCDCR is not initialized by the internal reset signal that is the source to cancel the Deep Software Standby mode.

DOCDF flag (Deep Software Standby OCD flag)

DOCDF flag indicates that a cancel request of Deep Software Standby mode by the MCUCTRL.DBIRQ bit has been generated. DOCDF flag is set to 1 when a cancel request is generated. This flag may be set to 1 when a cancel request is generated in any mode (not only in Deep Software Standby mode). Therefore, a transition to Deep Software Standby mode must be made after DOCDF flag is cleared to 0.

[Setting condition]

- A cancel request by the MCUCTRL.DBIRQ is generated

[Clearing condition]

- Writing 0 to the flag after reading the bit as 1
- When DBGEN bit is 0

DBGEN bit (Debugger Enable bit)

The DBGEN bit enables the on-chip debug mode. This bit must be set to 1 first in the on-chip debugger mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

Bit	Symbol	Function	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

DPSIEGR2不会由作为取消深度软件待机模式的源的内部复位信号初始化。有关详细信息，请参阅第5节，重置。

10.2.29 SOOCDCR:系统控制OCD控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x040E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DBGEN	—	—	—	—	—	—	DOCDF
重置后的值：	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	DOCDF	深度软件待机OCD标志 0：不产生DBIRQ1：产生DBIRQ	R/W*1
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	DBGEN	调试器使能位 在片上调试模式下首先设置为1。 0：禁用片上调试器1：启用片上调试器	R/W

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。
注1.写入0清除标志。写1被忽略

该寄存器不受任何安全属性寄存器（例如LPMSAR、DPFSAR）的控制。

当DBGSTR.CDBGPWRUPREQ=1（调试器已连接）时，可以写入SOOCDCR。

SOOCDCR不会由作为取消深度软件待机模式的源的内部复位信号初始化。

DOCDF标志（深度软件待机OCD标志）

DOCDF标志指示已通过MCUCTRL.DBIRQ位生成了深度软件待机模式的取消请求。生成取消请求时，DOCDF标志设置为1。当在任何模式下（不仅在深度软件待机模式下）生成取消请求时，此标志可能设置为1。因此，必须在DOCDF标志清零后转换到深度软件待机模式。

[Setting condition]

●MCUCTRL.DBIRQ产生取消请求

[Clearing condition]

●读取位为1后向标志位写入0

●DBGEN位为0时

DBGEN位（调试器启用位）

DBGEN位使能片上调试模式。在片上调试器模式下，该位必须首先设置为1。

[Setting condition]

●连接调试器时向该位写入1。

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

Note: Certain restrictions apply in terms of the MCU states in which the DBGEN bit can be set to 1. For details, see section 2.13.2. Restrictions on Connecting an OCD emulator.

10.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency changes when the SCKDIVCR register is set.

For information on module and clock associations, see section 8.2.2. SCKDIVCR : System Clock Division Control Register.

10.4 Module-Stop Function

The module stop function can stop the clock supply set for each peripheral module.

When the MSTPmi bit (m = A to E, i = 31 to 0) in MSTPCRn (n = A to E) is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Setting the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle.

After a reset is canceled, all modules other than the DMAC, DTC and SRAMn modules are placed in the module-stop state. Do not access the module while the corresponding MSTPmi bit is 1. Additionally, do not set 1 to the MSTPmi bit while the corresponding module is accessed.

When the PLL is selected as the clock source, MSTPmi bits must be changed only one bit at a time. In this case, wait at least 250 ns after changing each MSTPmi bit before starting subsequent processing if you change any of the following bits:

MSTPB12(USBHS), MSTPC31 (SCE9).

The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

10.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power consumption control mode according to the operating frequency, power consumption can be reduced in Normal mode and Sleep mode.

10.5.1 Setting Operating Power Control Mode

Ensure the operating condition such as the frequency range is always within the specified range before and after switching the operating power control modes.

This section provides example procedures for switching operating power control modes.

Table 10.5 Available oscillators in each mode

Mode	Oscillator						
	PLL, PLL2	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

(1) Switching from a higher power mode to a lower power mode

Example 1: From High-speed mode to Low-speed mode:

(Operation begins in High-speed mode)

1. Change the oscillator to what is used in Low-speed mode. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.

[Clearing condition]

●产生上电复位

●向该位写入0。

Note: 某些限制适用于可以将DBGEN位设置为1的MCU状态。有关详细信息，请参阅第2.13.2节。连接强迫症模拟器的限制。

10.3 通过切换时钟信号降低功耗

设置SCKDIVCR寄存器时，时钟频率会发生变化。

有关模块和时钟关联的信息，请参见第8.2.2节。SCKDIVCR:系统时钟分频控制Register.

10.4 Module-Stop Function

模块停止功能可以停止为每个外围模块设置的时钟供应。

当MSTPCRn(n=AtoE)中的MSTPmi位(m=AtoE i=31to0)设置为1时，指定模块停止运行并进入module-stop状态，但CPU继续运行独立。将MSTPmi位设置为0可取消模块停止状态，允许模块在总线周期结束时恢复运行。

取消复位后，除DMAC、DTC和SRAMn模块之外的所有模块都置于模块停止状态。相应的MSTPmi位为1时不要访问模块。另外，访问相应的模块时不要将MSTPmi位设置为1。

WhenthePLLisselectedastheclocksource MSTPmibitsmustbechangedonlyonebitatatime.在这种情况下，如果更改以下任何位，请在更改每个MSTPmi位后至少等待250ns，然后再开始后续处理：

MSTPB12(USBHS), MSTPC31 (SCE9).

测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

10.5 降低运行功耗的功能

通过根据工作频率选择合适的工作功耗控制模式，可以降低正常模式和睡眠模式下的功耗。

10.5.1 设置工作电源控制模式

确保在切换工作功率控制模式前后，频率范围等工作条件始终在规定范围内。

本节提供切换操作电源控制模式的示例程序。

Table 10.5 每种模式下可用的振荡器

Mode	Oscillator						
	PLL, PLL2	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	主时钟振荡器	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

(1) 从高功率模式切换到低功率模式

示例1：从高速模式到低速模式：

（以高速模式开始运行）

1.将振荡器更改为低速模式下使用的振荡器。将每个时钟的频率设置为低于低速模式下的最大工作频率。

2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM[1:0] bits to 11b (Low-speed mode).
5. Confirm that OPCCR.OPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Low-speed mode)

Example 2: From High-speed mode to Subosc-speed mode

(Operation begins in High-speed mode)

1. Switch the clock source to sub-clock oscillator. Turn off PLL, PLL2, HOCO, MOCO, LOCO and main oscillator.
2. Confirm that all clock sources other than the sub-clock oscillator are stopped.
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
5. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).

(Operation is now in Subosc-speed mode)

(2) Switching from a lower power mode to a higher power mode

Example 1: From Subosc-speed mode to High-speed mode

(Operation begins in Subosc-speed mode)

1. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
2. Set the SOPCCR.SOPCM bit to 0 (High-speed mode).
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Turn on the required oscillator in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

(Operation is now in High-speed mode)

Example 2: From Low-speed mode to High-speed mode

(Operation begins in Low-speed mode)

1. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
2. Set the OPCCR.OPCM[1:0] bits to 00b (High-speed mode).
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Turn on any required oscillator in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

(Operation is now in High-speed mode)

10.6 Sleep Mode

10.6.1 Transitioning to Sleep Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 13, Interrupt Controller Unit (ICU).

2.关闭低速模式下不需要的振荡器。
3.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
4.将OPCCR.OPCM[1:0]位设置为11b（低速模式）。
5.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

（操作现在处于低速模式）

示例2：从高速模式到Subosc速度模式

（以高速模式开始运行）

1.将时钟源切换为副时钟振荡器。关闭PLL、PLL2、HOCO、MOCO、LOCO和主振荡器。
2.确认除副时钟振荡器之外的所有时钟源都已停止。
3.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
4.将SOPCCR.SOPCM位设置为1（Subosc速度模式）。
5.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。

（操作现在处于Subosc速度模式）

(2) 从低功耗模式切换到高功耗模式

示例1：从Subosc速度模式到高速模式

（以Subosc速度模式开始运行）

1.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
2.将SOPCCR.SOPCM位设置为0（高速模式）。
3.确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
4.在高速模式下打开所需的振荡器。
5.将每个时钟的频率设置为低于高速模式的最大工作频率。

（操作现在处于高速模式）

示例2：从低速模式到高速模式

（以低速模式开始运行）

1.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
2.将OPCCR.OPCM[1:0]位设置为00b（高速模式）。
3.确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
4.在高速模式下打开任何需要的振荡器。
5.将每个时钟的频率设置为低于高速模式的最大工作频率。

（操作现在处于高速模式）

10.6 睡眠模式

10.6.1 转换到睡眠模式

当SBYCR.SSBY位为0时执行WFI指令，MCU进入休眠模式。在这种模式下，CPU停止运行，但其内部寄存器的内容被保留。其他外围功能不会停止。休眠模式下可用的复位或中断会导致MCU取消休眠模式。所有中断源均可用。如果使用中断取消休眠模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

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Counting by IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep mode, Software Standby mode or Snooze mode).

Counting by IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby mode or Snooze mode).

Counting by WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). Similarly, counting by WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 1 (WDT stops in Sleep mode).

Counting by WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). Similarly, counting by WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

10.6.2 Canceling Sleep Mode

Sleep mode is canceled by:

- An interrupt
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- An SRAM parity error reset
- An SRAM ECC error reset
- A bus master MPU error reset
- A TrustZone error reset
- A reset caused by an IWDT or a WDT underflow

The operations are as follows:

1. Canceling by an interrupt
   When an available interrupt request is generated, Sleep mode is canceled and the MCU starts the interrupt handling.
2. Canceling by RES pin reset
   When the RES pin is driven low, the MCU enters the reset state. Be sure to keep the RES pin low for the time period specified in section 53, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by IWDT reset
   - Sleep mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
4. Canceling by WDT reset
   Sleep mode is canceled by an internal reset generated by a WDT underflow and the MCU starts the reset exception handling. However, WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated in the following conditions:
   - OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
   - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
5. Canceling by other resets available in Sleep mode
   Sleep mode is canceled by other resets and the MCU starts the reset exception handling.

Note: For details on proper setting of the interrupts, see section 13, Interrupt Controller Unit (ICU).

当MCU进入休眠模式且IWDT处于自动启动模式且
OFS0.IWDTSTPCL位为1（IWDT在休眠模式、软件待机模式或贪睡模式下停止）。

当MCU进入休眠模式且IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为0（IWDT在休眠模式、软件待机模式或贪睡模式下不停止）时，IWDT继续计数。

当MCU进入休眠模式且WDT处于自动启动模式且
OFS0.WDTSTPCTL位为1（WDT在休眠模式下停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为1（WDT在休眠模式下停止）时，WDT停止计数。

当MCU进入休眠模式且WDT处于自动启动模式且
OFS0.WDTSTPCTL位为0（WDT在休眠模式下不停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为0（休眠模式下WDT不会停止）时，WDT继续计数。

10.6.2 取消睡眠模式

睡眠模式通过以下方式取消：

●中断
●ARES引脚复位
- A power-on reset
●电压监视器复位
●SRAM奇偶校验错误复位
●SRAMECC错误复位
●总线主控MPU错误复位
●TrustZone错误重置
●IWDT或WDT下溢引起的复位

操作如下：

1.中断取消
当产生可用的中断请求时，休眠模式被取消，MCU开始中断处理。

2.通过RES引脚复位取消
当RES引脚驱动为低电平时，MCU进入复位状态。请务必在第53节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。

3.IWDT复位取消

●休眠模式由IWDT下溢产生的内部复位取消，MCU开始复位
异常处理。但是，IWDT在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：

- OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

4.WDT复位取消
睡眠模式由WDT下溢产生的内部复位取消，MCU启动复位异常处理。但是，即使在正常模式下计数，WDT也会在休眠模式下停止，并且在以下情况下不会产生用于取消休眠模式的内部复位：

●OFS0.WDTSTRT=0（自动启动模式）和OFS0.WDTSTPCTL=1
●OFS0.WDTSTRT=1（寄存器启动模式）和WDTCSTPR.SLCSTP=1。

5.通过睡眠模式下可用的其他复位取消
休眠模式被其他复位取消，MCU开始复位异常处理。

Note: 有关正确设置中断的详细信息，请参阅第13节，中断控制器单元(ICU)。

10.7 Software Standby Mode

10.7.1 Transitioning to Software Standby Mode

When a WFI instruction is executed while SBYCR.SSBY bit is 1 and DPSBYCR.DPSBY bit is 0, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions and the oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O ports are retained. Software Standby mode allows significant reduction in power consumption because most of the oscillators stops in this mode. Table 10.2 shows the status of each on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode make the MCU to cancel Software Standby mode. See Table 10.3 for available interrupt sources and section 13.2.18. WUPEN0 : Wake Up Interrupt Enable Register 0, section 13.2.19. WUPEN1 : Wake Up interrupt enable register 1 for information on waking up the MCU from Software Standby mode. If using an interrupt to cancel an interrupt, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 13, Interrupt Controller Unit (ICU).

The status of address bus and bus control signals in Software Standby mode can be selected by SBYCR.OPE bit.

Clear DMAST.DMST bit and DTCST.DTCST bit to 0 before executing WFI instruction except when using DTC in Snooze mode. If DTC is required in Snooze mode, set DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by the IWDT stops if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep, Software Standby or Snooze mode).

Counting by the IWDT continues if the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep, Software Standby or Snooze mode).

WDT stops counting when the MCU enters Software Standby mode because the PCLKB stops.

Do not enter Software Standby mode while OSTDCR.OSTDE = 1 (oscillation stop detection function is enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE = 0). In case of executing WFI instruction while OSTDCR.OSTDE = 1, the MCU enters Sleep mode even if SBYCR.SSBY = 1.

Do not enter Software Standby mode while the flash memory is programming or erasing. To enter Software Standby mode, execute a WFI instruction after programming or erasing procedure completes.

When the PLL is selected as the clock source, set the following modules to the module-stop state before executing a WFI instruction:

USBHS, SCE9.

In this case, you must also insert a wait time of at least 750 ns before executing the WFI instruction. The recommended method to measure the wait time is through software. Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

10.7 软件待机模式

10.7.1 过渡到软件待机模式

当SBYCR.SSBY位为1且DPSBYCR.DPSBY位为0时执行WFI指令，MCU进入软件待机模式。在这种模式下，CPU、大部分片上外围功能和振荡器停止。但是，CPU内部寄存器和SRAM数据的内容、片上外围功能的状态和IO端口的状态会被保留。软件待机模式可显着降低功耗，因为大多数振荡器在此模式下停止。表10.2显示了每个片上外围功能和振荡器的状态。软件待机模式下可用的复位或中断使MCU取消软件待机模式。有关可用的中断源，请参见表10.3和第13.2.18节。WUPEN0：唤醒中断使能寄存器0，第13.2.19节。WUPEN1：唤醒中断使能寄存器1，用于将MCU从软件待机模式唤醒的信息。如果使用中断取消中断，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

软件待机模式下地址总线和总线控制信号的状态可以通过SBYCR.OPE位来选择。

在执行WFI指令之前将DMAST.DMST位和DTCST.DTCST位清除为0，除非在贪睡模式下使用DTC。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

如果MCU进入软件待机模式，而IWDT处于自动启动模式并且OFS0.IWDTSTPCTL位为1（IWDT在休眠、软件待机或贪睡模式下停止）。

如果MCU进入软件待机模式，而IWDT处于自动启动模式并且OFS0.IWDTSTPCTL位为0（IWDT在休眠、软件待机或贪睡模式下不停止）。

当MCU进入软件待机模式时，WDT停止计数，因为PCLKB停止。

OSTDCR.OSTDE=1时不要进入软件待机模式（振荡停止检测功能启用）。要进入软件待机模式，请在禁用振荡停止检测功能(OSTDCR.OSTDE=0)后执行WFI指令。如果在OSTDCR.OSTDE=1时执行WFI指令，即使SBYCR.SSBY=1，MCU也会进入休眠模式。

闪存正在编程或擦除时，请勿进入软件待机模式。要进入软件待机模式，请在编程或擦除过程完成后执行WFI指令。

WhenthePLLisselectedastheclocksource setthefollowingmodulestothemodule-stopstatebeforeexecutingaWFIinstruction:

USBHS, SCE9.

在这种情况下，您还必须在执行WFI指令之前插入至少750ns的等待时间。测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

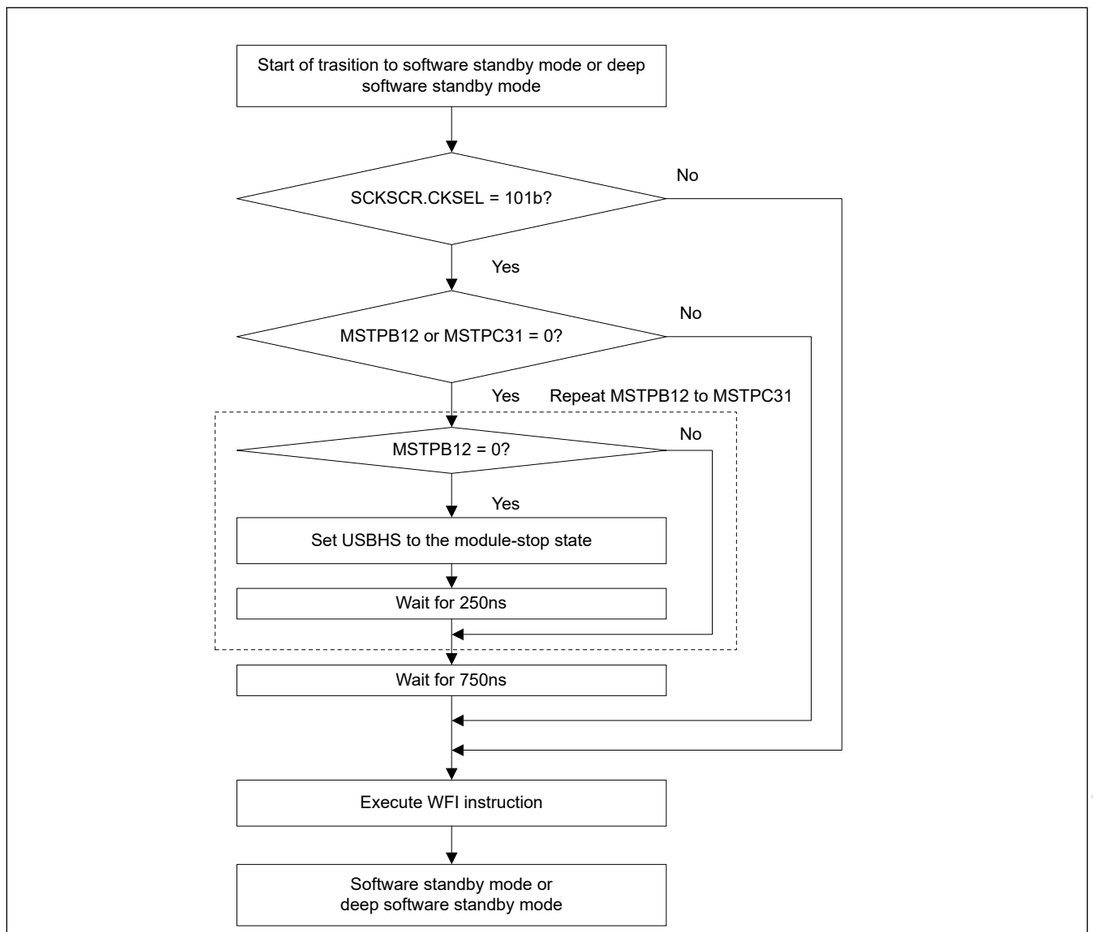


Figure 10.2 Example flow for transition to software standby mode or deep software standby mode

Table 10.6 shows the setting of the related control bits and the modes to enter after executing WFI instruction.

Table 10.6 Bit settings that affect modes when executing a WFI instruction (1 of 2)

		SBYCR.SSBY and PSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1			Sleep	Sleep
FENTRYR.FENTRYC FENTRYR.FENTRYD	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1			Sleep	Sleep
OFS0.IWDTSTPCTL	0	Sleep	Sleep	Software Standby	Software Standby
	1				Deep Software Standby
LVD1CR0.RI	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1				Software Standby

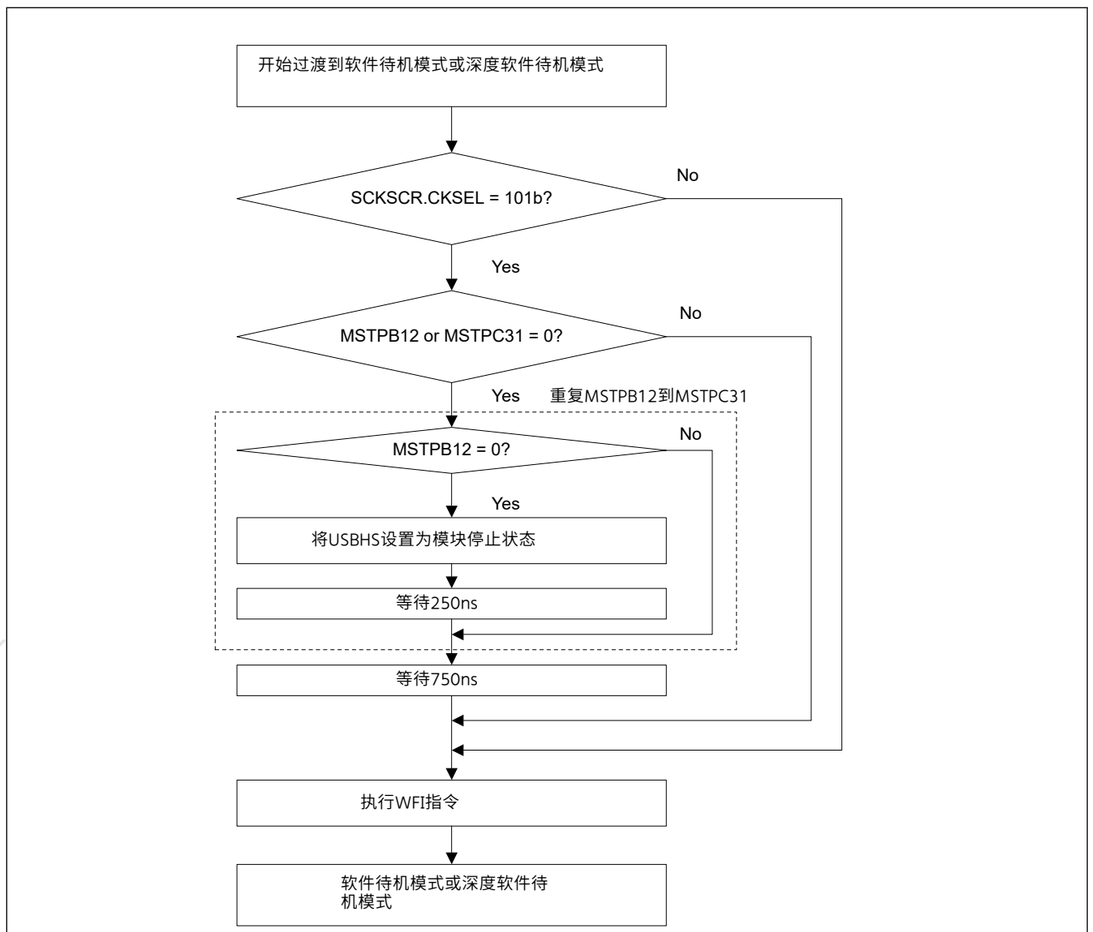


Figure 10.2 转换到软件待机模式或深度软件待机模式的示例流程

表10.6显示了相关控制位的设置以及执行WFI指令后进入的模式。

Table 10.6 执行WFI指令时影响模式的位设置(1of2)

		SBYCR.SSBY和PSBYCR.DPSBY位设置			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep	Sleep	软件待机	深度软件待机
	1			Sleep	Sleep
FENTRYR.FENTRYC FENTRYR.FENTRYD	0	Sleep	Sleep	软件待机	深度软件待机
	1			Sleep	Sleep
OFS0.IWDTSTPCTL	0	Sleep	Sleep	软件待机	软件待机
	1				深度软件待机
LVD1CR0.RI	0	Sleep	Sleep	软件待机	深度软件待机
	1				软件待机

Table 10.6 Bit settings that affect modes when executing a WFI instruction (2 of 2)

		SBYCR.SSBY and PSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
LVD2CR0.RI	0	Sleep	Sleep	Software Standby	Deep Software Standby
	1				Software Standby

10.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby mode, the oscillators that operate before the transition to the mode restart. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 13.2.18. WUPEN0 : Wake Up Interrupt Enable Register 0, section 13.2.19. WUPEN1 : Wake Up interrupt enable register 1 for information on how to wake up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

1. Canceling by an interrupt
When an available interrupt request (see Table 10.3) is generated, an oscillator that operates before the transition to Software Standby mode restarts. After all the oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode and starts the interrupt handling.
When the PLL is selected as the clock source, you must insert a wait time of at least 250 ns at the beginning of the interrupt handling. The recommended method to measure the wait time is through software.
Be sure to consider the worst-case conditions to ensure that the required wait time elapses.

Table 10.6 执行WFI指令时影响模式的位设置(2of2)

		SBYCR.SSBY和PSBYCR.DPSBY位设置			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
LVD2CR0.RI	0	Sleep	Sleep	软件待机	深度软件待机
	1				软件待机

10.7.2 取消软件待机模式

软件待机模式通过以下方式取消：

●可用中断如表10.3所示

●ARES引脚复位

- A power-on reset

●电压监视器复位

●IWDT下溢引起的复位。

在退出软件待机模式时，在转换到模式之前工作的振荡器会重新启动。在所有振荡器稳定后，MCU从软件待机模式返回到正常模式。请参阅第13.2.18节。WUPEN0：唤醒中断使能寄存器0，第13.2.19节。WUPEN1：唤醒中断使能寄存器1，用于了解如何将MCU从软件待机模式唤醒。

您可以通过以下任一方式取消软件待机模式：

1.中断取消
当一个可用的中断请求（见表10.3）产生时，一个振荡器在转换到
软件待机模式重新启动。在所有振荡器稳定后，MCU从软件返回到正常模式
待机模式并启动中断处理。
WhenthePLLisselectedastheclocksource youmustinsertawaittimeofatleast250nsatthebeginningoftheinterrupthandling.测量等待时间的推荐方法是通过软件。请务必考虑最坏情况，以确保经过所需的等待时间。

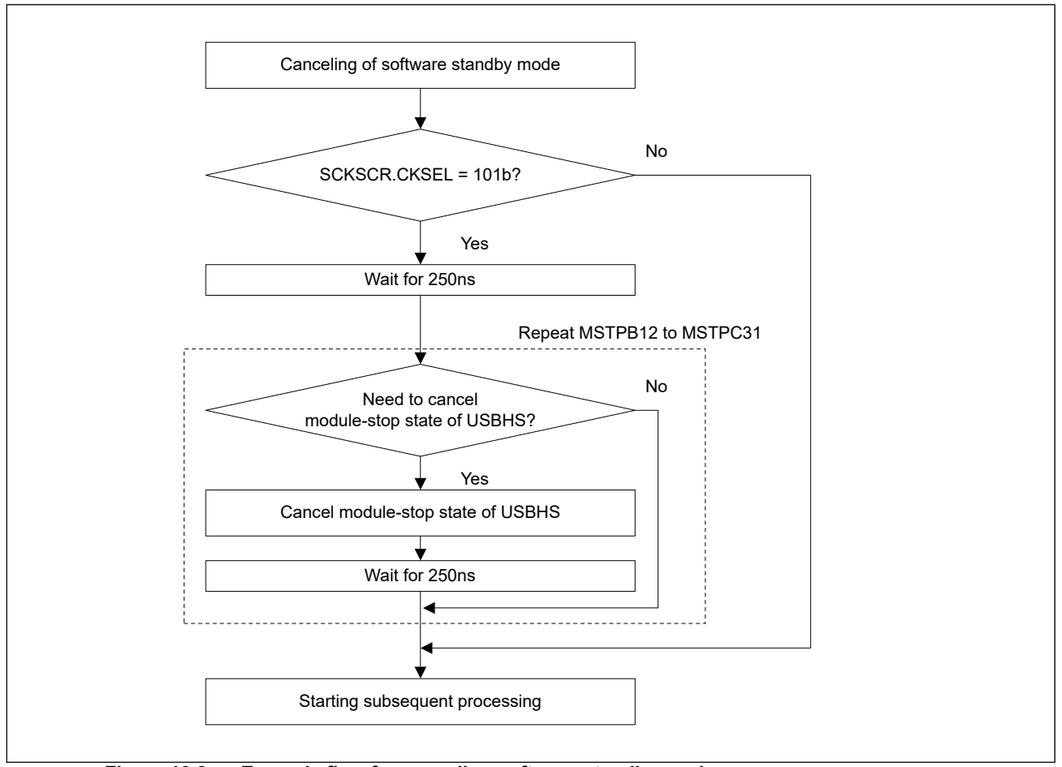


Figure 10.3 Example flow for canceling software standby mode

2. Canceling by a RES pin reset
   When the RES pin is driven low, the MCU enters the reset state, and the oscillators whose default status is operating, start the oscillation. Be sure to keep the RES pin low for the time period specified in section 53, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts the reset exception handling.
3. Canceling by a power-on reset
   Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.
4. Canceling by a voltage monitor reset
   Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
5. Canceling by IWDT reset
   Software Standby mode is canceled by an internal reset generated by an IWDT underflow and the MCU starts the reset exception handling. However, IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following condition:
   - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 Example of Software Standby Mode Application

Figure 10.4 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode by a rising edge of the IRQn pin.

In this example, an IRQn pin interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge) in Normal mode, and the IRQCRi.IRQMD[1:0] bits are set to 01b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

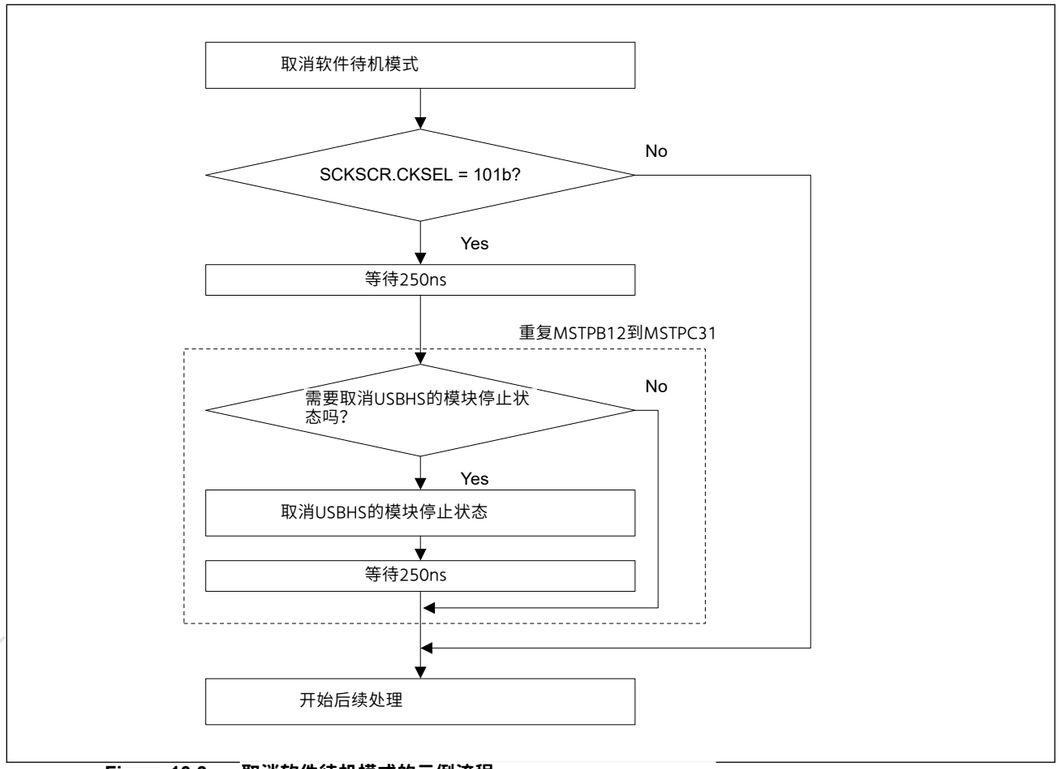


Figure 10.3 取消软件待机模式的示例流程

2.通过RES引脚复位取消
当RES引脚驱动为低电平时，MCU进入复位状态，默认状态为工作的振荡器开始振荡。请务必在第53节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。

3.上电复位取消
软件待机模式通过上电复位取消，MCU启动复位异常处理。

4.通过电压监视器复位取消
软件待机模式通过电压检测电路的电压监视器复位取消，MCU开始复位异常处理。

5.IWDT复位取消
软件待机模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。但是，IWDT在软件待机模式下停止，并且在以下情况下不会产生用于取消软件待机模式的内部复位：

- OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.

10.7.3 软件待机模式应用示例

图10.4显示了在检测到IRQn引脚的下降沿进入软件待机模式并在IRQn引脚的上升沿退出软件待机模式的示例。

在此示例中，接受IRQn引脚中断，同时ICU的IRQCRi.IRQMD[1:0]位设置为00b（下降沿）正常模式，并且IRQCRi.IRQMD[1:0]位设置为01b（上升沿）。之后，SBYCR.SSBY位设置为1并执行WFI指令。因此，软件待机模式的进入完成，软件待机模式的退出由IRQn引脚的上升沿启动。

Setting the ICU is also required to exit Software Standby mode. For details, see section 13, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 10.4 is specified in section 53, Electrical Characteristics.

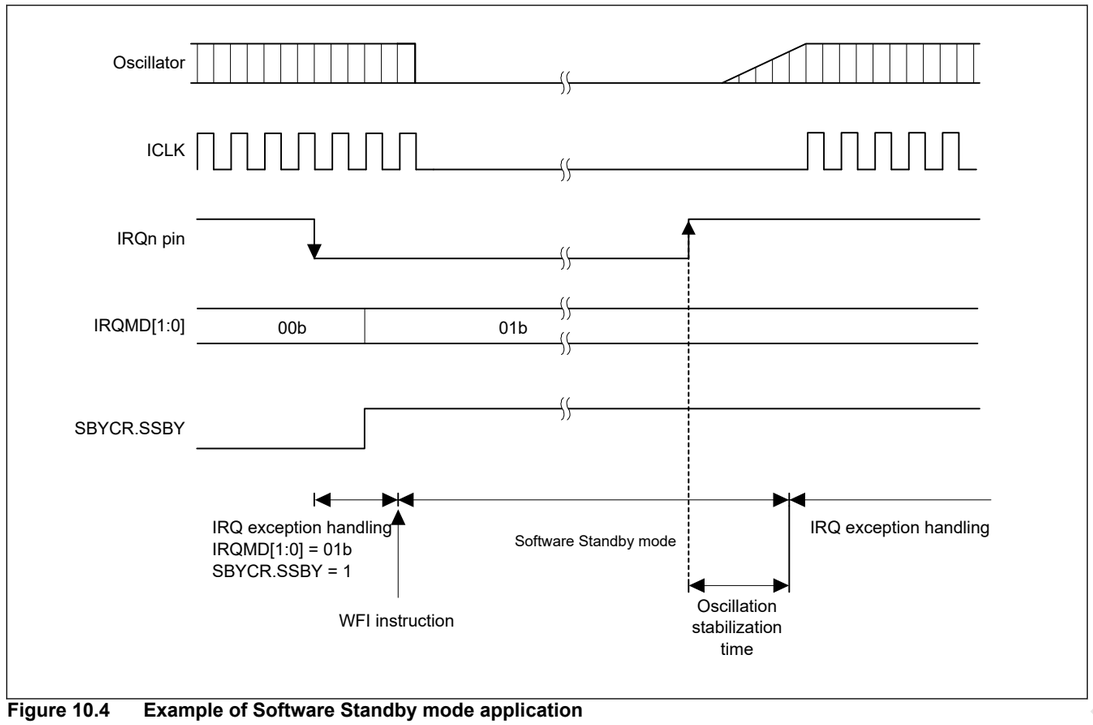


Figure 10.4 Example of Software Standby mode application

10.8 Snooze Mode

10.8.1 Transition to Snooze Mode

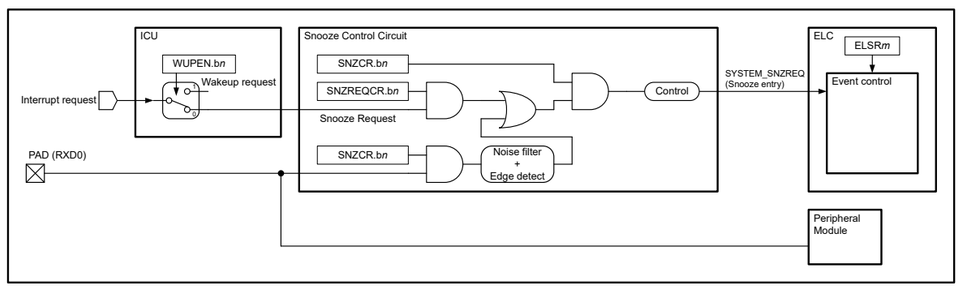


Figure 10.5 Snooze mode entry configuration

When the snooze control circuit accepts an available snooze request in Software Standby mode, the MCU transfers to Snooze mode. In this mode, some peripheral modules operates without waking the CPU. The peripheral modules that can operate in Snooze mode are shown in Table 10.2. Also, DTC operation in Snooze mode can be selected by the setting of SNZCR.SNZDTCEN bit.

退出软件待机模式也需要设置ICU。有关详细信息，请参阅第13节，中断控制器单元(ICU)。
图10.4中的振荡稳定时间在第53节"电气特性"中指定。

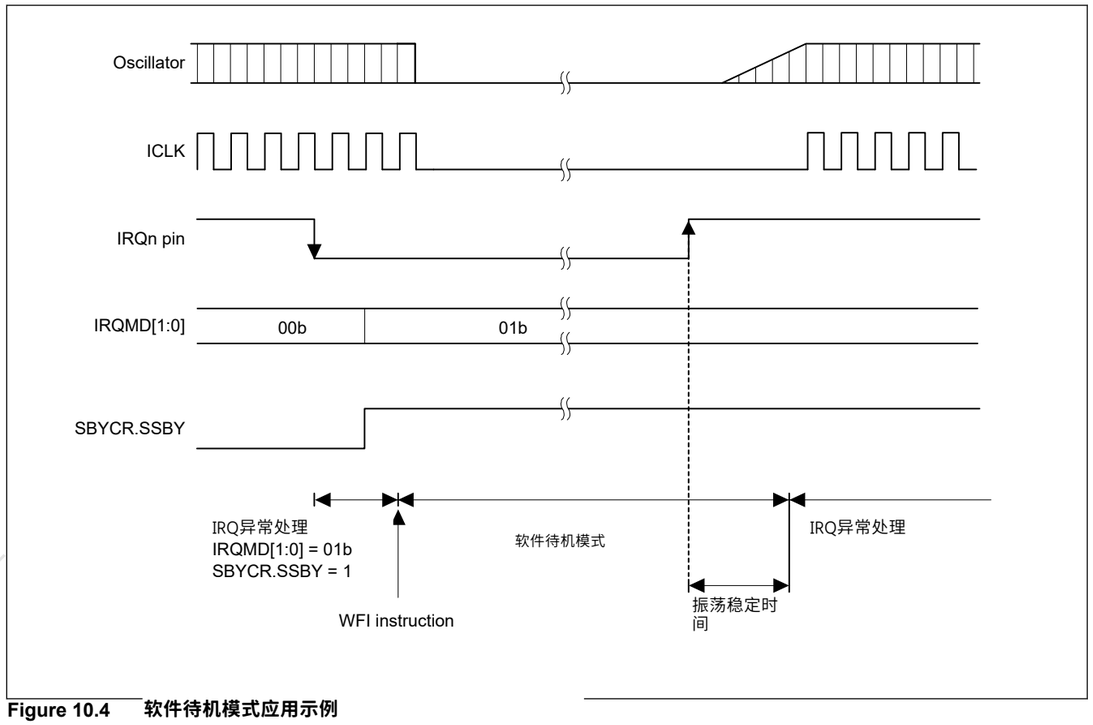


Figure 10.4 软件待机模式应用示例

10.8 贪睡模式

10.8.1 过渡到贪睡模式

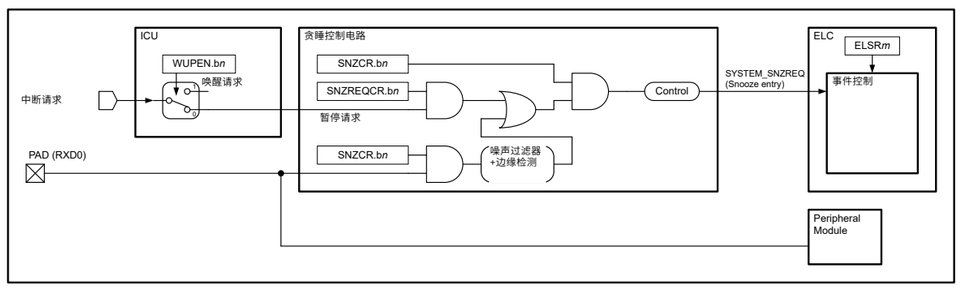


Figure 10.5 贪睡模式进入配置

当贪睡控制电路在软件待机模式下接受一个可用的贪睡请求时，MCU转移到贪睡模式。在这种模式下，一些外围模块在不唤醒CPU的情况下运行。可在贪睡模式下运行的外围模块如表10.2所示。此外，可以通过设置SNZCR.SNZDTCEN位来选择贪睡模式下的DTC操作。

Table 10.7 shows the Snooze requests that switch the MCU from Software Standby mode to Snooze mode. To use the listed Snooze requests as a trigger to switch to Snooze mode, the corresponding SNZREQENn bit of the SNZREQCRn register or RXDREQEN bit of SNZCR register must be set before entering Software Standby mode.

Table 10.7 Available snooze requests to switch to Snooze mode

Snooze request	Control Register	
	Register	Bit*1 *3
PORT_IRQn (n = 0 to 15)	SNZREQCR0	SNZREQENn (n = 0 to 15)
RTC_ALM	SNZREQCR0	SNZREQEN24
RTC_PRD	SNZREQCR0	SNZREQEN25
AGT1_AGTI	SNZREQCR0	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR0	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR0	SNZREQEN30
AGT3_AGTI	SNZREQCR1	SNZREQEN0
AGT3_AGTCMAI	SNZREQCR1	SNZREQEN1
AGT3_AGTCMBI	SNZREQCR1	SNZREQEN2
RXD0 falling edge	SNZCR	RXDREQEN*2

Note 1. Do not enable multiple snooze requests at the same time.
Note 2. Do not set the RXDREQEN bit to 1 except in asynchronous mode.
Note 3. When AGT1 is used for Snooze request factor, Snooze end factor is not allowed to set AGT3 (only AGT1).
When AGT3 is used for Snooze request factor, Snooze end factor is not allowed to set AGT1 (only AGT3).

Clear the DMAST.DMST and DTCST.DTCST bits to 0 before executing a WFI instruction, except when using the DTC in Snooze mode. If the DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

10.8.2 Canceling Snooze Mode

Snooze mode is canceled by an interrupt request that is available in Software Standby mode or a reset. Table 10.3 shows the requests that can be used to exit each mode. After canceling the Snooze mode, the MCU enters Normal mode and proceeds with exception processing for the given interrupt or reset. The action triggered by the interrupt requests, selected in SELSR0, cancels Snooze mode. Interrupt canceling Snooze mode must be selected in IELSRn to link to the NVIC for the corresponding interrupt handling. See section 13, Interrupt Controller Unit (ICU) for information on SELSR0 and IELSRn registers.

表10.7显示了将MCU从软件待机模式切换到贪睡模式的贪睡请求。要将列出的贪睡请求用作切换到贪睡模式的触发器，SNZREQCRn寄存器的相应SNZREQENn位或
在进入软件待机模式之前，必须设置SNZCR寄存器的RXDREQEN位。

Table 10.7 可用的贪睡请求以切换到贪睡模式

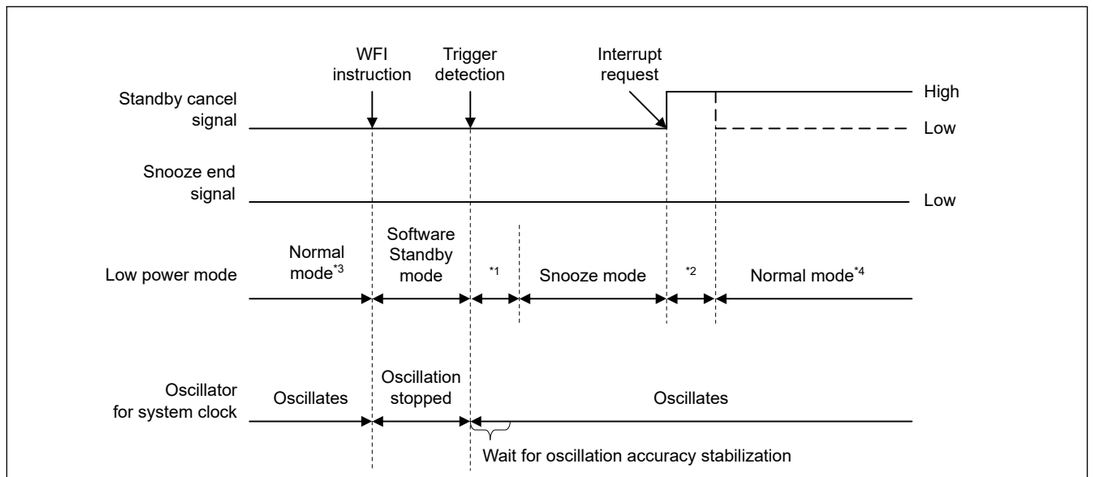
暂停请求	控制寄存器	
	Register	Bit*1 *3
PORT_IRQn (n = 0 to 15)	SNZREQCR0	SNZREQENn (n = 0 to 15)
RTC_ALM	SNZREQCR0	SNZREQEN24
RTC_PRD	SNZREQCR0	SNZREQEN25
AGT1_AGTI	SNZREQCR0	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR0	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR0	SNZREQEN30
AGT3_AGTI	SNZREQCR1	SNZREQEN0
AGT3_AGTCMAI	SNZREQCR1	SNZREQEN1
AGT3_AGTCMBI	SNZREQCR1	SNZREQEN2
RXD0下降沿	SNZCR	RXDREQEN*2

注意1.不要同时启用多个贪睡请求。
注2.除异步模式外，请勿将RXDREQEN位设置为1。
注3.当AGT1用于贪睡请求因子时，贪睡结束因子不允许设置AGT3（仅AGT1）。
当AGT3用于Snoozerequestfactor时，Snoozeendfactor不允许设置AGT1（仅AGT3）。

在执行WFI指令之前将DMAST.DMST和DTCST.DTCST位清零，除非在贪睡模式下使用DTC。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

10.8.2 取消贪睡模式

贪睡模式由软件待机模式下可用的中断请求或复位取消。表10.3显示了可用于退出每种模式的请求。取消贪睡模式后，MCU进入正常模式并继续对给定中断或复位进行异常处理。在SELSR0中选择的中断请求触发的动作取消贪睡模式。必须在IELSRn中选择中断取消贪睡模式以链接到NVIC以进行相应的中断处理。有关SELSR0和IELSRn寄存器的信息，请参见第13节，中断控制器单元(ICU)。



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Transition time from Snooze mode to Normal mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.
Note 4. Disable Snooze mode (SNZCR.SNZE = 0) immediately after returning to Normal mode.

Figure 10.6 Canceling of Snooze mode when an interrupt request signal is generated

10.8.3 Returning from Snooze Mode to Software Standby Mode

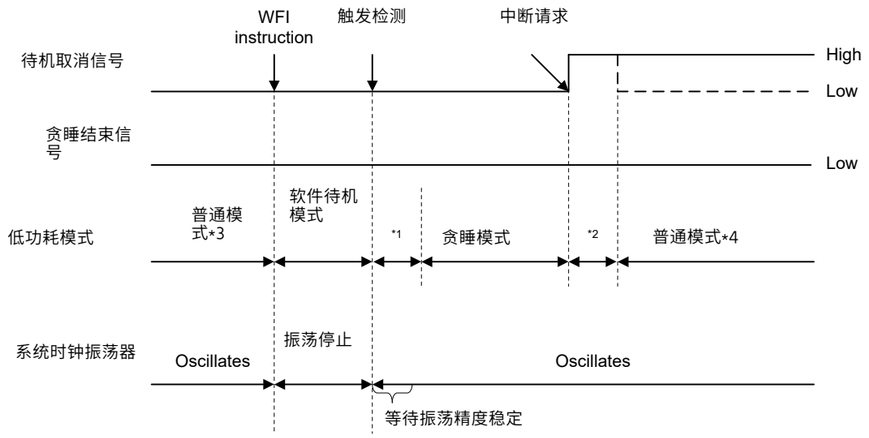
Table 10.8 shows the snooze end request that can be used as triggers to return to Software Standby mode. The snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each of the requests invokes transition to Software Standby mode from Snooze mode.

Table 10.9 shows the snooze end conditions that consist of the snooze end requests and the conditions of the peripheral modules. The CTSU, SCI0, ADC12n (n = 0, 1), and DTC modules can keep the MCU in Snooze mode until they complete the operation. However, an AGTn (n = 1, 3) underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of SCI0 operation.

Figure 10.7 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which snooze end requests are set in the SNZEDCR0 register. A snooze request is cleared automatically after returning to Software Standby mode.

Table 10.8 Available snooze end requests (triggers to return to Software Standby mode)

Peripheral Module	Snooze end request	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	Last DTC transmission completion (DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	Not Last DTC Transmission Completion (DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC120	Window A/B compare match (ADC120_WCMPM)	SNZEDCR0	AD0MATED
ADC120	Window A/B compare mismatch (ADC120_WCMPUM)	SNZEDCR0	AD0UMTED
ADC121	Window A/B compare match (ADC121_WCMPM)	SNZEDCR0	AD1MATED
ADC121	Window A/B compare mismatch (ADC121_WCMPUM)	SNZEDCR0	AD1UMTED
SCI0	SCI0 address mismatch (SCI0_DCUF)	SNZEDCR0	SCI0UMTED
AGT3	Underflow or measurement complete (AGT3_AGTI)	SNZEDCR1	AGT3UNFED



注1.从软件待机模式到贪睡模式的转换时间。
注2.从贪睡模式到正常模式的转换时间。
注3.在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。
注4.返回正常模式后立即禁用贪睡模式(SNZCR.SNZE=0)。

Figure 10.6 产生中断请求信号时取消贪睡模式

10.8.3 从贪睡模式返回到软件待机模式

表10.8显示了可用作返回到软件待机模式的触发器的贪睡结束请求。贪睡结束请求仅在贪睡模式下可用。如果请求是在MCU未处于贪睡模式时生成的，则它们将被忽略。选择多个请求时，每个请求都会从贪睡模式转移到软件待机模式。

表10.9显示了贪睡结束条件，包括贪睡结束请求和外围模块的条件。CTSU、SCI0、ADC12n(n=0 1)和DTC模块可以使MCU保持在贪睡模式，直到它们完成操作。但是，AGTn(n=1 3)下溢作为返回软件待机模式的触发器会取消贪睡模式，而无需等待SCI0操作完成。

图10.7显示了从贪睡模式转换到软件待机模式的时序图。该模式转换根据SNZEDCR0寄存器中设置的贪睡结束请求发生。返回软件待机模式后，贪睡请求会自动清除。

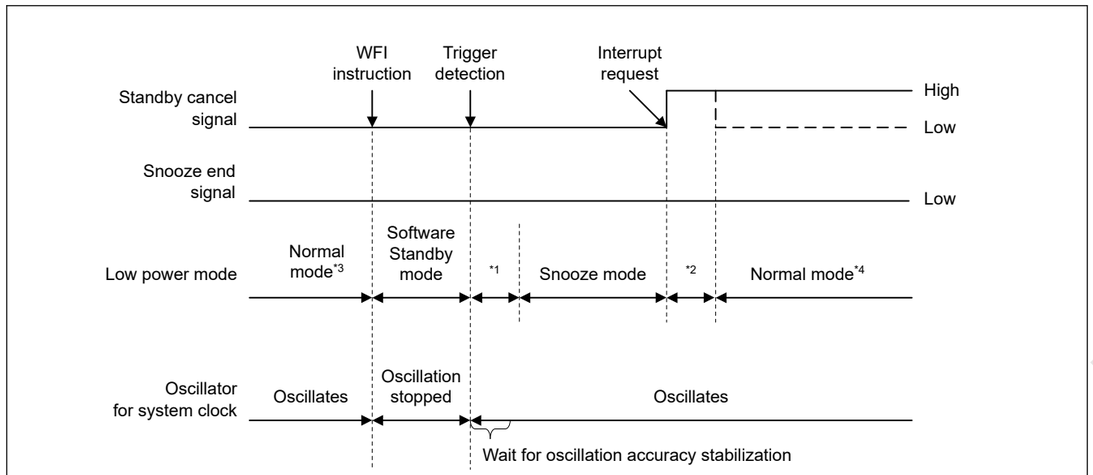
Table 10.8 可用的暂停结束请求（触发返回到软件待机模式）

Peripheral Module	暂停结束请求	Enable/Disable Control	
		Register	Symbol
AGT1	AGT1 underflow (AGT1_AGTI)	SNZEDCR0	AGTUNFED
DTC	上次DTC传输完成(DTC_COMPLETE)	SNZEDCR0	DTCZRED
DTC	不是最后一个DTC传输完成(DTC_TRANSFER)	SNZEDCR0	DTCNZRED
ADC120	窗口AB比较匹配(ADC120_WCMPM)	SNZEDCR0	AD0MATED
ADC120	窗口AB比较不匹配(ADC120_WCMPUM)	SNZEDCR0	AD0UMTED
ADC121	窗口AB比较匹配(ADC121_WCMPM)	SNZEDCR0	AD1MATED
ADC121	窗口AB比较不匹配(ADC121_WCMPUM)	SNZEDCR0	AD1UMTED
SCI0	SCI0地址不匹配(SCI0_DCUF)	SNZEDCR0	SCI0UMTED
AGT3	下溢或测量完成(AGT3_AGTI)	SNZEDCR1	AGT3UNFED

Table 10.9 Snooze end conditions

Operating module when a snooze end request occurs	Snooze end request	
	AGT1/AGT3 underflow	Other than AGT1/AGT3 underflow
DTC	The MCU transfers to the Software Standby mode after all of the modules listed in this table complete operation.	The MCU transfers to the Software Standby mode after all of the modules listed to the left of this column complete the operation.
ADC12n		
CTSU		
SCI0	The MCU transfers to the Software Standby mode immediately after the snooze end request is generated.	
Other than specified	The MCU transfers to the Software Standby mode immediately after a snooze end request is generated.	

Note: If the DTC is used to activate the ADC12n, CTSU, or SCI, the MCU transitions to Software Standby mode immediately after a snooze end request is generated.



Note 1. Transition time from Software Standby mode to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before switching to Software Standby mode.

Figure 10.7 Canceling of Snooze mode when an interrupt request signal is not generated

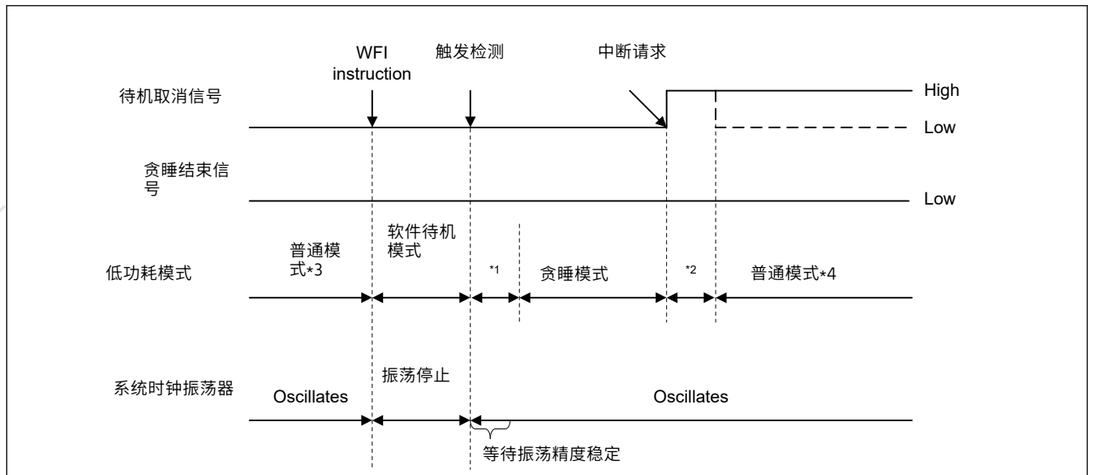
10.8.4 Snooze Operation Example

Figure 10.8 shows an example setting for using ELC in Snooze mode.

Table 10.9 暂停结束条件

发生贪睡结束请求时的操作模块	暂停结束请求	
	AGT1/AGT3 underflow	除了AGT1AGT3下溢
DTC	在此表中列出的所有模块完成操作后，MCU将进入软件待机模式。	在此列左侧列出的所有模块完成操作后，MCU将进入软件待机模式。
ADC12n		
CTSU		
SCI0	产生贪睡结束请求后，MCU立即进入软件待机模式。	
指定以外的	产生贪睡结束请求后，MCU立即转入软件待机模式。	

Note: 如果DTC用于激活ADC12n、CTSU或SCI，则MCU在产生贪睡结束请求后立即转换到软件待机模式。

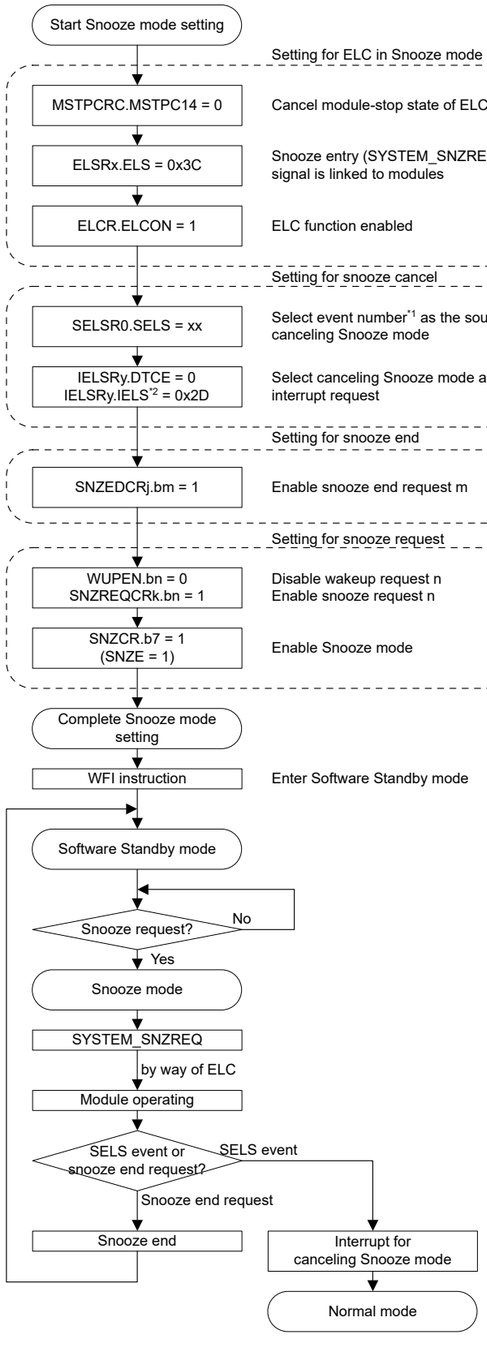


注1.从软件待机模式到贪睡模式的转换时间。
注2.在切换到软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。

Figure 10.7 未产生中断请求信号时取消贪睡模式

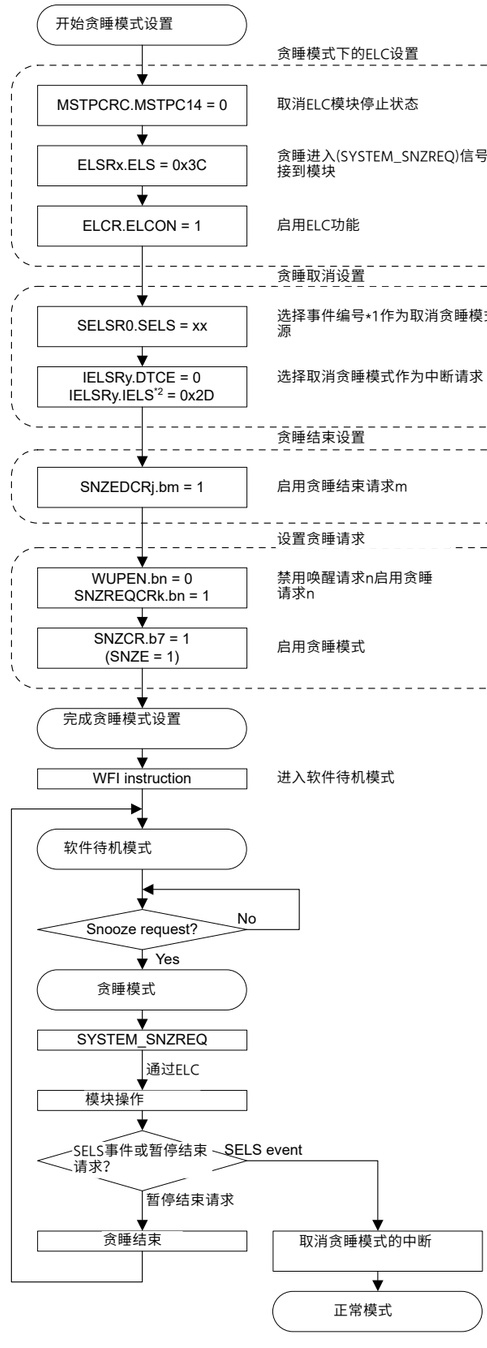
10.8.4 贪睡操作示例

图10.8显示了在贪睡模式下使用ELC的示例设置。



Note 1. See Table 13.4

Figure 10.8 Setting example of using ELC in Snooze mode



注1.见表13.4

Figure 10.8 在贪睡模式下使用ELC的设置示例

The MCU can transmit and receive data in SCI0 asynchronous mode without CPU intervention. When using the SCI0 in Snooze mode, use either High-speed mode or Low-speed mode.

Do not use Subosc-speed mode. Table 10.10 shows the maximum transfer rate of SCI0 in Snooze mode.

Table 10.10 HOCO: ± 1.4% (Ta = -20° to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency					
	LOCO is not operating			LOCO is operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

When using SCI0 in Snooze mode, use the following setting: BGDM = 0, ABCS = 0, ABCSE = 0. See section 30, Serial Communications Interface (SCI) for information on these bits.

Figure 10.9 shows a setting example for using SCI0 in Snooze mode entry.

MCU可以在SCI0异步模式下发送和接收数据，无需CPU干预。在使用SCI0时贪睡模式，使用高速模式或低速模式。

不要使用Subosc速度模式。表10.10显示了Snooze模式下SCI0的最大传输速率。

Table 10.10 HOCO: ± 1.4% (Ta = -20° to 105°C) (Unit: bps)

ICLK、PCLKA、PCLKB、PCLKC的最大分频比，PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency					
	LOCO没有运行			LOCO正在运营		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16						
32	1200			2400		
64						

在贪睡模式下使用SCI0时，使用以下设置：BGDM=0，ABCS=0，ABCSE=0。参见第30节，串行通信接口(SCI)以获取有关这些位的信息。

图10.9显示了在贪睡模式进入中使用SCI0的设置示例。

RA生态工作室

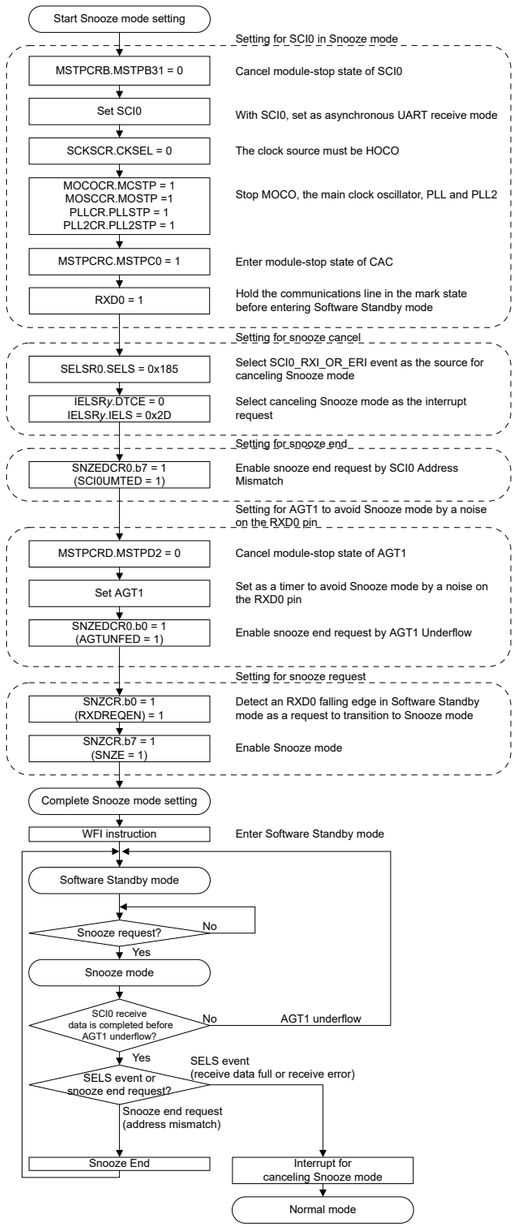


Figure 10.9 Setting example of using SCI0 in Snooze mode entry

10.9 Deep Software Standby Mode

10.9.1 Transitioning to Deep Software Standby Mode

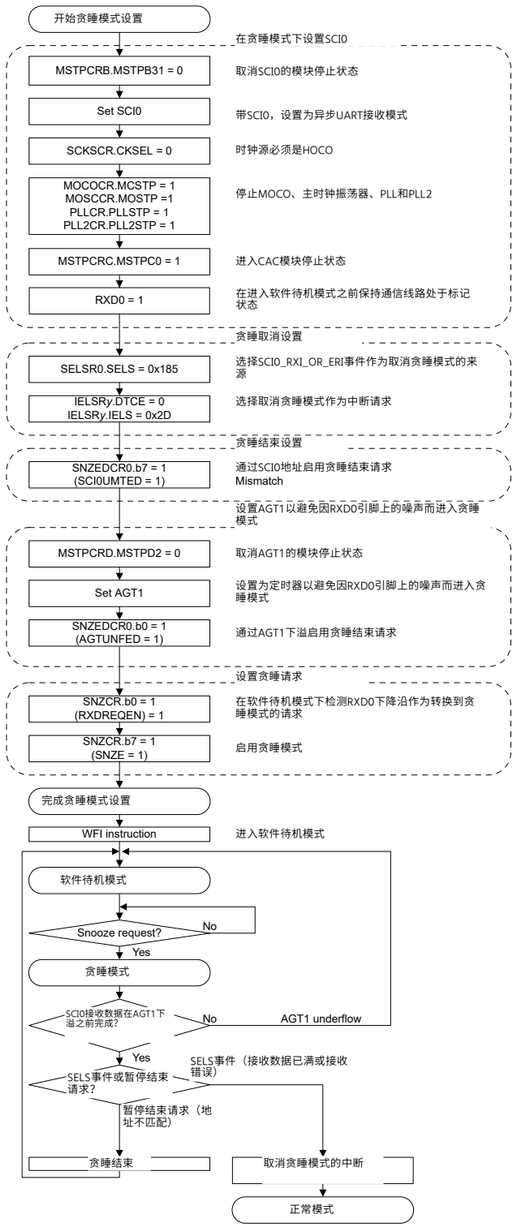


Figure 10.9 在Snooze模式进入使用SCI0的设置示例

10.9 深度软件待机模式

10.9.1 过渡到深度软件待机模式

When a WFI instruction is executed with the SBYCR.SSBY and DPSBYCR.DPSBY bits set to 1, the MCU enters Deep Software Standby mode. See Table 10.6 for the setting of the related control bits. In this mode, the CPU, on-chip peripheral functions (except for RTC alarm, RTC interval, and USB suspend/resume detecting unit), SRAM (except for standby RAM), and all oscillators (except for Sub-clock oscillator and Low-speed on-chip oscillator) are stopped. Also because the internal power supply to these modules is stopped, power consumption is remarkably reduced. The contents of all CPU registers and internal peripheral modules (except for RTC alarm, RTC interval, and USB suspend/resume detecting unit) become undefined.

Data in the standby SRAM are preserved if the setting of the DEEPCUT[1:0] bits are 00b. If the setting of the DEEPCUT[1:0] bits are 01b, the internal power supply to the standby SRAM and the USB resume detecting unit is cut off, reducing power consumption. Data in the standby SRAM becomes undefined at this time. If the setting of the DEEPCUT[1:0] bits are 11b, the internal power supply to the standby SRAM, and the USB resume detecting unit is cut off, the LVD is stopped, and the low-power-consumption function of the power-on reset circuit is enabled, so power consumption is further reduced. For details, see section 53, Electrical Characteristics.

When the MCU enters Deep Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1, power supply to the IWDT-dedicated clock and the IWDT is cut off, and counting by the IWDT stops.

When OFS0.IWDTSTPCTL bit is 0, the MCU enters Software Standby mode instead of Deep Software Standby mode, regardless of the setting of OFS0.IWDTSTRT bit or DPSBYCR.DPSBY bit. If OFS0.IWDTSTPCTL bit is 0 while OFS0.IWDTSTRT bit is 0 (auto start mode), IWDT-dedicated clock and IWDT continues the operation.

When LVD1CR0.RI = 1 (voltage monitor 1 reset selected) or LVD2CR0.RI = 1 (voltage monitor 2 reset selected), the MCU enters Software Standby mode instead of Deep Software Standby mode. The I/O port states are the same as in Software Standby mode.

When the PLL is selected as the clock source, set the following modules to the module-stop state before executing a WFI instruction:

USBHS, SCE9.

In this case, you must insert wait time at least 750 ns before executing a WFI instruction. Measurement of the waiting time, it is recommended the measurement by the software. If you use the timer, regardless of the use conditions, ensure that the waiting time has elapsed.

See Figure 10.2 for Example flow for transition to software standby mode or deep software standby mode.

Note: Conditions on the DTC, DMAC, and IWDT for transitioning to Software Standby mode should be met before the WFI instruction is executed. For details, see section 10.7. Software Standby Mode.

10.9.2 Cancelling Deep Software Standby Mode

Deep Software Standby mode is canceled by:

- An interrupt shown in Table 10.3
- A RES pin reset
- A power-on reset
- A voltage monitor 0 reset.

(1) Cancelling by an interrupt

Cancelling by interrupts is controlled by DPSIERn (n = 0 to 3) and DPSIFRn (n = 0 to 3). When a Deep Software Standby Cancelling interrupt is generated, the corresponding flag in DPSIFRn is set to 1. If the interrupt is enabled in DPSIERn, Deep Software Standby mode is canceled. Rising edge or falling edge can be selected by DPSIEGRn (n = 0 to 2). The interrupts for which an edge can be selected are the NMI, IRQn-DS (n = 0 to 15), voltage monitor 1, and voltage monitor 2 interrupts. When a Deep Software Standby mode canceling request occurs, the internal power is supplied and MOCO starts oscillating, and an internal reset (Deep Software Standby reset) is generated for the entire MCU.

The stable MOCO clock is supplied to the entire MCU and Deep Software Standby reset is canceled. The MCU starts reset exception handling.

When Deep Software Standby mode is canceled by an external interrupt pin or internal interrupt signal, the RSTSR0.DPSRSTF flag is set to 1.

当在SBYCR.SSBY和DPSBYCR.DPSBY位设置为1的情况下执行WFI指令时，MCU进入Deep
软件待机模式。相关控制位的设置见表10.6。在此模式下，CPU、片上外围功能（RTC闹钟、RTC间隔和USB暂停恢复检测单元除外）、SRAM（备用RAM除外）和所有振荡器（副时钟振荡器和Low-速度片上振荡器）停止。此外，由于这些模块的内部电源停止，功耗显着降低。所有CPU寄存器和内部外围模块（RTC警报、RTC间隔和USB暂停恢复检测单元除外）的内容变为未定义。

如果DEEPCUT[1:0]位的设置为00b，则保留备用SRAM中的数据。如果DEEPCUT[1:0]位设置为01b，则内部对待机SRAM和USB恢复检测单元的供电被切断，从而降低功耗。此时备用SRAM中的数据变为未定义。如果DEEPCUT[1:0]位设置为11b，则内部对待机SRAM的供电，以及USB恢复检测单元被切断，LVD停止，电源的低功耗功能-on复位电路使能，因此功耗进一步降低。有关详细信息，请参阅第53节，电气特性。

当MCU在IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为1时进入深度软件待机模式时，IWDT专用时钟和IWDT的电源被切断，IWDT的计数停止。

当OFS0.IWDTSTPCTL位为0时，MCU进入软件待机模式而不是深度软件待机模式，无论OFS0.IWDTSTRT位或DPSBYCR.DPSBY位如何设置。如果OFS0.IWDTSTPCL位为0而OFS0.IWDTSTRT位为0（自动启动模式），IWDT专用时钟和IWDT继续运行。

当LVD1CR0.RI=1（选择电压监视器1复位）或LVD2CR0.RI=1（选择电压监视器2复位）时，MCU进入软件待机模式而不是深度软件待机模式。IO端口状态与软件待机模式相同。

WhenthePLLisselectedastheclocksource setthefollowingmodulestothemodule-stopstatebeforeexecutingaWFIinstruction:

USBHS, SCE9.

在这种情况下，您必须在执行WFI指令之前插入至少750ns的等待时间。等待时间的测量，建议通过软件测量。如果您使用定时器，无论使用条件如何，请确保等待时间已过。

有关转换到软件待机模式或深度软件待机模式的示例流程，请参见图10.2。

Note: 在执行WFI指令之前，应满足DTC、DMAC和IWDT转换到软件待机模式的条件。有关详细信息，请参阅第10.7节。软件待机模式。

10.9.2 取消深度软件待机模式

深度软件待机模式通过以下方式取消：

●表10.3所示的中断

●ARES引脚复位

- A power-on reset

●电压监视器0复位。

(1) 通过中断取消

中断取消由DPSIERn(n=0到3)和DPSIFRn(n=0到3)控制。深度软件待机时
产生取消中断时，DPSIFRn中的相应标志置1。如果在DPSIERN中使能中断，
深度软件待机模式被取消。上升沿或下降沿可以通过DPSIEGRn(n=0到2)选择。可以选择边沿的中断是NMI、IRQn-DS（n=0到15）、电压监视器1和电压监视器2中断。当产生深度软件待机模式取消请求时，内部电源被提供，MOCO开始振荡，并为整个MCU产生内部复位（深度软件待机复位）。

为整个MCU提供稳定的MOCO时钟，并取消深度软件待机复位。MCU开始复位异常处理。

当深度软件待机模式被外部中断引脚或内部中断信号取消时，
RSTSR0.DPSRSTF标志设置为1。

(2) Cancelling by RES pin reset

When the RES pin is driven low, the MCU cancels Deep Software Standby mode and enters the reset state. Keep the RES pin low for the time specified in section 53, Electrical Characteristics. When RES pin is driven high after the specified time period, the CPU starts the reset exception handling.

(3) Cancelling by a power-on reset

Deep Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.

(4) Cancelling by a voltage monitor 0 reset

Deep Software Standby mode is canceled by a voltage monitor 0 reset from the voltage detection circuit and the MCU starts the reset exception handling.

10.9.3 Pin States when Deep Software Standby mode is Canceled

In Deep Software Standby mode, the I/O ports retain the same states from Software Standby mode. The MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, and reset exception handling starts immediately. The DPSBYCR.IOKEEP bit setting determines whether to initialize the I/O ports or to retain the I/O ports states for Software Standby mode. The following is the state of the I/O ports for each bit setting:

- When the DPSBYCR.IOKEEP bit = 0
  I/O ports are initialized by an internal reset generated when Deep Software Standby mode is canceled.
- When the DPSBYCR.IOKEEP bit = 1
  Although the MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, the I/O ports retain their states from Software Standby mode regardless of the MCU internal state. The I/O ports states remain unchanged from Software Standby mode even when settings are made to the I/O ports or peripheral modules. The retained I/O ports states are released by clearing the DPSBYCR.IOKEEP bit to 0, and the MCU operates according to the internal state. The DPSBYCR.IOKEEP bit is not initialized by any internal reset generated when Deep Software Standby mode is canceled.

10.9.4 Example of Deep Software Standby Mode Application

(1) Entering and exiting Deep Software Standby mode

Figure 10.10 shows an example where a transition to Deep Software Standby mode is made at the falling edge of the IRQn-DS pin, and exiting Deep Software Standby mode is made at the rising edge of the IRQn-DS pin. In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 00b (falling edge). After the DPSIEGRy.DIRQnEG (y = 0 or 1, n = 0 to 15) bit is set to 1 (rising edge) and the SBYCR.SSBY bit and DPSBYCR.DPSBY bit are both set to 1, the WFI instruction is executed. As a result, the MCU transitions to Deep Software Standby mode. Deep Software Standby mode is then canceled on the rising edge of the IRQn-DS pin.

(2) 通过RES引脚复位取消

当RES引脚驱动为低电平时，MCU取消深度软件待机模式并进入复位状态。在第53节“电气特性”中指定的时间内保持RES引脚为低电平。当RES引脚在指定时间段后被驱动为高电平时，CPU开始复位异常处理。

(3) 通过上电复位取消

深度软件待机模式通过上电复位取消，MCU启动复位异常处理。

(4) 通过电压监视器取消0复位

深度软件待机模式通过电压检测电路的电压监视器0复位取消，MCU开始复位异常处理。

10.9.3 取消深度软件待机模式时的引脚状态

在深度软件待机模式下，IO端口保持与软件待机模式相同的状态。MCU通过取消深度软件待机模式时产生的内部复位进行初始化，并立即开始复位异常处理。DPSBYCR.IOKEEP位设置确定是初始化IO端口还是保留软件待机模式下的IO端口状态。以下是每个位设置的IO端口状态：

- 当DPSBYCR.IOKEEP位=0时
  IO端口由取消深度软件待机模式时产生的内部复位进行初始化。
- 当DPSBYCR.IOKEEP位=1时
  虽然MCU由取消深度软件待机模式时产生的内部复位来初始化，但无论MCU内部状态如何，IO端口仍会保持软件待机模式下的状态。即使对IO端口或外围模块进行了设置，IO端口状态在软件待机模式下也保持不变。通过将DPSBYCR.IOKEEP位清0来释放保留的IO端口状态，MCU根据内部状态运行。DPSBYCR.IOKEEP位不会被取消深度软件待机模式时产生的任何内部复位初始化。

10.9.4 深度软件待机模式应用示例

(1) 进入和退出深度软件待机模式

图10.10显示了一个示例，其中在IRQnDS引脚的下降沿转换到深度软件待机模式，在IRQn-DS引脚的上升沿退出深度软件待机模式。在此示例中，接受IRQn中断，同时ICU的IRQCRi.IRQMD[1:0]位设置为00b（下降沿）。在DPSIEGRy.DIRQnEG（y=0或1，n=0到15）位设置为1（上升沿）并且SBYCR.SSBY位和

DPSBYCR.DPSBY位都设置为1，执行WFI指令。因此，MCU过渡到DeepSoftware待机模式。然后在IRQn-DS引脚的上升沿取消深度软件待机模式。

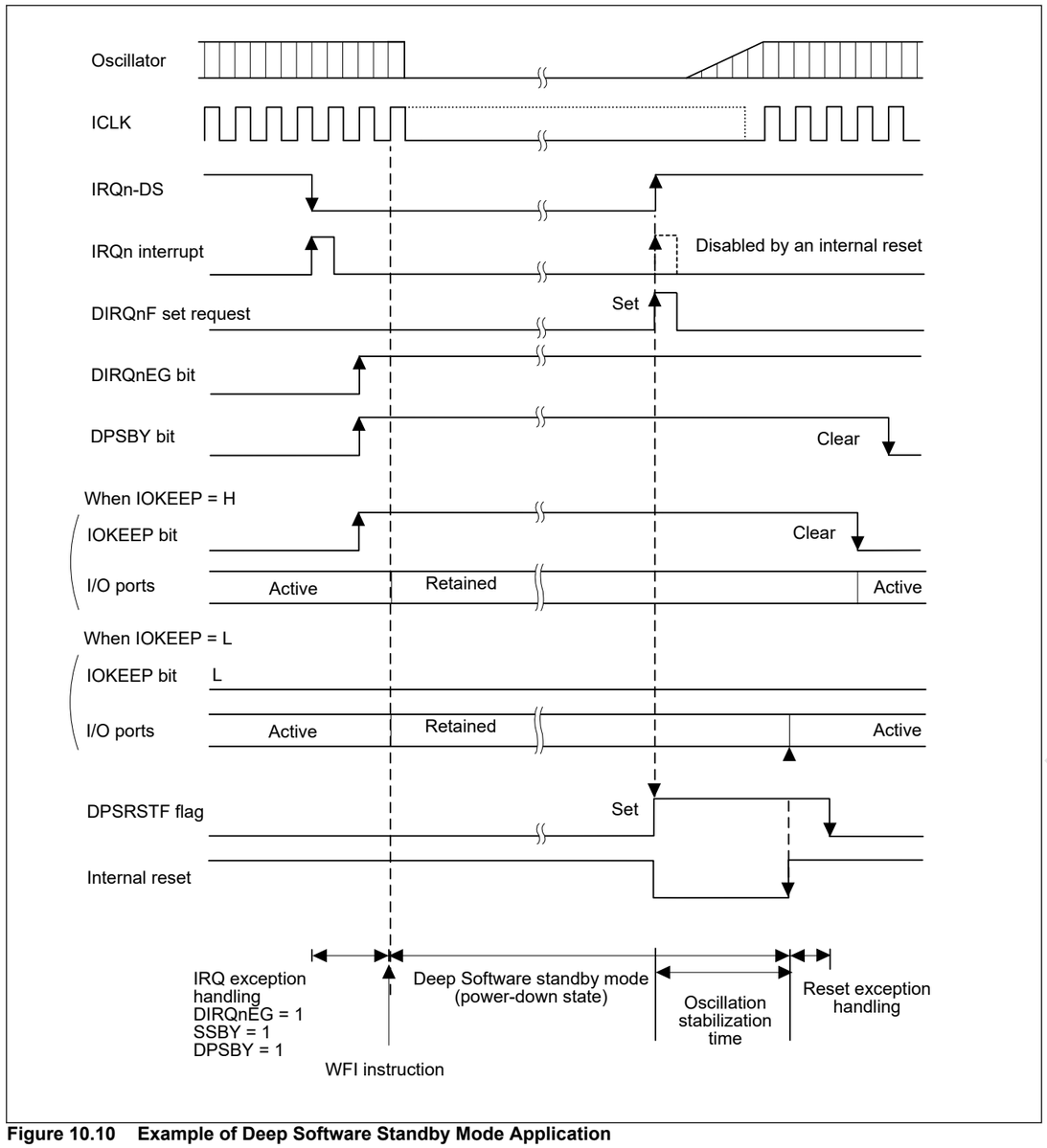


Figure 10.10 Example of Deep Software Standby Mode Application

10.9.5 Usage Flow for Deep Software Standby Mode

Figure 10.11 shows an example flow for using Deep Software Standby mode.

In this example, the RSTSR0.DPSRSTF flag of the reset function is read after the reset exception handling to determine whether a reset was generated by the RES pin or by the cancellation of Deep Software Standby mode.

For a reset by the RES pin, the MCU transitions to Deep Software Standby mode after the required register settings are made.

For a reset by cancellation of Deep Software Standby mode, the DPSBYCR.IOKEEP bit is cleared to 0 after the I/O port settings are made.

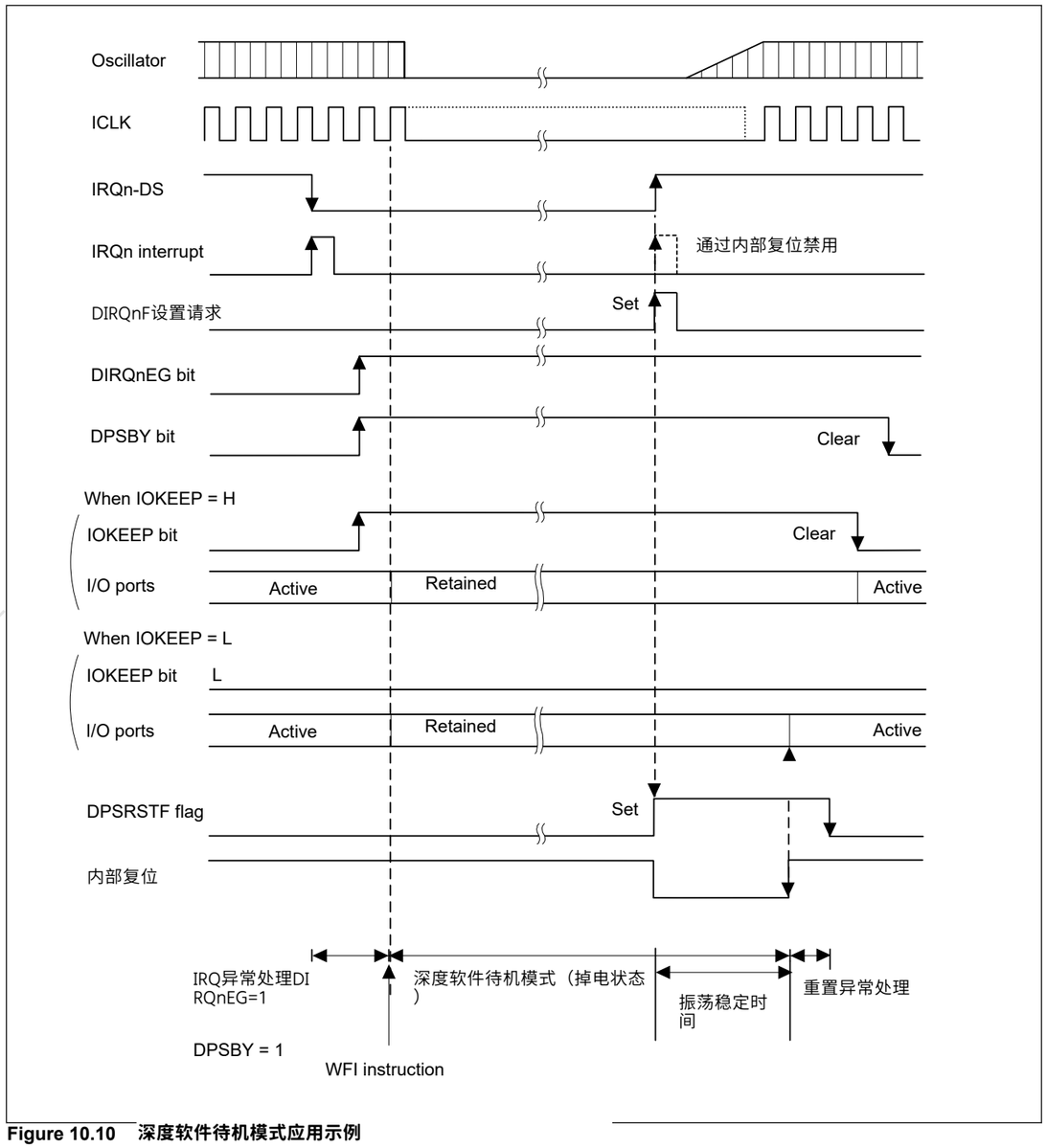


Figure 10.10 深度软件待机模式应用示例

10.9.5 深度软件待机模式的使用流程

图10.11显示了使用深度软件待机模式的示例流程。

在本例中，复位功能的RSTSR0.DPRSTF标志在复位异常处理后被读取，以确定复位是由RES引脚产生还是由深度软件待机模式的取消产生。

对于通过RES引脚进行的复位，在进行所需的寄存器设置后，MCU会转换到深度软件待机模式。

对于通过取消深度软件待机模式进行的复位，在IO端口设置完成后DPSBYCR.IOKEEP位被清零。

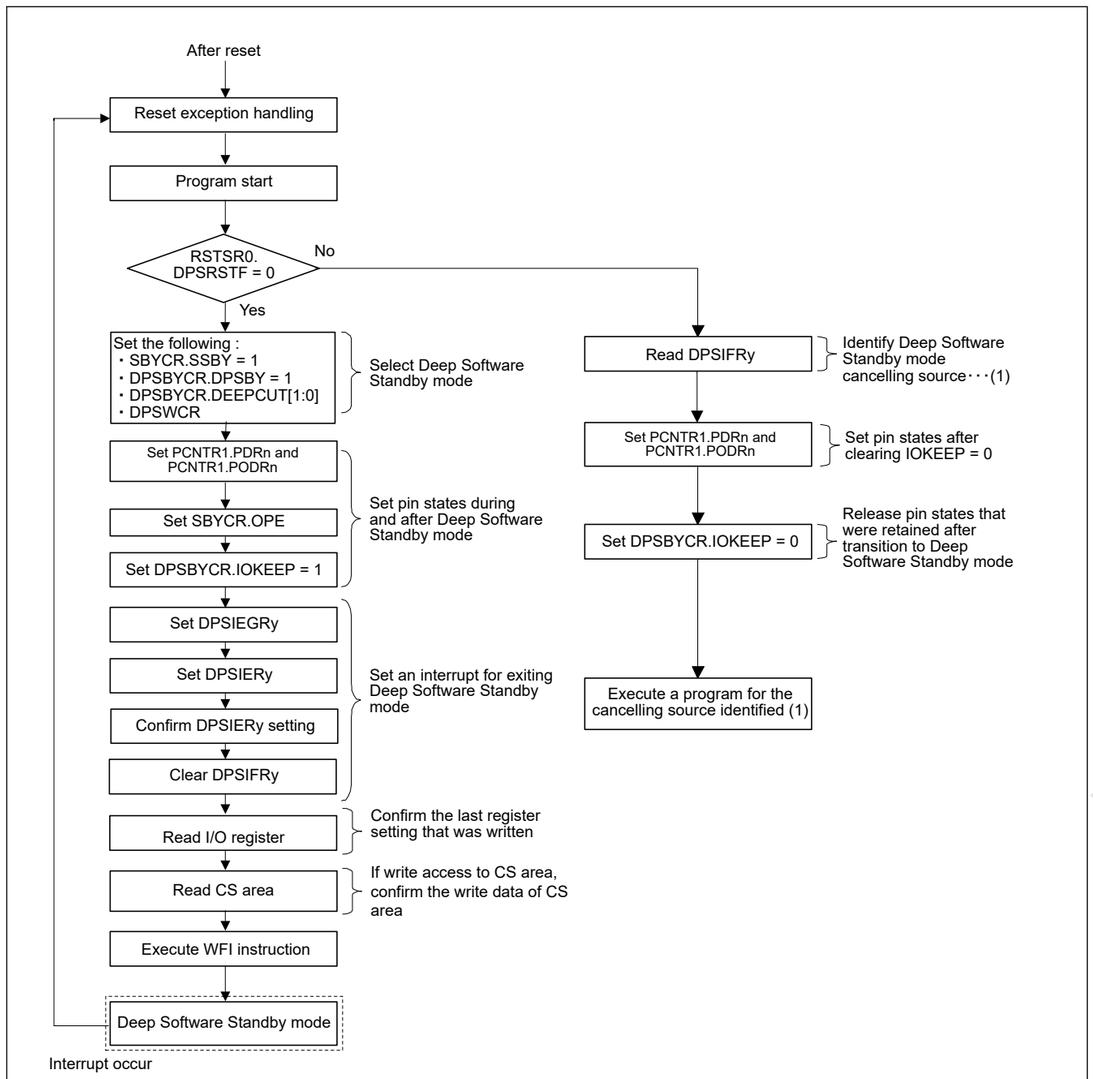


Figure 10.11 Example flow for using Deep Software Standby mode

10.10 Usage Notes

10.10.1 Register Access

(1) Invalid register write accesses during specific modes or transitions

Do not write to registers under any of the conditions listed in this section.

[Registers]

- All registers with a peripheral name of SYSTEM.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)

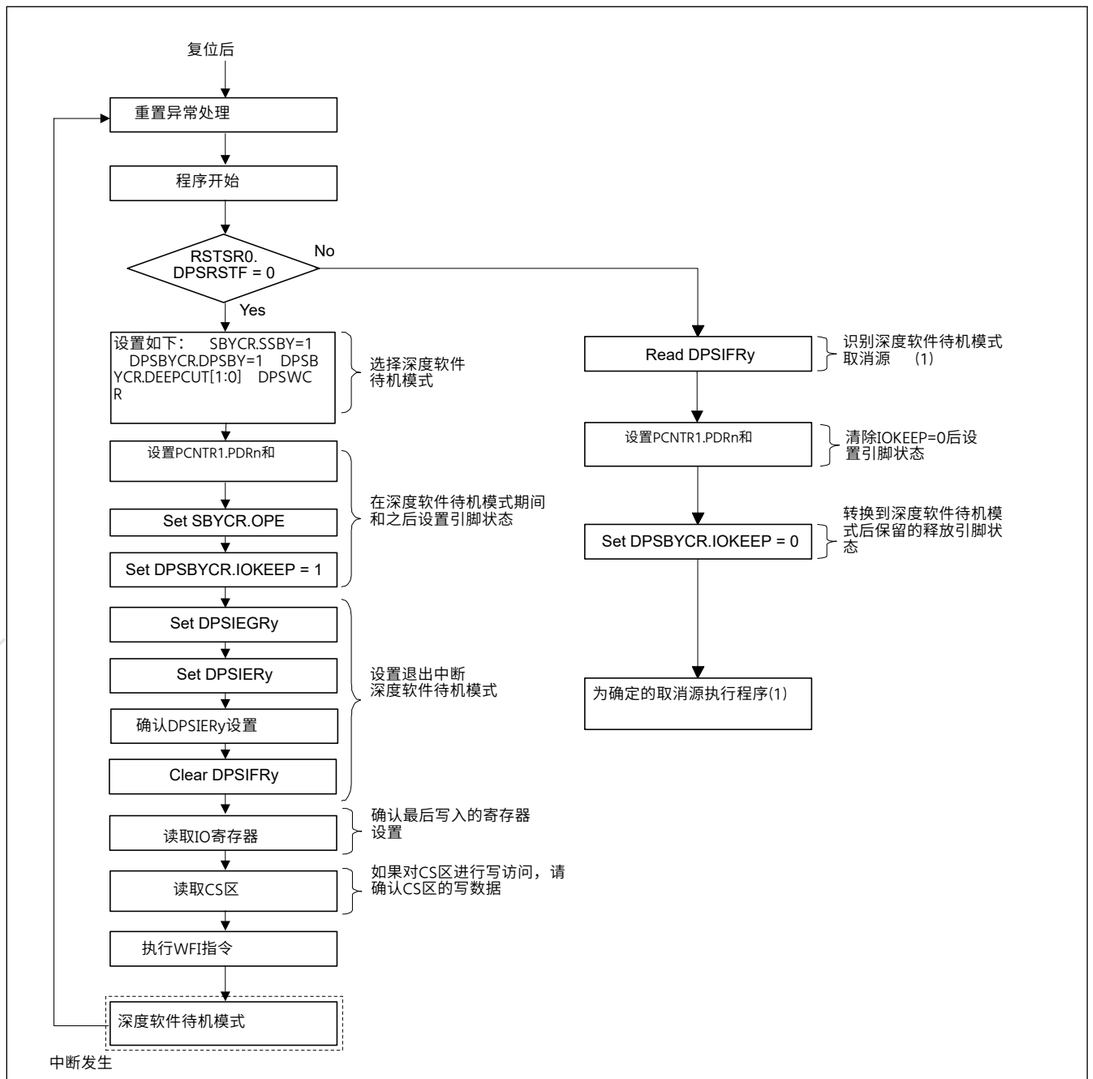


Figure 10.11 使用深度软件待机模式的示例流程

10.10 使用说明

10.10.1 注册访问

(1) 特定模式或转换期间的无效寄存器写访问

不要在本节列出的任何条件下写入寄存器。

[Registers]

●外设名称为SYSTEM的所有寄存器。

[Conditions]

●OPCCR.OPCMTSF=1或SOPCCR.SOPCMTSF=1（在工作功率控制模式转换期间）

- During the time period from executing a WFI instruction to returning to Normal mode
- FENTRYR.FENTRY0 = 1 or FENTRYR.FENTRYD = 1 (flash P/E mode, data flash P/E mode)

(2) Valid setting for the clock-related registers

Table 10.11 and Table 10.12 show the valid settings of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting. Each register has certain prohibited settings under conditions other than those related to the operating power control modes. See section 8, Clock Generation Circuit for another condition of each register.

Table 10.11 Valid settings for the clock-related registers (1)

Mode	Valid settings								
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0] ICK[2:0]	PLLCR.PLLSTP	PLL2CR.PLL2STP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub clock) 101b (PLL) *1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub clock)		1 (stop)	1 (stop)					
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	1 (stop)	1 (stop)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Note 1. SCKSCR.CKSEL[2:0] only

Table 10.12 Valid settings for the clock-related registers (2)

Operating oscillator	Valid settings	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
PLL, PLL2	0	00b
High-speed on-chip oscillator	0	00b, 11b
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	0, 1	00b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Invalid register write accesses in subosc-speed mode

Do not write to registers under the listed condition in this section.

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Invalid register write accesses by the DTC or DMAC

Do not write to registers listed in this section by the DTC or DMAC.

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, MSTPCRE

●从执行WFI指令到返回Normal模式的时间段内

●FENTRYR.FENTRY0=1或FENTRYR.FENTRYD=1（闪存PE模式，数据闪存PE模式）

(2) 时钟相关寄存器的有效设置

表10.11和表10.12显示了每种工作电源控制模式下时钟相关寄存器的有效设置。请勿写入有效设置以外的任何值。每个寄存器在与工作功率控制模式相关的条件下都有某些禁止设置。有关每个寄存器的另一个条件，请参见第8节，时钟生成电路。

Table 10.11 时钟相关寄存器的有效设置(1)

Mode	有效设置								
	SCKSCR.CKSEL[2:0] CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0] ICK[2:0]	PLLCR.PLLSTP	PLL2CR.PLL2STP	HOCOCR.HCSTP	MOCOCR.MCSTP	LOCOCR.LCSTP	MOSCCR.MOSTP	SOSCCR.SOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub clock) 101b (PLL) *1	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stop)	0 (operating) 1 (stop)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub clock)		1 (stop)	1 (stop)					
Subosc-speed	010b (LOCO) 100b (SOSC)	000b (1/1)	1 (stop)	1 (stop)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

注1.仅SCKSCR.CKSEL[2:0]

Table 10.12 时钟相关寄存器的有效设置(2)

操作振荡器	有效设置	
	SOPCCR.SOPCM	OPCCR.OPCM[1:0]
PLL, PLL2	0	00b
High-speed on-chip oscillator	0	00b, 11b
Middle-speed on-chip oscillator		
主时钟振荡器		
Low-speed on-chip oscillator	0, 1	00b, 11b
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) subosc-speed模式下的无效寄存器写访问

不要在本节列出的条件下写入寄存器。

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) DTC或DMAC的无效寄存器写访问

不要写入DTC或DMAC在本节中列出的寄存器。

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, MSTPCRE

(5) Invalid register write accesses in Snooze mode

Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode.

[Registers]

- SNZCR, SNZEDCRn, SNZREQCRn.

(6) Invalid write access to FLWT.FLWT[2:0]

Do not write any value other than 000b to the FLWT.FLWT[2:0] bits under the listed condition.

[Conditions]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(7) Invalid write access when PRCR.PRC1 is 0

Do not write to registers listed in this section when the PRCR.PRC1 bit is 0.

[Registers]

- SBYCR, SNZCR, SNZEDCRn, SNZREQCRn, OPCCR, SOPCCR, DPSBYCR, DPSWCR, DPSIERn, DPSIFRn, DPSIGRn, SYOCDCR

(8) Invalid write access when when PRCR.PRC4 bit is 0

Do not write to registers listed in this section when the PRCR.PRC4 bit is 0.

[Registers]

- LPMSAR, DPFSAR

10.10.2 I/O Port pin states

The I/O port pin states in Software Standby mode, Deep Software Standby and Snooze mode, unless modifying in Snooze mode, are the same before entering the modes. Therefore, power consumption is not reduced while the output signals are held high.

10.10.3 Module-Stop State of DTC, DMAC

Before writing 1 to MSTPCRA.MSTPA22, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0. For details, see section 16, DMA Controller (DMAC) and section 17, Data Transfer Controller (DTC).

10.10.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If setting the module-stop bit while an interrupt request is generated, a CPU interrupt source or a DTC or DMAC startup source cannot be cleared. Always disable the associated interrupts before setting the module-stop bits.

10.10.5 Input Buffer Control by DIRQnE Bit

Setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the associated input buffer of the IRQ0-DS to IRQ15-DS pins. Although inputs to these pins are sent to the DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, they are not sent to the interrupt controller (ICU), peripheral modules, and I/O ports.

10.10.6 Transitioning to Low Power Modes

Because the MCU does not support wakeup by events, do not enter the low power modes such as Sleep mode, Software Standby mode or Deep Software Standby Mode by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex-M33 core because the MCU does not support low power modes by SLEEPDEEP.

10.10.7 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register and CS area writes are complete, in which case operation might not be as intended. This can happen if the WFI is placed immediately after a write to an I/O register and CS area. To avoid this problem, read back the register and CS area that was written to confirm that the write completed.

(5) 贪睡模式下的无效寄存器写访问

不要在贪睡模式下写入本节中列出的寄存器。必须在进入软件待机模式之前设置它们。

[Registers]

- SNZCR, SNZEDCRn, SNZREQCRn.

(6) 对FLWT.FLWT[2:0]的写入访问无效

在所列条件下，请勿将000b以外的任何值写入FLWT.FLWT[2:0]位。

[Conditions]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(7) 当PRCR.PRC1为0时，写入访问无效

当PRCR.PRC1位为0时，不要写入本节中列出的寄存器。

[Registers]

- SBYCR, SNZCR, SNZEDCRn, SNZREQCRn, OPCCR, SOPCCR, DPSBYCR, DPSWCR, DPSIERn, DPSIFRn, DPSIGRn, SYOCDCR

(8) 当PRCR.PRC4位为0时，写访问无效

当PRCR.PRC4位为0时，不要写入本节中列出的寄存器。

[Registers]

- LPMSAR, DPFSAR

10.10.2 IO端口引脚状态

软件待机模式、深度软件待机和贪睡模式下的IO端口引脚状态，除非在贪睡模式下进行修改，否则在进入这些模式之前是相同的。因此，当输出信号保持为高时，功耗不会降低。

10.10.3 DTC、DMAC的模块停止状态

在将1写入MSTPCRA.MSTPA22之前，清除DMAC的DMAST.DMST位和DTCST.DTCST位
DTC为0。有关详细信息，请参阅第16节，DMA控制器(DMAC)和第17节，数据传输控制器(DTC)。

10.10.4 内部中断源

中断不会在模块停止状态下运行。如果在产生中断请求时设置模块停止位，则
无法清除CPU中断源或DTC或DMAC启动源。在设置模块停止位之前，始终禁用相关的中断。

10.10.5 通过DIRQnE位控制输入缓冲器

将DPSIERy.DIRQnE（y=0或1，n=0至15）位设置为1可使IRQ0-DS的相关输入缓冲器
IRQ15-DS引脚。尽管这些引脚的输入被发送到DPSIFRy.DIRQnF（y=0或1，n=0到15）位，但它们不会被发送到中断控制器(ICU)、外设模块和IO端口。

10.10.6 过渡到低功耗模式

由于MCU不支持事件唤醒，请勿进入睡眠模式、软件等低功耗模式
待机模式或深度软件待机模式通过执行WFE指令。此外，不要设置Cortex-M33内核中系统控制寄存器的SLEEPDEEP位，因为MCU不支持SLEEPDEEP的低功耗模式。

10.10.7 WFI指令的时间安排

WFI指令有可能在IO寄存器和CS区域写入完成之前执行，在这种情况下操作可能不符合预期。如果在写入IO寄存器和CS区域后立即放置WFI，则会发生这种情况。为避免此问题，请回读已写入的寄存器和CS区域以确认写入已完成。

10.10.8 Writing to the WDT/IWDT Registers by DTC or DMAC in Sleep Mode or Snooze Mode

Do not write to the WDT or IWDT registers by the DTC or DMAC while WDT or IWDT is stopped after entering Sleep mode or Snooze mode.

10.10.9 Oscillators in Snooze Mode

Oscillators that stop on entering Software Standby mode automatically restart when a trigger for switching to Snooze mode is generated. The MCU does not enter Snooze mode until all the oscillators stabilize. If in Snooze mode, you must disable oscillators that are not required in Snooze mode before entering Software Standby mode. Otherwise, the transition from Software Standby mode to Snooze mode takes longer.

10.10.10 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, the falling edge of RXD0 pin is used to switch MCU from Software Standby mode to Snooze mode when using UART of SCI0 in Snooze mode. In this case an interrupt such as SCI0_ERI, SCI0_RXI or an address mismatch event is used as the source for canceling Snooze mode. However noise on the RXD0 pin might cause the MCU to transfer from Software Standby mode to Snooze mode unexpectedly. In this case if the MCU does not receive RXD0 data after the noise, an interrupt such as SCI0_ERI or SCI0_RXI, or an address mismatch event is not generated and the MCU stays in Snooze mode. This can be avoided by using AGTn (n = 1, 3) underflow interrupt to return to Software Standby mode or Normal mode unless otherwise UART receive data is completed before AGTn (n = 1, 3) underflow. However, do not use the AGTn (n = 1, 3) underflow as a source to return to Software Standby mode during an UART communication. This causes the UART to stop the operation in a half-finished state.

10.10.11 Using UART of SCI0 in Snooze Mode

When using UART in Snooze mode, ensure that the snooze request (RXD0 falling edge) does not conflict with the wakeup requests set by the WUPEN register, otherwise UART cannot be guaranteed.

When using UART in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, PLL, PLL2, and the main clock oscillator must be stopped before entering Software Standby mode
- The RXD0 pin must be kept high before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI0 communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

10.10.12 Conditions of A/D Conversion Start in Snooze Mode

ADC120 can only be triggered by the ELC in Snooze mode. Do not use software trigger or ADTRGn (n = 0, 1) pin.

10.10.13 Conditions of CTSU in Snooze Mode

The CTSU can only be started by the ELC in Snooze mode.

10.10.14 ELC Events in Snooze Mode

This section lists available ELC events in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC120 window A/B compare match (ADC120_WCMPM)
- ADC120 window A/B compare mismatch (ADC120_WCMPUM)
- ADC121 window A/B compare match (ADC121_WCMPM)
- ADC121 window A/B compare mismatch (ADC121_WCMPUM)

10.10.8 在睡眠模式或贪睡模式下通过DTC或DMAC写入WDTIWDT寄存器 Mode

当WDT或IWDT在进入休眠模式或贪睡模式后停止时，请勿通过DTC或DMAC写入WDT或IWDT寄存器。

10.10.9 贪睡模式下的振荡器

进入软件待机模式时停止的振荡器会在生成切换到贪睡模式的触发器时自动重新启动。在所有振荡器稳定之前，MCU不会进入贪睡模式。如果处于贪睡模式，您必须在进入软件待机模式之前禁用贪睡模式中不需要的振荡器。否则，从软件待机模式到贪睡模式的转换需要更长的时间。

10.10.10 通过RXD0下降沿进入贪睡模式

当SNZCR.RXDREQEN位为1时，在贪睡模式下使用SCI0的UART时，RXD0引脚的下降沿用于将MCU从软件待机模式切换到贪睡模式。在这种情况下，中断如SCI0_ERI、SCI0_RXI或地址不匹配事件被用作取消贪睡模式的源。然而，RXD0引脚上的噪声可能会导致MCU意外地从软件待机模式转换到贪睡模式。在这种情况下，如果MCU没有收到

噪声后的RXD0数据，如SCI0_ERI或SCI0_RXI等中断，或地址不匹配事件不产生，MCU保持在贪睡模式。这可以通过使用AGTn(n=1 3)下溢中断返回到软件待机模式或正常模式来避免，除非在AGTn(n=1 3)下溢之前完成UART接收数据。但是，不要使用AGTn(n=1 3)下溢作为UART通信期间返回软件待机模式的源。这会导致UART在半完成状态下停止操作。

10.10.11 在贪睡模式下使用SCI0的UART

在Snooze模式下使用UART时，确保Snooze请求（RXD0下降沿）与WUPEN寄存器设置的唤醒请求不冲突，否则无法保证UART。

在Snooze模式下使用UART时，必须满足以下条件：

●时钟源必须是HOCO
●MOCO、PLL、PLL2和主时钟振荡器必须在进入软件待机模式之前停止
●进入软件待机模式前，RXD0引脚必须保持高电平
●在SCI0通信期间不得转换到软件待机模式
●MSTPCRC.MSTPC0位必须为1才能进入软件待机模式。

10.10.12 贪睡模式下AD转换开始的条件

ADC120只能由ELC在贪睡模式下触发。不要使用软件触发或ADTRGn(n=0 1)引脚。

10.10.13 CTSU在贪睡模式下的情况

CTSU只能由ELC在贪睡模式下启动。

10.10.14 贪睡模式下的ELC事件

本节列出了贪睡模式下可用的ELC事件。不要使用任何其他事件。如果进入贪睡模式后第一次启动外围模块，事件链接设置寄存器（ELSRn）必须设置贪睡模式进入事件（SYSTEM_SNZREQ）作为触发器。

●贪睡模式条目(SYSTEM_SNZREQ)
●DTC传输结束（DTC_DTCEND）
●ADC120窗口AB比较匹配(ADC120_WCMPM)
●ADC120窗口AB比较不匹配(ADC120_WCMPUM)
●ADC121窗口AB比较匹配(ADC121_WCMPM)
●ADC121窗口AB比较不匹配(ADC121_WCMPUM)

- Data operation circuit interrupt (DOC_DOPCI).

10.10.15 Module-Stop Bit Write Timing

It is possible that access to I/O register may be executed before the corresponding module-stop bit write completed. In this case, access to I/O register may not proceed as intended. To avoid this issue, before accessing I/O register, read back the module-stop bit that was written to confirm that the write completed.

●数据操作电路中断（DOC_DOPCI）。

10.10.15 模块停止位写时序

在相应的模块停止位写入完成之前，可能会执行对IO寄存器的访问。在这种情况下，对IO寄存器的访问可能不会按预期进行。为避免此问题，在访问IO寄存器之前，请回读已写入的模块停止位以确认写入已完成。

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11. Battery Backup Function

11.1 Overview

The MCU provides a battery backup function that maintains partial battery powering in the event of a power loss. Switching between VCC and VBATT, the battery-powered area includes RTC, SOSC, and backup memory.

During normal operation, the battery-powered area is powered by the main power supply, the VCC pin. When a VCC voltage drop is detected, the power source switches to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source switches back from VBATT to VCC.

11.1.1 Features of Battery Backup Function

The features include:

- Battery power supply switch
- Backup registers
- Time capture pin detection

11.1.2 Battery Power Supply Switch

When the voltage applied to the VCC pin drops, this feature switches the power supply from the VCC pin to the VBATT pin. When the voltage rises, it switches the power supply from the VBATT pin back to the VCC pin.

11.1.3 Backup Registers

The battery-powered area provides 128-byte backup registers. These registers retain data when power is supplied from the VBATT pin even when the VCC pin is in the power-off state.

11.1.4 Time Capture Pin Detection

The RTC detects input level changes on the time capture pin. For more information, see section 23, Realtime Clock (RTC).

Note: When VCC is < $V_{DETBATT}$ and > (VBATT + 0.6 V), the injected current flows from the VCC to the VBATT pin through an internal diode. If the power supply battery connected to the VBATT pin cannot support this current injection, for example if the battery is not rechargeable, Renesas strongly recommends that you connect through a low-voltage threshold diode between the power supply battery and the VBATT pin.

Note: You must enable voltage monitor 0 reset to use the battery backup function. The voltage monitor 0 level must be higher than the VBATT switch level.

Figure 11.1 shows the configuration of the battery backup function.

11. 电池备份功能

11.1 Overview

MCU提供电池备份功能，可在断电时保持部分电池供电。在VCC和VBATT之间切换，电池供电区域包括RTC、SOSC和备份存储器。

在正常工作期间，电池供电区域由主电源VCC引脚供电。当检测到VCC电压下降时，电源切换到专用电池备用电源引脚VBATT引脚。当电压再次上升时，电源从VBATT切换回VCC。

11.1.1 电池备份功能的特点

特点包括：

- 电池供电开关
- 备份寄存器
- 时间捕捉引脚检测

11.1.2 电池电源开关

当施加到VCC引脚的电压下降时，此功能将电源从VCC引脚切换到VBATT引脚。当电压上升时，它将电源从VBATT引脚切换回VCC引脚。

11.1.3 备份寄存器

电池供电区提供128字节的备份寄存器。这些寄存器在供电时保留数据
VBATT引脚即使在VCC引脚处于断电状态时。

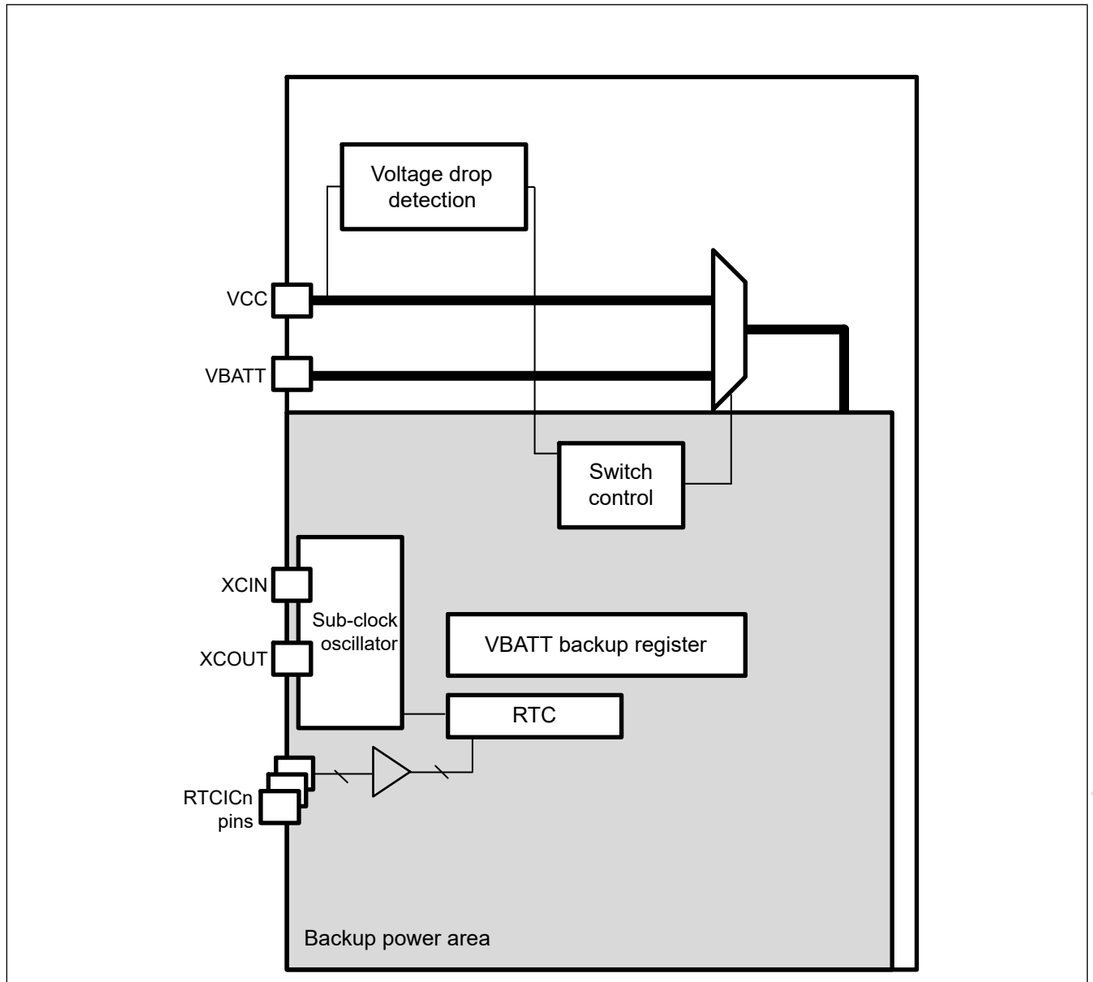
11.1.4 时间捕捉引脚检测

RTC检测时间捕捉引脚上的输入电平变化。有关详细信息，请参阅第23节，实时时钟(RTC)。

Note: 当VCC<VDETBATT且>(VBATT+0.6V)时，注入电流通过内部二极管从VCC流向VBATT引脚。如果连接到VBATT引脚的电源电池不能支持这种电流注入，例如，如果电池不可充电，瑞萨强烈建议您通过电源电池和VBATT引脚之间的低压阈值二极管进行连接。

Note: 您必须启用电压监视器0复位才能使用电池备份功能。电压监视器0电平必须高于VBATT开关电平。

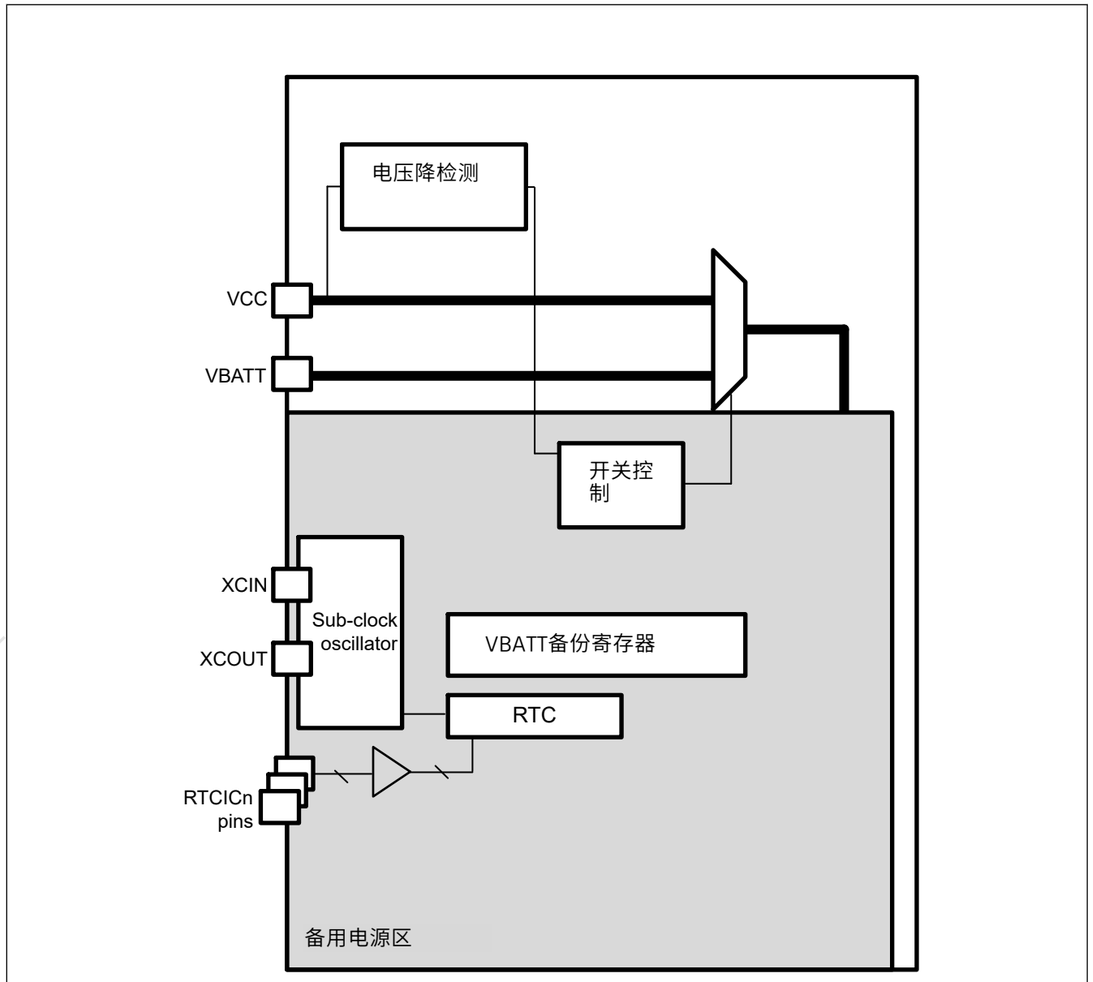
图11.1显示了电池备份功能的配置。



Note: VCC : Main power supply pin
VBATT: Battery backup power supply pin
XCIN/XCOUT: SOSC input/output
RTCICn (n = 0 to 2): Input port for battery backup function

Figure 11.1 Configuration of the battery backup function

11.2 Register Descriptions



Note: VCC:主电源引脚
VBATT：电池后备电源引脚
XCIN/XCOUT: SOSC input/output
RTCICn(n=0to2)：电池备份功能的输入端口

Figure 11.1 电池备份功能的配置

11.2 注册说明

11.2.1 BBFSAR : Battery Backup Function Security Attribute Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3D0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	NONSEC23	NONSEC22	NONSEC21	NONSEC20	NONSEC19	NONSEC18	NONSEC17	NONSEC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	Non Secure Attribute bit 0 Target register: VBATTMNSELR 0: Secure 1: Non Secure	R/W
1	NONSEC1	Non Secure Attribute bit 1 Target register: VBTBER 0: Secure 1: Non Secure	R/W
2	NONSEC2	Non Secure Attribute bit 2 Target register: VBTICTLR 0: Secure 1: Non Secure	R/W
15:3	—	These bits are read as 1. The write value should be 1.	R/W
16	NONSEC16	Non Secure Attribute bit 16 Target register: VBTBKRn (n = 0 to 15) 0: Secure 1: Non Secure	R/W
17	NONSEC17	Non Secure Attribute bit 17 Target register: VBTBKRn (n = 16 to 31) 0: Secure 1: Non Secure	R/W
18	NONSEC18	Non Secure Attribute bit 18 Target register: VBTBKRn (n = 32 to 47) 0: Secure 1: Non Secure	R/W
19	NONSEC19	Non Secure Attribute bit 19 Target register: VBTBKRn (n = 48 to 63) 0: Secure 1: Non Secure	R/W
20	NONSEC20	Non Secure Attribute bit 20 Target register: VBTBKRn (n = 64 to 79) 0: Secure 1: Non Secure	R/W
21	NONSEC21	Non Secure Attribute bit 21 Target register: VBTBKRn (n = 80 to 95) 0: Secure 1: Non Secure	R/W
22	NONSEC22	Non Secure Attribute bit 22 Target register: VBTBKRn (n = 96 to 111) 0: Secure 1: Non Secure	R/W

11.2.1 BBFSAR:电池备份功能安全属性寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3D0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	NONSEC23	NONSEC22	NONSEC21	NONSEC20	NONSEC19	NONSEC18	NONSEC17	NONSEC16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	NONSEC2	NONSEC1	NONSEC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	NONSEC0	非安全属性位0 Target register: VBATTMNSELR 0：安全1：不安全	R/W
1	NONSEC1	非安全属性位1目标寄存器：VBTBER 0：安全1：不安全	R/W
2	NONSEC2	非安全属性位2目标寄存器：VBTICTLR 0：安全1：不安全	R/W
15:3	—	这些位被读取为1。写入值应为1。	R/W
16	NONSEC16	非安全属性位16 目标寄存器：VBTBKRn（n=0到15） 0：安全1：不安全	R/W
17	NONSEC17	非安全属性位17 目标寄存器：VBTBKRn（n=16至31） 0：安全1：不安全	R/W
18	NONSEC18	非安全属性位18 目标寄存器：VBTBKRn（n=32到47） 0：安全1：不安全	R/W
19	NONSEC19	非安全属性位19 目标寄存器：VBTBKRn（n=48到63） 0：安全1：不安全	R/W
20	NONSEC20	非安全属性位20 目标寄存器：VBTBKRn（n=64到79） 0：安全1：不安全	R/W
21	NONSEC21	非安全属性位21 目标寄存器：VBTBKRn（n=80到95） 0：安全1：不安全	R/W
22	NONSEC22	非安全属性位22 目标寄存器：VBTBKRn（n=96至111） 0：安全1：不安全	R/W

Bit	Symbol	Function	R/W
23	NONSEC23	Non Secure Attribute bit 23 Target register: VBTBKRn (n = 112 to 127) 0: Secure 1: Non Secure	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The BBFSAR register controls the secure attribute of the battery backup function registers.

NONSEC0 bit (Non Secure Attribute bit 0)

This bit controls the security attribute of VBATTMNSELR.

NONSEC1 bit (Non Secure Attribute bit 1)

This bit controls the security attribute of VBTBER.

NONSEC2 bit (Non Secure Attribute bit 2)

This bit controls the security attribute of VBTICTLR.

NONSEC16 bit (Non Secure Attribute bit 16)

This bit controls the security attribute of VBTBKRn (n = 0 to 15).

NONSEC17 bit (Non Secure Attribute bit 17)

This bit controls the security attribute of VBTBKRn (n = 16 to 31).

NONSEC18 bit (Non Secure Attribute bit 18)

This bit controls the security attribute of VBTBKRn (n = 32 to 47).

NONSEC19 bit (Non Secure Attribute bit 19)

This bit controls the security attribute of VBTBKRn (n = 48 to 63).

NONSEC20 bit (Non Secure Attribute bit 20)

This bit controls the security attribute of VBTBKRn (n = 64 to 79).

NONSEC21 bit (Non Secure Attribute bit 21)

This bit controls the security attribute of VBTBKRn (n = 80 to 95).

NONSEC22 bit (Non Secure Attribute bit 22)

This bit controls the security attribute of VBTBKRn (n = 96 to 111).

NONSEC23 bit (Non Secure Attribute bit 23)

This bit controls the security attribute of VBTBKRn (n = 112 to 127).

11.2.2 VBATTMNSELR : Battery Backup Voltage Monitor Function Select Register

Base address: SYSC = 0x4001_E000

Offset address: 0x41D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	VBATTMNSEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23	NONSEC23	非安全属性位23 目标寄存器：VBTBKRn（n=112至127） 0：安全1：不安全	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

BBFSAR寄存器控制电池备份功能寄存器的安全属性。

NONSEC0位（非安全属性位0）

该位控制VBATTMNSELR的安全属性。

NONSEC1位（非安全属性位1）

该位控制VBTBER的安全属性。

NONSEC2位（非安全属性位2）

该位控制VBTICTLR的安全属性。

NONSEC16位（非安全属性位16）

该位控制VBTBKRn（n=0到15）的安全属性。

NONSEC17位（非安全属性位17）

该位控制VBTBKRn（n=16到31）的安全属性。

NONSEC18位（非安全属性位18）

该位控制VBTBKRn（n=32到47）的安全属性。

NONSEC19位（非安全属性位19）

该位控制VBTBKRn（n=48到63）的安全属性。

NONSEC20位（非安全属性位20）

该位控制VBTBKRn（n=64到79）的安全属性。

NONSEC21位（非安全属性位21）

该位控制VBTBKRn（n=80到95）的安全属性。

NONSEC22位（非安全属性位22）

该位控制VBTBKRn（n=96到111）的安全属性。

NONSEC23位（非安全属性位23）

该位控制VBTBKRn（n=112到127）的安全属性。

11.2.2 VBATTMNSELR：电池备用电压监控功能选择寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x41D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	VBATTMNSEL
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	VBATTMNSEL	VBATT Low Voltage Detect Function Select Bit 0: Disables VBATT low voltage detect function 1: Enables VBATT low voltage detect function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

VBATTMNSELR is the register which controls VBATT low voltage detect function.

This register is initialized by all reset sources including deep software standby reset.

VBATTMNSEL bit (VBATT Low Voltage Detect Function Select Bit)

Select VBATT low voltage detect function

Consumption current increases while VBATTMNSEL = 1. So, after monitoring the VBATT voltage level, clear VBATTMNSEL to 0 in order to reduce power consumption of VBATT power supply.

11.2.3 VBATTMONR : Battery Backup Voltage Monitor Register

Base address: SYSC = 0x4001_E000

Offset address: 0x41E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	VBATTMON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	VBATTMON	VBATT Voltage Monitor Bit Check VBATT voltage level 0 can be read when VBATT Low Voltage Detect Function Select Bit is 0. 0: VBATT ≥ Vbattldet*1 1: VBATT < Vbattldet	R
7:1	—	These bits are read as 0.	R

Note 1. Vbattldet is VBATT low voltage detection level . For more details, see section 53, Electrical Characteristics.

VBATTMONR is the register that can check VBATT voltage level when VBATTMNSELR.VBATTMNSEL = 1 and also VCC is supplied.

This register is initialized by all reset sources including deep software standby reset.

VBATTMON bit (VBATT Voltage Monitor Bit)

Monitor VBATT voltage level

11.2.4 VBTBER : VBATT Backup Enable Register

Base address: SYSC = 0x4001_E000

Offset address: 0x4C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	VBAE	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
0	VBATTMNSEL	VBATT低电压检测功能选择位 0：禁用VBATT低电压检测功能1：启用VBATT低电压检测功能	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
- 允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

VBATTMNSELR是控制VBATT低电压检测功能的寄存器。

该寄存器由所有复位源初始化，包括深度软件待机复位。

VBATTMNSEL位（VBATT低电压检测功能选择位）

选择VBATT低电压检测功能

VBATTMNSEL=1时消耗电流增加。因此，在监测VBATT电压电平后，清除VBATTMNSEL为0以降低VBATT电源的功耗。

11.2.3 VBATTMONR:电池备用电压监控寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x41E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	VBATTMON
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	VBATTMON	VBATT电压监控位检查当VBATT低电压检测功能选择位为0时，可以读取VBATT电压电平0。 0: VBATT ≥ Vbattldet*1 1: VBATT < Vbattldet	R
7:1	—	这些位读为0。	R

注1.Vbattldet为VBATT低电压检测电平。有关详细信息，请参阅第53节，电气特性。

VBATTMONR是当VBATTMNSELR.VBATTMNSEL=1时可以检查VBATT电压电平的寄存器。提供VCC。

该寄存器由所有复位源初始化，包括深度软件待机复位。

VBATTMON位（VBATT电压监控位）

监控VBATT电压电平

11.2.4 VBTBER:VBATT备份使能寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x4C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	VBAE	—	—	—
重置后的值:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	VBAE	VBATT backup register access enable bit 0: Disable to access VBTBKR 1: Enable to access VBTBKR	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

VBAE bit (VBATT backup register access enable bit)

You must write 1 to VBAE before accessing VBTBKR and you must write 0 to VBAE after finishing all access (write or read) to VBTBKR. If you do not write 0 to VBAE, the data of VBTBKR is not kept in VBATT mode.

To access VBTBKR, wait for at least 500 ns after writing 1 to VBAE, and then access VBTBKR.

Before entering the deep software standby mode, you must write 0 to VBAE.

To enter the deep software standby mode, wait for at least 250 ns after writing 0 to VBAE, then enter the deep software standby mode.

If you do not use VBTBKR, you should change VBAE to 0 to reduce power consumption of VBTBKR.

11.2.5 VBTBKR[n] : VBATT Backup Register (n = 0 to 127)

Base address: SYSC = 0x4001_E000

Offset address: 0x500 + 0x001 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	VBTBKRn							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	VBTBKRn	VBATT Backup Register The value of this register is retained even in VBATT mode. This register is not initialized by any reset sources.	R/W

Note: If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Table 11.1 VBATT Backup Register (1 of 2)

Address	Symbol
0x4001_E500 to 0x4001_E50F	VBTBKR[0] to VBTBKR[15]
0x4001_E510 to 0x4001_E51F	VBTBKR[16] to VBTBKR[31]
0x4001_E520 to 0x4001_E52F	VBTBKR[32] to VBTBKR[47]
0x4001_E530 to 0x4001_E53F	VBTBKR[48] to VBTBKR[63]
0x4001_E540 to 0x4001_E54F	VBTBKR[64] to VBTBKR[79]
0x4001_E550 to 0x4001_E55F	VBTBKR[80] to VBTBKR[95]
0x4001_E560 to 0x4001_E56F	VBTBKR[96] to VBTBKR[111]

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	VBAE	VBATT备份寄存器访问使能位 0：禁止访问VBTBKR1：允许访问VBTBKR	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

VBAE位（VBATT备份寄存器访问使能位）

在访问VBTBKR之前必须向VBAE写入1，在完成对VBTBKR的所有访问（写入或读取）后必须向VBAE写入0。如果不向VBAE写入0，则VBTBKR的数据不会在VBATT模式下保存。

要访问VBTBKR，请在向VBAE写入1后等待至少500ns，然后再访问VBTBKR。

在进入深度软件待机模式之前，必须将0写入VBAE。

要进入深度软件待机模式，在将0写入VBAE后至少等待250ns，然后进入深度软件待机模式。

如果不使用VBTBKR，则应将VBAE更改为0，以降低VBTBKR的功耗。

11.2.5 VBTBKR[n]:VBATT备份寄存器(n=0to127)

Base address: SYSC = 0x4001_E000

Offset address: 0x500 + 0x001 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	VBTBKRn							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	VBTBKRn	VBATT备份寄存器 即使在VBATT模式下，该寄存器的值也会保留。 该寄存器不被任何复位源初始化。	R/W

Note: 如果安全属性配置为安全，●
允许安全访问，
- 忽略非安全访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

Table 11.1 VBATT备份寄存器(1of2)

Address	Symbol
0x4001_E500 to 0x4001_E50F	VBTBKR[0] to VBTBKR[15]
0x4001_E510 to 0x4001_E51F	VBTBKR[16] to VBTBKR[31]
0x4001_E520 to 0x4001_E52F	VBTBKR[32] to VBTBKR[47]
0x4001_E530 to 0x4001_E53F	VBTBKR[48] to VBTBKR[63]
0x4001_E540 to 0x4001_E54F	VBTBKR[64] to VBTBKR[79]
0x4001_E550 to 0x4001_E55F	VBTBKR[80] to VBTBKR[95]
0x4001_E560 to 0x4001_E56F	VBTBKR[96] to VBTBKR[111]

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Table 11.1 VBATT Backup Register (2 of 2)

Address	Symbol
0x4001_E570 to 0x4001_E57F	VBTBKR[112] to VBTBKR[127]

11.2.6 VBTICTLR : VBATT Input Control Register

Base address: SYSC = 0x4001_E000

Offset address: 0x4BB

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	VCH2INEN	VCH1INEN	VCH0INEN
Value after reset:	0	0	0	0	0	x	x	x

Bit	Symbol	Function	R/W
0	VCH0INEN	VBATT CH0 Input Enable 0: RTCIC0 input disable 1: RTCIC0 input enable	R/W
1	VCH1INEN	VBATT CH1 Input Enable 0: RTCIC1 input disable 1: RTCIC1 input enable	R/W
2	VCH2INEN	VBATT CH2 Input Enable 0: RTCIC2 input disable 1: RTCIC2 input enable	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

VBTICTLR is the register that can select VBATT I/O direction as input. This register is not initialized by any reset.

VCHnINEN bits (VBATT CHn Input Enable Bits) (n = 0 to 2)

The VCHnINEN bit enables the input direction on the associated VBATT channel.

11.3 Operation

11.3.1 Battery Backup Function

When the voltage on the VCC pin drops, power can be supplied to the RTC and sub-clock oscillator from the VBATT pin. When a drop of power supply from VCC pin is detected, the power connection switches from VCC pin to the VBATT pin. The power supply from the VCC pin is resumed when the voltage on the VCC pin exceeds $V_{DETBATT}$. This power supply change does not affect the RTC operation.

You must enable voltage monitor 0 reset to use the battery backup function. The RTC supports time capture detection, triggered by a change of the time capture pin input level.

The VBATT pin supplies power to the following modules:

- RTC
- Sub-clock oscillator (including XCIN and XCOUT pins)
- VBATT Backup Register

Table 11.2 shows the operating states in VBATT mode.

Table 11.1 VBATT备份寄存器(2of2)

Address	Symbol
0x4001_E570 to 0x4001_E57F	VBTBKR[112] to VBTBKR[127]

11.2.6 VBTICTLR:VBATT输入控制寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x4BB

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	VCH2INEN	VCH1INEN	VCH0INEN
重置后的值:	0	0	0	0	0	x	x	x

Bit	Symbol	Function	R/W
0	VCH0INEN	VBATTCH0输入使能 0：RTCIC0输入禁止1：RTCIC0输入使能	R/W
1	VCH1INEN	VBATTCH1输入使能 0：RTCIC1输入禁止1：RTCIC1输入使能	R/W
2	VCH2INEN	VBATTCH2输入使能 0：RTCIC2输入禁止1：RTCIC2输入使能	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 在重写该寄存器之前将PRCR.PRC1位设置为1（允许写入）。

VBTICTLR是可以选择VBATTIO方向作为输入的寄存器。该寄存器不会被任何复位初始化。

VCHnINEN位（VBATTCHn输入使能位）（n=0到2）

VCHnINEN位使能相关VBATT通道上的输入方向。

11.3 Operation

11.3.1 电池备份功能

当VCC引脚上的电压下降时，可以从VBATT引脚为RTC和副时钟振荡器供电。当检测到来自VCC引脚的电源下降时，电源连接从VCC引脚切换到VBATT引脚。当VCC引脚上的电压超过VDETBATT时，重新从VCC引脚供电。此电源更改不会影响RTC操作。

您必须启用电压监视器0复位才能使用电池备份功能。RTC支持时间捕捉检测，由时间捕捉引脚输入电平的变化触发。

VBATT引脚为以下模块供电：

- RTC
- ●副时钟振荡器（包括XCIN和XCOUT引脚）
- ●VBATT备份寄存器

表11.2显示了VBATT模式下的操作状态。

Table 11.2 Operating States in VBATT Mode

Operating state	VBATT Mode
Transition condition	Detection of VCC voltage drop
Canceling method other than reset	Detection of VCC voltage rise
State after cancellation by an interrupt	—
State after cancellation by a reset	—
Main clock oscillator	Stop
Sub-clock oscillator	Operating
High-speed on-chip oscillator	Stop
Middle-speed on-chip oscillator	Stop
Low-speed on-chip oscillator	Stop
IWDT-dedicated on-chip oscillator	Stop
PLL	Stop
PLL2	Stop
CPU	Stop (Undefined)
SRAM (ECC RAM included)	Stop (Undefined)
Standby SRAM	Stop (Undefined)
VBATT Backup Register	Stop (Retained)
Flash memory	Stop (Retained)
Realtime clock (RTC)	Selectable when selecting clock which is operating as the count source.
AGTn (n = 0 to 3)	Stop (Undefined)
Low voltage detection circuit (LVD)	Stop
Power-on reset circuit	Stop
Other Peripheral modules	Stop (Undefined)
I/O ports	RTCICn ports (n = 0 to 2): Operating All ports not specified here: Undefined

Note: Selectable means that operating or stopped is selectable in the control registers. Some modules are also controlled by the associated module-stop bit.
Note: Stop (retained) means that the contents of the internal registers are retained but the operations are suspended.
Note: Stop (undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.

Figure 11.2 shows switching sequence of Battery backup function.

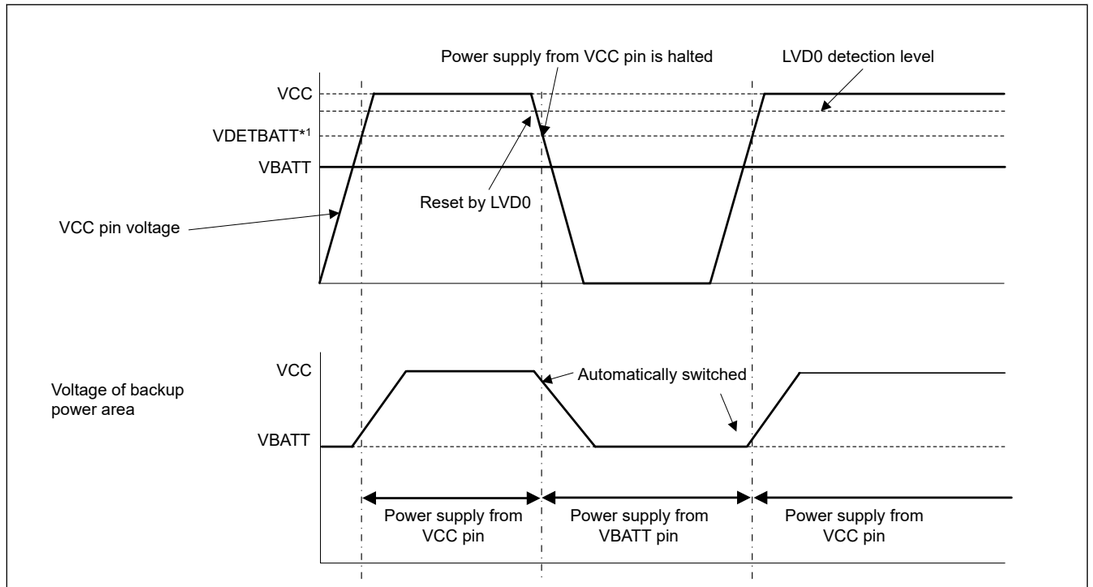
Table 11.2 VBATT模式下的操作状态

运行状态	VBATT Mode
过渡条件	检测VCC电压降
复位以外的取消方法	检测VCC电压上升
中断取消后的状态	—
通过复位取消后的状态	—
主时钟振荡器	Stop
Sub-clock oscillator	Operating
High-speed on-chip oscillator	Stop
Middle-speed on-chip oscillator	Stop
Low-speed on-chip oscillator	Stop
IWDT-dedicated on-chip oscillator	Stop
PLL	Stop
PLL2	Stop
CPU	Stop (Undefined)
SRAM (ECC RAM included)	Stop (Undefined)
Standby SRAM	Stop (Undefined)
VBATT备份寄存器	Stop (Retained)
闪存	Stop (Retained)
实时时钟(RTC)	选择用作计数源的时钟时可选择。
AGTn (n = 0 to 3)	Stop (Undefined)
低电压检测电路（LVD）	Stop
上电复位电路	Stop
其他外围模块	Stop (Undefined)
I/O ports	RTCICn端口（n=0到2）：工作 此处未指定的所有端口：未定义

Note: 可选意味着在控制寄存器中可以选择操作或停止。一些模块也由相关的模块停止位控制。

Note: 停止（retained）是指内部寄存器的内容被保留但操作被暂停。
Note: 停止（未定义）表示内部寄存器的内容未定义，内部电路的电源被切断。

图11.2显示了电池备份功能的切换顺序。



Note: For details, see section 53, Electrical Characteristics.
Note 1. $V_{DETBATT}$ indicates the threshold level of the power supply change between the VCC pin and the VBATT pin.

Figure 11.2 Switching sequence of Battery backup function.

11.3.2 VBATT Battery Power Supply Switch Usage

The battery power supply switch can switch the power supply from the VCC pin to the VBATT pin when the voltage being applied to the VCC pin drops. When the voltage rises, this switch changes the power supply from the VBATT pin to the VCC pin.

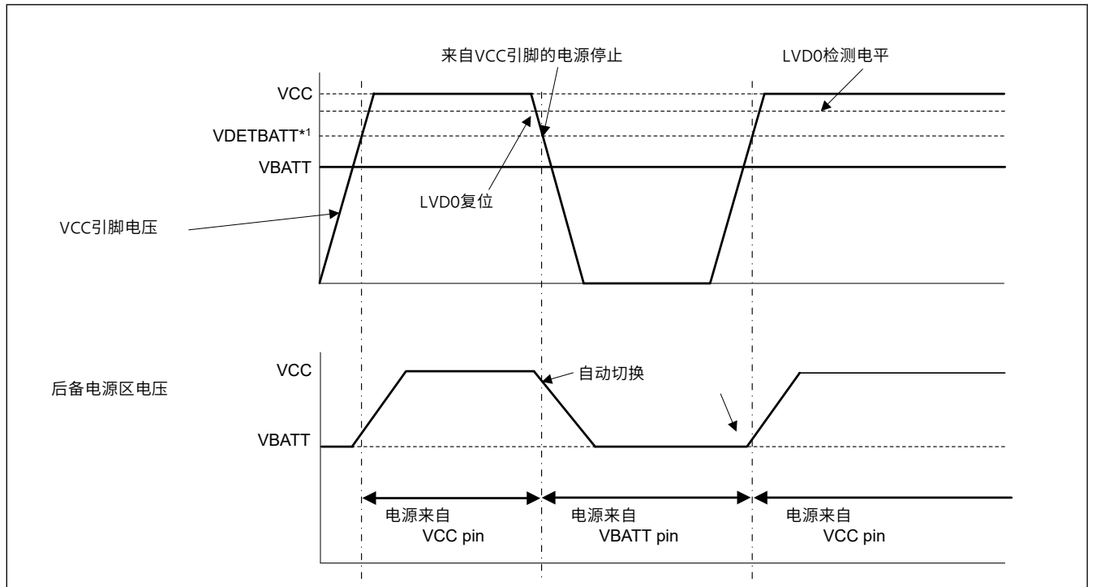
Note: The battery backup function should be used after the voltage monitor 0 reset is enabled (OFS1.LVDAS bit is 0). Voltage monitor 0 level should be higher than VBATT switch level.

11.3.3 VBATT Backup Register Usage

Use the VBATT backup registers VBTBKRn, where n = 0 to 127, to store or restore data with an 8-bit read or write operation.

11.4 Usage Notes

1. Operation of the sub-clock oscillator and RTC are not guaranteed when the voltage level on VBATT is lower than the guaranteed operation range. Initialize the RTC when the VBATT pin falls below the guaranteed operating voltage and then powers up again.
2. A reset generated while writing to registers described in this section might destroy the register value.
3. When VCC is higher than $V_{DETBATT}$, the VCC pin and VBATT pin are separated. When VCC is lower than $V_{DETBATT}$ and the switch is connected to the VBATT pin, and if the voltage on VBATT drops lower than (VCC - 0.6 V), current might flow into the VBATT pin through the parasitic diode between the VCC and VBATT pins.
4. During RTC operation using the voltage from the VBATT pin and the I/O ports within the backup, the power supply area can only be used as time capture event input pins for the RTC.



Note: 有关详细信息，请参阅第53节，电气特性。
注1.VDETBATT表示VCC引脚和VBATT引脚之间电源变化的阈值电平。

Figure 11.2 电池备份功能的切换顺序。

11.3.2 VBATT电池电源开关使用

当施加到VCC引脚的电压下降时，电池电源开关可以将电源从VCC引脚切换到VBATT引脚。当电压上升时，该开关将电源从VBATT引脚切换到VCC引脚。

Note: 电池备份功能应在电压监视器0复位使能（OFS1.LVDAS位为0）后使用。
电压监视器0电平应高于VBATT开关电平。

11.3.3 VBATT备份寄存器使用

使用VBATT备份寄存器VBTBKRn，其中n=0到127，通过8位读取或写入操作来存储或恢复数据。

11.4 使用说明

1.当VBATT上的电压电平低于保证工作范围时，不保证副时钟振荡器和RTC的工作。当VBATT引脚低于保证工作电压时初始化RTC，然后再次上电。

2.写入本节中描述的寄存器时产生的复位可能会破坏寄存器值。

3.当VCC高于VDETBATT时，VCC管脚和VBATT管脚是分开的。当VCC低于VDETBATT且开关连接到VBATT引脚时，如果VBATT上的电压低于(VCC0.6V)，电流可能会通过VCC和VBATT引脚之间的寄生二极管流入VBATT引脚。

4.RTC操作期间，使用来自VBATT引脚和备份内部IO端口的电压，电源区域只能用作RTC的时间捕捉事件输入引脚。

12. Register Write Protection

12.1 Overview

The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 12.1 lists the association between the bits in the PRCR register and the registers to be protected.

Table 12.1 Association between the bits in the PRCR register and registers to be protected

PRCR bit	Register to be protected
PRC0	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, EBCKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, CECCKDIVCR, USBCKCR, OCTACKCR, CANFDCKCR, USB60CKCR, CECCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR0, SNZEDCR1, SNZREQCR0, SNZREQCR1, OPCCR, SOPCCR, DPSBYCR, DPSWCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, SYOCDCR • Register related to the battery backup function: VBTBER, VBTICTLR, VBTBKRn (n = 0 to 127)
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVD1CMPCR, LVD2CMPCR, LVD1CR0, LVD2CR0, VBATTMNSELR
PRC4	• Registers related to the security function: CGFSAR, RSTSAR, LPMSAR, LVDSAR, BBFSAR, DPFSAR, CSAR, SRAMSAR, STBRAMSAR, DTCSAR, DMACSAR, ICUSARx, BUSSARx, MMPUSARx, TZFSAR, CPUDSAR, FSAR, PSARx, MSSAR, PmSAR, ELCSARx

12.2 Register Descriptions

12.2.1 PRCR : Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	PRC4	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	Enable writing to the registers related to the clock generation circuit 0: Disable writes 1: Enable writes	R/W
1	PRC1	Enable writing to the registers related to the low power modes, and the battery backup function 0: Disable writes 1: Enable writes	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	PRC3	Enable writing to the registers related to the LVD 0: Disable writes 1: Enable writes	R/W
4	PRC4	Enables writing to the registers related to the security function 0: Disable writes 1: Enable writes	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

12. 寄存器写保护

12.1 Overview

寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。

表12.1列出了PRCR寄存器中的位与要保护的寄存器之间的关联。

Table 12.1 PRCR寄存器中的位与要保护的寄存器之间的关联

PRCR bit	注册受保护
PRC0	• 与时钟产生电路相关的寄存器： SCKDIVCR, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, FLLCR1, FLLCR2, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, EBCKOCR, MOCOUTCR, HOCOUTCR, USBCKDIVCR, OCTACKDIVCR, CANFDCKDIVCR, USB60CKDIVCR, CECCKDIVCR, USBCKCR, OCTACKCR, CANFDCKCR, USB60CKCR, CECCKCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR
PRC1	• 与低功耗模式相关的寄存器： SBYCR, SNZCR, SNZEDCR0, SNZEDCR1, SNZREQCR0, SNZREQCR1, OPCCR, SOPCCR, DPSBYCR, DPSWCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, SYOCDCR • 与电池备份功能相关的寄存器：VBTBER VBTICT LR VBTBKRn(n=0to127)
PRC3	• 与LVD相关的寄存器： LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVD1CMPCR, LVD2CMPCR, LVD1CR0, LVD2CR0, VBATTMNSELR
PRC4	• 与安全功能相关的寄存器： CGFSAR, RSTSAR, LPMSAR, LVDSAR, BBFSAR, DPFSAR, CSAR, SRAMSAR, STBRAMSAR, DTCSAR, DMACSAR, ICUSARx, BUSSARx, MMPUSARx, TZFSAR, CPUDSAR, FSAR, PSARx, MSSAR, PmSAR, ELCSARx

12.2 注册说明

12.2.1 PRCR:保护寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x3FE

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	PRC4	PRC3	—	PRC1	PRC0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRC0	允许写入与时钟生成电路相关的寄存器 0：禁用写入1： 启用写入	R/W
1	PRC1	允许写入与低功耗模式相关的寄存器，以及电池备份功能 0：禁用写入1： 启用写入	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	PRC3	允许写入与LVD相关的寄存器 0：禁用写入1： 启用写入	R/W
4	PRC4	允许写入与安全功能相关的寄存器 0：禁用写入1： 启用写入	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
15:8	PRKEY[7:0]	PRC Key Code These bits control the write access to the PRCR register. To modify the PRCR register, write 0xA5 to the upper 8 bits and the target value to the lower 8 bits as a 16-bit unit.	W

PRCn bits (Protect bit n) (n = 0, 1, 3, 4)

The PRCn bits enable or disable writing to the protected registers listed in Table 12.1. Setting the PRCn bits to 1 or 0 enables or disables writing, respectively.

The register controlled by PRC4 may not reflect the PRC4 change when PRCR and its controlled registers are continuously written access. Avoid continuous write access or read the PRCR after PRC4 change, and then write access the PRC4-controlled register.

Bit	Symbol	Function	R/W
15:8	PRKEY[7:0]	中华人民共和国密钥代码 这些位控制对PRCR寄存器的写访问。修改PRCR寄存器，将0xA5写入高8位，将目标值写入低8位，以16位为单位。	W

PRCn位（保护位n）（n=0、1、3、4）

PRCn位启用或禁用对表12.1中列出的受保护寄存器的写入。将PRCn位设置为1或0分别启用或禁用写入。

当PRCR及其受控寄存器连续写入访问时，PRC4控制的寄存器可能无法反映PRC4的变化。避免连续写访问或在PRC4更改后读取PRCR，然后再写访问PRC4控制的寄存器。

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13. Interrupt Controller Unit (ICU)

13.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

Table 13.1 lists the ICU specifications, Figure 13.1 shows a block diagram, and Table 13.2 lists the I/O pins.

Table 13.1 ICU specifications

Parameter		Description
Maskable interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 287 (select factor within event list numbers 32 to 511)
	External pin interrupts	• Interrupt detection on low level*4, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source • Digital filter function supported • 16 sources, with interrupts from IRQi (i = 0 to 15) pins.
	Interrupt requests to CPU (NVIC)	• 96 interrupt requests are output to NVIC.
	DMAC control	• The DMAC can be activated using interrupt sources*1 • The target interrupt source can be selected individually for every DMAC channels.
	DTC control	• The DTC can be activated using interrupt sources*1 • The method for selecting an interrupt source is the same as that of the interrupt request to NVIC.
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Low voltage detection 1*3	Voltage monitor 1 interrupt of the voltage monitor 1 circuit (LVD_LVD1)
	Low voltage detection 2*3	Voltage monitor 2 interrupt of the voltage monitor 2 circuit (LVD_LVD2)
	RPEST*5	Interrupt on SRAM parity error
	RECCST*5	Interrupt on SRAM ECC error
	TZFST*5	TrustZone Filter error.
	CPEST*5	Cache RAM Parity error.
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillation has stopped
	Bus master MPU error*5	Interrupt on MPU bus master error
Low power modes		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register. • Snooze mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SELSR0 and WUPEN registers. See section 13.2.17. SELSR0 : SYS Event Link Setting Register and section 13.2.18. WUPEN0 : Wake Up Interrupt Enable Register 0, section 13.2.19. WUPEN1 : Wake Up interrupt enable register 1.
TrustZone Filter		Available

Note 1. For the DMAC and DTC activation sources, see Table 13.4.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as maskable interrupts. When used as maskable interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and voltage monitor 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.

13. 中断控制器单元(ICU)

13.1 Overview

中断控制器单元(ICU)控制哪些事件信号链接到嵌套向量中断控制器(NVIC)、DMA控制器(DMAC)和数据传输控制器(DTC)模块。ICU还控制不可屏蔽的中断。

表13.1列出了ICU规格，图13.1显示了框图，表13.2列出了IO引脚。

Table 13.1 ICU规格

Parameter		Description
Maskable interrupts	外设功能中断	• 来自外围模块的中断 源数：287（在事件列表编号32到511中选择因子）
	外部引脚中断	• 低电平中断检测*4、下降沿、上升沿、上升沿和下降沿。可以为每个来源设置其中一种检测方法 • 支持数字滤波功能 • 16个源，来自IRQi（i=0到15）引脚的中断。
	对CPU的中断请求(NVIC)	• 96个中断请求输出到NVIC。
	DMAC control	• 可以使用中断源激活DMAC*1 • 可以为每个DMAC通道单独选择目标中断源。
	DTC control	• 可以使用中断源激活DTC*1 • 中断源的选择方法与中断请求相同 NVIC.
Non-maskable interrupts*2	NMI引脚中断	• 来自NMI引脚的中断 • 下降沿或上升沿中断检测 • 支持数字滤波功能
	WDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	IWDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	低电压检测1*3	电压监视器1电路的电压监视器1中断(LVD_LVD1)
	低电压检测2*3	电压监视器2电路的电压监视器2中断(LVD_LVD2)
	RPEST*5	SRAM奇偶校验错误中断
	RECCST*5	SRAMECC错误中断
	TZFST*5	TrustZone过滤器错误。
	CPEST*5	高速缓存RAM奇偶校验错误。
	振荡停止检测中断*3	检测到主振荡停止时中断
	总线主控MPU错误*5	MPU总线主机错误中断
低功耗模式		• 睡眠模式：返回由不可屏蔽中断或任何其他中断源启动 • 软件待机模式：返回由不可屏蔽的中断启动。可以在WUPEN寄存器中选择中断。 • 贪睡模式：返回由不可屏蔽的中断发起。中断可以在SELSR0和WUPEN寄存器。 请参阅第13.2.17节。SELSR0：SYS事件链接设置寄存器和第13.2.18节。乌彭0：唤醒中断使能寄存器0，第13.2.19节。WUPEN1：唤醒中断使能寄存器1。
TrustZone Filter		Available

注1.对于DMAC和DTC激活源，请参见表13.4。
注2.不可屏蔽中断只能在复位释放后启用一次。
注3：这些不可屏蔽中断也可以用作可屏蔽中断。当用作可屏蔽中断时，不要从复位状态更改NMIER寄存器的值。要启用电压监视器1和电压监视器2中断，请将LVD1CR1.IRQSEL和LVD2CR1.IRQSEL位设置为1。

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Note 4. Low level: interrupt detection is not canceled if you do not clear it after a detection.
Note 5. These non-maskable interrupt sources cannot be recovered if the request source clock is stopped during low power mode.

Figure 13.1 shows the ICU block diagram.

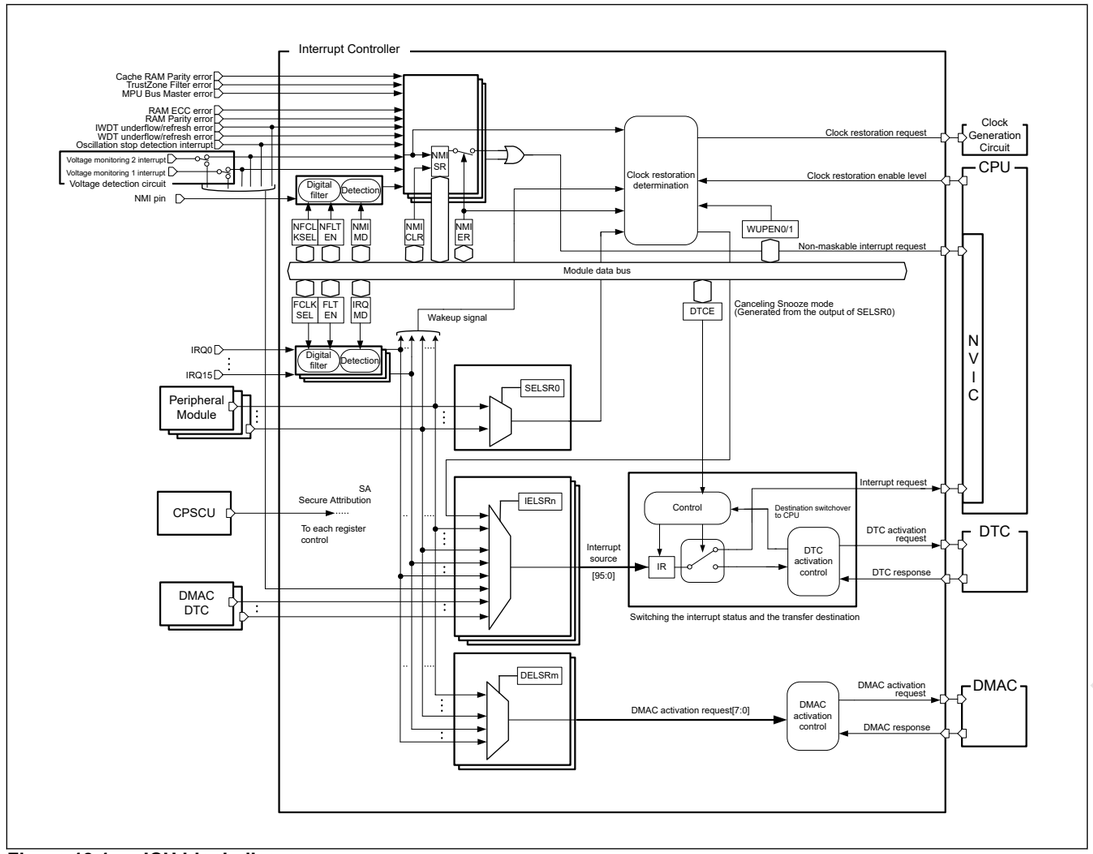

Figure 13.1 ICU block diagram

Table 13.2 lists the ICU input/output pins.

Table 13.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQi (i = 0 to 15)	Input	External interrupt request pins

13.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information about these registers, see ARM Limited., ARM® Cortex®-M33 Processor Technical Reference Manual (ARM 100230).

注4.低电平：检测后不清除中断检测不取消。
注5.如果请求源时钟在低功耗模式下停止，这些不可屏蔽的中断源将无法恢复。

图13.1显示了ICU框图。

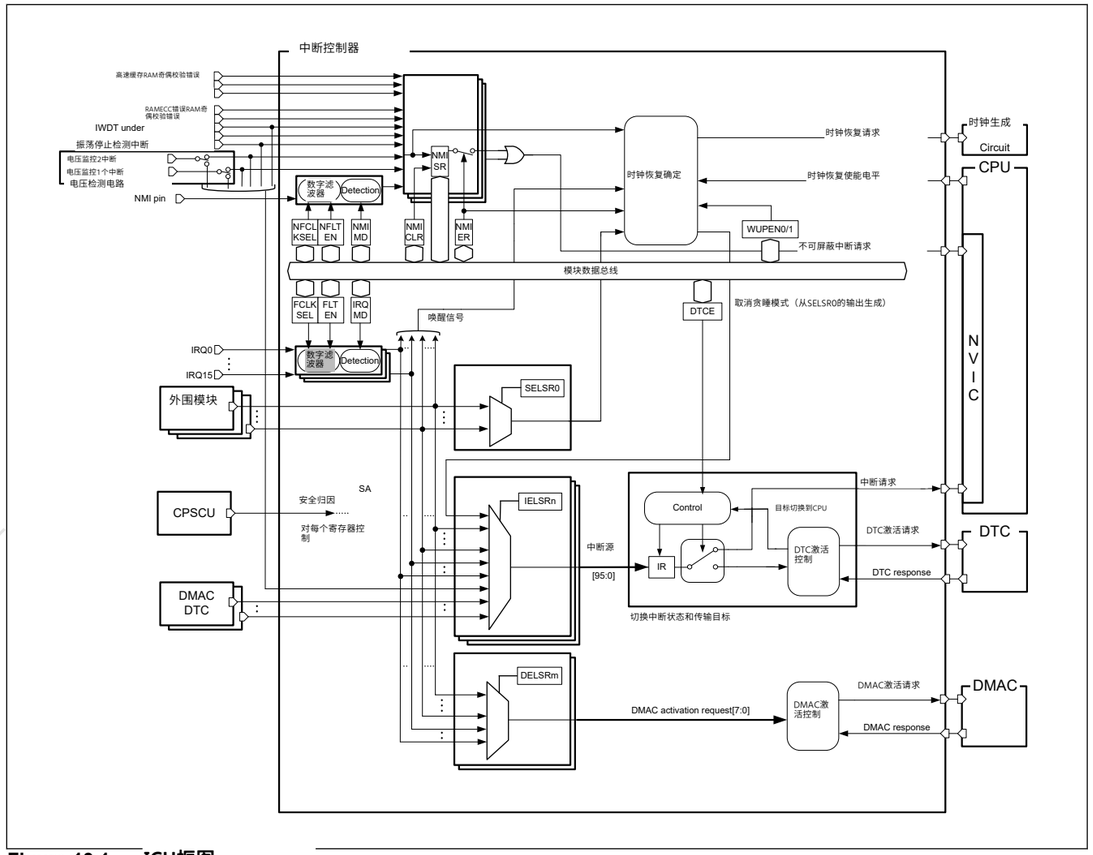

Figure 13.1 ICU框图

表13.2列出了ICU输入输出引脚。

Table 13.2 ICUIO引脚

引脚名称	I/O	Description
NMI	Input	不可屏蔽中断请求引脚
IRQi (i = 0 to 15)	Input	外部中断请求引脚

13.2 注册说明

本章不介绍Arm®NVIC内部寄存器。有关这些寄存器的信息，请参阅ARMLimited。
ARM®Cortex®-M33处理器技术参考手册(ARM100230)。

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13.2.1 ICUSARA : Interrupt Controller Unit Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIRQ CR15	SAIRQ CR14	SAIRQ CR13	SAIRQ CR12	SAIRQ CR11	SAIRQ CR10	SAIRQ CR9	SAIRQ CR8	SAIRQ CR7	SAIRQ CR6	SAIRQ CR5	SAIRQ CR4	SAIRQ CR3	SAIRQ CR2	SAIRQ CR1	SAIRQ CR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	SAIRQCR15 to SAIRQCR0	Security attributes of registers for the IRQCRn register 0: Secure 1: Non-secure	R/W
31:16	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIRQCRn bits (Security attributes of registers for the IRQCRn register)

The target registers are as follows:

- IRQCR0 to IRQCR15 registers
- WUPEN0.IRQWUPEN[15:0] bits

13.2.2 ICUSARB : Interrupt Controller Unit Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SANMI
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SANMI	Security attributes of registers for nonmaskable interrupt 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SANMI bit (Security attributes of registers for nonmaskable interrupt)

Security attributes of registers for non-maskable interrupt. The target registers are as follows:

13.2.1 ICUSARA:中断控制器单元安全属性寄存器A

Base address: CPSCU = 0x4000_8000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIRQ CR15	SAIRQ CR14	SAIRQ CR13	SAIRQ CR12	SAIRQ CR11	SAIRQ CR10	SAIRQ CR9	SAIRQ CR8	SAIRQ CR7	SAIRQ CR6	SAIRQ CR5	SAIRQ CR4	SAIRQ CR3	SAIRQ CR2	SAIRQ CR1	SAIRQ CR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	SAIRQCR15 to SAIRQCR0	IRQCRn寄存器的寄存器安全属性 0: Secure 1: Non-secure	R/W
31:16	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SAIRQCRn位（IRQCRn寄存器的寄存器安全属性）

目标寄存器如下：

●IRQCR0到IRQCR15寄存器

- WUPEN0.IRQWUPEN[15:0] bits

13.2.2 ICUSARB:中断控制器单元安全属性寄存器B

Base address: CPSCU = 0x4000_8000

Offset address: 0x44

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SANMI
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SANMI	不可屏蔽中断寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:1	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SANMI位（不可屏蔽中断的寄存器的安全属性）

不可屏蔽中断的寄存器的安全属性。目标寄存器如下：

- NMIER
- NMICLR
- NMICR

The value of AIRCR.BFHFNMINS bit [13] in Application Interrupt and Reset Control Register of ARM CPU should be the same as the value of security attribution. The initial values of AIRCR.BFHFNMINS and the SANMI bits are different. AIRCR.BFHFNMINS is secure and SANMI is non-secure. Polarity has the same meaning so program these to match.

Note: Only one of Secure and Non-Secure can set security attribution for non-maskable interrupt-related registers. If you program the Secure attribute as secure, it always goes to the Secure interrupt handler. To release any of the non-maskable interrupt sources to the non-secure user, write a function to execute a nonsecure program from the interrupt handler for Secure.

13.2.3 ICUSARC : Interrupt Controller Unit Security Attribution Register C

Base address: CPSCU = 0x4000_8000

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SADMAC7	SADMAC6	SADMAC5	SADMAC4	SADMAC3	SADMAC2	SADMAC1	SADMAC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SADMAC7 to SADMAC0	Security attributes of registers for DMAC channel 0: Secure 1: Non-secure	R/W
31:8	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SADMACn bits (Security attributes of registers for DMAC channel)

Security attributes of registers for DMAC channel. This register is referred to as the security attribute of the ICU and DMAC registers.

The controlled ICU register is:

- DELSRn

The controlled DMAC registers are:

- DMACn.DMSAR
- DMACn.DMSRR
- DMACn.DMDAR
- DMACn.DMDRR
- DMACn.DMCRA
- DMACn.DMCRB
- DMACn.DMTMD
- DMACn.DMINT
- DMACn.DMAMD

- NMIER
- NMICLR
- NMICR

ARMCPU的应用中断和复位控制寄存器AIRCR.BFHFNMINSbit[13]的值应与安全属性的值相同。AIRCR.BFHFNMINS和SANMI位的初始值不同。AIRCR.BFHFNMINS是安全的，而SANMI是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

Note: 只有Secure和Non-Secure之一可以为不可屏蔽的中断相关寄存器设置安全属性。如果您将Secure属性编程为安全，则它始终会转到Secure中断处理程序。要将任何不可屏蔽的中断源释放给非安全用户，请编写一个函数以从Secure的中断处理程序执行非安全程序。

13.2.3 ICUSARC:中断控制器单元安全属性寄存器C

Base address: CPSCU = 0x4000_8000

Offset address: 0x48

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SADMAC7	SADMAC6	SADMAC5	SADMAC4	SADMAC3	SADMAC2	SADMAC1	SADMAC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	SADMAC7 to SADMAC0	DMAC通道寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:8	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SADMACn位（DMAC通道寄存器的安全属性）

DMAC通道寄存器的安全属性。该寄存器被称为ICU的安全属性和
DMAC registers.

受控ICU寄存器为：

- DELSRn

受控的DMAC寄存器是：

- DMACn.DMSAR
- DMACn.DMSRR
- DMACn.DMDAR
- DMACn.DMDRR
- DMACn.DMCRA
- DMACn.DMCRB
- DMACn.DMTMD
- DMACn.DMINT
- DMACn.DMAMD

- DMACn.DMOFR
- DMACn.DMCNT
- DMACn.DMREQ
- DMACn.DMSTS
- DMACn.DMSBS
- DMACn.DMDBS
- DMACn.DMBWR

For details on DMAC registers, see section 16, DMA Controller (DMAC).

13.2.4 ICUSARD : Interrupt Controller Unit Security Attribution Register D

Base address: CPSCU = 0x4000_8000

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SASELSR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SASELSR0	Security attributes of registers for SELSR0 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

13.2.5 ICUSARE : Interrupt Controller Unit Security Attribution Register E

Base address: CPSCU = 0x4000_8000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIIC0WUP	SAAGT1CBWUP	SAAGT1CAWUP	SAAGT1UDWUP	SAUSBFS0WUP	SAUSBHSWUP	SARTCPRDWUP	SARTCALMWUP	—	—	—	—	SALVD2WUP	SALVD1WUP	—	SAIWDTWUP
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	—	These bits are read as 1. The write value should be 1.	R/W

- DMACn.DMOFR
- DMACn.DMCNT
- DMACn.DMREQ
- DMACn.DMSTS
- DMACn.DMSBS
- DMACn.DMDBS
- DMACn.DMBWR

有关DMAC寄存器的详细信息，请参见第16节，DMA控制器(DMAC)。

13.2.4 ICUSARD:中断控制器单元安全属性寄存器D

Base address: CPSCU = 0x4000_8000

Offset address: 0x4C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SASELSR0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SASELSR0	SELSR0寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:1	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

13.2.5 ICUSARE:中断控制器单元安全属性寄存器E

Base address: CPSCU = 0x4000_8000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIIC0WUP	SAAGT1CBWUP	SAAGT1CAWUP	SAAGT1UDWUP	SAUSBFS0WUP	SAUSBHSWUP	SARTCPRDWUP	萨特冷静WUP	—	—	—	—	SALVD2WUP	SALVD1WUP	—	SAIWDTWUP
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	—	这些位被读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
16	SAIWDTWUP	Security attributes of registers for WUPEN0.b16 0: Secure 1: Non-secure	R/W
17	—	This bit is read as 1. The write value should be 1.	R/W
18	SALVD1WUP	Security attributes of registers for WUPEN0.b18 0: Secure 1: Non-secure	R/W
19	SALVD2WUP	Security attributes of registers for WUPEN0.b19 0: Secure 1: Non-secure	R/W
23:20	—	These bits are read as 1. The write value should be 1.	R/W
24	SARTCALMWUP	Security attributes of registers for WUPEN0.b24 0: Secure 1: Non-secure	R/W
25	SARTCPRDWUP	Security attributes of registers for WUPEN0.b25 0: Secure 1: Non-secure	R/W
26	SAUSBHSWUP	Security attributes of registers for WUPEN0.b26 0: Secure 1: Non-secure	R/W
27	SAUSBFS0WUP	Security attributes of registers for WUPEN0.b27 0: Secure 1: Non-secure	R/W
28	SAAGT1UDWUP	Security attributes of registers for WUPEN0.b28 0: Secure 1: Non-secure	R/W
29	SAAGT1CAWUP	Security attributes of registers for WUPEN0.b29 0: Secure 1: Non-secure	R/W
30	SAAGT1CBWUP	Security attributes of registers for WUPEN0.b30 0: Secure 1: Non-secure	R/W
31	SAIIC0WUP	Security attributes of registers for WUPEN0.b31 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

13.2.6 ICUSARF : Interrupt Controller Unit Security Attribution Register F

Base address: CPSCU = 0x4000_8000
Offset address: 0x54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SAAGT3CBWUP	SAAGT3CAWUP	SAAGT3UDWUP
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
16	SAIWDTWUP	WUPEN0.b16寄存器的安全属性 0: Secure 1: Non-secure	R/W
17	—	该位读取为1。写入值应为1。	R/W
18	SALVD1WUP	WUPEN0.b18寄存器的安全属性 0: Secure 1: Non-secure	R/W
19	SALVD2WUP	WUPEN0.b19寄存器的安全属性 0: Secure 1: Non-secure	R/W
23:20	—	这些位被读取为1。写入值应为1。	R/W
24	SARTCALMWUP	WUPEN0.b24寄存器的安全属性 0: Secure 1: Non-secure	R/W
25	SARTCPRDWUP	WUPEN0.b25寄存器的安全属性 0: Secure 1: Non-secure	R/W
26	SAUSBHSWUP	WUPEN0.b26寄存器的安全属性 0: Secure 1: Non-secure	R/W
27	SAUSBFS0WUP	WUPEN0.b27寄存器的安全属性 0: Secure 1: Non-secure	R/W
28	SAAGT1UDWUP	WUPEN0.b28寄存器的安全属性 0: Secure 1: Non-secure	R/W
29	SAAGT1CAWUP	WUPEN0.b29寄存器的安全属性 0: Secure 1: Non-secure	R/W
30	SAAGT1CBWUP	WUPEN0.b30寄存器的安全属性 0: Secure 1: Non-secure	R/W
31	SAIIC0WUP	WUPEN0.b31寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

13.2.6 ICUSARF:中断控制器单元安全属性寄存器F

Base address: CPSCU = 0x4000_8000
Offset address: 0x54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SAAGT3CBWUP	SAAGT3CAWUP	SAAGT3UDWUP
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SAAGT3UDWUP	Security attributes of registers for WUPEN1.b0 0: Secure 1: Non-secure	R/W
1	SAAGT3CAWUP	Security attributes of registers for WUPEN1.b1 0: Secure 1: Non-secure	R/W
2	SAAGT3CBWUP	Security attributes of registers for WUPEN1.b2 0: Secure 1: Non-secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

13.2.7 ICUSARG : Interrupt Controller Unit Security Attribution Register G

Base address: CPSCU = 0x4000_8000

Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR31	SAIELSR30	SAIELSR29	SAIELSR28	SAIELSR27	SAIELSR26	SAIELSR25	SAIELSR24	SAIELSR23	SAIELSR22	SAIELSR21	SAIELSR20	SAIELSR19	SAIELSR18	SAIELSR17	SAIELSR16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR15	SAIELSR14	SAIELSR13	SAIELSR12	SAIELSR11	SAIELSR10	SAIELSR9	SAIELSR8	SAIELSR7	SAIELSR6	SAIELSR5	SAIELSR4	SAIELSR3	SAIELSR2	SAIELSR1	SAIELSR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR31 to SAIELSR0	Security attributes of registers for IELSR31 to IELSR0 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR31 to IELSR0)

The Secure Attribute managed within the Arm CPU NVIC must match the security attribution of IELSEn (n = 0 to 31).
NVIC internal registers are in NVIC_ITNS0[31:0]. The initial values of NVIC_ITNS0 and ICUSARG are different.
NVIC_ITNS0 is secure and ICUSARG is non-secure. Polarity has the same meaning so program these to match.

Bit	Symbol	Function	R/W
0	SAAGT3UDWUP	WUPEN1.b0寄存器的安全属性 0: Secure 1: Non-secure	R/W
1	SAAGT3CAWUP	WUPEN1.b1寄存器的安全属性 0: Secure 1: Non-secure	R/W
2	SAAGT3CBWUP	WUPEN1.b2寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

13.2.7 ICUSARG:中断控制器单元安全属性寄存器G

Base address: CPSCU = 0x4000_8000

Offset address: 0x70

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR31	SAIELSR30	SAIELSR29	SAIELSR28	SAIELSR27	SAIELSR26	SAIELSR25	SAIELSR24	SAIELSR23	SAIELSR22	SAIELSR21	SAIELSR20	SAIELSR19	SAIELSR18	SAIELSR17	SAIELSR16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR15	SAIELSR14	SAIELSR13	SAIELSR12	SAIELSR11	SAIELSR10	SAIELSR9	SAIELSR8	SAIELSR7	SAIELSR6	SAIELSR5	SAIELSR4	SAIELSR3	SAIELSR2	SAIELSR1	SAIELSR0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR31 to SAIELSR0	IELSR31到IELSR0寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

SAIELSRn位（IELSR31至IELSR0寄存器的安全属性）

ArmCPUNVIC中管理的安全属性必须与IELSEn的安全属性匹配（n=0到31）。
NVIC内部寄存器位于NVIC_ITNS0[31:0]。NVIC_ITNS0和ICUSARG的初始值不同。
NVIC_ITNS0是安全的，而ICUSARG是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

13.2.8 ICUSARH : Interrupt Controller Unit Security Attribution Register H

Base address: CPSCU = 0x4000_8000

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR63	SAIELSR62	SAIELSR61	SAIELSR60	SAIELSR59	SAIELSR58	SAIELSR57	SAIELSR56	SAIELSR55	SAIELSR54	SAIELSR53	SAIELSR52	SAIELSR51	SAIELSR50	SAIELSR49	SAIELSR48
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR47	SAIELSR46	SAIELSR45	SAIELSR44	SAIELSR43	SAIELSR42	SAIELSR41	SAIELSR40	SAIELSR39	SAIELSR38	SAIELSR37	SAIELSR36	SAIELSR35	SAIELSR34	SAIELSR33	SAIELSR32
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR63 to SAIELSR32	Security attributes of registers for IELSR63 to IELSR32 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR63 to IELSR32)

The Secure Attribute managed within the ARM CPU NVIC must match the security attribution of IELSEn (n = 32 to 63).
NVIC internal registers are in NVIC_ITNS1[31:0]. The initial values of NVIC_ITNS1 and ICUSARH are different.
NVIC_ITNS1 is secure and ICUSARH is non-secure. Polarity has the same meaning so program these to match.

13.2.9 ICUSARI : Interrupt Controller Unit Security Attribution Register I

Base address: CPSCU = 0x4000_8000

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR95	SAIELSR94	SAIELSR93	SAIELSR92	SAIELSR91	SAIELSR90	SAIELSR89	SAIELSR88	SAIELSR87	SAIELSR86	SAIELSR85	SAIELSR84	SAIELSR83	SAIELSR82	SAIELSR81	SAIELSR80
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR79	SAIELSR78	SAIELSR77	SAIELSR76	SAIELSR75	SAIELSR74	SAIELSR73	SAIELSR72	SAIELSR71	SAIELSR70	SAIELSR69	SAIELSR68	SAIELSR67	SAIELSR66	SAIELSR65	SAIELSR64
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR95 to SAIELSR64	Security attributes of registers for IELSR95 to IELSR64 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

SAIELSRn bits (Security attributes of registers for IELSR95 to IELSR64)

The Secure Attribute managed within the ARM CPU NVIC must match the security attribution of IELSEn (n = 64 to 95).
NVIC internal registers are in NVIC_ITNS2[31:0]. The initial values of NVIC_ITNS2 and ICUSARI are different.
NVIC_ITNS2 is secure and ICUSARI is non-secure. Polarity has the same meaning so program these to match.

13.2.8 ICUSARH：中断控制器单元安全属性寄存器H

Base address: CPSCU = 0x4000_8000

Offset address: 0x74

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR63	SAIELSR62	SAIELSR61	SAIELSR60	SAIELSR59	SAIELSR58	SAIELSR57	SAIELSR56	SAIELSR55	SAIELSR54	SAIELSR53	SAIELSR52	SAIELSR51	SAIELSR50	SAIELSR49	SAIELSR48
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR47	SAIELSR46	SAIELSR45	SAIELSR44	SAIELSR43	SAIELSR42	SAIELSR41	SAIELSR40	SAIELSR39	SAIELSR38	SAIELSR37	SAIELSR36	SAIELSR35	SAIELSR34	SAIELSR33	SAIELSR32
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR63 to SAIELSR32	IELSR63到IELSR32寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SAIELSRn位（IELSR63至IELSR32寄存器的安全属性）

在ARMCPUNVIC中管理的安全属性必须与IELSEn的安全属性匹配（n=32到63）。
NVIC内部寄存器位于NVIC_ITNS1[31:0]中。NVIC_ITNS1和ICUSARH的初始值不同。
NVIC_ITNS1是安全的，而ICUSARH是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

13.2.9 ICUSARI:中断控制器单元安全属性寄存器I

Base address: CPSCU = 0x4000_8000

Offset address: 0x78

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SAIELSR95	SAIELSR94	SAIELSR93	SAIELSR92	SAIELSR91	SAIELSR90	SAIELSR89	SAIELSR88	SAIELSR87	SAIELSR86	SAIELSR85	SAIELSR84	SAIELSR83	SAIELSR82	SAIELSR81	SAIELSR80
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SAIELSR79	SAIELSR78	SAIELSR77	SAIELSR76	SAIELSR75	SAIELSR74	SAIELSR73	SAIELSR72	SAIELSR71	SAIELSR70	SAIELSR69	SAIELSR68	SAIELSR67	SAIELSR66	SAIELSR65	SAIELSR64
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	SAIELSR95 to SAIELSR64	IELSR95到IELSR64寄存器的安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

SAIELSRn位（IELSR95至IELSR64寄存器的安全属性）

ARMCPUNVIC中管理的安全属性必须与IELSEn的安全属性相匹配（n=64到95）。
NVIC内部寄存器位于NVIC_ITNS2[31:0]中。NVIC_ITNS2和ICUSARI的初始值不同。
NVIC_ITNS2是安全的，而ICUSARI是不安全的。极性具有相同的含义，因此请对它们进行编程以匹配。

13.2.10 IRQCRi : IRQ Control Register (i = 0 to 15)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi Detection Sense Select 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
5:4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	FLTEN	IRQi Digital Filter Enable 0: Digital filter is disabled 1: Digital filter is enabled.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

IRQCRi register changes must satisfy the following conditions:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register value before setting the target IELSRn register (n = 0 to 95).
  You can change the register values only when the value of the target IELSRn register is 0x0000.
- For a DMAC trigger:
  Change the IRQCRi register value before setting the target DELSRn register (n = 0 to 7).
  You can change the register values only when the value of the target DELSRn register is 0x0000.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN0.IRQWUPEN[n] (n = 0 to 15). You can only change the register values when the target WUPEN0.IRQWUPEN[n] is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the IRQi external pin interrupt sources. For more information about the settings, see section 13.5.6. External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the IRQi external pin interrupt request pins, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 13.5.5. Digital Filter.

13.2.10 IRQCRi:IRQ控制寄存器(i=0to15)

Base address: ICU = 0x4000_6000

Offset address: 0x000 + 0x1 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	IRQMD[1:0]	IRQi检测检测选择 00：下降沿01：上升沿10： 上升沿和下降沿11：低电平	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
5:4	FCLKSEL[1:0]	IRQi数字滤波器采样时钟选择 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	FLTEN	IRQi数字滤波器启用 0：禁用数字滤波器1：启 用数字滤波器。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

IRQCRi寄存器变更必须满足以下条件：

●对于CPU中断或DTC触发：
在设置目标IELSRn寄存器（n=0到95）之前更改IRQCRi寄存器值。
仅当目标IELSRn寄存器的值为0x0000时才能更改寄存器值。

- For a DMAC trigger:
  在设置目标DELSRn寄存器（n=0到7）之前更改IRQCRi寄存器值。
  只有当目标DELSRn寄存器的值为0x0000时，才能更改寄存器值。

●对于唤醒使能信号：
在设置目标WUPEN0.IRQWUPEN[n]（n=0到15）之前更改IRQCRi寄存器设置。当目标WUPEN0.IRQWUPEN[n]为0时，您只能更改寄存器值。

IRQMD[1:0]位（IRQi检测检测选择）

IRQMD[1:0]位设置IRQi外部引脚中断源的检测检测方法。有关设置的更多信息，请参阅第13.5.6节。外部引脚中断。

FCLKSEL[1:0]位（IRQi数字滤波器采样时钟选择）

FCLKSEL[1:0]位选择IRQi外部引脚中断请求引脚的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB/8 (once every 8 cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

关于数字滤波器的详细信息，请参阅13.5.5节。数字滤波器。

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the IRQi external pin interrupt sources. The digital filter is enabled when the IRQCRi.FLTEN bit is 1 and disabled when the IRQCRi.FLTEN bit is 0. The IRQi pin level is sampled at the clock cycle specified in the IRQCRi.FCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 13.5.5. Digital Filter.

13.2.11 NMISR : Non-Maskable Interrupt Status Register

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEST	—	TZFST	—	BUSMST	—	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTST	IWDT Underflow/Refresh Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
1	WDTST	WDT Underflow/Refresh Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
5:4	—	These bits are read as 0.	R
6	OSTST	Oscillation Stop Detection Interrupt Status Flag 0: Interrupt not requested for main oscillation stop 1: Interrupt requested for main oscillation stop	R
7	NMIST	NMI Status Flag 0: Interrupt not requested 1: Interrupt requested	R
8	RPEST	SRAM Parity Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
9	RECCST	SRAM ECC Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
10	—	This bit is read as 0.	R
11	BUSMST	MPU Bus Master Error Interrupt Status Flag 0: Interrupt not requested 1: Interrupt requested	R
12	—	This bit is read as 0.	R
13	TZFST	TrustZone Filter Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R
14	—	This bit is read as 0.	R
15	CPEST	Cache RAM Parity Error Status Flag 0: Interrupt not requested 1: Interrupt requested	R

FLTEN位（IRQi数字滤波器使能）

FLTEN位使能用于IRQi外部引脚中断源的数字滤波器。数字滤波器在IRQCRi.FLTEN位为1时启用，在IRQCRi.FLTEN位为0时禁用。IRQi引脚电平在IRQCRi.FCLKSEL[1:0]位指定的时钟周期内采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。关于数字滤波器的详细信息，请参阅13.5.5节。数字滤波器。

13.2.11 NMISR：不可屏蔽中断状态寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEST	—	TZFST	—	BUSMST	—	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTST	IWDT下溢刷新错误状态标志 0：未请求中断1：请求中断	R
1	WDTST	WDT下溢刷新错误状态标志 0：未请求中断1：请求中断	R
2	LVD1ST	电压监视器1中断状态标志 0：未请求中断1：请求中断	R
3	LVD2ST	电压监视器2中断状态标志 0：未请求中断1：请求中断	R
5:4	—	这些位读为0。	R
6	OSTST	振荡停止检测中断状态标志 0：主振荡停止时不请求中断1：主振荡停止时请求中断	R
7	NMIST	NMI状态标志 0：未请求中断1：请求中断	R
8	RPEST	SRAM奇偶校验错误中断状态标志 0：未请求中断1：请求中断	R
9	RECCST	SRAMECC错误中断状态标志 0：未请求中断1：请求中断	R
10	—	该位读为0。	R
11	BUSMST	MPU总线主机错误中断状态标志 0：未请求中断1：请求中断	R
12	—	该位读为0。	R
13	TZFST	TrustZone过滤器错误状态标志 0：未请求中断1：请求中断	R
14	—	该位读为0。	R
15	CPEST	高速缓存RAM奇偶校验错误状态标志 0：未请求中断1：请求中断	R

RA生态工作室

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests are generated during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

The IWDTST flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

When the IWDT underflow/refresh error interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Status Flag)

The WDTST flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

When the WDT underflow/refresh error interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

When the voltage monitor 1 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates a request for voltage monitor 2 interrupt. It is read-only and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

When the voltage monitor 2 interrupt is generated and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates an oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

When the main oscillation stop detection interrupt is generated.

[Clearing condition]

When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Status Flag)

The NMIST flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

When an edge specified by the NMICR.NMIMD bit is input to the NMI pin.

NMISR寄存器监视不可屏蔽中断源的状态。忽略对NMISR寄存器的写入。不可屏蔽中断使能寄存器(NMIER)中的设置不会影响该寄存器中的状态标志。在不可屏蔽中断处理程序结束之前，检查该寄存器中的所有位是否都设置为0，以确认在处理程序处理期间没有产生其他NMI请求。

IWDTST标志（IWDT下溢刷新错误状态标志）

IWDTST标志指示IWDT下溢刷新错误中断 请求。它是只读的并由NMICLR.IWDTCLR bit.

[Setting condition]

当IWDT下溢刷新错误中断 产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.IWDTCLR位时。

WDTST标志（WDT下溢刷新错误状态标志）

WDTST标志指示WDT下溢刷新错误中断 请求。它是只读的并由NMICLR.WDTCLR bit.

[Setting condition]

当产生WDT下溢刷新错误中断 时。

[Clearing condition]

当1写入NMICLR.WDTCLR位时。

LVD1ST标志（电压监视器1中断状态标志）

LVD1ST标志指示电压监视器1中断请求。它是只读的，由NMICLR.LVD1CLR位清零。

[Setting condition]

当电压监视器1中断产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD1CLR位时。

LVD2ST标志（电压监视器2中断状态标志）

LVD2ST标志指示电压监视器2中断请求。它是只读的，由NMICLR.LVD2CLR位清零。

[Setting condition]

当电压监视器2中断产生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD2CLR位时。

OSTST标志（振荡停止检测中断状态标志）

OSTST标志表示振荡停止检测中断请求。它是只读的并由NMICLR.OSTCLR bit.

[Setting condition]

当产生主振荡停止检测中断时。

[Clearing condition]

当1写入NMICLR.OSTCLR位时。

NMIST标志（NMI状态标志）

NMIST标志指示NMI引脚中断请求。它是只读的，由NMICLR.NMICLR位清零。

[Setting condition]

当NMICR.NMIMD位指定的边沿输入到NMI引脚时。

[Clearing condition]

When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates an SRAM parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM parity error.

[Clearing condition]

When 1 is written to the NMICLR.RPECLR bit.

RECCST flag (SRAM ECC Error Interrupt Status Flag)

The RECCST flag indicates an SRAM ECC error interrupt request.

[Setting condition]

When an interrupt is generated in response to an SRAM ECC error.

[Clearing condition]

When 1 is written to the NMICLR.RECCCLR bit.

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

The BUSMST flag indicates a bus master error interrupt request.

[Setting condition]

When an interrupt is generated in response to a bus master error.

[Clearing condition]

When 1 is written to the NMICLR.BUSMCLR bit.

TZFST flag (TrustZone Filter Error Status Flag)

This flag indicates the TrustZone Filter error interrupt request.

[Setting condition]

When an interrupt is generated in response to a TrustZone Filter error

[Clearing condition]

When 1 is written to the NMICLR.TZFCLR bit

CPEST flag (Cache RAM Parity Error Status Flag)

This flag indicates the Cache RAM Parity error interrupt request.

[Setting condition]

When an interrupt is generated in response to an Cache RAM Parity error

[Clearing condition]

When 1 is written to the NMICLR.CPECLR bit

13.2.12 NMIER : Non-Maskable Interrupt Enable Register

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEEN	—	TZFEN	—	BUSMEN	—	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Clearing condition]

当1写入NMICLR.NMICLR位时。

RPEST标志（SRAM奇偶校验错误中断状态标志）

RPEST标志指示SRAM奇偶校验错误中断请求。

[Setting condition]

当响应SRAM奇偶校验错误而产生中断时。

[Clearing condition]

当1写入NMICLR.RPECLR位时。

RECCST标志（SRAMECC错误中断状态标志）

RECCST标志指示SRAMECC错误中断请求。

[Setting condition]

当响应SRAMECC错误而产生中断时。

[Clearing condition]

当1写入NMICLR.RECCCLR位时。

BUSMST标志（MPU总线主机错误中断状态标志）

BUSMST标志指示总线主机错误中断请求。

[Setting condition]

当响应总线主机错误而产生中断时。

[Clearing condition]

当1写入NMICLR.BUSMCLR位时。

TZFST标志（TrustZone过滤器错误状态标志）

该标志指示TrustZoneFilter错误中断请求。

[Setting condition]

当响应TrustZone过滤器错误而生成中断时

[Clearing condition]

当1写入NMICLR.TZFCLR位时

CPEST标志（高速缓存RAM奇偶校验错误状态标志）

该标志指示缓存RAM奇偶校验错误中断请求。

[Setting condition]

当响应高速缓存RAM奇偶校验错误而产生中断时

[Clearing condition]

当1写入NMICLR.CPECLR位时

13.2.12 NMIER:不可屏蔽中断使能寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x120

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPEEN	—	TZFEN	—	BUSMEN	—	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled.	R/W*1 *2
1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
2	LVD1EN	Voltage monitor 1 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
3	LVD2EN	Voltage monitor 2 Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTEN	Oscillation Stop Detection Interrupt Enable 0: Disabled 1: Enabled	R/W*1 *2
7	NMIEN	NMI Pin Interrupt Enable 0: Disabled 1: Enabled	R/W*1
8	RPEEN	SRAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
9	RECCEN	SRAM ECC Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMEN	MPU Bus Master Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZFEN	TrustZone Filter Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPEEN	Cache RAM Parity Error Interrupt Enable 0: Disabled 1: Enabled	R/W*1

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. You can write 1 to this bit only once after reset. Subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupt as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupt as an NMI trigger.

LVD1EN bit (Voltage monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupt as an NMI trigger.

Bit	Symbol	Function	R/W
0	IWDTEN	IWDT下溢刷新错误中断 使能 0：禁用1： 启用。	R/W*1 *2
1	WDTEN	WDT下溢刷新错误中断 使能 0：禁用1： 启用	R/W*1 *2
2	LVD1EN	电压监视器1中断使能 0：禁用1： 启用	R/W*1 *2
3	LVD2EN	电压监视器2中断使能 0：禁用1： 启用	R/W*1 *2
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	OSTEN	振荡停止检测中断使能 0：禁用1： 启用	R/W*1 *2
7	NMIEN	NMI引脚中断使能 0：禁用1： 启用	R/W*1
8	RPEEN	SRAM奇偶校验错误中断使能 0：禁用1： 启用	R/W*1
9	RECCEN	SRAMECC错误中断使能 0：禁用1： 启用	R/W*1
10	—	该位读取为0。写入值应为0。	R/W
11	BUSMEN	MPU总线主机错误中断使能 0：禁用1： 启用	R/W*1
12	—	该位读取为0。写入值应为0。	R/W
13	TZFEN	TrustZone过滤器错误中断启用 0：禁用1： 启用	R/W*1
14	—	该位读取为0。写入值应为0。	R/W
15	CPEEN	高速缓存RAM奇偶校验错误中断使能 0：禁用1： 启用	R/W*1

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.复位后您只能向该位写入1一次。随后的写访问无效。向该位写入0无效。
注2.当源用作事件信号时，请勿向该位写入1。

IWDTEN位（IWDT下溢刷新错误中断 允许）

IWDTEN位使能IWDT下溢刷新错误中断 作为NMI触发。

WDTEN位（WDT下溢刷新错误中断 允许）

WDTEN位使能WDT下溢刷新错误中断 作为NMI触发。

LVD1EN位（电压监视器1中断允许）

LVD1EN位使能电压监视器1中断作为NMI触发。

LVD2EN bit (Voltage monitor 2 Interrupt Enable)

The LVD2EN bit enables voltage monitor 2 interrupt as an NMI trigger.

OSTEN bit (Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main oscillation stop detection interrupt as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupt as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM parity error interrupt as an NMI trigger.

RECCEN bit (SRAM ECC Error Interrupt Enable)

The RECCEN bit enables SRAM ECC error interrupt as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupt as an NMI trigger.

TZFEN bit (TrustZone Filter Error Interrupt Enable)

TZFEN bit enables the TrustZone Filter error interrupt as an NMI trigger.

CPEEN bit (Cache RAM Parity Error Interrupt Enable)

CPEEN bit enables the Cache RAM Parity error interrupt as an NMI trigger.

13.2.13 NMICLR : Non-Maskable Interrupt Status Clear Register

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPECLR	—	TZFCLR	—	BUSMCLR	—	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT Clear 0: No effect 1: Clear the NMISR.IWDTST flag	R/W*1
1	WDTCLR	WDT Clear 0: No effect 1: Clear the NMISR.WDTST flag	R/W*1
2	LVD1CLR	LVD1 Clear 0: No effect 1: Clear the NMISR.LVD1ST flag	R/W*1
3	LVD2CLR	LVD2 Clear 0: No effect 1: Clear the NMISR.LVD2ST flag.	R/W*1
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	OSTCLR	OST Clear 0: No effect 1: Clear the NMISR.OSTST flag	R/W*1
7	NMICLR	NMI Clear 0: No effect 1: Clear the NMISR.NMIST flag	R/W*1

LVD2EN位（电压监视器2中断允许）

LVD2EN位使能电压监视器2中断作为NMI触发。

OSTEN位（振荡停止检测中断使能）

OSTEN位使能主振荡停止检测中断作为NMI触发。

NMIEN位（NMI引脚中断允许）

NMIEN位使能NMI引脚中断作为NMI触发器。

RPEEN位（SRAM奇偶校验错误中断使能）

RPEEN位启用SRAM奇偶校验错误中断作为NMI触发器。

RECCEN位（SRAMECC错误中断允许）

RECCEN位启用SRAMECC错误中断作为NMI触发器。

BUSMEN位（MPU总线主机错误中断允许）

BUSMEN位使能总线主机错误中断作为NMI触发器。

TZFEN位（TrustZone过滤器错误中断使能）

TZFEN位启用TrustZone过滤器错误中断作为NMI触发器。

CPEEN位（高速缓存RAM奇偶校验错误中断使能）

CPEEN位启用缓存RAM奇偶校验错误中断作为NMI触发器。

13.2.13 NMICLR:不可屏蔽中断状态清除寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x130

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CPECLR	—	TZFCLR	—	BUSMCLR	—	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IWDTCLR	IWDT Clear 0：无效1：清除NMISR.IWDTST标志	R/W*1
1	WDTCLR	WDT Clear 0：无效1：清除NMISR.WDTST标志	R/W*1
2	LVD1CLR	LVD1 Clear 0：无效1：清除NMISR.LVD1ST标志	R/W*1
3	LVD2CLR	LVD2 Clear 0：无效1：清除NMISR.LVD2ST标志。	R/W*1
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	OSTCLR	原声清除 0：无效1：清除NMISR.OSTST标志	R/W*1
7	NMICLR	NMI Clear 0：无效1：清除NMISR.NMIST标志	R/W*1

Bit	Symbol	Function	R/W
8	RPECLR	SRAM Parity Error Clear 0: No effect 1: Clear the NMISR.RPEST flag	R/W*1
9	RECCCLR	SRAM ECC Error Clear 0: No effect 1: Clear the NMISR.RECCST flag	R/W*1
10	—	This bit is read as 0. The write value should be 0.	R/W
11	BUSMCLR	Bus Master Error Clear 0: No effect 1: Clear the NMISR.BUSMST flag	R/W*1
12	—	This bit is read as 0. The write value should be 0.	R/W
13	TZFCLR	TrustZone Filter Error Clear 0: No effect 1: Clear the NMISR.TZFCLR flag	R/W*1
14	—	This bit is read as 0. The write value should be 0.	R/W
15	CPECLR	Cache RAM Parity Error Clear 0: No effect 1: Clear the NMISR.CPECLR flag	R/W*1

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Only write 1 to this bit.

IWDTCLR bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

WDTCLR bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (LVD2 Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

RPECLR bit (SRAM Parity Error Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. This bit is read as 0.

RECCCLR bit (SRAM ECC Error Clear)

Writing 1 to the RECCCLR bit clears the NMISR.RECCST flag. This bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMST flag. This bit is read as 0.

TZFCLR bit (TrustZone Filter Error Clear)

Writing 1 to the TZFCLR bit clears the NMISR.TZFST flag. This bit is read as 0.

Bit	Symbol	Function	R/W
8	RPECLR	SRAM奇偶校验错误清除 0：无效1：清除NMISR.RPEST标志	R/W*1
9	RECCCLR	SRAMECC错误清除 0：无效1：清除NMISR.RECCST标志	R/W*1
10	—	该位读取为0。写入值应为0。	R/W
11	BUSMCLR	总线主机错误清除 0：无效1：清除NMISR.BUSMST标志	R/W*1
12	—	该位读取为0。写入值应为0。	R/W
13	TZFCLR	TrustZone过滤器错误清除 0：无效1：清除NMISR.TZFCLR标志	R/W*1
14	—	该位读取为0。写入值应为0。	R/W
15	CPECLR	高速缓存RAM奇偶校验错误清除 0：无效1：清除NMISR.CPECLR标志	R/W*1

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.仅向该位写入1。

IWDTCLR bit (IWDT Clear)

将1写入IWDTCLR位会清除NMISR.IWDTST标志。该位读为0。

WDTCLR bit (WDT Clear)

将1写入WDTCLR位会清除NMISR.WDTST标志。该位读为0。

LVD1CLR bit (LVD1 Clear)

将1写入LVD1CLR位会清除NMISR.LVD1ST标志。该位读为0。

LVD2CLR bit (LVD2 Clear)

将1写入LVD2CLR位会清除NMISR.LVD2ST标志。该位读为0。

OSTCLR bit (OST Clear)

将1写入OSTCLR位会清除NMISR.OSTST标志。该位读为0。

NMICLR bit (NMI Clear)

将1写入NMICLR位会清除NMISR.NMIST标志。该位读为0。

RPECLR位（SRAM奇偶校验错误清除）

将1写入RPECLR位会清除NMISR.RPEST标志。该位读为0。

RECCCLR位（SRAMECC错误清除）

将1写入RECCCLR位会清除NMISR.RECCST标志。该位读为0。

BUSMCLR位（总线主机错误清除）

将1写入BUSMCLR位会清除NMISR.BUSMST标志。该位读为0。

TZFCLR位（TrustZone过滤器错误清除）

将1写入TZFCLR位会清除NMISR.TZFST标志。该位读为0。

CPECLR bit (Cache RAM Parity Error Clear)

Writing 1 to the CPECLR bit clears the NMISR.CPEST flag. This bit is read as 0.

13.2.14 NMICR : NMI Pin Interrupt Control Register

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI Detection Set 0: Falling edge 1: Rising edge	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
5:4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	NFLTEN	NMI Digital Filter Enable 0: Disabled 1: Enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Change the NMICR register settings before enabling NMI pin interrupts, that is, before setting NMIER.NMIEN to 1.

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for the NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for the NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every eight cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

For details of the digital filter, see section 13.5.5. Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1, and disabled when NFLTEN is 0. The NMI pin level is sampled at the clock cycle specified in NFCLKSEL[1:0]. When the sampled level matches three times, the output level from the digital filter changes. For details of the digital filter, see section 13.5.5. Digital Filter.

CPECLR位（高速缓存RAM奇偶校验错误清除）

将1写入CPECLR位会清除NMISR.CPEST标志。该位读为0。

13.2.14 NMICR:NMI引脚中断控制寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x100

Bit position:	7	6	5	4	3	2	1	0
Bit field:	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	NMIMD	NMI检测集 0：下降沿1： 上升沿	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
5:4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟选择 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	NFLTEN	NMI数字滤波器启用 0：禁用1： 启用	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在启用NMI引脚中断之前更改NMICR寄存器设置，即将NMIER.NMIEN设置为1。

NMIMD位（NMI检测集）

NMIMD位选择NMI引脚中断的检测检测方法。

NFCLKSEL[1:0]位（NMI数字滤波器采样时钟选择）

NFCLKSEL[1:0]位选择用于NMI引脚中断的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)

●PCLKB8（每八个周期一次）

- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles)

关于数字滤波器的详细信息，请参阅13.5.5节。数字滤波器。

NFLTEN位（NMI数字滤波器使能）

NFLTEN位使能用于NMI引脚中断的数字滤波器。滤波器在NFLTEN为1时启用，在NFLTEN为0时禁用。NMI引脚电平在NFCLKSEL[1:0]中指定的时钟周期进行采样。当采样电平匹配3次时，数字滤波器的输出电平会发生变化。关于数字滤波器的详细信息，请参阅13.5.5节。数字滤波器。

13.2.15 IELSRn : ICU Event Link Setting Register n (n = 0 to 95)

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	IELS[8:0]	ICU Event Link Select 0x00: Disable interrupts to the associated NVIC or DTC module Others: Event signal number to be linked. For details, see section 13.3.2. Event Number.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	Interrupt Status Flag 0: No interrupt request generated. 1: An interrupt request is generated.	R/W*1
23:17	—	These bits are read as 0. The write value should be 0.	R/W
24	DTCE	DTC Activation Enable 0: DTC activation is disabled. 1: DTC activation is enabled.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: This register requires halfword or word access.

Note 1. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQi source used by the NVIC. For details, see xref to Table 13.3. IELSRn corresponds to the NVIC IRQ input source number, where n = 0 to 95.

IELS[8:0] bits (ICU Event Link Select)

The IELS[8:0] bits link an event signal to the associated NVIC or DTC module. Event options are classified into 8 groups (groups 0 to 7). For details, see Table 13.3 and Table 13.4.

IR flag (Interrupt Status Flag)

The IR status flag indicates an individual interrupt request from the event specified in IELS[8:0].

[Setting condition]

When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing condition]

- The IR flag is cleared to 0 by writing 0.
- At the time other than the final transfer transfer end in DTC transfer during DTCE = 1, IR flag repeat set and cleared by Hardware.

When DTC transfer except last transfer is completed (DTCE bit is changed from 1 to 0).

During DTCE = 1, write 0 to IR register is prohibited.

In the case of level detection, clear of the IR flag should follow the steps below.

13.2.15 IELSRn:ICU事件链接设置寄存器n(n=0到95)

Base address: ICU = 0x4000_6000

Offset address: 0x300 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	IELS[8:0]	ICU事件链接选择 0x00：禁用相关NVIC或DTC模块的中断 其他：要链接的事件信号编号。详见13.3.2节。事件编号。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	IR	中断状态标志 0：不产生中断请求。1：产生中断请求。	R/W*1
23:17	—	这些位被读取为0。写入值应为0。	R/W
24	DTCE	DTC激活启用 0：禁用DTC激活。1：启用DTC激活。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 该寄存器需要半字或字访问。

注1.禁止向IR标志写入1。

IELSRn寄存器选择NVIC使用的IRQi源。有关详细信息，请参阅表13.3的外部参照。IELSRn对应于NVICIRQ输入源编号，其中n=0到95。

IELS[8:0]位（ICU事件链接选择）

IELS[8:0]位将事件信号链接到相关的NVIC或DTC模块。事件选项分为8组（组0到7）。详见表13.3和表13.4。

IR标志（中断状态标志）

IR状态标志指示来自IELS[8:0]中指定事件的单个中断请求。

[Setting condition]

当从相关外设模块或IRQi引脚接收到中断请求时。

[Clearing condition]

●IR标志通过写入0清除为0。

●在DTCE=1期间DTC传输中最后传输传输结束以外的时间，IR标志由硬件重复设置和清除。

完成最后一次传输以外的DTC传输时（DTCE位从1变为0）。

在DTCE=1期间，禁止向IR寄存器写入0。

在电平检测的情况下，清除IR标志应遵循以下步骤。

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.
3. Clear the IR flag by writing 0.

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

- When 1 is written to the DTCE bit.

[Clearing condition]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete.
- When 0 is written to the DTCE bit.

Note: Error during DTC transfer

If an error response occurs during DTC transfer, the DTC notifies the ICU that an error has occurred. ICU clears all bits of the target IELSRn (n = 0 to 95). IELSRn that is not the target is not cleared.

Note: DTC transfer error in snooze mode

When an error occurs in DTC transfer in Snooze mode, ICU issues a wakeup request. However, interrupt requests are not issued automatically. See section 17, Data Transfer Controller (DTC) for how to set the interrupt when a DTC error occurs.

13.2.16 DELSRn : DMAC Event Link Setting Register n (n = 0 to 7)

Base address: ICU = 0x4000 6000

Offset address: 0x280 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DELS[8:0]	DMAC Event Link Select 0x00: Disable interrupts to the associated DMAC module Others: Event signal number to be linked. For details, see Table 13.4.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	IR	DMAC Activation Request Status flag 0: No DMAC activation request occurred 1: DMAC activation request occurred.	R/W*1
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Writing 1 to the IR flag is prohibited.

1.取反输入中断信号。

2.对外设进行一次读取访问，并等待目标模块时钟的2个时钟周期。

3.写0清除IR标志。

DTCE位（DTC激活使能）

当DTCE位设置为1时，相关事件被选为DTC激活源。

[Setting condition]

●当1写入DTCE位时。

[Clearing condition]

●当指定数量的传输完成时。对于链式转移，当最后一次链式转移的指定转移次数完成时。

●当0写入DTCE位时。

Note: DTC传输期间出错

如果在DTC传输期间发生错误响应，则DTC会通知ICU发生了错误。ICU清除目标IELSRn(n=0到95)的所有位。不是目标的IELSRn不会被清除。

Note: 贪睡模式下的DTC传输错误

当贪睡模式下的DTC传输发生错误时，ICU会发出唤醒请求。但是，不会自动发出中断请求。有关如何在发生DTC错误时设置中断，请参见第17节，数据传输控制器(DTC)。

13.2.16 DELSRn：DMAC事件链接设置寄存器n（n=0到7）

Base address: ICU = 0x4000 6000

Offset address: 0x280 + 0x4 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DELS[8:0]	DMAC事件链接选择 0x00：禁用相关DMAC模块的中断 其他：要链接的事件信号编号。详见表13.4。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	IR	DMAC激活请求状态标志 0：未发生DMAC激活请求1：发生DMAC激活请求。	R/W*1
31:17	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.禁止向IR标志写入1。

DELS[8:0] bit (DMAC Event Link Select)

The DELS[8:0] bits link an event signal to the associated DMAC module. Do not set the same event number in multiple DELSRn registers.

IR flag (DMAC Activation Request Status flag)

The IR flag is the status flag of a DMAC activation request. This flag is associated with the DELS[8:0] bits of this register.

[Setting condition]

- The flag is set to 1 when a DMAC activation request is generated from the associated peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag
- At the start of a DMA transfer after the DMAC activation request is issued.

Note: The IR flag is automatically cleared after completion of DMA transfer, so do not write 0 unless an abort occurs. DMA transfer operation when 0 is written cannot be guaranteed.

Note: Error during DMAC transfer

If an error response occurs during DMAC transfer, the DMAC notifies the ICU that an error has occurred.

The ICU clears all bits of the target channel of DELSRn (n = 0 to 7). DELSRn that is not the target channel is not cleared.

13.2.17 SELSR0 : SYS Event Link Setting Register

Base address: ICU = 0x4000_6000

Offset address: 0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SELS[8:0]	SYS Event Link Select 0x00: Disable event output to the associated low-power mode module Others: Event signal number to be linked. For details, see Table 13.4.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The SELSR0 register selects the events that wake up the CPU from Snooze mode. You can use only the events listed in Table 13.4 checked as “Canceling Snooze mode using SELSR0”. Events specified in this register are defined as ICU_SNZCANCEL in Table 13.4. When ICU_SNZCANCEL is selected in the IELSRn.IELS[8:0] bits, the SELSR0 event interrupt occurs.

Caution: For security attribution added to parts related to a series of actions, make sure to match all security attribution so that security holes cannot be created.

About security attribution to be matched

- **Event source to be set to SELSR0.**
- **SELSR0**
- **IELSRn (n = 0 to 95) to receive event No. 45 (ICU_SNZCANCEL).**
- **NVIC internal registers from the CPU of the three specified interrupts.**
- **Interrupt Handler.**

DELS[8:0]位（DMAC事件链接选择）

DELS[8:0]位将事件信号链接到相关的DMAC模块。不要在多个中设置相同的事件编号
DELSRn registers.

IR标志（DMAC激活请求状态标志）

IR标志是DMAC激活请求的状态标志。该标志与该寄存器的DELS[8:0]位相关联。

[Setting condition]

●当相关外设模块或IRQi引脚产生DMAC激活请求时，该标志设置为1。

[Clearing conditions]

●标志写入0时

●在发出DMAC激活请求后开始DMA传输。

Note: IR标志在DMA传输完成后自动清除，因此除非发生中止，否则不要写0。无法保证写入0时的DMA传输操作。

Note: DMAC传输期间出错

如果在DMAC传输期间发生错误响应，则DMAC会通知ICU发生了错误。

ICU清除DELSRn（n=0到7）的目标通道的所有位。不是目标通道的DELSRn不会被清除。

13.2.17 SELSR0：SYS事件链接设置寄存器

Base address: ICU = 0x4000_6000

Offset address: 0x200

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	SELS[8:0]	SYS事件链接选择 0x00：禁用到相关低功耗模式模块的事件输出 其他：要链接的事件信号编号。详见表13.4。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SELSR0寄存器选择将CPU从贪睡模式唤醒的事件。您只能使用中列出的事件
表13.4选中“使用SELSR0取消贪睡模式”。该寄存器中指定的事件定义为
ICU_SNZCANCEL在表13.4中。在IELSRn.IELS[8:0]位中选择ICU_SNZCANCEL时，将发生SELSR0事件中断。

Caution: 对于添加到与一系列动作相关的部分的安全属性，请确保匹配所有的安全属性，以免造成安全漏洞。

关于要匹配的安全属性●

事件源设置为SELSR0。

- **SELSR0**
- **IELSRn(n=0到95)接收事件编号45(ICU_SNZCANCEL)。**
- **NVIC内部寄存器来自CPU的三个指定中断。**
- **中断处理程序。**

13.2.18 WUPEN0 : Wake Up Interrupt Enable Register 0

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFS0WUPEN	USBHSWUPEN	RTCPRDWUPEN	RTCALMWUPEN	—	—	—	—	LVD2WUPEN	LVD1WUPEN	—	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IRQWUPEN[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	IRQWUPEN[15:0]	IRQn Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IRQn interrupt is disabled 1: Software Standby/Snooze Mode returns by IRQn interrupt is enabled*1	R/W
16	IWDTWUPEN	IWDT Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IWDT interrupt is disabled 1: Software Standby/Snooze Mode returns by IWDT interrupt is enabled	R/W
17	—	This bit is read as 0. The write value should be 0.	R/W
18	LVD1WUPEN	LVD1 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by LVD1 interrupt is disabled 1: Software Standby/Snooze Mode returns by LVD1 interrupt is enabled	R/W
19	LVD2WUPEN	LVD2 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by LVD2 interrupt is disabled 1: Software Standby/Snooze Mode returns by LVD2 interrupt is enabled	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
24	RTCALMWUPEN	RTC Alarm Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by RTC alarm interrupt is disabled 1: Software Standby/Snooze Mode returns by RTC alarm interrupt is enabled	R/W
25	RTCPRDWUPEN	RTC Period Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by RTC period interrupt is disabled 1: Software Standby/Snooze Mode returns by RTC period interrupt is enabled	R/W
26	USBHSWUPEN	USBHS Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by USBHS interrupt is disabled 1: Software Standby/Snooze Mode returns by USBHS interrupt is enabled	R/W
27	USBFS0WUPEN	USBFS0 Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by USBFS0 interrupt is disabled 1: Software Standby/Snooze Mode returns by USBFS0 interrupt is enabled	R/W
28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 underflow interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 underflow interrupt is enabled	R/W
29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 compare match A interrupt is enabled	R/W
30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt is disabled 1: Software Standby/Snooze Mode returns by AGT1 compare match B interrupt is enabled	R/W

13.2.18 WUPEN0:唤醒中断使能寄存器0

Base address: ICU = 0x4000_6000

Offset address: 0x1A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFS0WUPEN	USBHSWUPEN	RTCPRDWUPEN	RTCALMWUPEN	—	—	—	—	LVD2WUPEN	LVD1WUPEN	—	IWDTWUPEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	IRQWUPEN[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	IRQWUPEN[15:0]	IRQn中断软件待机贪睡模式返回使能位 0：禁用IRQn中断返回软件待机贪睡模式1：启用IRQn中断返回软件待机贪睡模式*1	R/W
16	IWDTWUPEN	IWDT中断软件待机贪睡模式返回使能位 0：禁止通过IWDT中断返回软件待机贪睡模式1：使能通过IWDT中断返回软件待机贪睡模式	R/W
17	—	该位读取为0。写入值应为0。	R/W
18	LVD1WUPEN	LVD1中断软件待机贪睡模式返回使能位 0：禁用LVD1中断返回软件待机贪睡模式1：启用LVD1中断返回软件待机贪睡模式	R/W
19	LVD2WUPEN	LVD2中断软件待机贪睡模式返回使能位 0：禁用LVD2中断返回软件待机贪睡模式1：启用LVD2中断返回软件待机贪睡模式	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
24	RTCALMWUPEN	RTC闹钟中断软件待机贪睡模式返回使能位 0：禁用RTC闹钟中断返回软件待机贪睡模式1：启用RTC闹钟中断返回软件待机贪睡模式	R/W
25	RTCPRDWUPEN	RTC周期中断软件待机贪睡模式返回使能位 0：禁用RTC周期中断返回软件待机贪睡模式1：启用RTC周期中断返回软件待机贪睡模式	R/W
26	USBHSWUPEN	USBHS中断软件待机贪睡模式返回使能位 0：禁止通过USBHS中断返回软件待机贪睡模式1：使能通过USBHS中断返回软件待机贪睡模式	R/W
27	USBFS0WUPEN	USBFS0中断软件待机贪睡模式返回使能位 0：禁用USBFS0中断返回软件待机贪睡模式1：启用USBFS0中断返回软件待机贪睡模式	R/W
28	AGT1UDWUPEN	AGT1下溢中断软件待机贪睡模式返回使能位 0：禁用AGT1下溢中断返回软件待机贪睡模式1：启用AGT1下溢中断返回软件待机贪睡模式	R/W
29	AGT1CAWUPEN	AGT1比较匹配中断软件待机贪睡模式返回使能位 0：软件待机贪睡模式由AGT1比较匹配返回A中断被禁用 1：软件待机贪睡模式由AGT1比较匹配返回启用中断	R/W
30	AGT1CBWUPEN	AGT1比较匹配B中断软件待机贪睡模式返回使能位 0：软件待机贪睡模式由AGT1比较匹配B中断被禁用返回 1：软件待机贪睡模式由AGT1比较匹配B中断启用	R/W

Bit	Symbol	Function	R/W
31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby/Snooze Mode Returns Enable bit 0: Software Standby/Snooze Mode returns by IIC0 address match interrupt is disabled 1: Software Standby/Snooze Mode returns by IIC0 address match interrupt is enabled	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. Description is a description of each bit.

IRQWUPEN[15:0] bits (IRQn Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the IRQn pin as a Software standby return factor.

n = 0 to 15

IWDTWUPEN bit (IWDT Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the IWDT interrupt as an Software standby return factor.

LVD1WUPEN bit (LVD1 Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the LVD1 interrupt as an Software standby return factor.

LVD2WUPEN bit (LVD2 Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the LVD2 interrupt as an Software standby return factor.

RTCALMWUPEN bit (RTC Alarm Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the RTC alarm interrupt as an Software standby return factor.

RTCPRDWUPEN bit (RTC Period Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the RTC period interrupt as an Software standby return factor.

USBHSWUPEN bit (USBHS Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the USBHS interrupt as an Software standby return factor.

USBFS0WUPEN bit (USBFS0 Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the USBFS0 interrupt as an Software standby return factor.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the AGT1 underflow interrupt as an Software standby return factor.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the AGT1 compare match A interrupt as an Software standby return factor.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the AGT1 compare match B interrupt as an Software standby return factor.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby/Snooze Mode Returns Enable bit)

This bit is the enable bit to control the use of the IIC0 interrupt as an Software standby return factor.

Note: The security attribution of this register is set for each wakeup event.
To avoid the occurrence of a security hole, the target event of a wakeup and the security attribution added to this bit must match.

Bit	Symbol	Function	R/W
31	IIC0WUPEN	IIC0地址匹配中断软件待机贪睡模式返回使能位 0：软件待机贪睡模式由IIC0地址匹配中断返回被禁用 1：软件待机贪睡模式由IIC0地址匹配中断返回使能	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.描述是对每个位的描述。

IRQWUPEN[15:0]位（IRQn中断软件待机贪睡模式返回使能位）

该位是控制使用IRQn引脚作为软件待机返回因子的使能位。

n = 0 to 15

IWDTWUPEN位（IWDT中断软件待机贪睡模式返回使能位）

该位是控制使用IWDT中断作为软件待机返回因素的使能位。

LVD1WUPEN位（LVD1中断软件待机贪睡模式返回使能位）

该位是控制使用LVD1中断作为软件待机返回因素的使能位。

LVD2WUPEN位（LVD2中断软件待机贪睡模式返回使能位）

该位是控制使用LVD2中断作为软件待机返回因素的使能位。

RTCALMWUPEN位（RTC闹钟中断软件待机贪睡模式返回使能位）

该位是控制使用RTC闹钟中断作为软件待机返回因素的使能位。

RTCPRDWUPEN位（RTC周期中断软件待机贪睡模式返回使能位）

该位是控制使用RTC周期中断作为软件待机返回因素的使能位。

USBHSWUPEN位（USBHS中断软件待机贪睡模式返回使能位）

该位是控制使用USBHS中断作为软件待机返回因子的使能位。

USBFS0WUPEN位（USBFS0中断软件待机贪睡模式返回使能位）

该位是控制使用USBFS0中断作为软件待机返回因子的使能位。

AGT1UDWUPEN位（AGT1下溢中断软件待机贪睡模式返回使能位）

该位是控制使用AGT1下溢中断作为软件待机返回因素的使能位。

AGT1CAWUPEN位（AGT1比较匹配A中断软件待机贪睡模式返回使能位）

该位是控制使用AGT1比较匹配A中断作为软件待机返回因素的使能位。

AGT1CBWUPEN位（AGT1比较匹配B中断软件待机贪睡模式返回使能位）

该位是控制使用AGT1比较匹配B中断作为软件待机返回因素的使能位。

IIC0WUPEN位（IIC0地址匹配中断软件待机贪睡模式返回使能位）

该位是控制使用IIC0中断作为软件待机返回因素的使能位。

Note: 该寄存器的安全属性为每个唤醒事件设置。
为了避免安全漏洞的发生，唤醒的目标事件和添加到该位的安全属性必须匹配。

13.2.19 WUPEN1 : Wake Up interrupt enable register 1

Base address: ICU = 0x4000_6000

Offset address: 0x1A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	AGT3 CBWU PEN	AGT3 CAWU PEN	AGT3 UDWU PEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGT3UDWUPEN	AGT3 Underflow Interrupt Software Standby Return Enable bit 0: Software standby returns by AGT3 underflow interrupt is disabled 1: Software standby returns by AGT3 underflow interrupt is enabled	R/W
1	AGT3CAWUPEN	AGT3 Compare Match A Interrupt Software Standby Return Enable bit 0: Software standby returns by AGT3 compare match A interrupt is disabled 1: Software standby returns by AGT3 compare match A interrupt is enabled	R/W
2	AGT3CBWUPEN	AGT3 Compare Match B Interrupt Software Standby Return Enable bit 0: Software standby returns by AGT3 compare match B interrupt is disabled 1: Software standby returns by AGT3 compare match B interrupt is enabled	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R*1

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. This bit is read only

AGT3UDWUPEN bit (AGT3 Underflow Interrupt Software Standby Return Enable bit)

This bit is the enable bit to control the use of the AGT3 underflow interrupt as an Software standby return factor.

AGT3CAWUPEN bit (AGT3 Compare Match A Interrupt Software Standby Return Enable bit)

This bit is the enable bit to control the use of the AGT3 compare match A interrupt as an Software standby return factor.

AGT3CBWUPEN bit (AGT3 Compare Match B Interrupt Software Standby Return Enable bit)

This bit is the enable bit to control the use of the AGT3 compare match B interrupt as an Software standby return factor.

Note: The security attribution of this register is set for each wakeup event.
To avoid the occurrence of a security hole, the target event of a wakeup and the security attribution added to this bit must match.

13.3 Vector Table

The ICU detects maskable and non-maskable interrupts. Interrupt priorities are set up in the Arm NVIC. For information about these registers, see section 13.9. Reference.

13.3.1 Interrupt Vector Table

Table 13.3 describes the interrupt vector table. The interrupt vector addresses conform to the NVIC specifications.

13.2.19 WUPEN1：唤醒中断使能寄存器1

Base address: ICU = 0x4000_6000

Offset address: 0x1A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	AGT3 CBWU PEN	AGT3 CAWU PEN	AGT3 UDWU PEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AGT3UDWUPEN	AGT3下溢中断软件待机返回使能位 0：禁用AGT3下溢中断返回软件待机1：启用AGT3下溢中断返回软件待机	R/W
1	AGT3CAWUPEN	AGT3比较匹配A中断软件待机返回使能位 0：通过AGT3比较匹配A中断禁用软件待机返回1：通过AGT3比较匹配A中断启用软件待机返回	R/W
2	AGT3CBWUPEN	AGT3比较匹配B中断软件待机返回使能位 0：禁用AGT3比较匹配B中断返回软件待机1：启用AGT3比较匹配B中断返回软件待机	R/W
31:3	—	这些位被读取为0。写入值应为0。	R*1

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.该位是只读的

AGT3UDWUPEN位（AGT3下溢中断软件待机返回使能位）

该位是控制使用AGT3下溢中断作为软件待机返回因子的使能位。

AGT3CAWUPEN位（AGT3比较匹配A中断软件待机返回使能位）

该位是控制使用AGT3比较匹配A中断作为软件待机返回因子的使能位。

AGT3CBWUPEN位（AGT3比较匹配B中断软件待机返回使能位）

该位是控制使用AGT3比较匹配B中断作为软件待机返回因素的使能位。

Note: 该寄存器的安全属性为每个唤醒事件设置。
为了避免安全漏洞的发生，唤醒的目标事件和添加到该位的安全属性必须匹配。

13.3 向量表

ICU检测可屏蔽和不可屏蔽中断。中断优先级在ArmNVIC中设置。有关这些寄存器的信息，请参阅第13.9节。参考。

13.3.1 中断向量表

表13.3描述了中断向量表。中断向量地址符合NVIC规范。

Table 13.3 Interrupt vector table (1 of 3)

Exception number	IRQ number	Vector offset	Source	Description
0	—	0x000	Arm	Initial stack pointer
1	—	0x004	Arm	Initial program counter (reset vector)
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	Hard Fault
4	—	0x010	Arm	MemManage fault
5	—	0x014	Arm	BusFault
6	—	0x018	Arm	UsageFault
7	—	0x01C	Arm	SecureFault
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	Supervisor Call (SVCall)
12	—	0x030	Arm	DebugMonitor
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	Pendable request for system service (PendableSrvReq)
15	—	0x03C	Arm	System Tick Timer (SysTick)
16	0	0x040	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	0x044	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	0x048	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	0x04C	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	0x050	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	0x054	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	0x058	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	0x05C	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	0x060	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	0x064	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	0x068	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	0x06C	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	0x070	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	0x074	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	0x078	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	0x07C	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	0x080	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	0x084	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	0x088	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	0x08C	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	0x090	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	0x094	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	0x098	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	0x09C	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0x0A0	ICU.IELSR24	Event selected in the ICU.IELSR24 register

Table 13.3 中断向量表(1of3)

异常编号	IRQ number	矢量偏移	Source	Description
0	—	0x000	Arm	初始堆栈指针
1	—	0x004	Arm	初始程序计数器（复位向量）
2	—	0x008	Arm	Non-Maskable Interrupt (NMI)
3	—	0x00C	Arm	硬故障
4	—	0x010	Arm	MemManage fault
5	—	0x014	Arm	BusFault
6	—	0x018	Arm	UsageFault
7	—	0x01C	Arm	SecureFault
8	—	0x020	Arm	Reserved
9	—	0x024	Arm	Reserved
10	—	0x028	Arm	Reserved
11	—	0x02C	Arm	主管呼叫(SVCall)
12	—	0x030	Arm	DebugMonitor
13	—	0x034	Arm	Reserved
14	—	0x038	Arm	系统服务的挂起请求(PendableSrvReq)
15	—	0x03C	Arm	系统滴答计时器(SysTick)
16	0	0x040	ICU.IELSR0	在ICU.IELSR0寄存器中选择的事件
17	1	0x044	ICU.IELSR1	在ICU.IELSR1寄存器中选择的事件
18	2	0x048	ICU.IELSR2	在ICU.IELSR2寄存器中选择的事件
19	3	0x04C	ICU.IELSR3	在ICU.IELSR3寄存器中选择的事件
20	4	0x050	ICU.IELSR4	在ICU.IELSR4寄存器中选择的事件
21	5	0x054	ICU.IELSR5	在ICU.IELSR5寄存器中选择的事件
22	6	0x058	ICU.IELSR6	在ICU.IELSR6寄存器中选择的事件
23	7	0x05C	ICU.IELSR7	在ICU.IELSR7寄存器中选择的事件
24	8	0x060	ICU.IELSR8	在ICU.IELSR8寄存器中选择的事件
25	9	0x064	ICU.IELSR9	在ICU.IELSR9寄存器中选择的事件
26	10	0x068	ICU.IELSR10	在ICU.IELSR10寄存器中选择的事件
27	11	0x06C	ICU.IELSR11	在ICU.IELSR11寄存器中选择的事件
28	12	0x070	ICU.IELSR12	在ICU.IELSR12寄存器中选择的事件
29	13	0x074	ICU.IELSR13	在ICU.IELSR13寄存器中选择的事件
30	14	0x078	ICU.IELSR14	在ICU.IELSR14寄存器中选择的事件
31	15	0x07C	ICU.IELSR15	在ICU.IELSR15寄存器中选择的事件
32	16	0x080	ICU.IELSR16	在ICU.IELSR16寄存器中选择的事件
33	17	0x084	ICU.IELSR17	在ICU.IELSR17寄存器中选择的事件
34	18	0x088	ICU.IELSR18	在ICU.IELSR18寄存器中选择的事件
35	19	0x08C	ICU.IELSR19	在ICU.IELSR19寄存器中选择的事件
36	20	0x090	ICU.IELSR20	在ICU.IELSR20寄存器中选择的事件
37	21	0x094	ICU.IELSR21	在ICU.IELSR21寄存器中选择的事件
38	22	0x098	ICU.IELSR22	在ICU.IELSR22寄存器中选择的事件
39	23	0x09C	ICU.IELSR23	在ICU.IELSR23寄存器中选择的事件
40	24	0x0A0	ICU.IELSR24	在ICU.IELSR24寄存器中选择的事件

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Table 13.3 Interrupt vector table (2 of 3)

Exception number	IRQ number	Vector offset	Source	Description
41	25	0x0A4	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0x0A8	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0x0AC	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0x0B0	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0x0B4	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0x0B8	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0x0BC	ICU.IELSR31	Event selected in the ICU.IELSR31 register
48	32	0x0C0	ICU.IELSR32	Event selected in the ICU.IELSR32 register
49	33	0x0C4	ICU.IELSR33	Event selected in the ICU.IELSR33 register
50	34	0x0C8	ICU.IELSR34	Event selected in the ICU.IELSR34 register
51	35	0x0CC	ICU.IELSR35	Event selected in the ICU.IELSR35 register
52	36	0x0D0	ICU.IELSR36	Event selected in the ICU.IELSR36 register
53	37	0x0D4	ICU.IELSR37	Event selected in the ICU.IELSR37 register
54	38	0x0D8	ICU.IELSR38	Event selected in the ICU.IELSR38 register
55	39	0x0DC	ICU.IELSR39	Event selected in the ICU.IELSR39 register
56	40	0x0E0	ICU.IELSR40	Event selected in the ICU.IELSR40 register
57	41	0x0E4	ICU.IELSR41	Event selected in the ICU.IELSR41 register
58	42	0x0E8	ICU.IELSR42	Event selected in the ICU.IELSR42 register
59	43	0x0EC	ICU.IELSR43	Event selected in the ICU.IELSR43 register
60	44	0x0F0	ICU.IELSR44	Event selected in the ICU.IELSR44 register
61	45	0x0F4	ICU.IELSR45	Event selected in the ICU.IELSR45 register
62	46	0x0F8	ICU.IELSR46	Event selected in the ICU.IELSR46 register
63	47	0x0FC	ICU.IELSR47	Event selected in the ICU.IELSR47 register
64	48	0x100	ICU.IELSR48	Event selected in the ICU.IELSR48 register
65	49	0x104	ICU.IELSR49	Event selected in the ICU.IELSR49 register
66	50	0x108	ICU.IELSR50	Event selected in the ICU.IELSR50 register
67	51	0x10C	ICU.IELSR51	Event selected in the ICU.IELSR51 register
68	52	0x110	ICU.IELSR52	Event selected in the ICU.IELSR52 register
69	53	0x114	ICU.IELSR53	Event selected in the ICU.IELSR53 register
70	54	0x118	ICU.IELSR54	Event selected in the ICU.IELSR54 register
71	55	0x11C	ICU.IELSR55	Event selected in the ICU.IELSR55 register
72	56	0x120	ICU.IELSR56	Event selected in the ICU.IELSR56 register
73	57	0x124	ICU.IELSR57	Event selected in the ICU.IELSR57 register
74	58	0x128	ICU.IELSR58	Event selected in the ICU.IELSR58 register
75	59	0x12C	ICU.IELSR59	Event selected in the ICU.IELSR59 register
76	60	0x130	ICU.IELSR60	Event selected in the ICU.IELSR60 register
77	61	0x134	ICU.IELSR61	Event selected in the ICU.IELSR61 register
78	62	0x138	ICU.IELSR62	Event selected in the ICU.IELSR62 register
79	63	0x13C	ICU.IELSR63	Event selected in the ICU.IELSR63 register
80	64	0x140	ICU.IELSR64	Event selected in the ICU.IELSR64 register
81	65	0x144	ICU.IELSR65	Event selected in the ICU.IELSR65 register

Table 13.3 中断向量表(2of3)

异常编号	IRQ number	矢量偏移	Source	Description
41	25	0x0A4	ICU.IELSR25	在ICU.IELSR25寄存器中选择的事件
42	26	0x0A8	ICU.IELSR26	在ICU.IELSR26寄存器中选择的事件
43	27	0x0AC	ICU.IELSR27	在ICU.IELSR27寄存器中选择的事件
44	28	0x0B0	ICU.IELSR28	在ICU.IELSR28寄存器中选择的事件
45	29	0x0B4	ICU.IELSR29	在ICU.IELSR29寄存器中选择的事件
46	30	0x0B8	ICU.IELSR30	在ICU.IELSR30寄存器中选择的事件
47	31	0x0BC	ICU.IELSR31	在ICU.IELSR31寄存器中选择的事件
48	32	0x0C0	ICU.IELSR32	在ICU.IELSR32寄存器中选择的事件
49	33	0x0C4	ICU.IELSR33	在ICU.IELSR33寄存器中选择的事件
50	34	0x0C8	ICU.IELSR34	在ICU.IELSR34寄存器中选择的事件
51	35	0x0CC	ICU.IELSR35	在ICU.IELSR35寄存器中选择的事件
52	36	0x0D0	ICU.IELSR36	在ICU.IELSR36寄存器中选择的事件
53	37	0x0D4	ICU.IELSR37	在ICU.IELSR37寄存器中选择的事件
54	38	0x0D8	ICU.IELSR38	在ICU.IELSR38寄存器中选择的事件
55	39	0x0DC	ICU.IELSR39	在ICU.IELSR39寄存器中选择的事件
56	40	0x0E0	ICU.IELSR40	在ICU.IELSR40寄存器中选择的事件
57	41	0x0E4	ICU.IELSR41	在ICU.IELSR41寄存器中选择的事件
58	42	0x0E8	ICU.IELSR42	在ICU.IELSR42寄存器中选择的事件
59	43	0x0EC	ICU.IELSR43	在ICU.IELSR43寄存器中选择的事件
60	44	0x0F0	ICU.IELSR44	在ICU.IELSR44寄存器中选择的事件
61	45	0x0F4	ICU.IELSR45	在ICU.IELSR45寄存器中选择的事件
62	46	0x0F8	ICU.IELSR46	在ICU.IELSR46寄存器中选择的事件
63	47	0x0FC	ICU.IELSR47	在ICU.IELSR47寄存器中选择的事件
64	48	0x100	ICU.IELSR48	在ICU.IELSR48寄存器中选择的事件
65	49	0x104	ICU.IELSR49	在ICU.IELSR49寄存器中选择的事件
66	50	0x108	ICU.IELSR50	在ICU.IELSR50寄存器中选择的事件
67	51	0x10C	ICU.IELSR51	在ICU.IELSR51寄存器中选择的事件
68	52	0x110	ICU.IELSR52	在ICU.IELSR52寄存器中选择的事件
69	53	0x114	ICU.IELSR53	在ICU.IELSR53寄存器中选择的事件
70	54	0x118	ICU.IELSR54	在ICU.IELSR54寄存器中选择的事件
71	55	0x11C	ICU.IELSR55	在ICU.IELSR55寄存器中选择的事件
72	56	0x120	ICU.IELSR56	在ICU.IELSR56寄存器中选择的事件
73	57	0x124	ICU.IELSR57	在ICU.IELSR57寄存器中选择的事件
74	58	0x128	ICU.IELSR58	在ICU.IELSR58寄存器中选择的事件
75	59	0x12C	ICU.IELSR59	在ICU.IELSR59寄存器中选择的事件
76	60	0x130	ICU.IELSR60	在ICU.IELSR60寄存器中选择的事件
77	61	0x134	ICU.IELSR61	在ICU.IELSR61寄存器中选择的事件
78	62	0x138	ICU.IELSR62	在ICU.IELSR62寄存器中选择的事件
79	63	0x13C	ICU.IELSR63	在ICU.IELSR63寄存器中选择的事件
80	64	0x140	ICU.IELSR64	在ICU.IELSR64寄存器中选择的事件
81	65	0x144	ICU.IELSR65	在ICU.IELSR65寄存器中选择的事件

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Table 13.3 Interrupt vector table (3 of 3)

Exception number	IRQ number	Vector offset	Source	Description
82	66	0x148	ICU.IELSR66	Event selected in the ICU.IELSR66 register
83	67	0x14C	ICU.IELSR67	Event selected in the ICU.IELSR67 register
84	68	0x150	ICU.IELSR68	Event selected in the ICU.IELSR68 register
85	69	0x154	ICU.IELSR69	Event selected in the ICU.IELSR69 register
86	70	0x158	ICU.IELSR70	Event selected in the ICU.IELSR70 register
87	71	0x15C	ICU.IELSR71	Event selected in the ICU.IELSR71 register
88	72	0x160	ICU.IELSR72	Event selected in the ICU.IELSR72 register
89	73	0x164	ICU.IELSR73	Event selected in the ICU.IELSR73 register
90	74	0x168	ICU.IELSR74	Event selected in the ICU.IELSR74 register
91	75	0x16C	ICU.IELSR75	Event selected in the ICU.IELSR75 register
92	76	0x170	ICU.IELSR76	Event selected in the ICU.IELSR76 register
93	77	0x174	ICU.IELSR77	Event selected in the ICU.IELSR77 register
94	78	0x178	ICU.IELSR78	Event selected in the ICU.IELSR78 register
95	79	0x17C	ICU.IELSR79	Event selected in the ICU.IELSR79 register
96	80	0x180	ICU.IELSR80	Event selected in the ICU.IELSR80 register
97	81	0x184	ICU.IELSR81	Event selected in the ICU.IELSR81 register
98	82	0x188	ICU.IELSR82	Event selected in the ICU.IELSR82 register
99	83	0x18C	ICU.IELSR83	Event selected in the ICU.IELSR83 register
100	84	0x190	ICU.IELSR84	Event selected in the ICU.IELSR84 register
101	85	0x194	ICU.IELSR85	Event selected in the ICU.IELSR85 register
102	86	0x198	ICU.IELSR86	Event selected in the ICU.IELSR86 register
103	87	0x19C	ICU.IELSR87	Event selected in the ICU.IELSR87 register
104	88	0x1A0	ICU.IELSR88	Event selected in the ICU.IELSR88 register
105	89	0x1A4	ICU.IELSR89	Event selected in the ICU.IELSR89 register
106	90	0x1A8	ICU.IELSR90	Event selected in the ICU.IELSR90 register
107	91	0x1AC	ICU.IELSR91	Event selected in the ICU.IELSR91 register
108	92	0x1B0	ICU.IELSR92	Event selected in the ICU.IELSR92 register
109	93	0x1B4	ICU.IELSR93	Event selected in the ICU.IELSR93 register
110	94	0x1B8	ICU.IELSR94	Event selected in the ICU.IELSR94 register
111	95	0x1BC	ICU.IELSR95	Event selected in the ICU.IELSR95 register

13.3.2 Event Number

The following table lists heading details for Table 13.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	“ ✓” indicates the interrupt can be used as a CPU interrupt
Invoke DTC	“ ✓” indicates the interrupt can be used to request DTC activation
Invoke DMAC	“✓” indicates the interrupt can be used to request DMAC activation
Canceling Snooze	“ ✓” indicates the interrupt can be used to request a return from Snooze mode

Table 13.3 中断向量表(3of3)

异常编号	IRQ number	矢量偏移	Source	Description
82	66	0x148	ICU.IELSR66	在ICU.IELSR66寄存器中选择的事件
83	67	0x14C	ICU.IELSR67	在ICU.IELSR67寄存器中选择的事件
84	68	0x150	ICU.IELSR68	在ICU.IELSR68寄存器中选择的事件
85	69	0x154	ICU.IELSR69	在ICU.IELSR69寄存器中选择的事件
86	70	0x158	ICU.IELSR70	在ICU.IELSR70寄存器中选择的事件
87	71	0x15C	ICU.IELSR71	在ICU.IELSR71寄存器中选择的事件
88	72	0x160	ICU.IELSR72	在ICU.IELSR72寄存器中选择的事件
89	73	0x164	ICU.IELSR73	在ICU.IELSR73寄存器中选择的事件
90	74	0x168	ICU.IELSR74	在ICU.IELSR74寄存器中选择的事件
91	75	0x16C	ICU.IELSR75	在ICU.IELSR75寄存器中选择的事件
92	76	0x170	ICU.IELSR76	在ICU.IELSR76寄存器中选择的事件
93	77	0x174	ICU.IELSR77	在ICU.IELSR77寄存器中选择的事件
94	78	0x178	ICU.IELSR78	在ICU.IELSR78寄存器中选择的事件
95	79	0x17C	ICU.IELSR79	在ICU.IELSR79寄存器中选择的事件
96	80	0x180	ICU.IELSR80	在ICU.IELSR80寄存器中选择的事件
97	81	0x184	ICU.IELSR81	在ICU.IELSR81寄存器中选择的事件
98	82	0x188	ICU.IELSR82	在ICU.IELSR82寄存器中选择的事件
99	83	0x18C	ICU.IELSR83	在ICU.IELSR83寄存器中选择的事件
100	84	0x190	ICU.IELSR84	在ICU.IELSR84寄存器中选择的事件
101	85	0x194	ICU.IELSR85	在ICU.IELSR85寄存器中选择的事件
102	86	0x198	ICU.IELSR86	在ICU.IELSR86寄存器中选择的事件
103	87	0x19C	ICU.IELSR87	在ICU.IELSR87寄存器中选择的事件
104	88	0x1A0	ICU.IELSR88	在ICU.IELSR88寄存器中选择的事件
105	89	0x1A4	ICU.IELSR89	在ICU.IELSR89寄存器中选择的事件
106	90	0x1A8	ICU.IELSR90	在ICU.IELSR90寄存器中选择的事件
107	91	0x1AC	ICU.IELSR91	在ICU.IELSR91寄存器中选择的事件
108	92	0x1B0	ICU.IELSR92	在ICU.IELSR92寄存器中选择的事件
109	93	0x1B4	ICU.IELSR93	在ICU.IELSR93寄存器中选择的事件
110	94	0x1B8	ICU.IELSR94	在ICU.IELSR94寄存器中选择的事件
111	95	0x1BC	ICU.IELSR95	在ICU.IELSR95寄存器中选择的事件

13.3.2 事件编号

下表列出了表13.4的标题详细信息，其中描述了每个事件编号。

Heading	Description
中断请求源	产生中断请求的源名称
Name	中断名称
连接到NVIC	“ ”表示该中断可以作为CPU中断使用
Invoke DTC	“ ”表示该中断可用于请求DTC激活
Invoke DMAC	“ ”表示该中断可用于请求DMAC激活
取消贪睡	“ ”表示该中断可用于请求从贪睡模式返回

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Heading	Description
Canceling Software Standby	" ✓" indicates the interrupt can be used to request a return from Software Standby mode
Canceling Deep Software Standby	"✓" indicates the interrupt can be used to request a return from Deep Software Standby mode

Table 13.4 Event table (1 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x001	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
0x002		PORT_IRQ1	✓	✓	✓	✓	✓	✓
0x003		PORT_IRQ2	✓	✓	✓	✓	✓	✓
0x004		PORT_IRQ3	✓	✓	✓	✓	✓	✓
0x005		PORT_IRQ4	✓	✓	✓	✓	✓	✓
0x006		PORT_IRQ5	✓	✓	✓	✓	✓	✓
0x007		PORT_IRQ6	✓	✓	✓	✓	✓	✓
0x008		PORT_IRQ7	✓	✓	✓	✓	✓	✓
0x009		PORT_IRQ8	✓	✓	✓	✓	✓	✓
0x00A		PORT_IRQ9	✓	✓	✓	✓	✓	✓
0x00B		PORT_IRQ10	✓	✓	✓	✓	✓	✓
0x00C		PORT_IRQ11	✓	✓	✓	✓	✓	✓
0x00D		PORT_IRQ12	✓	✓	✓	✓	✓	✓
0x00E		PORT_IRQ13	✓	✓	✓	✓	✓	✓
0x00F		PORT_IRQ14	✓	✓	✓	✓	✓	✓
0x010		PORT_IRQ15	✓	✓	✓	✓	✓	✓
0x020	DMAC0	DMAC0_INT	✓	✓	—	—	—	—
0x021	DMAC1	DMAC1_INT	✓	✓	—	—	—	—
0x022	DMAC2	DMAC2_INT	✓	✓	—	—	—	—
0x023	DMAC3	DMAC3_INT	✓	✓	—	—	—	—
0x024	DMAC4	DMAC4_INT	✓	✓	—	—	—	—
0x025	DMAC5	DMAC5_INT	✓	✓	—	—	—	—
0x026	DMAC6	DMAC6_INT	✓	✓	—	—	—	—
0x027	DMAC7	DMAC7_INT	✓	✓	—	—	—	—
0x029	DTC	DTC_COMPLETE	✓	—	—	✓*3	—	—
0x02B	DMAC/DTC	DMA_TRANSERR	✓	—	—	✓	—	—
0x02D	ICU	ICU_SNZCANCEL	✓	—	—	✓	—	—
0x030	FCU	FCU_FIFERR	✓	—	—	—	—	—
0x031		FCU_FRDYI	✓	—	—	—	—	—
0x038	LVD	LVD_LVD1	✓	—	—	✓	✓	✓
0x039		LVD_LVD2	✓	—	—	✓	✓	✓
0x03B	MOSC	MOSC_STOP	✓	—	—	—	—	—
0x03C	LPW	SYSTEM_SNZREQ	—	✓	—	—	—	—
0x040	AGT0	AGT0_AGTI	✓	✓	✓	—	—	—
0x041		AGT0_AGTCMAI	✓	✓	✓	—	—	—
0x042		AGT0_AGTCMBI	✓	✓	✓	—	—	—

Heading	Description
取消软件待机	" "表示该中断可用于请求从软件待机模式返回
取消深度软件待机	" "表示该中断可用于请求从深度软件待机模式返回

Table 13.4 事件表（1个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件	取消深度
			连接至 NVIC	Invoke DTC	Invoke DMAC		Standby	Software Standby
0x001	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
0x002		PORT_IRQ1	✓	✓	✓	✓	✓	✓
0x003		PORT_IRQ2	✓	✓	✓	✓	✓	✓
0x004		PORT_IRQ3	✓	✓	✓	✓	✓	✓
0x005		PORT_IRQ4	✓	✓	✓	✓	✓	✓
0x006		PORT_IRQ5	✓	✓	✓	✓	✓	✓
0x007		PORT_IRQ6	✓	✓	✓	✓	✓	✓
0x008		PORT_IRQ7	✓	✓	✓	✓	✓	✓
0x009		PORT_IRQ8	✓	✓	✓	✓	✓	✓
0x00A		PORT_IRQ9	✓	✓	✓	✓	✓	✓
0x00B		PORT_IRQ10	✓	✓	✓	✓	✓	✓
0x00C		PORT_IRQ11	✓	✓	✓	✓	✓	✓
0x00D		PORT_IRQ12	✓	✓	✓	✓	✓	✓
0x00E		PORT_IRQ13	✓	✓	✓	✓	✓	✓
0x00F		PORT_IRQ14	✓	✓	✓	✓	✓	✓
0x010		PORT_IRQ15	✓	✓	✓	✓	✓	✓
0x020	DMAC0	DMAC0_INT	✓	✓	—	—	—	—
0x021	DMAC1	DMAC1_INT	✓	✓	—	—	—	—
0x022	DMAC2	DMAC2_INT	✓	✓	—	—	—	—
0x023	DMAC3	DMAC3_INT	✓	✓	—	—	—	—
0x024	DMAC4	DMAC4_INT	✓	✓	—	—	—	—
0x025	DMAC5	DMAC5_INT	✓	✓	—	—	—	—
0x026	DMAC6	DMAC6_INT	✓	✓	—	—	—	—
0x027	DMAC7	DMAC7_INT	✓	✓	—	—	—	—
0x029	DTC	DTC_COMPLETE	✓	—	—	✓*3	—	—
0x02B	DMAC/DTC	DMA_TRANSERR	✓	—	—	✓	—	—
0x02D	ICU	ICU_SNZCANCEL	✓	—	—	✓	—	—
0x030	FCU	FCU_FIFERR	✓	—	—	—	—	—
0x031		FCU_FRDYI	✓	—	—	—	—	—
0x038	LVD	LVD_LVD1	✓	—	—	✓	✓	✓
0x039		LVD_LVD2	✓	—	—	✓	✓	✓
0x03B	MOSC	MOSC_STOP	✓	—	—	—	—	—
0x03C	LPW	SYSTEM_SNZREQ	—	✓	—	—	—	—
0x040	AGT0	AGT0_AGTI	✓	✓	✓	—	—	—
0x041		AGT0_AGTCMAI	✓	✓	✓	—	—	—
0x042		AGT0_AGTCMBI	✓	✓	✓	—	—	—

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Table 13.4 Event table (2 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x043	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
0x044		AGT1_AGTCMAI	✓	✓	✓	✓	✓	—
0x045		AGT1_AGTCMBI	✓	✓	✓	✓	✓	—
0x046	AGT2	AGT2_AGTI	✓	✓	✓	—	—	—
0x047		AGT2_AGTCMAI	✓	✓	✓	—	—	—
0x048		AGT2_AGTCMBI	✓	✓	✓	—	—	—
0x049	AGT3	AGT3_AGTI	✓	✓	✓	✓	✓	✓
0x04A		AGT3_AGTCMAI	✓	✓	✓	✓	✓	—
0x04B		AGT3_AGTCMBI	✓	✓	✓	✓	✓	—
0x04C	AGT4	AGT4_AGTI	✓	✓	✓	—	—	—
0x04D		AGT4_AGTCMAI	✓	✓	✓	—	—	—
0x04E		AGT4_AGTCMBI	✓	✓	✓	—	—	—
0x04F	AGT5	AGT5_AGTI	✓	✓	✓	—	—	—
0x050		AGT5_AGTCMAI	✓	✓	✓	—	—	—
0x051		AGT5_AGTCMBI	✓	✓	✓	—	—	—
0x052	IWDT	IWDT_NMIUNDF	✓	—	—	✓	✓	—
0x053	WDT	WDT_NMIUNDF	✓	—	—	—	—	—
0x054	RTC	RTC_ALM	✓	—	—	✓	✓	✓
0x055		RTC_PRD	✓	—	—	✓	✓	✓
0x056		RTC_CUP	✓	—	—	—	—	—
0x059	CANFD	CAN_RXF	✓	—	—	—	—	—
0x05A		CAN_GLERR	✓	—	—	—	—	—
0x05B		CAN_RF_DMAREQ0	✓	✓	✓	—	—	—
0x05C		CAN_RF_DMAREQ1	✓	✓	✓	—	—	—
0x05D		CAN_RF_DMAREQ2	✓	✓	✓	—	—	—
0x05E		CAN_RF_DMAREQ3	✓	✓	✓	—	—	—
0x05F		CAN_RF_DMAREQ4	✓	✓	✓	—	—	—
0x060		CAN_RF_DMAREQ5	✓	✓	✓	—	—	—
0x061		CAN_RF_DMAREQ6	✓	✓	✓	—	—	—
0x062		CAN_RF_DMAREQ7	✓	✓	✓	—	—	—
0x063		CAN0_TX	✓	—	—	—	—	—
0x064		CAN0_CHERR	✓	—	—	—	—	—
0x065		CAN0_COMFRX	✓	—	—	—	—	—
0x066		CAN0_CF_DMAREQ	✓	✓	✓	—	—	—
0x067		CAN1_TX	✓	—	—	—	—	—
0x068		CAN1_CHERR	✓	—	—	—	—	—
0x069		CAN1_COMFRX	✓	—	—	—	—	—
0x06A		CAN1_CF_DMAREQ	✓	✓	✓	—	—	—

Table 13.4 事件表（2个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x043	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
0x044		AGT1_AGTCMAI	✓	✓	✓	✓	✓	—
0x045		AGT1_AGTCMBI	✓	✓	✓	✓	✓	—
0x046	AGT2	AGT2_AGTI	✓	✓	✓	—	—	—
0x047		AGT2_AGTCMAI	✓	✓	✓	—	—	—
0x048		AGT2_AGTCMBI	✓	✓	✓	—	—	—
0x049	AGT3	AGT3_AGTI	✓	✓	✓	✓	✓	✓
0x04A		AGT3_AGTCMAI	✓	✓	✓	✓	✓	—
0x04B		AGT3_AGTCMBI	✓	✓	✓	✓	✓	—
0x04C	AGT4	AGT4_AGTI	✓	✓	✓	—	—	—
0x04D		AGT4_AGTCMAI	✓	✓	✓	—	—	—
0x04E		AGT4_AGTCMBI	✓	✓	✓	—	—	—
0x04F	AGT5	AGT5_AGTI	✓	✓	✓	—	—	—
0x050		AGT5_AGTCMAI	✓	✓	✓	—	—	—
0x051		AGT5_AGTCMBI	✓	✓	✓	—	—	—
0x052	IWDT	IWDT_NMIUNDF	✓	—	—	✓	✓	—
0x053	WDT	WDT_NMIUNDF	✓	—	—	—	—	—
0x054	RTC	RTC_ALM	✓	—	—	✓	✓	✓
0x055		RTC_PRD	✓	—	—	✓	✓	✓
0x056		RTC_CUP	✓	—	—	—	—	—
0x059	CANFD	CAN_RXF	✓	—	—	—	—	—
0x05A		CAN_GLERR	✓	—	—	—	—	—
0x05B		CAN_RF_DMAREQ0	✓	✓	✓	—	—	—
0x05C		CAN_RF_DMAREQ1	✓	✓	✓	—	—	—
0x05D		CAN_RF_DMAREQ2	✓	✓	✓	—	—	—
0x05E		CAN_RF_DMAREQ3	✓	✓	✓	—	—	—
0x05F		CAN_RF_DMAREQ4	✓	✓	✓	—	—	—
0x060		CAN_RF_DMAREQ5	✓	✓	✓	—	—	—
0x061		CAN_RF_DMAREQ6	✓	✓	✓	—	—	—
0x062		CAN_RF_DMAREQ7	✓	✓	✓	—	—	—
0x063		CAN0_TX	✓	—	—	—	—	—
0x064		CAN0_CHERR	✓	—	—	—	—	—
0x065		CAN0_COMFRX	✓	—	—	—	—	—
0x066		CAN0_CF_DMAREQ	✓	✓	✓	—	—	—
0x067		CAN1_TX	✓	—	—	—	—	—
0x068		CAN1_CHERR	✓	—	—	—	—	—
0x069		CAN1_COMFRX	✓	—	—	—	—	—
0x06A		CAN1_CF_DMAREQ	✓	✓	✓	—	—	—

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Table 13.4 Event table (3 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x06B	USBFS	USBFS0_D0FIFO	✓	✓	✓	—	—	—
0x06C		USBFS0_D1FIFO	✓	✓	✓	—	—	—
0x06D		USBFS0_USBI	✓	—	—	—	—	—
0x06E		USBFS0_USBR	✓	—	—	✓	✓	✓
0x073	IIC0	IIC0_RXI	✓	✓	✓	—	—	—
0x074		IIC0_TXI	✓	✓	✓	—	—	—
0x075		IIC0_TEI	✓	—	—	—	—	—
0x076		IIC0_EEI	✓	—	—	—	—	—
0x077		IIC0_WUI	✓	—	—	✓	✓	—
0x078	IIC1	IIC1_RXI	✓	✓	✓	—	—	—
0x079		IIC1_TXI	✓	✓	✓	—	—	—
0x07A		IIC1_TEI	✓	—	—	—	—	—
0x07B		IIC1_EEI	✓	—	—	—	—	—
0x07D	IIC2	IIC2_RXI	✓	✓	✓	—	—	—
0x07E		IIC2_TXI	✓	✓	✓	—	—	—
0x07F		IIC2_TEI	✓	—	—	—	—	—
0x080		IIC2_EEI	✓	—	—	—	—	—
0x082	SDHI MMC	SDHI_MMC0_ACCS	✓	—	—	—	—	—
0x083		SDHI_MMC0_SDIO	✓	—	—	—	—	—
0x084		SDHI_MMC0_CARD	✓	—	—	—	—	—
0x085		SDHI_MMC0_ODMSDBREQ	—	✓	✓	—	—	—
0x08A	SSI	SSI0_SSITXI	✓	✓	✓	—	—	—
0x08B		SSI0_SSIRXI	✓	✓	✓	—	—	—
0x08D		SSI0_SSIF	✓	—	—	—	—	—
0x09A	CTSU	CTSU_CTSUWR	✓	✓	✓	—	—	—
0x09B		CTSU_CTSURD	✓	✓	✓	—	—	—
0x09C		CTSU_CTSUFN	✓	—	—	✓*3	—	—
0x09E	CAC	CAC_FEERI	✓	—	—	—	—	—
0x09F		CAC_MENDI	✓	—	—	—	—	—
0x0A0		CAC_OVFI	✓	—	—	—	—	—
0x0AB	CEC	CEC_INTDA	✓	✓	✓	—	—	—
0x0AC		CEC_INTCE	✓	—	—	—	—	—
0x0AD		CEC_INTERR	✓	—	—	—	—	—
0x0B1	PORT	IOPORT_GROUP1	✓	✓*1	✓*1	—	—	—
0x0B2		IOPORT_GROUP2	✓	✓*1	✓*1	—	—	—
0x0B3		IOPORT_GROUP3	✓	✓*1	✓*1	—	—	—
0x0B4		IOPORT_GROUP4	✓	✓*1	✓*1	—	—	—

Table 13.4 事件表（3个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x06B	USBFS	USBFS0_D0FIFO	✓	✓	✓	—	—	—
0x06C		USBFS0_D1FIFO	✓	✓	✓	—	—	—
0x06D		USBFS0_USBI	✓	—	—	—	—	—
0x06E		USBFS0_USBR	✓	—	—	✓	✓	✓
0x073	IIC0	IIC0_RXI	✓	✓	✓	—	—	—
0x074		IIC0_TXI	✓	✓	✓	—	—	—
0x075		IIC0_TEI	✓	—	—	—	—	—
0x076		IIC0_EEI	✓	—	—	—	—	—
0x077		IIC0_WUI	✓	—	—	✓	✓	—
0x078	IIC1	IIC1_RXI	✓	✓	✓	—	—	—
0x079		IIC1_TXI	✓	✓	✓	—	—	—
0x07A		IIC1_TEI	✓	—	—	—	—	—
0x07B		IIC1_EEI	✓	—	—	—	—	—
0x07D	IIC2	IIC2_RXI	✓	✓	✓	—	—	—
0x07E		IIC2_TXI	✓	✓	✓	—	—	—
0x07F		IIC2_TEI	✓	—	—	—	—	—
0x080		IIC2_EEI	✓	—	—	—	—	—
0x082	SDHI MMC	SDHI_MMC0_ACCS	✓	—	—	—	—	—
0x083		SDHI_MMC0_SDIO	✓	—	—	—	—	—
0x084		SDHI_MMC0_CARD	✓	—	—	—	—	—
0x085		SDHI_MMC0_ODMSDBREQ	—	✓	✓	—	—	—
0x08A	SSI	SSI0_SSITXI	✓	✓	✓	—	—	—
0x08B		SSI0_SSIRXI	✓	✓	✓	—	—	—
0x08D		SSI0_SSIF	✓	—	—	—	—	—
0x09A	CTSU	CTSU_CTSUWR	✓	✓	✓	—	—	—
0x09B		CTSU_CTSURD	✓	✓	✓	—	—	—
0x09C		CTSU_CTSUFN	✓	—	—	✓*3	—	—
0x09E	CAC	CAC_FEERI	✓	—	—	—	—	—
0x09F		CAC_MENDI	✓	—	—	—	—	—
0x0A0		CAC_OVFI	✓	—	—	—	—	—
0x0AB	CEC	CEC_INTDA	✓	✓	✓	—	—	—
0x0AC		CEC_INTCE	✓	—	—	—	—	—
0x0AD		CEC_INTERR	✓	—	—	—	—	—
0x0B1	PORT	IOPORT_GROUP1	✓	✓*1	✓*1	—	—	—
0x0B2		IOPORT_GROUP2	✓	✓*1	✓*1	—	—	—
0x0B3		IOPORT_GROUP3	✓	✓*1	✓*1	—	—	—
0x0B4		IOPORT_GROUP4	✓	✓*1	✓*1	—	—	—

Table 13.4 Event table (4 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0B5	ELC	ELC_SWEVT0	✓*2	✓	—	—	—	—
0x0B6		ELC_SWEVT1	✓*2	✓	—	—	—	—
0x0B7	POEG	POEG_GROUPA	✓	—	—	—	—	—
0x0B8		POEG_GROUPB	✓	—	—	—	—	—
0x0B9		POEG_GROUPC	✓	—	—	—	—	—
0x0BA		POEG_GROUPD	✓	—	—	—	—	—
0x0C0	GPT0	GPT0_CCMPA	✓	✓	✓	—	—	—
0x0C1		GPT0_CCMPB	✓	✓	✓	—	—	—
0x0C2		GPT0_CMPC	✓	✓	✓	—	—	—
0x0C3		GPT0_CMPD	✓	✓	✓	—	—	—
0x0C4		GPT0_CMPE	✓	✓	✓	—	—	—
0x0C5		GPT0_CMPF	✓	✓	✓	—	—	—
0x0C6		GPT0_OVF	✓	✓	✓	—	—	—
0x0C7		GPT0_UDF	✓	✓	✓	—	—	—
0x0C8		GPT0_PC	✓	✓	✓	—	—	—
0x0C9	GPT1	GPT1_CCMPA	✓	✓	✓	—	—	—
0x0CA		GPT1_CCMPB	✓	✓	✓	—	—	—
0x0CB		GPT1_CMPC	✓	✓	✓	—	—	—
0x0CC		GPT1_CMPD	✓	✓	✓	—	—	—
0x0CD		GPT1_CMPE	✓	✓	✓	—	—	—
0x0CE		GPT1_CMPF	✓	✓	✓	—	—	—
0x0CF		GPT1_OVF	✓	✓	✓	—	—	—
0x0D0		GPT1_UDF	✓	✓	✓	—	—	—
0x0D1		GPT1_PC	✓	✓	✓	—	—	—
0x0D2	GPT2	GPT2_CCMPA	✓	✓	✓	—	—	—
0x0D3		GPT2_CCMPB	✓	✓	✓	—	—	—
0x0D4		GPT2_CMPC	✓	✓	✓	—	—	—
0x0D5		GPT2_CMPD	✓	✓	✓	—	—	—
0x0D6		GPT2_CMPE	✓	✓	✓	—	—	—
0x0D7		GPT2_CMPF	✓	✓	✓	—	—	—
0x0D8		GPT2_OVF	✓	✓	✓	—	—	—
0x0D9		GPT2_UDF	✓	✓	✓	—	—	—

Table 13.4 事件表（4个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x0B5	ELC	ELC_SWEVT0	✓*2	✓	—	—	—	—
0x0B6		ELC_SWEVT1	✓*2	✓	—	—	—	—
0x0B7	POEG	POEG_GROUPA	✓	—	—	—	—	—
0x0B8		POEG_GROUPB	✓	—	—	—	—	—
0x0B9		POEG_GROUPC	✓	—	—	—	—	—
0x0BA		POEG_GROUPD	✓	—	—	—	—	—
0x0C0	GPT0	GPT0_CCMPA	✓	✓	✓	—	—	—
0x0C1		GPT0_CCMPB	✓	✓	✓	—	—	—
0x0C2		GPT0_CMPC	✓	✓	✓	—	—	—
0x0C3		GPT0_CMPD	✓	✓	✓	—	—	—
0x0C4		GPT0_CMPE	✓	✓	✓	—	—	—
0x0C5		GPT0_CMPF	✓	✓	✓	—	—	—
0x0C6		GPT0_OVF	✓	✓	✓	—	—	—
0x0C7		GPT0_UDF	✓	✓	✓	—	—	—
0x0C8		GPT0_PC	✓	✓	✓	—	—	—
0x0C9	GPT1	GPT1_CCMPA	✓	✓	✓	—	—	—
0x0CA		GPT1_CCMPB	✓	✓	✓	—	—	—
0x0CB		GPT1_CMPC	✓	✓	✓	—	—	—
0x0CC		GPT1_CMPD	✓	✓	✓	—	—	—
0x0CD		GPT1_CMPE	✓	✓	✓	—	—	—
0x0CE		GPT1_CMPF	✓	✓	✓	—	—	—
0x0CF		GPT1_OVF	✓	✓	✓	—	—	—
0x0D0		GPT1_UDF	✓	✓	✓	—	—	—
0x0D1		GPT1_PC	✓	✓	✓	—	—	—
0x0D2	GPT2	GPT2_CCMPA	✓	✓	✓	—	—	—
0x0D3		GPT2_CCMPB	✓	✓	✓	—	—	—
0x0D4		GPT2_CMPC	✓	✓	✓	—	—	—
0x0D5		GPT2_CMPD	✓	✓	✓	—	—	—
0x0D6		GPT2_CMPE	✓	✓	✓	—	—	—
0x0D7		GPT2_CMPF	✓	✓	✓	—	—	—
0x0D8		GPT2_OVF	✓	✓	✓	—	—	—
0x0D9		GPT2_UDF	✓	✓	✓	—	—	—

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Table 13.4 Event table (5 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0DB	GPT3	GPT3_CCMPA	✓	✓	✓	—	—	—
0x0DC		GPT3_CCMPB	✓	✓	✓	—	—	—
0x0DD		GPT3_CMPC	✓	✓	✓	—	—	—
0x0DE		GPT3_CMPD	✓	✓	✓	—	—	—
0x0DF		GPT3_CMPE	✓	✓	✓	—	—	—
0x0E0		GPT3_CMPF	✓	✓	✓	—	—	—
0x0E1		GPT3_OVF	✓	✓	✓	—	—	—
0x0E2		GPT3_UDF	✓	✓	✓	—	—	—
0x0E4	GPT4	GPT4_CCMPA	✓	✓	✓	—	—	—
0x0E5		GPT4_CCMPB	✓	✓	✓	—	—	—
0x0E6		GPT4_CMPC	✓	✓	✓	—	—	—
0x0E7		GPT4_CMPD	✓	✓	✓	—	—	—
0x0E8		GPT4_CMPE	✓	✓	✓	—	—	—
0x0E9		GPT4_CMPF	✓	✓	✓	—	—	—
0x0EA		GPT4_OVF	✓	✓	✓	—	—	—
0x0EB		GPT4_UDF	✓	✓	✓	—	—	—
0x0EC		GPT4_PC	✓	✓	✓	—	—	—
0x0ED	GPT5	GPT5_CCMPA	✓	✓	✓	—	—	—
0x0EE		GPT5_CCMPB	✓	✓	✓	—	—	—
0x0EF		GPT5_CMPC	✓	✓	✓	—	—	—
0x0F0		GPT5_CMPD	✓	✓	✓	—	—	—
0x0F1		GPT5_CMPE	✓	✓	✓	—	—	—
0x0F2		GPT5_CMPF	✓	✓	✓	—	—	—
0x0F3		GPT5_OVF	✓	✓	✓	—	—	—
0x0F4		GPT5_UDF	✓	✓	✓	—	—	—
0x0F5		GPT5_PC	✓	✓	✓	—	—	—
0x0F6	GPT6	GPT6_CCMPA	✓	✓	✓	—	—	—
0x0F7		GPT6_CCMPB	✓	✓	✓	—	—	—
0x0F8		GPT6_CMPC	✓	✓	✓	—	—	—
0x0F9		GPT6_CMPD	✓	✓	✓	—	—	—
0x0FA		GPT6_CMPE	✓	✓	✓	—	—	—
0x0FB		GPT6_CMPF	✓	✓	✓	—	—	—
0x0FC		GPT6_OVF	✓	✓	✓	—	—	—
0x0FD		GPT6_UDF	✓	✓	✓	—	—	—
0x0FE		GPT6_PC	✓	✓	✓	—	—	—

Table 13.4 事件表（5个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x0DB	GPT3	GPT3_CCMPA	✓	✓	✓	—	—	—
0x0DC		GPT3_CCMPB	✓	✓	✓	—	—	—
0x0DD		GPT3_CMPC	✓	✓	✓	—	—	—
0x0DE		GPT3_CMPD	✓	✓	✓	—	—	—
0x0DF		GPT3_CMPE	✓	✓	✓	—	—	—
0x0E0		GPT3_CMPF	✓	✓	✓	—	—	—
0x0E1		GPT3_OVF	✓	✓	✓	—	—	—
0x0E2		GPT3_UDF	✓	✓	✓	—	—	—
0x0E4	GPT4	GPT4_CCMPA	✓	✓	✓	—	—	—
0x0E5		GPT4_CCMPB	✓	✓	✓	—	—	—
0x0E6		GPT4_CMPC	✓	✓	✓	—	—	—
0x0E7		GPT4_CMPD	✓	✓	✓	—	—	—
0x0E8		GPT4_CMPE	✓	✓	✓	—	—	—
0x0E9		GPT4_CMPF	✓	✓	✓	—	—	—
0x0EA		GPT4_OVF	✓	✓	✓	—	—	—
0x0EB		GPT4_UDF	✓	✓	✓	—	—	—
0x0EC		GPT4_PC	✓	✓	✓	—	—	—
0x0ED	GPT5	GPT5_CCMPA	✓	✓	✓	—	—	—
0x0EE		GPT5_CCMPB	✓	✓	✓	—	—	—
0x0EF		GPT5_CMPC	✓	✓	✓	—	—	—
0x0F0		GPT5_CMPD	✓	✓	✓	—	—	—
0x0F1		GPT5_CMPE	✓	✓	✓	—	—	—
0x0F2		GPT5_CMPF	✓	✓	✓	—	—	—
0x0F3		GPT5_OVF	✓	✓	✓	—	—	—
0x0F4		GPT5_UDF	✓	✓	✓	—	—	—
0x0F5		GPT5_PC	✓	✓	✓	—	—	—
0x0F6	GPT6	GPT6_CCMPA	✓	✓	✓	—	—	—
0x0F7		GPT6_CCMPB	✓	✓	✓	—	—	—
0x0F8		GPT6_CMPC	✓	✓	✓	—	—	—
0x0F9		GPT6_CMPD	✓	✓	✓	—	—	—
0x0FA		GPT6_CMPE	✓	✓	✓	—	—	—
0x0FB		GPT6_CMPF	✓	✓	✓	—	—	—
0x0FC		GPT6_OVF	✓	✓	✓	—	—	—
0x0FD		GPT6_UDF	✓	✓	✓	—	—	—
0x0FE		GPT6_PC	✓	✓	✓	—	—	—

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Table 13.4 Event table (6 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x0FF	GPT7	GPT7_CCMPA	✓	✓	✓	—	—	—
0x100		GPT7_CCMPB	✓	✓	✓	—	—	—
0x101		GPT7_CMPC	✓	✓	✓	—	—	—
0x102		GPT7_CMPD	✓	✓	✓	—	—	—
0x103		GPT7_CMPE	✓	✓	✓	—	—	—
0x104		GPT7_CMPF	✓	✓	✓	—	—	—
0x105		GPT7_OVF	✓	✓	✓	—	—	—
0x106		GPT7_UDF	✓	✓	✓	—	—	—
0x108	GPT8	GPT8_CCMPA	✓	✓	✓	—	—	—
0x109		GPT8_CCMPB	✓	✓	✓	—	—	—
0x10A		GPT8_CMPC	✓	✓	✓	—	—	—
0x10B		GPT8_CMPD	✓	✓	✓	—	—	—
0x10C		GPT8_CMPE	✓	✓	✓	—	—	—
0x10D		GPT8_CMPF	✓	✓	✓	—	—	—
0x10E		GPT8_OVF	✓	✓	✓	—	—	—
0x10F		GPT8_UDF	✓	✓	✓	—	—	—
0x111	GPT9	GPT9_CCMPA	✓	✓	✓	—	—	—
0x112		GPT9_CCMPB	✓	✓	✓	—	—	—
0x113		GPT9_CMPC	✓	✓	✓	—	—	—
0x114		GPT9_CMPD	✓	✓	✓	—	—	—
0x115		GPT9_CMPE	✓	✓	✓	—	—	—
0x116		GPT9_CMPF	✓	✓	✓	—	—	—
0x117		GPT9_OVF	✓	✓	✓	—	—	—
0x118		GPT9_UDF	✓	✓	✓	—	—	—
0x150	GPT	GPT_UVWEDGE	✓	—	—	—	—	—
0x160	ADC120	ADC120_ADI	✓	✓	✓	—	—	—
0x161		ADC120_GBADI	✓	✓	✓	—	—	—
0x162		ADC120_CMPAI	✓	—	—	—	—	—
0x163		ADC120_CMPBI	✓	—	—	—	—	—
0x164		ADC120_WCMPM	—	✓	✓	✓*3	—	—
0x165		ADC120_WCMPUM	—	✓	✓	✓*3	—	—
0x166	ADC121	ADC121_ADII	✓	✓	✓	—	—	—
0x167		ADC121_GBADI	✓	✓	✓	—	—	—
0x168		ADC121_CMPAI	✓	—	—	—	—	—
0x169		ADC121_CMPBI	✓	—	—	—	—	—
0x16A		ADC121_WCMPM	—	✓	✓	✓*3	—	—
0x16B		ADC121_WCMPUM	—	✓	✓	✓*3	—	—
0x16F	ETHER	ETHER_EINT0	✓	—	—	—	—	—

Table 13.4 事件表（6个，共8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x0FF	GPT7	GPT7_CCMPA	✓	✓	✓	—	—	—
0x100		GPT7_CCMPB	✓	✓	✓	—	—	—
0x101		GPT7_CMPC	✓	✓	✓	—	—	—
0x102		GPT7_CMPD	✓	✓	✓	—	—	—
0x103		GPT7_CMPE	✓	✓	✓	—	—	—
0x104		GPT7_CMPF	✓	✓	✓	—	—	—
0x105		GPT7_OVF	✓	✓	✓	—	—	—
0x106		GPT7_UDF	✓	✓	✓	—	—	—
0x108	GPT8	GPT8_CCMPA	✓	✓	✓	—	—	—
0x109		GPT8_CCMPB	✓	✓	✓	—	—	—
0x10A		GPT8_CMPC	✓	✓	✓	—	—	—
0x10B		GPT8_CMPD	✓	✓	✓	—	—	—
0x10C		GPT8_CMPE	✓	✓	✓	—	—	—
0x10D		GPT8_CMPF	✓	✓	✓	—	—	—
0x10E		GPT8_OVF	✓	✓	✓	—	—	—
0x10F		GPT8_UDF	✓	✓	✓	—	—	—
0x111	GPT9	GPT9_CCMPA	✓	✓	✓	—	—	—
0x112		GPT9_CCMPB	✓	✓	✓	—	—	—
0x113		GPT9_CMPC	✓	✓	✓	—	—	—
0x114		GPT9_CMPD	✓	✓	✓	—	—	—
0x115		GPT9_CMPE	✓	✓	✓	—	—	—
0x116		GPT9_CMPF	✓	✓	✓	—	—	—
0x117		GPT9_OVF	✓	✓	✓	—	—	—
0x118		GPT9_UDF	✓	✓	✓	—	—	—
0x150	GPT	GPT_UVWEDGE	✓	—	—	—	—	—
0x160	ADC120	ADC120_ADI	✓	✓	✓	—	—	—
0x161		ADC120_GBADI	✓	✓	✓	—	—	—
0x162		ADC120_CMPAI	✓	—	—	—	—	—
0x163		ADC120_CMPBI	✓	—	—	—	—	—
0x164		ADC120_WCMPM	—	✓	✓	✓*3	—	—
0x165		ADC120_WCMPUM	—	✓	✓	✓*3	—	—
0x166	ADC121	ADC121_ADII	✓	✓	✓	—	—	—
0x167		ADC121_GBADI	✓	✓	✓	—	—	—
0x168		ADC121_CMPAI	✓	—	—	—	—	—
0x169		ADC121_CMPBI	✓	—	—	—	—	—
0x16A		ADC121_WCMPM	—	✓	✓	✓*3	—	—
0x16B		ADC121_WCMPUM	—	✓	✓	✓*3	—	—
0x16F	ETHER	ETHER_EINT0	✓	—	—	—	—	—

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Table 13.4 Event table (7 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x17D	USBHS	USBHS_D0FIFO	✓	✓	✓	—	—	—
0x17E		USBHS_D1FIFO	✓	✓	✓	—	—	—
0x17F		USBHS_USBIR	✓	—	—	✓	✓	✓
0x180	SCI0	SCI0_RXI	✓	✓	✓	—	—	—
0x181		SCI0_TXI	✓	✓	✓	—	—	—
0x182		SCI0_TEI	✓	—	—	—	—	—
0x183		SCI0_ERI	✓	—	—	—	—	—
0x184		SCI0_AM	✓	—	—	✓*3	—	—
0x185		SCI0_RXI_OR_ERI	—	—	—	✓*3	—	—
0x186	SCI1	SCI1_RXI	✓	✓	✓	—	—	—
0x187		SCI1_TXI	✓	✓	✓	—	—	—
0x188		SCI1_TEI	✓	—	—	—	—	—
0x189		SCI1_ERI	✓	—	—	—	—	—
0x18C	SCI2	SCI2_RXI	✓	✓	✓	—	—	—
0x18D		SCI2_TXI	✓	✓	✓	—	—	—
0x18E		SCI2_TEI	✓	—	—	—	—	—
0x18F		SCI2_ERI	✓	—	—	—	—	—
0x192	SCI3	SCI3_RXI	✓	✓	✓	—	—	—
0x193		SCI3_TXI	✓	✓	✓	—	—	—
0x194		SCI3_TEI	✓	—	—	—	—	—
0x195		SCI3_ERI	✓	—	—	—	—	—
0x196		SCI3_AM	✓	—	—	—	—	—
0x198	SCI4	SCI4_RXI	✓	✓	✓	—	—	—
0x199		SCI4_TXI	✓	✓	✓	—	—	—
0x19A		SCI4_TEI	✓	—	—	—	—	—
0x19B		SCI4_ERI	✓	—	—	—	—	—
0x19C		SCI4_AM	✓	—	—	—	—	—
0x19E	SCI5	SCI5_RXI	✓	✓	✓	—	—	—
0x19F		SCI5_TXI	✓	✓	✓	—	—	—
0x1A0		SCI5_TEI	✓	—	—	—	—	—
0x1A1		SCI5_ERI	✓	—	—	—	—	—
0x1A2		SCI5_AM	✓	—	—	—	—	—
0x1A4	SCI6	SCI6_RXI	✓	✓	✓	—	—	—
0x1A5		SCI6_TXI	✓	✓	✓	—	—	—
0x1A6		SCI6_TEI	✓	—	—	—	—	—
0x1A7		SCI6_ERI	✓	—	—	—	—	—
0x1A8		SCI6_AM	✓	—	—	—	—	—

Table 13.4 事件表（8个中的7个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x17D	USBHS	USBHS_D0FIFO	✓	✓	✓	—	—	—
0x17E		USBHS_D1FIFO	✓	✓	✓	—	—	—
0x17F		USBHS_USBIR	✓	—	—	✓	✓	✓
0x180	SCI0	SCI0_RXI	✓	✓	✓	—	—	—
0x181		SCI0_TXI	✓	✓	✓	—	—	—
0x182		SCI0_TEI	✓	—	—	—	—	—
0x183		SCI0_ERI	✓	—	—	—	—	—
0x184		SCI0_AM	✓	—	—	✓*3	—	—
0x185		SCI0_RXI_OR_ERI	—	—	—	✓*3	—	—
0x186	SCI1	SCI1_RXI	✓	✓	✓	—	—	—
0x187		SCI1_TXI	✓	✓	✓	—	—	—
0x188		SCI1_TEI	✓	—	—	—	—	—
0x189		SCI1_ERI	✓	—	—	—	—	—
0x18C	SCI2	SCI2_RXI	✓	✓	✓	—	—	—
0x18D		SCI2_TXI	✓	✓	✓	—	—	—
0x18E		SCI2_TEI	✓	—	—	—	—	—
0x18F		SCI2_ERI	✓	—	—	—	—	—
0x192	SCI3	SCI3_RXI	✓	✓	✓	—	—	—
0x193		SCI3_TXI	✓	✓	✓	—	—	—
0x194		SCI3_TEI	✓	—	—	—	—	—
0x195		SCI3_ERI	✓	—	—	—	—	—
0x196		SCI3_AM	✓	—	—	—	—	—
0x198	SCI4	SCI4_RXI	✓	✓	✓	—	—	—
0x199		SCI4_TXI	✓	✓	✓	—	—	—
0x19A		SCI4_TEI	✓	—	—	—	—	—
0x19B		SCI4_ERI	✓	—	—	—	—	—
0x19C		SCI4_AM	✓	—	—	—	—	—
0x19E	SCI5	SCI5_RXI	✓	✓	✓	—	—	—
0x19F		SCI5_TXI	✓	✓	✓	—	—	—
0x1A0		SCI5_TEI	✓	—	—	—	—	—
0x1A1		SCI5_ERI	✓	—	—	—	—	—
0x1A2		SCI5_AM	✓	—	—	—	—	—
0x1A4	SCI6	SCI6_RXI	✓	✓	✓	—	—	—
0x1A5		SCI6_TXI	✓	✓	✓	—	—	—
0x1A6		SCI6_TEI	✓	—	—	—	—	—
0x1A7		SCI6_ERI	✓	—	—	—	—	—
0x1A8		SCI6_AM	✓	—	—	—	—	—

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Table 13.4 Event table (8 of 8)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze	Canceling Software Standby	Canceling Deep Software Standby
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0x1AA	SCI7	SCI7_RXI	✓	✓	✓	—	—	—
0x1AB		SCI7_TXI	✓	✓	✓	—	—	—
0x1AC		SCI7_TEI	✓	—	—	—	—	—
0x1AD		SCI7_ERI	✓	—	—	—	—	—
0x1AE		SCI7_AM	✓	—	—	—	—	—
0x1B0	SCI8	SCI8_RXI	✓	✓	✓	—	—	—
0x1B1		SCI8_TXI	✓	✓	✓	—	—	—
0x1B2		SCI8_TEI	✓	—	—	—	—	—
0x1B3		SCI8_ERI	✓	—	—	—	—	—
0x1B4		SCI8_AM	✓	—	—	—	—	—
0x1B6	SCI9	SCI9_RXI	✓	✓	✓	—	—	—
0x1B7		SCI9_TXI	✓	✓	✓	—	—	—
0x1B8		SCI9_TEI	✓	—	—	—	—	—
0x1B9		SCI9_ERI	✓	—	—	—	—	—
0x1BA		SCI9_AM	✓	—	—	—	—	—
0x1BC	SCIX0	SCIX0_SCIX0	✓	—	—	—	—	—
0x1BD		SCIX0_SCIX1	✓	—	—	—	—	—
0x1BE		SCIX0_SCIX2	✓	—	—	—	—	—
0x1BF		SCIX0_SCIX3	✓	—	—	—	—	—
0x1C0	SCIX1	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1CE	CANFD ECC	CAN_AFLRAM0_ERI	✓	—	—	—	—	—
0x1CF		CAN_AFLRAM1_ERI	✓	—	—	—	—	—
0x1D0		CAN_MRAM_ERI	✓	—	—	—	—	—
0x1D9	OSPI	OSPI_INTR	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

Note 1. Only the first edge detection is valid.

Table 13.4 事件表（8个中的8个）

事件编号	中断请求源	Name	IELSRn		DELSRn	取消贪睡	取消软件 Standby	取消深度 Software Standby
			连接至 NVIC	Invoke DTC	Invoke DMAC			
0x1AA	SCI7	SCI7_RXI	✓	✓	✓	—	—	—
0x1AB		SCI7_TXI	✓	✓	✓	—	—	—
0x1AC		SCI7_TEI	✓	—	—	—	—	—
0x1AD		SCI7_ERI	✓	—	—	—	—	—
0x1AE		SCI7_AM	✓	—	—	—	—	—
0x1B0	SCI8	SCI8_RXI	✓	✓	✓	—	—	—
0x1B1		SCI8_TXI	✓	✓	✓	—	—	—
0x1B2		SCI8_TEI	✓	—	—	—	—	—
0x1B3		SCI8_ERI	✓	—	—	—	—	—
0x1B4		SCI8_AM	✓	—	—	—	—	—
0x1B6	SCI9	SCI9_RXI	✓	✓	✓	—	—	—
0x1B7		SCI9_TXI	✓	✓	✓	—	—	—
0x1B8		SCI9_TEI	✓	—	—	—	—	—
0x1B9		SCI9_ERI	✓	—	—	—	—	—
0x1BA		SCI9_AM	✓	—	—	—	—	—
0x1BC	SCIX0	SCIX0_SCIX0	✓	—	—	—	—	—
0x1BD		SCIX0_SCIX1	✓	—	—	—	—	—
0x1BE		SCIX0_SCIX2	✓	—	—	—	—	—
0x1BF		SCIX0_SCIX3	✓	—	—	—	—	—
0x1C0	SCIX1	SCIX1_SCIX0	✓	—	—	—	—	—
0x1C1		SCIX1_SCIX1	✓	—	—	—	—	—
0x1C2		SCIX1_SCIX2	✓	—	—	—	—	—
0x1C3		SCIX1_SCIX3	✓	—	—	—	—	—
0x1C4	SPI0	SPI0_SPRI	✓	✓	✓	—	—	—
0x1C5		SPI0_SPTI	✓	✓	✓	—	—	—
0x1C6		SPI0_SPII	✓	—	—	—	—	—
0x1C7		SPI0_SPEI	✓	—	—	—	—	—
0x1C8		SPI0_SPCEND	✓	—	—	—	—	—
0x1C9	SPI1	SPI1_SPRI	✓	✓	✓	—	—	—
0x1CA		SPI1_SPTI	✓	✓	✓	—	—	—
0x1CB		SPI1_SPII	✓	—	—	—	—	—
0x1CC		SPI1_SPEI	✓	—	—	—	—	—
0x1CD		SPI1_SPCEND	✓	—	—	—	—	—
0x1CE	CANFD ECC	CAN_AFLRAM0_ERI	✓	—	—	—	—	—
0x1CF		CAN_AFLRAM1_ERI	✓	—	—	—	—	—
0x1D0		CAN_MRAM_ERI	✓	—	—	—	—	—
0x1D9	OSPI	OSPI_INTR	✓	—	—	—	—	—
0x1DA	QSPI	QSPI_INTR	✓	—	—	—	—	—
0x1DB	DOC	DOC_DOPCI	✓	—	—	✓*3	—	—

注1.只有第一个边缘检测有效。

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Note 2. Only interrupts after DTC transfer are supported.
Note 3. Using SELSR0.

13.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation, and DMAC activation.

13.4.1 Detecting Interrupts

The ICU selects an event source input from a peripheral function interrupt or an external pin interrupt with IELSRn.IELS[8:0].

The accepted interrupt source sets the IELSRn.IR to 1 and sends an interrupt request to the NVIC.

External pin interrupt requests are detected by either:

- Edges (falling edge, rising edge, or rising and falling edges)
- Level (low level) of the interrupt signal.

Set the IRQCRi.IRQMD[1:0] bits to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see Table 13.3 and Table 13.4. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

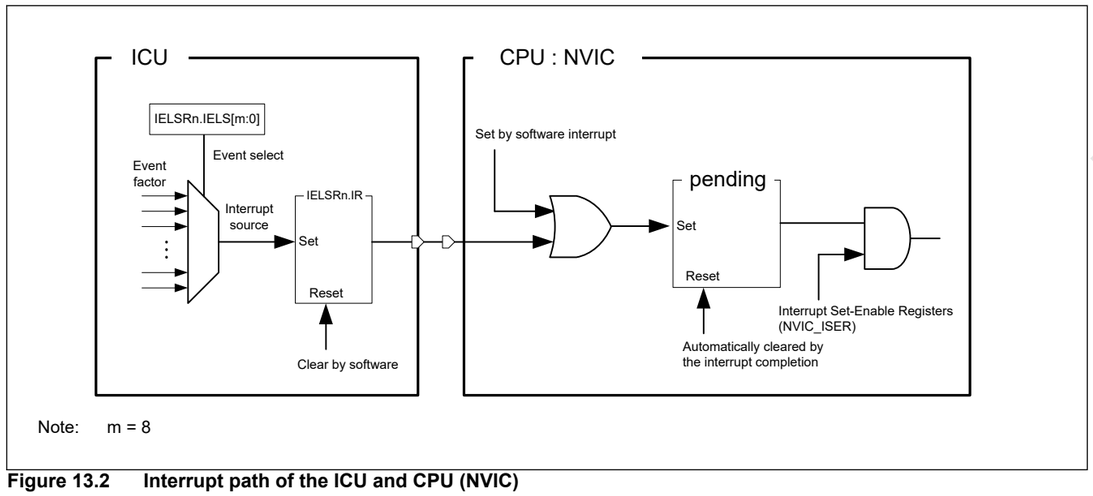

Figure 13.2 Interrupt path of the ICU and CPU (NVIC)

13.5 Interrupt setting procedure

13.5.1 Enabling Interrupt Requests

The procedure for enabling an interrupt request is as follows:

1. Set the Interrupt Set-Enable register (NVIC_ISER).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).

13.5.2 Disabling Interrupt Requests

注2.仅支持DTC传输后的中断。
注3.使用SELSR0。

13.4 中断操作

ICU执行以下功能：

●检测中断

●启用和禁用中断

●选择中断请求目标，例如CPU中断、DTC激活和DMAC激活。

13.4.1 检测中断

ICU通过IELSRn.IELS[8:0]从外围功能中断或外部引脚中断选择事件源输入。

接受的中断源将IELSRn.IR设置为1，并向NVIC发送中断请求。

外部引脚中断请求通过以下任一方式检测：

●边沿（下降沿、上升沿或上升沿和下降沿）

●中断信号的电平（低电平）。

设置IRQCRi.IRQMD[1:0]位以选择IRQi引脚的检测模式。对于与外围模块相关的中断源，请参见表13.3和表13.4。事件必须在中断发生之前被NVIC接受并被CPU接受。

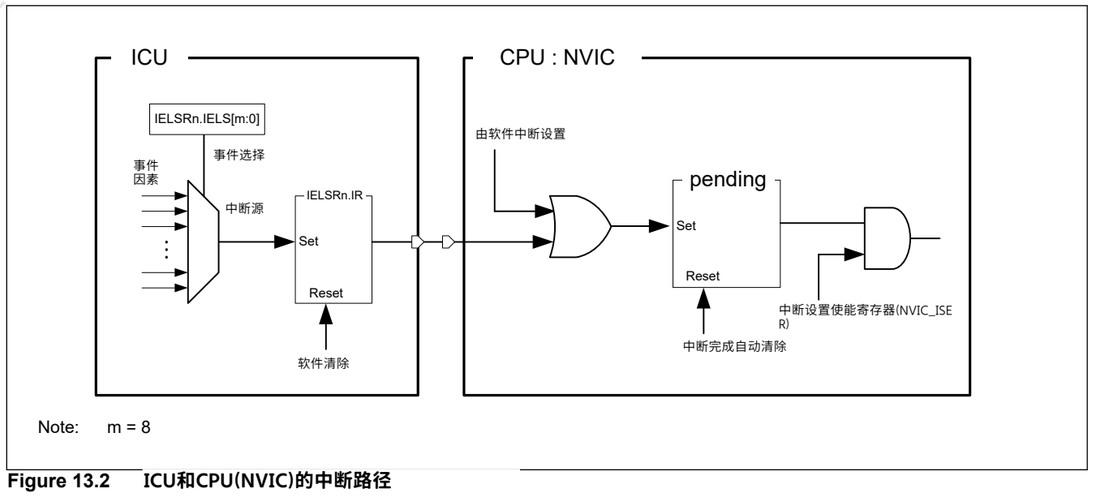

Figure 13.2 ICU和CPU(NVIC)的中断路径

13.5 中断设置程序

13.5.1 启用中断请求

使能中断请求的过程如下：

1.设置中断设置使能寄存器(NVIC_ISER)。

2.将IELSRn.IELS[8:0]位设置为中断源。

3.指定事件源的操作设置，例如DMAC激活（DELSRn.DELS[8:0]）、贪睡模式取消（SELSR0.SELS[8:0]）、软件待机模式取消（WUPEN寄存器设置）。

13.5.2 禁用中断请求

The procedure to disable the interrupt request is as follows:

1. Disable the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).
2. Clear the interrupt source setting (IELSRn.IELS[8:0] = 0x00).
3. Clear the interrupt status flag (IELSRn.IR = 0).
4. Clear the interrupt Clear-Enable register (NVIC_ICER) and interrupt Clear-Pending register (NVIC_ICPR).

13.5.3 Polling for interrupts

The procedure for polling for interrupt requests is as follows:

1. Set the Interrupt Clear-Enable register (NVIC_ICER).
2. Set the IELSRn.IELS[8:0] bits as the interrupt source.
3. Specify the operation settings for the event source, such as DMAC activation (DELSRn.DELS[8:0]), snooze mode cancellation (SELSR0.SELS[8:0]), software standby mode cancellation (WUPEN register setting).
4. Poll the interrupt Set-Pending register (NVIC_ISPR).

13.5.4 Selecting Interrupt Request Destinations

The available destinations are fixed for each interrupt, as described in Table 13.3, Table 13.4.

The interrupt output destination, CPU, DMAC, or DTC can be independently selected for each interrupt source.

Use an interrupt request destination setting that is indicated by a "✓" in the event list (see section 13.3.2. Event Number).

Note: Setting the same interrupt source for IELSRn and DELSRn is prohibited.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin, you must set the IRQCRi.IRQMD[1:0] bits for that interrupt to select edge detection.

13.5.4.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Set the IELSRn.IELS[8:0] bits to the target event and set the IELSRn.DTCE bit to 0.

13.5.4.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. Use the following procedure:

1. Set the IELSRn.IELS[8:0] bits to the target event and set the IELSRn.DTCE bit to 1.
2. Set the DTC Module Start bit (DTCST.DTCST) to 1.

Table 13.5 shows operation when the DTC is the interrupt request destination.

Table 13.5 Operation when DTC becomes interrupt request destination

Interrupt request destination	DISEL*1	Remaining transfer operations	Operation per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU(IELSRn.DTCE bit is cleared)
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer data	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	CPU(IELSRn.DTCE bit is cleared)

Note 1. DTC.MRB.DISEL bit controles the interrupt generates timing from DTC to CPU.

禁用中断请求的过程如下：

1.禁用事件源的操作设置，例如DMAC激活（DELSRn.DELS[8:0]）、贪睡模式取消（SELSR0.SELS[8:0]）、软件待机模式取消（WUPEN寄存器设置）。

2.清除中断源设置（IELSRn.IELS[8:0]=0x00）。

3.清除中断状态标志（IELSRn.IR=0）。

4.清除中断清除启用寄存器（NVIC_ICER）和中断清除挂起寄存器（NVIC_ICPR）。

13.5.3 轮询中断

轮询中断请求的过程如下：

1.设置中断清除启用寄存器(NVIC_ICER)。

2.将IELSRn.IELS[8:0]位设置为中断源。

3.指定事件源的操作设置，例如DMAC激活（DELSRn.DELS[8:0]）、贪睡模式取消（SELSR0.SELS[8:0]）、软件待机模式取消（WUPEN寄存器设置）。

4.轮询中断设置挂起寄存器(NVIC_ISPR)。

13.5.4 选择中断请求目标

每个中断的可用目的地都是固定的，如表13.3和表13.4中所述。

可以为每个中断源独立选择中断输出目标、CPU、DMAC或DTC。

使用事件列表中由"✓"指示的中断请求目标设置（参见第13.3.2节。事件编号）。

Note: 禁止为IELSRn和DELSRn设置相同的中断源。

如果选择DMAC或DTC作为来自IRQi引脚的请求的目标，则必须设置IRQCRi.IRQMD[1:0]位以使该中断选择边沿检测。

13.5.4.1 CPU中断请求

当IELSRn.DTCE=0时，将IELSRn寄存器中指定的事件输出到NVIC。将IELSRn.IELS[8:0]位设置为目标事件，并将IELSRn.DTCE位设置为0。

13.5.4.2 DTC activation

当IELSRn.DTCE=1时，将IELSRn寄存器中指定的事件输出到DTC。使用以下过程：

1.将IELSRn.IELS[8:0]位设置为目标事件，并将IELSRn.DTCE位设置为1。

2.将DTC模块起始位(DTCST.DTCST)设置为1。

表13.5显示了DTC是中断请求目标时的操作。

Table 13.5 DTC成为中断请求目标时的操作

中断请求目的地	DISEL*1	剩余的转移操作	按请求操作	IR*2	传输后的中断请求目的地
DTC*3	1	≠ 0	DTC传输→CPU中断	CPU接受中断时清零	DTC
		= 0	DTC传输→CPU中断	CPU接受中断时清零	CPU（IELSRn.DTCE位清零）
	0	≠ 0	DTC transfer	读取DTC传输数据后，在DTC数据传输开始时清零	DTC
		= 0	DTC传输→CPU中断	CPU接受中断时清零	CPU（IELSRn.DTCE位清零）

注1.DTC.MRB.DISEL位控制从DTC到CPU的中断产生时序。

Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.
Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. The DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 17.2 in section 17, Data Transfer Controller (DTC).

Note: Error during DTC transfer

If an error response occurs during DTC transfer, the DTC notifies the ICU that an error has occurred. ICU clears all bits of the target IELSRn (n = 0 to 95). IELSRn that is not the target is not cleared.

Note: DTC transfer error in snooze mode

When an error occurs in DTC transfer in Snooze mode, ICU issues a Wake Up request. However, interrupt requests are not issued automatically. See section 17, Data Transfer Controller (DTC) chapter for information on how to set the interrupt when a DTC error occurs.

13.5.4.3 DMAC Activation

Events specified in the DELSRn registers are output to the DMAC.

To set the interrupt source for DMAC, use the following procedure:

1. Set the DELSRn.DELS[8:0] bits to the event to activate the DMAC.
2. When using interrupts to CPU, set the IELSRn.IELS bit to factor of DMAC interrupt and IELSRn.DTCE bit to 0.
3. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
4. Set the DMAC transfer enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.
5. Set the DMAC operation enable bit (DMAST.DMST) to 1.

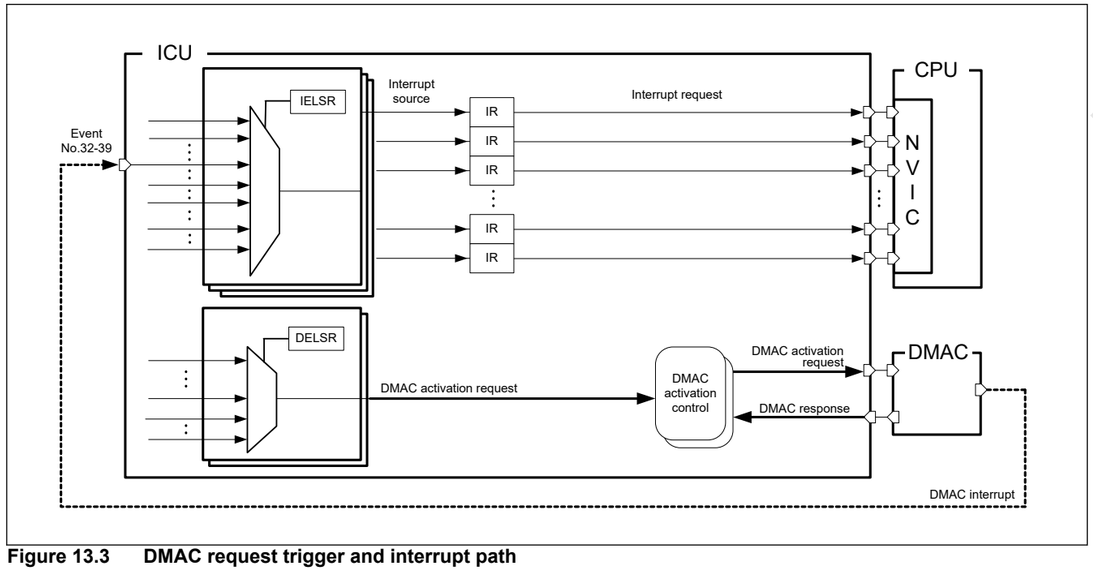

Figure 13.3 DMAC request trigger and interrupt path

Note: Error during DMAC transfer

If an error response occurs during DMAC transfer, the DMAC notifies the ICU that an error has occurred.

The ICU clears all bits of the target channel of DELSRn (n = 0 to 7). DELSRn that is not the target channel is not cleared.

注2.IELSRn.IR标志为1时，忽略再次发生的中断请求（DTC激活请求）。
注3.对于链式传输，DTC传输将持续到最后一个链式传输结束。DISEL位状态和剩余传输计数决定是否发生CPU中断、IELSRn.IR标志清除时序以及传输后的中断请求目的地。请参见第17节“数据传输控制器(DTC)”中的表17.2。

Note: DTC传输期间出错

如果在DTC传输期间发生错误响应，则DTC会通知ICU发生了错误。ICU清除目标IELSRn(n=0到95)的所有位。不是目标的IELSRn不会被清除。

Note: 贪睡模式下的DTC传输错误

当贪睡模式下的DTC传输发生错误时，ICU会发出唤醒请求。但是，不会自动发出中断请求。有关如何在发生DTC错误时设置中断的信息，请参见第17节，数据传输控制器(DTC)章节。

13.5.4.3 DMAC Activation

在DELSRn寄存器中指定的事件被输出到DMAC。

要为DMAC设置中断源，请使用以下过程：

1.将DELSRn.DELS[8:0]位设置为事件以激活DMAC。

2.当对CPU使用中断时，将IELSRn.IELS位设置为DMAC中断因素，并将IELSRn.DTCE位设置为0。

3.将目标DMAC通道（DMACm.DMTMD.DCTG[1:0]）的激活源设置为01b（中断模块检测）。

4.将目标DMAC通道(DMACm.DMCNT.DTE)的DMAC传输使能位设置为1。

5.将DMAC操作使能位(DMAST.DMST)设置为1。

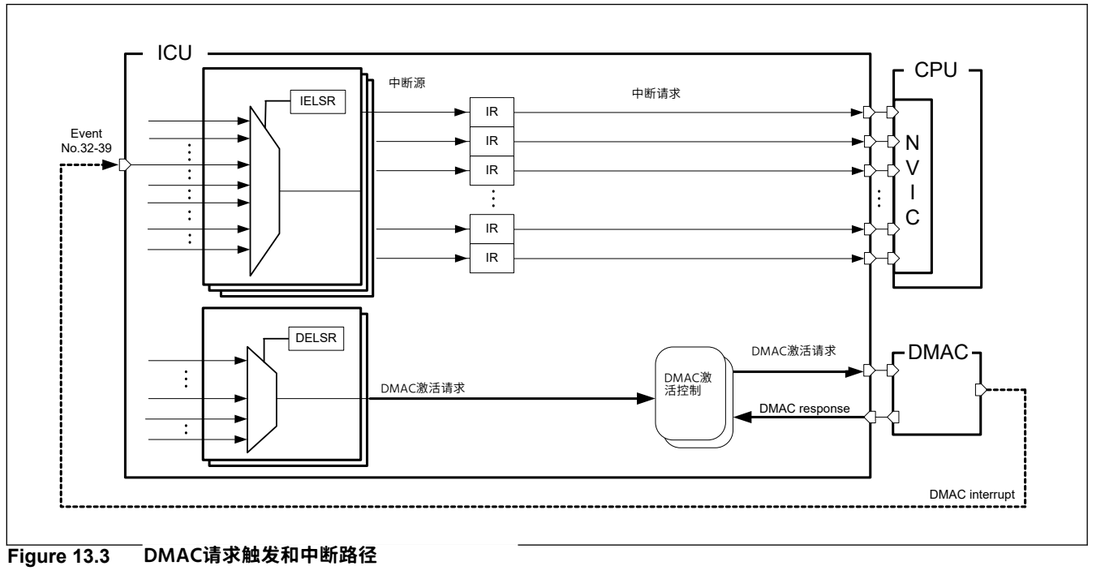

Figure 13.3 DMAC请求触发和中断路径

Note: DMAC传输期间出错

如果在DMAC传输期间发生错误响应，则DMAC会通知ICU发生了错误。

ICU清除DELSRn（n=0到7）的目标通道的所有位。不是目标通道的DELSRn不会被清除。

13.5.5 Digital Filter

A digital filter function is provided for the external interrupt request pins IRQi, (i = 0 to 15) and the NMI pin interrupt. It samples input signals on the filter PCLKB sampling clock, and removes any signal with a pulse width less than 3 sampling cycles.

To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits (i = 0 to 15).
2. Set the IRQCRi.FLTEN bit (i = 0 to 15) to 1 (digital filter enabled).

To use the digital filter for an NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 13.4 shows an example of digital filter operation.

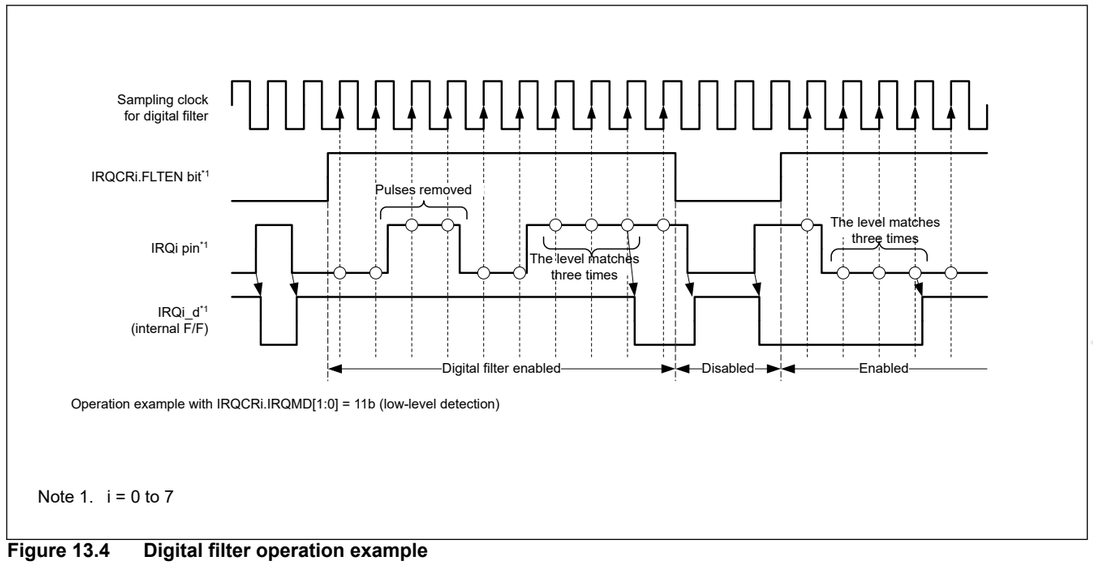

Figure 13.4 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The ICU clock stops in Software Standby mode.

On exiting Software Standby, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby, an incorrect edge might be detected. You can enable the digital filters again after exiting Software Standby mode.

13.5.6 External Pin Interrupts

To use external pin interrupts:

1. Configure I/O ports settings
2. Clear the IRQCRi.FLTEN bit (i = 0 to 15) to 0 (digital filter disabled).
3. Set the IRQMD[1:0] bits of the given IRQCRi register (i = 0 to 15) to select the senses of detection.
4. Set the FCLKSEL[1:0] bits, and the FLTEN bit of the IRQCRi register.
5. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS[8:0] bits and the IELSRn.DTCE bit to 0

13.5.5 数字滤波器

为外部中断请求引脚IRQi（i=0到15）和NMI引脚中断提供了数字过滤功能。它在滤波器PCLKB采样时钟上对输入信号进行采样，并去除脉冲宽度小于3个采样周期的任何信号。

为IRQi引脚使用数字滤波器：

1.在IRQCRi.FCLKSEL[1:0]位（i=0到15）中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。

2.将IRQCRi.FLTEN位（i=0到15）设置为1（启用数字滤波器）。

要将数字滤波器用于NMI引脚：

1.在NMICR.NFCLKSEL[1:0]位中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。

2.将NMICR.NFLTEN位设置为1（启用数字滤波器）。

图13.4显示了数字滤波器操作的示例。

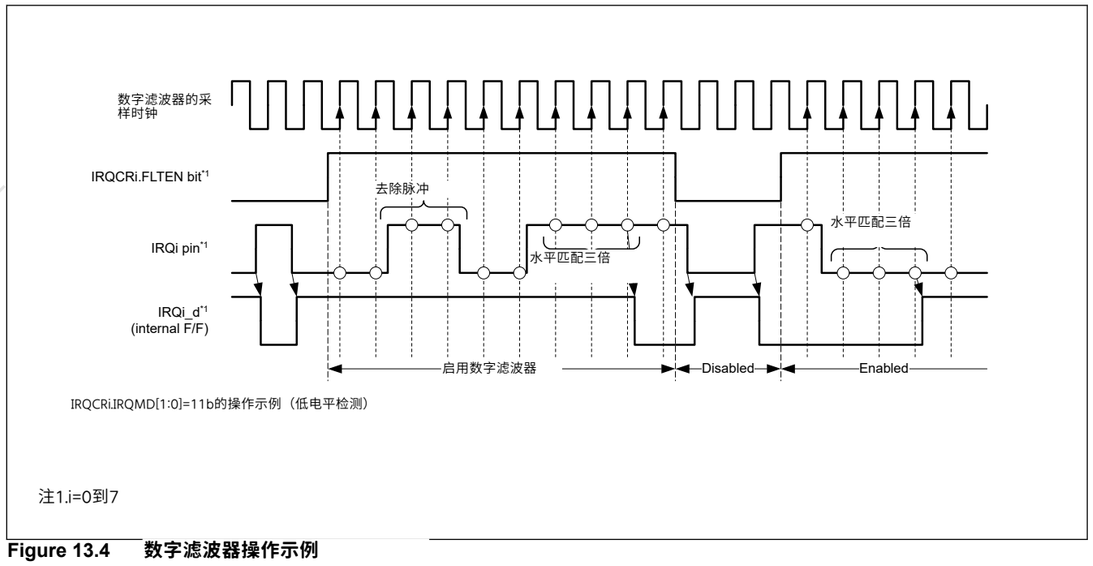

Figure 13.4 数字滤波器操作示例

在进入软件待机模式之前，通过清除IRQCRi.FLTEN和NMICR.NFLTEN位来禁用数字滤波器。ICU时钟在软件待机模式下停止。

在退出软件待机时，电路通过将待机前的状态与待机释放后的状态进行比较来检测边沿。如果在软件待机期间输入发生变化，则可能会检测到不正确的边沿。您可以在退出软件待机模式后再次启用数字滤波器。

13.5.6 外部引脚中断

要使用外部引脚中断：

1.配置IO端口设置

2.将IRQCRi.FLTEN位（i=0到15）清零（禁用数字滤波器）。

3.设置给定IRQCRi寄存器（i=0到15）的IRQMD[1:0]位以选择检测的意义。

4.设置FCLKSEL[1:0]位和IRQCRi寄存器的FLTEN位。

5.选择IRQ引脚如下：

- 如果IRQ引脚用于CPU中断请求，请将IELSRn.IELS[8:0]位和IELSRn.DTCE位设置为0

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- If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS[8:0] bits and the IELSRn.DTCE bit to 1.
- If the IRQ pin is to be used for DMAC activation, set the DELSRn.DELS[8:0] bits.

13.6 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- SRAM ECC error interrupt
- MPU bus master error interrupt
- TrustZone filter error interrupt
- Cache RAM parity error interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC or DMAC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts:

1. Clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. Set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register.
3. Write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI interrupt cannot be disabled when enabled, except by a reset.

The secure attribution managed within the Application Interrupt and Reset Control Register (AIRCR) of the Arm CPU must match the security attribution of NMI.

The NMI secure of the CPU is changed by AIRCR.BFHFNMINS. It is managed by software developers who manage Secure program.

13.6.1 Correspondence to TrustZone-M by NMI

Although there is only one NMI per CPU, multiple factors can be set. This section describes the procedure for mixing Secure and NonSecure programs of NMI. When doing so, the NMI-related registers of the ICU are set to Secure.

NMI-related registers:

- NMIER
- NMICLR
- NMICR

Set "0" to ICUSARB.SANMI.

The value of AIRCR.BFHFNMINS[13] in the Application Interrupt and Reset Control Register of the ARM CPU must be the same as the value of security attribution. The initial values of AIRCR.BFHFNMINS and ICUSARB.SANMI are different.

●如果IRQ引脚用于DTC激活，请将IELSRn.IELS[8:0]位和IELSRn.DTCE位设置为1。
●如果IRQ引脚用于激活DMAC，设置DELSRn.DELS[8:0]位。

13.6 不可屏蔽中断操作

以下源可以触发不可屏蔽中断：

●NMI引脚中断
●振荡停止检测中断
●WDT下溢刷新错误中断
●IWDT下溢刷新错误中断
●电压监控器1中断
●电压监测器2中断
●SRAM奇偶校验错误中断
●SRAMECC错误中断
●MPU总线主机错误中断
●TrustZone过滤器错误中断
●CacheRAM奇偶校验错误中断。

不可屏蔽中断只能用于CPU，不能激活DTC或DMAC。不可屏蔽中断优先于所有其他中断。不可屏蔽中断状态可以在不可屏蔽中断状态寄存器(NMISR)中验证。在从NMI处理程序返回之前，确认NMISR中的所有位都为0。

默认情况下禁用不可屏蔽中断。要使用不可屏蔽的中断：

1.将NMICR.NFLTEN位清为0（禁用数字滤波器）。
2.设置NMICR寄存器的NMIMD位、NFCLKSEL[1:0]位和NFLTEN位。
3.将1写入NMICLR.NMICLR位以将NMISR.NMIST标志清零。
4.通过将1写入不可屏蔽中断使能寄存器(NMIER)中的相关位来启用不可屏蔽中断。

将1写入NMIER寄存器后，随后对NMIER中的NMIEN位的写访问将被忽略。启用时不能禁用NMI中断，除非通过复位。

在ArmCPU的应用程序中断和复位控制寄存器(AIRCR)中管理的安全属性必须与NMI的安全属性相匹配。

CPU的NMI安全由AIRCR.BFHFNMINS更改。它由管理的软件开发人员管理
安全程序。

13.6.1 NMI与TrustZone-M的通信

虽然每个CPU只有一个NMI，但可以设置多个因素。本节介绍混合程序
NMI的安全和非安全程序。这样做时，ICU的NMI相关寄存器设置为Secure。

NMI-related registers:

- NMIER
- NMICLR
- NMICR

将"0"设置为ICUSARB.SANMI。

ARMCPU的应用中断和复位控制寄存器AIRCR.BFHFNMINS[13]的值必须与安全属性的值相同。AIRCR.BFHFNMINS和ICUSARB.SANMI的初始值不同。

AIRCR.BFHFNMINS is for secure and ICUSARB.SANMI is for non-secure. Polarity has the same meaning so program these to match.

If NMI is issued, jump to the NMI handler. When mixing secure and non-secure program, the NMI handler must branch according to the TrustZone-M rule. Figure 13.5 shows the flow.

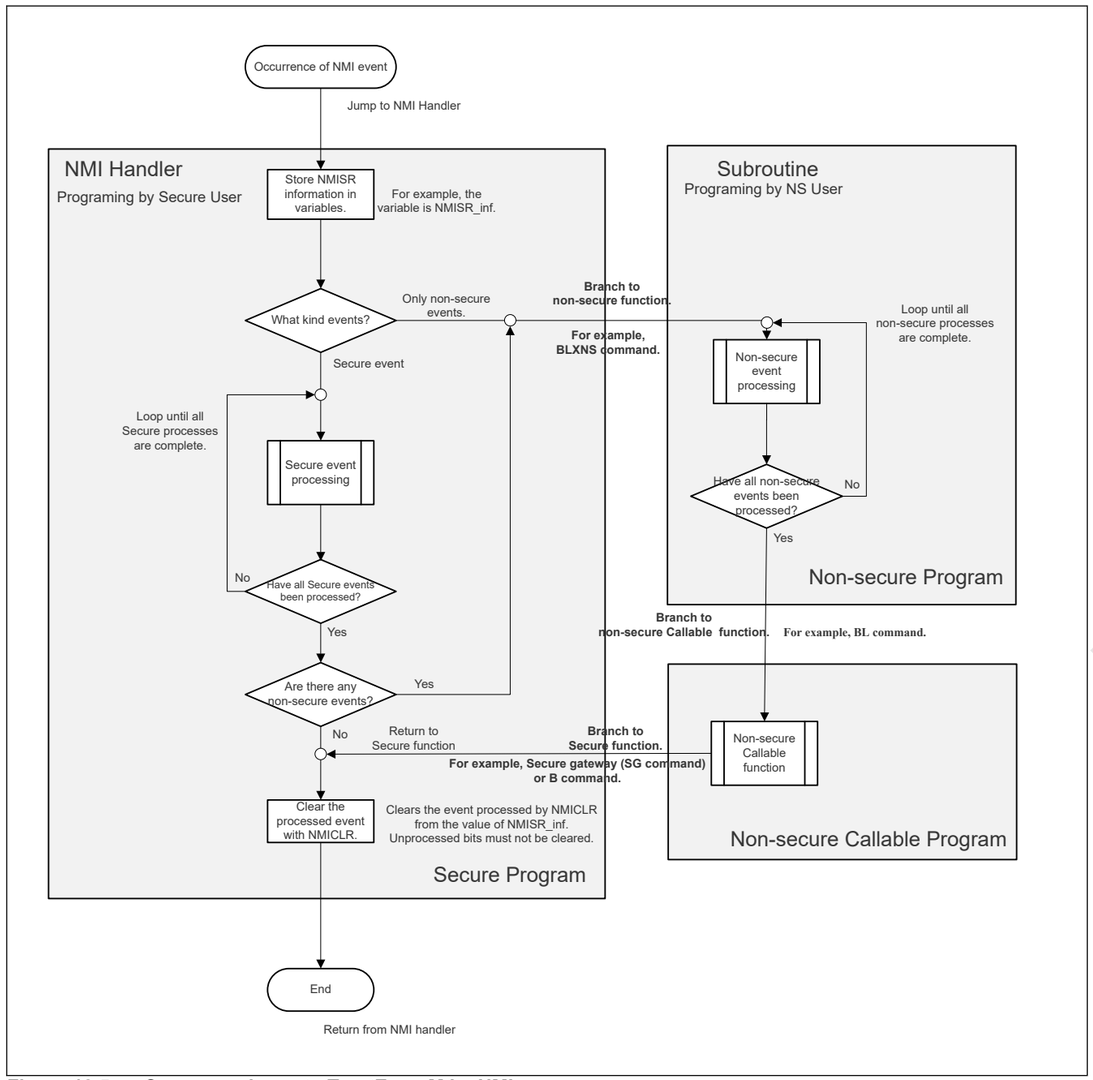

Figure 13.5 Correspondence to TrustZone-M by NMI

See the Arm documentation for details on how to move between secure and non-secure programs.

13.7 Return from Low Power Modes

Table 13.4 lists the interrupt sources you can use to exit Sleep, Snooze, or Software Standby mode. For more information, see section 10, Low Power Modes.

13.7.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

AIRCR.BFHFNMINS用于安全，ICURASB.SANMI用于非安全。极性具有相同的含义，因此请对它们进行编程以匹配。

如果发出NMI，则跳转到NMI处理程序。当混合安全和非安全程序时，NMI处理程序必须根据TrustZone-M规则进行分支。图13.5显示了流程。

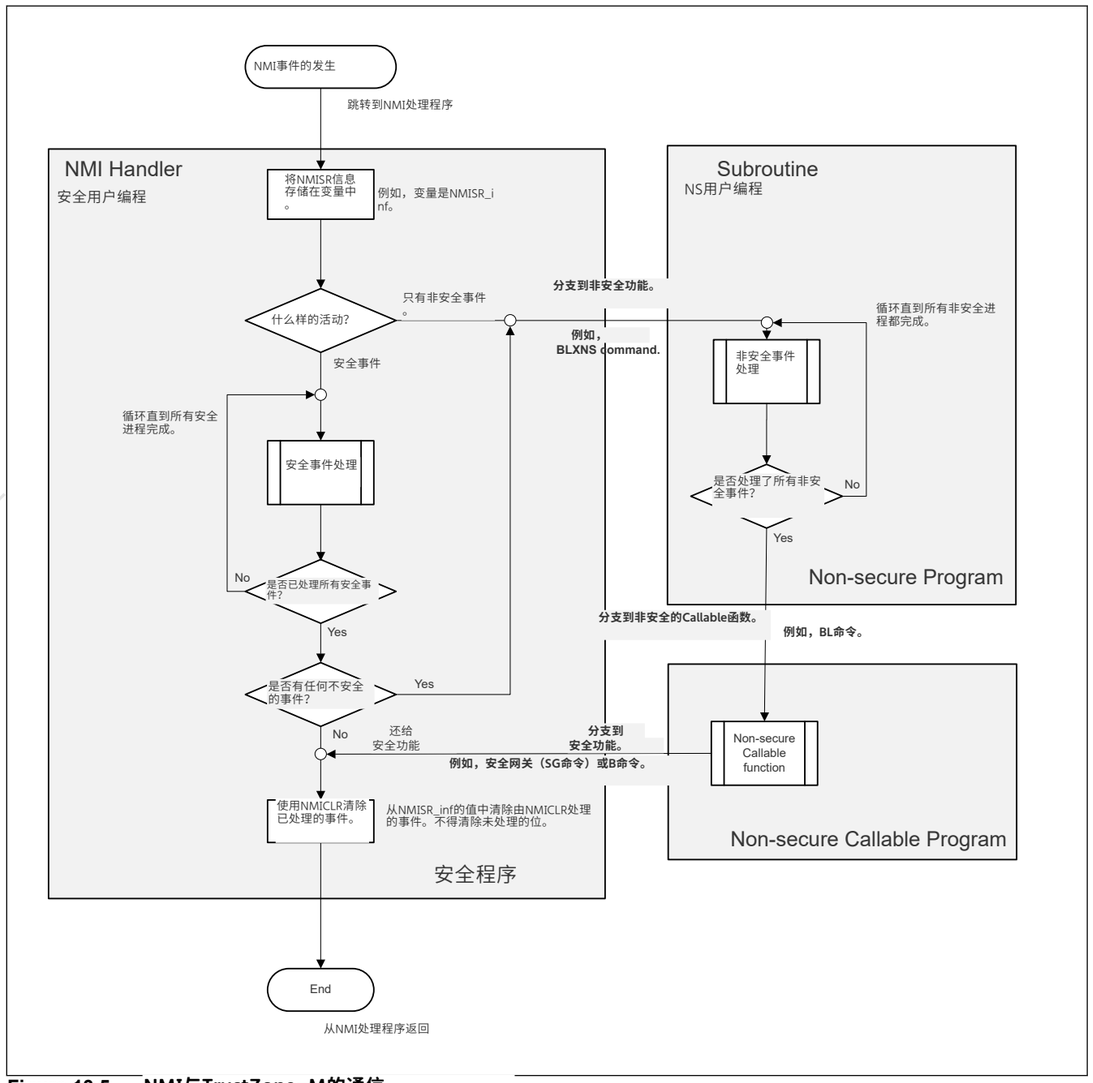

Figure 13.5 NMI与TrustZone-M的通信

有关如何在安全程序和非安全程序之间移动的详细信息，请参阅Arm文档。

13.7 从低功耗模式返回

表13.4列出了可用于退出睡眠、贪睡或软件待机模式的中断源。有关详细信息，请参阅第10节，低功耗模式。

13.7.1 从睡眠模式返回

从睡眠模式返回以响应中断：

non-maskable interrupt

- Use the NMIER register to enable the target interrupt request.

maskable interrupt

- Select the CPU as the interrupt request destination.
- Enable the interrupt in the NVIC.

13.7.2 Return from Software Standby Mode

The ICU returns from Software Standby mode using a non-maskable interrupt or a maskable interrupt. For maskable interrupt of canceling source, see Table 13.4.

To return from Software Standby mode:

1. Select the interrupt source that enables return from Software Standby:
   - For non-maskable interrupts, use the NMIER register to enable the target interrupt request
   - For maskable interrupts, use the WUPEN register to enable the target interrupt request.
2. Select the CPU as the interrupt request destination
3. Enable the interrupt in the NVIC.

Interrupt requests through the IRQn pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

Similarly, request for a non-maskable interrupt from a request source whose clock is stopped in Software Standby mode cannot be detected.

Transition to/from Software Standby mode

1. Before Software Standby mode is entered, disable the digital filter for the interrupt source as a return target (IRQCRi.FLTEN = 0, NMICR.NFLTEN = 0).
2. To use the digital filter again after returning from Software Standby mode, enable the digital filter (IRQCRi.FLTEN = 1, NMICR.NFLTEN = 1).

13.7.3 Return from Snooze Mode

The ICU can return to Normal mode from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Set the number of the required interrupt request in SELSR0.SELS[8:0]
2. Set the value 0x02D (ICU_SNZCANCEL) in IELSRn.IELS[8:0] (n = 0 to 95).
3. Select the CPU as the interrupt request destination.
4. Enable the interrupt in the NVIC.

Interrupt requests through the non-maskable that do not satisfy the above conditions are not detected while the clock is stopped in snooze mode.

Note: In Snooze mode, a clock is supplied to the ICU. If an event selected in IELSRn is detected, the CPU acknowledges the interrupt after returning to Normal mode from Software Standby mode. If an event selected in DELSRn is detected, the DMAC can acknowledge the interrupt after returning to Normal mode from Software Standby mode.

13.8 Using the WFI Instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

13.9 Reference

- ARM Limited., ARM® Cortex®-M33 Processor Technical Reference Manual (ARM 100230)

non-maskable interrupt

●使用NMIER寄存器启用目标中断请求。

maskable interrupt

●选择CPU作为中断请求目标。

●在NVIC中启用中断。

13.7.2 从软件待机模式返回

ICU使用不可屏蔽中断或可屏蔽中断从软件待机模式返回。取消源的可屏蔽中断见表13.4。

从软件待机模式返回：

1.选择允许从软件待机返回的中断源：

●对于不可屏蔽的中断，使用NMIER寄存器使能目标中断请求

●对于可屏蔽中断，使用WUPEN寄存器启用目标中断请求。

2.选择CPU作为中断请求目的地

3.在NVIC中启用中断。

不满足这些条件的通过IRQn引脚的中断请求在时钟停止时不会被检测到软件待机模式。

同样，无法检测到来自时钟在软件待机模式下停止的请求源的不可屏蔽中断请求。

从软件待机模式转换

1.在进入软件待机模式之前，禁用作为返回目标的中断源的数字滤波器（IRQCRi.FLTEN=0，NMICR.NFLTEN=0）。

2.要在从软件待机模式返回后再次使用数字滤波器，请启用数字滤波器（IRQCRi.FLTEN=1，NMICR.NFLTEN=1）。

13.7.3 从贪睡模式返回

ICU可以使用为该模式提供的中断从贪睡模式返回到正常模式。

要从贪睡模式返回正常模式：

1.在SELSR0.SELS[8:0]中设置所需中断请求的数量

2.在IELSRn.IELS[8:0]（n=0到95）中设置值0x02D(ICU_SNZCANCEL)。

3.选择CPU作为中断请求目标。

4.在NVIC中启用中断。

当时钟在贪睡模式下停止时，不会检测到通过不可屏蔽的不满足上述条件的中断请求。

Note: 在贪睡模式下，向ICU提供时钟。如果检测到在IELSRn中选择的事件，CPU在从软件待机模式返回到正常模式后确认中断。如果检测到在DELSRn中选择的事件，则DMAC可以在从软件待机模式返回正常模式后确认中断。

13.8 将WFI指令与不可屏蔽中断一起使用

每当执行WFI指令时，请确认NMISR寄存器中的所有状态标志为0。

13.9 Reference

●ARMLimited. ARM®Cortex®-M33处理器技术参考手册(ARM100230)

14. Buses

14.1 Overview

The buses consists of 32 bits AHB bus matrix. Table 14.1 lists the bus masters and bus slaves and Figure 14.1 shows the bus configuration.

Table 14.1 Bus Specifications

Classification	Bus Master/Slave name	Bus I/F Max Freq	Sync Clock	Specifications
Bus Masters	Code bus (Cortex-M33)	200 MHz	ICLK	Connected to the CPU Instruction Cache for instructions and operands
	System bus (Cortex-M33)	200 MHz	ICLK	Connected to the CPU Data Cache for system
	DMAC / DTC	200 MHz	ICLK	Connected to the DMAC/DTC
	EDMAC (Ether)	100 MHz	PCLKA	Connected to the EDMAC
Bus Slaves	FHBIU	200 MHz	ICLK	Connected to Code Flash memory and Configuration area
	FLBIU	50 MHz	FCLK	Connected to Data Flash memory, FACI
	S0BIU	200 MHz	ICLK	Connected to SRAM0 (Standby RAM)
	PSBIU	200 MHz	ICLK	Connected to peripheral system modules (DTC, DMAC, ICU, Flash, MPU, CSC, SRAM, Debug/Trace module, System controller and BUS controller)
	PLBIU	50 MHz	PCLKB	Connected to peripheral modules (CAC, ELC, I/O ports, POEG, RTC, WDT, IWDT, AGT, IIC, CANFD, USBFS, USBHS, CEC, SDHI, SSIE, TSN, and CTSU)
	PHBIU	100 MHz	PCLKA	Connected to peripheral modules (GPT, ETHERC, EDMAC, SCI, SPI, CRC, DOC, ADC12, DAC12 and SCE9)
	EQBIU (QSPI area)	100 MHz	PCLKA	Connected to the QSPI (External Memory Interface)
	EOBIU (OSPI area)	100 MHz	PCLKA	Connected to the OSPI (External Memory Interface)
	ECBIU (CS area)	100 MHz	BCLK	Connected to the external devices (External Memory Interface)

Note: BCLK (external-bus clock): 100MHz (max.) (The CSC (CS area controller) operate in synchronization with the BCLK)
BCLK pin output: The frequency is the same as the default of BCLK. 1/2 BCLK can be supplied by setting the EBCLK pin output select bit (BCKCR.BCLKDIV) in the external bus clock control register. For details, see section 8, Clock Generation Circuit.
FHBIU: Flash High speed Bus Interface Unit.
FLBIU: Flash Low speed Bus Interface Unit.
S0BIU: SRAM0 Bus Interface Unit.
PSBIU: Peripheral System Bus Interface Unit.
PLBIU: Peripheral Low speed Bus Interface Unit.
PHBIU: Peripheral High speed Bus Interface Unit.
EQBIU: External memory interface Qspi Bus Interface Unit.
EOBIU: External memory interface Ospi Bus Interface Unit.
ECBIU: External memory interface Csc Bus Interface Unit.

14. Buses

14.1 Overview

总线由32位AHB总线矩阵组成。表14.1列出了总线主机和总线从机，图14.1显示了总线配置。

Table 14.1 总线规格

Classification	总线主从名称	Bus I/F 最大频率	同步时钟	Specifications
巴士大师	代码总线(Cortex-M33)	200 MHz	ICLK	连接到CPU指令缓存以获取指令和操作数
	系统总线(Cortex-M33)	200 MHz	ICLK	连接到系统的CPU数据缓存
	DMAC / DTC	200 MHz	ICLK	连接到DMACDTC
	EDMAC (Ether)	100 MHz	PCLKA	连接到EDMAC
总线从站	FHBIU	200 MHz	ICLK	连接到代码闪存和配置区
	FLBIU	50 MHz	FCLK	连接到数据闪存，FACI
	S0BIU	200 MHz	ICLK	连接到SRAM0（备用RAM）
	PSBIU	200 MHz	ICLK	连接到外围系统模块（DTC、DMAC、ICU、Flash、MPU、CSC、SRAM、调试跟踪模块、系统控制器和总线控制器）
	PLBIU	50 MHz	PCLKB	连接到外围模块（CAC、ELC、IO端口、POEG、RTC, WDT, IWDT, AGT, IIC, CANFD, USBFS, USBHS, CEC, SDHI, SSIE, TSN, and CTSU)
	PHBIU	100 MHz	PCLKA	连接外围模块（GPT、ETHERC、EDMAC、SCI、SPI、CRC、DOC、ADC12、DAC12和SCE9）
	EQBIU (QSPI area)	100 MHz	PCLKA	连接到QSPI（外部存储器接口）
	EOBIU (OSPI area)	100 MHz	PCLKA	连接到OSPI（外部存储器接口）
	ECBIU (CS area)	100 MHz	BCLK	连接到外部设备（外部存储器接口）

Note: BCLK（外部总线时钟）：100MHz（最大值）（CSC（CS区域控制器）与BCLK同步运行）
BCLK引脚输出：频率与BCLK的默认值相同。12BCLK可以通过设置外部总线时钟控制寄存器中的EBCLK引脚输出选择位(BCKCR.BCLKDIV)来提供。有关详细信息，请参见第8节，时钟生成电路。FHBIU：闪存高速总线接口单元。FLBIU：闪存低速总线接口单元。

S0BIU：SRAM0总线接口单元。
PSBIU：外围系统总线接口单元。
PLBIU：外围低速总线接口单元。PHBIU：外围高速总线接口单元。
EQBIU：外部存储器接口Qspi总线接口单元。EOBIU：外部存储器接口OspiBusInterfaceUnit。ECBIU：外部存储器接口Csc总线接口单元。

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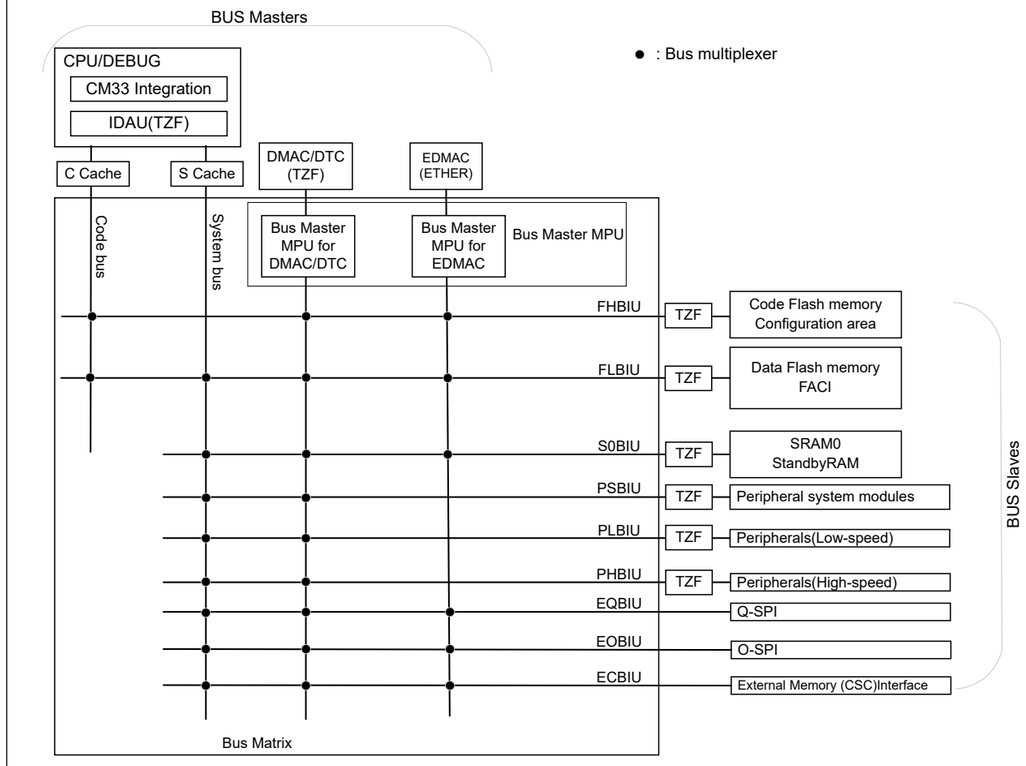


Note: TZF is TrustZone Filter. C cache is instruction cache. S cache is data cache.
For FLBIU, the code bus accesses the data flash memory and configuration areas (code region) through FLBIU. The system bus accesses FACI and SCDS (peripheral region) through FLBIU.

Figure 14.1 Bus Connection

14.2 Description of Buses

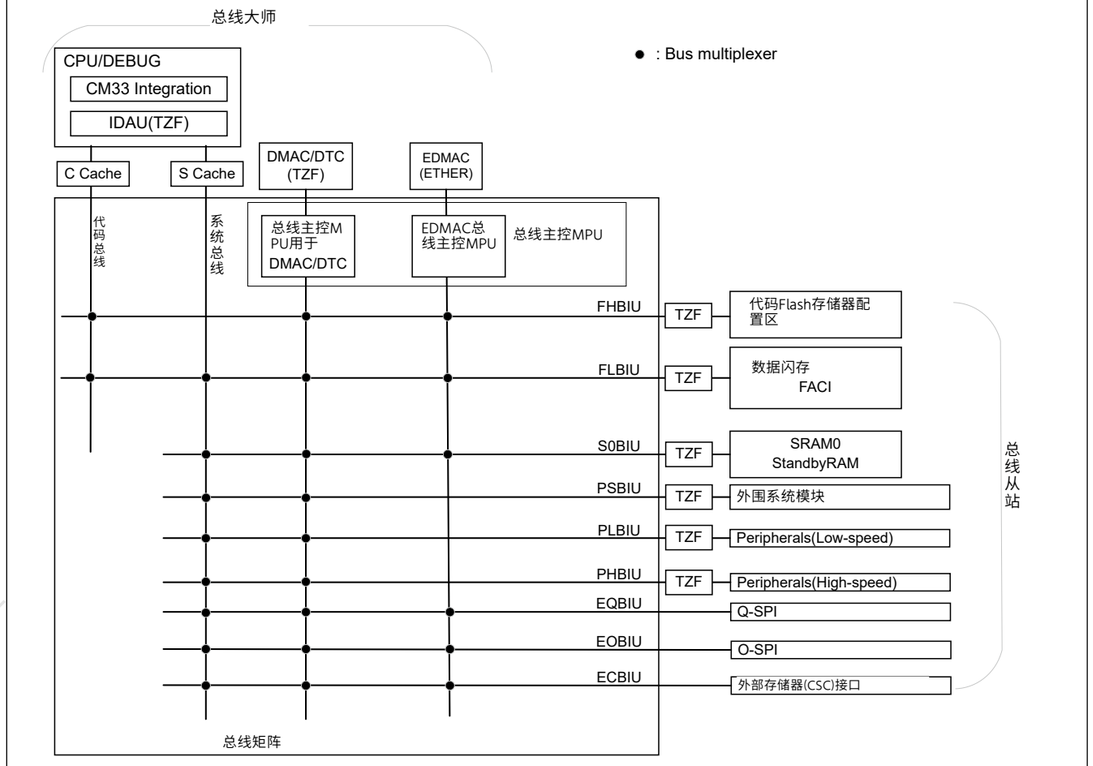
14.2.1 Arbitration

For arbitration between masters in each slave, fixed-priority and round-robin methods can be selected for each master. For details, see section 14.3.9. BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU, EQBIU, EOBIU, ECBIU), section 14.3.10. BUSSCNT<slave> : Slave Bus Control Register (<slave> = PSBIU, PLBIU, PHBIU).

14.2.2 External Bus

Table 14.2 lists the specifications of the external bus. The external bus controller arbitrates requests for bus mastership on the external address space and external bus controller registers (CSC) from Code bus, System bus, DMAC/DTC and EDMAC. The priority order can be set using the external bus priority control bits (BUSSCNTECBIU.ARBS3).

The bus system has external space for QSPI and OSPI. For details, see section 35, Quad Serial Peripheral Interface (QSPI) and section 36, Octa Serial Peripheral Interface (OSPI) for the specifications.



Note: TZF是TrustZone过滤器。C缓存是指令缓存。S缓存是数据缓存。
对于FLBIU，代码总线通过FLBIU访问数据闪存和配置区域（代码区域）。系统总线通过FLBIU访问FACI和SCDS（外围区域）。

Figure 14.1 巴士连接

14.2 巴士的描述

14.2.1 Arbitration

对于每个从属设备中的主设备之间的仲裁，可以为每个主设备选择固定优先级和循环方法。详见14.3.9节。BUSSCNT<slave>:从总线控制寄存器(<slave>=FHBIU FLBIU S0BIU EQBIU EOBIU ECBIU)，第14.3.10节。BUSSCNT<slave>:从总线控制寄存器(<slave>=PSBIU PLBIU PHBIU)。

14.2.2 外部总线

表14.2列出了外部总线的规格。外部总线控制器对来自代码总线、系统总线、DMACDTC和EDMAC的外部地址空间和外部总线控制器寄存器(CSC)上的总线控制请求进行仲裁。可以使用外部总线优先级控制位(BUSSCTECBIU.ARBS3)设置优先级顺序。

总线系统为QSPI和OSPI提供了外部空间。有关详细信息，请参阅第35节，四路串行外设接口(QSPI)和第36节，八路串行外设接口(OSPI)以了解规格。

Table 14.2 Specifications of the External Bus (External Memory Interface)

Parameter	Description
External address space	• The external address space is divided into 8 CS areas (CS0 to CS7). • Chip select signals can be output for each area. • The bus width can be set for each area: – Separate bus: Selectable to 8-bit or 16-bit bus space – Address/data multiplexed bus: Selectable to 8-bit or 16-bit bus space • Endian mode can be specified for each area.
CS area controller	• Recovery cycles can be inserted. – Read recovery: Up to 15 cycles – Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (for page access, up to 7 cycles) • Use wait control to set up the following: – Assertion and negation timing of chip select signals (CS0# to CS7#) – Assertion timing of the read signal (RD#) and write signals (WR0#/WR# and WR1# to WR3#) – Timing of data output starts and ends. • Write access modes: – Single-write strobe mode and byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
Write buffer function	When write data from the bus master is written to the write buffer, write access by the bus master is complete.
Frequency	The CS area controller (CSC) operates in synchronization with the external bus clock (BCLK).
TrustZone Filter	Security attribution is always non-secure

Table 14.3 lists the input/output pins of the external bus (External Memory Interface).

Table 14.3 Pin Configuration of the External Bus (External Memory Interface)

Pin Name	I/O	Description
A23 to A0*1	Output	Address output pins
D15 to D0	I/O	Data input/output pins D15 to D0 pins are enabled when the 16-bit bus space is specified. D7 to D0 pins are enabled when the 8-bit bus space is specified.
BC0#*1	Output	A strobe signal; (the BC0# signal being at the low level) during access to an external address space in single write strobe mode indicates that D7 to D0 are valid. When an 8-bit bus space is specified, this output pin is always held low regardless of write access mode.
BC1#	Output	A strobe signal; (the BC1# signal being at the low level) during access to an external address space in single write strobe mode indicates that D15 to D8 are valid. This pin is not used when the 8-bit bus space is specified.
CS0#	Output	A chip select signal for area 0 (CS0)
CS1#	Output	A chip select signal for area 1 (CS1)
CS2#	Output	A chip select signal for area 2 (CS2)
CS3#	Output	A chip select signal for area 3 (CS3)
CS4#	Output	A chip select signal for area 4 (CS4)
CS5#	Output	A chip select signal for area 5 (CS5)
CS6#	Output	A chip select signal for area 6 (CS6)
CS7#	Output	A chip select signal for area 7 (CS7)
RD#	Output	A strobe signal indicating that reading from an external address space (CS0 to CS7) is in progress
WR0#/WR#*2	Output	WR0# signal is a strobe signal indicates that (the WR0# signal being at the low level) writing to an external address space is in progress in byte strobe mode, and D7 to D0 are valid. WR# signal is a strobe signal that indicates writing to an external address space is in progress in single write strobe mode. When an 8-bit bus space is specified, this output pin is held low during a write access regardless of write access mode.
WR1#	Output	A strobe signal; (the WR1# signal being at the low level) during writing to an external address space in byte strobe mode indicates that D15 to D8 are valid. This signal is invalid in single write strobe mode. This pin is not used when the 8-bit bus space is specified.
ALE	Output	Address latch signal when address/data multiplexed bus is selected.
WAIT#	Input	A wait request signal when accessing the external address space (CS0 to CS7) (Low: Wait request)

Table 14.2 外部总线（外部存储器接口）的规格

Parameter	Description
外部地址空间	• 外部地址空间分为8个CS区域（CS0到CS7）。 • 可以为每个区域输出芯片选择信号。 • 可为每个区域设置总线宽度： – 独立总线：可选择8位或16位总线空间 – 地址数据复用总线：可选择8位或16位总线空间 • 可以为每个区域指定Endian模式。
CS区域控制器	• 可以插入恢复周期。 – 读取恢复：最多15个周期 – 写恢复：最多15个周期 • 循环等待功能：最多等待31个周期（对于页面访问，最多7个周期） • 使用等待控制来设置以下内容： – 片选信号（CS0#到CS7#）的断言和否定时序 – 读取信号(RD#)和写入信号(WR0#WR#和WR1#到WR3#)的断言时序 – 数据输出的时序开始和结束。 • 写访问模式： – 单写选通模式和字节选通模式 • 可以为每个区域设置单独的总线或地址数据复用总线。
写缓冲功能	当来自总线主控的写数据被写入写缓冲区时，总线主控的写访问就完成了。
Frequency	CS区域控制器(CSC)与外部总线时钟(BCLK)同步运行。
TrustZone Filter	安全归因始终是不安全的

表14.3列出了外部总线（外部存储器接口）的输入输出引脚。

Table 14.3 外部总线的引脚配置（外部存储器接口）

引脚名称	I/O	Description
A23 to A0*1	Output	地址输出引脚
D15 to D0	I/O	当指定16位总线空间时，数据输入输出引脚D15到D0引脚被启用。当指定8位总线空间时，D7到D0引脚被启用。
BC0#*1	Output	一个频闪信号；（BC0#信号为低电平）在单写选通模式下访问外部地址空间时，表明D7到D0有效。当指定8位总线空间时，无论写访问模式如何，该输出引脚始终保持低电平。
BC1#	Output	一个频闪信号；（BC1#信号为低电平）在单写选通模式下访问外部地址空间时，表明D15～D8有效。当指定8位总线空间时，不使用该引脚。
CS0#	Output	区域0(CS0)的片选信号
CS1#	Output	区域1(CS1)的片选信号
CS2#	Output	区域2(CS2)的片选信号
CS3#	Output	区域3(CS3)的片选信号
CS4#	Output	区域4(CS4)的片选信号
CS5#	Output	区域5(CS5)的片选信号
CS6#	Output	区域6(CS6)的片选信号
CS7#	Output	区域7(CS7)的片选信号
RD#	Output	指示正在从外部地址空间（CS0到CS7）读取的选通信号
WR0#/WR#*2	Output	WR0#信号为选通信号，表示（WR0#信号为低电平）字节选通模式下正在写入外部地址空间，D7～D0有效。WR#信号是一个选通信号，表示在单写选通模式下正在写入外部地址空间。当指定8位总线空间时，无论写访问模式如何，该输出引脚在写访问期间都保持低电平。
WR1#	Output	一个频闪信号；在字节选通模式下写入外部地址空间期间（WR1#信号为低电平）表示D15到D8有效。该信号在单写选通模式下无效。当指定8位总线空间时，不使用该引脚。
ALE	Output	选择地址数据复用总线时的地址锁存信号。
WAIT#	Input	访问外部地址空间（CS0至CS7）时的等待请求信号（低：等待请求）

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Note 1. The A0 and BC0# pin functions share the same pin, and either become effective according to the area, with the function being A0 in byte strobe mode and BC0# in single write strobe mode. Setting the 8-bit external bus width is prohibited in single write strobe mode. For information on other multiplexed pin functions, see section 19, I/O Ports.
Note 2. The WR0# signal and WR# signal are identical. The WR0# signal is particularly referred to as WR# in single write strobe mode.

14.2.3 Parallel Operation

Parallel operation is possible when different bus-master modules are requesting access to different slave modules. For example, if the CPU is fetching an instruction from Code Flash and an operand from SRAM0, the DMAC can handle transfer between a peripheral module and the external memory interface at the same time.

Figure 14.2 shows an example of parallel operations. In this example, the CPU uses code bus and system bus for simultaneous access to FHBIU and S0BIU, respectively. Furthermore, the DMAC/DTC or EDMAC simultaneously accesses the peripheral bus or the external bus during access to FHBIU and S0BIU by the CPU.

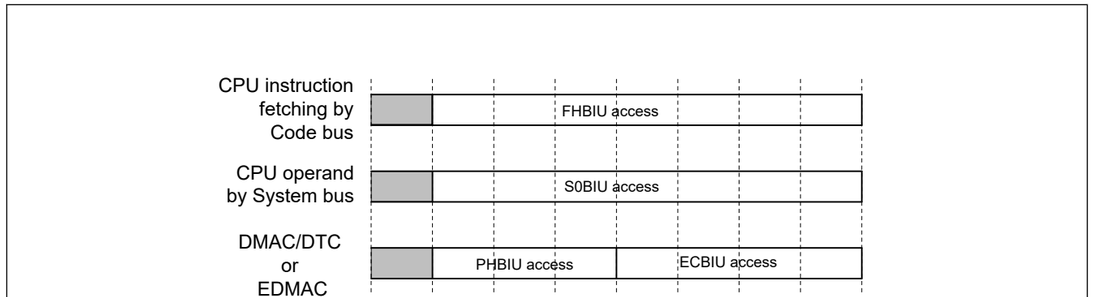

Figure 14.2 Example of Parallel Operations

14.2.4 Bus Settings

- Set the mode of the external bus in the CSn mode register (CSnMOD), CSn wait-control register 1 (CSnWCR1), CSn wait-control register 2 (CSnWCR2), CSn control register (CSnCR), CSn recovery-cycle setting register (CSnREC), CS recovery cycle insertion enable register (CSRECEN), and bus priority control register (BUSSCNT).
- I/O port assignments: PmnPFS.PMR = 1 and PmnPFS.PSEL[4:0] = 0x0B
- Frequency of the external bus clock (BCLK):SCKDIVCR register.

See section 19, I/O Ports for information on pin settings, and section 8, Clock Generation Circuit for information on SCKDIVCR.

14.2.5 Restrictions

(1) Restriction on Endian

Memory space must be little-endian in order to execute Cortex code.

(2) Bufferable write access

When CPU or DMAC perform Bufferable Write access to PLBIU or PHBIU, if an STZF error occurs then the error response is invalidated. So there is no error flag will be set and no NMI / RESET request is generated.

When CPU or DMAC perform Bufferable Write access to PHBIU or EOBIU, if a Slave BUS error occurs then the error response will become invalid and the error flag will not be set.

If error response is required, set the bus master to non-bufferable access.

(3) Access to reserved area of FLBIU and S0BIU

Access to the reserved area of FLBIU and S0BIU is prohibited. Operation is not guaranteed if accessed.

注1.A0和BC0#引脚功能共用同一个引脚，根据区域分别生效，功能为A0字节选通模式和BC0#单写选通模式。在单写选通模式下，禁止设置8位外部总线宽度。有关其他多路复用引脚功能的信息，请参见第19节，IO端口。

注2.WR0#信号和WR#信号相同。WR0#信号在单写选通模式下特别称为WR#。

14.2.3 并联运行

当不同的总线主模块请求访问不同的从模块时，并行操作是可能的。例如，如果CPU从CodeFlash中获取指令并从SRAM0中获取操作数，则DMAC可以同时处理外设模块和外部存储器接口之间的传输。

图14.2显示了并行操作的示例。在本例中，CPU使用代码总线和系统总线分别同时访问FHBIU和S0BIU。此外，在CPU访问FHBIU和S0BIU期间，DMACDTC或EDMAC同时访问外围总线或外部总线。

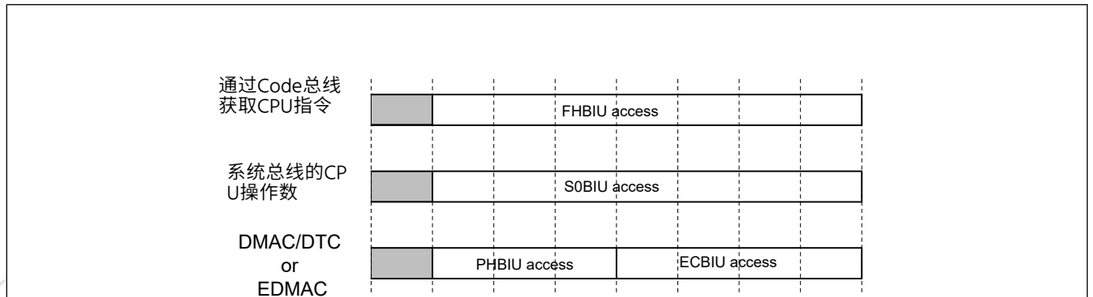

Figure 14.2 并行操作示例

14.2.4 总线设置

●在CSn模式寄存器（CSnMOD）、CSn等待控制寄存器1（CSnWCR1）、CSn等待控制寄存器2（CSnWCR2）、CSn控制寄存器（CSnCR）、CSn恢复周期设置寄存器中设置外部总线的模式(CSnREC)、CS恢复周期插入使能寄存器(CSRECEN)和总线优先级控制寄存器(BUSSCNT)。

●IO端口分配：PmnPFS.PMR=1和PmnPFS.PSEL[4:0]=0x0B

●外部总线时钟（BCLK）的频率：SCKDIVCR寄存器。

有关引脚设置的信息，请参见第19节，IO端口，有关引脚设置的信息，请参见第8节，时钟生成电路。
SCKDIVCR.

14.2.5 Restrictions

(1) 对字节序的限制

为了执行Cortex代码，内存空间必须是little-endian。

(2) 可缓冲的写访问

当CPU或DMAC对PLBIU或PHBIU执行可缓冲写访问时，如果发生STZF错误，则错误响应无效。因此不会设置错误标志，也不会生成NMIRESET请求。

当CPU或DMAC对PHBIU或EOBIU执行BufferableWrite访问时，如果发生SlaveBUS错误，则错误响应将变为无效并且不会设置错误标志。

如果需要错误响应，请将总线主机设置为非缓冲访问。

(3) 访问FLBIU和S0BIU的保留区

禁止访问FLBIU和S0BIU的保留区域。如果访问，则无法保证操作。

(4) Clock setting

The clock division ratio prohibits setting changes during bus access.

14.3 Register Descriptions

14.3.1 BUSSARA : BUS Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSA0	BUS Security Attribution A0 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

BUSSA0 bit (BUS Security Attribution A0)

The correspondence between register and BIU name is as follows

Connection (BUSSCNT<slave> = FHBIU/FLBIU/S0BIU/PSBIU/PLBIU/PHBIU/EQBIU/EOBIU/ECBIU)

Please see to Figure 14.1 for connection between BIU and BUS

- BUSSCNTFHBIU
- BUSSCNTFLBIU
- BUSSCNTS0BIU
- BUSSCNTPSBIU
- BUSSCNTPLBIU
- BUSSCNTPHBIU
- BUSSCNTEQBIU
- BUSSCNTEOBIU
- BUSSCNTECBIU

(4) 时钟设置

时钟分频比禁止在总线访问期间更改设置。

14.3 注册说明

14.3.1 BUSSARA:BUS安全属性寄存器A

Base address: CPSCU = 0x4000_8000

Offset address: 0x0100

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSA0	BUS安全属性A0 0: Secure 1: Non-Secure	R/W
31:1	—	这些位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

BUSSA0位（BUS安全属性A0）

寄存器和BIU名称的对应关系如下

Connection (BUSSCNT<slave> = FHBIU/FLBIU/S0BIU/PSBIU/PLBIU/PHBIU/EQBIU/EOBIU/ECBIU)

BIU和BUS的连接见图14.1

- BUSSCNTFHBIU
- BUSSCNTFLBIU
- BUSSCNTS0BIU
- BUSSCNTPSBIU
- BUSSCNTPLBIU
- BUSSCNTPHBIU
- BUSSCNTEQBIU
- BUSSCNTEOBIU
- BUSSCNTECBIU

14.3.2 BUSSARB : BUS Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSB0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSB0	BUS Security Attribution B0 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

BUSSB0 bit (BUS Security Attribution B0)

The BUSSB0 bit specifies the security attributes of registers for Bus Error Clear registers and DMAC/DTC Error Clear register.

BUS1ERRCLR: Code bus

BUS2ERRCLR: System bus

BUS3ERRCLR: DMAC/DTC

BUS4ERRCLR: EDMAC

DMACDTCERRCLR: DMAC/DTC (Master-TZF)

See Figure 14.1 for connection of each BUS.

14.3.3 CSnCR : CSn Control Register (n = 0 to 7)

Base address: BUS = 0x4000_3000

Offset address: 0x0802 + 0x10 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EXENB	Operation Enable 0: Operation is disabled. 1: Operation is enabled.	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
5:4	BSIZE[1:0]	External Bus Width Select 0 0: A 16-bit bus space is selected. 1 0: An 8-bit bus space is selected. Others: Setting prohibited	R/W

14.3.2 BUSSARB:BUS安全属性寄存器B

Base address: CPSCU = 0x4000_8000

Offset address: 0x0104

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BUSSB0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	BUSSB0	BUS安全属性B0 0: Secure 1: Non-Secure	R/W
31:1	—	这些位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

BUSSB0位（BUS安全属性B0）

BUSSB0位指定总线错误清除寄存器和DMACDTC错误清除寄存器的安全属性。

BUS1ERRCLR：代码总线

BUS2ERRCLR：系统总线

BUS3ERRCLR: DMAC/DTC

BUS4ERRCLR: EDMAC

DMACDTCERRCLR: DMAC/DTC (Master-TZF)

每个BUS的连接请参见图14.1。

14.3.3 CSnCR:CSn控制寄存器(n=0to7)

Base address: BUS = 0x4000_3000

Offset address: 0x0802 + 0x10 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EXENB	操作启用 0：禁止操作。1：使能操作。	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
5:4	BSIZE[1:0]	外部总线宽度选择 00：选择16位总线空间。10：选择8位总线空间。 其他：禁止设置	R/W

Bit	Symbol	Function	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	EMODE	Endian Mode 0: Little-endian 1: Big-endian	R/W
11:9	—	These bits are read as 0. The write value should be 0.	R/W
12	MPXEN	Address/Data Multiplexed I/O Interface Select 0: Separate bus interface is selected for area n. 1: Address/data multiplexed I/O interface is selected for area n.	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

Do not attempt to write the CSnCR register while the external bus is being accessed.

EXENB bit (Operation Enable)

This bit enables or disables operation of the respective CS areas. After the MCU is reset, operation is enabled (EXENB = 1) only for area 0. Operation in other areas is disabled (EXENB = 0). An attempt access to an area for which operation is disabled does not lead to access through the external bus.

BSIZE[1:0] bits (External Bus Width Select)

These bits specify the data bus width of each area. The data bus width of area 0 (CS0) after a reset depends on the setting of the bus width in operating mode. When the address/data multiplexed I/O interface is selected with the MPXEN bit, the BSIZE[1:0] bits should not be set to the 32-bit bus space. If set, the operation cannot be guaranteed.

EMODE bit (Endian Mode)

This bit specifies the endian of each area. As core endian is fixed little, When the endian setting for each area is different from that for the MCU, no instruction code can be allocated in the area. The instruction code should be allocated to the external space of little-endian setting.

MPXEN bit (Address/Data Multiplexed I/O Interface Select)

This bit specifies separate bus interface or address/data multiplexed I/O interface of each area.

14.3.4 CSnREC : CSn Recovery Cycle Register (n = 0 to 7)

Base address: BUS = 0x4000_3000

Offset address: 0x080A + 0x10 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	WRCV[3:0]				—	—	—	—	RRCV[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	RRCV[3:0]	Read Recovery 0x0: No recovery cycle is inserted. Others: RRCV[3:0] clock cycles are inserted for read recovery.	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
11:8	WRCV[3:0]	Write Recovery 0x0: No recovery cycle is inserted. Others: WRCV[3:0] clock cycles are inserted for write recovery.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

Do not attempt to write the CSnREC register while the external bus is being accessed.

When the preceding bus access is a separate bus access, CSnREC is valid when the recovery cycle insertion is enabled with the separate bus recovery cycle insertion enable bit (RCVENj (j = 0 to 7)) in CSRECEN.

Bit	Symbol	Function	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
8	EMODE	Endian Mode 0: Little-endian 1: Big-endian	R/W
11:9	—	这些位被读取为0。写入值应为0。	R/W
12	MPXEN	地址数据复用IO接口选择 0：为n区选择单独的总线接口。1：n区选择地址数据复用IO接口 。	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W

在访问外部总线时不要尝试写CSnCR寄存器。

EXENB bit (Operation Enable)

该位启用或禁用相应CS区域的操作。MCU复位后，仅对区域0启用操作(EXENB=1)。禁用其他区域的操作(EXENB=0)。尝试访问禁用操作的区域不会导致通过外部总线进行访问。

BSIZE[1:0]位（外部总线宽度选择）

这些位指定每个区域的数据总线宽度。复位后区域0(CS0)的数据总线宽度取决于操作模式下总线宽度的设置。当使用MPXEN位选择地址数据复用IO接口时，不应将BSIZE[1:0]位设置为32位总线空间。如果设置，则无法保证操作。

EMODE bit (Endian Mode)

该位指定每个区域的字节序。由于核心字节序固定很少，当每个区域的字节序设置与单片机不同时，该区域不能分配指令代码。指令代码应分配到little-endian设置的外部空间。

MPXEN位（地址数据复用IO接口选择）

该位指定每个区域的单独总线接口或地址数据复用IO接口。

14.3.4 CSnREC:CSn恢复周期寄存器(n=0to7)

Base address: BUS = 0x4000_3000

Offset address: 0x080A + 0x10 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	WRCV[3:0]				—	—	—	—	RRCV[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	RRCV[3:0]	读取恢复 0x0：不插入恢复周期。 其他：插入RRCV[3:0]时钟周期用于读取恢复。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
11:8	WRCV[3:0]	写恢复 0x0：不插入恢复周期。 其他：为写恢复插入WRCV[3:0]时钟周期。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W

在访问外部总线时不要尝试写CSnREC寄存器。

当前面的总线访问是单独的总线访问时，当使用CSRECEN中的单独总线恢复周期插入使能位(RCVENj(j=0至7))使能恢复周期插入时，CSnREC有效。

When the preceding bus access is an address/data multiplexed bus access, CSnREC is valid when the recovery cycle insertion is enabled with the multiplexed bus recovery cycle insertion enable bit (RCVENMj) in CSRECEN.

RRCV[3:0] bits (Read Recovery)

These bits specify the number of recovery cycles to be inserted after a read access to the external bus for CSn (n = 0 to 7).When the recovery cycle insertion is enabled and a value except 0000b is written to these bits, 1 to 15 recovery cycles are inserted in the following conditions:

- After a read access to the external bus, a read access is made to the external bus in the same area.
- After a read access to the external bus, a read access is made to the external bus in a different area.
- After a read access to the external bus, a write access is made to the external bus in the same area.
- After a read access to the external bus, a write access is made to the external bus in a different area.

WRCV[3:0] bits (Write Recovery)

These bits specify the number of recovery cycles to be inserted after a write access to the external bus for CSn (n = 0 to 7).When the recovery cycle insertion is enabled and a value except 0000b is written to these bits, one to 15 recovery cycles are inserted in the following cases.

- After a write access to the external bus, a read access is made to the external bus in the same area.
- After a write access to the external bus, a read access is made to the external bus in a different area.
- After a write access to the external bus, a write access is made to the external bus in the same area.
- After a write access to the external bus, a write access is made to the external bus in a different area.

14.3.5 CSRECEN : CS Recovery Cycle Insertion Enable Register

Base address: BUS = 0x4000_3000

Offset address: 0x0880

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RCVENM7	RCVENM6	RCVENM5	RCVENM4	RCVENM3	RCVENM2	RCVENM1	RCVENM0	RCVEN7	RCVEN6	RCVEN5	RCVEN4	RCVEN3	RCVEN2	RCVEN1	RCVEN0
Value after reset:	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	RCVEN0	Separate Bus Recovery Cycle Insertion Enable 0 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
1	RCVEN1	Separate Bus Recovery Cycle Insertion Enable 1 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
2	RCVEN2	Separate Bus Recovery Cycle Insertion Enable 2 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
3	RCVEN3	Separate Bus Recovery Cycle Insertion Enable 3 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
4	RCVEN4	Separate Bus Recovery Cycle Insertion Enable 4 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
5	RCVEN5	Separate Bus Recovery Cycle Insertion Enable 5 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
6	RCVEN6	Separate Bus Recovery Cycle Insertion Enable 6 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W

当前面的总线访问是地址数据复用总线访问时，CSnREC在通过CSRECEN中的复用总线恢复周期插入使能位(RCVENMj)使能恢复周期插入时有效。

RRCV[3:0] bits (Read Recovery)

这些位指定对CSn的外部总线进行读访问后插入的恢复周期数（n=0到7）。当启用恢复周期插入并将0000b以外的值写入这些位时，1到15在以下情况下插入恢复周期：

●对外部总线进行读访问后，对同一区域的外部总线进行读访问。
●对外部总线进行读访问后，对不同区域的外部总线进行读访问。
●对外部总线进行读访问后，对同一区域的外部总线进行写访问。
●对外部总线进行读访问后，对不同区域的外部总线进行写访问。

WRCV[3:0] bits (Write Recovery)

这些位指定对CSn的外部总线进行写访问后插入的恢复周期数（n=0到7）。当启用恢复周期插入并将0000b以外的值写入这些位时，1到15在以下情况下插入恢复周期。

●对外部总线进行写访问后，对同一区域的外部总线进行读访问。
●对外部总线进行写访问后，对不同区域的外部总线进行读访问。
●对外部总线进行写访问后，对同一区域的外部总线进行写访问。
●对外部总线进行写访问后，对不同区域的外部总线进行写访问。

14.3.5 CSRECEN:CS恢复周期插入使能寄存器

Base address: BUS = 0x4000_3000

Offset address: 0x0880

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RCVENM7	RCVENM6	RCVENM5	RCVENM4	RCVENM3	RCVENM2	RCVENM1	RCVENM0	RCVEN7	RCVEN6	RCVEN5	RCVEN4	RCVEN3	RCVEN2	RCVEN1	RCVEN0
重置后的值：	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	RCVEN0	单独的总线恢复周期插入使能0 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
1	RCVEN1	单独的总线恢复周期插入启用1 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
2	RCVEN2	单独的总线恢复周期插入启用2 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
3	RCVEN3	单独的总线恢复周期插入启用3 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
4	RCVEN4	单独的总线恢复周期插入启用4 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
5	RCVEN5	单独的总线恢复周期插入启用5 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
6	RCVEN6	单独的总线恢复周期插入使能6 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W

Bit	Symbol	Function	R/W
7	RCVEN7	Separate Bus Recovery Cycle Insertion Enable 7 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
8	RCVENM0	Multiplexed Bus Recovery Cycle Insertion Enable 0 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
9	RCVENM1	Multiplexed Bus Recovery Cycle Insertion Enable 1 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
10	RCVENM2	Multiplexed Bus Recovery Cycle Insertion Enable 2 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
11	RCVENM3	Multiplexed Bus Recovery Cycle Insertion Enable 3 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
12	RCVENM4	Multiplexed Bus Recovery Cycle Insertion Enable 4 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
13	RCVENM5	Multiplexed Bus Recovery Cycle Insertion Enable 5 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
14	RCVENM6	Multiplexed Bus Recovery Cycle Insertion Enable 6 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W
15	RCVENM7	Multiplexed Bus Recovery Cycle Insertion Enable 7 0: Recovery cycle insertion is disabled. 1: Recovery cycle insertion is enabled.	R/W

Do not attempt to write the CSRECEN register while the external bus is being accessed. For detail of insertion of recovery cycles, see section 14.5.4. Insertion of Recovery Cycles.

RCVENn bit (Separate Bus Recovery Cycle Insertion Enable n (n = 0 to 7)

This bit enables or disables the insertion of read or write recovery cycles when, after a read or write access to the external bus, a read or write access is made to the external bus in the same area.

RCVENMn bit (Multiplexed Bus Recovery Cycle Insertion Enable n (n = 0 to 7)

This bit enables or disables the insertion of read or write recovery cycles when, after a read or write access to the external bus, a read or write access is made to the external bus in the same area.

Table 14.4 Access type associations with the RCVENn bits (1 of 2)

Access Type	External Address Space	Insertion of Recovery Cycles	Corresponding Bits (Separate/ Multiplexed)
Read access after read access	Same area	Recovery cycles specified by the RRCV[3:0] bits of precedence access area are inserted.	RCVEN0/RCVENM0
	Different area	Recovery cycles specified by the RRCV[3:0] bits of precedence access area are inserted.	RCVEN1/RCVENM1
Write access after read access	Same area	Recovery cycles specified by the RRCV[3:0] bits of precedence access area are inserted.	RCVEN2/RCVENM2
	Different area	Recovery cycles specified by the RRCV[3:0] bits of precedence access area are inserted.	RCVEN3/RCVENM3

Bit	Symbol	Function	R/W
7	RCVEN7	单独的总线恢复周期插入启用7 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
8	RCVENM0	多路复用总线恢复周期插入使能0 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
9	RCVENM1	多路复用总线恢复周期插入使能1 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
10	RCVENM2	多路复用总线恢复周期插入使能2 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
11	RCVENM3	多路复用总线恢复周期插入使能3 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
12	RCVENM4	多路复用总线恢复周期插入使能4 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
13	RCVENM5	多路复用总线恢复周期插入使能5 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
14	RCVENM6	多路复用总线恢复周期插入使能6 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W
15	RCVENM7	多路复用总线恢复周期插入启用7 0：禁用恢复周期插入。1：启用恢复周期插入。	R/W

在访问外部总线时不要尝试写CSRECEN寄存器。有关恢复循环插入的详细信息，请参阅第14.5.4节。插入恢复周期。

RCVENn位（单独的总线恢复周期插入使能n（n=0至7）

当对外部总线进行读或写访问后，对同一区域的外部总线进行读或写访问时，该位启用或禁用读或写恢复周期的插入。

RCVENMn位（多路复用总线恢复周期插入使能n（n=0至7）

当对外部总线进行读或写访问后，对同一区域的外部总线进行读或写访问时，该位启用或禁用读或写恢复周期的插入。

Table 14.4 访问类型与RCVENn位的关联（1of2）

访问类型	External 地址空间	恢复周期的插入	对应位（单独 Multiplexed)
读访问后读访问	同一地区	由指定的恢复周期 插入优先访问区域的RRCV[3:0]位。	RCVEN0/RCVENM0
	不同区域	由指定的恢复周期 插入优先访问区域的RRCV[3:0]位。	RCVEN1/RCVENM1
读访问后写访问	同一地区	由指定的恢复周期 插入优先访问区域的RRCV[3:0]位。	RCVEN2/RCVENM2
	不同区域	由指定的恢复周期 插入优先访问区域的RRCV[3:0]位。	RCVEN3/RCVENM3

Table 14.4 Access type associations with the RCVENn bits (2 of 2)

Access Type	External Address Space	Insertion of Recovery Cycles	Corresponding Bits (Separate/ Multiplexed)
Read access after write access	Same area	Recovery cycles specified by the WRCV[3:0] bits of precedence access area are inserted.	RCVEN4/RCVENM4
	Different area	Recovery cycles specified by the WRCV[3:0] bits of precedence access area are inserted.	RCVEN5/RCVENM5
Write access after write access	Same area	Recovery cycles specified by the WRCV[3:0] bits of precedence access area are inserted.	RCVEN6/RCVENM6
	Different area	Recovery cycles specified by the WRCV[3:0] bits of precedence access area are inserted.	RCVEN7/RCVENM7

14.3.6 CSnMOD : CSn Mode Register (n = 0 to 7)

Base address: BUS = 0x4000_3000

Offset address: 0x0002 + 0x10 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRMOD	—	—	—	—	—	PWENB	PRENB	—	—	—	—	EWENB	—	—	WRMOD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WRMOD	Write Access Mode Select 0: Byte strobe mode 1: Single write strobe mode	R/W
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	EWENB	External Wait Enable 0: External wait is disabled. 1: External wait is enabled.	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	PRENB	Page Read Access Enable 0: Page read access is disabled. 1: Page read access is enabled.	R/W
9	PWENB	Page Write Access Enable 0: Page write access is disabled. 1: Page write access is enabled.	R/W
14:10	—	These bits are read as 0. The write value should be 0.	R/W
15	PRMOD	Page Read Access Mode Select 0: Normal access compatible mode 1: External data read continuous assertion mode	R/W

Note: Do not write to the CSnMOD register while access to the CSn area is in progress.

WRMOD bit (Write Access Mode Select)

This bit selects a write access operating mode.

Writing 0 to this bit selects byte strobe mode where data write operation is controlled by the WRn (n = 0 to 1) signal corresponding to the respective byte positions.

Writing 1 to this bit selects single write strobe mode where data write operation is controlled by the BCn (n = 0 to 1) signal and the WR signal corresponding to respective byte positions. Setting the external bus width of 8 bits is prohibited in single write strobe mode.

Table 14.4 与RCVENn位的访问类型关联（2个中的2个）

访问类型	External 地址空间	恢复周期的插入	对应位（单独 Multiplexed）
写访问后读访问	同一地区	由指定的恢复周期 插入优先访问区域的WRCV[3:0]位。	RCVEN4/RCVENM4
	不同区域	由指定的恢复周期 插入优先访问区域的WRCV[3:0]位。	RCVEN5/RCVENM5
写访问后的写访问	同一地区	由指定的恢复周期 插入优先访问区域的WRCV[3:0]位。	RCVEN6/RCVENM6
	不同区域	由指定的恢复周期 插入优先访问区域的WRCV[3:0]位。	RCVEN7/RCVENM7

14.3.6 CSnMOD:CSn模式寄存器(n=0到7)

Base address: BUS = 0x4000_3000

Offset address: 0x0002 + 0x10 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRMOD	—	—	—	—	—	PWENB	PRENB	—	—	—	—	EWENB	—	—	WRMOD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WRMOD	写访问模式选择 0：字节选通模式1：单写选 通模式	R/W
2:1	—	这些位被读取为0。写入值应为0。	R/W
3	EWENB	外部等待启用 0：禁用外部等待。1：启用 外部等待。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	PRENB	页面读取访问启用 0：禁用页面读取访问。1：启用 页面读取访问。	R/W
9	PWENB	页面写访问启用 0：禁用页面写访问。1：启用页 面写访问。	R/W
14:10	—	这些位被读取为0。写入值应为0。	R/W
15	PRMOD	页面读取访问模式选择 0：正常访问兼容模式1：外部数据读取连续断言 模式	R/W

Note: 在访问CSn区域的过程中不要写入CSnMOD寄存器。

WRMOD位（写访问模式选择）

该位选择写访问操作模式。

向该位写入0选择字节选通模式，其中数据写入操作由对应于各个字节位置的WRn（n=0到1）信号控制。

向该位写入1选择单次写入选通模式，其中数据写入操作由BCn(n=0到1)信号和对应于各个字节位置的WR信号控制。在单写选通模式下，禁止设置8位外部总线宽度。

Table 14.5 Control Signals for Write Access Mode

Mode	Pin Name			
Write Access Mode	**WR1#**	**WR0#/WR#**	**BC1#**	**BC0#**
Byte strobe mode	✓	✓ (WR0#)	—	—
Single write strobe mode	—	✓ (WR#)	✓	✓

Note: ✓: Enabled, —: Disabled

EWENB bit (External Wait Enable)

This bit enables or disables external wait.

Writing 1 to this bit selects external wait and allows control of the number of waits in each cycle with the WAIT# signal. In this state, wait cycles are inserted while the WAIT# signal is at the low level. Writing 0 to this bit disables the WAIT# signal.

PRENB bit (Page Read Access Enable)

This bit enables or disables page read accesses.

Note: When the address/data multiplexed I/O interface is selected with the MPXEN bit in CSnCR, this bit should not be set to enable page read accesses. Page read accesses are not supported in the address/data multiplexed I/O interface.

PWENB bit (Page Write Access Enable)

This bit enables or disables page write accesses.

Note: When the address/data multiplexed I/O interface is selected with the MPXEN bit in CSnCR, this bit should not be set to enable page write accesses. Page write accesses are not supported in the address/data multiplexed I/O interface.

PRMOD bit (Page Read Access Mode Select)

This bit selects a page read access operating mode.

Writing 0 to this bit selects normal access compatible mode where the RD# signal is negated and RD# assert wait is inserted each time data is read. However, when there is no RD# assert wait, the RD# signal is negated only in the final transfer of the external bus access.

Writing 1 to this bit selects external data read continuous assertion mode where RD# assert wait is inserted and the RD# signal is continuously asserted during this time period.

14.3.7 CSnWCR1 : CSn Wait Control Register 1 (n = 0 to 7)

Base address: BUS = 0x4000_3000

Offset address: 0x0004 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CSRWAIT[4:0]					—	—	—	CSWWAIT[4:0]				
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CSPRWAIT[2:0]			—	—	—	—	—	CSPWWAIT[2:0]		
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	CSPWWAIT[2:0]	Page Write Cycle Wait Select*1 The value (CSPWWAIT[2:0]) clock cycles are inserted.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	CSPRWAIT[2:0]	Page Read Cycle Wait Select*2 The value (CSPRWAIT[2:0]) clock cycles are inserted.	R/W

Table 14.5 写访问模式的控制信号

Mode	引脚名称			
写访问模式	**WR1#**	**WR0#/WR#**	**BC1#**	**BC0#**
字节选通模式	✓	✓ (WR0#)	—	—
单写选通模式	—	✓ (WR#)	✓	✓

Note: ：启用，—：禁用

EWENB位（外部等待使能）

该位启用或禁用外部等待。

向该位写入1选择外部等待，并允许使用WAIT#信号控制每个周期中的等待次数。在这种状态下，当WAIT#信号处于低电平时，会插入等待周期。向该位写入0将禁用WAIT#信号。

PRENB位（页面读取访问使能）

该位启用或禁用页面读取访问。

Note: 当使用CSnCR中的MPXEN位选择地址数据复用IO接口时，不应设置该位来启用页面读取访问。地址数据复用IO接口不支持页面读取访问。

PWENB位（页面写访问使能）

该位启用或禁用页面写访问。

Note: 当使用CSnCR中的MPXEN位选择地址数据复用IO接口时，不应设置该位来启用页写访问。地址数据复用IO接口不支持页写访问。

PRMOD位（页面读取访问模式选择）

该位选择页面读取访问操作模式。

向该位写入0选择正常访问兼容模式，其中RD#信号被取反，并且每次读取数据时插入RD#断言等待。但是，当没有RD#断言等待时，RD#信号仅在外部总线访问的最终传输中被否定。

向该位写入1选择外部数据读取连续断言模式，其中插入RD#断言等待，并且在此时间段内连续断言RD#信号。

14.3.7 CSnWCR1:CSn等待控制寄存器1(n=0to7)

Base address: BUS = 0x4000_3000

Offset address: 0x0004 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	CSRWAIT[4:0]					—	—	—	CSWWAIT[4:0]				
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	CSPRWAIT[2:0]			—	—	—	—	—	CSPWWAIT[2:0]		
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	CSPWWAIT[2:0]	页写周期等待选择*1 值(CSWWWAIT[2:0])时钟周期被插入。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
10:8	CSPRWAIT[2:0]	页面读取周期等待选择*2 值(CSPRWAIT[2:0])时钟周期被插入。	R/W

Bit	Symbol	Function	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
20:16	CSWWAIT[4:0]	Normal Write Cycle Wait Select The value (CSWWAIT[4:0]) clock cycles are inserted.	R/W
23:21	—	These bits are read as 0. The write value should be 0.	R/W
28:24	CSRWAIT[4:0]	Normal Read Cycle Wait Select The value (CSRWAIT[4:0]) clock cycles are inserted.	R/W
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The CSPWWAIT[2:0] value is valid only when the PWENB bit in CSnMOD is set to 1.
Note 2. The CSPRWAIT[2:0] value is valid only when the PRENB bit in CSnMOD is set to 1.

Do not attempt to write the CSnWCR1 register while the external bus is being accessed. Set each of these bits within a range of the restrictions described in section 14.5.7. Constraints.

CSPWWAIT[2:0] bits (Page Write Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the second and subsequent accesses during a page write cycle. This setting is enabled when the PRENB bit in CSnMOD is set to 1.

Note: Be sure to satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

CSPRWAIT[2:0] bits (Page Read Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the second and subsequent accesses during a page read cycle. This setting is enabled when the PRENB bit in CSnMOD is set to 1.

Note: Be sure to satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.

CSWWAIT[4:0] bits (Normal Write Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the first access during a normal write cycle or page write cycle.

Note: Be sure to satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSRWAIT[4:0] bits (Normal Read Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into the first access during a normal read cycle or page read cycle.

Note: Be sure to satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

14.3.8 CSnWCR2 : CSn Wait Control Register 2 (n = 0 to 7)

Base address: BUS = 0x4000_3000
Offset address: 0x0008 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CSON[2:0]			—	WDON[2:0]			—	WRON[2:0]			—	RDON[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	AWAIT[1:0]		—	WDOFF[2:0]			—	CSWOFF[2:0]			—	CSROFF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W
20:16	CSWWAIT[4:0]	正常写周期等待选择 值(CSWWAIT[4:0])时钟周期被插入。	R/W
23:21	—	这些位被读取为0。写入值应为0。	R/W
28:24	CSRWAIT[4:0]	正常读周期等待选择 插入值(CSRWAIT[4:0])时钟周期。	R/W
31:29	—	这些位被读取为0。写入值应为0。	R/W

注1.CSPWWAIT[2:0]值仅在CSnMOD中的PWENB位设置为1时有效。注2.CSPRWAIT[2:0]值仅在CSnMOD中的PRENB位设置为1时有效。

在访问外部总线时不要尝试写CSnWCR1寄存器。在14.5.7节中描述的限制范围内设置这些位中的每一个。约束。

CSWWAIT[2:0]位（页面写周期等待选择）

这些位指定在页写周期期间插入第二次和后续访问的等待周期数。当CSnMOD中的PRENB位设置为1时，该设置被启用。

Note: 一定要满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0]value和CSnWCR2.CSON[2:0]value≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSWWAIT[2:0]值。

CSPRWAIT[2:0]位（页面读取周期等待选择）

这些位指定在页读取周期期间插入第二次和后续访问的等待周期数。当CSnMOD中的PRENB位设置为1时，该设置被启用。

Note: 一定要满足CSnWCR2.CSON[2:0]值≤CSnWCR2.RDON[2:0]值≤CSnWCR1.CSPRWAIT[2:0]值。

CSWWAIT[4:0]位（正常写周期等待选择）

这些位指定在正常写周期或页写周期期间插入第一次访问的等待周期数。

Note: 一定要满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0]value和CSnWCR2.CSON[2:0]value≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSWWAIT[4:0]值。

CSRWAIT[4:0]位（正常读周期等待选择）

这些位指定在正常读周期或页读周期期间插入第一次访问的等待周期数。

Note: 一定要满足CSnWCR2.CSON[2:0]值≤CSnWCR2.RDON[2:0]值≤CSnWCR1.CSRWAIT[4:0]值。

14.3.8 CSnWCR2:CSn等待控制寄存器2(n=0to7)

Base address: BUS = 0x4000_3000
Offset address: 0x0008 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CSON[2:0]			—	WDON[2:0]			—	WRON[2:0]			—	RDON[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	AWAIT[1:0]		—	WDOFF[2:0]			—	CSWOFF[2:0]			—	CSROFF[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	CSROFF[2:0]	Read-Access CS Extension Cycle Select The value (CSROFF[2:0]) of wait clock cycles are inserted	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	CSWOFF[2:0]	Write-Access CS Extension Cycle Select The value (CSWOFF[2:0]) of wait clock cycles are inserted	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	WDOFF[2:0]	Write Data Output Extension Cycle Select The value (WDOFF[2:0]) number of wait clock cycles are inserted	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
13:12	AWAIT[1:0]	Address Cycle Wait Select The value (AWAIT[1:0]) of wait clock cycles are inserted	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W
18:16	RDON[2:0]	RD Assert Wait Select The value (RDON[2:0]) of wait clock cycles inserted	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
22:20	WRON[2:0]	WR Assert Wait Select The value (WRON[2:0]) of wait clock cycles are inserted	R/W
23	—	This bit is read as 0. The write value should be 0.	R/W
26:24	WDON[2:0]	Write Data Output Wait Select The value (WDON[2:0]) of wait clock cycles are inserted	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	CSON[2:0]	CS Assert Wait Select The value (CSON[2:0]) of wait clock cycles inserted	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Do not attempt to write the CSnWCR2 register while the external bus is being accessed. Set each of these bits within a range of the restrictions described in section 14.5.7. Constraints.

CSROFF[2:0] bits (Read-Access CS Extension Cycle Select)

These bits specify the number of wait cycles to be inserted in a time period from the end of a wait cycle (RD signal negated) until the CSn# signal (n = 0 to 7) is negated in read access mode.

CSWOFF[2:0] bits (Write-Access CS Extension Cycle Select)

These bits specify the number of wait cycles to be inserted in a time period from the end of a wait cycle (WRn signal (n = 0 to 1) negated) until the CSn# signal (n = 0 to 7) is negated in write access mode.

Note: Be sure to satisfy CSnWCR2.WDOFF[2:0] value ≤ CSnWCR2.CSWOFF[2:0] value.

WDOFF[2:0] bits (Write Data Output Extension Cycle Select)

These bits specify the number of wait cycles to be inserted in a time period from the end of a wait cycle (WRn signal (n = 0 to 1) negated) until the write data output is complete in write access mode.

Note: Be sure to satisfy CSnWCR2.WDOFF[2:0] value ≤ CSnWCR2.CSWOFF[2:0] value.

AWAIT[1:0] bits (Address Cycle Wait Select)

These bits specify the number of wait cycles to be inserted into an address output cycle with the address/data multiplexed I/O interface.

Note: CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value

For read access, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

For write access, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

Bit	Symbol	Function	R/W
2:0	CSROFF[2:0]	读访问CS扩展周期选择 插入等待时钟周期的值(CSROFF[2:0])	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	CSWOFF[2:0]	写访问CS扩展周期选择 插入等待时钟周期的值(CSWOFF[2:0])	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	WDOFF[2:0]	写数据输出扩展周期选择 插入等待时钟周期数的值(WDOFF[2:0])	R/W
11	—	该位读取为0。写入值应为0。	R/W
13:12	AWAIT[1:0]	地址周期等待选择 插入等待时钟周期的值(AWAIT[1:0])	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W
18:16	RDON[2:0]	RD断言等待选择 插入的等待时钟周期值(RDON[2:0])	R/W
19	—	该位读取为0。写入值应为0。	R/W
22:20	WRON[2:0]	WR断言等待选择 插入等待时钟周期的值(WRON[2:0])	R/W
23	—	该位读取为0。写入值应为0。	R/W
26:24	WDON[2:0]	写数据输出等待选择 插入等待时钟周期的值(WDON[2:0])	R/W
27	—	该位读取为0。写入值应为0。	R/W
30:28	CSON[2:0]	CS断言等待选择 插入的等待时钟周期值(CSON[2:0])	R/W
31	—	该位读取为0。写入值应为0。	R/W

在访问外部总线时不要尝试写CSnWCR2寄存器。在14.5.7节中描述的限制范围内设置这些位中的每一个。约束。

CSROFF[2:0]位（读访问CS扩展周期选择）

这些位指定在读访问模式下从等待周期结束（RD信号取反）到CSn#信号（n=0到7）取反的时间段内插入的等待周期数。

CSWOFF[2:0]位（写访问CS扩展周期选择）

这些位指定从等待周期结束（WRn信号（n=0到1）被否定）到CSn#信号（n=0到7）被否定的时间段内插入的等待周期数访问模式。

Note: 一定要满足CSnWCR2.WDOFF[2:0]值≤CSnWCR2.CSWOFF[2:0]值。

WDOFF[2:0]位（写数据输出扩展周期选择）

这些位指定在写访问模式下从等待周期结束（WRn信号（n=0到1）取反）到写数据输出完成的时间段内插入的等待周期数。

Note: 一定要满足CSnWCR2.WDOFF[2:0]值≤CSnWCR2.CSWOFF[2:0]值。

AWAIT[1:0]位（地址周期等待选择）

这些位指定在地址数据复用的地址输出周期中插入的等待周期数
I/O interface.

Note: CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value

对于读访问，满足CSnWCR2.AWAIT[1:0]value+2≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSRWAIT[4:0] value.

对于写访问，满足CSnWCR2.AWAIT[1:0]value+2≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0]值和CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.WDON[2:0]值≤CSnWCR1.CSWWAIT[4:0] value.

RDON[2:0] bits (RD Assert Wait Select)

These bits specify the number of wait cycles to be inserted before the RD signal is asserted.

Note: For normal read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

For page read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.

Note: When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

WRON[2:0] bits (WR Assert Wait Select)

These bits specify the number of wait cycles to be inserted before the WRn signal (n = 0 to 1) is asserted.

Note: For normal write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

For page write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

Note: When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

WDON[2:0] bits (Write Data Output Wait Select)

These bits specify the number of wait cycles to be inserted before the write data is output.

Note: For normal write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

For page write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

Note: When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSON[2:0] bits (CS Assert Wait Select)

These bits specify the number of wait cycles to be inserted before the CSn# signal (n = 0 to 7) is asserted.

Note: For normal read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

For page read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.

For normal write access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

For page write access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

Note: When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value.

RDON[2:0]位（RD断言等待选择）

这些位指定在RD信号置位之前要插入的等待周期数。

Note: 对于正常的读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSRWAIT[4:0] value.

对于页读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSPRWAIT[2:0] value.

Note: 选择地址数据复用IO接口时，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

WRON[2:0]位（WR断言等待选择）

这些位指定在WRn信号（n=0到1）被断言之前要插入的等待周期数。

Note: 对于正常写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0]值和CSnWCR2.CSON[2:0]值≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSWWAIT[4:0] value.

对于页写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0]值和CSnWCR2.CSON[2:0]值≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSPWWAIT[2:0] value.

Note: 选择地址数据复用IO接口时，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

WDON[2:0]位（写数据输出等待选择）

这些位指定在输出写数据之前要插入的等待周期数。

Note: 对于正常写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0] value.

对于页写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0] value.

Note: 选择地址数据复用IO接口时，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSON[2:0]位（CS断言等待选择）

这些位指定在置位CSn#信号（n=0到7）之前要插入的等待周期数。

Note: 对于正常的读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSRWAIT[4:0] value.

对于页读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSPRWAIT[2:0] value.

对于正常的写访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0] value.

对于页写访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0] value.

Note: 选择地址数据复用IO接口时，满足CSnWCR2.CSON[2:0]值≤CSnWCR2.AWAIT[1:0] value.

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14.3.9 BUSSCNT<slave> : Slave Bus Control Register (<slave> = FHBIU, FLBIU, S0BIU, EQBIU, EOBIU, ECBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1100 (BUSSCNTFHBIU)
0x1104 (BUSSCNTFLBIU)
0x1110 (BUSSCNTS0BIU)
0x1140 (BUSSCNTEQBIU)
0x1144 (BUSSCNTEOBIU)
0x1148 (BUSSCNTECBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ARBS[1:0]	Arbitration Select for three masters Specify the priority between bus master. > : Fixed Priority ↔: Round-Robin 0 0: EDMAC > DMAC/DTC > CPU 0 1: Setting prohibited 1 0: (EDMAC ↔ DMAC/DTC) > CPU 1 1: (EDMAC ↔ DMAC/DTC) ↔ CPU	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note:
- BUSSCNT<slave> : <slave> is bus interface unit name for Slave
- The change is prohibited from initial value (0) to reserved bit. Operation when changing is not guaranteed.
- Arbitrate EDMAC and DMAC/DTC first, and arbitrate the result with CPU.

ARBS[1:0] bits (Arbitration Select for three masters)

The ARBS bits sets the arbitration method of each master.

14.3.10 BUSSCNT<slave> : Slave Bus Control Register (<slave> = PSBIU, PLBIU, PHBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1120 (BUSSCNTPSBIU)
0x1130 (BUSSCNTPLBIU)
0x1134 (BUSSCNTPHBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ARBS	Arbitration Select for two masters Specify the priority between bus master. > : Fixed Priority ↔: Round-Robin 0: DMAC/DTC > CPU 1: DMAC/DTC ↔ CPU	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

14.3.9 BUSSCNT<slave>:从总线控制寄存器(<slave>=FHBIU FLBIU S0BIU EQBIU, EOBIU, ECBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1100 (BUSSCNTFHBIU)
0x1104 (BUSSCNTFLBIU)
0x1110 (BUSSCNTS0BIU)
0x1140 (BUSSCNTEQBIU)
0x1144 (BUSSCNTEOBIU)
0x1148 (BUSSCNTECBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ARBS[1:0]	三个主控的仲裁选择 指定总线主机之间的优先级。>:固定优先级↔:循环 00：EDMAC>DMACDTC>CPU01：设置禁止10：（EDMAC↔DMACDTC）>CPU11：（EDMAC↔DMACDTC）↔CPU	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note:
- BUSSCNT<slave>:<slave>是Slave的总线接口单元名称
- 禁止从初始值(0)更改为保留位。不保证更换时的操作。
- 先仲裁EDMAC和DMACDTC，再与CPU仲裁结果。

ARBS[1:0]位（三个主机的仲裁选择）

ARBS位设置每个主机的仲裁方法。

14.3.10 BUSSCNT<slave>:从总线控制寄存器(<slave>=PSBIU PLBIU PHBIU)

Base address: BUS = 0x4000_3000

Offset address: 0x1120 (BUSSCNTPSBIU)
0x1130 (BUSSCNTPLBIU)
0x1134 (BUSSCNTPHBIU)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ARBS	两个主机的仲裁选择 指定总线主机之间的优先级。>:固定优先级↔:循环 0: DMAC/DTC > CPU 1: DMAC/DTC ↔ CPU	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note:
- BUSSCNT<slave> : <slave> is bus interface unit name for Slave
- The change is prohibited from initial value (0) to reserved bit. Operation when changing is not guaranteed.

ARBS bit (Arbitration Select for two masters)

The ARBS bits sets the arbitration method of each master.

14.3.11 BUSnERRADD : BUS Error Address Register (n = 1 to 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BERAD[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	Bus Error Address When a bus error occurs, these bits store the error address	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU related reset, see section 5, Resets and section 15, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BUS1ERRADD : Code bus

BUS2ERRADD : System bus

BUS3ERRADD : DMAC/DTC

BUS4ERRADD : EDMAC

BERAD[31:0] bits (Bus Error Address)

The BERAD[31:0] bits indicate the address when an error occurs on the associated bus. For detail of error that occurs by bus, see section 14.3.15. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 4) and section 14.6. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of ILERRSTAT, MMERRSTAT, SLERRSTAT in BUSnERRSTAT (n = 1 to 4) is set to 1, at the same time, the BERAD[31:0] bits store the address of the bus error access.

BERAD[31:0] bits are only valid when ILERRSTAT, MMERRSTAT, and SLERRSTAT in BUSnERRSTAT (n = 1 to 4) are set to 1.

14.3.12 BUSnERRRW : BUS Error Read Write Register (n = 1 to 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RWSTAT
Value after reset:	0	0	0	0	0	0	0	0

Note: 如果安全属性配置为安全：
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：
- 允许安全和非安全访问。

Note:
- BUSSCNT<slave>:<slave>是Slave的总线接口单元名称
- 禁止从初始值(0)更改为保留位。不保证更换时的操作。

ARBS位（两个主机的仲裁选择）

ARBS位设置每个主机的仲裁方法。

14.3.11 BUSnERRADD：总线错误地址寄存器（n=1到4）

Base address: BUS = 0x4000_3000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BERAD[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BERAD[31:0]	总线错误地址 当发生总线错误时，这些位存储错误地址	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU相关复位的详细信息，请参阅第5节，复位和第15节，内存保护单元(MPU)。

以下总线错误对应于主总线：

BUS1ERRADD:代码总线

BUS2ERRADD:系统总线

BUS3ERRADD : DMAC/DTC

BUS4ERRADD : EDMAC

BERAD[31:0]位（总线错误地址）

BERAD[31:0]位指示相关总线上发生错误时的地址。有关总线发生错误的详细信息，请参阅第14.3.15节。BUSnERRSTAT：总线错误状态寄存器n（n=1到4）和第14.6节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～4）中ILERRSTAT、MMERRSTAT、SLERRSTAT的对应位置1，同时BERAD[31:0]位存储总线地址错误访问。

BERAD[31:0]位仅在BUSnERRSTAT（n=1至4）中的ILERRSTAT、MMERRSTAT和SLERRSTAT设置为1时有效。

14.3.12 BUSnERRRW：总线错误读写寄存器（n=1到4）

Base address: BUS = 0x4000_3000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RWSTAT
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RWSTAT	Error Access Read/Write Status The status at the time of the error 0: Read access 1: Write access	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU related reset, see section 5, Resets and section 15, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BUS1ERRRW : Code bus

BUS2ERRRW : System bus

BUS3ERRRW : DMAC/DTC

BUS4ERRRW : EDMAC

RWSTAT bit (Error Access Read/Write Status)

The RWSTAT bit indicates the access status, (write access or read access) when an error occurs on the associated bus. For detail of error that occurs by bus, see section 14.3.15. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 4) and section 14.6. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of ILERRSTAT, MMERRSTAT, SLERRSTAT in BUSnERRSTAT (n = 1 to 4) is set to 1, at the same time, the RWSTAT bits store the read/write status of the bus error access.

RWSTAT bit is only valid when ILERRSTAT, MMERRSTAT, and SLERRSTAT in BUSnERRSTAT (n = 1 to 4) are set to 1.

14.3.13 BTZFnERRADD : BUS TZF Error Address Register (n = 1 to 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1900 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BTZFERAD[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BTZFERAD[31:0]	Bus TrustZone Filter Error Address When a bus error occurs, these bits store the error address	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU related reset, see section 5, Resets and section 15, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BTZF1ERRADD : Code bus

BTZF2ERRADD : System bus

BTZF3ERRADD : DMAC/DTC

BTZF4ERRADD : EDMAC

See Figure 14.1 for connection of each BUS.

Bit	Symbol	Function	R/W
0	RWSTAT	错误访问读写状态 出错时的状态 0：读访问1：写访问	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU相关复位的详细信息，请参阅第5节，复位和第15节，内存保护单元(MPU)。

以下总线错误对应于主总线：

BUS1ERRRW:代码总线

BUS2ERRRW:系统总线

BUS3ERRRW : DMAC/DTC

BUS4ERRRW : EDMAC

RWSTAT位（错误访问读写状态）

RWSTAT位指示相关总线上发生错误时的访问状态（写访问或读访问）。有关总线发生错误的详细信息，请参阅第14.3.15节。BUSnERRSTAT：总线错误状态寄存器n（n=1到4）和第14.6节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～4）中ILERRSTAT、MMERRSTAT、SLERRSTAT的相应位被置1，同时RWSTAT位存储总线错误访问的读写状态。

RWSTAT位仅在BUSnERRSTAT（n=1至4）中的ILERRSTAT、MMERRSTAT和SLERRSTAT设置为1时有效。

14.3.13 BTZFnERRADD:BUSTZF错误地址寄存器(n=1to4)

Base address: BUS = 0x4000_3000

Offset address: 0x1900 + 0x10 × (n - 1)

Bit position:	31																													0
Bit field:	BTZFERAD[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	BTZFERAD[31:0]	总线TrustZone过滤器错误地址 当发生总线错误时，这些位存储错误地址	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU相关复位的详细信息，请参阅第5节，复位和第15节，内存保护单元(MPU)。

以下总线错误对应于主总线：

BTZF1ERRADD:代码总线

BTZF2ERRADD:系统总线

BTZF3ERRADD : DMAC/DTC

BTZF4ERRADD : EDMAC

每个BUS的连接请参见图14.1。

BTZFERAD[31:0] bits (Bus TrustZone Filter Error Address)

The BTZFERAD[31:0] bits indicate the address, when an error occurs on the associated bus. For detail of error that occurs by bus, see section 14.3.15. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 4) and section 14.6. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of STERRSTAT in BUSnERRSTAT (n = 1 to 4) is set to 1, at the same time, the BTZFERAD[31:0] bits store the address of the bus error access.

BTZFERAD[31:0] bits are only valid when STERRSTAT in BUSnERRSTAT (n = 1 to 4) is set to 1.

14.3.14 BTZFnERRRW : BUS TZF Error Read Write Register (n = 1 to 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1904 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRWSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRWSTAT	TrustZone filter error access Read/Write Status The status at the time of the error 0: Read access 1: Write access	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU related reset, see section 5, Resets and section 15, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BTZF1ERRRW : Code bus

BTZF2ERRRW : System bus

BTZF3ERRRW : DMAC/DTC

BTZF4ERRRW : EDMAC

See Figure 14.1 for connection of each BUS.

TRWSTAT bit (TrustZone filter error access Read/Write Status)

The TRWSTAT bit indicates the access status, (write access or read access), when an error occurs on the associated bus. For detail of error that occurs by bus, see section 14.3.15. BUSnERRSTAT : BUS Error Status Register n (n = 1 to 4) and section 14.6. Bus Error Monitoring Section.

When an error occurs on the bus, the corresponding bit of STERRSTAT in BUSnERRSTAT (n = 1 to 4) is set to 1, at the same time, the TRWSTAT bits store the read/write status of the bus error access. The TRWSTAT bit is only valid when STERRSTAT in BUSnERRSTAT (n = 1 to 4) is set to 1.

14.3.15 BUSnERRSTAT : BUS Error Status Register n (n = 1 to 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1A00 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRSTAT	MMERRSTAT	—	STERRSTAT	SLERRSTAT
Value after reset:	0	0	0	0	0	0	0	0

BTZFERAD[31:0]位（总线TrustZone过滤器错误地址）

当相关总线上发生错误时，BTZFERAD[31:0]位指示地址。有关总线发生错误的详细信息，请参阅第14.3.15节。BUSnERRSTAT：总线错误状态寄存器n（n=1到4）和第14.6节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～4）中STERRSTAT的对应位被置1，同时BTZFERAD[31:0]位存储总线错误访问的地址。

BTZFERAD[31:0]位仅在BUSnERRSTAT（n=1至4）中的STERRSTAT设置为1时有效。

14.3.14 BTZFnERRRW：BUSTZF错误读写寄存器（n=1到4）

Base address: BUS = 0x4000_3000

Offset address: 0x1904 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRWSTAT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TRWSTAT	TrustZone过滤器错误访问读写状态 出错时的状态 0：读访问1：写访问	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU相关复位的详细信息，请参阅第5节，复位和第15节，内存保护单元(MPU)。

以下总线错误对应于主总线：

BTZF1ERRRW:代码总线

BTZF2ERRRW:系统总线

BTZF3ERRRW : DMAC/DTC

BTZF4ERRRW : EDMAC

每个BUS的连接请参见图14.1。

TRWSTAT位（TrustZone过滤器错误访问读写状态）

当相关总线上发生错误时，TRWSTAT位指示访问状态（写访问或读访问）。有关总线发生错误的详细信息，请参阅第14.3.15节。BUSnERRSTAT：总线错误状态寄存器n（n=1到4）和第14.6节。总线错误监控部分。

当总线发生错误时，BUSnERRSTAT（n=1～4）中STERRSTAT的对应位被置1，同时TRWSTAT位存储总线错误访问的读写状态。TRWSTAT位仅在BUSnERRSTAT（n=1至4）中的STERRSTAT设置为1时有效。

14.3.15 BUSnERRSTAT：总线错误状态寄存器n（n=1到4）

Base address: BUS = 0x4000_3000

Offset address: 0x1A00 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRSTAT	MMERRSTAT	—	STERRSTAT	SLERRSTAT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRSTAT	Slave bus Error Status 0: No error occurred 1: Error occurred	R
1	STERRSTAT	Slave TrustZone filter Error Status 0: No error occurred 1: Error occurred	R
2	—	This bit is read as 0.	R
3	MMERRSTAT	Master MPU Error Status 0: No error occurred 1: Error occurred	R
4	ILERRSTAT	Illegal address access Error Status 0: No error occurred 1: Error occurred	R
7:5	—	These bits are read as 0.	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU related reset, see section 5, Resets and section 15, Memory Protection Unit (MPU).

The following bus errors correspond to the master bus:

BUS1ERRSTAT : Code bus

BUS2ERRSTAT : System bus

BUS3ERRSTAT : DMAC/DTC

BUS4ERRSTAT : EDMAC

See Figure 14.1 for connection of each BUS

When an illegal access error, master MPU error, and slave bus error all occurred at the same time, the STAT bit is only valid in the following order of priority. The left side has higher priority.

Master MPU Error > Illegal access error, slave bus error

Note: Illegal access error and slave bus error do not occur at the same time.

Once ILERRSTAT, MMERRSTAT or SLERRSTAT is set, it cannot be cleared.

SLERRSTAT bit (Slave bus Error Status)

When slave error occurs by bus, BUSnERRSTAT.SLERRSTAT (n = 1 to 4) is set to 1. Clear condition is reset and set condition is when BUSnERRCLR.SLERRCLR (n = 1 to 4) is 1. Slave error is an error that occurs on a slave such as a timeout. For detail of slave error that occurs by bus, see section 14.6. Bus Error Monitoring Section.

STERRSTAT bit (Slave TrustZone filter Error Status)

When slave TrustZone filter error occurs by bus, BUSnERRSTAT.STERRSTAT (n = 1 to 4) is set to 1. Clear condition is reset and set condition is when BUSnERRCLR.STERRCLR (n = 1 to 4) is 1. The STERRSTAT bit is not set when the debugger accesses the security area. For detail of slave TrustZone filter error that occurs by bus, see section 52, Security Features .

MMERRSTAT bit (Master MPU Error Status)

When master MPU error occurs by bus, BUSnERRSTAT.MMERRSTAT (n = 1 to 4) is set to 1. Clear condition is reset and set condition is when BUSnERRCLR.MMERRCLR (n = 1 to 4) is 1. For detail of master MPU error that occurs by bus, see section 15, Memory Protection Unit (MPU).

Note: At master MPU error is occur in DMAC or DTC access, if error address value is not as master MPU area, Illegal address access error or slave error is occurring before DMAC or DTC access. Decide the what error was happened by referring the error address value.

Bit	Symbol	Function	R/W
0	SLERRSTAT	从站总线错误状态 0：未发生错误1：发生错误	R
1	STERRSTAT	从站TrustZone过滤器错误状态 0：未发生错误1：发生错误	R
2	—	该位读为0。	R
3	MMERRSTAT	主控MPU错误状态 0：未发生错误1：发生错误	R
4	ILERRSTAT	非法地址访问错误状态 0：未发生错误1：发生错误	R
7:5	—	这些位读为0。	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU相关复位的详细信息，请参阅第5节，复位和第15节，内存保护单元(MPU)。

以下总线错误对应于主总线：

BUS1ERRSTAT:代码总线

BUS2ERRSTAT:系统总线

BUS3ERRSTAT : DMAC/DTC

BUS4ERRSTAT : EDMAC

每个BUS的连接见图14.1

当非法访问错误、主MPU错误和从总线错误同时发生时，STAT位仅按以下优先级顺序有效。左侧优先级更高。

MasterMPUError>Illegalaccesserror slavebuserror

Note: 非法访问错误和从总线错误不会同时发生。

一旦ILERRSTAT、MMERRSTAT或SLERRSTAT被设置，就不能被清除。

SLERRSTAT位（从总线错误状态）

当总线发生从站错误时，BUSnERRSTAT.SLERRSTAT(n=1到4)设置为1。清除条件被复位，设置条件为BUSnERRCLR.SLERRCLR(n=1到4)为1。从站错误是一个错误发生在从属设备上，例如超时。关于总线发生的从站错误的详细信息，请参阅14.6节。总线错误监控部分。

STERRSTAT位（从属TrustZone过滤器错误状态）

当总线发生从机TrustZone过滤器错误时，BUSnERRSTAT.STERRSTAT(n=1至4)设置为1。清除条件复位，设置条件为BUSnERRCLR.STERRCLR(n=1至4)为1。STERRSTAT位为调试器访问安全区域时不设置。有关总线发生的从属TrustZone过滤器错误的详细信息，请参阅第52节，安全功能。

MMERRSTAT位（主MPU错误状态）

当总线发生主MPU错误时，BUSnERRSTAT.MMERRSTAT(n=1至4)设置为1。清除条件被复位，设置条件为BUSnERRCLR.MMERRCLR(n=1至4)为1。有关主MPU的详细信息总线发生的错误，请参阅第15节，内存保护单元(MPU)。

Note: 在访问DMAC或DTC时发生主MPU错误，如果错误地址值不是主MPU区域，则在访问DMAC或DTC之前发生非法地址访问错误或从站错误。通过参考错误地址值来确定发生了什么错误。

ILERRSTAT bit (Illegal address access Error Status)

When illegal address access error occurs by bus, BUSnERRSTAT.ILERRSTAT (n = 1 to 4) is set to 1. Clear condition is reset and set condition is when BUSnERRCLR.ILERRCLR (n = 1 to 4) is 1. For detail of illegal address access error that occurs by bus, see section 14.6. Bus Error Monitoring Section.

14.3.16 DMACDTCERRSTAT : DMAC/DTC Error Status Register

Base address: BUS = 0x4000_3000

Offset address: 0x1A24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRSTAT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRSTAT	Master TrustZone Filter Error Status 0: No error occurred 1: Error occurred	R
7:1	—	These bits are read as 0.	R

This register is cleared by reset other than MPU- and TZF-related resets which are Bus Master MPU Error Reset and TrustZone Filter Error Reset.

For detail of MPU related reset, see section 5, Resets, section 15, Memory Protection Unit (MPU) and section 52.2. Arm TrustZone Security .

MTERRSTAT bit (Master TrustZone Filter Error Status)

When a master TrustZone filter error occurs by DMAC or DTC, DMACDTCERRSTAT.MTERRSTAT is set to 1. Clear condition is reset and set condition is when DMACDTCERRCLR.MTERRCLR is 1.

For detail of master TrustZone filter error that occurs by DMAC or DTC, see section 16, DMA Controller (DMAC) and section 17, Data Transfer Controller (DTC)

14.3.17 BUSnERRCLR : BUS Error Clear Register n (n = 1 to 4)

Base address: BUS = 0x4000_3000

Offset address: 0x1A08 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRCLR	MMERRCLR	—	STERRCLR	SLERRCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRCLR	Slave bus Error Clear Writing 1 to the SLERRCLR bit clears the BUSnERRSTAT.SLERRSTAT (n = 1 to 4)	R/W*1
1	STERRCLR	Slave TrustZone filter Error Clear Writing 1 to the STERRCLR bit clears the BUSnERRSTAT.STERRSTAT (n = 1 to 4)	R/W*1
2	—	This bit is read as 0. The write value should be 0.	R/W
3	MMERRCLR	Master MPU Error Clear Writing 1 to the MMERRCLR bit clears the BUSnERRSTAT.MMERRSTAT (n = 1 to 4)	R/W*1
4	ILERRCLR	Illegal Address Access Error Clear Writing 1 to the ILERRCLR bit clears the BUSnERRSTAT.ILERRSTAT (n = 1 to 4)	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

ILERRSTAT位（非法地址访问错误状态）

当总线发生非法地址访问错误时，BUSnERRSTAT.ILERRSTAT(n=1至4)设置为1。清除条件被复位，设置条件为BUSnERRCLR.ILERRCLR(n=1至4)为1。有关非 法地址的详细信息总线发生的地址访问错误，见14.6节。总线错误监控部分。

14.3.16 DMACDTCERRSTAT：DMACDTC错误状态寄存器

Base address: BUS = 0x4000_3000

Offset address: 0x1A24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRSTAT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRSTAT	主TrustZone过滤器错误状态 0：未发生错误1：发生错误	R
7:1	—	这些位读为0。	R

该寄存器由除MPU和TZF相关的复位之外的复位清除，这些复位是总线主控MPU错误复位和TrustZone过滤器错误重置。

有关MPU相关复位的详细信息，请参见第5节，复位，第15节，内存保护单元(MPU)和第52.2节。手臂TrustZone Security .

MTERRSTAT位（主TrustZone过滤器错误状态）

当DMAC或DTC发生主TrustZone过滤器错误时，DMACDTCERRSTAT.MTERRSTAT设置为1。清除条件复位，设置条件为DMACDTCERRCLR.MTERRCLR为1。

有关DMAC或DTC发生的主TrustZone过滤器错误的详细信息，请参阅第16节，DMA控制器(DMAC)和第17节，数据传输控制器(DTC)

14.3.17 BUSnERRCLR：总线错误清除寄存器n（n=1到4）

Base address: BUS = 0x4000_3000

Offset address: 0x1A08 + 0x10 × (n - 1)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	ILERRCLR	MMERRCLR	—	STERRCLR	SLERRCLR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SLERRCLR	从总线错误清除 将1写入SLERRCLR位会清除BUSnERRSTAT.SLERRSTAT（n=1到4）	R/W*1
1	STERRCLR	从站TrustZone过滤器错误清除 将1写入STERRCLR位会清除BUSnERRSTAT.STERRSTAT（n=1到4）	R/W*1
2	—	该位读取为0。写入值应为0。	R/W
3	MMERRCLR	主MPU错误清除 将1写入MMERRCLR位会清除BUSnERRSTAT.MMERRSTAT（n=1到4）	R/W*1
4	ILERRCLR	非法地址访问错误清除 将1写入ILERRCLR位会清除BUSnERRSTAT.ILERRSTAT（n=1到4）	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note 1. Only 1 can be written to this bit. This bit is read as 0. Writing 0 to this bit has no effect.

The following bus errors correspond to the master bus:

BUS1ERRCLR : Code bus

BUS2ERRCLR : System bus

BUS3ERRCLR : DMAC/DTC

BUS4ERRCLR : EDMAC

When writing 1 to BUSnERRCLR (n = 1 to 4), stop the bus access that causes an error in the corresponding bus master.

14.3.18 DMACDTCERRCLR : DMAC/DTC Error Clear Register

Base address: BUS = 0x4000_3000

Offset address: 0x1A2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRCLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRCLR	Master TrustZone filter Error Clear Writing 1 to this bit clears the DMACDTCERRSTAT.MTERRSTAT flag.	R/W*1
7:1	—	This bit is read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note 1. Only 1 can be written to this bit. This bit is read as 0. Writing 0 to this bit has no effect.

When writing 1 to DMACDTCERRCLR, stop the bus access that causes an error in DMAC/DTC.

14.4 Endian and Data Alignment

The external bus has a data alignment function to control which byte of the data bus (D15 to D8, or D7 to D0) is used when accessing the external address space (the CS areas). Alignment is based on the bus specifications of the area to be accessed such as 8-bit, 16-bit bus space, data size, and endian format.

14.4.1 Data Alignment Control for the CS Areas

14.4.1.1 16-Bit Bus Space

When a 16-bit bus space is selected by the BSIZE[1:0] bits in CSnCR, the address buses A23 to A1 are enabled to output address signals in 16-bit units, and the address bus A0 is disabled (always outputs low).

When byte strobe mode is selected (the WRMOD bit = 0 in CSnMOD), the WR0# and WR1# pins are enabled, and the WR2# and WR3# pins are disabled (fixed high). The BC0# to BC3# pins are not used.

When single write strobe mode is selected (the WRMOD bit = 1 in CSnMOD), only the WR0# pin is enabled and it always outputs the low during write access, regardless of the data size. In this case, the WR1# to WR3# pins are invalid (always output the high). The valid byte position is indicated by the BC0# and BC1# pins. The WR2# and WR3# pins are not used.

In 16-bit bus space, page access can occur for accesses to data in 32-bit units. Page access can only occur when an access does not extend over a 32-bit boundary and causes no change in BC0# and BC1# signals. The conditions in which page access occurs are indicated by the letter (p) in Figure 14.3 and Figure 14.4.

- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

注1.该位只能写入1。该位被读取为0。向该位写入0无效。

以下总线错误对应于主总线：

BUS1ERRCLR:代码总线

BUS2ERRCLR:系统总线

BUS3ERRCLR : DMAC/DTC

BUS4ERRCLR : EDMAC

向BUSnERRCLR（n=1到4）写入1时，停止导致相应总线主机出错的总线访问。

14.3.18 DMACDTCERRCLR:DMACDTC错误清除寄存器

Base address: BUS = 0x4000_3000

Offset address: 0x1A2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	MTERRCLR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MTERRCLR	主TrustZone过滤器错误清除 向该位写入1会清除DMACDTCERRSTAT.MTERRSTAT标志。	R/W*1
7:1	—	该位读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

注1.该位只能写入1。该位被读取为0。向该位写入0无效。

向DMACDTCERRCLR写入1时，停止导致DMACDTC错误的总线访问。

14.4 字节序和数据对齐

外部总线具有数据对齐功能，用于控制访问外部地址空间（CS区域）时使用数据总线的哪个字节（D15到D8，或D7到D0）。对齐基于要访问的区域的总线规范，例如8位、16位总线空间、数据大小和字节序格式。

14.4.1 CS区域的数据对齐控制

14.4.1.1 16位总线空间

当通过CSnCR的BSIZE[1:0]位选择16位总线空间时，地址总线A23到A1被使能，以16位为单位输出地址信号，地址总线A0被禁止（始终输出低）。

Whenbytestrobemodeisselected(theWRMODbit=0inCSnMOD) theWR0#andWR1#pinsareenabled andthe WR2#和WR3#引脚被禁用（固定为高电平）。不使用BC0#至BC3#引脚。

Whensinglewritestrobemodeisselected(theWRMODbit=1inCSnMOD) onlytheWR0#pinisenabledanditalwaysoutputsthelowduringwriteaccess regardlessofthedatasize.在这种情况下，WR1#到WR3#引脚无效（始终输出高电平）。有效字节位置由BC0#和BC1#引脚指示。不使用WR2#和WR3#引脚。

在16位总线空间中，对32位单元中的数据的访问可以发生页访问。只有当访问不超过32位边界并且不会导致BC0#和BC1#信号发生变化时，才会发生页面访问。页面访问发生的条件由图14.3和图14.4中的字母(p)表示。

In 16-bit bus space, the valid positions of data external to the MCU and of control signals differ according to whether the endian is big or little.

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 RD Data bus D15–D08	WR0/BC0 RD Data bus D07–D00
8 bits	4n	One	First	8 bits	4n			7–0
	4n+1	One	First	8 bits	4n		7–0	
	4n+2	One	First	8 bits	4n+2			7–0
	4n+3	One	First	8 bits	4n+2		7–0	
16 bits	4n	One	First	16 bits	4n		15–8	7–0
	4n+2	One	First	16 bits	4n+2		15–8	7–0
32 bits	4n	Two	First	16 bits	4n		15–8	7–0
			Second	16 bits	4n+2	(p)	31–24	23–16

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD)

Figure 14.3 Data alignment in 16-bit bus space with little-endian order for CS areas

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 RD Data bus D15–D08	WR0/BC0 RD Data bus D07–D00
8 bits	4n	One	First	8 bits	4n		7–0	
	4n+1	One	First	8 bits	4n			7–0
	4n+2	One	First	8 bits	4n+2		7–0	
	4n+3	One	First	8 bits	4n+2			7–0
16 bits	4n	One	First	16 bits	4n		15–8	7–0
	4n+2	One	First	16 bits	4n+2		15–8	7–0
32 bits	4n	Two	First	16 bits	4n		31–24	23–16
			Second	16 bits	4n+2	(p)	15–8	7–0

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD)

Figure 14.4 Data alignment in 16-bit bus space with big-endian order for CS areas

14.4.1.2 8-Bit Bus Space

When an 8-bit bus space is selected by the BSIZE[1:0] bits in CSnCR, the address buses A23 to A0 are enabled to output address signals in byte units.

In 8-bit bus space, only the WR0# pin is valid regardless of write access mode, and it always outputs low during write access. The WR1# to WR3# pins and the BC0# to BC3# pins are not used.

在16位总线空间中，MCU外部数据和控制信号的有效位置根据字节序的大小而有所不同。

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 RD 数据总线 D15–D08	WR0/BC0 RD 数据总线 D07–D00
8 bits	4n	One	First	8 bits	4n			7–0
	4n+1	One	First	8 bits	4n		7–0	
	4n+2	One	First	8 bits	4n+2			7–0
	4n+3	One	First	8 bits	4n+2		7–0	
16 bits	4n	One	First	16 bits	4n		15–8	7–0
	4n+2	One	First	16 bits	4n+2		15–8	7–0
32 bits	4n	Two	First	16 bits	4n		15–8	7–0
			Second	16 bits	4n+2	(p)	31–24	23–16

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）

Figure 14.3 16位总线空间中的数据对齐，CS区域采用little-endian顺序

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 RD 数据总线 D15–D08	WR0/BC0 RD 数据总线 D07–D00
8 bits	4n	One	First	8 bits	4n		7–0	
	4n+1	One	First	8 bits	4n			7–0
	4n+2	One	First	8 bits	4n+2		7–0	
	4n+3	One	First	8 bits	4n+2			7–0
16 bits	4n	One	First	16 bits	4n		15–8	7–0
	4n+2	One	First	16 bits	4n+2		15–8	7–0
32 bits	4n	Two	First	16 bits	4n		31–24	23–16
			Second	16 bits	4n+2	(p)	15–8	7–0

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）

Figure 14.4 16位总线空间中的数据对齐，CS区域采用大端顺序

14.4.1.2 8位总线空间

当CSnCR中的BSIZE[1:0]位选择8位总线空间时，地址总线A23到A0被启用，以字节为单位输出地址信号。

在8位总线空间中，无论写访问模式如何，只有WR0#引脚有效，并且在写访问期间始终输出低电平。不使用WR1#至WR3#引脚和BC0#至BC3#引脚。

Page access can occur for accesses to data in 16- or 32-bit units. Page access can only occur when an access does not extend over a 32-bit boundary. The conditions in which page access occurs are indicated by the letter (p) in Figure 14.5 and Figure 14.6.

In 8-bit bus space, the valid positions of data external to the MCU are D7 to D0 and WR0# is used as the control signal, regardless of the endian mode.

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 RD Data bus D15 D08	WR0/BC0 RD Data bus D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
	4n+2	Two	First	8 bits	4n+2			7 0
			Second	8 bits	4n+3	(p)		15 8
32 bits	4n	Four	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
			Third	8 bits	4n+2	(p)		23 16
			Fourth	8 bits	4n+3	(p)		31 24

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD)

Note:
- Tag holds the cached address [31:10] and is not cleared by the cache flush function.
- V is a valid bit and exists for each cache line. This bit shows the validated data stored in the cache line and is cleared by a reset and the cache flush function. This bit is also cleared when cache off status changes into cache on status. For example, CACTL.ENS/ENC changes from 0 to 1.
- Data holds 256 bits of data in each cache line.
- LRU (least recently used) is a way to replace for a cache line.
- Comparator determines whether data to be accessed is stored in the cache line. If the valid bit V is set and the address is the address stored in the tag, the cache determines that access is a hit. Otherwise, it is a miss hit.

Figure 14.5 Data alignment (little-endian) in 8-bit bus space

对16位或32位单元中的数据的访问可能会发生页访问。只有当访问不超过32位边界时，才会发生页面访问。页面访问发生的条件由图14.5和图14.6中的字母(p)表示。

在8位总线空间中，MCU外部数据的有效位置为D7到D0，WR0#用作控制信号，与字节序模式无关。

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 RD 数据总线 D15 D08	WR0/BC0 RD 数据总线 D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
	4n+2	Two	First	8 bits	4n+2			7 0
			Second	8 bits	4n+3	(p)		15 8
32 bits	4n	Four	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
			Third	8 bits	4n+2	(p)		23 16
			Fourth	8 bits	4n+3	(p)		31 24

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）

Note:
- 标签保存缓存地址[31:10]并且不会被缓存刷新功能清除。
- V是有效位并且存在于每个高速缓存行。该位显示存储在高速缓存行中的验证数据，并通过复位和高速缓存刷新功能清除。当缓存关闭状态变为缓存开启状态时，该位也会被清除。例如，CACTL.ENSENC从0变为1。
- 数据在每个高速缓存行中保存256位数据。
- LRU（最近最少使用）是一种替换缓存行的方法。
- 比较器确定要访问的数据是否存储在高速缓存行中。如果设置了有效位V并且地址是存储在标签中的地址，则缓存确定访问是命中的。否则，这是一个未命中的命中。

Figure 14.5 8位总线空间中的数据对齐（小端序）

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 RD D15 D08	WR0/BC0 RD D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			15 8
			Second	8 bits	4n+1	(p)		7 0
	4n+2	Two	First	8 bits	4n+2			15 8
			Second	8 bits	4n+3	(p)		7 0
32 bits	4n	Four	First	8 bits	4n			31 24
			Second	8 bits	4n+1	(p)		23 16
			Third	8 bits	4n+2	(p)		15 8
			Fourth	8 bits	4n+3	(p)		7 0

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD)

Figure 14.6 Data alignment in 8-bit bus space with big-endian order

14.5 Operation of CS Area Controller

14.5.1 Separate Bus

This section describes the various timings for bus operations.

The CS area controller (CSC) operates in synchronization with the external bus clock (BCLK). Operation cycles, such as wait cycles specified in the CSC register, are counted on BCLK. In the following description, the frequencies of BCLK and EBCLK pin output are the same, unless otherwise noted. Access through the external bus starts at the same point as the output of a rising edge on the EBCLK pin. However, if the external bus clock (BCLK) and the output on the EBCLK pin are at different frequencies so that a single request from a bus master for transfer leads to two or more rounds of access through the external bus, the wait settings may cause the start of access for the second and subsequent rounds to coincide with the falling edge of the output on the EBCLK pin (see Figure 14.12 to Figure 14.16). If recovery cycles are inserted for bus access, the setting for the number of recovery cycles may also cause the start of access for the second and subsequent rounds to coincide with the falling edge of the output on the EBCLK pin (see Figure 14.34).

(a) Tw1 to Twn (Clock Cycles of Waiting for a Normal Read Cycle or Normal Write Cycle)

The period from Tw1 to Twn is the number of clock cycles from the start of access through the external bus clock to 1 cycle before the strobe signal is valid. The number of cycles is selectable from 0 to 31. Within this period, the timing of CSn#, RD#, and WRn# assertion (driving the signals low) is determined by the respective wait settings. The wait periods are controlled by the CS Assert Wait Select bits (CSON), the RD Assert Wait Select bits (RDON), the WR Assert Wait Select bits (WRON), and the Write Data Output Wait Select bits (WDON) in CSn Wait Control Register 2 (CSnWCR2). The number of clock cycles for each of these wait periods is selectable as a value from 0 to 7, counted from the start of external bus access. The selectable numbers of cycles is also within the overall number of clock cycles required for waiting to read or write.

(b) Tend (Clock Cycle where the Strobe Signal is Valid)

Tend is the next clock cycle after completion of the wait period for a normal cycle of read or write, or for a cycle of page reading or page writing. If the wait select bit for these cycles is 0, bus access starts on the clock cycle where the strobe signal is valid. The RD# and WRn# signals are negated in the next clock cycle. For a read access, the clock cycle where the

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 RD D15 D08	WR0/BC0 RD D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			15 8
			Second	8 bits	4n+1	(p)		7 0
	4n+2	Two	First	8 bits	4n+2			15 8
			Second	8 bits	4n+3	(p)		7 0
32 bits	4n	Four	First	8 bits	4n			31 24
			Second	8 bits	4n+1	(p)		23 16
			Third	8 bits	4n+2	(p)		15 8
			Fourth	8 bits	4n+3	(p)		7 0

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）

Figure 14.6 8位总线空间中的数据对齐，大端顺序

14.5 CS区域控制器的操作

14.5.1 独立巴士

本节介绍总线操作的各种时序。

CS区域控制器(CSC)与外部总线时钟(BCLK)同步运行。操作周期，例如在CSC寄存器中指定的等待周期，在BCLK上计数。在以下描述中，BCLK和EBCLK引脚输出的频率是相同的，除非另有说明。通过外部总线的访问与EBCLK引脚上的上升沿输出在同一点开始。但是，如果外部总线时钟(BCLK)和EBCLK引脚上的输出频率不同，以至于来自总线主机的单个传输请求导致通过外部总线进行两轮或多轮访问，则等待设置可能会导致第二轮和后续轮次的访问开始与EBCLK引脚上输出的下降沿一致（参见图14.12至图14.16）。如果为总线访问插入恢复周期，恢复周期数的设置也可能导致第二轮及后续轮次的访问开始与EBCLK引脚输出的下降沿一致（见图14.34）。

(a)Tw1到Twn（等待正常读周期或正常写周期的时钟周期）

从Tw1到Twn的周期是从通过外部总线时钟开始访问到选通信号有效之前的1个周期的时钟周期数。周期数可在0到31之间选择。在此周期内，CSn#、RD#和WRn#断言（将信号驱动为低电平）的时序由各自的等待设置确定。等待周期由CS断言等待选择位(CSON)、RD断言等待选择位(RDON)、WR断言等待选择位(WRON)和CSn等待中的写数据输出等待选择位(WDON)控制控制寄存器2(CSnWCR2)。每个等待周期的时钟周期数可选择从0到7的值，从外部总线访问开始计算。可选择的周期数也在等待读取或写入所需的时钟周期总数之内。

(b)Tend（选通信号有效的时钟周期）

Tend是完成正常读取或写入周期或页面读取或页面写入周期的等待周期后的下一个时钟周期。如果这些周期的等待选择位为0，则总线访问在选通信号有效的时钟周期开始。RD#和WRn#信号在下一个时钟周期被否定。对于读访问，时钟周期

strobe signal is valid is where the data to be read is sampled. If an external wait is enabled, the wait signal is sampled on the cycle where the strobe signal is valid. The bus cycle is extended if the wait signal is low. The bus cycle completes in the next clock cycle if the wait signal is high. Tend indicates the cycle where sampling of the wait signal starts.

After the first cycle where the strobe signal is valid during page access, second and subsequent page access operations (point (e) below) start in the next cycle, except during write access with a setting other than 0 for write-data output extension clock cycles (point (d) below) has been made. If the setting for the RD or WR assertion wait is any value other than 0, the RD# and WRn# signals are negated in the next clock cycle. If the setting is 0, assertion continues. Additionally, the CSn# signal continues to be asserted rather than negated.

(c) Tn1 to Tnm (Clock Cycles of CS Extension)

For normal access, Tn1 to Tnm represent the clock cycles of the period following the cycle where the strobe signal is valid (Tend) up to negation of the CSn# signal. For read or write access, the negation timing can be controlled by the read-access CS Extension Cycle Select bits (CSROFF) and the write-access CS Extension Cycle Select bits (CSWOFF) in the CSn Wait Control Register 2 (CSnWCR2), respectively.

The number of cycles is counted from the cycle following the cycle where the strobe signal is valid.

For page access, Tn1 to Tnm represent the clock cycles of the period following the last cycle where the strobe signal is valid up to negation of the CSn# signal.

For write access, setting the Write Data Output Extension Cycle Select bits (WDOFF) controls extension of the period where the address and output data are valid.

(d) Tdw1 to Tdwn (Write-Data Output Extension Clock Cycles)

For write access, if the wait setting for write-data output extension is any value other than 0, the specified clock cycles are inserted from the cycle following the cycle where the strobe signal is valid (Tend).

For normal access, this period is inserted within the period of clock cycles for the CS extension (point (c) above).

For page access, this period is inserted within the period of the cycle where the strobe signal is valid and subsequent page accesses or within the period of clock cycles for the CS extension (point (c) above). Valid address and data output are extended over this period, and the WRn# signal is negated.

(e) Tpw1 to Tpwn (Page-Read Cycle Wait or Page-Write Cycle Wait)

For the second and subsequent bus cycles during page access, the values for a page-read cycle wait or page-write cycle wait are used instead of the settings for a normal read or write cycle wait. The settings in the WR Assert Wait Select bits become enabled in the same way as for the first access. The RD assertion control operation depends on the setting for page-read access mode (the PRMOD bit in CSnMOD) as follows:

CSnMOD.PRMOD = 0:

A wait until RD assertion is inserted in the same way as for the first access, and the RD# signal is negated.

CSnMOD.PRMOD = 1:

Although a wait until RD assertion is inserted in the same way as for normal-access compatibility mode, the RD# signal continues to be asserted over this period

(f) Tr1 to Trn (Recovery Cycles)

Recovery cycles can be inserted from the point where a bus cycle is complete (CSn# signal negation). The number of recovery cycles can be controlled by setting the Read Recovery (RRCV) or Write Recovery (WRCV) bits in the CSn Recovery Cycle Register (CSnREC). Both numbers of recovery cycles are counted from the end of a bus cycle (CSn# negation) and can be selected from 0 to 15 cycles. For details on recovery cycles, see section 14.5.4. Insertion of Recovery Cycles.

(1) Normal Access

When the PRENB and PWENB bits in CSnMOD are set to 0 to disable page-read and page-write access, all bus accesses takes the form of normal read and write operations. Even when these bits are set to 1 to enable page-read and page-write access, bus access other than page access takes the form of normal read and write operations.

Figure 14.7 to Figure 14.9 show the normal access operations.

选通信号有效是要读取的数据被采样的地方。如果启用了外部等待，则在选通信号有效的周期对等待信号进行采样。如果等待信号为低，则延长总线周期。如果等待信号为高电平，则总线周期在下一个时钟周期完成。Tend表示等待信号采样开始的周期。

在页面访问期间选通信号有效的第一个周期之后，第二个和后续页面访问操作（下面的(e)点）在下一个周期开始，但在写入数据输出扩展时钟设置为0以外的写入访问期间除外循环（下面的(d)点）已经完成。如果RD或WR断言等待的设置为0以外的任何值，则RD#和WRn#信号在下一个时钟周期被否定。如果设置为0，则断言继续。此外，CSn#信号继续被断言而不是被否定。

(c)Tn1到Tnm（CS扩展的时钟周期）

对于正常访问，Tn1至Tnm表示从选通信号有效(Tend)到CSn#信号无效的周期之后的周期的时钟周期。对于读或写访问，取反时序可由CSn等待中的读访问CS扩展周期选择位(CSROFF)和写访问CS扩展周期选择位(CSWOFF)控制

分别控制寄存器2(CSnWCR2)。

周期数从选通信号有效的周期之后的周期开始计数。

对于页访问，Tn1到Tnm表示从选通信号有效直到CSn#信号取反的最后一个周期之后的周期的时钟周期。

对于写访问，设置写数据输出延长周期选择位(WDOFF)控制地址和输出数据有效期间的延长。

(d)Tdw1到Tdwn（写数据输出扩展时钟周期）

对于写访问，如果写数据输出扩展的等待设置为0以外的任何值，则从选通信号有效(Tend)周期的下一个周期插入指定的时钟周期。

对于正常访问，此周期插入到CS扩展的时钟周期周期内（上面的(c)点）。

对于页面访问，该周期被插入到选通信号有效的周期和后续页面访问的周期内，或者在CS扩展的时钟周期周期内（上面的(c)点）。有效地址和数据输出在此期间延长，并且WRn#信号被取反。

(e)Tpw1到Tpwn（页面读取周期等待或页面写入周期等待）

对于页面访问期间的第二个和后续总线周期，使用页面读取周期等待或页面写入周期等待的值，而不是正常读取或写入周期等待的设置。WRAssertWaitSelect位中的设置以与第一次访问相同的方式启用。RD断言控制操作取决于页面读取访问模式的设置（CSnMOD中的PRMOD位），如下所示：

CSnMOD.PRMOD = 0:

等待RD断言以与第一次访问相同的方式插入，并且RD#信号被否定。

CSnMOD.PRMOD = 1:

尽管以与正常访问兼容模式相同的方式等待RD断言插入，但RD#信号在此期间继续断言

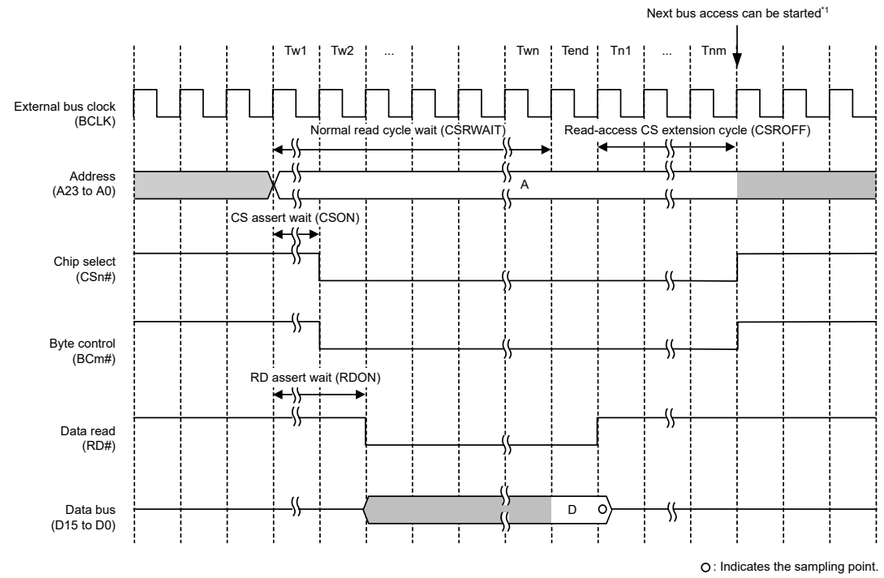
(f) Tr1 to Trn (Recovery Cycles)

恢复周期可以从总线周期完成的点插入（CSn#信号否定）。可以通过设置CSn恢复周期寄存器(CSnREC)中的读取恢复(RRCV)或写入恢复(WRCV)位来控制恢复周期的数量。两个恢复周期数都是从总线周期结束（CSn#否定）开始计算的，并且可以从0到15个周期中选择。有关恢复周期的详细信息，请参阅第14.5.4节。插入恢复周期。

(1) 正常访问

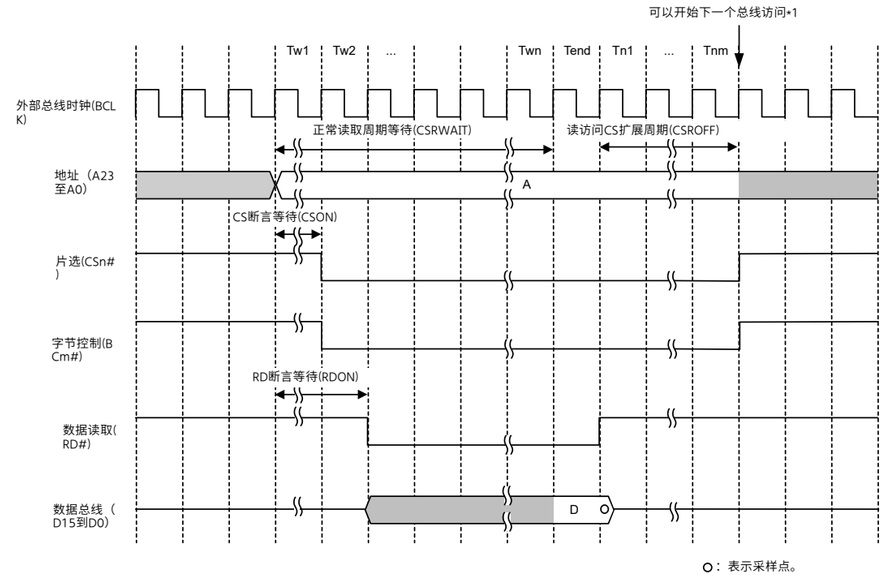
当CSnMOD中的PRENB和PWENB位设置为0以禁用页面读取和页面写入访问时，所有总线访问都采用正常读写操作的形式。即使将这些位设置为1以启用页面读取和页面写入访问，页面访问以外的总线访问仍采用正常读取和写入操作的形式。

图14.7至图14.9显示了正常的访问操作。



Note 1. When CSnWCR2.CSROFF[2:0] = 000b. the next round of bus access can start 1 cycle later.

Figure 14.7 Bus timing for normal read operation (n = 0 to 7, m = 0 to 1)



注1.当CSnWCR2.CSROFF[2:0]=000b时。下一轮总线访问可以在1个周期后开始。

Figure 14.7 正常读取操作的总线时序（n=0到7，m=0到1）

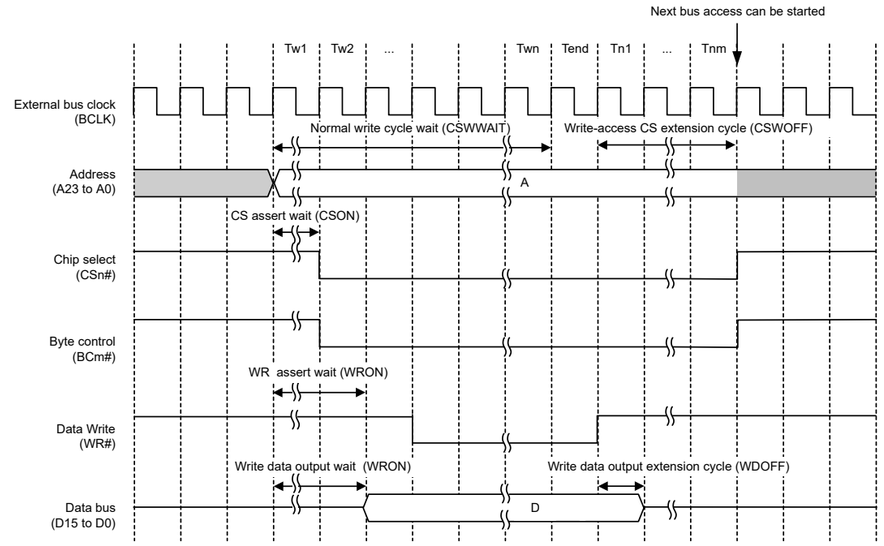


Figure 14.8 Bus timing for normal write operation in single-write strobe mode (n = 0 to 7, m = 0 to 1)

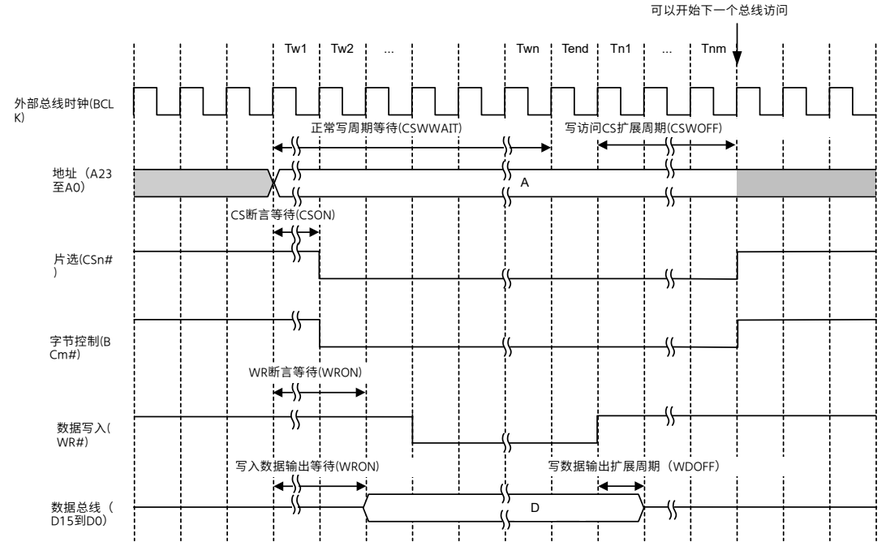


Figure 14.8 单次写入选通模式下正常写入操作的总线时序（n=0到7，m=0到1）

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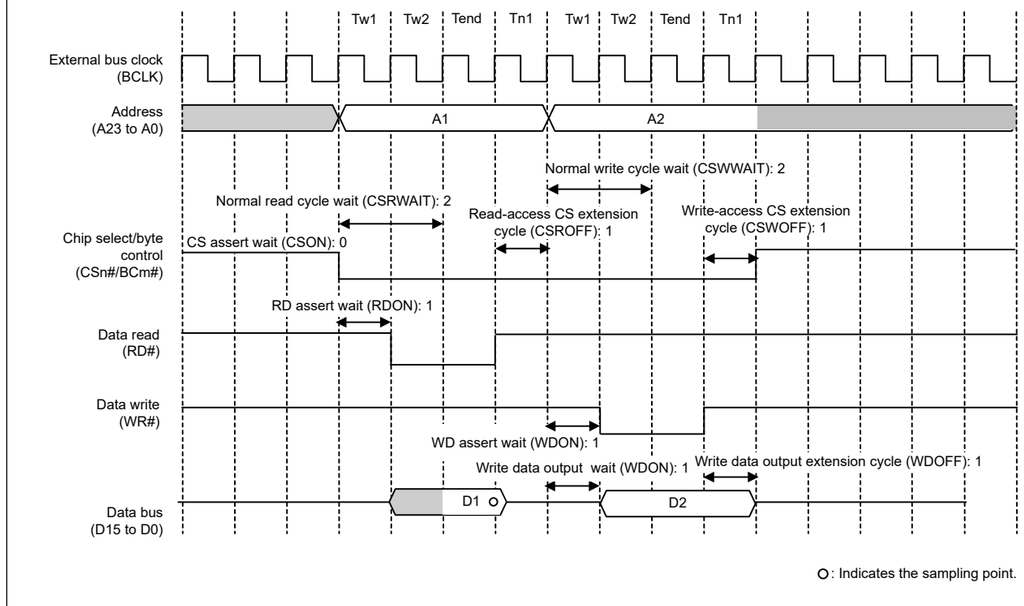


Figure 14.9 Example of normal access operation for read and write (n = 0 to 7, m = 0 to 1)

When two or more rounds of external bus access are required in response to a single request for transfer from a bus master, normal access operations (steps (a) to (d) above) are repeated. Figure 14.10 and Figure 14.11 show examples of operations when two rounds of bus access are generated in response to a single request for transfer. If the recovery cycle insertion condition is satisfied, recovery cycles (step (f) above) are also inserted in the second and subsequent external bus accesses (see Figure 14.32).

The values of the wait control registers shown in the figures are example settings. In your application, set the registers appropriately for the specifications of connected devices.

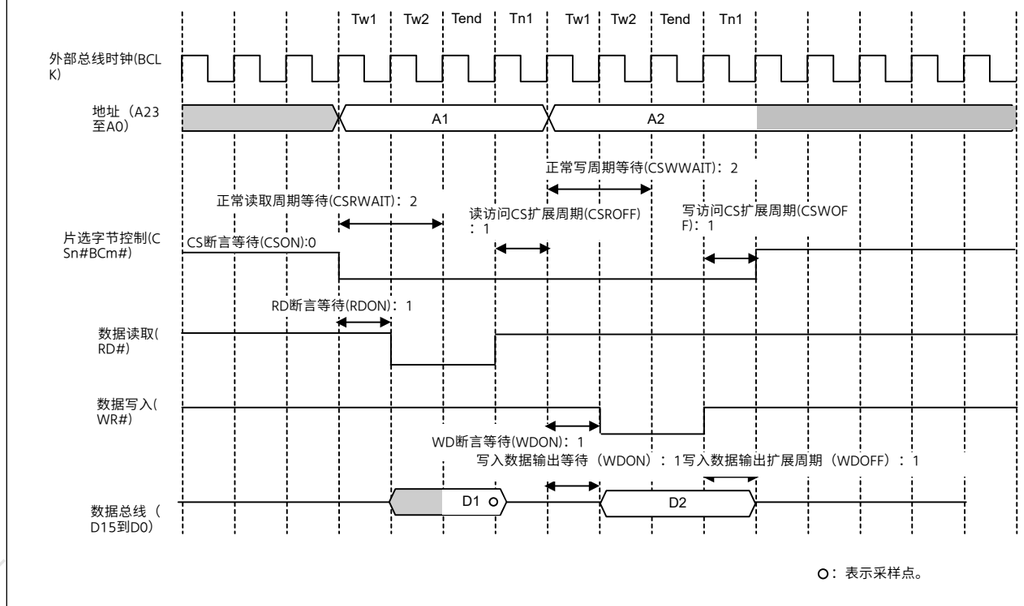


Figure 14.9 读取和写入的正常访问操作示例（n=0到7，m=0到1）

当响应来自总线主机的单个传输请求需要两轮或多轮外部总线访问时，重复正常访问操作（上述步骤（a）至（d））。图14.10和图14.11显示了为响应单个传输请求而生成两轮总线访问时的操作示例。如果恢复周期插入条件被满足，恢复周期（上面的步骤（f））也被插入到第二次和随后的外部总线访问中（见图14.32）。

图中所示的等待控制寄存器的值是示例设置。在您的应用程序中，根据连接设备的规格适当设置寄存器。

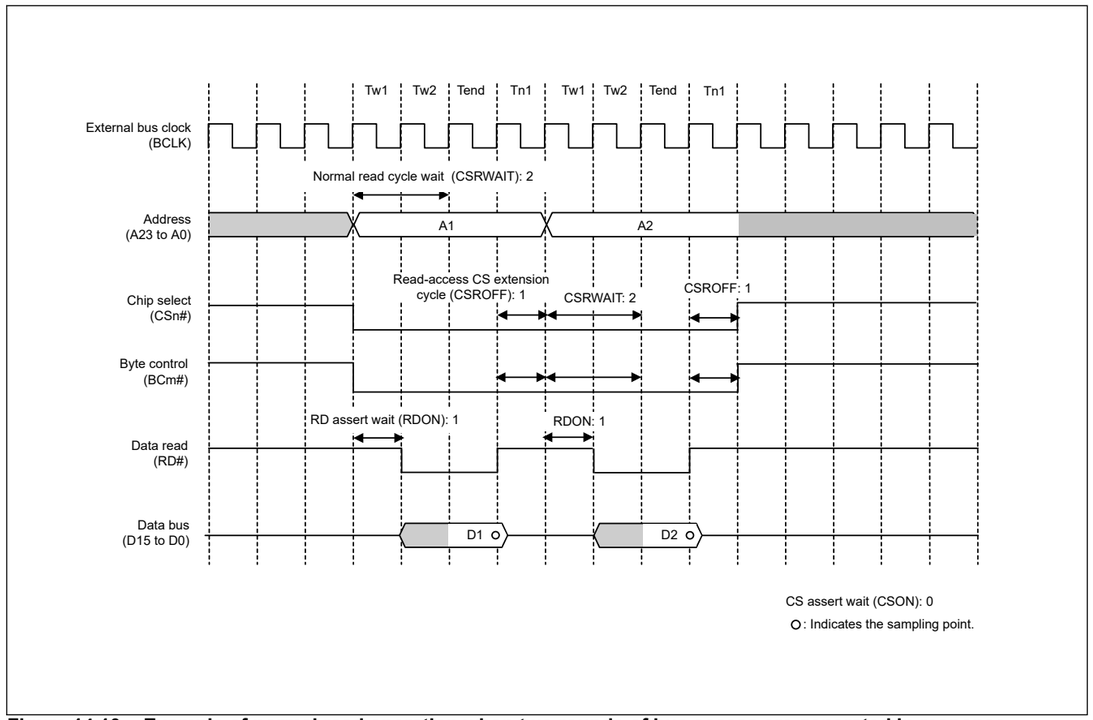


Figure 14.10 Example of normal read operation when two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0 to 1)

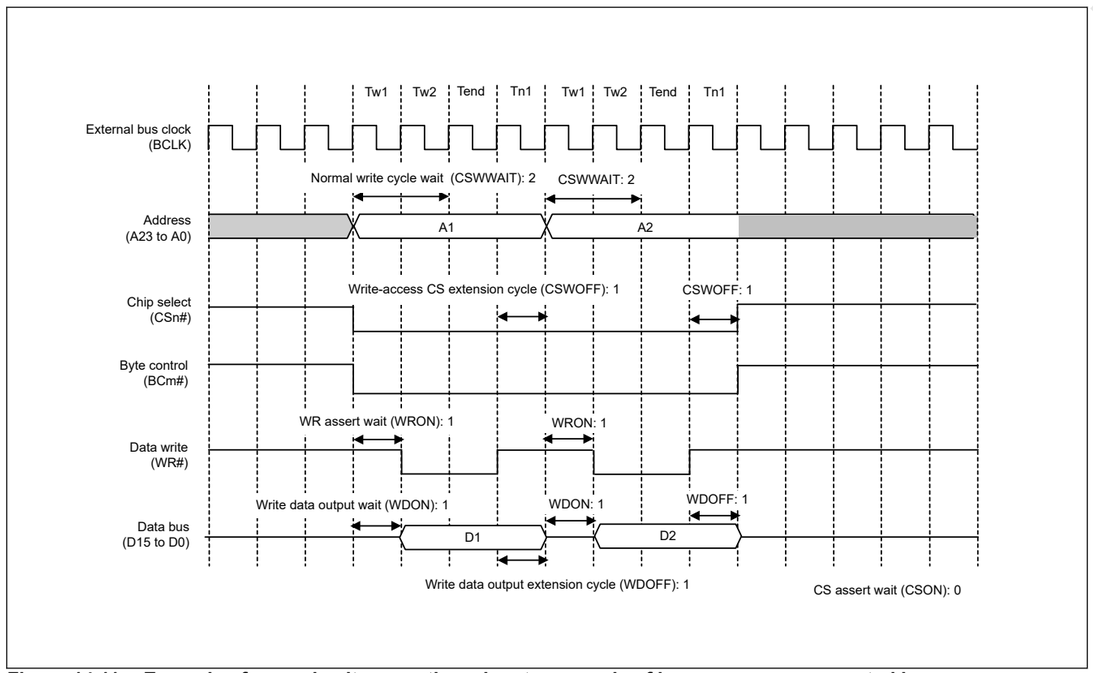


Figure 14.11 Example of normal write operation when two rounds of bus access are generated in response to a single transfer request in single-write strobe mode (n = 0 to 7, m = 0 to 1)

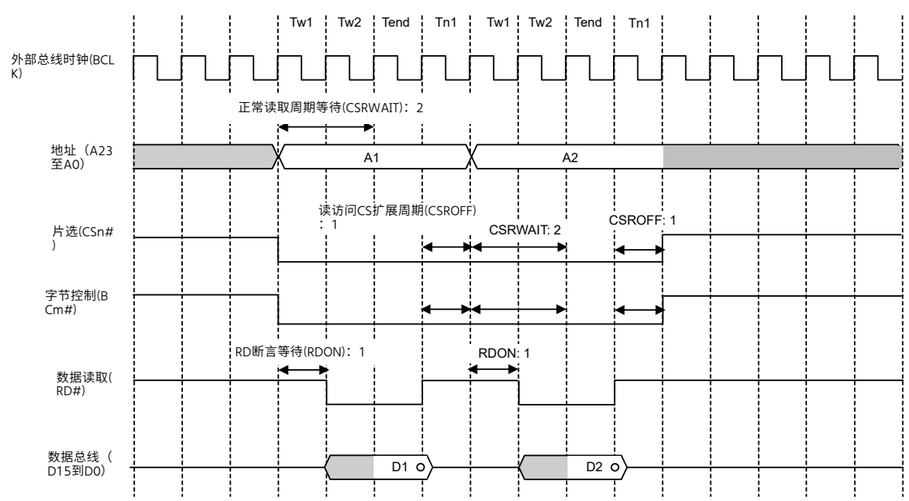


Figure 14.10 响应单个传输请求（n=0到7，m=0到1）生成两轮总线访问时的正常读取操作示例

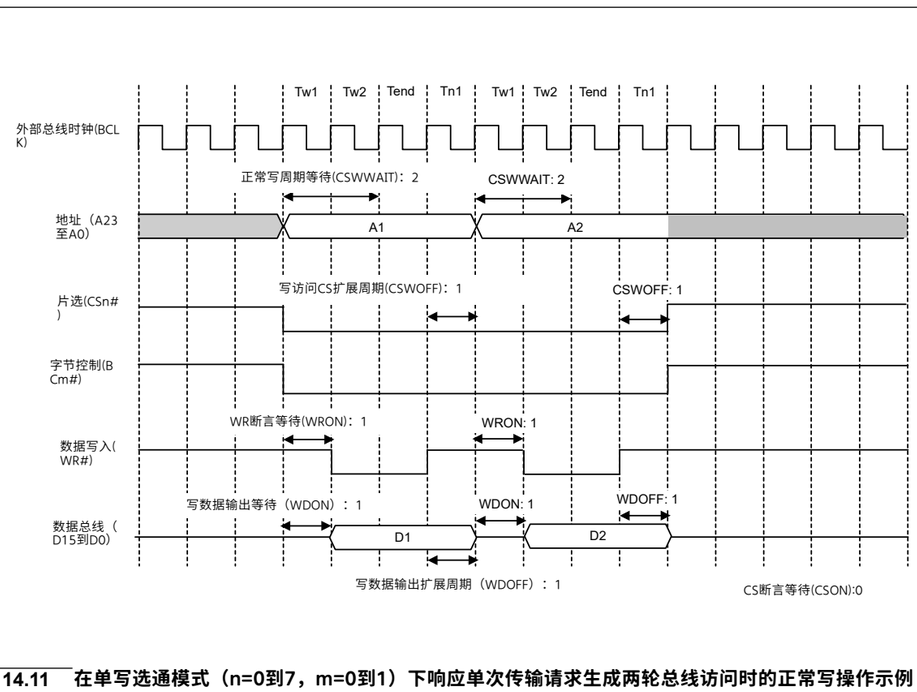


Figure 14.11 在单写选通模式（n=0到7，m=0到1）下响应单次传输请求生成两轮总线访问时的正常写操作示例

Figure 14.12 to Figure 14.16 show examples of normal accesses made when BCLK/2 is selected as the frequency division in the EBCLK Pin Output Select bit.

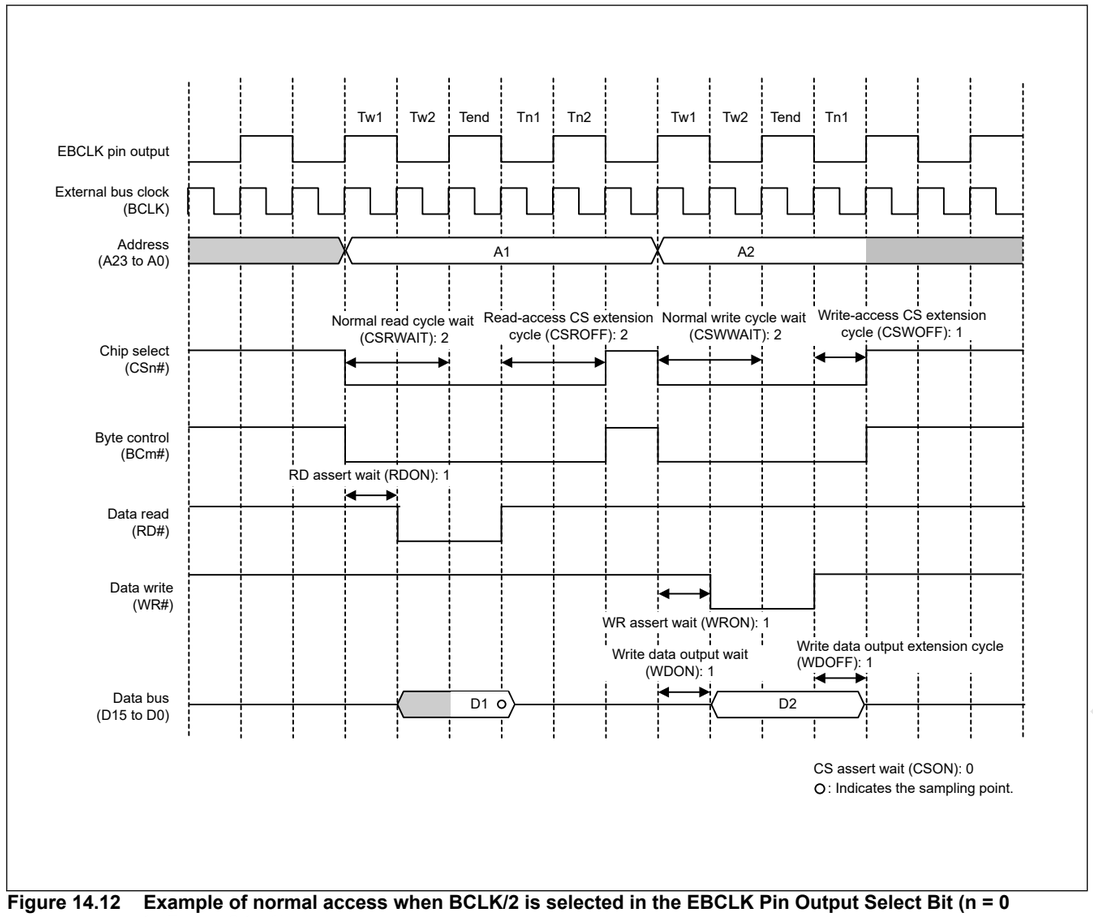


Figure 14.12 Example of normal access when BCLK/2 is selected in the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0 to 1)

图14.12至图14.16显示了在EBCLK引脚输出选择位中选择BCLK2作为分频时进行的正常访问示例。

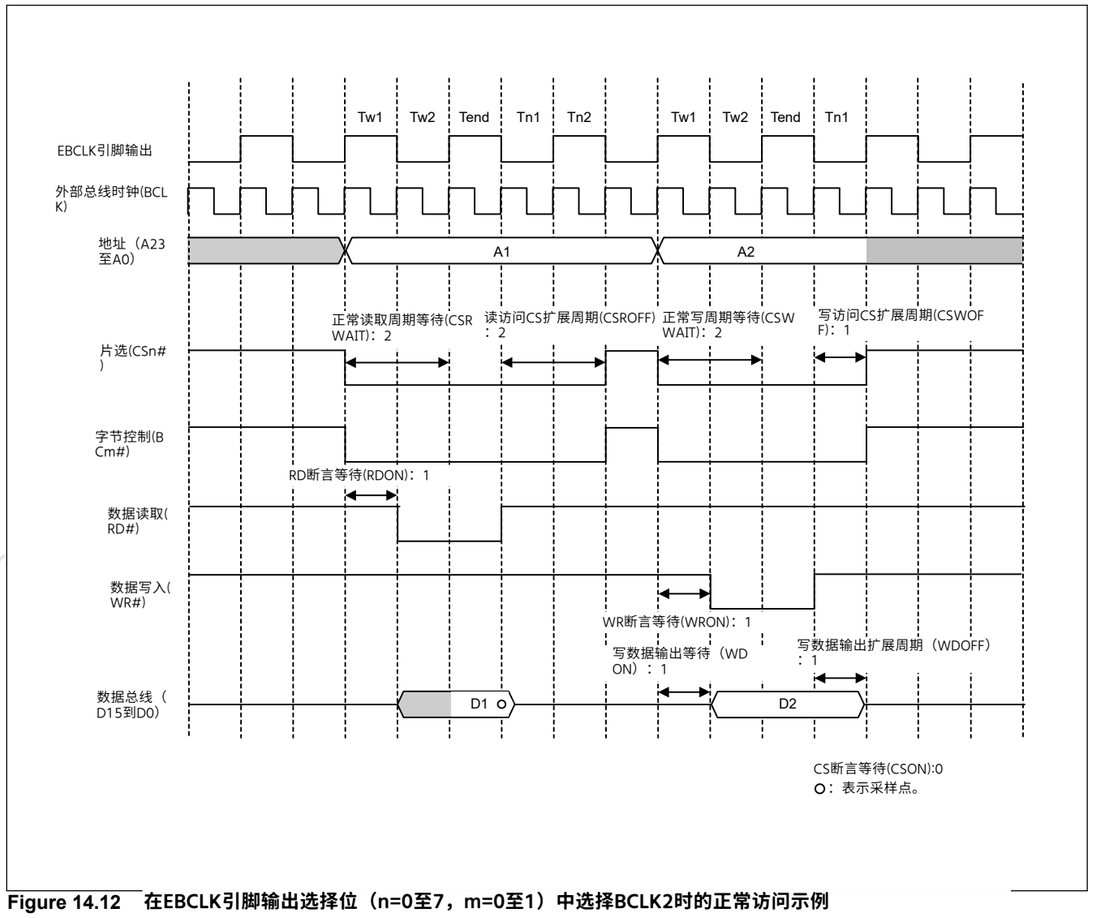


Figure 14.12 在EBCLK引脚输出选择位（n=0至7，m=0至1）中选择BCLK2时的正常访问示例

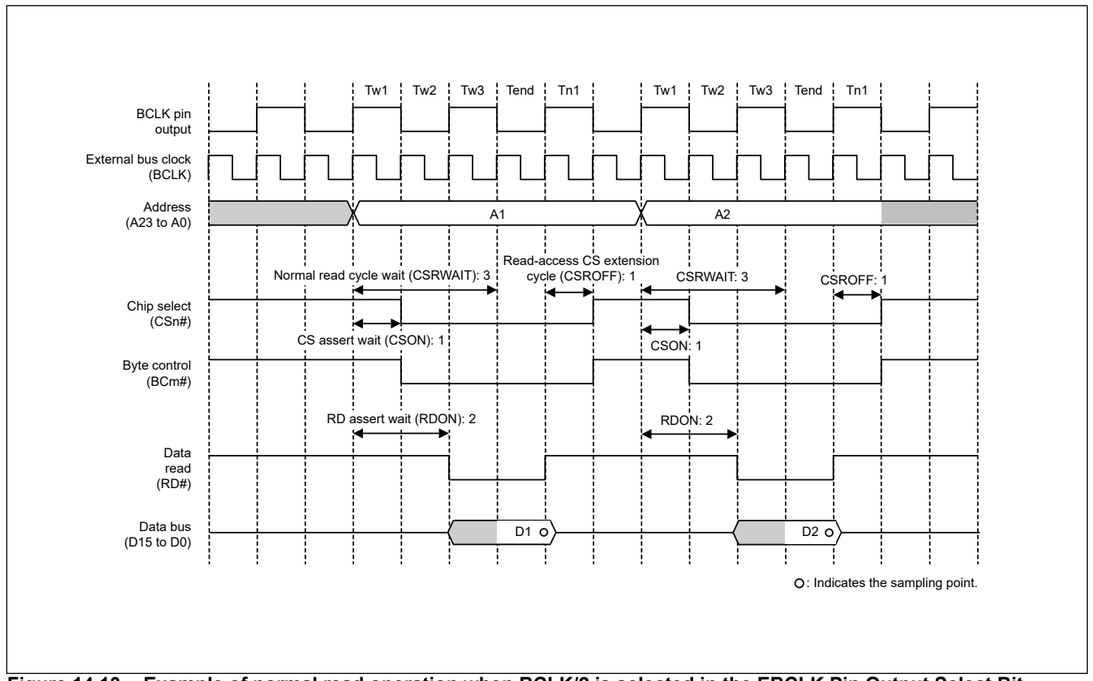


Figure 14.13 Example of normal read operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0 to 1)

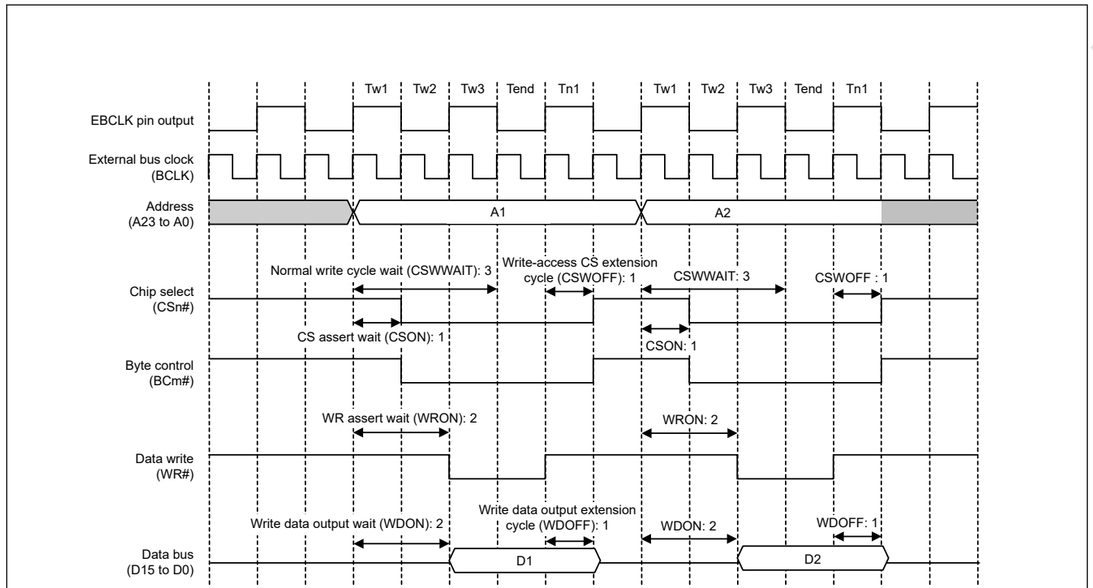


Figure 14.14 Example of normal write operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0 to 1)

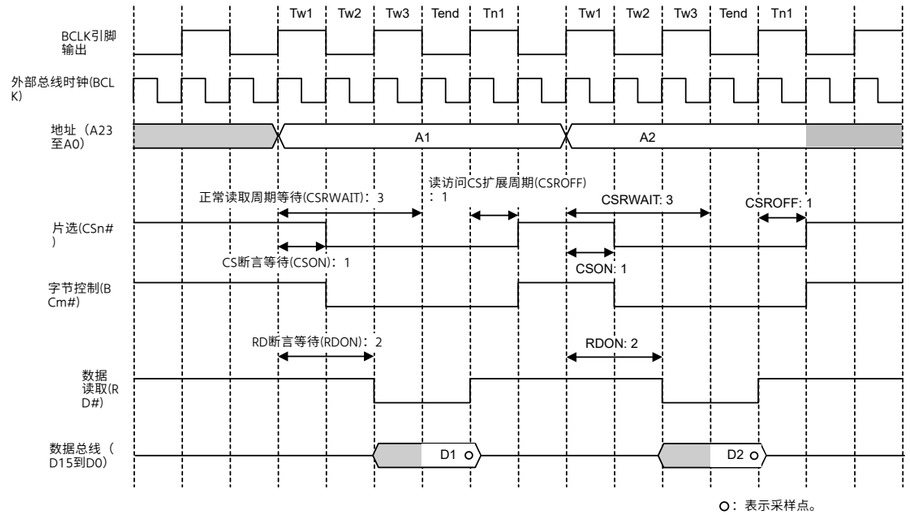


Figure 14.13 在EBCLK引脚输出选择位（n=0至7，m=0至1）中选择BCLK2时的正常读取操作示例

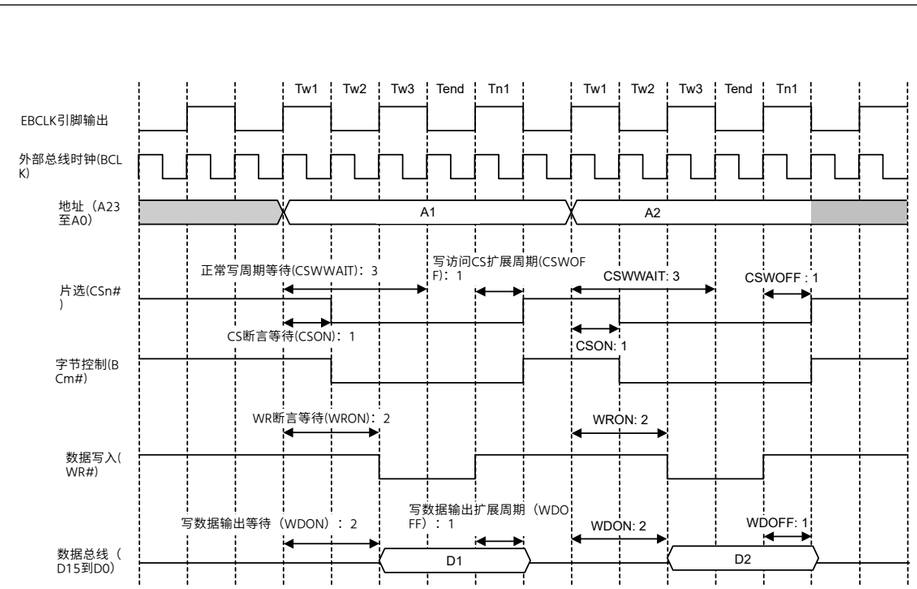


Figure 14.14 在EBCLK引脚输出选择中选择BCLK2时的正常写操作示例位（n=0到7，m=0到1）

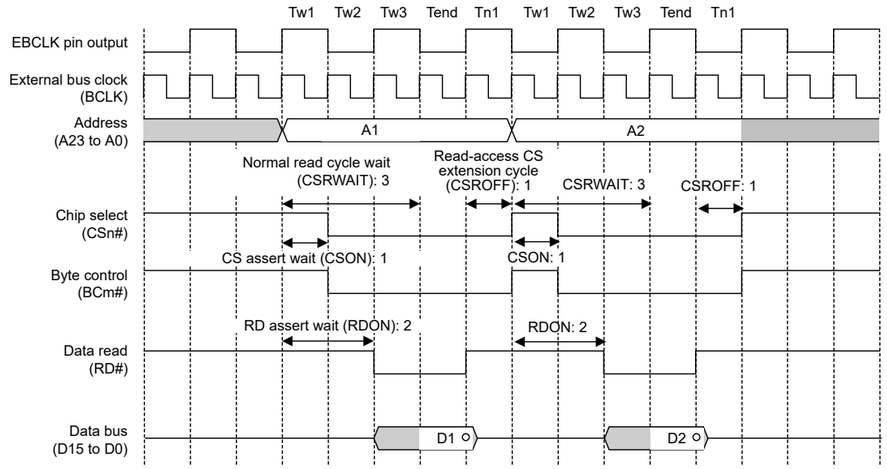


Figure 14.15 Example of normal read operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0 to 1)

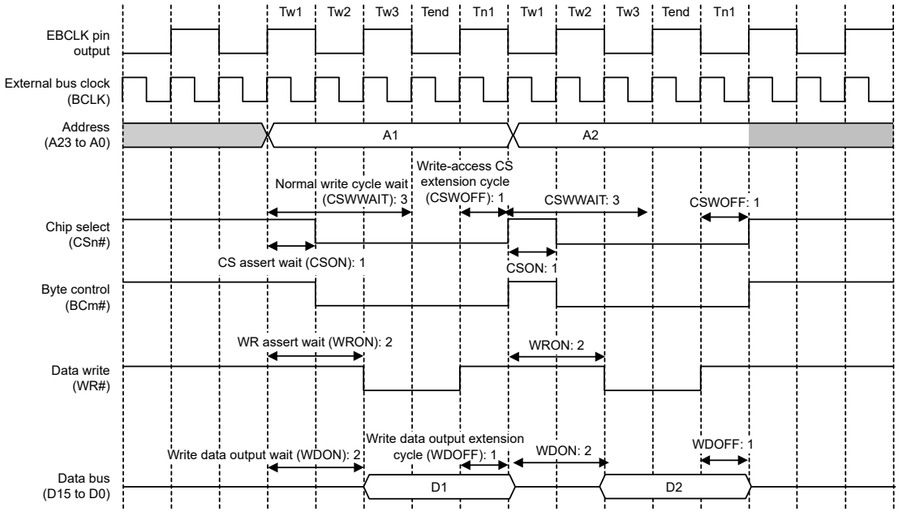


Figure 14.16 Example of normal write operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0 to 1)

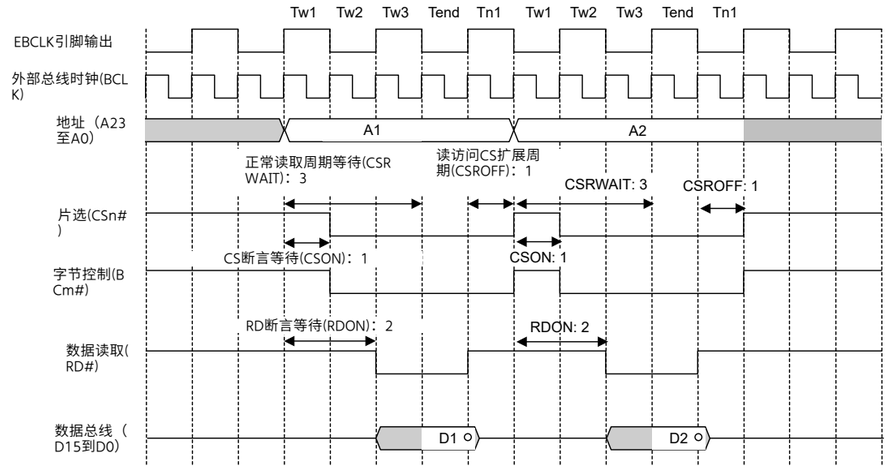


Figure 14.15 在EBCLK引脚输出选择位中选择BCLK2并且响应单个传输请求（n=0到7，m=0到1）生成两轮总线访问时的正常读取操作示例

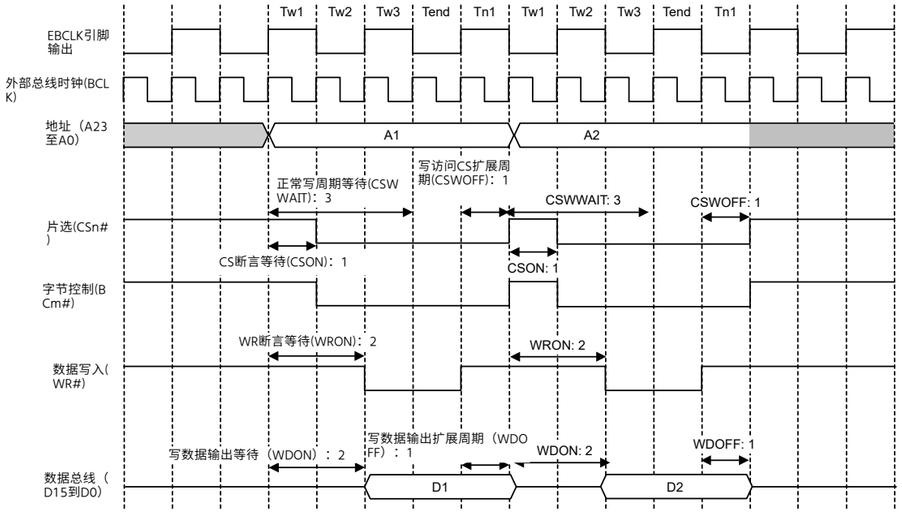
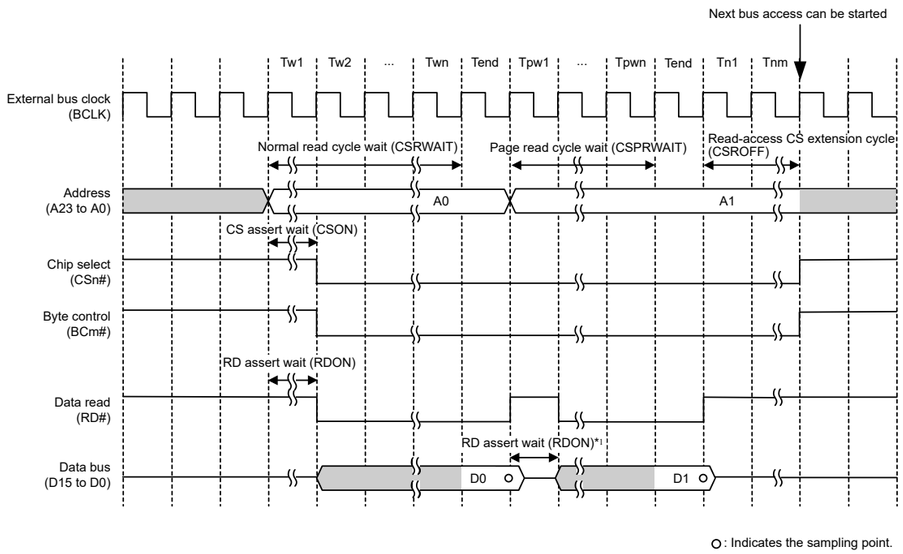


Figure 14.16 在EBCLK引脚输出选择中选择BCLK2时的正常写操作示例响应单个传输请求（n=0到7，m=0到1）产生位和两轮总线访问

(2) Page Access

When the PRENB and PWENB bits in CSnMOD are set to 1 to enable page-read and page-write access, the bus access for page access operations becomes page reading and writing. Page access can only occur when two or more rounds of external bus access are required for a single transfer request from the bus master. See Figure 14.3 to Figure 14.6 for the conditions under which page access occurs.

Figure 14.17 and Figure 14.18 show examples of page access operations.



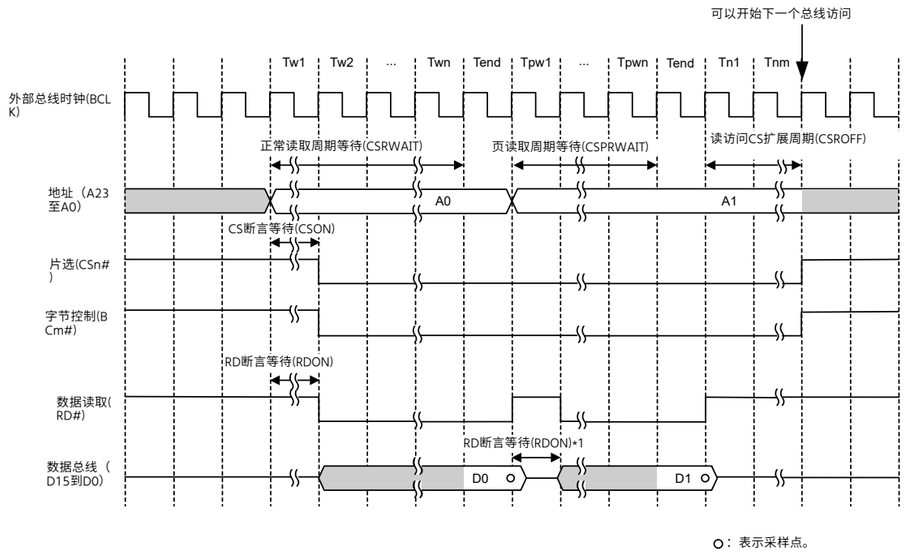
Note 1. The RD assert wait operation in the second and subsequent bus accesses depends on the page read access mode setting.

Figure 14.17 Page read access timing (n = 0 to 7, m = 0 to 1)

(2) 页面访问

当CSnMOD中的PRENB和PWENB位设置为1以启用页面读取和页面写入访问时，页面访问操作的总线访问变为页面读取和写入。只有当来自总线主机的单个传输请求需要两轮或多轮外部总线访问时，才会发生页面访问。有关页面访问发生的条件，请参见图14.3至图14.6。

图14.17和图14.18显示了页面访问操作的示例。



注1.第二次和后续总线访问中的RD断言等待操作取决于页面读取访问模式设置。

Figure 14.17 页读取访问时序（n=0到7，m=0到1）

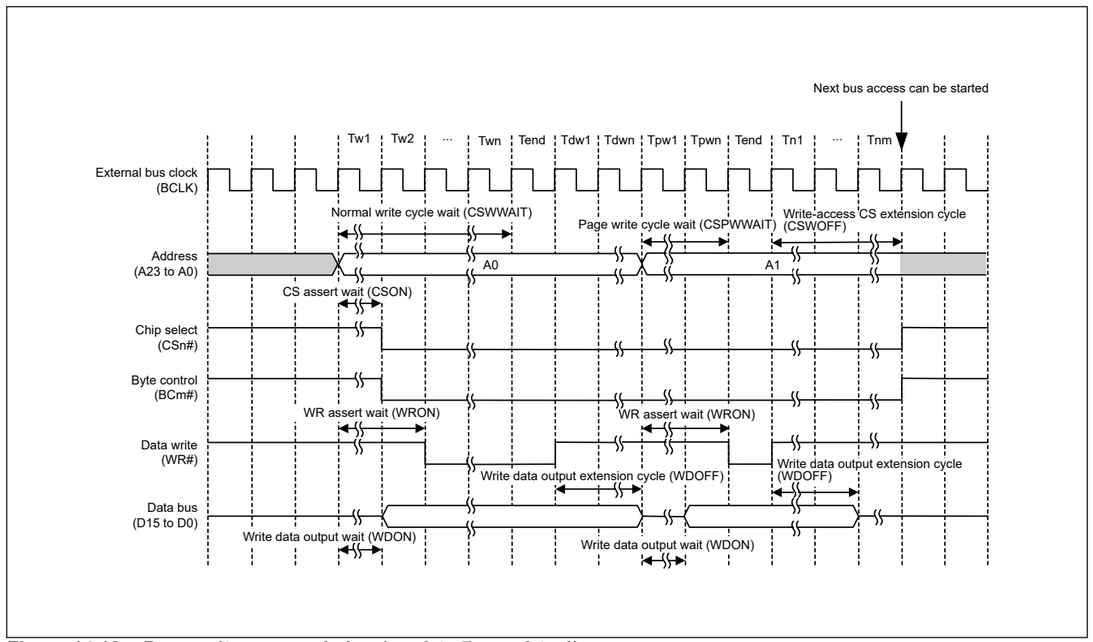


Figure 14.18 Page write access timing (n = 0 to 7, m = 0 to 1)

Figure 14.19 and Figure 14.20 show examples of operations for access to a 16-bit bus space in 32 bits. The values of the wait control registers shown in the figures are example settings. In your application, set the registers appropriately for the specifications of connected devices.

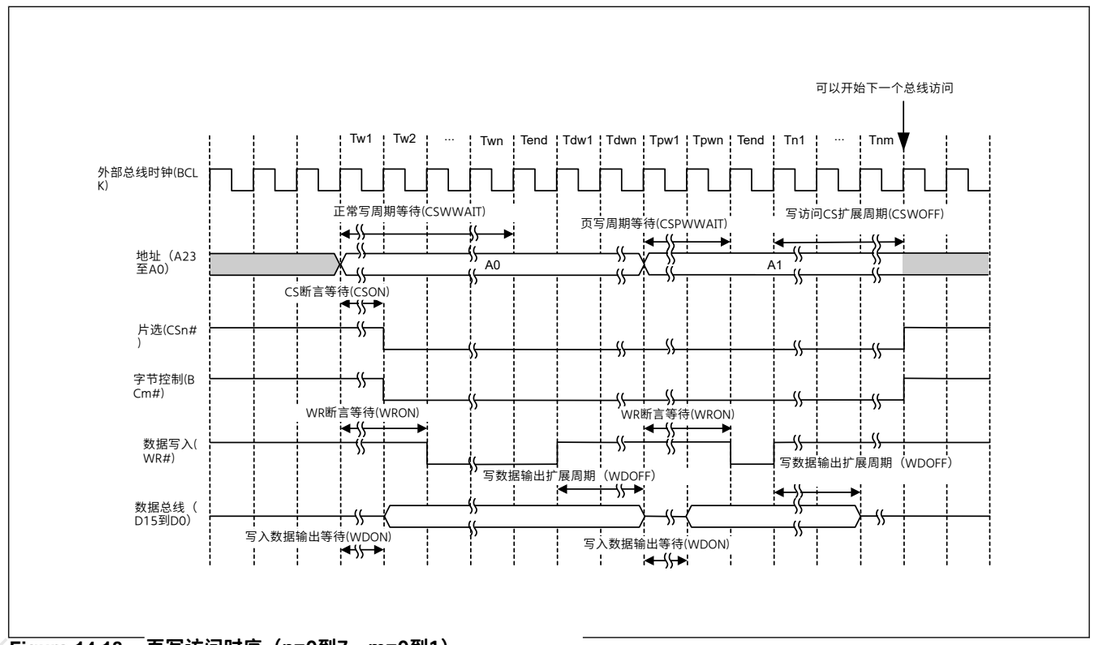


Figure 14.18 页写访问时序（n=0到7，m=0到1）

图14.19和图14.20显示了以32位访问16位总线空间的操作示例。图中所示的等待控制寄存器的值是示例设置。在您的应用程序中，根据连接设备的规格适当设置寄存器。

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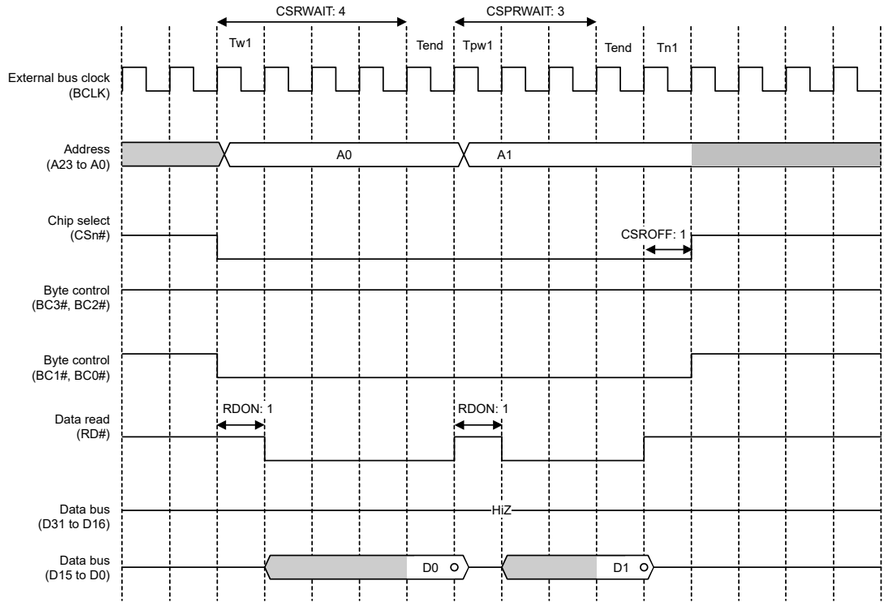

Figure 14.19 Example of page read access operation when 16-bit bus space is accessed in 32 bits (n = 0 to 7)

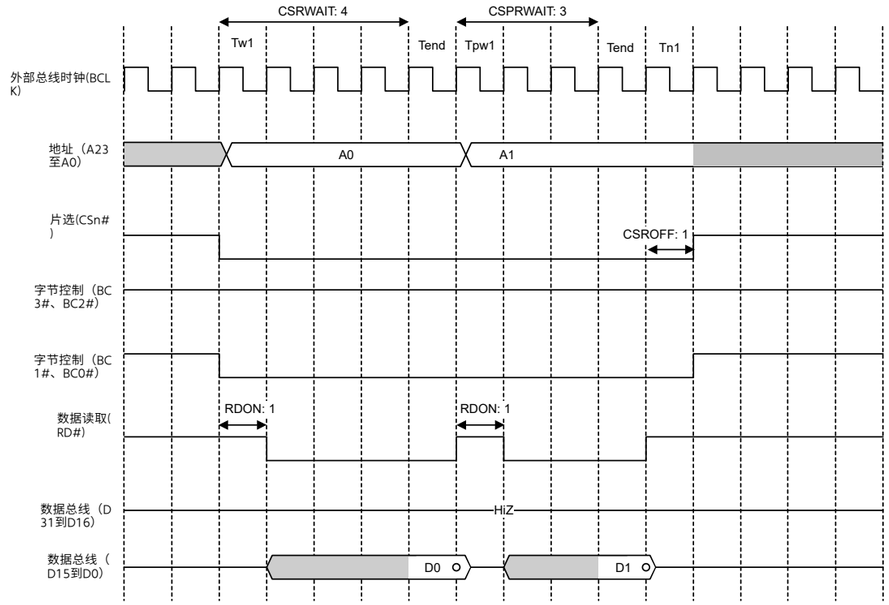

Figure 14.19 以32位（n=0到7）访问16位总线空间时的页读取访问操作示例

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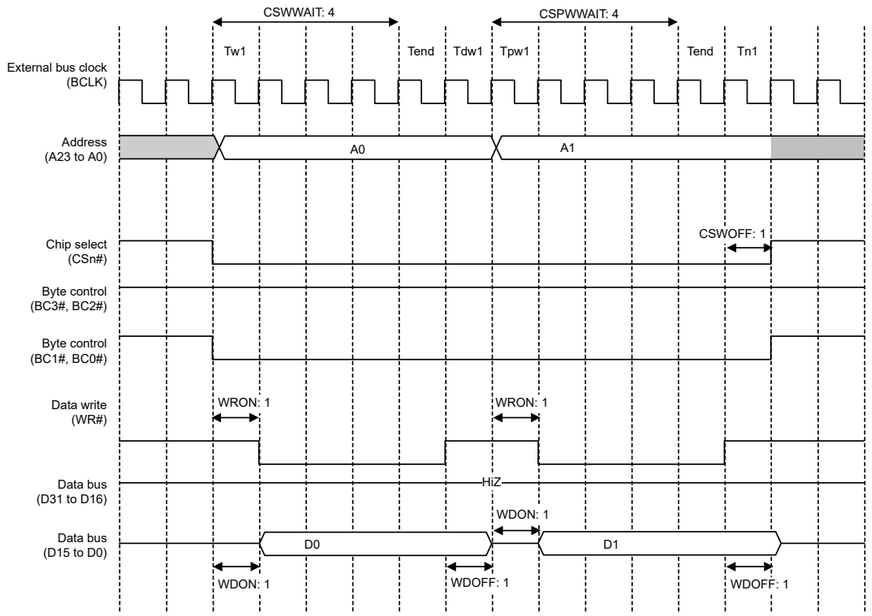

Figure 14.20 Example of page write access operation when 16-bit bus space is accessed in 32 bits in single-write strobe mode (n = 0 to 7)

Figure 14.21 and Figure 14.22 show examples of page access operations when BCLK/2 is selected as the frequency division in the EBCLK Pin Output Select bit.

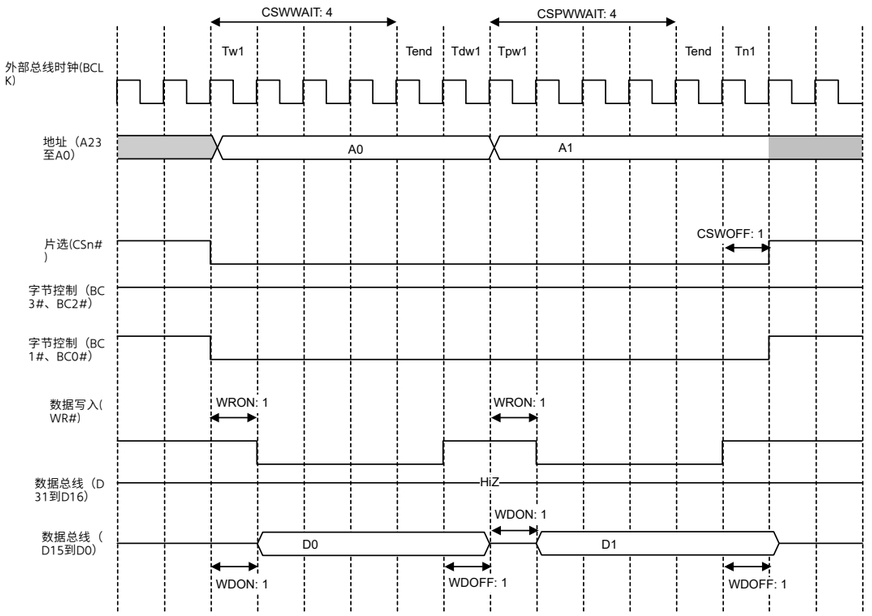

Figure 14.20 在单写选通模式（n=0到7）下以32位访问16位总线空间时的页写访问操作示例

图14.21和图14.22显示了在EBCLK引脚输出选择位中选择BCLK2作为分频时的页面访问操作示例。

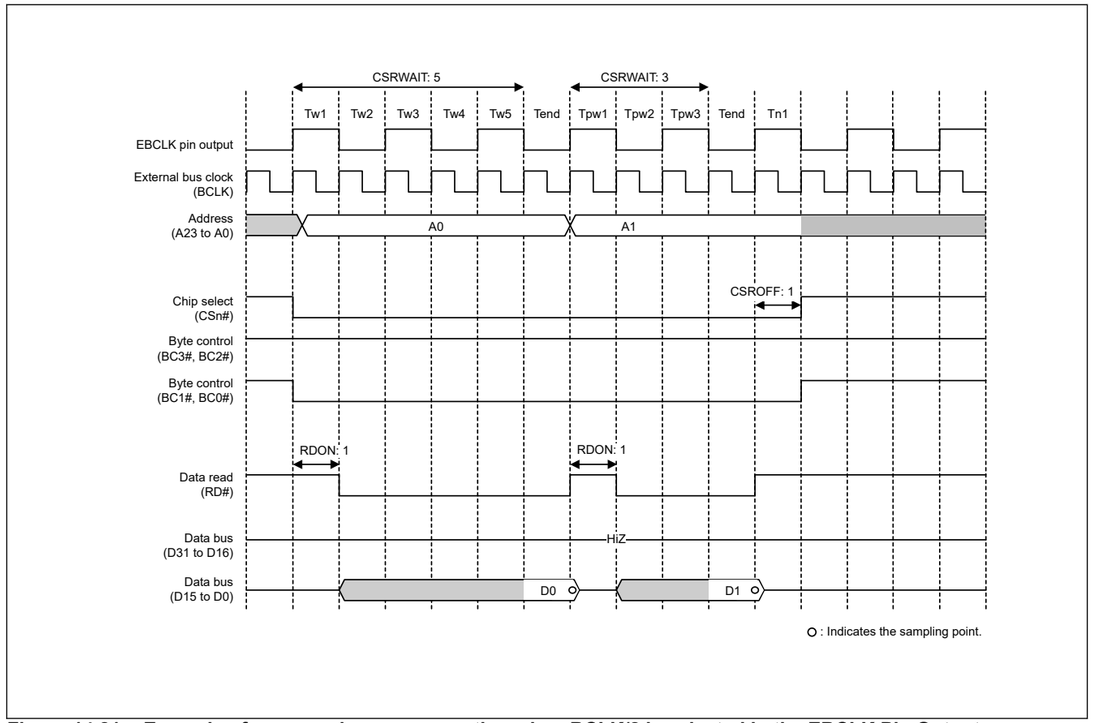

Figure 14.21 Example of page read access operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7)

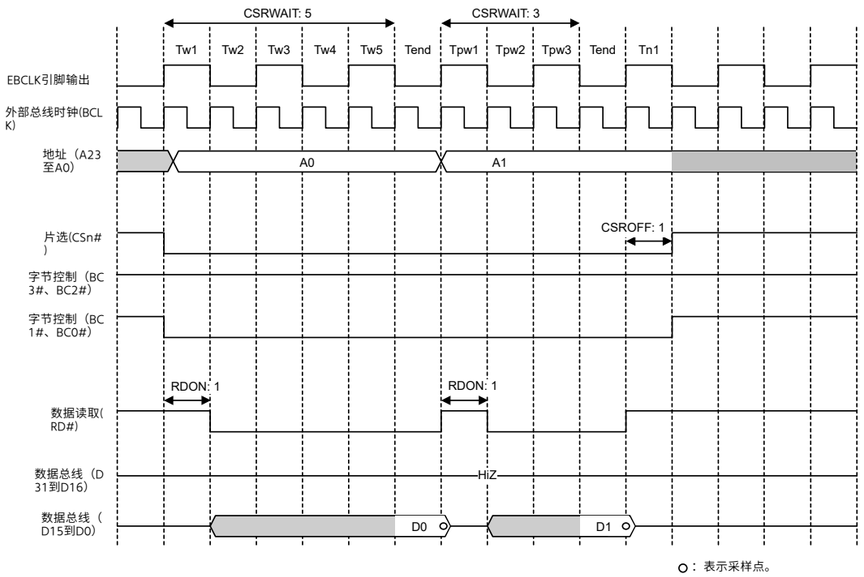

Figure 14.21 在EBCLK引脚输出中选择BCLK2时的页面读取访问操作示例
选择位并产生两轮总线访问以响应单个传输请求（n=0到7）

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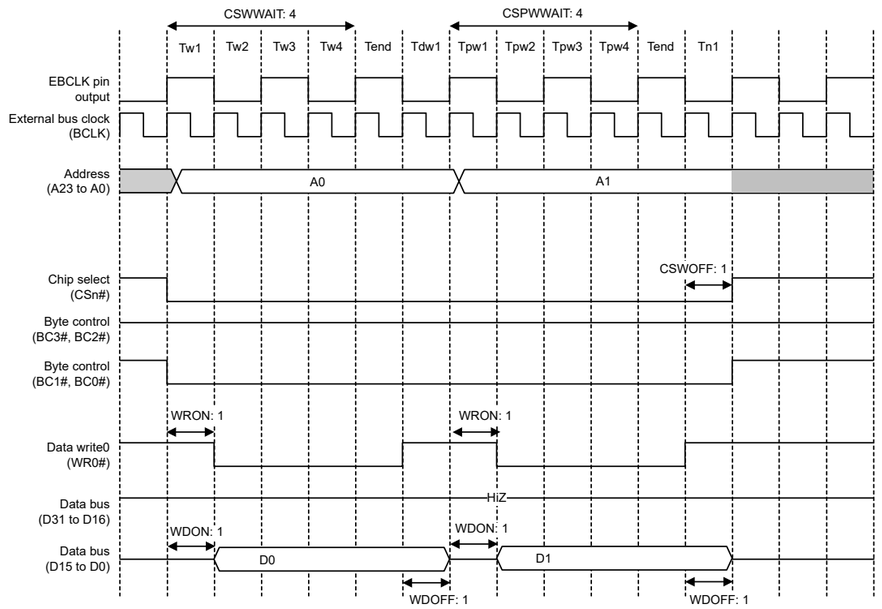


Figure 14.22 Example of page write access operation when BCLK/2 is selected in the EBCLK Pin Output Select Bit and two rounds of bus access are generated in response to a single transfer request in single-write strobe mode (n = 0 to 7)

14.5.2 Address/Data Multiplexed Bus

When the address/data multiplexed I/O interface select bit (MPXEN) in CSnCR is set to 1, addresses and data can be multiplexing input/output to/from the D15 to D0 pins in the corresponding area. Using this function enables direct connection of this MCU to peripherals of MCUs requiring address/data multiplexing. When 8-bit width is selected with the BSIZE[1:0] bits in CSnCR, D7 to D0 are multiplexed with A7 to A0. When 16-bit width is selected, D15 to D0 are multiplexed with A15 to A0. In the address/data multiplexed I/O space, accesses are controlled with the ALE, RD#, WRn#, and BCn# signals.

Byte strobe mode or single-write strobe mode is selectable in the same way as for a separate bus. However, with regard to the BCn# signals within the address cycle, the byte-control signal is output for the data being read or written.

During the address/data multiplexed I/O space access, after the number of wait cycles specified by the address cycle wait select bits (AWAIT[1:0]) in CSnWCR2 is inserted in the address output cycle, data access is performed.

Ta1 to Tan (Address Cycle Wait):

The period Ta1 to Tan is valid only when the address/data multiplexed I/O space is specified. This period is the number of clock cycles from the start of external bus access to 1 cycle before the address latch (ALE) signal is negated. The number of cycles is selectable from 0 to 3. Addresses are output until the next cycle of ALE signal negation (address cycle). The timing of ALE signal is the same as that of CS# assertion. After the address cycle, a data cycle is started. CSnWCR1 and CSnWCR2 should be set so that an address cycle and a data cycle do not overlap.

Page access to the address/data multiplexed I/O space is invalid. When the PRENB or PWENB bit in CSnMOD is set to 1 to enable page-read or page-write access, these settings are ignored and normal read or write operation is performed.

Figure 14.23 to Figure 14.25 show examples of operations with the address/data multiplexed I/O interface.

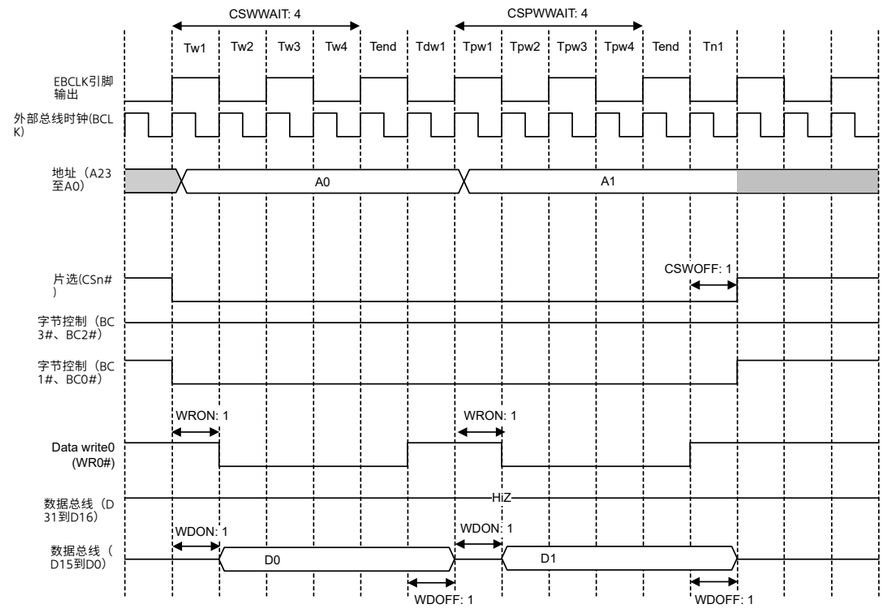


Figure 14.22 在EBCLK引脚输出中选择BCLK2时的页面写访问操作示例 在单写选通模式下（n=0到7）响应单次传输请求产生SelectBit和两轮总线访问

14.5.2 Address/Data Multiplexed Bus

当CSnCR中的地址数据复用IO接口选择位(MPXEN)设置为1时，地址和数据可以复用输入输出到相应区域的D15到D0引脚。使用此功能可以将此MCU直接连接到需要地址数据复用的MCU外设。当使用CSnCR中的BSIZE[1:0]位选择8位宽度时，D7到D0与A7到A0复用。When16-bitwidthisselected D15toD0aremultiplexedwithA15toA0.在地址数据复用IO空间中，访问由ALE、RD#、WRn#和BCn#信号控制。

字节选通模式或单写选通模式可以以与单独总线相同的方式进行选择。然而，对于地址周期内的BCn#信号，字节控制 信号被输出用于正在读取或写入的数据。

在地址数据复用IO空间访问期间，在地址输出周期插入CSnWCR2中的地址周期等待选择位（AWAIT[1:0]）指定的等待周期数后，执行数据访问。

Ta1到Tan（地址周期等待）：

只有在指定地址数据复用IO空间时，周期Ta1到Tan才有效。该周期是从外部总线访问开始到地址锁存(ALE)信号被否定之前的1个周期的时钟周期数。周期数可以从0到3选择。地址输出到ALE信号否定的下一个周期（地址周期）。ALE信号的时序与CS#断言的时序相同。在地址周期之后，开始一个数据周期。CSnWCR1和CSnWCR2应设置为地址周期和数据周期不重叠。

页访问地址数据复用的IO空间是无效的。当CSnMOD中的PRENB或PWENB位设置为1以启用页面读取或页面写入访问时，这些设置将被忽略并执行正常的读取或写入操作。

图14.23至图14.25显示了地址数据复用IO接口的操作示例。

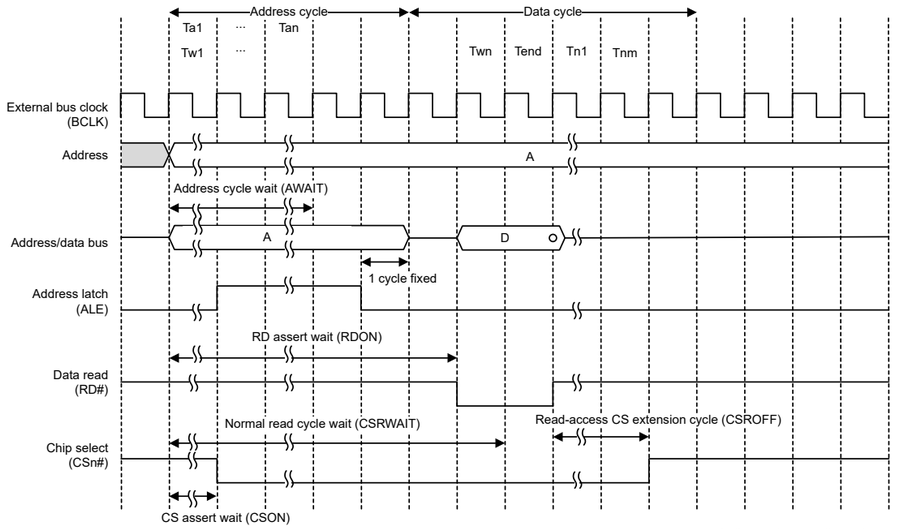


Figure 14.23 Example of read access operation with address/data multiplexed I/O interface (n = 0 to 7)

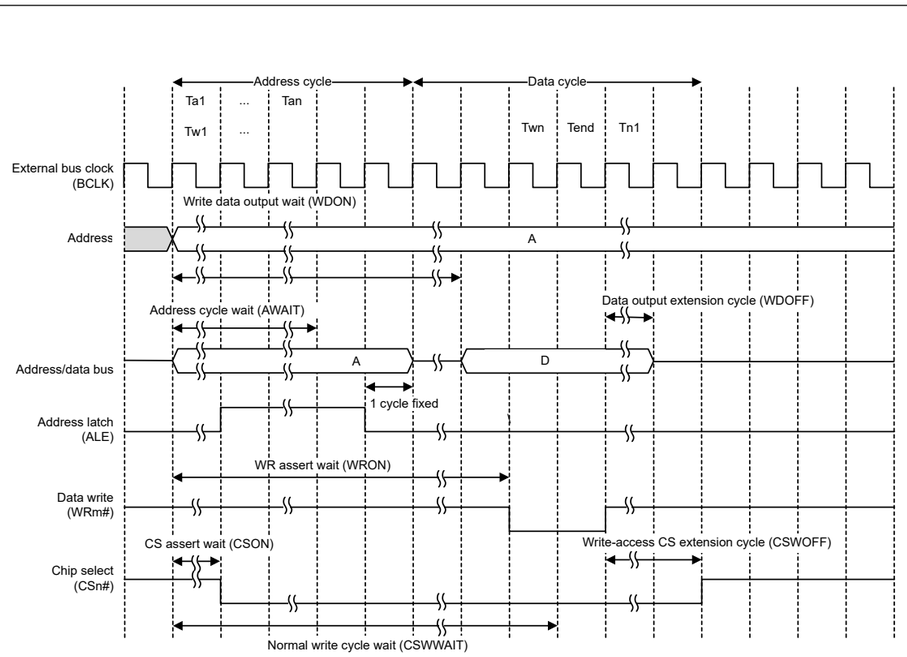


Figure 14.24 Example of write access operation with address/data multiplexed I/O interface (m = 0, 1)

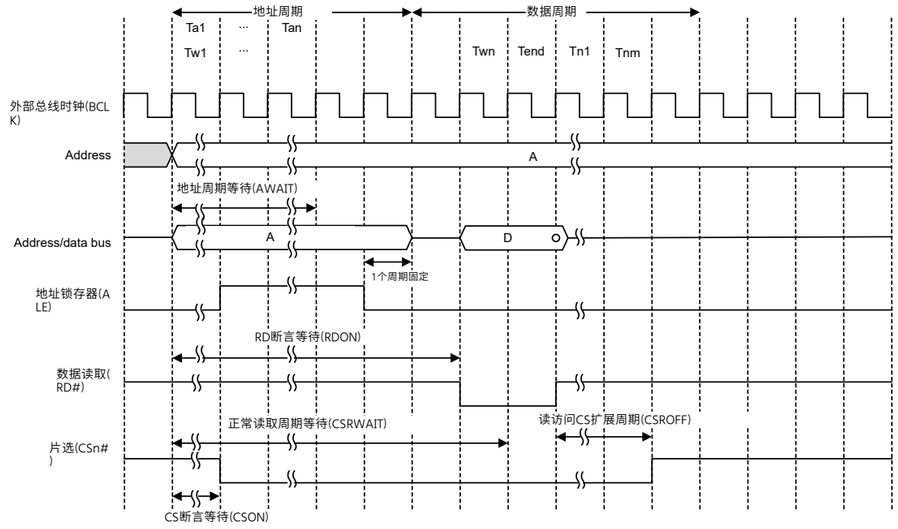


Figure 14.23 地址数据复用IO接口（n=0到7）的读访问操作示例

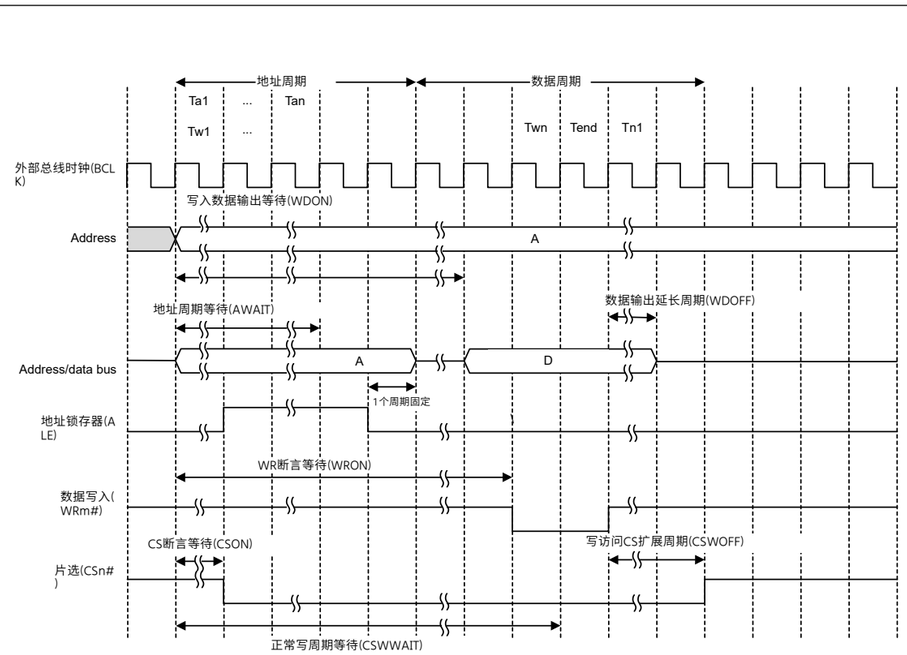


Figure 14.24 地址数据复用IO接口的写访问操作示例(m=0 1)

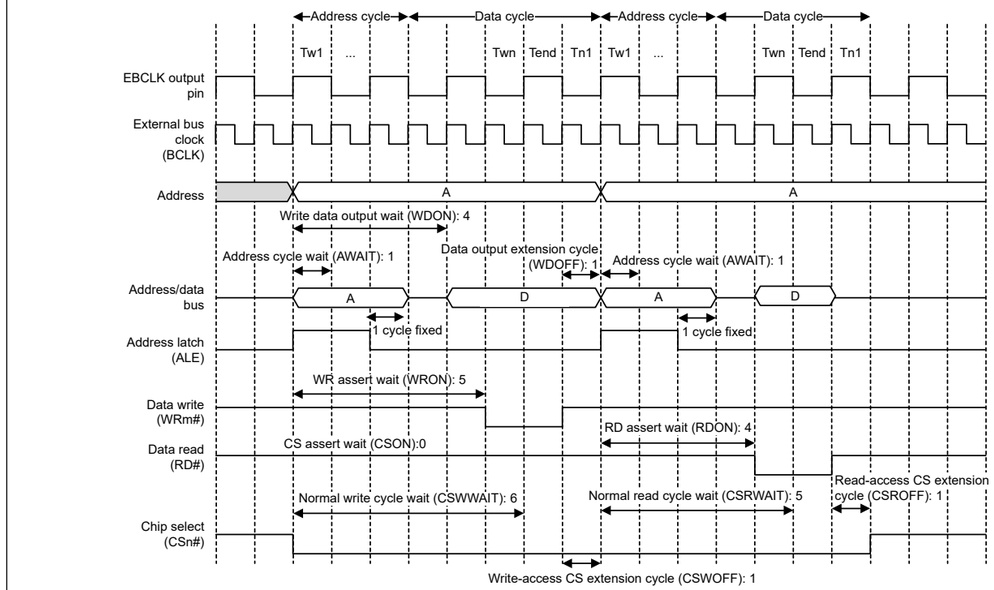


Figure 14.25 Example of bus timing with address/data multiplexed I/O interface (m = 0, 1)

14.5.3 External Wait Function

Wait cycles can be extended by the WAIT# signal beyond the length of normal access cycle wait specified in the CSRWAIT[4:0] and CSWWAIT[4:0] bits in CSnWCR1, and the page access cycle wait specified in the CSPRWAIT[2:0] and CSPWWAIT[2:0] bits in CSnWCR1.

All wait cycles specified in CSnWCR1 are inserted independently of the WAIT# signal.

When external wait is enabled (the EWENB bit = 1 in CSnMOD), wait cycles are inserted while the WAIT# signal is held low. When external wait is disabled (the EWENB bit = 0 in CSnMOD), the WAIT# signal has no effect.

(1) Normal Access

Sampling of the WAIT# signal begins on completion of the wait cycle (Tend) specified in CSnWCR1. The bus cycle is extended while the WAIT# signal is held low. The wait cycle ends (Tend) at the next cycle after the WAIT# signal goes high.

(2) Page Access

The first access operation is the same as the normal access operation. Sampling of the WAIT# signal begins on completion of the wait cycle (Tend) specified in the CSnWCR1 register. The bus cycle is extended while the WAIT# signal is held low. The wait cycle ends (Tend) at the next cycle after the WAIT# signal goes high.

With respect to the second and subsequent accesses, sampling of the WAIT# signal begins on completion of the wait cycle of the page access (Tend). The wait cycle of the page access is extended while the WAIT# signal is held low, and ends (Tend) at the next cycle after the WAIT# signal goes high.

Figure 14.26 to Figure 14.29 show examples of external wait insertion timing with the separate bus interface.

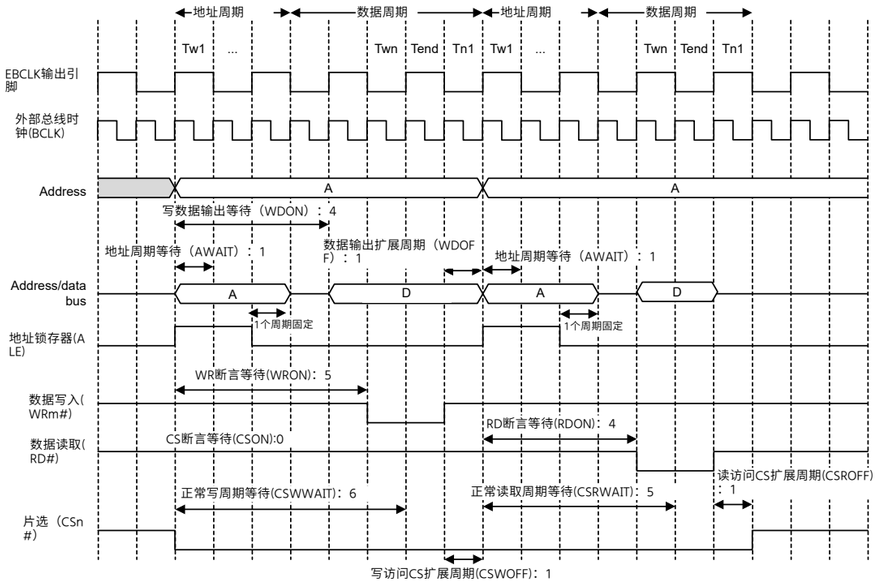


Figure 14.25 地址数据复用IO接口的总线时序示例(m=0 1)

14.5.3 外部等待功能

等待周期可以通过WAIT#信号延长到超出在指定的正常访问周期等待长度
CSnWCR1中的CSRWAIT[4:0]和CSWWAIT[4:0]位，以及在CSnWCR1中的CSPRWAIT[2:0]和CSWWWAIT[2:0]位中指定的页面访问周期等待。

CSnWCR1中指定的所有等待周期都是独立于WAIT#信号插入的。

当外部等待使能时（CSnMOD中的EWENB位=1），在WAIT#信号保持低电平时插入等待周期。当外部等待被禁用时（CSnMOD中的EWENB位=0），WAIT#信号无效。

(1) 正常访问

WAIT#信号的采样在CSnWCR1中指定的等待周期(Tend)完成时开始。当WAIT#信号保持低电平时，总线周期会延长。等待周期在WAIT#信号变高后的下一个周期结束(Tend)。

(2) 页面访问

第一次访问操作与正常访问操作相同。WAIT#信号的采样在CSnWCR1寄存器中指定的等待周期(Tend)完成时开始。当WAIT#信号保持低电平时，总线周期会延长。等待周期在WAIT#信号变高后的下一个周期结束(Tend)。

对于第二次和后续访问，WAIT#信号的采样在页面访问的等待周期（Tend）完成时开始。页访问的等待周期在WAIT#信号保持低电平时延长，并在WAIT#信号变为高电平后的下一个周期结束(Tend)。

图14.26至图14.29显示了使用独立总线接口的外部等待插入时序示例。

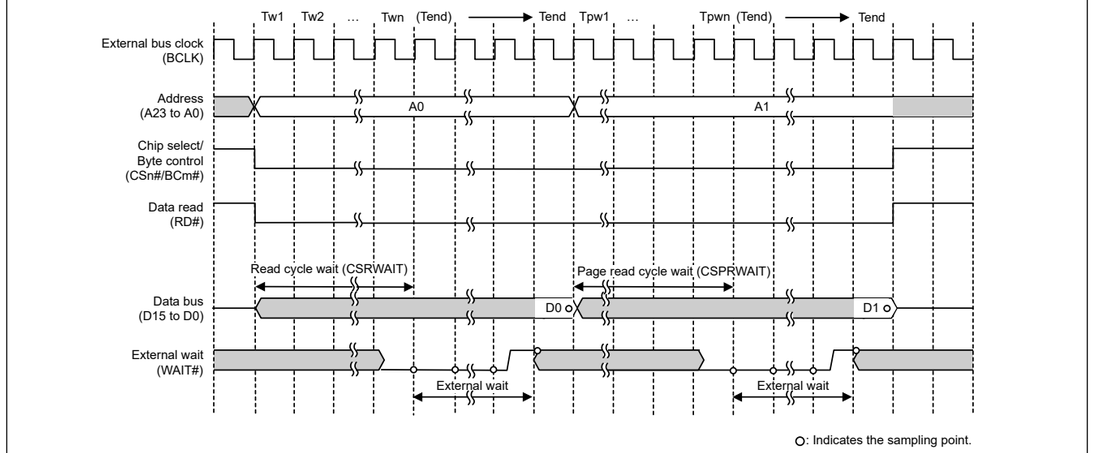


Figure 14.26 Example of external wait timing for page read access to 16-bit bus space when 1/1 BCLK is selected with the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0, 1)

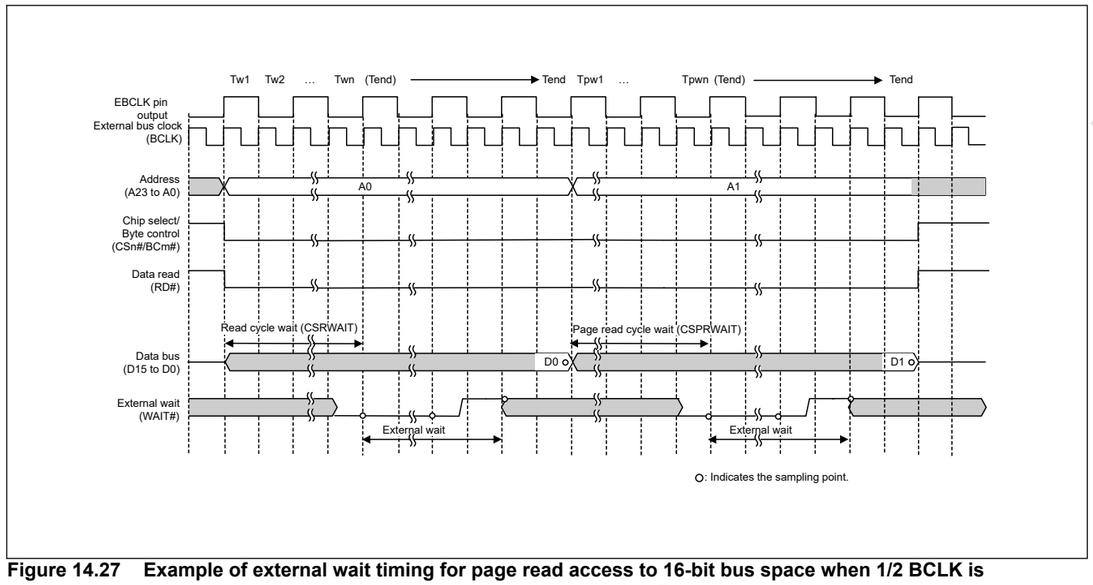


Figure 14.27 Example of external wait timing for page read access to 16-bit bus space when 1/2 BCLK is selected with the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0, 1)

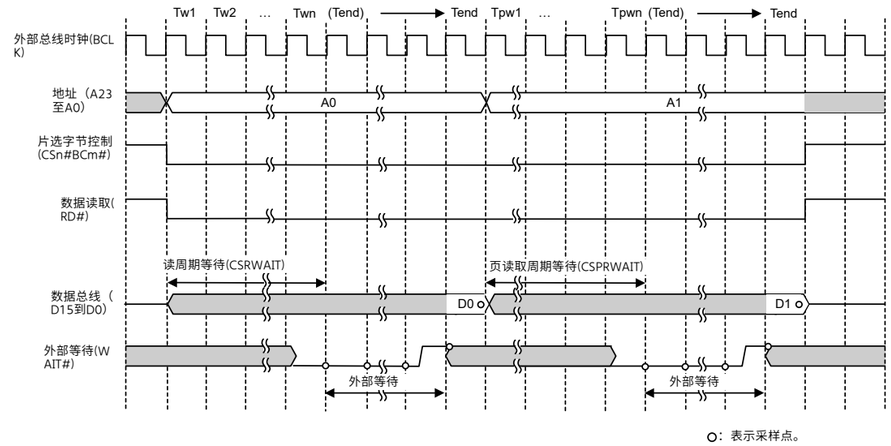


Figure 14.26 当使用EBCLK引脚输出选择位（n=0至7，m=0、1）选择11BCLK时，对16位总线空间进行页面读取访问的外部等待时序示例

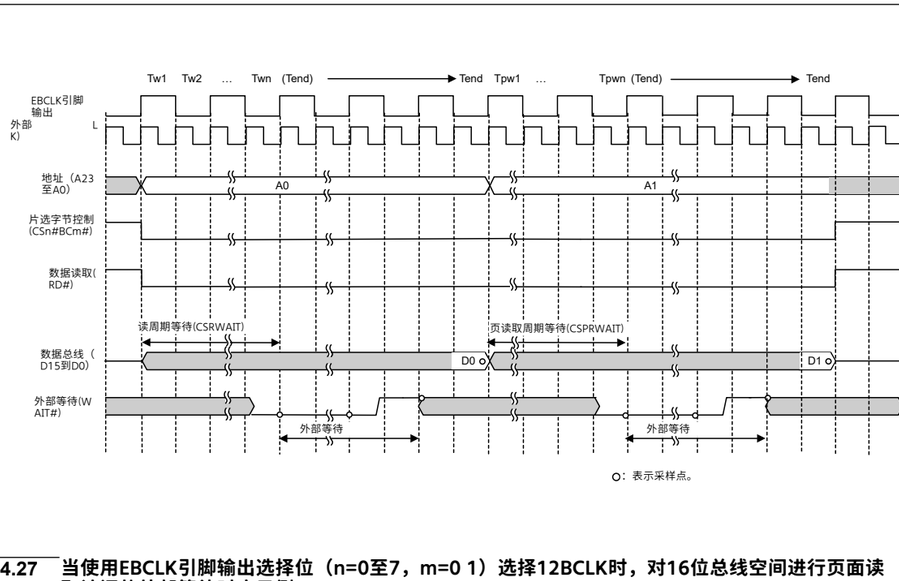


Figure 14.27 当使用EBCLK引脚输出选择位（n=0至7，m=0 1）选择12BCLK时，对16位总线空间进行页面读取访问的外部等待时序示例

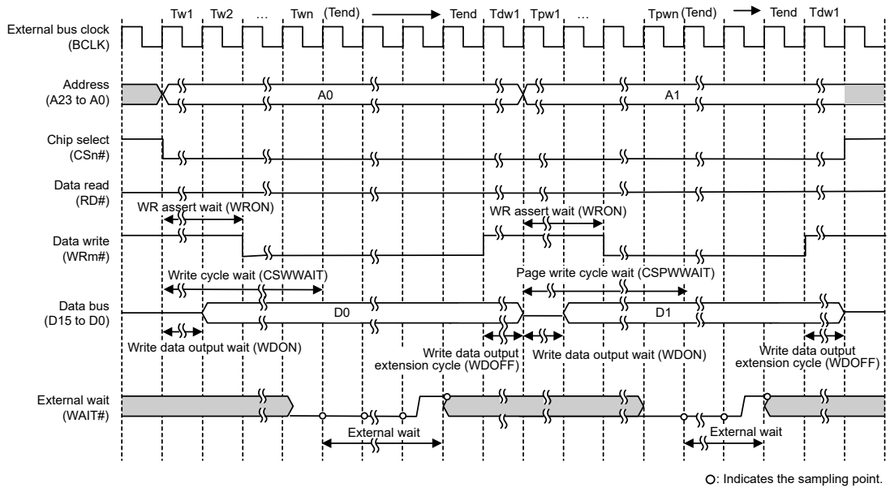


Figure 14.28 Example of external wait timing for page write access to 16-bit bus space in byte strobe mode when 1/1 BCLK is selected with the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0, 1)

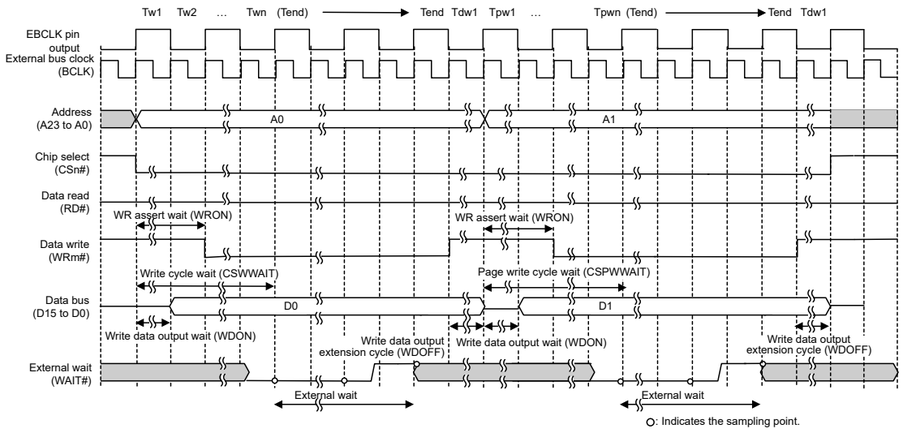


Figure 14.29 Example of external wait timing for page write access to 16-bit bus space in byte strobe mode when 1/2 BCLK is selected with the EBCLK Pin Output Select Bit (n = 0 to 7, m = 0, 1)

(3) Address/Data Multiplexed I/O Interface

In a data cycle with the address/data multiplexed I/O interface, programmed waits and pin waits using the WAIT pin can be inserted in the same way as that with the separate bus interface.

Address cycles are not affected by the wait control settings. Figure 14.30 shows an example of external wait insertion timing with the address/data multiplexed I/O interface.

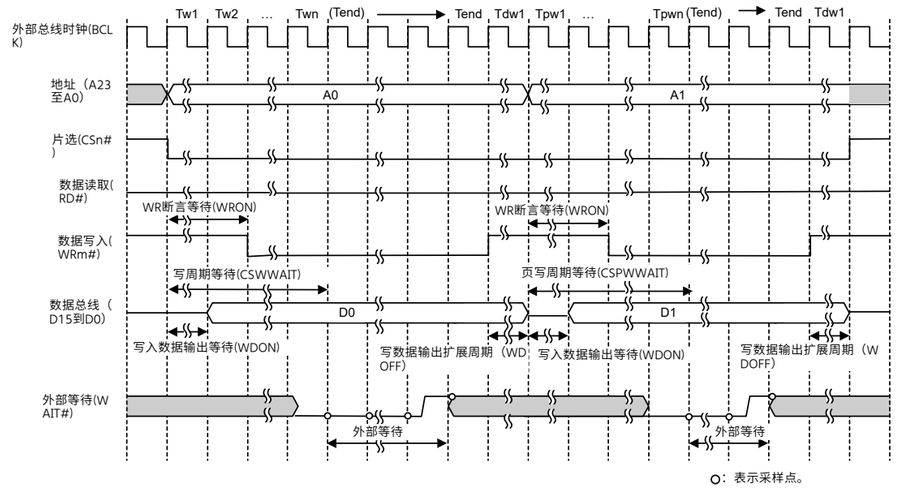


Figure 14.28 当使用EBCLK引脚输出选择位（n=0到7，m=0、1）选择11BCLK时，在字节选通模式下对16位总线空间进行页面写访问的外部等待时序示例

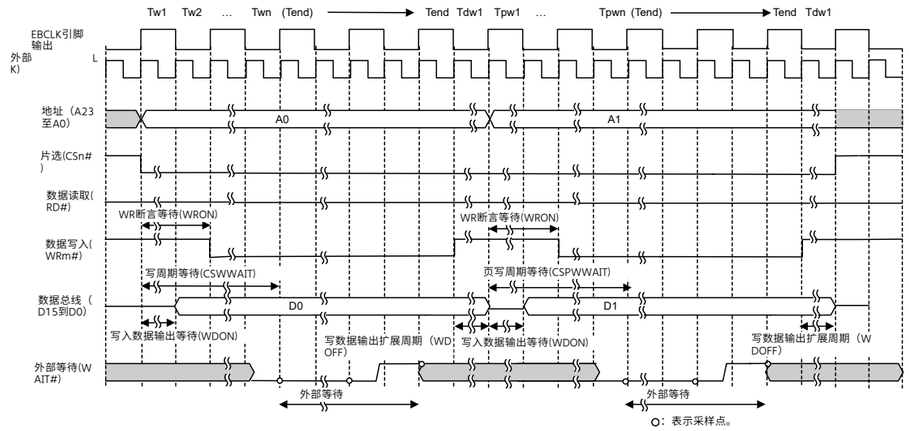


Figure 14.29 当使用EBCLK引脚输出选择位（n=0至7，m=0、1）选择12BCLK时，在字节选通模式下对16位总线空间进行页面写访问的外部等待时序示例

(3) Address/Data Multiplexed I/O Interface

在地址数据复用IO接口的数据周期中，编程等待和使用WAIT引脚的引脚等待可以以与单独总线接口相同的方式插入。

地址周期不受等待控制设置的影响。图14.30显示了地址数据复用IO接口的外部等待插入时序示例。

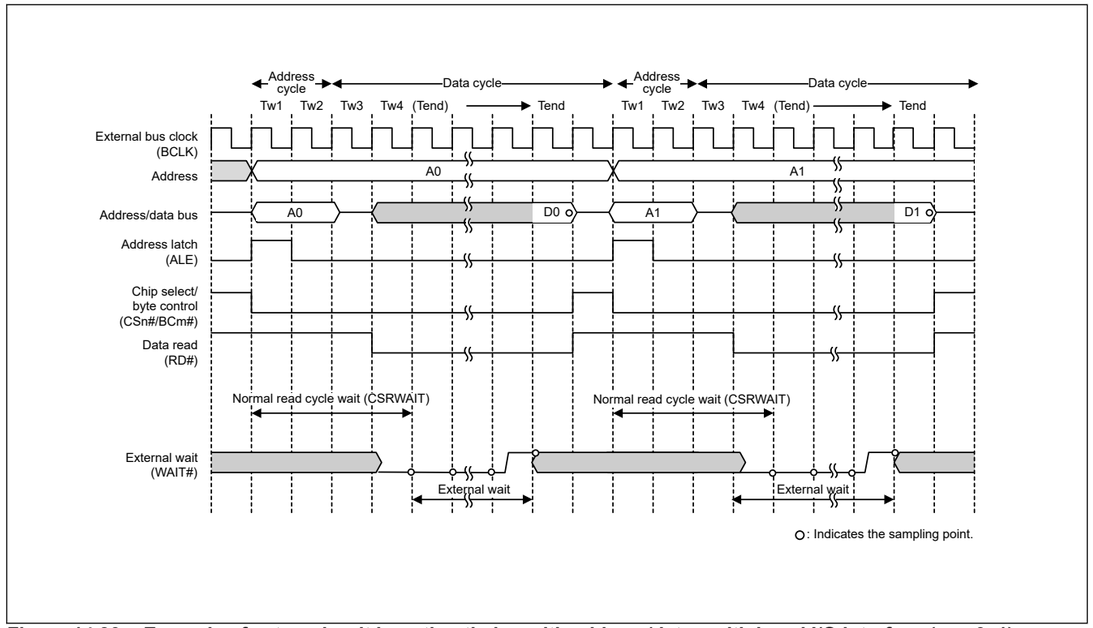


Figure 14.30 Example of external wait insertion timing with address/data multiplexed I/O interface (m = 0, 1)

14.5.4 Insertion of Recovery Cycles

Recovery cycles can be inserted between consecutive rounds of external bus access by setting the recovery cycle insertion enable bit in CSRECEN to 1.

The number of recovery cycles to be inserted after read cycles and write cycles can be separately set for each area using CSnREC. When the preceding bus cycle is a write access, the number of write recovery cycles should be set with the WRCV[3:0] bits for the area. When the preceding bus cycle is a read access, the number of read recovery cycles should be set with the RRCV[3:0] bits for the area. For example, when CS1 read access occurs after CS0 read access, the number of recovery cycles to be inserted between them is set by the RRCV[3:0] bits in CS0REC.

Recovery cycle insertion can be enabled or disabled with RCVENj (j = 0 to 7) in CSRECEN when the preceding bus access is a separate bus access, and with RCVENMj (j = 0 to 7) when the preceding bus access is an address/data multiplexed bus access.

Recovery cycles can be inserted on any of the following conditions:

- After a read access to the external bus, a read access is made to the external bus in the same area
- After a read access to the external bus, a read access is made to the external bus in a different area
- After a read access to the external bus, a write access is made to the external bus in the same area
- After a read access to the external bus, a write access is made to the external bus in a different area
- After a write access to the external bus, a read access is made to the external bus in the same area
- After a write access to the external bus, a read access is made to the external bus in a different area
- After a write access to the external bus, a write access is made to the external bus in the same area
- After a write access to the external bus, a write access is made to the external bus in a different area

The recovery cycle starts at the end of the preceding bus cycle, for example when the CSn# signal (n = 0 to 7) is negated. A high-level period of the CSn# signal is inserted for the specified recovery cycle period starting from this point.

In the fastest case, the CSn# signal for the next round of bus access is asserted immediately after the end of recovery cycles. Even if the next request for access to an external address space is generated during the recovery period, the next round of access over the external bus will start immediately after the end of recovery cycles.

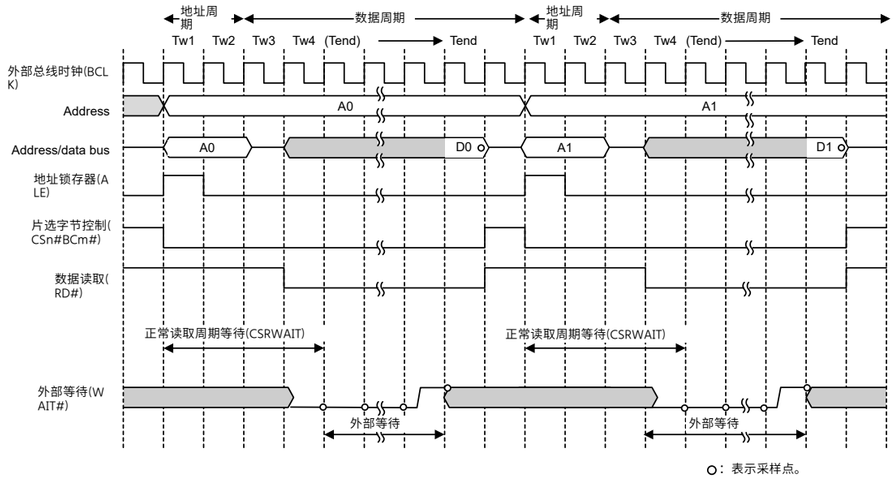


Figure 14.30 具有地址数据复用IO接口的外部等待插入时序示例(m=0 1)

14.5.4 恢复周期的插入

通过将CSRECEN中的恢复周期插入使能位设置为1，可以在连续的外部总线访问轮次之间插入恢复周期。

在读取周期和写入周期之后插入的恢复周期数可以使用以下方法为每个区域单独设置
CSnREC。当前一个总线周期是写访问时，写恢复周期的数量应该设置为
该区域的WRCV[3:0]位。当前一个总线周期是读访问时，读恢复周期的数量应该用该区域的RRCV[3:0]位设置。
例如，当CS1读访问发生在CS0读访问之后，在它们之间插入的恢复周期数由CS0REC中的RRCV[3:0]位设置。

当前面的总线访问是单独的总线访问时，可以使用CSRECEN中的RCVENj(j=0到7)启用或禁用恢复周期插入，当前面的总线访问是地址数据复用时，可以使用RCVENMj(j=0到7)启用或禁用恢复周期插入总线访问。

可以在以下任何条件下插入恢复周期：

- ●对外部总线进行读访问后，对同一区域的外部总线进行读访问
- ●对外部总线进行读访问后，对不同区域的外部总线进行读访问
- ●对外部总线进行读访问后，对同一区域的外部总线进行写访问
- ●对外部总线进行读访问后，对不同区域的外部总线进行写访问
- ●对外部总线进行写访问后，对同一区域的外部总线进行读访问
- ●对外部总线进行写访问后，对不同区域的外部总线进行读访问
- ●对外部总线进行写访问后，对同一区域的外部总线进行写访问
- ●对外部总线进行写访问后，对不同区域的外部总线进行写访问

恢复周期在前一个总线周期结束时开始，例如当CSn#信号（n=0到7）被否定时。从该点开始，在指定的恢复周期周期内插入CSn#信号的高电平周期。

在最快的情况下，下一轮总线访问的CSn#信号在恢复周期结束后立即置位。
即使在恢复期间产生了访问外部地址空间的下一个请求，通过外部总线的下一轮访问也将在恢复周期结束后立即开始。

When two or more external bus access cycles are required for a single transfer request from a bus master and the recovery cycle insertion condition is satisfied, recovery cycles are also inserted between these bus access cycles. However, when page read access is enabled (CSnMOD.PRENB = 1) or page write access is enabled (CSnMOD.PWENB = 1), recovery cycles are not inserted except after the last bus access cycle of the transfer even if the recovery cycle insertion condition is satisfied (see Figure 14.34).

Similarly, during normal accesses with page access enabled, recovery cycles are not inserted between bus access cycles but inserted only after the last bus access cycle of the transfer.

With the address/data multiplexed I/O interface, when the recovery cycle insertion condition is satisfied, recovery cycles are inserted between bus access cycles regardless of the page access enable setting.

Figure 14.31 to Figure 14.33 show examples of recovery cycle insertion with the separate bus interface.

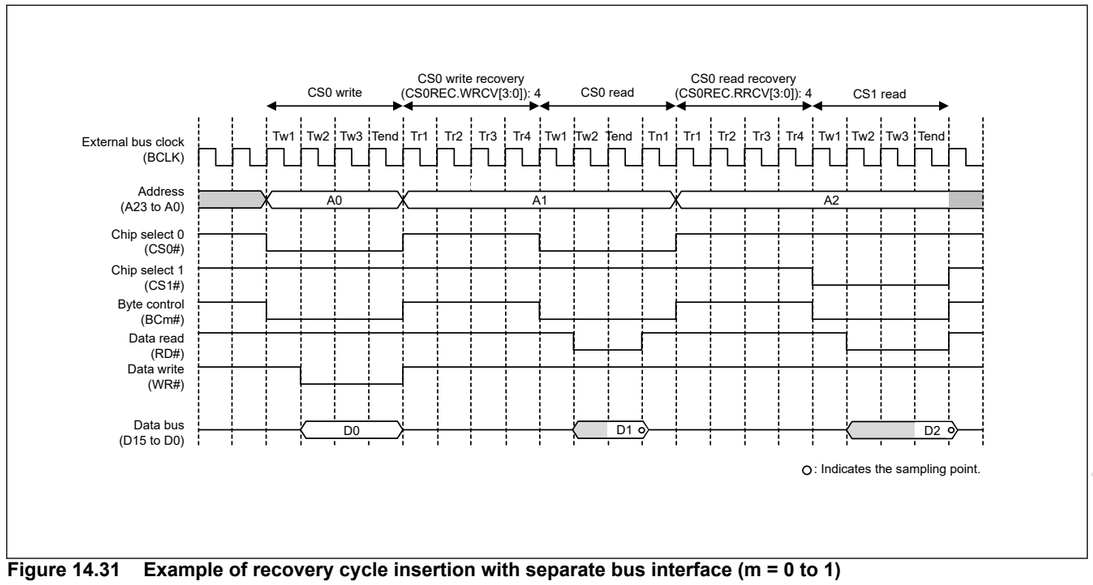


Figure 14.31 Example of recovery cycle insertion with separate bus interface (m = 0 to 1)

当来自总线主机的单个传输请求需要两个或多个外部总线访问周期并且恢复周期插入条件被满足时，恢复周期也在这些总线访问周期之间插入。但是，当启用页面读取访问(CSnMOD.PRENB=1)或启用页面写入访问(CSnMOD.PWENB=1)时，不会插入恢复周期，除非在传输的最后一个总线访问周期之后，即使恢复周期插入条件得到满足（见图14.34）。

类似地，在启用页面访问的正常访问期间，恢复周期不会插入总线访问周期之间，而是仅在传输的最后一个总线访问周期之后插入。

对于地址数据复用IO接口，当恢复周期插入条件满足时，无论页面访问使能设置如何，都会在总线访问周期之间插入恢复周期。

图14.31至图14.33显示了使用单独的总线接口插入恢复周期的示例。

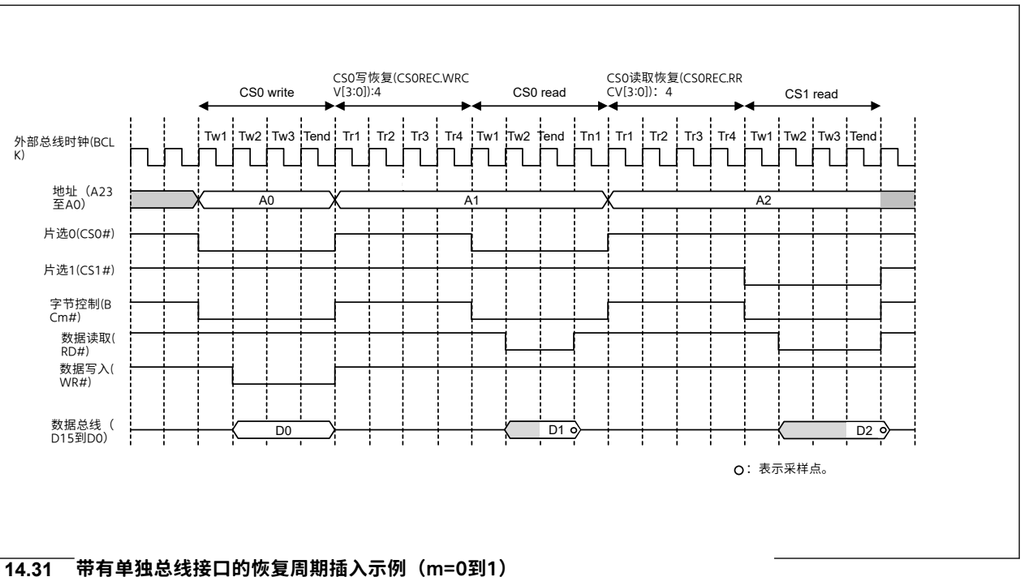


Figure 14.31 带有单独总线接口的恢复周期插入示例（m=0到1）

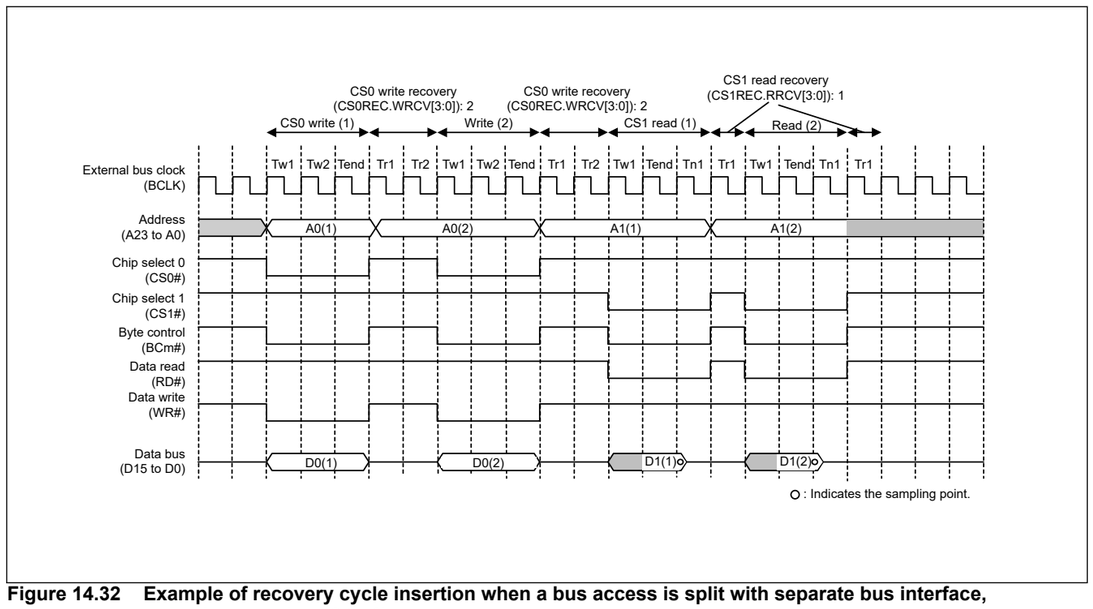


Figure 14.32 Example of recovery cycle insertion when a bus access is split with separate bus interface, normal access (m = 0 to 1)

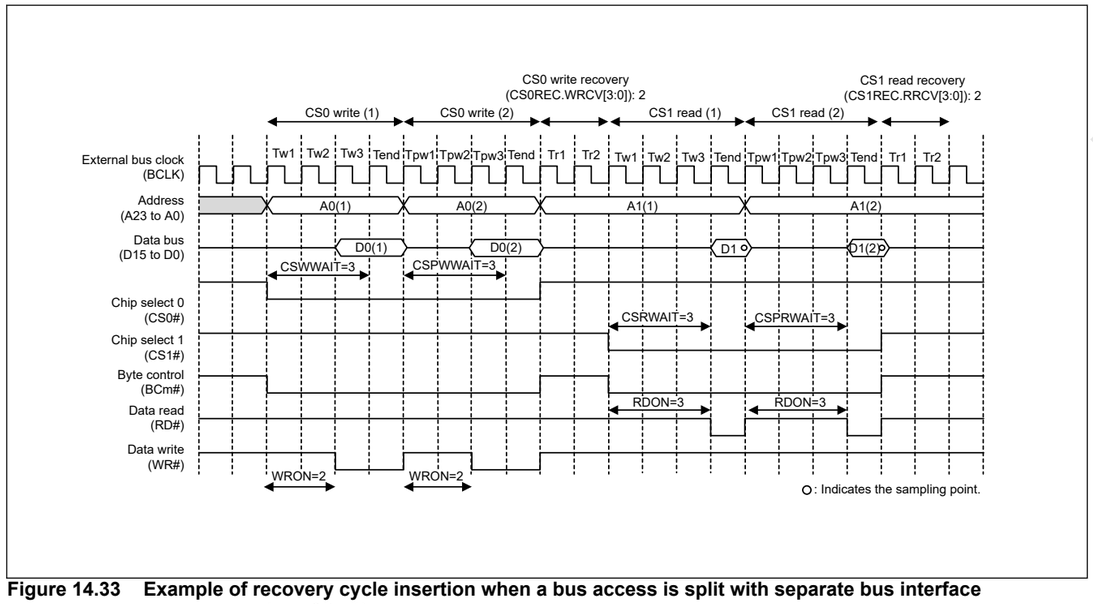


Figure 14.33 Example of recovery cycle insertion when a bus access is split with separate bus interface page access (m = 0 to 1)

Figure 14.34 shows examples of operations when the EBCLK pin output selection bits are set for frequency-division of BCLK by 2.

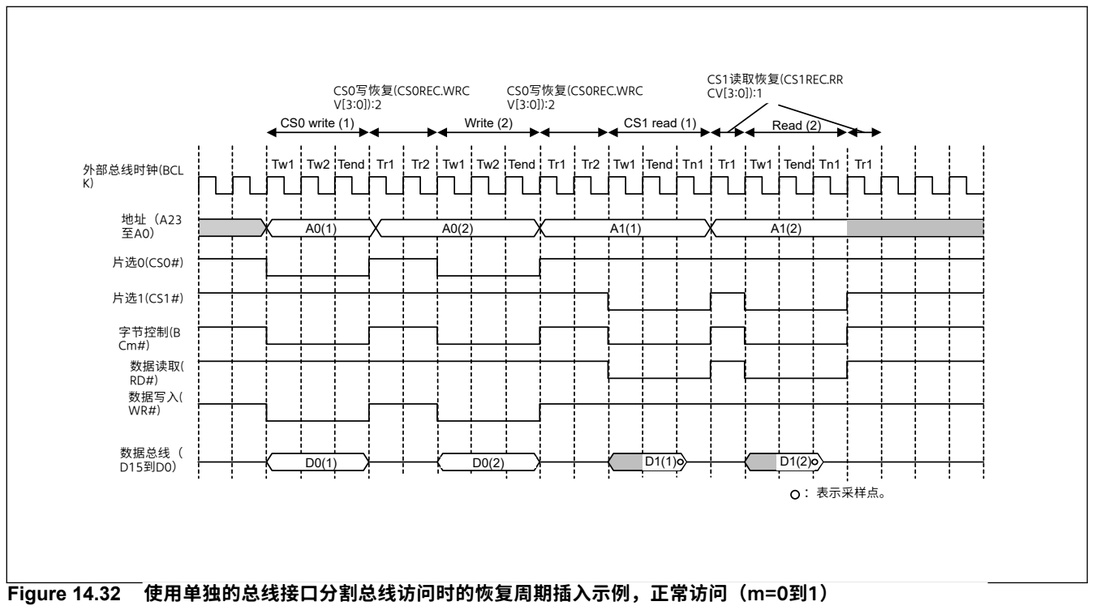


Figure 14.33 使用单独的总线接口分割总线访问时的恢复周期插入示例，正常访问（m=0到1）

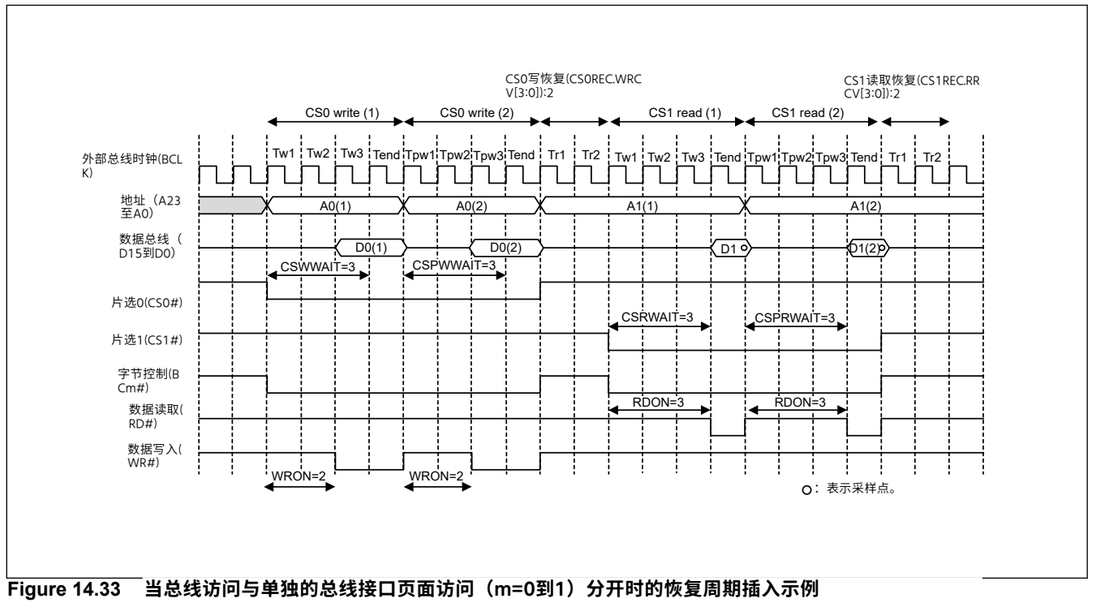


图14.34显示了将EBCLK引脚输出选择位设置为分频时的操作示例
BCLK by 2.

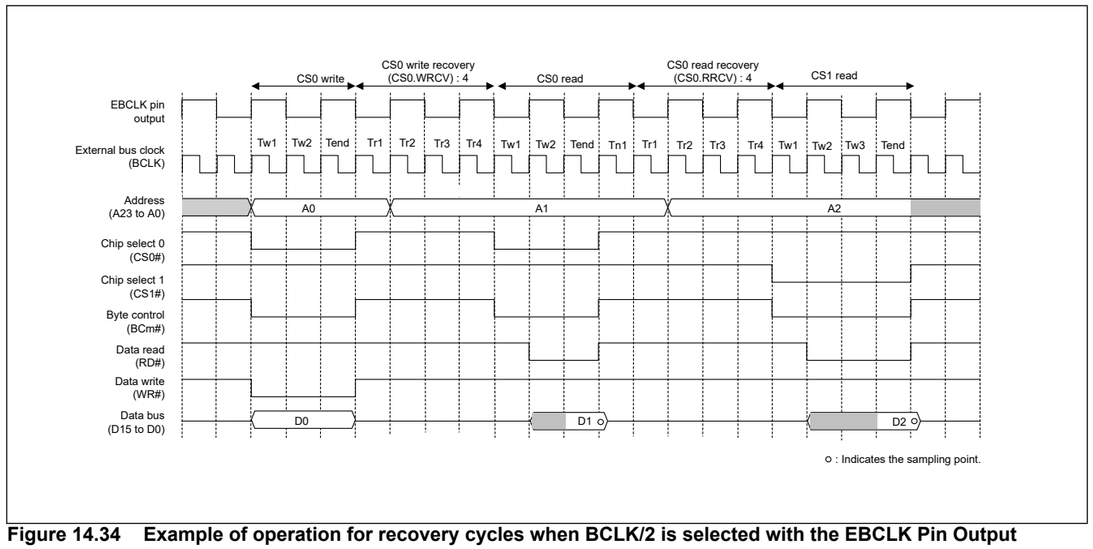


Figure 14.34 Example of operation for recovery cycles when BCLK/2 is selected with the EBCLK Pin Output Selection bits for normal access through a separate bus interface (m = 0 to 1)

With the address/data multiplexed I/O interface, recovery cycles are inserted in the same way as that with the separate bus interface. Figure 14.35 and Figure 14.36 show examples of recovery cycle insertion with the address/data multiplexed I/O interface.

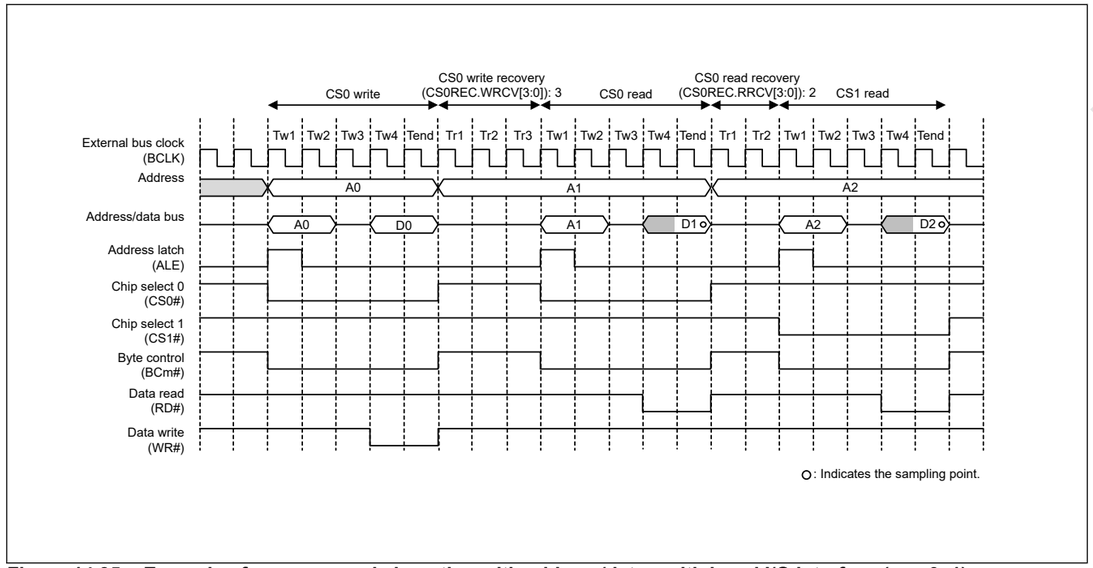


Figure 14.35 Example of recovery cycle insertion with address/data multiplexed I/O interface (m = 0, 1)

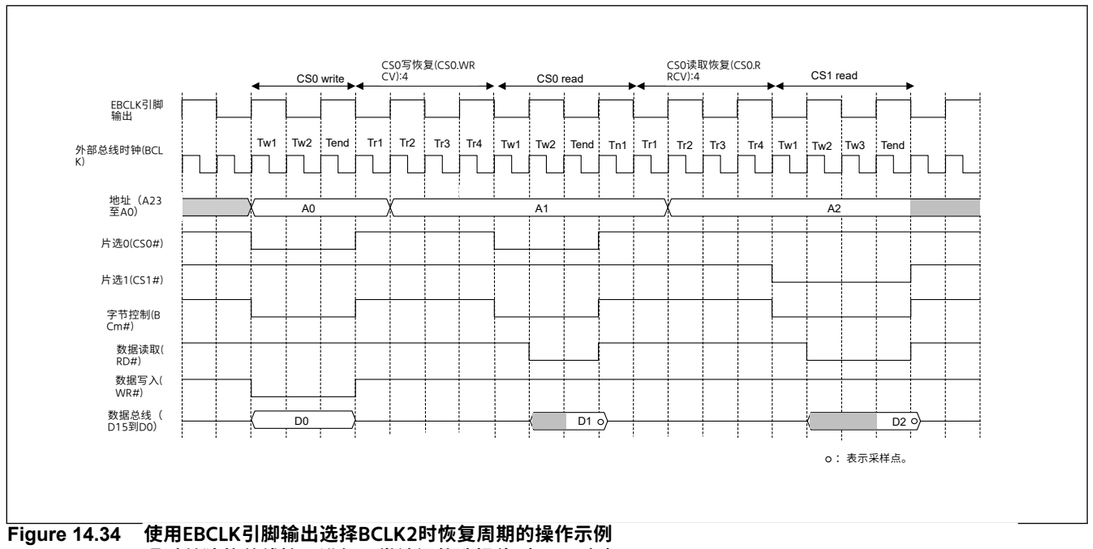


Figure 14.34 使用EBCLK引脚输出选择BCLK2时恢复周期的操作示例 通过单独的总线接口进行正常访问的选择位（m=0到1）

对于地址数据复用IO接口，恢复周期的插入方式与单独总线接口的插入方式相同。图14.35和图14.36显示了使用地址数据多路复用IO接口插入恢复周期的示例。

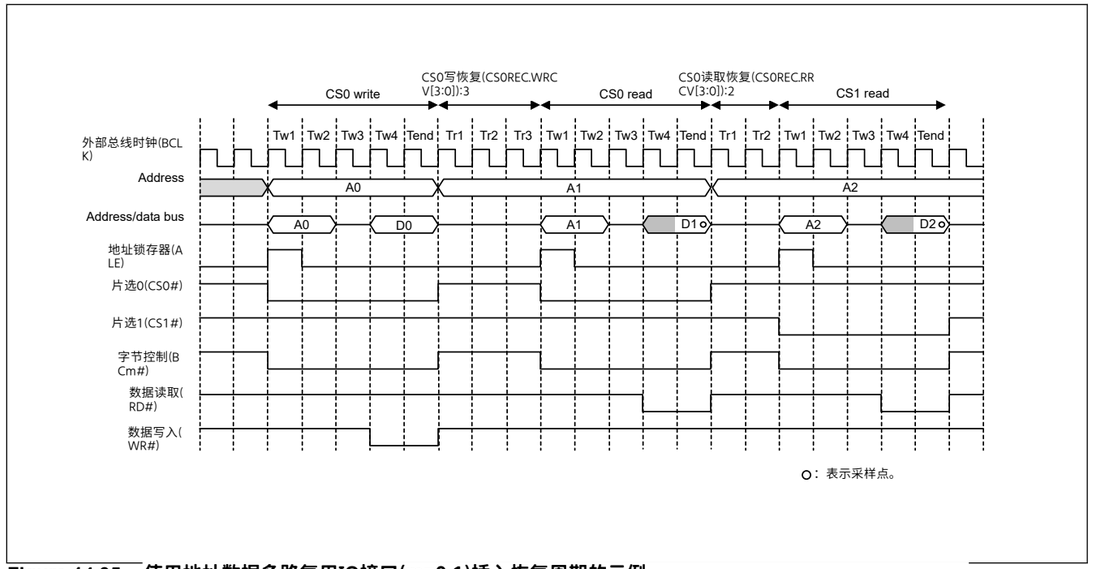


Figure 14.35 使用地址数据多路复用IO接口(m=0 1)插入恢复周期的示例

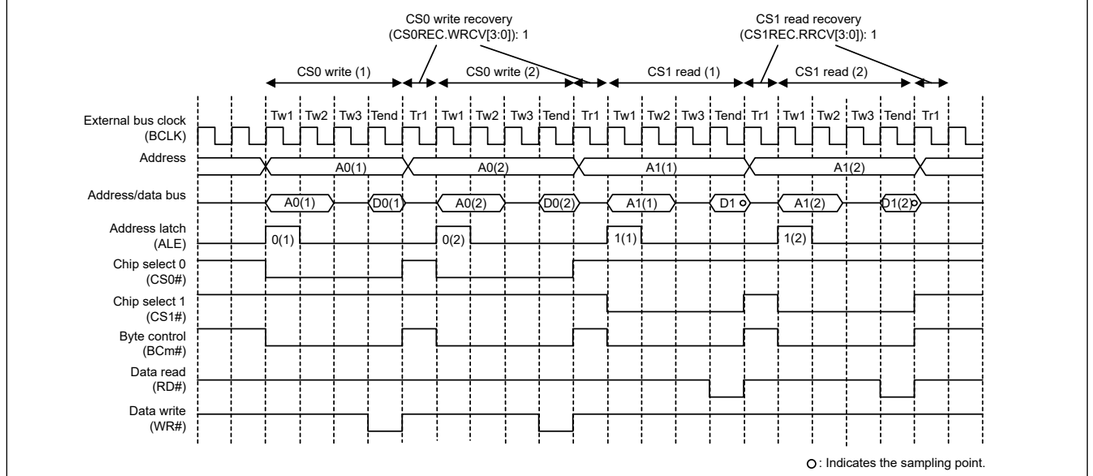


Figure 14.36 Example of recovery cycle insertion when a bus access is split with address/data multiplexed I/O interface (m = 0, 1)

14.5.5 No Access State

When no external address space is accessed, CSn#, BCn#, WRn#, and RDn# signals are high, ALE signal is low, and D15 to D0 are in the high-impedance state.

14.5.6 Write Buffer Function (External Bus)

In write access, the main bus is released from writing data to the write buffer before the access is complete. This allows the next round of bus access to start. However, if the next access is to an external address space or to a register of the external bus controller, it is suspended until the external bus operations already in progress are complete.

Figure 14.37 shows an example of operation when the write-buffer function is in use. When this function is in use, if the next operation after an external write is internal access, the internal access (access to on-chip memory or a peripheral module) is executed in parallel with the external write, that is without waiting for completion of the latter operation.

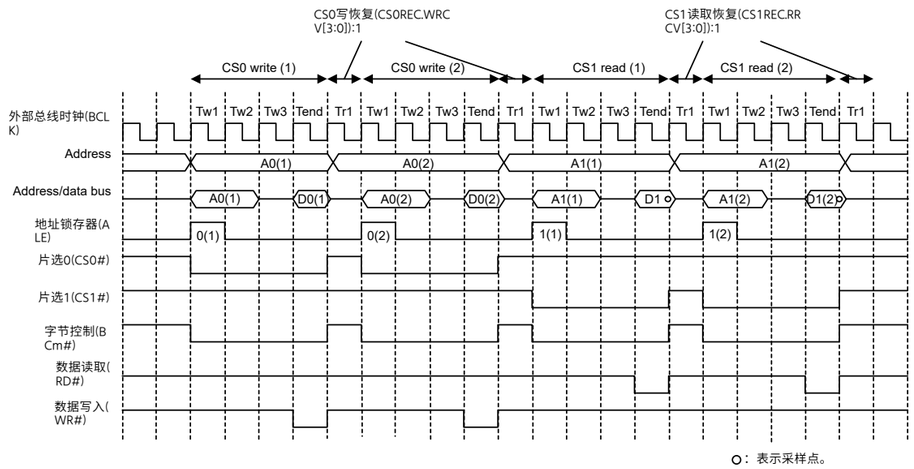


Figure 14.36 当总线访问被分割并复用地址数据时的恢复周期插入示例 I/O interface (m = 0, 1)

14.5.5 无访问状态

当没有访问外部地址空间时，CSn#、BCn#、WRn#和RDn#信号为高电平，ALE信号为低电平，D15到D0处于高阻状态。

14.5.6 写缓冲功能（外部总线）

在写访问中，主总线在访问完成之前从写数据到写缓冲区中被释放。这允许下一轮总线访问开始。然而，如果下一次访问是对外部地址空间或外部总线控制器的寄存器，则它会被挂起，直到已经在进行中的外部总线操作完成。

图14.37显示了使用写入缓冲区功能时的操作示例。使用该功能时，如果外部写入后的下一个操作是内部访问，则内部访问（访问片上存储器或外设模块）与外部写入并行执行，即无需等待完成后一种操作。

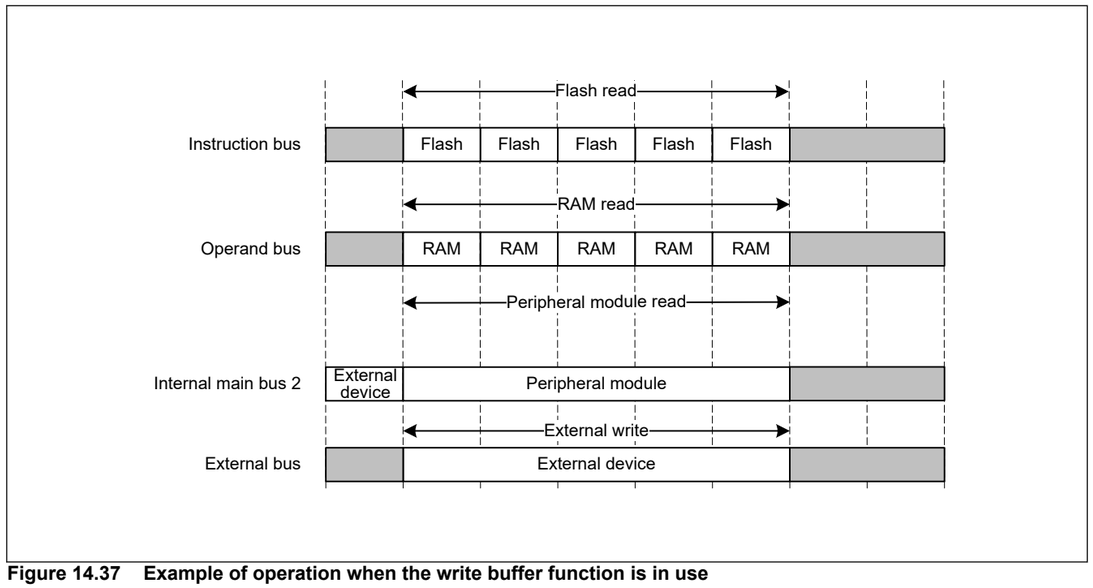


Figure 14.37 Example of operation when the write buffer function is in use

14.5.7 Constraints

(1) Constraints on Using Separate Bus Interface

Table 14.6 lists the constraints that apply to bits in the CSn Wait Control Register 1 (CSnWCR1) and CSn Wait Control Register 2 (CSnWCR2) when normal and page accesses occur.

Even if the Page Read Access Enable bit or Page Write Access Enable bit in the CSn Mode register is set to enable (CSnMOD.PRENB = 1 or CSnMOD.PWENB = 1), the first page access or access that does not fall within the scope of a page access is a normal access operation. Because of this, constraints on normal access must be satisfied.

Table 14.6 Constraints on normal access and page access

Constraints on normal access		Constraints on page access	
Reading	**Writing**	**Reading**	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON	CSON[2:0] ≤ CSPRWAIT RDON[2:0] ≤ CSPRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSPWWAIT WRON[2:0] ≤ CSPWWAIT WDON[2:0] ≤ CSPWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON

Note: When two or more external bus access cycles are required for a single transfer request from a bus master, and the recovery cycle insertion condition is satisfied, with page read access enabled (CSnMOD.PRENB = 1) or page write access enabled (CSnMOD.PWENB = 1), recovery cycles are not inserted between bus access cycles but inserted only after the last bus access cycle of the transfer.

(2) Constraints on Using Address/Data Multiplexed Bus Interface

In the address/data multiplexed I/O space, page accesses are invalid. If a page access setting is specified, the setting is ignored and the normal read or write operation is performed.

When the address/data multiplexed I/O interface is set, the BSIZE[1:0] bits in CSnCR should not be set to the 32-bit bus space. If set, the operation cannot be guaranteed.

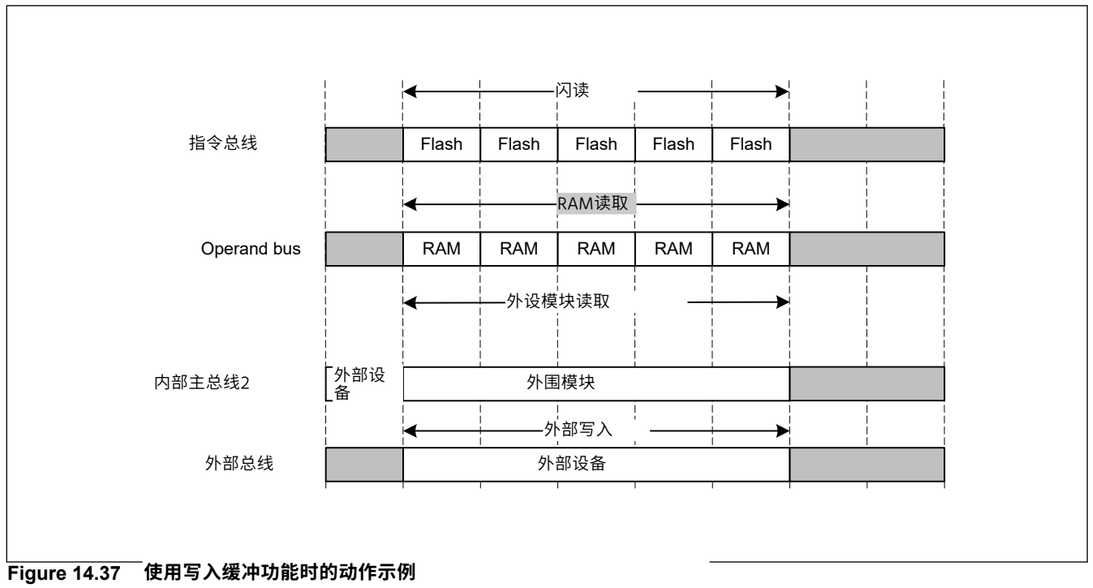


Figure 14.37 使用写入缓冲功能时的动作示例

14.5.7 Constraints

(1) 使用独立总线接口的限制

表14.6列出了适用于CSn等待控制寄存器1(CSnWCR1)和CSn等待控制中的位的约束
发生正常和页面访问时的寄存器2(CSnWCR2)。

即使CSn模式寄存器中的页面读访问使能位或页面写访问使能位设置为使能（CSnMOD.PRENB=1或CSnMOD.PWENB=1），第一个页面访问或不在范围内的访问页面访问是正常的访问操作。因此，必须满足对正常访问的限制。

Table 14.6 对正常访问和页面访问的限制

正常访问的限制		页面访问限制	
Reading	**Writing**	**Reading**	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON	CSON[2:0] ≤ CSPRWAIT RDON[2:0] ≤ CSPRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSPWWAIT WRON[2:0] ≤ CSPWWAIT WDON[2:0] ≤ CSPWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON

Note: 当来自总线主机的单个传输请求需要两个或多个外部总线访问周期，并且恢复周期插入条件满足时，启用页面读取访问(CSnMOD.PRENB=1)或启用页面写入访问(CSnMOD.PWENB=1)，恢复周期不在总线访问周期之间插入，而是仅在传输的最后一个总线访问周期之后插入。

(2) 使用地址数据复用总线接口的限制

在地址数据复用的IO空间中，页面访问是无效的。如果指定了页面访问设置，则忽略该设置并执行正常的读取或写入操作。

当设置地址数据复用IO接口时，CSnCR中的BSIZE[1:0]位不应设置为32位总线空间。如果设置，则无法保证操作。

Table 14.7 Constraints on normal access and page access

Limitations at the Time of Normal Access	
Reading	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON AWAIT[1:0] + 2 ≤ RDON CSON[2:0] ≤ AWAIT	CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON AWAIT[1:0] + 2 ≤ WRON AWAIT[1:0] + 2 ≤ WDON CSON[2:0] ≤ AWAIT

(3) Constraint on pin multiplexing between the A0 and BC0# Functions

When the A0 and BC0# pin functions share the same pin, setting the single write strobe mode is prohibited in the 8-bit bus space.

(4) Constraints when 1/2 BCLK is Selected with EBCLK Pin Output Select Bit

When 1/2 BCLK is selected in the EBCLK pin output select bit, the external bus access cycle starts on the rising edge of the EBCLK pin output. However, when 2 or more external bus access cycles are generated for a single transfer request from a bus master, the second or subsequent external bus access cycle can start on the falling edge of the EBCLK pin output, depending on the wait cycle settings. Set the registers appropriately for the specifications of connected devices. When 1/2 BCLK cycle is selected with the EBCLK pin output select bit, setting the external wait to enable (the EWENB bit = 1 in CSnMOD) is prohibited.

(5) Restriction on Instruction Code

You must fix the instruction code to little-endian order.

14.6 Bus Error Monitoring Section

The bus error monitoring system monitors each individual area, and when an error is detected, an error is returned to the requesting master IP using the AHB-Lite error response protocol.

14.6.1 Bus Error Types

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- TrustZone Filter error
- Bus error transmitted from each slave IP

Table 14.8 lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error. For more information on the bus master MPU, see section 15, Memory Protection Unit (MPU).

14.6.2 Operations When a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP.

Figure 14.38 shows operation from each error detection to user notification on the bus.

Table 14.7 对正常访问和页面访问的限制

正常访问时的限制	
Reading	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON AWAIT[1:0] + 2 ≤ RDON CSON[2:0] ≤ AWAIT	CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON AWAIT[1:0] + 2 ≤ WRON AWAIT[1:0] + 2 ≤ WDON CSON[2:0] ≤ AWAIT

(3) A0和BC0#功能之间引脚复用的约束

当A0和BC0#引脚功能共用同一个引脚时，禁止在8位总线空间设置单写选通模式。

(4) 使用EBCLK引脚输出选择位选择12BCLK时的约束

当在EBCLK引脚输出选择位选择12BCLK时，外部总线访问周期在EBCLK引脚输出。然而，当来自总线主机的单个传输请求产生2个或更多外部总线访问周期时，第二个或随后的外部总线访问周期可以在EBCLK引脚输出的下降沿开始，具体取决于等待周期设置。根据连接设备的规格适当设置寄存器。当使用EBCLK引脚输出选择位选择12BCLK周期时，设置外部等待使能（EWENB位=1

CSnMOD)被禁止。

(5) 指令码限制

您必须将指令代码修复为little-endian顺序。

14.6 总线错误监控部分

总线错误监控系统监控每个单独的区域，当检测到错误时，使用AHB-Lite错误响应协议将错误返回给请求的主IP。

14.6.1 总线错误类型

每条总线上都可能发生以下类型的错误：

- 非法地址访问
- 总线主控MPU错误
- TrustZone过滤器错误
- 从每个从IP传输的总线错误

表14.8列出了访问导致非法地址访问错误的地址范围。从机中的保留区域不会触发非法地址访问错误。有关总线主控MPU的更多信息，请参阅第15节，内存保护单元(MPU)。

14.6.2 发生总线错误时的操作

当发生总线错误时，无法保证操作，错误会返回到请求的主IP。

图14.38显示了从每个错误检测到总线上的用户通知的操作。

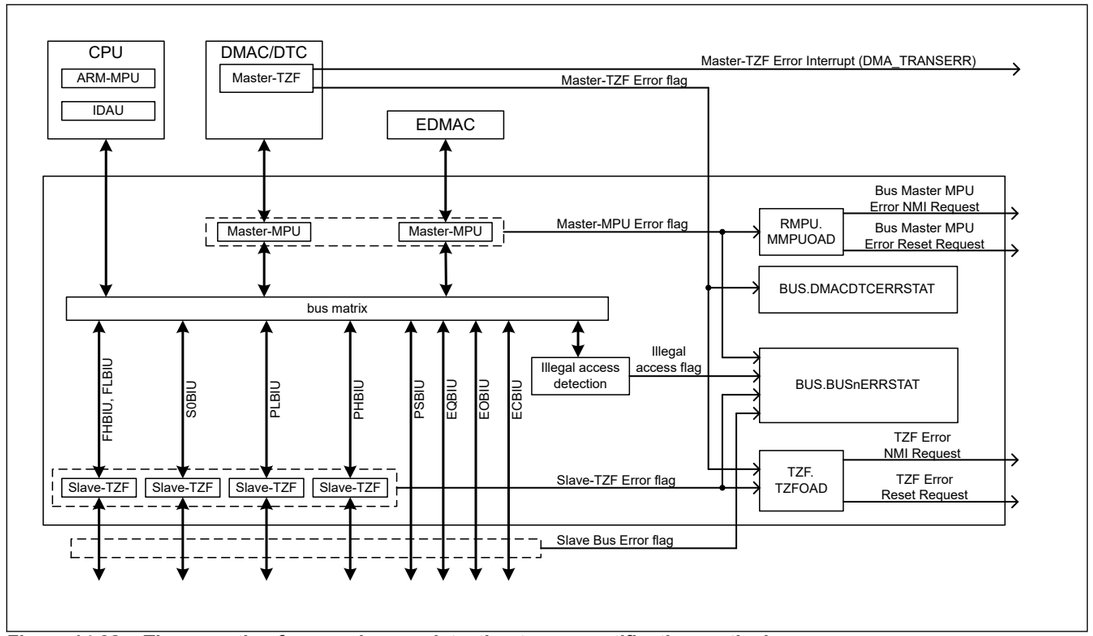


Figure 14.38 The operation from each error detection to user notification on the bus

(1) Bus Master MPU Error

The bus master of DMAC/DTC and EDMAC has a master MPU for access control of the set address area. The CPU does not have a master MPU because it has an Arm MPU. When a bus master MPU error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 3, 4).
2. Store the read/write information of the error in BUSnERRRW (n = 3, 4).
3. Set 1 to MMERRSTAT bit of BUSnERRSTAT (n = 3, 4).

An NMI request or a reset request is generated according to the MMPUOAD.OAD setting (see section 15, Memory Protection Unit (MPU)). Since BUSnERRADD (n = 3, 4), BUSnERRRW (n = 3, 4), and BUSnERRSTAT (n = 3, 4) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 3, 4), they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first bus master MPU error after a reset or clearing of BUSnERRSTAT.MMERRSTAT (n = 3, 4) bit by BUSnERRCLR (n = 3, 4).

(2) Illegal Access Error

section 14.6.3. Conditions Leading to Illegal Address Access Errors, describes illegal access errors. When an illegal access error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 1 to 4).
2. Store the read/write information of the error in BUSnERRRW (n = 1 to 4).
3. Set 1 to ILERRSTAT bit of BUSnERRSTAT (n = 1 to 4).

NMI request and reset request are not generated. Since BUSnERRADD (n = 1 to 4), BUSnERRRW (n = 1 to 4), BUSnERRSTAT (n = 1 to 4) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 4), they can be confirmed in the Bus Fault handler or the interrupt handler.

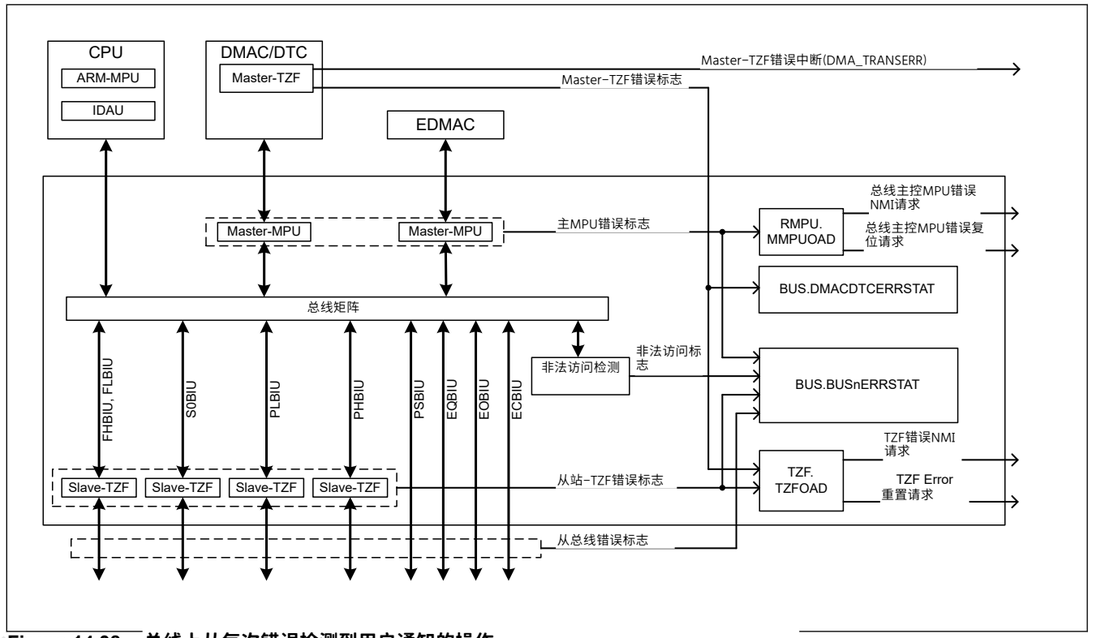


Figure 14.38 总线上从每次错误检测到用户通知的操作

(1) 总线主控MPU错误

DMACDTC和EDMAC的总线主控器有一个主控MPU，用于对设置的地址区域进行访问控制。CPU没有主MPU，因为它有一个ArmMPU。当检测到总线主控MPU错误时，会向主控返回错误响应。同时，执行以下步骤：

1.将错误地址存储在BUSnERRADD(n=3 4)中。

2.将错误的读写信息存入BUSnERRRW(n=3 4)。

3.将BUSnERRSTAT的MMERRSTAT位设置为1(n=3 4)。

根据MMPUOAD.OAD设置生成NMI请求或复位请求（参见第15节，内存保护单元（MPU））。由于BUSnERRADD(n=3 4)、BUSnERRRW(n=3 4)和BUSnERRSTAT(n=3 4)一直保持到除MPU和TZF相关复位之外的复位或被BUSnERRCLR(n=3 4)清除，它们可以在NMI处理程序中或在重置后进行验证。

NMI请求仅在复位或清除后第一个总线主MPU错误时生成BUSnERRCLR(n=3 4)中的BUSnERRSTAT.MMERRSTAT(n=3 4)位。

(2) 非法访问错误

第14.6.3节。导致非法地址访问错误的条件，描述非法访问错误。当检测到非法访问错误时，向主站返回错误响应。同时，执行以下步骤：

1.将错误地址存储在BUSnERRADD（n=1到4）中。

2.将错误的读写信息存入BUSnERRRW(n=1to4)。

3.将BUSnERRSTAT的ILERRSTAT位设置为1（n=1至4）。

不生成NMI请求和复位请求。由于BUSnERRADD（n=1到4）、BUSnERRRW（n=1到4），BUSnERRSTAT(n=1到4)保持到除MPU和TZF相关复位之外的复位或被BUSnERRCLR(n=1到4)清除之前，它们可以在总线故障处理程序或中断处理程序中确认。

(3) Master-TZF Error

As described in section 52, Security Features , DMAC/DTC has Master-TZF errors. When a Master-TZF error is detected, 1 is set to MTERRSTAT bit of DMACDTCERRSTAT, and because the DMAC/DTC does not perform bus access, no bus error information is stored in BTZF3ERRADD and BTZF3ERRRW.

An NMI request or reset request is generated according to the setting of TZFOAD.OAD. See section 16, DMA Controller (DMAC), section 17, Data Transfer Controller (DTC) for details on Master-TZF errors. Because DMACDTCERRSTAT is held until reset other than MPU- and TZF-related resets or cleared by DMACDTCERRCLR, they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first Master-TZF error after reset or clearing of the DMACDTCERRSTAT.MTERRSTAT bit by DMACDTCERRCLR.

(4) Slave-TZF Error

As described in section 52, Security Features , FHBIU (code flash), FLBIU (data flash), S0BIU (SRAM), PHBIU and PLBIU have Slave-TZF errors. When a Slave-TZF error is detected, perform the following steps:

1. Store the address of the error in BTZFnERRADD (n = 1 to 4).
2. Store the read/write information of the error in BTZFnERRRW (n = 1 to 4).
3. Set 1 to STERRSTAT bit of BUSnERRSTAT (n = 1 to 4).

NMI request or reset request is generated according to the setting in TZFOAD.OAD. Since BTZFnERRADD (n = 1 to 4), BTZFnERRRW (n = 1 to 4), and BUSnERRSTAT (n = 1 to 4) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 4), they can be verified in the NMI handler or after reset.

An NMI request is generated only on the first Slave-TZF error after a reset or clearing of the BUSnERRSTAT.STERRSTAT (n = 1 to 4) bit by BUSnERRCLR (n = 1 to 4).

(5) Slave Bus Error

Slave Bus Error occurs in the slave. When Slave Bus Error is detected, an Error response is returned to the master. At the same time, perform the following steps:

1. Store the address of the error in BUSnERRADD (n = 1 to 4)
2. Store the read/write information of the error in BUSnERRRW (n = 1 to 4)
3. Set 1 to SLERRSTAT bit of BUSnERRSTAT (n = 1 to 4).

An NMI request and reset request are not generated. Since BUSnERRADD (n = 1 to 4), BUSnERRRW (n = 1 to 4), and BUSnERRSTAT (n = 1 to 4) are held until reset other than MPU- and TZF-related resets or cleared by BUSnERRCLR (n = 1 to 4), they can be verified in the Bus Fault handler or interrupt handler. When a bus slave MPU error occurs, the error is returned to the requesting master IP and operation is not guaranteed.

14.6.3 Conditions Leading to Illegal Address Access Errors

Table 14.8 lists the address spaces for each bus that trigger illegal address access errors.

Table 14.8 Conditions leading to illegal address access errors (1 of 2)

Address	Slave bus	Master bus			
		CPU		DMA	EDMAC
		Code	System		
0x0000_0000 to 0x01FF_FFFF	FHBIU	—		—	—
0x0200_0000 to 0x07FF_FFFF	Reserved	E		E	E
0x0800_0000 to 0x0803_FFFF	FLBIU	—		—	—
0x0804_0000 to 0x0FFF_FFFF	Reserved	E		E	E
0x1000_0000 to 0x100F_FFFF	Reserved	—		E	E
0x1010_0000 to 0x1FFF_FFFF	Reserved	E		E	E

(3) Master-TZF Error

如第52节“安全功能”中所述，DMACDTC存在Master-TZF错误。当检测到Master-TZF错误时，将DMACDTCERRSTAT的MTERRSTAT位设置为1，并且由于DMACDTC不执行总线访问，因此BTZF3ERRADD和BTZF3ERRRW中不存储总线错误信息。

根据TZFOAD.OAD的设置生成NMI请求或复位请求。有关Master-TZF错误的详细信息，请参见第16节，DMA控制器(DMAC)，第17节，数据传输控制器(DTC)。因为除了MPU和TZF相关的复位或由DMACDTCERRCLR清除之外，DMACDTCERRSTAT一直保持到复位，所以可以在NMI处理程序中或在复位后对其进行验证。

NMI请求仅在复位或清除后第一个Master-TZF错误时生成DMACDTCERRCLR的DMACDTCERRSTAT.MTERRSTAT位。

(4) Slave-TZF Error

如第52节所述，安全功能、FHBIU（代码闪存）、FLBIU（数据闪存）、S0BIU（SRAM）、PHBIU和PLBIU有Slave-TZF错误。当检测到Slave-TZF错误时，执行以下步骤：

1.将错误地址存储在BTZFnERRADD（n=1到4）中。

2.将错误的读写信息存入BTZFnERRRW(n=1to4)。

3.将BUSnERRSTAT的STERRSTAT位设置为1（n=1至4）。

根据TZFOAD.OAD中的设置生成NMI请求或复位请求。由于BTZFnERRADD(n=1到4)、BTZFnERRRW(n=1到4)和BUSnERRSTAT(n=1到4)保持到除MPU和TZF相关复位之外的复位或被BUSnERRCLR(n=1到4)清除，它们可以在NMI处理程序中或在重置后进行验证。

NMI请求仅在BUSnERRCLR（n=1至4）复位或清除BUSnERRSTAT.STERRSTAT（n=1至4）位后的第一个Slave-TZF错误时生成。

(5) 从总线错误

从站总线错误发生在从站。当检测到从站总线错误时，将向主站返回错误响应。同时，执行以下步骤：

1.将错误的地址存储在BUSnERRADD(n=1to4)

2.将错误的读写信息存入BUSnERRRW(n=1to4)

3.将BUSnERRSTAT的SLERRSTAT位设置为1（n=1至4）。

不会生成NMI请求和复位请求。由于BUSnERRADD(n=1到4)、BUSnERRRW(n=1到4)和BUSnERRSTAT(n=1到4)一直保持到除MPU和TZF相关的复位之外的复位或被BUSnERRCLR(n=1到4)清除之前，它们可以在总线故障处理程序或中断处理程序中进行验证。当发生总线从MPU错误时，错误将返回到请求的主IP，并且无法保证操作。

14.6.3 导致非法地址访问错误的条件

表14.8列出了触发非法地址访问错误的每条总线的地址空间。

Table 14.8 导致非法地址访问错误的条件(1of2)

Address	从总线	主总线			
		CPU		DMA	EDMAC
		Code	System		
0x0000_0000 to 0x01FF_FFFF	FHBIU	—		—	—
0x0200_0000 to 0x07FF_FFFF	Reserved	E		E	E
0x0800_0000 to 0x0803_FFFF	FLBIU	—		—	—
0x0804_0000 to 0x0FFF_FFFF	Reserved	E		E	E
0x1000_0000 to 0x100F_FFFF	Reserved	—		E	E
0x1010_0000 to 0x1FFF_FFFF	Reserved	E		E	E

Table 14.8 Conditions leading to illegal address access errors (2 of 2)

Address	Slave bus	Master bus			
		CPU		DMA	EDMAC
		Code	System		
0x2000_0000 to 0x2800_FFFF	S0BIU		—	—	—
0x2801_0000 to 0x3FFF_FFFF	Reserved		E	E	E
0x4000_0000 to 0x4007_FFFF	PSBIU		—	—	E
0x4008_0000 to 0x400F_FFFF	PLBIU		—	—	E
0x4010_0000 to 0x4017_FFFF	PHBIU		—	—	E
0x4018_0000 to 0x407D_FFFF	Reserved		E	E	E
0x407E_0000 to 0x407F_FFFF	FLBIU		—	—	—
0x4080_0000 to 0x5FFF_FFFF	Reserved		E	E	E
0x6000_0000 to 0x67FF_FFFF	EQBIU		—	—	—
0x6800_0000 to 0x7FFF_FFFF	EOBIU		—	—	—
0x8000_0000 to 0x87FF_FFFF	ECBIU		—	—	—
0x8800_0000 to 0xDFFF_FFFF	Reserved		E	E	E
0xE000_0000 to 0xFFFF_FFFF	System for Cortex®-M33			E	E

Note: "E" : A bus error occurs.
" " : Transfer does not occur.
"—" : A bus error has not occurred. Even if there has reserved area, a bus error has not occurred.
Do not access reserved area in FLBIU and S0BIU. If accessed, a slave TZF error might occur.

14.6.4 Time-out

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain period of time, a timeout error is detected. A timeout error is returned to the requesting master IP using the AHB-Lite error response protocol.

14.7 References

1. ARM Limited, ARM v8-M Architecture Reference Manual (ARM DDI0553B.g)
2. ARM Limited, ARM Cortex-M33 Processor Technical Reference Manual Revision:r0p4 (ARM 100230_0004_00_en)
3. ARM Limited, ARM AMBA 5 AHB Protocol Specification AHB5, AHB-Lite (ARM IHI 0033B.b)
4. ARM Limited, ARM AMBA AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite (ARM IHI 0022D)
5. ARM Limited, ARM AMBA APB Protocol Specification Version: 2.0 (ARM IHI 0024C)

14.8 Cache

14.8.1 Overview

There are two types of caches:
- C-cache on code bus
- S-cache on system bus.

Table 14.9 lists the specifications of the cache, Figure 14.39 shows a block diagram of the cache, and Figure 14.40 shows the cache structure in details.

Table 14.8 导致非法地址访问错误的条件(2of2)

Address	从总线	主总线			
		CPU		DMA	EDMAC
		Code	System		
0x2000_0000 to 0x2800_FFFF	S0BIU		—	—	—
0x2801_0000 to 0x3FFF_FFFF	Reserved		E	E	E
0x4000_0000 to 0x4007_FFFF	PSBIU		—	—	E
0x4008_0000 to 0x400F_FFFF	PLBIU		—	—	E
0x4010_0000 to 0x4017_FFFF	PHBIU		—	—	E
0x4018_0000 to 0x407D_FFFF	Reserved		E	E	E
0x407E_0000 to 0x407F_FFFF	FLBIU		—	—	—
0x4080_0000 to 0x5FFF_FFFF	Reserved		E	E	E
0x6000_0000 to 0x67FF_FFFF	EQBIU		—	—	—
0x6800_0000 to 0x7FFF_FFFF	EOBIU		—	—	—
0x8000_0000 to 0x87FF_FFFF	ECBIU		—	—	—
0x8800_0000 to 0xDFFF_FFFF	Reserved		E	E	E
0xE000_0000 to 0xFFFF_FFFF	Cortex®-M33系统			E	E

Note: "E": 发生总线错误。"": 不发生传输。"—": 未发生总线错误。即使有保留区域，也没有发生总线错误。不要访问FLBIU和S0BIU中的保留区域。如果访问，可能会发生从属TZF错误。

14.6.4 Time-out

对于某些外围模块，模块停止功能会发生超时错误。当从机在一段时间内没有响应时，检测到超时错误。使用AHB-Lite错误响应协议将超时错误返回给请求的主IP。

14.7 References

1.ARMLimited，ARMv8-M架构参考手册（ARMDDI0553B.g）
2.ARMLimited，ARMCortex-M33处理器技术参考手册修订版：r0p4(ARM100230_0004_00_en)
3.ARMLimited、ARMAMBA5AHB协议规范AHB5、AHB-Lite(ARMIHI0033B.b)
4.ARMLimited、ARMAMBAAXI和ACE协议规范AXI3、AXI4和AXI4-Lite、ACE和ACE-Lite(ARMIHI0022D)
5.ARMLimited，ARMAMBAAPB协议规范版本：2.0（ARMIHI0024C）

14.8 Cache

14.8.1 Overview

缓存有两种类型：●代码总线上的C-cache●系统总线上的S-cache。

表14.9列出了缓存的规格，图14.39显示了缓存的框图，图14.40显示了详细的缓存结构。

Table 14.9 Cache specifications

Parameter	C-cache	S-cache
Capacity	2 KB	2 KB
Way	2-way set associative	2-way set associative
Line size	32/64 bytes	32/64 bytes
Number of entry	32/16 entry/way	32/16 entry/way
Write way	No write	Write-through, non-write allocate
Replace way	2-way: LRU (least recently used)	2-way: LRU (least recently used)
Cache support area	0x0000_0000 to 0x1FFF_FFFF	0x20000000 – 0xDFFFFFFF*1 except Standby SRAM area (0x2800_0000 to 0x2FFFF_FFFF)

Note 1. Peripheral area 0x4000_0000 to 0x5FFF_FFFF must not have the cacheable attribution in the Arm MPU.

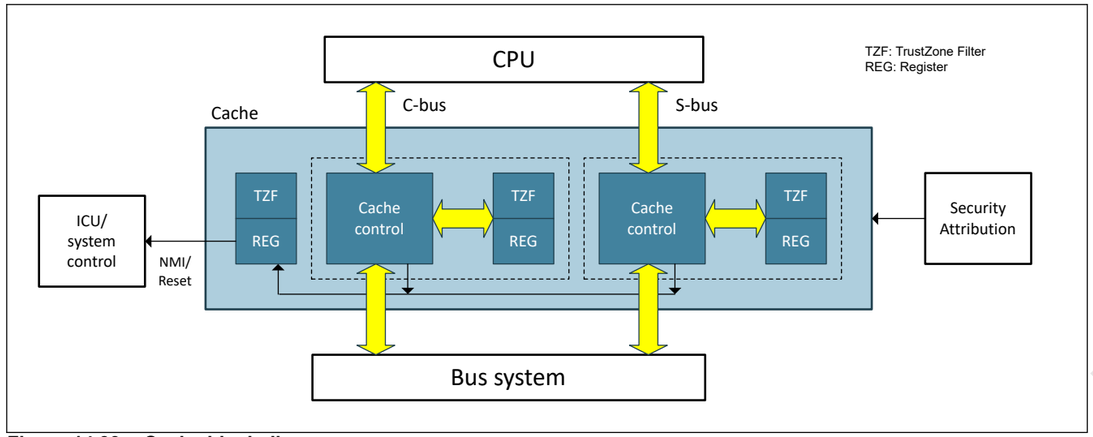


Figure 14.39 Cache block diagram

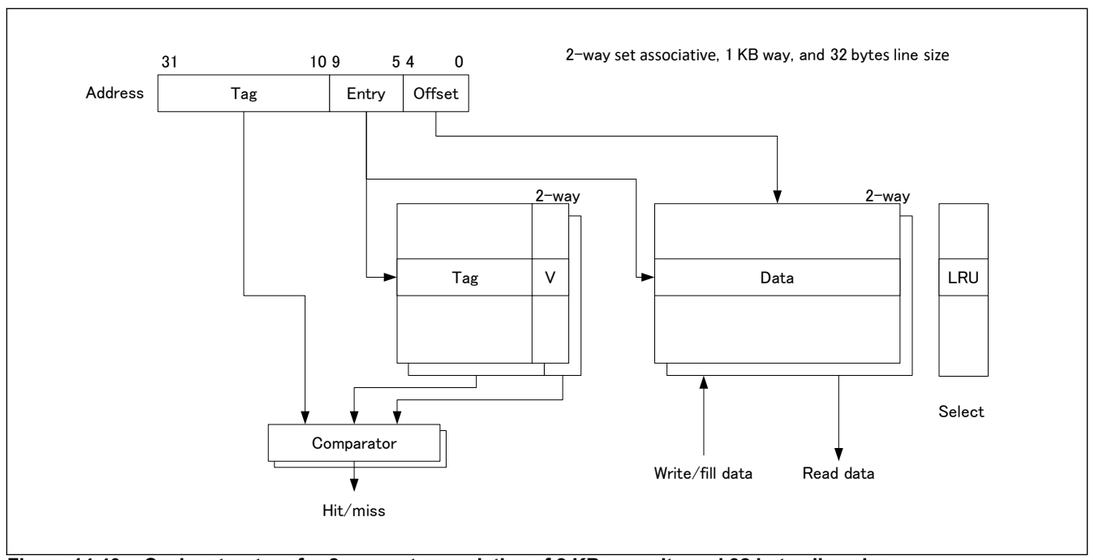


Figure 14.40 Cache structure for 2-way set associative of 2 KB capacity and 32 bytes line size

Table 14.9 缓存规范

Parameter	C-cache	S-cache
Capacity	2 KB	2 KB
Way	2路组关联	2路组关联
线条尺寸	32/64 bytes	32/64 bytes
入境次数	32/16 entry/way	32/16 entry/way
写法	不写	Write-through, non-write allocate
更换方式	2-way: LRU (least recently used)	2-way: LRU (least recently used)
缓存支持区	0x0000_0000 to 0x1FFF_FFFF	0x20000000 0xDFFFFFFF*1除了待机SRAM区域（0x2800_0000到0x2FFFF_FFFF）

注1.外设区域0x4000_0000到0x5FFF_FFFF在ArmMPU中不得具有可缓存属性。

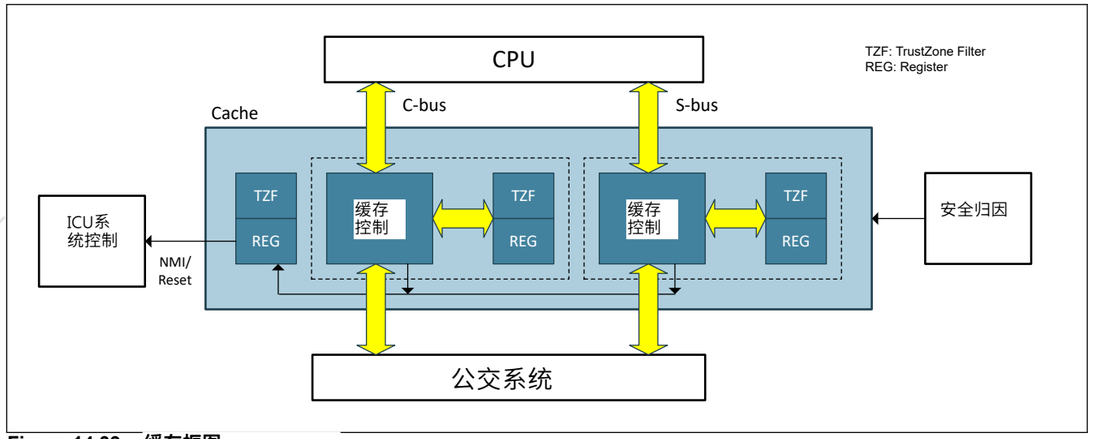


Figure 14.39 缓存框图

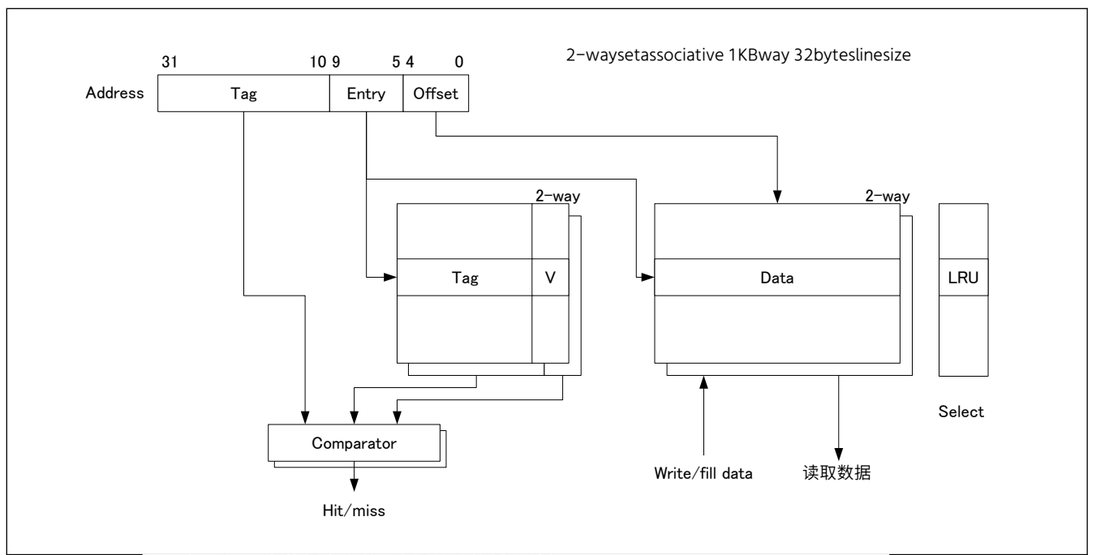


Figure 14.40 2KB容量和32字节行大小的2路组关联的缓存结构

14.8.2 Register Description

14.8.2.1 CSAR : Cache Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CACHEESA	CACHELSA	CACHESA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CACHESA	Security Attributes of Registers for Cache Control 0: Secure 1: Non-secure	R/W
1	CACHELSA	Security Attributes of Registers for Cache Line Configuration 0: Secure 1: Non-secure	R/W
2	CACHEESA	Security Attributes of Registers for Cache Error 0: Secure 1: Non-secure	R/W
31:3	—	These bits are read as 1.	R

Note: This register is write-protected by PRCR register.

CACHESA bit (Security Attributes of Registers for Cache Control)

The CACHESA bit indicates the security attributes of registers for cache control. The target registers are:

- CCACTL
- CCAFCT
- SCACTL
- SCAFCT.

CACHELSA bit (Security Attributes of Registers for Cache Line Configuration)

The CACHELSA bit indicates the security attributes of registers for cache line configuration. The target registers are:

- CCALCF
- SCALCF.

CACHEESA bit (Security Attributes of Registers for Cache Error)

The CACHEESA bit indicates the security attributes of registers for cache error.

- CAPOAD
- CAPRCR.

14.8.2 注册说明

14.8.2.1 CSAR:缓存安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	CACHEESA	CACHELSA	CACHESA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CACHESA	缓存控制寄存器的安全属性 0: Secure 1: Non-secure	R/W
1	CACHELSA	缓存行配置寄存器的安全属性 0: Secure 1: Non-secure	R/W
2	CACHEESA	缓存错误寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:3	—	这些位读为1。	R

Note: 该寄存器由PRCR寄存器写保护。

CACHESA位（缓存控制寄存器的安全属性）

CACHESA位指示用于缓存控制的寄存器的安全属性。目标寄存器是：●CCACTL●CCAFCT●SCACTL●SCAFCT。

CACHELSA位（缓存线配置寄存器的安全属性）

CACHELSA位指示用于高速缓存行配置的寄存器的安全属性。目标寄存器是：●CCALCF●SCALCF。

CACHEESA位（缓存错误寄存器的安全属性）

CACHEESA位指示缓存错误寄存器的安全属性。●CAPOAD●CAPRCR。

14.8.2.2 CCACTL : C-Cache Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x000

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENC	C-Cache Enable Set the C-cache enable: 0: Disable C-cache 1: Enable C-cache	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ENC bit (C-Cache Enable)

The ENC bit controls the cache enable of C-cache. When the ENC bit changes from 0 to 1, the Valid bit of C-cache is cleared.

14.8.2.3 CCAFCT : C-Cache Flush Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x004

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FC	C-Cache Flush Set the C-cache line flush: 0: No action 1: C-cache line flush (all lines invalidated)	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FC bit (C-Cache Flush)

The FC bit controls the cache flush of C-cache.

[Setting condition]

- When writing 1 to this bit.
- When setting CCACTL.ENC bit from "0" to "1".

[Clearing condition]

14.8.2.2 CCACTL:C-Cache控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x000

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENC	C-Cache Enable 设置C缓存启用： 0：禁用C-cache1 ：启用C-cache	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ENC bit (C-Cache Enable)

ENC位控制C-cache的缓存使能。当ENC位从0变为1时，C-cache的Valid位被清除。

14.8.2.3 CCAFCT:C-Cache刷新控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x004

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FC	C-Cache Flush 设置C-cache行刷新： 0：无操作1：C-cache行刷新（所有行无效）	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

FC bit (C-Cache Flush)

FC位控制C-cache的缓存刷新。

[Setting condition]

●向该位写入1时。

●将CCACTL.ENC位从"0"设置为"1"时。

[Clearing condition]

- This bit is cleared automatically when cache flush is performed.

14.8.2.4 CCALCF : C-Cache Line Configuration Register

Base address: CACHE = 0x4000_7000

Offset address: 0x008

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CC[1:0]	C-Cache Line Size Set the C-cache line size: 0 0: Prohibited 0 1: Cache line size 32 bytes 1 0: Cache line size 64 bytes 1 1: Prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

CC[1:0] bits (C-Cache Line Size)

The CC[1:0] bits control the cache line size of C-cache. This bit can be written when the CCACTL.ENC bit is 0. Otherwise, this bit cannot be written.

14.8.2.5 SCACTL : S-Cache Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x040

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENS	S-Cache Enable Set the S-cache enable: 0: Disable S-cache 1: Enable S-cache	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ENS bit (S-Cache Enable)

The ENS bit controls the cache enable of S-cache. When the ENS bit changes from 0 to 1, the Valid bit of S-cache is cleared.

●执行缓存刷新时，该位自动清零。

14.8.2.4 CCALCF:C-Cache行配置寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x008

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CC[1:0]	C-Cache行大小 设置C-cache行大小： 00：禁止01：缓存线大小32 字节10：缓存线大小64字节1 1：禁止	R/W
31:2	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

CC[1:0]位（C-CacheLineSize）

CC[1:0]位控制C-cache的高速缓存行大小。当CCACTL.ENC位为0时可以写入该位。否则，无法写入该位。

14.8.2.5 SCACTL:S-Cache控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x040

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ENS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENS	S-Cache Enable 设置S-cache启用： 0：禁用S-cache1 ：启用S-cache	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ENS位（S-Cache启用）

ENS位控制S-cache的缓存使能。当ENS位从0变为1时，S-cache的Valid位被清除。

14.8.2.6 SCAFCT : S-Cache Flush Control Register

Base address: CACHE = 0x4000_7000

Offset address: 0x044

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	S-Cache Flush Set the S-cache line flush: 0: No action 1: S-cache line flush (all lines invalidated)	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FS bit (S-Cache Flush)

The FS bit controls the cache flush of S-cache.

[Setting condition]

When writing 1 to this bit.

When setting SCACTL.ENS bit from "0" to "1".

[Clearing condition]

This bit is cleared automatically when cache flush is performed.

14.8.2.7 SCALCF : S-Cache Line Configuration Register

Base address: CACHE = 0x4000_7000

Offset address: 0x048

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CS[1:0]	S-Cache Line Size Set the S-cache line size: 0 0: Prohibited 0 1: Cache line size 32 bytes 1 0: Cache line size 64 bytes 1 1: Prohibited	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

14.8.2.6 SCAFCT:S-Cache刷新控制寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x044

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	S-Cache Flush 设置S-cache行刷新： 0：无操作1：S-cache行刷新（所有行无效）	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

FS bit (S-Cache Flush)

FS位控制S-cache的缓存刷新。

[Setting condition]

向该位写入1时。

将SCACTL.ENS位从“0”设置为“1”时。

[Clearing condition]

执行缓存刷新时，该位会自动清除。

14.8.2.7 SCALCF:S-Cache行配置寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x048

Bit position:	31																												1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
1:0	CS[1:0]	S-Cache行大小 设置S-cache行大小： 00：禁止01：缓存线大小32字节10：缓存线大小64字节1 1：禁止	R/W
31:2	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

CS[1:0] bits (S-Cache Line Size)

The CS[1:0] bits control the cache line size of S-cache. This bit can be written when the SCACTL.ENS bit is 0. Otherwise, this bit cannot be written.

[Setting condition]

This bit can be written when the CACTL.ENS bit is 0. Otherwise, this bit cannot be written.

14.8.2.8 CAPOAD : Cache Parity Error Operation After Detection Register

Base address: CACHE = 0x4000_7000

Offset address: 0x200

Bit position:	31																														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after Detection Select the operation after detection: 0: Non-maskable interrupt 1: Reset	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

OAD bit (Operation after Detection)

The OAD bit generates either a reset or a non-maskable interrupt when parity error is detected.

The protection register (CAPRCR) protects this register against writes. Modify the valid bit in the protection register (CAPRCR) to enable before writing to this bit. Do not write to CAPOAD while access to cache is in progress.

14.8.2.9 CAPRCR : Cache Protection Register

Base address: CACHE = 0x4000_7000

Offset address: 0x204

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	KW[6:0]							PRCR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRCR	Register Write Control Set the register write control: 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W
7:1	KW[6:0]	Write key code These bits enable or disable writes to the PRCR bit.	R/W

CS[1:0]位（S-Cache行大小）

CS[1:0]位控制S-cache的缓存线大小。当SCACTL.ENS位为0时可以写入该位。否则，无法写入该位。

[Setting condition]

当CACTL.ENS位为0时可以写入该位。否则，无法写入该位。

14.8.2.8 CAPOAD：检测寄存器后缓存奇偶校验错误操作

Base address: CACHE = 0x4000_7000

Offset address: 0x200

Bit position:	31																														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 检测后选择操作： 0：不可屏蔽中断1：复位	R/W
31:1	—	这些位被读取为0。写入值应为0。	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

OAD位（检测后的操作）

当检测到奇偶校验错误时，OAD位会产生复位或不可屏蔽中断。

保护寄存器(CAPRCR)保护该寄存器不被写入。在写入该位之前修改保护寄存器(CAPRCR)中的有效位以使能。在访问缓存的过程中不要写入CAPOAD。

14.8.2.9 CAPRCR:缓存保护寄存器

Base address: CACHE = 0x4000_7000

Offset address: 0x204

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	KW[6:0]							PRCR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRCR	寄存器写控制 设置寄存器写控制： 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W
7:1	KW[6:0]	编写关键代码 这些位启用或禁用对PRCR位的写入。	R/W

Bit	Symbol	Function	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

PRCR bit (Register Write Control)

The PRCR bit controls the write mode of the CAPOAD register. When this bit is set to 1, writing to the CAPOAD register is enabled. When writing to this bit, write 0x78 to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write key code)

The KW[6:0] bits enable or disable writes to the PRCR bit. When writing to the PRCR bit, write 0x78 to the KW[6:0] bits simultaneously. When a value other than 0x78 is written to KW[6:0] bits, the PRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

14.8.3 Operation

14.8.3.1 S-Cache

Figure 14.41 shows the access flow from CPU to S-cache.

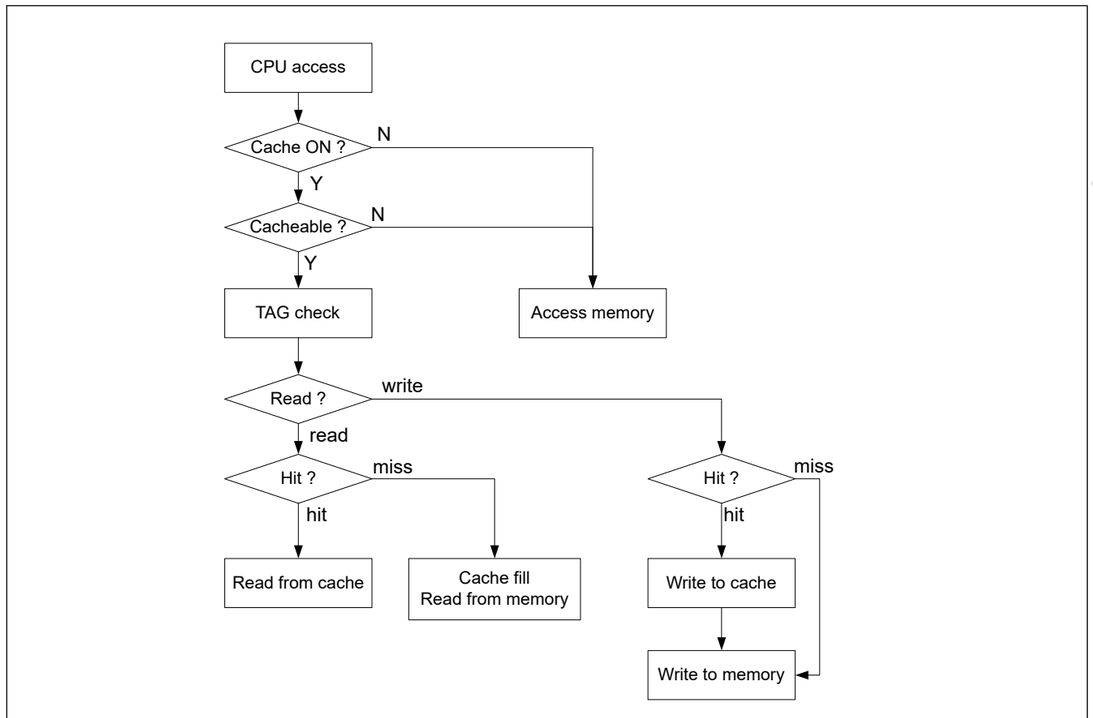


Figure 14.41 Access flow from CPU to S-cache

The cache function works when cache is enabled (CACTL.ENS = 1) and cacheable access is from CPU. The cache checks the address of CPU access request and request in cache tag, then determines whether the CPU access is a hit or a miss-hit.

Bit	Symbol	Function	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：
- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：
- 允许安全和非安全访问。

PRCR位（寄存器写控制）

PRCR位控制CAPOAD寄存器的写模式。当该位设置为1时，允许写入CAPOAD寄存器。写入该位时，同时将0x78写入KW[6:0]位。

KW[6:0]位（写键码）

KW[6:0]位启用或禁用对PRCR位的写入。写入PRCR位时，同时将0x78写入KW[6:0]位。当将0x78以外的值写入KW[6:0]位时，PRCR位不会更新。KW[6:0]位总是被读取为0x00。

14.8.3 Operation

14.8.3.1 S-Cache

图14.41显示了从CPU到S-cache的访问流程。

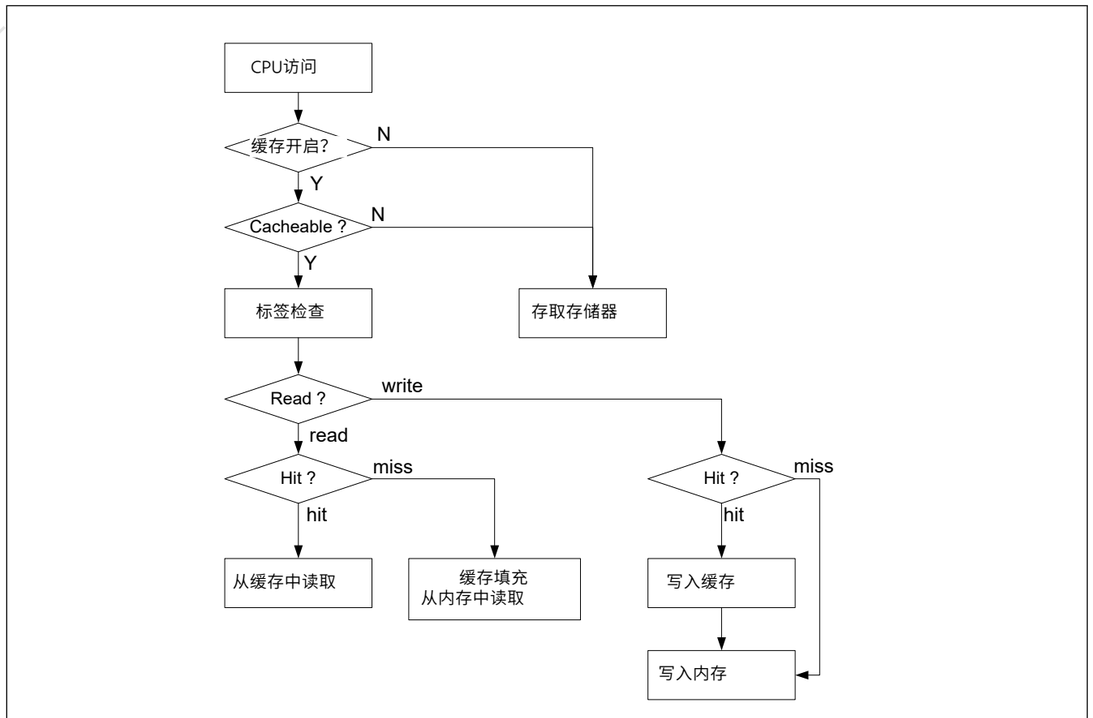


Figure 14.41 从CPU到S-cache的访问流程

缓存功能在启用缓存(CACTL.ENS=1)且可缓存访问来自CPU时起作用。缓存检查CPU访问请求的地址和缓存标签中的请求，然后确定CPU访问是命中还是未命中。

RA生态工作室

Read miss

The cache reads one cache line data from memory and stores it into the cache data. The cache then returns the required data to CPU.

Read hit

The cache reads required data from the cache data and returns it to CPU. Access cycle then determines it is a hit because of the 0 wait cycle.

Write miss

The cache processes only a write cycle to memory. No affect to cache data.

Write hit

The cache processes both a write cycle to cache data and a write cycle to memory.

14.8.3.2 C-Cache

Figure 14.42 shows the access flow from CPU to C-cache.

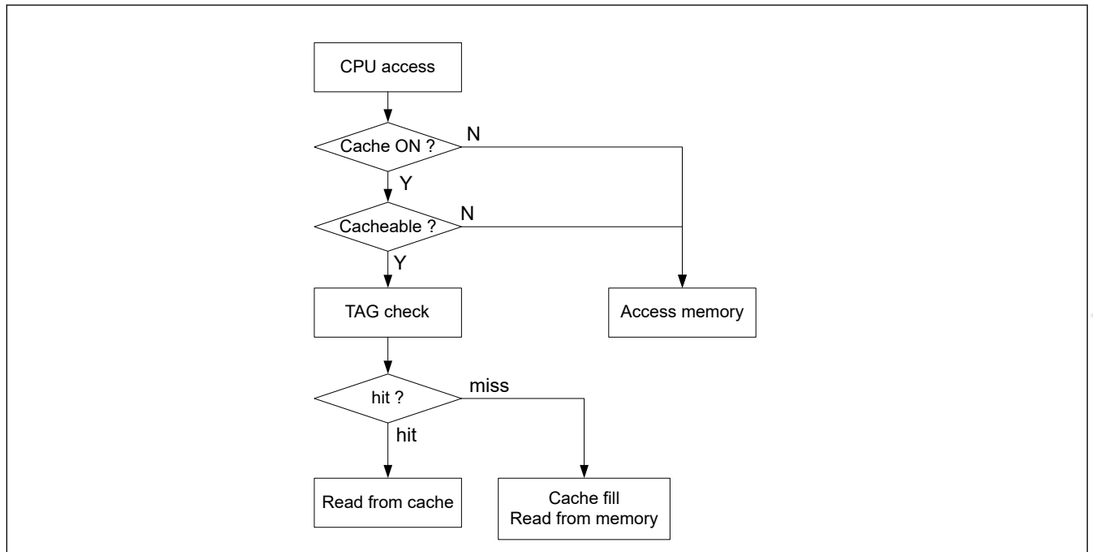


Figure 14.42 Access flow from CPU to C-cache

The cache function works when cache is enabled (CACTL.ENC = 1) and cacheable access is from CPU. The cache checks the address of CPU access request and request in cache tag, then determines whether the CPU access is a hit or a miss-hit.

Read miss

The cache reads one cache line data from memory and stores it into the cache data. The cache then returns the required data to CPU.

Read hit

The cache reads required data from the cache data and returns it to CPU. Access cycle then determines it is a hit because of the 0 wait cycle.

Because C-cache does not function in the ROM area of C-cache, therefore it operates in read-only access.

14.8.3.3 Cache Flush

The Valid bit is cleared with the CAFCT register. However, tag and cache data are not affected by the CAFCT register.

读未读

高速缓存从内存中读取一个高速缓存行数据并将其存储到高速缓存数据中。然后缓存将所需的数据返回给CPU。

阅读命中

缓存从缓存数据中读取需要的数据并返回给CPU。然后访问周期确定它是命中，因为等待周期为0。

写小姐

高速缓存仅处理对内存的写周期。不影响缓存数据。

写命中

高速缓存处理缓存数据的写周期和存储器的写周期。

14.8.3.2 C-Cache

图14.42显示了从CPU到C-cache的访问流程。

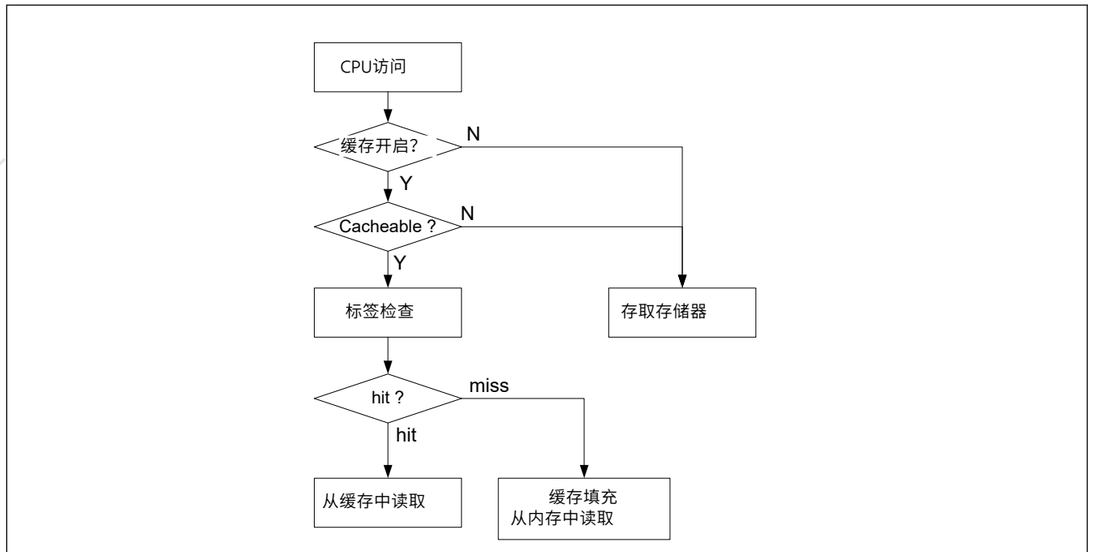


Figure 14.42 从CPU到C-cache的访问流程

缓存功能在启用缓存(CACTL.ENC=1)且可缓存访问来自CPU时起作用。缓存检查CPU访问请求的地址和缓存标签中的请求，然后确定CPU访问是命中还是未命中。

读未读

高速缓存从内存中读取一个高速缓存行数据并将其存储到高速缓存数据中。然后缓存将所需的数据返回给CPU。

阅读命中

缓存从缓存数据中读取需要的数据并返回给CPU。然后访问周期确定它是命中，因为等待周期为0。

由于C-cache在C-cache的ROM区域中不起作用，因此它以只读访问方式运行。

14.8.3.3 缓存刷新

有效位通过CAFCT寄存器清零。但是，标签和缓存数据不受 CAFCT寄存器的影响。

The valid bit is also cleared when CACTL is set from 0 to 1.

Note: After changing the cacheable attribute by the Arm MPU, clear the valid bit using the CAFCT register.

14.8.3.4 LRU and Replace

The cache uses LRU (Least Recently Used) mechanism as the cache replacement algorithm. If a CPU access is determined as a hit or a miss-hit, the cache replaces cache data that is not the last restored. Additionally, the cache is tagged as the latest data in LRU of the cache data. Therefore even when the cache line in cache ways are full, the cache can replace cache data using LRU which shows older data.

The algorithm for a 2-way LRU shows which way, for example way 0 or way 1, is the latest stored.

14.8.3.5 Parity Check

The cache has a parity check function for cache RAM that is stored as cache fill data. The cache has 4-bit parities for 32-bit data, that is when data is read, a parity bit is added to every 8-bit data of 32-bit data width. When the cache reads data with a hit status, it checks for parity errors. When a parity error occurs, a parity error notification is generated.

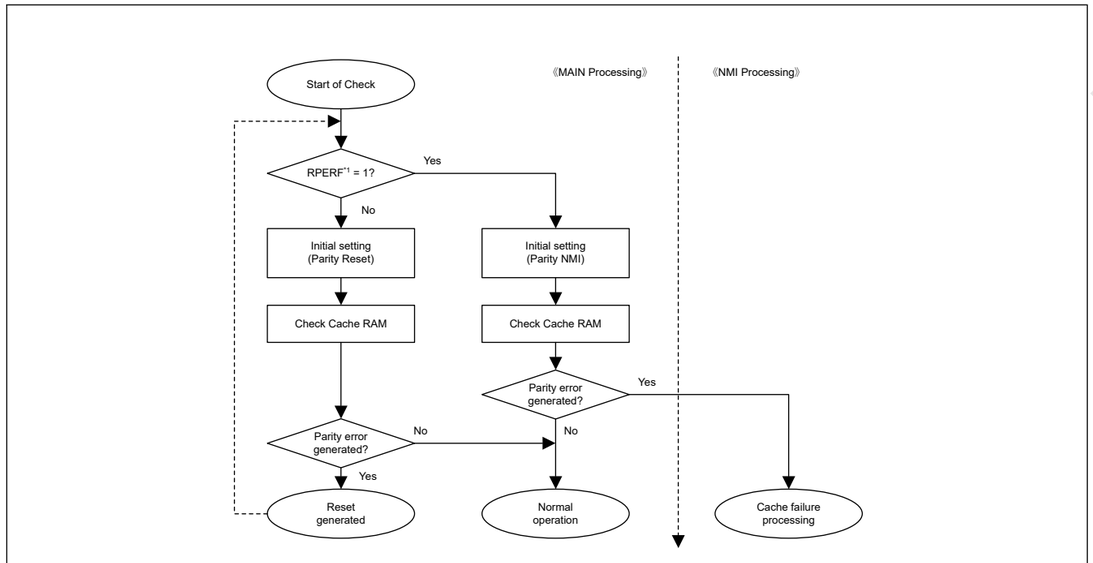
The cache reads 32-bit data even when the CPU requests a byte read or half-word read.

Note: A parity error might occur even though it is caused by a non validated-data byte of which the CPU does not request.

Parity error notification can be specified as a non-maskable interrupt or a reset request in the CAPOAD register. However, if the debug mode requests to suppress the parity error notification, then notification is not generated.

When a parity error occurs, the cache does not perform a cache flush and does not respond to the CPU with a bus error.

Parity errors often occur due to noise. To confirm whether the cause of the parity error is noise or corruption, see the flows for cache parity check in Figure 14.43 and Figure 14.44.



Note 1. RPERF: Cache Parity Error Reset Detect Flag (RSTSR1.RPERF)

Figure 14.43 Flow of cache parity check when parity reset is enabled

当CACTL从0设置为1时，有效位也会被清除。

Note: 通过ArmMPU更改可缓存属性后，使用CAFCT寄存器清除有效位。

14.8.3.4 LRU和替换

缓存使用LRU（最近最少使用）机制作为缓存替换算法。如果CPU访问被确定为命中或未命中，则缓存替换不是最后恢复的缓存数据。另外，缓存被标记为缓存数据的LRU中的最新数据。因此，即使缓存路中的缓存行已满，缓存也可以使用显示较旧数据的LRU替换缓存数据。

2路LRU的算法显示了最新存储的路，例如路0或路1。

14.8.3.5 奇偶校验

高速缓存具有用于存储为高速缓存填充数据的高速缓存RAM的奇偶校验功能。高速缓存对于32位数据有4位奇偶校验，即在读取数据时，每32位数据宽度的8位数据添加一个奇偶校验位。当缓存读取具有命中状态的数据时，它会检查奇偶校验错误。当发生奇偶校验错误时，会生成奇偶校验错误通知。

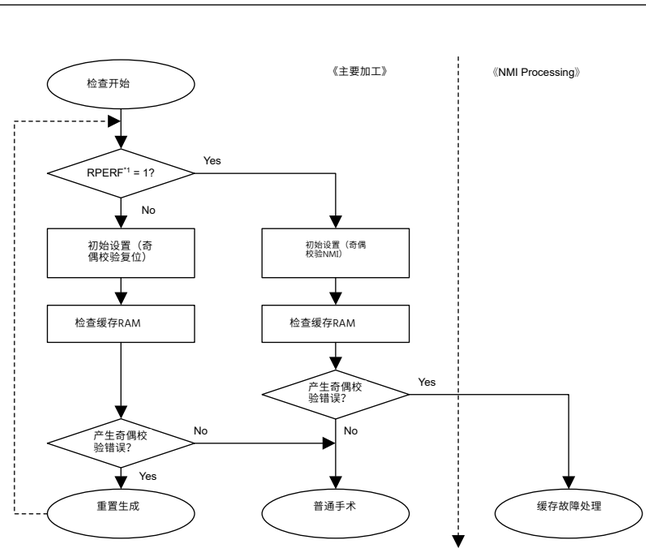
即使CPU请求字节读取或半字读取，缓存也会读取32位数据。

Note: 即使奇偶校验错误是由CPU未请求的未经验证的数据字节引起的，也可能发生奇偶校验错误。

奇偶校验错误通知可以指定为不可屏蔽中断或CAPOAD寄存器中的复位请求。但是，如果调试模式请求抑制奇偶校验错误通知，则不会生成通知。

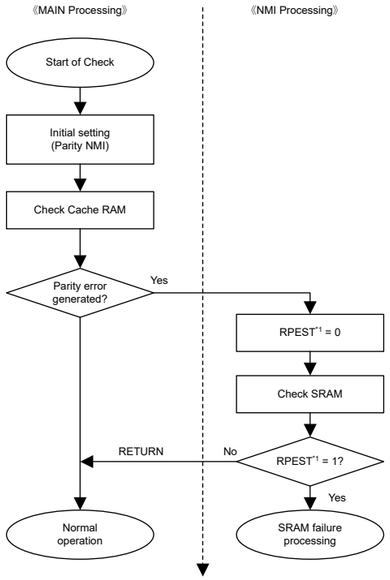
当发生奇偶校验错误时，缓存不会执行缓存刷新，也不会以总线错误响应CPU。

奇偶校验错误经常由于噪声而发生。要确认奇偶校验错误的原因是噪声还是损坏，请参见图14.43和图14.44中的缓存奇偶校验流程。



注1.RPERF：高速缓存奇偶校验错误复位检测标志(RSTSR1.RPERF)

Figure 14.43 启用奇偶校验时的缓存奇偶校验流程



Note 1. RPEST: Cache Parity Error Interrupt Detect Flag (NMISR.RPEST)

Figure 14.44 Flow of cache parity check when parity interrupt is enabled

14.8.3.5.1 Cache RAM Check

Parity error of cache RAM occurs at a read access by CPU with a cache status of read-hit. With a read-hit status, some conditions are required before performing a cache RAM check. For S-cache check, execute the check program in flash memory. For C-cache check, execute the check program in SRAM or external memory.

(1) Cache RAM check flow

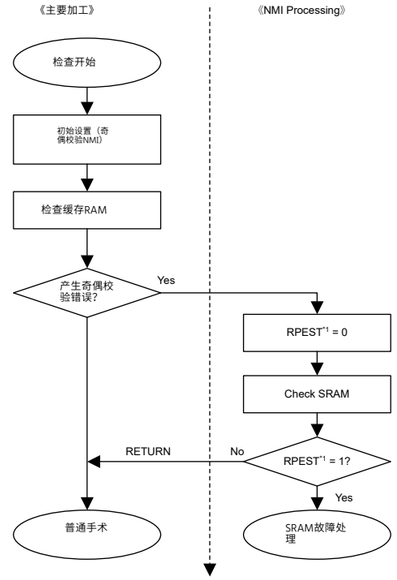
1. Flush all valid bits in cache to clear the cache enable bit.
2. Reserve a 2-KB work memory such as SRAM or external memory for S-cache. Because each cache in the MCU is a 2-way set associative with 1 KB RAM per way, a total of 2 KB is required for S-cache. The target address should not be used as reserved area.
3. Set the cache enable to 1.
4. Read data from the target word address of 2 KB using the CPU. The status of cache should be a read-miss with the result stored as cache fill data.
5. Read data in another cache way whose address is calculated by adding the address in step 4. with 1 KB address. The status of cache should be a read-miss with the result stored as cache fill data in another way. Cache RAM check for a write/read-hit status is now complete.
6. Write test data to the target word address in steps 4. and 5.. The status of cache in steps 4. and 5. should be a write-hit with the results written to the cache RAM.
7. Read from the target word address in steps 4. and 5. again. The status of cache in steps 4. and 5. should be a read-hit. Parity check for a word data is now complete.
8. Go to step 1. to continue parity check for different target addresses.

14.8.3.6 Bus Error

The association from a bus slave to a bus error is described in the sections that follow.

In cache off

The cache returns a bus error to the CPU.



注1.RPEST：高速缓存奇偶校验错误中断检测标志(NMISR.RPEST)

Figure 14.44 启用奇偶校验中断时的缓存奇偶校验流程

14.8.3.5.1 缓存RAM检查

高速缓存RAM的奇偶校验错误发生在CPU读取访问时，高速缓存状态为read-hit。对于读取命中状态，在执行高速缓存RAM检查之前需要一些条件。对于S-cache检查，执行闪存中的检查程序。对于C-cache检查，在SRAM或外部存储器中执行检查程序。

(1) 缓存RAM检查流程

1.刷新缓存中的所有有效位以清除缓存启用位。2.为S-cache预留2KB的工作存储器，例如SRAM或外部存储器。因为MCU中的每个缓存都是2way组，每路1KBRAM，所以S-cache总共需要2KB。目标地址不应用作保留区。3.将缓存使能设置为1。4.使用CPU从2KB的目标字地址读取数据。缓存的状态应该是读未命中，结果存储为缓存填充数据。5.以另一种缓存方式读取数据，其地址是通过将步骤4中的地址与1KB地址相加计算出来的。缓存的状态应该是读未命中，结果以另一种方式存储为缓存填充数据。写读命中状态的高速缓存RAM检查现已完成。6.在步骤4.和5.中将测试数据写入目标字地址。步骤4.和5.中的缓存状态应该是写入命中，结果写入缓存RAM。7.再次从步骤4.和5.中的目标字地址读取。第4步和第5步中缓存的状态应该是读取命中。单词数据的奇偶校验现已完成。8.转到步骤1.继续对不同的目标地址进行奇偶校验。

14.8.3.6 总线错误

从总线从站到总线错误的关联将在后面的部分中描述。

在缓存关闭

高速缓存将总线错误返回给CPU。

For non-cacheable access

The cache returns a bus error to the CPU.

During read accesses for cache fill

For the first data that corresponds to a CPU access request, the cache returns a bus error to the CPU. For other read data while filling the cache line, the cache cannot return a bus error to the CPU except for read data with early forwarding. The cache enable bit clears the cache line if the cache accepts a bus error response from the slave.

For write-hit status

The cache cannot return a bus error to the CPU because the cache enable bit does not clear the cache line.

For write-miss status

The cache cannot return a bus error to the CPU.

14.8.3.7 Early Forwarding Function

While filling data in the cache, if the address of the CPU read request and the address of the cache fill request are the same, the cache returns the data to CPU. Table 14.10 shows an example.

Table 14.10 Example of early forwarding

Operation	Access sequence								
Address of CPU read request	0x04	0x08	0x0C	0x14	→	0x10	→	→	→
Address of cache fill	0x04	0x08	0x0C	0x10	0x14	0x18	0x1C	0x00	—
CPU access status	Read (0x04)	Read (0x08)	Read (0x0C)	—	Read (0x14)	—	—	—	Read (0x10)

When the CPU requests read accesses and the addresses are 0x04, 0x08, 0x0C, 0x14 and 0x10 sequentially, the first read access to address 0x04 is of a miss-hit status and the cache starts to fill data into cache. The early forwarding function allows a return of read data to CPU when accesses are to addresses 0x08, 0x0C and 0x14 while the cache is filling the cache line. On the other hand, access to address 0x10 must wait for the completion of filling the cache line. The cache then returns data for address 0x10 when it finished filling the cache line.

14.8.4 Usage Notes

14.8.4.1 Cache Line Configuration Register

Writes to the Cache Line Configuration Register are allowed when the status is cache off (CACTL.ENS = 0 for S-cache, CACTL.ENC = 0 for C-cache).

14.8.4.2 Coherency

The coherency between the cache and the external memory / internal SRAM must be guaranteed by software.

When allocating shared memory between the CPU and a bus master such as DMAC in the cache support area, invalidate the cache data as necessary.

对于不可缓存的访问

高速缓存将总线错误返回给CPU。

在缓存填充的读取访问期间

对于与CPU访问请求对应的第一个数据，缓存将总线错误返回给CPU。对于其他在填充高速缓存行时读取的数据，除了提前转发的读取数据外，高速缓存不能向CPU返回总线错误。如果缓存接受来自从设备的总线错误响应，缓存使能位清除缓存行。

对于写命中状态

高速缓存无法向CPU返回总线错误，因为高速缓存启用位不会清除高速缓存行。

对于写未命中状态

高速缓存不能将总线错误返回给CPU。

14.8.3.7 提前转发功能

在缓存中填充数据时，如果CPU读取请求的地址和缓存填充请求的地址相同，则缓存将数据返回给CPU。表14.10显示了一个示例。

Table 14.10 提前转发示例

Operation	访问顺序								
CPU读请求地址	0x04	0x08	0x0C	0x14	→	0x10	→	→	→
缓存填充地址	0x04	0x08	0x0C	0x10	0x14	0x18	0x1C	0x00	—
CPU访问状态	Read (0x04)	Read (0x08)	Read (0x0C)	—	Read (0x14)	—	—	—	Read (0x10)

当CPU请求读访问，地址依次为0x04、0x08、0x0C、0x14和0x10时，对地址0x04的第一次读访问为未命中状态，缓存开始将数据填充到缓存中。早期转发功能允许在高速缓存填充高速缓存行时访问地址0x08、0x0C和0x14时将读取数据返回到CPU。另一方面，对地址0x10的访问必须等待缓存行的填充完成。然后，缓存在完成填充缓存行后返回地址0x10的数据。

14.8.4 使用说明

14.8.4.1 高速缓存行配置寄存器

当状态为高速缓存关闭时，允许写入高速缓存行配置寄存器（对于S-cache，CACTL.ENS=0，CACTL.ENC = 0 for C-cache).

14.8.4.2 Coherency

高速缓存和外部存储器内部SRAM之间的一致性必须由软件来保证。

在高速缓存支持区域中，在CPU和DMAC等总线主控器之间分配共享内存时，根据需要使高速缓存数据无效。

15. Memory Protection Unit (MPU)

15.1 Overview

The MCU has one Memory Protection Unit (MPU).

Table 15.1 lists the MPU specifications, and Table 15.2 shows the behavior on detection of each MPU error.

Table 15.1 MPU specifications

Classification	Module/Function	Specifications
Illegal memory access	Arm® Cortex®-M33 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs • The MPU can change a default memory map.
Memory protection	Arm MPU	Memory protection function for the CPU: • (8+8) region MPU with sub regions and background region for secure and non-secure.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • DMAC/DTC: 8 regions • EDMAC(Ether): 4 regions

Table 15.2 Behavior on MPU error detection

MPU type	Notification type	Error Response by HRESP signal of AHB I/F	Bus Access on error detection	Storing of error access information
Arm MPU	• Hard fault	Not supported	• Does not correctly write access • Does not correctly read access	Stored in the Cortex-M33 processor
Bus Master MPU	• Reset or Non-maskable interrupts • Hard fault	Supported	• Write access ignore • Read access is read as 0	Stored

For information on error access for the Arm MPU, see section 15.4. References. For information on error access for other MPUs, see section 14.3. Register Descriptions and section 14.6. Bus Error Monitoring Section in section 14, Buses.

15.2 Arm MPU

The Arm MCU monitors the addresses accessed by the CPU across the entire address space (0x0000_0000 to 0xFFFF_FFFF) and provides support for:

- (8 + 8) protected regions
- When memory regions overlap, the processor generates a fault if a core access hits the overlapping regions
- Setting access permissions to protected region (Read, Write, Execution)
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (Hard Fault) handler. For details, see reference 1., 3. and 4. in section 15.4. References.

15.3 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus masters in the entire address space (0x0000_0000 to 0xFFFF_FFFF). Access-control information can be set up to 8 regions in DMAC/DTC and 4 regions in EDMAC and monitor for access to each region is in accord with this information.

If access to a protected region is detected, the bus master MPU generates an internal reset or a non-maskable interrupt. For information on error access, see section 14.3. Register Descriptions and section 14.6. Bus Error Monitoring Section in section 14, Buses.

Table 15.3 lists the specifications of the bus master MPU.

15. 内存保护单元(MPU)

15.1 Overview

MCU有一个内存保护单元(MPU)。

表15.1列出了MPU规格，表15.2显示了检测每个MPU错误时的行为。

Table 15.1 MPU specifications

Classification	Module/Function	Specifications
非法内存访问	Arm®皮质®-M33 CPU	• ArmCPU有一个默认的内存映射。如果CPU进行非法访问，则会发生异常中断 • MPU可以更改默认内存映射。
内存保护	Arm MPU	CPU的内存保护功能：● (8+8)带有子区域和背景区域的区域MPU，用于安全和非安全。
	总线主控MPU	除CPU外的每个总线主控的内存保护功能：● • EDMAC(Ether): 4 regions

Table 15.2 MPU错误检测的行为

MPU type	通知类型	错误响应 AHB的HRESP信号 I/F	错误检测总线访问	存储错误访问信息
Arm MPU	• 硬故障	不支持	• 没有正确的写访问 • 未正确读取访问权限	存储在Cortex中 M33 processor
总线主控MPU	• 复位或不可屏蔽中断 • 硬故障	Supported	• 写访问忽略 • 读权限读为0	Stored

有关ArmMPU错误访问的信息，请参阅第15.4节。参考。有关其他错误访问的信息
MPU，见第14.3节。寄存器说明和第14.6节。第14节，总线中的总线错误监控部分。

15.2 Arm MPU

ArmMCU监控整个地址空间（0x0000_0000到0xFFFF_FFFF）中CPU访问的地址，并支持：

●(8+8)个保护区
●当内存区域重叠时，如果核心访问命中重叠区域，处理器将产生故障
●设置对受保护区域的访问权限（读、写、执行）
●将内存属性导出到系统。

ArmMPU不匹配和权限违规调用可编程优先级MemManage故障（硬故障）处理程序。详见15.4节中的参考1.、3.和4.。参考。

15.3 总线主控MPU

总线主控MPU监控整个地址空间（0x0000_0000到0xFFFF_FFFF）中总线主控访问的地址。访问控制信息在DMACDTC中最多可设置8个区域，在EDMAC中最多可设置4个区域，每个区域的访问监控与此信息一致。

如果检测到对受保护区域的访问，总线主控MPU会产生内部复位或不可屏蔽中断。有关错误访问的信息，请参阅第14.3节。寄存器说明和第14.6节。第14节，总线中的总线错误监控部分。

表15.3列出了总线主控MPU的规格。

Table 15.3 Bus master MPU specifications

Parameter	Description
Protected master groups	• DMAC, DTC • EDMAC(Ether)
Protected regions	0x0000_0000 to 0xFFFF_FFFF
Number of regions	• DMAC/DTC: 8 regions • EDMAC(Ether): 4 regions
Address specification for individual regions	• Specifying start and end address for individual regions
Enable or disable setting for memory protection in individual regions	• Enabling or disabling setting for the associated region
Access-control settings for individual regions	• Permission for read and write
Operation on error detection	• Reset or non-maskable interrupts
Register protection	• Protecting registers from illegal writes
TrustZone Filter	• DMAC: Security attribution can be set for each regions • EDMAC(Ether): Security attribution is always non-secure

15.3.1 Register Descriptions

Bus access must be stopped before writing to MPU registers.

15.3.1.1 MMPUSARA : Master Memory Protection Unit Security Attribution Register A

Base address: CPSCU = 0x4000_8000

Offset address: 0x130

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MMPUASA7	MMPUASA6	MMPUASA5	MMPUASA4	MMPUASA3	MMPUASA2	MMPUASA1	MMPUASA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	MMPUASAn	MMPUA Security Attribution (n = 0 to 7) 0: Secure 1: Non-Secure	R/W
31:8	—	These bits are read as 1.	R*1

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. This bit is read only.

MMPUASAn bits (MMPUA Security Attribution (n = 0 to 7))

The MMPUASAn bits specify the security attributes of registers for the Bus Master MPU Region Setting register. The target registers are:

- MMPUSDMACn (n = 0 to 7)
- MMPUEDMACn (n = 0 to 7)
- MMPUACDMACn (n = 0 to 7)

Table 15.3 总线主控MPU规格

Parameter	Description
受保护的主组	• DMAC, DTC • EDMAC(Ether)
保护区	0x0000_0000 to 0xFFFF_FFFF
地区数量	• DMAC/DTC: 8 regions • EDMAC(Ether): 4 regions
个别地区的地址规范	• 指定各个区域的开始和结束地址
在各个区域启用或禁用内存保护设置	• 启用或禁用关联区域的设置
各个区域的访问控制设置	• 读写权限
错误检测操作	• 复位或不可屏蔽中断
注册保护	• 保护寄存器免受非法写入
TrustZone Filter	• DMAC：可以为每个区域设置安全属性 • EDMAC(Ether)：安全属性总是不安全的

15.3.1 注册说明

在写入MPU寄存器之前必须停止总线访问。

15.3.1.1 MMPUSARA:主内存保护单元安全属性寄存器A

Base address: CPSCU = 0x4000_8000

Offset address: 0x130

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	MMPUASA7	MMPUASA6	MMPUASA5	MMPUASA4	MMPUASA3	MMPUASA2	MMPUASA1	MMPUASA0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	MMPUASAn	MMPUA安全属性（n=0到7） 0: Secure 1: Non-Secure	R/W
31:8	—	这些位读为1。	R*1

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
注1.该位是只读的。

MMPUASan位（MMPUA安全属性（n=0到7））

MMPUASan位指定总线主控MPU区域设置寄存器的寄存器的安全属性。目标寄存器是：

- MMPUSDMACn (n = 0 to 7)
- MMPUEDMACn (n = 0 to 7)
- MMPUACDMACn (n = 0 to 7)

15.3.1.2 MMPUSARB : Master Memory Protection Unit Security Attribution Register B

Base address: CPSCU = 0x4000_8000

Offset address: 0x134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MMPUBSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MMPUBSA0	MMPUB Security Attribution 0: Secure 1: Non-Secure	R/W
31:1	—	These bits are read as 1.	R*1

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note 1. This bit is read-only.

MMPUBSA0 bit (MMPUB Security Attribution)

The MMPUBSA0 bit specifies the security attributes of registers for the Bus Master MPU Region Setting register, Protect register, and OAD register. The target registers are:

- MMPUENDMAC
- MMPUENPTDMAC
- MMPURPTDMAC
- MMPURPTDMAC_SEC
- MMPUOAD
- MMPUOADPT

The Secure user provides a Secure API to Non-secure user for the modification of the MMPURPTDMAC value when MMPUBSA0 bit is set to 0 (Secure).

15.3.1.3 MMPUSDMACn : MMPU Start Address Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0204 + 0x010 × n

Bit position:	31	5	4	3	2	1	0
Bit field:	MMPUS[31:5]	—	—	—	—	—	—
Value after reset:	x	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 0. The write value should be 0.	R/W
31:5	MMPUS[31:5]	Region start address register Address where the region starts, for use in region determination	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed

15.3.1.2 MMPUSARB:主存储器保护单元安全属性寄存器B

Base address: CPSCU = 0x4000_8000

Offset address: 0x134

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MMPUBSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MMPUBSA0	MMPUB安全归因 0: Secure 1: Non-Secure	R/W
31:1	—	这些位读为1。	R*1

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
注1.该位是只读的。

MMPUBSA0位（MMPUB安全属性）

MMPUBSA0位指定总线主控MPU区域设置寄存器、保护寄存器和OAD寄存器的寄存器的安全属性。目标寄存器是：

- MMPUENDMAC
- MMPUENPTDMAC
- MMPURPTDMAC
- MMPURPTDMAC_SEC
- MMPUOAD
- MMPUOADPT

安全用户向非安全用户提供一个安全API，用于在以下情况下修改MMPURPTDMAC值
MMPUBSA0位设置为0（安全）。

15.3.1.3 MMPUSDMACn：DMAC的MMPU起始地址寄存器（n=0到7）

Base address: RMPU = 0x4000_0000

Offset address: 0x0204 + 0x010 × n

Bit position:	31	5	4	3	2	1	0
Bit field:	MMPUS[31:5]	—	—	—	—	—	—
重置后的值:	x	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为0。写入值应为0。	R/W
31:5	MMPUS[31:5]	区域起始地址寄存器 区域起始地址，用于区域确定	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问

- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

The MMPUSDMACn (n = 0 to 7) register specifies the start address where the region starts.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

Regions set by MMPUSDMACn (n = 0 to 7), MMPUEDMACn (n = 0 to 7) and MMPUACDMACn (n = 0 to 7) registers, can be set for a secure access or a non-secure access with the MMPUSARA register. If the corresponding MMPUSARA.MMPUASAn (n = 0 to 7) bit is set to 1, only non-secure access is permitted for that region. On the other hand, if the corresponding MMPUSARA.MMPUASAn (n = 0 to 7) bit is set to 0, only secure access is permitted for that region.

15.3.1.4 MMPUSEDMACn : MMPU Start Address Register for EDMAC (n = 0 to 3)

Base address: RMPU = 0x4000_0000

Offset address: 0x0604 + 0x010 × n

Bit position:	31																								5					0
Bit field:	MMPUS[31:5]																								—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 0. The write value should be 0.	R/W
31:5	MMPUS[31:5]	Region start address register for EDMAC Address where the region starts, for use in region determination	R/W

The MMPUSEDMACn (n = 0 to 3) register specifies the start address where the region starts.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

15.3.1.5 MMPUEDMACn : MMPU End Address Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0208 + 0x010 × n

Bit position:	31																								5					0
Bit field:	MMPUE[31:5]																								—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
31:5	MMPUE[31:5]	Region end address register Address where the region end, for use in region determination	R/W

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

The MMPUEDMAC (n = 0 to 7) register specifies the end address where the region ends.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

MMPUSDMACn（n=0到7）寄存器指定区域开始的起始地址。

该寄存器需要字访问。禁止字节访问和半字访问。当执行字节访问和半字访问时，不能保证操作。

由MMPUSDMACn（n=0到7）、MMPUEDMACn（n=0到7）和MMPUACDMACn（n=0到7）寄存器设置的区域可以通过MMPUSARA寄存器设置为安全访问或非安全访问。如果相应的MMPUSARA.MMPUASAn（n=0到7）位设置为1，则该区域仅允许非安全访问。另一方面，如果相应的MMPUSARA.MMPUASAn(n=0到7)位设置为0，则仅允许对该区域进行安全访问。

15.3.1.4 MMPUSEDMACn：EDMAC的MMPU起始地址寄存器（n=0到3）

Base address: RMPU = 0x4000_0000

Offset address: 0x0604 + 0x010 × n

Bit position:	31																								5					0
Bit field:	MMPUS[31:5]																								—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为0。写入值应为0。	R/W
31:5	MMPUS[31:5]	EDMAC的区域起始地址寄存器 区域起始地址，用于区域确定	R/W

MMPUSEDMACn(n=0to3)寄存器指定区域开始的起始地址。

该寄存器需要字访问。禁止字节访问和半字访问。当执行字节访问和半字访问时，不能保证操作。

15.3.1.5 MMPUEDMACn：DMAC的MMPU结束地址寄存器（n=0到7）

Base address: RMPU = 0x4000_0000

Offset address: 0x0208 + 0x010 × n

Bit position:	31																								5					0
Bit field:	MMPUE[31:5]																								—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为1。写入值应为1。	R/W
31:5	MMPUE[31:5]	区域结束地址寄存器 区域结束的地址，用于区域确定	R/W

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

MMPUEDMAC（n=0到7）寄存器指定区域结束的结束地址。

该寄存器需要字访问。禁止字节访问和半字访问。当执行字节访问和半字访问时，不能保证操作。

15.3.1.6 MMPUEEDMACn : MMPU End Address Register for EDMAC (n = 0 to 3)

Base address: RMPU = 0x4000_0000

Offset address: 0x0608 + 0x010 × n

Bit position:	31																							5	4	3	2	1	0
Bit field:	MMPUE[31:5]																							—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
31:5	MMPUE[31:5]	Region end address register for EDMAC Address where the region ends, for use in region determination	R/W

The MMPUEEDMACn (n = 0 to 3) register specifies the end address where the region ends.

This register requires word access. Byte access and half word access is prohibited. When byte access and half word access is executed, operation is not guaranteed.

15.3.1.7 MMPUACDMACn : MMPU Access Control Register for DMAC (n = 0 to 7)

Base address: RMPU = 0x4000_0000

Offset address: 0x0200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Region enable 0: DMAC Region n unit is disabled 1: DMAC Region n unit is enabled	R/W
1	RP	Read protection 0: Read permission 1: Read protection	R/W
2	WP	Write protection 0: Write permission 1: Write protection	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Region n unit sets the ENABLE bit, the RP bit, and the WP bit each.

ENABLE bit (Region enable)

The ENABLE bit controls the enable or disable of DMAC/DTC region n (n = 0 to 7) unit.

When the ENABLE bit is set to 1, the RP bit and the WP bit control access permission for read and write protection to MMPUSDMACn (n = 0 to 7) and MMPUEDMACn (n = 0 to 7).

When the ENABLE bit is set to 0, access to DMAC region n (n = 0 to 7) is the outside region.

RP bit (Read protection)

The RP bit enables or disables read protection of DMAC/DTC region n (n = 0 to 7).

15.3.1.6 MMPUEEDMACn：EDMAC的MMPU结束地址寄存器（n=0到3）

Base address: RMPU = 0x4000_0000

Offset address: 0x0608 + 0x010 × n

Bit position:	31																							5	4	3	2	1	0
Bit field:	MMPUE[31:5]																							—	—	—	—	—	—
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为1。写入值应为1。	R/W
31:5	MMPUE[31:5]	EDMAC的区域结束地址寄存器 区域结束的地址，用于区域确定	R/W

MMPUEEDMACn(n=0to3)寄存器指定区域结束的结束地址。

该寄存器需要字访问。禁止字节访问和半字访问。当执行字节访问和半字访问时，不能保证操作。

15.3.1.7 MMPUACDMACn：用于DMAC的MMPU访问控制寄存器（n=0到7）

Base address: RMPU = 0x4000_0000

Offset address: 0x0200 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	区域启用 0：禁用DMAC区域n单元1：启用DMAC区域n单元	R/W
1	RP	读保护 0：读取权限1：读取保护	R/W
2	WP	写保护 0：写权限1：写保护	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

区域n单元分别设置ENABLE位、RP位和WP位。

ENABLE位（区域使能）

ENABLE位控制DMACDTC区域n（n=0到7）单元的启用或禁用。

当ENABLE位设置为1时，RP位和WP位控制读写保护的访问权限MMPUSDMACn（n=0到7）和MMPUEDMACn（n=0到7）。

当ENABLE位设置为0时，访问DMAC区域n（n=0到7）是外部区域。

RP bit (Read protection)

RP位启用或禁用DMACDTC区域n（n=0到7）的读保护。

When the ENABLE bit is set to 1, the RP bit is available.

WP bit (Write protection)

The WP bit enables or disables write protection of DMAC/DTC region n (n = 0 to 7).

When the ENABLE bit is set to 1, the WP bit is available.

Table 15.4 Function of Region Control Circuit for DMAC

MMPUACDMACn (n = 0 to 7)			Access	Region	Output of DMAC Region n unit (n = 0 to 7)
ENABLE	RP	WP			
0	—	—	Read	—	Outside region
			Write		Outside region
1	0	0	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	0	1	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region
	1	0	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	1	1	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region

Note: Each regions of DMAC / DTC are set for secure access and non-secure access by MMPUSARA register. In this case, Non-Secure regions in secure access and secure regions in Non-Secure access are outside regions.

Table 15.5 Function of Master Control Circuit for DMAC

MMPUENDMAC	Output of DMAC Region 0 unit	Output of DMAC Region 1 unit	Output of DMAC Region 2-7 unit	Function of DMAC
ENABLE				
1	Protected region	Don't care	Don't care	Generate error
	Don't care	Protected region	Don't care	Generate error
	Don't care	Don't care	Protected region	Generate error
	Outside region	Outside region	Outside region	Generate error
Other cases				No error

A master MPU error occurs on the following conditions:

1. MMPUENDMAC.ENABLE = 1, and output of one or more Region n unit is protected region.
2. MMPUENDMAC.ENABLE = 1, and output of all Region n unit are outside region.

Other cases are handled as permitted region.

当ENABLE位设置为1时，RP位可用。

WP bit (Write protection)

WP位启用或禁用DMACDTC区域n（n=0到7）的写保护。

当ENABLE位设置为1时，WP位可用。

Table 15.4 DMAC区域控制电路的功能

MMPUACDMACn (n = 0 to 7)			Access	Region	DMAC区域n单元的输出（n=0到7）
ENABLE	RP	WP			
0	—	—	Read	—	区域外
			Write		区域外
1	0	0	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	0	1	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外
	1	0	Read	Inside	保护区
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	1	1	Read	Inside	保护区
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外

Note: DMACDTC的每个区域都通过MMPUSARA寄存器设置为安全访问和非安全访问。在这种情况下，安全访问中的非安全区域和非安全访问中的安全区域是外部区域。

Table 15.5 DMAC主控电路的功能

MMPUENDMAC	DMAC区域0单元的输出	DMAC区域1单元的输出	DMAC区域2−7单元的输出	DMAC的功能
ENABLE				
1	保护区	Don't care	Don't care	产生错误
	Don't care	保护区	Don't care	产生错误
	Don't care	Don't care	保护区	产生错误
	区域外	区域外	区域外	产生错误
其他案例				没有错误

主控MPU错误发生在以下情况：

1.MMPUENDMAC.ENABLE=1，一个或多个Regionn单元的输出为受保护区域。

2.MMPUENDMAC.ENABLE=1，所有Regionn单元的输出都在Region外。

其他情况按许可区域处理。

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15.3.1.8 MMPUACEDMACn : MMPU Access Control Register for EDMAC (n = 0 to 3)

Base address: RMPU = 0x4000_0000

Offset address: 0x0600 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Region enable 0: EDMAC Region n unit is disabled 1: EDMAC Region n unit is enabled	R/W
1	RP	Read protection 0: Read permission 1: Read protection	R/W
2	WP	Write protection 0: Write permission 1: Write protection	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W

Region n unit sets the ENABLE bit, the RP bit, and the WP bit each.

ENABLE bit (Region enable)

The ENABLE bit controls enable or disable of EDMAC region n (n = 0 to 3) unit.

When the ENABLE bit is set to 1, the RP bit and the WP bit control access permission to read and write protection of MMPUSEDMACn (n = 0 to 3) and MMPUEEDMACn (n = 0 to 3).

When the ENABLE bit is set to 0, access to EDMAC region n (n = 0 to 3) is the outside region.

RP bit (Read protection)

The RP bit controls enable or disable read protection of EDMAC region n (n = 0 to 3).

When the ENABLE bit is set to 1, the RP bit is valid.

WP bit (Write protection)

The WP bit controls enable or disable write protection of EDMAC region n (n = 0 to 3).

When the ENABLE bit is set to 1, the WP bit is valid.

Table 15.6 Function of Region Control Circuit for EDMAC (1 of 2)

MMPUACEDMACn (n = 0 to 3)			Access	Region	Output of EDMAC Region n unit (n = 0 to 3)
ENABLE	RP	WP			
0	—	—	Read	—	Outside region
			Write		Outside region

15.3.1.8 MMPUACEDMACn：用于EDMAC的MMPU访问控制寄存器（n=0到3）

Base address: RMPU = 0x4000_0000

Offset address: 0x0600 + 0x010 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	区域启用 0：禁用EDMAC区域n单元1：启用EDMAC区域n单元	R/W
1	RP	读保护 0：读取权限1：读取保护	R/W
2	WP	写保护 0：写权限1：写保护	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W

区域n单元分别设置ENABLE位、RP位和WP位。

ENABLE位（区域使能）

ENABLE位控制EDMAC区域n（n=0到3）单元的启用或禁用。

当ENABLE位设置为1时，RP位和WP位控制读写保护的访问权限MMPUSEDMACn（n=0到3）和MMPUEEDMACn（n=0到3）。

当ENABLE位设置为0时，访问EDMAC区域n（n=0到3）是外部区域。

RP bit (Read protection)

RP位控制启用或禁用EDMAC区域n（n=0到3）的读保护。

当ENABLE位设置为1时，RP位有效。

WP bit (Write protection)

WP位控制启用或禁用EDMAC区域n（n=0到3）的写保护。

当ENABLE位设置为1时，WP位有效。

Table 15.6 EDMAC区域控制电路的功能(1of2)

MMPUACEDMACn (n = 0 to 3)			Access	Region	EDMAC区域n单元的输出（n=0到3）
ENABLE	RP	WP			
0	—	—	Read	—	区域外
			Write		区域外

Table 15.6 Function of Region Control Circuit for EDMAC (2 of 2)

MMPUACEDMACn (n = 0 to 3)			Access	Region	Output of EDMAC Region n unit (n = 0 to 3)
ENABLE	RP	WP			
1	0	0	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	0	1	Read	Inside	Permitted region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region
	1	0	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Permitted region
				Outside	Outside region
	1	1	Read	Inside	Protection region
				Outside	Outside region
			Write	Inside	Protection region
				Outside	Outside region

Note: Each regions of EDMAC is set for secure access and non-secure access by MMPUSARA register. In this case, Non-Secure regions in secure access and secure regions in Non-Secure access are outside regions.

Table 15.7 Function of Master Control Circuit for EDMAC

MMPUENEDMAC	Output of EDMAC Region0 unit	Output of EDMAC Region1 unit	Output of EDMAC Region2-3 unit	Function of EDMAC
ENABLE				
1	Protected region	Don't care	Don't care	Generate error
	Don't care	Protected region	Don't care	Generate error
	Don't care	Don't care	Protected region	Generate error
	Outside region	Outside region	Outside region	Generate error
Other cases				No error

Master MPU Error occur on the following condition.

1. MMPUENEDMAC.ENABLE=1, and output of one or more Region n unit is protection region.
2. MMPUENEDMAC.ENABLE=1, and output of all Region n unit are outside region.

Other cases are handled as permitted region.

15.3.1.9 MMPUENDMAC : MMPU Enable Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15.6 EDMAC区域控制电路的功能(2of2)

MMPUACEDMACn (n = 0 to 3)			Access	Region	EDMAC区域n单元的输出（n=0到3）
ENABLE	RP	WP			
1	0	0	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	0	1	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外
	1	0	Read	Inside	保护区
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	1	1	Read	Inside	保护区
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外

Note: EDMAC的每个区域都通过MMPUSARA寄存器设置为安全访问和非安全访问。在这种情况下，安全访问中的非安全区域和非安全访问中的安全区域是外部区域。

Table 15.7 EDMAC主控电路的功能

MMPUENEDMAC	EDMAC的输出 Region0 unit	EDMAC的输出 Region1 unit	EDMAC的输出 Region2-3 unit	EDMAC的功能
ENABLE				
1	保护区	Don't care	Don't care	产生错误
	Don't care	保护区	Don't care	产生错误
	Don't care	Don't care	保护区	产生错误
	区域外	区域外	区域外	产生错误
其他案例				没有错误

主MPU错误发生在以下情况。

1.MMPUENEDMAC.ENABLE=1，一个或多个Regionn单元的输出为保护区域。

2.MMPUENEDMAC.ENABLE=1，所有Regionn单元的输出都在Region外。

其他情况按许可区域处理。

15.3.1.9 MMPUENDMAC:DMAC的MMPU使能寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Bus Master MPU of DMAC enable 0: Bus Master MPU of DMAC is disabled. 1: Bus Master MPU of DMAC is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the ENABLE bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

ENABLE bit (Bus Master MPU of DMAC enable)

The ENABLE bit controls enable or disable of the bus master MPU function of each master group.

When the ENABLE bit is set to 1, MMPUACDMACn (n = 0 to 7) is valid. When the ENABLE bit is set to 0, MMPUACDMACn (n = 0 to 7) is invalid for all regions. The bus master MPU function sets the ENABLE bit of each master group. When the ENABLE bit is set, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the ENABLE bit. When writing to the ENABLE bit, write 0xA5 in KEY[7:0] bits at the same time. When values other than 0xA5 are written to KEY[7:0] bits, the ENABLE bit is not updated. The KEY[7:0] bits are always read as 0x00.

15.3.1.10 MMPUENEDMAC : MMPU Enable Register for EDMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0500

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	Bus Master MPU of EDMAC enable 0: Bus Master MPU of EDMAC is disabled. 1: Bus Master MPU of EDMAC is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the ENABLE bit.	W

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

ENABLE bit (Bus Master MPU of EDMAC enable)

The ENABLE bit controls enable or disable of the bus master MPU function of each master group.

When the ENABLE bit is set to 1, MMPUACEDMACn (n = 0 to 3) is valid. When the ENABLE bit is set to 0, MMPUACEDMACn (n = 0 to 3) is invalid for all regions.

The bus master MPU function sets the ENABLE bit of each master group.

When the ENABLE bit is set, write 0xA5 in KEY[7:0] bits at the same time.

Bit	Symbol	Function	R/W
0	ENABLE	DMAC的总线主控MPU使能 0：DMAC的总线主控MPU禁用。1：DMAC的总线主控MPU使能。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对ENABLE位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

ENABLE位（DMAC的总线主控MPU使能）

ENABLE位控制每个主机组的总线主机MPU功能的启用或禁用。

当ENABLE位设置为1时，MMPUACDMACn（n=0至7）有效。当ENABLE位设置为0时，MMPUACDMACn(n=0to7)对所有地区都无效。总线主控MPU功能设置每个主控组的ENABLE位。当ENABLE位置位时，同时在KEY[7:0]中写入0xA5。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对ENABLE位的写入。写入ENABLE位时，将0xA5写入KEY[7:0]位。当0xA5以外的值写入KEY[7:0]位时，ENABLE位不会更新。
KEY[7:0]位总是读为0x00。

15.3.1.10 MMPUENEDMAC:EDMAC的MMPU使能寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0500

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ENABLE	EDMAC总线主控MPU使能 0：EDMAC的总线主控MPU禁用。1：EDMAC的总线主控MPU使能。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对ENABLE位的写入。	W

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

ENABLE位（EDMAC的总线主控MPU使能）

ENABLE位控制每个主机组的总线主机MPU功能的启用或禁用。

当ENABLE位设置为1时，MMPUACEDMACn（n=0至3）有效。当ENABLE位设置为0时，MMPUACEDMACn（n=0到3）对所有区域都无效。

总线主控MPU功能设置每个主控组的ENABLE位。

设置ENABLE位时，同时向KEY[7:0]位写入0xA5。

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the ENABLE bit. When writing to the ENABLE bit, write 0xA5 in KEY[7:0] bits at the same time. When values other than 0xA5 are written to KEY[7:0] bits, the ENABLE bit is not updated. The KEY[7:0] bits are always read as 0x00.

15.3.1.11 MMPUENPTDMAC : MMPU Enable Protect Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0104

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUENDMAC register writes are possible. 1: MMPUENDMAC register writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the MMPUENDMAC register.

When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time. When values other than 0xA5 are written in KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

15.3.1.12 MMPUENPTEDMAC : MMPU Enable Protect Register for EDMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0504

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUENEDMAC register writes are possible. 1: MMPUENEDMAC register writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对ENABLE位的写入。写入ENABLE位时，将0xA5写入KEY[7:0]位。当0xA5以外的值写入KEY[7:0]位时，ENABLE位不会更新。
KEY[7:0]位总是读为0x00。

15.3.1.11 MMPUENPTDMAC:MMPU启用DMAC的保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0104

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以写入MMPUENDMAC寄存器。1：MMPUENDMAC寄存器写受保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对MMPUENDMAC寄存器的写入。

写入PROTECT位时，同时向KEY[7:0]写入0xA5。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，将0xA5写入KEY[7:0]同时进行。当KEY[7:0]位中写入0xA5以外的值时，PROTECT位不会更新。
KEY[7:0]位总是读为0x00。

15.3.1.12 MMPUENPTEDMAC:用于EDMAC的MMPU启用保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0504

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：MMPUENEDMAC寄存器可以写。1：MMPUENEDMAC寄存器写受保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the MMPUENEDMAC register.

When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 in KEY[7:0] at the same time. When values other than 0xA5 are written in KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

15.3.1.13 MMPURPTDMAC : MMPU Regions Protect Register for DMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus Master MPU register for DMAC writing is possible. 1: Bus Master MPU register for DMAC writing is protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTDMAC.PROTECT controls the following registers:

- MMPUSDMACn (n = 0 to 7) of Non-Secure program
- MMPUEDMACn (n = 0 to 7) of Non-Secure program
- MMPUACDMACn (n = 0 to 7) of Non-Secure program

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits always read as 0x00.

Bit	Symbol	Function	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对MMPUENEDMAC寄存器的写入。

写入PROTECT位时，同时向KEY[7:0]写入0xA5。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，将0xA5写入KEY[7:0]同时进行。当KEY[7:0]位中写入0xA5以外的值时，PROTECT位不会更新。
KEY[7:0]位总是读为0x00。

15.3.1.13 MMPURPTDMAC:DMAC的MMPU区域保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0108

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以进行DMAC写入的总线主控MPU寄存器。1：用于DMAC写入的总线主控MPU寄存器受保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPURPTDMAC.PROTECT控制以下寄存器：

- ●非安全程序的MMPUSDMACn(n=0到7)
- ●非安全程序的MMPUEDMACn(n=0到7)
- ●非安全程序的MMPUACDMACn(n=0to7)

写入PROTECT位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将0xA5写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。

KEY[7:0]位总是读为0x00。

15.3.1.14 MMPURPTDMAC_SEC : MMPU Regions Protect register for DMAC Secure

Base address: RMPU = 0x4000_0000

Offset address: 0x010C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus master MPU register for DMAC secure writes are possible. 1: Bus master MPU register for DMAC secure writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTDMAC_SEC.PROTECT controls the following registers:

- MMPUSDMACn (n = 0 to 7) of Secure program
- MMPUEDMACn (n = 0 to 7) of Secure program
- MMPUACDMACn (n = 0 to 7) of Secure program

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits are always read as 0x00.

15.3.1.15 MMPURPTEDMAC : MMPU Regions Protect Register for EDMAC

Base address: RMPU = 0x4000_0000

Offset address: 0x0508

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: Bus Master MPU register for EDMAC writing is possible. 1: Bus Master MPU register for EDMAC writing is protected. Read is possible.	R/W

15.3.1.14 MMPURPTDMAC_SEC：用于DMACSecure的MMPU区域保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x010C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以进行DMAC安全写入的总线主控MPU寄存器。1：用于DMAC安全写入的总线主控MPU寄存器受到保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPURPTDMAC_SEC.PROTECT控制以下寄存器：

●Secure程序的MMPUSDMACn(n=0to7)

●安全程序的MMPUEDMACn(n=0到7)

●安全程序的MMPUACDMACn(n=0to7)

写入PROTECT位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将0xA5写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。

KEY[7:0]位总是读为0x00。

15.3.1.15 MMPURPTEDMAC:EDMAC的MMPU区域保护寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0508

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：可以进行EDMAC写入的总线主控MPU寄存器。1：EDMAC写入的总线主控MPU寄存器受保护。读取是可能的。	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code This bit is used to enable or disable writing of the PROTECT bit.	W

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPURPTEDMAC.PROTECT controls the following registers:

- MMPUSEDMACn (n = 0 to 3)
- MMPUEEDMACn (n = 0 to 3)
- MMPUACEDMACn (n = 0 to 3)

When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated.

The KEY[7:0] bits are always read as 0x00.

15.3.1.16 MMPUOAD : MMPU Operation After Detection Register

Base address: RMPU = 0x4000_0000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code This bit enables or disables writes to the OAD bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

OAD bit (Operation after detection)

The OAD bit is specified to generate either reset or non-maskable interrupt when the access to the protect region is detected by the BUS Master MPU.

When writing to the OAD bit, write 0xA5 simultaneously to the KEY[7:0] bits using halfword access.

Bit	Symbol	Function	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 该位用于启用或禁用PROTECT位的写入。	W

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPURPTEDMAC.PROTECT控制以下寄存器：

- MMPUSEDMACn (n = 0 to 3)
- MMPUEEDMACn (n = 0 to 3)
- MMPUACEDMACn (n = 0 to 3)

写入PROTECT位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将0xA5写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。

KEY[7:0]位总是读为0x00。

15.3.1.16 MMPUOAD:检测后的MMPU操作寄存器

Base address: RMPU = 0x4000_0000

Offset address: 0x0000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 该位启用或禁用对OAD位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

OAD位（检测后的操作）

当总线主控MPU检测到对保护区域的访问时，OAD位被指定为产生复位或不可屏蔽中断。

写入OAD位时，使用半字访问同时将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the OAD bit. When writing to the OAD bit, write 0xA5 simultaneously to the KEY[7:0] bits. When other values are written, the OAD bit is not updated.

The KEY[7:0] bits always read as 0x00.

15.3.1.17 MMPUOADPT : MMPU Operation After Detection Protect Register

Base address: RMPU = 0x4000_0000

Offset address: 0x0004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: MMPUOAD register writes are possible. 1: MMPUOAD register writes are protected. Read is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key code These bits enable or disable writes to the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: It is necessary to write by half word access.
Byte write access is prohibited. When byte write access is executed, operation is not guaranteed.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected.

MMPUOADPT.PROTECT controls the following register:

- MMPUOAD

When the PROTECT bit is set simultaneously, write 0xA5 to the KEY[7:0] bits using half word access.

KEY[7:0] bits (Key code)

The KEY[7:0] bits enable or disable writes to the PROTECT bit. When writing to the PROTECT bit simultaneously, write 0xA5 to the KEY[7:0] bits. When other values are written to the KEY[7:0] bits, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 0x00.

15.3.2 Operation

15.3.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

Bus Master MPU can be set for up to 8 protection regions. It is protection region when set up of permission region and protection region overlaps. It is protection region when set up of two protection region overlaps.

Bus Master MPU has master groups of DMAC/DTC and EDMAC.

Memory protection checks the address of the bus which the master group unified. Therefore, all the access of a master group is detected by memory protection.

KEY[7:0] bits (Key Code)

KEY[7:0]位启用或禁用写入OAD位。写入OAD位时，同时将0xA5写入KEY[7:0]位。写入其他值时，不会更新OAD位。

KEY[7:0]位总是读为0x00。

15.3.1.17 MMPUOADPT:检测保护寄存器后的MMPU操作

Base address: RMPU = 0x4000_0000

Offset address: 0x0004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：MMPUOAD寄存器写入是可能的。1：MMPUOAD寄存器写受保护。读取是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位启用或禁用对PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 必须通过半字访问写入。
禁止字节写访问。当执行字节写访问时，不能保证操作。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。

MMPUOADPT.PROTECT控制以下寄存器：

- MMPUOAD

当PROTECT位同时置位时，使用半字访问将0xA5写入KEY[7:0]位。

KEY[7:0] bits (Key code)

KEY[7:0]位启用或禁用对PROTECT位的写入。同时写入PROTECT位时，将0xA5写入KEY[7:0]位。当其他值写入KEY[7:0]位时，PROTECT位不会更新。KEY[7:0]位总是读为0x00。

15.3.2 Operation

15.3.2.1 内存保护

总线主控MPU使用为访问控制区域单独进行的控制设置来监视内存访问。如果检测到对受保护区域的访问，则总线主控MPU会产生内存保护错误。

总线主控MPU最多可设置8个保护区域。许可区域与保护区域的设置重叠时为保护区域。两个保护区域重叠设置时为保护区域。

总线主控MPU有DMACDTC和EDMAC主控组。

内存保护检查主组统一的总线地址。因此，一个主组的所有访问都被内存保护检测到。

The region setting registers of the Bus Master MPU for DMAC/DTC can be set for secure access and Non-Secure access using the MMPUSARA register. Make secure access and Non-Secure access settings the same for each DMAC/DTC channel and the corresponding region setting registers of the Bus Master MPU.

Bus Master MPU is permission of all regions after reset. All region is protected by setting MMPUENDMAC.ENABLE = 1 or MMPUENEDMAC.ENABLE = 1.

Each region sets up a permission region on the protection region. If access to the protected region is detected, Bus Master MPU will generate an error.

Figure 15.1 shows the use case of a bus master MPU.

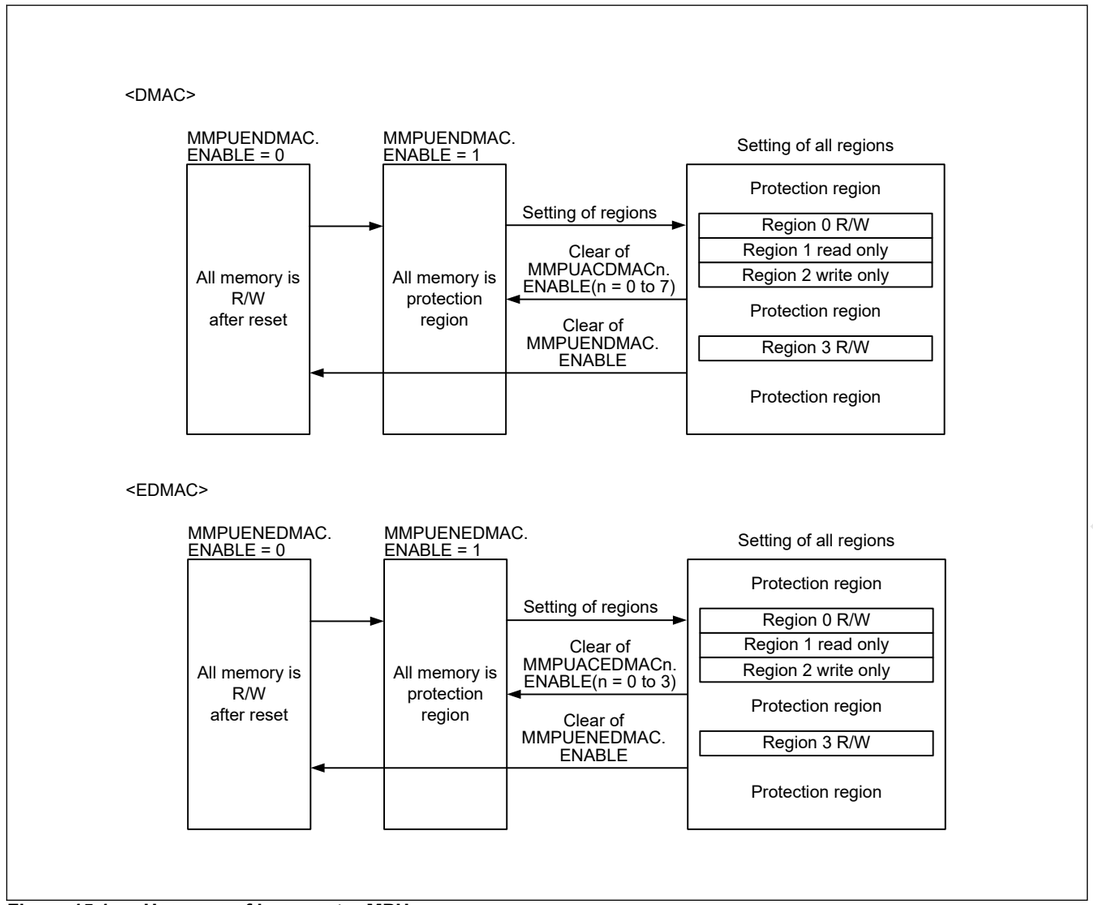

Figure 15.1 Use case of bus master MPU

Figure 15.2 shows the access permission or protection by the overlapping bus master MPU regions.

Access control for the overlapping regions is as follows:

- The region is handled as a protected region when output of one or more region units is a protected region
- The region is handled as a protected region when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

可以使用MMPUSARA寄存器为DMACDTC的总线主控MPU的区域设置寄存器设置安全访问和非安全访问。使每个DMACDTC通道和总线主控MPU的相应区域设置寄存器的安全访问和非安全访问设置相同。

BusMasterMPU是复位后所有区域的权限。通过设置MMPUENDMAC.ENABLE=1或MMPUENEDMAC.ENABLE=1来保护所有区域。

每个区域在保护区域上设置一个权限区域。如果检测到对受保护区域的访问，则总线主控MPU会产生错误。

图15.1显示了总线主控MPU的用例。

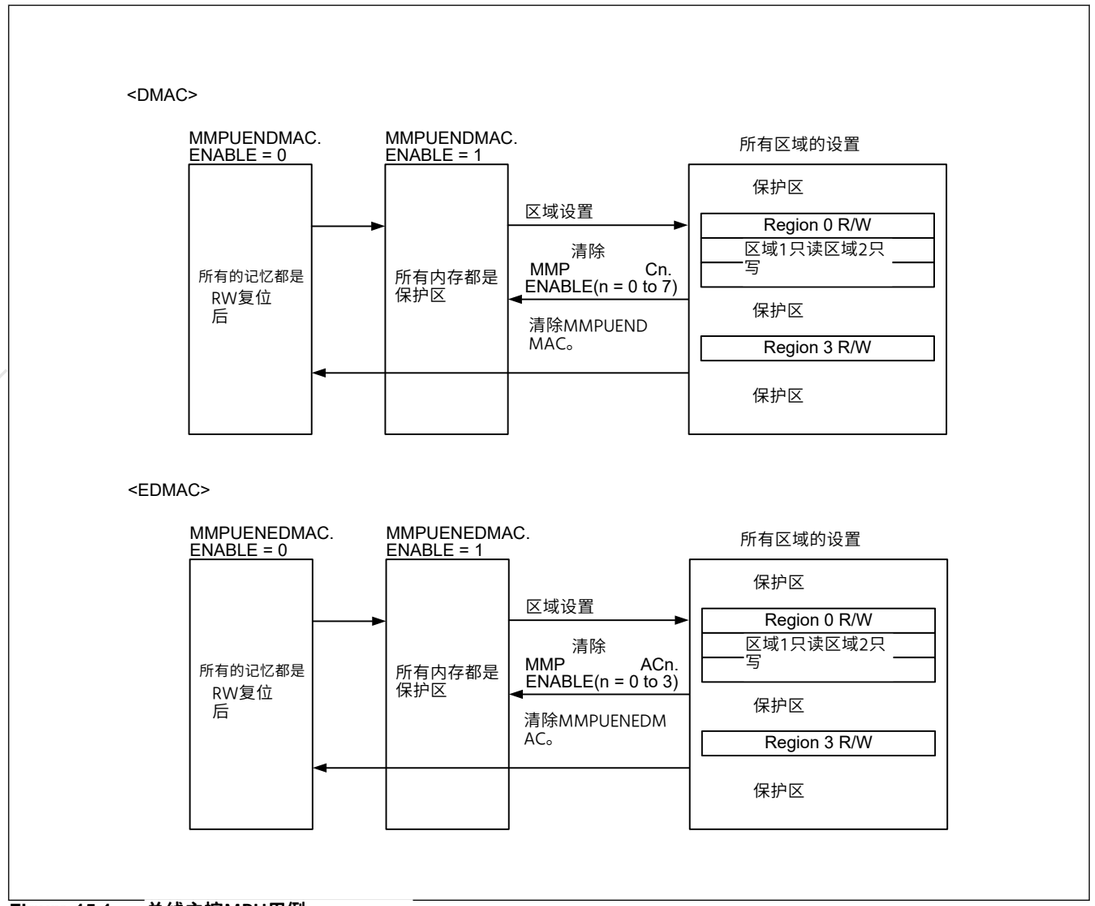

Figure 15.1 总线主控MPU用例

图15.2显示了重叠总线主控MPU区域的访问许可或保护。

重叠区域的访问控制如下：

- ●当一个或多个区域单元的输出为受保护区域时，该区域被视为受保护区域
- ●当所有区域单元的输出都在区域之外时，该区域被视为受保护区域
- ●其他情况按许可区域处理。

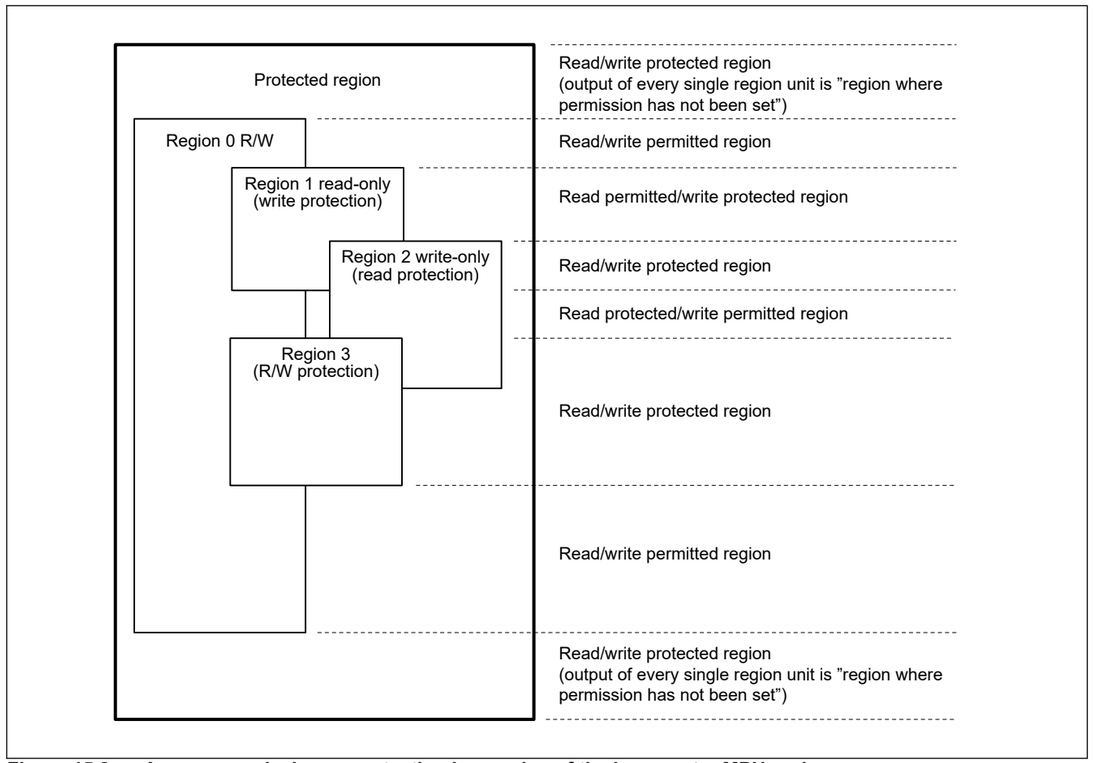

Figure 15.2 Access permission or protection by overlap of the bus master MPU regions

Figure 15.3 shows the register setting flow after reset. During this register setting, stop all bus masters except the CPU.

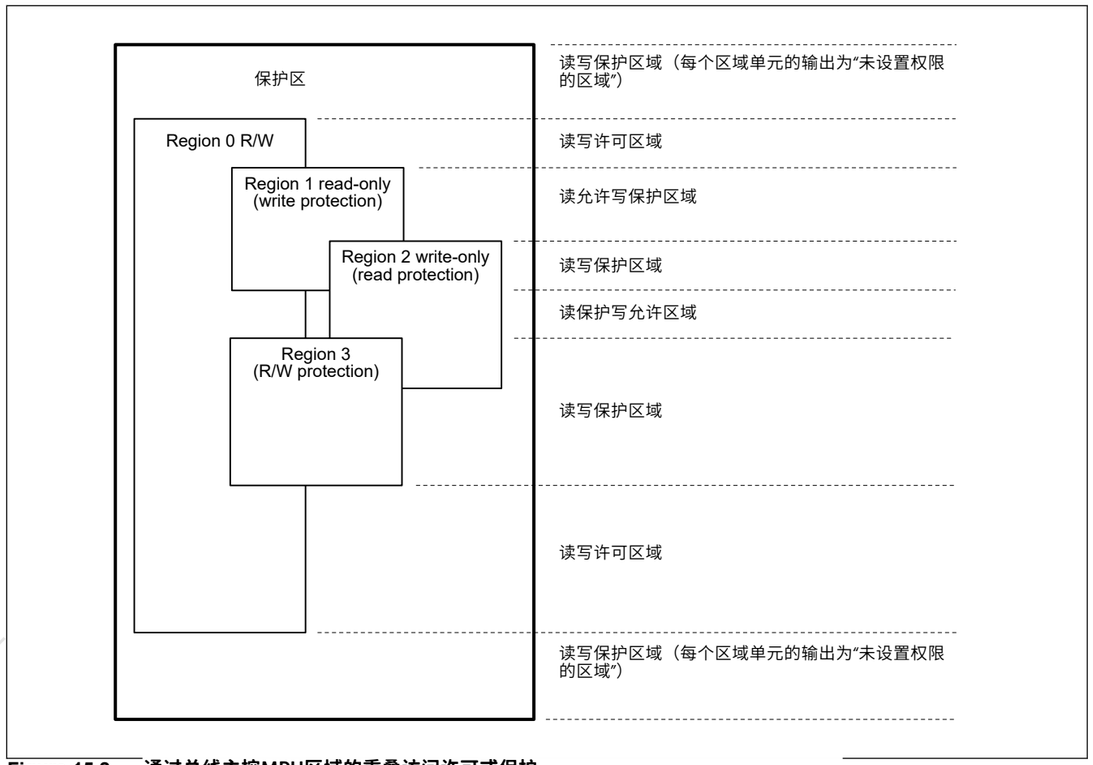

Figure 15.2 通过总线主控MPU区域的重叠访问许可或保护

图15.3显示了复位后的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有总线主机。

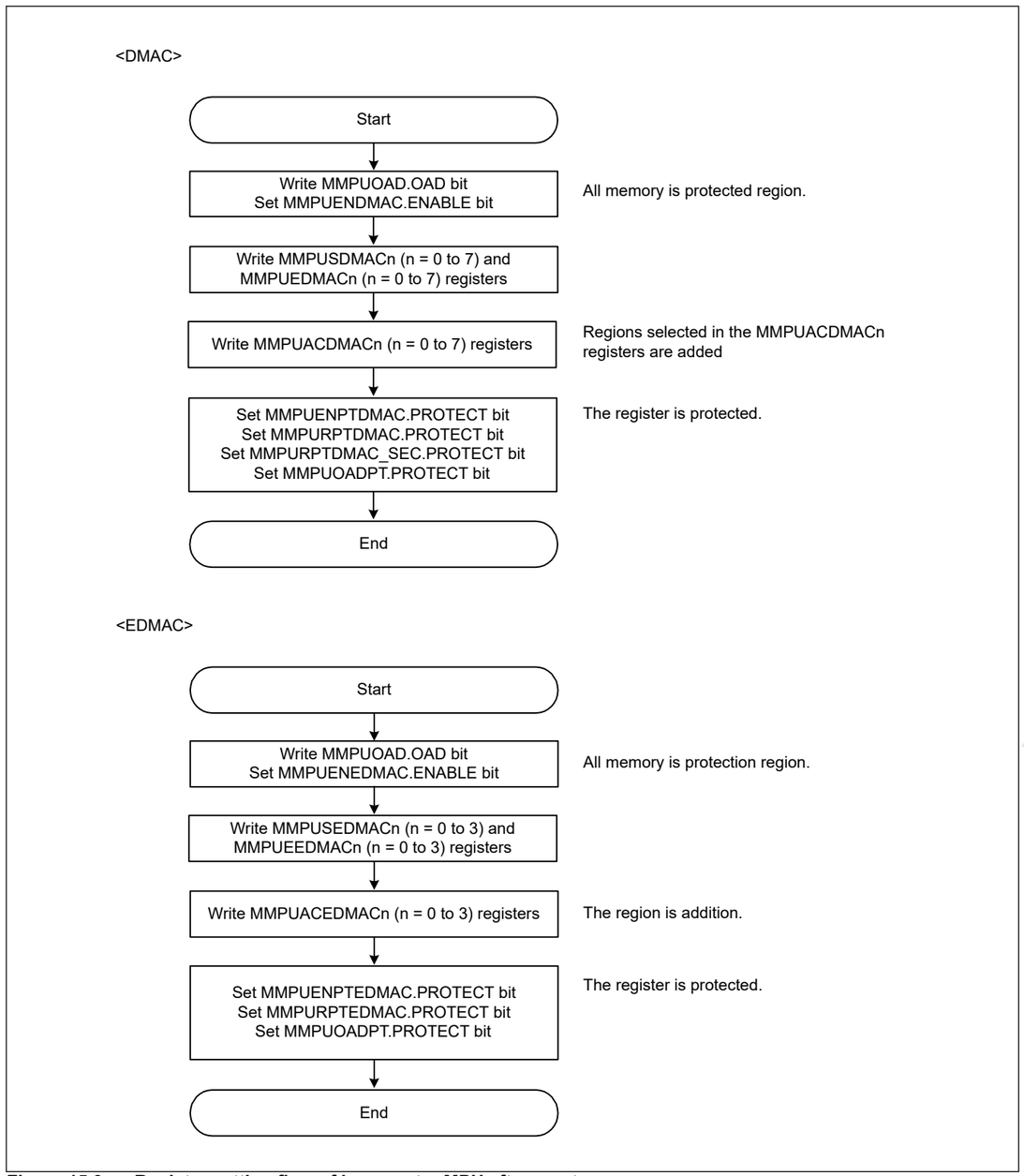

Figure 15.3 Register setting flow of bus master MPU after reset

Figure 15.4 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

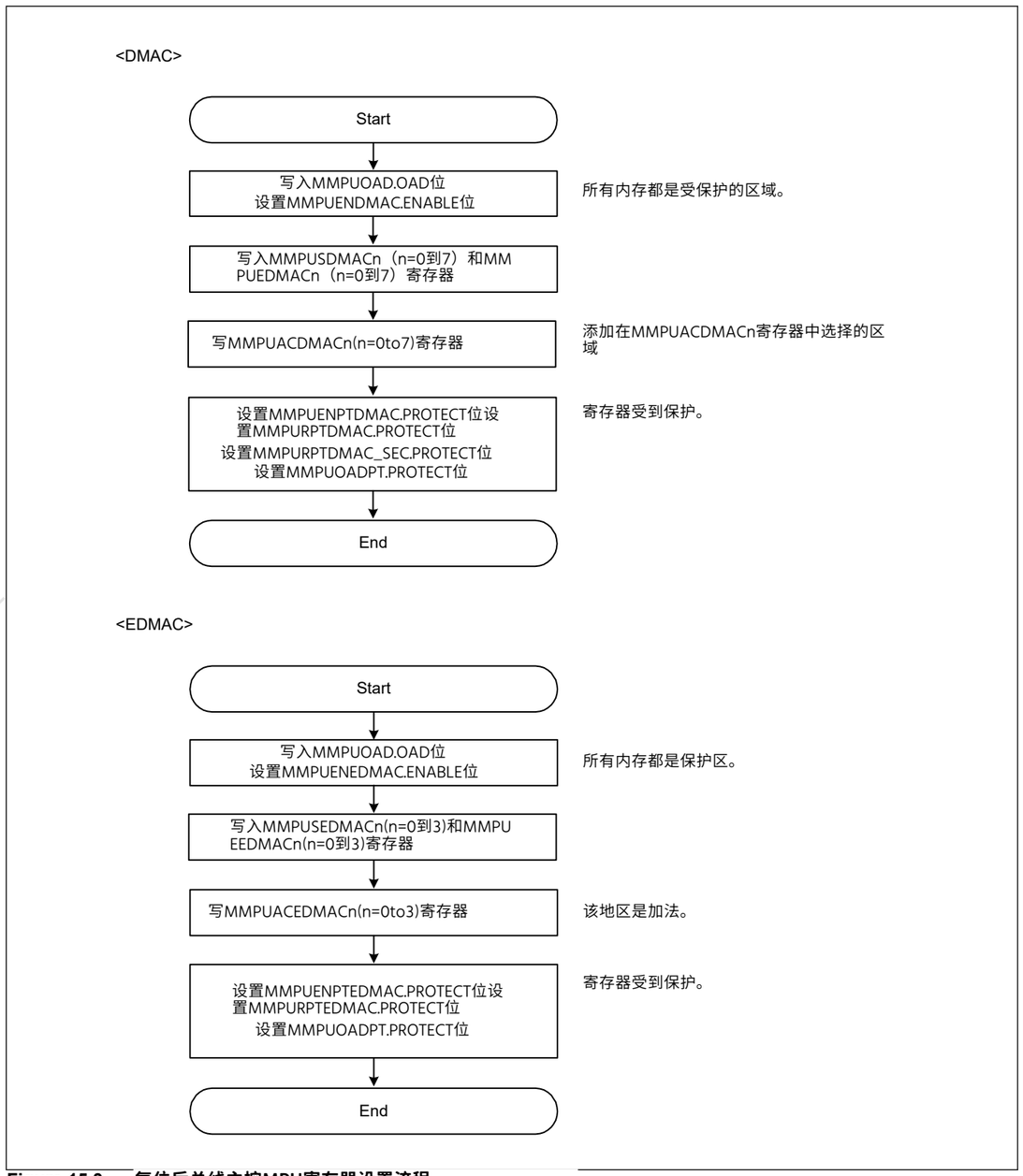

Figure 15.3 复位后总线主控MPU寄存器设置流程

图15.4显示了添加区域的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有主机。

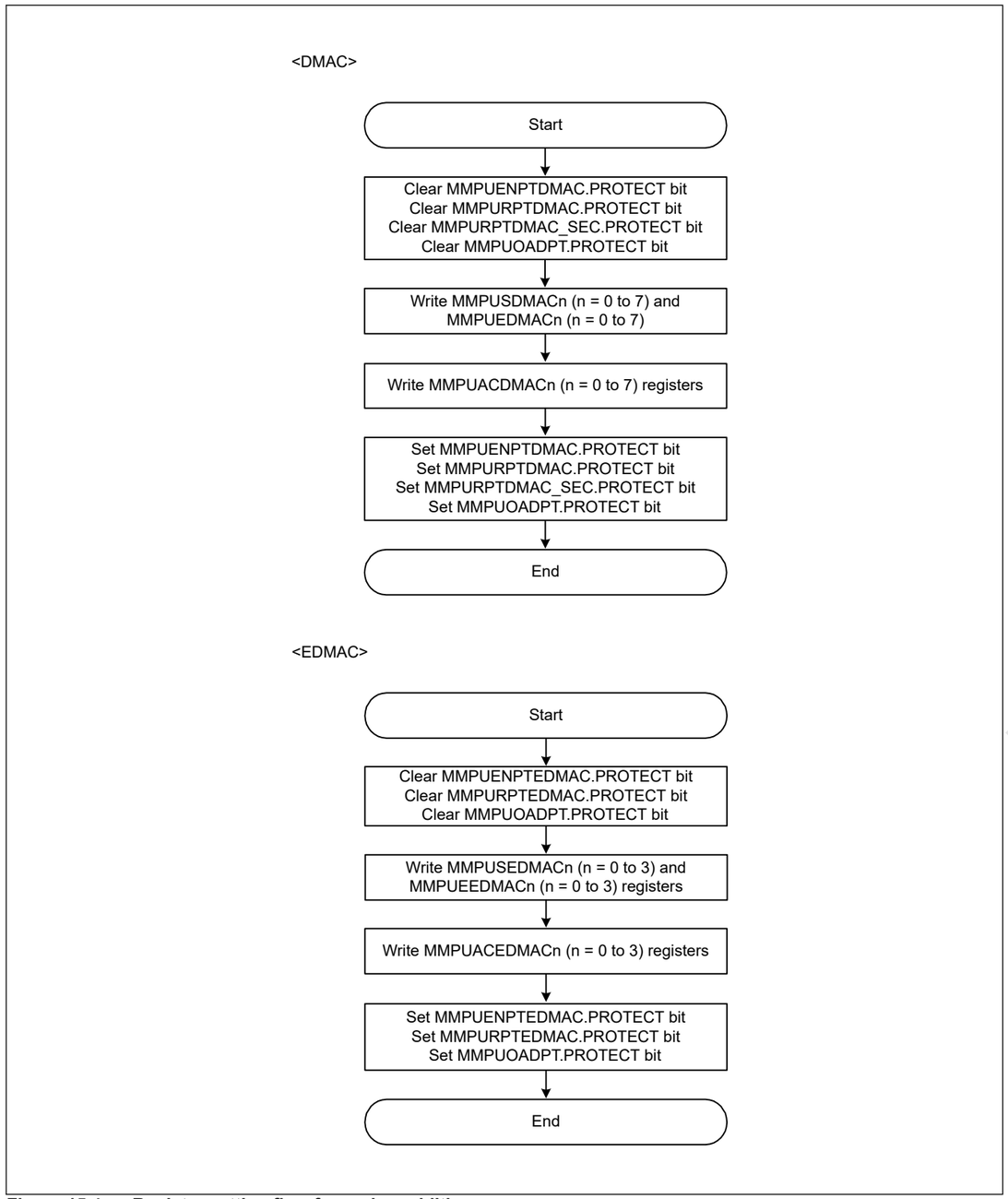

Figure 15.4 Register setting flow for region addition

15.3.2.2 Protecting the registers

Registers related to the Bus Master MPU can be protected with the PROTECT bit in the MMPUENPTDMA, MMPUENPTEDMAC, MMPURPTDMAC, MMPURPTDMAC_SEC, MMPURPTEDMAC and MMPUOADPT registers.

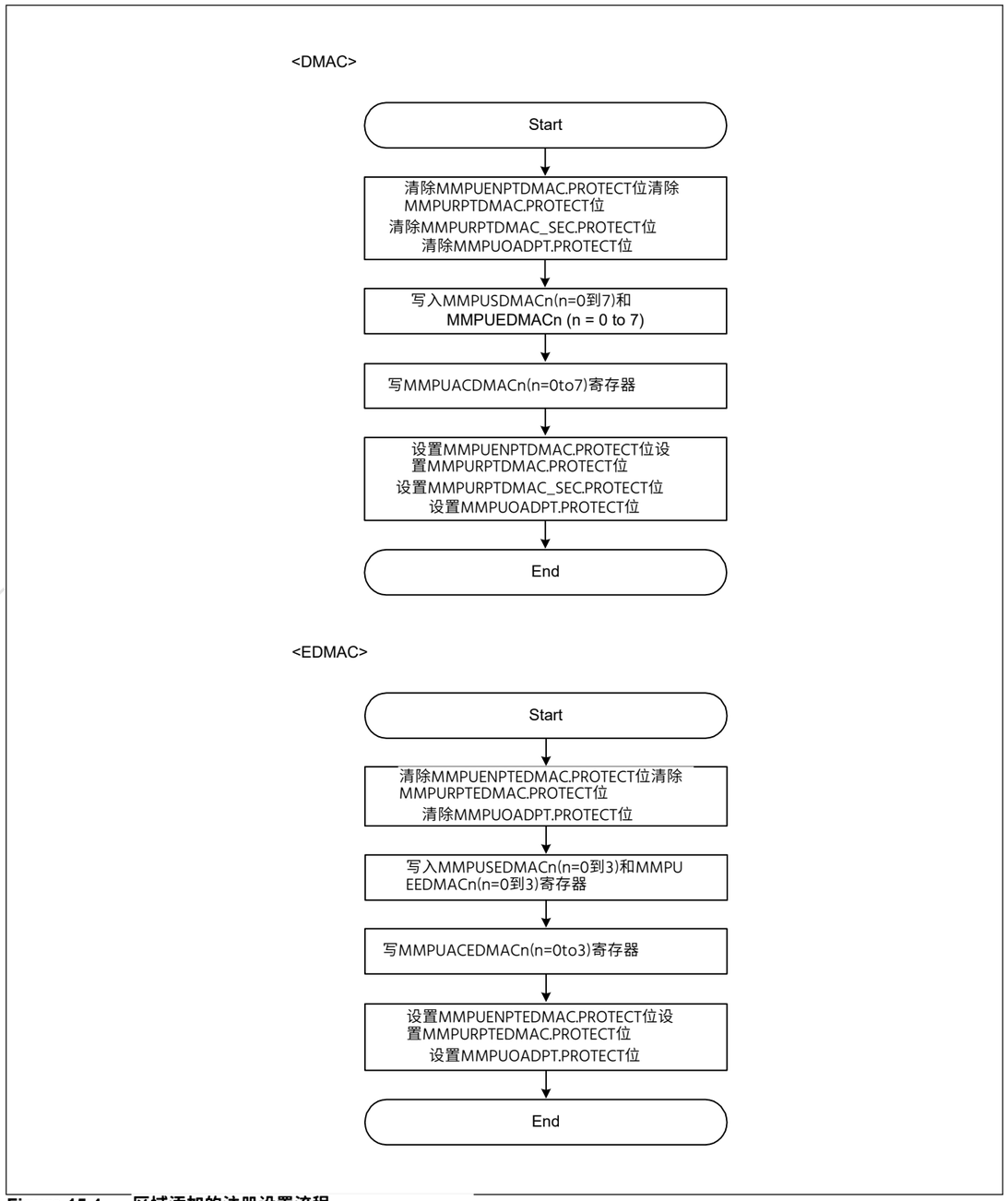

Figure 15.4 区域添加的注册设置流程

15.3.2.2 保护寄存器

与总线主控MPU相关的寄存器可以通过MMPUENPTDMA中的PROTECT位进行保护，MMPUENPTEDMAC、MMPURPTDMAC、MMPURPTDMAC_SEC、MMPURPTEDMAC和MMPUOADPT寄存器。

Table 15.8 PROTECT bit and Protected target registers

PROTECT bit	Protect target registers
MMPUENPTDMAC.PROTECT	MMPUENDMAC
MMPUENPTEDMAC.PROTECT	MMPUENEDMAC
MMPURPTDMAC.PROTECT	The following registers set to Non-Secure by MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPURPTDMAC_SEC.PROTECT	The following registers set to Secure by MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPURPTEDMAC.PROTECT	MMPUSEDMACn (n = 0 to 3) MMPUEEDMACn (n = 0 to 3) MMPUACEDMACn (n = 0 to 3)
MMPUOADPT.PROTECT	MMPUOAD

15.3.2.3 Memory protection error

If access to a protected region is detected, the bus master MPU generates an error. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or a reset.

A non-maskable interrupt or a reset is shared between bus master MPU Group DMAC/DTC and EDMAC.

The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST. For details, see section 13, Interrupt Controller Unit (ICU). The reset status is indicated in SYSTEM.RSTSR1.BUSMRF. For details, see section 5, Resets.

15.4 References

1. *Arm®v8-M Architecture Reference Manual* (ARM DDI0553B.g)
2. *Arm® Cortex®-M33 Processor Technical Reference Manual* (ARM 100230_0004_00_en)

Table 15.8 PROTECT位和受保护的目标寄存器

保护位	保护目标寄存器
MMPUENPTDMAC.PROTECT	MMPUENDMAC
MMPUENPTEDMAC.PROTECT	MMPUENEDMAC
MMPURPTDMAC.PROTECT	以下寄存器设置为非安全由 MMPUSARA.MMPUASAn (n = 0 to 7). MMPUSDMACn (n = 0 to 7) MMPUEDMACn (n = 0 to 7) MMPUACDMACn (n = 0 to 7)
MMPURPTDMAC_SEC.PROTECT	以下寄存器由MMPUSARA.MMPUASan（n=0到7）设置为Secure。 MMPUSDMACn（n=0到7）MMPUEDMACn（n=0到7） MMPUACDMACn (n = 0 to 7)
MMPURPTEDMAC.PROTECT	MMPUSEDMACn (n = 0 to 3) MMPUEEDMACn (n = 0 to 3) MMPUACEDMACn (n = 0 to 3)
MMPUOADPT.PROTECT	MMPUOAD

15.3.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线主控MPU会产生错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。

总线主控MPU组DMACDTC和EDMAC共享不可屏蔽中断或复位。

不可屏蔽中断状态在ICU.NMISR.BUSMST中指示。有关详细信息，请参阅第13节，中断控制器单位（ICU）。复位状态在SYSTEM.RSTSR1.BUSMRF中指示。有关详细信息，请参阅第5节，重置。

15.4 References

1.Arm®v8-M架构参考手册（ARMDDI0553B.g）
2.Arm®Cortex®-M33处理器技术参考手册（ARM100230_0004_00_en）

16. DMA Controller (DMAC)

16.1 Overview

The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 16.1 lists the DMAC specifications, and Figure 16.1 shows a block diagram of the DMAC.

Table 16.1 DMAC specifications (1 of 2)

Item		Description
Number of channels		8 channels (DMACn (n = 0 to 7))
Transfer space		4 GB (0x00000000 to 0xFFFFFFFF excluding reserved areas)
Maximum transfer volume		64 M data (Maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks)
DMAC activation source		Selectable for each channel: ● Software trigger ● Interrupt requests from peripheral modules or trigger from external interrupt input pins.*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	● One data transfer by one DMA transfer request ● Free running function (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	● One data transfer by one DMA transfer request ● Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. ● Maximum settable repeat size: 1,024 ● Selectable free running function
	Repeat-block transfer mode	● One block data transfer by one DMA transfer request ● Maximum settable block size: 1,024 ● Block transfer can be repeated ● Maximum settable repeat size: 64K ● Selectable free running function
	Block transfer mode	● One block data transfer by one DMA transfer request ● Maximum settable block size: 1,024 data ● Selectable free running function
Selective functions	Extended repeat area function	● Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed ● Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination
Processing on DMAC transfer error		● When the DMAC transfer error occurs, it is stop the transfer that caused the error channel ● Request to clear the register for activation request of DMAC error channel to ICU
Interrupt (DMACn_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	● Generated when the repeat size of data transfer is completed. ● Generated when the source address extended repeat area overflows. ● Generated when the destination address extended repeat area overflows.
Interrupt (DMA_TRANSERR)	Error response detection interrupt	● Generated when the DMAC transfer error occurs
Event link activation (DMACn_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred).

16. DMA Controller (DMAC)

16.1 Overview

MCU包括一个8通道直接内存访问控制器(DMAC)，无需CPU干预即可传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。

表16.1列出了DMAC规范，图16.1显示了DMAC的框图。

Table 16.1 DMAC规格(1of2)

Item		Description
通道数		8个通道（DMACn（n=0到7））
转移空间		4GB（0x00000000到0xFFFFFFFF不包括保留区域）
最大传输量		64M数据（块传输模式下的最大传输数：1 024数据×65 536块）
DMAC激活源		每个通道可选择：● 软件触发 ● 来自外围模块的中断请求或来自外部中断输入引脚的触发。*1
通道优先级		Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest)
传输数据	单一数据	位长：8、16、32位
	块大小	数据数量：1至1 024
传输模式	正常传输模式	● 1个DMA传输请求1个数据传输 ● 自由运行功能（不指定数据传输总数的设置）可设置
	重复传输模式	● 1个DMA传输请求1个数据传输 ● 为传输源或目标指定的重复数据传输大小完成后，程序返回传输起始地址。 ● 最大可设置重复大小：1 024 ● 可选择的自由运行功能
	重复块传输模式	● 1个DMA传输请求的1个块数据传输 ● 最大可设置块大小：1 024 ● 块传输可以重复 ● 最大可设置重复大小：64K ● 可选择的自由运行功能
	块传输模式	● 1个DMA传输请求的1个块数据传输 ● 最大可设置块大小：1 024个数据 ● 可选择的自由运行功能
选择性功能	扩展重复区域功能	● 可以通过重复指定范围内的地址值来传输数据的功能，其中传输地址寄存器中的高位值是固定的 ● 2字节至128兆字节的区域可单独设置为传输源和目标的扩展重复区域
处理DMAC传输错误		● 当发生DMAC传输错误时，是停止传输导致错误通道 ● 请求清除寄存器以激活对ICU的DMAC错误通道的请求
Interrupt (DMACn_INT)	传输结束中断	在传输计数器指定的传输数据量完成时生成。
	传输转义结束中断	● 数据传输的重复大小完成时生成。 ● 当源地址扩展重复区溢出时产生。 ● 当目标地址扩展重复区溢出时产生。
Interrupt (DMA_TRANSERR)	错误响应检测中断	● 发生DMAC传输错误时生成
事件链接激活(DMACn_INT)		每次数据传输后都会生成一个事件链接请求（对于块传输，在每个块传输后）。

Table 16.1 DMAC specifications (2 of 2)

Item	Description
Master TrustZone Filter	TrustZone violation area of Flash and SRAM is detected before a non-secure channel access the bus.
Power consumption reduction function	Module-stop state can be set.
TrustZone Filter	Security attribution can be set for each channels

Note: Security attribution Register of DMAC channel is described in ICU.ICUSARC
Note 1. For details on DMAC activation sources, see Table 13.4 in section 13, Interrupt Controller Unit (ICU).

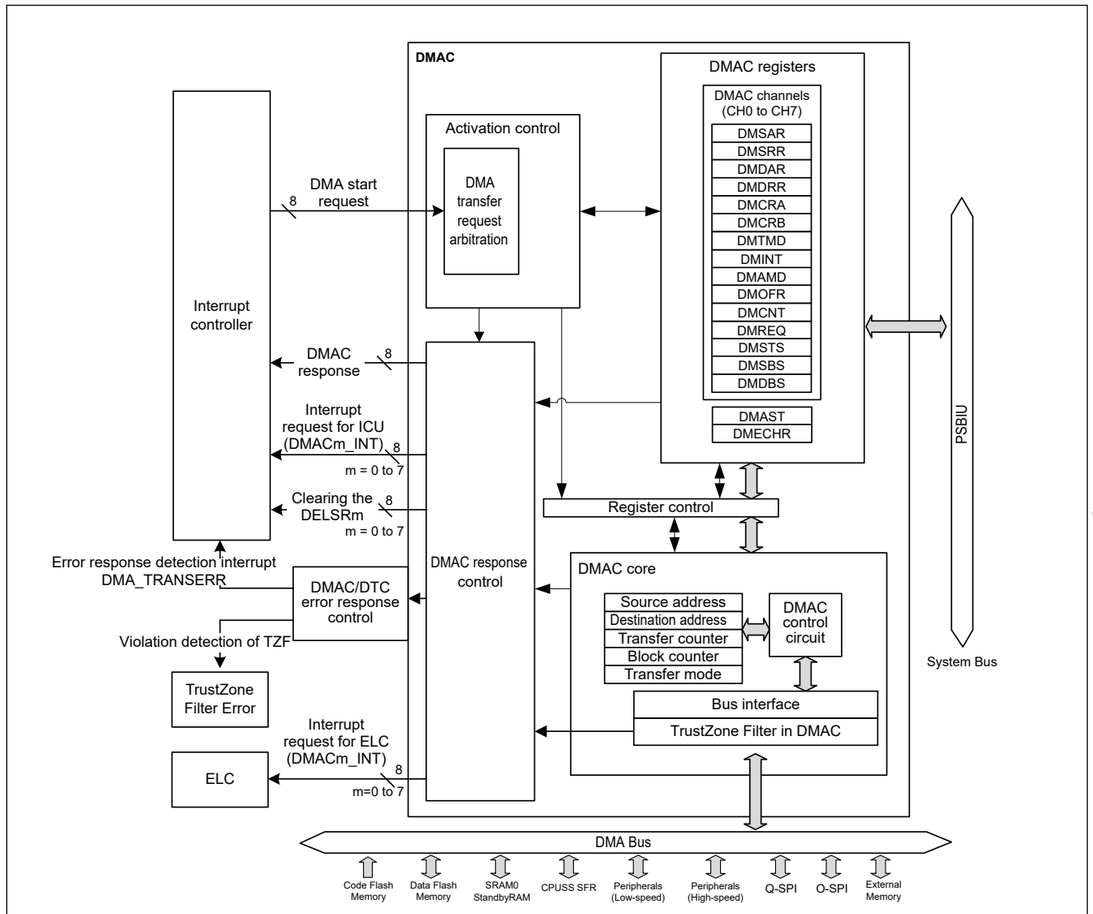

Figure 16.1 Block Diagram of DMAC

Table 16.1 DMAC规范（2个中的2个）

Item	Description
主信任区过滤器	在非安全通道访问总线之前检测到Flash和SRAM的TrustZone违规区域。
功耗降低功能	可设置模块停止状态。
TrustZone Filter	可以为每个通道设置安全属性

Note: ICU.ICUSARC中描述了DMAC通道的安全属性寄存器
注1.有关DMAC激活源的详细信息，请参见第13节“中断控制器单元(ICU)”中的表13.4。

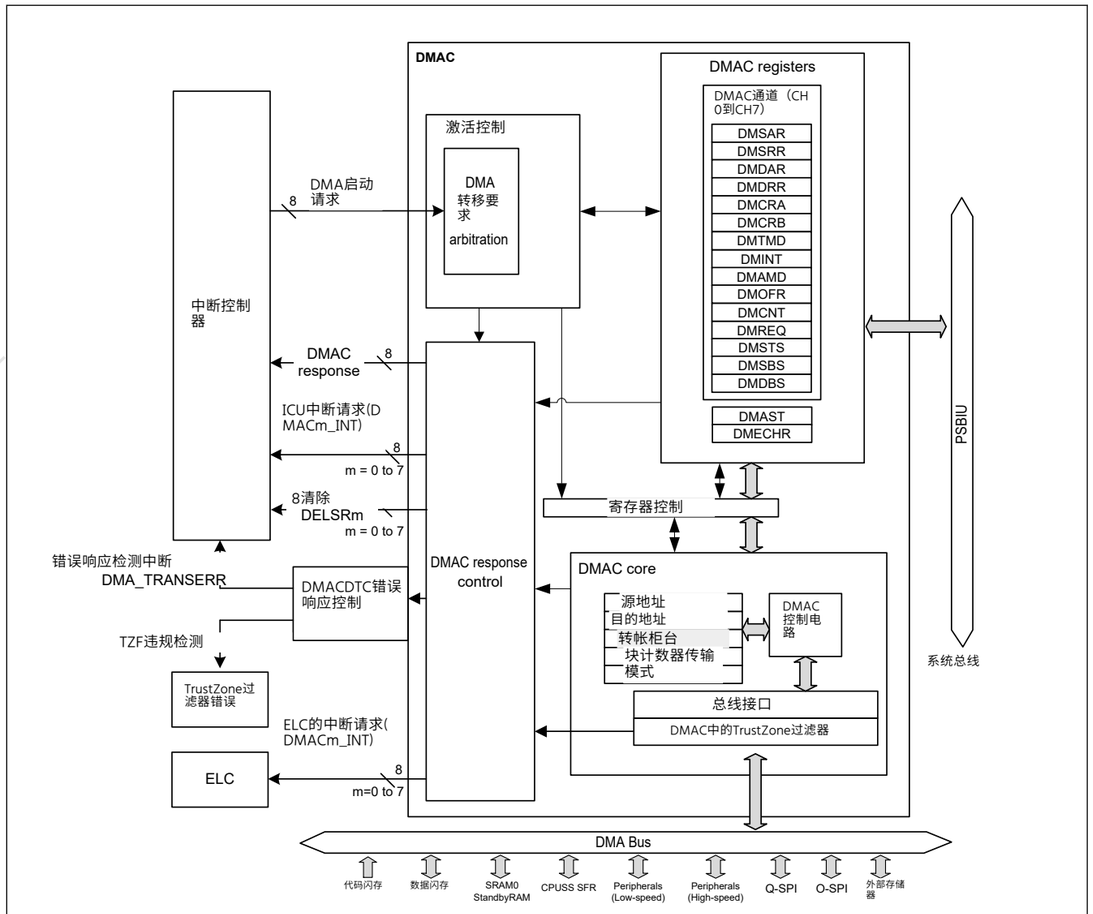

Figure 16.1 DMAC框图

16.2 Register Descriptions

16.2.1 DMACSAR : DMAC Controller Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMASTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DMASTSA	DMAST Security Attribution 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

For DMAC, security attribution is set for each channel. However, this register only sets the DMAST register security attribute. The security attribution setting of each channel is described in the section 13.2.3. ICUSARC : Interrupt Controller Unit Security Attribution Register C.

DMASTSA bit (DMAST Security Attribution)

Security attributes of registers for DMAST. Do not write to DMASTSA bit while DMA transfer is enabled or a bus master is writing to the DMA registers.

16.2.2 DMSAR : DMA Source Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x00

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer source start address Setting range is 0x00000000 to 0xFFFFFFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMSAR while DMAC activation is disabled (the DMAST.DMST bit = 0) or DMA transfer is disabled (the DMCNT.DTE bit = 0).

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

16.2 注册说明

16.2.1 DMACSAR:DMAC控制器安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMASTSA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DMASTSA	DMAST安全归因 0: Secure 1: Non-secure	R/W
31:1	—	这些位读为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

对于DMAC，为每个通道设置安全属性。但是，该寄存器仅设置DMAST寄存器安全属性。每个通道的安全属性设置在13.2.3小节中描述。ICUSARC：中断控制器单元安全属性寄存器C。

DMASTSA位（DMAST安全属性）

DMAST寄存器的安全属性。在启用DMA传输或总线主机正在写入DMA寄存器时，不要写入DMASTSA位。

16.2.2 DMSAR：DMA源地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x00

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输源起始地址 设置范围是0x00000000到0xFFFFFFFF（4GB）。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活（DMAST.DMST位=0）或禁用DMA传输（DMCNT.DTE bit = 0).

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

16.2.3 DMSRR : DMA Source Reload Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x20

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer source reload address 0x0000 0000 to 0xFFFF FFFF (4 Gbytes)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMSRR while DMAC activation is disabled (DMAST.DMST = 0) or DMA transfer is disabled (DMCNT.DTE = 0).

DMSRR is initial value of DMSAR. In repeat-block transfer mode, DMSAR reloads value of DMSRR after specified transfer finished.

In normal transfer mode, repeat transfer mode and block transfer mode, DMSRR is not used. The setting is invalid.

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

16.2.4 DMDAR : DMA Destination Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer destination start address setting range is 0x00000000 to 0xFFFFFFFF (4 Gbytes).	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMDAR while DMAC activation is disabled (the DMAST.DMST bit = 0) or DMA transfer is disabled (the DMCNT.DTE bit = 0).

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

16.2.3 DMSRR:DMA源重载地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x20

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输源重载地址0x00000000到0xFFFFF FFF(4GB)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活(DMAST.DMST=0)或禁用DMA传输(DMCNT.DTE=0)时设置DMSRR。

DMSRR是DMSAR的初始值。在重复块传输模式下，DMSAR在指定传输完成后重新加载DMSRR的值。

在正常传输模式、重复传输模式和块传输模式下，不使用DMSRR。设置无效。

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

16.2.4 DMDAR:DMA目标地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x04

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输目标起始地址设置范围为0x00000000到0xFFFF FFFF(4GB)。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活（DMAST.DMST位=0）或禁用DMA传输（
DMCNT.DTE bit = 0).

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

16.2.5 DMDRR : DMA Destination Reload Address Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x24

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the transfer destination reload address 0000 0000h to FFFF FFFFh (4 Gbytes)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set DMDRR while DMAC activation is disabled (the DMAST.DMST bit = 0) or DMA transfer is disabled (the DMCNT.DTE bit = 0).

DMDRR is initial value of DMDAR. In repeat-block transfer mode, DMDAR reloads value of DMDRR after specified transfer finished.

In normal transfer mode, repeat transfer mode and block transfer mode, DMDRR is not used. The setting is invalid.

Note: Address alignment in this register must match the Transfer Data Size value selected in the DMTMD.SZ bit.

16.2.6 DMCRA : DMA Transfer Count Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	DMCRAH[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRAL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRAL[15:0]	Lower bits of transfer count Specifies the number of transfer operations.	R/W
25:16	DMCRAH[9:0]	Upper bits of transfer count Specifies the number of transfer operations.	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMCRAH and DMCRAL in repeat transfer mode and block transfer mode. Bits 15 to 10 are fixed to 0 in repeat transfer mode and block transfer mode.

16.2.5 DMDRR:DMA目标重载地址寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x24

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	指定传输目标重载地址00000000h至FFFFFFFFh(4GB)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在禁用DMAC激活（DMAST.DMST位=0）或禁用DMA传输（
DMCNT.DTE bit = 0).

DMDRR是DMDAR的初始值。在重复块传输模式下，DMDAR在指定传输完成后重新加载DMDRR的值。

在正常传输模式、重复传输模式和块传输模式下，不使用DMDRR。设置无效。

Note: 该寄存器中的地址对齐必须与在DMTMD.SZ位中选择的传输数据大小值相匹配。

16.2.6 DMCRA:DMA传输计数寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	DMCRAH[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRAL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRAL[15:0]	传输计数的低位 指定传输操作的数量。	R/W
25:16	DMCRAH[9:0]	传输计数的高位 指定传输操作的数量。	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在重复传输模式和块传输模式下，为DMCRAH和DMCRAL设置相同的值。在重复传输模式和块传输模式中，位15到10固定为0。

(1) Normal Transfer Mode (DMTMD.MD[1:0] = 00b)

DMCRAL functions as a 16-bit transfer counter.

The number of transfer operations is one when the setting is 0x0001, and 65,535 when it is 0xFFFF. The value is decremented by one each time data is transferred.

When the setting is 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running function).

Free running function is not selected by DMTMD.TKP bit in normal transfer mode.

DMCRAH is not used in normal transfer mode. Write 0x0000 to DMCRAH.

(2) Repeat Transfer Mode (DMTMD.MD[1:0] = 01b)

DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter.

The number of transfer operations is one when the setting is 0x001, 1,023 when it is 0x3FF, and 1,024 when it is 0x000. In repeat transfer mode, a value in the range of 0x000 to 0x3FF (1 to 1,024) can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

(3) Block Transfer Mode (DMTMD.MD[1:0] = 10b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

The block size is one when the setting is 0x001, 1,023 when it is 0x3FF, and 1,024 when it is 0x000. In block transfer mode, a value in the range of 0x000 to 0x3FF can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 0x000, at which the value in DMCRAH is loaded into DMCRAL.

(4) Repeat-Block Transfer Mode (DMTMD.MD[1:0] = 11b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In repeat-block transfer mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which the value in DMCRAH is loaded into DMCRAL.

16.2.7 DMCRB : DMA Block Transfer Count Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMCRBH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRBL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) 正常传输模式（DMTMD.MD[1:0]=00b）

DMCRAL用作16位传输计数器。

设置为0x0001时传输操作数为1，设置为0xFFFF时为65 535。每次传输数据时，该值减一。

设置为0x0000时，不设置具体的传输操作次数；在传输计数器停止的情况下执行数据传输（自由运行功能）。

在正常传输模式下，DMMTD.TKP位不选择自由运行功能。

DMCRAH不用于正常传输模式。将0x0000写入DMCRAH。

(2) 重复传输模式(DMTMD.MD[1:0]=01b)

DMCRAH指定重复大小，DMCRAL用作10位传输计数器。

设置为0x001时传输操作数为1，设置为0x3FF时为1 023，设置为0x000时为1 024。在重复传输模式下，可以为DMCRAH和DMCRAL设置0x000到0x3FF（1到1 024）范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。

每次传输数据时，DMCRAL中的值减1，直到到达0x000，此时DMCRAL中的值DMCRAH被加载到DMCRAL中。

(3) 块传输模式（DMTMD.MD[1:0]=10b）

DMCRAH指定块大小，DMCRAL用作10位块大小计数器。

设置为0x001时块大小为1，设置为0x3FF时为1 023，设置为0x000时为1 024。在块传输模式下，可以为DMCRAH和DMCRAL设置0x000到0x3FF范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。

每次传输数据时，DMCRAL中的值减1，直到到达0x000，此时DMCRAL中的值DMCRAH被加载到DMCRAL中。

(4) 重复块传输模式(DMTMD.MD[1:0]=11b)

DMCRAH指定块大小，DMCRAL用作10位块大小计数器。

设置为001h时块大小为1，设置为3FFh时为1023，设置为000h时为1024。在重复块传输模式下，可以为DMCRAH和DMCRAL设置000h到3FFh范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。

每次传输数据时，DMCRAL中的值减1，直到达到000h，此时DMCRAL中的值DMCRAH被加载到DMCRAL中。

16.2.7 DMCRB:DMA块传输计数寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMCRBH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMCRBL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMCRBL[15:0]	Functions as a number of block, repeat or repeat-block transfer counter. 0001h to FFFFh (1 to 65,535) 0000h (65,536)	R/W
31:16	DMCRBH[15:0]	Specifies the number of block, repeat or repeat-block transfer operations. 0001h to FFFFh (1 to 65,535) 0000h (65,536)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Set the same value for DMCRBH and DMCRBL in repeat transfer mode, block transfer mode and repeat-block transfer mode.

DMCRBH specifies the number of block, repeat and repeat-block transfer operations, and DMCRBL functions as a 16-bit the number of block counter in block, repeat, repeat-block transfer mode, respectively.

The number of transfer operations is one when the setting is 0001h, 65,535 when it is FFFFh, and 65,536 when it is 0000h.

In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred.

In block transfer mode and repeat-block transfer mode, the value is decremented by one when the final data of one block size is transferred.

In normal transfer mode, DMCRB is not used. The setting is invalid.

When DMTMD.TKP is 1 and final data of one repeat size or one block size is transferred, DMCRBL reloads value of DMCRBH automatically.

16.2.8 DMTMD : DMA Transfer Mode Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		DTS[1:0]		—	TKP	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	DCTG[1:0]	Transfer Request Source Select 0 0: Software request 0 1: Hardware request*1 1 0: Setting prohibited 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	SZ[1:0]	Transfer Data Size Select 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	R/W
10	TKP	Transfer Keeping 0: Transfer is stopped by completion of specified total number of transfer operations. 1: Transfer is not stopped by completion of specified total number of transfer operations. (free-running)	R/W
11	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
15:0	DMCRBL[15:0]	用作多个块、重复或重复块传输计数器。0001h至FFFFh(1至65 535)0000 0h(65 536)	R/W
31:16	DMCRBH[15:0]	指定块、重复或重复块传输操作的数量。0001h至FFFFh(1至65 535)0000 h(65 536)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在重复传输模式、块传输模式和重复块传输模式中，将DMCRBH和DMCRBL设置为相同的值。

DMCRBH指定块、重复和重复块传输操作的数量，DMCRBL分别用作块、重复、重复块传输模式下的16位块数计数器。

设置为0001h时传输操作数为1，设置为FFFFh时为65 535，设置为0000h时为65 536。

在重复传输模式下，当传输一个重复大小的最终数据时，该值减一。

在块传输模式和重复块传输模式中，当传输一个块大小的最终数据时，该值减一。

在正常传输模式下，不使用DMCRB。设置无效。

当DMTMD.TKP为1并且传输一个重复大小或一个块大小的最终数据时，DMCRBL重新加载值
DMCRBH automatically.

16.2.8 DMTMD:DMA传输模式寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		DTS[1:0]		—	TKP	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	DCTG[1:0]	传输请求源选择 00：软件请求01：硬件 请求*1 10：禁止设置11：禁 止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
9:8	SZ[1:0]	传输数据大小选择 00：8位01：16位10 ：32位11：禁止设置	R/W
10	TKP	转让保管 0：完成指定的传输操作总数后停止传输。1：完成指定的传输操作总数后传输不会停止。（自由奔跑）	R/W
11	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13:12	DTS[1:0]	Repeat Area Select 0 0: The destination is specified as the repeat area or block area 0 1: The source is specified as the repeat area or block area 1 0: The repeat area or block area is not specified 1 1: Setting prohibited	R/W
15:14	MD[1:0]	Transfer Mode Select 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Repeat-block transfer	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note 1. To select the DMAC activation source, use the DELSRn registers of the ICU. For details on DMAC activation sources, see Table 13.4 in section 13, Interrupt Controller Unit (ICU).

DTS[1:0] bits (Repeat Area Select)

DTS[1:0] select either the source or destination as the repeat area in repeat or block transfer mode. In normal or repeat-block transfer mode, setting these bits is invalid.

TKP bits (Transfer Keeping)

TKP selects either stopping transfer or keeping transfer by completion of specified total number of transfer operations in repeat, block or repeat-block transfer mode. In normal transfer mode, setting these bits is invalid.

16.2.9 DMINT : DMA Interrupt Setting Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable 0: Disables an interrupt request for an extended repeat area overflow on the destination address 1: Enables an interrupt request for an extended repeat area overflow on the destination address	R/W
1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable 0: Disables an interrupt request for an extended repeat area overflow on the source address 1: Enables an interrupt request for an extended repeat area overflow on the source address	R/W
2	RPTIE	Repeat Size End Interrupt Enable 0: Disables the repeat size end interrupt request 1: Enables the repeat size end interrupt request	R/W
3	ESIE	Transfer Escape End Interrupt Enable 0: Disables the transfer escape end interrupt request 1: Enables the transfer escape end interrupt request	R/W
4	DTIE	Transfer End Interrupt Enable 0: Disables the transfer end interrupt request 1: Enables the transfer end interrupt request	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
13:12	DTS[1:0]	重复区域选择 00：目标指定为重复区域或块区域01：源指定为重复区域或块区域10：不指定重复区域或块区域11：设置禁止	R/W
15:14	MD[1:0]	传输模式选择 00：正常传输01：重复传输10：块传输11：重复块传输	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

注1.要选择DMAC激活源，请使用ICU的DELSRn寄存器。有关DMAC激活源的详细信息，请参见第13节“中断控制器单元(ICU)”中的表13.4。

DTS[1:0]位（重复区域选择）

DTS[1:0]在重复或块传输模式中选择源或目标作为重复区域。在正常或重复块传输模式下，设置这些位无效。

TKP bits (Transfer Keeping)

TKP通过在重复、块或重复块传输模式下完成指定的传输操作总数来选择停止传输或保持传输。在正常传输模式下，设置这些位无效。

16.2.9 DMINT:DMA中断设置寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DARIE	目标地址扩展重复区溢出中断使能 0：禁用目标地址上扩展重复区域溢出的中断请求 1：使能目标地址上扩展重复区域溢出的中断请求	R/W
1	SARIE	源地址扩展重复区溢出中断使能 0：禁用源地址上扩展重复区域溢出的中断请求 1：使能源地址上扩展重复区域溢出的中断请求	R/W
2	RPTIE	重复大小结束中断使能 0：禁用重复大小结束中断请求1：启用重复大小结束中断请求	R/W
3	ESIE	传输转义结束中断使能 0：禁用传输转义结束中断请求1：启用传输转义结束中断请求	R/W
4	DTIE	传输结束中断使能 0：禁止传输结束中断请求1：允许传输结束中断请求	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DARIE bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the destination address occurs while DARIE bit is set to 1, the DMCNT.DTE bit is cleared to 0. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that an interrupt by an extended repeat area overflow on the destination address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DMCNT.DTE bit of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the destination address, this bit is ignored.

When set to repeat-block transfer mode, do not use this bit.

SARIE bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the source address occurs while SARIE bit is set to 1, the DMCNT.DTE bit is cleared to 0. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that an interrupt by an extended repeat area overflow on the source address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DMCNT.DTE bit of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the source address, this bit is ignored.

When set to repeat-block transfer mode, do not use this bit.

RPTIE bit (Repeat Size End Interrupt Enable)

When RPTIE bit is set to 1 in repeat transfer mode, the DMCNT.DTE bit is cleared to 0 after completion of a 1-repeat size data transfer. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DMTMD.DTS[1:0] bits are 10b (= repeat area or block area is not specified).

When this bit is set to 1 in block transfer mode, the DMCNT.DTE bit is cleared to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the DMSTS.ESIF flag is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DMTMD.DTS[1:0] bits are 10b (= repeat area or block area is not specified).

When set to repeat-block transfer mode, do not use this bit.

ESIE bit (Transfer Escape End Interrupt Enable)

ESIE bit enables or disables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that are generated during DMA transfer.

The transfer escape end interrupt is generated when the DMSTS.ESIF flag is set to 1 with this bit set to 1. The transfer escape end interrupt is cleared by clearing this bit or the DMSTS.ESIF flag to 0.

DTIE bit (Transfer End Interrupt Enable)

DTIE bit enables or disables the transfer end interrupt request to be generated on completion of a specified number of data transfers.

The transfer end interrupt is generated when the DMSTS.DTIF flag is set to 1 with this bit set to 1. The transfer end interrupt is cleared by clearing this bit or the DMSTS.DTIF flag to 0.

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DARIE位（目标地址扩展重复区域溢出中断允许）

当DARIE位设置为1时目标地址发生扩展重复区域溢出时，DMCNT.DTE位清零。同时，DMSTS.ESIF标志设置为1，表示由请求目标地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后请求中断。将停止传输的通道的DMCNT.DTE位设置为1时，将从停止传输时的状态恢复传输。

当没有为目标地址指定扩展重复区域时，该位被忽略。

当设置为重复块传输模式时，不要使用该位。

SARIE位（源地址扩展重复区溢出中断使能）

当SARIE位设置为1时源地址发生扩展重复区域溢出时，DMCNT.DTE位清零。同时，DMSTS.ESIF标志设置为1，表示由请求源地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后请求中断。将停止传输的通道的DMCNT.DTE位设置为1时，将从停止传输时的状态恢复传输。

当源地址没有指定扩展重复区域时，该位被忽略。

当设置为重复块传输模式时，不要使用该位。

RPTIE位（重复大小结束中断允许）

当RPTIE位在重复传输模式下设置为1时，DMCNT.DTE位在完成1次重复大小的数据传输后被清除为0。同时，将DMSTS.ESIF标志设置为1，表示已产生重复大小结束中断请求。即使DMTMD.DTS[1:0]位为10b（=未指定重复区域或块区域），也可以生成重复大小结束中断请求。

当该位在块传输模式下设置为1时，DMCNT.DTE位在完成1块数据传输后清零，方法与重复传输模式相同。同时，将DMSTS.ESIF标志设置为1，表示已产生重复大小结束中断请求。即使DMTMD.DTS[1:0]位为10b（=未指定重复区域或块区域），也可以生成重复大小结束中断请求。

当设置为重复块传输模式时，不要使用该位。

ESIE位（传输转义结束中断使能）

ESIE位启用或禁用在DMA传输期间产生的传输转义结束中断请求（重复大小结束中断请求和扩展重复区域溢出中断请求）。

当DMSTS.ESIF标志设置为1且该位设置为1时，将产生传输转义结束中断。通过清除该位或DMSTS.ESIF标志为0来清除传输转义结束中断。

DTIE位（传输结束中断允许）

DTIE位启用或禁用在完成指定数量的数据传输时生成的传输结束中断请求。

当DMSTS.DTIF标志设置为1且该位设置为1时，将产生传输结束中断。通过清除该位或DMSTS.DTIF标志为0来清除传输结束中断。

16.2.10 DMAMD : DMA Address Mode Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SM[1:0]		SADR	SARA[4:0]					DM[1:0]		DADR	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DARA[4:0]	Destination Address Extended Repeat Area Specifies the extended repeat area on the destination address. For details on the settings, see Table 16.2.	R/W
5	DADR	Destination Address Update Select After Reload 0: Only reloading 1: Add index after reloading	R/W
7:6	DM[1:0]	Destination Address Update Mode 0 0: Destination address is fixed 0 1: Offset addition 1 0: Destination address is incremented 1 1: Destination address is decremented	R/W
12:8	SARA[4:0]	Source Address Extended Repeat Area Specifies the extended repeat area on the source address. For details on the settings, see Table 16.2.	R/W
13	SADR	Source Address Update Select After Reload 0: Only reloading 1: Add index after reloading	R/W
15:14	SM[1:0]	Source Address Update Mode 0 0: Source address is fixed 0 1: Offset addition 1 0: Source address is incremented 1 1: Source address is decremented	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DARA[4:0] bits (Destination Address Extended Repeat Area)

DARA[4:0] bits specify the extended repeat area on the destination address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer destination, do not specify the extended repeat area on the destination address. When repeat transfer or block transfer is selected, and when DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat area or block area), write 00000b in the DARA[4:0] bits.

In repeat-block transfer mode, write 00000b in the DARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DMINT.DARIE bit set to 1. Table 16.2 lists the settings and the corresponding extended repeat areas.

DADR bits (Destination Address Update Select After Reload)

In repeat-block transfer mode, this bit specifies the behavior of DMDAR after reloading DMDRR.

When this bit is set to 1, an index value ((DMDBSH-DMDBSL) × DataSize) is added to DMDAR after reloading DMDRR.

16.2.10 DMAMD:DMA地址模式寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SM[1:0]		SADR	SARA[4:0]					DM[1:0]		DADR	DARA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DARA[4:0]	目标地址扩展重复区域 指定目标地址上的扩展重复区域。有关设置的详细信息，请参见表16.2。	R/W
5	DADR	重新加载后目标地址更新选择 0：仅重新加载1：重新加载 后添加索引	R/W
7:6	DM[1:0]	目的地址更新模式 00：目标地址固定01：偏移量加法10： 目标地址递增11：目标地址递减	R/W
12:8	SARA[4:0]	源地址扩展重复区 指定源地址上的扩展重复区域。有关设置的详细信息，请参阅 Table 16.2.	R/W
13	SADR	重新加载后源地址更新选择 0：仅重新加载1：重新加载 后添加索引	R/W
15:14	SM[1:0]	源地址更新模式 00：源地址固定01：偏移量加法10： 源地址递增11：源地址递减	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DARA[4:0]位（目标地址扩展重复区）

DARA[4:0]位指定目标地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，剩余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意2次幂。

当低位地址以地址增量溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，当低位地址通过地址减量使扩展重复区域下溢时，设置扩展重复区域的结束地址。

将重复区域或块区域指定为传输目标时，请勿在目标地址上指定扩展重复区域。Whenrepeattransferorblocktransferisselected andwhenDMTMD.DTS[1:0]=00b(thetransferdestinationisspecifiedastherepeatareaorblockarea) write00000bintheDARA[4:0]bits.

在重复块传输模式下，将00000b写入DARA[4:0]位。

当DMINT.DARIE位设置为1的扩展重复区域发生上溢或下溢时，可以请求中断。表16.2列出了设置和相应的扩展重复区域。

DADR位（重载后目标地址更新选择）

在重复块传输模式下，该位指定重新加载DMDRR后DMDAR的行为。

当该位设置为1时，在重新加载DMDRR后将索引值((DMDBSH-DMDBSL)×DataSize)添加到DMDAR。

RA生态工作室

When this bit is set to 0, DMDAR only reloads DMDRR. This behavior is described in Table 16.13.

In normal, repeat or block transfer mode, this bit is ignored.

DM[1:0] bits (Destination Address Update Mode)

DM[1:0] bits select the mode of updating the destination address.

When increment is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the destination address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMOFR register is added to the address.

SARA[4:0] bits (Source Address Extended Repeat Area)

SARA[4:0] bits specify the extended repeat area on the source address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer source, do not specify the extended repeat area on the source address. When repeat transfer or block transfer is selected, and when DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat area or block area), write 00000b in the SARA[4:0] bits.

In repeat-block transfer mode, write 00000b in the SARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DMINT.SARIE bit set to 1. Table 16.2 lists the settings and the corresponding extended repeat areas.

SADR bits (Source Address Update Select After Reload)

In repeat-block transfer mode, this bit specifies the behavior of DMSAR after reloading DMSRR.

When this bit is set to 1, an index value ((DMSBSH-DMSBSL) × DataSize) is added to DMSAR after reloading DMSRR.

When this bit is set to 0, DMSAR only reloads DMSRR. This behavior is described in Table 16.12.

In normal, repeat or block transfer mode, this bit is ignored.

SM[1:0] bits (Source Address Update Mode)

SM[1:0] bits select the mode of updating the source address.

When increment is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the DMTMD.SZ[1:0] bits are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMOFR register is added to the address.

Table 16.2 SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas (1 of 2)

SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas	Extended Repeat Area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address

当该位设置为0时，DMDAR仅重新加载DMDRR。表16.13中描述了这种行为。

在正常、重复或块传输模式下，该位被忽略。

DM[1:0]位（目标地址更新模式）

DM[1:0]位选择更新目标地址的模式。

Whenincrementisselectedandthe DMTMD.SZ[1:0]bitsaresetto00b 01b and10b thedestinationaddressis incrementedby1 2 and4 respectively.

WhendecrementisselectedandtheDMTMD.SZ[1:0]bitsaresetto00b 01b and10b thedestinationaddressis decrementedby1 2 and4 respectively.

选择偏移添加后，将DMOFR寄存器指定的偏移添加到地址中。

SARA[4:0]位（源地址扩展重复区）

SARA[4:0]位指定源地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，剩余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意2次幂。

当低位地址以地址增量溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，当低位地址通过地址减量使扩展重复区域下溢时，设置扩展重复区域的结束地址。

当重复区域或块区域被指定为传输源时，不要在源地址上指定扩展重复区域。Whenrepeattransferorblocktransferisselected andwhenDMTMD.DTS[1:0]=01b(thetransfersourceisspecifiedastherepeatareaorblockarea) write 00000bintheSARA[4:0]bits.

在重复块传输模式下，将00000b写入SARA[4:0]位。

当DMINT.SARIE位设置为1的扩展重复区域发生上溢或下溢时，可以请求中断。表16.2列出了设置和相应的扩展重复区域。

SADR位（重载后源地址更新选择）

在重复块传输模式下，该位指定重新加载DMSRR后DMSAR的行为。

当该位设置为1时，在重新加载DMSRR后将索引值((DMSBSH−DMSBSL)×DataSize)添加到DMSAR。

当该位设置为0时，DMSAR仅重新加载DMSRR。这种行为在表16.12中描述。

在正常、重复或块传输模式下，该位被忽略。

SM[1:0]位（源地址更新模式）

SM[1:0]位选择更新源地址的模式。

WhenincrementisselectedandtheDMTMD.SZ[1:0]bitsaresetto00b 01b and10b thesourceaddressisincrementedby 1 2 and4 respectively.

WhendecrementisselectedandtheDMTMD.SZ[1:0]bitsaresetto00b 01b and10b thesourceaddressisdecremente dby1 2 and4 respectively.

选择偏移添加后，将DMOFR寄存器指定的偏移添加到地址中。

Table 16.2 SARA[4:0]或DARA[4:0]设置和对应的重复区域(1of2)

SARA[4:0]或DARA[4:0]设置和对应的重复区域	扩展重复区域
00000b	未指定
00001b	由地址的低1位指定为扩展重复区域的2个字节
00010b	由地址的低2位指定为扩展重复区域的4个字节
00011b	由地址的低3位指定为扩展重复区域的8个字节
00100b	由地址的低4位指定为扩展重复区域的16个字节
00101b	由地址的低5位指定为扩展重复区域的32个字节
00110b	由地址的低6位指定为扩展重复区域的64个字节

Table 16.2 SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas (2 of 2)

SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas	Extended Repeat Area
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 Kbyte specified as extended repeat area by the lower 10 bits of the address
01011b	2 Kbytes specified as extended repeat area by the lower 11 bits of the address
01100b	4 Kbytes specified as extended repeat area by the lower 12 bits of the address
01101b	8 Kbytes specified as extended repeat area by the lower 13 bits of the address
01110b	16 Kbytes specified as extended repeat area by the lower 14 bits of the address
01111b	32 Kbytes specified as extended repeat area by the lower 15 bits of the address
10000b	64 Kbytes specified as extended repeat area by the lower 16 bits of the address
10001b	128 Kbytes specified as extended repeat area by the lower 17 bits of the address
10010b	256 Kbytes specified as extended repeat area by the lower 18 bits of the address
10011b	512 Kbytes specified as extended repeat area by the lower 19 bits of the address
10100b	1 Mbyte specified as extended repeat area by the lower 20 bits of the address
10101b	2 Mbytes specified as extended repeat area by the lower 21 bits of the address
10110b	4 Mbytes specified as extended repeat area by the lower 22 bits of the address
10111b	8 Mbytes specified as extended repeat area by the lower 23 bits of the address
11000b	16 Mbytes specified as extended repeat area by the lower 24 bits of the address
11001b	32 Mbytes specified as extended repeat area by the lower 25 bits of the address
11010b	64 Mbytes specified as extended repeat area by the lower 26 bits of the address
11011b	128 Mbytes specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited.

16.2.11 DMOFR : DMA Offset Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x18

Bit position: 31 ... 0

Bit field:

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	n/a	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination 0x00000000 to 0x00FFFFFF (0 bytes to (16 M – 1) bytes) 0xFF000000 to 0xFFFFFFFF (–16 Mbytes to –1 byte)	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Write to this register while the DMAC operation is stopped or DMA transfer is disabled (not during data transfer).

Setting bits 31 to 25 is invalid; a value of bit 24 is extended to bits 31 to 25. Reading DMOFR returns the extended value.

In repeat-block transfer mode, the offset is not specified by DMOFR when offset addition is selected, write 0 to DMOFR.

Table 16.2 SARA[4:0]或DARA[4:0]设置和对应的重复区域(2of2)

SARA[4:0]或DARA[4:0]设置和对应的重复区域	扩展重复区域
00111b	由地址的低7位指定为扩展重复区域的128个字节
01000b	由地址的低8位指定为扩展重复区域的256个字节
01001b	由地址的低9位指定为扩展重复区域的512个字节
01010b	1KB由地址的低10位指定为扩展重复区域
01011b	2KB由地址的低11位指定为扩展重复区域
01100b	由地址的低12位指定为扩展重复区域的4KB
01101b	8KB由地址的低13位指定为扩展重复区域
01110b	16KB由地址的低14位指定为扩展重复区域
01111b	32KB由地址的低15位指定为扩展重复区域
10000b	64KB由地址的低16位指定为扩展重复区域
10001b	128KB由地址的低17位指定为扩展重复区域
10010b	256KB由地址的低18位指定为扩展重复区域
10011b	512KB由地址的低19位指定为扩展重复区域
10100b	1MB由地址的低20位指定为扩展重复区域
10101b	2MB由地址的低21位指定为扩展重复区域
10110b	4MB由地址的低22位指定为扩展重复区域
10111b	8MB由地址的低23位指定为扩展重复区域
11000b	16MB由地址的低24位指定为扩展重复区域
11001b	32MB由地址的低25位指定为扩展重复区域
11010b	64MB由地址的低26位指定为扩展重复区域
11011b	128MB由地址的低27位指定为扩展重复区域
11100b to 11111b	禁止设置。

16.2.11 DMOFR:DMA偏移寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x18

Bit position: 31 ... 0

Bit field:

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
31:0	n/a	Specifiestheoffsetwhenoffsetadditionisselectedastheaddressupdatemodefortransfersource ordestination0x00000000to0x00FFFFFF(0bytesto(16M 1)bytes)0xFF000000to0xFFFFFFFF(16Mbytesto 1byte)	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

在DMAC操作停止或禁用DMA传输时（不是在数据传输期间）写入该寄存器。

设置位31到25无效；位24的值扩展到位31到25。读取DMOFR将返回扩展值。

Inrepeat-blocktransfermode theoffsetisnotspecifiedbyDMOFRwhenoffsetadditionisselected write0toDMOFR.

16.2.12 DMCNT : DMA Transfer Enable Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTE	DMA Transfer Enable 0: Disables DMA transfer 1: Enables DMA transfer	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DTE bit (DMA Transfer Enable)

When the DMAST.DMST bit is set to 1 (DMAC activation is enabled) and this bit is set to 1 (DMA transfer is enabled), DMA transfer can be started for the corresponding channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit.
- When the specified total volume of data transfer is completed.
- When DMA transfer is stopped by the repeat size end interrupt.
- When DMA transfer is stopped by the extended repeat area overflow interrupt.
- When DMA transfer is stopped by the access error occurs. Refer to section 16.5. Processing on DMA Transfer Error.

16.2.13 DMREQ : DMA Software Start Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWREQ	DMA Software Start 0: DMA transfer is not requested 1: DMA transfer is requested	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	CLRS	DMA Software Start Bit Auto Clear Select 0: SWREQ bit is cleared after DMA transfer is started by software 1: SWREQ bit is not cleared after DMA transfer is started by software	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

16.2.12 DMCNT：DMA传输使能寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTE	DMA传输使能 0：禁用DMA传输1：启用DMA传输	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

DTE位（DMA传输使能）

当DMAST.DMST位设置为1（启用DMAC激活）并且该位设置为1（启用DMA传输）时，可以为相应的通道启动DMA传输。

[Setting condition]

●向该位写入1时。

[Clearing conditions]

●当0写入该位时。
●当指定的总数据传输量完成时。
●当DMA传输因重复大小结束中断而停止时。
●当DMA传输因扩展重复区域溢出中断而停止时。
●DMA传输因访问错误而停止时。请参阅第16.5节。处理DMA传输错误。

16.2.13 DMREQ:DMA软件启动寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CLRS	—	—	—	SWREQ
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWREQ	DMA软件启动 0：不请求DMA传输1：请求DMA传输	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	CLRS	DMA软件起始位自动清除选择 0：软件启动DMA传输后SWREQ位清零1：软件启动DMA传输后SWREQ位不清零	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SWREQ bit (DMA Software Start)

When 1 is written to SWREQ bit, a DMA transfer request is generated. After DMA transfer is started in response to the request, this bit is cleared to 0 if the CLRS bit is set to 0. This bit is not cleared to 0 while the CLRS bit is set to 1. In this case, a DMA transfer request can be issued again after completion of a transfer.

Note that, however, setting this bit is valid and DMA transfer by software is enabled only when the DMTMD.DCTG[1:0] bits are set to 00b (DMAC activation source is software).

Setting this bit is invalid when the DMTMD.DCTG[1:0] bits are set to a value other than 00b.

To start DMA transfer by software with the CLRS bit being 0, ensure that the SWREQ bit is 0, and then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started while the CLRS bit is set to 0 (the SWREQ bit is cleared after DMA transfer is started by software).
- When 0 is written to this bit.

CLRS bit (DMA Software Start Bit Auto Clear Select)

CLRS bit specifies whether to clear the SWREQ bit to 0 after DMA transfer is started in response to the DMA transfer request generated by setting the SWREQ bit to 1. With this bit set to 0, the SWREQ bit is cleared to 0 after DMA transfer is started. With this bit set to 1, the SWREQ bit is not cleared to 0. In this case, a DMA transfer request can be issued again after completion of a transfer.

16.2.14 DMSTS : DMA Status Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESIF	Transfer Escape End Interrupt Flag 0: A transfer escape end interrupt has not been generated 1: A transfer escape end interrupt has been generated	R/W*1
3:1	—	These bits are read as 0. The write value should be 0.	R
4	DTIF	Transfer End Interrupt Flag 0: A transfer end interrupt has not been generated 1: A transfer end interrupt has been generated	R/W*1
6:5	—	These bits are read as 0. The write value should be 0.	R
7	ACT	DMAC Active Flag 0: DMAC is in the idle state 1: DMAC is operating	R

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SWREQ位（DMA软件启动）

当SWREQ位写入1时，会产生DMA传输请求。响应请求启动DMA传输后，如果CLRS位设置为0，则该位清零。当CLRS位设置为1时，该位不清零。在这种情况下，DMA传输请求转让完成后可再次发行。

但是请注意，设置该位有效，并且仅当DMTMD.DCTG[1:0]位设置为00b（DMAC激活源为软件）时，才启用软件进行的DMA传输。

当DMTMD.DCTG[1:0]位设置为00b以外的值时，设置该位无效。

软件启动DMA传输时CLRS位为0，确保SWREQ位为0，然后将1写入
SWREQ bit.

[Setting condition]

●向该位写入1时。

[Clearing conditions]

●当CLRS位设置为0（软件启动DMA传输后SWREQ位清零）时，接受软件的DMA传输请求并启动DMA传输。

●当0写入该位时。

CLRS位（DMA软件起始位自动清除选择）

CLRS位指定在DMA传输开始后是否将SWREQ位清除为0，以响应通过将SWREQ位设置为1产生的DMA传输请求。当该位设置为0时，在DMA传输完成后SWREQ位被清除为0开始了。该位设置为1时，SWREQ位不会被清除为0。在这种情况下，可以在传输完成后再次发出DMA传输请求。

16.2.14 DMSTS:DMA状态寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	DTIF	—	—	—	ESIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESIF	传输转义结束中断标志 0：未产生传输转义结束中断1：已产生传输转义结束中断	R/W*1
3:1	—	这些位被读取为0。写入值应为0。	R
4	DTIF	传输结束中断标志 0：未产生传输结束中断1：已产生传输结束中断	R/W*1
6:5	—	这些位被读取为0。写入值应为0。	R
7	ACT	DMAC活动标志 0：DMAC处于空闲状态1： DMAC正在运行	R

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：

- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the flag.

ESIF flag (Transfer Escape End Interrupt Flag)

This flag indicates that the transfer escape end interrupt has been generated.

[Setting conditions]

- When 1-repeat size data transfer is completed in repeat transfer mode with the DMINT.RPTIE bit set to 1.
- When 1-block data transfer is completed in block transfer mode with the DMINT.RPTIE bit set to 1.
- When an extended repeat area overflow on the source address occurs while the DMINT.SARIE bit is set to 1 and the DMAMD.SARA[4:0] bits are set to a value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs while the DMINT.DARIE bit is set to 1 and the DMAMD.DARA[4:0] bits are set to a value other than 00000b (extended repeat area is specified on the transfer destination address)

[Clearing conditions]

- When 0 is written to this bit.
- When 1 is written to the DMCNT.DTE bit.

DTIF flag (Transfer End Interrupt Flag)

This flag indicates that the transfer end interrupt has been generated.

[Setting conditions]

- When the specified number of unit-transfers are completed in normal transfer mode (the value of DMCRAL becoming 0 on completion of transfer)
- When the specified number of repeat transfer operations are completed in repeat transfer mode (the value of DMCRBL becoming 0 on completion of transfer with DMTMD.TKP = 0 or the value of DMCRBL reloading DMCRBH with DMTMD.TKP = 1)
- When the specified number of blocks have been transferred in block transfer mode (the value of DMCRBL becoming 0 on completion of transfer with DMTMD.TKP = 0 or the value of DMCRBL reloading DMCRBH with DMTMD.TKP = 1)

[Clearing conditions]

- When 0 is written to this bit
- When 1 is written to the DMCNT.DTE bit

ACT flag (DMAC Active Flag)

This flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts data transfer operation

[Clearing condition]

- When data transfer in response to one transfer request is completed

- 允许安全和非安全访问。

注1.只能写入0来清除标志。

ESIF标志（传输转义结束中断标志）

该标志表明传输转义结束中断已经产生。

[Setting conditions]

●当DMINT.RPTIE位设置为1在重复传输模式下完成1次重复大小的数据传输时。

●当DMINT.RPTIE位设置为1在块传输模式下完成1块数据传输时。

●当DMINT.SARIE位设置为1且DMAMD.SARA[4:0]位设置为00000b以外的值时，当源地址发生扩展重复区域溢出时（扩展重复区域在传输时指定源地址）

●当DMINT.DARIE位设置为1且DMAMD.DARA[4:0]位设置为00000b以外的值时，当目标地址发生扩展重复区域溢出时（扩展重复区域在传输时指定目的地址）

[Clearing conditions]

●当0写入该位时。

●当1写入DMCNT.DTE位时。

DTIF标志（传输结束中断标志）

该标志表示已产生传输结束中断。

[Setting conditions]

●在正常传输模式下完成指定数量的unit-transfer时（传输完成时DMCRAL的值变为0）

●在重复传输模式下完成指定次数的重复传输操作时（DMCRBL的值在DMTMD.TKP=0的传输完成时变为0或DMCRBL的值在DMTMD.TKP=1时重新加载DMCRBH）

●在块传输模式下已经传输了指定数量的块时（DMCRBL的值在传输完成时变为0且DMTMD.TKP=0或DMCRBL的值在DMTMD.TKP=1时重新加载DMCRBH）

[Clearing conditions]

●当0写入该位时

●当1写入DMCNT.DTE位时

ACT标志（DMAC活动标志）

该标志指示DMAC是处于空闲状态还是活动状态。

[Setting condition]

●DMAC开始数据传输操作时

[Clearing condition]

●当响应一个传输请求的数据传输完成时

RA生态工作室

16.2.15 DMSBS : DMA Source Buffer Size Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMSBSH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMSBSL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMSBSL[15:0]	Functions as data transfer counter in repeat-block transfer mode See Table 16.3 for available settings.	R/W
31:16	DMSBSH[15:0]	Specifies the repeat-area size in repeat-block transfer mode See Table 16.3 for available settings.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Table 16.3 Available setting for DMSBS register in repeat-block transfer mode

Source Address Update Mode (DMAMD.SM)	Transfer Data Size (DMTMD.SZ)	Available Setting for DMSBSH and DMSBSL bits
Source address is fixed (SM = 00b)	Don't care	0x0000 (DMSBS is not used)
Offset addition (SM = 01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
Source address is incremented or decremented (SM = 1xb)	Don't care	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

Set the same value for DMSBSH and DMSBSL in repeat-block transfer mode. Write 00000000h to DMSBS in normal, repeat and block transfer mode.

DMSBSH specifies buffer size and DMSBSL functions as a 16-bit buffer size counter in repeat-block transfer mode. In repeat-block transfer mode, source repeat area is specified by DMSBSH.

When address update mode is incremented address or decremented address, this register means the numbers of data of whole buffer. When address update mode is offset addition, this register means the numbers of data of an individual buffer. In offset addition, setting DMSBSH and DMSBSL to 0x0000 is prohibited. When final data of one buffer size is transferred, DMSBSL reloads value of DMSBSH. When address update mode is fixed address, this register is ignored. Table 16.3 shows the setting values of DMA Source Buffer Size Register corresponding to Transfer Data Size in Source Address Update Mode.

In normal, repeat and block transfer mode, DMSBS is not used. The setting is invalid.

16.2.15 DMSBS:DMA源缓冲区大小寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMSBSH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMSBSL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMSBSL[15:0]	在重复块传输模式中用作数据传输计数器 有关可用设置，请参见表16.3。	R/W
31:16	DMSBSH[15:0]	指定重复块传输模式下的重复区域大小 有关可用设置，请参见表16.3。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Table 16.3 重复块传输模式下DMSBS寄存器的可用设置

源地址更新模式(DMAMD.SM)	传输数据大小(DMTMD.SZ)	DMSBSH的可用设置和 DMSBSL bits
源地址是固定的（SM=00b）	不在乎	0x0000（未使用DMSBS）
偏移量加法(SM=01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
源地址递增或递减(SM=1xb)	不在乎	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

在重复块传输模式下为DMSBSH和DMSBSL设置相同的值。在正常、重复和块传输模式下将00000000h写入DMSBS。

DMSBSH指定缓冲区大小，DMSBSL用作重复块传输模式下的16位缓冲区大小计数器。在重复块传输模式下，源重复区域由DMSBSH指定。

当地址更新模式为递增地址或递减地址时，该寄存器表示整个缓冲区的数据个数。当地址更新模式为偏移加法时，该寄存器表示单个缓冲区的数据个数。此外，禁止将DMSBSH和DMSBSL设置为0x0000。当传输一个缓冲区大小的最终数据时，DMSBSL重新加载DMSBSH的值。当地址更新模式为固定地址时，该寄存器被忽略。表16.3显示了与源地址更新模式下的传输数据大小相对应的DMA源缓冲区大小寄存器的设置值。

在正常、重复和块传输模式下，不使用DMSBS。设置无效。

16.2.16 DMDBS : DMA Destination Buffer Size Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMDBSH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMDBSL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMDBSL[15:0]	Functions as data transfer counter in repeat-block transfer mode See Table 16.4 for available settings.	R/W
31:16	DMDBSH[15:0]	Specifies the repeat-area size in repeat-block transfer mode See Table 16.4 for available settings.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Table 16.4 Available setting for DMDBS register in repeat-block transfer mode

Destination Address Update Mode (DMAMD.SM)	Transfer Data Size (DMTMD.SZ)	Available Setting for DMDBSH and DMDBSL bits
Destination address is fixed (SM = 00b)	Don't care	0x0000 (DMDBS is not used)
Offset addition (SM = 01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
Destination address is incremented or decremented (SM = 1xb)	Don't care	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

Set the same value for DMDBSH and DMDBSL in repeat-block transfer mode. Write 00000000h to DMDBS in normal, repeat and block transfer mode.

DMDBSH specifies buffer size and DMDBSL functions as a 16-bit buffer size counter in repeat-block transfer mode. In repeat-block transfer mode, destination repeat area is specified by DMDBSH.

When address update mode is incremented address or decremented address, this register means the numbers of data of whole buffer. When address update mode is offset addition, this register means the numbers of data of an individual buffer. In offset addition, setting DMDBSH and DMDBSL to 0x0000 is prohibited. When final data of one buffer size is transferred, DMDBSL reloads value of DMDBSH. When address update mode is fixed address, this register is ignored. Table 16.4 shows the setting values of Destination Buffer Size Register corresponding to Transfer Data Size in Destination Address Update Mode.

In normal, repeat and block transfer mode, DMDBS is not used. The setting is invalid.

16.2.16 DMDBS:DMA目标缓冲区大小寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DMDBSH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMDBSL[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	DMDBSL[15:0]	在重复块传输模式中用作数据传输计数器 有关可用设置，请参见表16.4。	R/W
31:16	DMDBSH[15:0]	指定重复块传输模式下的重复区域大小 有关可用设置，请参见表16.4。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Table 16.4 重复块传输模式下DMDBS寄存器的可用设置

目标地址更新模式(DMAMD.SM)	传输数据大小(DMTMD.SZ)	DMDBSH的可用设置和 DMDBSL bits
目标地址是固定的（SM=00b）	不在乎	0x0000（未使用DMDBS）
偏移量加法(SM=01b)	8 bits (SZ = 00b)	0x0001 to 0xFFFF (1 to 65535)
	16 bits (SZ = 01b)	0x0001 to 0x7FFF (1 to 32767)
	32 bits (SZ = 10b)	0x0001 to 0x3FFF (1 to 16383)
目标地址递增或递减(SM=1xb)	不在乎	0x0000 (infinite) 0x0001 to 0xFFFF (1 to 65535)

在重复块传输模式下为DMDBSH和DMDBSL设置相同的值。在正常、重复和块传输模式下将00000000h写入DMDBS。

DMDBSH指定缓冲区大小，DMDBSL用作重复块传输模式下的16位缓冲区大小计数器。在重复块传输模式中，目标重复区域由DMDBSH指定。

当地址更新模式为递增地址或递减地址时，该寄存器表示整个缓冲区的数据个数。当地址更新模式为偏移加法时，该寄存器表示单个缓冲区的数据个数。此外，禁止将DMDBSH和DMDBSL设置为0x0000。当传输一个缓冲区大小的最终数据时，DMDBSL重新加载DMDBSH的值。当地址更新模式为固定地址时，该寄存器被忽略。表16.4显示了与Destination中的TransferDataSize对应的DestinationBufferSizeRegister的设置值

地址更新模式。

在正常、重复和块传输模式下，不使用DMDBS。设置无效。

16.2.17 DMBWR : DMA Bufferable Write Enable Register

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x30

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BWE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BWE	Bufferable Write Enable 0: Disables Bufferable Write 1: Enables Bufferable Write	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

BWE bit (Bufferable Write Enable)

BWE bit indicates bufferable write is either enabled or disabled.

This bit is only supported when the destination is the Octa-SPI area. If the destination is not the Octa-SPI area, don't set this bit to 1.

When this bit is 1 and the destination is the Octa-SPI area, the Octa-SPI returns immediate response regardless of whether memory device was written. and high-speed write between DMAC and Octa-SPI is enabled.

Note that if this bit is 1, even if the write access as DMAC is completed, the actual Octa-SPI write may not have ended. Even if an error occurs during write access to the Octa-SPI area, transfer cannot be stopped automatically. Also, the error response detection interrupt (DMA_TRANSERR) do not occurs. Stop or reconfigure manually in the interrupt handler generated by the Octa-SPI.

[Setting condition]

- When 1 is written to this bit

[Clearing conditions]

- When 0 is written to this bit

16.2.18 DMAST : DMA Module Activation Register

Base address: DMA = 0x4000_5200

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DMST	DMAC Operation Enable 0: DMAC activation is disabled 1: DMAC activation is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed

16.2.17 DMBWR:DMA可缓冲写使能寄存器

Base address: DMACn = 0x4000_5000 + 0x0040 × n (n = 0 to 7)

Offset address: 0x30

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BWE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BWE	可缓冲写使能 0：禁用可缓冲写入1：启用可缓冲写入	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

BWE位（可缓冲写使能）

BWE位指示启用或禁用可缓冲写入。

仅当目标为Octa-SPI区域时才支持该位。如果目标不是Octa-SPI区域，请不要将此位设置为1。

当该位为1且目标为Octa-SPI区域时，无论是否写入存储设备，Octa-SPI都会立即返回响应。并启用DMAC和Octa-SPI之间的高速写入。

请注意，如果该位为1，即使作为DMAC的写访问完成，实际的Octa-SPI写可能还没有结束。即使在对Octa-SPI区域的写访问期间发生错误，也无法自动停止传输。此外，不会发生错误响应检测中断(DMA_TRANSERR)。在Octa-SPI生成的中断处理程序中手动停止或重新配置。

[Setting condition]

●向该位写入1时

[Clearing conditions]

●当0写入该位时

16.2.18 DMAST:DMA模块激活寄存器

Base address: DMA = 0x4000_5200

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DMST	DMAC操作使能 0：禁用DMAC激活1：启用DMAC激活	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问

- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

DMST bit (DMAC Operation Enable)

Setting the DMAST.DMST to 1 enables DMAC activation for all channels. When the DMST bit is set to 1 (DMAC activation is enabled), and 1 is written to the DMCNT.DTE bit (DMA transfer is enabled) for multiple channels, all of the associated channels can be placed in the transfer request ready state at the same time.

When the DMST bit clears to 0 during DMA transfer, DMA transfer is suspended after the current data transfer associated with a single transfer request completes. To resume DMA transfer, set the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit

[Clearing condition]

- When 0 is written to this bit

16.2.19 DMECHR : DMAC Error Channel Register

Base address: DMA = 0x4000_5200

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMESTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMECHSAM	—	—	—	—	—	DMECH		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DMECH	DMAC Error channel Indicates the channel number causing the error 0 0 0: Error occurred on Channel 0 0 0 1: Error occurred on Channel 1 0 1 0: Error occurred on Channel 2 ⋮ ⋮ 1 1 1: Error occurred on Channel 7	R
7:3	—	These bits are read as 0. The write value should be 0.	R
8	DMECHSAM	DMAC Error channel Security Attribution Monitor Indicates the security attribution of a channel causing the error 0: secure channel 1: non-secure channel	R
15:9	—	These bits are read as 0. The write value should be 0.	R
16	DMESTA	DMAC Error Status 0: No DMA transfer error occurred 1: DMA transfer error occurred	R/W*1
31:17	—	These bits are read as 0. The write value should be 0.	R

Note 1. Writing to DMESTA depends on the value of DMECHSAM

DMECH[2:0] bit (DMAC Error channel)

When a transfer error due to DMA transfer occurs, it stores the channel of DMAC that was violated.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

DMST位（DMAC操作使能）

将DMAST.DMST设置为1会启用所有通道的DMAC激活。当DMST位设置为1（启用DMAC激活），并将1写入多个通道的DMCNT.DTE位（启用DMA传输）时，所有相关联的通道都可以置于传输请求就绪状态同时。

当DMA传输期间DMST位清除为0时，在与单个传输请求相关的当前数据传输完成后，DMA传输将暂停。要恢复DMA传输，请将DMST位再次设置为1。

[Setting condition]

●向该位写入1时

[Clearing condition]

●当0写入该位时

16.2.19 DMECHR:DMAC错误通道寄存器

Base address: DMA = 0x4000_5200

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMESTA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DMECHSAM	—	—	—	—	—	DMECH		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DMECH	DMAC错误通道 指示导致错误的通道号 000：通道0发生错误001：通道1发生错误010：通道2发生错误 ⋮ ⋮ 111：通道7发生错误	R
7:3	—	这些位被读取为0。写入值应为0。	R
8	DMECHSAM	DMAC错误通道安全归因监视器 指示导致错误的通道的安全属性 0：安全通道1：非安全通道	R
15:9	—	这些位被读取为0。写入值应为0。	R
16	DMESTA	DMAC错误状态 0：未发生DMA传输错误1：发生DMA传输错误	R/W*1
31:17	—	这些位被读取为0。写入值应为0。	R

注1.写入DMESTA取决于DMECHSAM的值

DMECH[2:0]位（DMAC错误通道）

当由于DMA传输而发生传输错误时，它会存储违反的DMAC通道。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

- When the DMAC transfer error occurs and DMESTA = 0.

[Clearing condition]

- When 1 is written to DMESTA.

DMECHSAM bit (DMAC Error channel Security Attribution Monitor)

When a transfer error due to DMA transfer occurs, it indicates the security attribution of the violating DMAC channel.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs and DMESTA = 0.

[Clearing condition]

- When 1 is written to DMESTA.

DMESTA bit (DMAC Error Status)

Indicates whether or not a DMA transfer error occurred.

DMECH, DMECHSAM, DMESTA are cleared by writing 1 to DMESTA. Writing 0 to DMESTA is ignored.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs.

[Clearing condition]

- When 1 is written to DMESTA.

Note: When DMECHSAM = 1, it can be cleared in the secure state and non-secure state. DMECHSAM = 0, it can not be cleared in the non-secure state.

16.3 Operation

16.3.1 Transfer Mode

16.3.1.1 Normal Transfer Mode

In normal transfer mode, one data is transferred by one transfer request. A maximum of 65535 can be set as the number of transfer operations using the DMCRAL register. When these bits are set to 0x0000, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running function). Setting DMCRB register is invalid in normal transfer mode. Except in free running function, a transfer end interrupt request can be generated after completion of the specified number of transfer operations.

Table 16.5 summarizes the register update operation in normal transfer mode, and Figure 16.2 shows the operation in normal transfer mode.

Table 16.5 Register Update Operation in Normal Transfer Mode (1 of 2)

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request
DMSAR	Transfer source address	Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition
DMCRAL	Transfer count	Decremented by one/not updated (in free running function)
DMCRAH	—	Not updated (Not used in normal transfer mode)

[Set condition]

●发生DMAC传输错误且DMESTA=0时。

[Clearing condition]

●当1被写入DMESTA时。

DMECHSAM位（DMAC错误通道安全属性监视器）

当由于DMA传输而发生传输错误时，表明违规DMAC通道的安全属性。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误且DMESTA=0时。

[Clearing condition]

●当1被写入DMESTA时。

DMESTA位（DMAC错误状态）

指示是否发生DMA传输错误。

DMECH、DMECHSAM、DMESTA通过向DMESTA写入1清零。将0写入DMESTA将被忽略。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误时。

[Clearing condition]

●当1被写入DMESTA时。

Note: 当DMECHSAM=1时，可以在安全状态和非安全状态下清零。DMECHSAM=0，在非安全状态下不能清零。

16.3 Operation

16.3.1 传输模式

16.3.1.1 正常传输模式

在正常传输模式下，一个数据由一个传输请求传输。使用DMCRAL寄存器最多可以设置65535个传输操作数。当这些位设置为0x0000时，没有设置具体的传输操作数；在传输计数器停止的情况下执行数据传输（自由运行功能）。在正常传输模式下设置DMCRB寄存器无效。除自由运行功能外，在完成指定次数的传输操作后可以产生传输结束中断请求。

表16.5总结了正常传输模式下的寄存器更新操作，图16.2显示了正常传输模式下的操作。

Table 16.5 正常传输模式下的寄存器更新操作(1of2)

Register	Function	一次转账完成后更新操作 Request
DMSAR	传输源地址	Increment/decrement/fixed/offset addition
DMDAR	转移目的地地址	Increment/decrement/fixed/offset addition
DMCRAL	转移计数	减一未更新（在自由运行功能中）
DMCRAH	—	未更新（ 未在正常传输模式下使用）

Table 16.5 Register Update Operation in Normal Transfer Mode (2 of 2)

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request
DMCRB	—	Not updated (Not used in normal transfer mode)

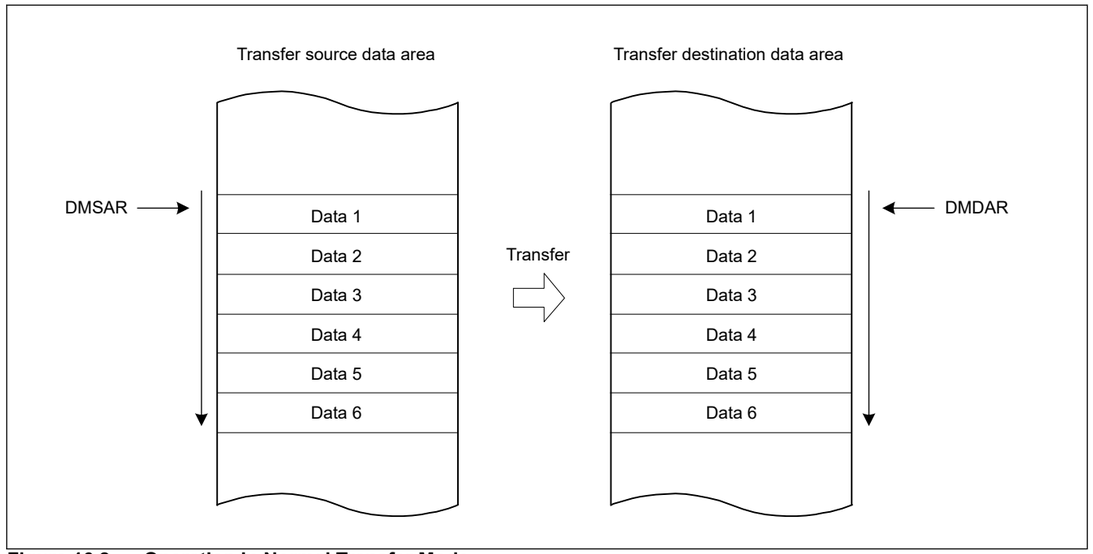

Figure 16.2 Operation in Normal Transfer Mode

16.3.1.2 Repeat Transfer Mode

In repeat transfer mode, one data is transferred by one transfer request.

A maximum of 1K data can be set as a total repeat transfer size using DMCRA register.

A maximum of 64K can be set as the number of repeat transfer operations using DMCRB register; therefore, a maximum of 64M data (1K data × 64K counts of repeat transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a repeat area. When transfer of the repeat size data is completed, the address of the specified repeat area (DMSAR or DMDAR) returns to the transfer start address. When data of the specified repeat size has all been transferred in repeat transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfer operations.

Table 16.6 summarizes the register update operation in repeat transfer mode, and Figure 16.3 shows the operation in repeat transfer mode.

Table 16.6 Register Update Operation in Repeat Transfer Mode (1 of 2)

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request	
		When DMCRAL register is not 1	When DMCRAL register is 1 (Transfer of the Last Data in Repeat Size)
DMSAR	Transfer source address	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b Initial value of DMSAR • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition

Table 16.5 正常传输模式下的寄存器更新操作(2of2)

Register	Function	一次转账完成后更新操作 Request
DMCRB	—	未更新（ 未在正常传输模式下使用）

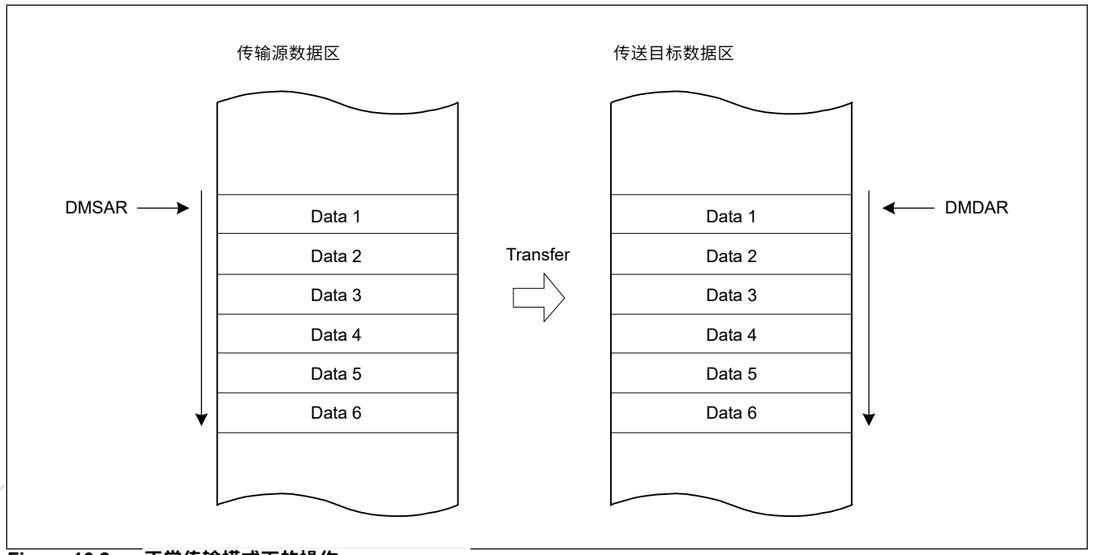

Figure 16.2 正常传输模式下的操作

16.3.1.2 重复传输模式

在重复传输模式下，一个数据由一个传输请求传输。

使用DMCRA寄存器最多可以将1K数据设置为总重复传输大小。

使用DMCRB寄存器最多可以设置64K作为重复传输操作的次数；因此，最多可以将64M数据（1K数据×64K重复传输操作计数）设置为总数据传输大小。

可以将传输源或传输目标指定为重复区域。当重复大小数据的传输完成时，指定的重复区域（DMSAR或DMDAR）的地址返回到传输起始地址。当指定重复大小的数据在重复传输模式下全部传输完毕后，可以停止DMA传输并请求重复大小结束中断。DMA传输可以通过在重复大小结束中断处理中向DMCNT.DTE位写入1来恢复。

完成指定次数的重复传输操作后，可以产生传输结束中断请求。

表16.6总结了重复传输模式下的寄存器更新操作，图16.3显示了重复传输模式下的操作。

Table 16.6 重复传输模式下的寄存器更新操作（1of2）

Register	Function	通过一个传输请求完成传输后更新操作	
		当DMCRAL寄存器不为1时	当DMCRAL寄存器为1时（传输重复大小的最后一个数据）
DMSAR	传输源地址	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b DMSAR初始值 • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition

Table 16.6 Register Update Operation in Repeat Transfer Mode (2 of 2)

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request	
		When DMCRAL register is not 1	When DMCRAL register is 1 (Transfer of the Last Data in Repeat Size)
DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b Initial value of DMDAR • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	Repeat size	Not updated	Not updated
DMCRAL	Transfer count	Decremented by one	DMCRAH
DMCRBH	Number of repeat transfer operations	Not updated	Not updated
DMCRBL	Count of repeat transfer operations	Not updated	Decremented by one

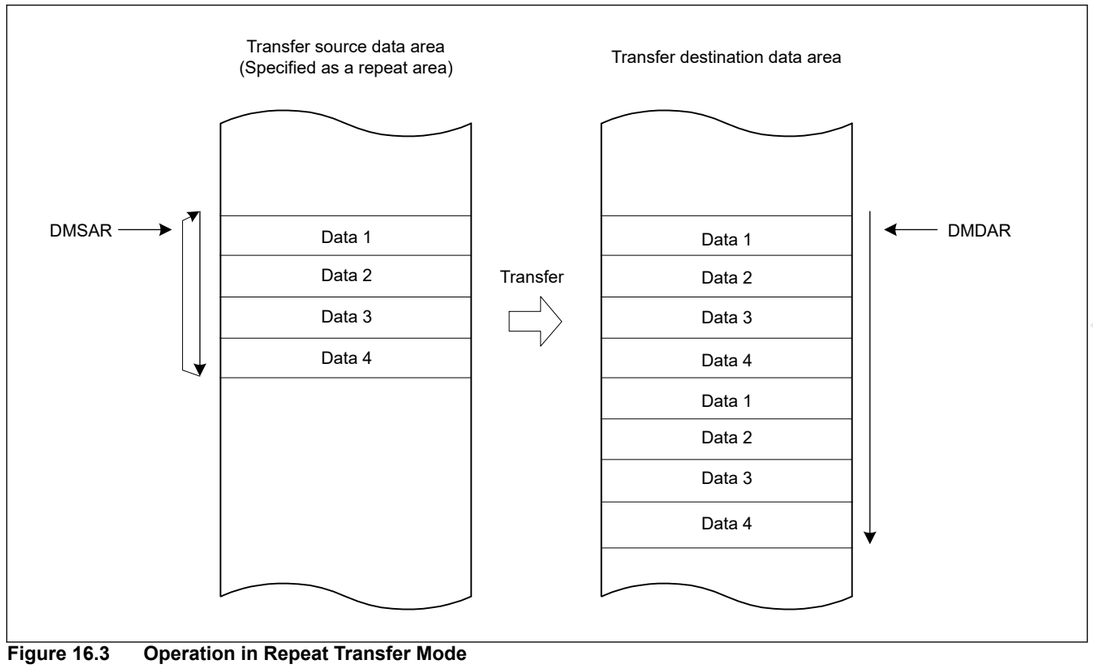

Figure 16.3 Operation in Repeat Transfer Mode

16.3.1.3 Block Transfer Mode

In block transfer mode, a single block data is transferred by one transfer request.

A maximum of 1K data can be set as a total block transfer size using DMCRA register.

A maximum of 64K can be set as the number of block transfer operations using DMCRB register; therefore, a maximum of 64M data (1K data × 64K counts of block transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a block area. When transfer of a single block data is completed, the address of the specified block area (DMSAR or DMDAR) returns to the transfer start address. When a single block data has all been transferred in block transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the repeat size end interrupt handling.

Transfer end interrupt request can be generated after completion of the specified number of block transfer operations.

Table 16.6 重复传输模式下的寄存器更新操作(2of2)

Register	Function	通过一个传输请求完成传输后更新操作	
		当DMCRAL寄存器不为1时	当DMCRAL寄存器为1时（传输重复大小的最后一个数据）
DMDAR	转移目的地地址	Increment/decrement/fixed/offset addition	• DMTMD.DTS[1:0] = 00b DMDAR的初始值 • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	重复大小	未更新	未更新
DMCRAL	转移计数	减一	DMCRAH
DMCRBH	重复传输操作数	未更新	未更新
DMCRBL	重复传输操作的计数	未更新	减一

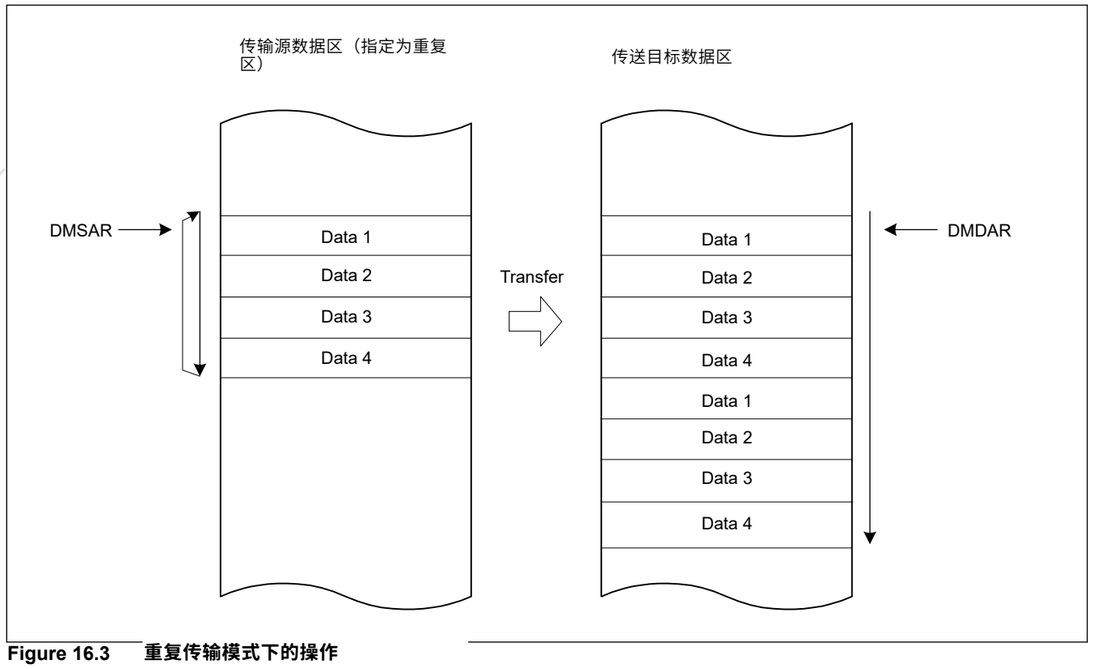

Figure 16.3 重复传输模式下的操作

16.3.1.3 块传输模式

在块传输模式下，单个块数据由一个传输请求传输。

使用DMCRA寄存器最多可以将1K数据设置为总块传输大小。

使用DMCRB寄存器最多可以设置64K作为块传输操作的数量；因此，最多可以将64M数据（1K数据×64K块传输操作计数）设置为总数据传输大小。

可以将传输源或传输目标指定为块区域。当单个块数据的传输完成时，指定块区域（DMSAR或DMDAR）的地址返回到传输起始地址。在块传输模式下，当单个块数据已全部传输完毕后，可以停止DMA传输并请求重复大小结束中断。DMA传输可以通过在重复大小结束中断处理中向DMCNT.DTE位写入1来恢复。

在完成指定数量的块传输操作后，可以产生传输结束中断请求。

Table 16.7 summarizes the register update operation in block transfer mode, and Figure 16.4 shows the operation in block transfer mode.

Table 16.7 Register Update Operation in Block Transfer Mode

Register	Function	Update Operation after Completion of Single-Block Transfer by One Transfer Request
DMSAR	Transfer source address	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b Initial value of DMSAR • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	Transfer destination address	• DMTMD.DTS[1:0] = 00b Initial value of DMDAR • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	Block size	Not updated
DMCRAL	Transfer count	DMCRAH
DMCRBH	Number of block transfer operations	Not updated
DMCRBL	Count of block transfer operations	Decremented by one

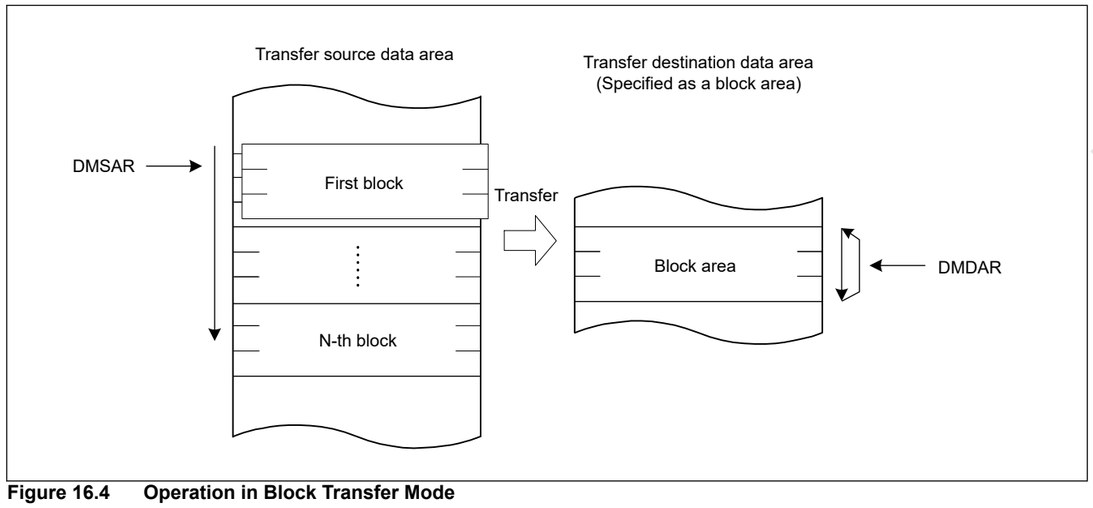

Figure 16.4 Operation in Block Transfer Mode

16.3.1.4 Repeat-Block Transfer Mode

Repeat-block transfer is the operation mode with the following functions added to the block transfer function.

Repeat function: Added function (ring buffer) to repeat specified address area.

Offset function: Multiple areas with offset can be specified within one block transfer.

The repeat function and the offset function can be used for both the transfer source and the transfer destination of repeat-block transfer.

Figure 16.5 shows an example of adding a repeat function to the transfer destination.

Figure 16.6 shows repeat-block transfer with an offset to the transfer destination.

In repeat-block transfer mode, a single block data is transferred by one transfer request.

表16.7总结了块传输模式下的寄存器更新操作，图16.4显示了块传输模式下的操作。

Table 16.7 块传输模式下的寄存器更新操作

Register	Function	一次传输完成单块传输后的更新操作 Request
DMSAR	传输源地址	• DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 01b DMSAR初始值 • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMDAR	转移目的地地址	• DMTMD.DTS[1:0] = 00b DMDAR的初始值 • DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition • DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition
DMCRAH	块大小	未更新
DMCRAL	转移计数	DMCRAH
DMCRBH	块传输操作数	未更新
DMCRBL	块传输操作的计数	减一

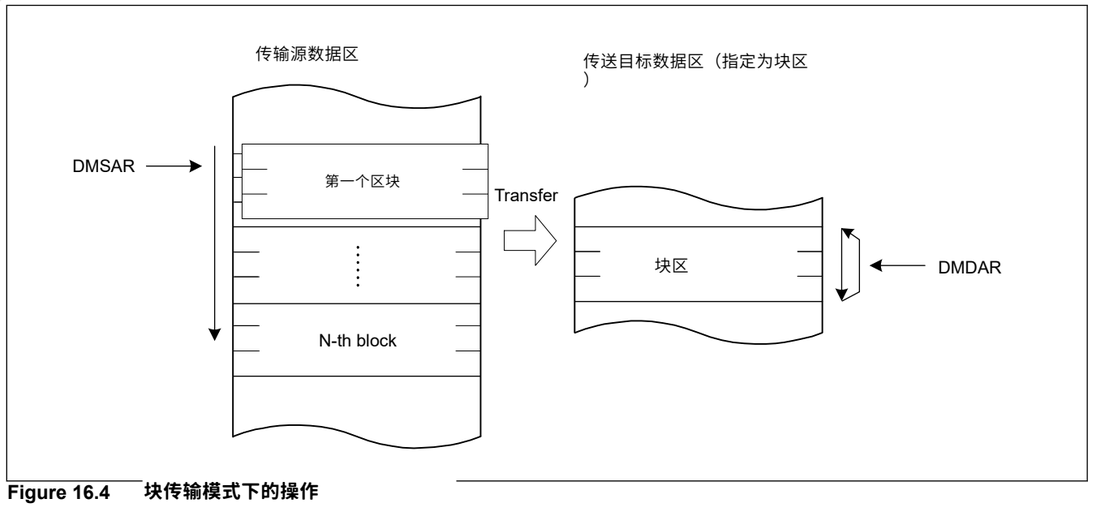

Figure 16.4 块传输模式下的操作

16.3.1.4 重复块传输模式

重复块传输是在块传输功能中添加了以下功能的操作模式。

重复功能：增加了重复指定地址区域的功能（环形缓冲区）。

偏移功能：在一次块传输中可以指定多个带偏移的区域。

重复块传输的传输源和传输目标都可以使用重复函数和偏移函数。

图16.5显示了向传输目的地添加重复功能的示例。

图16.6显示了到传输目标的偏移量的重复块传输。

在重复块传输模式中，单个块数据由一个传输请求传输。

A maximum of 1K data can be set as a total block transfer size using DMCRA of the DMACn.

A maximum of 64K can be set as the number of block transfer operations using DMCRB of the DMACn; therefore, a maximum of 64M data (1K data × 64K counts of block transfer operations) can be set as a total data transfer size.

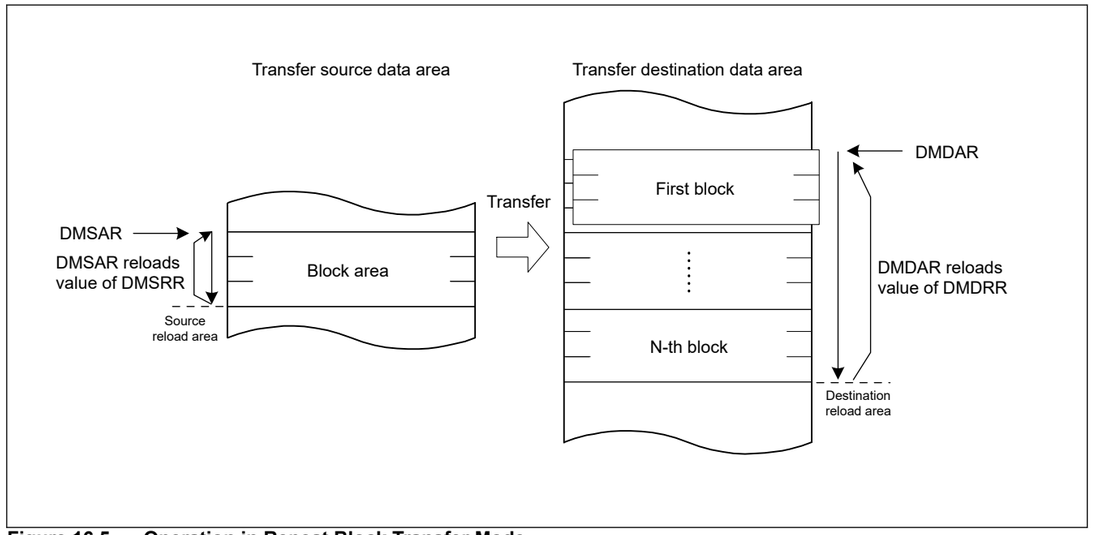

Figure 16.5 Operation in Repeat Block Transfer Mode

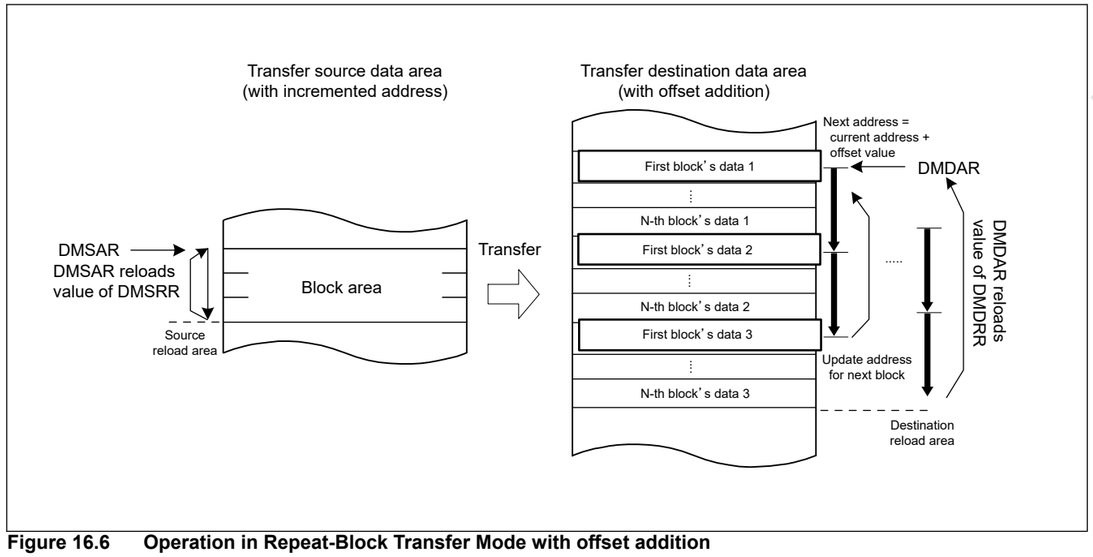

Figure 16.6 Operation in Repeat-Block Transfer Mode with offset addition

Table 16.8 to Table 16.13 summarize the register update operations in repeat-block transfer mode.

使用DMACn的DMCRA可以将最大1K数据设置为总块传输大小。

使用DMACn的DMCRB最多可以设置64K作为块传输操作的数量；因此，最多可以将64M数据（1K数据×64K块传输操作计数）设置为总数据传输大小。

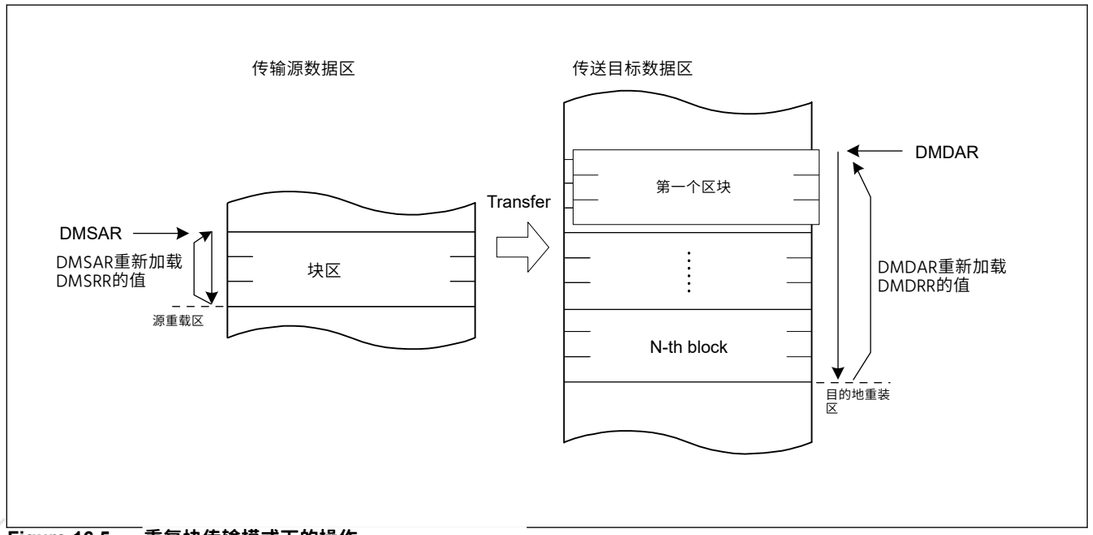

Figure 16.5 重复块传输模式下的操作

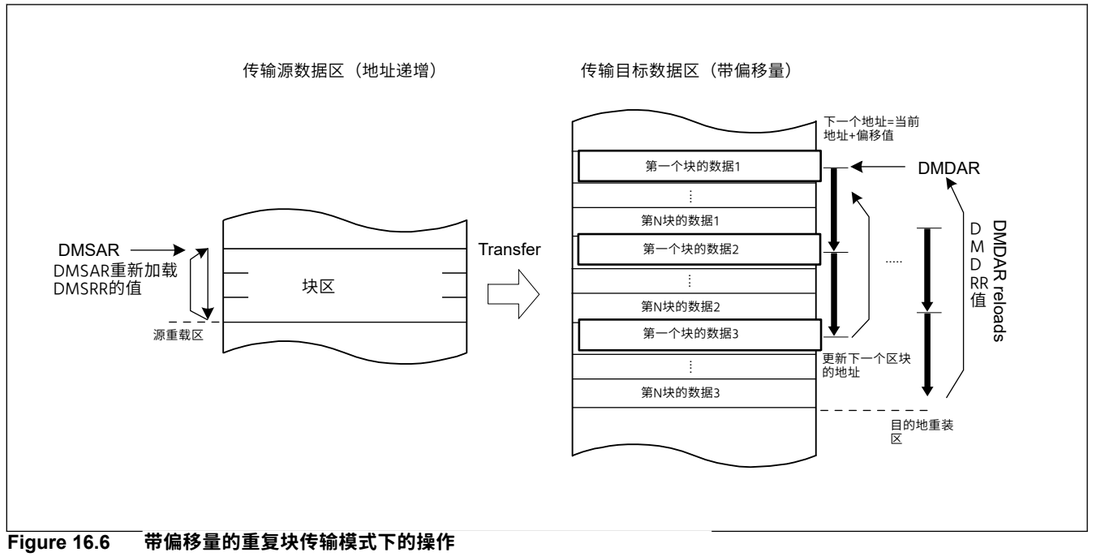

Figure 16.6 带偏移量的重复块传输模式下的操作

表16.8至表16.13总结了重复块传输模式下的寄存器更新操作。

Table 16.8 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Fixed address DMAMD.SM[1:0] = 00b)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated
DMSAR	Transfer source address	Not updated	Not updated	Not updated
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]

Table 16.9 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Fixed address DMAMD.DM[1:0] = 00b)

Register	Function	Update operation after single data is transferred		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated
DMDAR	Transfer destination address	Not updated	Not updated	Not updated
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]

Table 16.10 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Incremented or Decre-mented address DMAMD.SM[1:0] = 10b or 11b) (1 of 2)

Register	Function	Update operation after single data is transferred					
		DMSBSL[15:0] is not 1			DMSBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated

Table 16.8 重复块传输模式下与源区域相关的寄存器更新操作（固定地址 DMAMD.SM[1:0] = 00b)

Register	Function	单条数据传输后的更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重载地址	未更新	未更新	未更新
DMSAR	传输源地址	未更新	未更新	未更新
DMCRAH[9:0]	块大小	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]

Table 16.9 重复块传输模式下与目标区域相关的寄存器更新操作（固定地址DMAMD.DM[1:0]=00b）

Register	Function	单条数据传输后的更新操作		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重载地址	未更新	未更新	未更新
DMDAR	转移目的地地址	未更新	未更新	未更新
DMCRAH[9:0]	块大小	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]

Table 16.10 与重复块传输模式中的源区域相关的寄存器更新操作（递增或递减地址DMAMD.SM[1:0]=10b或11b）（1of2）

Register	Function	单条数据传输后的更新操作					
		DMSBSL[15:0]不是1			DMSBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重载地址	未更新	未更新	未更新	未更新	未更新	未更新

Table 16.10 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Incremented or Decre-mented address DMAMD.SM[1:0] = 10b or 11b) (2 of 2)

Register	Function	Update operation after single data is transferred					
		DMSBSL[15:0] is not 1			DMSBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSAR	Transfer source address when DMTMD.SM[1:0] = 10b	Incremented by Data Size			DMSRR		
	Transfer source address when DMTMD.SM[1:0] = 11b	Decremented by Data Size			DMSRR		
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	Source buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMSBSL[15:0]	Count of transfer data in source buffer	Decremented by 1	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH	DMSBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]			DMCRBH[15:0]

Table 16.11 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Incremented or Decremented address DMAMD.DM[1:0] = 10b or 11b) (1 of 2)

Register	Function	Update operation after single data is transferred					
		DMDBSL[15:0] is not 1			DMDBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated

Table 16.10 重复块传输模式中与源区域相关的寄存器更新操作（递增或递减地址DMAMD.SM[1:0]=10b或11b）（2of2）

Register	Function	单条数据传输后的更新操作					
		DMSBSL[15:0]不是1			DMSBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSAR	DMTMD.SM[1:0]=10b时传输源地址	按数据大小递增			DMSRR		
	DMTMD.SM[1:0]=11b时传输源地址	按数据大小递减			DMSRR		
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	源缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新	未更新
DMSBSL[15:0]	源缓冲区中的传输数据计数	Decremented by 1	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH	DMSBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]			DMCRBH[15:0]

Table 16.11 与重复块传输模式中的目标区域相关的寄存器更新操作（递增或递减地址DMAMD.DM[1:0]=10b或11b）（1of2）

Register	Function	单条数据传输后的更新操作					
		DMDBSL[15:0]不是1			DMDBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重载地址	未更新	未更新	未更新	未更新	未更新	未更新

Table 16.11 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Incremented or Decremented address DMAMD.DM[1:0] = 10b or 11b) (2 of 2)

Register	Function	Update operation after single data is transferred					
		DMDBSL[15:0] is not 1			DMDBSL[15:0] is 1		
		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)		DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1		DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDAR	Transfer destination address when DMTMD.DM[1:0] = 10b	Incremented by Data Size			DMDRR		
	Transfer destination address when DMTMD.DM[1:0] = 11b	Decremented by Data Size			DMDRR		
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	Destina-tion buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMDBSL[15:0]	Count of transfer data in destination buffer	Decremented by 1	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH	DMDBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Not updated	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]			DMCRBH[15:0]

Table 16.12 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Offset addition DMAMD.SM[1:0] = 01b) (1 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMSBSL[15:0] is not 1		DMSBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSRR	Transfer source reload address	Not updated	Not updated	Not updated	Not updated	Not updated

Table 16.11 与重复块传输模式中的目标区域相关的寄存器更新操作（递增或递减地址DMAMD.DM[1:0]=10b或11b）（2of2）

Register	Function	单条数据传输后的更新操作					
		DMDBSL[15:0]不是1			DMDBSL[15:0] is 1		
		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）		DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1		DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDAR	DMTMD.DM[1:0]=10b时传输目标地址	按数据大小递增			DMDRR		
	DMTMD.DM[1:0]=11b时传输目标地址	按数据大小递减			DMDRR		
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]
DMDBSH[15:0]	目标缓冲区大小（Repeat-size）	未更新	未更新	未更新	未更新	未更新	未更新
DMDBSL[15:0]	目标缓冲区中的传输数据计数	Decremented by 1	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH	DMDBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	未更新	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]			DMCRBH[15:0]

Table 16.12 与重复块传输模式中的源区域相关的寄存器更新操作（偏移量加法DMAMD.SM[1:0]=01b）（1of2）

Register	Function	DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）			
			DMSBSL[15:0]不是1		DMSBSL[15:0] is 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSRR	传输源重载地址	未更新	未更新	未更新	未更新	未更新

Table 16.12 Register Update Operation associated with source area in Repeat-Block Transfer Mode (Offset addition DMAMD.SM[1:0] = 01b) (2 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMSBSL[15:0] is not 1		DMSBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMSAR	Transfer source address when DMAMD.SADR = 0	Offset addition by DMSBSH	DMSRR		DMSRR	
	Transfer source address when DMAMD.SADR = 1		DMSRR + (DMS-BSH - DMSBSL) × DataSize			
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	Source buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated
DMSBSL[15:0]	Count of transfer data in source buffer	Not updated	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]		DMCRBH[15:0]

Table 16.13 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Offset addition DMAMD.DM[1:0] = 01b) (1 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMDBSL[15:0] is not 1		DMDBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDRR	Transfer destination reload address	Not updated	Not updated	Not updated	Not updated	Not updated
DMSAR	Transfer destination address when DMAMD.DADR = 0	Offset addition by DMDBSH	DMDRR		DMDRR	
	Transfer destination address when DMAMD.DADR = 1		DMDRR + (DMDBSH - DMDBSL) × DataSize			
DMCRAH[9:0]	Block size	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRAL[15:0]	Block size count	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]

Table 16.12 重复块传输模式中与源区域相关的寄存器更新操作（偏移量加法DMAMD.SM[1:0]=01b）（2of2）

Register	Function	DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）			
			DMSBSL[15:0]不是1		DMSBSL[15:0] is 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMSAR	DMAMD.SADR=时传输源地址 0	偏移量加法 DMSBSH	DMSRR		DMSRR	
	DMAMD.SADR=时传输源地址 1		DMSRR + (DMS-BSH - DMSBSL) × DataSize			
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]
DMSBSH[15:0]	源缓冲区大小（重复大小）	未更新	未更新	未更新	未更新	未更新
DMSBSL[15:0]	源缓冲区中的传输数据计数	未更新	Decremented by 1	Decremented by 1	DMSBSH	DMSBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]		DMCRBH[15:0]

Table 16.13 与重复块传输模式中的目标区域相关的寄存器更新操作（偏移量加法DMAMD.DM[1:0]=01b）（1of2）

Register	Function	DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）			
			DMDBSL[15:0]不是1		DMDBSL[15:0] is 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDRR	传输目的地重载地址	未更新	未更新	未更新	未更新	未更新
DMSAR	当DMAMD.DADR=时传输目标地址 0	偏移量加法 DMDBSH	DMDRR		DMDRR	
	当DMAMD.DADR=时传输目标地址 1		DMDRR + (DMDBSH - DMDBSL) × DataSize			
DMCRAH[9:0]	块大小	未更新	未更新	未更新	未更新	未更新
DMCRAL[15:0]	块大小计数	Decremented by 1	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]	DMCRAH[9:0]

Table 16.13 Register Update Operation associated with destination area in Repeat-Block Transfer Mode (Offset addition DMAMD.DM[1:0] = 01b) (2 of 2)

Register	Function	DMCRAL[15:0] is not 1	DMCRAL[15:0] is 1 (single block is transferred)			
			DMDBSL[15:0] is not 1		DMDBSL[15:0] is 1	
			DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1	DMCRBL[15:0] is not 1	DMCRBL[15:0] is 1
DMDBSH[15:0]	Destina-tion buffer size (Repeat-size)	Not updated	Not updated	Not updated	Not updated	Not updated
DMDBSL[15:0]	Count of transfer data in destination buffer	Not updated	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH
DMCRBH[15:0]	Number of block transfer operations	Not updated	Not updated	Not updated	Not updated	Not updated
DMCRBL[15:0]	Count of block transfer operations when DMTMD.TKP = 0	Not updated	Decremented by 1	0	Decremented by 1	0
	Count of block transfer operations when DMTMD.TKP = 1			DMCRBH[15:0]		DMCRBH[15:0]

16.3.2 Extended Repeat Area Function

The DMAC supports a function to specify the extended repeat areas on the transfer source and destination addresses. With the extended repeat areas set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat areas can be specified separately to the transfer source address register (DMSAR) and transfer destination address register (DMDAR).

The extended repeat area on the source address is specified by the DMAMD.SARA[4:0] bits. The extended repeat area on the destination address is specified by the DMAMD.DARA[4:0] bits. The size can be specified separately for the source and destination sides.

However, the area (of transfer source or transfer destination) which is specified as the repeat area or block area should not be specified as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an interrupt by an extended repeat area overflow can be requested. When an overflow occurs in the extended repeat area on the transfer source while the DMINT.SARIE bit is set to 1, the DMSTS.ESIF flag is set to 1 and the DMCNT.DTE bit is cleared to 0 to stop DMA transfer. At this time, if the DMINT.ESIE bit is set to 1, an interrupt by an extended repeat area overflow is requested. When the DMINT.DARIE bit is set to 1, the destination address register becomes a target to apply the function. DMA transfer can be resumed by writing 1 to the DMCNT.DTE bit in the interrupt handling.

Figure 16.7 shows an example of the extended repeat area operation.

Table 16.13 与重复块传输模式中的目标区域相关的寄存器更新操作（偏移量加法DMAMD.DM[1:0]=01b）（2之2）

Register	Function	DMCRAL[15:0]不是1	DMCRAL[15:0]为1（传输单个块）			
			DMDBSL[15:0]不是1		DMDBSL[15:0] is 1	
			DMCRBL[15:0]不是1	DMCRBL[15:0] is 1	DMCRBL[15:0]不是1	DMCRBL[15:0] is 1
DMDBSH[15:0]	目标缓冲区大小（Repeat-size）	未更新	未更新	未更新	未更新	未更新
DMDBSL[15:0]	目标缓冲区中的传输数据计数	未更新	Decremented by 1	Decremented by 1	DMDBSH	DMDBSH
DMCRBH[15:0]	块传输操作数	未更新	未更新	未更新	未更新	未更新
DMCRBL[15:0]	DMTMD.TKP=0时的块传输操作计数	未更新	Decremented by 1	0	Decremented by 1	0
	DMTMD.TKP=1时的块传输操作计数			DMCRBH[15:0]		DMCRBH[15:0]

16.3.2 扩展重复区域功能

DMAC支持在传输源地址和目标地址上指定扩展重复区域的功能。通过设置扩展重复区域，地址寄存器重复指示指定扩展重复区域的地址。

扩展重复区域可以分别指定到传输源地址寄存器(DMSAR)和传输目标地址寄存器(DMDAR)。

源地址上的扩展重复区域由DMAMD.SARA[4:0]位指定。目标地址上的扩展重复区域由DMAMD.DARA[4:0]位指定。可以为源端和目标端分别指定大小。

但是，指定为重复区域或块区域的区域（传送源或传送目的地）不应指定为扩展重复区域。

当地址寄存器值到达扩展重复区的结束地址且扩展重复区溢出时，
DMA传输停止并且可以请求由扩展重复区域溢出引起的中断。当DMINT.SARIE位设置为1时传输源上的扩展重复区域发生溢出时，DMSTS.ESIF标志设置为1并且DMCNT.DTE位清零以停止DMA传输。此时，如果DMINT.ESIE位设置为1，则请求由扩展重复区域溢出引起的中断。当DMINT.DARIE位设置为1时，目标地址寄存器成为应用该功能的目标。可以通过在中断处理中向DMCNT.DTE位写入1来恢复DMA传输。

图16.7显示了扩展重复区域操作的示例。

Eight bytes are specified as an extended repeat area by the lower three bits of DMSAR (DMAMD.SARA[4:0] bits = 00011b). The data size is eight bits (DMTMD.SZ[1:0] = 00b).

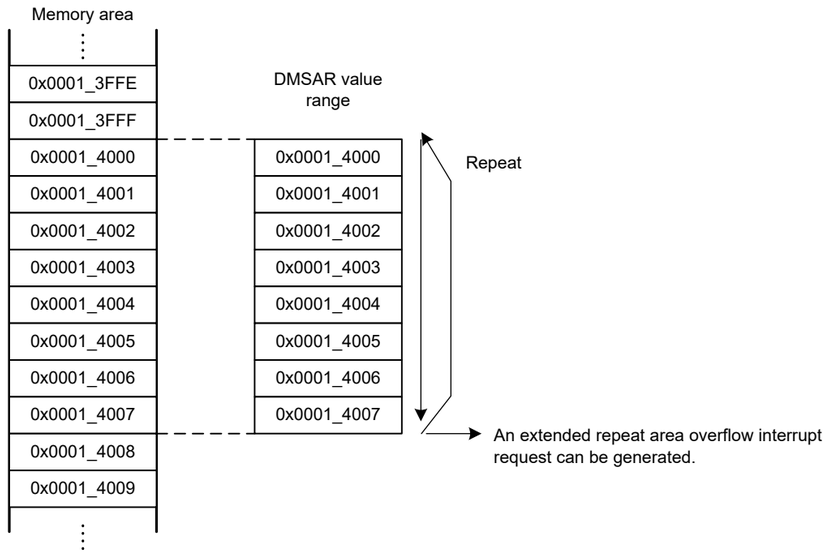

Figure 16.7 Example of Extended Repeat Area Operation

When an interrupt by an extended repeat area overflow is used in block transfer mode, the following should be taken into consideration.

When a transfer is stopped by an interrupt by an extended repeat area overflow, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the interrupt by the overflow is suspended until transfer of the block is completed, and the transfer overruns.

Figure 16.8 shows an example when the extended repeat area function is used in block transfer mode.

八个字节由DMSAR的低三位指定为扩展重复区域（DMAMD.SARA[4:0]位=00011b）。数据大小为8位(DMTMD.SZ[1:0]=00b)。

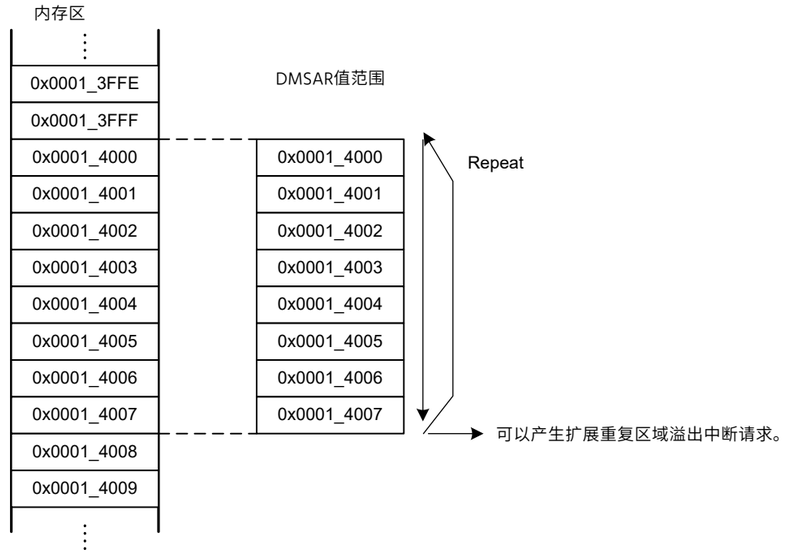

Figure 16.7 扩展重复区域操作示例

在块传输模式下使用扩展重复区域溢出中断时，应考虑以下事项。

当传输因扩展重复区域溢出中断而停止时，地址寄存器必须设置为块大小为2的幂或块大小边界与扩展重复区域边界对齐。当一个块的传输过程中扩展重复区域发生溢出时，溢出中断被暂停，直到块传输完成，传输溢出。

图16.8显示了在块传输模式下使用扩展重复区域功能的示例。

Eight bytes are specified as an extended repeat area by the lower three bits of DMSAR (DMAMD.SARA[4:0] bits = 00011b), block transfer mode with block size 5 is set (DMCRA = 0x0005_0005), and transfer source address is not specified as a block area. Data size is eight bits (DMTMD.SZ[1:0] bits = 00b).

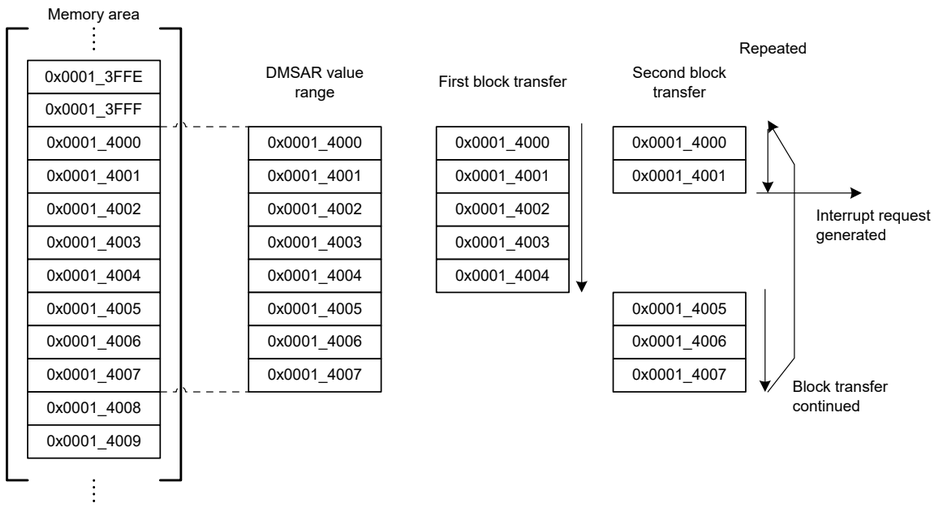

Figure 16.8 Example of Extended Repeat Area Function in Block Transfer Mode

16.3.3 Free-running Function

The DMAC supports free-running function. This function allows to transfer repeatedly without reconfiguring in interrupt handler.

16.3.3.1 In Normal Transfer Mode

In normal transfer mode, when DMCRA.DMCRAL bits are set to 0000h, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped.

For more information, see section 16.3.1.1. Normal Transfer Mode.

16.3.3.2 In Other Transfer Mode

In repeat, block and repeat-block transfer mode, the DMAC supports free-running function using the DMTMD.TKP bit. If the DMTMD.TKP bit is to be set to 1, the transfer is not stopped by completion of specified total number of transfer operations and reloads DMCRBH repeatedly.

Figure 16.9 show an example of block transfer operation without free-running function.

8个字节被DMSAR的低三位指定为扩展重复区域（DMAMD.SARA[4:0]bits=00011b），设置块大小为5的块传输模式（DMCRA=0x0005_0005），传输源地址为未指定为块区域。数据大小为8位（DMTMD.SZ[1:0]位=00b）。

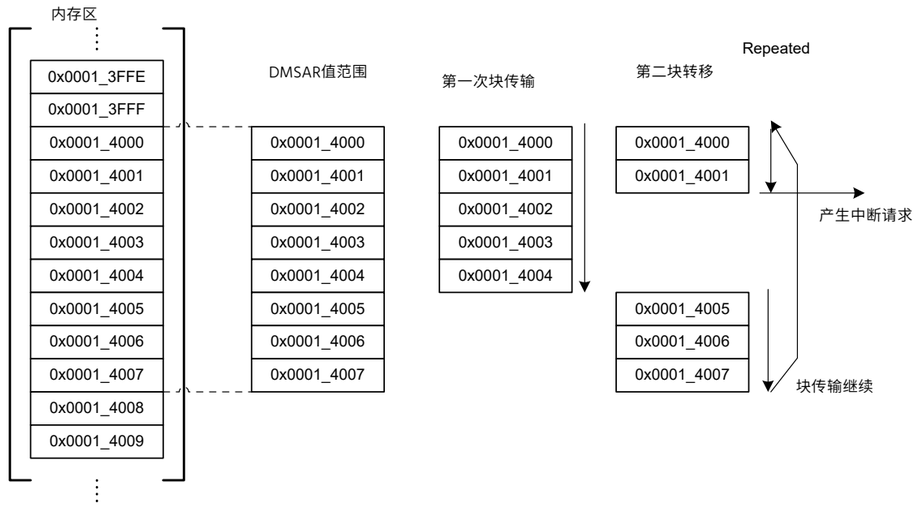

Figure 16.8 块传输模式下的扩展重复区域功能示例

16.3.3 Free-running Function

DMAC支持自由运行功能。此功能允许重复传输而无需在中断处理程序中重新配置。

16.3.3.1 在正常传输模式下

在正常传输模式下，当DMCRA.DMCRAL位设置为0000h时，不设置具体的传输操作数；在传输计数器停止的情况下执行数据传输。

有关详细信息，请参阅第16.3.1.1节。正常传输模式。

16.3.3.2 在其他传输模式下

在重复、块和重复块传输模式下，DMAC使用DMTMD.TKP位支持自由运行功能。如果要设置DMTMD.TKP位为1，则在完成指定的传输操作总数时不会停止传输并重复重新加载DMCRBH。

图16.9显示了一个没有自由运行功能的块传输操作示例。

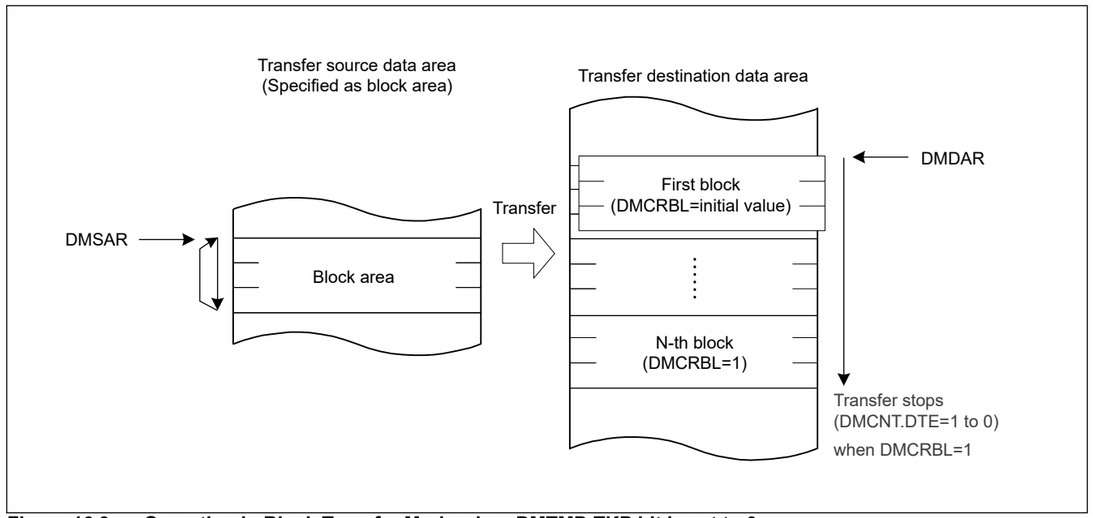

Figure 16.9 Operation in Block Transfer Mode when DMTMD.TKP bit is set to 0

Figure 16.10 show an example of block transfer operation with free-running function.

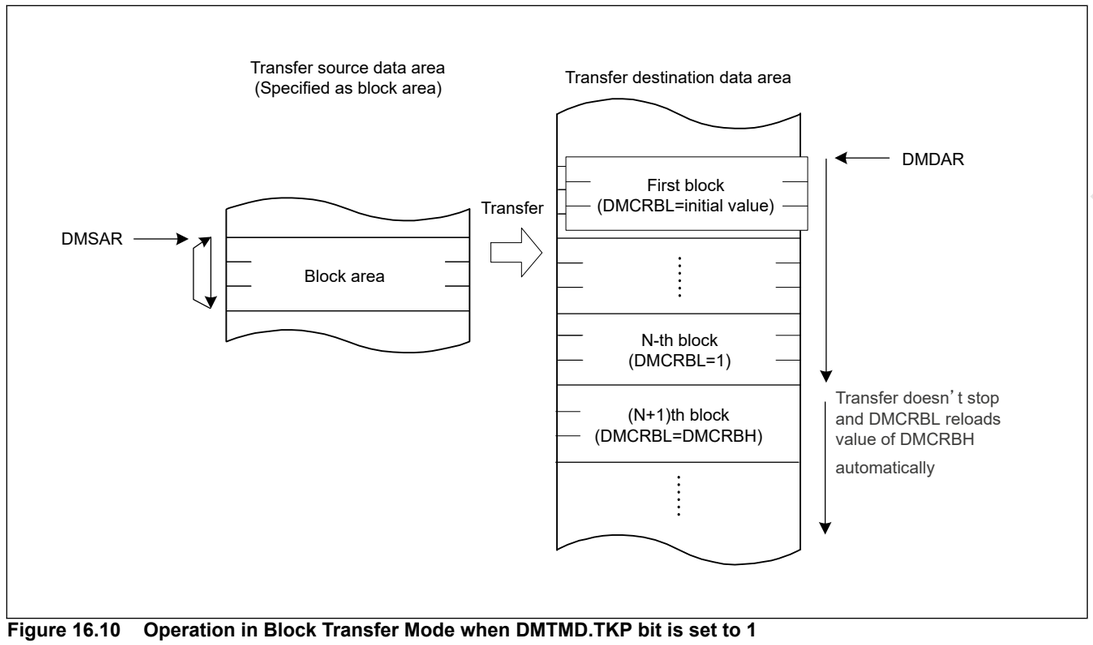

Figure 16.10 Operation in Block Transfer Mode when DMTMD.TKP bit is set to 1

16.3.4 Address Update Function using Offset

The source and destination addresses can be updated by fixing, increment, decrement, or offset addition. In normal, repeat and block transfer mode, when the offset addition is selected, the offset specified by the DMA offset register (DMOFR) is added to the address every time the DMAC performs one data transfer. This function realizes a data transfer where addresses are allocated to separated areas.

Offset subtraction can also be realized by setting a negative value in DMOFR. In this case, the negative value must be 2's complement.

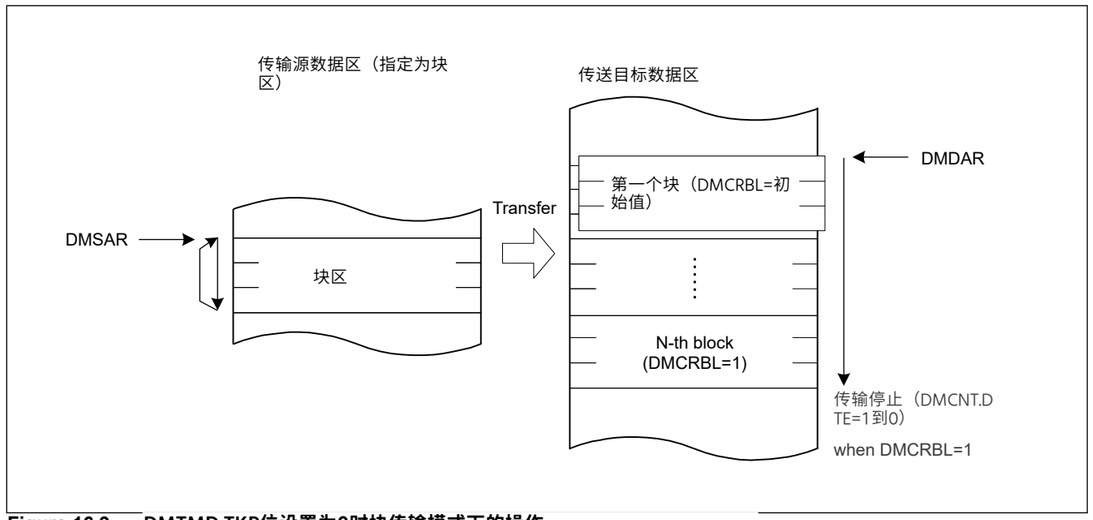

Figure 16.9 DMTMD.TKP位设置为0时块传输模式下的操作

图16.10显示了具有自由运行功能的块传输操作示例。

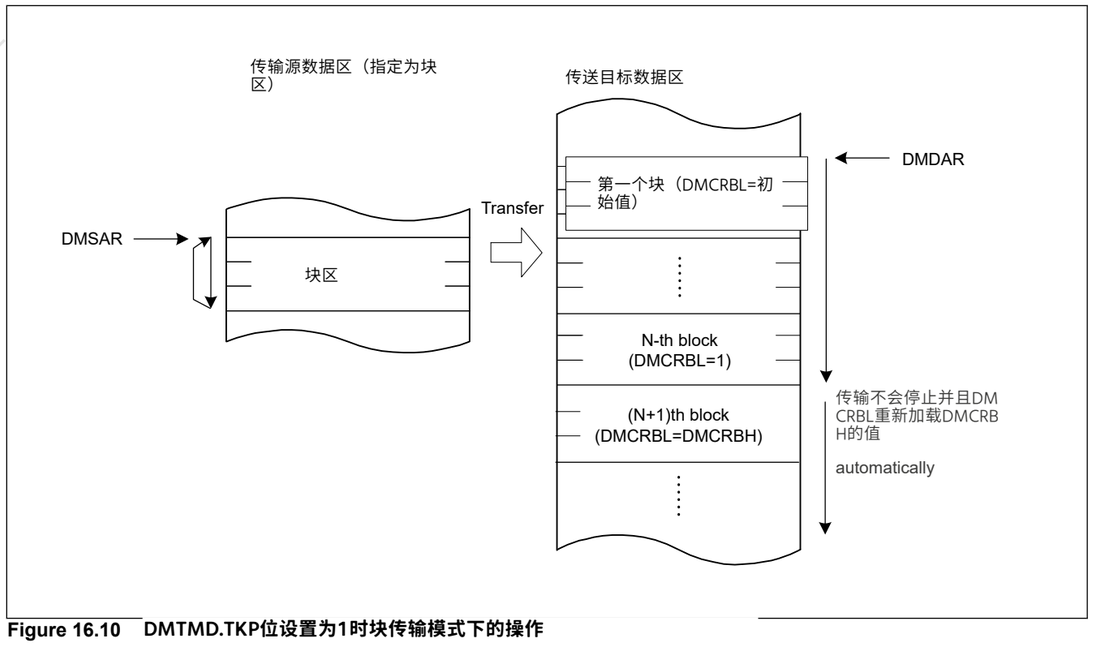

Figure 16.10 DMTMD.TKP位设置为1时块传输模式下的操作

16.3.4 使用偏移的地址更新功能

可以通过固定、递增、递减或偏移添加来更新源地址和目标地址。在正常的重复和块传输模式下，选择偏移添加时，每次DMAC执行一个数据传输时，DMA偏移寄存器（DMOFR）指定的偏移量都会添加到地址。该功能实现了将地址分配到不同区域的数据传输。

偏移量减法也可以通过在DMOFR中设置一个负值来实现。在这种情况下，负值必须是2的补码。

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DMSBS or DMDBS are used instead of DMOFR in repeat-block transfer mode. For more information section 16.3.1.4. Repeat-Block Transfer Mode

Table 16.14 shows the address update method in each address update mode.

Table 16.14 Address Update Method in Each Address Update Mode

Address Update Mode	Settings of DMAMD.SM[1:0] and DMAMD.DM[1:0] for Address Update Modes	Address Update Method (for Different SZ[1:0] Settings in DMTMD)		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

Note 1. When setting a negative value in the DMA Offset Register, the value must be in two's complement, obtained by the following formula:
two's complement of a negative offset value = ~ (offset) + 1 (~ = bit inversion)

16.3.4.1 Basic Transfer Using Offset Addition

Figure 16.11 shows an example of address updating using offset addition.

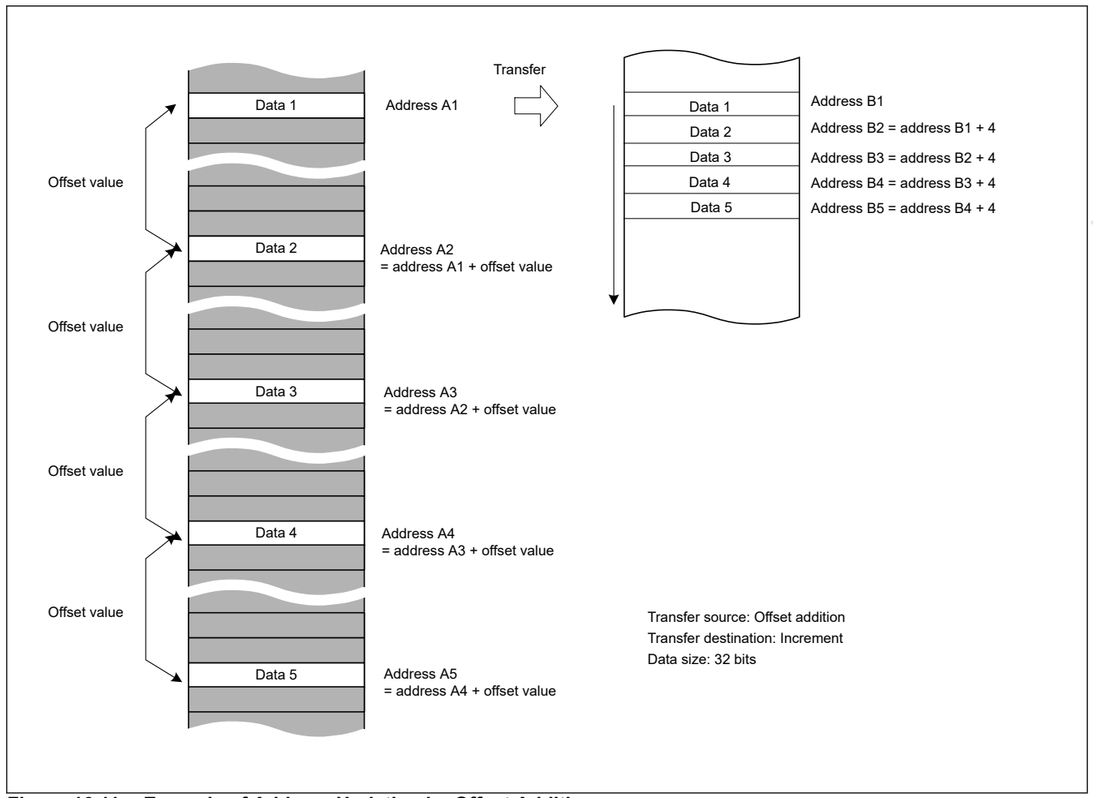

Figure 16.11 Example of Address Updating by Offset Addition

Figure 16.11 shows the setting of the following.

- The transfer data is 32 bits long
- Offset addition is set as the transfer source address update

在重复块传输模式中使用DMSBS或DMDBS代替DMOFR。有关详细信息，请参阅第16.3.1.4节。
重复块传输模式

表16.14显示了每种地址更新模式下的地址更新方法。

Table 16.14 各地址更新模式下的地址更新方法

地址更新模式	DMAMD.SM[1:0]的设置和DMAMD.DM[1:0]用于地址更新Modes	地址更新方法（针对DMTMD中的不同SZ[1:0]设置）		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
地址固定	00b	Fixed		
偏移量加法	01b	+DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	–1	–2	–4

注1.在DMA偏移寄存器中设置负值时，该值必须是二进制补码，由以下公式获得：负偏移值的二进制补码=~(offset)+1(~=bitinversion)

16.3.4.1 使用偏移加法的基本传输

图16.11显示了使用偏移量加法进行地址更新的示例。

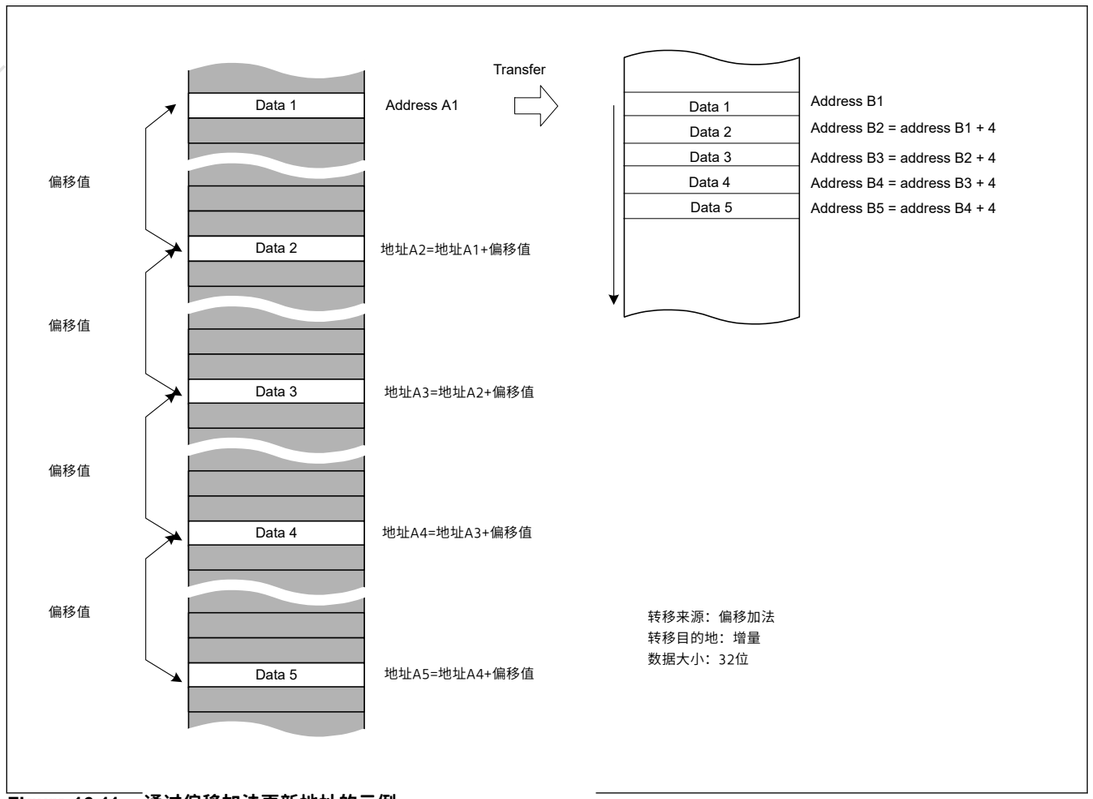

Figure 16.11 通过偏移加法更新地址的示例

图16.11显示了以下设置。

●传输数据为32位长

●偏移量加法设置为传输源地址更新

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- Increment is set as the transfer destination address update mode

The second and subsequent data is each read from the transfer source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to the continuous locations on the destination.

16.3.4.2 Example of XY Conversion Using Offset Addition

Figure 16.12 shows the XY conversion using offset addition in repeat transfer mode.

Settings are as follows:

- DMAMD.SM — Transfer source address update mode: Offset addition
- DMAMD.DM — Transfer destination address update mode: Destination address is incremented.
- DMTMD.SZ — Transfer data size select: 32 bits
- DMTMD.MD — Transfer mode select: Repeat transfer
- DMTMD.DTS — Repeat area select: The source is specified as the repeat area.
- DMOFR — Offset address: 0x10
- DMCRA — Repeat size: 0x4
- DMINT.RPTIE — The repeat size end interrupt is enabled.

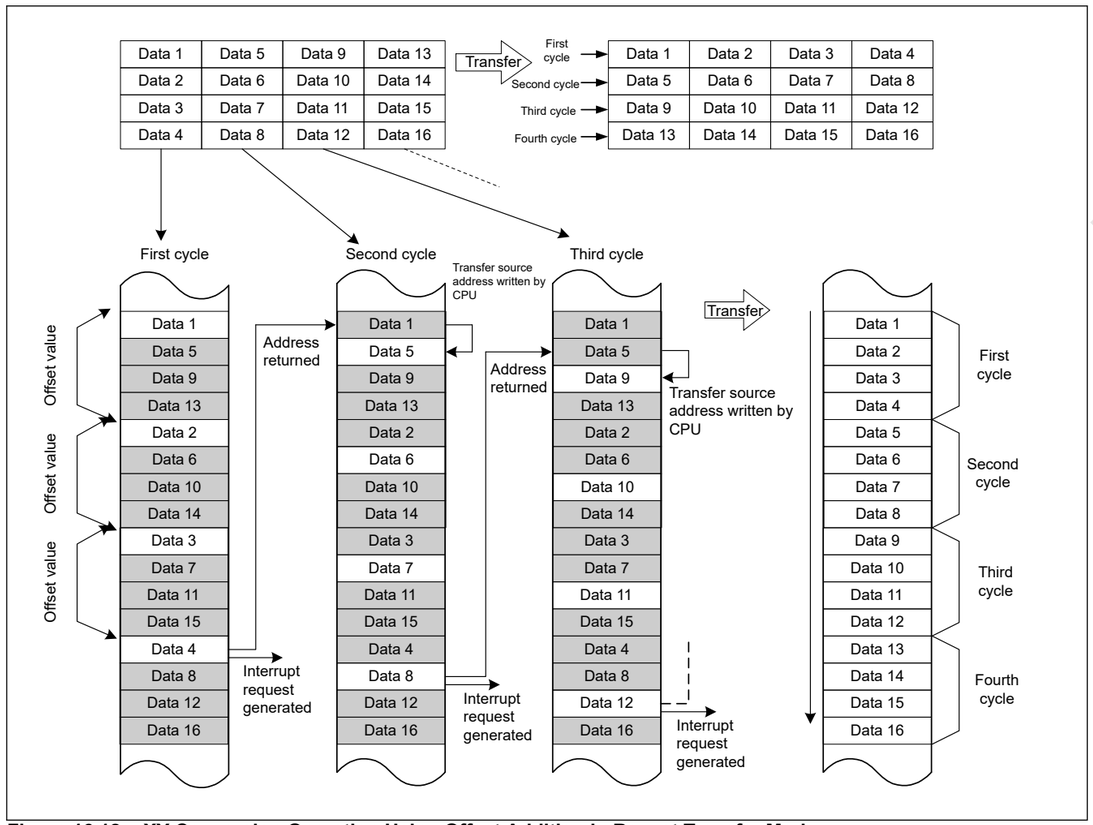

Figure 16.12 XY Conversion Operation Using Offset Addition in Repeat Transfer Mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to continuous transfer destination addresses. When data 4 is transferred:

- The repeat size of data transfer is complete.

●增量设置为传输目标地址更新模式

第二个和随后的数据分别从通过将偏移值与前一个地址相加而获得的传输源地址读取。以指定间隔从地址读取的数据被写入目标上的连续位置。

16.3.4.2 使用偏移加法的XY转换示例

图16.12显示了在重复传输模式下使用偏移添加的XY转换。

设置如下：

●DMAMD.SM—传输源地址更新模式：偏移量加法

●DMAMD.DM—传输目标地址更新模式：目标地址递增。

●DMTMD.SZ—传输数据大小选择：32位

●DMTMD.MD—传输模式选择：重复传输

●DMTMD.DTS—重复区域选择：源被指定为重复区域。

- DMOFR — Offset address: 0x10
- DMCRA — Repeat size: 0x4

●DMINT.RPTIE—启用重复大小结束中断。

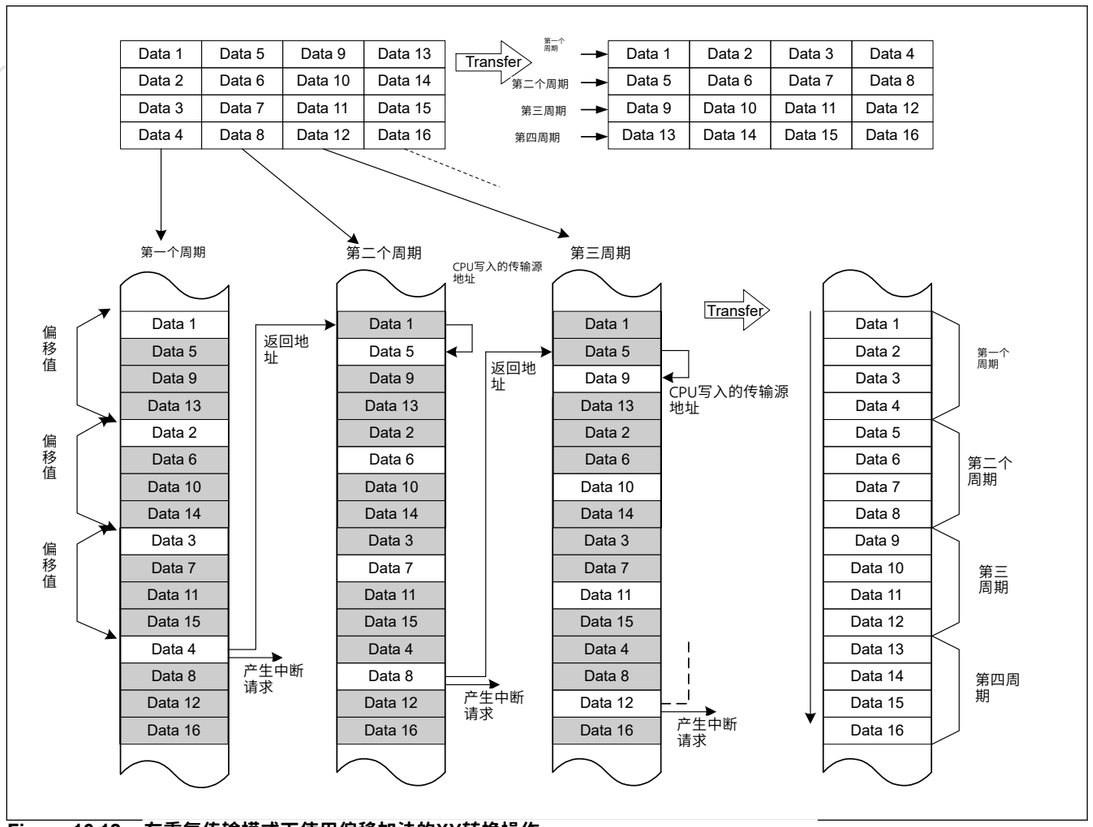

Figure 16.12 在重复传输模式下使用偏移加法的XY转换操作

传输开始时，每次传输数据时，都会将偏移值添加到传输源地址。传输数据被写入连续的传输目标地址。传输数据4时：

●数据传输的重复大小已完成。

- The transfer source address returns to the transfer start address (the address of data 1 on the transfer source).
- A repeat size end interrupt is requested.

During the time this interrupt pauses the transfer, the following operations are performed.

- DMSAR — Rewrite the DMA transfer source address to the address of data 5 (with the above example, the data 1 address + 4).
- DMCNT — Set the DTE bit to 1.

The DMA transfer is resumed from the state when the DMA transfer is stopped. After that, the operations described above are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 16.13 shows a flowchart of the XY conversion.

●传输源地址返回传输起始地址（传输源上数据1的地址）。

●请求重复大小结束中断。

在此中断暂停传输期间，将执行以下操作。

●DMSAR—将DMA传输源地址重写为数据5的地址（在上面的示例中，数据1地址+4）。

●DMCNT—将DTE位设置为1。

DMA传输从DMA传输停止时的状态恢复。之后，重复上述操作，直到将传送源数据转置到目的地区域（XY转换）。

图16.13显示了XY转换的流程图。

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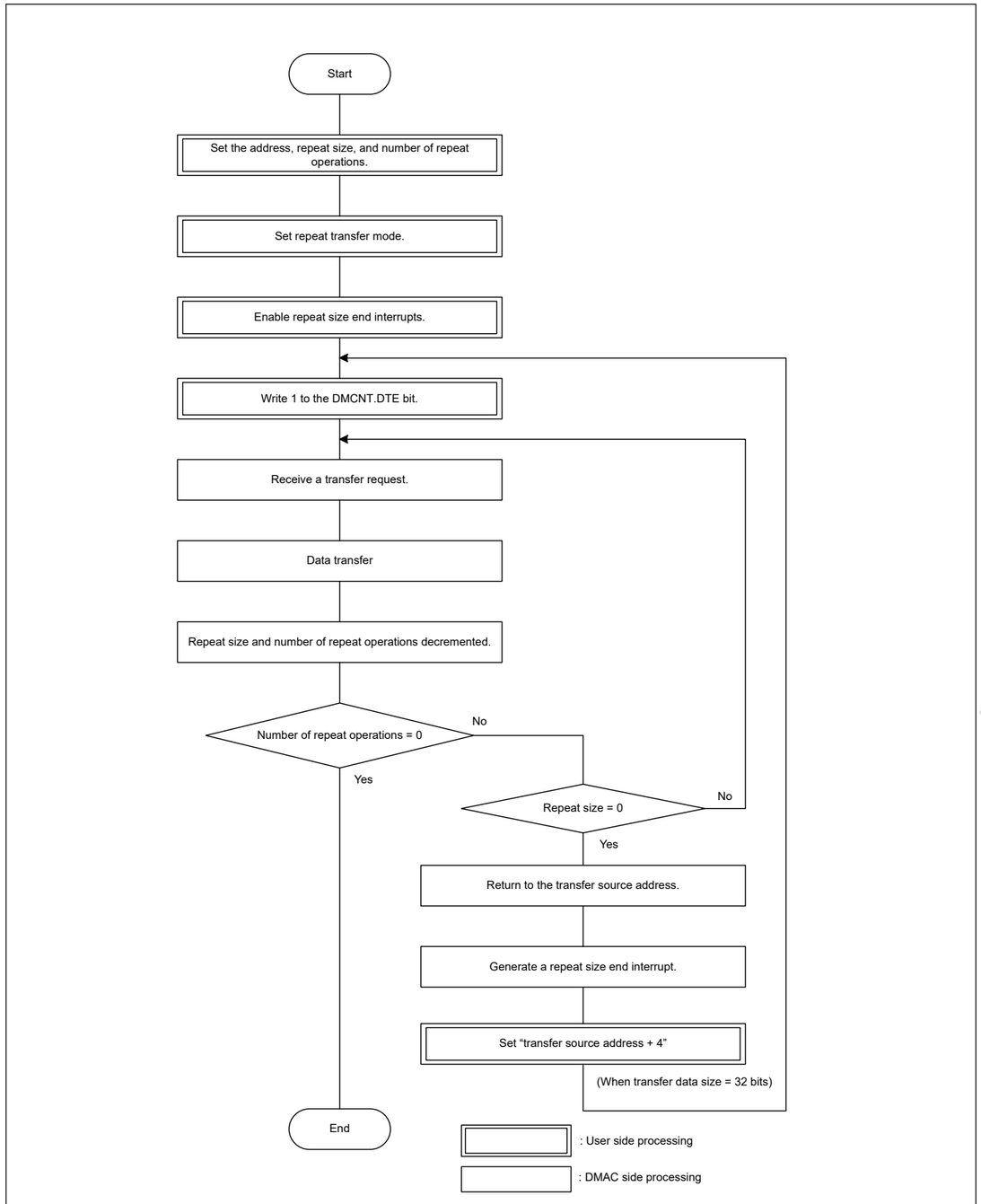

Figure 16.13 XY Conversion Flowchart Using Offset Addition in Repeat Transfer Mode

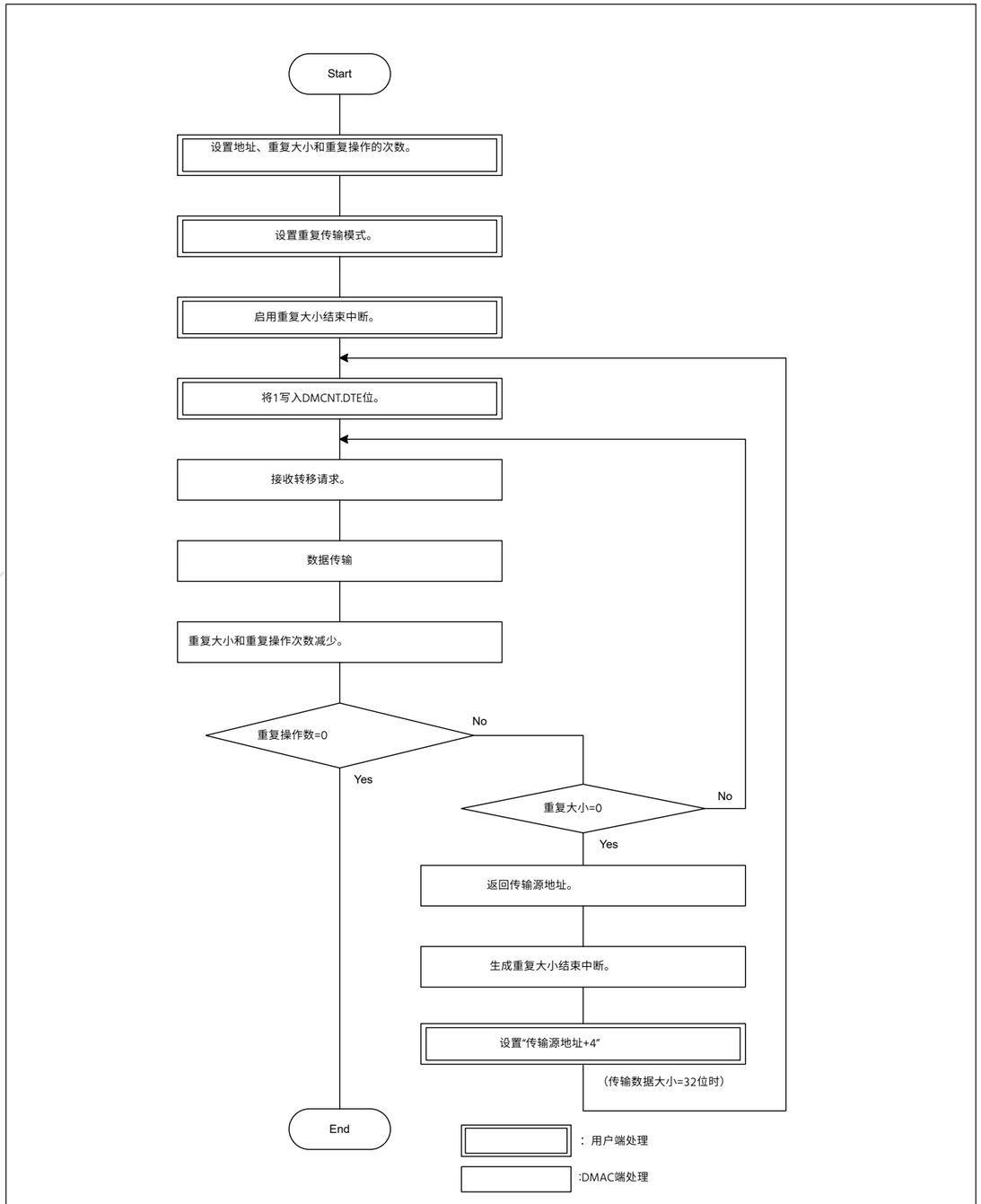

Figure 16.13 重复传输模式下使用偏移加法的XY转换流程图

16.3.5 Address Update Function in Repeat-Block Transfer Mode

Repeat-block transfer mode is an extension of repeat transfer mode and block transfer mode. However, the detailed behavior of the address update is different from these two modes. Here are the details of the address update function in repeat-block transfer mode.

16.3.5.1 Fixed Address Mode

When DMAMD.SM[1:0] is set to 00b, the address update mode of the source is fixed address. And when DMAMD.DM[1:0] is set to 00b, the address update mode of the destination is fixed address.

In fixed address, the address is not updated from the initial value of DMSAR and DMDAR. If the block size (DMCRA) is larger than 1, the same data will be transferred multiple times for one request.

Figure 16.14 shows address update in fixed address.

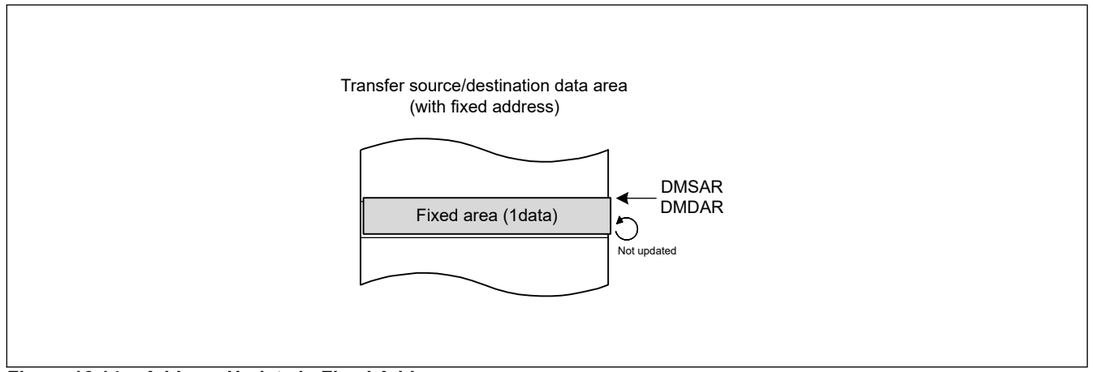

Figure 16.14 Address Update in Fixed Address

16.3.5.2 Incremental and Decremental Address mode

When DMAMD.SM[1:0] is set to 10b, the address update mode of the source is incremental address. And when DMAMD.DM[1:0] is set to 10b, the address update mode of the destination is incremental address. When DMAMD.SM[1:0] is set to 11b, the address update mode of the source is decremental address. And when DMAMD.DM[1:0] is set to 11b, the address update mode of the destination is decremental address.

In these update modes, the address is incremented or decremented according to the setting of DMTMD.SZ[1:0].

In these update modes DMSBS and DMDBS indicates a reload area. The unit of DMSBS and DMDBS is "number of data". At the start of transfer, DMSBSL and DMDBSL, which is the lower 16 bits of DMSBS and DMDBS, operates as a down counter and decrements each time one data transfer is performed. When the value becomes 1, DMSAR and DMDAR reloads the value of DMSRR and DMDRR.

Figure 16.15 shows address update in incremental address.

16.3.5 重复块传输模式中的地址更新功能

重复块传输模式是重　　复传输模式和块传输模式的扩展。但是，地址更新的详细行为与这两种模式不同。以下是重复块传输模式下地址更新功能的详细信息。

16.3.5.1 固定地址模式

当DMAMD.SM[1:0]设置为00b时，源的地址更新方式为固定地址。什么时候DMAMD.DM[1:0]设置为00b，目的地址更新方式为固定地址。

在固定地址中，地址不会从DMSAR和DMDAR的初始值更新。如果块大小（DMCRA）大于1，则一个请求将多次传输相同的数据。

图16.14显示了固定地址中的地址更新。

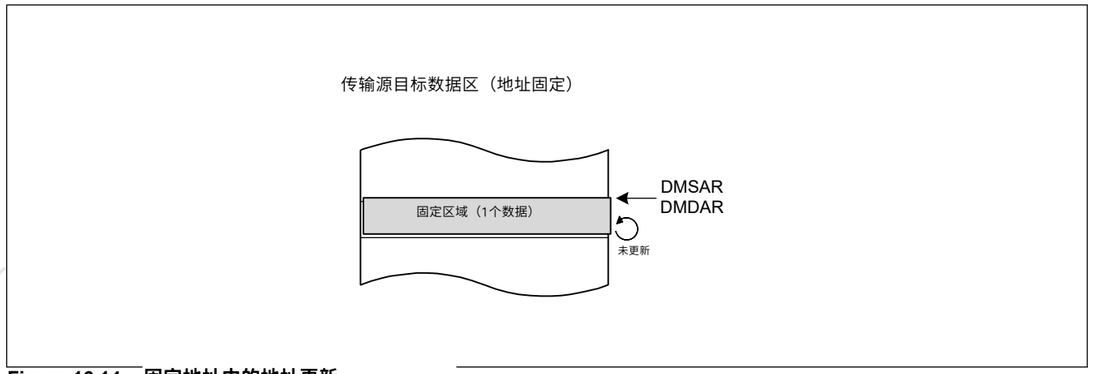

Figure 16.14 固定地址中的地址更新

16.3.5.2 递增和递减地址模式

当DMAMD.SM[1:0]设置为10b时，源地址更新方式为增量地址。什么时候DMAMD.DM[1:0]设置为10b，目的地址更新方式为增量地址。当DMAMD.SM[1:0]设置为11b时，源地址更新方式为递减地址。什么时候

DMAMD.DM[1:0]设置为11b，目的地址更新方式为递减地址。

在这些更新模式中，地址根据DMTMD.SZ[1:0]的设置递增或递减。

在这些更新模式中，DMBSS和DMDBS表示重新加载区域。DMSBS和DMDBS的单位是"数据数"。在传输开始时，作为DMSBS和DMDBS的低16位的DMSBSL和DMDBSL作为递减计数器运行，并在每次执行数据传输时递减。当值变为1时，DMSAR和DMDAR重新加载DMSRR和DMDRR的值。

图16.15显示了增量地址中的地址更新。

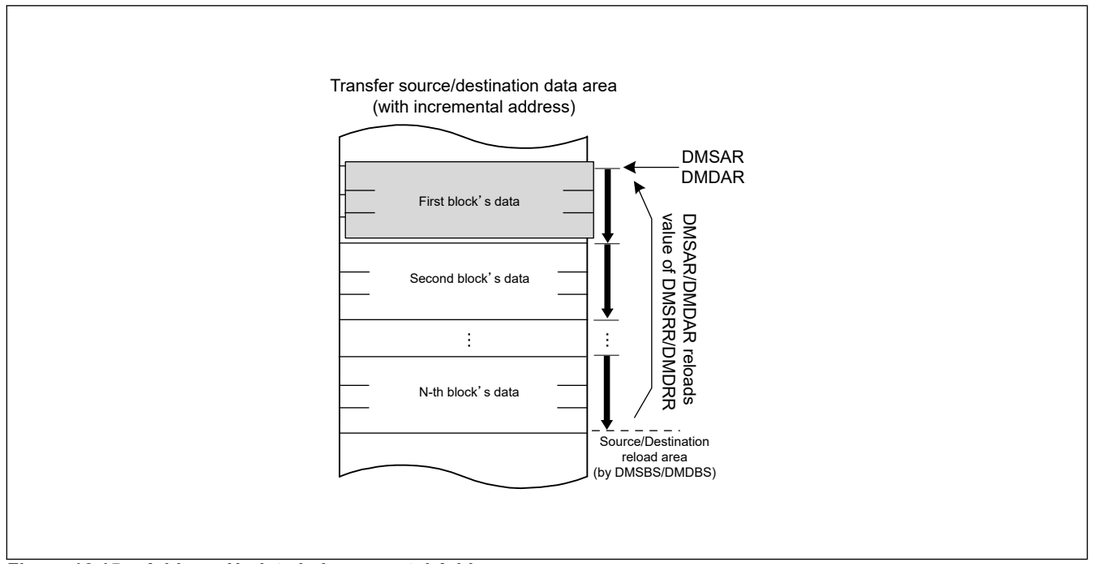

Figure 16.15 Address Update in Incremental Address

16.3.5.3 Offset Addition Mode

When DMAMD.SM[1:0] is set to 01b, the address update mode of the source is offset addition. And when DMAMD.DM[1:0] is set to 01b, the address update mode of the destination is offset addition.

In offset addition, DMSBS and DMDBS indicates reload area and also works as an access offset value. Unlike other transfer modes, DMOFR register is not used in repeat-block transfer mode. In offset addition, the unit of DMSBS and DMDBS is the number of blocks. When the transfer starts, DMCRAL operates as a down counter, DMSAR and DMDAR reloads the value of DMSRR and DMDRR every time one block is transferred. In addition, DMSBSL and DMDBSL, which is the lower 16 bits of DMSBS and DMDBS, also operates as a down counter and decrements every time one block is transferred. When the DMSBS and DMDBS value becomes 1, DMSAR and DMDAR reloads the value of DMSRR and DMDRR.

When DMAMD.SADR and DMAMD.DADR is set to 0, offset addition operation of the same area is repeated. DMDAR only reloads DMDRR. section 16.3.5.3. Offset Addition Mode shows address update in offset addition with DMAMD.SADR and DMAMD.DADR=0.

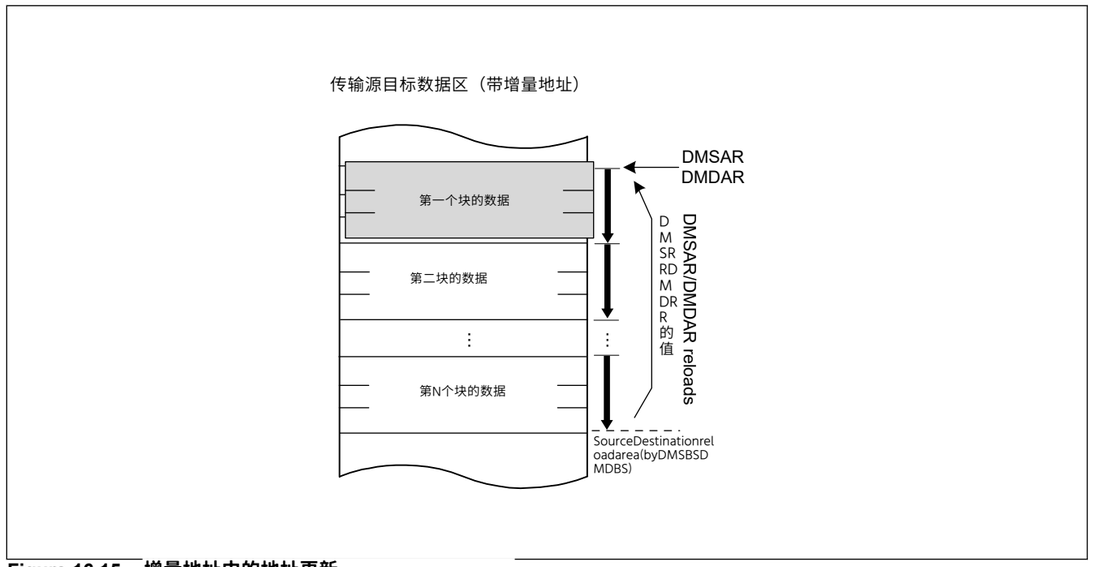

Figure 16.15 增量地址中的地址更新

16.3.5.3 偏移加法模式

当DMAMD.SM[1:0]设置为01b时，源地址更新方式为偏移加法。什么时候DMAMD.DM[1:0]设置为01b，目的地址更新方式为偏移加法。

除了偏移量之外，DMBSS和DMDBS表示重载区域，也用作访问偏移量值。与其他传输模式不同，DMOFR寄存器不用于重复块传输模式。除了偏移量之外，DMSBS和DMDBS的单位是块数。当传输开始时，DMCRAL作为一个递减计数器运行，DMSAR和DMDAR在每次传输一个块时重新加载DMSRR和DMDRR的值。此外，作为DMSBS和DMDBS的低16位的DMSBSL和DMDBSL也用作递减计数器，并且每传输一个块就递减。当DMSBS和DMDBS的值变为1时，DMSAR和DMDAR重新加载DMSRR和DMDRR的值。

当DMAMD.SADR和DMAMD.DADR设置为0时，重复相同区域的偏移添加操作。DMDAR仅重新加载DMDRR。第16.3.5.3节。偏移加法模式显示偏移加法中的地址更新，其中DMAMD.SADR和DMAMD.DADR=0。

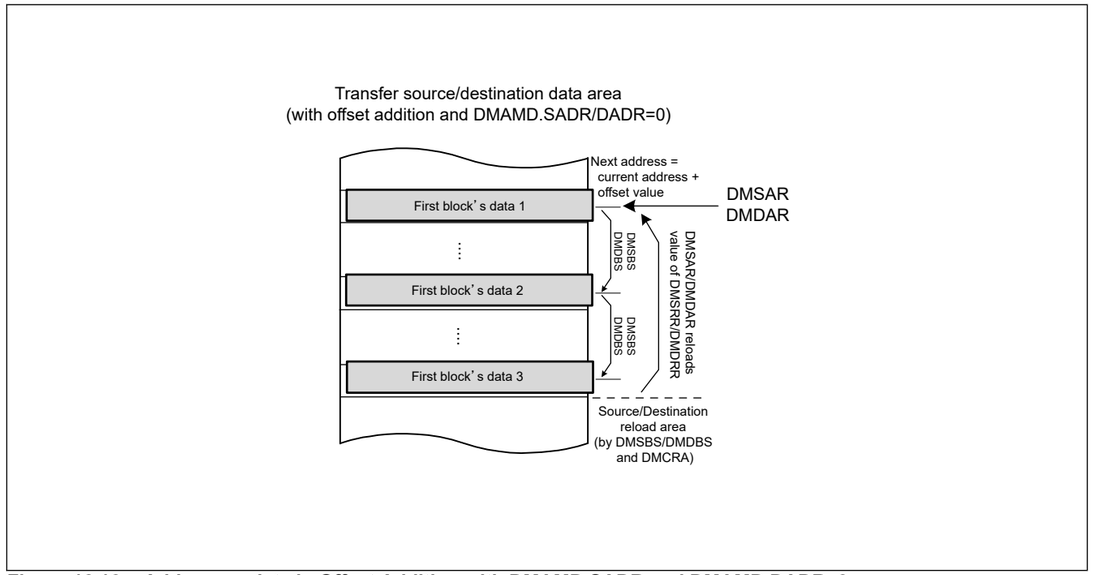

Figure 16.16 Address update in Offset Addition with DMAMD.SADR and DMAMD.DADR=0

When DMAMD.SADR and DMAMD.DADR is set to 1, the address is incremented by one data unit after DMSRR and DMDRR is reloaded by DMCRAL=1. In other words, an index value ((DMDBSH-DMDBSL) × DataSize) is added to DMDAR after DMDRR is reloaded. This behavior is used to implement multiple ring buffers. Figure 16.17 shows address update in offset addition with DMAMD.SADR and DMAMD.DADR=1.

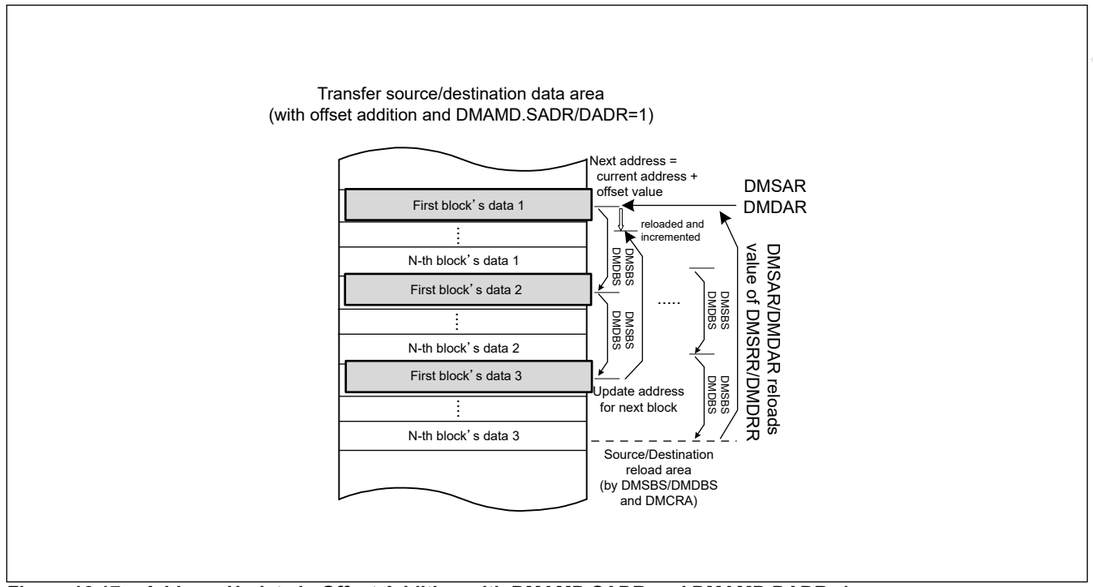

Figure 16.17 Address Update in Offset Addition with DMAMD.SADR and DMAMD.DADR=1

16.3.6 Example of Using Repeat-Block Transfer Mode

In repeat-block transfer mode, it is possible to realize repeated access to interval data and single or multiple ring buffers by combining the above address update modes. Following sections shows some usage examples.

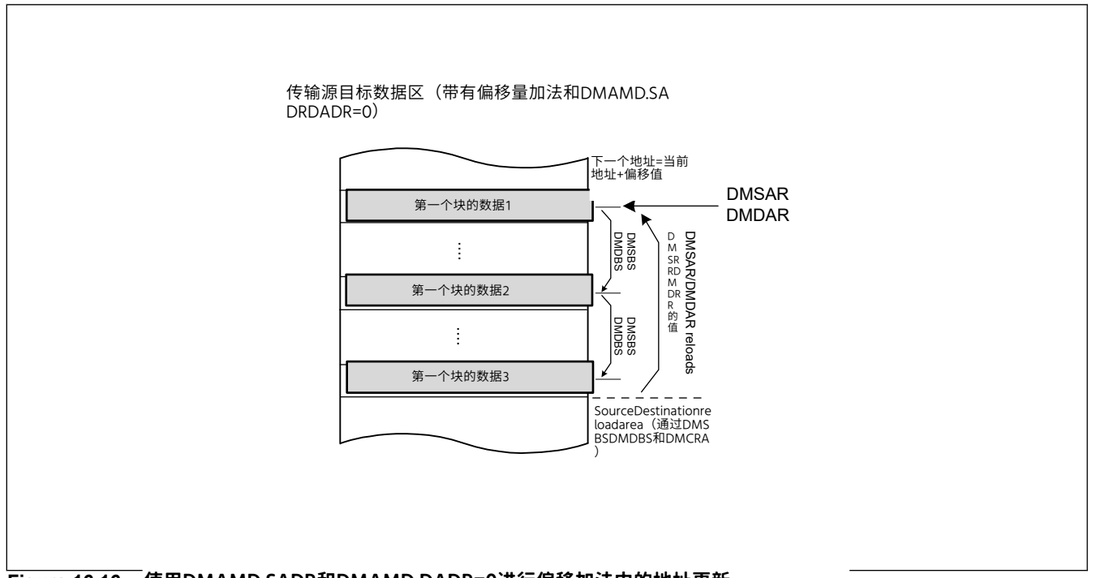

Figure 16.16 使用DMAMD.SADR和DMAMD.DADR=0进行偏移加法中的地址更新

当DMAMD.SADR和DMAMD.DADR设置为1时，在DMSRR和DMCRAL=1重新加载DMDRR后，地址增加一个数据单元。换句话说，一个索引值((DMDBSH-DMDBSL)×DataSize)被添加到
重新加载DMDRR后的DMDAR。此行为用于实现多个环形缓冲区。图16.17显示了DMAMD.SADR和DMAMD.DADR=1的偏移加法中的地址更新。

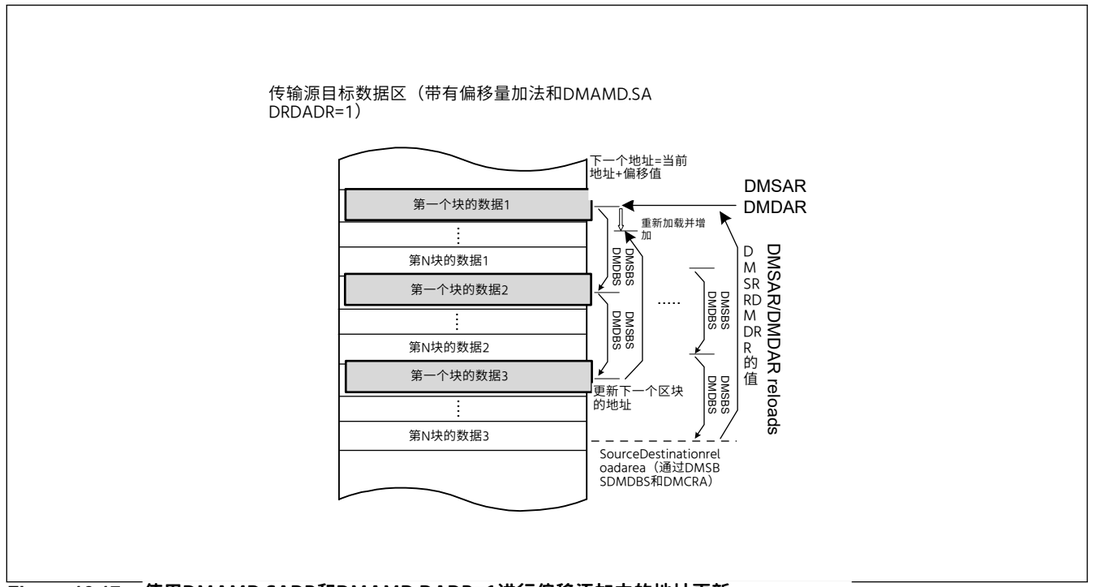

Figure 16.17 使用DMAMD.SADR和DMAMD.DADR=1进行偏移添加中的地址更新

16.3.6 使用重复块传输模式的示例

在重复块传输模式下，结合上述地址更新模式，可以实现对区间数据和单个或多个环形缓冲区的重复访问。以下部分显示了一些使用示例。

16.3.6.1 Interval Address to Single Ring Buffer

Figure 16.18 shows an example of reading interval ADDRn registers (data register) of ADC12 module and storing it in single ring buffer. It transfers 2 data every 4 halfwords per 1 request. DMSAR is incremented by one data every one request. This can be achieved by setting the transfer source to offset addition and DMAMD.SADR=1, the block size (DMCRA) to 2, and the transfer source offset (DMSBS) to 4. Table 16.15 shows setting of this example.

Table 16.15 Setting of use case: from interval address to single ring buffer

Register	Value	Description
DMSAR, DMSRR	0x4017_0020	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	10b	Data size is halfword
DMAMD.SADR	1	Incremental source address after reloading
DMAMD.SM[1:0]	01b	Source update mode is offset addition
DMAMD.DM[1:0]	10b	Destination update mode is incremental address
DMCRAH, DMCRAL	2	Transfer block size
DMSBSH, DMSBSL	4	Source whole buffer size (unit is 'blocks') and Source access offset (unit is 'data')
DMDBSH, DMDBSL	N × 2(DMCRA)	Destination buffer size (unit is 'data')

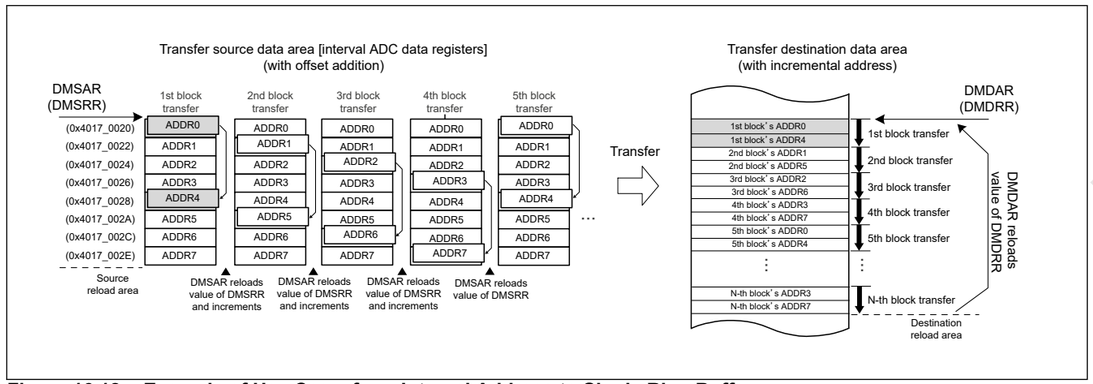

Figure 16.18 Example of Use Case: from Interval Address to Single Ring Buffer

16.3.6.2

16.3.6.2.1 Unaligned Ring Buffer to Single Ring Buffer

Figure 16.19 shows an example of reading ADBUFn registers of ADC12 module (conversion result storage ring buffer) incrementally and storing it in single ring buffer. In this example, wrapping occurs because ADBUFn overflows in the fourth scan, but transfer source address of DMAC is also updated accordingly. This can be realized by setting the transfer source to incremental address and setting the DMSBS register to 16 which is the length of ADBUFn. This makes it possible to continue transfer without performing CPU processing using interrupts. Table 16.16 shows setting of this example.

Table 16.16 Setting of use case: from unaligned ring buffer to single ring buffer (1 of 2)

Register	Value	Description
DMSAR, DMSRR	0x4017_00B0	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	10b	Data size is halfword
DMAMD.SM[1:0]	10b	Source update mode is incremental address

16.3.6.1 单个环形缓冲区的间隔地址

图16.18显示了读取ADC12模块的间隔ADDRn寄存器（数据寄存器）并将其存储在单个环形缓冲区中的示例。它每1个请求每4个半字传输2个数据。DMSAR每请求一个数据就增加一个数据。这可以通过将传输源设置为偏移加法和DMAMD.SADR=1，将块大小(DMCRA)设置为2，将传输源偏移量(DMSBS)设置为4来实现。表16.15显示了此示例的设置。

Table 16.15 用例设置：从区间地址到单环缓冲区

Register	Value	Description
DMSAR, DMSRR	0x4017_0020	初始源地址
DMDAR, DMDRR	0x2000_0000	初始目标地址
DMTMD.SZ[1:0]	10b	数据大小为半字
DMAMD.SADR	1	重载后增量源地址
DMAMD.SM[1:0]	01b	源更新方式为偏移量加法
DMAMD.DM[1:0]	10b	目标更新方式为增量地址
DMCRAH, DMCRAL	2	传输块大小
DMSBSH, DMSBSL	4	源整个缓冲区大小（单位是"块"）和源访问偏移量（单位是"数据"）
DMDBSH, DMDBSL	N × 2(DMCRA)	目标缓冲区大小（单位是"数据"）

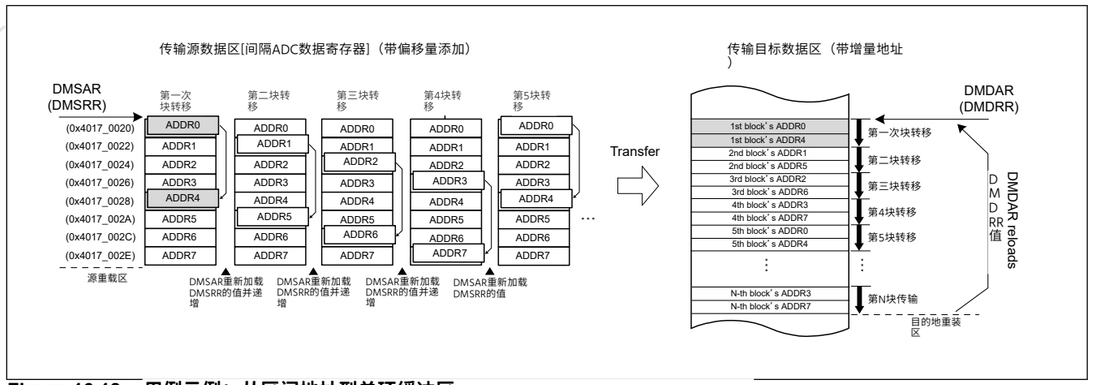

Figure 16.18 用例示例：从区间地址到单环缓冲区

16.3.6.2

16.3.6.2.1 未对齐的环形缓冲区到单个环形缓冲区

图16.19显示了增量读取ADC12模块（转换结果存储环形缓冲区）的ADBUFn寄存器并将其存储在单个环形缓冲区中的示例。在本例中，由于ADBUFn在第四次扫描中溢出，因此发生了回绕，但DMAC的传输源地址也相应更新。这可以通过将传输源设置为增量地址并将DMSBS寄存器设置为16来实现，即ADBUFn的长度。这使得可以在不使用中断执行CPU处理的情况下继续传输。表16.16显示了此示例的设置。

Table 16.16 用例设置：从未对齐的环形缓冲区到单个环形缓冲区（1of2）

Register	Value	Description
DMSAR, DMSRR	0x4017_00B0	初始源地址
DMDAR, DMDRR	0x2000_0000	初始目标地址
DMTMD.SZ[1:0]	10b	数据大小为半字
DMAMD.SM[1:0]	10b	源更新方式为增量地址

Table 16.16 Setting of use case: from unaligned ring buffer to single ring buffer (2 of 2)

Register	Value	Description
DMAMD.DM[1:0]	10b	Destination update mode is incremental address
DMCRAH, DMCRAL	5	Transfer block size
DMSBSH, DMSBSL	16	Source buffer size (unit is 'data')
DMDBSH, DMDBSL	N × 5(DMCRA)	Destination buffer size (unit is 'data')

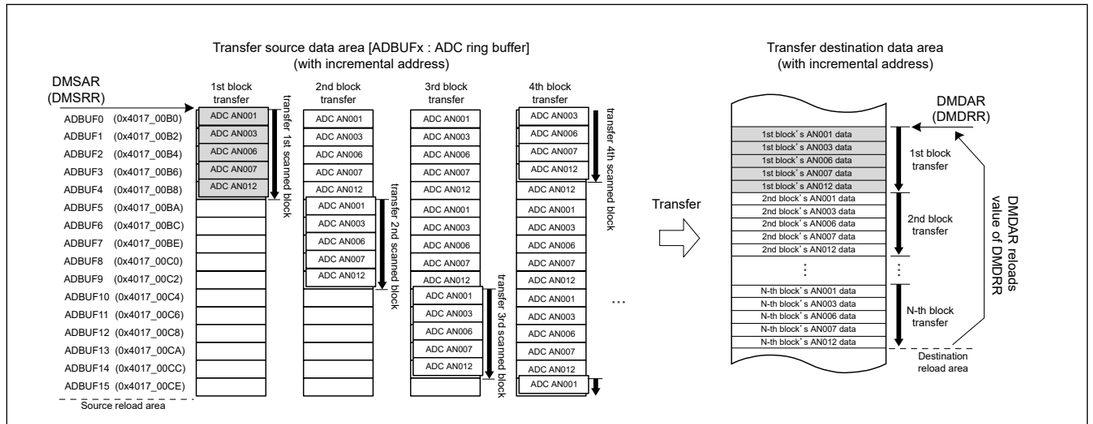

Figure 16.19 Example of Use Case: from Unaligned Ring Buffer to Single Ring Buffer

16.3.6.3 Single Block to Multi Ring Buffer

Figure 16.20 shows an example of storing the continuous ADDRn registers (data register) of ADC12 module individually in multiple ring buffers. In this example, a ring buffer in which only the first element (ADDR0) in a single block is arranged in transfer order is created at the destination. Also, in the next area, create a ring buffer in which only the second element (ADDR1) is arranged in transfer order. In the following case, create a ring buffer of length N, which is defined by DMDBS. And the number of data elements in the block is 3, which is defined by DMCRA. Table 16.17 shows setting of this example.

Table 16.17 Setting of use case: from single block to multi ring buffer

Register	Value	Description
DMSAR, DMSRR	0x4017_0020	Initial source address
DMDAR, DMDRR	0x2000_0000	Initial destination address
DMTMD.SZ[1:0]	10b	Data size is halfword
DMAMD.DADR	1	Incremental destination address after reloading
DMAMD.SM[1:0]	10b	Source update mode is incremental address
DMAMD.DM[1:0]	01b	Destination update mode is offset addition
DMCRAH, DMCRAL	3	Transfer block size
DMSBSH, DMSBSL	3	Source buffer size (unit is 'data')
DMDBSH, DMDBSL	N	Destination whole buffer size (unit is 'blocks') and Destination access offset (unit is 'data')

Table 16.16 用例设置：从未对齐的环形缓冲区到单个环形缓冲区（2of2）

Register	Value	Description
DMAMD.DM[1:0]	10b	目标更新方式为增量地址
DMCRAH, DMCRAL	5	传输块大小
DMSBSH, DMSBSL	16	源缓冲区大小（单位是"数据"）
DMDBSH, DMDBSL	N × 5(DMCRA)	目标缓冲区大小（单位是"数据"）

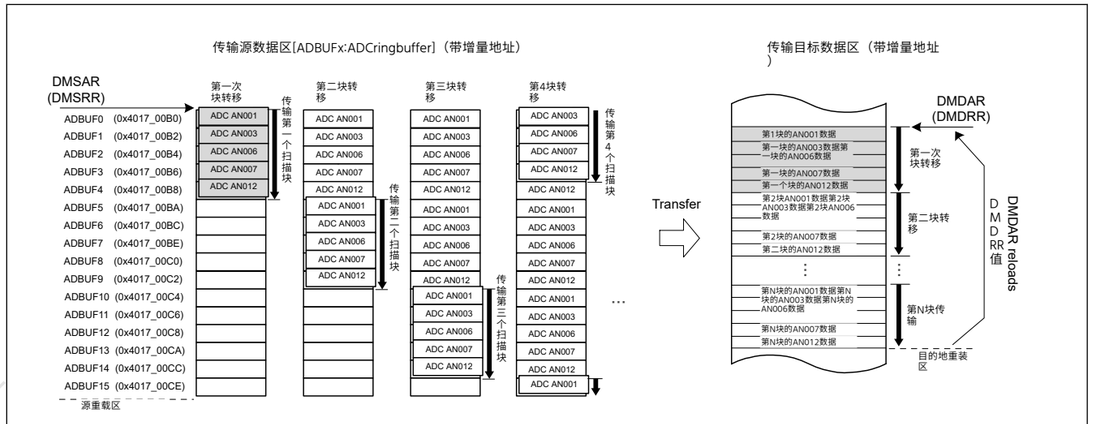

Figure 16.19 用例示例：从未对齐的环形缓冲区到单环形缓冲区

16.3.6.3 单块到多环缓冲区

图16.20显示了将ADC12模块的连续ADDRn寄存器（数据寄存器）单独存储在多个环形缓冲区中的示例。在此示例中，在目的地创建了一个环形缓冲区，其中仅单个块中的第一个元素（ADDR0）按传输顺序排列。此外，在下一个区域中，创建一个环形缓冲区，其中只有第二个元素(ADDR1)按传输顺序排列。在以下情况下，创建一个长度为N的环形缓冲区，由DMDBS定义。块中的数据元素个数为3，由DMCRA定义。表16.17显示了此示例的设置。

Table 16.17 用例设置：从单块到多环缓冲区

Register	Value	Description
DMSAR, DMSRR	0x4017_0020	初始源地址
DMDAR, DMDRR	0x2000_0000	初始目标地址
DMTMD.SZ[1:0]	10b	数据大小为半字
DMAMD.DADR	1	重新加载后的增量目标地址
DMAMD.SM[1:0]	10b	源更新方式为增量地址
DMAMD.DM[1:0]	01b	目的地更新方式为偏移量加法
DMCRAH, DMCRAL	3	传输块大小
DMSBSH, DMSBSL	3	源缓冲区大小（单位是"数据"）
DMDBSH, DMDBSL	N	目标整个缓冲区大小（单位是"块"）和目标访问偏移量（单位是"数据"）

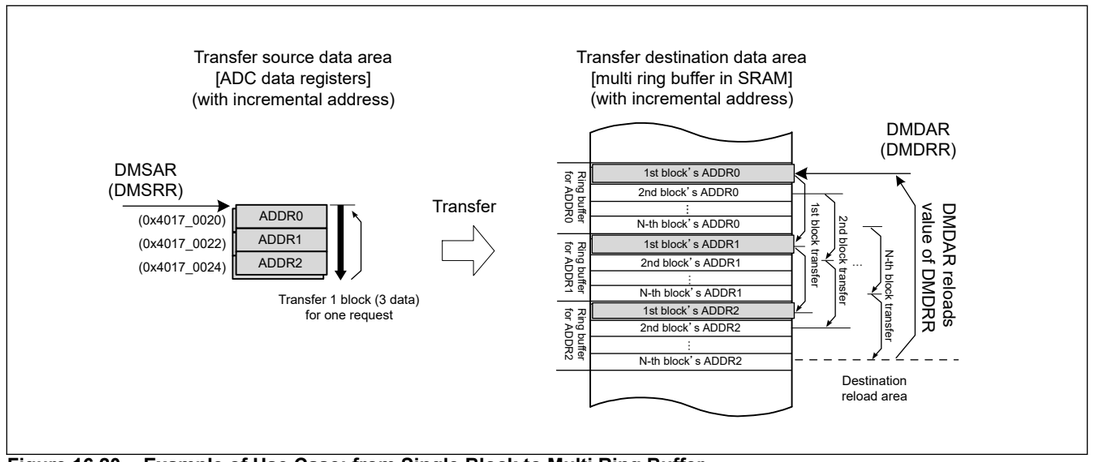

Figure 16.20 Example of Use Case: from Single Block to Multi Ring Buffer

16.3.7 Activation Sources

Software, interrupt requests from the peripheral modules, and external interrupt requests can all be specified as DMAC activation sources. Set the DMTMD.DCTG[1:0] bits to select the activation source.

16.3.7.1 DMAC Activation by Software

When start DMA transfer by software, follow below procedure.

1. Set the DMTMD.DCTG[1:0] bits to 00b
2. Set the DMCNT.DTE bit to 1 (DMA transfer is enabled)
3. Set the DMAST.DMST bit set to 1 (DMAC activation enabled)
4. Set the DMREQ.SWREQ bit to 1 (DMA requested)

When the DMAC is activated by software while the DMREQ.CLRS bit is 0, the DMREQ.SWREQ bit is cleared to 0 after data transfer is started in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, the SWREQ bit is not cleared to 0 after data transfer is started. In this case, a DMA transfer request is issued again after completion of a transfer.

16.3.7.2 DMAC Activation through Interrupt Requests from On-Chip Peripheral Modules or External Interrupt Requests

You can specify interrupt requests from on-chip peripheral modules and external interrupt requests as DMAC activation sources. The activation sources can be selected individually for each channel in ICU.DELSRn.DELS[8:0] (n = 0 to 7).

To start DMA transfer through an interrupt request from an on-chip peripheral module or an external interrupt request, follow the procedures as indicated below.

1. Set ICU.DELSRn.DELS[8:0] (n = 0 to 7) to the event number (select the DMAC event link).
2. Set the DMTMD.DCTG[1:0] bits to 01b (interrupts from the peripheral modules and the external interrupt pins).
3. Set the DMCNT.DTE bit to 1 (enable DMA transfer).
4. Set the DMAST.DMST bit set to 1 (DMAC activation enabled)

For interrupt requests specified as DMAC activation sources, see Table 13.3, in section 13, Interrupt Controller Unit (ICU).

16.3.8 Operation Timing

The following timing charts have indicated the number of execution cycles of the minimum.

Figure 16.21 and Figure 16.22 show DMAC operation timing examples.

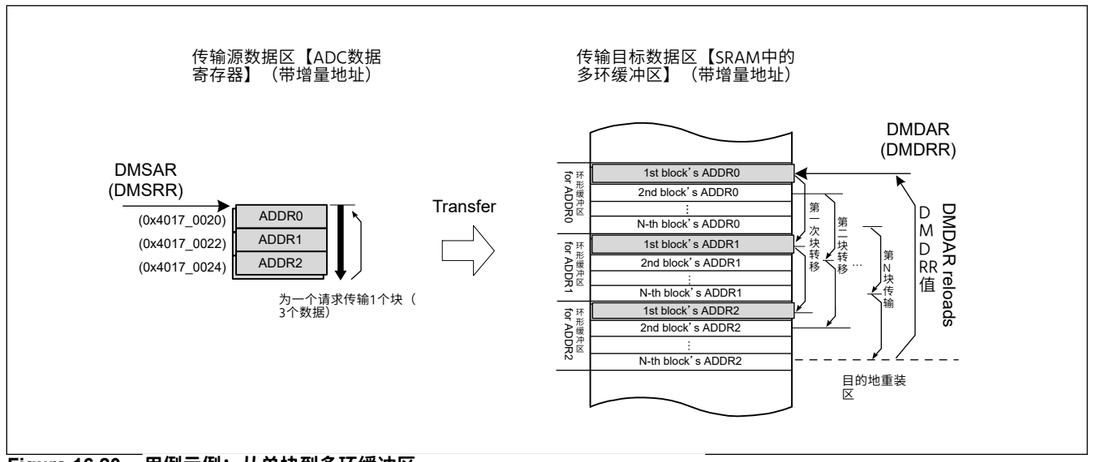

Figure 16.20 用例示例：从单块到多环缓冲区

16.3.7 激活源

软件、外设模块的中断请求和外部中断请求都可以指定为DMAC激活源。设置DMTMD.DCTG[1:0]位以选择激活源。

16.3.7.1 软件激活DMAC

当通过软件启动DMA传输时，请遵循以下步骤。

1.将DMTMD.DCTG[1:0]位设置为00b

2.将DMCNT.DTE位设置为1（启用DMA传输）

3.将DMAST.DMST位设置为1（启用DMAC激活）

4.将DMREQ.SWREQ位设置为1（请求DMA）

当DMREQ.CLRS位为0时由软件激活DMAC时，在响应DMA传输请求开始数据传输后，DMREQ.SWREQ位清零。

当CLRS位为1时由软件激活DMAC时，数据传输开始后SWREQ位不会被清零。在这种情况下，在传输完成后再次发出DMA传输请求。

16.3.7.2 通过来自片上外围模块或外部中断请求的中断请求激活DMAC

您可以将来自片上外围模块的中断请求和外部中断请求指定为DMAC激活源。可以为ICU.DELSRn.DELS[8:0]（n=0到7）中的每个通道单独选择激活源。

要通过来自片上外围模块的中断请求或外部中断请求启动DMA传输，请按照以下步骤操作。

1.将ICU.DELSRn.DELS[8:0]（n=0到7）设置为事件编号（选择DMAC事件链接）。

2.将DMTMD.DCTG[1:0]位设置为01b（来自外围模块和外部中断引脚的中断）。

3.将DMCNT.DTE位设置为1（启用DMA传输）。

4.将DMAST.DMST位设置为1（启用DMAC激活）

对于指定为DMAC激活源的中断请求，请参见第13节“中断控制器单元(ICU)”中的表13.3。

16.3.8 操作时间

下面的时序图已经表明了最小的执行周期数。

图16.21和图16.22显示了DMAC操作时序示例。

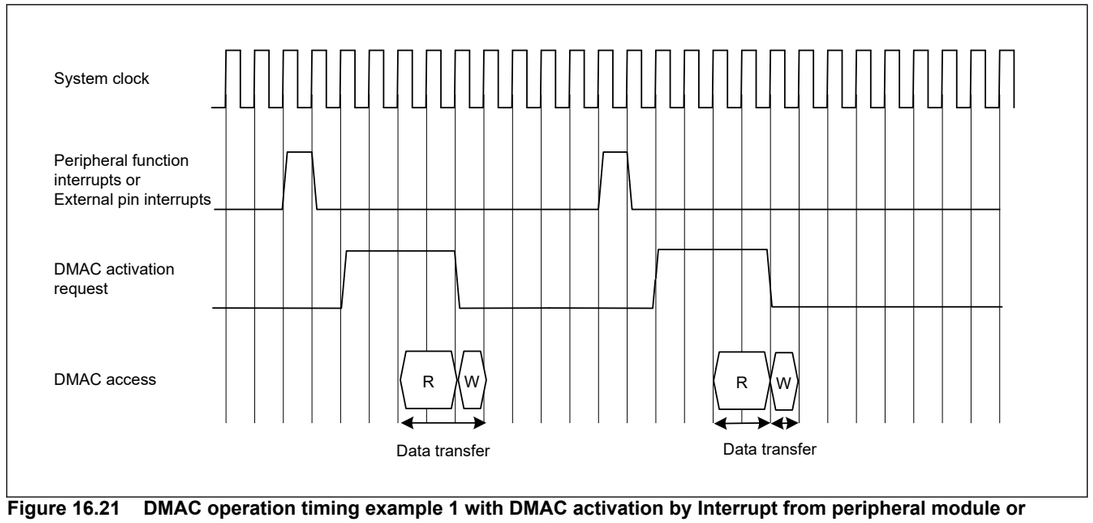

Figure 16.21 DMAC operation timing example 1 with DMAC activation by Interrupt from peripheral module or external interrupt input pin, in normal transfer mode or repeat transfer mode

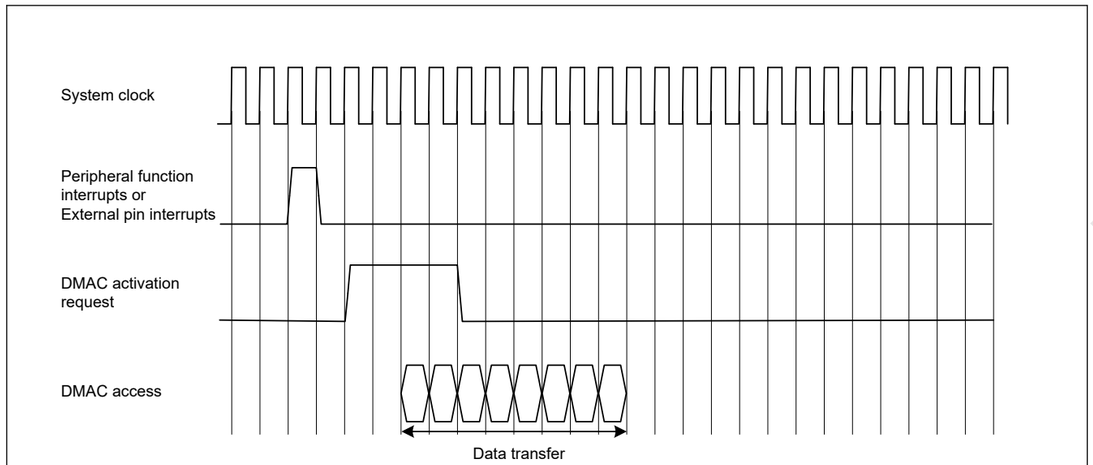

Figure 16.22 DMAC operation timing example 2 with DMAC activation by interrupt from peripheral module or external interrupt input pin, in block transfer mode with block size = 4

16.3.9 DMAC Execution Cycles

Table 16.18 lists execution cycles in one DMAC data transfer operation.

Table 16.18 DMAC Execution Cycles

Transfer Mode	Data Transfer (Read)	Data Transfer (Write)
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P: Block size (DMCRAH register setting)
Cr: Data read destination access cycle
Cw: Data write destination access cycle
Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle is applied.

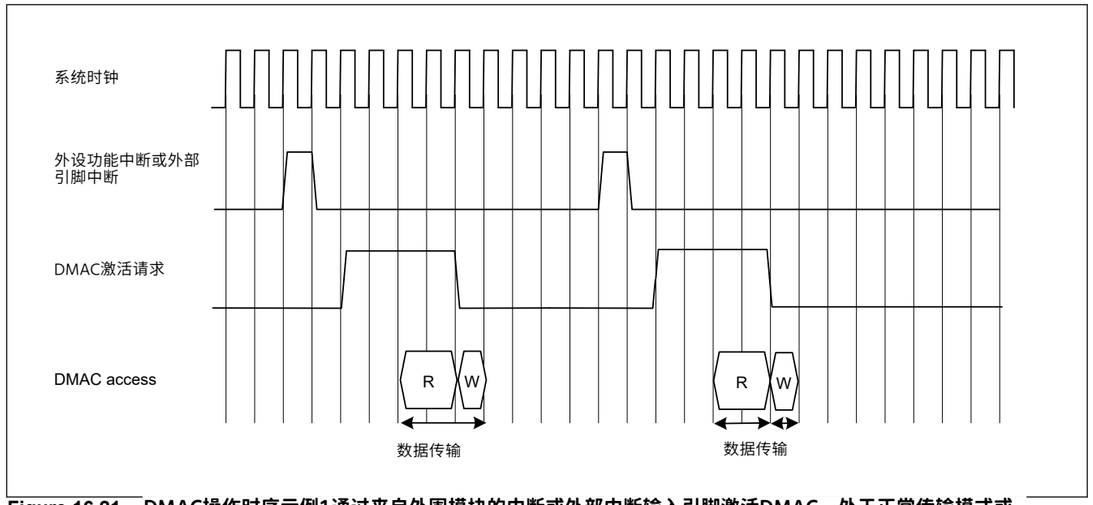

Figure 16.21 DMAC操作时序示例1通过来自外围模块的中断或外部中断输入引脚激活DMAC，处于正常传输模式或重复传输模式

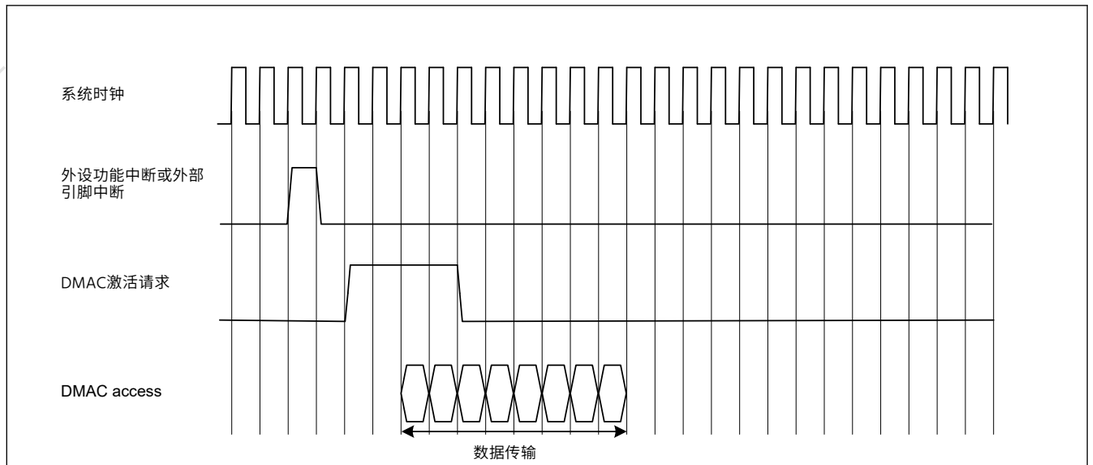

Figure 16.22 DMAC操作时序示例2，通过来自外围模块或外部中断输入引脚的中断激活DMAC，在块大小=4的块传输模式下

16.3.9 DMAC执行周期

表16.18列出了一个DMAC数据传输操作中的执行周期。

Table 16.18 DMAC执行周期

传输模式	数据传输（读取）	数据传输（写入）
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	P × Cr	P × Cw

Note: P：块大小（DMCRAH寄存器设置）Cr：数据读取目标访问周期Cw：数据写入目标访问周期
注1.这是块大小为2或更大的情况。当块大小为1时，应用正常传输周期。

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Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 48, SRAM, section 50, Flash Memory, section 14, Buses. The frequency ratio of the system clock and the peripheral clock is also taken into consideration.

The unit for +1 in “Data Transfer (Read)” column is one system clock cycle (ICLK). For the operation example, see section 16.3.8. Operation Timing.

16.3.10 Activating the DMAC

Table 16.19 shows the register setting procedure of normal, repeat and block transfer mode and Table 16.20 shows register setting procedure of repeat-block transfer mode.

Table 16.19 Register Setting Procedure of Normal Transfer Mode, Repeat Transfer Mode and Block Transfer Mode (1 of 2)

No.	Step Name	Description
1	Disable the peripheral function as the DMACn request source.	To use peripheral function interrupts as DMAC activation sources. Disable the control register for the peripheral function.
2	Disable the IRQn pin as the DMACn request source.	To use external pin interrupts as DMAC activation sources.
3	Set the DMACn Event Link select (ICU.DELSRn.DELS[8:0]) to 0x00	Disable the DMACn request.
4	Clear the DMCNT.DTE bit to 0	Disable DMA transfer.
5	Set the interrupt request as a DMACn request source in the DMAC Event Link Setting Register (ICU.DELSRn) by using the ICU.	To use internal peripheral interrupts or external pin interrupts as DMAC activation sources. Enable the interrupt bit for the activation source. Set the DMACn activation source.
6	Set the peripheral module as a DMACn request source	To use peripheral function interrupt as a DMAC activation source. Set the control register for the peripheral function without starting it.
7	Set the IRQn pin function by using the ICU.	To use external pin interrupt as a DMAC activation source. Set the IRQn pin function by using the Interrupt Controller Unit.
8	Set the DMAMD.DM[1:0] bits Set the DMAMD.SM[1:0] bits Set the DMAMD.DARA[4:0] bits Set the DMAMD.SARA[4:0] bits	Set the Transfer destination address update mode bits Set the Transfer source address update mode bits Set the Transfer destination address extended repeat area bits Set the Transfer source address extended repeat area bits
9	Set the DMTMD.DCTG[1:0] bits Set the DMTMD.SZ[1:0] bits Set the DMTMD.DTS[1:0] bits Set the DMTMD.MD[1:0] bits Set the DMTMD.TKB bit	Set the Transfer request select bits Set the Data transfer size bits Set the Repeat area select bits Set the Transfer mode select bits Set the transfer keeping select bit
10	Set the DMSAR register Set the DMDAR register Set the DMCRA register	Set the transfer source start address. Set the transfer destination start address. Set the number of transfer operations.
11	Set the DMCRB register	To use block transfer mode or repeat transfer mode. Set the number of block transfer operations.
12	Set the DMOFR register	To use the address update function with offset. Set the offset value.
13	Set the DMINT.DTIE bit to 1	To use the DMA transfer end interrupts. Enable DMACn transfer end interrupts.
14	Set the DMINT.RPTIE bit Set the DMINT.SARIE bit Set the DMINT.DARIE bit Set the DMINT.ESIE bit to 1	To use the DMA transfer escape end interrupts Set the repeat size end interrupt. Set the transfer source address extended repeat area overflow interrupt. Set the transfer destination address extended repeat area overflow interrupt. Enable the DMA transfer escape end interrupt.
15	Set the DMCNT.DTE bit to 1	Enable DMA transfer.

Cr和Cw取决于访问目的地。对于每个访问目标的周期数，请参阅第48节，SRAM，第50节，闪存，第14节，总线。系统时钟和外设时钟的频率比也被考虑在内。

“数据传输（读取）”列中+1的单位是一个系统时钟周期（ICLK）。操作示例见16.3.8节。操作时间。

16.3.10 激活DMAC

表16.19显示了正常、重复和块传输模式的寄存器设置过程，表16.20显示了重复块传输模式的寄存器设置过程。

Table 16.19 正常传输模式、重复传输模式和块传输的寄存器设置过程
模式（2个中的1个）

No.	步骤名称	Description
1	禁用外设功能作为DMACn请求源。	使用外设功能中断作为DMAC激活源。禁用外围功能的控制寄存器。
2	禁用IRQn引脚作为DMACn请求源。	使用外部引脚中断作为DMAC激活源。
3	将DMACn事件链接选择(ICU.DELSRn.DELS[8:0])设置为0x00	禁用DMACn请求。
4	将DMCNT.DTE位清0	禁用DMA传输。
5	将中断请求设置为DMACn请求源 DMAC事件链接设置寄存器(ICU.DELSRn)通过使用 ICU.	使用内部外设中断或外部引脚中断作为DMAC激活源。 启用激活源的中断位。设置DMACn激活源。
6	将外设模块设置为DMACn请求源	使用外设功能中断作为DMAC激活源。设置外围功能的控制寄存器而不启动它。
7	使用ICU设置IRQn引脚功能。	使用外部引脚中断作为DMAC激活源。 使用中断控制器单元设置IRQn引脚功能。
8	设置DMAMD.DM[1:0]位设置 DMAMD.SM[1:0]位 设置DMAMD.DARA[4:0]位设置 DMAMD.SARA[4:0]位	设置传输目标地址更新模式位 设置传输源地址更新模式位 设置传输目标地址扩展重复区域位 设置传输源地址扩展重复区域位
9	设置DMTMD.DCTG[1:0]位 设置DMTMD.SZ[1:0]位设置D MTMD.DTS[1:0]位设置DMTM D.MD[1:0]位 设置DMTMD.TKB位	设置传输请求选择位 设置数据传输大小位设置重复 区域选择位 设置传输模式选择位设置传输保 持选择位
10	设置DMSAR寄存器设置 DMDAR寄存器设置DMC RA寄存器	设置传输源起始地址。设置传送目的地起 始地址。 设置传输操作的次数。
11	设置DMCRB寄存器	使用块传输模式或重复传输模式。 设置块传输操作的数量。
12	设置DMOFR寄存器	使用带偏移量的地址更新功能。 设置偏移值。
13	将DMINT.DTIE位设置为1	使用DMA传输结束中断。启用DMACn 传输结束中断。
14	设置DMINT.RPTIE位设置 DMINT.SARIE位设置DMI NT.DARIE位 将DMINT.ESIE位设置为1	使用DMA传输转义结束中断 设置重复尺寸结束中断。 设置传输源地址扩展重复区溢出中断。设置传送目标地址扩展 重复区域溢出中断。启用DMA传输转义结束中断。
15	将DMCNT.DTE位设置为1	启用DMA传输。

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Table 16.19 Register Setting Procedure of Normal Transfer Mode, Repeat Transfer Mode and Block Transfer Mode (2 of 2)

No.	Step Name	Description
16	Set the DMAST.DMST bit to 1	Enable DMAC operation. *1 Common settings for DMAC
17	Start the peripheral function as a DMACn request source	To use peripheral function interrupt as a DMAC activation source
18	Enable the IRQn pin as a DMACn request source	To use external pin interrupt as a DMAC activation source
19	End of initial settings	For activation by software On completion of the initial settings, writing 1 to the DMA software start bit (DMREQ.SWREQ) starts DMA transfer.

Note: n: DMAC channel (n = 0 to 7)
Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

Table 16.20 Register Setting Procedure of Repeat-Block Transfer Mode (1 of 2)

No.	Step Name	Description
1	Disable the peripheral function as the DMACn request source.	To use peripheral function interrupts as DMA activation sources. Disable the control register for the peripheral function.
2	Disable the IRQ pin as the DMACn request source.	To use external pin interrupts as DMA activation sources.
3	Set the DMACn Event Link select (ICU.DELSRn.DELS[8:0]) to 00h	Disable the DMACn request.
4	Clear the DMCNT.DTE bit to 0	Disable DMACn transfer.
5	Set the interrupt request as a DMACn request source in the DMACn Event Link Setting Register (ICU.DELSRn) by using the ICU.	To use internal peripheral interrupts or external pin interrupts as DMA activation sources. Enable the interrupt bit for the activation source. Set the DMACn activation source.
6	Set the peripheral module as a DMACn request source	To use peripheral function interrupt as a DMA activation source. Set the control register for the peripheral function without starting it.
7	Set the IRQ pin function by using the Interrupt Controller Unit.	To use external pin interrupt as a DMA activation source. Set the IRQ pin function by using the Interrupt Controller Unit.
8	Set the DMAMD.DM[1:0] bits Set the DMAMD.SM[1:0] bits Set the DMAMD.DARA[4:0] bits Set the DMAMD.SARA[4:0] bits Set the DMAMD.DADR[4:0] bits Set the DMAMD.SADR[4:0] bits	Set the Transfer destination address update mode bits Set the Transfer source address update mode bits Set the Transfer destination address extended repeat area bits Set the Transfer source address extended repeat area bits Set the Transfer destination address update select after reload Set the Transfer source address update select after reload
9	Set the DMTMD.DCTG[1:0] bits Set the DMTMD.SZ[1:0] bits Set the DMTMD.MD[1:0] bits Set the DMTMD.TKB bit	Set the Transfer request select bits Set the Data transfer size bits Set the Transfer mode to repeat-block transfer mode Set the transfer keeping select bit
10	Set the DMSAR register Set the DMDAR register Set the DMSRR register Set the DMDRR register Set the DMCRA register Set the DMCRB register	Set the transfer source start address Set the transfer destination start address Set the initial value of source start address Set the initial value of destination start address Set the number of transfer operations Set the number of block transfer operations
11	Set the DMSBS register Set the DMDBS register	To use the address update function with incremental, decremental or offset Set the source buffer size and access offset Set the destination buffer size and access offset
12	Set the DMINT.DTIE bit to 1	To use DMA transfer end interrupts. Enable DMACn transfer end interrupts.
13	Set the DMCNT.DTE bit to 1	Enable DMACn transfer
14	Set the DMAST.DMST bit to 1	Enable DMAC operation. *1*1
15	Start the peripheral function as a DMACn request source	To use peripheral function interrupt as a DMA activation source

Table 16.19 正常传输模式、重复传输模式和块传输的寄存器设置过程 模式（2之2）

No.	步骤名称	Description
16	将DMAST.DMST位设置为1	启用DMAC操作。*1 DMAC的常用设置
17	作为DMACn请求源启动外设功能	使用外设功能中断作为DMAC激活源
18	启用IRQn引脚作为DMACn请求源	使用外部引脚中断作为DMAC激活源
19	初始设置结束	通过软件激活 初始设置完成后，将1写入DMA软件启动位(DMREQ.SWREQ)开始DMA传输。

Note: n：DMAC通道（n=0到7）
注1.DMAST.DMST位设置不一定要遵循各个激活源的设置。

Table 16.20 重复块传输模式的寄存器设置过程（1of2）

No.	步骤名称	Description
1	禁用外设功能作为DMACn请求源。	使用外设功能中断作为DMA激活源。 禁用外围功能的控制寄存器。
2	禁用IRQ引脚作为DMACn请求源。	使用外部引脚中断作为DMA激活源。
3	将DMACn事件链接选择(ICU.DELSRn.DELS[8:0])设置为00h	禁用DMACn请求。
4	将DMCNT.DTE位清0	禁用DMACn传输。
5	将中断请求设置为DMACn请求源 DMACn事件链接设置寄存器(ICU.DELSRn)通过使用ICU.	使用内部外设中断或外部引脚中断作为DMA激活源。 启用激活源的中断位。 设置DMACn激活源。
6	将外设模块设置为DMACn请求源	使用外设功能中断作为DMA激活源。设置外围功能的控制寄存器而不启动它。
7	使用中断控制器单元设置IRQ引脚功能。	使用外部引脚中断作为DMA激活源。 使用中断控制器单元设置IRQ引脚功能。
8	设置DMAMD.DM[1:0]位设置 DMAMD.SM[1:0]位 设置DMAMD.DARA[4:0]位设置 DMAMD.SARA[4:0]位设置DMA MD.DADR[4:0]位设置DMAMD.S ADR[4:0]位	设置传输目标地址更新模式位 设置传输源地址更新模式位 设置传输目标地址扩展重复区域位设置传输源地址扩展重复区域位设置重载后传输目标地址更新选择 重新加载后设置传输源地址更新选择
9	设置DMTMD.DCTG[1:0]位 设置DMTMD.SZ[1:0]位设置D MTMD.MD[1:0]位 设置DMTMD.TKB位	设置传输请求选择位 设置数据传输大小位 将传输模式设置为重复块传输模式 设置传输保持选择位
10	设置DMSAR寄存器设置 DMDAR寄存器设置DMS RR寄存器设置DMDRR寄 存器设置DMCRA寄存器 设置DMCRB寄存器	设置传输源起始地址 设置传输目标起始地址 设置源起始地址的初始值 设置目的起始地址的初始值 设置传输操作的次数 设置块传输操作的数量
11	设置DMSBS寄存器设置 DMDBS寄存器	使用增量、减量或偏移的地址更新功能设置源缓冲区大小和访问偏移量 设置目标缓冲区大小和访问偏移量
12	将DMINT.DTIE位设置为1	使用DMA传输结束中断。 启用DMACn传输结束中断。
13	将DMCNT.DTE位设置为1	启用DMACn传输
14	将DMAST.DMST位设置为1	启用DMAC操作。*1*1
15	作为DMACn请求源启动外设功能	使用外设功能中断作为DMA激活源

Table 16.20 Register Setting Procedure of Repeat-Block Transfer Mode (2 of 2)

No.	Step Name	Description
16	Enable the IRQ pin as a DMACn request source	To use external pin interrupt as a DMA activation source
17	End of initial settings	For activation by software On completion of the initial settings, writing 1 to the DMA software start bit (DMREQ.SWREQ) starts DMA transfer.

Note: m: DELSRn.DELS bit number (m = 0 to 8)
n: DMAC channel (n = 0 to 7)
Note 1. The DMAST.DMST bit setting does not necessarily have to follow the settings for the individual activation sources.

16.3.11 Starting DMA Transfer

To enable the DMA transfer, set the DMCNT.DTE bit to 1 (enable the DMA transfer), and then set the DMAST.DMST bit to 1 (enable the DMAC activation).

New activation requests are not accepted during the transfer of another DMAC channel or DTC. When the preceding transfer is complete, channel arbitration selects the DMA transfer request of the highest priority channel, and the DMA transfer of that channel starts. When the DMA transfer starts, the DMSTS.ACT flag is set to 1 (the DMAC is in the active state).

16.3.12 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers to be updated are DMSAR, DMDAR, DMCRA, DMCRB, DMSBS, DMDBS, DMCNT, and DMSTS.

DMA Source Address Register (DMSAR)

When data has been transferred in response to one transfer request, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, see Table 16.5 to Table 16.13.

DMA Destination Address Register (DMDAR)

When data has been transferred in response to one transfer request, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, see Table 16.5 to Table 16.13.

DMA Transfer Count Register (DMCRA)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 16.5 to Table 16.13.

DMA Block Transfer Count Register (DMCRB)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, see Table 16.5 to Table 16.13.

DMA Source Buffer Size Register (DMSBS)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, refer to Table 16.8 to Table 16.13.

DMA Destination Buffer Size Register (DMDBS)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, refer to Table 16.8 to Table 16.13.

Table 16.20 重复块传输模式的寄存器设置过程(2of2)

No.	步骤名称	Description
16	启用IRQ引脚作为DMACn请求源	使用外部引脚中断作为DMA激活源
17	初始设置结束	通过软件激活 初始设置完成后，将1写入DMA软件启动位(DMREQ.SWREQ)开始DMA传输。

Note: m：DELSRn.DELS位号（m=0到8）n：DMAC通道（n=0到7）
注1.DMAST.DMST位设置不一定要遵循各个激活源的设置。

16.3.11 启动DMA传输

要启用DMA传输，请将DMCNT.DTE位设置为1（启用DMA传输），然后将DMAST.DMST位设置为1（启用DMAC激活）。

在传输另一个DMAC通道或DTC期间不接受新的激活请求。当前面的传输完成后，通道仲裁选择最高优先级通道的DMA传输请求，该通道的DMA传输开始。当DMA传输开始时，DMSTS.ACT标志设置为1（DMAC处于活动状态）。

16.3.12 DMA传输期间的寄存器

DMAC寄存器由DMA传输更新。要更新的值根据其他设置和传输状态而有所不同。要更新的寄存器是DMSAR、DMDAR、DMCRA、DMRCB、DMSBS、DMDBS、DMCNT和DMSTS。

DMA源地址寄存器(DMSAR)

当响应一个传输请求而传输了数据时，DMSAR的内容将更新为下一个传输请求要访问的地址。

每种传输模式下寄存器更新操作的详细信息，请参见表16.5至表16.13。

DMA目标地址寄存器(DMDAR)

当响应一个传输请求传输了数据时，DMDAR的内容被更新为下一个传输请求要访问的地址。

每种传输模式下寄存器更新操作的详细信息，请参见表16.5至表16.13。

DMA传输计数寄存器(DMCRA)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

每种传输模式下寄存器更新操作的详细信息，请参见表16.5至表16.13。

DMA块传输计数寄存器(DMCRB)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

每种传输模式下寄存器更新操作的详细信息，请参见表16.5至表16.13。

DMA源缓冲区大小寄存器(DMSBS)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

有关各传输模式下的寄存器更新操作的详细信息，请参阅表16.8至表16.13。

DMA目标缓冲区大小寄存器(DMDBS)

当响应一个传输请求传输数据时，更新计数值。更新操作取决于选择的传输模式。

有关各传输模式下的寄存器更新操作的详细信息，请参阅表16.8至表16.13。

DMA Transfer Enable Bit (DMCNT.DTE)

Although the DMCNT.DTE bit enables or disables data transfer by the register write access, it is automatically cleared to 0 by the DMAC according to the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is completed
- When DMA transfer is stopped by the repeat size end interrupt
- When DMA transfer is stopped by the extended repeat area overflow interrupt
- When DMA transfer error occurs

Writing to the registers for the channels when the corresponding DMCNT.DTE bit is set to 1 is prohibited (except for DMCNT). In this case, writing must be performed after the bit is cleared to 0.

DMAC Active Flag (DMSTS.ACT)

The DMSTS.ACT flag indicates whether the DMACn is in the idle or active state.

This flag is set to 1 when the DMAC starts data transfer, and is cleared to 0 when data transfer in response to one transfer request is completed.

Even when DMA transfer is stopped by writing 0 to the DMCNT.DTE bit during DMA transfer, this flag remains 1 until DMA transfer is completed.

Transfer End Interrupt Flag (DMSTS.DTIF)

The DMSTS.DTIF flag is set to 1 after DMA transfer of the total transfer size of data is completed.

When both this flag and the DMINT.DTIE bit are set to 1, a transfer end interrupt is requested.

This flag is set to 1 when the DMA transfer bus cycle is completed and the DMSTS.ACT flag is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DMCNT.DTE bit is set to 1 during the interrupt handling.

Transfer Escape End Interrupt Flag (DMSTS.ESIF)

The DMSTS.ESIF flag is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt is requested. When this bit and the DMINT.ESIE bit are set to 1, a transfer escape end interrupt is requested.

This flag is set to 1 when the bus cycle of the DMA transfer having caused the interrupt request is completed and the DMSTS.ACT flag is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DMCNT.DTE bit is set to 1 during an interrupt handling.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set.

For details, see section 13, Interrupt Controller Unit (ICU).

16.3.13 Channel Priority

When multiple DMA transfer requests are present, the DMAC determines the priority of channels that have DMA transfer requests.

- The channel priority is fixed as follows: Channel 0 > Channel 1 > Channel 2 > Channel 3… > Channel 7 (Channel 0: Highest).

When a DMA transfer request is generated during data transfer, channel arbitration is started after the final data has been transferred, and DMA transfer of the higher-priority channel starts.

16.3.14 Channel Security

The security attribute of transfer access of DMACn, security attribute of access to register of DMACn, security attribute of access to the ICU.DELSRn register are controlled by ICUSARC.SADMACn bit. For details on the ICUSARC register, see section 13, Interrupt Controller Unit (ICU).

When the ICUSARC.SADMACn bit is 0, transfer of DMACn is secure access for both read and write. At the same time, the registers of channel n and the DELSRn register are protected from a non-secure access.

DMA传输使能位(DMCNT.DTE)

虽然DMCNT.DTE位通过寄存器写访问启用或禁用数据传输，但它会根据DMA传输状态由DMAC自动清零。

DMAC清除该位的条件如下：

- ●当指定的总数据传输量完成时
- ●当DMA传输因重复大小结束中断而停止时
- ●当DMA传输因扩展重复区域溢出中断而停止时
- ●发生DMA传输错误时

当相应的DMCNT.DTE位设置为1时，禁止写入通道的寄存器（除了DMCNT）。在这种情况下，必须在该位清0后进行写入。

DMAC活动标志(DMSTS.ACT)

DMSTS.ACT标志指示DMACn是处于空闲状态还是活动状态。

该标志在DMAC开始数据传输时设置为1，并在响应一个传输请求的数据传输完成时清除为0。

即使在DMA传输期间通过向DMCNT.DTE位写入0来停止DMA传输，该标志仍 保持为1，直到DMA传输完成。

传输结束中断标志(DMSTS.DTIF)

在数据的总传输大小的DMA传输完成后，DMSTS.DTIF标志设置为1。

当该标志和DMINT.DTIE位都设置为1时，请求传输结束中断。

当DMA传输总线周期完成并且DMSTS.ACT标志被清除为0时，该标志设置为1，表示DMA传输结束。

在中断处理期间，当DMCNT.DTE位设置为1时，该标志自动清零。

传输转义结束中断标志(DMSTS.ESIF)

当请求重复大小结束中断或扩展重复区域溢出中断时，DMSTS.ESIF标志设置为1。
当该位和DMINT.ESIE位设置为1时，请求传输转义结束中断。

当导致中断请求的DMA传输的总线周期完成并且DMSTS.ACT标志清零，表示DMA传输结束。

在中断处理期间，当DMCNT.DTE位设置为1时，该标志自动清零。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。

有关详细信息，请参阅第13节，中断控制器单元(ICU)。

16.3.13 频道优先级

当存在多个DMA传输请求时，DMAC确定具有DMA传输请求的通道的优先级。

●通道优先级固定如下：通道0>通道1>通道2>通道3…>通道7（通道0：最高）。

如果在数据传输过程中产生DMA传输请求，则在传输完最终数据后启动通道仲裁，并开始高优先级通道的DMA传输。

16.3.14 渠道安全

DMACn的传输访问的安全属性、DMACn的寄存器访问的安全属性、ICU.DELSRn寄存器的访问的安全属性由ICUSARC.SADMACn位控制。有关ICUSARC寄存器的详细信息，请参见第13节，中断控制器单元(ICU)。

当ICUSARC.SADMACn位为0时，DMACn的传输对于读和写都是安全访问。同时，通道n的寄存器和DELSRn寄存器受到保护，不会被非安全访问。

When the ICUSARC.SADMACn bit is 1, transfer of DMACn is non-secure access for both read and write. At the same time, the registers of channel n and the DELSRn register are non-secure attributes.

Do not write to the ICUSARC.SADMACn bit while DMA transfer of same channel is enabled or a bus master is writing to the DMA registers of same channel.

Figure 16.23 shows security attribute about each DMAC channels.

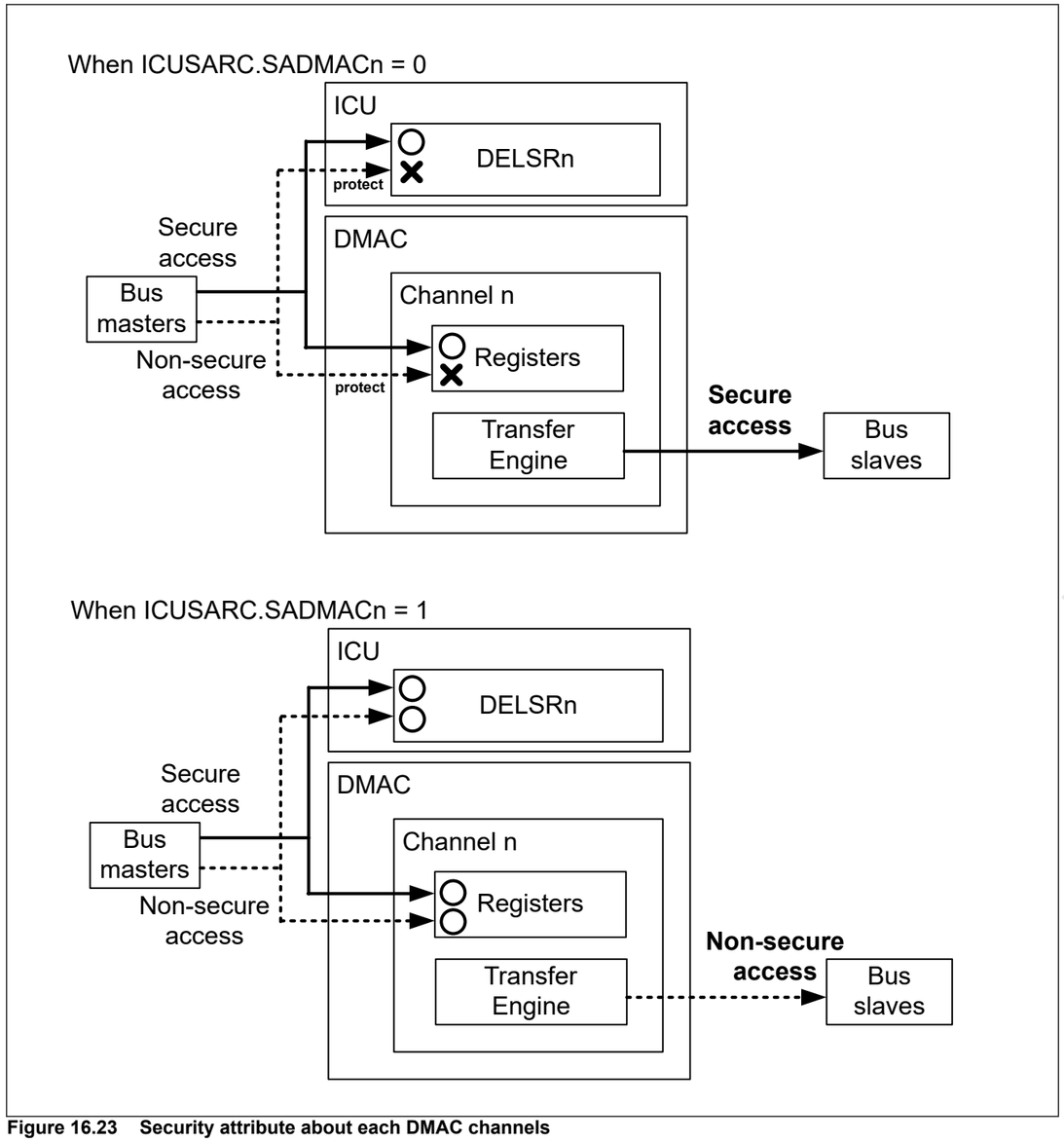


Figure 16.23 Security attribute about each DMAC channels

16.3.15 Master TrustZone Filter in DMAC

DMAC has the Master TrustZone Filter. The MasterTrustZone Filter in DMAC can detect the security areas of Flash area(code Flash and data Flash) and SRAM area(ECC / Parity RAM) defined by IDAU. When set No-secure channel

当ICUSARC.SADMACn位为1时，DMACn的传输对于读和写都是非安全访问。同时，通道n的寄存器和DELSRn寄存器是非安全属性。

当启用同一通道的DMA传输或总线主机正在写入同一通道的DMA寄存器时，请勿写入ICUSARC.SADMACn位。

图16.23显示了每个DMAC通道的安全属性。

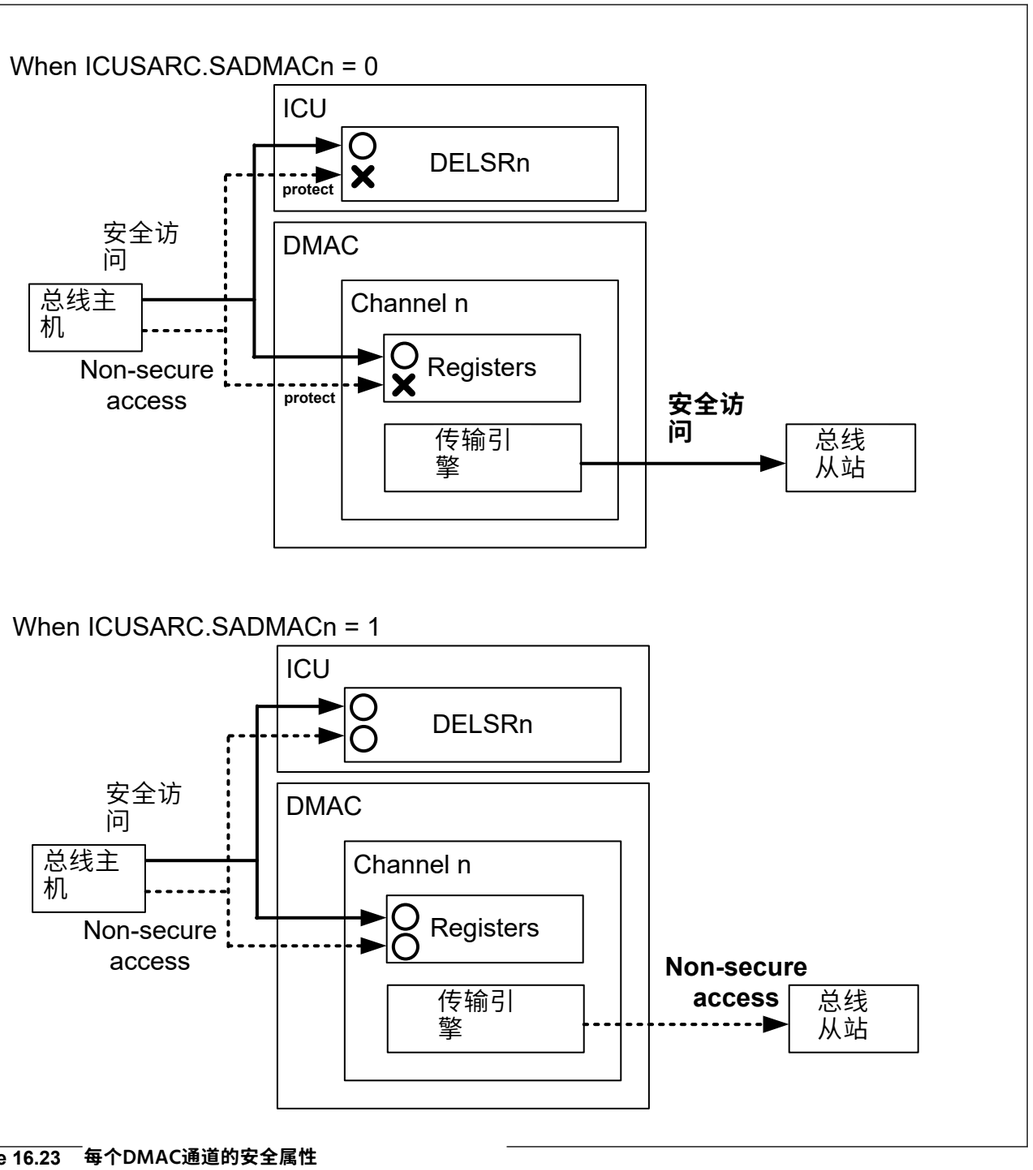


Figure 16.23 每个DMAC通道的安全属性

16.3.15 DMAC中的主TrustZone过滤器

DMAC具有MasterTrustZone过滤器。DMAC中的MasterTrustZoneFilter可以检测IDAU定义的Flash区域（代码Flash和数据Flash）和SRAM区域（ECCParityRAM）的安全区域。设置无安全通道时

accesses those addresses, it detects the security violation. Access of violation address is not performed. Detected the error is handled as the Master TrustZone Filter error.

16.4 Ending DMA Transfer

The operation for ending DMA transfer depends on the transfer end conditions. When DMA transfer ends, the DMCNT.DTE bit and the DMSTS.ACT flag are changed from 1 to 0, indicating that DMA transfer has ended.

16.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In Normal Transfer Mode (DMTMD.MD[1:0] = 00b)

When the value of DMCRAL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bitT is 1 at this time, a transfer end interrupt request is issued to the CPU or the DTC.

(2) In Repeat Transfer Mode (DMTMD.MD[1:0] = 01b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

If the DMTMD.TKP bit is 1 (in free-running function), the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

(3) In Block Transfer Mode (DMTMD.MD[1:0] = 10b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set.

For details, see section 13, Interrupt Controller Unit (ICU).

If the DMTMD.TKP bit is 1 (in free-running function),the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

(4) In Repeat-Block Transfer Mode (DMTMD.MD[1:0] = 11b)

When the value of DMCRBL changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DMCNT.DTE bit is cleared to 0 and the DMSTS.DTIF flag is set to 1 at the same time. If the DMINT.DTIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 13, Interrupt Controller Unit (ICU).

If the DMTMD.TKP bit is 1 (in free-running function),the DMSTS.DTIF bit is set to 1, but the DMCNT.DTE bit is not cleared to 0.

16.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, a repeat size end interrupt is requested when transfer of a 1-repeat size of data is completed while the DMINT.RPTIE bit is set to 1. When the interrupt is requested to complete DMA transfer, the DMCNT.DTE bit is cleared to 0 and the DMSTS.ESIF flag is set to 1 even if the DMTMD.TKP bit is 1 (in free-running function). If the DMINT.ESIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC. Here, the transfer can be resumed by writing 1 to the DMCNT.DTE bit.

A repeat size end interrupt can be requested also in block transfer mode. In block transfer mode, the interrupt is requested in the same way as in repeat transfer mode when transfer of a 1-block size data is completed.

Repeat size end interrupt cannot be requested in repeat-block transfer mode.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 13, Interrupt Controller Unit (ICU).

访问这些地址时，它会检测到安全违规。不执行违规地址的访问。检测到的错误作为MasterTrustZoneFilter错误处理。

16.4 结束DMA传输

结束DMA传输的操作取决于传输结束条件。当DMA传输结束时，DMCNT.DTE位和DMSTS.ACT标志由1变为0，表示DMA传输已经结束。

16.4.1 完成指定的转移操作总数后转移结束

(1) 在正常传输模式下（DMTMD.MD[1:0]=00b）

当DMCRAL的值由1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIEbitT为1，则向CPU或DTC发出传输结束中断请求。

(2) 在重复传输模式下(DMTMD.MD[1:0]=01b)

当DMCRBL的值从1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIE位为1，则向CPU或DTC发出中断请求。

如果DMTMD.TKP位为1（在自由运行功能中），则DMSTS.DTIF位设置为1，但DMCNT.DTE位不清除为0。

(3) 在块传输模式下(DMTMD.MD[1:0]=10b)

当DMCRBL的值从1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIE位为1，则向CPU或DTC发出中断请求。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。

有关详细信息，请参阅第13节，中断控制器单元(ICU)。

如果DMTMD.TKP位为1（在自由运行功能中），则DMSTS.DTIF位设置为1，但DMCNT.DTE位不清除为0。

(4) 在重复块传输模式下(DMTMD.MD[1:0]=11b)

当DMCRBL的值从1变为0时，相应通道上的DMA传输结束，同时DMCNT.DTE位清0，同时DMSTS.DTIF标志置1。如果此时DMINT.DTIE位为1，则向CPU或DTC发出中断请求。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

如果DMTMD.TKP位为1（在自由运行功能中），则DMSTS.DTIF位设置为1，但DMCNT.DTE位不清除为0。

16.4.2 按重复大小结束传输结束中断

在重复传输模式下，当DMINT.RPTIE位设置为1时完成1次重复大小的数据传输时，请求重复大小结束中断。当请求中断以完成DMA传输时，DMCNT.DTE位即使DMTMD.TKP位为1（在自由运行功能中），清除为0并且DMSTS.ESIF标志设置为1。如果此时DMINT.ESIE位为1，则向CPU或DTC发出中断请求。在这里，可以通过将1写入DMCNT.DTE位来恢复传输。

在块传输模式下也可以请求重复大小结束中断。在块传输模式中，当1块大小的数据传输完成时，以与重复传输模式相同的方式请求中断。

在重复块传输模式下不能请求重复大小结束中断。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

16.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the DMINT.SARIE or DMINT.DARIE bit is set to 1 even if the DMTMD.TKP bit is 1 (in free-running function), an interrupt by an extended repeat area overflow is requested. When the interrupt is requested, the DMA transfer is terminated, the DMCNT.DTE bit is cleared to 0, and the ESIF flag in DMSTS is set to 1. If the DMINT.ESIE bit is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Even if an interrupt by an extended repeat area overflow is requested during a read cycle, the following write cycle is performed.

In block transfer mode, even if an interrupt by an extended repeat area overflow is requested during a 1-block transfer, the remaining data in the block is transferred; transfer is terminated after a block transfer.

An interrupt by an extended repeat area overflow cannot be requested in repeat-block transfer mode.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 13, Interrupt Controller Unit (ICU).

16.5 Processing on DMA Transfer Error

DMA transfer error occurs with the Master TrustZone Filter error in DMAC, the Slave TrustZone Filter error, the Master MPU error, the Slave Bus Error or the Illegal Access Error. If the access error occurs during the DMA transfer, the DMAC immediately stops the transfer of error occurred channel. At this time, the ICU setting of the corresponding channel is also cleared. If there is a request other than the channel which caused the error, it will be re-arbitration as it is.

When the transfer error occurs, DMCNT.DTE of the error causing channel is set to 0. Also, the error response is informed to the ICU.DELSRn of the corresponding channel is cleared. Write back to each register is not performed. Furthermore, it generates the error response detection interrupt request (DMA_TRANSERR) to notify that an error has occurred by DMAC/DTC transfer.

When the Master TrustZone Filter error occurs, the Slave TrustZone error occurs or the Master MPU error occurs, it is possible to confirm the error information of DMAC by selecting NMI. The DMAC error channel register is cleared by selecting reset. Under the conditions where NMI is generated due to transfer error in DMAC, two interrupts(NMI and DMAC_TRANSERR) are generated. In this case, NMI always responds first.

The error response detection interrupt request (DMA_TRANSERR) occurs when the Slave Bus error or the Illegal Access error occurs. Furthermore, it occurs after NMI when the error response detection interrupt request (DMA_TRANSERR) is not cleared in NMI handler.

section 16.5.1. Processing on NMI handler describes how to confirm the error information of the DMAC in the NMI handler.

section 16.5.2. Processing on Error response detection interrupt request (DMA_TRANSERR) handler describes how to confirm the error information of the DMAC in the DMA_TRANSERR handler.

Interrupts and the error information generated due to transfer errors are shown in section 16.6.2. Transfer Error Interrupt.

16.5.1 Processing on NMI handler

The cause of NMI due to the DMA transfer error is the Master TrustZone Filter error, the Slave TrustZone Filter error or the Master MPU error. When NMI occurs due to the DMAC transfer error, the error response detection interrupt request (DMA_TRANSERR) will occur after the end of NMI handler. It is possible to confirm the cause of the error and the DMAC channel in which the error occurred. When NMI occurs, perform the necessary processing according to the flow described in the ICU chapter.

Figure 16.24 shows the flow for confirm the channel that caused the Master TrustZone Filter Error in DMAC

Figure 16.25 shows the flow for confirm the channel that caused the Slave TrustZone Filter Error in DMAC

Figure 16.26 shows the flow for confirm the channel and Security Attribute that caused the Master MPU error in DMAC.

If completing all processing in NMI handler, it is possible to clear the error response detection interrupt request (DMA_TRANSERR) that occurs subsequently.

16.4.3 扩展重复区溢出中断传输结束

如果在指定扩展重复区域时扩展重复区域发生溢出，并且即使DMTMD.TKP位为1，DMINT.SARIE或DMINT.DARIE位也设置为1（在自由运行功能中），中断由请求扩展重复区域溢出。请求中断时，终止DMA传输，DMCNT.DTE位清0，DMSTS中的ESIF标志置1。如果此时DMINT.ESIE位为1，则发出中断请求到CPU或DTC。

即使在读取周期期间请求由扩展重复区域溢出引起的中断，也会执行下一个写入周期。

在块传输模式下，即使在1块传输期间请求扩展重复区域溢出中断，也会传输块中剩余的数据；块传输后终止传输。

在重复块传输模式下不能请求由扩展重复区域溢出引起的中断。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

16.5 DMA传输错误处理

DMA传输错误发生在DMAC中的MasterTrustZoneFilter错误、SlaveTrustZoneFilter错误、Master MPU错误、从总线错误或非法访问错误。如果在DMA传输过程中发生访问错误，DMAC立即停止发生错误通道的传输。此时相应通道的ICU设置也被清除。如果存在引起错误的通道以外的请求，将按原样重新仲裁。

当发生传输错误时，错误引起通道的DMCNT.DTE设置为0。同时，错误响应被通知给ICU。相应通道的DELSRn被清除。不执行回写到每个寄存器。此外，它会生成错误响应检测中断请求(DMA_TRANSERR)，以通知DMACDTC传输发生错误。

当MasterTrustZoneFilter发生错误、SlaveTrustZone错误或MasterMPU错误时，可以通过选择NMI来确认DMAC的错误信息。通过选择复位来清除DMAC错误通道寄存器。在由于DMAC中的传输错误而产生NMI的情况下，会产生两个中断（NMI和DMAC_TRANSERR）。在这种情况下，NMI总是首先响应。

当发生SlaveBus错误或IllegalAccess错误时，会发生错误响应检测中断请求(DMA_TRANSERR)。此外，当NMI处理程序中未清除错误响应检测中断请求(DMA_TRANSERR)时，它会在NMI之后发生。

第16.5.1节。NMIhandler上的处理描述了如何在NMIhandler中确认DMAC的错误信息。

第16.5.2节。错误响应检测中断请求（DMA_TRANSERR）处理程序的处理描述了如何在DMA_TRANSERR处理程序中确认DMAC的错误信息。

因传输错误而产生的中断和错误信息见16.6.2节。传输错误中断。

16.5.1 在NMI处理程序上处理

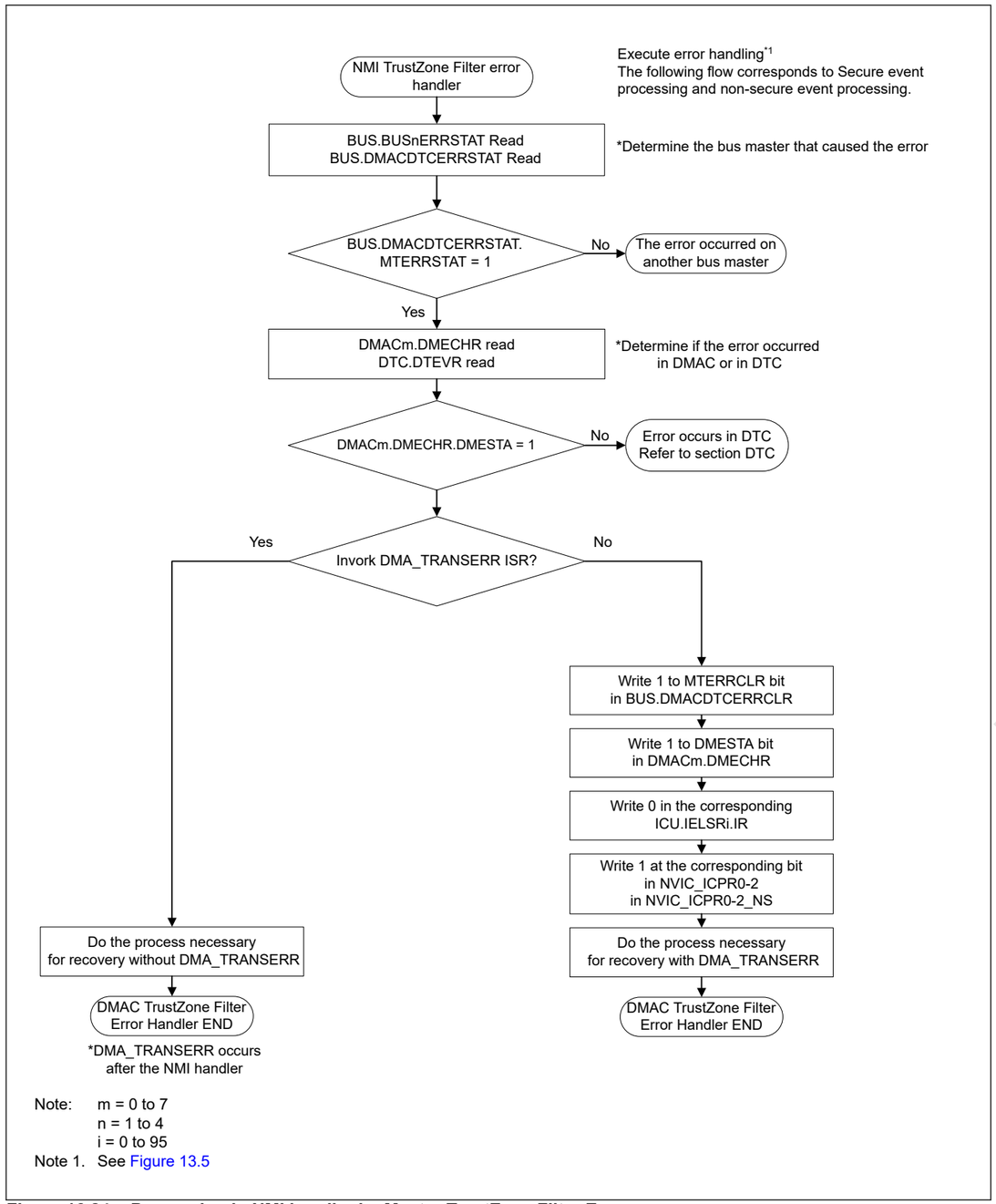
由于DMA传输错误导致NMI的原因是MasterTrustZoneFilter错误、SlaveTrustZoneFilter错误或MasterMPU错误。当由于DMAC传输错误而发生NMI时，错误响应检测中断请求(DMA_TRANSERR)将在NMI处理程序结束后发生。可以确认错误的原因和发生错误的DMAC通道。当发生NMI时，按照ICU章节中描述的流程进行必要的处理。

图16.24显示了在DMAC中确认导致MasterTrustZoneFilterError的通道的流程

图16.25显示了在DMAC中确认导致SlaveTrustZoneFilterError的通道的流程

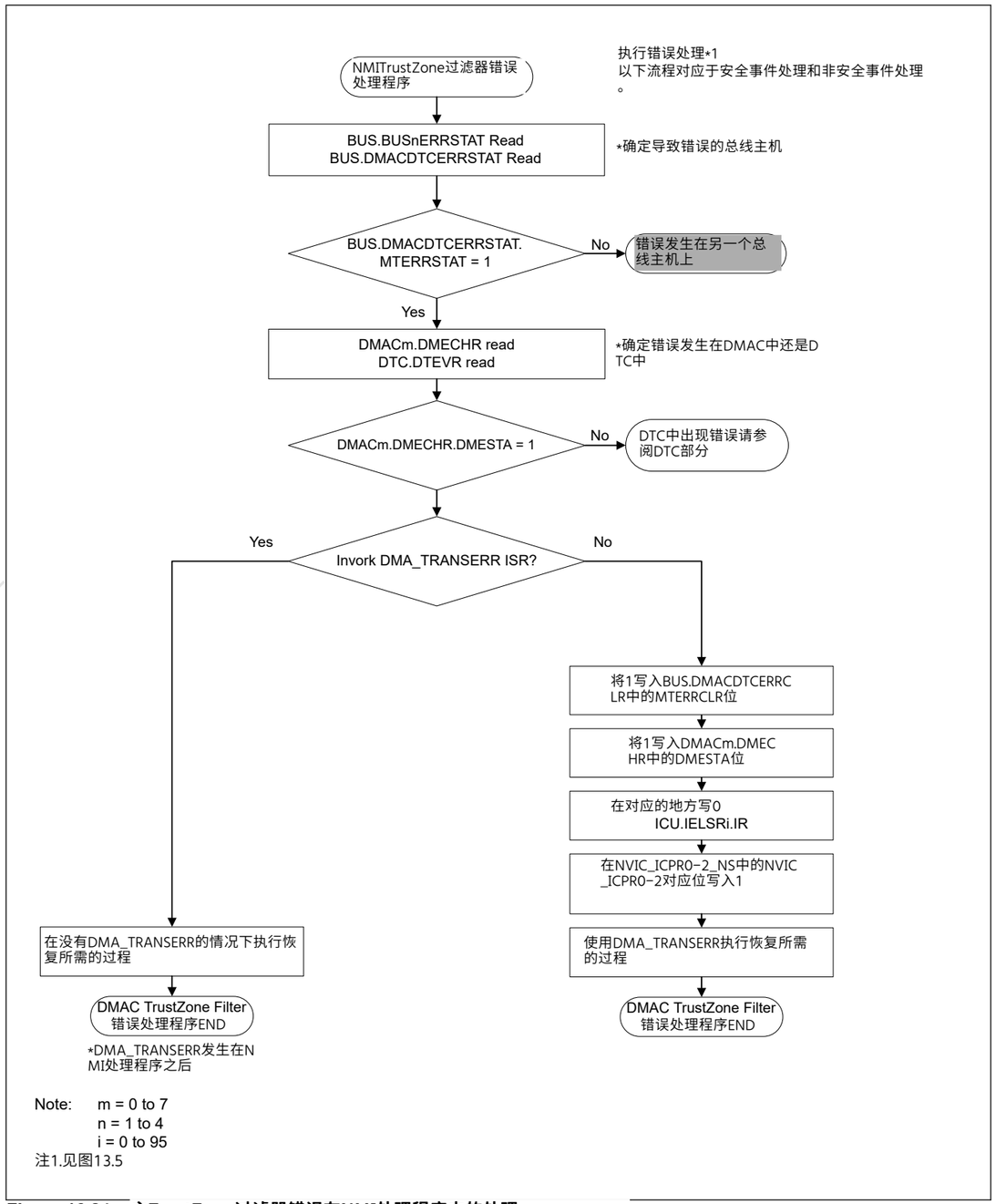
图16.26显示了在DMAC中确认导致MasterMPU错误的通道和安全属性的流程。

如果完成NMI处理程序中的所有处理，则可以清除随后发生的错误响应检测中断请求(DMA_TRANSERR)。



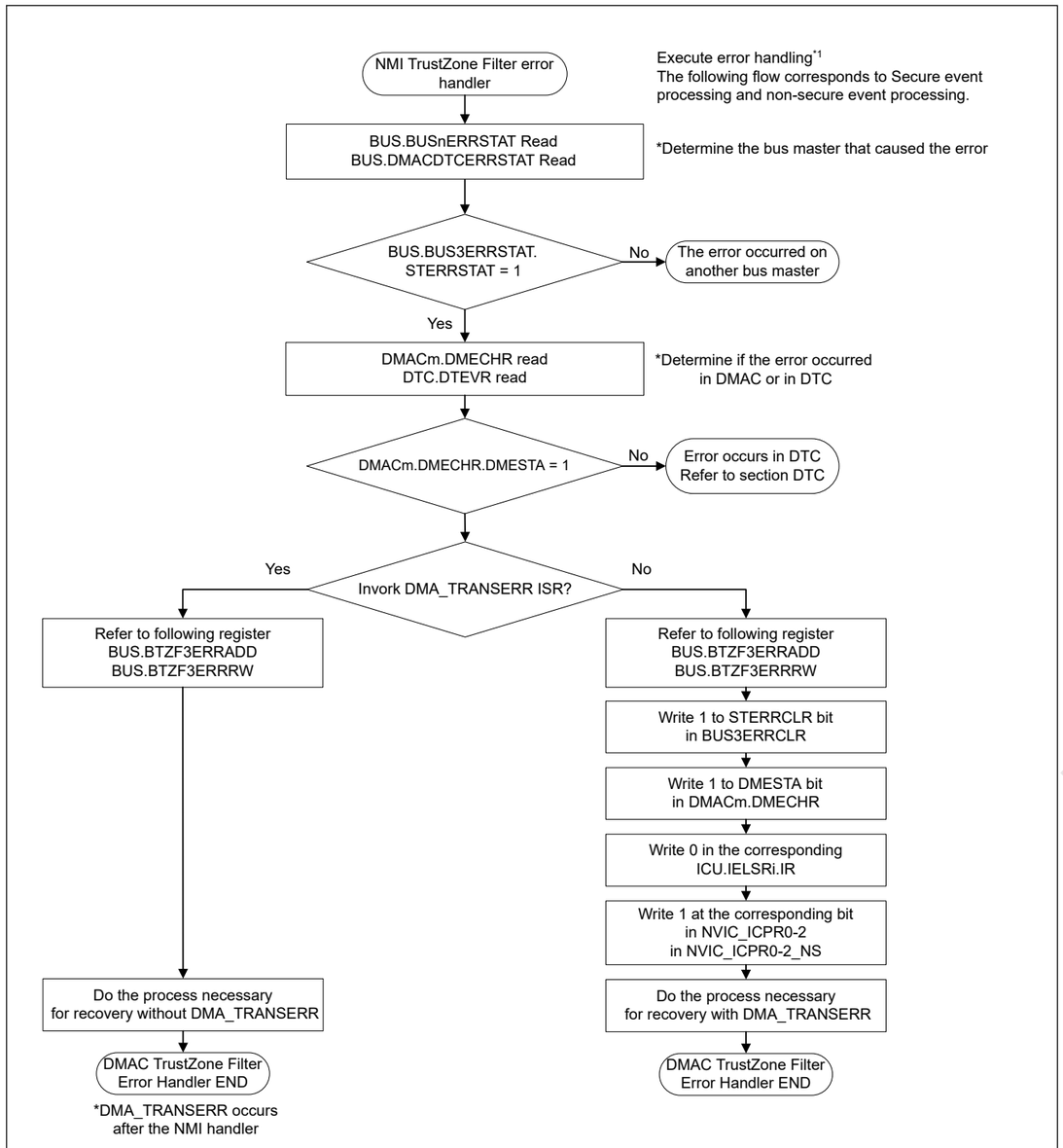
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
Note 1. See Figure 13.5

Figure 16.24 Processing in NMI handler by Master TrustZone Filter Error



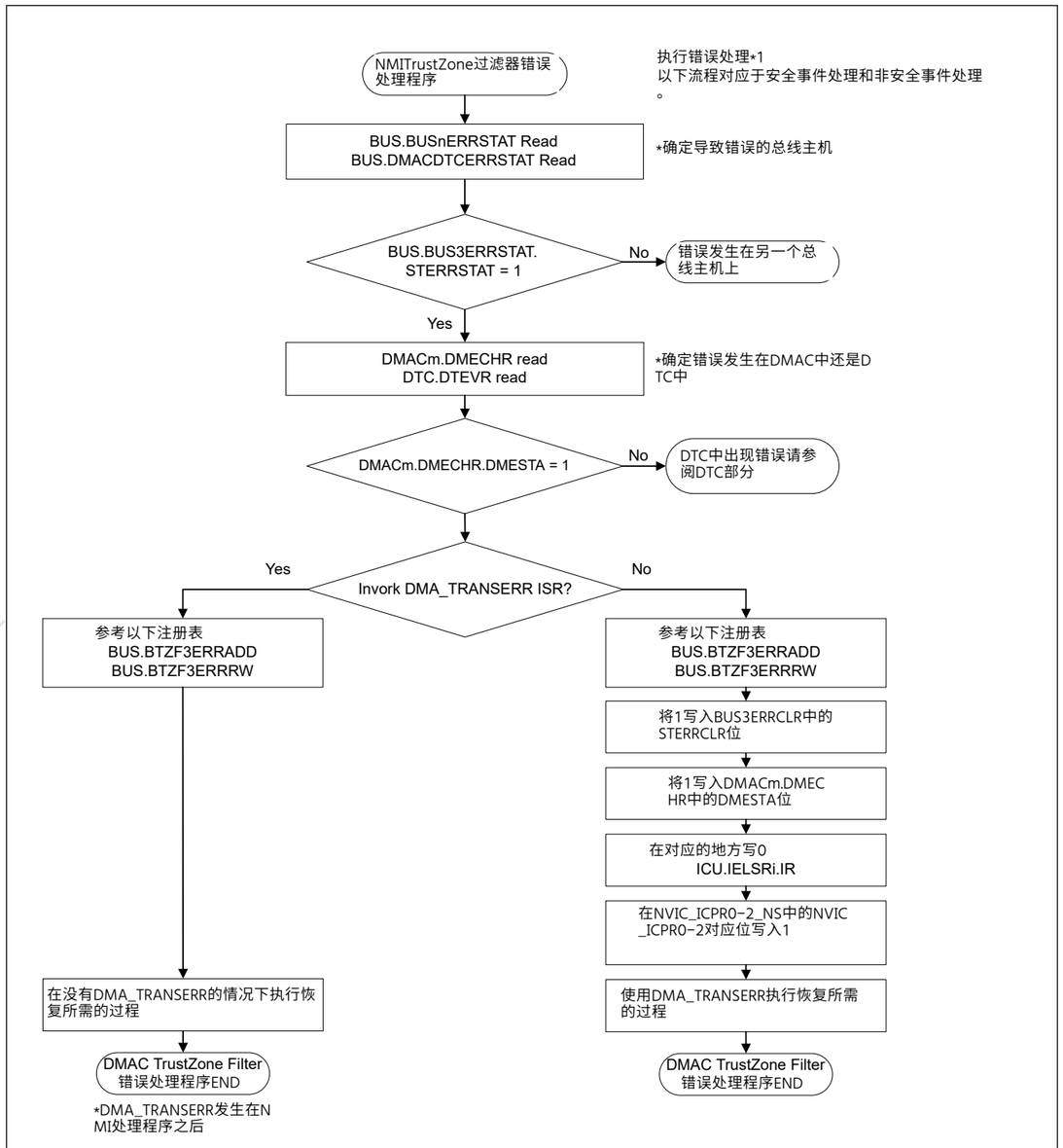
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
注1.见图13.5

Figure 16.24 主TrustZone过滤器错误在NMI处理程序中的处理



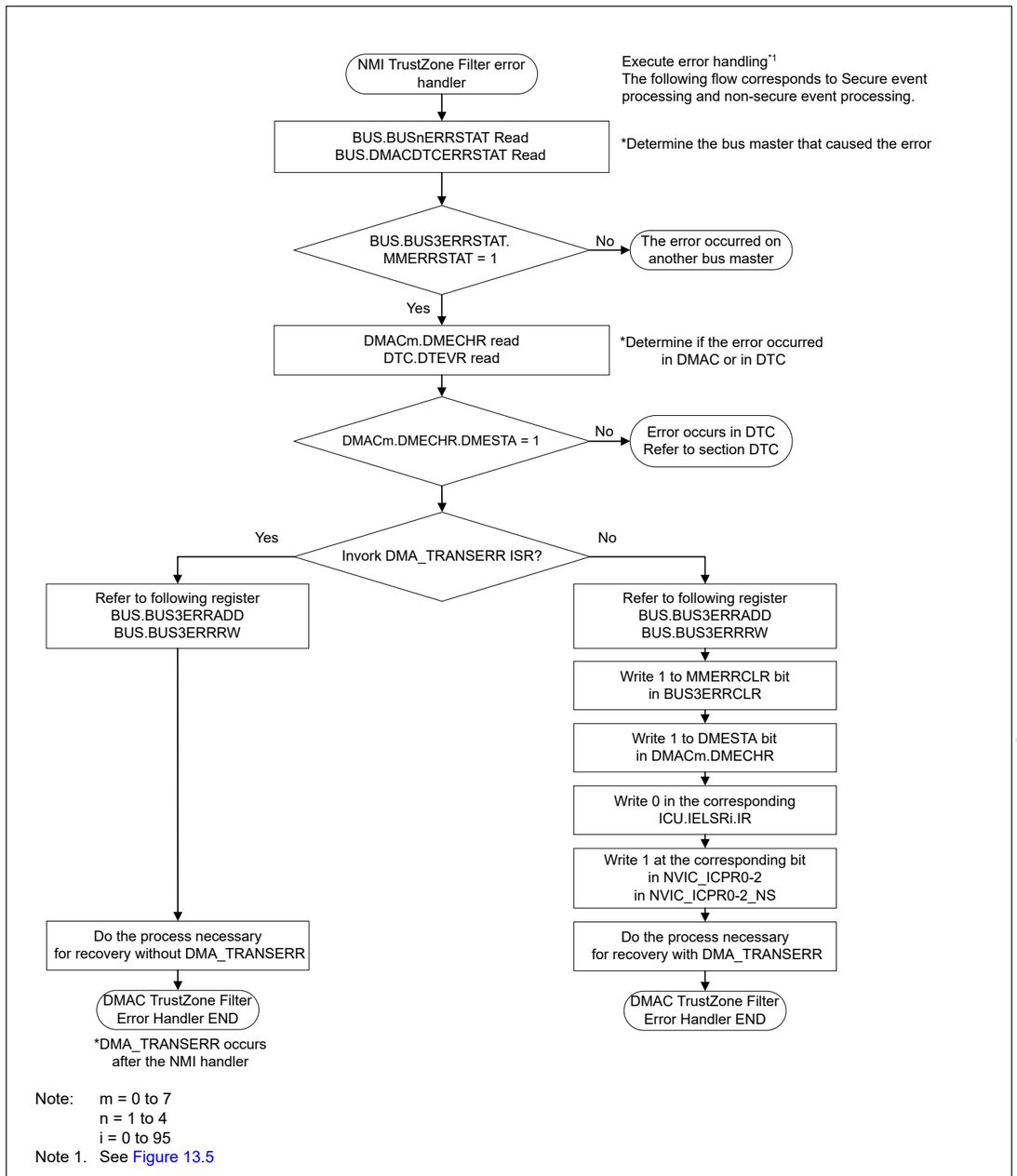
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
Note 1. See Figure 13.5

Figure 16.25 Processing in NMI handler by Slave TrustZone Filter Error



Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
注1.见图13.5

Figure 16.25 从属TrustZone过滤器错误在NMI处理程序中的处理

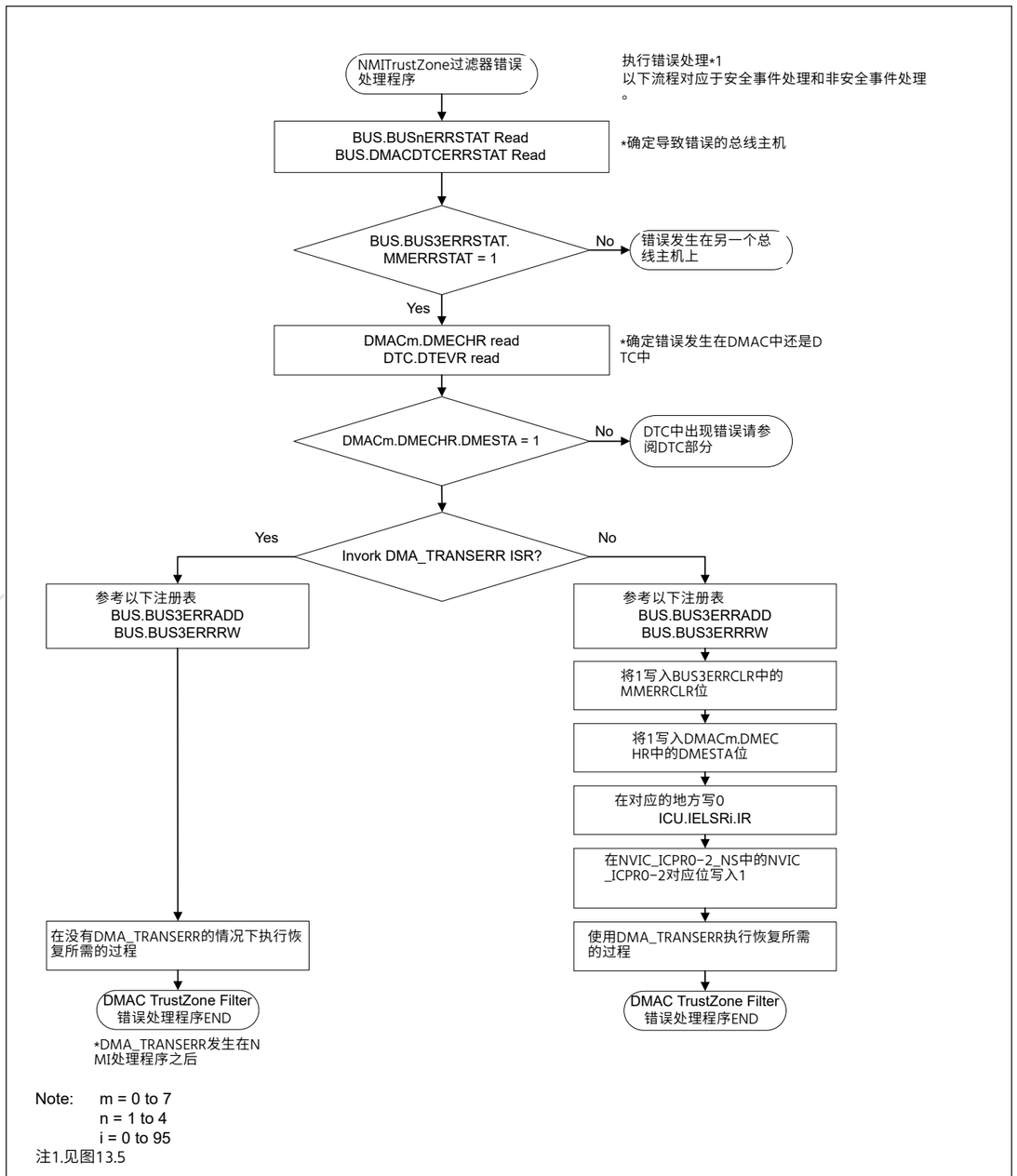


Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
Note 1. See Figure 13.5

Figure 16.26 Processing in NMI handler by Master MPU Error

16.5.2 Processing on Error response detection interrupt request (DMA_TRANSERR) handler

The cause of error response detection interrupt request (DMA_TRANSERR) due to DMA transfer error is the Slave Bus Error or Illegal Access Error. Also, it occurs after the NMI handler error response detection interrupt request (DMA_TRANSERR) is not cleared by the NMI handler.



Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
注1.见图13.5

Figure 16.26 主MPU错误在NMI处理程序中的处理

16.5.2 错误响应检测中断请求(DMA_TRANSERR)处理程序的处理

由于DMA传输错误导致错误响应检测中断请求(DMA_TRANSERR)的原因是从总线错误或非法访问错误。此外，它发生在NMI处理程序错误响应检测中断请求(DMA_TRANSERR)未被NMI处理程序清除之后。

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It is possible to confirm the cause of the error and the DMAC channel in which the error occurred.

Error cause confirmation procedure is shown Figure 16.27.

Figure 16.28 shows the flow for confirm the channel that caused the Master TrustZone Filter Error in DMAC

Figure 16.29 shows the flow for confirm the channel that caused the Slave TrustZone Filter Error in DMAC

Figure 16.30 shows the flow for confirm the channel and Security Attribute that caused the Master MPU Error in DMAC

Figure 16.31 shows the flow for confirm the channel and Security Attribute that caused the Slave Bus Error in DMAC

Figure 16.32 shows the flow for confirm the channel and Security Attribute that caused the Illegal Access Error in DMAC

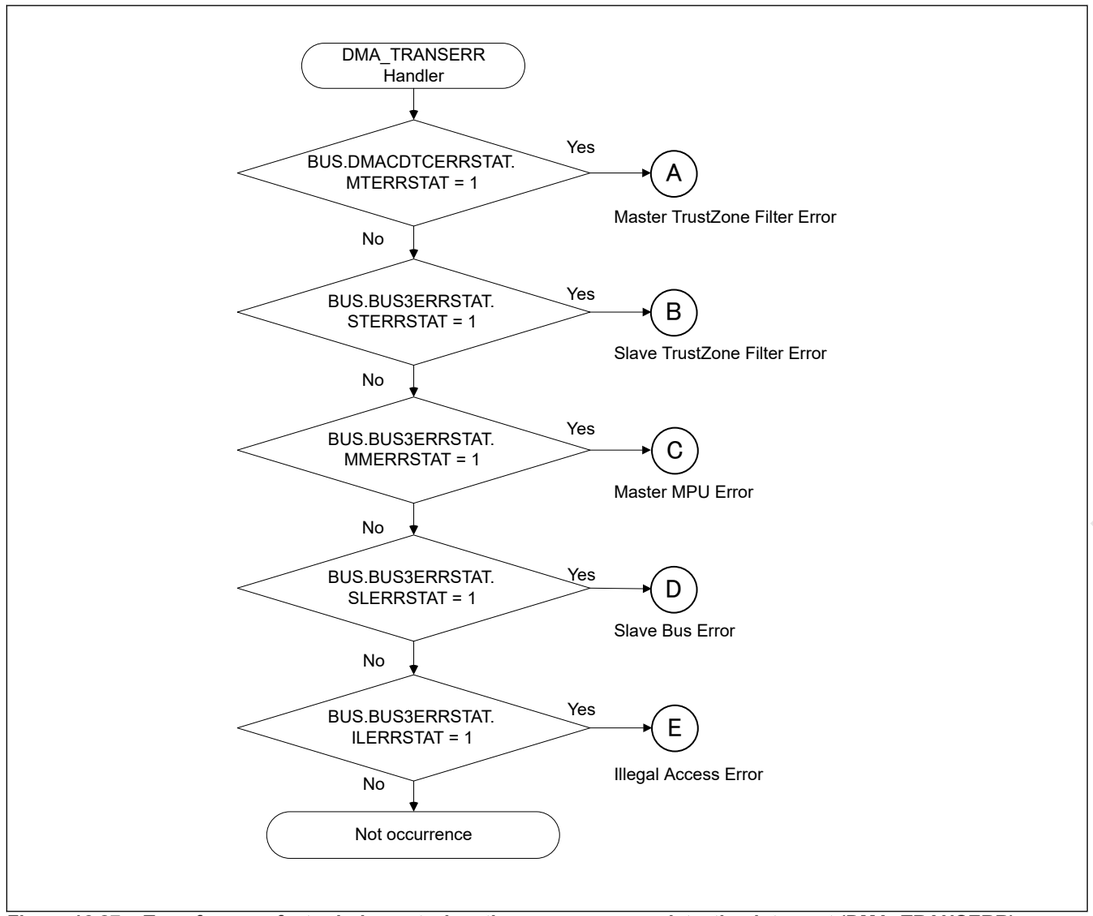


Figure 16.27 Transfer error factor judgment when the error response detection interrupt (DMA_TRANSERR) occurs

可以确认错误的原因和发生错误的DMAC通道。

错误原因确认流程如图16.27所示。

图16.28显示了在DMAC中确认导致MasterTrustZoneFilterError的通道的流程

图16.29显示了在DMAC中确认导致SlaveTrustZoneFilterError的通道的流程

图16.30显示了在DMAC中确认导致MasterMPU错误的通道和安全属性的流程

图16.31显示了在DMAC中确认导致SlaveBusError的通道和安全属性的流程

图16.32显示了确认导致DMAC中非法访问错误的通道和安全属性的流程

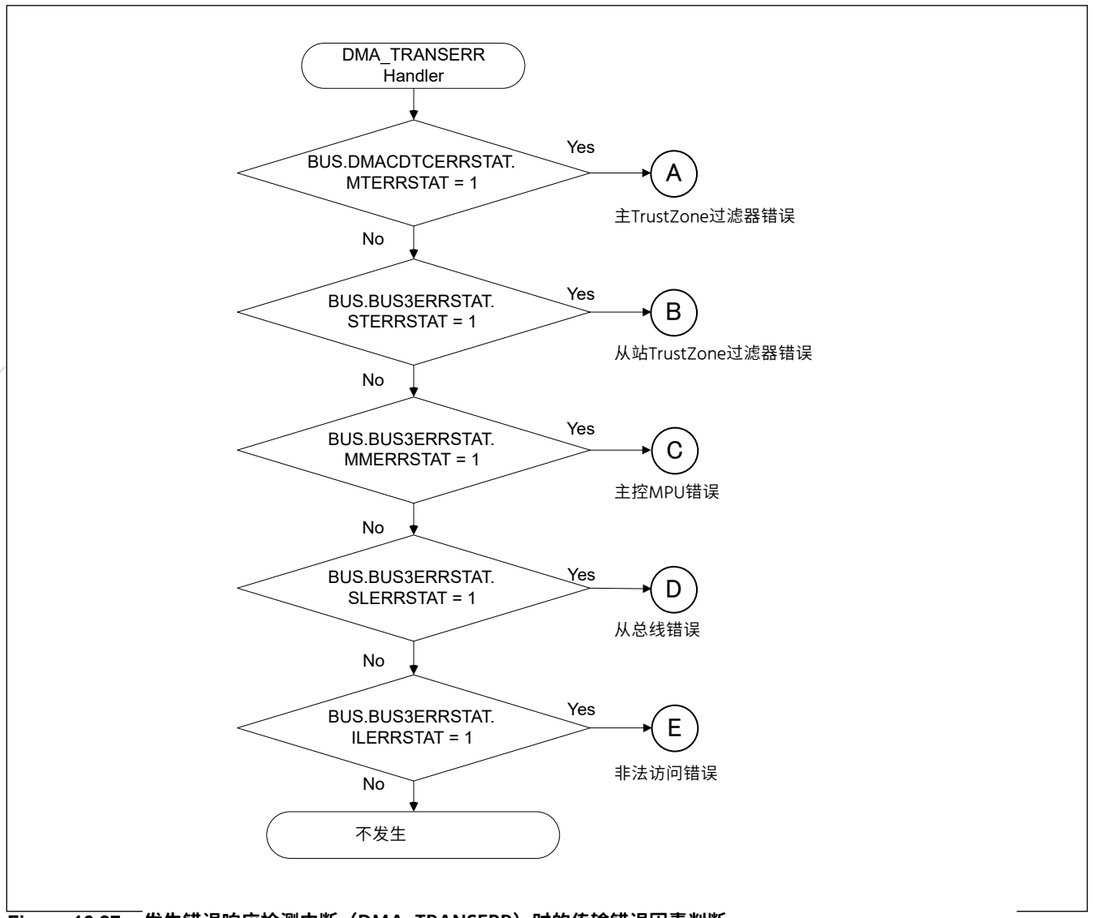


Figure 16.27 发生错误响应检测中断（DMA_TRANSERR）时的传输错误因素判断

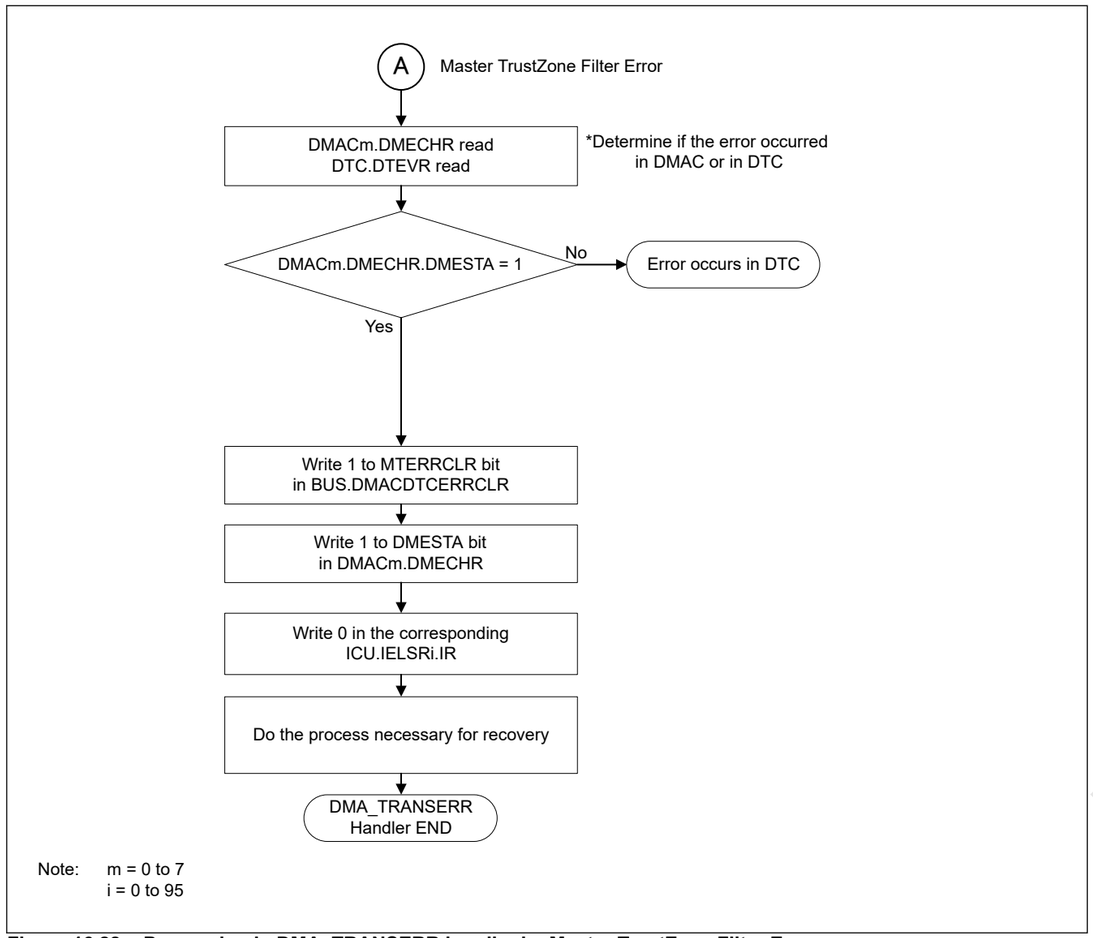


Figure 16.28 Processing in DMA_TRANSERR handler by Master TrustZone Filter Error

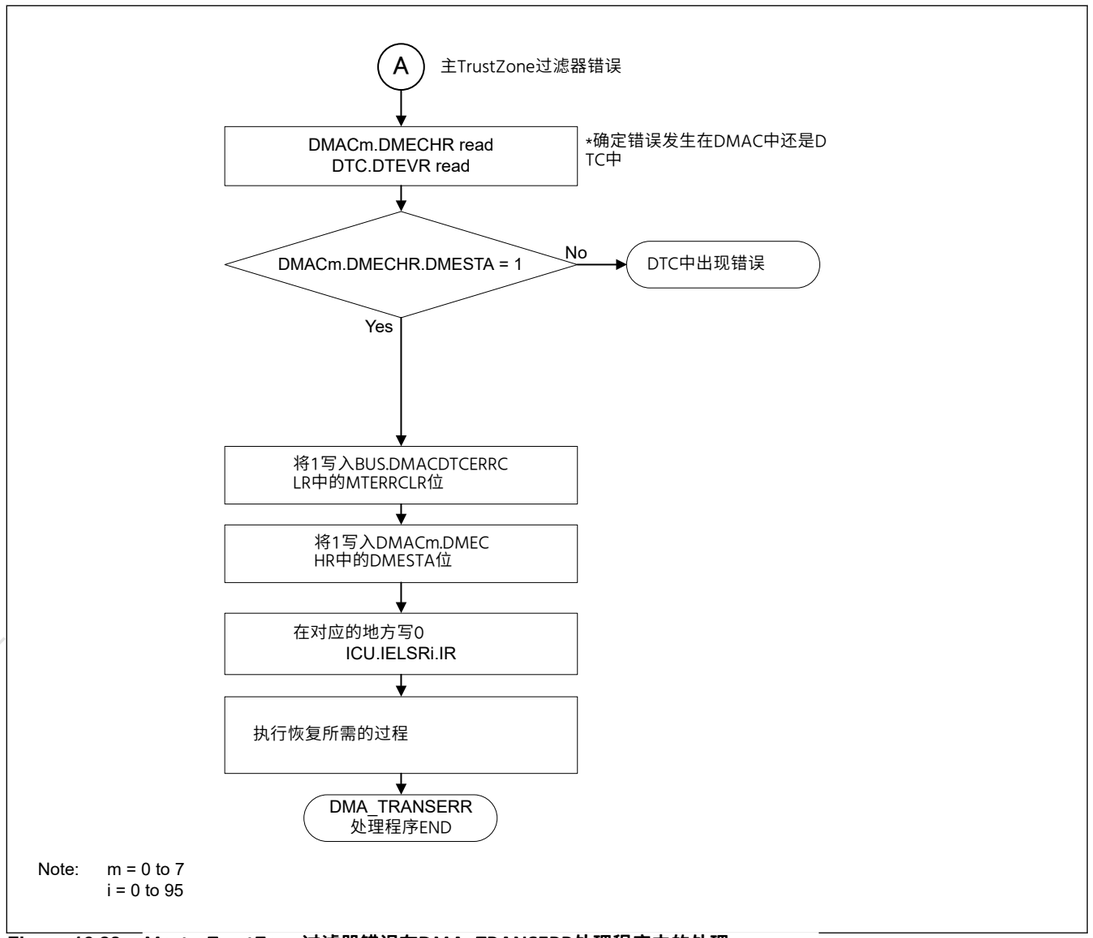


Figure 16.28 MasterTrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

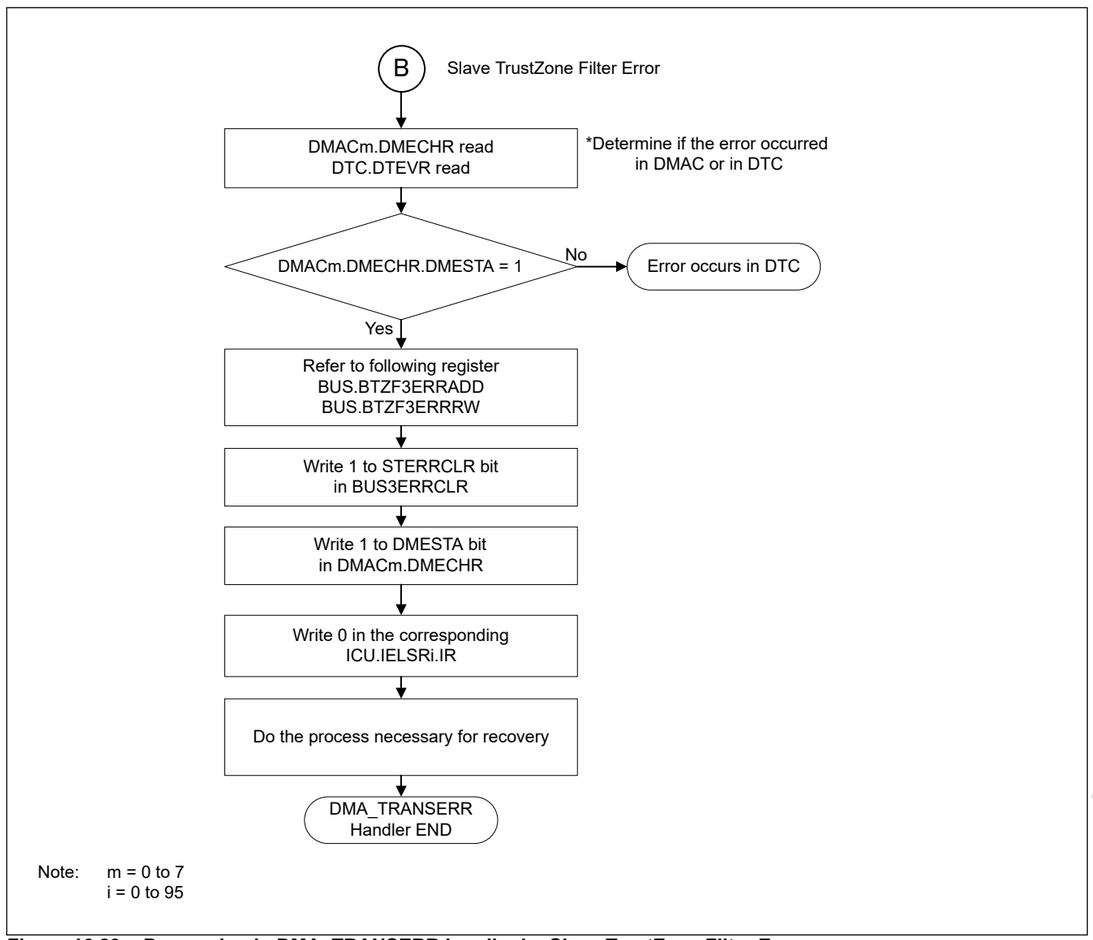


Figure 16.29 Processing in DMA_TRANSERR handler by Slave TrustZone Filter Error

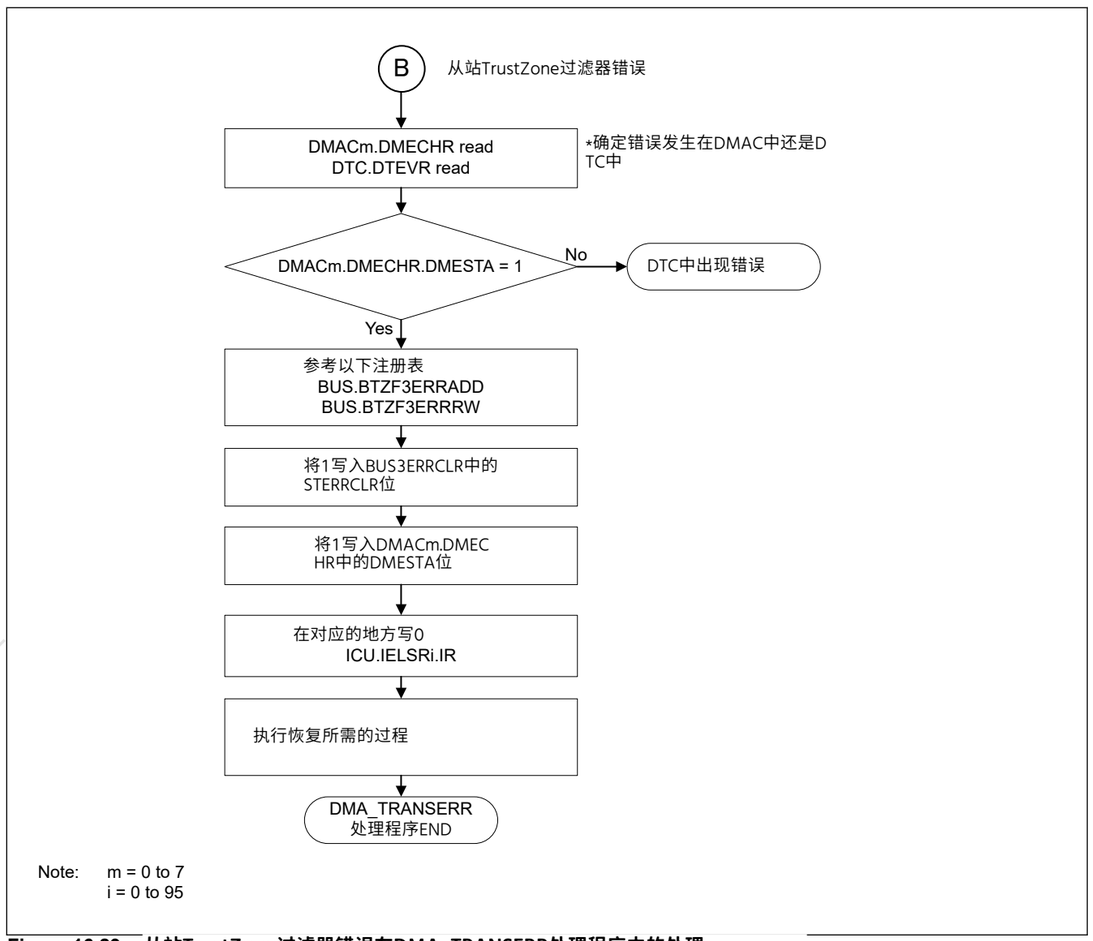


Figure 16.29 从站TrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

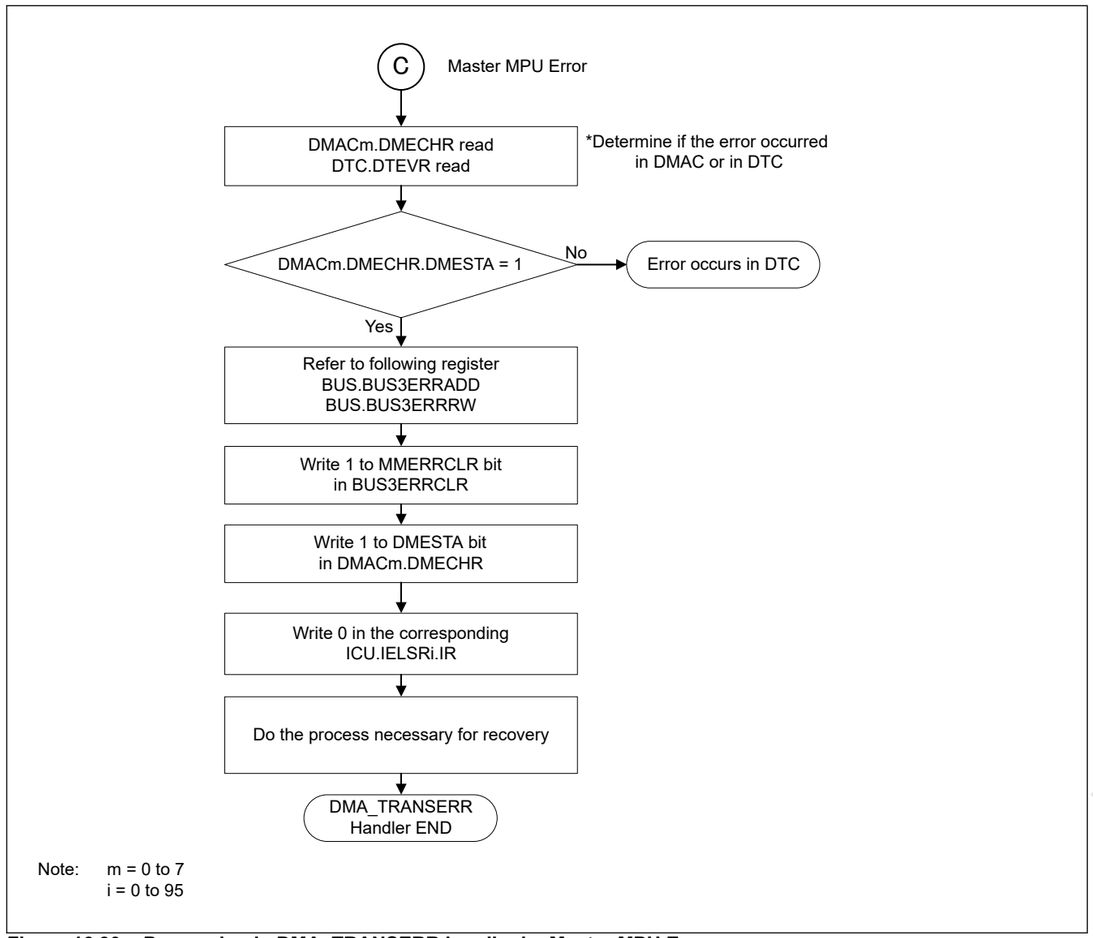


Figure 16.30 Processing in DMA_TRANSERR handler by Master MPU Error

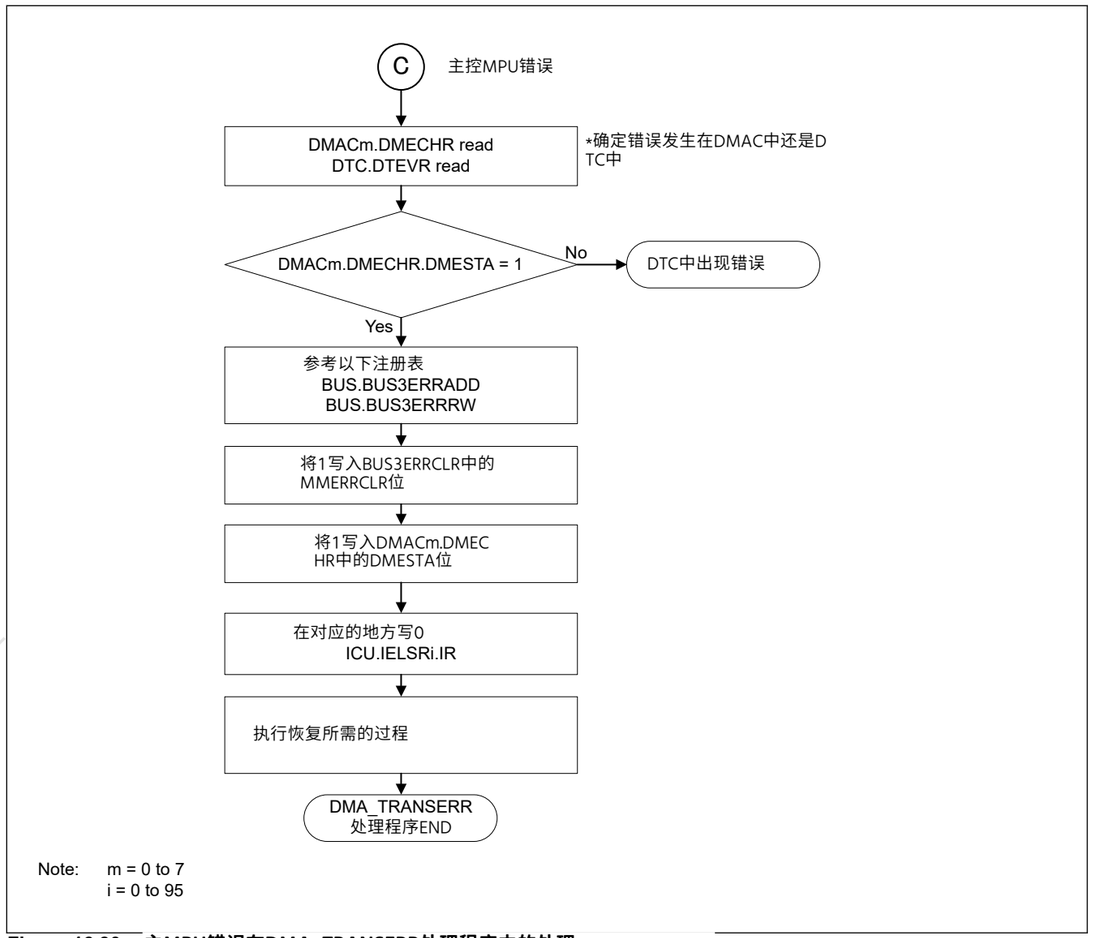


Figure 16.30 主MPU错误在DMA_TRANSERR处理程序中的处理

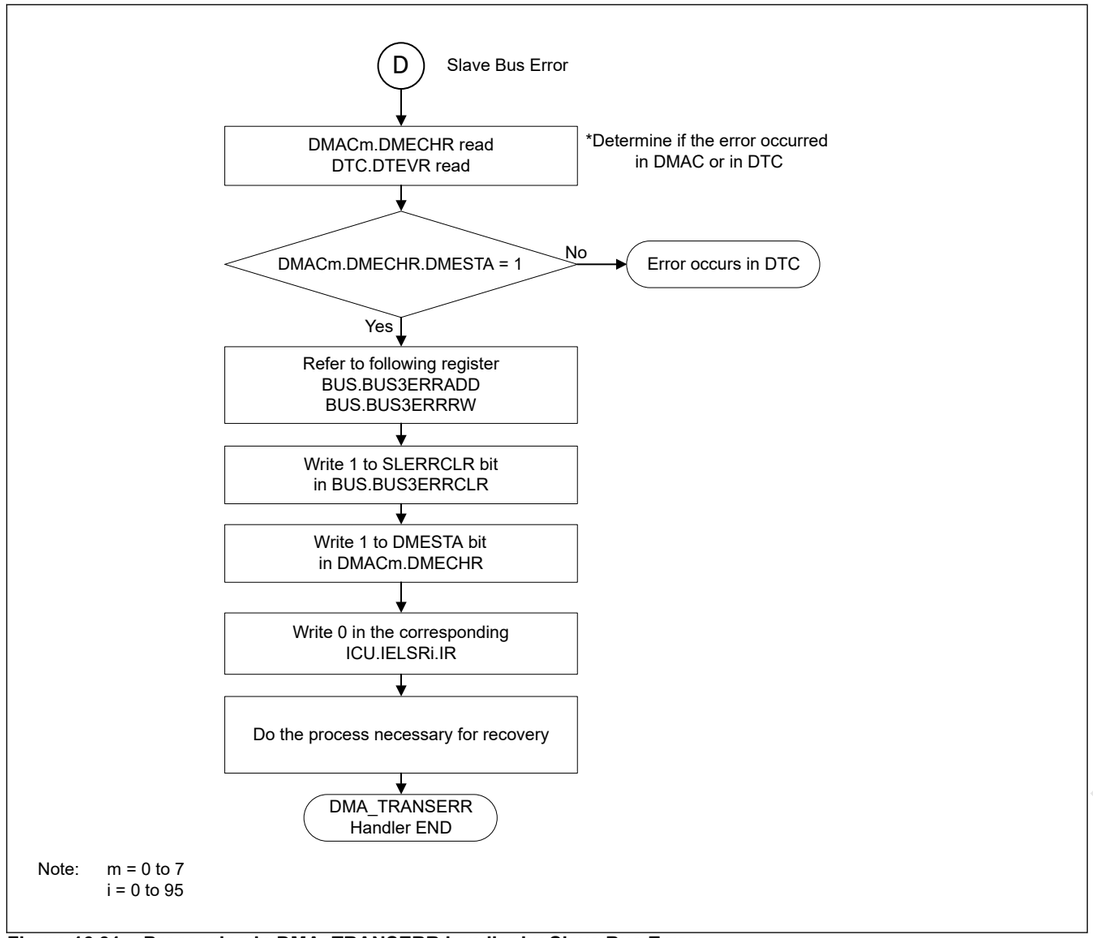


Figure 16.31 Processing in DMA_TRANSERR handler by Slave Bus Error

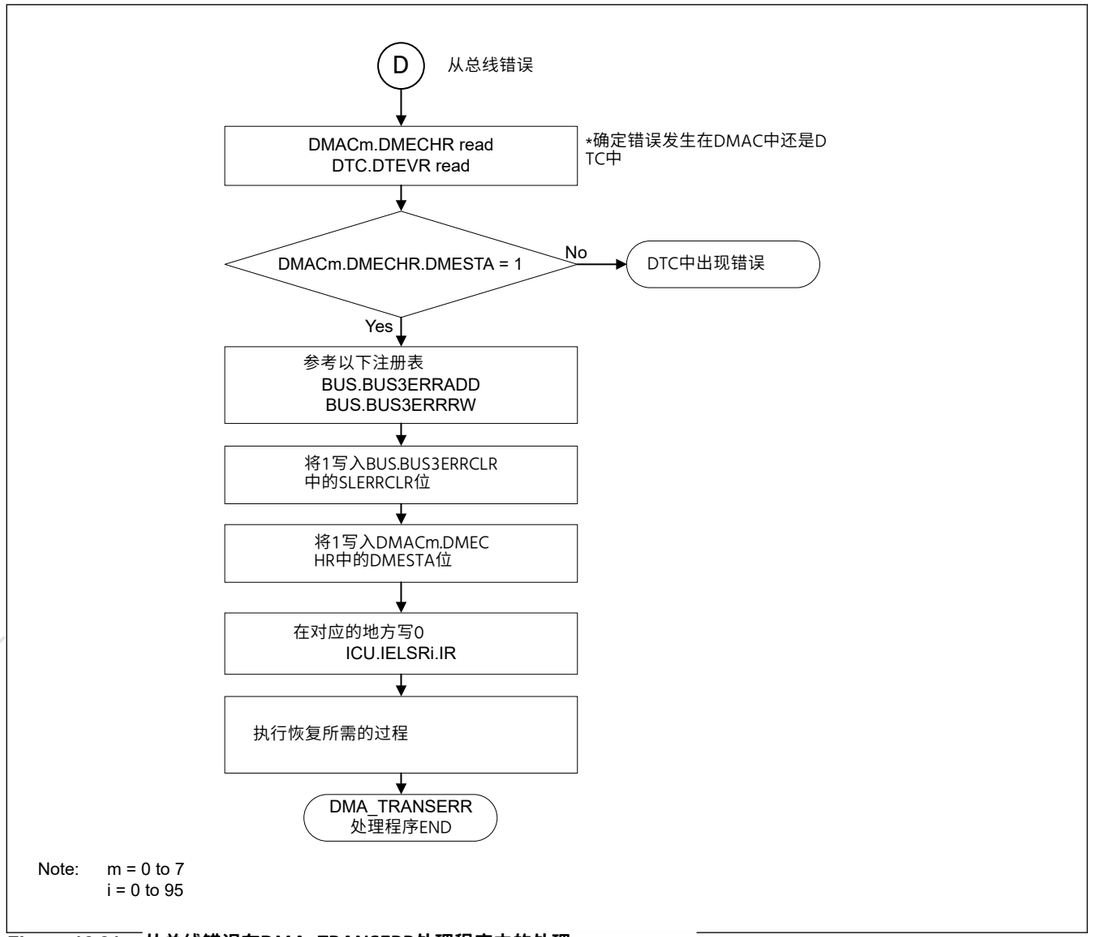


Figure 16.31 从总线错误在DMA_TRANSERR处理程序中的处理

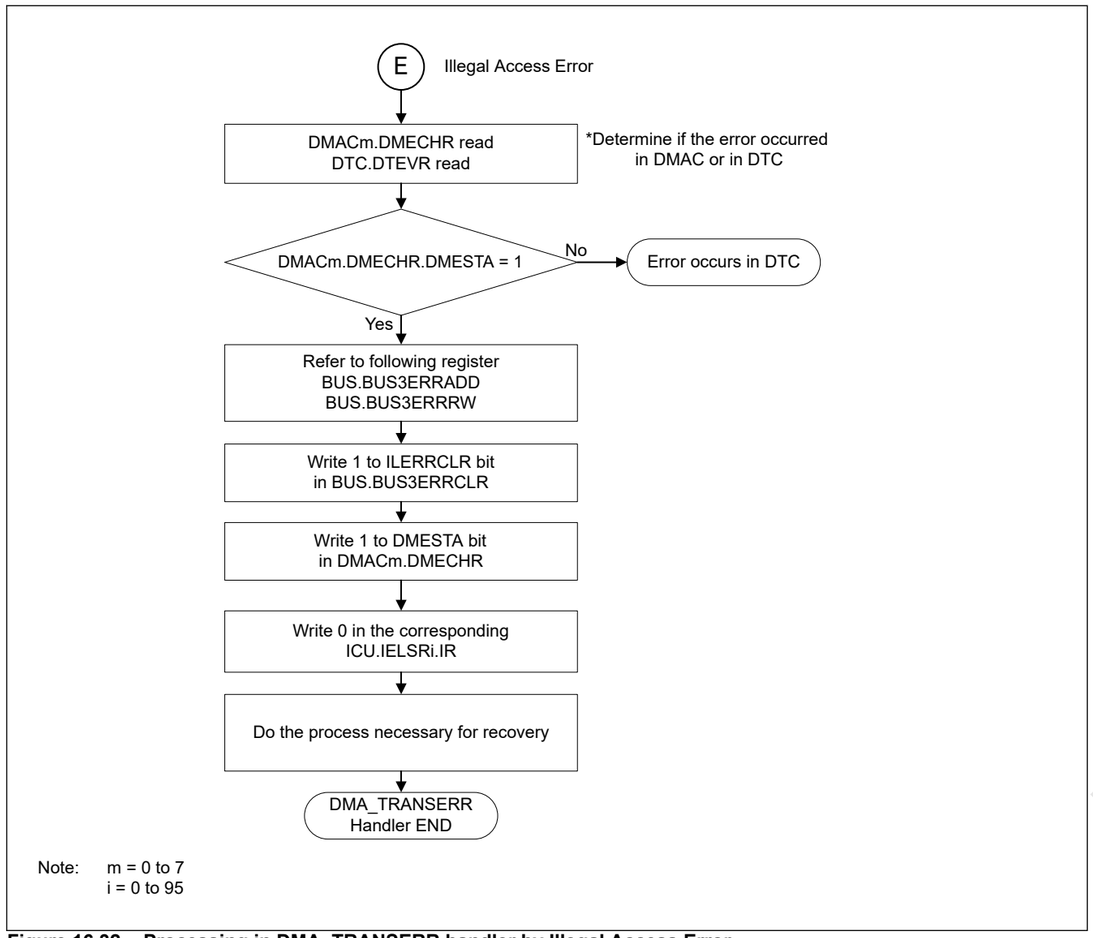


Figure 16.32 Processing in DMA_TRANSERR handler by Illegal Access Error

16.6 Interrupts

16.6.1 Transfer End Interrupt

Each DMAC channel can output an interrupt request (DMACn_INT) to the CPU or the DTC after transfer in response to one request is completed.

When the transfer destination is the external bus, an interrupt request is generated upon completion of data write to the write buffer not to the actual transfer destination.

In repeat-block transfer mode, do not enable escape transfer end interrupt.

Table 16.21 lists the relation among the interrupt sources, the interrupt status flags, and the interrupt enable bits. Figure 16.33 shows the schematic logic diagram of interrupt outputs (DMACn (n = 0 to 7)). Figure 16.34 shows the DMAC interrupt handling routine to resume/terminate DMA transfer.

Table 16.21 Relation among Interrupt Sources, Interrupt Status Flags, and Interrupt Enable Bits (1 of 2)

Interrupt Sources	Interrupt Enable Bits	Interrupt Status Flags	Request Output Enable Bits
Transfer end	—	DMSTS.DTIF	DMINT.DTIE

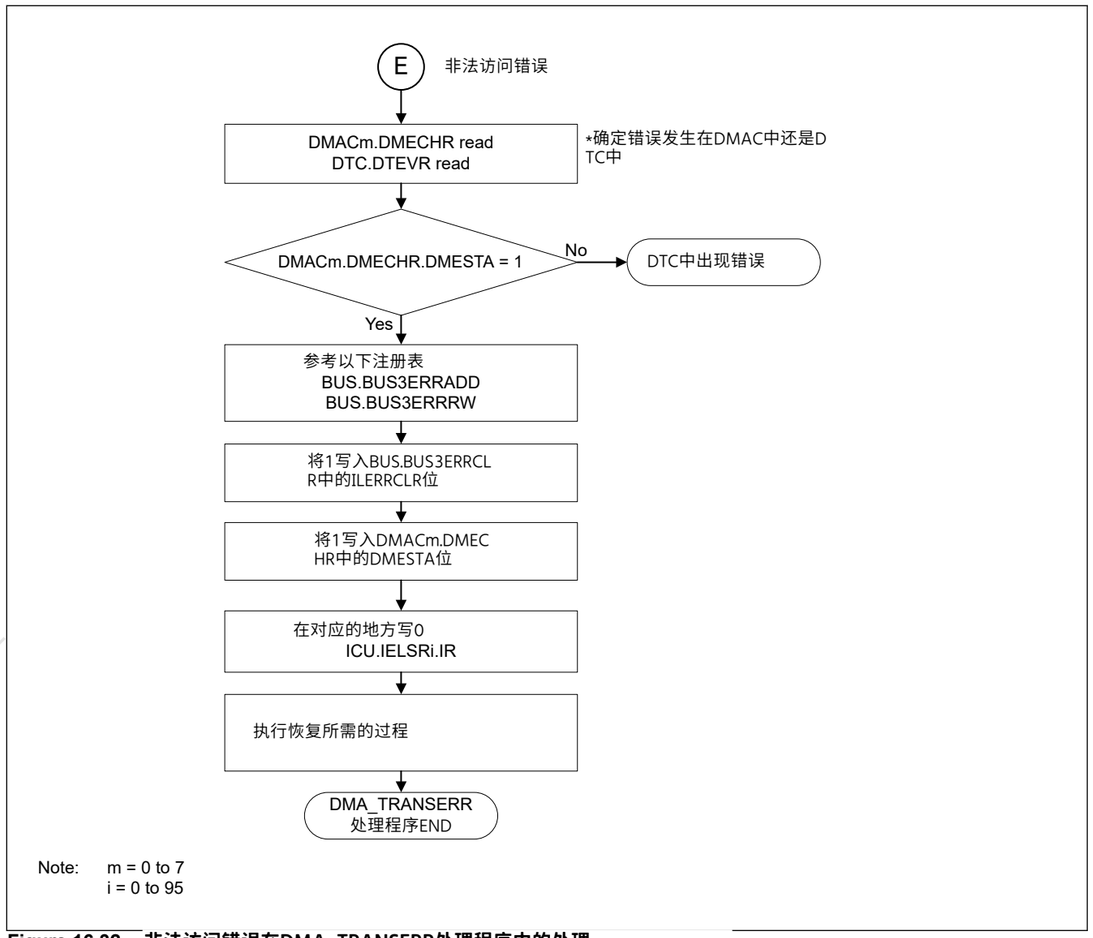


Figure 16.32 非法访问错误在DMA_TRANSERR处理程序中的处理

16.6 Interrupts

16.6.1 传输结束中断

每个DMAC通道可以在响应一个请求的传输完成后向CPU或DTC输出一个中断请求（DMACn_INT）。

当传输目的地是外部总线时，当数据写入写入缓冲区而不是实际传输目的地时，将产生中断请求。

在重复块传输模式下，不要启用转义传输结束中断。

表16.21列出了中断源、中断状态标志和中断使能位之间的关系。图16.33显示了中断输出(DMACn(n=0to7))的逻辑示意图。图16.34显示了用于恢复终止DMA传输的DMAC中断处理程序。

Table 16.21 中断源、中断状态标志和中断允许位之间的关系（1of2）

中断源	中断使能位	中断状态标志	请求输出使能 Bits
转账结束	—	DMSTS.DTIF	DMINT.DTIE

Table 16.21 Relation among Interrupt Sources, Interrupt Status Flags, and Interrupt Enable Bits (2 of 2)

Interrupt Sources		Interrupt Enable Bits	Interrupt Status Flags	Request Output Enable Bits
Escape transfer end	Repeat size end	DMINT.RPTIE	DMSTS.ESIF	DMINT.ESIE
	Source address extended repeat area overflow	DMINT.SARIE		
	Destination address extended repeat area overflow	DMINT.DARIE		

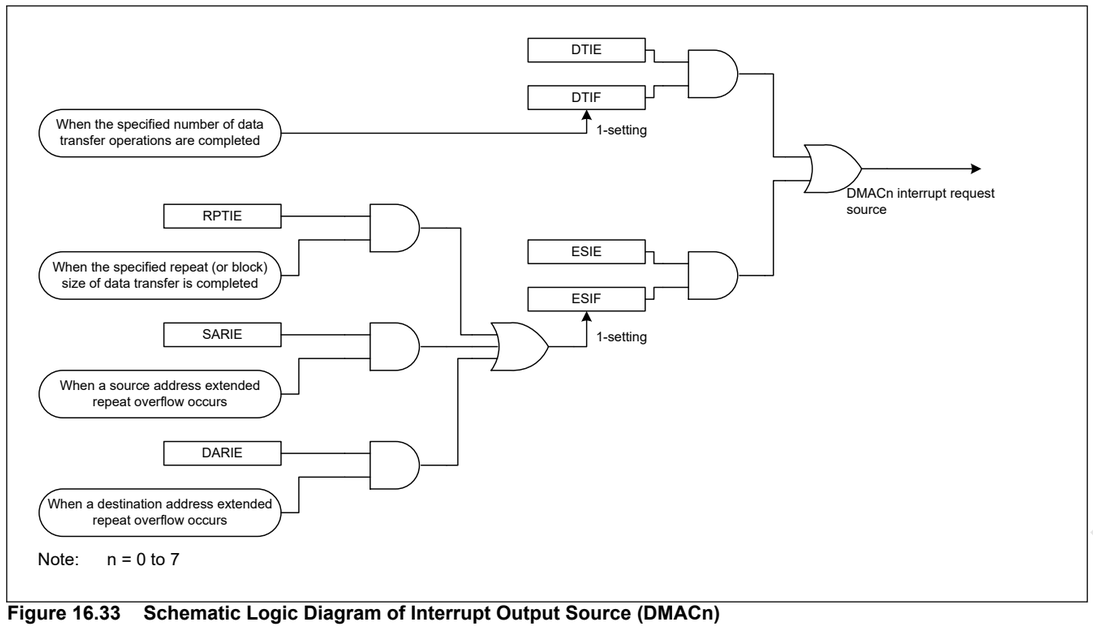


Figure 16.33 Schematic Logic Diagram of Interrupt Output Source (DMACn)

Specifically, the different procedures are used for canceling an interrupt to restart DMA transfer in the following two cases:

- When terminating a DMA transfer
- When continuing a DMA transfer

16.6.1.1 When Terminating a DMA Transfer

Write 0 to the DMSTS.DTIF flag to clear a transfer end interrupt, and to the DMSTS.ESIF flag to clear a repeat size interrupt and an extended repeat area overflow interrupt. The DMACn remains in the stop state. When starting another DMA transfer after that, set the appropriate registers, and set the DMCNT.DTE bit to 1 (DMA transfer enabled).

16.6.1.2 When Continuing a DMA Transfer

Write 1 to the DMCNT.DTE bit. The DMSTS.ESIF flag is automatically cleared to 0 (interrupt source cleared), and DMA transfer is resumed.

Table 16.21 中断源、中断状态标志和中断允许位之间的关系(2of2)

中断源		中断使能位	中断状态标志	请求输出使能 Bits
逃生转移结束	重复大小结束	DMINT.RPTIE	DMSTS.ESIF	DMINT.ESIE
	源地址扩展重复区溢出	DMINT.SARIE		
	目的地址扩展重复区溢出	DMINT.DARIE		

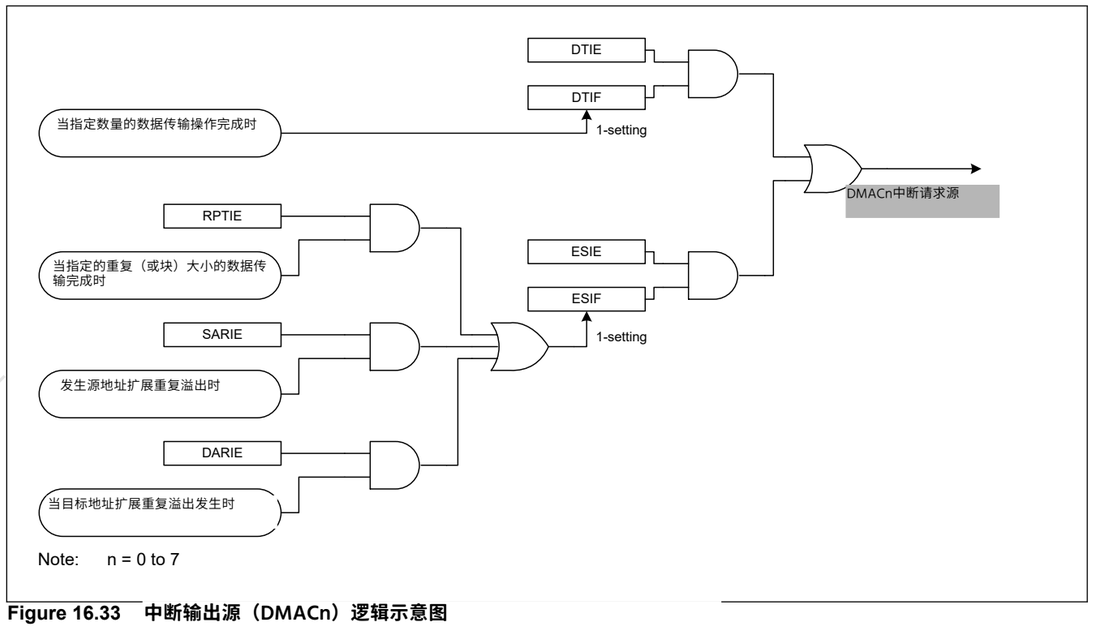


Figure 16.33 中断输出源（DMACn）逻辑示意图

具体来说，在以下两种情况下，不同的程序用于取消中断以重新启动DMA传输：

- ●终止DMA传输时
- ●继续DMA传输时

16.6.1.1 终止DMA传输时

将0写入DMSTS.DTIF标志以清除传输结束中断，写入DMSTS.ESIF标志以清除重复大小中断和扩展重复区域溢出中断。DMACn保持在停止状态。之后开始另一个DMA传输时，设置适当的寄存器，并将DMCNT.DTE位设置为1（启用DMA传输）。

16.6.1.2 继续DMA传输时

将1写入DMCNT.DTE位。DMSTS.ESIF标志自动清零（中断源清零），DMA传输恢复。

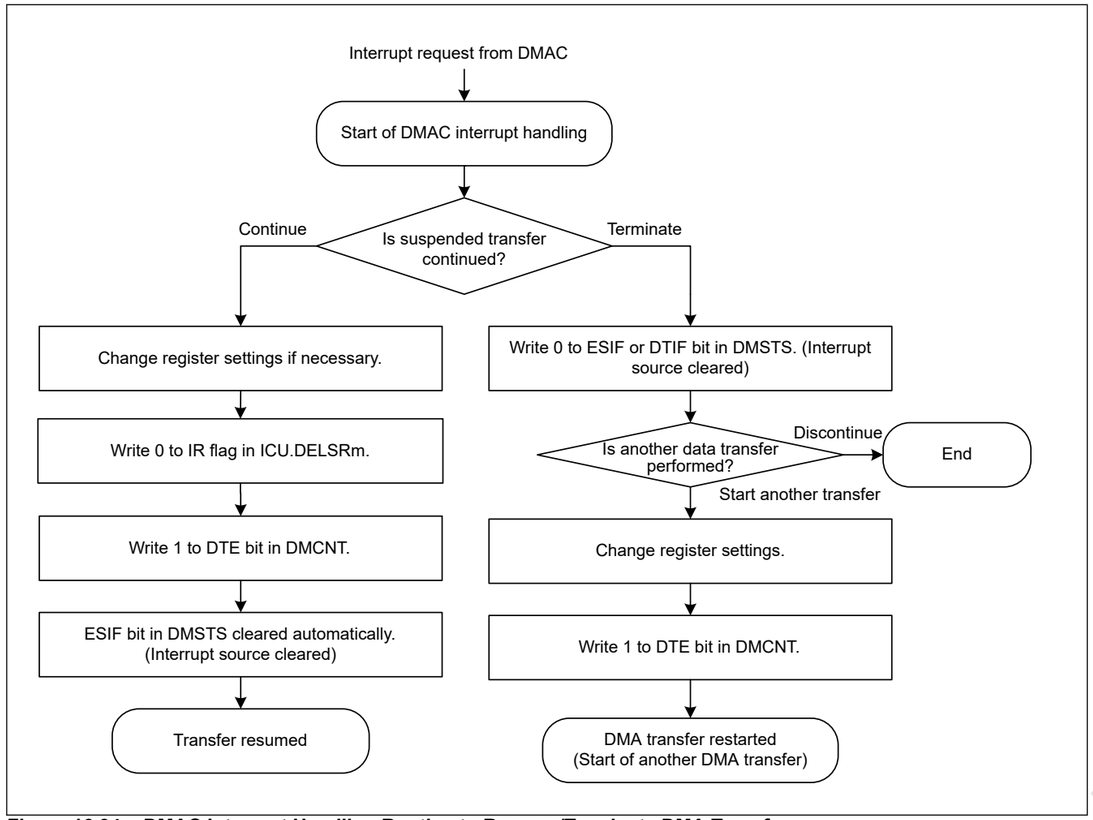


Figure 16.34 DMAC Interrupt Handling Routine to Resume/Terminate DMA Transfer

16.6.2 Transfer Error Interrupt

Error response detection interrupt request (DMA_TRANSERR) is generated from the DMAC/DTC when the transfer error is detected during DMAC transfer. The types of interrupts that occur when a DMAC transfer error occurs are listed in the Table 16.22. The Table 16.22 also shows error information stored when a transfer error occurs.

Table 16.22 Interrupt and error information due to DMAC transfer error cause

Transfer error factor	NMI/RESET*1 Request	Interrupt Request	Bus Error Status	Error Address Error R/W	Error Channel Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DMACn.DMECHR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DMACn.DMECHR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMACn.DMECHR
Slave Bus Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMACn.DMECHR
Illegal Access Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMACn.DMECHR

Note 1. Interrupt generated, when NMI request selected as the operation after detection of the Master MPU error and the TrustZone Filter error. By confirming BUS.BUS3ERRSTAT and BUS.DMACDTCERRSTAT, judge whether it is the Master or the Slave.
Note 2. If the error response detection interrupt (DMA_TRANSERR) occurs and NMI of the Master MPU or NMI of the TrustZone Filter has not occurred, treat it as the Illegal address access error or the Slave Bus Error. It can be judged also by BUS.BUS3ERRSTAT and BUS. DMACDTCERRSTAT.

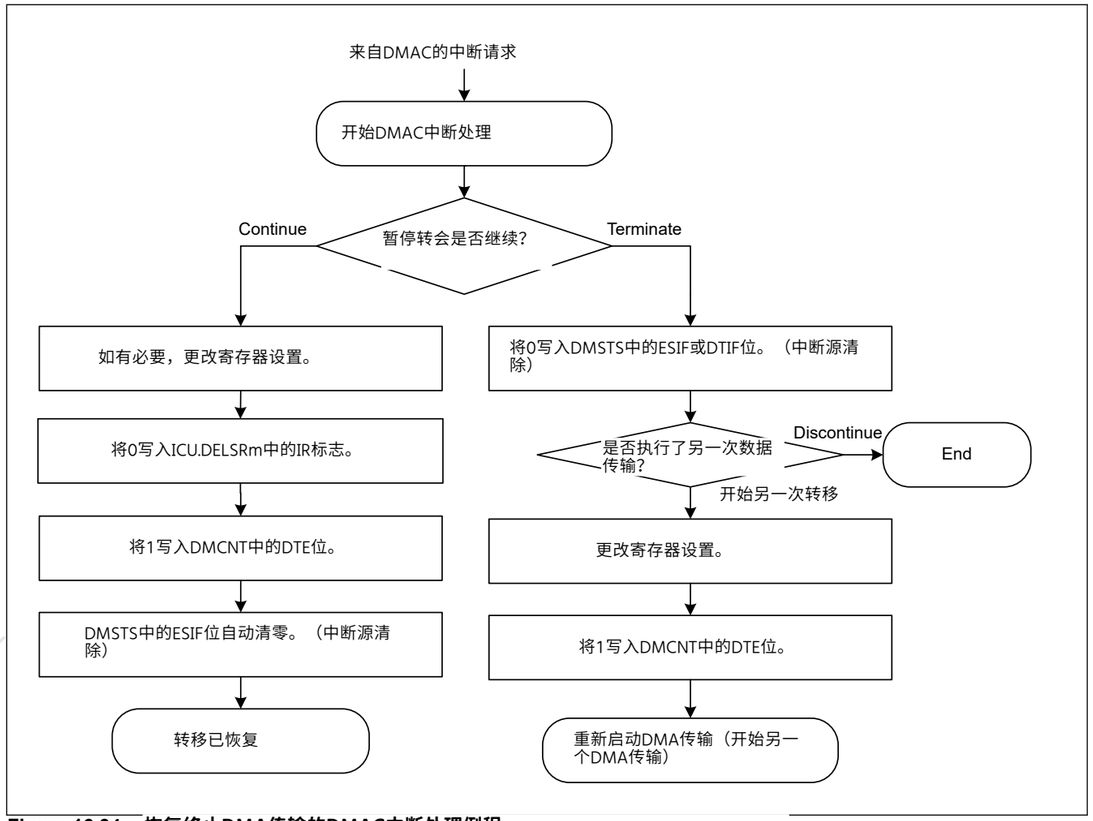


Figure 16.34 恢复终止DMA传输的DMAC中断处理例程

16.6.2 传输错误中断

在DMAC传输期间检测到传输错误时，从DMACDTC生成错误响应检测中断请求(DMA_TRANSERR)。发生DMAC传输错误时发生的中断类型在表16.22中列出。表16.22还显示了发生传输错误时存储的错误信息。

Table 16.22 由于DMAC传输错误原因导致的中断和错误信息

传递误差因子	NMI/RESET*1 Request	中断请求	总线错误状态	错误地址 Error R/W	错误通道 Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DMACn.DMECHR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DMACn.DMECHR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMACn.DMECHR
从总线错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMACn.DMECHR
非法访问错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DMACn.DMECHR

注意1.中断，当NMI请求在检测主MPU错误和Trustzone滤波器错误后选择为操作时中断。通过确认BUS.BUS3ERRSTAT和BUS.DMACDTCERRSTAT，判断是Master还是Slave。
注2.如果错误响应检测中断(DMA_TRANSERR)发生且MasterMPU的NMI或TrustZoneFilter的NMI未发生，则将其视为Illegaladdressaccesserror或SlaveBusError。也可以通过BUS.BUS3ERRSTAT和BUS来判断。DMACDTCERRSTAT。

Note that if the bus error occurs when writing the last data of transfer, the transfer end event and the error response detection interrupt (DMA_TRANSERR) occurs.

16.7 Event Link

Each DMAC channel outputs an event link request signal (DMACn_INT) every time it completes a data transfer, or a block transfer in block transfer mode.

When the transfer destination is the external bus, an event link request signal is generated when the writing to the write buffer is accepted.

For details, see section 18, Event Link Controller (ELC).

If a bus error occurs when writing the last data of transfer, a transfer end event and error response detection interrupt (DMA_TRANSERR) occurs.

16.8 Low-Power Consumption Function

Before entering the module-stop state or Software Standby mode, or Deep Software Standby mode, you must first set the DMAST.DMST bit to 0 (the DMAC module suspended), and use the settings in the sections that follow.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DMAC. If a DMA transfer is in progress when 1 is written to the MSTPA22 bit, the transition to the module-stop state proceeds after the DMA transfer ends. Access to the DMAC registers is prohibited while the MSTPA22 bit is 1. Writing 0 to the MSTPA22 bit releases the DMAC from the module-stop state.

(2) Software Standby mode and Deep Software Standby mode

Use the settings described in section 10.7.1. Transitioning to Software Standby Mode, or in section 10.9.1. Transitioning to Deep Software Standby Mode .

If DMA transfer operations are in progress when the WFI instruction is executed, the DMA transfer completes before the transition to Software Standby mode or Deep Software Standby mode.

(3) Notes on low power consumption function

For information on the WFI instruction and register settings, see section 10.10.7. Timing of WFI Instruction.

To perform a DMA transfer after returning from a low power consumption mode, set the DMAST.DMST bit to 1 again. To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination, as described in section 13.4.1. Detecting Interrupts, and then execute the WFI instruction.

16.9 Usage Notes

16.9.1 DMA Transfer to External Devices

In a DMA transfer to an external device, the DMSTS.ACT flag may change to 0 (the DMAC suspended) before the external bus access ends after the final data write is started.

16.9.2 Access to the Registers during DMA Transfer

Do not write to the following registers while the DMSTS.ACT flag of the same channel is set to 1 (DMAC active state) or the DMCNT.DTE bit of the same channel is set to 1 (DMA transfer enabled):

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT

请注意，如果在写入传输的最后一个数据时发生总线错误，则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

16.7 活动链接

每个DMAC通道在每次完成数据传输或块传输模式下的块传输时都会输出一个事件链接请求信号(DMACn_INT)。

当传输目的地是外部总线时，当接受写入缓冲区的写入时，将生成事件链接请求信号。

有关详细信息，请参阅第18节，事件链接控制器(ELC)。

如果在写入传输的最后一个数据时发生总线错误，则会发生传输结束事件和错误响应检测中断(DMA_TRANSERR)。

16.8 低功耗功能

在进入模块停止状态或软件待机模式或深度软件待机模式之前，您必须先设置DMAST.DMST位为0（DMAC模块挂起），并使用以下部分中的设置。

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DMAC的模块停止功能。如果在向MSTPA22位写入1时正在进行DMA传输，则在DMA传输结束后继续转换到模块停止状态。当MSTPA22位为1时，禁止访问DMAC寄存器。将0写入MSTPA22位可将DMAC从模块停止状态释放。

(2) 软件待机模式和深度软件待机模式

使用第10.7.1节中描述的设置。转换到软件待机模式，或在第10.9.1节中。过渡到深度软件待机模式。

如果在执行WFI指令时DMA传输操作正在进行，则DMA传输在转换到软件待机模式或深度软件待机模式之前完成。

(3) 低功耗功能注意事项

有关WFI指令和寄存器设置的信息，请参阅第10.10.7节。WFI指令的时间安排。

要在从低功耗模式返回后执行DMA传输，请将DMAST.DMST位再次设置为1。要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DMAC启动请求，请将CPU指定为中断请求目标，如第13.4.1节所述。检测中断，然后执行WFI指令。

16.9 使用说明

16.9.1 DMA传输到外部设备

在到外部设备的DMA传输中，在开始最终数据写入后外部总线访问结束之前，DMSTS.ACT标志可能会变为0（DMAC挂起）。

16.9.2 在DMA传输期间访问寄存器

当同一通道的DMSTS.ACT标志设置为1（DMAC活动状态）或同一通道的DMCNT.DTE位设置为1（启用DMA传输）时，请勿写入以下寄存器：

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT

- DMAMD
- DMOFR
- DMSBS
- DMDBS
- DMSRR
- DMDRR
- DMBWR
- ICUSARC
- DMACSAR

16.9.3 DMA Transfer to Reserved Areas

DMA transfer to the reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on the reserved areas, see section 4, Address Space.

16.9.4 Setting of DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU.DELSRn n = 0 to 7)

The DMAC event link setting register (ICU.DELSRn) should be set while the DMA transfer enable bit (DMCNT.DTE) is cleared to 0 (DMA transfer is disabled). Moreover, the DTC activation enable register (ICU.IELSRn.DTCE (n = 0 to 95)) that corresponds to the same event number that has been set by the ICU.DELSRn register should not be set to 1. For details on the ICU.IELSRn.DTCE and ICU.DELSRn, see section 13, Interrupt Controller Unit (ICU).

16.9.5 Suspending or Restarting DMAC Activation

To suspend a DMAC activation request, write 0x00 to the DMAC Event Link select bits (ICU.DELSRn.DELS[8:0]). To restart the DMA transfer, write the event number to the ICU.DELSRn.DELS[8:0] bits following the settings shown in section 16.3.10. Activating the DMAC.

16.9.6 Precautions for Resuming DMA Transfer

A DMAC activation request might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMAC activation request is held in the DMAC. To prevent this, stop the DMAC activation requests by setting the DELSRn.DELS[8:0] bits in the ICU to 0.

When a DMAC activation request occurs after the last round of the DMA transfer is generated, clear the DMAC activation request with either of the following approaches.

- Clear the DMAC activation request with a DMA dummy transfer.
- Set the DMCNT.DTE bit to 0 and then set the ICU.DELSRn.IR flag to 0.

See Figure 16.35.

- DMAMD
- DMOFR
- DMSBS
- DMDBS
- DMSRR
- DMDRR
- DMBWR
- ICUSARC
- DMACSAR

16.9.3 DMA传输到保留区域

禁止对保留区域进行DMA传输。如果进行此类访问，则无法保证传输结果。有关保留区域的详细信息，请参阅第4节，地址空间。

16.9.4 中断控制器单元的DMAC事件链接设置寄存器的设置(ICU.DELSRnn=0到7)

DMAC事件链接设置寄存器(ICU.DELSRn)应在DMA传输启用位(DMCNT.DTE)清除为0（禁用DMA传输）时设置。此外，与已由ICU.DELSRn寄存器设置的相同事件编号对应的DTC激活使能寄存器(ICU.IELSRn.DTCE(n=0至95))不应设置为1。有关ICU的详细信息.IELSRn.DTCE和ICU.DELSRn，请参见第13节，中断控制器单元(ICU)。

16.9.5 暂停或重新启动DMAC激活

要暂停DMAC激活请求，请将0x00写入DMAC事件链接选择位(ICU.DELSRn.DELS[8:0])。要重新启动DMA传输，请按照第16.3.10节中所示的设置将事件编号写入ICU.DELSRn.DELS[8:0]位。激活DMAC。

16.9.6 恢复DMA传输的注意事项

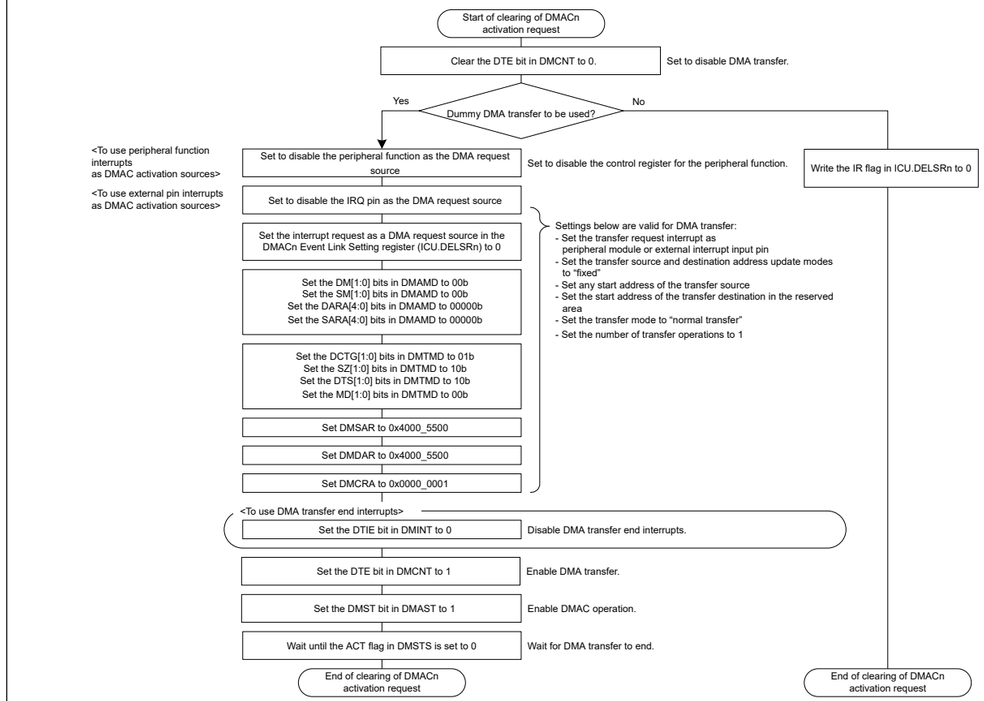
DMA传输完成后的下一个请求中可能会出现DMAC激活请求。如果发生这种情况，DMA传输开始并且DMAC激活请求被保存在DMAC中。为防止这种情况，请通过将ICU中的DELSRn.DELS[8:0]位设置为0来停止DMAC激活请求。

当最后一轮DMA传输生成后出现DMAC激活请求时，可通过以下任一方法清除DMAC激活请求。

●使用DMA虚拟传输清除DMAC激活请求。

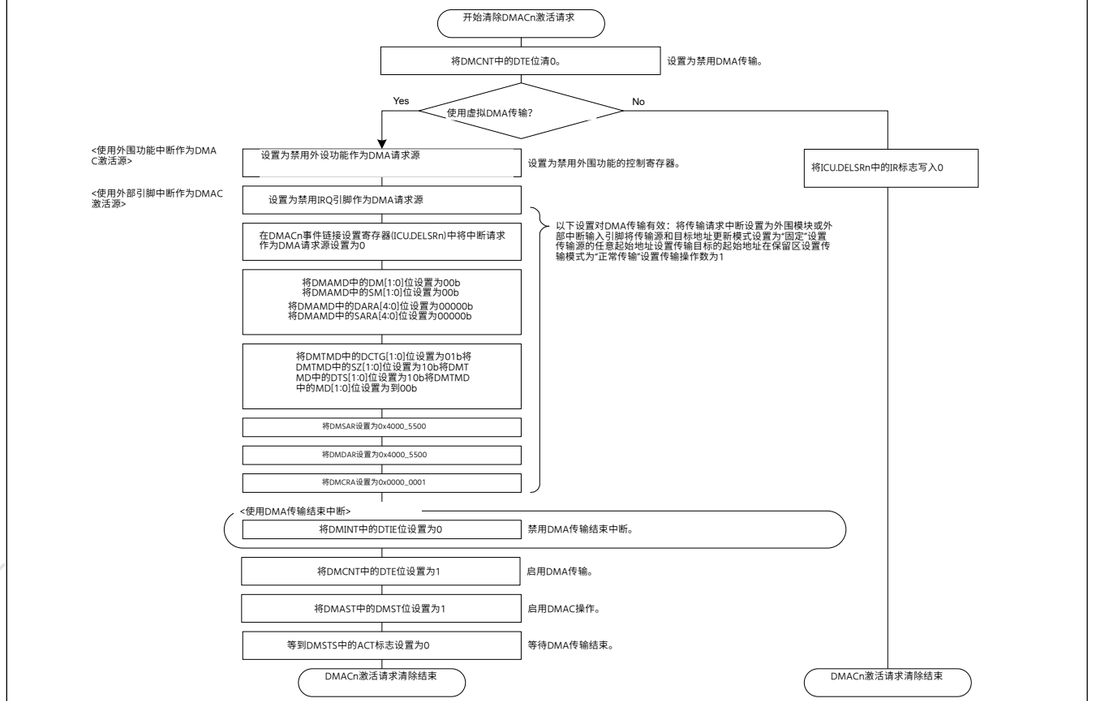
●将DMCNT.DTE位设置为0，然后将ICU.DELSRn.IR标志设置为0。

请参见图16.35。



Note: n: 0 to 7

Figure 16.35 Example of register setting procedure to clear the DMAC activation interrupt



Note: n: 0 to 7

Figure 16.35 清除DMAC激活中断的寄存器设置过程示例

17. Data Transfer Controller (DTC)

17.1 Overview

A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 17.1 lists the DTC specifications and Figure 17.1 shows DTC block diagram.

Table 17.1 DTC specifications

Parameter	Description
Transfer modes	● Normal transfer mode A single activation leads to a single data transfer. ● Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes) ● Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	● Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) ● Multiple data units can be transferred on a single activation source (chain transfer) ● Chain transfers are selectable to either execute when the counter is 0, or always execute.
Transfer space	● 4 GB area from 0x0000_0000 to 0xFFFF_FFFF, excluding reserved areas
Data transfer units	● Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) ● Single block size: 1 to 256 data units.
CPU interrupt source	● An interrupt request can be generated to the CPU on a DTC activation interrupt ● An interrupt request can be generated to the CPU after a single data transfer ● An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Processing on DTC transfer error	● When the DTC transfer error occurs, it stops the transfer that caused the error ● Request to clear the register for activation request of DTC error number to ICU
Error response detection interrupt	Generated when the DTC transfer error occurs
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped
TrustZone	TrustZone violation area of Flash and SRAM is detected in advance before access the bus.
Module-stop function	Module-stop state can be set to reduce power consumption
TrustZone Filter	Security attribution can be set for each activation source

Note: Security attribution Regiser of DTC is described in ICU.ICUSARG, ICU.ICUSARH and ICU.ICUSARI

17. 数据传输控制器(DTC)

17.1 Overview

数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。

表17.1列出了DTC规范，图17.1显示了DTC框图。

Table 17.1 DTC specifications

Parameter	Description
传输模式	● 正常传输模式 单次激活导致单次数据传输。 ● 重复传输模式 单次激活导致单次数据传输。 数据传输次数达到指定的重复大小后，传输地址返回起始地址。最大重复传输次数为256，最大数据传输大小为256×32位（1024字节） ● 块传输模式 单个激活导致单个块的传输。最大块大小为256×32位=1024字节。
传输通道	● 通道传输可以与中断源相关联（由来自ICU的DTC激活请求传输） ● 可以在单个激活源上传输多个数据单元（链式传输） ● 链式传输可选择在计数器为0时执行或始终执行。
转移空间	● 4GB区域，从0x0000_0000到0xFFFF_FFFF，不包括保留区域
数据传输单元	● 单个数据单元：1个字节（8位）、1个半字（16位）、1个字（32位） ● 单块大小：1到256个数据单元。
CPU中断源	● 可以在DTC激活中断时向CPU生成中断请求 ● 单次数据传输后可向CPU产生中断请求 ● 在指定卷的数据传输后，可以向CPU产生中断请求。
DTC传输错误的处理	● 当发生DTC传输错误时，它会停止导致错误的传输 ● 向ICU请求清除DTC错误号激活请求的寄存器
错误响应检测中断	发生DTC传输错误时生成
事件链接功能	一次数据传输后产生事件链接请求（对于块，在一次块传输后）
阅读跳过	可以跳过读取传输信息
Write-back skip	当传输源或目标地址指定为固定时，可以跳过传输信息的回写
TrustZone	在访问总线之前，预先检测到Flash和SRAM的TrustZone违规区域。
Module-stop function	可设置模块停止状态以降低功耗
TrustZone Filter	可以为每个激活源设置安全属性

Note: ICU.ICUSARG、ICU.ICUSARH和ICU.ICUSARI中描述了DTC的安全属性注册器

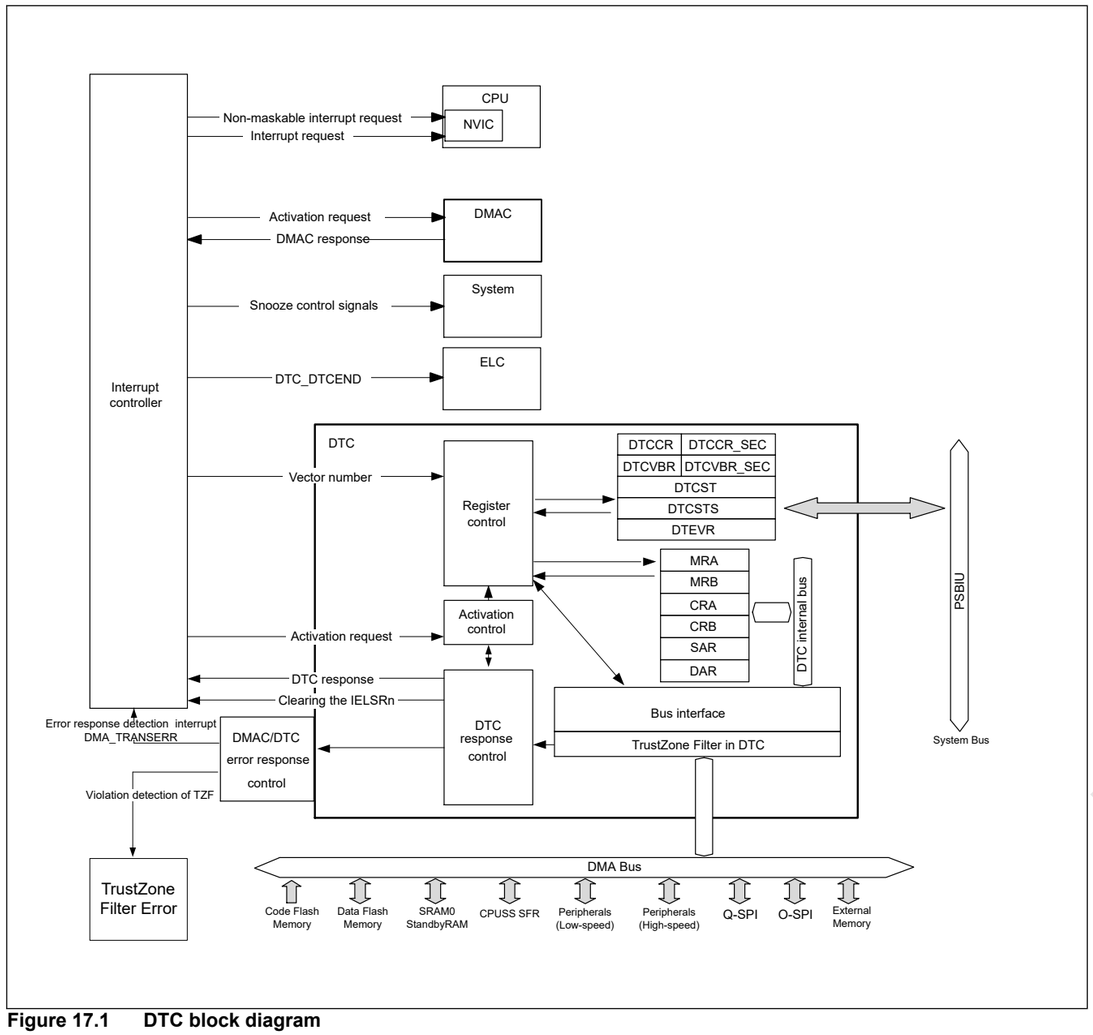


Figure 17.1 DTC block diagram

See section 13.1. Overview in section 13, Interrupt Controller Unit (ICU) for the connections between the DTC and NVIC in the CPU.

17.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

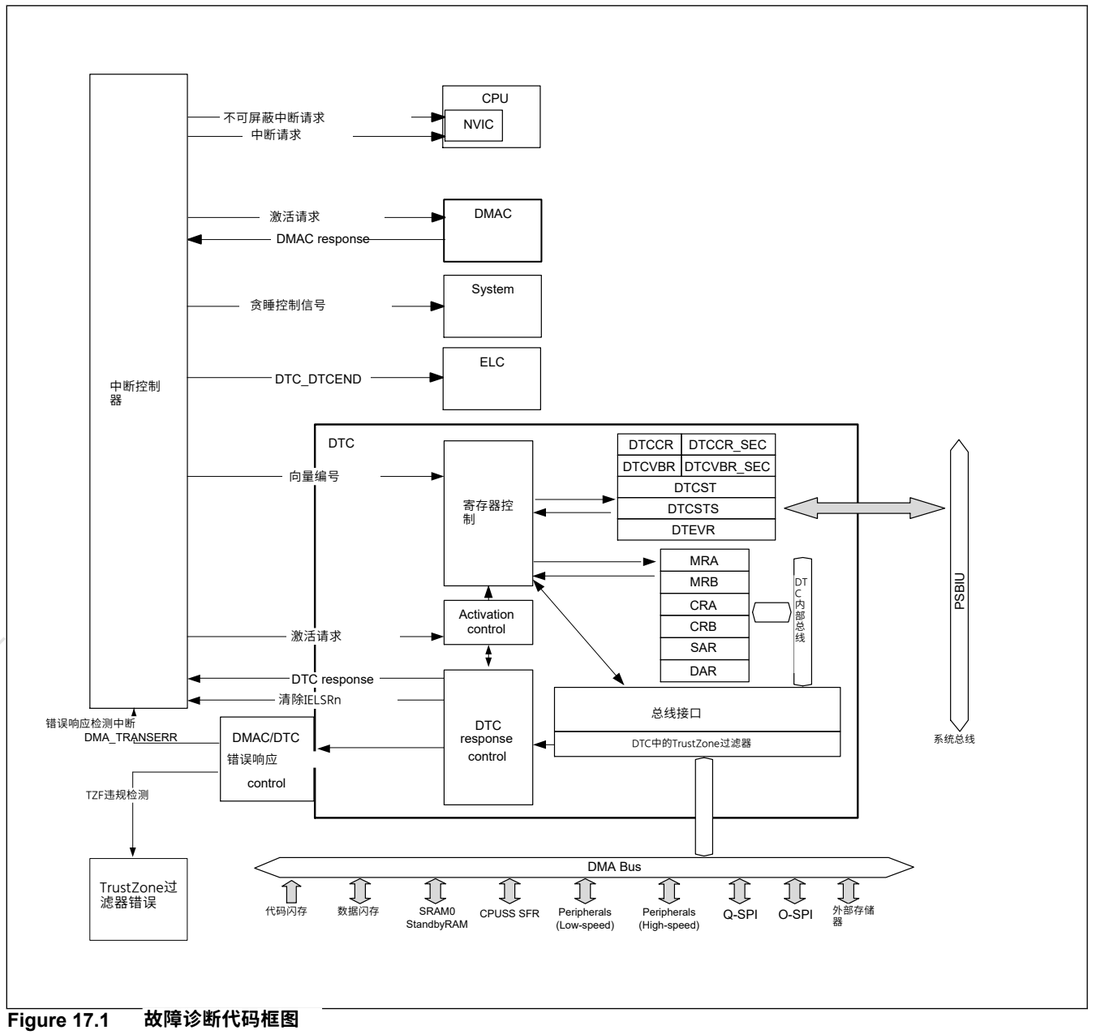


Figure 17.1 故障诊断代码框图

请参见第13.1节。第13节，中断控制器单元(ICU)中的概述，用于CPU中的DTC和NVIC之间的连接。

17.2 注册说明

MRA、MRB、SAR、DAR、CRA、CRB都是DTC内部寄存器，不能直接从CPU访问。在这些DTC内部寄存器中设置的值作为传输信息放置在SRAM区域中。当产生激活请求时，DTC从SRAM区域读取传输信息并将其设置在其内部寄存器中。数据传输结束后，内部寄存器内容作为传输信息回写到SRAM区域。

17.2.1 DTCSAR : DTC Controller Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTCSTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DTCSTSA	DTC Security Attribution 0: Secure. 1: Non-Secure.	R/W
31:1	—	This bit is read as 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

This register only sets the DTCST security attribute.

DTCSTSA bit (DTC Security Attribution)

Security attributes of registers for DTCST.

Do not write to the DTCSTSA bit while DTC transfer is enabled or a bus master is writing to the DTC registers.

17.2.2 MRA : DTC Mode Register A

Base address: DTCVBR

Offset address: 0x03 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 17.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	SM[1:0]	Transfer Source Address Addressing Mode 0 0: Address in the SAR register is fixed (write-back to SAR is skipped.) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped.) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—

17.2.1 DTCSAR：DTC控制器安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTCSTSA
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	DTCSTSA	DTC安全归因 0: Secure. 1: Non-Secure.	R/W
31:1	—	该位读为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

该寄存器仅设置DTCST安全属性。

DTCSTSA位（DTC安全属性）

DTCST寄存器的安全属性。

当DTC传输启用或总线主机正在写入DTC寄存器时，请勿写入DTCSTSA位。

17.2.2 MRA:DTC模式寄存器A

Base address: DTCVBR

Offset address: 0x03+0x4×向量编号（无法直接从CPU访问。请参阅第17.3.1节。分配传输信息和DTC向量表）

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	读取的值未定义。写入值应为0。	—
3:2	SM[1:0]	传输源地址寻址方式 00：固定SAR寄存器中的地址（跳过对SAR的回写。）01：固定SAR寄存器中的地址（跳过对SAR的回写。）10：数据传输后SAR值递增:+1当SZ[1:0]=00b时+2当SZ[1:0]=01b时+4当SZ[1:0]=10b时 11：数据传输后SAR值递减：-1当SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b	—

Bit	Symbol	Function	R/W
5:4	SZ[1:0]	DTC Data Transfer Size 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited	—
7:6	MD[1:0]	DTC Transfer Mode Select 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

The MRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x03) and DTC transfers it automatically to and from the MRA register. See section 17.3.1. Allocating Transfer Information and DTC Vector Table.

17.2.3 MRB : DTC Mode Register B

Base address: DTCVBR

Offset address: 0x02 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 17.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	The read values are undefined. The write value should be 0.	—
3:2	DM[1:0]	Transfer Destination Address Addressing Mode 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in the DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b 1 1: DAR value is decremented after data transfer: -1 when MRA.SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b	—
4	DTS	DTC Transfer Mode Select 0: Select transfer destination as repeat or block area 1: Select transfer source as repeat or block area	—
5	DISEL	DTC Interrupt Select 0: Generate an interrupt request to the CPU when specified data transfer is complete 1: Generate an interrupt request to the CPU each time DTC data transfer is performed	—
6	CHNS	DTC Chain Transfer Select 0: Chain transfer is continuous 1: Chain transfer occurs only when the transfer counter changes from 1 to 0 or 1 to CRAH	—
7	CHNE	DTC Chain Transfer Enable 0: Chain transfer is disabled 1: Chain transfer is enabled	—

The MRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0x02) and DTC transfers it automatically to and from the MRB register. See section 17.3.1. Allocating Transfer Information and DTC Vector Table.

Bit	Symbol	Function	R/W
5:4	SZ[1:0]	DTC数据传输大小 00：字节（8位）传送01：半字（16位）传送10：字（32位）传送11：禁止设置	—
7:6	MD[1:0]	DTC传输模式选择 00：正常传输模式01：重复传输模式10：块传输模式11：禁止设置	—

MRA寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0x03）并且DTC会自动将其传输到MRA寄存器或从MRA寄存器传输。请参阅第17.3.1节。分配传输信息和DTC向量表。

17.2.3 MRB:DTC模式寄存器B

Base address: DTCVBR

Offset address: 0x02+0x4×向量编号（无法直接从CPU访问。请参阅第17.3.1节。分配传输信息和DTC向量表）

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	—	读取的值未定义。写入值应为0。	—
3:2	DM[1:0]	传输目标地址寻址模式 00：DAR寄存器中的地址固定（跳过DAR的回写）01：DAR寄存器中的地址固定（跳过DAR的回写）10：数据传输后DAR值递增：+1当MRA.SZ[1:0]=00b+2当SZ[1:0]=01b+4当SZ[1:0]=10b 11：数据传输后DAR值递减：-1当MRA.SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b	—
4	DTS	DTC传输模式选择 0：选择传输目标为重复区域或块区域1：选择传输源为重复区域或块区域	—
5	DISEL	DTC中断选择 0：指定数据传输完成时向CPU产生中断请求1：每次执行DTC数据传输时向CPU产生中断请求	—
6	CHNS	DTC链转移选择 0：链转移连续1：链转移仅在转移计数器从1变为0或1变为CRAH时发生	—
7	CHNE	DTC链转移启用 0：禁止链式传输1：启动链式传输	—

MRB寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0x02）并且DTC自动将其传输到MRB寄存器和从MRB寄存器传输。请参阅第17.3.1节。分配传输信息和DTC向量表。

DM[1:0] bits (Transfer Destination Address Addressing Mode)

The DM[1:0] bits is to fix the address of the DAR register or specify increment / decrement of the DAR register after transfer.

DTS bit (DTC Transfer Mode Select)

The DTS bit specifies whether the transfer source or destination is the repeat or block area in repeat or block transfer mode.

DISEL bit (DTC Interrupt Select)

The DISEL bit specifies the condition for generating an interrupt request to the CPU.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 17.3.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected by the CHNS bit. For details on chain transfer, see section 17.4.6. Chain Transfer.

17.2.4 SAR : DTC Transfer Source Register

Base address: DTCVBR

Offset address: 0x04 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 17.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The SAR sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x04) and DTC transfers it automatically to and from the SAR register. See section 17.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

17.2.5 DAR : DTC Transfer Destination Register

Base address: DTCVBR

Offset address: 0x08 + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 17.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	31																												0
Bit field:																													
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The DAR sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x08) and DTC transfers it automatically to and from the DAR register. See section 17.3.1. Allocating Transfer Information and DTC Vector Table.

Misalignment is prohibited for DTC transfers. Bit[0] must be 0 when MRA.SZ[1:0] = 01b, and bit[1] and bit[0] must be 0 when MRA.SZ[1:0] = 10b.

DM[1:0]位（传输目标地址寻址模式）

DM[1:0]位用于固定DAR寄存器的地址或指定DAR寄存器在传输后递增递减。

DTS位（DTC传输模式选择）

DTS位指定传输源或目标是否是重复或块传输模式下的重复或块区域。

DISEL位（DTC中断选择）

DISEL位指定向CPU产生中断请求的条件。

CHNS位（DTC链传输选择）

CHNS位选择链传输条件。当CHNE为0时，忽略CHNS设置。链转移条件详见表17.3。

当下一次传输是链式传输时，指定的传输次数未确定，激活源标志未清除，也不向CPU产生中断请求。

CHNE位（DTC链传输使能）

CHNE位启用链式传输。链传输条件由CHNS位选择。有关链式转移的详细信息，请参阅第17.4.6节。链转移。

17.2.4 SAR：DTC传输源寄存器

Base address: DTCVBR

Offset address: 0x04+0x4×向量编号（无法直接从CPU访问。请参阅第17.3.1节。分配传输信息和DTC向量表）

Bit position:	31																												0
Bit field:																													
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

SAR设置传输源起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x04），并且DTC会自动将其传输到SAR寄存器或从SAR寄存器传输。请参阅第17.3.1节。分配传输信息和DTC向量表。

DTC传输禁止错位。当MRA.SZ[1:0]=01b时Bit[0]必须为0，当MRA.SZ[1:0]=10b时bit[1]和bit[0]必须为0。

17.2.5 DAR:DTC传输目的地寄存器

Base address: DTCVBR

Offset address: 0x08+0x4×向量编号（无法直接从CPU访问。请参阅第17.3.1节。分配传输信息和DTC向量表）

Bit position:	31																												0
Bit field:																													
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

DAR设置传输目标起始地址，不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x08）并且DTC会自动将其传输到DAR寄存器或从DAR寄存器传输。请参阅第17.3.1节。分配传输信息和DTC向量表。

DTC传输禁止错位。当MRA.SZ[1:0]=01b时Bit[0]必须为0，当MRA.SZ[1:0]=10b时bit[1]和bit[0]必须为0。

17.2.6 CRA : DTC Transfer Count Register A

Base address: DTCVBR

Offset address: 0x0E + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 17.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	Transfer Counter A Lower Register Specify the transfer count.	—
15:8	CRAH	Transfer Counter A Upper Register Specify the transfer count.	—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register consists of 16 bits. CRAL is the lower 8 bits and CRAH is the upper 8 bits. CRA is used in normal mode.

CRAL and CRAH are used in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0E) and DTC transfers it automatically to and from the CRA register. See section 17.3.1. Allocating Transfer Information and DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 0x01, 0xFF, and 0x00, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 0x00, the CRAH value is transferred to CRAL.

17.2.7 CRB : DTC Transfer Count Register B

Base address: DTCVBR

Offset address: 0x0C + 0x4 × Vector number
(Inaccessible directly from the CPU. See section 17.3.1. Allocating Transfer Information and DTC Vector Table)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The CRB sets the block transfer count for block transfer mode. The transfer count is 1, 65535, and 65536 when the set value is 0x0001, 0xFFFF, and 0x0000, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

17.2.6 CRA:DTC传输计数寄存器A

Base address: DTCVBR

Offset address: 0x0E+0x4×向量编号（无法直接从CPU访问。请参阅第17.3.1节。分配传输信息和DTC向量表）

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	CRAL	传送计数器A低位寄存器 指定传输计数。	—
15:8	CRAH	传送计数器A高位寄存器 指定传输计数。	—

Note: 该功能取决于传输模式。
Note: 在重复传输模式和块传输模式下，将CRAH和CRAL设置为相同的值。

CRA寄存器由16位组成。CRAL是低8位，CRAH是高8位。CRA在正常模式下使用。

CRAL和CRAH用于重复传输模式和块传输模式。

CRA寄存器不能直接从CPU访问。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x0E），DTC会自动将其传输到CRA寄存器或从CRA寄存器传输。请参阅第17.3.1节。分配传输信息和DTC向量表。

(1) 正常传输模式（MRA.MD[1:0]=00b）

在正常传输模式下，CRA用作16位传输计数器。当设置值为0x0001、0xFFFF和0x0000时，传输计数分别为1、65535和65536。CRA值在每次数据传输时递减(-1)。

(2) 重复传输模式(MRA.MD[1:0]=01b)

在重复传输模式下，CRAH寄存器保存传输计数，CRAL寄存器用作8位传输计数器。当设置值为0x01、0xFF和0x00时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(-1)。当它达到0x00时，CRAH值被传送到CRAL。

(3) 块传输模式（MRA.MD[1:0]=10b）

在块传输模式下，CRAH寄存器保存块大小，CRAL寄存器用作8位块大小计数器。当设置值为0x01、0xFF和0x00时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(-1)。当它达到0x00时，CRAH值被传送到CRAL。

17.2.7 CRB:DTC传输计数寄存器B

Base address: DTCVBR

Offset address: 0x0C+0x4×向量编号（无法直接从CPU访问。请参阅第17.3.1节。分配传输信息和DTC向量表）

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

CRB设置块传输模式的块传输计数。当设置值为0x0001、0xFFFF和0x0000时，传输计数分别为1、65535和65536。当传输单个块大小的最终数据时，CRB值递减(-1)。Whennormaltransfermodeorrepeattransfermodeisselected thisregisterisnotusedandthesetvalueisignored.

The CRB cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 0x0C) and DTC transfers it automatically to and from the CRB register. See section 17.3.1. Allocating Transfer Information and DTC Vector Table.

17.2.8 DTCCR : DTC Control Register

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable 0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

17.2.9 DTCCR_SEC : DTC Control Register for secure Region

Base address: DTC = 0x4000_5400

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 1. The write value should be 1.	R/W
4	RRS	DTC Transfer Information Read Skip Enable for Secure 0: Transfer information read is not skipped. 1: Transfer information read is skipped when vector numbers match.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: Secure access is allowed. Non-secure access is read-only.

RRS bit (DTC Transfer Information Read Skip Enable for Secure)

The RRS bit enables skipping of transfer information reads when vector numbers match. The DTC vector number is compared with the vector number in the previous activation process. When these vector numbers match and the RRS bit is

不能直接从CPU访问CRB。但是，CPU可以访问SRAM区域（传输信息(n)起始地址+0x0C），并且DTC会自动将其传输到CRB寄存器或从CRB寄存器传输。请参阅第17.3.1节。分配传输信息和DTC向量表。

17.2.8 DTCCR:DTC控制寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	RRS	DTC传输信息读取跳过启用 0：不跳过传输信息读取1：当向量编号匹配时，跳过传输信息读取	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

RRS位（DTC传输信息读取跳过使能）

当向量编号匹配时，RRS位允许跳过传输信息读取。将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量编号匹配并且RRS位设置为1时，执行DTC数据传输而不读取传输信息。但是，当前一次传输是链式传输时，无论RRS位如何，都会读取传输信息。

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位的值如何，都将读取传输信息。

17.2.9 DTCCR_SEC：安全区域的DTC控制寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RRS	—	—	—	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	—	该位读取为1。写入值应为1。	R/W
4	RRS	DTC传输信息读取跳过启用安全 0：不跳过读取的传输信息。1：当向量号匹配时跳过传输信息读取。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 允许安全访问。非安全访问是只读的。

RRS位（用于安全的DTC传输信息读取跳过启用）

当向量编号匹配时，RRS位允许跳过传输信息读取。将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量编号匹配且RRS位为

set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

17.2.10 DTCVBR : DTC Vector Base Register

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address Set the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

17.2.11 DTCVBR_SEC : DTC Vector Base Register for secure Region

Base address: DTC = 0x4000_5400

Offset address: 0x14

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC Vector Base Address for secure region Set DTC Vector Base Address for secure region. The lower 10 bits should be 0.	R/W

Note: Secure access is allowed. Non-secure access is read-only.

The DTCVBR_SEC sets the base address for calculating the DTC vector table address, which can be set in the range of 0x0000_0000 to 0xFFFF_FFFF (4 GB) in 1-KB units.

17.2.12 DTCST : DTC Module Start Register

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC Module Start 0: DTC module stopped 1: DTC module started	R/W

设置为1，执行DTC数据传输而不读取传输信息。但是，当前一次传输是链式传输时，无论RRS位如何，都会读取传输信息。

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位的值如何，都将读取传输信息。

17.2.10 DTCVBR:DTC向量基址寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	DTC向量基地址 设置DTC向量基地址。低10位应为0。	R/W

DTCVBR设置计算DTC向量表地址的基地址，可以设置在0x0000_0000到0xFFFF_FFFF(4GB)的范围内，以1KB为单位。

17.2.11 DTCVBR_SEC：安全区域的DTC向量基址寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x14

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	安全区域的DTC向量基地址 为安全区域设置DTC向量基地址。低10位应为0。	R/W

Note: 允许安全访问。非安全访问是只读的。

DTCVBR_SEC设置计算DTC向量表地址的基地址，可以设置在0x0000_0000到0xFFFF_FFFF(4GB)的范围内，以1-KB为单位。

17.2.12 DTCST:DTC模块启动寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTCST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DTCST	DTC模块启动 0：DTC模块停止1：DTC模块启动	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted. If this bit is set to 0 during a data transfer, the accepted transfer request is active until processing completes.

DTCST must be set to 0 before transitioning to one of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition.
- Deep Software standby mode

For details on these transitions, see section 17.10. Low Power Consumption Function and section 10, Low Power Modes.

17.2.13 DTCSTS : DTC Status Register

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-Activating Vector Number Monitoring These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
14:8	—	These bits are read as 0.	R
15	ACT	DTC Active Flag 0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the ACT flag is 1, indicating a DTC transfer in progress, and invalid if the ACT flag is 0, indicating no DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

Bit	Symbol	Function	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
● 忽略非安全写入访问，不会生成TrustZone访问错误。
如果安全属性配置为非安全：●
允许安全和非安全访问。

DTCST位（DTC模块启动）

将DTCST位设置为1以使DTC接受传输请求。当该位设置为0时，不再接受传输请求。如果在数据传输期间该位设置为0，则接受的传输请求将处于活动状态，直到处理完成。

在转换到以下状态或模式之一之前，必须将DTCST设置为0：

- Module-stop state
- ●没有贪睡模式转换的软件待机模式。
- ●深度软件待机模式

有关这些转换的详细信息，请参阅第17.10节。低功耗功能和第10节，低功耗模式。

17.2.13 DTCSTS:DTC状态寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ACT	—	—	—	—	—	—	—	VECN[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	VECN[7:0]	DTC-激活向量数量监测 当DTC传输正在进行时，这些位指示激活源的向量编号。该值仅在DTC传输正在进行（ACT标志为1）时有效。	R
14:8	—	这些位读为0。	R
15	ACT	DTC活动标志 0：未进行DTC传输操作1：正在进行DTC传输操作	R

VECN[7:0]位（DTC-激活向量编号监控）

当DTC进行传输时，VECN[7:0]位指示与传输激活源相关的向量编号。如果ACT标志为1，则从VECN[7:0]位读取的值有效，表示正在进行DTC传输，如果ACT标志为0，则表示无效，表示没有DTC传输正在进行。

ACT标志（DTC活动标志）

ACT标志指示DTC传输操作的状态。

[Setting condition]

●当DTC被传输请求激活时。

[Clearing condition]

●当DTC传输完成时，响应传输请求。

17.2.14 DTEVR : DTC Error Vector Register

Base address: DTC = 0x4000_5400

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTESTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTEVSAM	DTEV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DTEV[7:0]	DTC Error Vector Number These bits represent error vector of the DTC.	R
8	DTEVSAM	DTC Error Vector Number SA Monitor Indicates the SA of vector number causing the error. 0: Secure vector number 1: Non-Secure vector number	R
15:9	—	These bits are read as 0. The write value should be 0.	R
16	DTESTA	DTC Error Status Flag 0: No DTC transfer error occurred 1: DTC transfer error occurred	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R

Note: Writing to DTESTA depends on the value of DTEVSAM

DTEV[7:0] bit (DTC Error Vector Number)

When a transfer error due to DTC transfer occurs, it stores the channel of DTC that was violated.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DTC transfer error occurs and DTESTA = 0.

[Clearing condition]

- When 1 is written to DTEVR.DTESTA.

DTEVSAM bit (DTC Error Vector Number SA Monitor)

When a transfer error due to DTC transfer occurs, it indicates the SA of the violating DTC vector number.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DTC transfer error occurs and DTESTA = 0.

[Clearing condition].

- When 1 is written to DTEVR.DTESTA.

DTESTA bit (DTC Error Status Flag)

Indicates whether or not a DTC transfer error occurred.

DTEV, DTEVSAM, DTESTA are cleared by writing 1 to DTESTA.

17.2.14 DTEVR:DTC错误向量寄存器

Base address: DTC = 0x4000_5400

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DTESTA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DTEVSAM	DTEV[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DTEV[7:0]	DTC错误向量编号 这些位代表DTC的误差向量。	R
8	DTEVSAM	DTC错误向量编号SA监视器 指示导致错误的向量号的SA。 0：安全向量编号1：非安全向量编号	R
15:9	—	这些位被读取为0。写入值应为0。	R
16	DTESTA	DTC错误状态标志 0：未发生DTC传输错误1：发生DTC传输错误	R/W
31:17	—	这些位被读取为0。写入值应为0。	R

Note: 写入DTESTA取决于DTEVSAM的值

DTEV[7:0]位（DTC错误向量编号）

当由于DTC传输而发生传输错误时，它会存储违反的DTC通道。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DTC传输错误且DTESTA=0时。

[Clearing condition]

●当1写入DTEVR.DTESTA时。

DTEVSAM位（DTC错误向量编号SA监视器）

当由于DTC传输而发生传输错误时，它指示违规DTC向量号的SA。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DTC传输错误且DTESTA=0时。

[Clearing condition].

●当1写入DTEVR.DTESTA时。

DTESTA位（DTC错误状态标志）

指示是否发生DTC传输错误。

DTEV、DTEVSAM、DTESTA通过向DTESTA写入1清零。

Writing 0 to DTESTA is ignored.

When reset was selected in MPU.MMPUOAD.OAD and TZF.TZFOAD.OAD, Since this register is also reset. Please select NMI when you want to debug the program.

[Set condition]

- When the DMAC transfer error occurs.

[Clearing condition]

- When 1 is written to DTEVR.DTESTA.

Note: When DTEVSAM = 1, it can be cleared in the secure state and non-secure state. DTEVSAM = 0, it cannot be cleared in the non-secure state.

17.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 95. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number *n* is selected in ICU.IELSRn.IELS[8:0] where n = 0 to 95, as listed in section 13.3.2. Event Number in section 13, Interrupt Controller Unit (ICU). For activation by software, see section 18.2.2. ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepted an activation request, it does not accept another activation request until transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DTC transfer, a highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC Module Start bit (DTCST.DTCST) is 0, the DTC accepts the highest priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR flag of the activation source is set to 0 at the start of the data transfer.

17.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

DTC has two vector tables, non-secure side or secure side. Because the interrupt vector number that serves as a trigger for DTC is divided into non-secure or secure. Place the vector table of the interrupt vector number of SA = 1 in DTCVBR which is the non-secure side. Place the vector table of interrupt number SA = 0 in DTCVBR_SEC which is the secure side.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information *n* with vector number *n* must be 4n added to the base address in the vector table.

Figure 17.2 shows the relationship between the DTC vector table and transfer information. Figure 17.3 shows the allocation of transfer information in the SRAM area.

将0写入DTESTA将被忽略。

当在MPU.MMPUOAD.OAD和TZF.TZFOAD.OAD中选择了复位时，由于该寄存器也被复位。请选择NMI当你想调试程序时。

[Set condition]

●发生DMAC传输错误时。

[Clearing condition]

●当1写入DTEVR.DTESTA时。

Note: 当DTEVSAM=1时，可以在安全状态和非安全状态下清零。DTEVSAM=0，在非安全状态下不能清零。

17.3 激活源

DTC由中断请求激活。将ICU.IELSRn.DTCE位设置为1可以通过相关中断激活DTC。ICU.IELSRn中设置的选择器输出n个数被定义为中断向量号，其中n=0到95。对于一个使能的中断，在ICU.IELSRn.IELS中选择与每个中断向量号n相关的特定DTC中断源[8:0]其中n=0到95，如第13.3.2节中所列。第13节，中断控制器单元(ICU)中的事件编号。关于通过软件激活，请参见第18.2.2节。ELSEGRn：事件链接软件事件生成寄存器n(n=0 1)。

中断向量编号相当于DTC向量表编号。在DTC接受激活请求后，它不会接受另一个激活请求，直到该单个请求的传输完成，无论请求的优先级如何。如果在DTC传输期间生成多个激活请求，则在传输完成时接受最高优先级的请求。当DTC模块起始位(DTCST.DTCST)为0时产生多个激活请求时，当DTCST.DTCST随后设置为1时，DTC接受最高优先级请求。较小的中断向量编号具有较高的优先级。

DTC在单次数据传输开始时执行以下操作，或者对于链式传输，在最后一次连续传输之后执行以下操作：

●完成指定轮次的数据传输后，ICU.IELSRn.DTCE位设置为0，并向CPU发送中断请求

●如果MRB.DISEL位为1，则在数据传输完成时向CPU发送中断请求

●对于其他传输，激活源的ICU.IELSRn.IR标志在数据传输开始时设置为0。

17.3.1 分配传输信息和DTC向量表

DTC从向量表中读取与每个激活源相关联的传输信息的起始地址，并读取从该地址开始的传输信息。

DTC有两个向量表，非安全端或安全端。因为作为DTC触发的中断向量号分为非安全和安全。将SA=1的中断向量号的向量表放在非安全端DTCVBR中。将中断号SA=0的向量表放在安全侧DTCVBR_SEC中。

向量表的定位必须使基地址（起始地址）的低10位为0。使用DTC向量基址寄存器(DTCVBR)设置DTC向量表的基地址。传输信息分配在SRAM区域中。在SRAM区域中，向量编号为n的传输信息n的起始地址必须与向量表中的基地址相加4n。

图17.2显示了DTC向量表和传输信息之间的关系。图17.3显示了SRAM区域中传输信息的分配。

IELSRn setting example

ICU.IELSRn setting	SA
IELSR0	0
IELSR1	1
IELSR2	0
IELSR3	1
IELSR4	1
. . .	
IELSRn	0

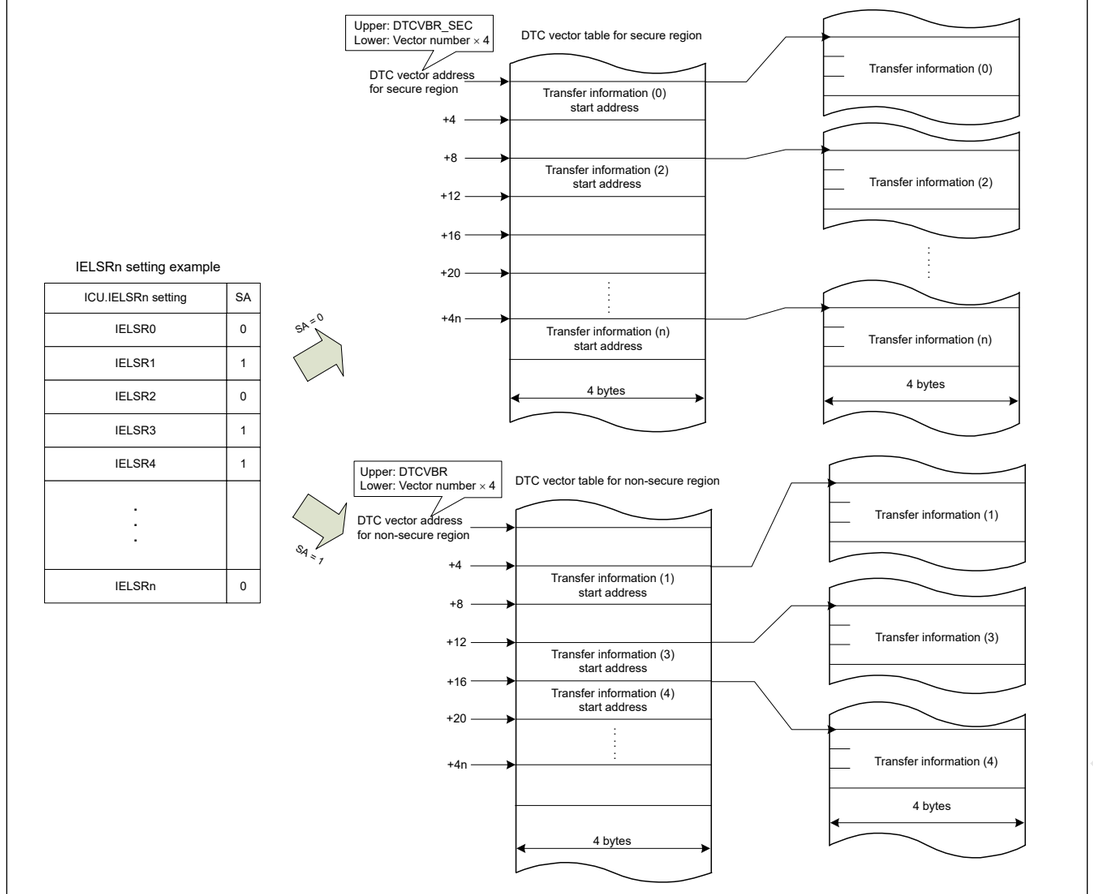


Figure 17.2 DTC vector table and transfer information

IELSRn设置示例

ICU.IELSRn setting	SA
IELSR0	0
IELSR1	1
IELSR2	0
IELSR3	1
IELSR4	1
. . .	
IELSRn	0

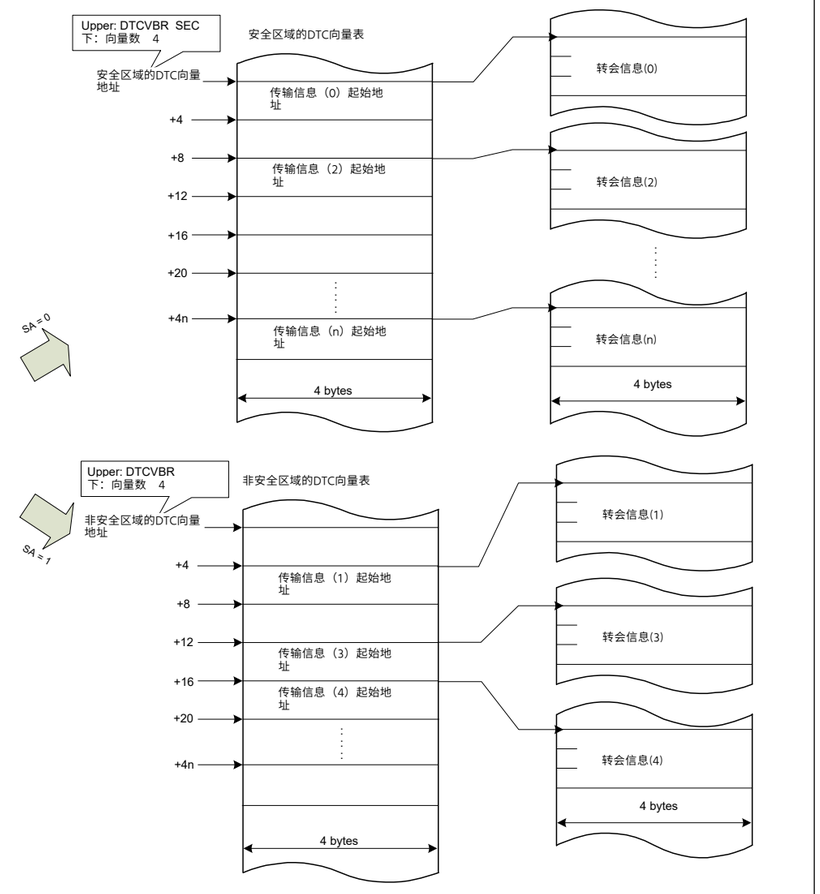


Figure 17.2 DTC向量表和传输信息

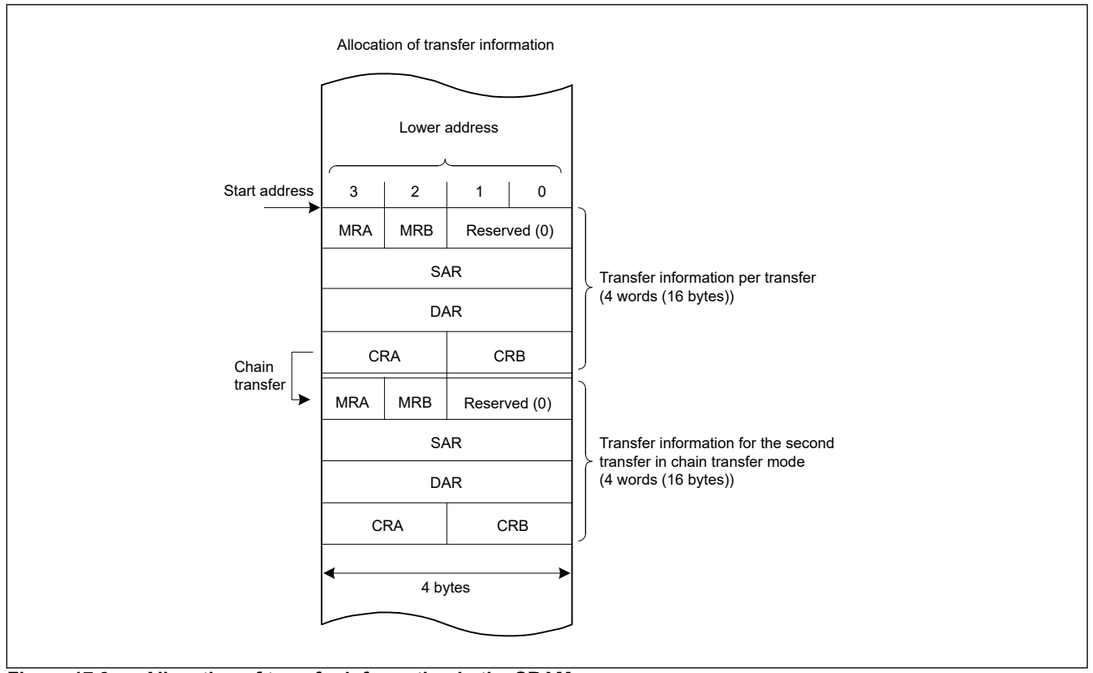


Figure 17.3 Allocation of transfer information in the SRAM area

17.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

The transfer modes include:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values of these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 17.2 describes the DTC transfer modes.

Table 17.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte (8 bit), 1 halfword (16 bit), 1 word (32 bit)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set the transfer source or transfer destination as the repeat area.
Note 2. Set the transfer source or transfer destination as the block area.

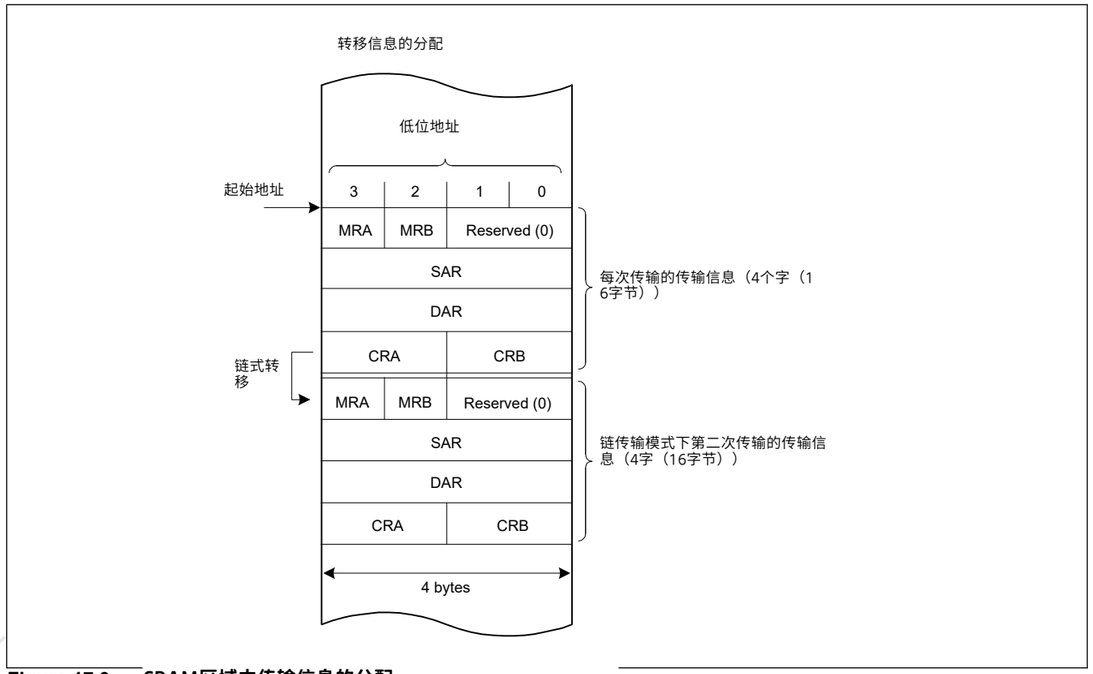


Figure 17.3 SRAM区域中传输信息的分配

17.4 Operation

DTC根据传输信息传输数据。在进行DTC操作之前，需要在SRAM区域中存储传输信息。当DTC被激活时，它会读取与向量编号相关联的DTC向量。DTC从DTC向量引用的传输信息存储地址中读取传输信息并传输数据。数据传输后，DTC写回传输信息。将传输信息存储在SRAM区域中可以实现任意数量的通道的数据传输。

传输模式包括：

- ●普通传输模式
- ●重复传输模式
- ●块传输模式。

DTC指定SAR寄存器中的传输源地址和DAR寄存器中的传输目标地址。这些寄存器的值在数据传输后独立地递增、递减或固定地址。

表17.2描述了DTC传输模式。

Table 17.2 DTC传输模式

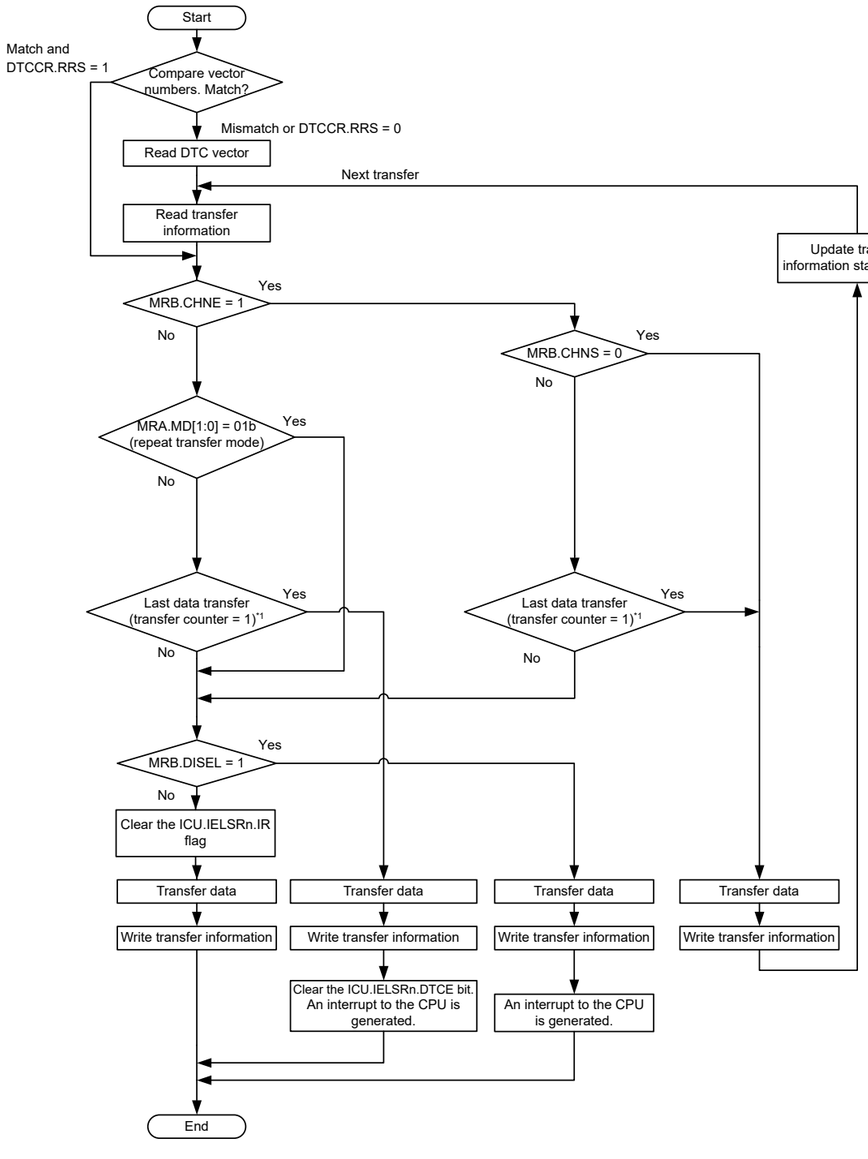
传输模式	在单个传输请求上传输的数据大小	内存地址的递增或递减	可设置的传输次数
正常传输模式	1个字节（8位）、1个半字（16位）、1个字（32位）	递增或递减1、2或4或固定地址	1 to 65536
重复传输模式*1	1个字节（8位）、1个半字（16位）、1个字（32位）	递增或递减1、2或4或固定地址	1 to 256*3
块传输模式*2	CRAH中指定的块大小（1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节））	递增或递减1、2或4或固定地址	1 to 65536

注1.将传输源或传输目标设置为重复区域。注2.将传输源或传输目标设置为块区域。

Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

Setting the MRB.CHNE bit to 1 allows multiple transfers or chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 17.4 shows the operation flow of the DTC. Table 17.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.



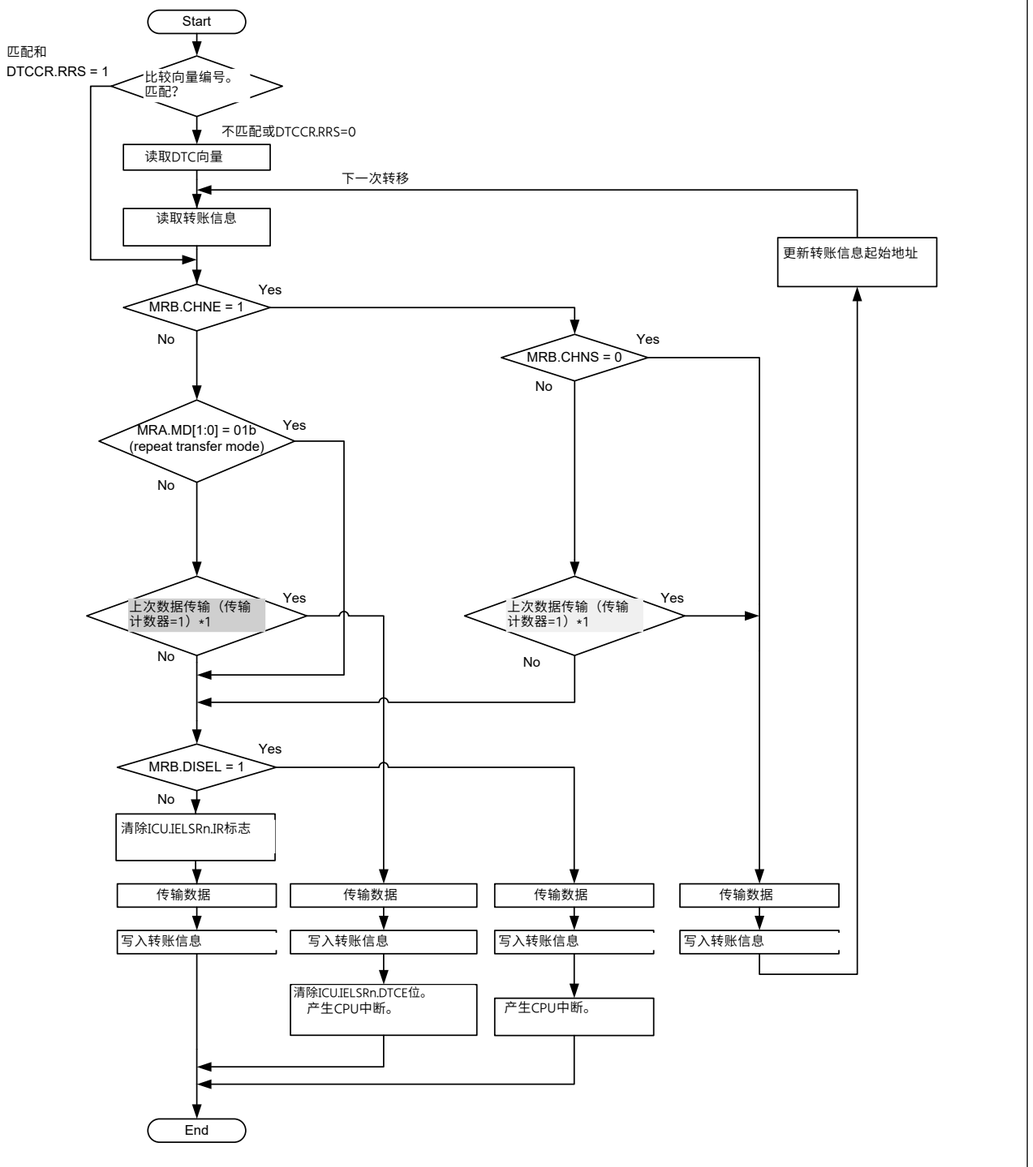
Note 1. Counter value before starting data transfer.

Figure 17.4 DTC operation flow

注3.指定计数的数据传输后，恢复初始状态并重新开始操作。

将MRB.CHNE位设置为1允许在单个激活源上进行多次传输或链式传输。当指定的数据传输完成时，它还启用链式传输。

图17.4显示了DTC的操作流程。表17.3列出了链转移条件。该表中省略了用于第二次和后续传输的控制信息的组合。



注1.开始数据传输前的计数器值。

Figure 17.4 DTC操作流程

Table 17.3 Chain transfer conditions

First transfer				Second transfer*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1 *2	
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE = 1 is omitted.

17.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared with the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, and when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the RRS bit. Figure 17.12 shows an example of a transfer information read skip.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, then set the RRS bit to 1. The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

17.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 17.4 lists the transfer information write-back skip conditions and the associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 17.3 链转移条件

首次转让				二次转让*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	转帐计数器*1*2	CHNE bit	CHNS bit	DISEL bit	转帐计数器*1*2	
0	—	0	（1→0）以外	—	—	—	—	在第一次传输后结束
0	—	0	(1 → 0)	—	—	—	—	在第一次传输后结束，向CPU发出中断请求
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	0	(1→*)以外	—	—	—	—	在第一次传输后结束
1	1	—	(1 → *)	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	1	(1→*)以外	—	—	—	—	在第一次传输后结束，向CPU发出中断请求

注1.使用的传输计数器取决于传输模式，如下所示：
正常传输模式—CRA寄存器重复传输模式—CRAL寄存器
块传输模式——CRB寄存器

注2.数据传输完成后，计数器操作如下：1→0在正常和块传输模式下1→CRAH在重复传输模式下(1→*)表中表示这两种操作，取决于模式。

注3.第二次及以后的转账可选择链式转账。省略了二次传输和CHNE=1的组合条件。

17.4.1 传输信息读取跳过功能

通过设置DTCCR.RRS位可以跳过向量地址和传输信息的读取。当产生DTC激活请求时，将当前DTC向量编号与之前激活过程中的DTC向量编号进行比较。当这些向量编号匹配且RRS位设置为1时，执行DTC数据传输而不读取向量地址和传输信息。但是，当上一次传输是链式传输时，会读取向量地址和传输信息。此外，如果在上次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位如何，都将读取传输信息。图17.12显示了传输信息读取跳过的示例。

要更新向量表和传输信息，请将RRS位设置为0，更新向量表和传输信息，然后将RRS位设置为1。通过将RRS位设置为0，丢弃存储的向量编号。更新的DTC向量在下一个激活过程中读取表和传输信息。

17.4.2 传输信息回写跳过功能

当MRA.SM[1:0]位或MRB.DM[1:0]位设置为地址固定时，部分传输信息不会被写回。表17.4列出了传输信息回写跳过条件和相关寄存器。回写CRA和CRB寄存器，跳过回写MRA和MRB寄存器。

Table 17.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR register	DAR register
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

17.4.3 Normal Transfer Mode

The normal transfer mode allows a 1-byte (8 bit), 1-halfword (16 bit), 1-word (32 bit) data transfer on a single activation source. The transfer count can be set to 1 to 65536. Transfer source and destination addresses can be independently set to increment, decrement, or fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 17.5 lists register functions in normal transfer mode, and Figure 17.5 shows the memory map of normal transfer mode.

Table 17.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

Table 17.4 传输信息回写跳过条件和适用寄存器

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR寄存器	DAR寄存器
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

17.4.3 正常传输模式

正常传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）、1字（32位）数据。传输计数可以设置为1到65536。传输源地址和目标地址可以独立设置为递增、递减或固定。此模式允许在指定计数传输结束时向CPU生成中断请求。

表17.5列出了正常传输模式下的寄存器功能，图17.5显示了正常传输模式下的内存映射。

Table 17.5 正常传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	递增、递减或固定*1
DAR	转移目的地地址	递增、递减、固定*1
CRA	转帐柜台A	CRA - 1
CRB	转帐柜台B	未更新

注1.在地址固定模式下会跳过回写操作。

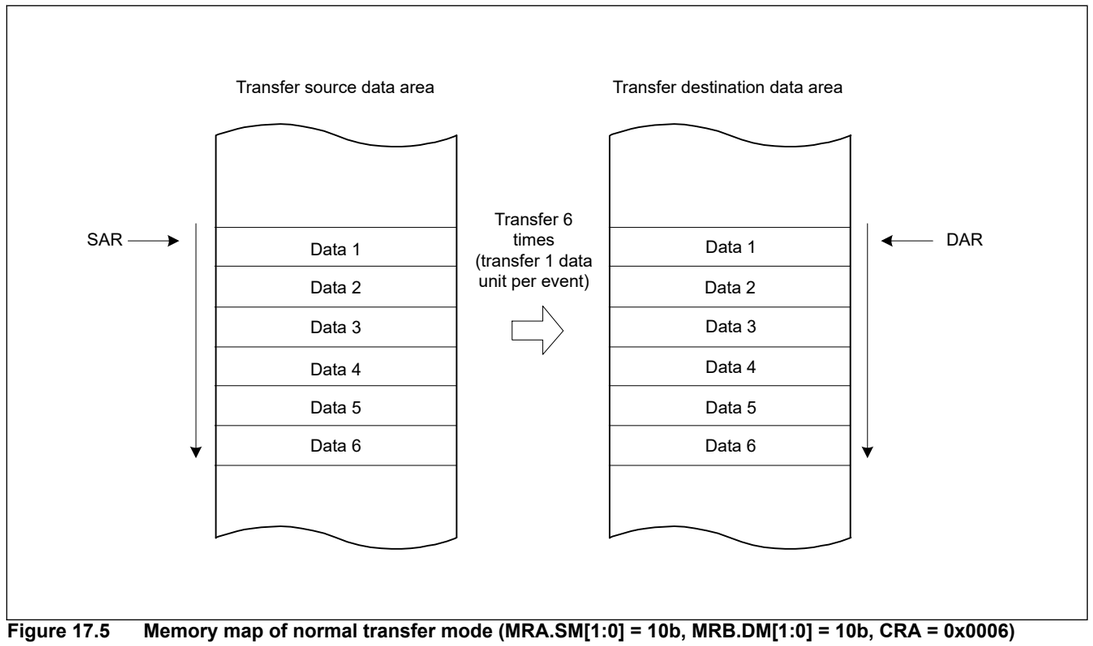


Figure 17.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0x0006)

17.4.4 Repeat Transfer Mode

The repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Transfer source or transfer destination for the repeat area must be specified in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified transfer count is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 0x00 in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not clear to 0x00, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer completes.

Table 17.6 lists the register functions in repeat transfer mode, and Figure 17.6 shows the memory map of repeat transfer mode.

Table 17.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	When CRAL is 1
SAR	Transfer source address	Increment, decrement, fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed*1
CRAH	Retains transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

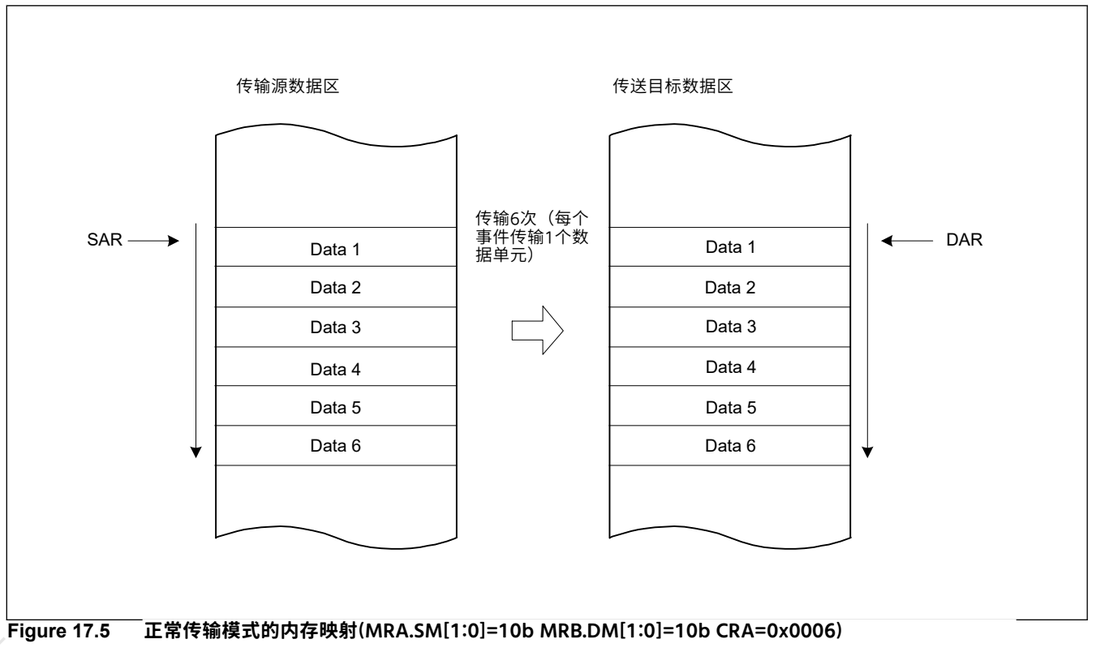


Figure 17.5 正常传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRA=0x0006)

17.4.4 重复传输模式

重复传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）或1字（32位）数据。重复区域的传输源或传输目标必须在MRB.DTS位中指定。传输计数可设置为1到256。当指定的传输计数完成时，将恢复重复区域中指定的地址寄存器的初始值，恢复传输计数器的初始值，并重复传输。另一个地址寄存器连续递增或递减或保持不变。

当传输计数器CRAL在重复传输模式下递减到0x00时，CRAL值将更新为CRAH寄存器中设置的值。因此，传输计数器不会清为0x00，这会在MRB.DISEL位设置为0时禁用对CPU的中断请求。当指定的数据传输完成时，会向CPU发出中断请求。

表17.6列出了重复传输模式下的寄存器功能，图17.6显示了重复传输模式的内存映射。

Table 17.6 重复传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值	
		当CRAL不为1时	当CRAL为1时
SAR	传输源地址	递增、递减、固定*1	• 当MRB.DTS位为0时 递增、递减或固定*1 • MRB.DTS位为1时 SAR寄存器初始值
DAR	转移目的地地址	递增、递减或固定*1	• 当MRB.DTS位为0时 DAR寄存器初始值 • MRB.DTS位为1时 递增、递减或固定*1
CRAH	保留转帐计数器	CRAH	CRAH
CRAL	转帐柜台A	CRAL - 1	CRAH
CRB	转帐柜台B	未更新	未更新

注1.在地址固定模式下会跳过回写。

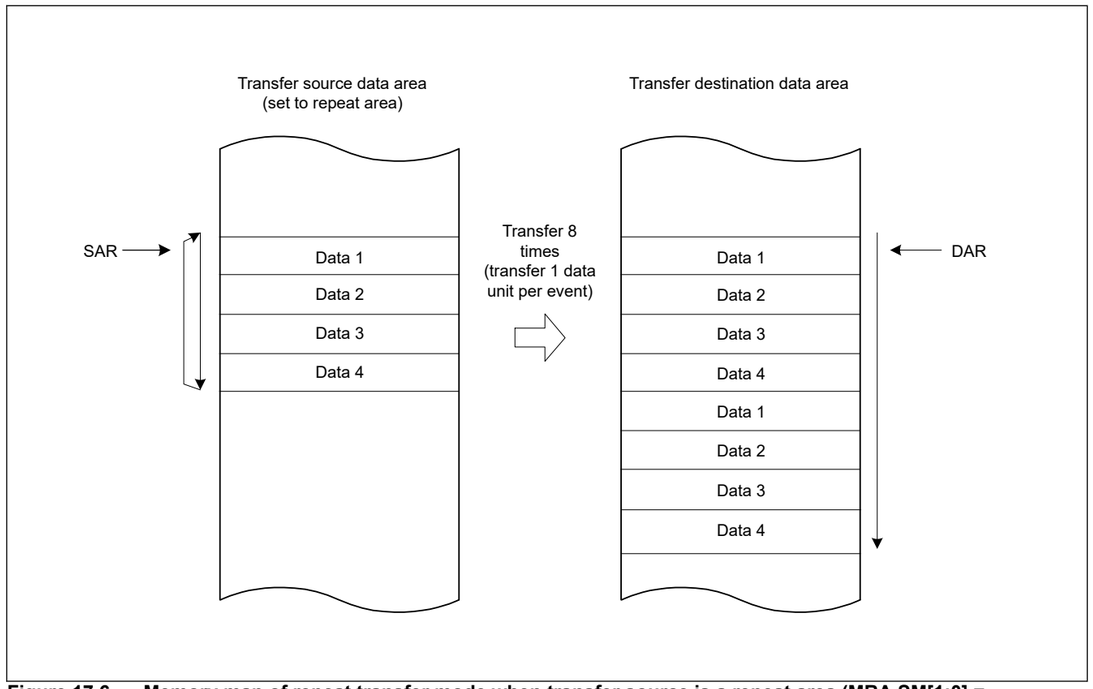


Figure 17.6 Memory map of repeat transfer mode when transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 0x04)

17.4.5 Block Transfer Mode

The block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS = 1 or the DAR register when the DTS = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 17.7 lists the register functions in block transfer mode, and Figure 17.7 shows the memory map for block transfer mode.

Table 17.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed*1.
CRAH	Holds block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

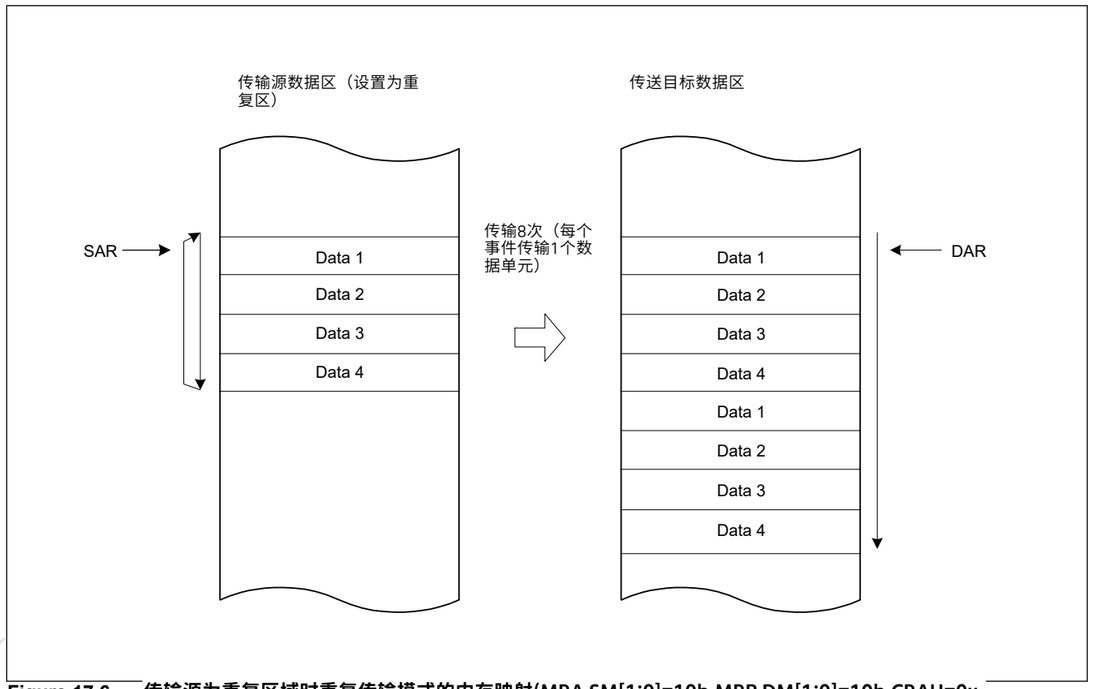


Figure 17.6 传输源为重复区域时重复传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRAH=0x04)

17.4.5 块传输模式

块传输模式允许在单个激活源上进行单块数据传输。块区域的传输源或传输目标必须在MRB.DTS位中指定。块大小可以设置为1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节）。当指定块的传送完成时，块区域中指定的块大小计数器CRAL和地址寄存器（MRB.DTS=1时为SAR寄存器或DTS=0时为DAR寄存器）的初始值被恢复。另一个地址寄存器连续递增或递减或保持不变。

传输计数（块计数）可设置为1到65536。此模式允许在指定计数块传输结束时向CPU生成中断请求。

表17.7列出了块传输模式下的寄存器功能，图17.7显示了块传输模式下的存储器映射。

Table 17.7 块传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	• 当MRB.DTS位为0时 递增、递减或固定*1 • 当MRB.DTS位为1时SAR 寄存器初始值。
DAR	转移目的地地址	• 当MRB.DTS位为0DAR寄 存器初始值 • 当MRB.DTS位为1时 递增、递减或固定*1。
CRAH	保持块大小	CRAH
CRAL	块大小计数器	CRAH
CRB	块传输计数器	CRB - 1

注1.在地址固定模式下会跳过回写。

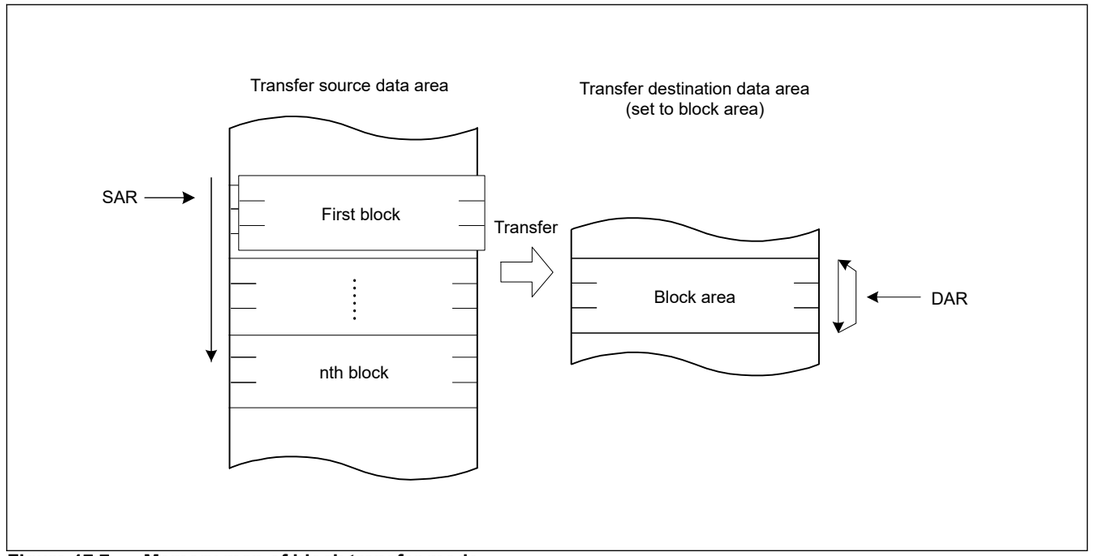


Figure 17.7 Memory map of block transfer mode

17.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If the MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR flag of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 17.8 shows a chain transfer operation.

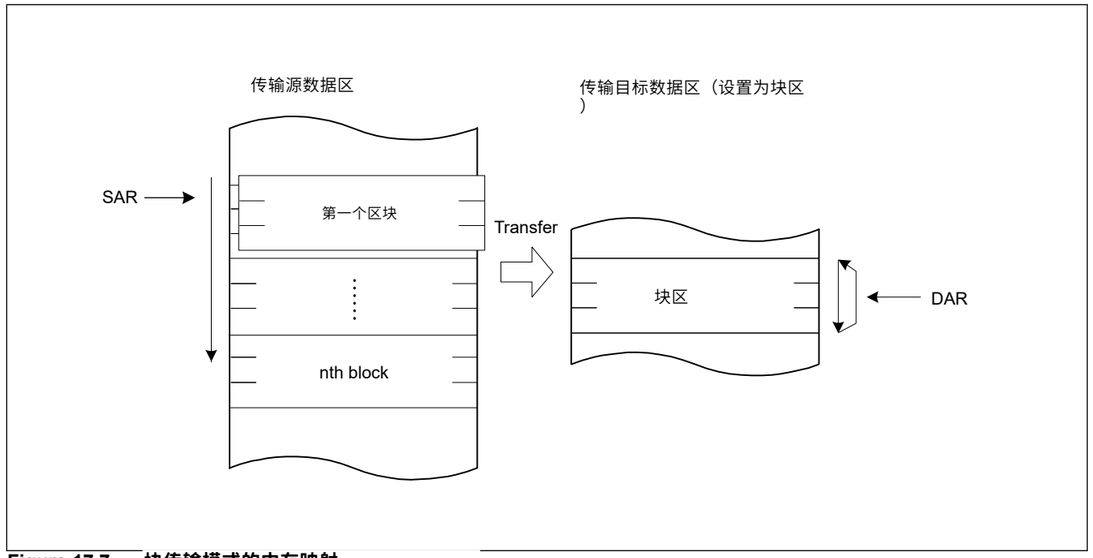


Figure 17.7 块传输模式的内存映射

17.4.6 链转移

将MRB.CHNE位设置为1允许在单个激活源上连续执行链传输。如果MRB.CHNE设置为1，CHNS设置为0，则在完成指定的传输轮数或将MRB.DISEL位设置为1时不会向CPU产生中断请求。中断请求被发送到每次执行DTC数据传输时CPU。数据传输对激活源的ICU.IELSRn.IR标志没有影响。

SAR、DAR、CRA、CRB、MRA和MRB寄存器可以相互独立设置以定义数据传输。
图17.8显示了链式转移操作。

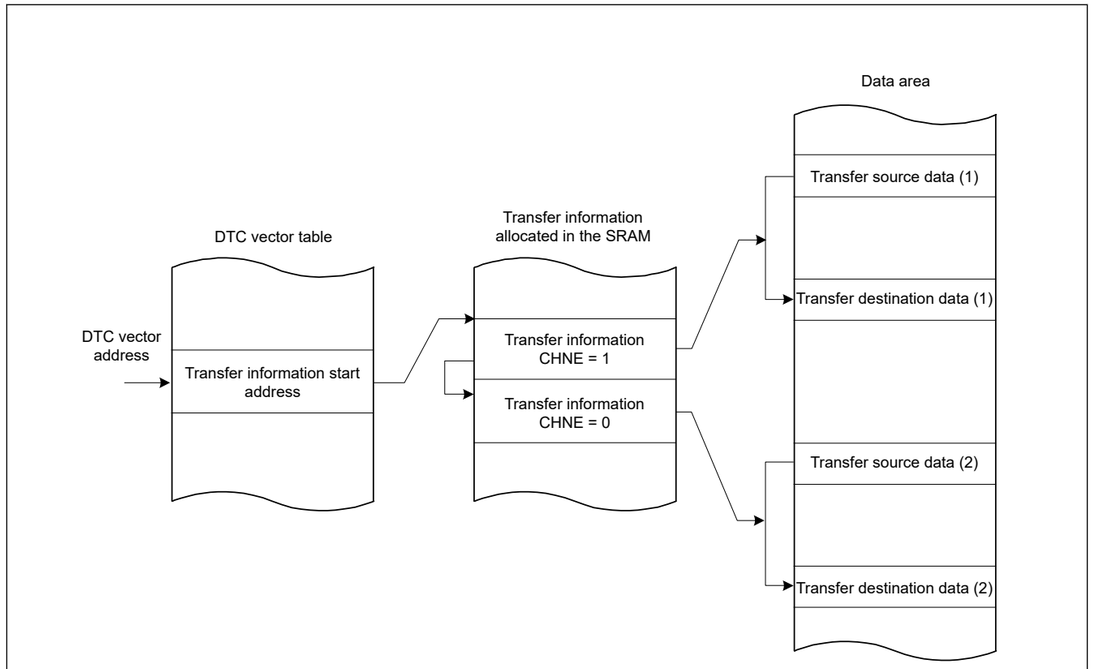


Figure 17.8 Chain transfer operation

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 17.2.

17.4.7 Operation Timing

Figure 17.9 to Figure 17.12 are timing diagrams that show the minimum number of execution cycles.

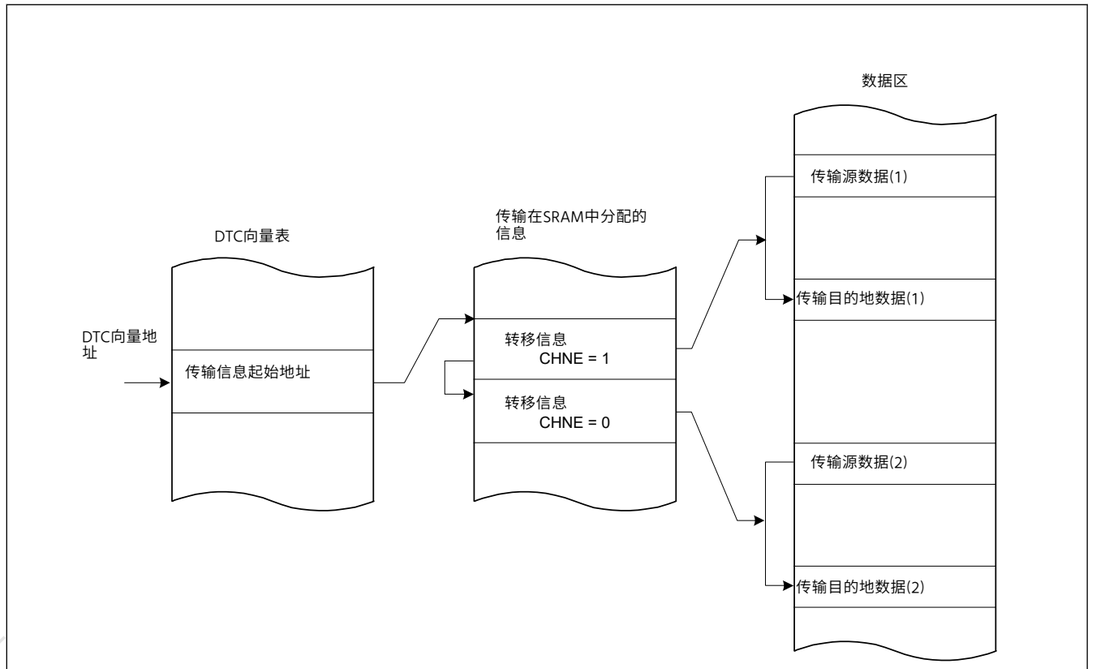


Figure 17.8 链转移操作

将1写入MRB.CHNE和CHNS位可以使链式传输仅在完成指定的数据传输后执行。在重复传输模式下，在完成指定的数据传输后执行链式传输。有关链转移条件的详细信息，请参见表17.2。

17.4.7 操作时间

图17.9至图17.12是显示最小执行周期数的时序图。

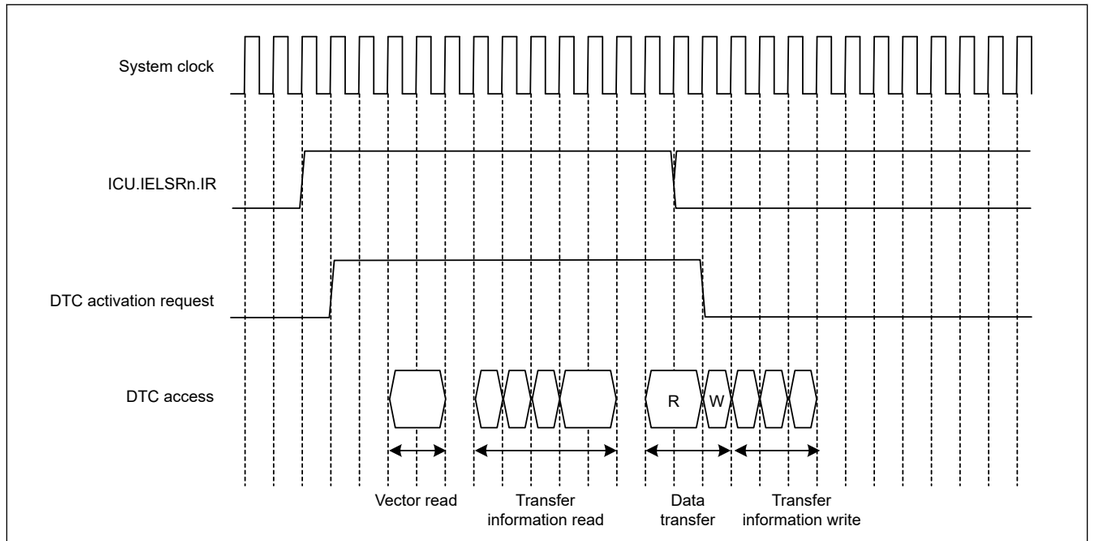


Figure 17.9 Example 1 of DTC operation timing in normal transfer and repeat transfer modes

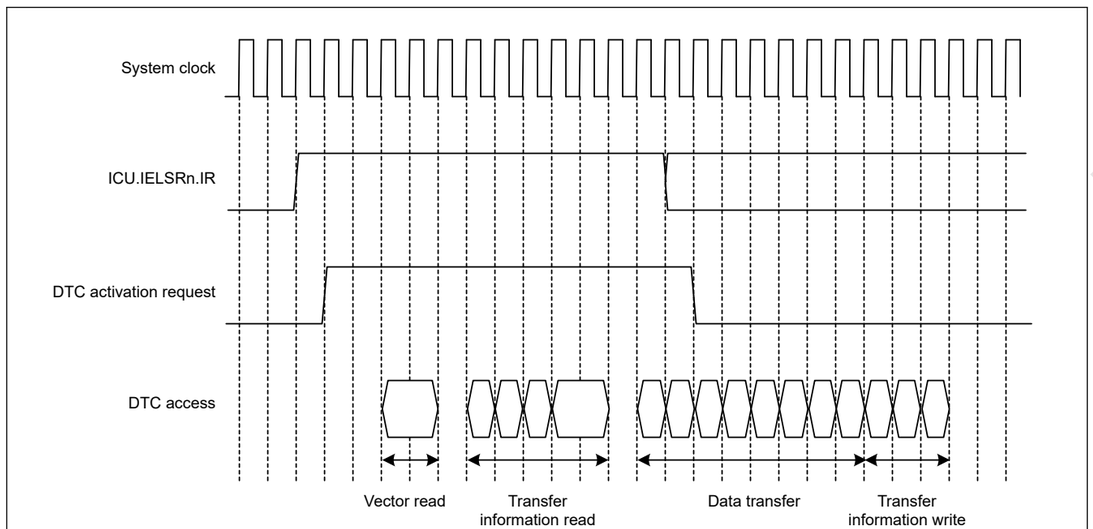


Figure 17.10 Example 2 of DTC operation timing in block transfer mode when the block size = 4

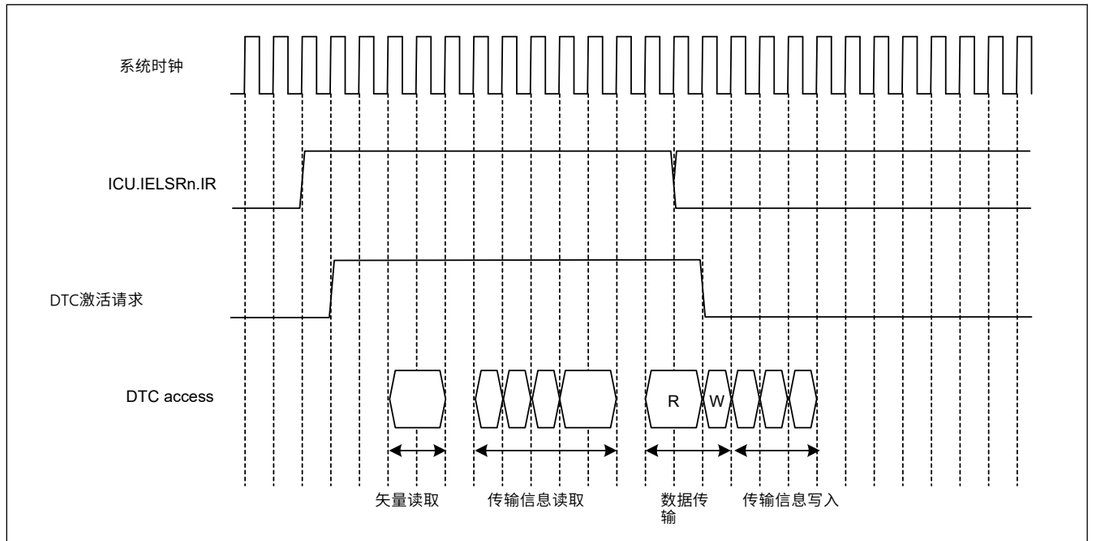


Figure 17.9 正常传输和重复传输模式下的DTC操作时序示例1

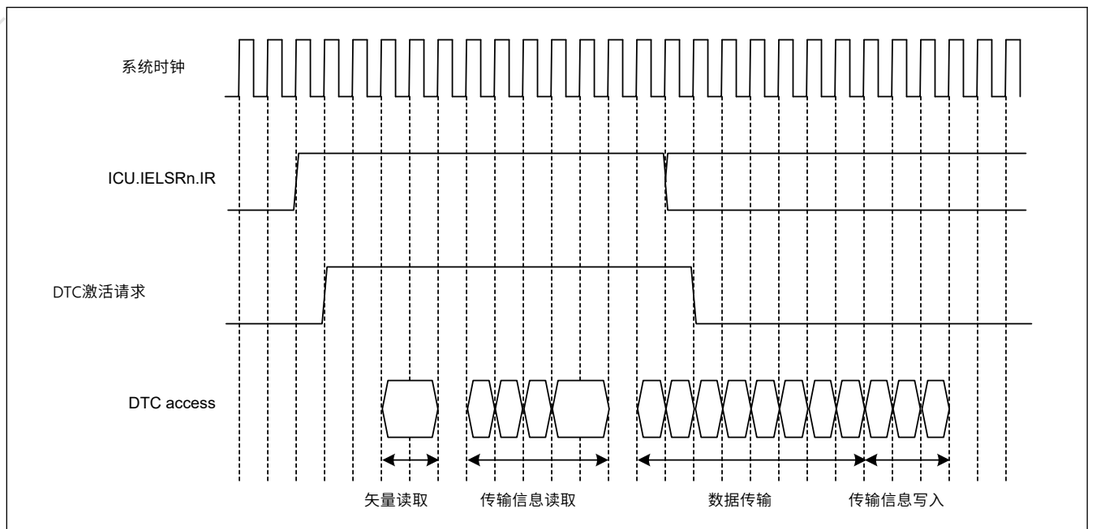


Figure 17.10 块大小=4时块传输模式下的DTC操作时序示例2

RA生态工作室

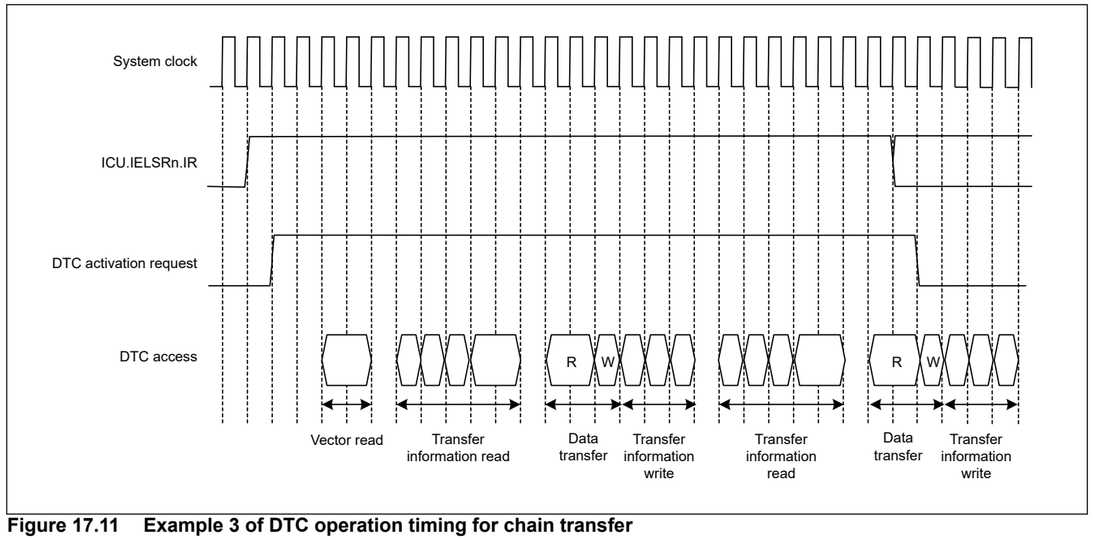
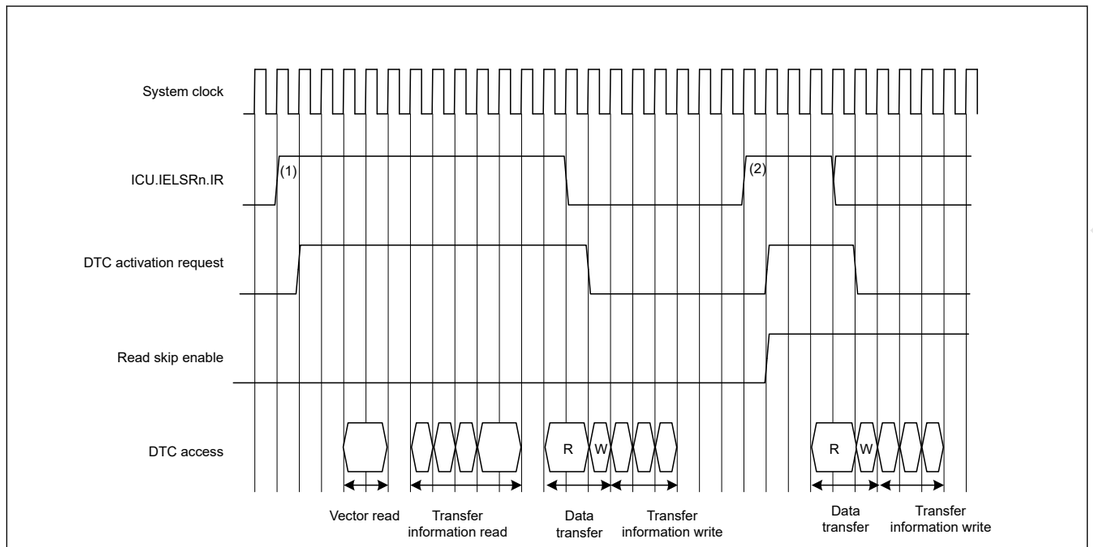


Figure 17.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS = 1, the transfer information read for request (2) is skipped.

Figure 17.12 Example of operation when a transfer information read is skipped with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

17.4.8 Execution Cycles of DTC

Table 17.8 lists the execution cycles of single data transfer of the DTC. For the order of the execution states, see section 17.4.7. Operation Timing.

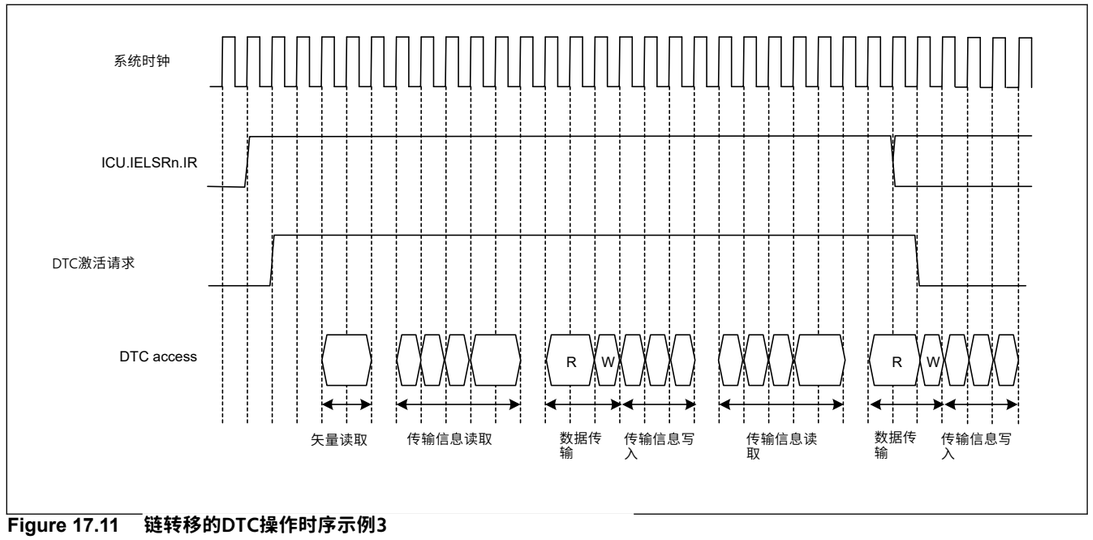
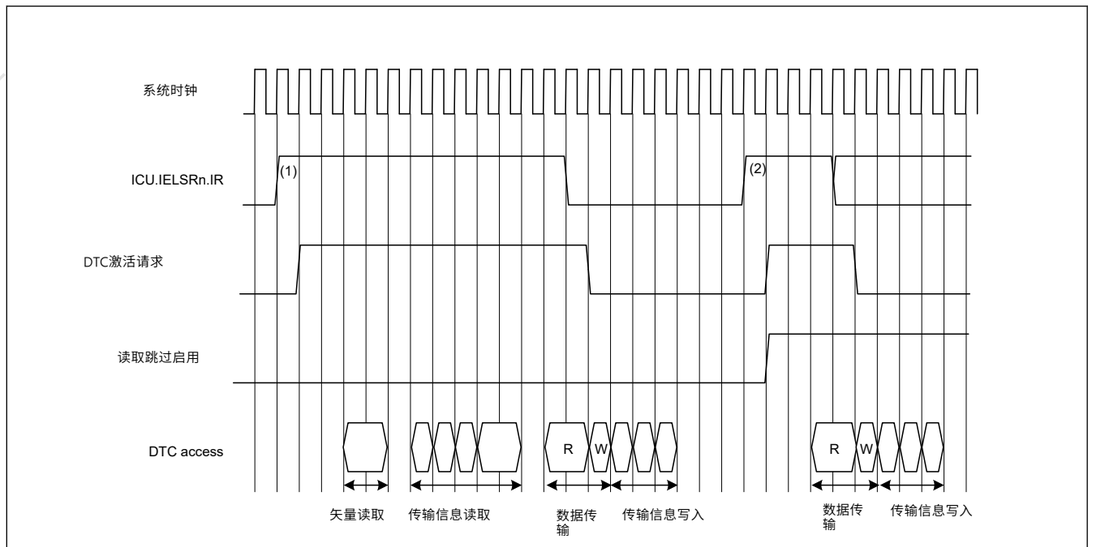


Figure 17.11 链转移的DTC操作时序示例3



Note: 当(1)和(2)的激活源(向量号)相同且RRS=1时，跳过请求(2)读取的传输信息。

Figure 17.12 使用SRAM上的向量、传输信息和传输目标数据以及外围模块上的传输源数据跳过传输信息读取时的操作示例

17.4.8 DTC的执行周期

表17.8列出了DTC单次数据传输的执行周期。有关执行状态的顺序，请参见第17.4.7节。操作时间。

Table 17.8 Execution cycles of DTC

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
The unit is for system clocks (ICLK) + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 48, SRAM, section 50, Flash Memory, and section 14, Buses.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
Table 17.8 does not include the time until DTC data transfer starts after the DTC activation source becomes active.

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer applies.

17.4.9 DTC Bus Mastership Release Timing

The DTC does not release the bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 14, Buses.

17.4.10 Vector Security

The security attribute of transfer access of DTC vector n and security attribute of access to the IELSRn(n = 0 to 95) register of ICU are controlled by SAIELSRn bit of ICUSARx(x = G,H or I) registers in CPSCU. For details on the CPSCU.ICUSARx registers, see section 13, Interrupt Controller Unit (ICU).

When the CPSCU.ICUSARx.SAIELSRn bit is 0, transfer of DTC vector n is secure access for both read and write. At the same time, the IELSRn register are protected from a non-secure access.

When the CPSCU.ICUSARx.SAIELSRn bit is 1, transfer of DTC vector n is non-secure access for both read and write. At the same time, the IELSRn register are non-secure attributes.

Do not write to the CPSCU.ICUSARx.SAIELSRn bit while DTC transfer is enabled or a bus master is writing to the DTC registers of same channel.

section 17.3.1. Allocating Transfer Information and DTC Vector Table shows security attribute about each DTC vectors.

17.4.11 Master TrustZone Filter in DTC

DTC has the Master TrustZone Filter. The Master TrustZone Filter in DTC can detect the security areas of Flash area(code Flash and data Flash) and SRAM area(ECC / Parity RAM) defined by IDAU. When no-secure accesses those addresses, it detects the security violation. Access of violation address is not performed. Detected the error is handled as the Master TrustZone Filter error.

17.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Set the ICU.IELSRn.IELS[8:0] bits to 0 to disable the interrupt in the NVIC and follow the procedure in Table 17.9 to set the DTC.

Table 17.8 DTC的执行周期

P：块大小（CRAH和CRAL的初始设置）
Cv：访问向量传输信息存储目标的周期Ci：访问传输信息存储目标地址的周期
Cr：访问数据读取目标的周期Cw：访问数据写入目标的周期
单位为系统时钟(ICLK)+1在Vectorread、Transferinformationread和Datatransferread列中和2在内部操作列中。Cv、Ci、Cr和Cw根据相应的访问目的地而变化。有关各个访问目标的周期数，请参见第48节SRAM、第50节闪存和第14节总线。系统时钟和外设时钟的频率比也被考虑在内。

DTC响应时间是从检测到DTC激活源到DTC传输开始的时间。
表17.8不包括从DTC激活源激活到DTC数据传输开始的时间。

传输模式	矢量读取		传输信息读取		传输信息写入			数据传输		内部运作	
								Read	Write		
Normal	Cv + 1	0*1	4 × Ci + 1	0*1	3 × Ci + 1*2	2 × Ci + 1*3	Ci*4	Cr + 1	Cw + 1	2	0*1
Repeat								Cr + 1	Cw + 1		
Block*5								P × Cr	P × Cw		

注1.跳过传输信息读取时。
注2.当SAR和DAR均未设置为地址固定模式时。
注3.当SAR或DAR设置为地址固定模式时。
注4.当SAR和DAR设置为地址固定模式时。
注5.当块大小为2或更大时。如果块大小为1，则适用正常传输的周期数。

17.4.9 DTC总线主控释放时序

在传输信息读取期间，DTC不会释放总线主控权。在读取或写入传输信息之前，根据总线主仲裁器确定的优先级对总线进行仲裁。对于总线仲裁，请参见第14节，总线。

17.4.10 矢量安全

DTC向量n的传输访问的安全属性和对ICU的IELSRn(n=0到95)寄存器的访问的安全属性由CPSCU中ICUSARx(x=G H或I)寄存器的SAIELSRn位控制。有关CPSCU.ICUSARx寄存器的详细信息，请参见第13节，中断控制器单元(ICU)。

当CPSCU.ICUSARx.SAIELSRn位为0时，DTC向量n的传输对于读和写都是安全访问。同时，保护IELSRn寄存器免受非安全访问。

当CPSCU.ICUSARx.SAIELSRn位为1时，DTC向量n的传输对于读取和写入都是非安全访问。同时，IELSRn寄存器是非安全属性。

当DTC传输使能或总线主机正在写入同一通道的DTC寄存器时，请勿写入CPSCU.ICUSARx.SAIELSRn位。

第17.3.1节。分配传输信息和DTC向量表显示每个DTC向量的安全属性。

17.4.11 DTC中的主TrustZone过滤器

DTC具有MasterTrustZone过滤器。DTC中的MasterTrustZoneFilter可以检测IDAU定义的Flash区域（代码Flash和数据Flash）和SRAM区域（ECCParityRAM）的安全区域。当no-secure访问这些地址时，它会检测到安全违规。不执行违规地址的访问。检测到的错误作为MasterTrustZoneFilter错误处理。

17.5 DTC设置程序

在使用DTC之前，请设置DTC向量基址寄存器(DTCVBR)。将ICU.IELSRn.IELS[8:0]位设置为0以禁用NVIC中的中断，并按照表17.9中的程序设置DTC。

Table 17.9 DTC setting procedure

No.	Step Name	Description
1	Set the DTCCR*1.RRS bit to 0	Set the DTCCR*1.RRS bit to 0 to reset the transfer information read skip flag. After that, the transfer information read is not skipped while the DTC is activated. Be sure to specify this setting when the transfer information is updated.
2	Set transfer information (MRA, MRB, SAR, DAR, CRA, and CRB)	Allocate transfer information (MRA, MRB, SAR, DAR, CRA, and CRB) in the data area. To set transfer information, see section 17.2. Register Descriptions. To allocate transfer information, see section 17.3.1. Allocating Transfer Information and DTC Vector Table.
3	Set transfer information start addresses in the DTC vector table	Set the transfer information start addresses in the DTC vector table. To set the DTC vector table, see section 17.3.1. Allocating Transfer Information and DTC Vector Table.
4	Set the DTCCR*1.RRS bit to 1	Set the DTCCR*1.RRS bit to 1 to enable skipping of the second and subsequent transfer information read cycles for continuous DTC activation from the same interrupt source. The RRS bit can be set to 1, but if this is set during DTC transfer, it becomes valid from the next transfer.
5	Set the ICU.IELSRn.DTCE bit to 1. Set the ICU.IELSRn.IELS[8:0] as interrupt source. The interrupt should be enabled in the NVIC.	Set the ICU.IELSRn.DTCE bit to 1. Set ICU.IELSRn.IELS[8:0] as interrupt sources that trigger DTC. The interrupt must be enabled in the NVIC. See section 13.3.2. Event Number in section 13, Interrupt Controller Unit (ICU).
6	Set the enable bit for an activation source interrupt	Set the enable bit for the activation source interrupts to 1. When a source interrupt is generated, the DTC is activated. To set the interrupt source enable bit, see the settings for the modules that are to be the activation sources.
7	Set the DTCST.DTCST bit to 1	Set the DTC Module Start bit (DTCST.DTCST) to 1.

Note: The DTCST.DTCST bit can be set even if the setting for each activation source is not completed.
Note: When used in non-secure state, DTCSAR.DTCSTSA = 1 or DTCST.DTCST = 1 must be set.
Note 1. When used in secure state, access DTCCR_SEC instead of DTCCR.

17.6 Examples of DTC Usage

17.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE = 0 and MRB.DISEL = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of the SRAM area for data storage in the DAR register, and 128 (0x0080) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table settings

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS[8:0] as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the SCIn_RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

Table 17.9 DTC设置程序

No.	步骤名称	Description
1	将DTCCR*1.RRS位设置为0	将DTCCR*1.RRS位设置为0以重置传输信息读取跳过标志。之后，在激活DTC时不会跳过读取的传输信息。请务必在传输信息更新时指定此设置。
2	设置传输信息（MRA、MRB、SAR、DAR、CRA和CRB）	在数据区分配传输信息（MRA、MRB、SAR、DAR、CRA和CRB）。要设置传输信息，请参阅第17.2节。注册说明。要分配传输信息，请参阅第17.3.1节。分配传输信息和DTC向量表。
3	在DTC向量表中设置传输信息起始地址	在DTC向量表中设置传输信息起始地址。要设置DTC矢量表，请参见第17.3.1节。分配传输信息和DTC向量表。
4	将DTCCR*1.RRS位设置为1	将DTCCR*1.RRS位设置为1，以允许跳过第二个和后续传输信息读取周期，以便从同一中断源连续激活DTC。RRS位可以设置为1，但如果在DTC传输期间设置，则从下一次传输开始生效。
5	将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS[8:0]设置为中断源。应在NVIC中启用中断。	将ICU.IELSRn.DTCE位设置为1。将ICU.IELSRn.IELS[8:0]设置为触发的中断源故障诊断码。必须在NVIC中启用中断。请参阅第13.3.2节。第13节中的事件编号，中断控制器单元（ICU）。
6	设置激活源中断的使能位	将激活源中断的使能位设置为1。当产生源中断时，将激活DTC。要设置中断源使能位，请参见要成为激活源的模块的设置。
7	将DTCST.DTCST位设置为1	将DTC模块起始位(DTCST.DTCST)设置为1。

Note: 即使每个激活源的设置未完成，也可以设置DTCST.DTCST位。
Note: 在非安全状态下使用时，必须设置DTCSAR.DTCSTSA=1或DTCST.DTCST=1。
注1.在安全状态下使用时，访问DTCCR_SEC而不是DTCCR。

17.6 DTC使用示例

17.6.1 正常转移

本节提供从SCI接收128字节数据时的DTC用法及其应用示例。

(1) 传输信息设置

在MRA寄存器中，选择固定源地址（MRA.SM[1:0]=00b）、正常传输模式（MRA.MD[1:0]=00b）和字节大小传输（MRA.SZ[1:0]=00b）。在MRB寄存器中，指定目标地址的递增(MRB.DM[1:0]=10b)和单个中断的单个数据传输(MRB.CHNE=0和MRB.DISEL=0)。MRB.DTS位可以设置为任何值。在SAR寄存器中设置SCI的RDR寄存器地址，

SRAM区域用于DAR寄存器中的数据存储，以及CRA寄存器中的128(0x0080)。CRB寄存器可以设置为任何值。

(2) DTC向量表设置

RXI中断的传输信息的起始地址在DTC的向量表中设置。

(3) ICU设置和DTC模块激活

将ICU.IELSRn.DTCE位设置为1，并将ICU.IELSRn.IELS[8:0]设置为SCI中断。必须在NVIC中启用中断。将DTCST.DTCST位设置为1。

(4) SCI设置

通过将SCI中的SCR.RIE位设置为1来使能SCIn_RXI中断。如果在SCI接收操作期间发生接收错误，则接收停止。要管理此问题，请使用允许CPU接受接收错误中断的设置。

(5) DTC transfer

Each time a reception of 1 byte by the SCI is complete, an SCIn_RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an SCIn_RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

17.6.2 Chain transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for the GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPTm.GTCCRC register (m = 320 to 323, 164 to 169). For the second transfer, normal transfer mode is specified for transfer to the GPTm.GTCCRE register (m = 320 to 323, 164 to 169). For the third transfer of the chained transfer, normal transfer mode for transfer to the GPTm.GTPBR register (m = 320 to 323, 164 to 169) is specified. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE = 0.

The following example shows how to use the counter overflow interrupt with the GPT320.GTPR register as an activating source for the DTC.

(1) First transfer information setting

Set up transfer to the GPT320.GTCCRC register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information setting

Set up for transfer to the GPT320.GTCCRE register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1, MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information set

Set up transfer to the GPT320.GTPBR register.

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up single data transfer per interrupt (MRB.CHNE = 0, MRB.DISEL = 0). The MRB.DTS bit can be set to any value.

(5) DTC transfer

每次SCI完成1个字节的接收，就会产生一个SCIn_RXI中断来激活DTC。DTC将接收到的字节从SCI的RDR传输到SRAM，之后DAR寄存器递增，CRA寄存器递减。

(6) 中断处理

在128轮数据传输完成且CRA寄存器中的值变为0后，向CPU产生SCIn_RXI中断请求。完成该中断处理程序中的处理。

17.6.2 链式转移

本节提供了一个DTC链传输的示例，并描述了它在General输出脉冲中的使用
PWM定时器(GPT)。您可以使用链式传输来传输PWM定时器比较数据并更改GPT的PWM定时器的周期。

对于第一个链传输，指定正常传输模式以传输到GPTm.GTCCRC寄存器（m=320到323、164到169）。对于第二次传输，指定正常传输模式以传输到GPTm.GTCCRE寄存器（m=320到323、164到169）。对于链式传输的第三次传输，指定用于传输到GPTm.GTPBR寄存器（m=320至323、164至169）的正常传输模式。这是因为在完成指定数量的传输时清除激活源和产生中断仅限于链传输的第三个，即在MRB.CHNE=0时传输。

以下示例显示如何使用GPT320.GTPR寄存器的计数器溢出中断作为DTC的激活源。

(1) 首次转账信息设置

设置传输到GPT320.GTCCRC寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链传输（MRB.CHNE=1和MRB.CHNS=0）。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTCCRC寄存器的地址。

6.将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(2) 二转信息设置

设置传输到GPT320.GTCCRE寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链传输（MRB.CHNE=1，MRB.CHNS=0）。

4.将SAR寄存器设置为数据表的首地址。

5.将DAR寄存器设置为GPT320.GTCCRE寄存器的地址。

6.将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(3) 三转信息集

设置传输到GPT320.GTPBR寄存器。

1.在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。

2.将传输设置为正常传输模式（MRA.MD[1:0]=00b）和字长传输（MRA.SZ[1:0]=10b）。

3.在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置每次中断的单次数据传输（MRB.CHNE=0，MRB.DISEL=0）。MRB.DTS位可以设置为任何值。

4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT320.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(4) Transfer information assignment

Place the transfer information for use in the transfer to the GPT320.GTPBR immediately after the transfer control information for use in the GPT320.GTCCRC and GPT320.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT320.GTCCRC and GPT320.GTCCRE registers starts.

(6) ICU setting and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT320 counter overflow interrupt.
2. Set the ICU.IELSRn.IELS[8:0] bits and specify the GPT320 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT320.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT320.GTCCRA and GPT320.GTCCRB registers and the next PWM timer compare values in the GPT320.GTCCRC and GPT320.GTCCRE registers.
3. Set the default PWM timer period values in the GPT320.GTPR register and the next PWM timer period values in the GPT320.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the Peripheral Select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT320.GTSTR.CSTRT bits to 1 to start the GPT320.GTCNT counter.

(9) DTC transfer

Each time a GPT320 counter overflow is generated with the GPT320.GTPR register, the next PWM timer compare values are transferred to the GPT320.GTCCRC and GPT320.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT320.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT320 counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

17.6.3 Chain Transfer when Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 1-KB input buffer, where the input buffer is set so that its lower address starts with 0x00. Figure 17.13 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   (a) Transfer source address = fixed.
   (b) CRA register = 0x0200 (512) times.
   (c) MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).

4.将SAR寄存器设置为数据表的首地址。
5.将DAR寄存器设置为GPT320.GTPBR寄存器的地址。
6.将CRA寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(4) 转移信息分配

将用于传输到GPT320.GTPBR的传输信息放置在GPT320.GTCCRC和GPT320.GTCCRE寄存器中使用的传输控制信息之后。

(5) DTC向量表

在DTC向量表中，设置用于传输到GPT320.GTCCRC和GPT320.GTCCRE寄存器的传输控制信息的起始地址。

(6) ICU设置和DTC模块激活

1.设置与GPT320计数器溢出中断相关的ICU.IELSRn.DTCE位。
2.设置ICU.IELSRn.IELS[8:0]位并指定GPT320计数器溢出。
3.将DTCST.DTCST位设置为1。

(7) GPT settings

1.设置GPT320.GTIOR寄存器，使GTCCRA和GTCCRB寄存器作为输出比较寄存器运行。
2.在GPT320.GTCCRA和GPT320.GTCCRB寄存器中设置默认PWM定时器比较值，在GPT320.GTCCRC和GPT320.GTCCRE寄存器中设置下一个PWM定时器比较值。
3.在GPT320.GTPR寄存器中设置默认PWM定时器周期值，在GPT320.GTPBR寄存器中设置下一个PWM定时器周期值。
4.将PmnPFS.PDR中的输出位设置为1，并将PmnPFS.PSEL[4:0]中的外设选择位设置为00011b。

(8) GPT activation

将GPT320.GTSTR.CSTRT位设置为1以启动GPT320.GTCNT计数器。

(9) DTC transfer

每次使用GPT320.GTPR寄存器产生GPT320计数器溢出时，下一个PWM定时器比较值被传送到GPT320.GTCCRC和GPT320.GTCCRE寄存器。下一个PWM定时器周期的设置被传送到GPT320.GTPBR寄存器。

(10)中断处理

在指定轮次的数据传输完成后，例如当GPT传输的CRA寄存器中的值变为0时，会向CPU发出GPT320计数器溢出中断请求。在处理例程中完成该中断的处理。

17.6.3 Counter=0时的链式转移

仅当在第一次数据传输中将传输计数器设置为0时才执行第二次数据传输，并且在第二次传输中重复改变第一数据传输信息。链式转移使转移可以重复256次或更多。

以下过程显示了配置1KB输入缓冲区的示例，其中输入缓冲区设置为使其低地址从0x00开始。图17.13显示了当计数器=0时的链式传输。

1.将普通传输模式设置为第一次数据传输的输入数据。设置以下内容：
   (a) 传输源地址=固定。
   (b) CRA寄存器=0x0200(512)次。
   (c) MRB.CHNE位=1（启用链式传输）。
   (d) MRB.CHNS位=1（仅当传输计数器为0时才执行链式传输）。

(e) MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).

2. Prepare the upper 8-bit address of the start address at every 512 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 0x8000 to 0x83FF, prepare 0x82 and 0x80.
3. For the second data transfer:
   (a) Set the repeat transfer mode (with transfer source and destination address = fixed.) to reset the transfer counter of the first data transfer.
   (b) Specify the CRA register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 1 (chain transfer is enabled).
   (d) Set the MRB.CHNS bit = 0 (select continuous chain transfer).
   (e) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (f) CRA register = 0x0101 (The transfer count is 1).
4. For the third data transfer:
   (a) Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   (b) Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   (c) Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   (d) Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   (e) When setting the input buffer to 0x8000 to 0x83FF, also set the transfer counter to 2.
5. The first data transfer is performed by an interrupt 512 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
6. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x82. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
7. In succession, the first data transfer is performed by an interrupt 512 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the transfer counter of the first data transfer to 0x0200. The lower 8 bits of the transfer destination address and the transfer counter of the first data transfer becomes 0x0200.
8. The second data transfer is performed by an interrupt 1 times. When the transfer counter of the first data transfer becomes 0, the third data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 0x80. The lower 8 bits of the transfer destination address becomes 0x00 and the transfer counter of the first data transfer becomes 0x0200.
9. Steps 5 to 8 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

(e) MRB.DISEL位=0（指定数据传输完成时向CPU产生中断请求）。

2.在flash等不同区域的第一次数据传输中，每512次传输目标地址准备起始地址的高8位地址。比如设置输入缓冲区为0x8000到0x83FF时，准备0x82和0x80。

3.对于第二次数据传输：
   (a) 设置重复传输模式（传输源和目标地址=固定）以重置第一次数据传输的传输计数器。
   (b) 在传输目标的第一个传输信息区域中指定CRA寄存器。
   (c) 设置MRB.CHNE位=1（启用链式传输）。
   (d) 设置MRB.CHNS位=0（选择连续链传输）。
   (e) 设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   (f) CRA寄存器=0x0101（传输计数为1）。
4.对于第三次数据传输：
   (a) 设置重复传输模式（以源为重复区域）重置第一次数据传输的传输目标地址。
   (b) 在传输目标的第一个传输信息区域中指定DAR寄存器的高8位。
   (c) 设置MRB.CHNE位=0（禁用链传输）。
   (d) 设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   (e) 将输入缓冲区设置为0x8000到0x83FF时，还要将传输计数器设置为2。
5.第一次数据传输由中断执行512次。当第一次数据传输的传输计数器变为0，第二次数据传输开始。将第一次数据传输的传输计数器设置为0x0200。第一次数据传输的传输目标地址和传输计数器的低8位变为0x0200。

6.第二次数据传输由中断执行1次。当第一次数据传输的传输计数器变为0，开始第三次数据传输。将第一次数据传输的传输目标地址的高8位设置为0x82。传送目标地址的低8位变为0x00，第一次数据传送的传送计数器变为0x0200。

7.接连地，第一次数据传输由中断执行512次，如为第一次数据传输指定的那样。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输计数器设置为0x0200。第一次数据传输的传输目标地址和传输计数器的低8位变为0x0200。

8.第二次数据传输由中断执行1次。当第一次数据传输的传输计数器变为0，开始第三次数据传输。将第一次数据传输的传输目标地址的高8位设置为0x80。传送目标地址的低8位变为0x00，第一次数据传送的传送计数器变为0x0200。

9.步骤5到8无限重复。因为第二次数据传输是重复传输模式，所以不会产生对CPU的中断请求。

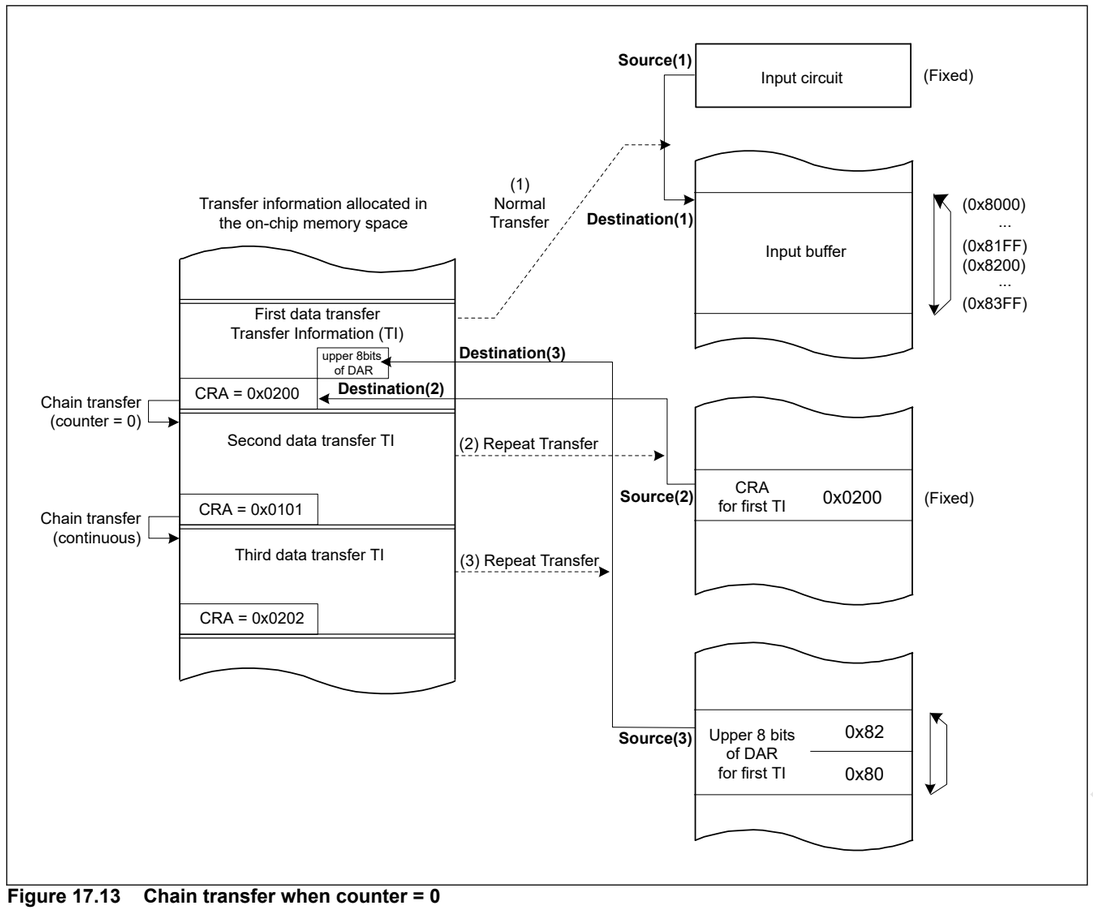


Figure 17.13 Chain transfer when counter = 0

17.7 Processing on DTC Transfer Error

If the access error occurs during DTC transfer, the DTC immediately stops access during transfer. To stop only the vector number that caused the error, inform the vector number that caused the error to the ICU and clear the corresponding ICU setting. After that, if there is a request other than the vector number which caused the error, it will be re-arbitration as it is. The condition under which the transfer error occurs is indicated when TrustZone Filter in DTC detects a violation.

The error response is informed to ICU when the transfer error occurs. ICU clears the ICU.IELSRn of the corresponding vector number which caused the transfer error. Furthermore, it generates an error response detection interrupt to notify that an error has occurred by DMAC/DTC transfer. (section 17.8.2. Interrupt Request of Transfer Error). Write back to SRAM is not performed.

When the Master TrustZone Filter error occurs, the Slave TrustZone error occurs or the Master MPU error occurs, it is possible to confirm the error information of DTC by selecting NMI. The DTC error vector register is cleared by selecting reset. Under the conditions where NMI is generated due to transfer error in DTC, two interrupts(NMI and DMAC_TRANSERR) are generated. In this case, NMI always responds first.

The error response detection interrupt request (DMA_TRANSERR) occurs when the Slave Bus error or the Illegal Access error occurs. Furthermore, it occurs after NMI when the error response detection interrupt request (DMA_TRANSERR) is not cleared in NMI handler.

section 17.7.1. Processing on NMI handler describes how to confirm the error information of the DTC in the NMI handler. section 17.7.2. Processing on Error response detection interrupt request (DMA_TRANSERR) handler describes how to confirm the error information of the DTC in the DMA_TRANSERR handler.

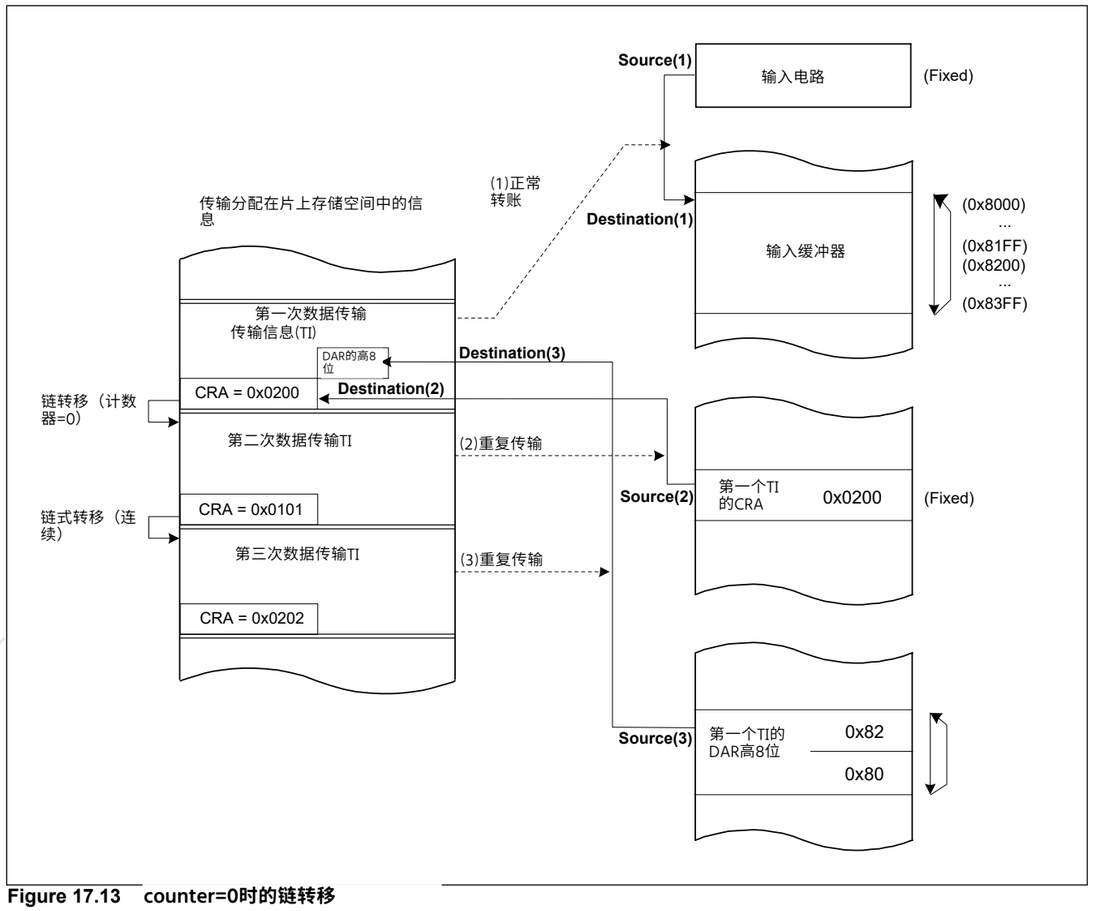


Figure 17.13 counter=0时的链转移

17.7 DTC传输错误的处理

如果在DTC传输过程中发生访问错误，则DTC会在传输过程中立即停止访问。要仅停止导致错误的向量编号，请将导致错误的向量编号通知ICU并清除相应的ICU设置。之后，如果有引起错误的向量号以外的请求，将按原样重新仲裁。当DTC中的TrustZone过滤器检测到违规时，会指示发生传输错误的条件。

当发生传输错误时，将错误响应通知给ICU。ICU清除导致传输错误的相应向量号的ICU.IELSRn。此外，它会生成错误响应检测中断，以通知DMACDTC传输发生错误。（第17.8.2节。传输错误的中断请求）。不执行回写到SRAM。

当MasterTrustZoneFilter发生错误、SlaveTrustZone错误或MasterMPU错误时，可以通过选择NMI来确认DTC的错误信息。通过选择复位清除DTC错误向量寄存器。在由于DTC中的传输错误而产生NMI的情况下，会产生两个中断（NMI和DMAC_TRANSERR）。在这种情况下，NMI总是首先响应。

当发生SlaveBus错误或IllegalAccess错误时，会发生错误响应检测中断请求(DMA_TRANSERR)。此外，当NMI处理程序中未清除错误响应检测中断请求(DMA_TRANSERR)时，它会在NMI之后发生。

第17.7.1节。NMIhandler上的处理描述了如何在NMIhandler中确认DTC的错误信息。第17.7.2节。错误响应检测中断请求(DMA_TRANSERR)处理程序的处理描述了如何在DMA_TRANSERR处理程序中确认DTC的错误信息。

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Interrupts and the error information generated due to transfer errors are shown in section 17.8.2. Interrupt Request of Transfer Error.

17.7.1 Processing on NMI handler

The cause of NMI due to the DMA transfer error is the Master TrustZone Filter error, the Slave TrustZone Filter error or the Master MPU error. When NMI occurs due to the DTC transfer error, the error response detection interrupt request (DMA_TRANSERR) will occur after the end of NMI handler. It is possible to confirm the cause of the error and the DTC vector number in which the error occurred. When NMI occurs, perform the necessary processing according to the flow described in the ICU chapter.

Figure 17.14 shows the flow for confirm the vector number that caused the Master TrustZone Filter Error in DTC

Figure 17.15 shows the flow for confirm the vector number that caused the Slave TrustZone Filter Error in DTC

Figure 17.16 shows the flow for confirm the vector number and Security Attribute that caused the Master MPU error in DTC

If completing all processing in NMI handler, it is possible to clear the error response detection interrupt request (DMA_TRANSERR) that occurs subsequently.

因传输错误而产生的中断和错误信息见17.8.2节。中断请求
传输错误。

17.7.1 在NMI处理程序上处理

由于DMA传输错误导致NMI的原因是MasterTrustZoneFilter错误、SlaveTrustZoneFilter错误或
主控MPU错误。当由于DTC传输错误而发生NMI时，错误响应检测中断请求(DMA_TRANSERR)将在NMI处理程序结束后发生。可以确认错误的原因和发生错误的DTC向量编号。当发生NMI时，按照ICU章节中描述的流程进行必要的处理。

图17.14显示了在DTC中确认导致MasterTrustZoneFilterError的向量号的流程

图17.15显示了在DTC中确认导致SlaveTrustZoneFilterError的向量号的流程

图17.16显示了确认导致MasterMPU错误的向量号和安全属性的流程
DTC

如果完成NMI处理程序中的所有处理，则可以清除随后发生的错误响应检测中断请求(DMA_TRANSERR
)。

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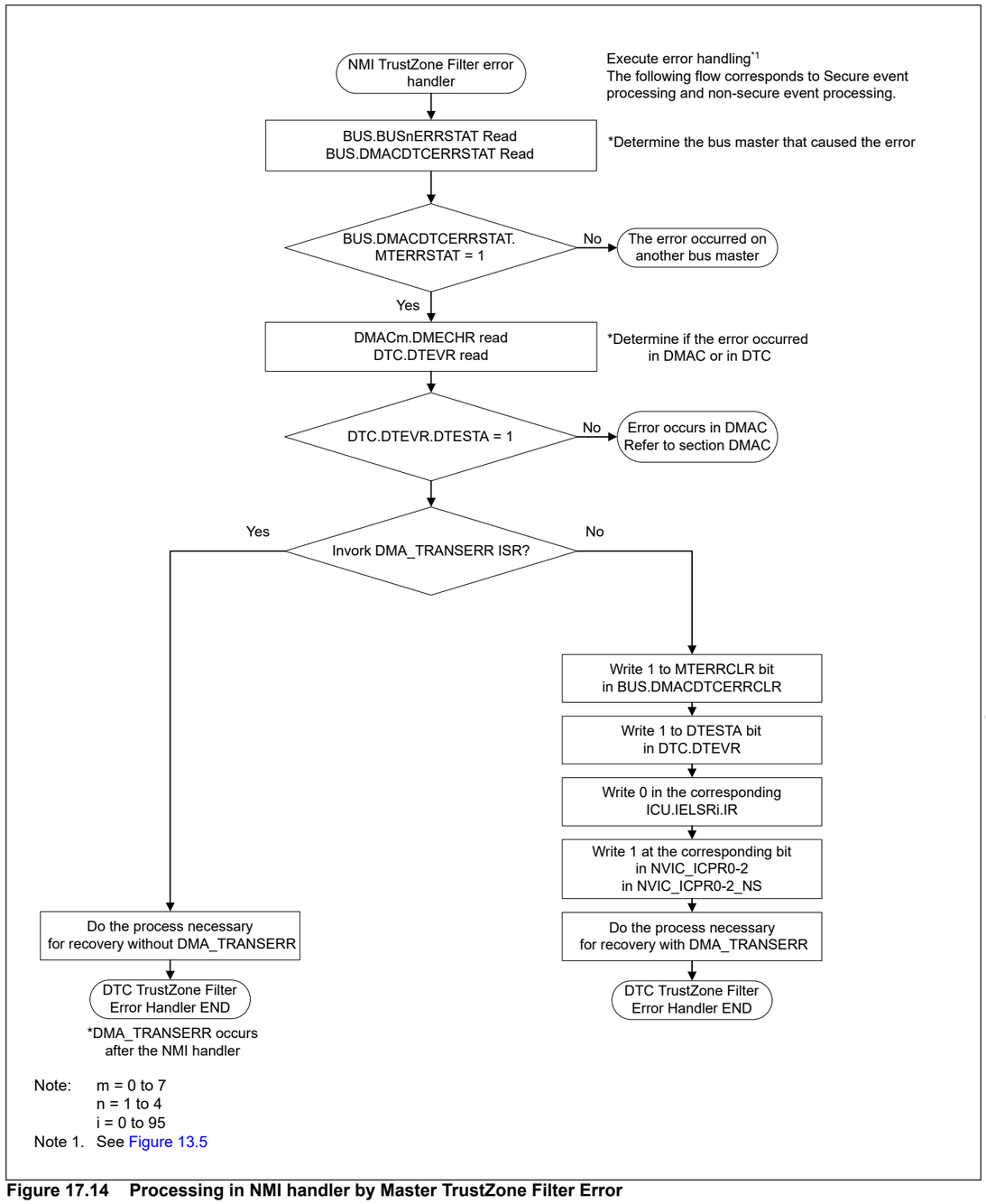
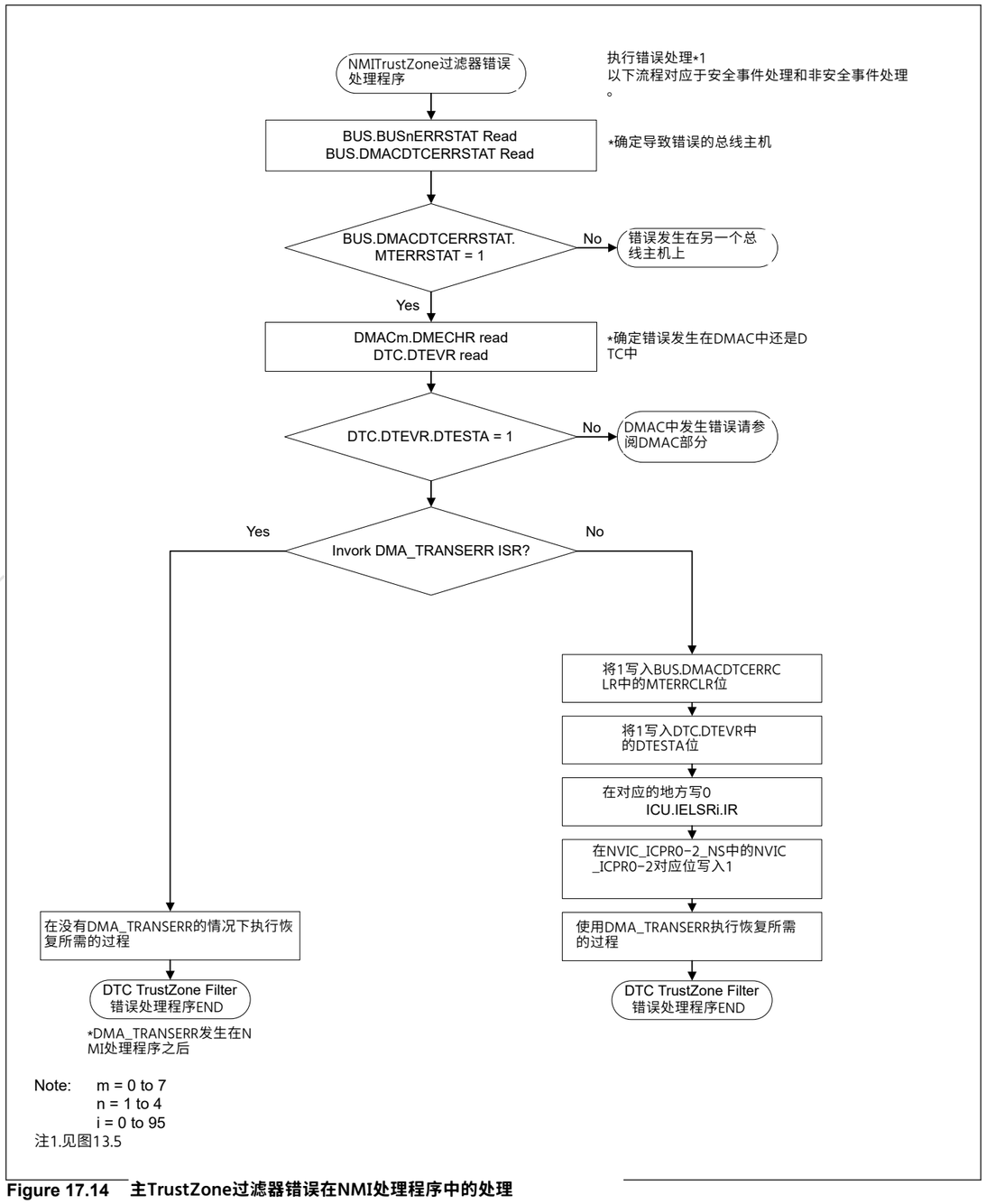


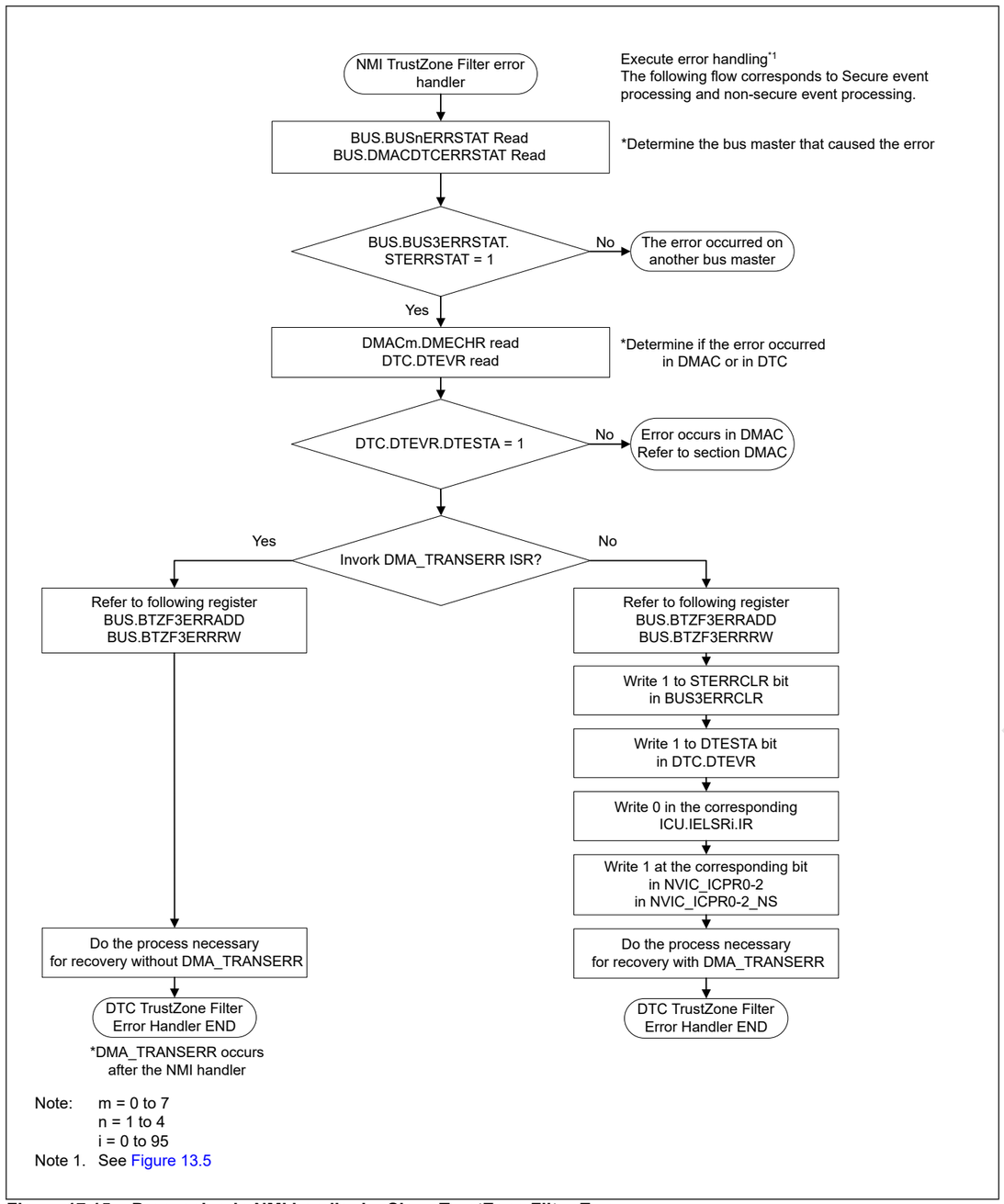
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
Note 1. See Figure 13.5

Figure 17.14 Processing in NMI handler by Master TrustZone Filter Error



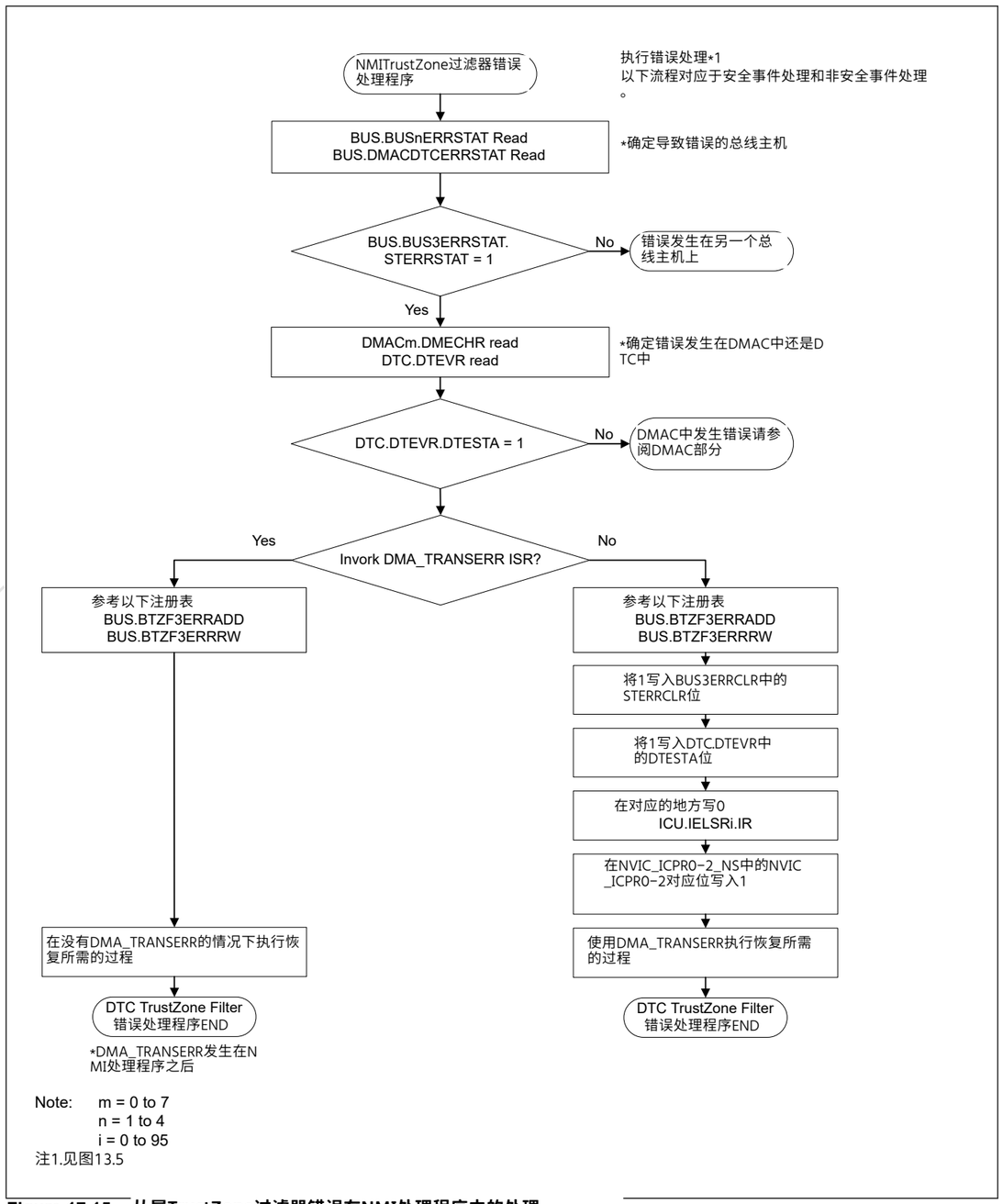
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
注1.见图13.5

Figure 17.14 主TrustZone过滤器错误在NMI处理程序中的处理



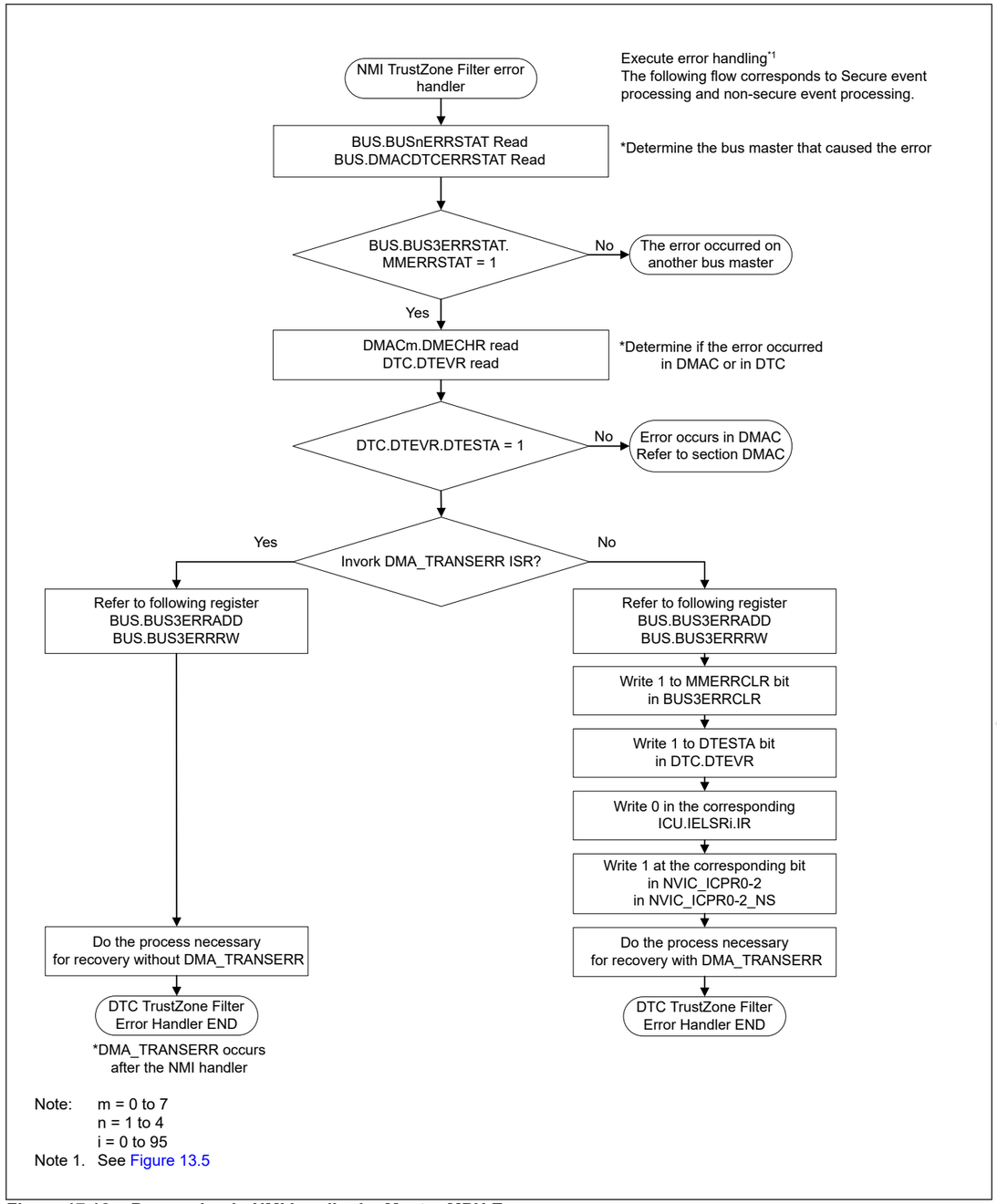
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
Note 1. See Figure 13.5

Figure 17.15 Processing in NMI handler by Slave TrustZone Filter Error



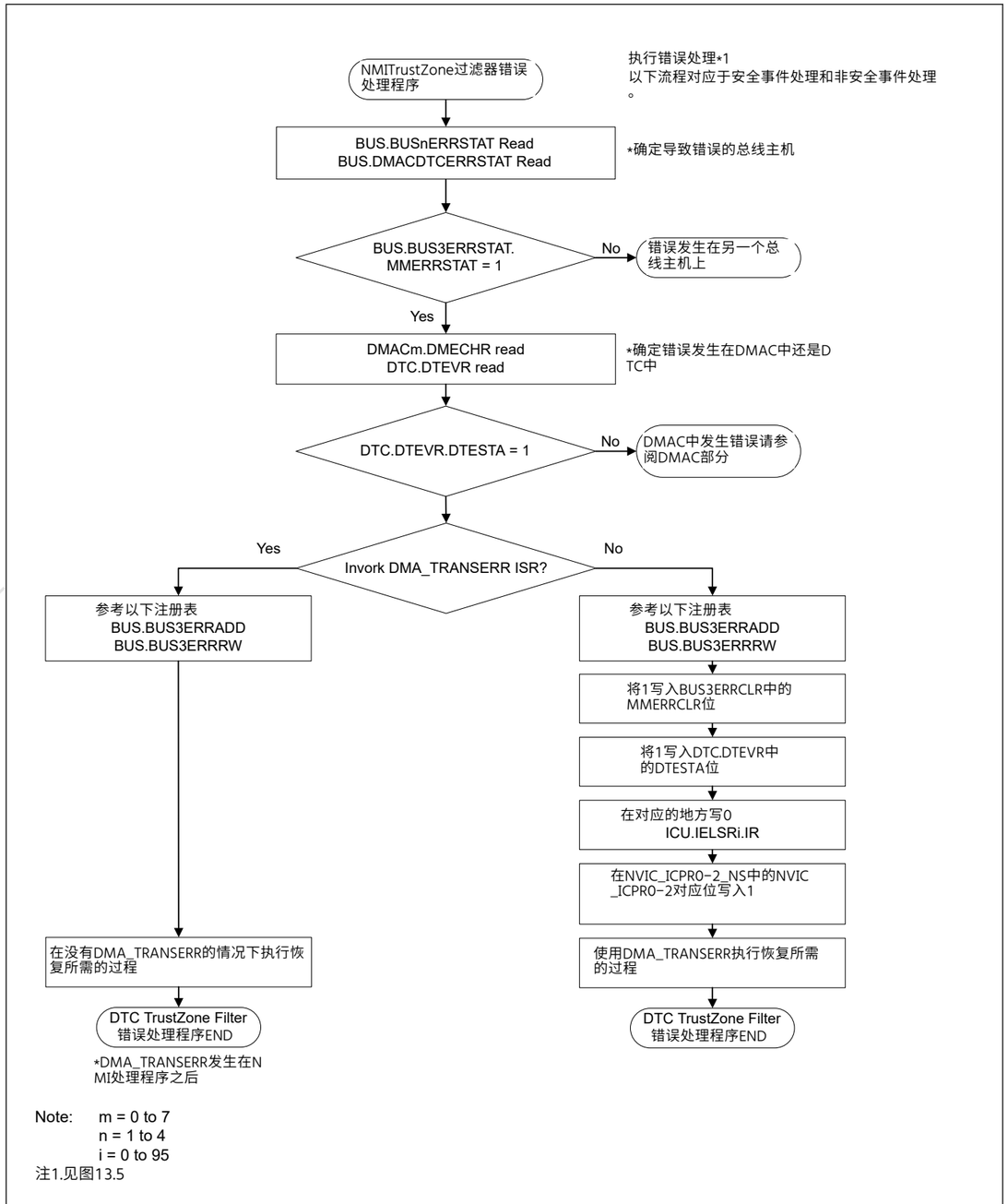
Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
注1.见图13.5

Figure 17.15 从属TrustZone过滤器错误在NMI处理程序中的处理



Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
Note 1. See Figure 13.5

Figure 17.16 Processing in NMI handler by Master MPU Error



Note: m = 0 to 7
n = 1 to 4
i = 0 to 95
注1.见图13.5

Figure 17.16 主MPU错误在NMI处理程序中的处理

17.7.2 Processing on Error response detection interrupt request (DMA_TRANSERR) handler

The cause of error response detection interrupt request (DMA_TRANSERR) due to DMA transfer error is the Slave Bus Error or Illegal Access Error. Also, it occurs after the NMI handler error response detection interrupt request (DMA_TRANSERR) is not cleared by the NMI handler.

It is possible to confirm the cause of the error and the vector number of DTC in which the error occurred.

Error cause confirmation procedure is shown Figure 17.17.

Figure 17.18 shows the flow for confirm the vector number that caused the Master TrustZone Filter Error in DTC

Figure 17.19 shows the flow for confirm the vector number that caused the Slave TrustZone Filter Error in DTC

Figure 17.20 shows the flow for confirm the vector number and Security Attribute that caused the Master MPU Error in DTC

Figure 17.21 shows the flow for confirm the vector number and Security Attribute that caused the Slave Bus Error in DTC

Figure 17.22 shows the flow for confirm the vector number and Security Attribute that caused the Illegal Access Error in DTC

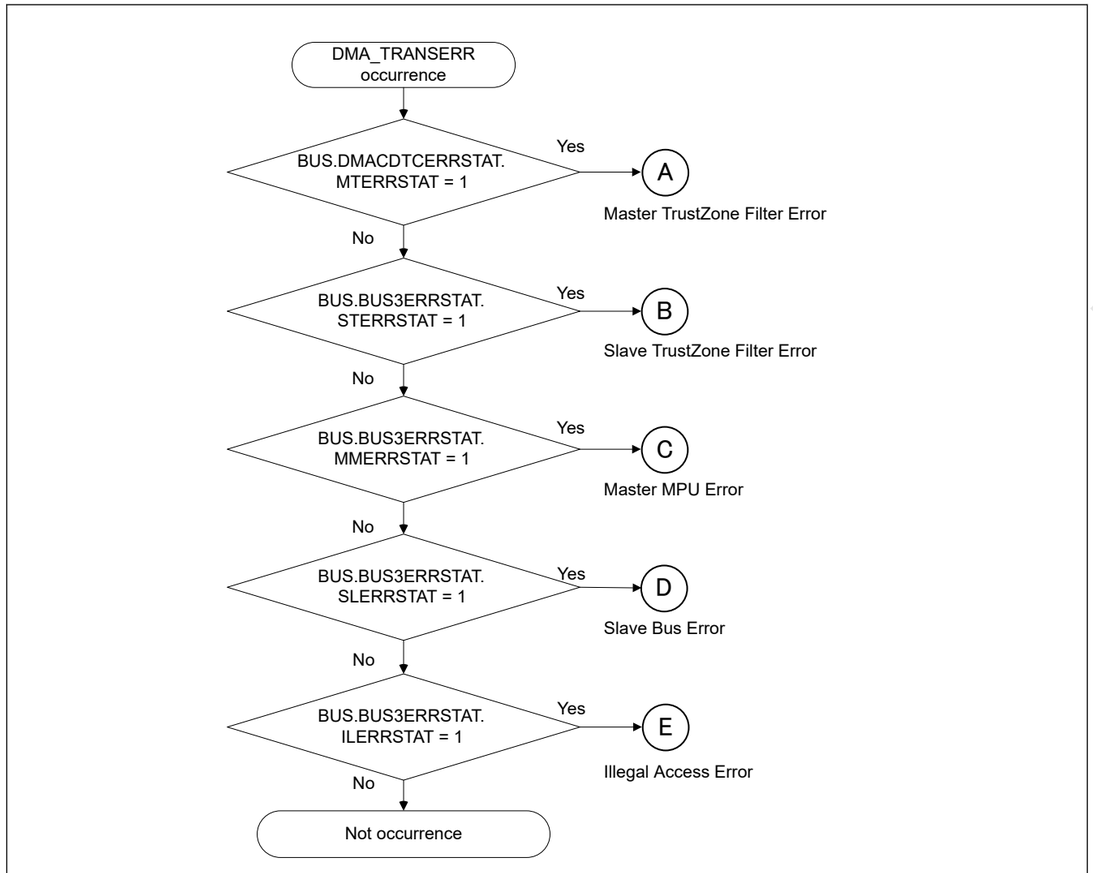


Figure 17.17 Transfer error factor judgment when the error response detection interrupt (DMA_TRANSERR) occurs

17.7.2 错误响应检测中断请求(DMA_TRANSERR)处理程序的处理

由于DMA传输错误导致错误响应检测中断请求(DMA_TRANSERR)的原因是从总线错误或非法访问错误。此外，它发生在NMI处理程序错误响应检测中断请求(DMA_TRANSERR)未被NMI处理程序清除之后。

可以确认错误的原因和发生错误的DTC的向量号。

错误原因确认流程如图17.17所示。

图17.18显示了在DTC中确认导致MasterTrustZoneFilterError的向量号的流程

图17.19显示了在DTC中确认导致SlaveTrustZoneFilterError的向量号的流程

图17.20显示了确认导致MasterMPU错误的向量号和安全属性的流程DTC

图17.21显示了在DTC中确认导致从总线错误的向量号和安全属性的流程

图17.22显示了确认导致非法访问错误的向量号和安全属性的流程DTC

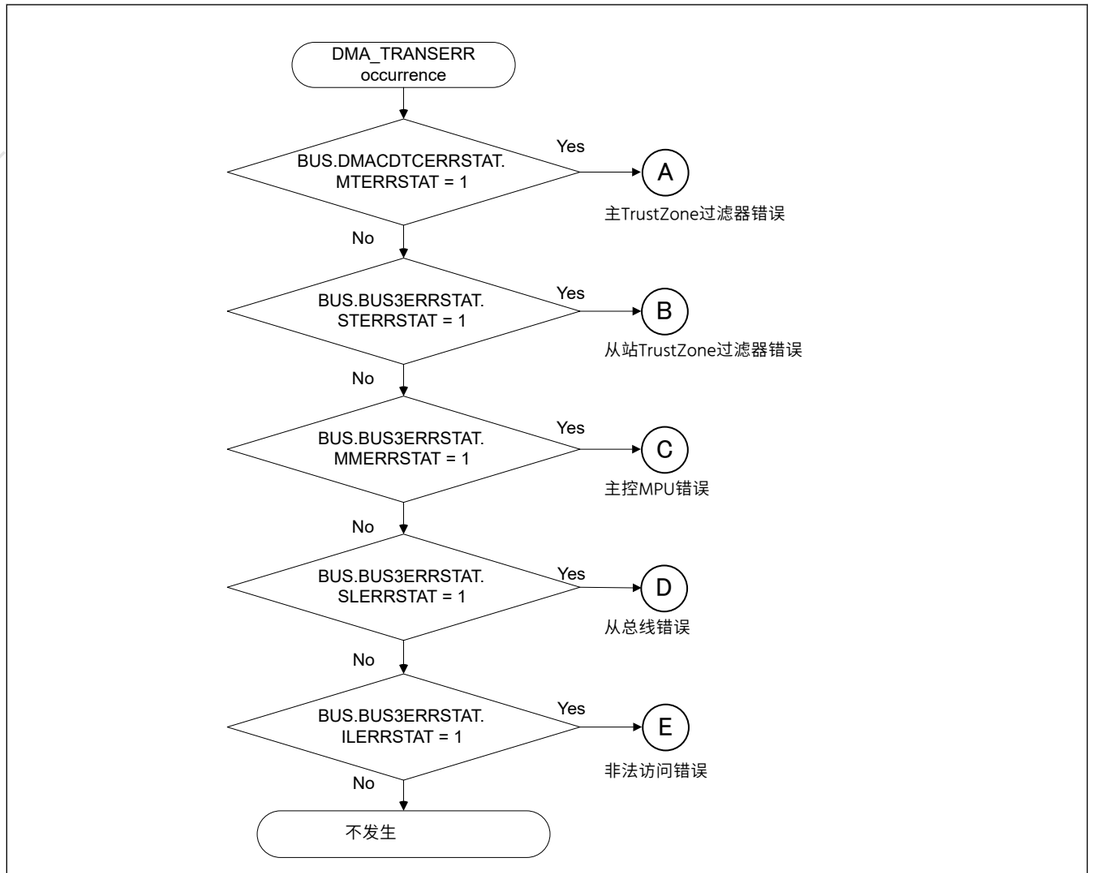


Figure 17.17 发生错误响应检测中断（DMA_TRANSERR）时的传输错误因素判断

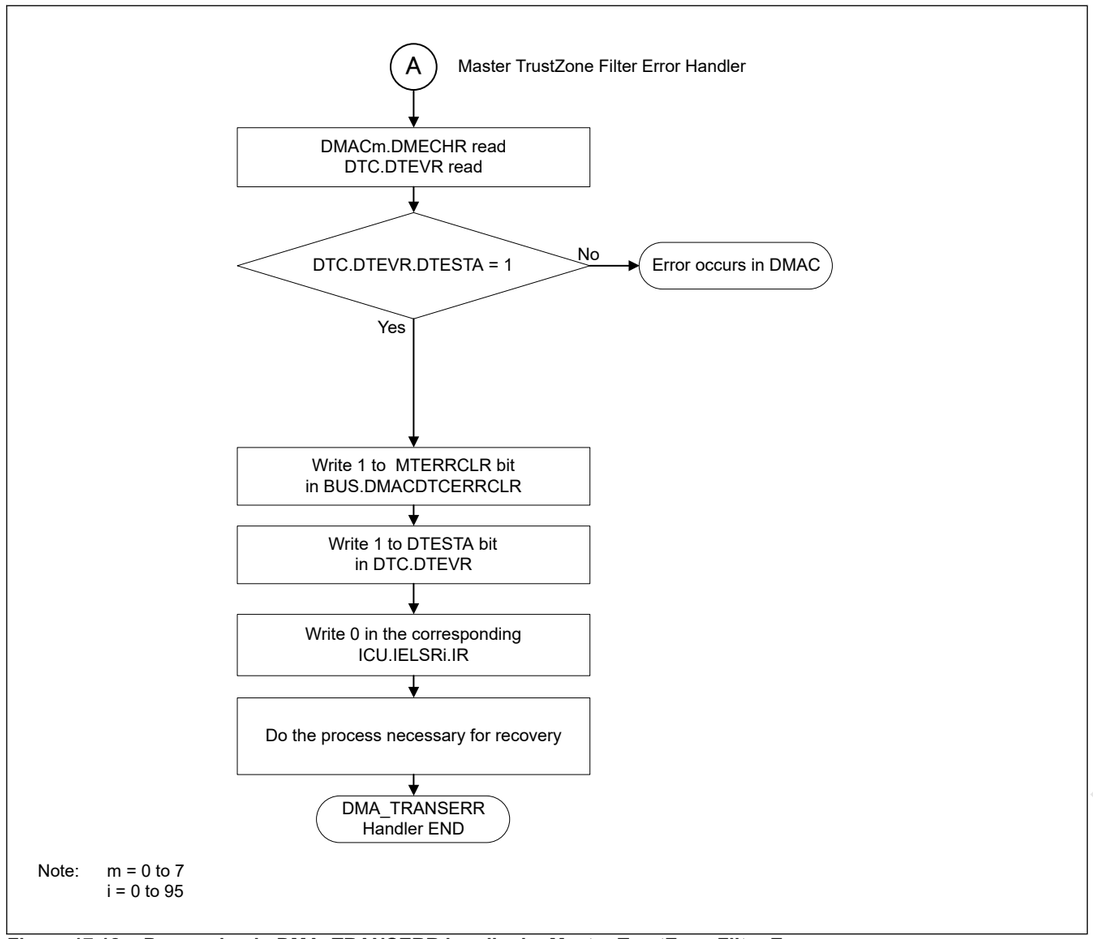


Figure 17.18 Processing in DMA_TRANSERR handler by Master TrustZone Filter Error

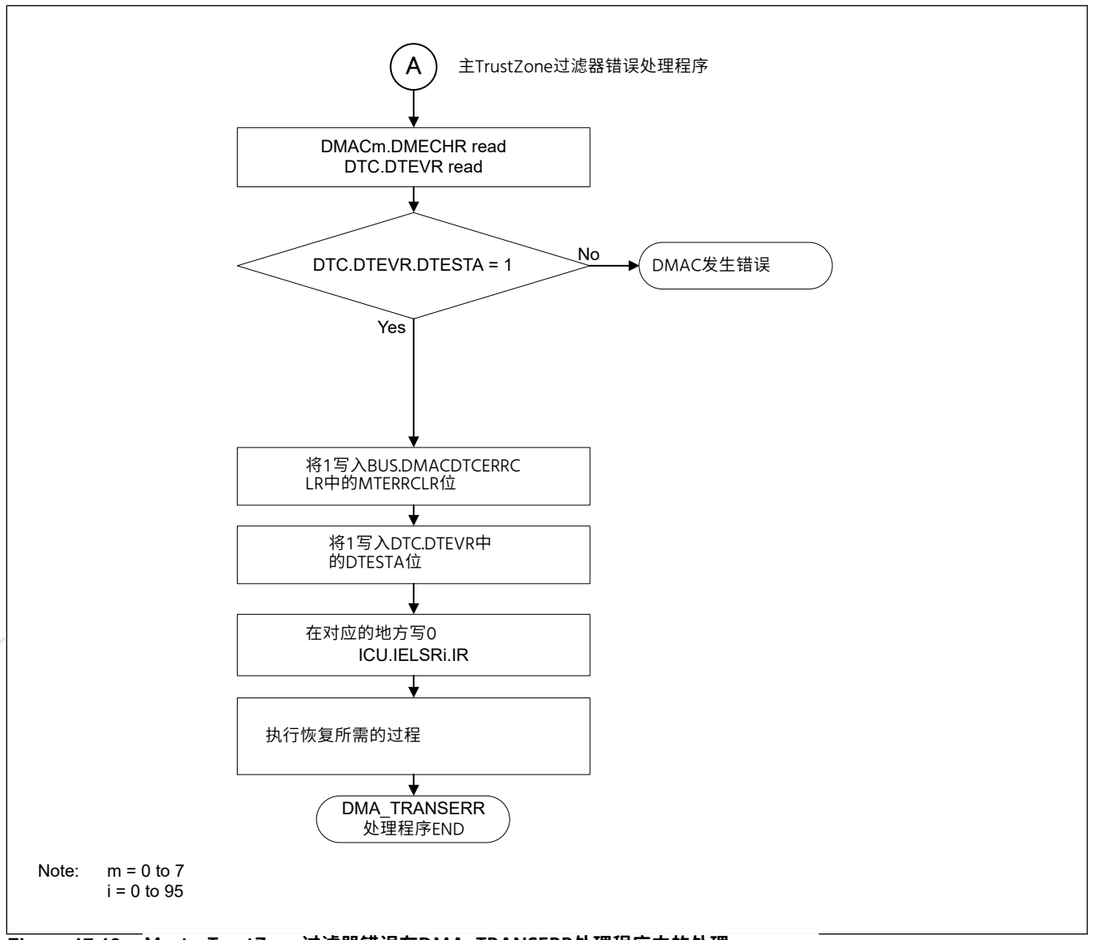


Figure 17.18 MasterTrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

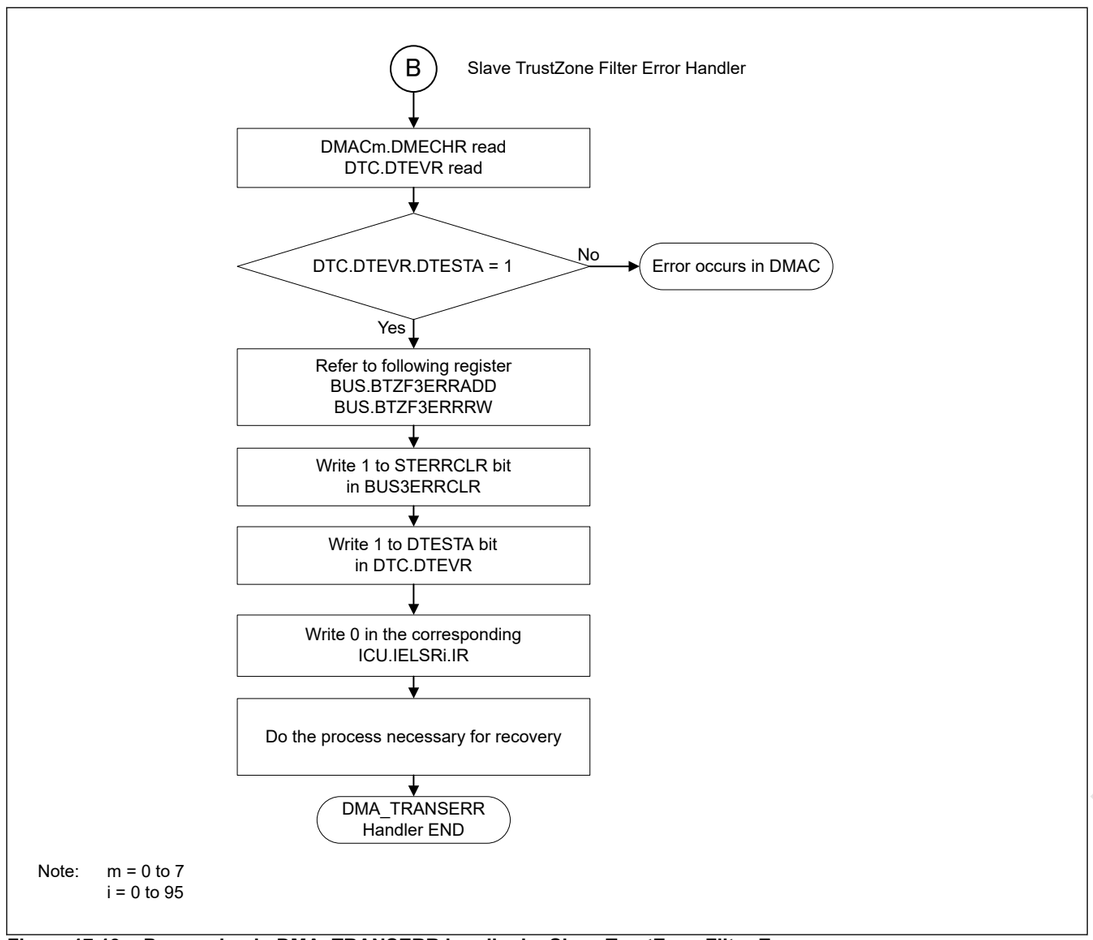


Figure 17.19 Processing in DMA_TRANSERR handler by Slave TrustZone Filter Error

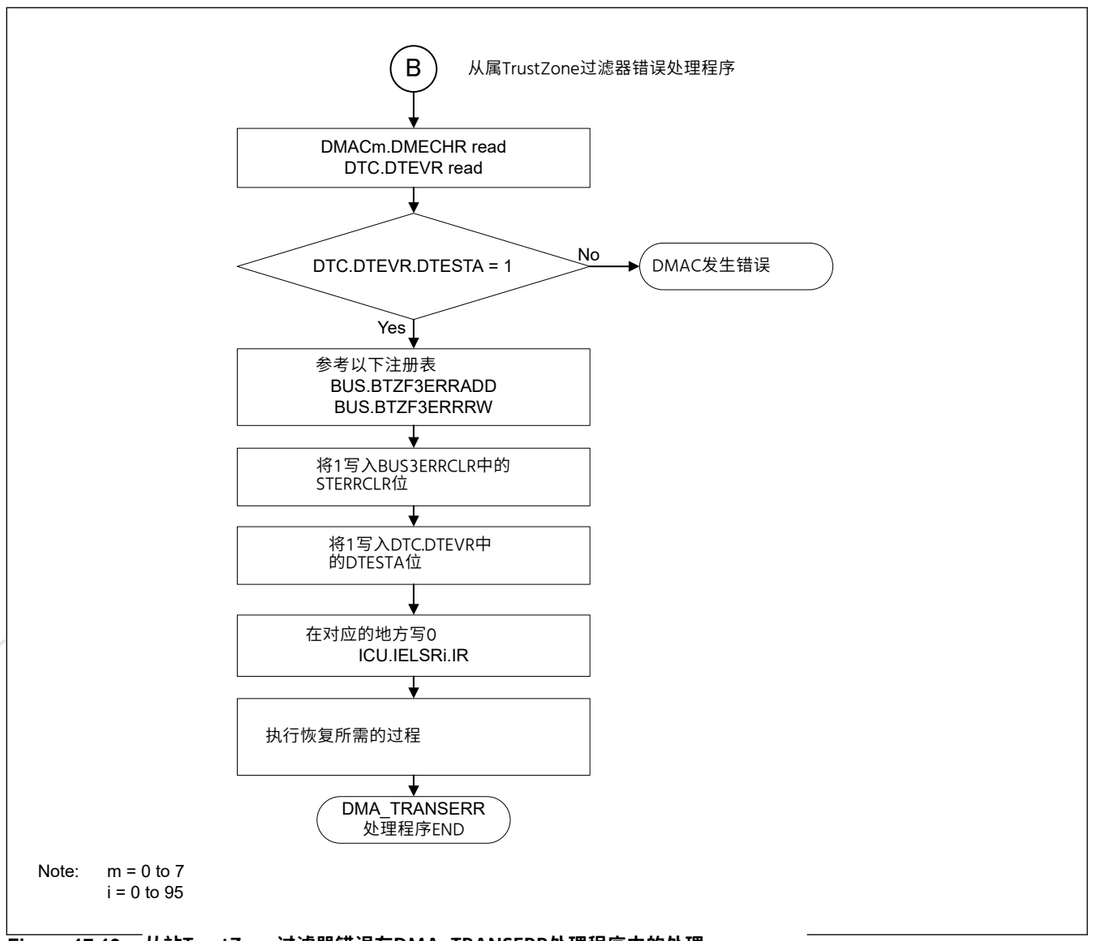


Figure 17.19 从站TrustZone过滤器错误在DMA_TRANSERR处理程序中的处理

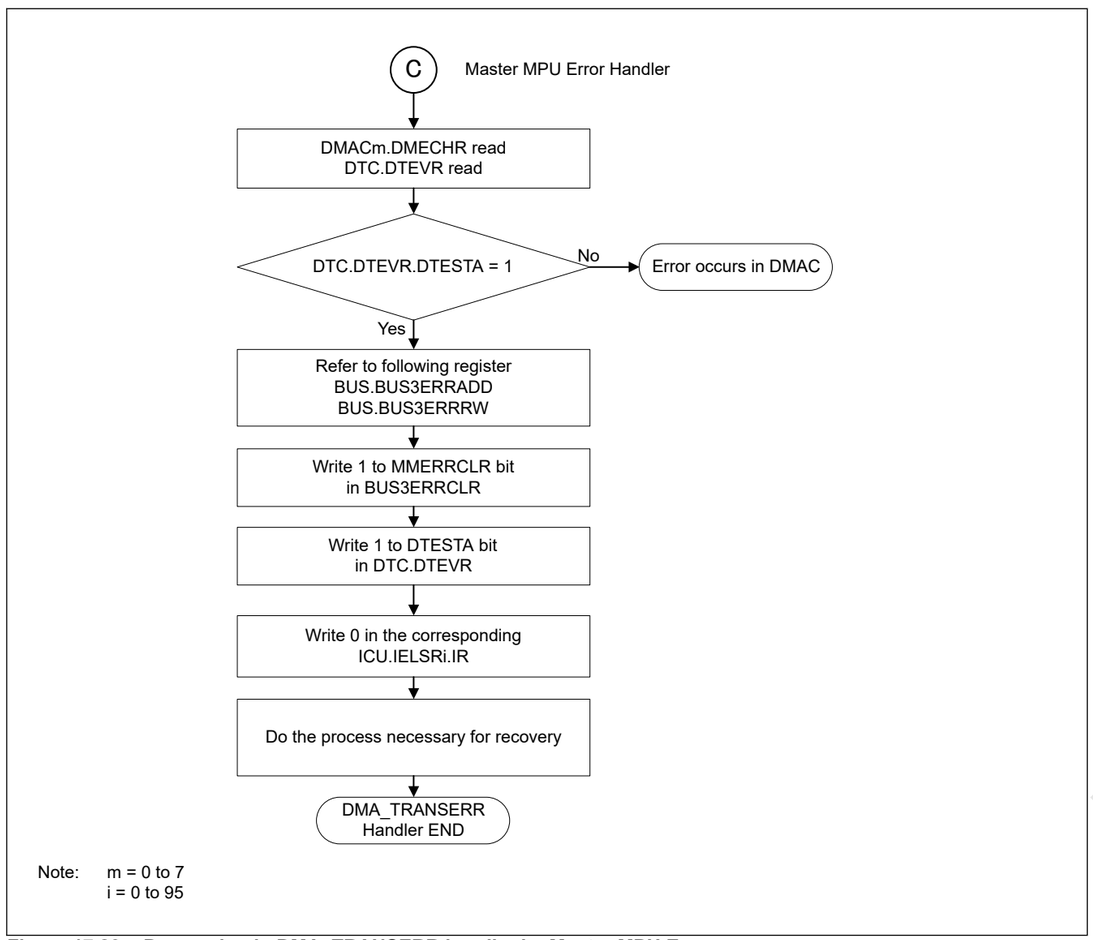


Figure 17.20 Processing in DMA_TRANSERR handler by Master MPU Error

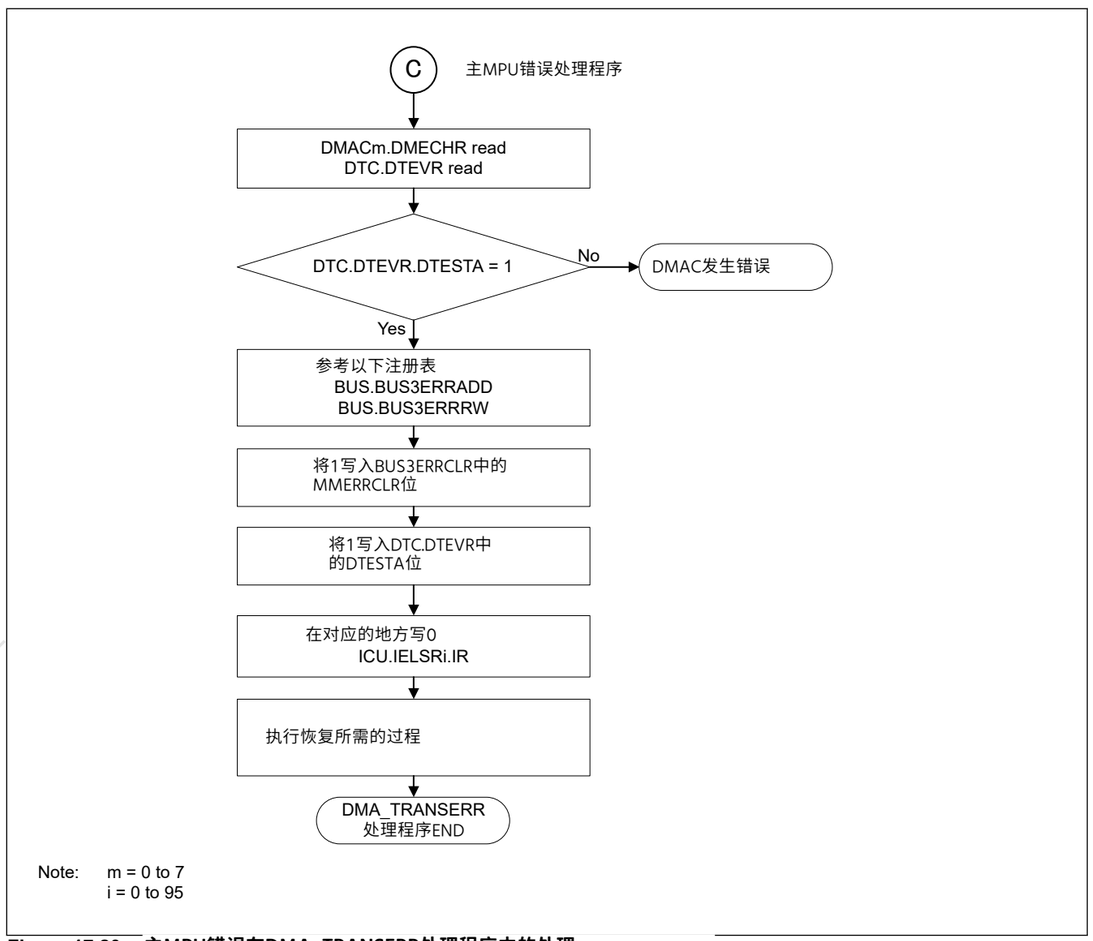


Figure 17.20 主MPU错误在DMA_TRANSERR处理程序中的处理

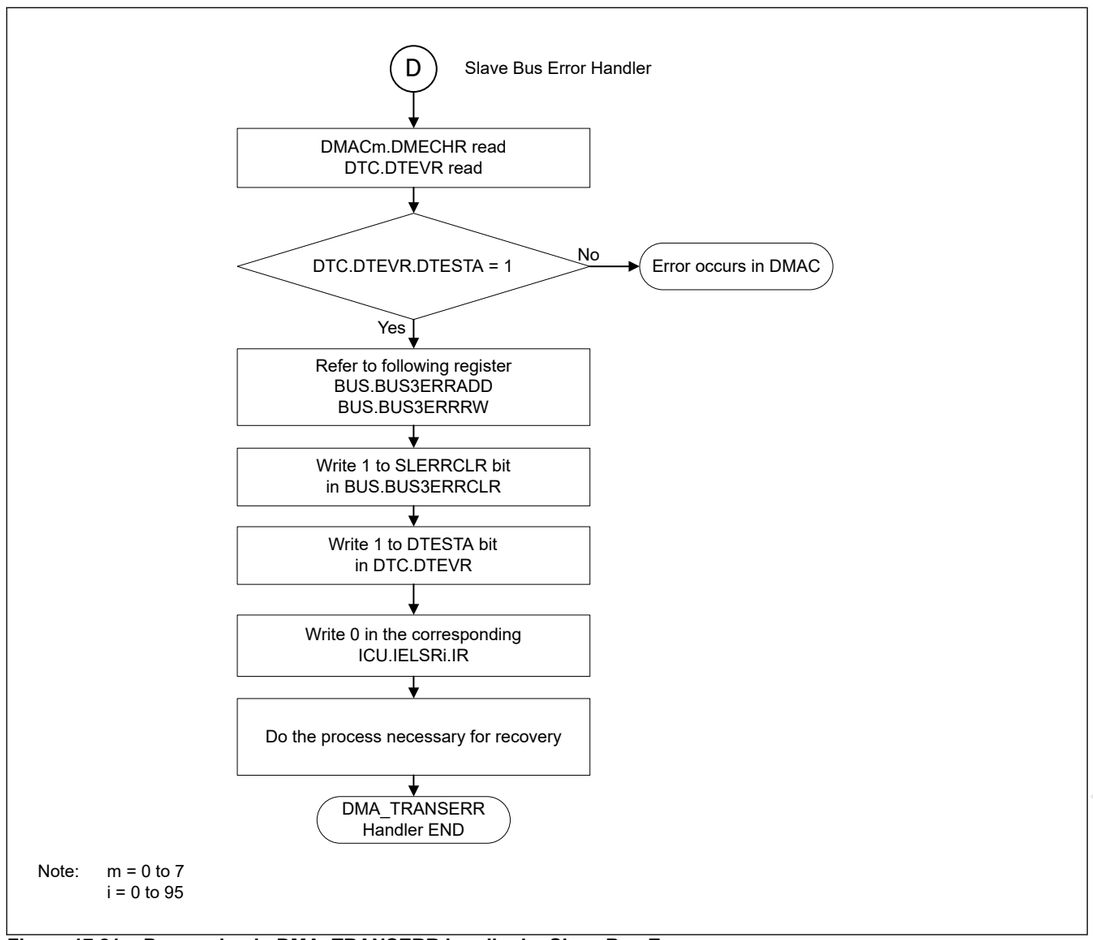


Figure 17.21 Processing in DMA_TRANSERR handler by Slave Bus Error

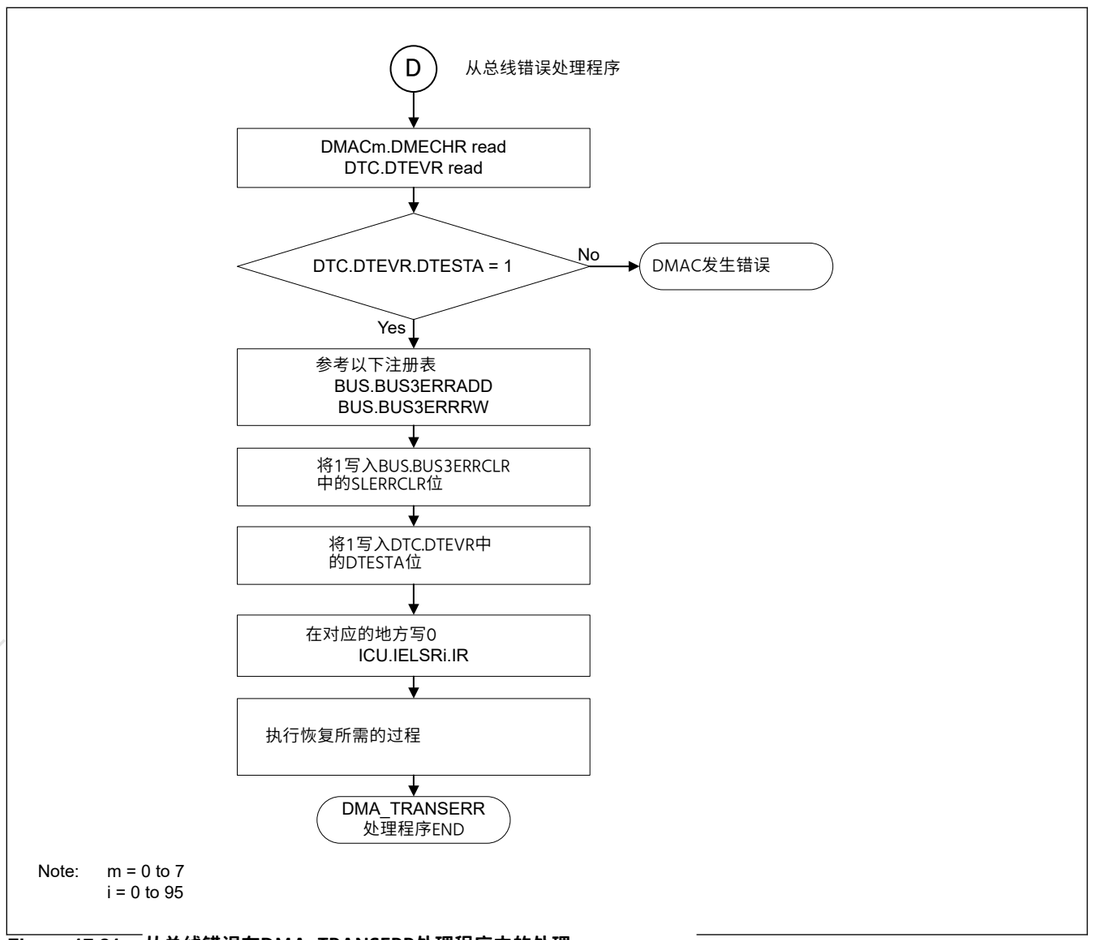


Figure 17.21 从总线错误在DMA_TRANSERR处理程序中的处理

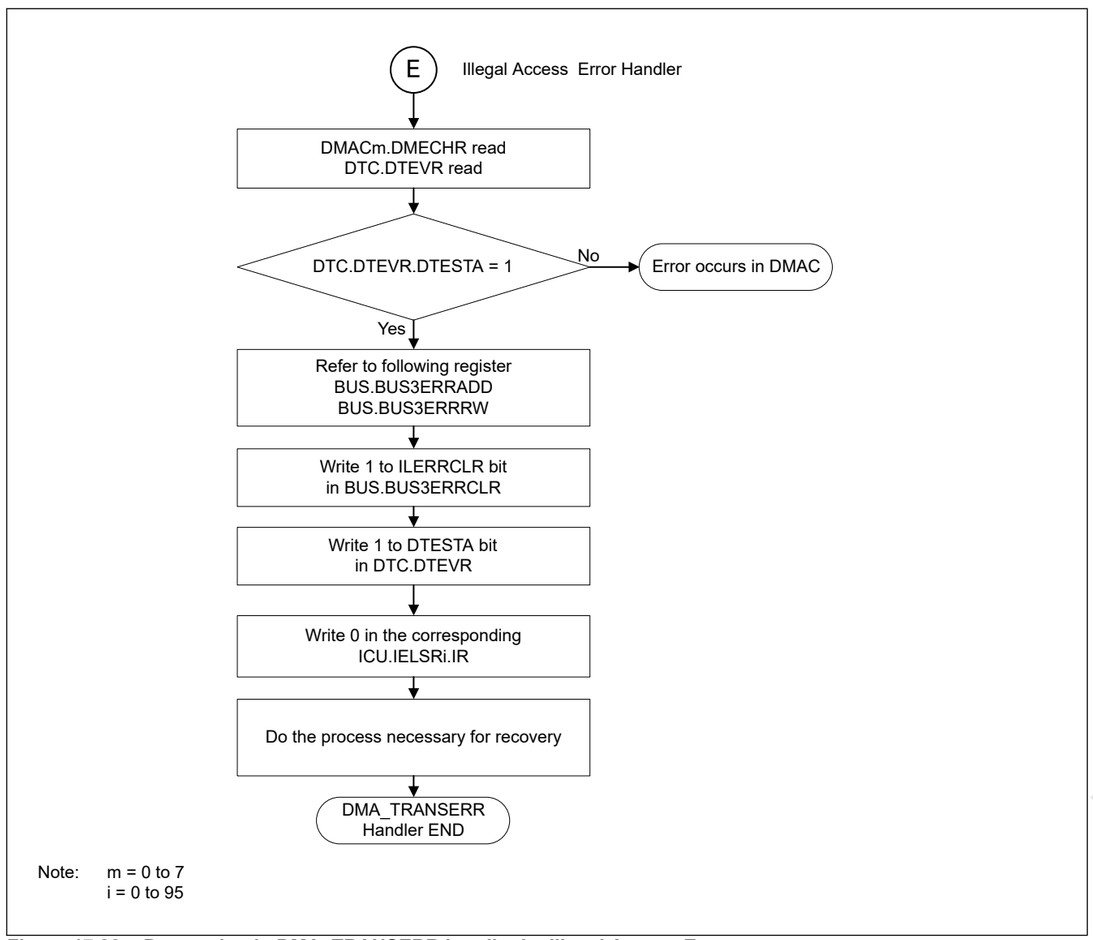


Figure 17.22 Processing in DMA_TRANSERR handler by Illegal Access Error

17.8 Interrupt

17.8.1 Interrupt Request of Transfer End

When the DTC completes data transfer of the specified count or when data transfer with MRB.DISEL set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Two types of interrupt are available: interrupts triggered by a DTC activation (per channel) and an interrupt triggered by the event signal DTC_COMPLETE (common to all channels). Interrupts to the CPU are controlled according to the settings in the NVIC and the ICU.IELSRn.IELS[8:0] bits. See section 13, Interrupt Controller Unit (ICU). The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

17.8.2 Interrupt Request of Transfer Error

The error response detection interrupt request (DMA_TRANSERR) is generated from the DMAC/DTC when the transfer error is detected during DTC transfer. The types of interrupts that occur when the DTC transfer error occurs are listed in the Table 17.10. The Table 17.10 also shows error information stored when a transfer error occurs.

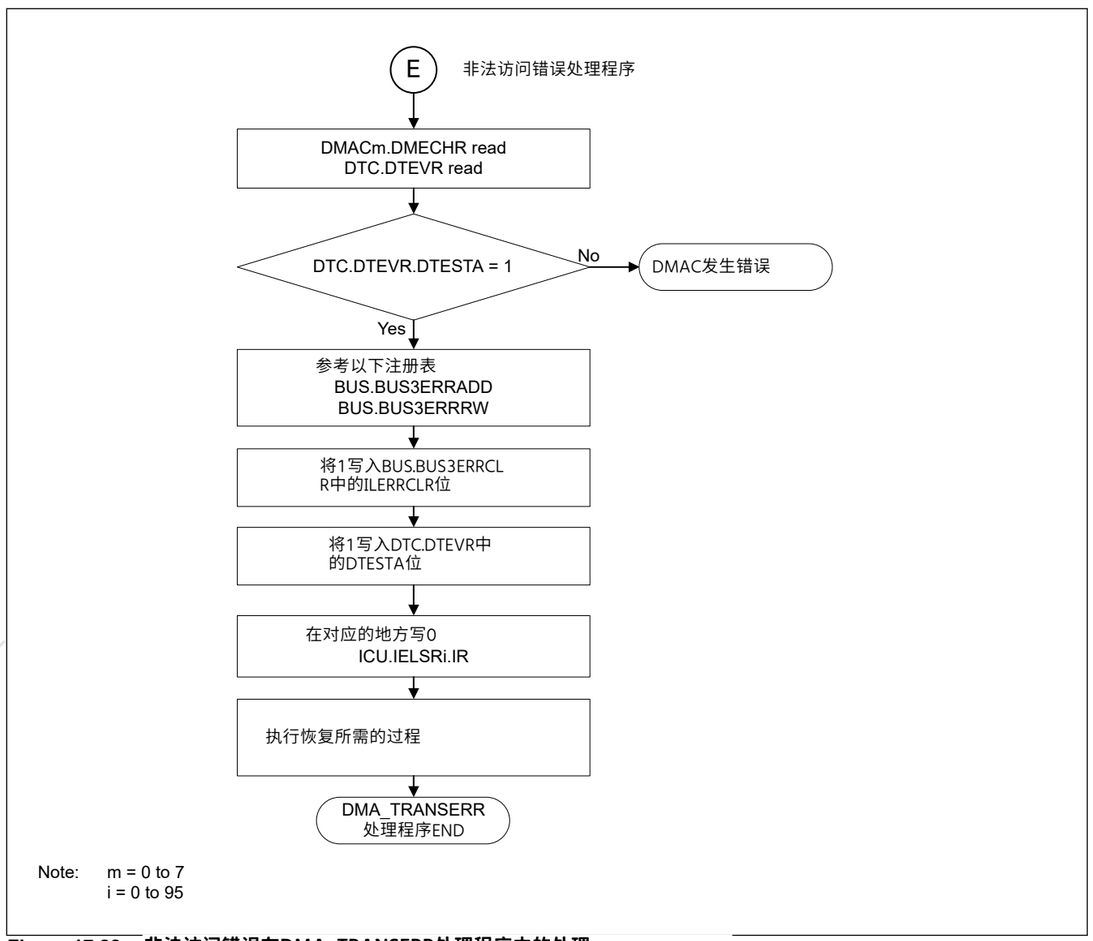


Figure 17.22 非法访问错误在DMA_TRANSERR处理程序中的处理

17.8 Interrupt

17.8.1 传输结束中断请求

当DTC完成指定计数的数据传输或MRB.DISEL设置为1的数据传输完成时，DTC激活源向CPU生成中断。有两种类型的中断可用：由DTC激活触发的中断（每个通道）和由事件信号DTC_COMPLETE触发的中断（所有通道通用）。CPU的中断根据NVIC和ICU.IELSRn.IELS[8:0]位中的设置进行控制。请参阅第13节，中断控制器单元(ICU)。DTC通过授予较小的中断向量编号较高的优先级来确定激活源的优先级。CPU中断的优先级由NVIC优先级决定。

17.8.2 传输错误中断请求

在DTC传输期间检测到传输错误时，从DMACDTC生成错误响应检测中断请求(DMA_TRANSERR)。发生DTC传输错误时发生的中断类型在表17.10中列出。表17.10还显示了发生传输错误时存储的错误信息。

Table 17.10 Interrupt and error information due to DMAC transfer error cause

Transfer error factor	NMI/RESET*1 Request	Interrupt Request	Bus Error Status	Error Address Error R/W	Error Channel Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DTC.DTEVR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DTC.DTEVR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
Slave Bus Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
Illegal Access Error	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR

Note 1. Interrupt generated, when NMI request selected as the operation after detection of the Master MPU error and The TrustZone Filter error. By confirming BUS.BUS3ERRSTAT and BUS.DMACDTCERRSTAT, judge whether it is the Master or the Slave.
Note 2. If the error response detection interrupt (DMA_TRANSERR) occurs and NMI of the Master MPU or NMI of the TrustZone Filter has not occurred, treat it as the Illegal address access error or the Slave Bus Error. It can be judged also by BUS.BUS3ERRSTAT and BUS. DMACDTCERRSTAT.

Note that if the bus error occurs when writing the last data of transfer, the transfer end event and the error response detection interrupt (DMA_TRANSERR) occurs.

17.9 Event Link

The DTC can produce an event link request on completion of one transfer request. When the destination for transfer is an external bus, however, the event link request will be issued after completion of writing to the write buffer rather than after completion of writing to the actual destination for transfer.

17.10 Low Power Consumption Function

Before transitioning to the module-stop function, Software Standby mode without Snooze mode transition, deep software standby mode, set the DTCST.DTCST bit to 0, and then perform the operations described in the following sections. The DTC is available in Snooze mode by setting the SYSTEM.SNZCR.SNZDTCEN bit to 1. See section 10, Low Power Modes.

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If the DTC transfer is in progress at the time, 1 is written to the MSTPCRA.MSTPA22 bit. The transition to the module-stop state proceeds after DTC transfer ends. While the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited. Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby mode, deep software standby mode

Use the settings described in section 10.7.1. Transitioning to Software Standby Mode or section 10.9.1. Transitioning to Deep Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode or deep software standby mode follows the completion of the DTC transfer.

(3) Snooze Mode

When the snooze control circuit receives a snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 10.8.1. Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, before transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through DTC, set SYSTEM.SNZEDCR0.DTCZRED or SYSTEM.SNZEDCR0.DTCNZRED to 1. See section 10.8.3. Returning from Snooze Mode to Software Standby Mode. SYSTEM.SNZEDCR0.DTCZRED enables or disables a snooze end request on completion of the last DTC transmission, detected on DTC transmission completion when CRA and CRB are 0. SYSTEM.SNZEDCR0.DTCNZRED enables or disables a snooze end request on a not last DTC transmission completion

Table 17.10 由于DMAC传输错误原因导致的中断和错误信息

传递误差因子	NMI/RESET*1 Request	中断请求	总线错误状态	错误地址 Error R/W	错误通道 Information
Master TrustZone Filter (in DMAC/DTC)	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.DMACDTCERRSTAT.MTERRSTAT*1	—	DTC.DTEVR
Slave TrustZone Filter	ICU.NMISR.TZFST*1	DMA_TRANSERR	BUS.BUS3ERRSTAT.STERRSTAT*1	BUS.BTZF3ERRADD BUS.BTZF3ERRRW	DTC.DTEVR
Master MPU	ICU.NMISR.BUSMST	DMA_TRANSERR	BUS.BUS3ERRSTAT.MMERRSTAT	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
从总线错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.SLERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR
非法访问错误	—*2	DMA_TRANSERR	BUS.BUS3ERRSTAT.ILERRSTAT*2	BUS.BUS3ERRADD BUS.BUS3ERRRW	DTC.DTEVR

注意1.中断，当NMI请求在检测主MPU错误和Trustzone滤波器错误后选择为操作时中断。通过确认BUS.BUS3ERRSTAT和BUS.DMACDTCERRSTAT，判断是Master还是Slave。
注2.如果错误响应检测中断(DMA_TRANSERR)发生且MasterMPU的NMI或TrustZoneFilter的NMI未发生，则将其视为Illegaladdressaccesserror或SlaveBusError。也可以通过BUS.BUS3ERRSTAT和BUS来判断。DMACDTCERRSTAT。

请注意，如果在写入传输的最后一个数据时发生总线错误，则会发生传输结束事件和错误响应检测中断（DMA_TRANSERR）。

17.9 活动链接

DTC可以在一个传输请求完成时产生一个事件链接请求。然而，当传输目的地是外部总线时，事件链接请求将在写入缓冲区写入完成后发出，而不是在实际传输目标写入完成后发出。

17.10 低功耗功能

在转换到模块停止功能、没有贪睡模式转换的软件待机模式、深度软件待机模式之前，将DTCST.DTCST位设置为0，然后执行以下部分中描述的操作。通过将SYSTEM.SNZCR.SNZDTCEN位设置为1，可以在贪睡模式下使用DTC。请参阅第10节，低功耗

Modes.

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DTC的模块停止功能。如果此时DTC传输正在进行，则将1写入MSTPCRA.MSTPA22位。在DTC传输结束后继续向模块停止状态的转换。当MSTPCRA.MSTPA22位为1时，禁止访问DTC寄存器。将0写入MSTPCRA.MSTPA22位可将DTC从模块停止状态释放。

(2) 软件待机模式，深度软件待机模式

使用第10.7.1节中描述的设置。转换到软件待机模式或第10.9.1节。过渡到深度软件待机模式。

如果在执行WFI指令时DTC传输操作正在进行，则在DTC传输完成后转换到软件待机模式或深度软件待机模式。

(3) 贪睡模式

当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转入贪睡模式。请参阅第10.8.1节。过渡到贪睡模式。贪睡模式下的DTC操作可以在

SYSTEM.SNZCR.SNZDTCEN位。如果在贪睡模式下启用DTC操作，则在转换到软件待机模式之前，将DTCST.DTCST位设置为1。要通过DTC返回到软件待机模式，请将SYSTEM.SNZEDCR0.DTCZRED或SYSTEM.SNZEDCR0.DTCNZRED设置为1。请参阅第10.8.3节。从贪睡回来

模式到软件待机模式。SYSTEM.SNZEDCR0.DTCZRED在最后一次DTC传输完成时启用或禁用贪睡结束请求，当CRA和CRB为0时在DTC传输完成时检测到。SYSTEM.SNZEDCR0.DTCNZRED在非最后一次DTC传输时启用或禁用贪睡结束请求完成

(CRA and CRB are not 0), detected on DTC transmission completion when CRA and CRB are not 0. The DTC activation request from the ICU is stopped during Software Standby mode but not stopped during Snooze mode.

(4) Notes on Low Power Consumption Function

For the WFI instruction and the register setting procedure, see section 10, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without a Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 13.4.1. Detecting Interrupts, then execute the WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

17.11 Usage Notes

17.11.1 Transfer Information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

（CRA和CRB不为0），当CRA和CRB不为0时，在DTC传输完成时检测到。来自ICU的DTC激活请求在软件待机模式期间停止，但在贪睡模式期间不停止。

(4) 低功耗功能注意事项

关于WFI指令和寄存器设置过程，请参见第10节，低功耗模式。

要在从低功耗模式返回后执行DTC传输而不进行贪睡模式转换，请将DTCST.DTCST位再次为1。

要将在软件待机模式下生成的请求用作对CPU的中断请求，而不是用作DTC激活请求，请按照第13.4.1节中的说明将CPU指定为中断请求目标。检测中断，然后执行WFI指令。如果在贪睡模式下启用DTC操作，请勿使用DTC的模块停止功能。

17.11 使用说明

17.11.1 传输信息起始地址

您必须为向量表中的传输信息起始地址设置4的倍数。否则，这些地址的最低2位被视为00b。

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18. Event Link Controller (ELC)

18.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 18.1 lists the ELC specifications, and Figure 18.1 shows a block diagram.

Table 18.1 ELC Specifications

Item	Description
Event link function	219 types of event signals can be directly connected to modules. The ELC generates the ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set.
TrustZone Filter	Security attribution can be set for each registers

18. 事件链接控制器(ELC)

18.1 Overview

EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。

表18.1列出了ELC规范，图18.1显示了框图。

Table 18.1 ELC Specifications

Item	Description
事件链接功能	219种事件信号可以直接连接到模块。ELC生成ELC事件信号和激活DTC的事件。
Module-stop function	可设置模块停止状态。
TrustZone Filter	可以为每个寄存器设置安全属性

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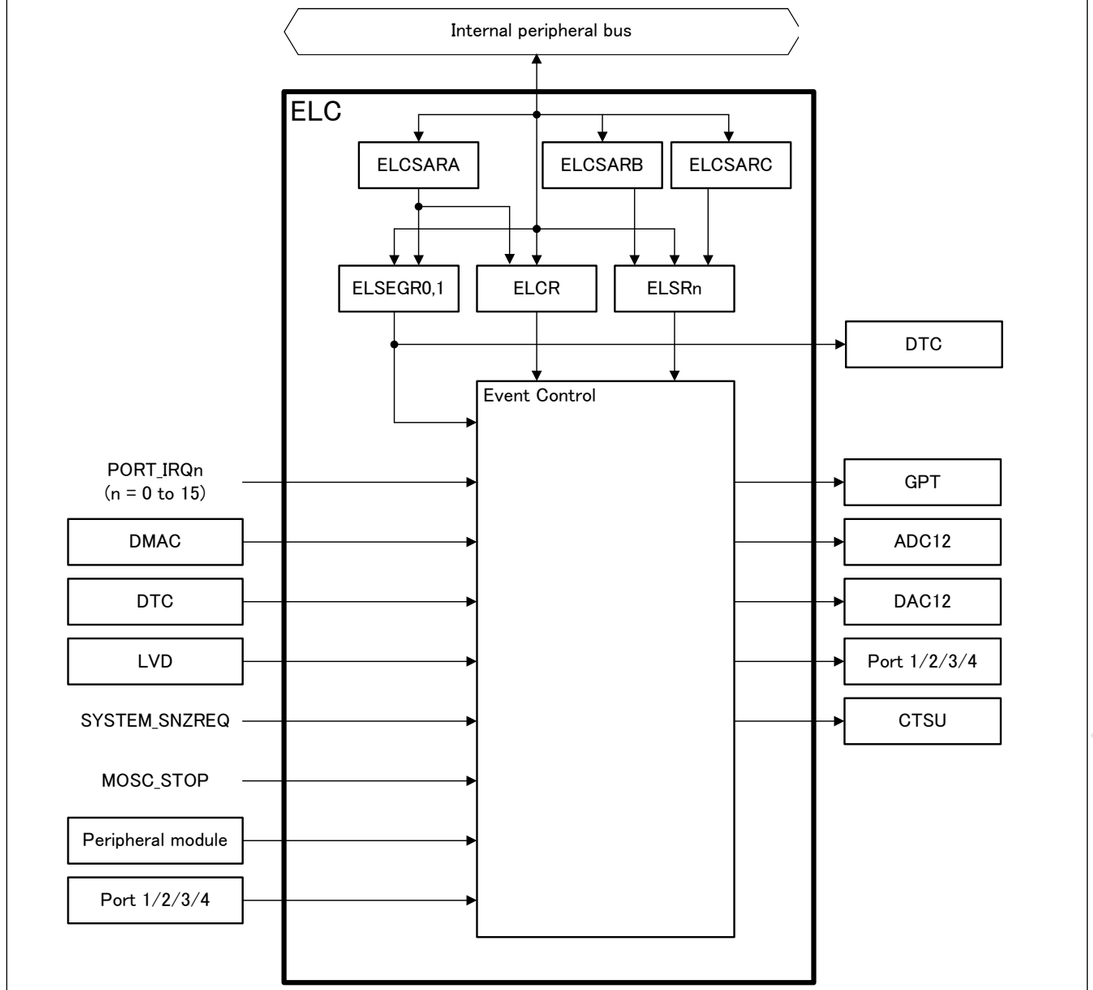

Figure 18.1 ELC block diagram

18.2 Register Descriptions

18.2.1 ELCR : Event Link Controller Register

Base address: ELC = 0x4008_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

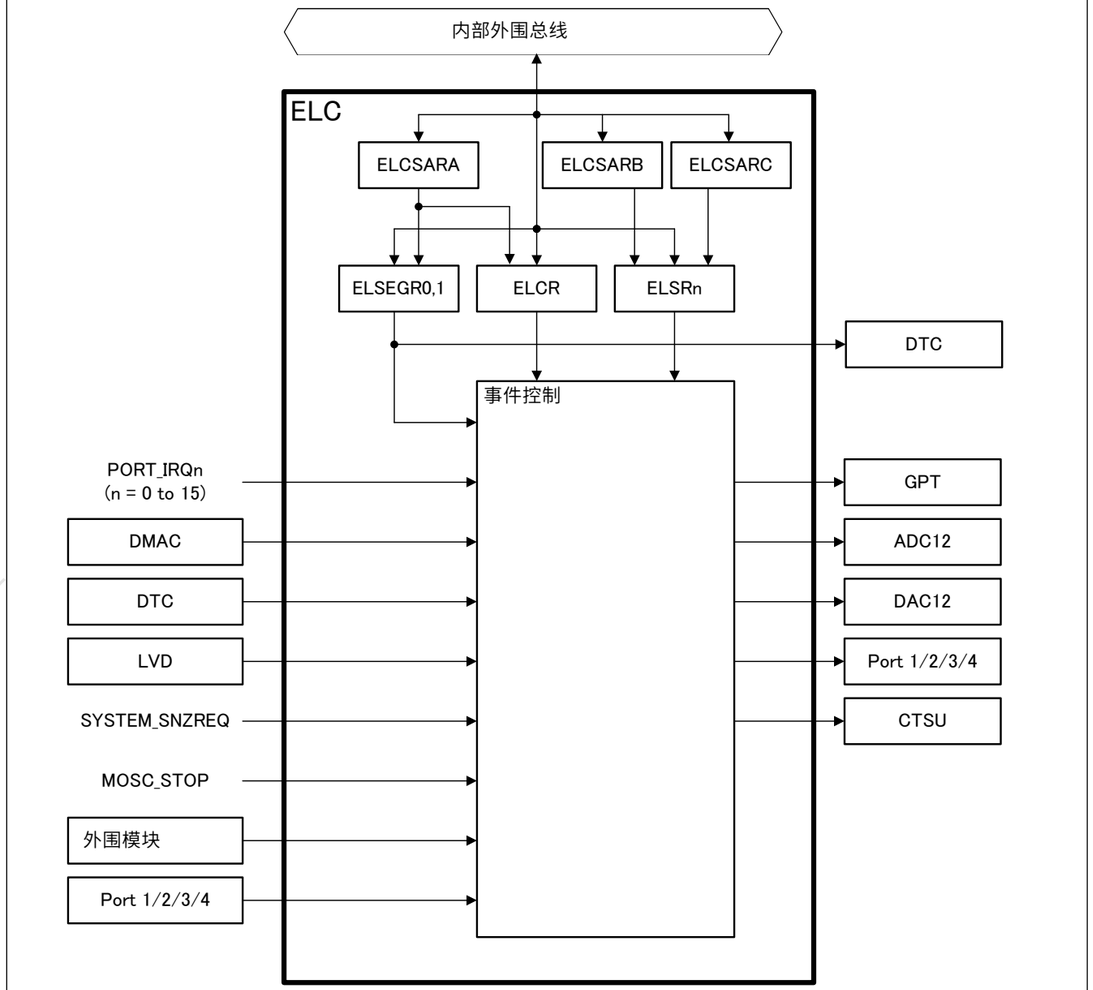

Figure 18.1 ELC框图

18.2 注册说明

18.2.1 ELCR:事件链接控制器寄存器

Base address: ELC = 0x4008_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ELCON	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	ELCON	All Event Link Enable 0: ELC function is disabled. 1: ELC function is enabled.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ELCR register controls the ELC operation.

18.2.2 ELSEGRn : Event Link Software Event Generation Register n (n = 0, 1)

Base address: ELC = 0x4008_2000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	Software Event Generation 0: Normal operation 1: Software event is generated.	W
5:1	—	These bits are read as 0. The write value should be 0.	R/W
6	WE	SEG Bit Write Enable 0: Write to SEG bit disabled. 1: Write to SEG bit enabled.	R/W
7	WI	ELSEGR Register Write Disable 0: Write to ELSEGR register enabled. 1: Write to ELSEGR register disabled.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	ELCON	所有事件链接启用 0：ELC功能关闭。1：ELC功能使能。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ELCR寄存器控制ELC操作。

18.2.2 ELSEGRn:事件链接软件事件生成寄存器n(n=0 1)

Base address: ELC = 0x4008_2000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WI	WE	—	—	—	—	—	SEG
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SEG	软件事件生成 0：正常操作1：产生软件事件。	W
5:1	—	这些位被读取为0。写入值应为0。	R/W
6	WE	SEG位写使能 0：禁止写入SEG位。1：写入SEG位使能。	R/W
7	WI	ELSEGR寄存器写入禁用 0：允许写入ELSEGR寄存器。1：禁止写入ELSEGR寄存器。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SEG位（软件事件生成）

当WE位为1时向SEG位写入1时，将产生软件事件。该位被读取为0。即使向该位写入1，也不存储数据。在写入该位之前，WE位必须设置为1。

软件事件可以触发链接的DTC事件。

WE位（SEG位写使能）

SEG位只能在WE位为1时写入。在写入该位之前将WI位清零。

[Setting condition]

●如果在WI位为0时向该位写入1，则该位变为1。

[Clearing condition]

●如果在WI位为0时向该位写入0，则该位变为0。

WI位（ELSEGR寄存器写入禁止）

只有当WI位的写入值为0时，才能写入ELSEGR寄存器。该位读为1。在设置之前WE或SEG位，WI位必须设置为0。

18.2.3 ELSRn : Event Link Setting Register n (n = 0 to 18)

Base address: ELC = 0x4008_2000

Offset address: 0x10 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ELS[8:0]	Event Link Select 0x000: Event output disabled for the associated peripheral module 0x001: Number setting for the event signal to be linked ⋮ 0x1DB: Number setting for the event signal to be linked Others: Settings prohibited	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ELSRn register specifies an event signal to be linked to each peripheral module. Table 18.2 shows the association between the ELSRnELSRn register and the peripheral modules. Table 18.3 shows the association between the event signal names set in the ELSRn register and the signal numbers.

Table 18.2 Association between the ELSRn registers and peripheral functions

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR10	ADC12A1	ELC_AD10
ELSR11	ADC12B1	ELC_AD11
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4
ELSR18	CTSU	ELC_CTSU

18.2.3 ELSRn：事件链接设置寄存器n（n=0到18）

Base address: ELC = 0x4008_2000

Offset address: 0x10 + 0x04 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	ELS[8:0]	活动链接选择 0x000：相关外围模块的事件输出禁用0x001：要链接的事件信号的编号设置 ⋮ 0x1DB：要联动的事件信号的编号设置其他：禁止设置	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ELSRn寄存器指定要链接到每个外围模块的事件信号。表18.2显示了ELSRnELSRn寄存器和外围模块之间的关联。表18.3显示了在ELSRn寄存器中设置的事件信号名称和信号编号之间的关联。

Table 18.2 ELSRn寄存器和外设功能之间的关联

注册名称	外设功能（模块）	活动名称
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR10	ADC12A1	ELC_AD10
ELSR11	ADC12B1	ELC_AD11
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4
ELSR18	CTSU	ELC_CTSU

Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (1 of 6)

Event number	Interrupt request source	Name	Description
0x001	Port	PORT_IRQ0*1	External pin interrupt 0
0x002		PORT_IRQ1*1	External pin interrupt 1
0x003		PORT_IRQ2*1	External pin interrupt 2
0x004		PORT_IRQ3*1	External pin interrupt 3
0x005		PORT_IRQ4*1	External pin interrupt 4
0x006		PORT_IRQ5*1	External pin interrupt 5
0x007		PORT_IRQ6*1	External pin interrupt 6
0x008		PORT_IRQ7*1	External pin interrupt 7
0x009		PORT_IRQ8*1	External pin interrupt 8
0x00A		PORT_IRQ9*1	External pin interrupt 9
0x00B		PORT_IRQ10*1	External pin interrupt 10
0x00C		PORT_IRQ11*1	External pin interrupt 11
0x00D		PORT_IRQ12*1	External pin interrupt 12
0x00E		PORT_IRQ13*1	External pin interrupt 13
0x00F		PORT_IRQ14*1	External pin interrupt 14
0x010		PORT_IRQ15*1	External pin interrupt 15
0x020	DMAC	DMAC0_INT	DMAC transfer end 0
0x021		DMAC1_INT	DMAC transfer end 1
0x022		DMAC2_INT	DMAC transfer end 2
0x023		DMAC3_INT	DMAC transfer end 3
0x024		DMAC4_INT	DMAC transfer end 4
0x025		DMAC5_INT	DMAC transfer end 5
0x026		DMAC6_INT	DMAC transfer end 6
0x027		DMAC7_INT	DMAC transfer end 7
0x02A	DTC	DTC_DTCEND*4	DTC transfer end
0x038	LVD	LVD_LVD1	Voltage monitor 1 interrupt
0x039		LVD_LVD2	Voltage monitor 2 interrupt
0x03B	MOSC	MOSC_STOP	Mail Clock oscillation stop
0x03C	LPW	SYSTEM_SNZREQ*3*4	Snooze enrty
0x040	AGT0	AGT0_AGTI	AGT interrupt
0x041		AGT0_AGTCMAI	Compare match A
0x042		AGT0_AGTCMBI	Compare match B
0x043	AGT1	AGT1_AGTI	AGT interrupt
0x044		AGT1_AGTCMAI	Compare match A
0x045		AGT1_AGTCMBI	Compare match B
0x046	AGT2	AGT2_AGTI	AGT interrupt
0x047		AGT2_AGTCMAI	Compare match A
0x048		AGT2_AGTCMBI	Compare match B

Table 18.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（1of6）

事件编号	中断请求源	Name	Description
0x001	Port	PORT_IRQ0*1	外部引脚中断0
0x002		PORT_IRQ1*1	外部引脚中断1
0x003		PORT_IRQ2*1	外部引脚中断2
0x004		PORT_IRQ3*1	外部引脚中断3
0x005		PORT_IRQ4*1	外部引脚中断4
0x006		PORT_IRQ5*1	外部引脚中断5
0x007		PORT_IRQ6*1	外部引脚中断6
0x008		PORT_IRQ7*1	外部引脚中断7
0x009		PORT_IRQ8*1	外部引脚中断8
0x00A		PORT_IRQ9*1	外部引脚中断9
0x00B		PORT_IRQ10*1	外部引脚中断10
0x00C		PORT_IRQ11*1	外部引脚中断11
0x00D		PORT_IRQ12*1	外部引脚中断12
0x00E		PORT_IRQ13*1	外部引脚中断13
0x00F		PORT_IRQ14*1	外部引脚中断14
0x010		PORT_IRQ15*1	外部引脚中断15
0x020	DMAC	DMAC0_INT	DMAC传输结束0
0x021		DMAC1_INT	DMAC传输结束1
0x022		DMAC2_INT	DMAC传输结束2
0x023		DMAC3_INT	DMAC传输结束3
0x024		DMAC4_INT	DMAC传输结束4
0x025		DMAC5_INT	DMAC传输结束5
0x026		DMAC6_INT	DMAC传输结束6
0x027		DMAC7_INT	DMAC传输结束7
0x02A	DTC	DTC_DTCEND*4	DTC传输结束
0x038	LVD	LVD_LVD1	电压监视器1中断
0x039		LVD_LVD2	电压监视器2中断
0x03B	MOSC	MOSC_STOP	邮件时钟振荡停止
0x03C	LPW	SYSTEM_SNZREQ*3*4	Snooze enrty
0x040	AGT0	AGT0_AGTI	AGT interrupt
0x041		AGT0_AGTCMAI	比较匹配A
0x042		AGT0_AGTCMBI	比较匹配B
0x043	AGT1	AGT1_AGTI	AGT interrupt
0x044		AGT1_AGTCMAI	比较匹配A
0x045		AGT1_AGTCMBI	比较匹配B
0x046	AGT2	AGT2_AGTI	AGT interrupt
0x047		AGT2_AGTCMAI	比较匹配A
0x048		AGT2_AGTCMBI	比较匹配B

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Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (2 of 6)

Event number	Interrupt request source	Name	Description
0x049	AGT3	AGT3_AGTI	AGT interrupt
0x04A		AGT3_AGTCMAI	Compare match A
0x04B		AGT3_AGTCMBI	Compare match B
0x04C	AGT4	AGT4_AGTI	AGT interrupt
0x04D		AGT4_AGTCMAI	Compare match A
0x04E		AGT4_AGTCMBI	Compare match B
0x04F	AGT5	AGT5_AGTI	AGT interrupt
0x050		AGT5_AGTCMAI	Compare match A
0x051		AGT5_AGTCMBI	Compare match B
0x052	IWDT	IWDT_NMIUNDF	IWDT underflow
0x053	CWDT	WDT_NMIUNDF	WDT underflow
0x055	RTC	RTC_PRD	Periodic interrupt
0x073	IIC0	IIC0_RXI	Receive data full
0x074		IIC0_TXI	Transmit data empty
0x075		IIC0_TEI	Transmit end
0x076		IIC0_EEI	Transfer error
0x078	IIC1	IIC1_RXI	Receive data full
0x079		IIC1_TXI	Transmit data empty
0x07A		IIC1_TEI	Transmit end
0x07B		IIC1_EEI	Transfer error
0x07D	IIC2	IIC2_RXI	Receive data full
0x07E		IIC2_TXI	Transmit data empty
0x07F		IIC2_TEI	Transmit end
0x080		IIC2_EEI	Transfer error
0x0B1	I/O Port	IOPORT_GROUP1	Port 1 event
0x0B2		IOPORT_GROUP2	Port 2 event
0x0B3		IOPORT_GROUP3	Port 3 event
0x0B4		IOPORT_GROUP4	Port 4 event
0x0B5	ELC	ELC_SWEVT0	Software event 0
0x0B6		ELC_SWEVT1	Software event 1
0x0C0	GPT0	GPT0_CCMPA	Compare match A
0x0C1		GPT0_CCMPB	Compare match B
0x0C2		GPT0_CMPC	Compare match C
0x0C3		GPT0_CMPD	Compare match D
0x0C4		GPT0_CMPE	Compare match E
0x0C5		GPT0_CMPF	Compare match F
0x0C6		GPT0_OVF	Overflow
0x0C7		GPT0_UDF	Underflow
0x0C8		GPT0_PC	Cycle count function end

Table 18.3 在ELSRn.ELS[8:0]位中设置的事件信号名称和信号编号之间的关联（6个中的2个）

事件编号	中断请求源	Name	Description
0x049	AGT3	AGT3_AGTI	AGT interrupt
0x04A		AGT3_AGTCMAI	比较匹配A
0x04B		AGT3_AGTCMBI	比较匹配B
0x04C	AGT4	AGT4_AGTI	AGT interrupt
0x04D		AGT4_AGTCMAI	比较匹配A
0x04E		AGT4_AGTCMBI	比较匹配B
0x04F	AGT5	AGT5_AGTI	AGT interrupt
0x050		AGT5_AGTCMAI	比较匹配A
0x051		AGT5_AGTCMBI	比较匹配B
0x052	IWDT	IWDT_NMIUNDF	IWDT underflow
0x053	CWDT	WDT_NMIUNDF	WDT underflow
0x055	RTC	RTC_PRD	周期性中断
0x073	IIC0	IIC0_RXI	接收数据已满
0x074		IIC0_TXI	传输数据为空
0x075		IIC0_TEI	发射端
0x076		IIC0_EEI	传输错误
0x078	IIC1	IIC1_RXI	接收数据已满
0x079		IIC1_TXI	传输数据为空
0x07A		IIC1_TEI	发射端
0x07B		IIC1_EEI	传输错误
0x07D	IIC2	IIC2_RXI	接收数据已满
0x07E		IIC2_TXI	传输数据为空
0x07F		IIC2_TEI	发射端
0x080		IIC2_EEI	传输错误
0x0B1	I/O Port	IOPORT_GROUP1	端口1事件
0x0B2		IOPORT_GROUP2	端口2事件
0x0B3		IOPORT_GROUP3	端口3事件
0x0B4		IOPORT_GROUP4	端口4事件
0x0B5	ELC	ELC_SWEVT0	软件事件0
0x0B6		ELC_SWEVT1	软件事件1
0x0C0	GPT0	GPT0_CCMPA	比较匹配A
0x0C1		GPT0_CCMPB	比较匹配B
0x0C2		GPT0_CMPC	比较匹配C
0x0C3		GPT0_CMPD	比较匹配D
0x0C4		GPT0_CMPE	比较匹配E
0x0C5		GPT0_CMPF	比较匹配F
0x0C6		GPT0_OVF	Overflow
0x0C7		GPT0_UDF	Underflow
0x0C8		GPT0_PC	循环计数功能结束

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Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (3 of 6)

Event number	Interrupt request source	Name	Description
0x0C9	GPT1	GPT1_CCMPA	Compare match A
0x0CA		GPT1_CCMPB	Compare match B
0x0CB		GPT1_CMPC	Compare match C
0x0CC		GPT1_CMPD	Compare match D
0x0CD		GPT1_CMPE	Compare match E
0x0CE		GPT1_CMPF	Compare match F
0x0CF		GPT1_OVF	Overflow
0x0D0		GPT1_UDF	Underflow
0x0D1		GPT1_PC	Cycle count function end
0x0D2	GPT2	GPT2_CCMPA	Compare match A
0x0D3		GPT2_CCMPB	Compare match B
0x0D4		GPT2_CMPC	Compare match C
0x0D5		GPT2_CMPD	Compare match D
0x0D6		GPT2_CMPE	Compare match E
0x0D7		GPT2_CMPF	Compare match F
0x0D8		GPT2_OVF	Overflow
0x0D9		GPT2_UDF	Underflow
0x0DB	GPT3	GPT3_CCMPA	Compare match A
0x0DC		GPT3_CCMPB	Compare match B
0x0DD		GPT3_CMPC	Compare match C
0x0DE		GPT3_CMPD	Compare match D
0x0DF		GPT3_CMPE	Compare match E
0x0E0		GPT3_CMPF	Compare match F
0x0E1		GPT3_OVF	Overflow
0x0E2		GPT3_UDF	Underflow
0x0E4	GPT4	GPT4_CCMPA	Compare match A
0x0E5		GPT4_CCMPB	Compare match B
0x0E6		GPT4_CMPC	Compare match C
0x0E7		GPT4_CMPD	Compare match D
0x0E8		GPT4_CMPE	Compare match E
0x0E9		GPT4_CMPF	Compare match F
0x0EA		GPT4_OVF	Overflow
0x0EB		GPT4_UDF	Underflow
0x0EC		GPT4_PC	Cycle count function end

Table 18.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（3of6）

事件编号	中断请求源	Name	Description
0x0C9	GPT1	GPT1_CCMPA	比较匹配A
0x0CA		GPT1_CCMPB	比较匹配B
0x0CB		GPT1_CMPC	比较匹配C
0x0CC		GPT1_CMPD	比较匹配D
0x0CD		GPT1_CMPE	比较匹配E
0x0CE		GPT1_CMPF	比较匹配F
0x0CF		GPT1_OVF	Overflow
0x0D0		GPT1_UDF	Underflow
0x0D1		GPT1_PC	循环计数功能结束
0x0D2	GPT2	GPT2_CCMPA	比较匹配A
0x0D3		GPT2_CCMPB	比较匹配B
0x0D4		GPT2_CMPC	比较匹配C
0x0D5		GPT2_CMPD	比较匹配D
0x0D6		GPT2_CMPE	比较匹配E
0x0D7		GPT2_CMPF	比较匹配F
0x0D8		GPT2_OVF	Overflow
0x0D9		GPT2_UDF	Underflow
0x0DB	GPT3	GPT3_CCMPA	比较匹配A
0x0DC		GPT3_CCMPB	比较匹配B
0x0DD		GPT3_CMPC	比较匹配C
0x0DE		GPT3_CMPD	比较匹配D
0x0DF		GPT3_CMPE	比较匹配E
0x0E0		GPT3_CMPF	比较匹配F
0x0E1		GPT3_OVF	Overflow
0x0E2		GPT3_UDF	Underflow
0x0E4	GPT4	GPT4_CCMPA	比较匹配A
0x0E5		GPT4_CCMPB	比较匹配B
0x0E6		GPT4_CMPC	比较匹配C
0x0E7		GPT4_CMPD	比较匹配D
0x0E8		GPT4_CMPE	比较匹配E
0x0E9		GPT4_CMPF	比较匹配F
0x0EA		GPT4_OVF	Overflow
0x0EB		GPT4_UDF	Underflow
0x0EC		GPT4_PC	循环计数功能结束

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Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (4 of 6)

Event number	Interrupt request source	Name	Description
0x0ED	GPT5	GPT5_CCMPA	Compare match A
0x0EE		GPT5_CCMPB	Compare match B
0x0EF		GPT5_CMPC	Compare match C
0x0F0		GPT5_CMPD	Compare match D
0x0F1		GPT5_CMPE	Compare match E
0x0F2		GPT5_CMPF	Compare match F
0x0F3		GPT5_OVF	Overflow
0x0F4		GPT5_UDF	Underflow
0x0F5		GPT5_PC	Cycle count function end
0x0F6	GPT6	GPT6_CCMPA	Compare match A
0x0F7		GPT6_CCMPB	Compare match B
0x0F8		GPT6_CMPC	Compare match C
0x0F9		GPT6_CMPD	Compare match D
0x0FA		GPT6_CMPE	Compare match E
0x0FB		GPT6_CMPF	Compare match F
0x0FC		GPT6_OVF	Overflow
0x0FD		GPT6_UDF	Underflow
0x0FE		GPT6_PC	Cycle count function end
0x0FF	GPT7	GPT7_CCMPA	Compare match A
0x100		GPT7_CCMPB	Compare match B
0x101		GPT7_CMPC	Compare match C
0x102		GPT7_CMPD	Compare match D
0x103		GPT7_CMPE	Compare match E
0x104		GPT7_CMPF	Compare match F
0x105		GPT7_OVF	Overflow
0x106		GPT7_UDF	Underflow
0x108	GPT8	GPT8_CCMPA	Compare match A
0x109		GPT8_CCMPB	Compare match B
0x10A		GPT8_CMPC	Compare match C
0x10B		GPT8_CMPD	Compare match D
0x10C		GPT8_CMPE	Compare match E
0x10D		GPT8_CMPF	Compare match F
0x10E		GPT8_OVF	Overflow
0x10F		GPT8_UDF	Underflow

Table 18.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（4of6）

事件编号	中断请求源	Name	Description
0x0ED	GPT5	GPT5_CCMPA	比较匹配A
0x0EE		GPT5_CCMPB	比较匹配B
0x0EF		GPT5_CMPC	比较匹配C
0x0F0		GPT5_CMPD	比较匹配D
0x0F1		GPT5_CMPE	比较匹配E
0x0F2		GPT5_CMPF	比较匹配F
0x0F3		GPT5_OVF	Overflow
0x0F4		GPT5_UDF	Underflow
0x0F5		GPT5_PC	循环计数功能结束
0x0F6	GPT6	GPT6_CCMPA	比较匹配A
0x0F7		GPT6_CCMPB	比较匹配B
0x0F8		GPT6_CMPC	比较匹配C
0x0F9		GPT6_CMPD	比较匹配D
0x0FA		GPT6_CMPE	比较匹配E
0x0FB		GPT6_CMPF	比较匹配F
0x0FC		GPT6_OVF	Overflow
0x0FD		GPT6_UDF	Underflow
0x0FE		GPT6_PC	循环计数功能结束
0x0FF	GPT7	GPT7_CCMPA	比较匹配A
0x100		GPT7_CCMPB	比较匹配B
0x101		GPT7_CMPC	比较匹配C
0x102		GPT7_CMPD	比较匹配D
0x103		GPT7_CMPE	比较匹配E
0x104		GPT7_CMPF	比较匹配F
0x105		GPT7_OVF	Overflow
0x106		GPT7_UDF	Underflow
0x108	GPT8	GPT8_CCMPA	比较匹配A
0x109		GPT8_CCMPB	比较匹配B
0x10A		GPT8_CMPC	比较匹配C
0x10B		GPT8_CMPD	比较匹配D
0x10C		GPT8_CMPE	比较匹配E
0x10D		GPT8_CMPF	比较匹配F
0x10E		GPT8_OVF	Overflow
0x10F		GPT8_UDF	Underflow

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Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (5 of 6)

Event number	Interrupt request source	Name	Description
0x111	GPT9	GPT9_CCMPA	Compare match A
0x112		GPT9_CCMPB	Compare match B
0x113		GPT9_CMPC	Compare match C
0x114		GPT9_CMPD	Compare match D
0x115		GPT9_CMPE	Compare match E
0x116		GPT9_CMPF	Compare match F
0x117		GPT9_OVF	Overflow
0x118		GPT9_UDF	Underflow
0x150	GPT	GPT_UVWEDGE	UVW edge event
0x160	ADC12	ADC120_ADI	A/D scan end interrupt
0x164		ADC120_WCMPM*4	Compare match
0x165		ADC120_WCMPUM*4	Compare mismatch
0x166		ADC121_ADI	A/D scan end interrupt
0x16A		ADC121_WCMPM*4	Compare match
0x16B		ADC121_WCMPUM*4	Compare mismatch
0x180	SCI0	SCI0_RXI*2	Receive data full
0x181		SCI0_TXI*2	Transmit data empty
0x182		SCI0_TEI*2	Transmit end
0x183		SCI0_ERI	Receive error
0x184		SCI0_AM	Address match event
0x186	SCI1	SCI1_RXI*2	Received data full
0x187		SCI1_TXI*2	Transmit data empty
0x188		SCI1_TEI*2	Transmit end
0x189		SCI1_ERI	Receive error
0x18C	SCI2	SCI2_RXI*2	Received data full
0x18D		SCI2_TXI*2	Transmit data empty
0x18E		SCI2_TEI*2	Transmit end
0x18F		SCI2_ERI	Receive error
0x192	SCI3	SCI3_RXI*2	Received data full
0x193		SCI3_TXI*2	Transmit data empty
0x194		SCI3_TEI*2	Transmit end
0x195		SCI3_ERI	Receive error
0x196		SCI3_AM	Address match event
0x198	SCI4	SCI4_RXI*2	Received data full
0x199		SCI4_TXI*2	Transmit data empty
0x19A		SCI4_TEI*2	Transmit end
0x19B		SCI4_ERI	Receive error
0x19C		SCI4_AM	Address match event
0x19E	SCI5	SCI5_RXI*2	Received data full
0x19F		SCI5_TXI*2	Transmit data empty

Table 18.3 在ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（5of6）

事件编号	中断请求源	Name	Description
0x111	GPT9	GPT9_CCMPA	比较匹配A
0x112		GPT9_CCMPB	比较匹配B
0x113		GPT9_CMPC	比较匹配C
0x114		GPT9_CMPD	比较匹配D
0x115		GPT9_CMPE	比较匹配E
0x116		GPT9_CMPF	比较匹配F
0x117		GPT9_OVF	Overflow
0x118		GPT9_UDF	Underflow
0x150	GPT	GPT_UVWEDGE	UVW边缘事件
0x160	ADC12	ADC120_ADI	AD扫描结束中断
0x164		ADC120_WCMPM*4	比较匹配
0x165		ADC120_WCMPUM*4	比较不匹配
0x166		ADC121_ADI	AD扫描结束中断
0x16A		ADC121_WCMPM*4	比较匹配
0x16B		ADC121_WCMPUM*4	比较不匹配
0x180	SCI0	SCI0_RXI*2	接收数据已满
0x181		SCI0_TXI*2	传输数据为空
0x182		SCI0_TEI*2	发射端
0x183		SCI0_ERI	接收错误
0x184		SCI0_AM	地址匹配事件
0x186	SCI1	SCI1_RXI*2	接收数据已满
0x187		SCI1_TXI*2	传输数据为空
0x188		SCI1_TEI*2	发射端
0x189		SCI1_ERI	接收错误
0x18C	SCI2	SCI2_RXI*2	接收数据已满
0x18D		SCI2_TXI*2	传输数据为空
0x18E		SCI2_TEI*2	发射端
0x18F		SCI2_ERI	接收错误
0x192	SCI3	SCI3_RXI*2	接收数据已满
0x193		SCI3_TXI*2	传输数据为空
0x194		SCI3_TEI*2	发射端
0x195		SCI3_ERI	接收错误
0x196		SCI3_AM	地址匹配事件
0x198	SCI4	SCI4_RXI*2	接收数据已满
0x199		SCI4_TXI*2	传输数据为空
0x19A		SCI4_TEI*2	发射端
0x19B		SCI4_ERI	接收错误
0x19C		SCI4_AM	地址匹配事件
0x19E	SCI5	SCI5_RXI*2	接收数据已满
0x19F		SCI5_TXI*2	传输数据为空

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Table 18.3 Association between event signal names set in ELSRn.ELS[8:0] bits and signal numbers (6 of 6)

Event number	Interrupt request source	Name	Description
0x1A0		SCI5_TEI*2	Transmit end
0x1A1		SCI5_ERI	Receive error
0x1A2		SCI5_AM	Address match event
0x1A4	SCI6	SCI6_RXI*2	Received data full
0x1A5		SCI6_TXI	Transmit data empty
0x1A6		SCI6_TEI*2	Transmit end
0x1A7		SCI6_ERI	Receive error
0x1A8		SCI6_AM	Address match event
0x1AA	SCI7	SCI7_RXI*2	Received data full
0x1AB		SCI7_TXI*2	Transmit data empty
0x1AC		SCI7_TEI*2	Transmit end
0x1AD		SCI7_ERI	Receive error
0x1AE		SCI7_AM	Address match event
0x1B0	SCI8	SCI8_RXI*2	Received data full
0x1B1		SCI8_TXI*2	Transmit data empty
0x1B2		SCI8_TEI*2	Transmit end
0x1B3		SCI8_ERI	Receive error
0x1B4		SCI8_AM	Address match event
0x1B6	SCI9	SCI9_RXI*2	Received data full
0x1B7		SCI9_TXI*2	Transmit data empty
0x1B8		SCI9_TEI*2	Transmit end
0x1B9		SCI9_ERI	Receive error
0x1BA		SCI9_AM	Address match event
0x1C4	SPI0	SPI0_SPRI	Receive buffer full
0x1C5		SPI0_SPTI	Transmit buffer empty
0x1C6		SPI0_SPII	Idle
0x1C7		SPI0_SPEI	Error
0x1C8		SPI0_SPCEND	Communication complete event
0x1C9	SPI1	SPI1_SPRI	Receive buffer full
0x1CA		SPI1_SPTI	Transmit buffer empty
0x1CB		SPI1_SPII	Idle
0x1CC		SPI1_SPEI	Error
0x1CD		SPI1_SPCEND	Transmission complete event
0x1DB	DOC	DOC_DOPCI*4	Data operation circuit interrupt

Note 1. Only pulse (edge detection) is supported.
Note 2. This event is not supported in FIFO mode.
Note 3. ELSR8 to ELSR11, ELSR14 to ELSR17, and ELSR18 can select this event.
Note 4. This event can occur in Snooze mode.

Table 18.3 ELSRn.ELS[8:0]位中设置的事件信号名称与信号编号之间的关联（6个中的6个）

事件编号	中断请求源	Name	Description
0x1A0		SCI5_TEI*2	发射端
0x1A1		SCI5_ERI	接收错误
0x1A2		SCI5_AM	地址匹配事件
0x1A4	SCI6	SCI6_RXI*2	接收数据已满
0x1A5		SCI6_TXI	传输数据为空
0x1A6		SCI6_TEI*2	发射端
0x1A7		SCI6_ERI	接收错误
0x1A8		SCI6_AM	地址匹配事件
0x1AA	SCI7	SCI7_RXI*2	接收数据已满
0x1AB		SCI7_TXI*2	传输数据为空
0x1AC		SCI7_TEI*2	发射端
0x1AD		SCI7_ERI	接收错误
0x1AE		SCI7_AM	地址匹配事件
0x1B0	SCI8	SCI8_RXI*2	接收数据已满
0x1B1		SCI8_TXI*2	传输数据为空
0x1B2		SCI8_TEI*2	发射端
0x1B3		SCI8_ERI	接收错误
0x1B4		SCI8_AM	地址匹配事件
0x1B6	SCI9	SCI9_RXI*2	接收数据已满
0x1B7		SCI9_TXI*2	传输数据为空
0x1B8		SCI9_TEI*2	发射端
0x1B9		SCI9_ERI	接收错误
0x1BA		SCI9_AM	地址匹配事件
0x1C4	SPI0	SPI0_SPRI	接收缓冲区已满
0x1C5		SPI0_SPTI	发送缓冲区为空
0x1C6		SPI0_SPII	Idle
0x1C7		SPI0_SPEI	Error
0x1C8		SPI0_SPCEND	通讯完成事件
0x1C9	SPI1	SPI1_SPRI	接收缓冲区已满
0x1CA		SPI1_SPTI	发送缓冲区为空
0x1CB		SPI1_SPII	Idle
0x1CC		SPI1_SPEI	Error
0x1CD		SPI1_SPCEND	传输完成事件
0x1DB	DOC	DOC_DOPCI*4	数据运算电路中断

注1.仅支持脉冲（边沿检测）。注2.FIFO模式不支持此事件。
注3.ELSR8到ELSR11、ELSR14到ELSR17和ELSR18可以选择此事件。
注4.此事件可能在贪睡模式下发生。

18.2.4 ELCSARA : Event Link Controller Security Attribution Register A

Base address: ELC = 0x4008_2000

Offset address: 0x74

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSEGR1	ELSEGR0	ELCR
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	ELCR	Event Link Controller Register Security Attribution Target register: ELCR 0: Secure 1: Non-secure	R/W
1	ELSEGR0	Event Link Software Event Generation Register 0 Security Attribution 0: Secure 1: Non-secure	R/W
2	ELSEGR1	Event Link Software Event Generation Register 1 Security Attribution 0: Secure 1: Non-secure	R/W
15:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The ELCR register controls operation of the ELC.

18.2.5 ELCSARB : Event Link Controller Security Attribution Register B

Base address: ELC = 0x4008_2000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ELSR[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	ELSR[15:0]	Event Link Setting Register n Security Attribution Target register: ELSRn (n = 0 to 15) 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

This register specifies the security attribution for the Register ELSRn (n = 0 to 15).

18.2.4 ELCSARA:事件链接控制器安全属性寄存器A

Base address: ELC = 0x4008_2000

Offset address: 0x74

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSEGR1	ELSEGR0	ELCR
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	ELCR	事件链接控制器注册安全属性 Target register: ELCR 0: Secure 1: Non-secure	R/W
1	ELSEGR0	事件链接软件事件生成寄存器0安全属性 0: Secure 1: Non-secure	R/W
2	ELSEGR1	事件链接软件事件生成寄存器1安全属性 0: Secure 1: Non-secure	R/W
15:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

ELCR寄存器控制ELC的操作。

18.2.5 ELCSARB:事件链接控制器安全属性寄存器B

Base address: ELC = 0x4008_2000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ELSR[15:0]															
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	ELSR[15:0]	事件链接设置寄存器n安全属性 目标寄存器：ELSRn（n=0到15） 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

该寄存器指定寄存器ELSRn（n=0到15）的安全属性。

18.2.6 ELCSARC : Event Link Controller Security Attribution Register C

Base address: ELC = 0x4008_2000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSR[18:16]		
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
2:0	ELSR[18:16]	Event Link Setting Register n Security Attribution (n = 16 to 18) Target register: ELSRn (n = 16 to 18) 0: Secure 1: Non-secure	R/W
15:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

This register specifies the security attribution for the Register ELSRn (n = 16 to 18)

18.3 Operation

18.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

18.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 18.4 lists the operations of modules when an event occurs.

Table 18.4 Module operations when event occurs

Module	Operations When Event is Input
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture
DAC12	Start D/A conversion
I/O Ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT 1 PORT 2 PORT 3 PORT 4
CTSU	Start measurement operation
ADC12	Start A/D conversion
DTC	Start DTC data transfer

18.3.3 Example of Procedure for Linking Events

To link events:

18.2.6 ELCSARC:事件链接控制器安全属性寄存器C

Base address: ELC = 0x4008_2000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	ELSR[18:16]		
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
2:0	ELSR[18:16]	事件链接设置寄存器n安全属性（n=16到18） 目标寄存器：ELSRn（n=16到18） 0: Secure 1: Non-secure	R/W
15:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

该寄存器指定寄存器ELSRn的安全属性（n=16到18）

18.3 Operation

18.3.1 中断处理和事件链接的关系

事件链接的事件编号与关联中断源的事件编号相同。有关生成事件信号的信息，请参阅每个事件源模块的章节中的说明。

18.3.2 链接事件

当事件发生并且该事件已在事件链接设置寄存器(ELSRn)中设置为触发器时，将激活相关模块。模块的操作必须提前设置好。表18.4列出了事件发生时模块的操作。

Table 18.4 事件发生时的模块操作

Module	输入事件时的操作
GPT	• 开始计数 • 停止计数 • 清除计数 • 向上计数 • 向下计数 • 输入捕捉
DAC12	开始DA转换
I/O Ports	• 根据EORR（复位）或EOSR（设置）更改引脚输出 • EIDR的锁存器引脚状态 • 以下端口可用于ELC： PORT 1 PORT 2 PORT 3 PORT 4
CTSU	开始测量操作
ADC12	开始AD转换
DTC	开始DTC数据传输

18.3.3 链接事件的过程示例

链接事件：

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn.ELS[8:0] bits for the module to be linked.
3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 0 to the ELSRn.ELS[8:0] bit associated with the modules. To stop linkage of all the events, set the ELCR.ELCON bit to 0.

If event link output from the RTC is to be used, set the ELC after the RTC settings, for example, for initialization and time setting. Unintended events may be generated if RTC settings are made after the ELC settings.

If event link output from the LVD is to be used, set the ELC after setting the LVD. To disable the LVD, do so after setting 0x00 to the associated ELSRn register.

18.4 Usage Notes

18.4.1 Linking DMAC/DTC Transfer End Signals as Events

When linking the DMAC/DTC transfer end signals as events, do not set the same peripheral module as the DMAC/DTC transfer destination and event link destination. If set, the peripheral module might be started before DMAC/DTC transfer to the peripheral module is complete.

18.4.2 Setting Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in low power mode in which the module is stopped (Software Standby mode or Deep Software Standby mode).

Some modules can perform in Snooze mode. For more information, see Table 18.3 and section 10, Low Power Modes.

18.4.3 Module-Stop Function Setting

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register. For more information, see Table 18.3 and section 10, Low Power Modes.

18.4.4 ELC Delay Time

In Figure 18.2, module A accesses module B through the ELC. There is a delay time in the ELC between module A and module B. Table 18.5 shows the ELC delay time.

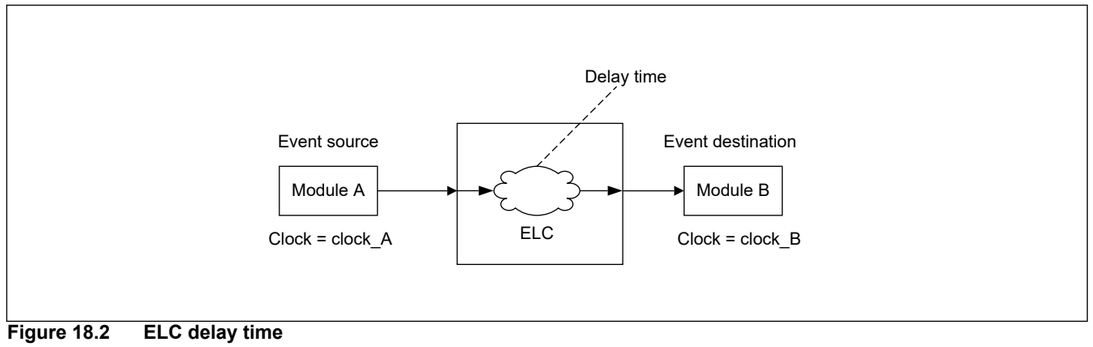


Figure 18.2 ELC delay time

1.设置要链接事件的模块的操作。

2.为要链接的模块设置适当的ELSRn.ELS[8:0]位。

3.将ELCR.ELCON位设置为1以启用所有事件的链接。

4.配置输出事件的模块并激活模块。两个模块之间的链接现在处于活动状态。

5.要单独停止模块的事件链接，请将与模块关联的ELSRn.ELS[8:0]位设置为0。要停止所有事件的链接，请将ELCR.ELCON位设置为0。

如果要使用RTC的事件链接输出，请在RTC设置之后设置ELC，例如，用于初始化和时间设置。如果在ELC设置之后进行RTC设置，则可能会产生意外事件。

如果要使用来自LVD的事件链接输出，请在设置LVD后设置ELC。要禁用LVD，请在将0x00设置为相关的ELSRn寄存器后执行此操作。

18.4 使用说明

18.4.1 将DMACDTC传输结束信号作为事件链接

将DMACDTC传输结束信号作为事件链接时，请勿将外设模块设置为DMACDTC传输目标和事件链接目标。如果设置，则外围模块可能会在DMACDTC传输到外围模块完成之前启动。

18.4.2 设置时钟

要链接事件，您必须启用ELC和相关模块。如果相关模块处于模块停止状态或模块停止的低功耗模式（软件待机模式或深度软件待机模式），则模块无法运行。

某些模块可以在贪睡模式下执行。有关详细信息，请参阅表18.3和第10节，低功耗模式。

18.4.3 模块停止功能设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用ELC操作。ELC在复位后最初停止。释放模块停止状态可以访问寄存器。在使用模块停止控制寄存器禁用ELC操作之前，必须将ELCON位设置为0。有关详细信息，请参阅表18.3和第10节，低功耗模式。

18.4.4 ELC延迟时间

在图18.2中，模块A通过ELC访问模块B。模块A和模块B之间的ELC中有一个延迟时间。表18.5显示了ELC延迟时间。

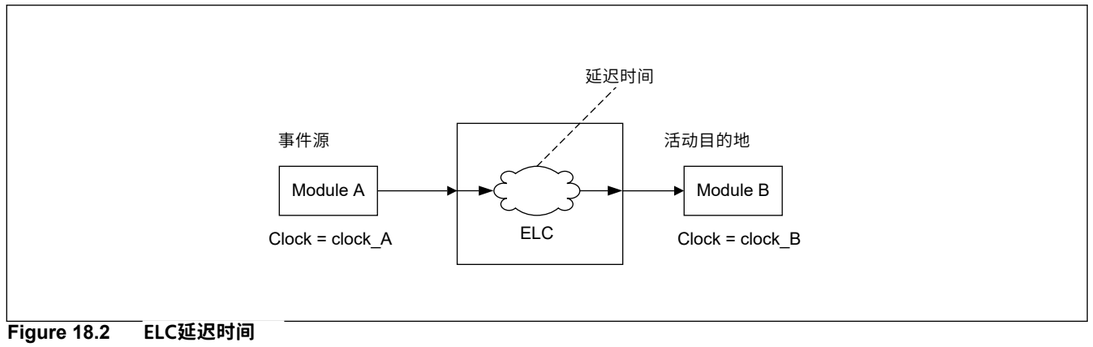


Figure 18.2 ELC延迟时间

Table 18.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of clock_B
	clock_A < clock_B	1 cycle to 2 cycles of clock_A

Table 18.5 ELC延迟时间

时钟域	时钟频率	ELC延迟时间
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1个周期到2个周期
	clock_A > clock_B	1个周期到2个clock_B周期
	clock_A < clock_B	1个周期到2个clock_A周期

RA生态工作室

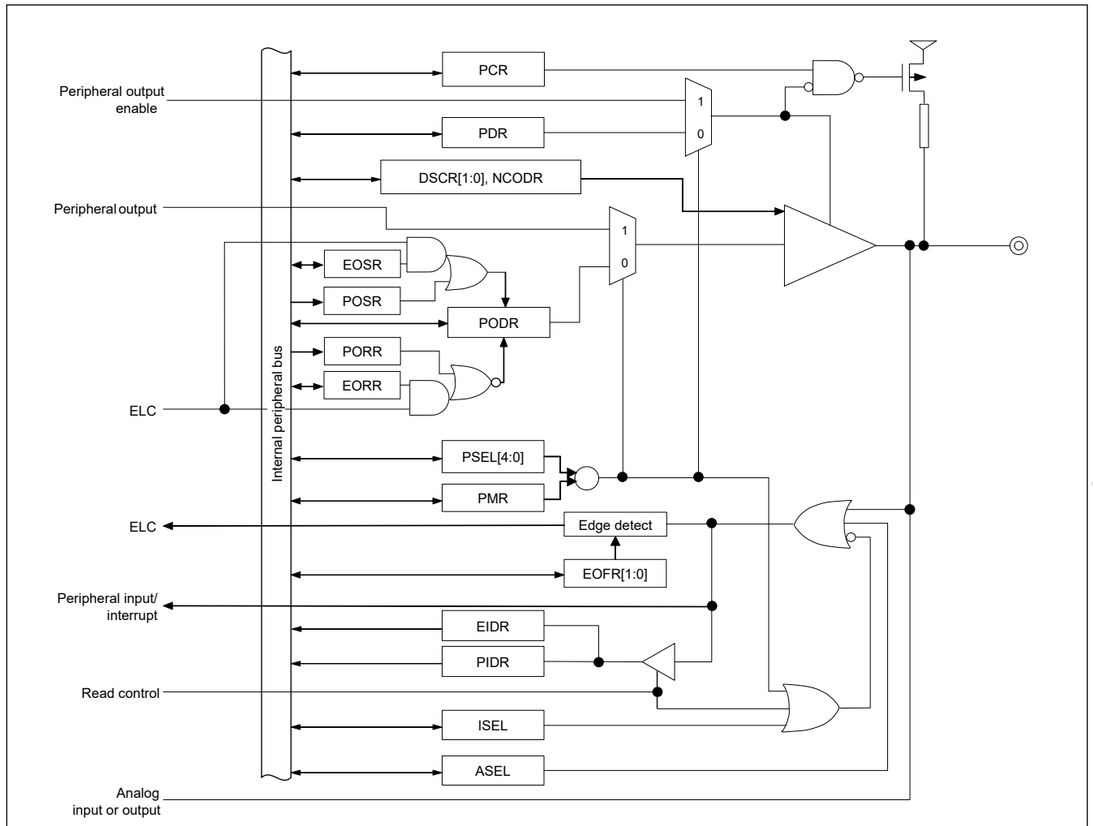
19. I/O Ports

19.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for the ELC, or bus control pins.

All pins except P109 (as TDO of JTAG ports) operate as input pins immediately after a reset, and pin functions are switched by register settings. The I/O ports and peripheral modules for each pin are specified in the associated registers.

Figure 19.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs for different packages. Table 19.1 lists the I/O port specifications by package, and Table 19.2 lists the port functions.



Note: This figure shows a basic port configuration. The configuration differs depending on the ports.

Figure 19.1 Connection diagram for I/O port registers

Table 19.1 I/O port specifications (1 of 2)

Port	Package 176 pins	Number of pins	Package 144 pins	Number of pins	Package 100 pins	Number of pins
PORT0	P000 to P010, P014, P015	13	P000 to P009, P014, P015	12	P000 to P008, P014, P015	11
PORT1	P100 to P115	16	P100 to P115	16	P100 to P115	16
PORT2	P200 to P214	15	P200 to P214	15	P200,P201, P205 to P214	12

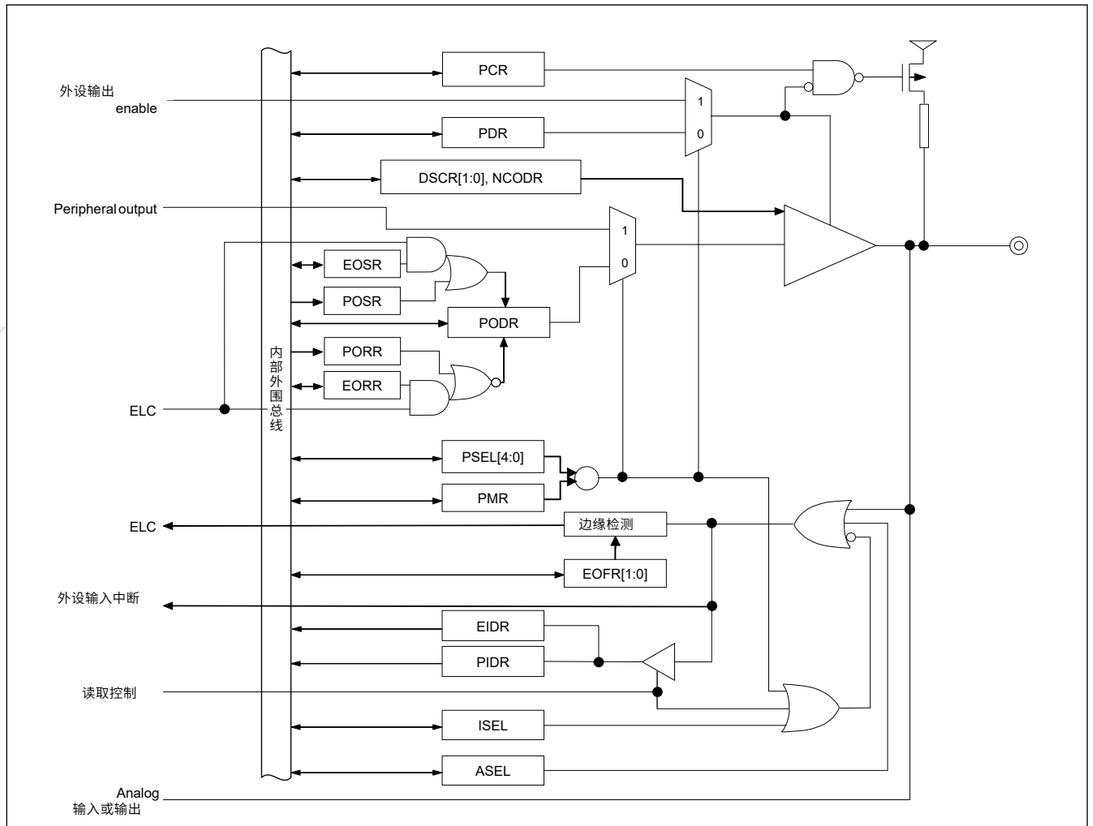
19. I/O Ports

19.1 Overview

IO端口引脚用作通用IO端口引脚、外围模块的IO引脚、中断输入引脚、模拟IO、ELC的端口组功能或总线控制引脚。

除P109外的所有引脚（作为JTAG端口的TDO）在复位后立即作为输入引脚工作，引脚功能通过寄存器设置切换。每个引脚的IO端口和外围模块在相关寄存器中指定。

图19.1显示了IO端口寄存器的连接图。不同封装的IO端口配置不同。表19.1按封装列出了IO端口规格，表19.2列出了端口功能。



Note: 此图显示了基本端口配置。配置因端口而异。

Figure 19.1 IO端口寄存器的连接图

Table 19.1 IO端口规格(1of2)

Port	Package 176 pins	引脚数	Package 144 pins	引脚数	Package 100 pins	引脚数
PORT0	P000 to P010, P014, P015	13	P000 to P009, P014, P015	12	P000 to P008, P014, P015	11
PORT1	P100 to P115	16	P100 to P115	16	P100 to P115	16
PORT2	P200 to P214	15	P200 to P214	15	P200,P201, P205 to P214	12

Table 19.1 I/O port specifications (2 of 2)

Port	Package 176 pins	Number of pins	Package 144 pins	Number of pins	Package 100 pins	Number of pins
PORT3	P300 to P315	16	P300 to P313	14	P300 to P307	8
PORT4	P400 to P415	16	P400 to P415	16	P400 to P415	16
PORT5	P500 to P508,P511 to P513	12	P500 to P507,P511, P512	10	P500 to P505	6
PORT6	P600 to P615	16	P600 to P605, P608 to P614	13	P600 to P602, P608 to P610	6
PORT7	P700 to P708	9	P700 to P705, P708 to P713	12	P708	1
PORT8	P800to P806	7	P800, P801	2	—	0
PORT9	P900, P901,P905 to P908	6	—	0	—	0
PORTA	PA00, PA01,PA08 to PA10	5	—	0	—	0
PORTB	PB00, PB01	2	—	0	—	0

Table 19.2 I/O port functions

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5V tolerant	I/O
PORT0	P000 to P010, P014, P015	✓	✓	Low	—	Input / Output
PORT1	P100 to P107	✓	✓	Low, middle, high, high speed, high drive	—	Input / Output
	P108 to P115	✓	✓	Low, middle, high	—	Input / Output
PORT2	P200	✓	—	—	—	Input
	P201	✓	✓	Low	—	Input / Output
	P202 to P204, P207, P212, P213	✓	✓	Low, middle, high	—	Input / Output
	P208 to P211, P214	✓	✓	Low, middle, high, high speed, high drive	—	Input / Output
	P205, P206	✓	✓	Low, middle, high	✓	Input / Output
PORT3	P300 to P315	✓	✓	Low, middle, high	—	Input / Output
PORT4	P400, P401, P407 to P415	✓	✓	Low, middle, high	✓	Input / Output
	P402 to P406	✓	✓	Low, middle, high	—	Input / Output
PORT5	P500 to P508, P513	✓	✓	Low, middle, high	—	Input / Output
	P511, P512	✓	✓	Low, middle, high	✓	Input / Output
PORT6	P600, P601	✓	✓	Low, middle, high, high speed high drive	—	Input / Output
	P602 to P615	✓	✓	Low, middle, high, high speed, high drive	—	Input / Output
PORT7	P700 to P707	✓	✓	Low, middle, high	—	Input / Output
	P708 to P713	✓	✓	Low, middle, high	✓	Input / Output
PORT8	P800 to P806	✓	✓	Low, middle, high	—	Input / Output
PORT9	P900, P901, P905 to P908	✓	✓	Low, middle, high	—	Input / Output
PORTA	PA00, PA01, PA08 to PA10	✓	✓	Low, middle, high	—	Input / Output
PORTB	PB00	✓	✓	Low, middle, high	—	Input / Output
	PB01	✓	✓	Low, middle, high	✓	Input / Output

Note: ✓: Available
—: Setting prohibited

Table 19.1 IO端口规格(2of2)

Port	Package 176 pins	引脚数	Package 144 pins	引脚数	Package 100 pins	引脚数
PORT3	P300 to P315	16	P300 to P313	14	P300 to P307	8
PORT4	P400 to P415	16	P400 to P415	16	P400 to P415	16
PORT5	P500 to P508,P511 to P513	12	P500 to P507,P511, P512	10	P500 to P505	6
PORT6	P600 to P615	16	P600 to P605, P608 to P614	13	P600 to P602, P608 to P610	6
PORT7	P700 to P708	9	P700 to P705, P708 to P713	12	P708	1
PORT8	P800to P806	7	P800, P801	2	—	0
PORT9	P900, P901,P905 to P908	6	—	0	—	0
PORTA	PA00, PA01,PA08 to PA10	5	—	0	—	0
PORTB	PB00, PB01	2	—	0	—	0

Table 19.2 IO口功能

Port	端口名称	Input pull-up	Open-drain output	驱动容量切换	5V tolerant	I/O
PORT0	P000 to P010, P014, P015	✓	✓	Low	—	输入输出
PORT1	P100 to P107	✓	✓	低、中、高、高速、高驱动	—	输入输出
	P108 to P115	✓	✓	低、中、高	—	输入输出
PORT2	P200	✓	—	—	—	Input
	P201	✓	✓	Low	—	输入输出
	P202 to P204, P207, P212, P213	✓	✓	低、中、高	—	输入输出
	P208 to P211, P214	✓	✓	低、中、高、高速、高驱动	—	输入输出
	P205, P206	✓	✓	低、中、高	✓	输入输出
PORT3	P300 to P315	✓	✓	低、中、高	—	输入输出
PORT4	P400, P401, P407 to P415	✓	✓	低、中、高	✓	输入输出
	P402 to P406	✓	✓	低、中、高	—	输入输出
PORT5	P500 to P508, P513	✓	✓	低、中、高	—	输入输出
	P511, P512	✓	✓	低、中、高	✓	输入输出
PORT6	P600, P601	✓	✓	低、中、高速、高速高速驱动	—	输入输出
	P602 to P615	✓	✓	低、中、高、高速、高驱动	—	输入输出
PORT7	P700 to P707	✓	✓	低、中、高	—	输入输出
	P708 to P713	✓	✓	低、中、高	✓	输入输出
PORT8	P800 to P806	✓	✓	低、中、高	—	输入输出
PORT9	P900, P901, P905 to P908	✓	✓	低、中、高	—	输入输出
PORTA	PA00, PA01, PA08 to PA10	✓	✓	低、中、高	—	输入输出
PORTB	PB00	✓	✓	低、中、高	—	输入输出
	PB01	✓	✓	低、中、高	✓	输入输出

Note: :可用—:禁止设置

RA生态工作室

19.2 Register Descriptions

19.2.1 PCNTR1/PODR/PDR : Port Control Register 1

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 9, A, B)

Offset address: 0x000 (PCNTR1/PODR)
0x002 (PDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W*1
31:16	PODR15 to PODR00	Pmn Output Data 0: Low output 1: High output	R/W*2

Note: m = 0 to 9, A, B, n = 00 to 15
Note 1. If the security attribution is configured as Secure,
- Secure access and Non-secure read access are allowed,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note 2. If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

The Port Control Register 1 (PCNTR1/PODR/PDR) is a 32-bit or 16-bit read/write register that controls port direction and port output data. The PCNTR1 specifies the port direction and output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

PDRn bits (Pmn Direction)

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit unit. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0. In the case of input only ports, PDRn bits are reserved. See Table 19.2. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

PODRn bits (Pmn Output Data)

The PODRn bits hold data to be output from the general I/O pins. Bits of non-existent port m are reserved. Reserved bits are read as 0. The write value should be 0. In the case of input only ports, PODRn bits are reserved. See Table 19.2. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

19.2 注册说明

19.2.1 PCNTR1PODRPDR:端口控制寄存器1

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 9, A, B)

Offset address: 0x000 (PCNTR1/PODR)
0x002 (PDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	PDR15 to PDR00	Pmn Direction 0：输入（用作输入引脚）1：输出（用作输出引脚）	R/W*1
31:16	PODR15 to PODR00	Pmn输出数据 0：低输出1：高输出	R/W*2

Note: m = 0 to 9, A, B, n = 00 to 15
注1.如果安全属性配置为Secure，●
允许安全访问和非安全读取访问，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

注2.如果安全属性配置为Secure，●
允许安全访问，
- 非安全读取值为0，但不会产生TrustZone访问错误，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

端口控制寄存器1(PCNTR1PODRPDR)是一个32位或16位读写寄存器，用于控制端口方向和端口输出数据。PCNTR1指定端口方向和输出数据，并以32位为单位进行访问。PDRn（PCNTR1中的位[15:0]）和PODRn（PCNTR1中的位[31:16]）分别以16位为单位进行访问。

PDRn bits (Pmn Direction)

当引脚配置为通用IO引脚时，PDRn位选择相关端口上各个引脚的输入或输出方向。端口m上的每个引脚都与一个PORTm.PCNTR1.PDRn位相关联。可以以1位为单位指定IO方向。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。在仅输入端口的情况下，保留PDRn位。见表19.2。PORTm.PCNTR1寄存器中的PDRn位与PFS.PmnPFS寄存器中的PDR位具有相同的功能。

PODRn位（Pmn输出数据）

PODRn位保存要从通用IO引脚输出的数据。不存在的端口m的位被保留。保留位读取为0。写入值应为0。在仅输入端口的情况下，保留PODRn位。见表19.2。PORTm.PCNTR1寄存器中的PODRn位与PFS.PmnPFS寄存器中的PODR位具有相同的功能。

19.2.2 PCNTR2/EIDR/PIDR : Port Control Register 2

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 9, A, B)

Offset address: 0x004 (PCNTR2/EIDR)
0x006 (PIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0: Low level 1: High level	R
31:16	EIDR15 to EIDR00 *2	Port Event Input Data*1 When an ELC_PORTx signal occurs 0: Low input 1: High input	R

Note: If the security attribution is configured as Secure,
- Secure read access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure read access are allowed.

Note: m = 0 to 9, A, B, n = 00 to 15
Note 1. x = 1, 2, 3 or 4 for EIDR only
Note 2. Supported by ports 1, 2, 3 or 4.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and the port event input data, and is accessed in 32-bit units.

The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

PIDRn bits (Pmn State)

The PIDRn bits reflect the individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- RTC Time Capture input (RTCIC)
- CS area controller (CSC)
- Analog function (ASEL = 1)
- Capacitive Touch Sensing Unit (CTSU)

EIDRn bits (Port Event Input Data)

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

19.2.2 PCNTR2EIDRPIDR：端口控制寄存器2

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 9, A, B)

Offset address: 0x004 (PCNTR2/EIDR)
0x006 (PIDR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	PIDR15 to PIDR00	Pmn State 0：低电平1 ：高电平	R
31:16	EIDR15 to EIDR00 *2	端口事件输入数据*1 当发生ELC_PORTx信号时 0：低输入1 ：高输入	R

Note: 如果安全属性配置为安全，●
允许安全读取访问，
- 非安全读取值为0，但不会产生TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全读取访问。

Note: m = 0 to 9, A, B, n = 00 to 15
注1.x=1、2、3或4仅适用于EIDR
注2.端口1、2、3或4支持。

端口控制寄存器2(PCNTR2EIDRPIDR)允许使用32位或16位访问对Pmn状态和端口事件输入数据进行读取访问。

PCNTR2指定Pmn状态和端口事件输入数据，并以32位为单位进行访问。

PIDRn（PCNTR2中的位[15:0]）和EIDRn（PCNTR2中的位[31:16]）分别以16位为单位进行访问。与不存在的引脚相关的位被保留。保留位被读取为未定义。

PIDRn bits (Pmn State)

PIDRn位反映端口的各个引脚状态，与PmnPFS.PMR和
PORTm.PCNTR1.PDRn。PORTm.PCNTR2寄存器中的PIDRn位与
PFS.PmnPFS register.

当启用以下功能之一时，引脚状态无法反映在PIDRn中：

- ●RTC时间捕捉输入(RTCIC)
- ●CS区域控制器（CSC）
- ●模拟功能（ASEL=1）
- ●电容式触控感应单元(CTSU)

EIDRn位（端口事件输入数据）

当ELC_PORTx信号出现时，EIDRn位锁存引脚状态。引脚状态只能输入到EIDRn时
PmnPFS.PMR和PORTm.PCNTR1.PDRn为0。当PmnPFS.ASEL位设置为1时，相关引脚状态不会反映在EIDRn中。

19.2.3 PCNTR3/PORR/POSR : Port Control Register 3

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 9, A, B)

Offset address: 0x008 (PCNTR3/PORR)
0x00A (POSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn Output Set 0: No effect on output 1: High output	W
31:16	PORR15 to PORR00	Pmn Output Reset 0: No effect on output 1: Low output	W

Note: If the security attribution is configured as Secure,
- Secure write access is allowed,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure write access are allowed.

Note: m = 0 to 9, A, B, n = 00 to 15

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit or 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units.

The POSRn (bits [15:0] in PCNTR3) and the PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSRn bits (Pmn Output Set)

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 = 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, POSRn bits are reserved. See Table 19.2.

PORRn bits (Pmn Output Reset)

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.PORR00 = 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, PORRn bits are reserved. See Table 19.2.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: PORRn and POSRn should not be set at the same time.

19.2.3 PCNTR3PORRPOSR：端口控制寄存器3

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 0 to 9, A, B)

Offset address: 0x008 (PCNTR3/PORR)
0x00A (POSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PORR15	PORR14	PORR13	PORR12	PORR11	PORR10	PORR09	PORR08	PORR07	PORR06	PORR05	PORR04	PORR03	PORR02	PORR01	PORR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	POSR15	POSR14	POSR13	POSR12	POSR11	POSR10	POSR09	POSR08	POSR07	POSR06	POSR05	POSR04	POSR03	POSR02	POSR01	POSR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	POSR15 to POSR00	Pmn输出设置 0：不影响输出1：高输出	W
31:16	PORR15 to PORR00	Pmn输出复位 0：对输出无影响1：低输出	W

Note: 如果安全属性配置为安全，●
允许安全写访问，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全写访问。

Note: m = 0 to 9, A, B, n = 00 to 15

端口控制寄存器3(PCNTR3PORRPOSR)是一个32位或16位写寄存器，用于控制端口输出数据的设置或复位。

PCNTR3控制端口输出数据的设置或复位，并以32位为单位进行访问。

POSRn（PCNTR3中的位[15:0]）和PORRn（PCNTR3中的位[31:16]）分别以16位为单位进行访问。

POSRn位（Pmn输出设置）

POSR在通过软件写入设置时改变PODR。例如，对于P100，当PORT1.PCNTR3.POSR00=1时，PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留POSRn位。见表19.2。

PORRN位（Pmn输出复位）

PORR在通过软件写入复位时改变PODR。例如，对于P100，当PORT1.PCNTR3.PORR00=1时，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留PORRN位。见表19.2。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: PORRn和POSRn不应同时设置。

19.2.4 PCNTR4/EORR/EOSR : Port Control Register 4

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 1 to 4)

Offset address: 0x00C (PCNTR4/EORR)
0x00E (EOSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn Event Output Set When an ELC_PORTx signal occurs 0: No effect on output 1: High output	R/W
31:16	EORR15 to EORR0	Pmn Event Output Reset When an ELC_PORTx signal occurs 0: No effect on output 1: Low output	R/W

Note: If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note: m = 1 to 4, n = 00 to 15, x = 1 to 4

The Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit or 16-bit read/write register that controls the setting or resetting of the port output data by an event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by an event input from the ELC, and is accessed in 32-bit units.

The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSRn bits (Pmn Event Output Set)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, EOSRn bits are reserved. See Table 19.2.

EORRn bits (Pmn Event Output Reset)

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100 if PORT1.PCNTR4.EORR00 = 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. In the case of input only ports, EORRn bits are reserved. See Table 19.2.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.

Note: EORRn and EOSRn should not be set at the same time.

19.2.4 PCNTR4EORREOSR：端口控制寄存器4

Base address: PORTm = 0x4008_0000 + 0x0020 × m (m = 1 to 4)

Offset address: 0x00C (PCNTR4/EORR)
0x00E (EOSR)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	EORR15	EORR14	EORR13	EORR12	EORR11	EORR10	EORR09	EORR08	EORR07	EORR06	EORR05	EORR04	EORR03	EORR02	EORR01	EORR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EOSR15	EOSR14	EOSR13	EOSR12	EOSR11	EOSR10	EOSR09	EOSR08	EOSR07	EOSR06	EOSR05	EOSR04	EOSR03	EOSR02	EOSR01	EOSR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	EOSR15 to EOSR00	Pmn事件输出集 当发生ELC_PORTx信号时 0：不影响输出1：高输出	R/W
31:16	EORR15 to EORR0	Pmn事件输出复位 当发生ELC_PORTx信号时 0：对输出无影响1：低输出	R/W

Note: 如果安全属性配置为安全，●
允许安全访问，
- 非安全读取值为0，但不会产生TrustZone访问错误，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

Note: m = 1 to 4, n = 00 to 15, x = 1 to 4

端口控制寄存器4(PCNTR4EORREOSR)是一个32位或16位读写寄存器，通过来自ELC的事件输入来控制端口输出数据的设置或复位。

PCNTR4通过来自ELC的事件输入来控制端口输出数据的设置或复位，并以32位为单位进行访问。

分别以16位为单位访问EOSRn（PCNTR4中的位[15:0]）和EORRn（PCNTR4中的位[31:16]）。

EOSRn位（Pmn事件输出设置）

EOSR在设置时会更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果在ELC_PORTx发生时PORT1.PCNTR4.EOSR00设置为1，则PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留EOSRn位。见表19.2。

EORRN位（Pmn事件输出复位）

EORR会在复位时更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果PORT1.PCNTR4.EORR00=1当ELC_PORTx发生时，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。在仅输入端口的情况下，保留EORRn位。见表19.2。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。

Note: EORRn和EOSRn不应同时设置。

19.2.5 PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 9, A, B, n = 00 to 15)

Base address: PFS = 0x4008_0800

Offset address: 0x000 + 0x040 × m + 0x004 × n (PmnPFS)
0x002 + 0x040 × m + 0x004 × n (PmnPFS_HA)
0x003 + 0x040 × m + 0x004 × n (PmnPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0	0	0	0	0	0*1	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	Port Output Data 0: Low output 1: High output	R/W*3
1	PIDR	Pmn State 0: Low level 1: High level	R*4
2	PDR	Port Direction 0: Input (functions as an input pin) 1: Output (functions as an output pin)	R/W*5
3	—	This bit is read as 0. The write value should be 0.	R/W
4	PCR	Pull-up Control 0: Disable input pull-up 1: Enable input pull-up	R/W*5
5	—	This bit is read as 0. The write value should be 0.	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W*5
9:7	—	These bits are read as 0. The write value should be 0.	R/W
11:10	DSCR[1:0]	Port Drive Capability 0 0: Low drive 0 1: Middle drive 1 0: High-speed high-drive 1 1: High drive	R/W*5
13:12	EOFR[1:0]	Event on Falling/Event on Rising*2 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W*5
14	ISEL	IRQ Input Enable 0: Not used as an IRQn input pin 1: Used as an IRQn input pin	R/W*5
15	ASEL	Analog Input Enable 0: Not used as an analog pin 1: Used as an analog pin	R/W*5
16	PMR	Port Mode Control 0: Used as a general I/O pin 1: Used as an I/O port for peripheral functions	R/W*5

19.2.5 PmnPFSPmnPFS_HAPmnPFS_BY:端口mn引脚功能选择寄存器（m=0到9，A，B，n=00到15）

Base address: PFS = 0x4008_0800

Offset address: 0x000 + 0x040 × m + 0x004 × n (PmnPFS)
0x002 + 0x040 × m + 0x004 × n (PmnPFS_HA)
0x003 + 0x040 × m + 0x004 × n (PmnPFS_BY)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASEL	ISEL	EOFR[1:0]		DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值:	0	0	0	0	0	0*1	0	0	0	0	0	0*1	0	0	x	0

Bit	Symbol	Function	R/W
0	PODR	端口输出数据 0：低输出1： 高输出	R/W*3
1	PIDR	Pmn State 0：低电平1 ：高电平	R*4
2	PDR	港口方向 0：输入（用作输入引脚）1：输出（ 用作输出引脚）	R/W*5
3	—	该位读取为0。写入值应为0。	R/W
4	PCR	Pull-up Control 0：禁止输入上拉1：使 能输入上拉	R/W*5
5	—	该位读取为0。写入值应为0。	R/W
6	NCODR	N-Channel Open-Drain Control 0: CMOS output 1: NMOS open-drain output	R/W*5
9:7	—	这些位被读取为0。写入值应为0。	R/W
11:10	DSCR[1:0]	端口驱动能力 00：低速驱动01：中速驱 动10：高速高速驱动11： 高速驱动	R/W*5
13:12	EOFR[1:0]	下降事件上升事件*2 00：无关01：检测上升 沿10：检测下降沿11： 检测两个沿	R/W*5
14	ISEL	IRQ输入使能 0：不用作IRQn输入引脚1：用作I RQn输入引脚	R/W*5
15	ASEL	模拟输入使能 0：不用作模拟引脚1：用作模 拟引脚	R/W*5
16	PMR	端口模式控制 0：用作通用IO引脚1：用作外围功能的IO端口	R/W*5

Bit	Symbol	Function	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
28:24	PSEL[4:0]	Peripheral Select These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W*5
31:29	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value of P108, P109, P110, P201 and P300 is not 0x0000_0000. P108 is 0x0001_0410, P109 is 0x0001_0400, P110 is 0x0001_0010, P201 is 0x0000_0010, and P300 is 0x0001_0010.
Note 2. Supported by PORTn (n = 1 to 4).
Note 3. If the security attribution is configured as Secure,
- Secure access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Note 4. If the security attribution is configured as Secure,
- Secure read access is allowed,
- Non-secure read value is 0, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure read access are allowed.

Note 5. If the security attribution is configured as Secure,
- Secure access and Non-secure read access are allowed,
- Non-secure write access is ignored, but TrustZone access error is not generated.

If the security attribution is configured as Non-secure,
- Secure and Non-secure access are allowed.

Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, or 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (PmnPFS [15:0] bits) is accessed in 16-bit units. PmnPFS_BY (PmnPFS[7:0] bits) is accessed in 8-bit units.

The available Port mn pin depends on the product. For details, see Table 19.1

PODR bit (Port Output Data), PIDR bit (Port State), PDR bit (Port Direction)

The PDR, PIDR, and PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

PCR bit (Pull-up Control)

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

NCODR bit (N-Channel Open-Drain Control)

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

DSCR[1:0] bits (Port Drive Capability)

The DSCR[1:0] bits switches the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is a read/write bit, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

EOFR[1:0] bits (Event on Falling/Event on Rising)

The EOFR[1:0] bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOFR[1:0] bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and the GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

Bit	Symbol	Function	R/W
23:17	—	这些位被读取为0。写入值应为0。	R/W
28:24	PSEL[4:0]	外设选择 这些位选择外设功能。对于各个引脚功能，请参见本章中的相关表格。	R/W*5
31:29	—	这些位被读取为0。写入值应为0。	R/W

注1.P108、P109、P110、P201、P300的初始值不是0x0000_0000。P108为0x0001_0410，P109为0x0001_0400，P110为0x0001_0010，P201为0x0000_0010，P300为0x0001_0010。
注2.受PORTn支持（n=1至4）。
注3.如果安全属性配置为Secure，●
允许安全访问，
- 非安全读取值为0，但不会产生TrustZone访问错误，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。
注4.如果安全属性配置为Secure，●
允许安全读取访问，
- 非安全读取值为0，但不会产生TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全读取访问。
注5.如果安全属性配置为Secure，●
允许安全访问和非安全读取访问，
- 忽略非安全写入访问，但不会生成TrustZone访问错误。

如果安全属性配置为非安全，●
允许安全和非安全访问。

端口mn引脚功能选择寄存器（PmnPFSPmnPFS_HAPmnPFS_BY）是选择端口mn引脚功能的32位、16位或8位读写控制寄存器，以32位为单位进行访问。PmnPFS_HA（PmnPFS[15:0]位）以16位为单位进行访问。PmnPFS_BY（PmnPFS[7:0]位）以8位为单位进行访问。

可用的端口mn引脚取决于产品。详见表19.1

PODR位（端口输出数据）、PIDR位（端口状态）、PDR位（端口方向）

PDR、PIDR和PODR位的功能与PCNTR相同。读取这些位时，将读取PCNTR值。

PCR bit (Pull-up Control)

PCR位启用或禁用各个端口引脚上的输入上拉电阻。当引脚处于输入状态且PmnPFS.PCR中的相关位设置为1时，连接到该引脚的上拉电阻被启用。当引脚设置为通用端口输出引脚或外围功能输出引脚时，无论PCR设置如何，该引脚的上拉电阻都被禁用。上拉电阻在复位状态下也被禁用。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

NCODR bit (N-Channel Open-Drain Control)

NCODR位指定端口引脚的输出类型。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

DSCR[1:0]位（端口驱动能力）

DSCR[1:0]位切换端口的驱动能力。如果某个管脚的驱动能力是固定的，那么相关的位就是一个读写位，但是驱动能力是不能改变的。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

EOFR[1:0]位（下降事件事件上升事件）

EOFR[1:0]位选择端口组输入信号的边沿检测方法。这些位支持上升沿、下降沿或两个边沿检测。当EOFR[1:0]位设置为01b、10b或11b时，IO单元的输入使能有效。随后，事件脉冲从外部引脚输入，GPIO将事件脉冲输出到ELC。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

ISEL bit (IRQ Input Enable)

The ISEL bit specifies IRQ input pins. This setting can be used in combination with the peripheral functions, although an IRQn (external pin interrupt) of the same number must only be enabled for one pin. The ISEL bit for an unspecified IRQn is reserved.

ASEL bit (Analog Input Enable)

The ASEL bit specifies analog pins. When a pin is set as an analog pin by this bit:

1. Specify it as a general I/O port in the Port Mode Control bit (PmnPFS.PMR).
2. Disable the pull-up resistor in the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input in the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

The ASEL bit for an unspecified analog I/O pin is reserved.

PMR bit (Port Mode Control)

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

PSEL[4:0] bits (Peripheral Select)

The PSEL[4:0] bits assign the peripheral function.

19.2.6 PWPR : Write-Protect Register

Base address: PFS = 0x4008_0800

Offset address: 0x503

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled	R/W
7	B0WI	PFSWE Bit Write Disable 0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

ISEL位（IRQ输入使能）

ISEL位指定IRQ输入引脚。此设置可以与外围功能结合使用，尽管
相同编号的IRQn（外部引脚中断）只能为一个引脚启用。未指定的IRQn的ISEL位被保留。

ASEL位（模拟输入使能）

ASEL位指定模拟引脚。当一个引脚被该位设置为模拟引脚时：

1.在端口模式控制位(PmnPFS.PMR)中将其指定为通用IO端口。

2.在上拉控制位(PmnPFS.PCR)中禁用上拉电阻。

3.在端口方向位(PmnPFS.PDR)中指定输入。此时无法读取引脚状态。PmnPFS寄存器受写保护寄存器(PWPR)保护。在修改寄存器之前释放写保护。

未指定的模拟IO引脚的ASEL位被保留。

PMR位（端口模式控制）

PMR位指定端口引脚功能。与不存在的引脚相关的位被保留。写入值应为0。

PSEL[4:0] bits (Peripheral Select)

PSEL[4:0]位分配外设功能。

19.2.6 PWPR : Write-Protect Register

Base address: PFS = 0x4008_0800

Offset address: 0x503

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	PFSWE	PmnPFS寄存器写使能 0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器	R/W
7	B0WI	PFSWE位写入禁用 0：允许写入PFSWE位1：禁止写入PFSWE位	R/W

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时才允许写入PmnPFS寄存器。您必须先将0写入B0WI位，然后再将PFSWE设置为1。

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

19.2.7 PFENET : Ethernet Control Register

Base address: PFS = 0x4008_0800

Offset address: 0x500

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PHYMODE0	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	PHYMODE0	Ethernet Mode Setting ch0 0: RMII mode (ETHERC channel 0) 1: MII mode (ETHERC channel 0)	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

Note: The access to PHYMODE0 bit is controlled by PSARB.PSARB15 bit.

PHYMODE0 bit (Ethernet Mode Setting ch0)

The PHYMODE0 bit specifies the PHY mode of ETHERC channel 0. Select the same mode as that specified in the pin function select bits (PmnPFS.PSEL[4:0]). When the signals for the RMII mode are specified in the PmnPFS.PSEL[4:0] bits, set the PHYMODE bit to 0 (RMII mode). When the signals for the MII mode are specified in the PmnPFS.PSEL[4:0] bits, set the PHYMODE bit to 1 (MII mode).

19.2.8 PWPRS : Write-Protect Register for Secure

Base address: PFS = 0x4008_0800

Offset address: 0x505

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	PFSWE	PmnPFS Register Write Enable 0: Disable writes to the PmnPFS register 1: Enable writes to the PmnPFS register	R/W
7	B0WI	PFSWE Bit Write Disable 0: Enable writes the PFSWE bit 1: Disable writes to the PFSWE bit	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register of the IO port pin set as secure by the PmSAR register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

19.2.7 PFENET:以太网控制寄存器

Base address: PFS = 0x4008_0800

Offset address: 0x500

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PHYMODE0	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	PHYMODE0	以太网模式设置ch0 0：RMII模式（ETHERC通道0）1：MII模式（ETHERC通道0）	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

Note: 对PHYMODE0位的访问由PSARB.PSARB15位控制。

PHYMODE0位（以太网模式设置ch0）

PHYMODE0位指定ETHERC通道0的PHY模式。选择与引脚功能选择位(PmnPFS.PSEL[4:0])中指定的模式相同的模式。当在PmnPFS.PSEL[4:0]位中指定RMII模式的信号时，将PHYMODE位设置为0（RMII模式）。当在PmnPFS.PSEL[4:0]位中指定MII模式的信号时，将PHYMODE位设置为1（MII模式）。

19.2.8 PWPRS:安全的写保护寄存器

Base address: PFS = 0x4008_0800

Offset address: 0x505

Bit position:	7	6	5	4	3	2	1	0
Bit field:	B0WI	PFSWE	—	—	—	—	—	—
重置后的值:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	PFSWE	PmnPFS寄存器写使能 0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器	R/W
7	B0WI	PFSWE位写入禁用 0：允许写入PFSWE位1：禁止写入PFSWE位	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时，才能写入由PmSAR寄存器设置为安全的IO端口引脚的PmnPFS寄存器。您必须先将0写入B0WI位，然后才能将PFSWE设置为1。

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

19.2.9 PmSAR : Port Security Attribution register (m = 0 to 9, A, B)

Base address: PFS = 0x4008_0800

Offset address: 0x510 + 0x002 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PMNSA[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	PMNSA[15:0]	Pmn Security Attribution Target I/O port pin : Pmn 0: Secure 1: Non Secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.
Note: m = 0 to 9, A, B, n = 00 to 15

Port Security Attribution Register is a 16-bit register that setting the Security Attribution of the each port, the registers are accessed only in 16-bit units.

PMNSA[15:0] bits (Pmn Security Attribution)

The PmnSA bit specifies the Security Attribution of Pmn.

19.3 Operation

19.3.1 General I/O Ports

All pins except P108 to P110,and P300 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or by individual pins with the Port mn Pin Function Select register. For details on these registers, see section 19.2. Register Descriptions.

Each port has the following bits:

- Port Security Attribution register (PmSAR)(m = 0 to 9, A, B), which indicates the security attribution.
- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin states
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs.

19.3.2 Port Function Select

The following port functions are available for configuring each pin:

- Security function: Security attribution for each pins.
- I/O configuration: Complementary or open-drain output, pull-up control, and drive strength

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

19.2.9 PmSAR:端口安全属性寄存器(m=0to9 A B)

Base address: PFS = 0x4008_0800

Offset address: 0x510 + 0x002 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PMNSA[15:0]															
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	PMNSA[15:0]	Pmn安全属性目标IO端口引脚：Pmn 0：安全1：不安全	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。
Note: m = 0 to 9, A, B, n = 00 to 15

端口安全属性寄存器是一个16位的寄存器，用于设置每个端口的安全属性，寄存器只能以16位为单位访问。

PMNSA[15:0]位（Pmn安全属性）

PmnSA位指定Pmn的安全属性。

19.3 Operation

19.3.1 通用IO端口

除P108至P110和P300外的所有引脚在复位后都作为通用IO端口工作。通用IO端口组织为每个端口16位，可以通过端口控制寄存器（PCNTRn，其中n=1到4）通过端口访问，或者通过端口mn引脚功能选择寄存器通过单个引脚访问。有关这些寄存器的详细信息，请参阅第19.2节。注册说明。

每个端口都有以下位：

- ●端口安全属性寄存器(PmSAR)(m=0to9 A B)，表示安全属性。
- ●端口方向位（PDRn），选择输入或输出方向
- ●端口输出数据位(PODRn)，用于保存输出数据
- ●端口输入数据位（PIDRn），指示引脚状态
- ●事件输入数据位(EIDRn)，当ELC_PORTn（n=1、2、3或4）信号发生时指示引脚状态
- ●端口输出设置位（POSRn），表示发生软件写时的输出值
- ●端口输出复位位（PORRn），表示发生软件写入时的输出值
- ●事件输出设置位（EOSRn），表示发生ELC_PORTn（n=1、2、3或4）信号时的输出值
- ●事件输出复位位（EORRn），指示发生ELC_PORTn（n=1、2、3或4）信号时的输出值。

19.3.2 端口功能选择

以下端口功能可用于配置每个引脚：

- ●安全功能：每个引脚的安全属性。
- ●IO配置：互补或开漏输出、上拉控制和驱动强度

- General I/O port: Port direction, output data setting, and read input data
- Alternate function: Configured function mapping to the pin.

Each pin is associated with a Port mn Pin Function Select register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes the following:

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR[1:0]: Drive capacity control bit that selects the drive capacity
- EOFR[1:0]: For selecting the edge of the event that input from the port group
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Port mn Pin Function Select register. For details, see section 19.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 9, A, B, n = 00 to 15).

19.3.3 Port Group Function for ELC

In the MCU, Port 1 to Port 4 are assigned for the ELC port group function.

19.3.3.1 Behavior When ELC_PORTn (n = 1, 2, 3 or 4) is Input from ELC

The MCU supports the two functions described in this section when an ELC_PORTn (n = 1, 2, 3 or 4) signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORTn (n = 1, 2, 3 or 4) signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins are read into the EIDR bit. See Figure 19.2

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input into the EIDR bit from the external pins.

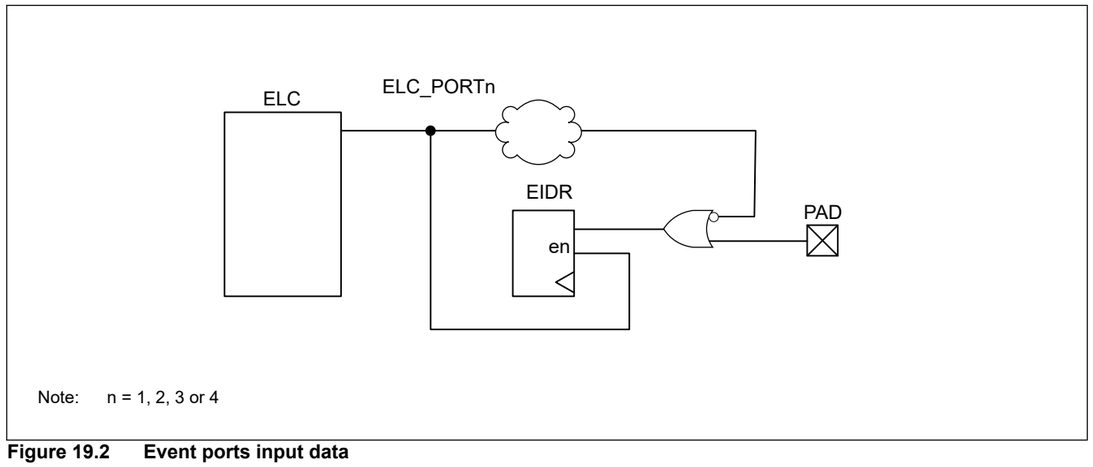


Figure 19.2 Event ports input data

(2) Output from PODR by EOSR and EORR

When an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs, the data is output from the PODR to the external pin based on the settings in the EOSR and EORR registers.

●通用IO口：端口方向、输出数据设置、读取输入数据

●备用功能：配置的功能映射到引脚。

每个引脚都与一个端口mn引脚功能选择寄存器(PmnPFS)相关联，该寄存器包括相关的PODR、PIDR和PDR位。此外，PmnPFS寄存器包括以下内容：

●PCR：上拉电阻控制位，打开或关闭输入上拉MOS

●NCODR：N沟道开漏控制位，用于选择每个引脚的输出类型

●DSCR[1:0]：驱动容量控制位，选择驱动容量

●EOFR[1:0]：用于选择从端口组输入的事件的边沿

●ISEL：IRQ输入使能位，用于指定IRQ输入引脚

●ASEL：模拟输入使能位，用于指定模拟引脚

●PMR：端口模式位，指定每个端口的引脚功能

●PSEL[4:0]：端口功能选择位，用于选择相关的外设功能。

这些配置可以通过单个寄存器访问端口mn引脚功能选择寄存器来进行。详见19.2.5节。PmnPFSPmnPFS_HAPmnPFS_BY：端口mn引脚功能选择寄存器（m=0到9，A，B，n=00到15）。

19.3.3 ELC的端口组功能

在MCU中，端口1到端口4被分配用于ELC端口组功能。

19.3.3.1 当ELC_PORTn（n=1、2、3或4）从ELC输入时的行为

当ELC_PORTn（n=1、2、3或4）信号来自ELC时，MCU支持本节中描述的两种功能。

(1) 输入到EIDR

对于GPI功能（PmnPFS寄存器中的PDR=0和PMR=0），当ELC_PORTn（n=1、2、3或4）信号来自ELC时，IO单元的输入使能有效，并且数据从外部引脚读入EIDR位。见图19.2

对于GPO功能(PDR=1)或外设模式(PMR=1)，0从外部引脚输入到EIDR位。

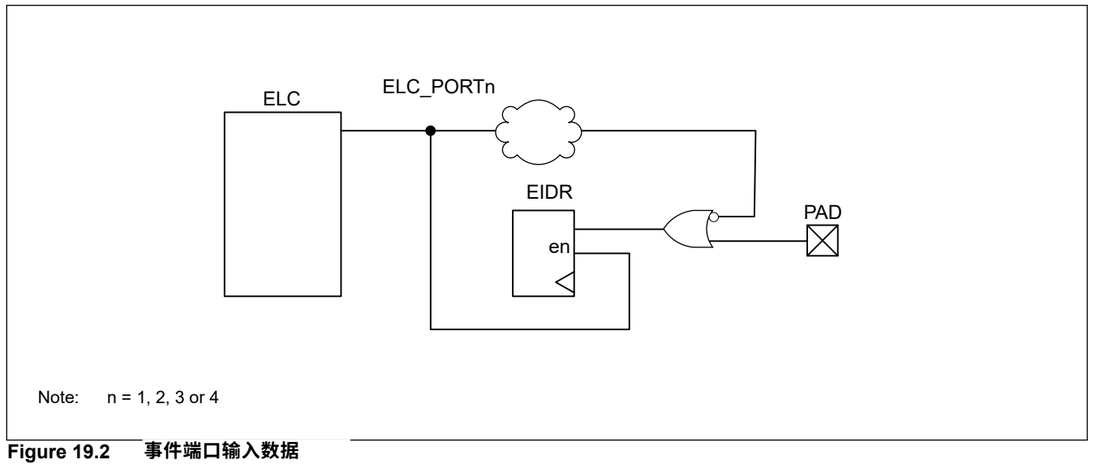


Figure 19.2 事件端口输入数据

(2) EOSR和EORR从PODR输出

当ELC_PORTn（n=1、2、3或4）信号发生时，数据会根据EOSR和EORR寄存器中的设置从PODR输出到外部引脚。

- If EOSR is set to 1, when an ELC_PORTn (n = 1, 2, 3 or 4) signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is retained.
- If EORR is set to 1, when ELC_PORTn (n = 1, 2, 3 or 4) signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is retained.

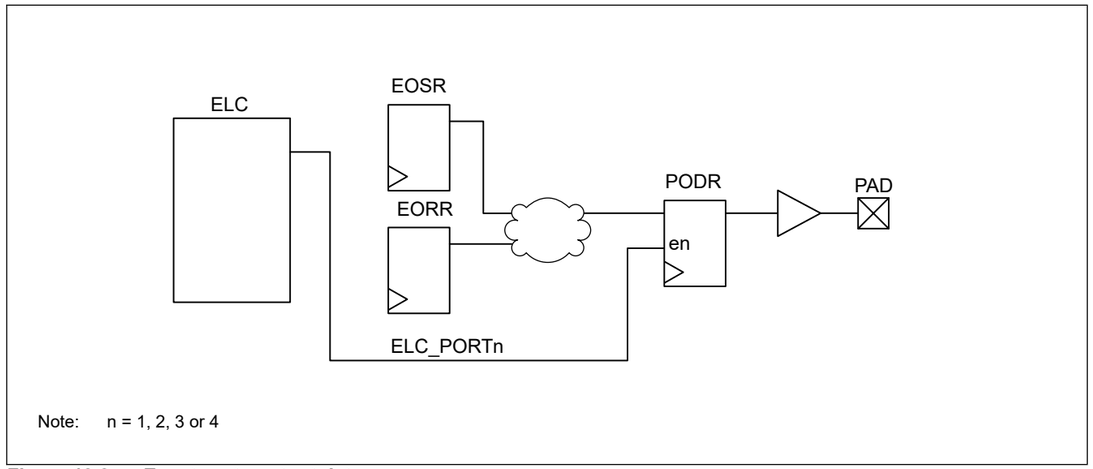


Figure 19.3 Event ports output data

19.3.3.2 Behavior When an Event Pulse is Output to ELC

To output the event pulse from the external pins to the ELC, set the EOFR[1:0] bits in the PmnPFS register. For details, see section 19.2.5. PmnPFS/PmnPFS_HA/PmnPFS_BY : Port mn Pin Function Select Register (m = 0 to 9, A, B, n = 00 to 15). When the EOFR[1:0] bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for Port 1, when the data is input from P100 to P115, the data of those 16 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORTn (n = 2 to 4) is also the same as Port 1. See Figure 19.4.

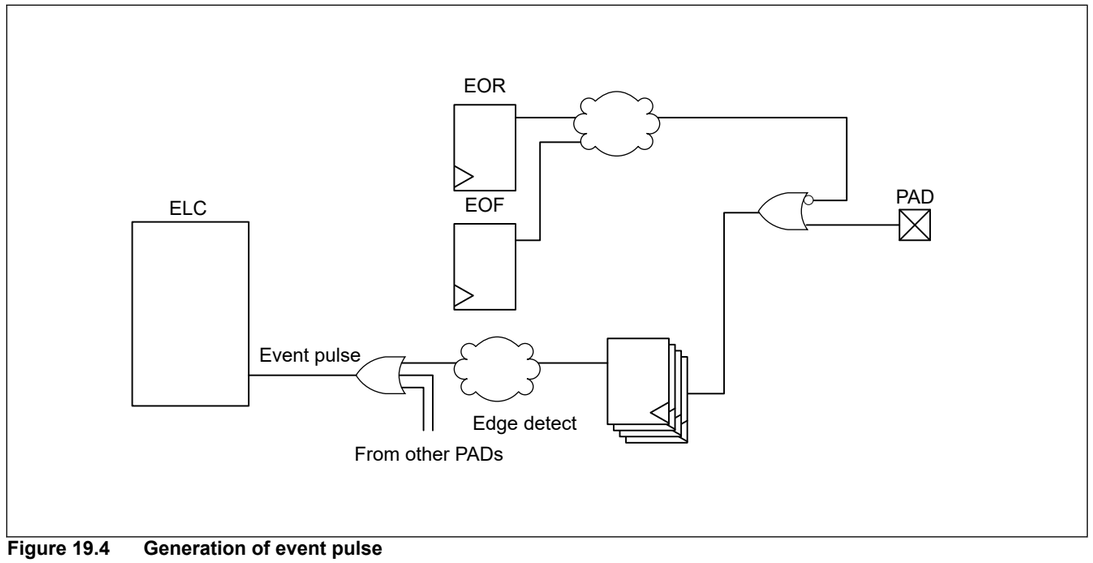


Figure 19.4 Generation of event pulse

●如果EOSR设置为1，当ELC_PORTn(n=1 2 3or4)信号出现时，PODR寄存器输出1到外部引脚。否则，当EOSR=0时，保留PODR值。

●如果EORR设置为1，当ELC_PORTn(n=1 2 3or4)信号出现时，PODR寄存器输出0到外部引脚。否则，当EORR=0时，保留PODR值。

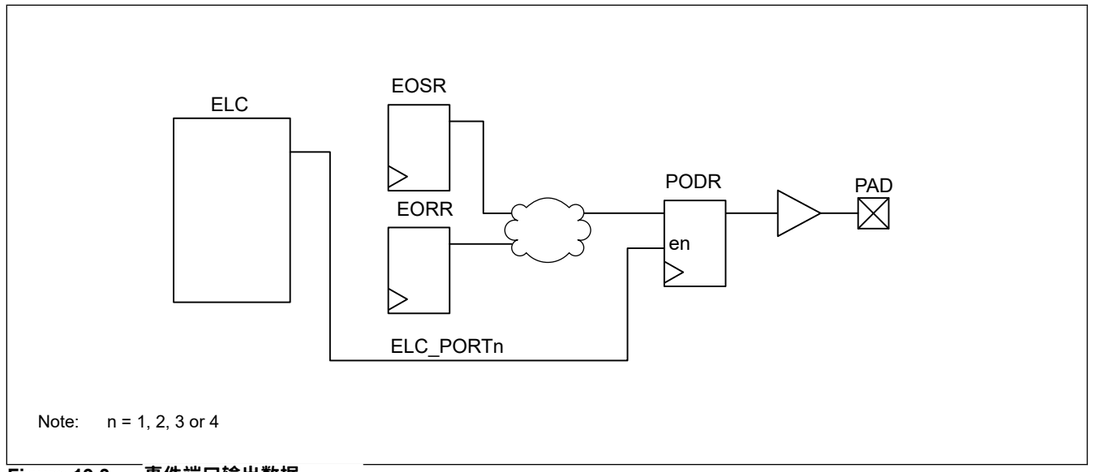


Figure 19.3 事件端口输出数据

19.3.3.2 事件脉冲输出到ELC时的行为

要将事件脉冲从外部引脚输出到ELC，请设置PmnPFS寄存器中的EOFR[1:0]位。详见19.2.5节。PmnPFSPmnPFS_HAPmnPFS_BY：端口mn引脚功能选择寄存器（m=0到9，A，B，n=00到15）。当EOFR[1:0]位被置位时，IO单元的输入使能被置位。

来自外部引脚的数据是输入。例如，对于端口1，当数据从P100输入到P115时，这16个引脚的数据由OR逻辑组织。该数据形成一个单次脉冲，该脉冲进入ELC。PORTn（n=2到4）的操作也与端口1相同。见图19.4。

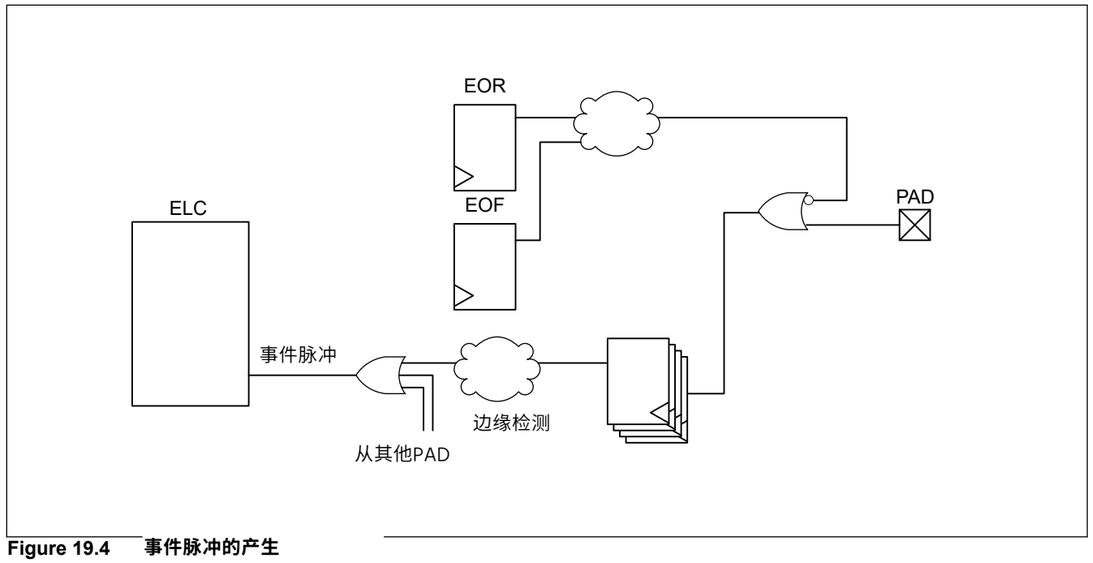


Figure 19.4 事件脉冲的产生

19.4 Handling of Unused Pins

Table 19.3 shows how to handle unused pins.

Table 19.3 Handling of unused pins

Pin name	Description
MD	Use as a mode selection pin
RES	Connect to VCC through a resistor (pulling up)
USB_DP	Keep pin open
USB_DM	Keep pin open
P200/NMI	Connect to VCC through a resistor (pulling up)
EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports 1 to 8.
XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When the external clock is input to the EXTAL pin, the XTAL pin functions as P213. When this pin is not used as port P213, configure it in the same way as ports 1 to 8.
XCIN	Connect to VSS through a resistor (pulling down)
XCOUT	Keep pin open
P000 to P015	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor *1 • If the direction is set to output (PCNTR1.PDRn = 1), keep pin open *1
Other ports	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor. *1 *2 • If the direction is set to output (PCNTR1.PDRn = 1), keep pin open. *1 *3
USBHS_DP USBHS_DM USBHS_RREF	• Preconditions: – AVCC_USBHS = VCC_USBHS: Connect to VCC – AVSS_USBHS = PVSS_USBHS = VSS1_USBHS = VSS2_USBHS: Connect to VSS – Set the module-stop state for USBHS (MSTPCRB.MSTPB12 = 1) • Processing details: – USBHS_DP, USBHS_DM, and USBHS_RREF: Open
VREFH0, VREFH	Connect to AVCC0
VREFL0, VREFL	Connect to AVSS0
VBATT	Connect to VCC or VSS.

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108, P110, and P300 are recommended for pull up VCC (pulled up) through a resistor, because these pins are input pull-up enabled from the initial value (PmnPFS.PCR = 1).
Note 3. P109 is recommended for setting the direction to output (PCNTR1.PDRn = 1), because this pin is output from the initial value.

19.5 Usage Notes

19.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.*1
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.*1
3. Clear the Port Mode Control bit in the PMR to 0 for the target pin to select the general I/O port.
4. Specify the I/O function for the pin through the PSEL[4:0] bits settings in the PmnPFS register.
5. Set the PMR bit to 1 as required to switch to the selected I/O function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.*1
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.*1

Note 1. When the security attribution of Pmn is set to 0, should to set the PWPRS register to enable writing the PmnPFS register.

19.4 未使用引脚的处理

表19.3显示了如何处理未使用的引脚。

Table 19.3 处理未使用的引脚

引脚名称	Description
MD	用作模式选择引脚
RES	通过一个电阻连接到VCC（上拉）
USB_DP	保持引脚打开
USB_DM	保持引脚打开
P200/NMI	通过一个电阻连接到VCC（上拉）
EXTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P212）。当该管脚不作为端口P212使用时，配置方式与端口1到8相同。
XTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P213）。当外部时钟输入到EXTAL引脚时，XTAL引脚起到P213的作用。当该管脚不作为端口P213使用时，配置方式与端口1到8相同。
XCIN	通过一个电阻连接到VSS（下拉）
XCOUT	保持引脚打开
P000 to P015	• 如果方向设置为输入(PCNTR1.PDRn=0)，则通过电阻器将相关引脚连接到AVCC0（上拉）或通过电阻器连接到AVSS0（下拉）*1 • 如果方向设置为输出(PCNTR1.PDRn=1)，保持引脚开路*1
其他端口	• 如果方向设置为输入(PCNTR1.PDRn=0)，则通过电阻将相关引脚连接到VCC（上拉）或通过电阻连接到VSS（下拉）。*1*2 • 如果方向设置为输出(PCNTR1.PDRn=1)，则保持引脚开路。*1*3
USBHS_DP USBHS_DM USBHS_RREF	• Preconditions: – AVCC_USBHS=VCC_USBHS：连接到VCC – AVSS_USBHS=PVSS_USBHS=VSS1_USBHS=VSS2_USBHS：连接到VSS – 设置USBHS的模块停止状态(MSTPCRB.MSTPB12=1) • Processing details: – USBHS_DP、USBHS_DM和USBHS_RREF：打开
VREFH0, VREFH	连接到AVCC0
VREFL0, VREFL	连接到AVSS0
VBATT	连接到VCC或VSS。

注1.将PmnPFS.PMR、PmnPFS.ISEL、PmnPFS.PCR和PmnPFS.ASEL位清零。
注2.推荐使用P108、P110和P300通过电阻上拉VCC（上拉），因为这些引脚从初始值（PmnPFS.PCR=1）开始输入上拉使能。

注3.推荐使用P109设置输出方向（PCNTR1.PDRn=1），因为该引脚是从初始值输出的。

19.5 使用说明

19.5.1 指定引脚功能的步骤

要指定IO引脚功能：

1.将PWPR寄存器中的B0WI位清零。这允许写入PWPR寄存器中的PFSWE位。*1

2.将PWPR寄存器中的PFSWE位设置为1。这允许写入PmnPFS寄存器。*1

3.将PMR中的PortModeControl位清为0，以便目标引脚选择通用IO端口。

4.通过PmnPFS寄存器中的PSEL[4:0]位设置指定引脚的IO功能。

5.根据需要将PMR位设置为1，以切换到为引脚选择的IO功能。

6.将PWPR寄存器中的PFSWE位清零。这将禁止写入PmnPFS寄存器。*1

7.将PWPR寄存器中的B0WI位设置为1。这将禁止写入PWPR寄存器中的PFSWE位。*1

注1.当Pmn的安全属性设置为0时，应设置PWPRS寄存器以允许写入PmnPFS寄存器。

19.5.2 Procedure for Using Port Group Input

To use the port group input (port n (n = 1 to 4)):

1. Set the ELSRx.ELS[8:0] bits to all 0 to ignore unexpected pulses. For more information, see section 18, Event Link Controller (ELC).
2. Set the EOFR[1:0] bits of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[8:0] bits to enable the event signals.

19.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Outputs 0 if PCNTR4.EORR is set to 1 when ELC_PORTn (n = 1, 2, 3 or 4) signal occurs.
2. Outputs 1 if PCNTR4.EOSR is set to 1 when ELC_PORTn (n = 1, 2, 3 or 4) signal occurs.
3. Outputs 0 if PCNTR3.PORR is set to 1.
4. Outputs 1 if PCNTR3.POSR is set to 1.
5. Outputs 0 or 1 because PCNTR1.PODRn is set.
6. Outputs 0 or 1 because PmnPFS.PODRn is set.

Numbers in this list correspond to the priority for writing to the PODRn. For example, if 1. and 3. from the list occur at the same time, the higher priority event 1. is executed.

19.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and the Port Direction bit (PDRn) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select Register (PmnPFS.ASEL) to 1.

19.5.5 I/O Buffer Specification

The P402, P403, and P404 can be used as the RTC input, AGT input and other peripheral functions. Table 19.4 lists the P402, P403, P404 specifications.

Table 19.4 P402, P403, P404 specifications

I/O port	RTC and AGT			Other peripheral	
	RTC and AGT input enable register	RTC	AGT	other peripheral enable register	CAC, GPT, CAN, SCI, SSIE, ETHERC (MII), ETHERC (RMII), and interrupt
P402	VBTICTLR.VCH0INEN	RTCIC0	AGTIO0 AGTIO1 AGTIO2 AGTIO3	P402PFS.PSEL and PMR	For details, see section 19.6. Peripheral Select Settings for Each Product.
P403	VBTICTLR.VCH1INEN	RTCIC1	AGTIO0 AGTIO1 AGTIO2 AGTIO3	P403PFS.PSEL and PMR	
P404	VBTICTLR .VCH2INEN	RTCIC2	AGTIO0 AGTIO1 AGTIO2 AGTIO3	P404PFS.PSEL and PMR	

These RTC and AGT inputs are controlled by the VBTICTLR register. And this register is the highest priority which selecting the functions.

P402, P403, and P404 can be used as IRQn-DS(n = 4, 14, 15) whether RTC and AGT inputs are selected or not. When using these interrupts, set the interrupt procedure after setting the VBTICTLR register. (see section 11.2.6. VBTICTLR : VBATT Input Control Register.)

19.5.2 使用端口组输入的过程

要使用端口组输入（端口n（n=1到4））：

1.将ELSRx.ELS[8:0]位设置为全0以忽略意外脉冲。有关详细信息，请参阅第18节，事件链接控制器(ELC)。

2.设置PmnPFS寄存器的EOFR[1:0]位以指定上升沿、下降沿或两个边沿检测。

3.执行虚拟读取或等待一小段时间，例如100ns。忽略意外脉冲取决于外部引脚的初始值。

4.设置ELSRx.ELS[8:0]位以启用事件信号。

19.5.3 端口输出数据寄存器(PODR)摘要

该寄存器输出数据如下：

1.如果PCNTR4.EORR在ELC_PORTn（n=1、2、3或4）信号发生时设置为1，则输出0。

2.如果PCNTR4.EOSR在ELC_PORTn（n=1、2、3或4）信号发生时设置为1，则输出1。

3.如果PCNTR3.PORR设置为1，则输出0。

4.如果PCNTR3.POSR设置为1，则输出1。

5.输出0或1，因为PCNTR1.PODRn已设置。

6.输出0或1，因为PmnPFS.PODRn已设置。

此列表中的数字对应于写入PODRn的优先级。例如，如果列表中的1.和3.同时发生，则执行优先级较高的事件1.。

19.5.4 使用模拟功能的注意事项

要使用模拟功能，请将端口模式控制位(PMR)和端口方向位(PDRn)设置为0，以便引脚用作通用输入端口。接下来，将端口mn引脚功能选择寄存器(PmnPFS.ASEL)中的模拟输入启用位(ASEL)设置为1。

19.5.5 IO缓冲器规格

P402、P403和P404可用作RTC输入、AGT输入和其他外围功能。表19.4列出了
P402, P403, P404 specifications.

Table 19.4 P402, P403, P404 specifications

IO端口	RTC和AGT			其他周边	
	RTC和AGT输入使能寄存器	RTC	AGT	其他外设使能寄存器	CAC、GPT、CAN、SCI、SSIE、ETHERC(MII)、ETHERC(RMII)和中断
P402	VBTICTLR.VCH0INEN	RTCIC0	AGTIO0 AGTIO1 AGTIO2 AGTIO3	P402PFS.PSEL and PMR	有关详细信息，请参阅第19.6节。外设选择每个产品的设置。
P403	VBTICTLR.VCH1INEN	RTCIC1	AGTIO0 AGTIO1 AGTIO2 AGTIO3	P403PFS.PSEL and PMR	
P404	VBTICTLR .VCH2INEN	RTCIC2	AGTIO0 AGTIO1 AGTIO2 AGTIO3	P404PFS.PSEL and PMR	

这些RTC和AGT输入由VBTICTLR寄存器控制。而这个寄存器是选择功能的最高优先级。

无论是否选择RTC和AGT输入，P402、P403和P404都可以用作IRQn-DS(n=4 14 15)。使用这些中断时，请在设置VBTICTLR寄存器后设置中断程序。（参见第11.2.6节。VBTICTLR：VBATT输入控制寄存器。）

See Figure 19.5.

The VBTICTLR register is not initialized on reset. Therefore, when not using the RTC or AGT inputs, the associated bit of VBTICTLR register must be set to 0 after reset.

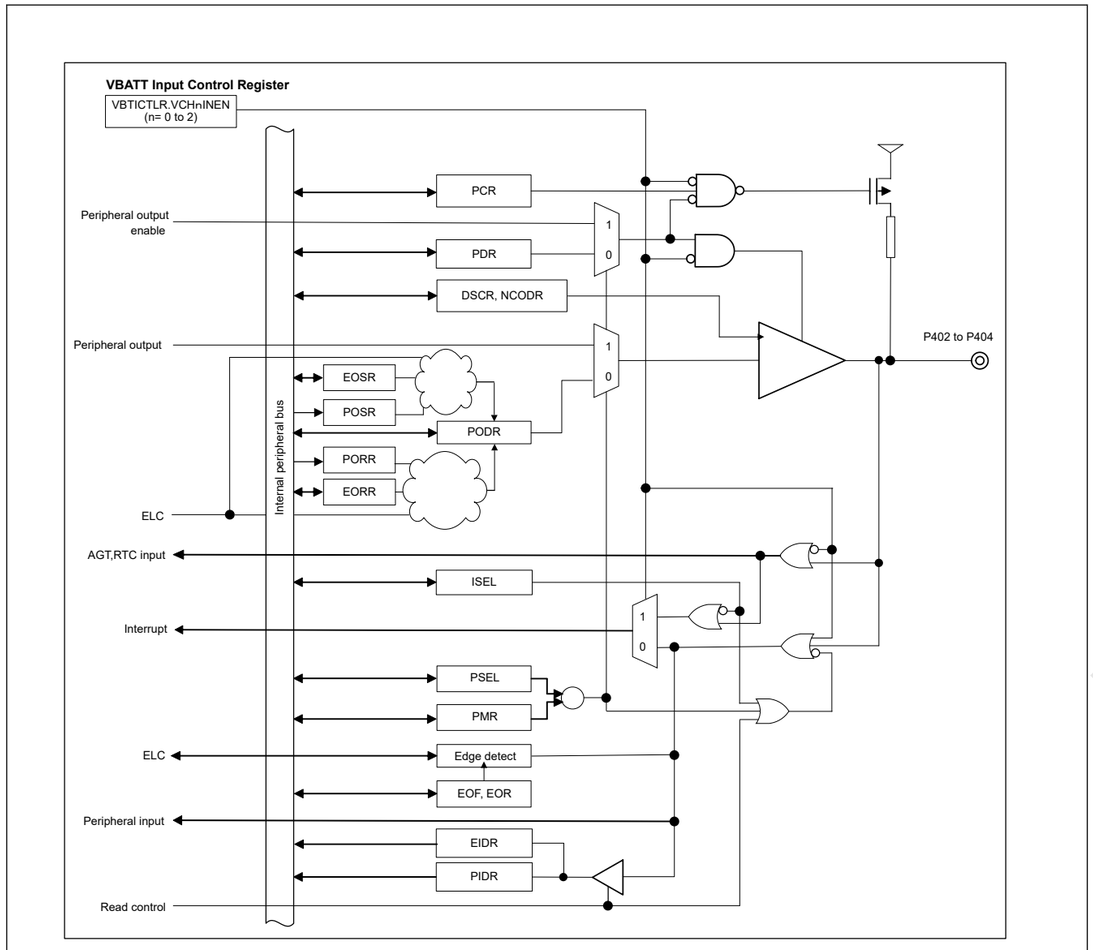


Figure 19.5 P402, P403, P404 diagram

19.6 Peripheral Select Settings for Each Product

This section describes the pin function select configuration using the PmnPFS register. Some pin names have added _A, _B, or _C suffixes. When assigning IIC, SPI, SSIE, ETHERC, and SDHI functionality, select the functional pins having the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

1. In Pmn pin function select register(PmnPFS), the PSEL bits have to be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, the unexpected edges may be input at the input function or the unexpected pulses may be output to the external pin at the output function.
2. Only the allowed values (functions) should be specified in the PSEL bits of PmnPFS register. If a value which is not allowed for the register is specified, the correct operation is not guaranteed.

请参见图19.5。

VBTICTLR寄存器在复位时未初始化。因此，当不使用RTC或AGT输入时，相关的位复位后VBTICTLR寄存器必须设置为0。

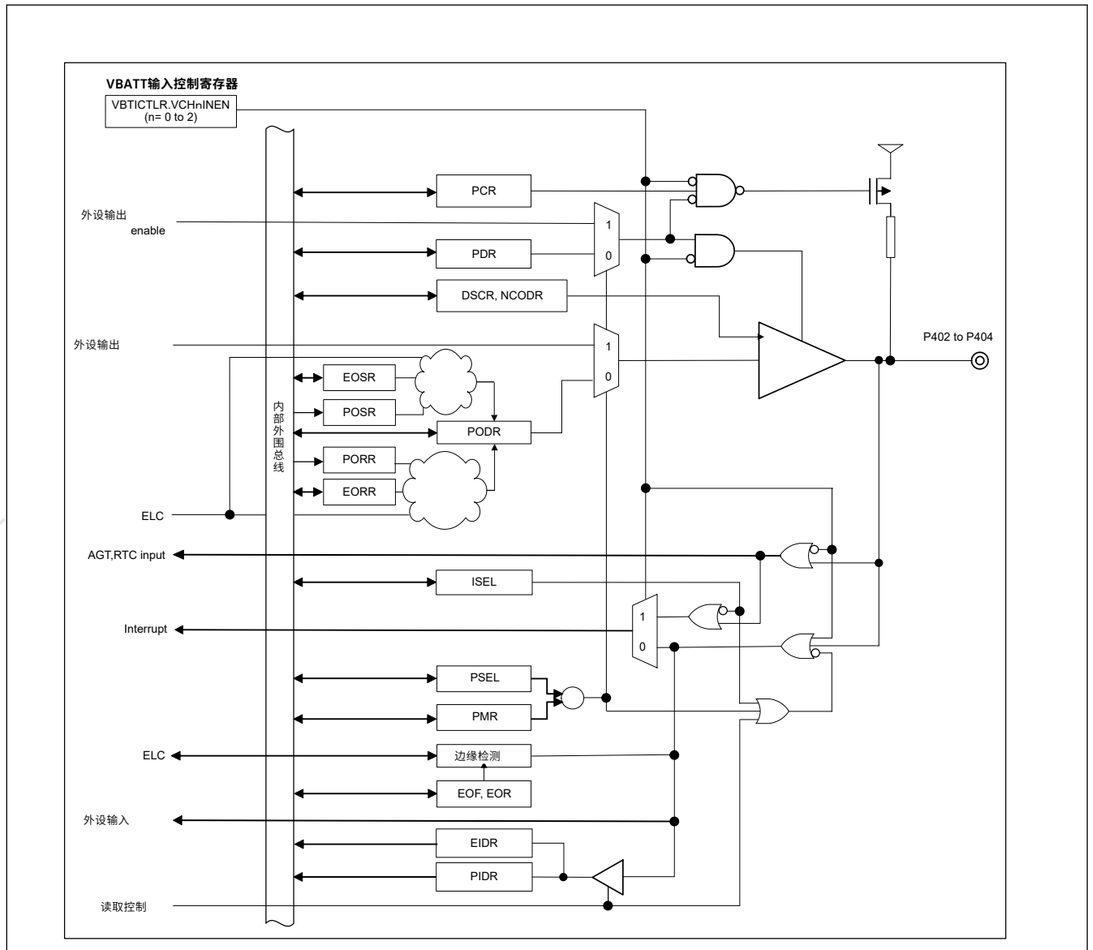


Figure 19.5 P402, P403, P404 diagram

19.6 每个产品的外设选择设置

本节介绍使用PmnPFS寄存器的引脚功能选择配置。一些引脚名称添加了_A、_B或_C后缀。分配IIC、SPI、SSIE、ETHERC和SDHI功能时，选择具有相同后缀的功能管脚。无论后缀如何，都可以选择其他引脚。禁止将相同的功能同时分配给两个或多个引脚。

1.在Pmn引脚功能选择寄存器（PmnPFS）中，当目标引脚的PMR位为0时，必须设置PSEL位。如果在PMR位为1时设置PSEL位，可能会在输入功能或意外脉冲可能会在输出功能处输出到外部引脚。

2.PmnPFS寄存器的PSEL位只能指定允许的值（功能）。如果指定了寄存器不允许的值，则不能保证正确操作。

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3. The single function should not be assigned to the multiple pins by PmnPFS register. When the GPT1, GPT5, SCI3, IIC0 or SPI0 are configured as secure and these pin function is being assigned to the pin which security attribution is set as secure by the PmSAR register, the write access to the PSEL bits for setting same function as secure pin in other pins is ignored when the security attribution of that pin is non-secure. For example, if the PSARE.PSARE30 bit is 0 (GPT1 is secure) and the P109PFS.PSEL bits is 00011b (pin function is GTIOC1A) and the P1SAR.109SA bit is 0 (P109 is secure), the write 00011b to the P405PFS.PSEL bits is ignored when the P4SAR.405SA bit is 1 (P405 is non-secure).
4. The PORT0 and 5 have the analog functions such as A/D converter. When these pins are used as an analog function, for avoiding the loss of resolution, the PMR bit should be set to 0 and PDR bit should be set to 0. After that, ASEL bit should be set to 1

Table 19.5 Register settings for input/output pin function (PORT0)

PSEL[4:0] settings	Function	pin												
		P000	P001	P002	P003	P004	P005	P006	P007	P008	P009	P010	P014	P015
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z												
ASEL bit		AN000/ AN100	AN001/ AN101	AN002/ AN102	AN003	AN004	AN005	AN006	AN007	AN008	AN009	AN010	AN012/DA0	AN013/DA1
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS	—	IRQ9-DS	IRQ10-DS	IRQ11-DS	—	IRQ12-DS	IRQ13-DS	IRQ14	—	IRQ13
DSCR[1:0] bits	Drive capacity control*1	L	L	L	L	L	L	L	L	L	L	L	L	L
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—	✓	✓

✓: Available
—: Setting prohibited

Note 1. The drive strength of this port cannot be controlled by PmnPFS.DSCR[1:0] bits.

Table 19.6 Register settings for input/output pin function (PORT1) (1 of 2)

PSEL[4:0] settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z								TMS/ SWDIO	TDO/SWO	TDI	Hi-Z				
00001b	AGT	AGTIO0	AGTEE0	AGTO0	AGTIO2	AGTEE2	AGTO2	AGTOB0	AGTOA0	AGTOA3	AGTOB3	AGTEE3	AGTOA5	AGTOB5	AGTEE5	AGTIO5	—
00010b	GPT*2	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—	GTOULO	GTOVUP	GTOVLO	—	—	—	—	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC3A	GTIOC3B	GTIOC2A	GTIOC2B	GTIOC4A
00100b	SCI	RXD0/ MISO0/ SCL0	TXD0/ MOSI0/ SDA0	SCK0	CTS0_ RTS0/ SS0	RXD8/ MISO8/ SCL8	TXD8/ MOSI8/ SDA8	SCK8	CTS8_ RTS8/ SS8	—	—	CTS2_ RTS2/ SS2	SCK2	TXD2/ MOSI2/ SDA2/ TXDX2/ SIOX2	RXD2/ MISO2/ SCL2/ RXDX2	—	—
00101b	SCI	SCK1	CTS1_ RTS1/ SS1	—	—	—	—	—	—	CTS9_ RTS9/ SS9	TXD9/ MOSI9/ SDA9	RXD9/ MISO9/ SCL9	SCK9	SCK1	—	CTS9	—
00110b	SPI*1	MISOB_A	MOSIB_A	RSPCKB_A	SSLB0_A	SSLB1_A	SSLB2_A	SSLB3_A	—	SSLA0_B	MOSIA_B	MISOA_B	RSPCKA_B	SSLA0_B	—	—	—
01001b	CLKOUT/ RTC	—	—	—	—	—	—	—	—	—	CLKOUT	—	—	—	—	—	—
01010b	CAC/ ADC12	—	—	ADTRG0	—	—	—	—	—	—	—	—	—	—	—	—	—
01011b	BUS	D00[A00/D00]	D01[A01/D01]	D02[A02/D02]	D03[A03/D03]	D04[A04/D04]	D05[A05/D05]	D06[A06/D06]	D07[A07/D07]	—	—	—	A05	A04	A03	A02	A01
10000b	CANFD	—	—	CRX0	CTX0	—	—	—	—	—	CTX1	CRX1	—	—	—	—	—
10001b	QSPI	QSPCLK	QIO1	QIO0	QIO3	QIO2	—	—	—	—	—	—	—	QSSL	—	—	—

3.PmnPFS寄存器不应将单一功能分配给多个引脚。当GPT1、GPT5、SCI3、IIC0或SPI0配置为安全且这些引脚功能被分配给由PmSAR寄存器设置安全属性为安全的引脚时，对PSEL位的写访问以将相同功能设置为安全当该pin的安全属性为非安全时，其他pin中的pin将被忽略。例如，如果PSARE.PSARE30位为0（GPT1是安全的）并且P109PFS.PSEL位是00011b（引脚功能是GTIOC1A）并且P1SAR.109SA位是0（P109是安全的），则将00011b写入P405PFS当P4SAR.405SA位为1（P405不安全）时，.PSEL位被忽略。

4.PORT0和5具有AD转换器等模拟功能。当这些引脚用作模拟功能时，为避免分辨率损失，PMR位应设置为0，PDR位应设置为0。之后，ASEL位应设置为1

Table 19.5 输入输出引脚功能（PORT0）的寄存器设置

PSEL[4:0] settings	Function	pin												
		P000	P001	P002	P003	P004	P005	P006	P007	P008	P009	P010	P014	P015
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z												
ASEL bit		AN000/ AN100	AN001/ AN101	AN002/ AN102	AN003	AN004	AN005	AN006	AN007	AN008	AN009	AN010	AN012/DA0	AN013/DA1
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS	—	IRQ9-DS	IRQ10-DS	IRQ11-DS	—	IRQ12-DS	IRQ13-DS	IRQ14	—	IRQ13
DSCR[1:0] bits	驱动容量控制*1	L	L	L	L	L	L	L	L	L	L	L	L	L
NCODR bit	N沟道开漏	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—	✓	✓

:可用—:禁止设置

注1.此端口的驱动强度不能由PmnPFS.DSCR[1:0]位控制。

Table 19.6 输入输出引脚功能的寄存器设置(PORT1)(1of2)

PSEL[4:0] settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z								TMS/ SWDIO	TDO/SWO	TDI	Hi-Z				
00001b	AGT	AGTIO0	AGTEE0	AGTO0	AGTIO2	AGTEE2	AGTO2	AGTOB0	AGTOA0	AGTOA3	AGTOB3	AGTEE3	AGTOA5	AGTOB5	AGTEE5	AGTIO5	—
00010b	GPT*2	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—	GTOULO	GTOVUP	GTOVLO	—	—	—	—	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A	GTIOC0B	GTIOC1A	GTIOC1B	GTIOC3A	GTIOC3B	GTIOC2A	GTIOC2B	GTIOC4A
00100b	SCI	RXD0/ MISO0/ SCL0	TXD0/ MOSI0/ SDA0	SCK0	CTS0_ RTS0/ SS0	RXD8/ MISO8/ SCL8	TXD8/ MOSI8/ SDA8	SCK8	CTS8_ RTS8/ SS8	—	—	CTS2_ RTS2/ SS2	SCK2	TXD2/ MOSI2/ SDA2/ TXDX2/ SIOX2	RXD2/ MISO2/ SCL2/ RXDX2	—	—
00101b	SCI	SCK1	CTS1_ RTS1/ SS1	—	—	—	—	—	—	CTS9_ RTS9/ SS9	TXD9/ MOSI9/ SDA9	RXD9/ MISO9/ SCL9	SCK9	SCK1	—	CTS9	—
00110b	SPI*1	MISOB_A	MOSIB_A	RSPCKB_A	SSLB0_A	SSLB1_A	SSLB2_A	SSLB3_A	—	SSLA0_B	MOSIA_B	MISOA_B	RSPCKA_B	SSLA0_B	—	—	—
01001b	CLKOUT/ RTC	—	—	—	—	—	—	—	—	—	CLKOUT	—	—	—	—	—	—
01010b	CAC/ ADC12	—	—	ADTRG0	—	—	—	—	—	—	—	—	—	—	—	—	—
01011b	BUS	D00[A00/D00]	D01[A01/D01]	D02[A02/D02]	D03[A03/D03]	D04[A04/D04]	D05[A05/D05]	D06[A06/D06]	D07[A07/D07]	—	—	—	A05	A04	A03	A02	A01
10000b	CANFD	—	—	CRX0	CTX0	—	—	—	—	—	CTX1	CRX1	—	—	—	—	—
10001b	QSPI	QSPCLK	QIO1	QIO0	QIO3	QIO2	—	—	—	—	—	—	—	QSSL	—	—	—

Table 19.6 Register settings for input/output pin function (PORT1) (2 of 2)

PSEL[4:0] settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
10010b	SSIE*1	—	—	—	—	—	—	—	—	—	—	—	—	SSIBCK0_B	SSILRCK0/SSIFS0_B	SSIRXD0_B	SSITXD0_B
11100b	OSPI	OM_SCLK	OM_SIO7	OM_SIO1	OM_SIO6	OM_DQS	OM_SIO5	OM_SIO0	OM_SIO3	—	—	—	—	OM_CS1	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—	—	—	IRQ3	IRQ4	—	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 2. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 19.7 Register settings for input/output pin function (PORT2) (1 of 2)

PSEL[4:0] settings	Function	Pin														
		P200*4	P201	P202	P203	P204	P205	P206	P207	P208	P209	P210	P211	P212	P213	P214
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z														
00001b	AGT	—	—	AGTOB3	AGTOA3	AGTIO1	AGTO1	—	—	—	AGTEE5	AGTOB5	AGTOA5	AGTEE1	AGTEE2	AGTO5
00010b	GPT*2	—	—	—	—	GTIW	GTIV	GTIU	—	GTOVLO	GTOVUP	GTIW	GTIV	GTETRGD	GTETRGC	GTIU
00011b	GPT*2	—	—	GTIOC5B	GTIOC5A	GTIOC4B	GTIOC4A	—	—	—	—	—	—	GTIOC0B	GTIOC0A	—
00100b	SCI	—	—	SCK2	CTS2_RTS2/SS2	SCK4	TXD4/MOSI4/SDA4	RXD4/MISO4/SCL4	TXD4/MOSI4/SDA4	—	—	—	—	—	—	—
00101b	SCI	—	—	RXD9/MISO9/SCL9	TXD9/MOSI9/SDA9	SCK9	CTS9_RTS9/SS9	CTS9	—	—	—	—	—	RXD1/MISO1/SCL1/RXDX1	TXD1/MOSI1/SDA1/TXDX1/SIOX1	—
00110b	SPI*1	—	—	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	—	—	—	—	—	—	—
00111b	IIC*1	—	—	—	—	—	SCL1_B	SDA1_B	—	—	—	—	—	—	—	—
01001b	CLKOUT/RTC	—	—	—	—	—	CLKOUT	—	—	—	—	—	—	—	—	—
01010b	CAC/ADC12	—	—	—	—	CACREF	—	—	—	—	—	—	—	—	ADTRG1	—
01011b	BUS	—	—	WR1/BC1	A19	A18	A16	WAIT	A17	CS4	CS5	CS6	CS7	—	—	—
01100b	CTSU	—	—	TS19	TS18	TS00	TS01	TS02	TSCAP	—	—	—	—	—	—	—
10000b	CANFD	—	—	CRX0	CTX0	—	—	—	—	—	—	—	—	—	—	—
10001b	QSPI	—	—	—	—	—	—	—	QSSL	QIO3	QIO2	QIO1	QIO0	—	—	QSPCLK
10010b	SSIE*1	—	—	—	—	SSIBCK0_C	SSILRCK0/SSIFS0_C	SSIDATA0_C	—	—	—	—	—	—	—	—
10011b	USBFS	—	—	—	—	USB_OVRCURB-DS	USB_OVRCURA-DS	USB_VBUSEN	—	—	—	—	—	—	—	—

Table 19.6 输入输出引脚功能的寄存器设置(PORT1)(2of2)

PSEL[4:0] settings	Function	pin															
		P100	P101	P102	P103	P104	P105	P106	P107	P108	P109	P110	P111	P112	P113	P114	P115
10010b	SSIE*1	—	—	—	—	—	—	—	—	—	—	—	—	SSIBCK0_B	SSILRCK0/SSIFS0_B	SSIRXD0_B	SSITXD0_B
11100b	OSPI	OM_SCLK	OM_SIO7	OM_SIO1	OM_SIO6	OM_DQS	OM_SIO5	OM_SIO0	OM_SIO3	—	—	—	—	OM_CS1	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ2	IRQ1	—	—	IRQ1	IRQ0	—	—	—	—	IRQ3	IRQ4	—	—	—	—
DSCR[1:0] bits	驱动容量控制	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

注1.建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

注2.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出歪斜规格(tGTISK)

Table 19.7 输入输出引脚功能的寄存器设置(PORT2)(1of2)

PSEL[4:0] settings	Function	Pin														
		P200*4	P201	P202	P203	P204	P205	P206	P207	P208	P209	P210	P211	P212	P213	P214
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z														
00001b	AGT	—	—	AGTOB3	AGTOA3	AGTIO1	AGTO1	—	—	—	AGTEE5	AGTOB5	AGTOA5	AGTEE1	AGTEE2	AGTO5
00010b	GPT*2	—	—	—	—	GTIW	GTIV	GTIU	—	GTOVLO	GTOVUP	GTIW	GTIV	GTETRGD	GTETRGC	GTIU
00011b	GPT*2	—	—	GTIOC5B	GTIOC5A	GTIOC4B	GTIOC4A	—	—	—	—	—	—	GTIOC0B	GTIOC0A	—
00100b	SCI	—	—	SCK2	CTS2_RTS2/SS2	SCK4	TXD4/MOSI4/SDA4	RXD4/MISO4/SCL4	TXD4/MOSI4/SDA4	—	—	—	—	—	—	—
00101b	SCI	—	—	RXD9/MISO9/SCL9	TXD9/MOSI9/SDA9	SCK9	CTS9_RTS9/SS9	CTS9	—	—	—	—	—	RXD1/MISO1/SCL1/RXDX1	TXD1/MOSI1/SDA1/TXDX1/SIOX1	—
00110b	SPI*1	—	—	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	—	—	—	—	—	—	—
00111b	IIC*1	—	—	—	—	—	SCL1_B	SDA1_B	—	—	—	—	—	—	—	—
01001b	CLKOUT/RTC	—	—	—	—	—	CLKOUT	—	—	—	—	—	—	—	—	—
01010b	CAC/ADC12	—	—	—	—	CACREF	—	—	—	—	—	—	—	—	ADTRG1	—
01011b	BUS	—	—	WR1/BC1	A19	A18	A16	WAIT	A17	CS4	CS5	CS6	CS7	—	—	—
01100b	CTSU	—	—	TS19	TS18	TS00	TS01	TS02	TSCAP	—	—	—	—	—	—	—
10000b	CANFD	—	—	CRX0	CTX0	—	—	—	—	—	—	—	—	—	—	—
10001b	QSPI	—	—	—	—	—	—	—	QSSL	QIO3	QIO2	QIO1	QIO0	—	—	QSPCLK
10010b	SSIE*1	—	—	—	—	SSIBCK0_C	SSILRCK0/SSIFS0_C	SSIDATA0_C	—	—	—	—	—	—	—	—
10011b	USBFS	—	—	—	—	USB_OVRCURB-DS	USB_OVRCURA-DS	USB_VBUSEN	—	—	—	—	—	—	—	—

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Table 19.7 Register settings for input/output pin function (PORT2) (2 of 2)

PSEL[4:0] settings	Function	Pin														
		P200*4	P201	P202	P203	P204	P205	P206	P207	P208	P209	P210	P211	P212	P213	P214
10101b	SDHI*1	—	—	SD0DAT6_A	SD0DAT5_A	SD0DAT4_A	SD0DAT3_A	SD0DAT2_A	—	SD0DAT0_B	SD0WP	SD0CD	SD0CMD_B	—	—	SD0CLK_B
10110b	ETHERC (MII)	—	—	ET0_ERXD2	ET0_COL	ET0_RX_DV	ET0_WOL	ET0_LINKSTA	—	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
10111b	ETHERC (RMII)	—	—	—	—	—	ET0_WOL	ET0_LINKSTA	—	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
11010b	Trace (Debug)	—	—	—	—	—	—	—	—	TDATA3	TDATA2	TDATA1	TDATA0	—	—	TCLK
11101b	CEC	—	—	—	—	—	—	CECIO_B	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	IRQ3-DS	IRQ2-DS	—	IRQ1-DS	IRQ0-DS	—	—	—	—	—	IRQ3	IRQ2	—
DSCR[1:0] bits	Drive capacity control	—	L*3	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H/HH
NCODR bit	N-ch open-drain	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})
Note 3. The driver strength of this port can not be controlled by PmnPFS.DSCR[1:0] bits.
Note 4. When using NMI pin interrupt, Port related registers setting are not required.

Table 19.8 Register settings for input/output pin function (PORT3) (1 of 2)

PSEL[4:0] settings	Function	Pin															
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313	P314	P315
00000b (value after reset)	Hi-Z/ JTAG/SWD	TCK/ SWCLK	Hi-Z														
00001b	AGT	—	AGTIO0	—	—	AGTEE2	AGTOB2	AGTOA2	AGTEE4	AGTOB4	AGTOA4	AGTEE1	AGTOB1	AGTOA1	—	—	—
00010b	GPT*2	GTOUUP	GTOULO	GTOUUP	—	GTOWLO	GTOWUP	GTOULO	GTOUUP	—	—	—	—	—	—	—	—
00011b	GPT*2	GTIOC0A	GTIOC4B	GTIOC4A	GTIOC7B	GTIOC7A	—	—	—	—	—	—	—	—	—	—	—
00100b	SCI	—	RXD2/ MISO2/ SCL2/ RXDX2	TXD2/ MOSI2/ SDA2/ TXDX2/ SIOX2	—	RXD6/ MISO6/ SCL6	TXD6/ MOSI6/ SDA6	SCK6	CTS6_RTS6/ SS6	CTS6	—	—	—	—	—	—	RXD4
00101b	SCI	—	CTS9_RTS9/ SS9	—	CTS9	—	—	—	—	CTS3	RXD3/ MISO3/ SCL3	TXD3/ MOSI3/ SDA3	SCK3	CTS3_RTS3/ SS3	—	—	—
00110b	SPI*1	SSLA1_B	SSLA2_B	SSLA3_B	—	—	—	—	—	—	—	—	—	—	—	ADTRG0	—
01011b	BUS	—	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	CS2	CS3	A20	A21	A22
10001b	QSPI	—	—	—	—	—	QSPCLK	QSSL	QIO0	QIO1	QIO2	QIO3	—	—	—	—	—
10101b	SDHI	—	—	—	—	—	—	—	—	—	—	—	—	—	SD0DAT7_A	—	—
10110b	ETHERC (MII)	—	—	—	—	—	—	—	—	—	—	—	—	—	ET0_ERXD3	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	IRQ6	IRQ5	—	IRQ9	IRQ8	—	—	—	—	—	—	—	—	—	—

Table 19.7 输入输出引脚功能的寄存器设置(PORT2)(2of2)

PSEL[4:0] settings	Function	Pin														
		P200*4	P201	P202	P203	P204	P205	P206	P207	P208	P209	P210	P211	P212	P213	P214
10101b	SDHI*1	—	—	SD0DAT6_A	SD0DAT5_A	SD0DAT4_A	SD0DAT3_A	SD0DAT2_A	—	SD0DAT0_B	SD0WP	SD0CD	SD0CMD_B	—	—	SD0CLK_B
10110b	ETHERC (MII)	—	—	ET0_ERXD2	ET0_COL	ET0_RX_DV	ET0_WOL	ET0_LINKSTA	—	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
10111b	ETHERC (RMII)	—	—	—	—	—	ET0_WOL	ET0_LINKSTA	—	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
11010b	Trace (Debug)	—	—	—	—	—	—	—	—	TDATA3	TDATA2	TDATA1	TDATA0	—	—	TCLK
11101b	CEC	—	—	—	—	—	—	CECIO_B	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	IRQ3-DS	IRQ2-DS	—	IRQ1-DS	IRQ0-DS	—	—	—	—	—	IRQ3	IRQ2	—
DSCR[1:0] bits	驱动容量控制	—	L*3	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H/HH
NCODR bit	N沟道开漏	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	—	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

注1.建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

注2.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出歪斜规格(t_{GTISK})

注3.此端口的驱动强度不能由PmnPFS.DSCR[1:0]位控制。
注4.当使用NMI引脚中断时，不需要设置端口相关的寄存器。

Table 19.8 输入输出引脚功能的寄存器设置(PORT3)(1of2)

PSEL[4:0] settings	Function	Pin															
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313	P314	P315
00000b (value after reset)	Hi-Z/ JTAG/SWD	TCK/ SWCLK	Hi-Z														
00001b	AGT	—	AGTIO0	—	—	AGTEE2	AGTOB2	AGTOA2	AGTEE4	AGTOB4	AGTOA4	AGTEE1	AGTOB1	AGTOA1	—	—	—
00010b	GPT*2	GTOUUP	GTOULO	GTOUUP	—	GTOWLO	GTOWUP	GTOULO	GTOUUP	—	—	—	—	—	—	—	—
00011b	GPT*2	GTIOC0A	GTIOC4B	GTIOC4A	GTIOC7B	GTIOC7A	—	—	—	—	—	—	—	—	—	—	—
00100b	SCI	—	RXD2/ MISO2/ SCL2/ RXDX2	TXD2/ MOSI2/ SDA2/ TXDX2/ SIOX2	—	RXD6/ MISO6/ SCL6	TXD6/ MOSI6/ SDA6	SCK6	CTS6_RTS6/ SS6	CTS6	—	—	—	—	—	—	RXD4
00101b	SCI	—	CTS9_RTS9/ SS9	—	CTS9	—	—	—	—	CTS3	RXD3/ MISO3/ SCL3	TXD3/ MOSI3/ SDA3	SCK3	CTS3_RTS3/ SS3	—	—	—
00110b	SPI*1	SSLA1_B	SSLA2_B	SSLA3_B	—	—	—	—	—	—	—	—	—	—	—	ADTRG0	—
01011b	BUS	—	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	CS2	CS3	A20	A21	A22
10001b	QSPI	—	—	—	—	—	QSPCLK	QSSL	QIO0	QIO1	QIO2	QIO3	—	—	—	—	—
10101b	SDHI	—	—	—	—	—	—	—	—	—	—	—	—	—	SD0DAT7_A	—	—
10110b	ETHERC (MII)	—	—	—	—	—	—	—	—	—	—	—	—	—	ET0_ERXD3	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	IRQ6	IRQ5	—	IRQ9	IRQ8	—	—	—	—	—	—	—	—	—	—

Table 19.8 Register settings for input/output pin function (PORT3) (2 of 2)

PSEL[4:0] settings	Function	Pin															
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313	P314	P315
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 2. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 19.9 Register settings for input/output pin function (PORT4) (1 of 2)

PSEL[4:0] settings	Function	pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z															
00001b	AGT	AGTIO1	—	—	—	—	—	AGTO5	AGTIO0	AGTOB2	AGTOA2	AGTOB1	AGTOA1	AGTEE1	AGTEE3	AGTIO5	AGTIO4
00010b	GPT*3	—	GTETRGA	—	—	—	—	—	—	GTOWLO	GTOWUP	GTOVLO	GTOVUP	GTOULO	GTOUUP	—	—
00011b	GPT*3	GTIOC6A	GTIOC6B	—	GTIOC3A	GTIOC3B	GTIOC1A	GTIOC1B	GTIOC6A	GTIOC6B	—	GTIOC9B	GTIOC9A	—	—	GTIOC0B	GTIOC0A
00100b	SCI	SCK4	CTS4_RTS4/SS4	CTS4	—	—	—	—	CTS4_RTS4/SS4	CTS4	—	RXD0/MISO0/SCL0	TXD0/MOSI0/SDA0	SCK0	CTS0_RTS0/SS0	CTS0	—
00101b	SCI	SCK7	TXD7/MOSI7/SDA7	RXD7/MISO7/SCL7	CTS7_RTS7/SS7	CTS7	—	—	—	RXD3/MISO3/SCL3	TXD3/MOSI3/SDA3	SCK3	CTS3_RTS3/SS3	CTS3	—	—	—
00110b	SPI*2	—	—	—	—	—	—	SSLA3_C	SSLA3_A	—	—	MISOB_B	MOSIB_B	RSPCKB_B	SSLB0_B	SSLB1_B	SSLB2_B
00111b	IIC*2	SCL0_A	SDA0_A	—	—	—	—	—	SDA0_B	SCL0_B	SDA2_A	SCL2_A	—	—	—	SDA2_B	SCL2_B
01001b	CLKOUT/ RTC	—	—	—	—	—	—	—	RTCOUT	—	—	—	—	—	—	—	—
01010b	CAC/ ADC12	ADTRG1	—	CACREF	—	—	—	—	ADTRG0	—	—	—	—	—	—	—	—
01100b	CTSU	—	—	—	—	—	—	—	TS03	TS4	TS5	TS06	TS07	TS08	TS09	TS10	TS11
10000b	CANFD	—	CTX0	CRX0	—	—	—	—	—	—	—	—	—	—	—	—	—
10010b	SSIE*2	AUDIO_CLK	—	AUDIO_CLK	SSIBCK0_A	SSILRCK0/SSIFS0_A	SSITXD0_A	SSIRXD0_A	—	—	—	—	—	—	—	—	—
10011b	USBFS	—	—	—	—	—	—	—	USB_VBUS	USB_ID	USB_EXICEN	—	—	—	—	—	USB_VBUSEN
10100b	USBHS	—	—	—	—	—	—	—	—	USBHS_ID	USBHS_EXICEN	—	—	—	—	—	—
10101b	SDHI*2	—	—	—	—	—	—	—	—	—	—	SD0DAT1_A	SD0DAT0_A	SD0CMD_A	SD0CLK_A	SD0WP	SD0CD
10110b	ETHERC (MII)	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	ET0_TX_EN	ET0_RX_ER	ET0_EXOUT	ET0_CRS	ET0_RX_CLK	ET0_ERXD0	ET0_ERXD1	ET0_ETXD0	ET0_ETXD1	ET0_RX_ER	ET0_TX_EN
10111b	ETHERC (RMII)	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	RMII0_TXD_EN_B	RMII0_TXD1_B	ET0_EXOUT	RMII0_CRS_DV_A	RMII0_RX_ER_A	RMII0_RXD1_A	RMII0_RXD0_A	REF50CK0_A	RMII0_TXD0_A	RMII0_TXD1_A	RMII0_TXD_EN_A

Table 19.8 输入输出引脚功能的寄存器设置(PORT3)(2of2)

PSEL[4:0] settings	Function	Pin															
		P300	P301	P302	P303	P304	P305	P306	P307	P308	P309	P310	P311	P312	P313	P314	P315
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—	—	—	—

:可用—:禁止设置

注1.建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

注2.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出歪斜规格(tGTISK)

Table 19.9 输入输出引脚功能的寄存器设置(PORT4)(1of2)

PSEL[4:0] settings	Function	pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z															
00001b	AGT	AGTIO1	—	—	—	—	—	AGTO5	AGTIO0	AGTOB2	AGTOA2	AGTOB1	AGTOA1	AGTEE1	AGTEE3	AGTIO5	AGTIO4
00010b	GPT*3	—	GTETRGA	—	—	—	—	—	—	GTOWLO	GTOWUP	GTOVLO	GTOVUP	GTOULO	GTOUUP	—	—
00011b	GPT*3	GTIOC6A	GTIOC6B	—	GTIOC3A	GTIOC3B	GTIOC1A	GTIOC1B	GTIOC6A	GTIOC6B	—	GTIOC9B	GTIOC9A	—	—	GTIOC0B	GTIOC0A
00100b	SCI	SCK4	CTS4_RTS4/SS4	CTS4	—	—	—	—	CTS4_RTS4/SS4	CTS4	—	RXD0/MISO0/SCL0	TXD0/MOSI0/SDA0	SCK0	CTS0_RTS0/SS0	CTS0	—
00101b	SCI	SCK7	TXD7/MOSI7/SDA7	RXD7/MISO7/SCL7	CTS7_RTS7/SS7	CTS7	—	—	—	RXD3/MISO3/SCL3	TXD3/MOSI3/SDA3	SCK3	CTS3_RTS3/SS3	CTS3	—	—	—
00110b	SPI*2	—	—	—	—	—	—	SSLA3_C	SSLA3_A	—	—	MISOB_B	MOSIB_B	RSPCKB_B	SSLB0_B	SSLB1_B	SSLB2_B
00111b	IIC*2	SCL0_A	SDA0_A	—	—	—	—	—	SDA0_B	SCL0_B	SDA2_A	SCL2_A	—	—	—	SDA2_B	SCL2_B
01001b	CLKOUT/ RTC	—	—	—	—	—	—	—	RTCOUT	—	—	—	—	—	—	—	—
01010b	CAC/ ADC12	ADTRG1	—	CACREF	—	—	—	—	ADTRG0	—	—	—	—	—	—	—	—
01100b	CTSU	—	—	—	—	—	—	—	TS03	TS4	TS5	TS06	TS07	TS08	TS09	TS10	TS11
10000b	CANFD	—	CTX0	CRX0	—	—	—	—	—	—	—	—	—	—	—	—	—
10010b	SSIE*2	AUDIO_CLK	—	AUDIO_CLK	SSIBCK0_A	SSILRCK0/SSIFS0_A	SSITXD0_A	SSIRXD0_A	—	—	—	—	—	—	—	—	—
10011b	USBFS	—	—	—	—	—	—	—	USB_VBUS	USB_ID	USB_EXICEN	—	—	—	—	—	USB_VBUSEN
10100b	USBHS	—	—	—	—	—	—	—	—	USBHS_ID	USBHS_EXICEN	—	—	—	—	—	—
10101b	SDHI*2	—	—	—	—	—	—	—	—	—	—	SD0DAT1_A	SD0DAT0_A	SD0CMD_A	SD0CLK_A	SD0WP	SD0CD
10110b	ETHERC (MII)	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	ET0_TX_EN	ET0_RX_ER	ET0_EXOUT	ET0_CRS	ET0_RX_CLK	ET0_ERXD0	ET0_ERXD1	ET0_ETXD0	ET0_ETXD1	ET0_RX_ER	ET0_TX_EN
10111b	ETHERC (RMII)	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	RMII0_TXD_EN_B	RMII0_TXD1_B	ET0_EXOUT	RMII0_CRS_DV_A	RMII0_RX_ER_A	RMII0_RXD1_A	RMII0_RXD0_A	REF50CK0_A	RMII0_TXD0_A	RMII0_TXD1_A	RMII0_TXD_EN_A

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Table 19.9 Register settings for input/output pin function (PORT4) (2 of 2)

PSEL[4:0] settings	Function	pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
Don't-care	AGT, RTC	—	—	AGTIO0*1/ AGTIO1*1/ AGTIO2*1/ AGTIO3*1/ RTCIC0*1	AGTIO0*1/ AGTIO1*1/ AGTIO2*1/ AGTIO3*1/ RTCIC1*1	AGTIO0*1/ AGTIO1*1/ AGTIO2*1/ AGTIO3*1/ RTCIC2*1	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ0	IRQ5-DS	IRQ4-DS	IRQ14-DS	IRQ15-DS	—	—	—	IRQ7	IRQ6	IRQ5	IRQ4	—	—	IRQ9	IRQ8
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. To use this pin function, set the associated pin as a general input (set the PmnPFS.PDR and PmnPFS.PMR bits to 0).
Note 2. Recommend using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 19.10 Register settings for input/output pin function (PORT5) (1 of 2)

PSEL[4:0] settings	Function	pin											
		P500	P501	P502	P503	P504	P505	P506	P507	P508	P511	P512	P513
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z											
00001b	AGT	AGTOA0	AGTOB0	AGTOA2	AGTOB2	AGTOA3	AGTOB3	—	—	—	—	—	—
00010b	GPT*1	GTIU	GTIV	GTIW	GTETRGC	GTETRGD	—	—	—	—	—	—	—
00011b	GPT*1	—	—	—	—	—	—	—	—	—	GTIOC0B	GTIOC0A	—
00100b	SCI	—	—	CTS6	CTS6_RTS6/ SS6	SCK6	RXD6/ MISO6/ SCL6	TXD6/ MOSI6/ SDA6	SCK6	—	RXD4/ MISO4/ SCL4	TXD4/ MOSI4/ SDA4	—
00101b	SCI	CTS5	TXD5/ MISO5/ SDA5	RXD5/ MISO5/ SCL5	SCK5	CTS5_RTS5/S S5	—	—	SCK5	CTS_RTS5	—	—	RXD5
00111b	IIC	—	—	—	—	—	—	—	—	—	SDA1_A	SCL1_A	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—	—	—	—	—	—	—
01011b	BUS	—	—	—	—	ALE	—	—	—	—	—	—	—
10000b	CANFD	—	—	—	—	—	—	—	—	—	CRX1	CTX1	—
10001b	QSPI	QSPCLK	QSSL	QIO0	QIO1	QIO2	QIO3	—	—	—	—	—	—
10011b	USBFS	USB_VBUSEN	USB_OVRCURA	USB_OVRCURB	USB_EXICEN	USB_ID	—	—	—	—	—	—	—
ASEL bit		AN116	AN117	AN118	AN119	AN120	AN121	AN122	AN123	AN124	—	—	—
ISEL bit		—	IRQ11	IRQ12	—	—	IRQ14	IRQ15	—	—	IRQ15	IRQ14	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	—

Table 19.9 输入输出引脚功能的寄存器设置(PORT4)(2of2)

PSEL[4:0] settings	Function	pin															
		P400	P401	P402	P403	P404	P405	P406	P407	P408	P409	P410	P411	P412	P413	P414	P415
Don't-care	AGT, RTC	—	—	AGTIO0*1/ AGTIO1*1/ AGTIO2*1/ AGTIO3*1/ RTCIC0*1	AGTIO0*1/ AGTIO1*1/ AGTIO2*1/ AGTIO3*1/ RTCIC1*1	AGTIO0*1/ AGTIO1*1/ AGTIO2*1/ AGTIO3*1/ RTCIC2*1	—	—	—	—	—	—	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		IRQ0	IRQ5-DS	IRQ4-DS	IRQ14-DS	IRQ15-DS	—	—	—	IRQ7	IRQ6	IRQ5	IRQ4	—	—	IRQ9	IRQ8
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
100针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

注1.要使用此引脚功能，请将相关引脚设置为通用输入（将PmnPFS.PDR和PmnPFS.PMR位设置为0）。
注2.建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

注3.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出歪斜规格(tGTISK)

Table 19.10 输入输出引脚功能的寄存器设置(PORT5)(1of2)

PSEL[4:0] settings	Function	pin											
		P500	P501	P502	P503	P504	P505	P506	P507	P508	P511	P512	P513
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z											
00001b	AGT	AGTOA0	AGTOB0	AGTOA2	AGTOB2	AGTOA3	AGTOB3	—	—	—	—	—	—
00010b	GPT*1	GTIU	GTIV	GTIW	GTETRGC	GTETRGD	—	—	—	—	—	—	—
00011b	GPT*1	—	—	—	—	—	—	—	—	—	GTIOC0B	GTIOC0A	—
00100b	SCI	—	—	CTS6	CTS6_RTS6/ SS6	SCK6	RXD6/ MISO6/ SCL6	TXD6/ MOSI6/ SDA6	SCK6	—	RXD4/ MISO4/ SCL4	TXD4/ MOSI4/ SDA4	—
00101b	SCI	CTS5	TXD5/ MISO5/ SDA5	RXD5/ MISO5/ SCL5	SCK5	CTS5_RTS5/S S5	—	—	SCK5	CTS_RTS5	—	—	RXD5
00111b	IIC	—	—	—	—	—	—	—	—	—	SDA1_A	SCL1_A	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—	—	—	—	—	—	—
01011b	BUS	—	—	—	—	ALE	—	—	—	—	—	—	—
10000b	CANFD	—	—	—	—	—	—	—	—	—	CRX1	CTX1	—
10001b	QSPI	QSPCLK	QSSL	QIO0	QIO1	QIO2	QIO3	—	—	—	—	—	—
10011b	USBFS	USB_VBUSEN	USB_OVRCURA	USB_OVRCURB	USB_EXICEN	USB_ID	—	—	—	—	—	—	—
ASEL bit		AN116	AN117	AN118	AN119	AN120	AN121	AN122	AN123	AN124	—	—	—
ISEL bit		—	IRQ11	IRQ12	—	—	IRQ14	IRQ15	—	—	IRQ15	IRQ14	—
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N沟道开漏	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	—

Table 19.10 Register settings for input/output pin function (PORT5) (2 of 2)

PSEL[4:0] settings	Function	pin											
		P500	P501	P502	P503	P504	P505	P506	P507	P508	P511	P512	P513
100 pins product		✓	✓	✓	✓	✓	✓	—	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 19.11 Register settings for input/output pin function (PORT6)

PSEL[4:0] settings	Function	Pin															
		P600	P601	P602	P603	P604	P605	P606	P607	P608	P609	P610	P611	P612	P613	P614	P615
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z															
00001b	AGT	AGTIO3	AGTEE3	AGTO3	AGTIO4	AGTEE4	AGTO4	—	—	—	AGTO5	AGTO4	AGTO3	AGTO2	AGTO1	AGTO0	—
00011b	GPT	GTIOC6B	GTIOC6A	GTIOC7B	GTIOC7A	GTIOC8B	GTIOC8A	—	—	GTIOC4B	GTIOC5A	GTIOC5B	—	—	—	—	—
00100b	SCI	—	—	—	—	—	CTS8	CTS_RTS8	RXD8	—	—	—	—	—	—	—	—
00101b	SCI	SCK9	RXD9/ MISO9/ SCL9	TXD9/ MOSI9/ SDA9	CTS9_ RTS9/ SS9	CTS9	—	—	—	—	—	CTS7	CTS7_ RTS7/ SS7	SCK7	TXD7	RXD7	—
01001b	CLKOUT/ RTC	CLKOUT	—	—	—	—	—	RTCOUT	—	—	—	—	CLKOUT	—	—	—	—
01010b	CAC/ ADC12	CACREF	—	—	—	—	—	—	—	—	—	—	CACREF	—	—	—	—
01011b	BUS	RD	WR/ WR0	EBCLK	D13[A13/D13]	D12[A12/D12]	D11[A11/D11]	—	—	A00/BC0	CS1	CS0	—	D08[A08/D08]	D09[A09/D09]	D10[A10/D10]	—
10000b	CANFD	—	—	—	—	—	—	—	—	—	CTX1	CRX1	—	—	—	—	—
10011b	USBFS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	USB_VBUSEN
11100b	OSPI	OM_SIO4	OM_SIO2	OM_CS1	—	—	—	—	—	—	OM_ECS	OM_CS0	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IRQ7
DSCR[1:0] bits	Drive capacity control	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	—
100 pins product		✓	✓	✓	—	—	—	—	—	✓	✓	✓	—	—	—	—	—

✓: Available
—: Setting prohibited

Table 19.12 Register settings for input/output pin function (PORT7) (1 of 2)

PSEL[4:0] settings	Function	Pin													
		P700	P701	P702	P703	P704	P705	P706	P707	P708	P709	P710	P711	P712	P713
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z													
00001b	AGT	AGTO4	AGTO3	AGTO2	AGTO1	AGTO0	AGTIO0	—	—	—	—	—	AGTEE0	AGTOB0	AGTOA0
00011b	GPT*1	GTIOC5A	GTIOC5B	GTIOC6A	GTIOC6B	—	—	—	—	—	—	—	—	GTIOC2B	GTIOC2A
00101b	SCI	—	—	—	—	—	CTS3	RXD3	TXD3	RXD1/ MISO1/ SCL1/ RXDX1/ SCL1	TXD1/ MOSI1/ SDA1/ TXDX1/ SIOX1/ SDA1	SCK1	CTS1_RTS1/ SS1	—	—

Table 19.10 输入输出引脚功能的寄存器设置(PORT5)(2of2)

PSEL[4:0] settings	Function	pin											
		P500	P501	P502	P503	P504	P505	P506	P507	P508	P511	P512	P513
100针产品		✓	✓	✓	✓	✓	✓	—	—	—	—	—	—

:可用一:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出歪斜规格(tGTISK)

Table 19.11 输入输出引脚功能（PORT6）的寄存器设置

PSEL[4:0] settings	Function	Pin															
		P600	P601	P602	P603	P604	P605	P606	P607	P608	P609	P610	P611	P612	P613	P614	P615
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z															
00001b	AGT	AGTIO3	AGTEE3	AGTO3	AGTIO4	AGTEE4	AGTO4	—	—	—	AGTO5	AGTO4	AGTO3	AGTO2	AGTO1	AGTO0	—
00011b	GPT	GTIOC6B	GTIOC6A	GTIOC7B	GTIOC7A	GTIOC8B	GTIOC8A	—	—	GTIOC4B	GTIOC5A	GTIOC5B	—	—	—	—	—
00100b	SCI	—	—	—	—	—	CTS8	CTS_RTS8	RXD8	—	—	—	—	—	—	—	—
00101b	SCI	SCK9	RXD9/ MISO9/ SCL9	TXD9/ MOSI9/ SDA9	CTS9_ RTS9/ SS9	CTS9	—	—	—	—	—	CTS7	CTS7_ RTS7/ SS7	SCK7	TXD7	RXD7	—
01001b	CLKOUT/ RTC	CLKOUT	—	—	—	—	—	RTCOUT	—	—	—	—	CLKOUT	—	—	—	—
01010b	CAC/ ADC12	CACREF	—	—	—	—	—	—	—	—	—	—	CACREF	—	—	—	—
01011b	BUS	RD	WR/ WR0	EBCLK	D13[A13/D13]	D12[A12/D12]	D11[A11/D11]	—	—	A00/BC0	CS1	CS0	—	D08[A08/D08]	D09[A09/D09]	D10[A10/D10]	—
10000b	CANFD	—	—	—	—	—	—	—	—	—	CTX1	CRX1	—	—	—	—	—
10011b	USBFS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	USB_VBUSEN
11100b	OSPI	OM_SIO4	OM_SIO2	OM_CS1	—	—	—	—	—	—	OM_ECS	OM_CS0	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IRQ7
DSCR[1:0] bits	驱动容量控制	L/M/H/HH	L/M/H/HH	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	—
100针产品		✓	✓	✓	—	—	—	—	—	✓	✓	✓	—	—	—	—	—

:可用一:禁止设置

Table 19.12 输入输出引脚功能的寄存器设置(PORT7)(1of2)

PSEL[4:0] settings	Function	Pin													
		P700	P701	P702	P703	P704	P705	P706	P707	P708	P709	P710	P711	P712	P713
00000b (value after reset)	Hi-Z/ JTAG/SWD	Hi-Z													
00001b	AGT	AGTO4	AGTO3	AGTO2	AGTO1	AGTO0	AGTIO0	—	—	—	—	—	AGTEE0	AGTOB0	AGTOA0
00011b	GPT*1	GTIOC5A	GTIOC5B	GTIOC6A	GTIOC6B	—	—	—	—	—	—	—	—	GTIOC2B	GTIOC2A
00101b	SCI	—	—	—	—	—	CTS3	RXD3	TXD3	RXD1/ MISO1/ SCL1/ RXDX1/ SCL1	TXD1/ MOSI1/ SDA1/ TXDX1/ SIOX1/ SDA1	SCK1	CTS1_RTS1/ SS1	—	—

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Table 19.12 Register settings for input/output pin function (PORT7) (2 of 2)

PSEL[4:0] settings	Function	Pin													
		P700	P701	P702	P703	P704	P705	P706	P707	P708	P709	P710	P711	P712	P713
00110b	SPI	MISOA_C	MOSIA_C	RSPCKA_C	SSLA0_C	SSLA1_C	SSLA2_C	—	—	SSLB3_B	—	—	—	—	—
01010b	CAC/ADC12	—	—	—	—	—	—	—	—	CACREF	—	—	—	—	—
01100b	CTSU	—	—	—	—	—	—	—	—	TS12	TS13	TS14	TS15	TS16	TS17
10000b	CANFD	—	—	—	—	CTX0	CRX0	—	—	—	—	—	—	—	—
10010b	SSIE	—	—	—	—	—	—	—	—	AUDIO_CLK	—	—	—	—	—
10100b	USBHS	—	—	—	—	—	—	USBHS_OVRCURB	USBHS_OVRCURA	—	—	—	—	—	—
10110b	ETHERC (MII)	ET0_ETXD1	ET0_ETXD0	ET0_ERXD1	ET0_ERXD0	ET0_RX_CLK	ET0_CRS	—	—	ET0_ETXD3	ET0_ETXD2	ET0_TX_ER	ET0_TX_CLK	—	—
10111b	ETHERC (RMII)	RMII0_TXD0_B	REF50CK0_B	RMII0_RXD0_B	RMII0_RXD1_B	RMII0_RX_ER_B	RMII0_CRS_DV_B	—	—	—	—	—	—	—	—
11101b	CEC	—	—	—	—	—	—	—	—	CECIO_A	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	—	—	—	IRQ7	IRQ8	IRQ11	IRQ10	—	—	—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—
144 pins product		✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓
100 pins product		—	—	—	—	—	—	—	—	✓	—	—	—	—	—

✓: Available
—: Setting prohibited

Note 1. There are 2 types output buffer which are middle drive and high drive. Recommend using same drive buffer for output skew spec (t_{GTISK})

Table 19.13 Register settings for input/output pin function (PORT8)

PSEL[4:0] settings	Function	Pin						
		P800	P801	P802	P803	P804	P805	P806
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00001b	AGT	AGTOA4	AGTOB4	—	—	—	—	—
00100b	SCI	CTS0	CTS8	—	—	—	—	—
00101b	SCI	—	—	—	—	—	TXD5	—
01011b	BUS	D14[A14/D14]	D15[A15/D15]	—	—	—	—	—
ASEL bit		AN125	AN126	AN127	AN128	—	—	—
ISEL bit		—	—	IRQ3	IRQ2	IRQ1	—	IRQ0
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓	✓
144 pins product		✓	✓	—	—	—	—	—
100 pins product		—	—	—	—	—	—	—

✓: Available
—: Setting prohibited

Table 19.12 输入输出引脚功能的寄存器设置(PORT7)(2of2)

PSEL[4:0] settings	Function	Pin													
		P700	P701	P702	P703	P704	P705	P706	P707	P708	P709	P710	P711	P712	P713
00110b	SPI	MISOA_C	MOSIA_C	RSPCKA_C	SSLA0_C	SSLA1_C	SSLA2_C	—	—	SSLB3_B	—	—	—	—	—
01010b	CAC/ADC12	—	—	—	—	—	—	—	—	CACREF	—	—	—	—	—
01100b	CTSU	—	—	—	—	—	—	—	—	TS12	TS13	TS14	TS15	TS16	TS17
10000b	CANFD	—	—	—	—	CTX0	CRX0	—	—	—	—	—	—	—	—
10010b	SSIE	—	—	—	—	—	—	—	—	AUDIO_CLK	—	—	—	—	—
10100b	USBHS	—	—	—	—	—	—	USBHS_OVRCURB	USBHS_OVRCURA	—	—	—	—	—	—
10110b	ETHERC (MII)	ET0_ETXD1	ET0_ETXD0	ET0_ERXD1	ET0_ERXD0	ET0_RX_CLK	ET0_CRS	—	—	ET0_ETXD3	ET0_ETXD2	ET0_TX_ER	ET0_TX_CLK	—	—
10111b	ETHERC (RMII)	RMII0_TXD0_B	REF50CK0_B	RMII0_RXD0_B	RMII0_RXD1_B	RMII0_RX_ER_B	RMII0_CRS_DV_B	—	—	—	—	—	—	—	—
11101b	CEC	—	—	—	—	—	—	—	—	CECIO_A	—	—	—	—	—
ASEL bit		—	—	—	—	—	—	—	—	—	—	—	—	—	—
ISEL bit		—	—	—	—	—	—	IRQ7	IRQ8	IRQ11	IRQ10	—	—	—	—
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N沟道开漏	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—
144针产品		✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓	✓	✓	✓
100针产品		—	—	—	—	—	—	—	—	✓	—	—	—	—	—

:可用—:禁止设置

注1.输出缓冲器有中驱动和高驱动两种。推荐使用相同的驱动缓冲器输出歪斜规格(tGTISK)

Table 19.13 输入输出引脚功能（PORT8）的寄存器设置

PSEL[4:0] settings	Function	Pin						
		P800	P801	P802	P803	P804	P805	P806
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00001b	AGT	AGTOA4	AGTOB4	—	—	—	—	—
00100b	SCI	CTS0	CTS8	—	—	—	—	—
00101b	SCI	—	—	—	—	—	TXD5	—
01011b	BUS	D14[A14/D14]	D15[A15/D15]	—	—	—	—	—
ASEL bit		AN125	AN126	AN127	AN128	—	—	—
ISEL bit		—	—	IRQ3	IRQ2	IRQ1	—	IRQ0
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓	✓
144针产品		✓	✓	—	—	—	—	—
100针产品		—	—	—	—	—	—	—

:可用—:禁止设置

Table 19.14 Register settings for input/output pin function (PORT9)

PSEL[4:0] settings	Function	Pin					
		P900	P901	P905	P906	P907	P908
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z					
00001b	AGT	—	AGTIO	—	—	—	—
00100b	SCI	TXD4	SCK4	—	—	—	—
01011b	BUS	A23	—	—	—	—	—
10011b	USBFS	—	—	USB_ID	USB_EXICEN	—	—
10100b	USBHS	—	—	—	—	USBHS_ID	USBHS_EXICEN
ASEL bit		—	—	—	—	—	—
ISEL bit		—	—	IRQ8	IRQ9	IRQ10	IRQ11
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓	✓
144 pins product		—	—	—	—	—	—
100 pins product		—	—	—	—	—	—

✓: Available
—: Setting prohibited

Table 19.15 Register settings for input/output pin function (PORTA)

PSEL[4:0] settings	Function	Pin				
		PA00	PA01	PA08	PA09	PA10
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00100b	SCI	TXD8	SCK8	—	—	—
10011b	USBFS	—	—	USB_OVRCURA	USB_OVRCURB	—
ASEL bit		—	—	—	—	—
ISEL bit		—	—	IRQ6	IRQ5	IRQ4
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
176 pins product		✓	✓	✓	✓	✓
144 pins product		—	—	—	—	—
100 pins product		—	—	—	—	—

✓: Available
—: Setting prohibited

Table 19.16 Register settings for input/output pin function (PORTB)

PSEL[4:0] settings	Function	Pin	
		PB00	PB01
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00101b	SCI	SCK3	CTS_RTS3
10100b	USBHS	USBHS_VBUSEN	USBHS_VBUS
ASEL bit		—	—
ISEL bit		—	—
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
176 pins product		✓	✓
144 pins product		—	—
100 pins product		—	—

✓: Available
—: Setting prohibited

Table 19.14 输入输出引脚功能（PORT9）的寄存器设置

PSEL[4:0] settings	Function	Pin					
		P900	P901	P905	P906	P907	P908
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z					
00001b	AGT	—	AGTIO	—	—	—	—
00100b	SCI	TXD4	SCK4	—	—	—	—
01011b	BUS	A23	—	—	—	—	—
10011b	USBFS	—	—	USB_ID	USB_EXICEN	—	—
10100b	USBHS	—	—	—	—	USBHS_ID	USBHS_EXICEN
ASEL bit		—	—	—	—	—	—
ISEL bit		—	—	IRQ8	IRQ9	IRQ10	IRQ11
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓	✓
144针产品		—	—	—	—	—	—
100针产品		—	—	—	—	—	—

:可用—:禁止设置

Table 19.15 输入输出引脚功能（PORTA）的寄存器设置

PSEL[4:0] settings	Function	Pin				
		PA00	PA01	PA08	PA09	PA10
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00100b	SCI	TXD8	SCK8	—	—	—
10011b	USBFS	—	—	USB_OVRCURA	USB_OVRCURB	—
ASEL bit		—	—	—	—	—
ISEL bit		—	—	IRQ6	IRQ5	IRQ4
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
176针产品		✓	✓	✓	✓	✓
144针产品		—	—	—	—	—
100针产品		—	—	—	—	—

:可用—:禁止设置

Table 19.16 输入输出引脚功能（PORTB）的寄存器设置

PSEL[4:0] settings	Function	Pin	
		PB00	PB01
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00101b	SCI	SCK3	CTS_RTS3
10100b	USBHS	USBHS_VBUSEN	USBHS_VBUS
ASEL bit		—	—
ISEL bit		—	—
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
176针产品		✓	✓
144针产品		—	—
100针产品		—	—

:可用—:禁止设置

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20. Port Output Enable for GPT (POEG)

20.1 Overview

The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state in one of the following ways:

- Input level detection of the GTETRGn (n = A to D) pins
- Output-disable request from the GPT
- Oscillation stop detection of the clock generation circuit
- Register settings

The GTETRGn (n = A to D) pins can be used as GPT external trigger input pins.

Table 20.1 lists the POEG specifications, Figure 20.1 shows a block diagram, and Table 20.2 lists the input pins.

Table 20.1 POEG specifications

Parameter	Specifications
Output-disable control through input level detection	• The GPT output pins can be disabled when a GTETRGn rising edge or high level is sampled after polarity and filter selection.
Output-disable request from the GPT	• When the GTIOCxA pin and the GTIOCxB pin are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG. Through reception of these requests, the POEG can control whether the GTIOCxA and GTIOCxB pins are output-disabled.
Output-disable control through oscillation stop detection	• The GPT output pins can be disabled when oscillation of the clock generation circuit stops.
Output-disable control by software (registers)	• The GPT output pins can be disabled by modifying the register settings.
Interrupt	• Interrupts can be generated by detecting the input level of external trigger input pins (GTETRGn pins). • Interrupts can be generated when all GPT output pins are driven to an active level simultaneously.
External trigger output to the GPT	• The GTETRGn signals can be output to the GPT after polarity and filter selection. (count start, count stop, count clear, up-count, down-count, or input capture function)
Noise filtering	• For input from the GTETRGn pins, PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be selected as the noise filtering clock. (Filtering is performed by sampling the input signals three times using the selected clock.) • Positive or negative polarity can be selected for any of the GTETRGn input pins. • Signal state after polarity and filter selection can be monitored.
TrustZone Filter	• Security attribution can be set for each groups.

Note: n = A to D, x = 0 to 9

20. GPT(POEG)的端口输出使能

20.1 Overview

端口输出使能(POEG)功能可以通过以下方式之一将通用PWM定时器(GPT)输出引脚置于输出禁用状态：

●GTETRn(n=AtoD)引脚的输入电平检测
●来自GPT的输出禁用请求
●时钟发生电路的振荡停止检测
●注册设置

GTETRn(n=AtoD)引脚可用作GPT外部触发输入引脚。
表20.1列出了POEG规范，图20.1显示了框图，表20.2列出了输入引脚。

Table 20.1 POEG specifications

Parameter	Specifications
通过输入电平检测进行输出禁用控制	• 在极性和滤波器选择后采样GTETRn上升沿或高电平时，可以禁用GPT输出引脚。
来自GPT的输出禁用请求	• 当GTIOCxA引脚和GTIOCxB引脚同时被驱动为有效电平时，GPT向POEG生成一个输出禁用请求。通过接收这些请求，POEG可以控制GTIOCxA和GTIOCxB引脚是否输出禁用。
通过振荡停止检测进行输出禁用控制	• 当时钟生成电路的振荡停止时，可以禁用GPT输出引脚。
通过软件（寄存器）进行输出禁用控制	• 通过修改寄存器设置可以禁用GPT输出引脚。
Interrupt	• 可以通过检测外部触发输入引脚（GTETRn引脚）的输入电平来产生中断。 • 当所有GPT输出引脚同时驱动到有效电平时，可能会产生中断。
到GPT的外部触发输出	• GTETRn信号可以在极性和滤波器选择后输出到GPT。（计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉功能）
噪声过滤	• 对于来自GTETRn引脚的输入，可以选择PCLKB1、PCLKB8、PCLKB32或PCLKB128作为噪声过滤时钟。（通过使用所选时钟对输入信号进行3次采样来执行滤波。） • 可以为任何GTETRn输入引脚选择正极性或负极性。 • 可以监控极性和滤波器选择后的信号状态。
TrustZone Filter	• 可以为每个组设置安全属性。

Note: n = A to D, x = 0 to 9

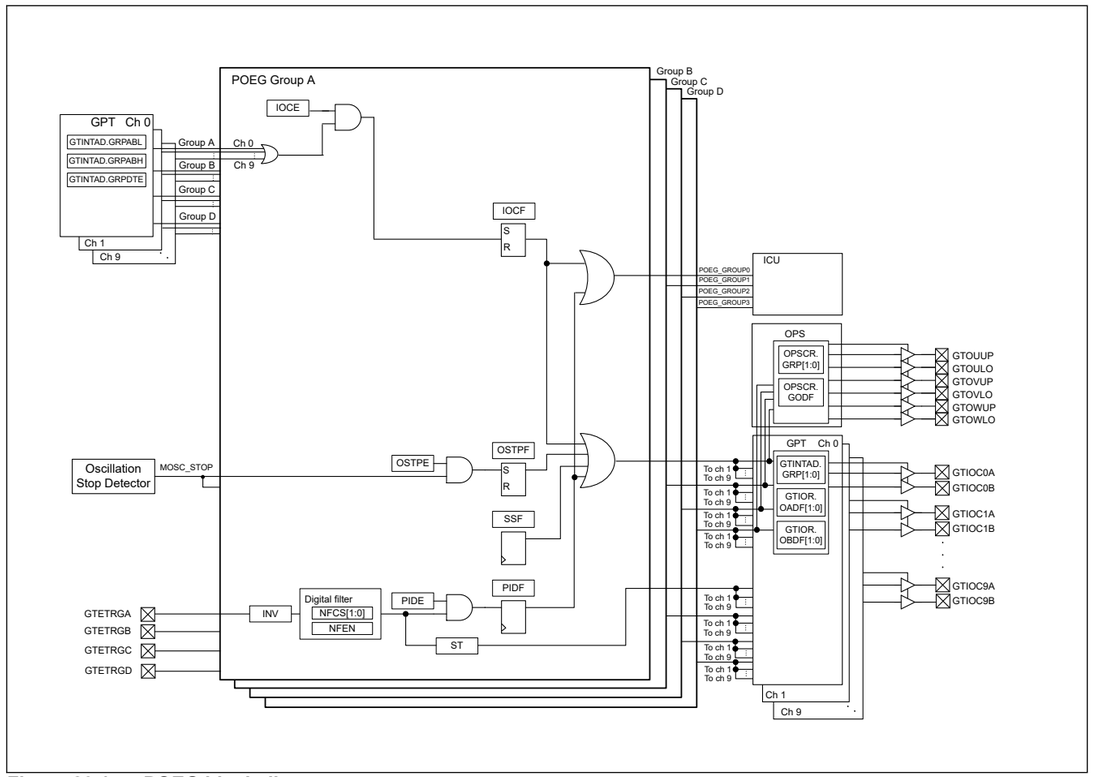


Figure 20.1 POEG block diagram

Table 20.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal or GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal or GPT external trigger input pin B
GTETRGC	Input	GPT output pin output-disable request signal or GPT external trigger input pin C
GTETRGD	Input	GPT output pin output-disable request signal or GPT external trigger input pin D

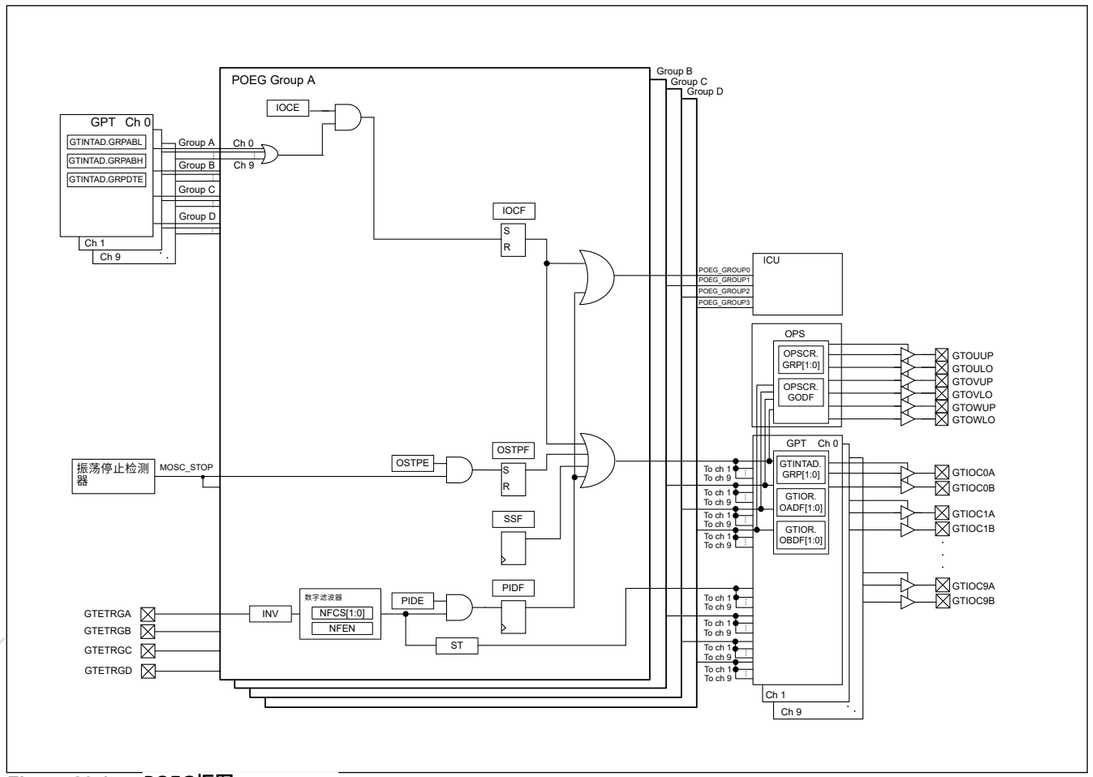


Figure 20.1 POEG框图

Table 20.2 POEG输入引脚

引脚名称	I/O	Description
GTETRGA	Input	GPT输出引脚输出禁止请求信号或GPT外部触发输入引脚A
GTETRGB	Input	GPT输出引脚输出禁止请求信号或GPT外部触发输入引脚B
GTETRGC	Input	GPT输出引脚输出禁止请求信号或GPT外部触发输入引脚C
GTETRGD	Input	GPT输出引脚输出禁止请求信号或GPT外部触发输入引脚D

20.2 Register Descriptions

20.2.1 POEGGn : POEG Group n Setting Register (n = A to D)

Base address: POEG = 0x4008_A000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)
0x200 (POEGGC)
0x300 (POEGGD)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIDF	Port Input Detection Flag 0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R/W*1
1	IOCF	Detection Flag for GPT Output-Disable Request 0: No output-disable request from GPT occurred. 1: Output-disable request from GPT occurred.	R/W*1
2	OSTPF	Oscillation Stop Detection Flag 0: No output-disable request from oscillation stop detection occurred 1: Output-disable request from oscillation stop detection occurred	R/W*1
3	SSF	Software Stop Flag 0: No output-disable request from software occurred 1: Output-disable request from software occurred	R/W
4	PIDE	Port Input Detection Enable 0: Disable output-disable requests from the GTETRGn pins 1: Enable output-disable requests from the GTETRGn pins	R/W*2
5	IOCE	Enable for GPT Output-Disable Request 0: Disable output-disable requests from GPT 1: Enable output-disable requests from GPT	R/W*2
6	OSTPE	Oscillation Stop Detection Enable 0: Disable output-disable requests from oscillation stop detection 1: Enable output-disable requests from oscillation stop detection	R/W*2
15:7	—	These bits are read as 0. The write value should be 0.	R/W
16	ST	GTETRGn Input Status Flag 0: GTETRGn input after filtering was 0 1: GTETRGn input after filtering was 1	R
27:17	—	These bits are read as 0. The write value should be 0.	R/W
28	INV	GTETRGn Input Reverse 0: Input GTETRGn as-is 1: Input GTETRGn in reverse	R/W
29	NFEN	Noise Filter Enable 0: Disable noise filtering 1: Enable noise filtering	R/W

20.2 注册说明

20.2.1 POEGGn:POEG组n设置寄存器(n=A到D)

Base address: POEG = 0x4008_A000

Offset address: 0x000 (POEGGA)
0x100 (POEGGB)
0x200 (POEGGC)
0x300 (POEGGD)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIDF	端口输入检测标志 0：未发生来自GTETRn引脚的输出禁止请求1：发生了来自GTETRn引脚的输出禁止请求。	R/W*1
1	IOCF	GPT输出禁用请求的检测标志 0：未发生来自GPT的输出禁用请求。1：发生了来自GPT的输出禁用请求。	R/W*1
2	OSTPF	振荡停止检测标志 0：未发生振荡停止检测的输出禁止请求1：发生了振荡停止检测的输出禁止请求	R/W*1
3	SSF	软件停止标志 0：没有来自软件的输出禁止请求1：有来自软件的输出禁止请求	R/W
4	PIDE	端口输入检测启用 0：禁止来自GTETRn引脚的输出禁止请求1：使能来自GTETRn引脚的输出禁止请求	R/W*2
5	IOCE	启用GPT输出禁用请求 0：禁用来自GPT的输出禁用请求1：启用来自GPT的输出禁用请求	R/W*2
6	OSTPE	振荡停止检测使能 0：禁止来自振荡停止检测的输出禁止请求1：允许来自振荡停止检测的输出禁止请求	R/W*2
15:7	—	这些位被读取为0。写入值应为0。	R/W
16	ST	GTETRn输入状态标志 0：滤波后的GTETRn输入为01：滤波后的GTETRn输入为1	R
27:17	—	这些位被读取为0。写入值应为0。	R/W
28	INV	GTETRn输入反向 0：按原样输入GTETRn1：反向输入GTETRn	R/W
29	NFEN	噪声过滤器启用 0：禁用噪声过滤1：启用噪声过滤	R/W

RA生态工作室

Bit	Symbol	Function	R/W
31:30	NFCS[1:0]	Noise Filter Clock Select 0 0: Sample GTETRGn pin input level three times every PCLKB 0 1: Sample GTETRGn pin input level three times every PCLKB/8 1 0: Sample GTETRGn pin input level three times every PCLKB/32 1 1: Sample GTETRGn pin input level three times every PCLKB/128	R/W

Note 1. Only 0 can be written to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGn (n = A to D) registers control the output-disable state of the GPT pins, interrupts, and the external trigger input to the GPT.

In the descriptions, POEGGn represents the POEGGn (n = A to D) registers.

20.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output-disable:

- Input level or edge detection of the GTETRGn pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled by GTINTAD. The GTINTAD.GRPABH and GTINTAD.GRPABL settings apply to the group selected by the GPT register GTINTAD.GRP[1:0] or OPSCR.GRP[1:0].
- Oscillation stop detection for the clock generation circuit
  While POEGGn.OSTPE is 1, the halt status of the main clock oscillator is detected and the POEGGn. OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the PWM output is disabled.

The output-disable state is controlled in the GPT module. The output-disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in GPTx. The output-disable of the 3-phase PWM output for BLDC motor control pins is set in the OPSCR.GRP[1:0] bits and OPSCR.GODF bit in GPT_OPS.

20.3.1 Pin Input Level Detection Operation

If the input conditions set in POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN, and POEGGn.INV occur on the GTETRGn pins, the GPT output pins are output-disabled.

20.3.1.1 Digital Filter

Figure 20.2 shows high-level detection by the digital filter. When a high level associated with the POEGGn.INV polarity setting is detected three times consecutively with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, the detected level is recognized as high, and the GPT output pins are output-disabled. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not output, changes of the levels on the GTETRGn pins are ignored.

Bit	Symbol	Function	R/W
31:30	NFCS[1:0]	噪声滤波器时钟选择 00：每PCLKB采样GTETRn引脚输入电平3次01：每PCLKB采样GTETRn引脚输入电平3次810：每PCLKB采样GTETRn引脚输入电平3次3211：每PCLKB采样GTETRn引脚输入电平3次128	R/W

注1.只能写入0来清除标志。
注2.复位后只能修改一次。

POEGGn(n=AtoD)寄存器控制GPT引脚的输出禁用状态、中断和GPT的外部触发输入。

在描述中，POEGGn代表POEGGn（n=A到D）寄存器。

20.3 输出禁用控制操作

如果满足以下任一条件，则GTIOCxA、GTIOCxB和BLDC电机控制引脚的3相PWM输出可设置为输出禁用：

●GTETRn引脚的输入电平或边沿检测
当POEGGn.PIDE为1时，POEGGn.PIDF标志设置为1。

●来自GPT的输出禁用请求
当POEGGn.IOCE为1时，如果禁用请求由GTINTAD启用，则POEGGn.IOCF标志设置为1。这GTINTAD.GRPABH和GTINTAD.GRPABL设置适用于GPT寄存器选择的组GTINTAD.GRP[1:0] or OPSCR.GRP[1:0].

●时钟产生电路的振荡停止检测
当POEGGn.OSTPE为1时，检测到主时钟振荡器的停止状态和POEGGn。OSTPF标志设置为1。

●SSF位设置
当POEGGn.SSF设置为1时，PWM输出被禁用。

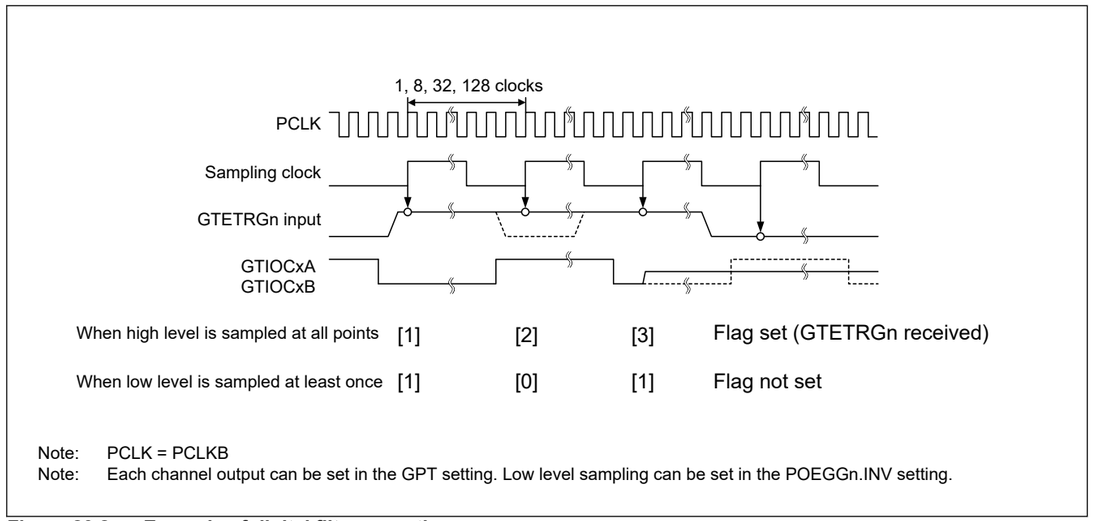
输出禁用状态由GPT模块控制。GTIOCxA和GTIOCxB引脚的输出禁用在GPTx中的GTINTAD.GRP[1:0]、GTIOR.OADF[1:0]和GTIOR.OBDF[1:0]位中设置。BLDC电机控制引脚的3相PWM输出的输出禁用在GPT_OPS中的OPSCR.GRP[1:0]位和OPSCR.GODF位中设置。

20.3.1 引脚输入电平检测操作

如果在POEGGn.PIDE、POEGGn.NFCS[1:0]、POEGGn.NFEN和POEGGn.INV中设置的输入条件发生在GTETRn引脚，GPT输出引脚输出禁用。

20.3.1.1 数字滤波器

图20.2显示了数字滤波器的高电平检测。当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续3次检测到与POEGGn.INV极性设置相关的高电平时，检测到的电平被识别为高电平，并且GPT输出引脚为输出禁用。如果在此间隔期间甚至检测到一个低电平，则检测到的电平不会被识别为高电平。此外，在不输出采样时钟的时间间隔内，GTETRn引脚的电平变化被忽略。



Note: PCLK = PCLKB
Note: Each channel output can be set in the GPT setting. Low level sampling can be set in the POEGGn.INV setting.

Figure 20.2 Example of digital filter operation

20.3.2 Output-Disable Requests from the GPT

For details on the operation, see the description for GTIOC Pin Output Negate Control in section 21, General PWM Timer (GPT).

20.3.3 Output-Disable Control Using Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are output-disabled for each group.

20.3.4 Output-Disable Control Using Registers

The GPT output pins can be directly controlled by writing 1 to the Software Stop flag, POEGGn.SSF.

20.3.5 Release from Output-Disable

To release the GPT output pins placed in the output-disable state, either return them to their initial state with a reset or clear all of the following flags:

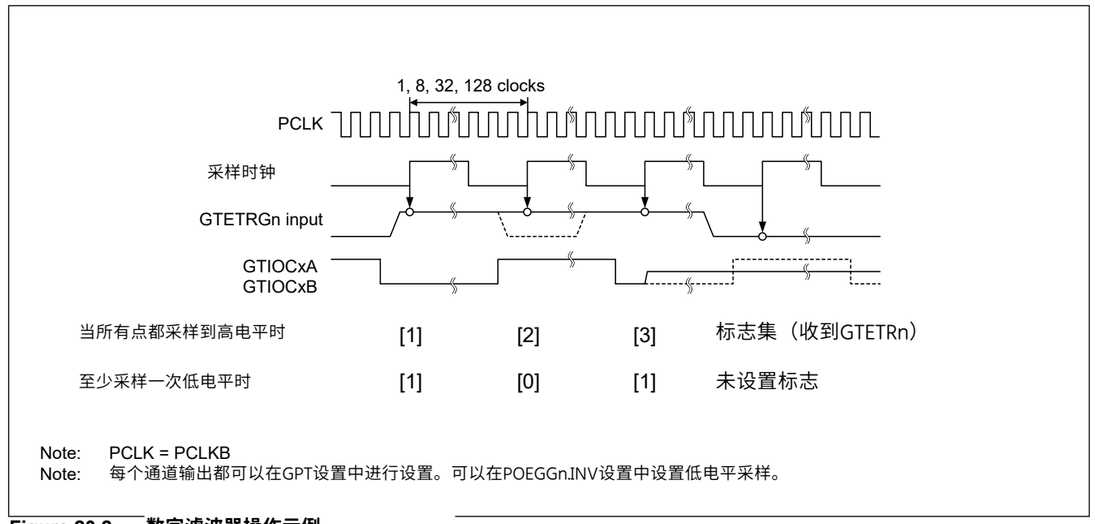
- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins, GTETRGn are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.OABHF and GTST.OABLF flags in the GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the flag set takes precedence.

Figure 20.3 shows the release timing for output-disable. The output-disable is released at the beginning of the next count cycle of the GPT after the flag is cleared.



Note: PCLK = PCLKB
Note: 每个通道输出都可以在GPT设置中进行设置。可以在POEGGn.INV设置中设置低电平采样。

Figure 20.2 数字滤波器操作示例

20.3.2 来自GPT的输出禁用请求

有关操作的详细信息，请参见第21节通用PWM定时器(GPT)中对GTIOC引脚输出取反控制的描述。

20.3.3 使用停止振荡检测的输出禁用控制

当时钟发生电路中的振荡停止检测功能检测到停止振荡时
POEGGn.OSTPE为1，每组的GPT输出引脚输出禁用。

20.3.4 使用寄存器的输出禁用控制

GPT输出引脚可以通过将1写入软件停止标志POEGGn.SSF来直接控制。

20.3.5 从输出禁用释放

要释放处于输出禁用状态的GPT输出引脚，可以通过复位将它们返回到初始状态，或者清除以下所有标志：

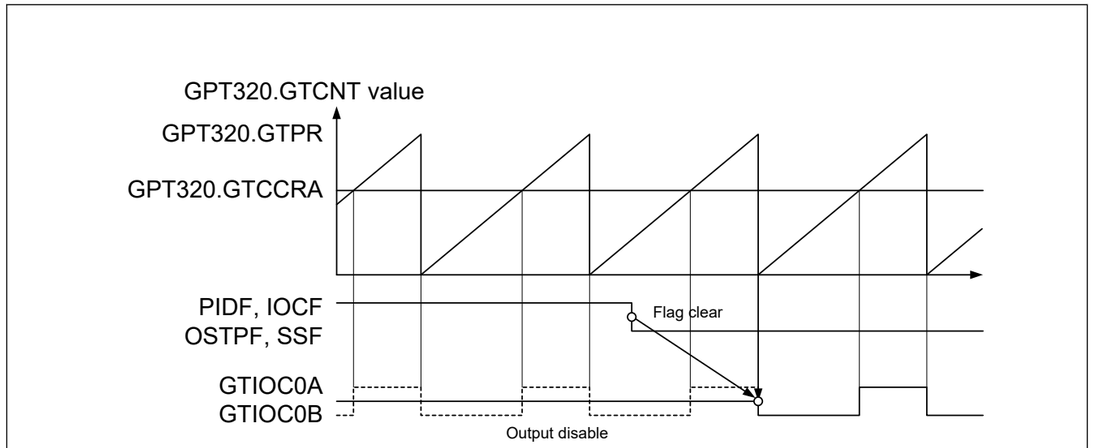
- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF

如果外部输入引脚GTETRn未被禁用且POEGGn.ST位未设置为0，则忽略向POEGGn.PIDF标志写入0（该标志不被清除）。

仅当GPT中的所有GTST.OABHF和GTST.OABLF标志都设置为0时，向POEGGn.IOCF标志写入0才有效（该标志被清除）。

如果时钟生成电路中的OSTDSR.OSTDF标志未设置为0，则忽略向POEGGn.OSTPF标志写入0（该标志不被清除）。此外，当标志设置和释放同时发生时，标志集优先。

图20.3显示了输出禁用的释放时序。标志清零后，在GPT的下一个计数周期开始时，输出禁用被释放。



Note: The base address of the registers are the same.

Figure 20.3 Output-disable release timing for GPT pin outputs

20.4 Interrupt Sources

The POEG generates an interrupt request when triggered by these sources:

- Output-disable control by the input level detection
- Output-disable request from the GPT

Table 20.3 lists the conditions for interrupt requests.

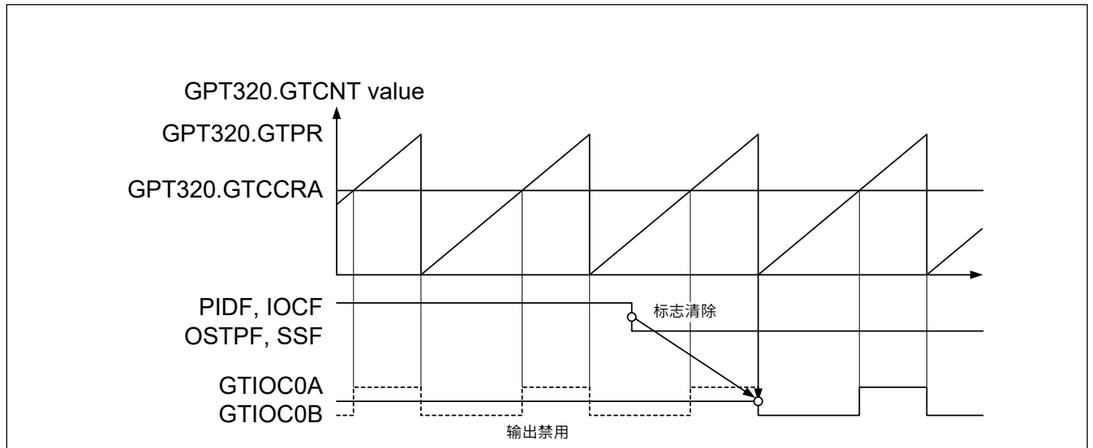
Table 20.3 Interrupt sources and conditions

Interrupt source	Symbol	Associated flag	Trigger conditions
POEG group A interrupt	POEG_GROUPA	POEGGA.IOCF	An output-disable request from a GPT disable request occurred
		POEGGA.PIDF	An output-disable request from the GTETRGA pin occurred
POEG group B interrupt	POEG_GROUPB	POEGGB.IOCF	An output-disable request from a GPT disable request occurred
		POEGGB.PIDF	An output-disable request from the GTETRGB pin occurred
POEG group C interrupt	POEG_GROUPC	POEGGC.IOCF	An output-disable request from a GPT disable request occurred
		POEGGC.PIDF	An output-disable request from the GTETRGC pin occurred
POEG group D interrupt	POEG_GROUPD	POEGGD.IOCF	An output-disable request from a GPT disable request occurred
		POEGGD.PIDF	An output-disable request from the GTETRGD pin occurred

20.5 External Trigger Output to the GPT

The POEG outputs signals generated by filtering and level detection of GTETRGn pins input signals as the GPT operation trigger signal for the following:

- Count start
- Count stop
- Count clear
- Up-count
- Down-count
- Input capture



Note: 寄存器的基地址相同。

Figure 20.3 GPT引脚输出的输出禁用释放时序

20.4 中断源

当这些源触发时，POEG会产生一个中断请求：

●通过输入电平检测进行输出禁止控制

●来自GPT的输出禁用请求

表20.3列出了中断请求的条件。

Table 20.3 中断源和条件

中断源	Symbol	相关标志	触发条件
POEGA组中断	POEG_GROUPA	POEGGA.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGA.PIDF	发生了来自GTETRGA引脚的输出禁用请求
POEGB组中断	POEG_GROUPB	POEGGB.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGB.PIDF	发生来自GTETRGB引脚的输出禁用请求
POEGC组中断	POEG_GROUPC	POEGGC.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGC.PIDF	发生了来自GTETRGC引脚的输出禁用请求
POEGD组中断	POEG_GROUPD	POEGGD.IOCF	发生了来自GPT禁用请求的输出禁用请求
		POEGGD.PIDF	发生来自GTETRGD引脚的输出禁用请求

20.5 到GPT的外部触发输出

POEG输出GTETRn管脚输入信号滤波和电平检测产生的信号作为GPT操作触发信号，用于以下用途：

●计数开始

●计数停止

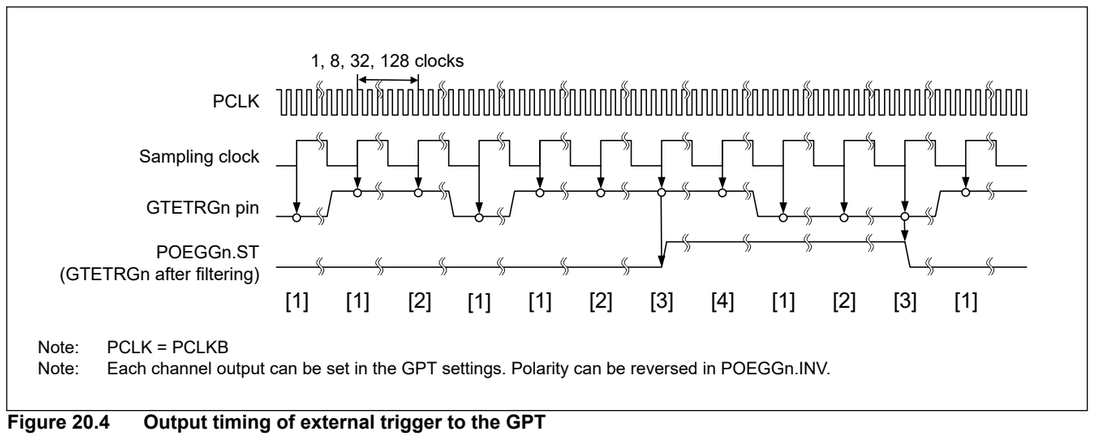
●清点

- Up-count
- Down-count

●输入捕捉

For the POEGGn.INV polarity setting signal, when the same level is input three times continuously with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, that value is output. Set the control registers the same as for the input level detection operation described in section 20.3.1. Pin Input Level Detection Operation The state after filtering can be monitored in POEGGn.ST.

Figure 20.4 shows the output timing of an external trigger to the GPT.



Note: PCLK = PCLKB
Note: Each channel output can be set in the GPT settings. Polarity can be reversed in POEGGn.INV.

Figure 20.4 Output timing of external trigger to the GPT

20.6 Usage Notes

20.6.1 Transition to Software Standby Mode

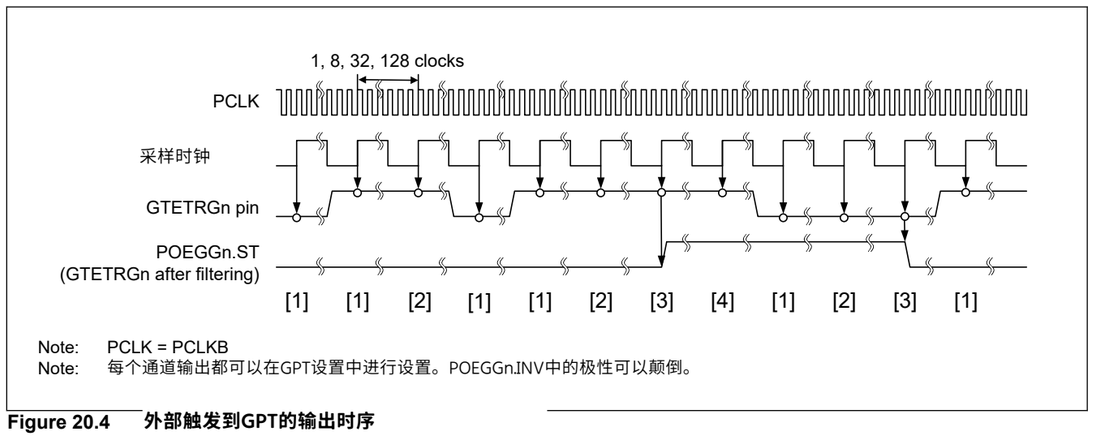
When using the POEG, do not invoke Software Standby mode. In this mode, the POEG stops and therefore output disable of the pins cannot be controlled.

20.6.2 Specifying Pins Associated with the GPT

The POEG controls output-disable only when a pin is associated with the GPT in the PmnPFS.PMR and PmnPFS.PSEL settings. When the pin is specified as a general I/O pin, the POEG does not perform output-disable control.

对于POEGGn.INV极性设置信号，当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续输入相同电平3次时，输出该值。控制寄存器的设置与20.3.1节中描述的输入电平检测操作相同。引脚输入电平检测操作滤波后的状态可以在POEGGn.ST中监控。

图20.4显示了外部触发到GPT的输出时序。



Note: PCLK = PCLKB
Note: 每个通道输出都可以在GPT设置中进行设置。POEGGn.INV中的极性可以颠倒。

Figure 20.4 外部触发到GPT的输出时序

20.6 使用说明

20.6.1 过渡到软件待机模式

使用POEG时，请勿调用软件待机模式。在此模式下，POEG停止，因此无法控制引脚的输出禁用。

20.6.2 指定与GPT关联的引脚

仅当引脚与PmnPFS.PMR和PmnPFS.PSEL设置中的GPT关联时，POEG才控制输出禁用。当引脚指定为通用IO引脚时，POEG不执行输出禁用控制。

21. General PWM Timer (GPT)

21.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 4 channels and a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.

Table 21.1 lists the GPT specifications, Table 21.2 shows the GPT functions, and Figure 21.1 shows a block diagram.

Table 21.1 GPT specifications

Parameter	Description
Functions	• 32 bits × 4 channels (GPT32n (n = 0 to 3)) • 16 bits × 6 channels (GPT16m (m = 4 to 9)) • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation • Synchronous starting, stopping and clearing counters for arbitrary channels • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 8 ELC events • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of 4 external triggers • Output pin disable function by detected short-circuits between output pins • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW. • Period count function • Logical operation between the channel output • Bus clock: PCLKA, Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64)

Table 21.2 GPT functions (1 of 2)

Parameter	Description
Count clock	PCLKD PCLKD/2 PCLKD/4 PCLKD/8 PCLKD/16 PCLKD/32 PCLKD/64 PCLKD/256 PCLKD/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR

21. 通用PWM定时器(GPT)

21.1 Overview

通用PWM定时器(GPT)是一个具有GPT32×4通道的32位定时器和一个具有GPT16×6通道的16位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，
可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。

表21.1列出了GPT规范，表21.2显示了GPT功能，图21.1显示了框图。

Table 21.1 GPT specifications

Parameter	Description
Functions	• 32位×4通道(GPT32n(n=0到3)) • 16位×6通道(GPT16m(m=4to9)) • 每个计数器的递增计数或递减计数（锯齿波）或递增递减计数（三角波） • 每个通道可独立选择时钟源 • 每个通道两个输入输出引脚 • 每个通道两个输出比较输入捕捉寄存器 • 每个通道的两个输出比较输入捕捉寄存器，提供四个寄存器作为缓冲寄存器，在不使用缓冲时可以作为比较寄存器工作 • 在输出比较操作中，缓冲器切换可以处于波峰或波谷，从而能够生成横向不对称的PWM波形 • 用于在每个通道中设置帧周期的寄存器，能够在上溢或下溢时产生中断 • 在PWM操作中产生死区 • 任意通道的同步启动、停止和清除计数器 • 响应最多8个ELC事件的计数开始、计数停止、计数清除、递增计数、递减计数或输入捕获操作 • 计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉操作以响应两个输入引脚的状态 • 计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉操作，以响应最多4个外部触发 • 通过检测到输出引脚之间的短路禁用输出引脚功能 • 可生成控制无刷直流电机的PWM波形 • 比较匹配A到F事件、上溢下溢事件和输入UVW边缘事件可以输出到ELC • 为输入捕获和输入UVW启用噪声滤波器。 • 周期计数功能 • 通道输出之间的逻辑运算 • 总线时钟：PCLKA，核心时钟：PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64)

Table 21.2 GPT函数(1of2)

Parameter	Description
计数时钟	PCLKD PCLKD/2 PCLKD/4 PCLKD/8 PCLKD/16 PCLKD/32 PCLKD/64 PCLKD/256 PCLKD/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
输出比较输入捕捉寄存器(GTCCR)	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF
周期设定寄存器	GTPR

Table 21.2 GPT functions (2 of 2)

Parameter		Description
Cycle setting buffer register		GTPBR
I/O pins		GTIOCnA GTIOCnB (n = 0 to 9)
External trigger input pin*1		GTETRGA GTETRGB GTETRGC GTETRGD
Counter clear sources		GTPR register compare match Input capture Input pin status ELC event input GTETRGn (n = A to D) pin input
Period count function		Available (GPT32n (n = 0, 1), GPT16m (m = 4 to 6))
Compare match output	Low output	Available
	High output	Available
	Toggle output	Available
Input capture function		Available
Automatic addition of dead time		Available (no dead time buffer)
PWM mode		Available
Phase count function		Available
Buffer operation		Double buffer Simultaneous operation disable control for multiple channels
One-shot operation		Available
DMAC/DTC activation		All the interrupt sources
Brushless DC motor control function		Available
Interrupt sources		9 sources • GTCCRA comare match/input capture(GPTn_CCMPA) • GTCCRB comare match/input capture(GPTn_CCMPB) • GTCCRC comare match(GPTn_CMPC) • GTCCRD comare match(GPTn_CMPD) • GTCCRE comare match(GPTn_CMPE) • GTCCRF comare match(GPTn_CMPF) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF) • GTPC count stop(GPTx_PC) (x = 0,1,4-6)
Event linking (ELC) function		Available*2
Noise filtering function		Available
Logical operation between the channel output		Available
TrustZone Filter		Available

Note 1. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPCRD.MSTPDn (n = 11 to 14) bit.
Note 2. see section 21.5. Operations Linked by ELC

Table 21.2 GPT功能（2个中的2个）

Parameter		Description
周期设置缓冲寄存器		GTPBR
I/O pins		GTIOCnA GTIOCnB (n = 0 to 9)
外部触发输入引脚*1		GTETRGA GTETRGB GTETRGC GTETRGD
反清源		GTPR寄存器比较匹配 输入捕捉 输入引脚状态EL C事件输入 GTETRn(n=AtoD)引脚输入
周期计数功能		可用（GPT32n（n=0、1）、GPT16m（m=4到6））
比较匹配输出	低输出	Available
	高输出	Available
	切换输出	Available
输入捕捉功能		Available
自动添加死区时间		可用（无死区时间缓 冲区）
PWM mode		Available
相位计数功能		Available
缓冲操作		双缓冲 多通道同时操作禁用控制
One-shot operation		Available
DMAC/DTC activation		所有中断源
直流无刷电机控制功能		Available
中断源		9 sources • GTCCRA comare match/input capture(GPTn_CCMPA) • GTCCRB comare match/input capture(GPTn_CCMPB) • GTCCRC comare match(GPTn_CMPC) • GTCCRD comare match(GPTn_CMPD) • GTCCRE comare match(GPTn_CMPE) • GTCCRF comare match(GPTn_CMPF) • GTCNT溢出（GTPR比较匹配）（GPTn_OVF） • GTCNT underflow (GPTn_UDF) • GTPC count stop(GPTx_PC) (x = 0,1,4-6)
事件链接(ELC)功能		Available*2
噪音过滤功能		Available
通道输出之间的逻辑运算		Available
TrustZone Filter		Available

注1.GTETRn通过POEG模块连接到GPT。因此，要使用GPT功能，通过清除
MSTPCRD.MSTPDn（n=11到14）位。
注2：见第21.5节。由ELC链接的操作

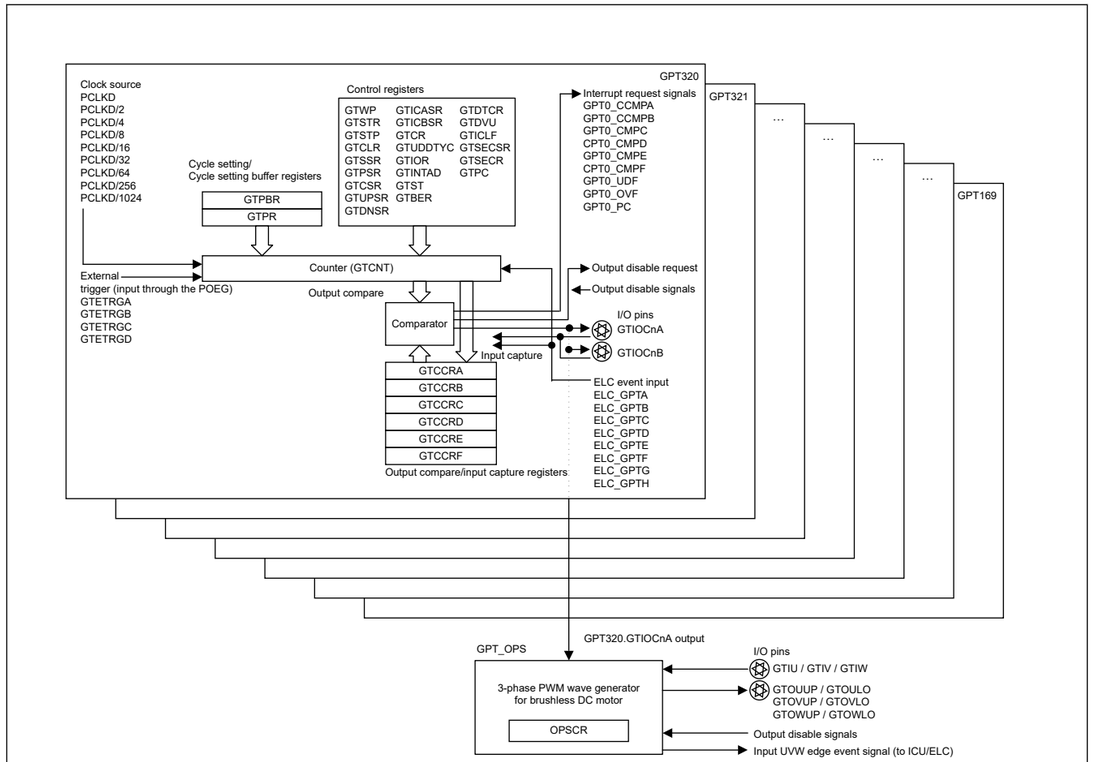


Figure 21.1 GPT block diagram

Figure 21.2 shows an example using multiple GPTs.

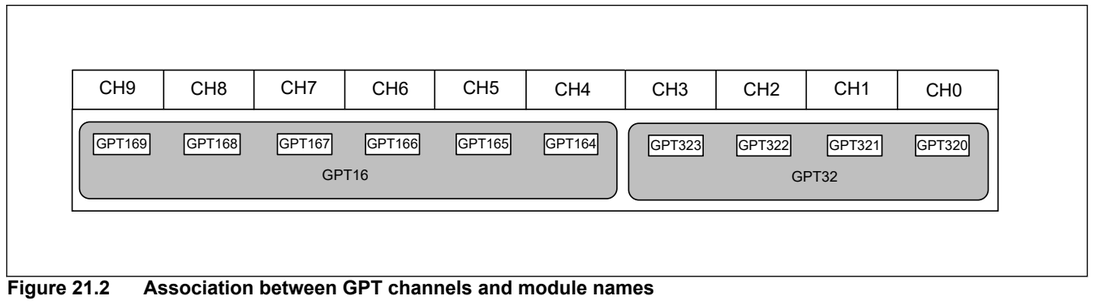


Figure 21.2 Association between GPT channels and module names

Table 21.3 lists the I/O pins.

Table 21.3 GPT I/O pins (1 of 2)

Channel	Pin name	I/O	Function
Common	GTETRGx	Input	External trigger input pin x (input through the POEG)
GPT32n	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin

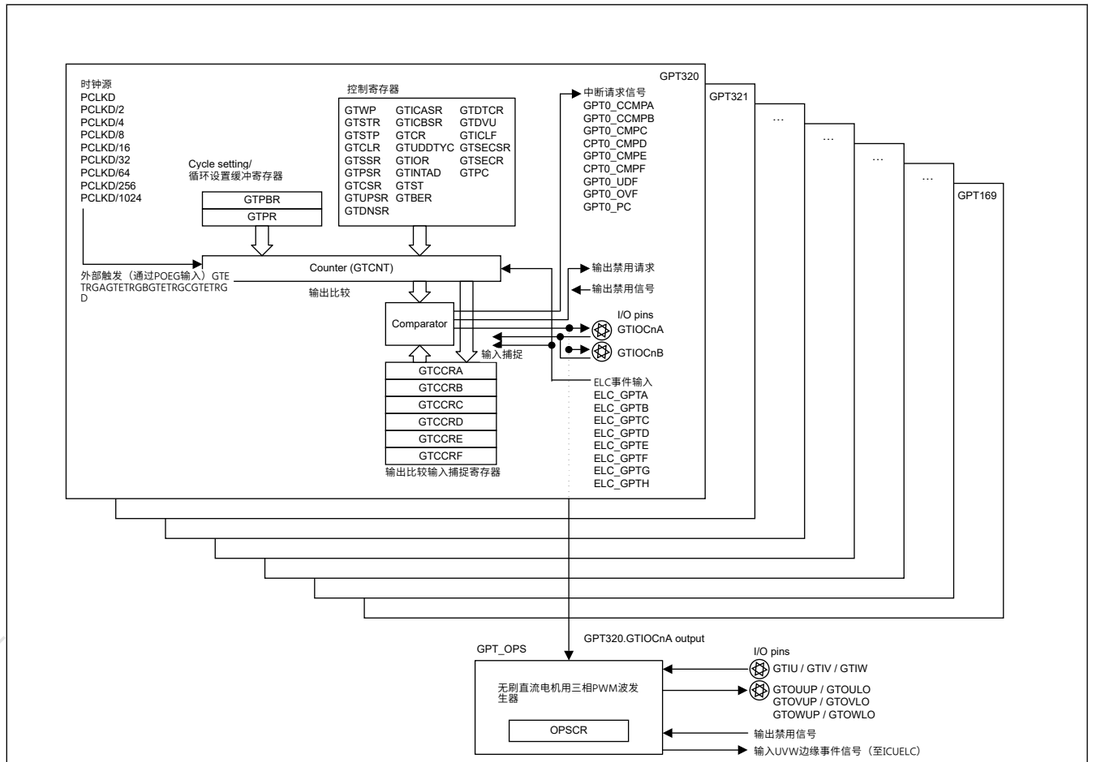


Figure 21.1 GPT框图

图21.2显示了一个使用多个GPT的示例。

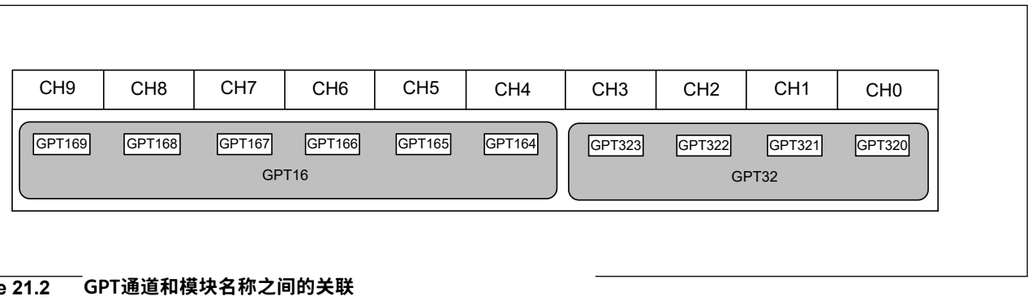


Figure 21.2 GPT通道和模块名称之间的关联

表21.3列出了IO引脚。

Table 21.3 GPTIO引脚（2个中的1个）

Channel	引脚名称	I/O	Function
Common	GTETRGx	Input	外部触发输入引脚x（通过POEG输入）
GPT32n	GTIOCnA	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOCnB	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚

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Table 21.3 GPT I/O pins (2 of 2)

Channel	Pin name	I/O	Function
GPT16m	GTIOCnA	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOCnB	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

Note: x: A to D
n: 0 to 3
m: 4 to 9

21.2 Register Descriptions

21.2.1 GTWP : General PWM Timer Write-Protection Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	Register Write Disable 0: Write to the register enabled 1: Write to the register disabled	R/W
1	STRWP	GTSTR.CSTRT Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
2	STPWP	GTSTP.CSTOP Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
3	CLRWP	GTCLR.CCLR Bit Write Disable 0: Write to the bit is enabled 1: Write to the bit is disabled	R/W
4	CMNWP	Common Register Write Disabled 0: Write to the register is enabled 1: Write to the register is disabled	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Table 21.3 GPTIO引脚（2个中的2个）

Channel	引脚名称	I/O	Function
GPT16m	GTIOCnA	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOCnB	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT_OPS	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）

Note: x: A to D
n: 0 to 3
m: 4 to 9

21.2 注册说明

21.2.1 GTWP:通用PWM定时器写保护寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PRKEY[7:0]								—	—	—	CMNWP	CLRWP	STPWP	STRWP	WP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	WP	寄存器写禁用 0：允许写入寄存器1：禁止写入寄存器	R/W
1	STRWP	GTSTR.CSTRT位写入禁止 0：允许写入位1：禁止写入位	R/W
2	STPWP	GTSTP.CSTOP位写禁止 0：允许写入位1：禁止写入位	R/W
3	CLRWP	GTCLR.CCLR位写入禁止 0：允许写入位1：禁止写入位	R/W
4	CMNWP	公共寄存器写入禁用 0：允许写入寄存器1：禁止写入寄存器	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
15:8	PRKEY[7:0]	GTWP Key Code When 0xA5 is written to these bits, writing to the WP, STRWP, STPWP, CLRWP, and CMNWP bits are permitted. These bits are read as 0.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

GTWP enables or disables writing to registers to prevent accidental modification. Protection by the GTWP register is only for the writes by the CPU. GTWP does not protect registers from updates that occur in association with CPU writes.

WP bit (Register Write Disable)

The following is a list of write enabled or disabled registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU, GTICLF, GTPC.

STRWP bit (GTSTR.CSTRT Bit Write Disable)

The STRWP bit enables or disables starting the updating of counter values by writing to the CSTRTn bit (n = 0 to 9) corresponding to a channel number in the GTSTR register.

The bit position of each CSTRTn bit in the GTSTR register is allocated to the channel with the corresponding number, and writing to the GTSTR register for any channel results in writing to the registers of all channels. The STRWP bit for each channel does not control writing but only controls updating of the CSTRT bit for the corresponding channel in the case of simultaneous writing to all channels.

Thus, in the case of writing to the CSTRT bits of a channel for which the setting of the STRWP bit is 1(disabling writing), the CSTRT bit for the given channel will not be updated, but the CSTRT bits corresponding to channel for which the setting of the STRWP bit is 0 (enabling writing) will be updated. For example, when the setting of the GTWP.STRWP bit of GPT channel 0 is 0 (enabling writing), writing 1 to the GTSTR.CSTRT0 bit of GPT channel 1 when its current setting is 0 will lead to updating of the value, and the GPT320.GTCNT counter starts running. When the setting of the GTWP.STRWP bit of GPT channel 0 is 1(disabling writing), writing 1 to the GTSTR.CSTRT0 bit of GPT channel 1 when its current setting is 0 will leave the bit with the value 0, and the GPT320.GTCNT counter will not start running.

If you want to protect all bits in the GTSTR register from being updated, set the STRWP bits of all channels to 1.

STPWP bit (GTSTP.CSTOP Bit Write Disable)

The STPWP bit enables or disables starting the updating of counter values by writing to the CSTOPn bit (n = 0 to 9) corresponding to a channel number in the GTSTP register.

The bit position of each CSTOPn bit in the GTSTP registers is allocated to the channel with the corresponding number, and the writing to the GTSTP register for any channel results in writing to the registers of all channels. The STPWP bit for each channel does not control writing but only controls updating of the CSTOP bit for the corresponding channel in the case of simultaneous writing to all channels.

Thus, in the case of writing to the CSTOP bits of a channel for which the setting of the STPWP bit is 1(disabling writing), the CSTOP bit for the given channel will not be updated, but the CSTOP bits corresponding to channel for which the setting of the STPWP bit is 0 (enabling writing) will be updated. For example, when the setting of the GTWP.STPWP bit of GPT channel 0 is 0(enabling writing), writing 1 to the GTSTP.CSTOP0 bit of GPT channel 1 when its current setting is 0 will lead to updating of the value, and the GPT320.GTCNT counter is stopped. When the setting of the GTWP.STPWP bit of GPT channel 0 is 1 (disabling writing), writing 1 to the GTSTP.CSTOP0 bit of GPT channel 1 when its current setting is 0 will leave the bit with the value 0, and the GPT320.GTCNT counter will not be stopped.

If you want to protect all bits in the GTSTP register from being updated, set the STPWP bits of all channels to 1.

CLRWP bit (GTCLR.CCLR Bit Write Disable)

CLRWP bit enables or disables starting the updating of counter values by writing to the CCLRn bit (n = 0 to 9) corresponding to a channel number in the GTCLR register.

The bit position of each CCLRn bit in the GTCLR registers is allocated to the channel with the corresponding number, and the writing to the GTCLR register for any channel results in writing to the registers of all channels. The CLRWP bit for each channel does not control writing but only controls updating of the CCLR bit for the corresponding channel in the case of simultaneous writing to all channels.

Bit	Symbol	Function	R/W
15:8	PRKEY[7:0]	GTWP密钥代码 当0xA5写入这些位时，写入WP、STRWP、STPWP、CLRWP和允许CMNWP位。这些位读为0。	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

GTWP启用或禁用写入寄存器以防止意外修改。GTWP寄存器的保护只针对CPU的写操作。GTWP不保护寄存器免受与CPU写入相关的更新。

WP位（寄存器写禁止）

以下是写启用或禁用寄存器的列表：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU, GTICLF, GTPC.

STRWP位（GTSTR.CSTRT位写入禁止）

STRWP位通过写入与GTSTR寄存器中的通道号相对应的CSTRTn位（n=0到9）来启用或禁用开始更新计数器值。

GTSTR寄存器中每个CSTRTn位的位位置分配给对应编号的通道，对任何通道写入GTSTR寄存器都会导致写入所有通道的寄存器。每个通道的STRWP位不控制写入，而仅控制在同时写入所有通道的情况下相应通道的CSTRT位的更新。

因此，在写入STRWP位设置为1的通道的CSTRT位（禁止写入）的情况下，给定通道的CSTRT位将不会被更新，但对应于通道的CSTRT位将被更新。STRWP位的设置为0（允许写入）将被更新。例如，当GPT通道0的GTWP.STRWP位设置为0（允许写入）时，当前设置为0时向GPT通道1的GTSTR.CSTRT0位写入1将导致值更新，并且GPT320.GTCNT计数器开始运行。当GPT通道0的GTWP.STRWP位设置为1时（禁止写入），当前设置为0时，向GPT通道1的GTSTR.CSTRT0位写入1将保留该位的值0，而GPT320.GTCNT计数器不会开始运行。

如果要保护GTSTR寄存器中的所有位不被更新，请将所有通道的STRWP位设置为1。

STPWP位（GTSTP.CSTOP位写入禁用）

STPWP位通过写入与GTSTP寄存器中的通道号对应的CSTOPn位（n=0到9）来启用或禁用开始更新计数器值。

GTSTP寄存器中每个CSTOPn位的位位置分配给对应编号的通道，对任何通道写入GTSTP寄存器都会导致写入所有通道的寄存器。每个通道的STPWP位不控制写入，而仅控制在同时写入所有通道的情况下相应通道的CSTOP位的更新。

因此，在写入STPWP位设置为1的通道的CSTOP位（禁止写入）的情况下，给定通道的CSTOP位将不会被更新，但对应于其通道的CSTOP位STPWP位的设置为0（允许写入）将被更新。例如，当GPT通道0的GTWP.STPWP位设置为0（允许写入）时，当前设置为0时向GPT通道1的GTSTP.CSTOP0位写入1将导致值更新，并且GPT320.GTCNT计数器停止。当GPT通道0的GTWP.STPWP位设置为1时（禁止写入），当前设置为0时向GPT通道1的GTSTP.CSTOP0位写入1将保留该位的值0，而GPT320.GTCNT计数器不会停止。

如果要保护GTSTP寄存器中的所有位不被更新，请将所有通道的STPWP位设置为1。

CLRWP位（GTCLR.CCLR位写入禁止）

CLRWP位通过写入与GTCLR寄存器中的通道号对应的CCLRn位（n=0到9）来启用或禁用开始更新计数器值。

GTCLR寄存器中每个CCLRn位的位位置分配给对应编号的通道，对任何通道写入GTCLR寄存器都会导致写入所有通道的寄存器。每个通道的CLRWP位不控制写入，而仅控制在同时写入所有通道的情况下相应通道的CCLR位的更新。

Thus, in the case of writing to the CCLR bits of a channel for which the setting of the CLRWP bit is 1(disabling writing), the CCLR bit for the given channel will not be updated, but the CCLR bits corresponding to channel for which the setting of the CLRWP bit is 0 (enabling writing) will be updated. For example, when the setting of the GTWP.CLRWP bit of GPT channel 0 is 0(enabling writing), writing 1 to the GTCLR.CCLR0 bit of GPT channel 1 when its current setting is 0 will lead to updating of the value, and the GPT320.GTCNT counter is cleared. When the setting of the GTWP.CLRWP bit of GPT channel 0 is 1(disabling writing), writing 1 to the GTCLR.CCLR0 bit of GPT channel 1 when its current setting is 0 will leave the bit with the value 0, and the GPT320.GTCNT counter will not be cleared.

If you want to protect all bits in the GTCLR register from being updated, set the CLRWP bits of all channels to 1.

CMNWP bit (Common Register Write Disabled)

CMNWP bit enables or disables starting the updating of counter values by writing to the SECSELn bit (n = 0 to 9) corresponding to a channel number in the GTSECSR register or to the GTSECR register.

The bit position of each SECSEL bit in the GTSECSR registers is allocated to the channel with the corresponding number, and the writing to the GTSECSR register for any channel results in writing to the registers of all channels. Writing to the GTSECR register of any channel leads to writing to the registers of all channels. The CMNWP bit for each channel does not control writing but only controls updating of the SECSEL bit and the GTSECR register value for the corresponding channel in the case of simultaneous writing to all channels.

Thus, in the case of writing to the SECSEL bit and the GTSECR register value of a channel for which the setting of the CMNWP bit is 1(disabling writing), the SECSEL bit and the GTSECR register value for the given channel will not be updated, but the SECSEL bit and the GTSECR register value corresponding to channel for which the setting of the CMNWP bit is 0(enabling writing) will be updated.

For example, when the setting of the GTWP.CMNWP bit of GPT channel 0 is 0 (enabling writing), writing to the GTSECSR.SECSEL0 bit of GPT channel 1 will lead to updating of the value of the GTSECSR.SECSEL0 bit of GPT channel 0. In the same way, writing to the GPT321.GTSECR register will update the value of the GPT320.GTSECR register. When the setting of the GTWP.CMNWP bit of GPT channel 0 is 1 (disabling writing), writing to the GTSECSR.SECSEL0 bit of GPT channel 1 will not lead to updating of the value of the GTSECSR.SECSEL0 bit of GPT channel 0. In the same way, writing to the GPT321.GTSECR register will not lead to updating of the value of the GPT320.GTSECR register.

If you want to protect all bits in the GTSECSR and GTSECR registers from being updated, set the CMNWP bits of all channels to 1.

PRKEY[7:0] bit (GTWP Key Code)

This bit controls whether the WP, STRWP, STPWP, CLRWP, and CMNWP bits can be overwritten.

21.2.2 GTSTR : General PWM Timer Software Start Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x04

Bit position:	31																												0
Bit field:	CSTRT31 to CSTRT0																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	Channel n GTCNT Count Start (n : the same as bit position value) 0: GTCNT counter not start 1: GTCNT counter start	R/W

Note 1. The bits that can be used vary depending on the product. The n of CSTRTn is the same as the GPT channel number. For this product, n is 0 to 9.

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 9.

因此，在写入CLRWP位设置为1（禁止写入）的通道的CCLR位的情况下，给定通道的CCLR位将不会被更新，但对应于通道的CCLR位将被更新。CLRWP位的设置为0（允许写入）将被更新。例如，当GPT通道0的GTWP.CLRWP位设置为0（允许写入）时，当前设置为0时向GPT通道1的GTCLR.CCLR0位写入1将导致值更新，并且GPT320.GTCNT计数器清零。当GPT通道0的GTWP.CLRWP位设置为1时（禁止写入），当前设置为0时向GPT通道1的GTCLR.CCLR0位写入1将保留该位的值0，而GPT320.GTCNT计数器不会被清除。

如果要保护GTCLR寄存器中的所有位不被更新，请将所有通道的CLRWP位设置为1。

CMNWP位（公共寄存器写入禁用）

CMNWP位通过写入与GTSECSR寄存器中的通道号或GTSECR寄存器中对应的SECSELn位（n=0至9）来启用或禁用开始更新计数器值。

GTSECSR寄存器中每个SECSEL位的位位置分配给对应编号的通道，对任何通道写入GTSECSR寄存器都会导致写入所有通道的寄存器。写入任何通道的GTSECR寄存器会导致写入所有通道的寄存器。每个通道的CMNWP位不控制写入，而仅控制在同时写入所有通道的情况下相应通道的SECSEL位和GTSECR寄存器值的更新。

因此，在写入CMNWP位设置为1（禁止写入）的通道的SECSEL位和GTSECR寄存器值的情况下，将不会更新给定通道的SECSEL位和GTSECR寄存器值，但与CMNWP位设置为0（允许写入）的通道对应的SECSEL位和GTSECR寄存器值将被更新。

例如，当GPT通道0的GTWP.CMNWP位设置为0（允许写入）时，写入GPT通道1的GTSECSR.SECSEL0位将导致GPT通道0的GTSECSR.SECSEL0位的值更新。同理，写入GPT321.GTSECR寄存器将更新GPT320.GTSECR寄存器的值。当GPT通道0的GTWP.CMNWP位设置为1（禁止写入）时，写入GPT通道1的GTSECSR.SECSEL0位不会导致GPT通道0的GTSECSR.SECSEL0位的值更新。同样，写入GPT321.GTSECR寄存器不会导致GPT320.GTSECR寄存器的值更新。

如果要保护GTSECSR和GTSECR寄存器中的所有位不被更新，请将所有通道的CMNWP位设置为1。

PRKEY[7:0]位（GTWP密钥代码）

该位控制是否可以覆盖WP、STRWP、STPWP、CLRWP和CMNWP位。

21.2.2 GTSTR:通用PWM定时器软件启动寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x04

Bit position:	31																												0
Bit field:	CSTRT31 to CSTRT0																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CSTRT0 to CSTRT31*1	通道nGTCNT计数开始（n：与位位置值相同） 0：GTCNT计数器不启动1： GTCNT计数器启动	R/W

注1.可使用的钻头因产品而异。CSTRTn的n与GPT通道号相同。对于本产品，n为0到9。

GTSTR启动每个通道n的GTCNT计数器操作，其中n=0到9。

The GTSTR bit number represents the channel number. The GTSTR register of each channel is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTR register.

The bit corresponding to channel which security attribution is configured as secure can be read by non-secure access but can not be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the CSTRT0 bit can not be written by non-secure access to GTSTR register in GPT channel 1, and the GTCNT counter operation status of GPT channel 0 is not changed. When the GTSTR register in GPT channel 1 is read by non-secure access in the same security configuratin as the previous example, the GTCNT counter operation status of GPT channel 0 (CSTRT0 bit) can be read.

For the association between GTSTR bit number and a channel number, see Figure 21.2.

CSTRTn bits (Channel n GTCNT Count Start (n = 0 to 9))

The CSTRTn bits start channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 9) has no effect unless the GTSSR.CSTRT bit is set to 1.

The read data shows the counter status of each channel (GTCR.CST bit). Zero means the counter is stopped and 1 means the counter is running.

21.2.3 GTSTP : General PWM Timer Software Stop Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x08

Bit position:	31																													0
Bit field:	CSTOP31 to CSTOP0																													
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	Channel n GTCNT Count Stop (n : the same as bit position value) 0: GTCNT counter not stop 1: GTCNT counter stop	R/W

Note 1. The bits that can be used vary depending on the product. The n of CSTOPn is the same as the GPT channel number. For this product, n is 0 to 9.

The GTSTP stops the GTCNT counter operation for each channel n, where n = 0 to 9.

The GTSTP bit number represents the channel number. The GTSTP register of each channel is shared by all the channels. The GTCNT counter stops for the channel associated with the GTSTP bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTP register.

The bit corresponding to channel which security attribution is configured as secure can be read by non-secure access but can not be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the CSTOP0 bit can not be written by non-secure access to GTSTP register in GPT channel 1, and the GTCNT counter operation status of GPT channel 0 is not changed. When the GTSTP register in GPT 1 is read by non-secure access in the same security configuratin as the previous example, the GTCNT counter operation status of GPT channel 0 (CSTOP0 bit) can be read.

For the association between GTSTP bit number and a channel number, see Figure 21.2.

CSTOPn bits (Channel n GTCNT Count Stop (n = 0 to 9))

The CSTOPn bits stop channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 9) has no effect unless the GTPSR.CSTOP bit is set to 1. The read data shows the counter status of each channel (invert of GTCR.CST bit). Zero means the counter is running and 1 means the counter is stopped.

GTSTR位号代表通道号。每个通道的GTSTR寄存器由所有通道共享。GTCNT计数器针对与写入1的GTSTR位号关联的通道启动。写0对GTCNT计数器的状态和GTSTR寄存器的值没有影响。

安全属性配置为安全的通道对应的位可以被非安全访问读取，但不能被非安全访问写入。例如，如果GPT通道0配置为安全，而其他GPT配置为非安全，则不能通过非安全访问GPT通道1中的GTSTR寄存器来写入CSTRT0位，以及GPT通道的GTCNT计数器操作状态0不变。当GPT通道1中的GTSTR寄存器通过与上例相同的安全配置中的非安全访问被读取时，可以读取GPT通道0的GTCNT计数器操作状态（CSTRT0位）。

GTSTR位号与通道号的关系见图21.2。

CSTRTn位（通道nGTCNT计数开始（n=0到9））

CSTRTn位启动GTCNT计数器操作的通道n。除非GTSSR.CSTRT位设置为1，否则写入GTSTR.CSTRTn位（n=0到9）无效。

读取的数据显示每个通道的计数器状态（GTCR.CST位）。零表示计数器停止，1表示计数器正在运行。

21.2.3 GTSTP:通用PWM定时器软件停止寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x08

Bit position:	31																													0
Bit field:	CSTOP31 to CSTOP0																													
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	CSTOP0 to CSTOP31*1	通道nGTCNT计数停止（n：与位位置值相同） 0：GTCNT计数器不停止1： GTCNT计数器停止	R/W

注1.可使用的钻头因产品而异。CSTOPn的n与GPT通道号相同。对于本产品，n为0到9。

GTSTP停止每个通道n的GTCNT计数器操作，其中n=0到9。

GTSTP位号代表通道号。每个通道的GTSTP寄存器由所有通道共享。
对于与写入1的GTSTP位号相关的通道，GTCNT计数器停止。写0对GTCNT计数器的状态和GTSTP寄存器的值没有影响。

安全属性配置为安全的通道对应的位可以被非安全访问读取，但不能被非安全访问写入。例如，如果GPT通道0配置为安全，其他GPT配置为非安全，则不能通过非安全访问GPT通道1中的GTSTP寄存器来写入CSTOP0位，以及GPT通道的GTCNT计数器操作状态0不变。当GPT1中的GTSTP寄存器通过与上例相同的安全配置中的非安全访问读取时，可以读取GPT通道0（CSTOP0位）的GTCNT计数器操作状态。

GTSTP位号与通道号的关系见图21.2。

CSTOPn位（通道nGTCNT计数停止（n=0到9））

CSTOPn位停止GTCNT计数器操作的通道n。除非GTPSR.CSTOP位设置为1，否则写入GTSTP.CSTOPn位（n=0至9）无效。读取的数据显示每个通道的计数器状态（反转GTCR.CST位）。零表示计数器正在运行，1表示计数器停止。

21.2.4 GTCLR : General PWM Timer Software Clear Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x0C

Bit position:	31																													0
Bit field:	CCLR31 to CCLR0																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	Channel n GTCNT Count Clear (n : the same as bit position value) 0: GTCNT counter is not cleared 1: GTCNT counter is cleared	W

Note 1. The bits that can be used vary depending on the product. The n of CCLRn is the same as the GPT channel number. For this product, n is 0 to 9.

The GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 9.

The GTCLR bit number represents the channel number. The GTCLR register of each channel is shared by all the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of GTCNT counter.

The bit corresponding to channel which security attribution is configured as secure can not be written by non-secure access. For example, if GPT channel 0 is configured as secure and other GPTs are configured as non-secure, the CCLR0 bit can not be written by non-secure access to GTCLR register in GPT channel 1, and the GTCNT counter of GPT channel 0 is not cleared.

For the association between GTCLR bit number and a channel number, see Figure 21.2.

CCLRn bits (Channel n GTCNT Count Clear (n = 0 to 9))

When the counting direction flag is set for decrementation (GTST.TUCF flag = 0) with saw-wave mode selected in the GTCR.MD[2:0] bits, the value of the GTCNT counter becomes that of the corresponding GTPR register in response to writing 1 to the CCLRn bit. The value of the counter becomes 0x0000 0000 with other settings. These bits are read as 0.

21.2.5 GTSSR : General PWM Timer Start Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGA input 1: Counter start enabled on the rising edge of GTETRGA input	R/W

21.2.4 GTCLR:通用PWM定时器软件清零寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x0C

Bit position:	31																													0
Bit field:	CCLR31 to CCLR0																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CCLR0 to CCLR31*1	ChannelnGTCNTCountClear（n：与位位置值相同） 0：GTCNT计数器不清零1：GTCNT计数器清零	W

注1.可使用的钻头因产品而异。CCLRn的n与GPT通道号相同。对于本产品，n为0到9。

GTCLR是一个只写寄存器，用于清除每个通道n的GTCNT计数器操作，其中n=0到9。

GTCLR位号代表通道号。每个通道的GTCLR寄存器由所有通道共享。与写入1的GTCLR位号关联的通道的GTCNT计数器清零。写0对GTCNT计数器的状态没有影响。

安全属性配置为安全的通道对应的位不能被非安全访问写入。例如，如果GPT通道0配置为安全，而其他GPT配置为非安全，则CCLR0位不能通过对GPT通道1中的GTCLR寄存器的非安全访问来写入，并且GPT通道0的GTCNT计数器为未清除。

GTCLR位号与通道号的关系见图21.2。

CCLRn位（通道nGTCNT计数清除（n=0至9））

当计数方向标志设置为递减（GTST.TUCF标志=0）并在GTCR.MD[2:0]位中选择锯齿波模式时，GTCNT计数器的值变为相应GTPR寄存器的值作为响应向CCLRn位写入1。使用其他设置，计数器的值变为0x00000000。这些位读为0。

21.2.5 GTSSR：通用PWM定时器启动源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSGTRGAR	GTETRGA引脚上升输入源计数器启动使能 0：在GTETRGA输入的上升沿禁止计数器启动1：在GTETRGA输入的上升沿使能计数器启动	R/W

Bit	Symbol	Function	R/W
1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGA input 1: Counter start enabled on the falling edge of GTETRGA input	R/W
2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGB input 1: Counter start enabled on the rising edge of GTETRGB input	R/W
3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGB input 1: Counter start enabled on the falling edge of GTETRGB input	R/W
4	SSGTRGCR	GTETRGC Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGC input 1: Counter start enabled on the rising edge of GTETRGC input	R/W
5	SSGTRGCF	GTETRGC Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGC input 1: Counter start enabled on the falling edge of GTETRGC input	R/W
6	SSGTRGDR	GTETRGD Pin Rising Input Source Counter Start Enable 0: Counter start disabled on the rising edge of GTETRGD input 1: Counter start enabled on the rising edge of GTETRGD input	R/W
7	SSGTRGDF	GTETRGD Pin Falling Input Source Counter Start Enable 0: Counter start disabled on the falling edge of GTETRGD input 1: Counter start enabled on the falling edge of GTETRGD input	R/W
8	SSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	SSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	SSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	SSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter start enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	SSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	SSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	SSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W

Bit	Symbol	Function	R/W
1	SSGTRGAF	GTETRGA引脚下降输入源计数器启动使能 0：在GTETRGA输入的下降沿禁用计数器启动1：在GTETRGA输入的下降沿启用计数器启动	R/W
2	SSGTRGBR	GTETRGB引脚上升输入源计数器启动使能 0：在GTETRGB输入的上升沿禁止计数器启动1：在GTETRGB输入的上升沿使能计数器启动	R/W
3	SSGTRGBF	GTETRGB引脚下降输入源计数器启动使能 0：在GTETRGB输入的下降沿禁用计数器启动1：在GTETRGB输入的下降沿启用计数器启动	R/W
4	SSGTRGCR	GTETRGC引脚上升沿输入源计数器启动使能 0：在GTETRGC输入的上升沿禁止计数器启动1：在GTETRGC输入的上升沿使能计数器启动	R/W
5	SSGTRGCF	GTETRGC引脚下降输入源计数器启动使能 0：在GTETRGC输入的下降沿禁止计数器启动1：在GTETRGC输入的下降沿使能计数器启动	R/W
6	SSGTRGDR	GTETRGD引脚上升沿输入源计数器启动使能 0：在GTETRGD输入的上升沿禁止计数器启动1：在GTETRGD输入的上升沿使能计数器启动	R/W
7	SSGTRGDF	GTETRGD引脚下降输入源计数器启动使能 0：在GTETRGD输入的下降沿禁止计数器启动1：在GTETRGD输入的下降沿使能计数器启动	R/W
8	SSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器启动使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器启动 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿启用计数器启动	R/W
9	SSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器启动使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器启动 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿启用计数器启动	R/W
10	SSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器启动使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器启动 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿启用计数器启动	R/W
11	SSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器启动使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器启动 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿启用计数器启动	R/W
12	SSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器启动使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器启动 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿启用计数器启动	R/W
13	SSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器启动使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器启动 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿启用计数器启动	R/W
14	SSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器启动使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器启动 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿启用计数器启动	R/W

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Bit	Symbol	Function	R/W
15	SSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable 0: Counter start disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter start enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	SSELCA	ELC_GPTA Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTA input 1: Counter start enabled at the ELC_GPTA input	R/W
17	SSELCB	ELC_GPTB Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTB input 1: Counter start enabled at the ELC_GPTB input	R/W
18	SSELCC	ELC_GPTC Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTC input 1: Counter start enabled at the ELC_GPTC input	R/W
19	SSELCD	ELC_GPTD Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTD input 1: Counter start enabled at the ELC_GPTD input	R/W
20	SSELCE	ELC_GPTE Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTE input 1: Counter start enabled at the ELC_GPTE input	R/W
21	SSELCF	ELC_GPTF Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTF input 1: Counter start enabled at the ELC_GPTF input	R/W
22	SSELCG	ELC_GPTG Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTG input 1: Counter start enabled at the ELC_GPTG input	R/W
23	SSELCH	ELC_GPTH Event Source Counter Start Enable 0: Counter start disabled at the ELC_GPTH input 1: Counter start enabled at the ELC_GPTH input	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTRT	Software Source Counter Start Enable 0: Counter start disabled by the GTSTR register 1: Counter start enabled by the GTSTR register	R/W

The GTSSR sets the source to start the GTCNT counter.

Input from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGB pin input.

SSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Start Enable)

The SSGTRGCR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGC pin input.

Bit	Symbol	Function	R/W
15	SSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器启动使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器启动 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用计数器启动	R/W
16	SSELCA	ELC_GPTA事件源计数器启动启用 0：在ELC_GPTA输入处禁用计数器启动1：在ELC_GPTA输入处启用计数器启动	R/W
17	SSELCB	ELC_GPTB事件源计数器启动启用 0：在ELC_GPTB输入处禁用计数器启动1：在ELC_GPTB输入处启用计数器启动	R/W
18	SSELCC	ELC_GPTC事件源计数器启动启用 0：在ELC_GPTC输入处禁用计数器启动1：在ELC_GPTC输入处启用计数器启动	R/W
19	SSELCD	ELC_GPTD事件源计数器启动启用 0：在ELC_GPTD输入处禁用计数器启动1：在ELC_GPTD输入处启用计数器启动	R/W
20	SSELCE	ELC_GPTE事件源计数器启动启用 0：在ELC_GPTE输入处禁用计数器启动1：在ELC_GPTE输入处启用计数器启动	R/W
21	SSELCF	ELC_GPTF事件源计数器启动启用 0：在ELC_GPTF输入处禁用计数器启动1：在ELC_GPTF输入处启用计数器启动	R/W
22	SSELCG	ELC_GPTG事件源计数器启动启用 0：在ELC_GPTG输入处禁用计数器启动1：在ELC_GPTG输入处启用计数器启动	R/W
23	SSELCH	ELC_GPTH事件源计数器启动启用 0：在ELC_GPTH输入处禁用计数器启动1：在ELC_GPTH输入处启用计数器启动	R/W
30:24	—	这些位被读取为0。写入值应为0。	R/W
31	CSTRT	软件源计数器启动使能 0：由GTSTR寄存器禁止计数器启动1：由GTSTR寄存器使能计数器启动	R/W

GTSSR设置启动GTCNT计数器的源。

GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性POEG.

SSGTRGAR位（GTETRGA引脚上升沿输入源计数器启动使能）

SSGTRGAR位启用或禁用GTCNT计数器在GTETRGA引脚输入的上升沿启动。

SSGTRGAF位（GTETRGA引脚下降输入源计数器启动使能）

SSGTRGAF位启用或禁用GTCNT计数器在GTETRGA引脚输入的下降沿启动。

SSGTRGBR位（GTETRGB引脚上升沿输入源计数器启动使能）

SSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSGTRGBF位（GTETRGB引脚下降输入源计数器启动使能）

SSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器启动。

SSGTRGCR位（GTETRGC引脚上升沿输入源计数器启动使能）

SSGTRGCR位启用或禁用GTCNT计数器在GTETRGC引脚输入的上升沿启动。

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SSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Start Enable)

The SSGTRGCF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGC pin input.

SSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Start Enable)

The SSGTRGDR bit enables or disables the GTCNT counter start on the rising edge of the GTETRGD pin input.

SSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Start Enable)

The SSGTRGDF bit enables or disables the GTCNT counter start on the falling edge of the GTETRGD pin input.

SSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

SSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

SSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

SSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

SSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

SSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables the GTCNT counter start on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

SSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

SSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables the GTCNT counter start on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables the GTCNT counter start at the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables the GTCNT counter start by GTSTR register.

21.2.6 GTPSR : General PWM Timer Stop Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA

SSGTRGCF位（GTETRGC引脚下降输入源计数器启动使能）

SSGTRGCF位启用或禁用GTCNT计数器在GTETRGC引脚输入的下降沿启动。

SSGTRGDR位（GTETRGD引脚上升沿输入源计数器启动使能）

SSGTRGDR位启用或禁用GTCNT计数器在GTETRGD引脚输入的上升沿启动。

SSGTRGDF位（GTETRGD引脚下降输入源计数器启动使能）

SSGTRGDF位启用或禁用GTCNT计数器在GTETRGD引脚输入的下降沿启动。

SSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器启动使能）

SSCARBL位启用或禁用GTCNT计数器在GTIOCnA引脚输入的上升沿启动，当GTIOCnB输入为0。

SSCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器启动使能）

SSCARBH位启用或禁用GTCNT计数器在GTIOCnA引脚输入的上升沿启动，当GTIOCnB输入为1。

SSCAFBL位（在GTIOCnB值低电平源计数器启动使能期间GTIOCnA引脚下降输入）

SSCAFBL位启用或禁用GTCNT计数器在GTIOCnA引脚输入的下降沿启动，当GTIOCnB输入为0。

SSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器启动使能）

SSCAFBH位启用或禁用GTCNT计数器在GTIOCnA引脚输入的下降沿启动，当GTIOCnB输入为1。

SSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器启动使能）

SSCBRAL位启用或禁用GTCNT计数器在GTIOCnB引脚输入的上升沿启动，当GTIOCnA输入为0。

SSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器启动使能）

SSCBRAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的上升沿启动，当GTIOCnA输入为1。

SSCBFAL位（GTIOCnA值低电平源计数器启动使能期间GTIOCnB引脚下降输入）

SSCBFAL位使能或禁止GTCNT计数器在GTIOCnB引脚输入的下降沿启动，当GTIOCnA输入为0。

SSCBFAH位（GTIOCnA值高电平源计数器启动使能期间的GTIOCnB引脚下降输入）

SSCBFAH位启用或禁用GTCNT计数器在GTIOCnB引脚输入的下降沿启动，当GTIOCnA输入为1。

SSELCm位（ELC_GPTm事件源计数器启动启用）（m=A到H）

SSELCm位启用或禁用在ELC_GPTm事件输入时启动的GTCNT计数器。

CSTRT位（软件源计数器启动使能）

CSTRT位启用或禁用由GTSTR寄存器启动的GTCNT计数器。

21.2.6 GTPSR：通用PWM定时器停止源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA

Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCB FAH	PSCB FAL	PSCB RAH	PSCB RAL	PSCA FBH	PSCA FBL	PSCA RBH	PSCA RBL	PSGT RGDF	PSGT RGDR	PSGT RGCF	PSGT RGCR	PSGT RGBF	PSGT RGBR	PSGT RGAF	PSGT RGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGA input 1: Counter stop enabled on the rising edge of GTETRGA input	R/W
1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGA input 1: Counter stop enabled on the falling edge of GTETRGA input	R/W
2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGB input 1: Counter stop enabled on the rising edge of GTETRGB input	R/W
3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGB input 1: Counter stop enabled on the falling edge of GTETRGB input	R/W
4	PSGTRGCR	GTETRGC Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGC input 1: Counter stop enabled on the rising edge of GTETRGC input	R/W
5	PSGTRGCF	GTETRGC Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGC input 1: Counter stop enabled on the falling edge of GTETRGC input	R/W
6	PSGTRGDR	GTETRGD Pin Rising Input Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTETRGD input 1: Counter stop enabled on the rising edge of GTETRGD input	R/W
7	PSGTRGDF	GTETRGD Pin Falling Input Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTETRGD input 1: Counter stop enabled on the falling edge of GTETRGD input	R/W
8	PSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	PSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	PSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	PSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter stop enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	PSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W

重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSCB FAH	PSCB FAL	PSCB RAH	PSCB RAL	PSCA FBH	PSCA FBL	PSCA RBH	PSCA RBL	PSGT RGDF	PSGT RGDR	PSGT RGCF	PSGT RGCR	PSGT RGBF	PSGT RGBR	PSGT RGAF	PSGT RGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PSGTRGAR	GTETRGA引脚上升输入源计数器停止使能 0：在GTETRGA输入的上升沿禁止计数器停止1：在GTETRGA输入的上升沿使能计数器停止	R/W
1	PSGTRGAF	GTETRGA引脚下降输入源计数器停止使能 0：在GTETRGA输入的下降沿禁止计数器停止1：在GTETRGA输入的下降沿使能计数器停止	R/W
2	PSGTRGBR	GTETRGB引脚上升输入源计数器停止使能 0：在GTETRGB输入的上升沿禁止计数器停止1：在GTETRGB输入的上升沿使能计数器停止	R/W
3	PSGTRGBF	GTETRGB引脚下降输入源计数器停止使能 0：在GTETRGB输入的下降沿禁用计数器停止1：在GTETRGB输入的下降沿启用计数器停止	R/W
4	PSGTRGCR	GTETRGC引脚上升输入源计数器停止使能 0：在GTETRGC输入的上升沿禁止计数器停止1：在GTETRGC输入的上升沿使能计数器停止	R/W
5	PSGTRGCF	GTETRGC引脚下降输入源计数器停止使能 0：在GTETRGC输入的下降沿禁止计数器停止1：在GTETRGC输入的下降沿使能计数器停止	R/W
6	PSGTRGDR	GTETRGD引脚上升输入源计数器停止使能 0：在GTETRGD输入的上升沿禁止计数器停止1：在GTETRGD输入的上升沿使能计数器停止	R/W
7	PSGTRGDF	GTETRGD引脚下降输入源计数器停止使能 0：在GTETRGD输入的下降沿禁止计数器停止1：在GTETRGD输入的下降沿使能计数器停止	R/W
8	PSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器停止使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器停止 1：当GTIOCnB输入为0时，在GTIOCnA输入上升沿使能计数器停止	R/W
9	PSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器停止使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器停止 1：当GTIOCnB输入为1时，在GTIOCnA输入上升沿使能计数器停止	R/W
10	PSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器停止使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器停止 1：当GTIOCnB输入为0时，在GTIOCnA输入下降沿使能计数器停止	R/W
11	PSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器停止使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器停止 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器停止	R/W
12	PSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器停止使能 0：当GTIOCnA输入为0时，在GTIOCnB输入上升沿禁止计数器停止 1：当GTIOCnA输入为0时，在GTIOCnB输入上升沿使能计数器停止	R/W

Bit	Symbol	Function	R/W
13	PSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	PSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	PSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable 0: Counter stop disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter stop enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	PSELCA	ELC_GPTA Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTA input 1: Counter stop enabled at the ELC_GPTA input	R/W
17	PSELCB	ELC_GPTB Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTB input 1: Counter stop enabled at the ELC_GPTB input	R/W
18	PSELCC	ELC_GPTC Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTC input 1: Counter stop enabled at the ELC_GPTC input	R/W
19	PSELCD	ELC_GPTD Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTD input 1: Counter stop enabled at the ELC_GPTD input	R/W
20	PSELCE	ELC_GPTE Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTE input 1: Counter stop enabled at the ELC_GPTE input	R/W
21	PSELCF	ELC_GPTF Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTF input 1: Counter stop enabled at the ELC_GPTF input	R/W
22	PSELCG	ELC_GPTG Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTG input 1: Counter stop enabled at the ELC_GPTG input	R/W
23	PSELCH	ELC_GPTH Event Source Counter Stop Enable 0: Counter stop disabled at the ELC_GPTH input 1: Counter stop enabled at the ELC_GPTH input	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CSTOP	Software Source Counter Stop Enable 0: Counter stop disabled by the GTSTP register 1: Counter stop enabled by the GTSTP register	R/W

The GTPSR sets the source to stop the GTCNT counter.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGA pin input.

Bit	Symbol	Function	R/W
13	PSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器停止使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器停止 1：当GTIOCnA输入为1时，在GTIOCnB输入上升沿使能计数器停止	R/W
14	PSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器停止使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器停止 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器停止	R/W
15	PSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器停止使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器停止 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿使能计数器停止	R/W
16	PSELCA	ELC_GPTA事件源计数器停止启用 0：在ELC_GPTA输入处禁用计数器停止1：在ELC_GPTA输入处启用计数器停止	R/W
17	PSELCB	ELC_GPTB事件源计数器停止启用 0：在ELC_GPTB输入处禁用计数器停止1：在ELC_GPTB输入处启用计数器停止	R/W
18	PSELCC	ELC_GPTC事件源计数器停止使能 0：在ELC_GPTC输入处禁用计数器停止1：在ELC_GPTC输入处启用计数器停止	R/W
19	PSELCD	ELC_GPTD事件源计数器停止启用 0：在ELC_GPTD输入处禁用计数器停止1：在ELC_GPTD输入处启用计数器停止	R/W
20	PSELCE	ELC_GPTE事件源计数器停止启用 0：在ELC_GPTE输入处禁用计数器停止1：在ELC_GPTE输入处启用计数器停止	R/W
21	PSELCF	ELC_GPTF事件源计数器停止启用 0：在ELC_GPTF输入处禁用计数器停止1：在ELC_GPTF输入处启用计数器停止	R/W
22	PSELCG	ELC_GPTG事件源计数器停止使能 0：在ELC_GPTG输入处禁用计数器停止1：在ELC_GPTG输入处启用计数器停止	R/W
23	PSELCH	ELC_GPTH事件源计数器停止启用 0：在ELC_GPTH输入处禁用计数器停止1：在ELC_GPTH输入处启用计数器停止	R/W
30:24	—	这些位被读取为0。写入值应为0。	R/W
31	CSTOP	软件源计数器停止使能 0：GTSTP寄存器禁止计数器停止1：GTSTP寄存器使能计数器停止	R/W

GTPSR设置源以停止GTCNT计数器。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性POEG.

PSGTRGAR位（GTETRGA引脚上升沿输入源计数器停止使能）

PSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGAF位（GTETRGA引脚下降输入源计数器停止使能）

PSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器停止。

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PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

PSGTRGBR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Stop Enable)

PSGTRGCR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGC pin input.

PSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Stop Enable)

The PSGTRGCF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGC pin input.

PSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Stop Enable)

PSGTRGDR bit enables or disables the GTCNT counter stop on the rising edge of the GTETRGD pin input.

PSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Stop Enable)

The PSGTRGDF bit enables or disables the GTCNT counter stop on the falling edge of the GTETRGD pin input.

PSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

PSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Stop Enable)

This bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

PSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

PSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

PSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

PSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables the GTCNT counter stop on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

PSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

PSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables the GTCNT counter stop on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

PSELCm bit (ELCm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables the GTCNT counter stop at the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables the GTCNT counter stop by the GTSTP register.

PSGTRGBR位（GTETRGB引脚上升沿输入源计数器停止使能）

PSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGBF位（GTETRGB引脚下降输入源计数器停止使能）

PSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGCR位（GTETRGC引脚上升沿输入源计数器停止使能）

PSGTRGCR位使能或禁止GTCNT计数器在GTETRGC引脚输入的上升沿停止。

PSGTRGCF位（GTETRGC引脚下降输入源计数器停止使能）

PSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGDR位（GTETRGD引脚上升沿输入源计数器停止使能）

PSGTRGDR位启用或禁用GTCNT计数器在GTETRGD引脚输入的上升沿停止。

PSGTRGDF位（GTETRGD引脚下降输入源计数器停止使能）

PSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器停止使能）

PSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为0。

PSCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器停止使能）

当GTIOCnB输入为1时，该位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSCAFBL位（GTIOCnB值低电平源计数器停止使能期间GTIOCnA引脚下降输入）

PSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为0。

PSCAFBH位（GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器停止使能）

PSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnB输入为1。

PSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器停止使能）

PSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCnA输入为0。

PSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器停止使能）

PSCBRAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的上升沿停止，当GTIOCnA输入为1。

PSCBFAL位（GTIOCnA值低源计数器停止使能期间GTIOCnB引脚下降输入）

PSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCnA输入为0。

PSCBFAH位（GTIOCnA值高电平源计数器停止使能期间的GTIOCnB引脚下降输入）

PSCBFAH位使能或禁止GTCNT计数器在GTIOCnB引脚输入的下降沿停止，当GTIOCnA输入为1。

PSELCm位（ELCm事件源计数器停止使能）（m=A到H）

PSELCm位启用或禁用GTCNT计数器在ELC_GPTm事件输入处停止。

CSTOP位（软件源计数器停止使能）

CSTOP位通过GTSTP寄存器启用或禁用GTCNT计数器停止。

21.2.7 GTCSR : General PWM Timer Clear Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTETRGA input 1: Counter clear enabled on the rising edge of GTETRGA input	R/W
1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGA input 1: Counter clear enabled on the falling edge of GTETRGA input	R/W
2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input	R/W
3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGB input 1: Counter clear enabled on the falling edge of GTETRGB input	R/W
4	CSGTRGCR	GTETRGC Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGC input 1: Enable counter clear on the rising edge of GTETRGC input	R/W
5	CSGTRGCF	GTETRGC Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGC input 1: Counter clear enabled on the falling edge of GTETRGC input	R/W
6	CSGTRGDR	GTETRGD Pin Rising Input Source Counter Clear Enable 0: Disable counter clear on the rising edge of GTETRGD input 1: Enable counter clear on the rising edge of GTETRGD input	R/W
7	CSGTRGDF	GTETRGD Pin Falling Input Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTETRGD input 1: Counter clear enabled on the falling edge of GTETRGD input	R/W
8	CSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	CSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	CSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W

21.2.7 GTCSR：通用PWM定时器清零源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CSGTRGAR	GTETRGA引脚上升输入源计数器清零使能 0：在GTETRGA输入的上升沿禁止计数器清除1：在GTETRGA输入的上升沿使能计数器清除	R/W
1	CSGTRGAF	GTETRGA引脚下降输入源计数器清零使能 0：在GTETRGA输入的下降沿禁止计数器清除1：在GTETRGA输入的下降沿使能计数器清除	R/W
2	CSGTRGBR	GTETRGB引脚上升输入源计数器清零使能 0：在GTETRGB输入的上升沿禁止计数器清零1：在GTETRGB输入的上升沿使能计数器清零	R/W
3	CSGTRGBF	GTETRGB引脚下降输入源计数器清除启用 0：在GTETRGB输入的下降沿禁用计数器清除1：在GTETRGB输入的下降沿启用计数器清除	R/W
4	CSGTRGCR	GTETRGC引脚上升沿输入源计数器清零使能 0：在GTETRGC输入的上升沿禁止计数器清零1：在GTETRGC输入的上升沿使能计数器清零	R/W
5	CSGTRGCF	GTETRGC引脚下降输入源计数器清零使能 0：在GTETRGC输入的下降沿禁止计数器清除1：在GTETRGC输入的下降沿使能计数器清除	R/W
6	CSGTRGDR	GTETRGD引脚上升沿输入源计数器清零使能 0：在GTETRGD输入的上升沿禁止计数器清零1：在GTETRGD输入的上升沿使能计数器清零	R/W
7	CSGTRGDF	GTETRGD引脚下降输入源计数器清零使能 0：在GTETRGD输入的下降沿禁止计数器清除1：在GTETRGD输入的下降沿使能计数器清除	R/W
8	CSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器清零使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器清零 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能计数器清零	R/W
9	CSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器清零使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器清零 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能计数器清零	R/W
10	CSCAFBL	GTIOCnB值低电平源计数器清除启用期间的GTIOCnA引脚下降输入 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器清零 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能计数器清零	R/W

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Bit	Symbol	Function	R/W
11	CSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter clear enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	CSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	CSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	CSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	CSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable 0: Counter clear disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter clear enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	CSELCA	ELC_GPTA Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTA input 1: Counter clear enabled at the ELC_GPTA input	R/W
17	CSELCB	ELC_GPTB Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTB input 1: Counter clear enabled at the ELC_GPTB input	R/W
18	CSELCC	ELC_GPTC Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTC input 1: Counter clear enabled at the ELC_GPTC input	R/W
19	CSELCD	ELC_GPTD Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTD input 1: Counter clear enabled at the ELC_GPTD input	R/W
20	CSELCE	ELC_GPTE Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTE input 1: Counter clear enabled at the ELC_GPTE input	R/W
21	CSELCF	ELC_GPTF Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTF input 1: Counter clear enabled at the ELC_GPTF input	R/W
22	CSELCG	ELC_GPTG Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTG input 1: Counter clear enabled at the ELC_GPTG input	R/W
23	CSELCH	ELC_GPTH Event Source Counter Clear Enable 0: Counter clear disabled at the ELC_GPTH input 1: Counter clear enabled at the ELC_GPTH input	R/W
30:24	—	These bits are read as 0. The write value should be 0.	R/W
31	CCLR	Software Source Counter Clear Enable 0: Counter clear disabled by the GTCLR register 1: Counter clear enabled by the GTCLR register	R/W

The GTCSR sets the source to clear the GTCNT counter.

Counter clearing can be executed whether the counter is running (GTCR.CST=1) or stopped (GTCR.CST=0).

Bit	Symbol	Function	R/W
11	CSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器清零使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器清零 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器清零	R/W
12	CSCBRAL	GTIOCnB引脚在GTIOCnA值低电平期间的上升沿输入源计数器清零使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器清零 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能计数器清零	R/W
13	CSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器清零使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器清零 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能计数器清零	R/W
14	CSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器清零使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器清零 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器清零	R/W
15	CSCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器清零使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器清零 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿启用计数器清零	R/W
16	CSELCA	ELC_GPTA事件源计数器清除启用 0：在ELC_GPTA输入处禁用计数器清除1：在ELC_GPTA输入处启用计数器清除	R/W
17	CSELCB	ELC_GPTB事件源计数器清除启用 0：在ELC_GPTB输入处禁用计数器清除1：在ELC_GPTB输入处启用计数器清除	R/W
18	CSELCC	ELC_GPTC事件源计数器清除启用 0：在ELC_GPTC输入处禁用计数器清除1：在ELC_GPTC输入处启用计数器清除	R/W
19	CSELCD	ELC_GPTD事件源计数器清除启用 0：在ELC_GPTD输入处禁用计数器清除1：在ELC_GPTD输入处启用计数器清除	R/W
20	CSELCE	ELC_GPTE事件源计数器清除启用 0：在ELC_GPTE输入处禁用计数器清除1：在ELC_GPTE输入处启用计数器清除	R/W
21	CSELCF	ELC_GPTF事件源计数器清除启用 0：在ELC_GPTF输入处禁用计数器清除1：在ELC_GPTF输入处启用计数器清除	R/W
22	CSELCG	ELC_GPTG事件源计数器清除启用 0：在ELC_GPTG输入处禁用计数器清除1：在ELC_GPTG输入处启用计数器清除	R/W
23	CSELCH	ELC_GPTH事件源计数器清除启用 0：在ELC_GPTH输入处禁用计数器清除1：在ELC_GPTH输入处启用计数器清除	R/W
30:24	—	这些位被读取为0。写入值应为0。	R/W
31	CCLR	软件源计数器清除启用 0：GTCLR寄存器禁止计数器清零1：GTCLR寄存器使能计数器清零	R/W

GTCSR设置源以清除GTCNT计数器。

无论计数器正在运行(GTCR.CST=1)还是停止(GTCR.CST=0)，都可以执行计数器清除。

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Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Clear Enable)

The CSGTRGCR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGC pin input.

CSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Clear Enable)

The CSGTRGCF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGC pin input.

CSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Clear Enable)

The CSGTRGDR bit enables or disables the GTCNT counter clear on the rising edge of the GTETRGD pin input.

CSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Clear Enable)

The CSGTRGDF bit enables or disables the GTCNT counter clear on the falling edge of the GTETRGD pin input.

CSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

CSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

CSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

CSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

CSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

CSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables the GTCNT counter clear on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

CSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

CSGTRGAR位（GTETRGA引脚上升沿输入源计数器清零使能）

CSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGAF位（GTETRGA引脚下降输入源计数器清零使能）

CSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGBR位（GTETRGB引脚上升沿输入源计数器清零使能）

CSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGBF位（GTETRGB引脚下降输入源计数器清零使能）

CSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGCR位（GTETRGC引脚上升沿输入源计数器清零使能）

CSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGCF位（GTETRGC引脚下降输入源计数器清零使能）

CSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGDR位（GTETRGD引脚上升沿输入源计数器清零使能）

CSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGDF位（GTETRGD引脚下降输入源计数器清零使能）

CSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器清零使能）

CSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器清零，当
GTIOCnB输入为0。

CSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚上升沿输入源计数器清零使能）

CSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器清零，当
GTIOCnB输入为1。

CSCAFBL位（GTIOCnB值低电平源计数器清除使能期间GTIOCnA引脚下降输入）

CSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器清零，当
GTIOCnB输入为0。

CSCAFBH位（GTIOCnB值高电平源计数器清零使能期间GTIOCnA引脚下降输入）

CSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器清零，当
GTIOCnB输入为1。

CSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器清零使能）

CSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器清零，当
GTIOCnA输入为0。

CSCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器清零使能）

CSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器清零，当
GTIOCnA输入为1。

CSCBFAL位（GTIOCnA值低电平源计数器清零使能期间GTIOCnB引脚下降输入）

CSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器清零，当
GTIOCnA输入为0。

CSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables the GTCNT counter clear on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

CSELCm bit (ELCm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables the GTCNT counter clear at the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables the GTCNT counter clear by the GTCLR register.

21.2.8 GTUPSR : General PWM Timer Up Count Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGA input 1: Counter count up enabled on the rising edge of GTETRGA input	R/W
1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGA input 1: Counter count up enabled on the falling edge of GTETRGA input	R/W
2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGB input 1: Counter count up enabled on the rising edge of GTETRGB input	R/W
3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGB input 1: Counter count up enabled on the falling edge of GTETRGB input	R/W
4	USGTRGCR	GTETRGC Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGC input 1: Counter count up enabled on the rising edge of GTETRGC input	R/W
5	USGTRGCF	GTETRGC Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGC input 1: Counter count up enabled on the falling edge of GTETRGC input	R/W
6	USGTRGDR	GTETRGD Pin Rising Input Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTETRGD input 1: Counter count up enabled on the rising edge of GTETRGD input	R/W
7	USGTRGDF	GTETRGD Pin Falling Input Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTETRGD input 1: Counter count up enabled on the falling edge of GTETRGD input	R/W
8	USCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W

CSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器清零使能）

CSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCnA输入为1。

CSELCm位（ELCm事件源计数器清除启用）（m=A到H）

CSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器清零。

CCLR位（软件源计数器清除启用）

CCLR位启用或禁用由GTCLR寄存器清除的GTCNT计数器。

21.2.8 GTUPSR：通用PWM定时器向上计数源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USGTRGAR	GTETRGA引脚上升输入源计数器向上计数使能 0：在GTETRGA输入的上升沿禁止向上计数1：在GTETRGA输入的上升沿使能向上计数	R/W
1	USGTRGAF	GTETRGA引脚下降输入源计数器向上计数使能 0：在GTETRGA输入的下降沿禁止向上计数1：在GTETRGA输入的下降沿使能向上计数	R/W
2	USGTRGBR	GTETRGB引脚上升输入源计数器向上计数使能 0：在GTETRGB输入的上升沿禁止向上计数1：在GTETRGB输入的上升沿使能向上计数	R/W
3	USGTRGBF	GTETRGB引脚下降输入源计数器向上计数使能 0：在GTETRGB输入的下降沿禁止向上计数1：在GTETRGB输入的下降沿使能向上计数	R/W
4	USGTRGCR	GTETRGC引脚上升沿输入源计数器向上计数使能 0：在GTETRGC输入的上升沿禁止向上计数1：在GTETRGC输入的上升沿使能向上计数	R/W
5	USGTRGCF	GTETRGC引脚下降输入源计数器向上计数使能 0：在GTETRGC输入的下降沿禁止向上计数1：在GTETRGC输入的下降沿使能向上计数	R/W
6	USGTRGDR	GTETRGD引脚上升输入源计数器向上计数使能 0：在GTETRGD输入的上升沿禁止计数器向上计数1：在GTETRGD输入的上升沿使能计数器向上计数	R/W
7	USGTRGDF	GTETRGD引脚下降输入源计数器向上计数使能 0：在GTETRGD输入的下降沿禁止向上计数1：在GTETRGD输入的下降沿使能向上计数	R/W
8	USCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器向上计数 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能计数器向上计数	R/W

Bit	Symbol	Function	R/W
9	USCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	USCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	USCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count up enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	USCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	USCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	USCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	USCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable 0: Counter count up disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count up enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	USELCA	ELC_GPTA Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTA input 1: Counter count up enabled at the ELC_GPTA input	R/W
17	USELCB	ELC_GPTB Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTB input 1: Counter count up enabled at the ELC_GPTB input	R/W
18	USELCC	ELC_GPTC Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTC input 1: Counter count up enabled at the ELC_GPTC input	R/W
19	USELCD	ELC_GPTD Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTD input 1: Counter count up enabled at the ELC_GPTD input	R/W
20	USELCE	ELC_GPTE Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTE input 1: Counter count up enabled at the ELC_GPTE input	R/W
21	USELCF	ELC_GPTF Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTF input 1: Counter count up enabled at the ELC_GPTF input	R/W
22	USELCG	ELC_GPTG Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTG input 1: Counter count up enabled at the ELC_GPTG input	R/W

Bit	Symbol	Function	R/W
9	USCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器向上计数 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能计数器向上计数	R/W
10	USCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源计数器向上计数使能 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器向上计数 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能计数器向上计数	R/W
11	USCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器向上计数使能 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器向上计数 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能计数器向上计数	R/W
12	USCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向上计数使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器向上计数 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能计数器向上计数	R/W
13	USCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器向上计数使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器向上计数 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能计数器向上计数	R/W
14	USCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源计数器向上计数使能 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器向上计数 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器向上计数	R/W
15	USCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器向上计数使能 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器向上计数 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿使能计数器向上计数	R/W
16	USELCA	ELC_GPTA事件源计数器向上计数启用 0：在ELC_GPTA输入处禁用计数器向上计数1：在ELC_GPTA输入处启用计数器向上计数	R/W
17	USELCB	ELC_GPTB事件源计数器向上计数使能 0：在ELC_GPTB输入处禁用计数器向上计数1：在ELC_GPTB输入处启用计数器向上计数	R/W
18	USELCC	ELC_GPTC事件源计数器向上计数使能 0：在ELC_GPTC输入处禁用计数器向上计数1：在ELC_GPTC输入处启用计数器向上计数	R/W
19	USELCD	ELC_GPTD事件源计数器向上计数启用 0：在ELC_GPTD输入处禁用计数器向上计数1：在ELC_GPTD输入处启用计数器向上计数	R/W
20	USELCE	ELC_GPTE事件源计数器向上计数启用 0：在ELC_GPTE输入处禁用计数器向上计数1：在ELC_GPTE输入处启用计数器向上计数	R/W
21	USELCF	ELC_GPTF事件源计数器向上计数启用 0：在ELC_GPTF输入处禁用计数器向上计数1：在ELC_GPTF输入处启用计数器向上计数	R/W
22	USELCG	ELC_GPTG事件源计数器向上计数使能 0：在ELC_GPTG输入处禁用计数器向上计数1：在ELC_GPTG输入处启用计数器向上计数	R/W

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Bit	Symbol	Function	R/W
23	USELCH	ELC_GPTH Event Source Counter Count Up Enable 0: Counter count up disabled at the ELC_GPTH input 1: Counter count up enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

Number of increment in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGB pin input.

USGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Up Enable)

The USGTRGCR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGC pin input.

USGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Up Enable)

The USGTRGCF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGC pin input.

USGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Up Enable)

The USGTRGDR bit enables or disables the GTCNT counter count up on the rising edge of the GTETRGD pin input.

USGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Up Enable)

The USGTRGDF bit enables or disables the GTCNT counter count up on the falling edge of the GTETRGD pin input.

USCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of GTIOCnA pin input, when GTIOCnB input is 0.

USCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

USCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

USCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

Bit	Symbol	Function	R/W
23	USELCH	ELC_GPTH事件源计数器向上计数启用 0：在ELC_GPTH输入处禁用计数器向上计数1：在ELC_GPTH输入处启用计数器向上计数	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

GTUPSR将源设置为对GTCNT计数器进行计数。

当GTUPSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行计数。在这种情况下，GTCR.TPCS无效。

即使同时生成多个源，计数中的增量数也是1。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

USGTRGAR位（GTETRGA引脚上升沿输入源计数器向上计数使能）

USGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGAF位（GTETRGA引脚下降输入源计数器向上计数使能）

USGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGBR位（GTETRGB引脚上升沿输入源计数器向上计数使能）

USGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGBF位（GTETRGB引脚下降输入源计数器向上计数使能）

USGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGCR位（GTETRGC引脚上升沿输入源计数器向上计数使能）

USGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGCF位（GTETRGC引脚下降输入源计数器向上计数使能）

USGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGDR位（GTETRGD引脚上升沿输入源计数器向上计数使能）

USGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGDF位（GTETRGD引脚下降输入源计数器向上计数使能）

USGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能）

USCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为0。

USCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向上计数使能）

USCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为1。

USCAFBL位（GTIOCnB值低电平源计数器向上计数启用期间的GTIOCnA引脚下降输入）

USCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为0。

USCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器向上计数使能）

USCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCnB输入为1。

USCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

USCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables the GTCNT counter count up on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

USCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables the GTCNT counter count up on the falling edge of the GTIOCnB pin input, when the GTIOCnA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables the GTCNT counter count up at the ELC_GPTm event input.

21.2.9 GTDNSR : General PWM Timer Down Count Source Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGA input 1: Counter count down enabled on the rising edge of GTETRGA input	R/W
1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGA input 1: Counter count down enabled on the falling edge of GTETRGA input	R/W
2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGB input 1: Counter count down enabled on the rising edge of GTETRGB input	R/W
3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGB input 1: Counter count down enabled on the falling edge of GTETRGB input	R/W
4	DSGTRGCR	GTETRGC Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGC input 1: Counter count down enabled on the rising edge of GTETRGC input	R/W
5	DSGTRGCF	GTETRGC Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGC input 1: Counter count down enabled on the falling edge of GTETRGC input	R/W

USCBRAL位（GTIOCnA值低电平源计数器向上计数启用期间的GTIOCnB引脚上升沿输入）

USCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCnA输入为0。

USCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器向上计数使能）

当GTIOCnA输入为1时，USCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USCBFAL位（GTIOCnA值低电平源计数器向上计数启用期间的GTIOCnB引脚下降输入）

当GTIOCnA输入为0时，USCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCBFAH位（GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器向上计数使能）

当GTIOCnA输入为1时，USCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USELCm位（ELC_GPTm事件源计数器向上计数启用）（m=A到H）

USELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器向上计数。

21.2.9 GTDNSR：通用PWM定时器递减计数源选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DSGTRGAR	GTETRGA引脚上升输入源计数器倒计时使能 0：在GTETRGA输入的上升沿禁用计数器递减计数1：在GTETRGA输入的上升沿启用计数器递减计数	R/W
1	DSGTRGAF	GTETRGA引脚下降输入源计数器倒计时使能 0：在GTETRGA输入的下降沿禁用计数器递减计数1：在GTETRGA输入的下降沿启用计数器递减计数	R/W
2	DSGTRGBR	GTETRGB引脚上升输入源计数器倒计时使能 0：在GTETRGB输入的上升沿禁用计数器递减计数1：在GTETRGB输入的上升沿启用计数器递减计数	R/W
3	DSGTRGBF	GTETRGB引脚下降输入源计数器倒计时使能 0：在GTETRGB输入的下降沿禁用计数器递减计数1：在GTETRGB输入的下降沿启用计数器递减计数	R/W
4	DSGTRGCR	GTETRGC引脚上升输入源计数器倒计时使能 0：在GTETRGC输入的上升沿禁用计数器递减计数1：在GTETRGC输入的上升沿启用计数器递减计数	R/W
5	DSGTRGCF	GTETRGC引脚下降输入源计数器倒计时使能 0：在GTETRGC输入的下降沿禁用计数器减计数1：在GTETRGC输入的下降沿启用计数器减计数	R/W

Bit	Symbol	Function	R/W
6	DSGTRGDR	GTETRGD Pin Rising Input Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTETRGD input 1: Counter count down enabled on the rising edge of GTETRGD input	R/W
7	DSGTRGDF	GTETRGD Pin Falling Input Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTETRGD input 1: Counter count down enabled on the falling edge of GTETRGD input	R/W
8	DSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	DSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	DSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	DSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: Counter count down enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	DSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	DSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	DSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	DSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable 0: Counter count down disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: Counter count down enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTA input 1: Counter count down enabled at the ELC_GPTA input	R/W
17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTB input 1: Counter count down enabled at the ELC_GPTB input	R/W

Bit	Symbol	Function	R/W
6	DSGTRGDR	GTETRGD引脚上升输入源计数器倒计时使能 0：在GTETRGD输入的上升沿禁用计数器递减计数1：在GTETRGD输入的上升沿启用计数器递减计数	R/W
7	DSGTRGDF	GTETRGD引脚下降输入源计数器倒计时使能 0：在GTETRGD输入的下降沿禁用计数器递减计数1：在GTETRGD输入的下降沿启用计数器递减计数	R/W
8	DSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止计数器递减计数 1：当GTIOCnB输入为0时，在GTIOCnA输入上升沿使能计数器递减计数	R/W
9	DSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止计数器递减计数 1：当GTIOCnB输入为1时，在GTIOCnA输入上升沿使能计数器递减计数	R/W
10	DSCAFBL	GTIOCnB值低源计数器倒计时期间的GTIOCnA引脚下降输入Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止计数器递减计数 1：当GTIOCnB输入为0时，在GTIOCnA输入下降沿使能计数器递减计数	R/W
11	DSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源计数器倒计时Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止计数器递减计数 1：当GTIOCnB输入为1时，在GTIOCnA输入下降沿使能计数器递减计数	R/W
12	DSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止计数器递减计数 1：当GTIOCnA输入为0时，在GTIOCnB输入上升沿使能计数器递减计数	R/W
13	DSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止计数器递减计数 1：当GTIOCnA输入为1时，在GTIOCnB输入上升沿使能计数器递减计数	R/W
14	DSCBFAL	GTIOCnA值低源计数器倒计时期间的GTIOCnB引脚下降输入Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止计数器递减计数 1：当GTIOCnA输入为0时，在GTIOCnB输入下降沿使能计数器递减计数	R/W
15	DSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源计数器倒计时Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止计数器递减计数 1：当GTIOCnA输入为1时，在GTIOCnB输入下降沿使能计数器递减计数	R/W
16	DSELCA	ELC_GPTA事件源计数器倒计时启用 0：在ELC_GPTA输入处禁用计数器递减计数1：在ELC_GPTA输入处启用计数器递减计数	R/W
17	DSELCB	ELC_GPTB事件源计数器倒计时启用 0：在ELC_GPTB输入处禁用计数器递减计数1：在ELC_GPTB输入处启用计数器递减计数	R/W

Bit	Symbol	Function	R/W
18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTC input 1: Counter count down enabled at the ELC_GPTC input	R/W
19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTD input 1: Counter count down enabled at the ELC_GPTD input	R/W
20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTE input 1: Counter count down enabled at the ELC_GPTE input	R/W
21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W
22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTG input 1: Counter count down enabled at the ELC_GPTG input	R/W
23	DSELCH	ELC_GPTF Event Source Counter Count Down Enable 0: Counter count down disabled at the ELC_GPTF input 1: Counter count down enabled at the ELC_GPTF input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR sets the source to count down the GTCNT counter.

Number of decrement in counting is one even when multiple sources are generated simultaneously.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted down by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Down Enable)

The DSGTRGCR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGC pin input.

DSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Down Enable)

The DSGTRGCF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGC pin input.

DSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Down Enable)

The DSGTRGDR bit enables or disables the GTCNT counter count down on the rising edge of the GTETRGD pin input.

DSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Down Enable)

The DSGTRGDF bit enables or disables the GTCNT counter count down on the falling edge of the GTETRGD pin input.

Bit	Symbol	Function	R/W
18	DSELCC	ELC_GPTC事件源计数器倒计时使能 0：在ELC_GPTC输入处禁用计数器递减计数1：在ELC_GPTC输入处启用计数器递减计数	R/W
19	DSELCD	ELC_GPTD事件源计数器倒计时启用 0：在ELC_GPTD输入处禁用计数器递减计数1：在ELC_GPTD输入处启用计数器递减计数	R/W
20	DSELCE	ELC_GPTE事件源计数器倒计时启用 0：在ELC_GPTE输入处禁用计数器递减计数1：在ELC_GPTE输入处启用计数器递减计数	R/W
21	DSELCF	ELC_GPTF事件源计数器倒计时启用 0：在ELC_GPTF输入处禁用计数器递减计数1：在ELC_GPTF输入处启用计数器递减计数	R/W
22	DSELCG	ELC_GPTG事件源计数器倒计时使能 0：在ELC_GPTG输入处禁用计数器递减计数1：在ELC_GPTG输入处启用计数器递减计数	R/W
23	DSELCH	ELC_GPTF事件源计数器倒计时启用 0：在ELC_GPTF输入处禁用计数器递减计数1：在ELC_GPTF输入处启用计数器递减计数	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

GTDNSR将源设置为对GTCNT计数器进行倒计时。

即使同时生成多个源，计数的减量也是一。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

当GTDNSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行倒数计数。在这种情况下，GTCR.TPCS无效。

DSGTRGAR位（GTETRGA引脚上升沿输入源计数器倒计时使能）

DSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGAF位（GTETRGA引脚下降输入源计数器倒计时使能）

DSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGBR位（GTETRGB引脚上升输入源计数器倒计时使能）

DSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGBF位（GTETRGB引脚下降输入源计数器倒计时使能）

DSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGCR位（GTETRGC引脚上升沿输入源计数器向下计数使能）

DSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGCF位（GTETRGC引脚下降输入源计数器倒计时使能）

DSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGDR位（GTETRGD引脚上升沿输入源计数器倒计时使能）

DSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGDF位（GTETRGD引脚下降输入源计数器倒计时使能）

DSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

DSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

DSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

DSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables the GTCNT counter count down on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables the GTCNT counter count down on the rising edge of GTIOCnB pin input, when GTIOCnA input is 1.

DSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

DSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables the GTCNT counter count down on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables the GTCNT counter count down at the ELC_GPTm event input.

21.2.10 GTICASR : General PWM Timer Input Capture Source Select Register A

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR

DSCARBL位（GTIOCnB值低电平期间GTIOCnA引脚上升沿输入源计数器向下计数Enable)

当GTIOCnB输入为0时，DSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚上升沿输入源计数器向下计数Enable)

DSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnB输入为1。

DSCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源计数器倒计时Enable)

当GTIOCnB输入为0时，DSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源计数器向下计数Enable)

当GTIOCnB输入为1时，DSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源计数器向下计数Enable)

DSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为0。

DSCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源计数器向下计数Enable)

DSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为1。

DSCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源计数器向下计数Enable)

DSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器倒计时，当GTIOCnA输入为0。

DSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源计数器倒计时Enable)

当GTIOCnA输入为1时，DSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSELCm位（ELC_GPTm事件源计数器倒计时启用）（m=A到H）

DSELCm位在ELC_GPTm事件输入处启用或禁用GTCNT计数器倒计时。

21.2.10 GTICASR：通用PWM定时器输入捕捉源选择寄存器A

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR

Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGA input 1: GTCCRA input capture enabled on the rising edge of GTETRGA input	R/W
1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGA input 1: GTCCRA input capture enabled on the falling edge of GTETRGA input	R/W
2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGB input 1: GTCCRA input capture enabled on the rising edge of GTETRGB input	R/W
3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGB input 1: GTCCRA input capture enabled on the falling edge of GTETRGB input	R/W
4	ASGTRGCR	GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGC input 1: GTCCRA input capture enabled on the rising edge of GTETRGC input	R/W
5	ASGTRGCF	GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGC input 1: GTCCRA input capture enabled on the falling edge of GTETRGC input	R/W
6	ASGTRGDR	GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTETRGD input 1: GTCCRA input capture enabled on the rising edge of GTETRGD input	R/W
7	ASGTRGDF	GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTETRGD input 1: GTCCRA input capture enabled on the falling edge of GTETRGD input	R/W
8	ASCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W
9	ASCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	ASCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	ASCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	ASCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W

重置后的值: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
0	ASGTRGAR	GTETRGA引脚上升输入源GTCCRA输入捕捉使能 0：在GTETRGA输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGA输入的上升沿启用GTCCRA输入捕捉	R/W
1	ASGTRGAF	GTETRGA引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGA输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGA输入的下降沿启用GTCCRA输入捕捉	R/W
2	ASGTRGBR	GTETRGB引脚上升输入源GTCCRA输入捕捉使能 0：在GTETRGB输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGB输入的上升沿启用GTCCRA输入捕捉	R/W
3	ASGTRGBF	GTETRGB引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGB输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGB输入的下降沿启用GTCCRA输入捕捉	R/W
4	ASGTRGCR	GTETRGC引脚上升沿输入源GTCCRA输入捕捉使能 0：在GTETRGC输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGC输入的上升沿启用GTCCRA输入捕捉	R/W
5	ASGTRGCF	GTETRGC引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGC输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGC输入的下降沿启用GTCCRA输入捕捉	R/W
6	ASGTRGDR	GTETRGD引脚上升沿输入源GTCCRA输入捕捉使能 0：在GTETRGD输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGD输入的上升沿启用GTCCRA输入捕捉	R/W
7	ASGTRGDF	GTETRGD引脚下降输入源GTCCRA输入捕捉使能 0：在GTETRGD输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGD输入的下降沿启用GTCCRA输入捕捉	R/W
8	ASCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能GTCCRA输入捕捉	R/W
9	ASCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能GTCCRA输入捕捉	R/W
10	ASCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止GTCCRA输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能GTCCRA输入捕捉	R/W
11	ASCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿启用GTCCRA输入捕捉	R/W
12	ASCBRAL	GTIOCnB引脚在GTIOCnA值低电平期间的上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能GTCCRA输入捕捉	R/W

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Bit	Symbol	Function	R/W
13	ASCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	ASCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	ASCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRA input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTA input 1: GTCCRA input capture enabled at the ELC_GPTA input	R/W
17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTB input 1: GTCCRA input capture enabled at the ELC_GPTB input	R/W
18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTC input 1: GTCCRA input capture enabled at the ELC_GPTC input	R/W
19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTD input 1: GTCCRA input capture enabled at the ELC_GPTD input	R/W
20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTE input 1: GTCCRA input capture enabled at the ELC_GPTE input	R/W
21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTF input 1: GTCCRA input capture enabled at the ELC_GPTF input	R/W
22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTG input 1: GTCCRA input capture enabled at the ELC_GPTG input	R/W
23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable 0: GTCCRA input capture disabled at the ELC_GPTH input 1: GTCCRA input capture enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The GTICASR sets the source of input capture for GTCCRA.

When at least one bit among bits in the GTICASR register is set to 1, input capture operation making the GTCCRA register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGA pin input.

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGA pin input.

Bit	Symbol	Function	R/W
13	ASCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止GTCCRA输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能GTCCRA输入捕捉	R/W
14	ASCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿启用GTCCRA输入捕捉	R/W
15	ASCBFAH	GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁用GTCCRA输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用GTCCRA输入捕捉	R/W
16	ASELCA	ELC_GPTA事件源GTCCRA输入捕获启用 0：在ELC_GPTA输入处禁用GTCCRA输入捕捉1：在ELC_GPTA输入处启用GTCCRA输入捕捉	R/W
17	ASELCB	ELC_GPTB事件源GTCCRA输入捕获启用 0：在ELC_GPTB输入处禁用GTCCRA输入捕捉1：在ELC_GPTB输入处启用GTCCRA输入捕捉	R/W
18	ASELCC	ELC_GPTC事件源GTCCRA输入捕捉使能 0：在ELC_GPTC输入处禁用GTCCRA输入捕捉1：在ELC_GPTC输入处启用GTCCRA输入捕捉	R/W
19	ASELCD	ELC_GPTD事件源GTCCRA输入捕获启用 0：在ELC_GPTD输入处禁用GTCCRA输入捕捉1：在ELC_GPTD输入处启用GTCCRA输入捕捉	R/W
20	ASELCE	ELC_GPTE事件源GTCCRA输入捕获启用 0：在ELC_GPTE输入处禁用GTCCRA输入捕捉1：在ELC_GPTE输入处启用GTCCRA输入捕捉	R/W
21	ASELCF	ELC_GPTF事件源GTCCRA输入捕获启用 0：在ELC_GPTF输入处禁用GTCCRA输入捕捉1：在ELC_GPTF输入处启用GTCCRA输入捕捉	R/W
22	ASELCG	ELC_GPTG事件源GTCCRA输入捕捉使能 0：在ELC_GPTG输入处禁用GTCCRA输入捕捉1：在ELC_GPTG输入处启用GTCCRA输入捕捉	R/W
23	ASELCH	ELC_GPTH事件源GTCCRA输入捕获启用 0：在ELC_GPTH输入处禁用GTCCRA输入捕捉1：在ELC_GPTH输入处启用GTCCRA输入捕捉	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

GTICASR设置GTCCRA的输入捕获源。

当GTICASR寄存器中的至少一位被设置为1时，执行将GTCCRA寄存器作为输入捕捉寄存器的输入捕捉操作。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

ASGTRGAR位（GTETRGA引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGAF位（GTETRGA引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

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ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGCR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGC pin input.

ASGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGCF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGC pin input.

ASGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGDR bit enables or disables the input capture for GTCCRA on the rising edge of the GTETRGD pin input.

ASGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGDF bit enables or disables the input capture for GTCCRA on the falling edge of the GTETRGD pin input.

ASCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

ASCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

ASCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnA pin input, when the GTIOCnB input is 1.

ASCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when the GTIOCnA input is 0.

ASCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables the input capture for GTCCRA on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

ASGTRGBR位（GTETRGB引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBF位（GTETRGB引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGCR位（GTETRGC引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGCF位（GTETRGC引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGDR位（GTETRGD引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGDF位（GTETRGD引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCARBL位（GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为0。

ASCARBH位（GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为1。

ASCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable)

ASCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnB输入为0。

ASCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源GTCCRA输入捕捉Enable)

当GTIOCnB输入为1时，ASCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCBRAL位（GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable)

当GTIOCnA输入为0时，ASCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASCBRAH位（GTIOCnA值高电平期间GTIOCnB引脚上升沿输入源GTCCRA输入捕捉Enable)

ASCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为1。

ASCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为0。

ASCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables the input capture for GTCCRA on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables the input capture for GTCCRA at the ELC_GPTm event input.

21.2.11 GTICBSR : General PWM Timer Input Capture Source Select Register B

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGA input 1: GTCCRB input capture enabled on the rising edge of GTETRGA input	R/W
1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGA input 1: GTCCRB input capture enabled on the falling edge of GTETRGA input	R/W
2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGB input 1: GTCCRB input capture enabled on the rising edge of GTETRGB input	R/W
3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGB input 1: GTCCRB input capture enabled on the falling edge of GTETRGB input	R/W
4	BSGTRGCR	GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGC input 1: GTCCRB input capture enabled on the rising edge of GTETRGC input	R/W
5	BSGTRGCF	GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGC input 1: GTCCRB input capture enabled on the falling edge of GTETRGC input	R/W
6	BSGTRGDR	GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTETRGD input 1: GTCCRB input capture enabled on the rising edge of GTETRGD input	R/W
7	BSGTRGDF	GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTETRGD input 1: GTCCRB input capture enabled on the falling edge of GTETRGD input	R/W
8	BSCARBL	GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 0	R/W

ASCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCnA输入为1。

ASELCm位（ELC_GPTm事件源计数器GTCCRA输入捕捉使能）（m=A到H）

ASELCm位在ELC_GPTm事件输入处启用或禁用GTCCRA的输入捕捉。

21.2.11 GTICBSR：通用PWM定时器输入捕捉源选择寄存器B

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BSGTRGAR	GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGA输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGA输入的上升沿启用GTCCRB输入捕捉	R/W
1	BSGTRGAF	GTETRGA引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGA输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGA输入的下降沿启用GTCCRB输入捕捉	R/W
2	BSGTRGBR	GTETRGB引脚上升输入源GTCCRB输入捕捉使能 0：在GTETRGB输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGB输入的上升沿启用GTCCRB输入捕捉	R/W
3	BSGTRGBF	GTETRGB引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGB输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGB输入的下降沿启用GTCCRB输入捕捉	R/W
4	BSGTRGCR	GTETRGC引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGC输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGC输入的上升沿启用GTCCRB输入捕捉	R/W
5	BSGTRGCF	GTETRGC引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGC输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGC输入的下降沿启用GTCCRB输入捕捉	R/W
6	BSGTRGDR	GTETRGD引脚上升沿输入源GTCCRB输入捕捉使能 0：在GTETRGD输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGD输入的上升沿启用GTCCRB输入捕捉	R/W
7	BSGTRGDF	GTETRGD引脚下降输入源GTCCRB输入捕捉使能 0：在GTETRGD输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGD输入的下降沿启用GTCCRB输入捕捉	R/W
8	BSCARBL	GTIOCnB值低电平期间的GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的上升沿使能GTCCRB输入捕捉	R/W

Bit	Symbol	Function	R/W
9	BSCARBH	GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnA input when GTIOCnB input is 1	R/W
10	BSCAFBL	GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 0	R/W
11	BSCAFBH	GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnA input when GTIOCnB input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnA input when GTIOCnB input is 1	R/W
12	BSCBRAL	GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 0	R/W
13	BSCBRAH	GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the rising edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the rising edge of GTIOCnB input when GTIOCnA input is 1	R/W
14	BSCBFAL	GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 0 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 0	R/W
15	BSCBFAH	GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled on the falling edge of GTIOCnB input when GTIOCnA input is 1 1: GTCCRB input capture enabled on the falling edge of GTIOCnB input when GTIOCnA input is 1	R/W
16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTA input 1: GTCCRB input capture enabled at the ELC_GPTA input	R/W
17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTB input 1: GTCCRB input capture enabled at the ELC_GPTB input	R/W
18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTC input 1: GTCCRB input capture enabled at the ELC_GPTC input	R/W
19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTD input 1: GTCCRB input capture enabled at the ELC_GPTD input	R/W
20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTE input 1: GTCCRB input capture enabled at the ELC_GPTE input	R/W
21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTF input 1: GTCCRB input capture enabled at the ELC_GPTF input	R/W

Bit	Symbol	Function	R/W
9	BSCARBH	GTIOCnB值高电平期间的GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的上升沿使能GTCCRB输入捕捉	R/W
10	BSCAFBL	GTIOCnB值低电平期间的GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为0时，在GTIOCnA输入的下降沿使能GTCCRB输入捕捉	R/W
11	BSCAFBH	GTIOCnB值高电平期间的GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnB输入为1时，在GTIOCnA输入的下降沿使能GTCCRB输入捕捉	R/W
12	BSCBRAL	GTIOCnA值低电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的上升沿使能GTCCRB输入捕捉	R/W
13	BSCBRAH	GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的上升沿使能GTCCRB输入捕捉	R/W
14	BSCBFAL	GTIOCnA值低电平期间的GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为0时，在GTIOCnB输入的下降沿使能GTCCRB输入捕捉	R/W
15	BSCBFAH	GTIOCnA值高电平期间的GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable 0：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿禁止GTCCRB输入捕捉 1：当GTIOCnA输入为1时，在GTIOCnB输入的下降沿启用GTCCRB输入捕捉	R/W
16	BSELCA	ELC_GPTA事件源GTCCRB输入捕获启用 0：在ELC_GPTA输入处禁用GTCCRB输入捕捉1：在ELC_GPTA输入处启用GTCCRB输入捕捉	R/W
17	BSELCB	ELC_GPTB事件源GTCCRB输入捕捉使能 0：在ELC_GPTB输入处禁用GTCCRB输入捕捉1：在ELC_GPTB输入处启用GTCCRB输入捕捉	R/W
18	BSELCC	ELC_GPTC事件源GTCCRB输入捕捉使能 0：在ELC_GPTC输入处禁用GTCCRB输入捕捉1：在ELC_GPTC输入处启用GTCCRB输入捕捉	R/W
19	BSELCD	ELC_GPTD事件源GTCCRB输入捕获启用 0：在ELC_GPTD输入处禁用GTCCRB输入捕捉1：在ELC_GPTD输入处启用GTCCRB输入捕捉	R/W
20	BSELCE	ELC_GPTE事件源GTCCRB输入捕获启用 0：在ELC_GPTE输入处禁用GTCCRB输入捕捉1：在ELC_GPTE输入处启用GTCCRB输入捕捉	R/W
21	BSELCF	ELC_GPTF事件源GTCCRB输入捕获启用 0：在ELC_GPTF输入处禁用GTCCRB输入捕捉1：在ELC_GPTF输入处启用GTCCRB输入捕捉	R/W

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Bit	Symbol	Function	R/W
22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTG input 1: GTCCRB input capture enabled at the ELC_GPTG input	R/W
23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable 0: GTCCRB input capture disabled at the ELC_GPTH input 1: GTCCRB input capture enabled at the ELC_GPTH input	R/W
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The GTICBSR sets the source of input capture for GTCCRB.

When at least one bit among bits in the GTICBSR register is set to 1, input capture operation making the GTCCRB register as an input capture register is performed.

Inputs from GTETRGn (n = A to D) pins are input to the GPT via the POEG. Set the polarity of these signals with the POEG.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables the input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGCR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGC pin input.

BSGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGCF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGC pin input.

BSGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGDR bit enables or disables the input capture for GTCCRB on the rising edge of GTETRGD pin input.

BSGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGDF bit enables or disables the input capture for GTCCRB on the falling edge of the GTETRGD pin input.

BSCARBL bit (GTIOCnA Pin Rising Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when the GTIOCnB input is 0.

BSCARBH bit (GTIOCnA Pin Rising Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCAFBL bit (GTIOCnA Pin Falling Input during GTIOCnB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 0.

Bit	Symbol	Function	R/W
22	BSELCG	ELC_GPTG事件源GTCCRB输入捕捉使能 0：在ELC_GPTG输入处禁用GTCCRB输入捕捉1：在ELC_GPTG输入处启用GTCCRB输入捕捉	R/W
23	BSELCH	ELC_GPTH事件源GTCCRB输入捕捉使能 0：在ELC_GPTH输入处禁用GTCCRB输入捕捉1：在ELC_GPTH输入处启用GTCCRB输入捕捉	R/W
31:24	—	这些位被读取为0。写入值应为0。	R/W

GTICBSR设置GTCCRB的输入捕获源。

当GTICBSR寄存器中的至少一位被设置为1时，执行将GTCCRB寄存器作为输入捕捉寄存器的输入捕捉操作。

来自GTETRn（n=A到D）引脚的输入通过POEG输入到GPT。设置这些信号的极性
POEG.

BSGTRGAR位（GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGAF位（GTETRGA引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBR位（GTETRGB引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBF位（GTETRGB引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGCR位（GTETRGC引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGCF位（GTETRGC引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGDR位（GTETRGD引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGDF位（GTETRGD引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSCARBL位（GTIOCnB值低电平期间GTIOCnA引脚上升沿输入源GTCCRB输入捕捉Enable)

当GTIOCnB输入为0时，BSCARBL位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSCARBH位（GTIOCnB值高电平期间GTIOCnA引脚的上升沿输入源GTCCRB输入捕捉Enable)

BSCARBH位在GTIOCnA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当
GTIOCnB输入为1。

BSCAFBL位（GTIOCnB值低电平期间GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBL位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当
GTIOCnB输入为0。

BSCAFBH bit (GTIOCnA Pin Falling Input during GTIOCnB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnA pin input, when GTIOCnB input is 1.

BSCBRAL bit (GTIOCnB Pin Rising Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBRAH bit (GTIOCnB Pin Rising Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables the input capture for GTCCRB on the rising edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSCBFAL bit (GTIOCnB Pin Falling Input during GTIOCnA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 0.

BSCBFAH bit (GTIOCnB Pin Falling Input during GTIOCnA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables the input capture for GTCCRB on the falling edge of the GTIOCnB pin input, when GTIOCnA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables the input capture for GTCCRB at the ELC_GPTm event input.

21.2.12 GTCR : General PWM Timer Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	TPCS[3:0]				—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	Count Start 0: Count operation is stopped 1: Count operation is performed	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

BSCAFBH位（GTIOCnB值高电平期间GTIOCnA引脚下降输入源GTCCRB输入捕捉Enable)

BSCAFBH位在GTIOCnA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnB输入为1。

BSCBRAL位（GTIOCnA值低电平期间GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAL位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为0。

BSCBRAH位（GTIOCnA值高电平期间的GTIOCnB引脚上升沿输入源GTCCRB输入捕捉Enable)

BSCBRAH位在GTIOCnB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为1。

BSCBFAL位（GTIOCnA值低电平期间GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAL位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为0。

BSCBFAH位（GTIOCnA值高电平期间GTIOCnB引脚下降输入源GTCCRB输入捕捉Enable)

BSCBFAH位在GTIOCnB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCnA输入为1。

BSELCm位（ELC_GPTm事件源计数器GTCCRB输入捕捉使能）（m=A到H）

BSELCm位在ELC_GPTm事件输入处启用或禁用GTCCRB的输入捕捉。

21.2.12 GTCR:通用PWM定时器控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	TPCS[3:0]				—	—	—	—	MD[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CST	计数开始 0：停止计数1：进行计数	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
18:16	MD[2:0]	Mode Select 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer is possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer is possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited	R/W
22:19	—	These bits are read as 0. The write value should be 0.	R/W
26:23	TPCS[3:0]	Timer Prescaler Select 0 0 0 0: PCLKD/1 0 0 0 1: PCLKD/2 0 0 1 0: PCLKD/4 0 0 1 1: PCLKD/8 0 1 0 0: PCLKD/16 0 1 0 1: PCLKD/32 0 1 1 0: PCLKD/64 0 1 1 1: Setting prohibited 1 0 0 0: PCLKD/256 1 0 0 1: Setting prohibited 1 0 1 0: PCLKD/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (Via the POEG) 1 1 0 1: GTETRGB (Via the POEG) 1 1 1 0: GTETRGC (Via the POEG) 1 1 1 1: GTETRGD (Via the POEG)	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

The GTCR controls GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- The GTSTR value where the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input that are enabled by GTSSR for the starting counter source, occurs (n = 0 to 9)
- 1 is written by software directly.

[Clearing conditions]

- The GTSTP value where the channel number associated with the bit number is set to 1 with the GTPSR.CSTOP bit at 1
- The ELC event input, the external trigger, or the GTIOCnA/GTIOCnB input enabled by GTSSR as the counter stop source, occurs (n = 0 to 9)
- 0 is written by software directly.
- When the period count function is finished while the GTPC.ASTP bit is 1.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

TPCS[3:0] bits (Timer Prescaler Select)

The TPCS[3:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[3:0] bits must be set while the GTCNT operation is stopped.

Bit	Symbol	Function	R/W
18:16	MD[2:0]	模式选择 000：Saw-wavePWM模式（单缓存或双缓存均可）001：Saw-waveOne-shot脉冲模式（固定缓存操作）010：禁止设置011：禁止设置100：三角波PWM模式1（波谷32位传输）（单缓冲器或双缓冲器均可） 101：三角波PWM模式2（波峰和波谷32位传输）（单缓冲器或双缓冲器均可） 110：三角波PWM模式3（谷底64位传输）（固定缓冲操作）111：禁止设置	R/W
22:19	—	这些位被读取为0。写入值应为0。	R/W
26:23	TPCS[3:0]	定时器预分频器选择 0000：PCLKD10001：PCLKD20010：PCLKD40011：PCLKD80100：PCLKD160101：PCLKD320110：PCLKD640111：禁止设置1000：PCLKD2561001：禁止设置1010：PCLKD10241011：禁止设置1100：GTETRGA（通过POEG）1101：GTETRGB（通过POEG）1110：GTETRGC（通过POEG）1111：GTETRGD（通过POEG）	R/W
31:27	—	这些位被读取为0。写入值应为0。	R/W

GTCR控制GTCNT。

CST bit (Count Start)

CST位控制GTCNT计数器的启动和停止。

[Setting conditions]

●GTSTR值，其中与位号关联的通道号设置为1，GTSSR.CSTRT位为1

●发生由GTSSR为启动计数器源启用的ELC事件输入、外部触发或GTIOCnAGTIOCnB输入（n=0到9）

●1由软件直接写入。

[Clearing conditions]

●GTSTP值，其中与位号关联的通道号设置为1，且GTPSR.CSTOP位为1

●发生ELC事件输入、外部触发或GTSSR作为计数器停止源使能的GTIOCnAGTIOCnB输入（n=0至9）

●0由软件直接写入。

●当GTPC.ASTP位为1时，周期计数功能完成。

MD[2:0] bits (Mode Select)

MD[2:0]位选择GPT操作模式。当GTCNT操作停止时，必须设置MD[2:0]位。

TPCS[3:0] bits (Timer Prescaler Select)

TPCS[3:0]位选择GTCNT的时钟。可为每个通道独立选择时钟预分频器。这
当GTCNT操作停止时，必须设置TPCS[3:0]位。

21.2.13 GTUDDTYC : General PWM Timer Count Direction and Duty Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	Count Direction Setting 0: GTCNT counts down 1: GTCNT counts up	R/W
1	UDF	Forcible Count Direction Setting 0: Not forcibly set 1: Forcibly set	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	OADTY[1:0]	GTIOCnA Output Duty Setting 0 0: GTIOCnA pin duty depends on the compare match 0 1: GTIOCnA pin duty depends on the compare match 1 0: GTIOCnA pin duty 0% 1 1: GTIOCnA pin duty 100%	R/W
18	OADTYF	Forcible GTIOCnA Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
19	OADTYR	GTIOCnA Output Value Selecting after Releasing 0%/100% Duty Setting 0: Apply output value set in 0%/100% duty to GTIOA[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOA[3:2] function after releasing 0%/100% duty setting	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
25:24	OBDTY[1:0]	GTIOCnB Output Duty Setting 0 0: GTIOCnB pin duty depends on the compare match 0 1: GTIOCnB pin duty depends on the compare match 1 0: GTIOCnB pin duty 0% 1 1: GTIOCnB pin duty 100%	R/W
26	OBDTYF	Forcible GTIOCnB Output Duty Setting 0: Not forcibly set 1: Forcibly set	R/W
27	OBDTYR	GTIOCnB Output Value Selecting after Releasing 0%/100% Duty Setting 0: Apply output value set in 0%/100% duty to GTIOB[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOB[3:2] function after releasing 0%/100% duty setting	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTUDDTYC sets the direction in which the GTCNT counts (up-counting or down-counting), and sets the duty of the GTIOCnA/GTIOCnB pin output.

The setting is invalid during the event count operation.

Count Direction:

21.2.13 GTUDDTYC:通用PWM定时器计数方向和占空比设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	UD	计数方向设置 0：GTCNT向下计数1：G TCNT向上计数	R/W
1	UDF	强制计数方向设置 0：不强制设置1 ：强制设置	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
17:16	OADTY[1:0]	GTIOCnA输出占空比设置 00：GTIOCnA引脚占空比取决于比较匹配01：GTIOCnA 引脚占空比取决于比较匹配10：GTIOCnA引脚占空比0% 11：GTIOCnA引脚占空比100%	R/W
18	OADTYF	强制GTIOCnA输出占空比设置 0：不强制设置1 ：强制设置	R/W
19	OADTYR	解除0%100%占空比设置后GTIOCnA输出值选择 0：释放0%100%duty设置后，将0%100%duty中设置的输出值应用于GTIOA[3:2] 功能 1：释放0%100%占空比设置后，将屏蔽比较匹配输出值应用于GTIOA[3:2]函数	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
25:24	OBDTY[1:0]	GTIOCnB输出占空比设置 00：GTIOCnB引脚占空比取决于比较匹配01：GTIOCnB 引脚占空比取决于比较匹配10：GTIOCnB引脚占空比0% 11：GTIOCnB引脚占空比100%	R/W
26	OBDTYF	强制GTIOCnB输出占空比设置 0：不强制设置1 ：强制设置	R/W
27	OBDTYR	GTIOCnB释放后输出值选择0%100%占空比设置 0：解除0%100%duty设置后，将0%100%duty中设置的输出值应用于GTIOB[3:2] 功能 1：在释放0%100%占空比设置后，将屏蔽比较匹配输出值应用到GTIOB[3:2]函数	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTUDDTYC设置GTCNT计数的方向（向上计数或向下计数），并设置GTIOCnAGTIOCnB引脚输出。

该设置在事件计数操作期间无效。

Count Direction:

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- In saw-wave mode.
  When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting stops, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting stops, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).
  When the UDF bit is set to 1 while counting stops, the UD bit value is reflected in the count direction when counting starts.
- In triangle-wave mode.
  When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting stops, the change is not reflected in the count direction when counting starts.
  When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only 0 should be written to this bit during counter operation. When 1 is written to this bit while counting stops, return this bit to 0 before counting starts.

Output duty

- In saw-wave mode.
  When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR).
  When the OADTY/OBDTY value is changed during down-counting, the duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops the output duty is not reflected at the starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.
- In triangle-wave mode.
  When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 0 and while counting stops, the output duty is not reflected at the starting counter operation. The output duty is reflected at an underflow.
  When the OADTY/OBDTY value is changed with the OADTYF/OBDTYF bit being 1 and while counting stops, the output duty is reflected at starting counter operation.

In both saw-wave mode and triangle-wave mode, when the OADTYF/OBDTYF bit is set back to 0 and the OADTY[1:0]/OBDTY[1:0] bits are set after setting the OADTYF/OBDTYF bit to 1 and setting the OADTY[1:0]/OBDTY[1:0] bits for the duty of first cycle while count operation is stopped, these duty-cycle set during stopping count operation are reflected in the first cycle and the second cycle after starting count operation.

OmDTY[1:0] bits (GTIOCm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty (0%, 100% or compare match control) of the GTIOCm pin.

OmDTYF bit (Forcible GTIOCm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation.

●在锯齿波模式下。
如果在向上计数期间将UD值设置为0，则计数方向会在溢出时发生变化（GTCNT值变为GTPR值后与计数时钟同步的时序）。在递减计数期间将UD值设置为1时，计数方向会在下溢（GTCNT值变为0后与计数时钟同步的时序）下发生变化。当UDF位为0时UD值从1变为0并且在计数停止时，计数器开始计数并且计数方向在溢出时改变（GTCNT值变为GTPR值后与计数时钟同步的时序）。当UDF位为0时UD值从0变为1并且在计数停止时，计数器开始递减计数并且计数方向在下溢时改变（GTCNT值变为0后与计数时钟同步的时序）。当计数停止时UDF位设置为1时，UD位值在计数开始时反映在计数方向上。

●三角波模式。
计数过程中UD值变化时，计数方向不变。当UDF位为0时UD值发生变化并且计数停止时，该变化不会反映在计数开始时的计数方向上。当计数停止时UDF位设置为1时，UD值在计数开始时反映在计数方向上。

UD位（计数方向设置）

UD位设置GTCNT的计数方向（向上计数或向下计数）。

UDF位（强制计数方向设置）

当GTCNT开始操作时，UDF位将计数方向强制设置为UD值。在计数器操作期间，只能将0写入该位。当计数停止时向该位写入1时，在计数开始前将该位返回0。

输出占空比

●在锯齿波模式下。
当OADTYOBDTY值在递增计数期间发生变化时，占空比反映在溢出处(GTCNT=GTPR)。
在递减计数期间更改OADTYOBDTY值时，占空比反映为下溢(GTCNT=0)。在OADTYFOBDTYF位为0的情况下更改OADTYOBDTY值并且在计数停止时，输出占空比不会反映在启动计数器操作中。当计数方向向上时，输出占空比反映在溢出处(GTCNT=GTPR)。当计数方向向下时，输出占空比反映为下溢(GTCNT=0)。当OADTYFOBDTYF位为1并改变OADTYOBDTY值时，当计数停止时，输出占空比反映在开始计数器操作时。

●三角波模式。
当计数期间OADTYOBDTY值发生变化时，占空比反映为下溢。
在OADTYFOBDTYF位为0的情况下更改OADTYOBDTY值并且在计数停止时，输出占空比不会反映在开始计数器操作中。输出占空比反映在下溢处。当OADTYFOBDTYF位为1并改变OADTYOBDTY值时，当计数停止时，输出占空比反映在开始计数器操作时。

在锯齿波模式和三角波模式中，当OADTYFOBDTYF位被设置回0并且OADTY[1:0]OBDTY[1:0]位在设置OADTYFOBDTYF位为1并设置OADTY[1:0]OBDTY[1:0]位用于计数操作停止时第一个周期的占空比，这些在停止计数操作期间设置的占空比反映在开始计数操作后的第一个周期和第二个周期中。

OmDTY[1:0]位（GTIOCm输出占空比设置）（m=A，B）

OmDTY[1:0]位设置GTIOCm引脚的输出占空比（0%、100%或比较匹配控制）。

OmDTYF位（强制GTIOCm输出占空比设置）（m=A，B）

OmDTYF位强制将输出占空比设置为OmDTY设置。在计数器操作期间将此位设置为0。

OmDTYR bit (GTIOCm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bit selects the value that is the object of output retained or toggled at cycle end, when the control changes from 0% or 100% duty setting to compare match for the GTIOCm pin and GTIOR. The GTIOm[3:2] bits are set to 00b (output retained at cycle end) or the GTIOR.GTIOm[3:2] bits are set to 11b (output toggled at cycle end).

The GPT internally continues to perform compare match operation while 0% or 100% duty operation is running. When the OmDTYR bit is set to 1, the value of the compare match at cycle end is applied to the GTIOR.GTIOm [3:2] bits.

21.2.14 GTIOR : General PWM Timer I/O Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA Pin Function Select See Table 21.4.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	OADFLT	GTIOCnA Pin Output Value Setting at the Count Stop 0: The GTIOCnA pin outputs low when counting stops 1: The GTIOCnA pin outputs high when counting stops	R/W
7	OAHLD	GTIOCnA Pin Output Setting at the Start/Stop Count 0: The GTIOCnA pin output level at the start or stop of counting depends on the register setting 1: The GTIOCnA pin output level is retained at the start or stop of counting	R/W
8	OAE	GTIOCnA Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
10:9	OADF[1:0]	GTIOCnA Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnA pin is set to Hi-Z on output disable 1 0: GTIOCnA pin is set to 0 on output disable 1 1: GTIOCnA pin is set to 1 on output disable	R/W
12:11	—	These bits are read as 0. The write value should be 0.	R/W
13	NFAEN	Noise Filter A Enable 0: The noise filter for the GTIOCnA pin is disabled 1: The noise filter for the GTIOCnA pin is enabled	R/W
15:14	NFCSA[1:0]	Noise Filter A Sampling Clock Select 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W
20:16	GTIOB[4:0]	GTIOCnB Pin Function Select See Table 21.4.	R/W
21	—	This bit is read as 0. The write value should be 0.	R/W

OmDTYR位（释放0%100%占空比设置后选择GTIOCm输出值）（m=A、B）

当控制从0%或100%占空比设置更改为GTIOCm引脚和GTIOR比较匹配时，OmDTYR位选择作为输出对象在周期结束时保留或切换的值。GTIOm[3:2]位设置为00b（输出在循环结束时保留）或GTIOR.GTIOm[3:2]位设置为11b（输出在循环结束时切换）。

GPT在内部继续执行比较匹配操作，而0%或100%占空比操作正在运行。当。。。的时候OmDTYR位设置为1，循环结束时比较匹配的值应用于GTIOR.GTIOm[3:2]位。

21.2.14 GTIOR：通用PWM定时器IO控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	GTIOA[4:0]	GTIOCnA引脚功能选择 见表21.4。	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	OADFLT	计数停止时的GTIOCnA引脚输出值设置 0：计数停止时GTIOCnA引脚输出低电平1：计数停止时GTIOCnA引脚输出高电平	R/W
7	OAHLD	开始停止计数时的GTIOCnA引脚输出设置 0：GTIOCnA引脚在计数开始或停止时的输出电平取决于寄存器设置 1：GTIOCnA引脚输出电平在计数开始或停止时保持不变	R/W
8	OAE	GTIOCnA引脚输出使能 0：禁用输出1：启用输出	R/W
10:9	OADF[1:0]	GTIOCnA引脚禁用值设置 00：禁止输出01：GTIOCnA引脚设置为Hi-Z，输出禁止10：GTIOCnA引脚设置为0，输出禁止11：GTIOCnA引脚设置为1，输出禁止	R/W
12:11	—	这些位被读取为0。写入值应为0。	R/W
13	NFAEN	噪声滤波器A启用 0：GTIOCnA引脚的噪声滤波器禁用1：GTIOCnA引脚的噪声滤波器启用	R/W
15:14	NFCSA[1:0]	噪声滤波器A采样时钟选择 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W
20:16	GTIOB[4:0]	GTIOCnB引脚功能选择 见表21.4。	R/W
21	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
22	OBDFLT	GTIOCnB Pin Output Value Setting at the Count Stop 0: The GTIOCnB pin outputs low when counting stops 1: The GTIOCnB pin outputs high when counting stops	R/W
23	OBHLD	GTIOCnB Pin Output Setting at the Start/Stop Count 0: The GTIOCnB pin output level at the start/stop of counting depends on the register setting 1: The GTIOCnB pin output level is retained at the start/stop of counting	R/W
24	OBE	GTIOCnB Pin Output Enable 0: Output is disabled 1: Output is enabled	R/W
26:25	OBDF[1:0]	GTIOCnB Pin Disable Value Setting 0 0: Output disable is prohibited 0 1: GTIOCnB pin is set to Hi-Z on output disable 1 0: GTIOCnB pin is set to 0 on output disable 1 1: GTIOCnB pin is set to 1 on output disable	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFBEN	Noise Filter B Enable 0: The noise filter for the GTIOCnB pin is disabled 1: The noise filter for the GTIOCnB pin is enabled	R/W
31:30	NFCSB[1:0]	Noise Filter B Sampling Clock Select 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

The GTIOR sets the functions of the GTIOCnA and GTIOCnB pins.

GTIOA[4:0] bits (GTIOCnA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCnA pin function. For details, see Table 21.4.

OADFLT bit (GTIOCnA Pin Output Value Setting at the Count Stop)

The OADFLT bit sets whether the GTIOCnA pin outputs high or low when counting stops.

OAHLD bit (GTIOCnA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCnA pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OAHLD bit is set to 0:

- The value specified in bit [4] of the GTIOA[4:0] bits is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OAHLD bit is set to 1:

- The output is retained when counting starts or stops.

OAE bit (GTIOCnA Pin Output Enable)

The OAE bit disables or enables the GTIOCnA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCnA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCnA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of the GTIOCnA pin when an output disable request occurs.

Bit	Symbol	Function	R/W
22	OBDFLT	计数停止时GTIOCnB引脚输出值设置 0：计数停止时GTIOCnB引脚输出低电平1：计数停止时GTIOCnB引脚输出高电平	R/W
23	OBHLD	开始停止计数时的GTIOCnB引脚输出设置 0：GTIOCnB引脚在计数开始停止时的输出电平取决于寄存器设置 1：GTIOCnB引脚输出电平在计数开始停止时保持	R/W
24	OBE	GTIOCnB引脚输出使能 0：禁用输出1：启用输出	R/W
26:25	OBDF[1:0]	GTIOCnB引脚禁用值设置 00：禁止输出01：GTIOCnB引脚在输出禁止时设置为Hi-Z10：GTIOCnB引脚在输出禁止时设置为011：GTIOCnB引脚在输出禁止时设置为1	R/W
28:27	—	这些位被读取为0。写入值应为0。	R/W
29	NFBEN	噪声滤波器B启用 0：GTIOCnB引脚的噪声滤波器禁用1：GTIOCnB引脚的噪声滤波器启用	R/W
31:30	NFCSB[1:0]	噪声滤波器B采样时钟选择 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

GTIOR设置GTIOCnA和GTIOCnB引脚的功能。

GTIOA[4:0]位（GTIOCnA引脚功能选择）

GTIOA[4:0]位选择GTIOCnA引脚功能。详见表21.4。

OADFLT位（计数停止时的GTIOCnA引脚输出值设置）

OADFLT位设置当计数停止时GTIOCnA引脚输出高电平还是低电平。

OAHLD位（开始停止计数时的GTIOCnA引脚输出设置）

OAHLD位指定是保留GTIOCnA引脚输出电平还是计数开始或停止时的电平取决于寄存器设置。

当OAHLD位设置为0时：

- ●GTIOA[4:0]位的位[4]中指定的值在计数开始时输出
- ●计数停止时输出OADFLT位中指定的值
- ●如果在计数停止时修改OADFLT位，则新值会立即反映在输出中。

当OAHLD位设置为1时：

- ●计数开始或停止时保持输出。

OAE位（GTIOCnA引脚输出使能）

OAE位禁用或启用GTIOCnA引脚输出。

当GTCCRA寄存器用作输入捕捉寄存器时（GTICASR寄存器中至少有一位设置为1），无论OAE位值如何，GTIOCnA引脚都不输出。

OADF[1:0]位（GTIOCnA引脚禁用值设置）

当出现输出禁用请求时，OADF[1:0]位选择GTIOCnA引脚的输出值。

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCnA pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCnA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCnB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCnB pin function. For details, see Table 21.4.

OBDFLT bit (GTIOCnB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCnB pin outputs high or low when counting stops.

OBHLD bit (GTIOCnB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether theGTIOCnB pin output level is retained or the level at the start or stop of counting depends on the register setting.

When the OBHLD bit is set to 0:

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting stops, the new value is immediately reflected in the output.

When the OBHLD bit is set to 1:

- The output is retained when counting starts or stops.

OBE bit (GTIOCnB Pin Output Enable)

The OBE bit disables or enables the GTIOCnB pin output.

When GTCCRB register is used as the input capture register (at least one bit in the GTICBSR register is set to 1), the GTIOCnB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCnB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of the GTIOCnB pin, when an output disable request occurs.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCnB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCnB pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

NFAEN位（噪声滤波器A使能）

NFAEN位禁用或启用来自GTIOCnA引脚的输入的噪声滤波器。因为更改位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSA[1:0]位（噪声滤波器A采样时钟选择）

NFCSA[1:0]位设置GTIOCnA引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

GTIOB[4:0]位（GTIOCnB引脚功能选择）

GTIOB[4:0]位选择GTIOCnB引脚功能。详见表21.4。

OBDFLT位（计数停止时GTIOCnB引脚输出值设置）

OBDFLT位设置当计数停止时GTIOCnB引脚输出高电平还是低电平。

OBHLD位（GTIOCnB引脚输出设置在开始停止计数）

OBHLD位指定是保留GTIOCnB引脚输出电平还是计数开始或停止时的电平取决于寄存器设置。

当OBHLD位设置为0时：

●GTIOB[4:0]位的位[4]中指定的值在计数开始时输出

●计数停止时输出OBDFLT位中指定的值

●如果在计数停止时修改了OBDFLT位，则新值会立即反映在输出中。

当OBHLD位设置为1时：

●计数开始或停止时保持输出。

OBE位（GTIOCnB引脚输出使能）

OBE位禁用或启用GTIOCnB引脚输出。

当GTCCRB寄存器用作输入捕捉寄存器时（GTICBSR寄存器中至少有一位设置为1），
无论OBE位值如何，GTIOCnB引脚都不输出。

OBDF[1:0]位（GTIOCnB引脚禁用值设置）

当输出禁用请求发生时，OBDF[1:0]位选择GTIOCnB引脚的输出值。

NFBEN位（噪声滤波器B启用）

NFBEN位禁用或启用来自GTIOCnB引脚的输入的噪声滤波器。因为更改位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSB[1:0]位（噪声滤波器B采样时钟选择）

NFCSB[1:0]位设置GTIOCnB引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

Table 21.4 Settings of GTIOA[4:0] and GTIOB[4:0] bits

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1 *2 *3	b1, b0*2
0	0	0	0	0	Initial output is low	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	0	1	0			High output at GTCCRA/GTCCRB compare match
0	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	0	1	1	0			High output at GTCCRA/GTCCRB compare match
0	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	0	1	0			High output at GTCCRA/GTCCRB compare match
0	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
0	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
0	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
0	1	1	1	0			High output at GTCCRA/GTCCRB compare match
0	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	0	0	0	Initial output is high	Output retained at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	0	1	0			High output at GTCCRA/GTCCRB compare match
1	0	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	0	1	0	0		Low output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	0	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	0	1	1	0			High output at GTCCRA/GTCCRB compare match
1	0	1	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	0	0	0		High output at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	0	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	0	1	0			High output at GTCCRA/GTCCRB compare match
1	1	0	1	1			Output toggled at GTCCRA/GTCCRB compare match
1	1	1	0	0		Output toggled at cycle end	Output retained at GTCCRA/GTCCRB compare match
1	1	1	0	1			Low output at GTCCRA/GTCCRB compare match
1	1	1	1	0			High output at GTCCRA/GTCCRB compare match
1	1	1	1	1			Output toggled at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT changes from GTPR to 0 in up-counting) or underflow (GTCNT changes from 0 to GTPR in down-counting). The GTCNT counter is cleared for saw waves and for the trough (GTCNT changes from 0 to 1) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

Table 21.4 GTIOA[4:0]和GTIOB[4:0]位的设置

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2*1 *2 *3	b1, b0*2
0	0	0	0	0	初始输出低	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
0	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
0	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
0	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
0	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
0	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
0	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	0	0	0	初始输出高	输出在循环结束时保留	GTCCRAGTCCRB比较匹配时保留的输出
1	0	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	1	0	0		循环结束时输出低	GTCCRAGTCCRB比较匹配时保留的输出
1	0	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	0	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	0	0	0		循环结束时的高输出	GTCCRAGTCCRB比较匹配时保留的输出
1	1	0	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	0	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	1	0	0		输出在循环结束时切换	GTCCRAGTCCRB比较匹配时保留的输出
1	1	1	0	1			GTCCRAGTCCRB比较匹配时的低输出
1	1	1	1	0			GTCCRAGTCCRB比较匹配时的高输出
1	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出

注1.循环结束是指上溢（递增计数时GTCNT从GTPR变为0）或下溢（递减计数时GTCNT从0变为GTPR）。锯齿波和波谷（GTCNT从0变为1）的三角波清除GTCNT计数器。

注2.在比较匹配操作中，当一个周期结束的时序和GTCCRAGTCCRB比较匹配的时序相同时，在锯齿波PWM模式下，b3和b2设置优先，b1和b0设置优先在任何其他模式下都具有优先权。

注3.在GTUPSR或GTDNSR中至少一位设置为1的事件计数操作中，忽略b3和b2的设置。

21.2.15 GTINTAD : General PWM Timer Interrupt Output Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disable Source Select 0 0: Group A output disable request is selected 0 1: Group B output disable request is selected 1 0: Group C output disable request is selected 1 1: Group D output disable request is selected	R/W
28:26	—	These bits are read as 0. The write value should be 0.	R/W
29	GRPABH	Same Time Output Level High Disable Request Enable 0: Same time output level high disable request disabled 1: Same time output level high disable request enabled	R/W
30	GRPABL	Same Time Output Level Low Disable Request Enable 0: Same time output level low disable request disabled 1: Same time output level low disable request enabled	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The GTINTAD enables or disables interrupt requests and output disable requests.

GRP[1:0] bits (Output Disable Source Select)

The GRP[1:0] bits select the GTIOCnA pin and GTIOCnB pin output disable sources.

GTST.ODF shows the request of the output disable source group that is selected with the GRP[1:0] bits. Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE bits are 0.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables the output disable request when the GTIOCnA pin and GTIOCnB pin output 0 at the same time.

21.2.15 GTINTAD:通用PWM定时器中断输出设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	—	这些位被读取为0。写入值应为0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择A组输出禁用请求选择B组输出禁用请 0 1: 求选择C 组输出禁用请求选择D组输出禁用 1 0: 请求 1 1:	R/W
28:26	—	这些位被读取为0。写入值应为0。	R/W
29	GRPABH	同时输出电平高禁用请求启用 0：禁止同时输出电平高禁止请求1：允许同时输出电平高禁止请求	R/W
30	GRPABL	同时输出电平低禁用请求启用 0：禁止同时输出电平低禁止请求1：允许同时输出电平低禁止请求	R/W
31	—	该位读取为0。写入值应为0。	R/W

GTINTAD启用或禁用中断请求和输出禁用请求。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择GTIOCnA引脚和GTIOCnB引脚输出禁用源。

GTST.ODF显示了使用GRP[1:0]位选择的输出禁用源组的请求。当GTIOR.OAE和GTIOR.OBE位均为0时，设置GRP[1:0]位。

GRPABH位（同时输出电平高禁用请求启用）

GRPABH位允许或禁止GTIOCnA引脚和GTIOCnB引脚同时输出1时的输出禁止请求。

GRPABL位（同时输出电平低禁用请求启用）

当GTIOCnA引脚和GTIOCnB引脚同时输出0时，GRPABL位允许或禁止输出禁止请求。

21.2.16 GTST : General PWM Timer Status Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PCF	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	Input Capture/Compare Match Flag A 0: No input capture/compare match of GTCCRA is generated 1: An input capture/compare match of GTCCRA is generated	R/(W)*1
1	TCFB	Input Capture/Compare Match Flag B 0: No input capture/compare match of GTCCRB is generated 1: An input capture/compare match of GTCCRB is generated	R/(W)*1
2	TCFC	Input Compare Match Flag C 0: No compare match of GTCCRC is generated 1: A compare match of GTCCRC is generated	R/(W)*1
3	TCFD	Input Compare Match Flag D 0: No compare match of GTCCRD is generated 1: A compare match of GTCCRD is generated	R/(W)*1
4	TCFE	Input Compare Match Flag E 0: No compare match of GTCCRE is generated 1: A compare match of GTCCRE is generated	R/(W)*1
5	TCFF	Input Compare Match Flag F 0: No compare match of GTCCRF is generated 1: A compare match of GTCCRF is generated	R/(W)*1
6	TCFPO	Overflow Flag 0: No overflow (crest) occurred 1: An overflow (crest) occurred	R/(W)*1
7	TCFPU	Underflow Flag 0: No underflow (trough) occurred 1: An underflow (trough) occurred	R/(W)*1
14:8	—	These bits are read as 0. The write value should be 0.	R/W
15	TUCF	Count Direction Flag 0: GTCNT counter counts downward 1: GTCNT counter counts upward	R
23:16	—	These bits are read as 0. The write value should be 0.	R/W
24	ODF	Output Disable Flag 0: No output disable request is generated 1: An output disable request is generated	R
28:25	—	These bits are read as 0. The write value should be 0.	R/W
29	OABHF	Same Time Output Level High Flag 0: GTIOCnA pin and GTIOCnB pin do not output 1 at the same time 1: GTIOCnA pin and GTIOCnB pin output 1 at the same time	R
30	OABLF	Same Time Output Level Low Flag 0: GTIOCnA pin and GTIOCnB pin do not output 0 at the same time 1: GTIOCnA pin and GTIOCnB pin output 0 at the same time	R

21.2.16 GTST：通用PWM定时器状态寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PCF	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值：	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCFA	输入捕捉比较匹配标志A 0：不产生GTCCRA的输入捕捉比较匹配1：产生GTCCRA的输入捕捉比较匹配	R/(W)*1
1	TCFB	输入捕捉比较匹配标志B 0：不生成GTCCRB的输入捕捉比较匹配1：生成GTCCRB的输入捕捉比较匹配	R/(W)*1
2	TCFC	输入比较匹配标志C 0：没有生成GTCCRC的比较匹配1：生成了GTCCRC的比较匹配	R/(W)*1
3	TCFD	输入比较匹配标志D 0：不产生GTCCRD的比较匹配1：产生GTCCRD的比较匹配	R/(W)*1
4	TCFE	输入比较匹配标志E 0：不生成GTCCRE的比较匹配1：生成GTCCRE的比较匹配	R/(W)*1
5	TCFF	输入比较匹配标志F 0：不产生GTCCRF的比较匹配1：产生GTCCRF的比较匹配	R/(W)*1
6	TCFPO	溢出标志 0：未发生溢出（波峰）1：发生溢出（波峰）	R/(W)*1
7	TCFPU	Underflow Flag 0：未发生下溢（波谷）1：发生下溢（波谷）	R/(W)*1
14:8	—	这些位被读取为0。写入值应为0。	R/W
15	TUCF	计数方向标志 0：GTCNT计数器向下计数1：GTCNT计数器向上计数	R
23:16	—	这些位被读取为0。写入值应为0。	R/W
24	ODF	输出禁用标志 0：不产生输出禁止请求1：产生输出禁止请求	R
28:25	—	这些位被读取为0。写入值应为0。	R/W
29	OABHF	同时输出电平高标志 0：GTIOCnA管脚和GTIOCnB管脚不同时输出11：GTIOCnA管脚和GTIOCnB管脚同时输出1	R
30	OABLF	同时输出电平低标志 0：GTIOCnA管脚和GTIOCnB管脚不同时输出01：GTIOCnA管脚和GTIOCnB管脚同时输出0	R

RA生态工作室

Bit	Symbol	Function	R/W
31	PCF	Period Count Function Finish Flag 0: No period count function finish has occurred 1: A period count function finish has occurred	R/(W)*1

Note 1. Only 0 can be written to this bit. Do not write 1.

The GTST indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFA flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA, when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB, when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)

Bit	Symbol	Function	R/W
31	PCF	周期计数功能完成标志 0：未发生周期计数功能完成1：已发生周期计数功能完成	R/(W)*1

注1.该位只能写入0。不要写1。

GTST指示GPT的状态。

TCFA标志（输入捕捉比较匹配标志A）

TCFA标志指示GTCCRA的输入捕获或比较匹配的状态。

[Setting conditions]

●GTCNT=GTCCRA，当GTCCRA寄存器用作比较匹配寄存器时

●当GTCCRA寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRA。

[Clearing condition]

●0写入此标志。

TCFB标志（输入捕捉比较匹配标志B）

TCFB标志指示GTCCRB的输入捕获或比较匹配的状态。

[Setting conditions]

●GTCNT=GTCCRB，当GTCCRB寄存器用作比较匹配寄存器时

●当GTCCRB寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRB。

[Clearing condition]

●0写入此标志。

TCFC标志（输入比较匹配标志C）

TCFC标志指示GTCCRC比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRC.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=01b 10b 11b（GTCCRC执行缓冲操作）。

TCFD标志（输入比较匹配标志D）

TCFD标志指示GTCCRD比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRD.

[Clearing condition]

●0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)

- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR - 1) has occurred
- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this bit.

- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=10b 11b（GTCCRD执行缓冲操作）。

TCFE标志（输入比较匹配标志E）

TCFE标志指示GTCCRE比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRE.

[Clearing condition]

- 0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=01b 10b 11b（GTCCRE执行缓冲操作）。

TCFF标志（输入比较匹配标志F）

TCFF标志表示GTCCRF比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRF.

[Clearing condition]

- 0写入此标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (Triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=10b 11b（GTCCRF执行缓冲操作）。

TCFPO flag (Overflow Flag)

TCFPO标志指示何时发生溢出或波峰。

[Setting conditions]

- 在锯齿波模式下，发生溢出（GTCNT在递增计数中从GTPR变为0）
- 在三角波模式中，出现波峰（GTCNT从GTPR变为GTPR1）
- 在硬件源的计数中，发生了溢出（GTCNT在递增计数中从GTPR变为0）。

[Clearing condition]

- 0写入此标志。

TCFPU flag (Underflow Flag)

TCFPU标志指示何时发生下溢或波谷。

[Setting conditions]

- 在锯齿波模式下，发生下溢（GTCNT在向下计数中从0变为GTPR）
- 在三角波模式下，出现波峰（GTCNT从0变为1）
- 在硬件源计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

[Clearing condition]

- 0写入该位。

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and to 0 in down-counting.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits.

When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCnA pin and GTIOCnB pin output 1 at the same time.

When the GTIOCnA or GTIOCnB pin outputs 0, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to POEG as an output disable request.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCnA and GTIOCnB pins output 0 at the same time.

When the GTIOCnA pin or GTIOCnB pin outputs 1, this flag returns to 0. This flag is read only. Writing 0 to clear the flag is prohibited.

When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to POEG as an output disable request.

[Setting condition]

- The GTIOCnA and GTIOCnB pins output 0 at the same time when both OAE and OBE bits are set to 1.

[Clearing conditions]

- The GTIOCnA pin output value is different from the GTIOCnB pin output value when both OAE and OBE bits are set to 1
- The GTIOCnA and GTIOCnB pins output 1 at the same time when both OAE and OBE bits are set to 1
- Either the OAE bit or the OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flag are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. When the output disable state is active, a compare match is performed continuously in the GPT and the OABHF/OABLF flag is updated in association with the result of the compared value.

PCF flag (Period Count Function Finish Flag)

This bit is status flag of period count function finish.

[Setting condition]

- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1 at the end of cycle.
- The GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 0 at the count clock.

[Clearing condition]

TUCF标志（计数方向标志）

TUCF标志表示GTCNT的计数方向。在事件计数操作中，该标志在递增计数时设置为1，在递减计数时设置为0。

ODF标志（输出禁用标志）

ODF标志显示在GRP[1:0]位中选择的输出禁用源组的请求。

当输出禁用时，输出禁用控制不会在输出禁用请求被否定的同一周期内释放。它在下一个周期中发布。

OABHF标志（同时输出电平高标志）

OABHF标志表示GTIOCnA引脚和GTIOCnB引脚同时输出1。

当GTIOCnA或GTIOCnB引脚输出0时，该标志返回0。该标志为只读。禁止写入0清除标志。

当通过OABHF标志启用中断时(GTINTAD.GRPABH=1)，OABHF标志作为输出禁用请求输出到POEG。

[Setting condition]

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出1。

[Clearing conditions]

●当OAE和OBE位都设置为1时，GTIOCnA引脚输出值与GTIOCnB引脚输出值不同

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出0

●OAE位或OBE位设置为0。

OABLF标志（同时输出电平低标志）

OABLF标志表示GTIOCnA和GTIOCnB管脚同时输出0。

当GTIOCnA引脚或GTIOCnB引脚输出1时，该标志返回0。该标志为只读。禁止写入0清除标志。

当启用OABLF标志的中断时(GTINTAD.GRPABL=1)，OABLF标志作为输出禁用请求输出到POEG。

[Setting condition]

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB引脚同时输出0。

[Clearing conditions]

●当OAE和OBE位都设置为1时，GTIOCnA引脚输出值与GTIOCnB引脚输出值不同

●当OAE和OBE位都设置为1时，GTIOCnA和GTIOCnB管脚同时输出1

●OAE位或OBE位都设置为0。

生成OABHFOABLF标志的比较目标信号是比较匹配输出（PWM输出）信号，在它们被输出禁用功能屏蔽之前。
当输出禁用状态激活时，在GPT中连续执行比较匹配，并根据比较值的结果更新OABHFOABLF标志。

PCF标志（周期计数功能完成标志）

该位是周期计数功能完成的状态标志。

[Setting condition]

●GTPC.PCEN位为1，GTPC.PCNT计数器在周期结束时为1。

●GTPC.PCEN位为1，GTPC.PCNT计数器在计数时钟为0。

[Clearing condition]

- 0 is written to this bit.

21.2.17 GTBER : General PWM Timer Buffer Enable Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD1	BD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
1	BD1	GTPR Buffer Operation Disable 0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
17:16	CCRA[1:0]	GTCCRA Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔GTCCRC) Others: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	R/W
19:18	CCRB[1:0]	GTCCRB Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) Others: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	R/W
21:20	PR[1:0]	GTPR Buffer Operation 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) Others: Setting prohibited	R/W
22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	W
31:23	—	These bits are read as 0. The write value should be 0.	R/W

The GTBER register provides settings for the buffer operation and must be set while the GTCNT operation stops.

BD0 bit (GTCCR Buffer Operation Disable)

The BD0 bit disables the buffer operation using GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1 and when BD0 is set to 0, GTCCRB does not perform buffer operation. The GTCCRB register is automatically set to a compare match value for negative-phase waveform with dead time.

A value for the BD0 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDCE or GTSECR.SBDCD.

BD1 bit (GTPR Buffer Operation Disable)

The BD1 bit disables the buffer operation using GTPR and GTPBR combined.

A value for the BD1 bit in the channel related to the position of the bit written with 1 by the GTSECSR register can be set when 1 is written to the GTSECR.SBDPE or GTSECR.SBDPD.

●0写入该位。

21.2.17 GTBER:通用PWM定时器缓冲器使能寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD1	BD0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BD0	GTCCR缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
1	BD1	GTPR缓冲区操作禁用 0：启用缓冲操作1：禁用缓冲操作	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
17:16	CCRA[1:0]	GTCCRA缓冲区操作 00：无缓冲操作01：单缓冲操作（GTCCRA↔GTCCRC） 其他：双缓冲操作（GTCCRA↔GTCCRC↔GTCCRD）	R/W
19:18	CCRB[1:0]	GTCCRB缓冲区操作 00：无缓冲操作01：单缓冲操作（GTCCRB↔GTCCRE） 其他：双缓冲操作（GTCCRB↔GTCCRE↔GTCCRF）	R/W
21:20	PR[1:0]	GTPR缓冲区操作 00：无缓冲操作01：单缓冲操作（GTPBR→GTPR） 其他：禁止设置	R/W
22	CCRSWT	GTCCRA和GTCCRB强制缓冲区操作向该位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0。	W
31:23	—	这些位被读取为0。写入值应为0。	R/W

GTBER寄存器为缓冲区操作提供设置，并且必须在GTCNT操作停止时设置。

BD0位（GTCCR缓冲区操作禁用）

BD0位使用GTCCRA、GTCCRB、GTCCRC、GTCCRD、GTCCRE和GTCCRF组合禁用缓冲区操作。

当GTDTCR.TDE为1且BD0设置为0时，GTCCRB不执行缓冲操作。GTCCRB寄存器自动设置为带有死区时间的负相位波形的比较匹配值。

当向GTSECR.SBDCE或GTSECR.SBDCD写入1时，可以设置与由GTSECSR寄存器写入1的位的位置相关的通道中的BD0位的值。

BD1位（GTPR缓冲区操作禁用）

BD1位禁用使用GTPR和GTPBR组合的缓冲区操作。

当向GTSECR.SBDPE或GTSECR.SBDPD写入1时，可以设置与由GTSECSR寄存器写入1的位的位置相关的通道中的BD1位的值。

RA生态工作室

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set the buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set the buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When the buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.

The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set the buffer operation with GTPR and GTPBR combined.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the 1 is written. This bit is read as 0, and is valid only when counting is stopped with a compare match operation specified.

21.2.18 GTCNT : General PWM Timer Counter

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x48

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT is a 32-bit read/write counter for GPT32n (n = 0 to 3). For GPT16m (m = 4 to 9), GTCNT is a 16-bit register. GTCNT can only be written to after counting stops. For GPT16m (m = 4 to 9), the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.	R/W

21.2.19 GTCCRk : General PWM Timer Compare Capture Register k (k = A to F)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																													0
Bit field:																														
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

CCRA[1:0]位（GTCCRA缓冲区操作）

CCRA[1:0]位设置与GTCCRA、GTCCRC和GTCCRD组合的缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。

缓冲器操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（波谷64位传输）。

CCRB[1:0]位（GTCCRB缓冲区操作）

CCRB[1:0]位使用GTCCRB、GTCCRE和GTCCRF组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。

缓冲器操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（波谷64位传输）。

PR[1:0]位（GTPR缓冲区操作）

PR[1:0]位设置结合GTPR和GTPBR的缓冲区操作。

CCRSWT位（GTCCRA和GTCCRB强制缓冲操作）

向CCRSWT位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0，仅当计数停止并指定比较匹配操作时才有效。

21.2.18 GTCNT:通用PWM定时器计数器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x48

Bit position:	31																													0
Bit field:																														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	GTCNT是GPT32n（n=0到3）的32位读写计数器。对于GPT16m（m=4到9），GTCNT是一个16位寄存器。GTCNT只能在计数停止后写入。 对于GPT16m（m=4到9），用于访问32位单元的高16位始终被读取为0x0000，并且忽略写入这些位。GTCNT必须设置在0≤GTCNT≤GTPR的范围内。	R/W

21.2.19 GTCCRk:通用PWM定时器比较捕捉寄存器k(k=AtoF)

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x4C (GTCCRA)
0x50 (GTCCRB)
0x54 (GTCCRC)
0x58 (GTCCRE)
0x5C (GTCCRD)
0x60 (GTCCRF)

Bit position:	31																													0
Bit field:																														
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRk registers are read/write registers. The effective size of GTCCRk is the same as GTCNT (16- or 32-bit). If the effective size of GTCCRk is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. GTCCRA and GTCCRB are registers used for both output compare and input capture. GTCCRC and GTCCRE are compare match registers, and can also function as buffer registers for GTCCRA and GTCCRB. GTCCRD and GTCCRF are compare match registers, and can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

21.2.20 GTPR : General PWM Timer Cycle Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x64

Bit position:	31																													0
Bit field:																														
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR is a read/write register that sets the maximum count value of GTCNT. The effective size of GTPR is the same as GTCNT (16- or 32-bit). If the effective size of GTPR is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

21.2.21 GTPBR : General PWM Timer Cycle Setting Buffer Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x68

Bit position:	31																													0
Bit field:																														
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR is a read/write register that functions as a buffer register for GTPR. The effective size of GTPBR is the same as GTCNT (16- or 32-bit). If the effective size of GTPBR is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored.	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

Bit	Symbol	Function	R/W
31:0	n/a	GTCCRk寄存器是读写寄存器。GTCCRk的有效大小与GTCNT（16位或32位）。如果GTCCRk的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。GTCCRA和GTCCRB是用于输出比较和输入捕捉的寄存器。GTCCRC和GTCCRE是比较匹配寄存器，也可以作为GTCCRA和GTCCRB的缓冲寄存器。GTCCRD和GTCCRF是比较匹配寄存器，也可以作为GTCCRC和GTCCRE的缓冲寄存器（GTCCRA和GTCCRB的双缓冲寄存器）。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

21.2.20 GTPR：通用PWM定时器周期设置寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x64

Bit position:	31																													0
Bit field:																														
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPR是一个读写寄存器，设置GTCNT的最大计数值。GTPR的有效大小与GTCNT（16位或32位）相同。如果GTPR的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。对于锯齿波，(GTPR+1)的值就是周期。对于三角波，（GTPR值×2）的值就是周期。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

21.2.21 GTPBR:通用PWM定时器周期设置缓冲寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x68

Bit position:	31																													0
Bit field:																														
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTPBR是一个读写寄存器，用作GTPR的缓冲寄存器。GTPBR的有效大小与GTCNT（16位或32位）相同。如果GTPBR的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

21.2.22 GTDTCR : General PWM Timer Dead Time Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDE	Negative-Phase Waveform Setting 0: GTCCRB is set without using GTDVU 1: GTDVU sets the compare match value for negative-phase waveform with automatic dead time in GTCCRB	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. GPT has a dead time control function and the GTDVU register is used for setting dead time value.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU. When GTDVU is used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB:

- Triangle waves:
  Upper limit value: GTPR − 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode:
  Upper limit value: GTPR
  Lower limit value: 0.

21.2.23 GTDVU : General PWM Timer Dead Time Value Register U

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x8C

Bit position:	31																											0
Bit field:																												
Value after reset:*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.22 GTDTCR:通用PWM定时器死区时间控制寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x88

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TDE	负相位波形设置 0：不使用GTDVU设置GTCCRB1：GTDVU在GTCCRB中设置带自动死区时间的反相波形比较匹配值	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

GTDTCR可以自动设置带死区时间的负相位波形的比较匹配值。GPT具有死区时间控制功能，GTDVU寄存器用于设置死区时间值。

TDE位（负相位波形设置）

TDE位指定是否使用GTDVU。使用GTDVU时，通过正相波形的比较匹配值(GTCCRA)和死区时间值(GTDVU)获得的带死区时间的负相波形的比较匹配值自动设置在GTCCRB中。

TDE位设置在锯齿波PWM模式下被忽略，并且不会进行自动设置。

GTCCRB值是自动设置的，具有以下上下限值。如果得到的GTCCRB值不在上限或下限范围内，则在GTCCRB中设置以下限制值：

- Triangle waves:
  上限值：GTPR−1
  下限值：加1，减0

●锯波单发脉冲模式：上限值：
GTPR
下限值：0。

21.2.23 GTDVU:通用PWM定时器死区值寄存器U

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0x8C

Bit position:	31																											0
Bit field:																												
复位后的值：*1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
31:0	n/a	GTDVU is a read/write register that sets the dead time for generating PWM waveforms with dead time. The effective size of GTDVU is the same as GTCNT (16 or 32 bits). If the effective size of GTDVU is 16 bits, the upper 16 bits for access in a 32-bit unit are always read as 0x0000, and writing to these bits is ignored. Setting a GTDVU value greater than or equal to GTPR is prohibited. When using the automatic dead time setting function, do not set a value that makes a change point of the waveform exceeding the count period. The set value can be confirmed by reading from GTCCRB. When GTDVU is used, writing to GTCCRB is prohibited. When this register is set to 0, waveforms without dead time are output. While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, stop the GPT with the CST bit in the GTCR register.	R/W

Note 1. For GPT16m (m = 4 to 9), the value of the upper 16 bits after reset is 0x0000.

21.2.24 GTICLF : General PWM Timer Inter Channel Logical Operation Function Setting Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0xB8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ICLFA[2:0]	GTIOCnA Output Logical Operation Function Select 0 0 0: A (no delay) 0 0 1: NOT A (no delay) 0 1 0: C (1PCLKD delay) 0 1 1: NOT C (1PCLKD delay) 1 0 0: A AND C (1PCLKD delay)*2 1 0 1: A OR C (1PCLKD delay)*2 1 1 0: A EXOR C (1PCLKD delay)*2 1 1 1: A NOR C (1PCLKD delay)*2	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
9:4	ICLFSELC[5:0]	Inter Channel Signal C Select*1*2 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
31:0	n/a	GTDVU是一个读写寄存器，用于设置死区时间，以生成带死区时间的PWM波形。GTDVU的有效大小与GTCNT相同（16或32位）。如果GTDVU的有效大小为16位，则在32位单元中访问的高16位始终被读取为0x0000，并且忽略写入这些位。禁止将GTDVU值设置为大于或等于GTPR。使用自动死区时间设置功能时，请勿设置使波形变化点超过计数周期的值。设定值可以通过读取GTCCRB来确认。使用GTDVU时，禁止写入GTCCRB。当该寄存器设置为0时，输出无死区时间的波形。在GPT运行时，禁止更改GTDVU值。要将GTDVU更改为新值，请使用GTCR寄存器中的CST位停止GPT。	R/W

注1.对于GPT16m（m=4到9），复位后高16位的值为0x0000。

21.2.24 GTICLF:通用PWM定时器通道间逻辑运算功能设置 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0xB8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	ICLFSELD[5:0]						—	ICLFB[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ICLFSELC[5:0]						—	ICLFA[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ICLFA[2:0]	GTIOCnA输出逻辑运算功能选择 000：A（无延迟）001：NOTA（无延迟）010：C（1PCLKD延迟）011：NOTC（1PCLKD延迟）100：AANDC（1PCLKD延迟）*2 101：A OR C (1PCLKD delay)*2 110：A EXOR C (1PCLKD delay)*2 111：A NOR C (1PCLKD delay)*2	R/W
3	—	该位读取为0。写入值应为0。	R/W
9:4	ICLFSELC[5:0]	通道间信号C选择*1*2 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
18:16	ICLFB[2:0]	GTIOCnB Output Logical Operation Function Select 0 0 0: B (no delay) 0 0 1: NOT B (no delay) 0 1 0: D (1PCLKD delay) 0 1 1: NOT D (1PCLKD delay) 1 0 0: B AND D (1PCLKD delay)*3 1 0 1: B OR D (1PCLKD delay)*3 1 1 0: B EXOR D (1PCLKD delay)*3 1 1 1: B NOR D (1PCLKD delay)*3	R/W
19	—	This bit is read as 0. The write value should be 0.	R/W
25:20	ICLFSELD[5:0]	Inter Channel Signal D Select*1*3 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The signal before performing output disable control is selected.
Note 2. When channel's own GTIOCnA is selected, C is treated as "1".
Note 3. When channel's own GTIOCnB is selected, D is treated as "1".

The GTICLF register sets the logical operation function between compare match outputs. The logical operation is performed with the signals that the duty 0%/100% control is performed after compare match control. (The output disable control is performed with the signal after logical operation.)

Access in 8-bit units to GTICLF is prohibited.

ICLFm[2:0] bit (GTIOCm Output Logical Operation Function Select) (m = A, B)

These bits select the logical operation function between signals before performing output disable control for GTIOCm. To prevent hazard to the GPT output, the signal after logical operation is latched with PCLKD. After latching, the output disable control is performed. When the logical operation function which causes the delay of 1 PCLKD is selected, the output enable signal is also delayed with 1 PCLKD and input to the output disable control.

When the same signal to operate logical function AND, OR, EXOR and NOR is selected, one signal is treated as "1".

ICLFSELk[5:0] bit (Inter Channel Signal k Select) (k = C, D)

These bits select the signal k that the logical operation is performed with the signal before performing output disable control for GTIOCnm.

21.2.25 GTPC : General PWM Timer Period Count Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0, 1)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 6)

Offset address: 0xBC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PCNT[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
18:16	ICLFB[2:0]	GTIOCnB输出逻辑运算功能选择 000：B（无延迟）001：NOTB（无延迟）010：D（1PCLKD延迟）011：NOTD（1PCLKD延迟）100：BANDD（1PCLKD延迟）*3 1 0 1: B OR D (1PCLKD delay)*3 1 1 0: B EXOR D (1PCLKD delay)*3 1 1 1: B NOR D (1PCLKD delay)*3	R/W
19	—	该位读取为0。写入值应为0。	R/W
25:20	ICLFSELD[5:0]	通道间信号D选择*1*3 0x00: GTIOC0A 0x01: GTIOC0B 0x02: GTIOC1A 0x03: GTIOC1B 0x04: GTIOC2A 0x05: GTIOC2B 0x06: GTIOC3A 0x07: GTIOC3B 0x3E: GTIOC31A 0x3F: GTIOC31B	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

注1.选择执行输出禁用控制之前的信号。注意2.选择频道自己的GTIOCNA时，C将其视为"1"。注意3.选择频道自己的GTIOCNB时，D将视为"1"。

GTICLF寄存器设置比较匹配输出之间的逻辑运算功能。通过比较匹配控制后执行占空比0%100%控制的信号执行逻辑运算。（输出禁止控制是通过逻辑运算后的信号进行的。）

禁止以8位为单位访问GTICLF。

ICLFm[2:0]位（GTIOCm输出逻辑运算功能选择）（m=A B）

这些位在执行GTIOCm的输出禁用控制之前选择信号之间的逻辑运算功能。为防止对GPT输出造成危害，逻辑运算后的信号由PCLKD锁存。锁存后，执行输出禁用控制。Whenthelogicaloperationfunctionwhichcausesthedelayof1PCLKDisselected theoutputenablesignalisalsodelayedwith1PCLKDandinputtotheoutputdisablecontrol.

当相同的信号运行逻辑函数，或者选择exorand也没有选择时，一个信号被视为"1"。

ICLFSELk[5:0]位（通道间信号k选择）（k=C D）

这些位选择在执行GTIOCnm的输出禁用控制之前的信号执行逻辑运算的信号k。

21.2.25 GTPC：通用PWM定时器周期计数寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0, 1)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 6)

Offset address: 0xBC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	PCNT[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ASTP	—	—	—	—	—	—	—	PCEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PCEN	Period Count Function Enable 0: Period count function is disabled 1: Period count function is enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	ASTP	Automatic Stop Function Enable 0: Automatic stop function is disabled 1: Automatic stop function is enabled	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
27:16	PCNT[11:0]	Period Counter Counter for the number of period	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The GTPC register counts the number of period.

PCEN bit (Period Count Function Enable)

This bit enables or disables period count function.

Writing is available when counting is both in progress and stopped.

When 1 is written to either the GTSECR.SPCE bit or the GTSECR.SPCD bit, the value is simultaneously set to the PCEN bit in the channels set to 1 by the GTSECSR register.

ASTP bit (Automatic Stop Function Enable)

This bit enables or disables the GTCNT counter automatic stopping after finishing counting the number of period.

When the PCEN bis is 0, writing is available.

When the PCEN bit is 1, writing is disabled.

When the PCEN bit is 1, the ASTP bit is 1, and the PCNT counter is stopped at PCNT = 0, the GTCNT counter is also stopped. When the ASTP bit is 0, the GTCNT counter continues to count.

PCNT[11:0] bit (Period Counter)

This counter counts the number of period.

When the PCEN bis is 0, writing the number of period is available.

When the PCEN bit is 1, writing is disabled, and down-counting is performed at the end of period. In saw-wave mode, the end of period refers to overflow, underflow, or counter clearing. In triangle-wave mode, it refers to trough.

When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immediately after that.

Bit	Symbol	Function	R/W
0	PCEN	周期计数功能启用 0：周期计数功能无效1：周期计数功能有效	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	ASTP	自动停止功能启用 0：自动停机功能无效1：自动停机功能有效	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
27:16	PCNT[11:0]	周期计数器 周期数计数器	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

GTPC寄存器计算周期数。

PCEN位（周期计数功能使能）

该位启用或禁用周期计数功能。

当计数正在进行和停止时，可以写入。

当1写入GTSECR.SPCE位或GTSECR.SPCD位时，该值同时设置到由GTSECSR寄存器设置为1的通道中的PCEN位。

ASTP位（自动停止功能使能）

该位使能或禁止GTCNT计数器在完成周期数计数后自动停止。

当PCENbis为0时，可以写入。

当PCEN位为1时，禁止写入。

当PCEN位为1，ASTP位为1，PCNT计数器在PCNT=0时停止，GTCNT计数器也停止。当ASTP位为0时，GTCNT计数器继续计数。

PCNT[11:0] bit (Period Counter)

该计数器计算周期数。

当PCENbis为0时，可写入周期数。

当PCEN位为1时，写入被禁止，并且在周期结束时执行递减计数。在锯齿波模式下，周期结束是指上溢、下溢或计数器清零。在三角波模式中，它指的是波谷。

当PCNT计数器在周期结束时为1时，它变为0并停止计数。

当GTCNT计数器停止而周期计数功能使能时，PCNT计数器保持其值。当。。。的时候GTCNT计数器重新开始计数且PCEN位为1，PCNT计数器重新从保持值开始向下计数。

当PCEN位从0变为1且PCNT计数器为0且ASTP位为1时，GTCNT计数器立即在计数时钟处停止。

21.2.26 GTSECSR : General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0xD0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SECSEL9	SECSEL8	SECSEL7	SECSEL6	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SECSEL0	Channel 0 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
1	SECSEL1	Channel 1 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
2	SECSEL2	Channel 2 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
3	SECSEL3	Channel 3 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
4	SECSEL4	Channel 4 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
5	SECSEL5	Channel 5 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
6	SECSEL6	Channel 6 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
7	SECSEL7	Channel 7 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
8	SECSEL8	Channel 8 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
9	SECSEL9	Channel 9 Operation Enable Bit Simultaneous Control Channel Select 0: Disable simultaneous control 1: Enable simultaneous control	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

The GTSECSR register selects an intended channel for updating an operation enable bit by the GTSECR register. A bit position for the GTSECSR register indicates a channel number. The GTSECSR register of each channel is a common register, and writing 1 to a bit in the GTSECSR register in any channel and updating it changes a channel, related to the position of the bit written with 1 by the GTSECSR register, to be simultaneously controlled of the operation enable bit by the GTSECR register.

21.2.26 GTSECSR：通用PWM定时器操作使能位同时控制通道选择寄存器

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0xD0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SECSEL9	SECSEL8	SECSEL7	SECSEL6	SECSEL5	SECSEL4	SECSEL3	SECSEL2	SECSEL1	SECSEL0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SECSEL0	通道0操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
1	SECSEL1	通道1操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
2	SECSEL2	通道2操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
3	SECSEL3	通道3操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
4	SECSEL4	通道4操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
5	SECSEL5	通道5操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
6	SECSEL6	通道6操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
7	SECSEL7	通道7操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
8	SECSEL8	通道8操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
9	SECSEL9	通道9操作使能位同时控制通道选择 0：同时控制无效1：同时控制有效	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

GTSECSR寄存器通过GTSECR寄存器选择用于更新操作使能位的预期通道。GTSECSR寄存器的位位置表示通道号。每个通道的GTSECSR寄存器是一个公共寄存器，在任何通道的GTSECSR寄存器中写入1并更新它会改变一个通道，与GTSECSR寄存器写入1的位的位置有关，同时被控制GTSECR寄存器的操作使能位。

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The bit corresponding to channel which security attribution is configured as secure can be read by non-secure access but can not be written by non-secure access. For example, if GPT0 is configured as secure and other GPTs are configured as non-secure, the SECSEL0 bit can not be written by non-secure access to GPT1.GTSECSR register, and the simultaneous control status of GPT0 is not changed. When the GPT1.GTSECSR register is read by non-secure access in the same security configuratin as the previous example, the simultaneous control status of GPT0 (SECSEL0 bit) can be read.

Access in 8-bit or 16-bit units to GTSECSR is prohibited, and it should be accessed in 32-bit units.

SECSELn bit (Operation Enable Bit Simultaneous Control Channel Select) (n = 0 to 9)

This bit enables or disables the simultaneous control of operation enable in channel n.

When the bit is set to 1, the simultaneous control is enabled, and disabled when the bit is 0.

21.2.27 GTSECR : General PWM Timer Operation Enable Bit Simultaneous Control Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0xD4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	SPCD	—	—	—	—	—	—	—	SPCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SBDPD	SBDCD	—	—	—	—	—	—	SBDPE	SBDCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SBDCE	GTCCR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTCCR buffer operations 1: Enable GTCCR register buffer operations simultaneously	R/W
1	SBDPE	GTPR Register Buffer Operation Simultaneous Enable 0: Disable simultaneous enabling GTPR buffer operations 1: Enable GTPR register buffer operations simultaneously	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	SBDCD	GTCCR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTCCR buffer operations 1: Disable GTCCR register buffer operations simultaneously	R/W
9	SBDPD	GTPR Register Buffer Operation Simultaneous Disable 0: Disable simultaneous disabling GTPR buffer operations 1: Disable GTPR register buffer operations simultaneously	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	SPCE	Period Count Function Simultaneous Enable 0: Disable simultaneous enabling period count function 1: Enable period count function simultaneously	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
24	SPCD	Period Count Function Simultaneous Disable 0: Disable simultaneous disabling period count function 1: Disable period count function simultaneously	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The GTSECR register simultaneously updates the value for operation enable bits of a channel set by the GTSECSR register.

安全属性配置为安全的通道对应的位可以被非安全访问读取，但不能被非安全访问写入。例如，如果GPT0配置为安全，而其他GPT配置为非安全，则SECSEL0位不能通过对GPT1.GTSECSR寄存器的非安全访问来写入，并且GPT0的同时控制状态不会改变。当GPT1.GTSECSR寄存器通过与上例相同的安全配置中的非安全访问读取时，可以读取GPT0（SECSEL0位）的同时控制状态。

禁止以8位或16位为单位访问GTSECSR，应以32位为单位进行访问。

SECSELn位（操作使能位同时控制通道选择）（n=0至9）

该位启用或禁用通道n中操作启用的同时控制。

该位设置为1时启用同步控制，该位设置为0时禁用同步控制。

21.2.27 GTSECR：通用PWM定时器操作使能位同时控制 Register

Base address: GPT32n = 0x4016_9000 + 0x0100 × n (n = 0 to 3)
GPT16m = 0x4016_9000 + 0x0100 × m (m = 4 to 9)

Offset address: 0xD4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	SPCD	—	—	—	—	—	—	—	SPCE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SBDPD	SBDCD	—	—	—	—	—	—	SBDPE	SBDCE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SBDCE	GTCCR寄存器缓冲器操作同时使能 0：禁止同时使能GTCCR缓冲操作1：同时使能GTCCR寄存器缓冲操作	R/W
1	SBDPE	GTPR寄存器缓冲区操作同时使能 0：禁止同时使能GTPR缓冲区操作1：同时使能GTPR寄存器缓冲区操作	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	SBDCD	GTCCR寄存器缓冲区操作同时禁用 0：禁用同时禁用GTCCR缓冲区操作1：同时禁用GTCCR寄存器缓冲区操作	R/W
9	SBDPD	GTPR寄存器缓冲区操作同时禁用 0：禁用同时禁用GTPR缓冲区操作1：同时禁用GTPR寄存器缓冲区操作	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
16	SPCE	周期计数功能同时启用 0：禁用同时启用周期计数功能1：同时启用周期计数功能	R/W
23:17	—	这些位被读取为0。写入值应为0。	R/W
24	SPCD	期间计数功能同时禁用 0：禁用同时禁用周期计数功能1：同时禁用周期计数功能	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

GTSECR寄存器同时更新由GTSECSR寄存器设置的通道的操作使能位的值。

Writing 1 to a bit in the GTSECR register in any channel and updating it updates an operation enable bit for all channels, related to the position of the bit written with 1 by the all GTSECSR registers.

The GTSECR register of channel which security attribution is configured as secure can not be written by non-secure access. For example, if GPT0 is configured as secure and other GPTs are configured as non-secure, the GPT0.GTSECR register can not be written by non-secure access to GPT1.GTSECR register even if the simulataneous control of GPT0 is enabled, and the simultaneous control status of GPT0 is not changed.

Setting enable and disable bits for the same operation enable bit to 1 in the GTSECR is prohibited.

A bit written to 1 is automatically cleared. When the GTSECR is read, 0 is read.

Access in 8-bit or 16-bit units to the GTSECR register is prohibited, and it should be accessed in 32-bit units.

SBDCE bit (GTCCR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are enabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPE bit (GTPR Register Buffer Operation Simultaneous Enable)

When 1 is written to this bit, 0 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPBR, registers are enabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SBDCD bit (GTCCR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[0] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTCCRA, GTCCRC, and GTCCRD registers and using the GTCCRB, GTCCRE, and GTCCRF registers are disabled.

Simultaneous setting of SBDCE and SBDCD bits to 1 is prohibited.

SBDPD bit (GTPR Register Buffer Operation Simultaneous Disable)

When 1 is written to this bit, 1 is simultaneously set to a GTBER.BD[1] bit in the channels set to 1 by the GTSECSR register, and buffer operations using the GTPR, GTPBR, registers are disabled.

Simultaneous setting of SBDPE and SBDPD bits to 1 is prohibited.

SPCE bit (Period Count Function Simultaneous Enable)

When 1 is written to this bit, 1 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is enabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

SPCD bit (Period Count Function Simultaneous Disable)

When 1 is written to this bit, 0 is simultaneously set to GTPC.PCEN bit in the channels set to 1 by the GTSECSR register, and period count function is disabled.

Simultaneous setting of SPCE and SPCD bits to 1 is prohibited.

将1写入任何通道的GTSECR寄存器中的位并更新它会更新所有通道的操作使能位，这与所有GTSECSR寄存器写入1的位的位置有关。

安全属性配置为安全的通道的GTSECR寄存器不能被非安全访问写入。例如，如果GPT0配置为安全，而其他GPT配置为非安全，则即使GPT0的同时控制使能，也不能通过非安全访问GPT1.GTSECR寄存器来写入GPT0.GTSECR寄存器，并且GPT0的同时控制状态不变。

禁止在GTSECR中将同一操作使能位的使能位和禁用位设置为1。

写入1的位会自动清除。读取GTSECR时，读取0。

禁止以8位或16位为单位访问GTSECR寄存器，应以32位为单位进行访问。

SBDCE位（GTCCR寄存器缓冲区操作同时使能）

向该位写入1时，通过GTSECSR寄存器设置为1的通道中的GTBER.BD[0]位同时设置为0，并且使用GTCCRA、GTCCRC和GTCCRD寄存器以及使用GTCCRB、GTCCRE进行缓冲操作 和GTCCRF寄存器被启用。

禁止将SBDCE和SBDCD位同时设置为1。

SBDPE位（GTPR寄存器缓冲区操作同时使能）

向该位写入1时，同时将GTSECSR寄存器设置为1的通道中的GTBER.BD[1]位设置为0，并启用使用GTPR、GTPBR寄存器的缓冲操作。

禁止将SBDPE和SBDPD位同时设置为1。

SBDCD位（GTCCR寄存器缓冲区操作同时禁用）

当向该位写入1时，同时将1设置为由GTSECSR寄存器设置为1的通道中的GTBER.BD[0]位，并使用GTCCRA、GTCCRC和GTCCRD寄存器以及使用GTCCRB、GTCCRE进行缓冲操作 和GTCCRF寄存器被禁用。

禁止将SBDCE和SBDCD位同时设置为1。

SBDPD位（GTPR寄存器缓冲区操作同时禁用）

当向该位写入1时，同时将1设置到由GTSECSR寄存器设置为1的通道中的GTBER.BD[1]位，并且使用GTPR、GTPBR寄存器的缓冲操作被禁用。

禁止将SBDPE和SBDPD位同时设置为1。

SPCE位（周期计数功能同时使能）

向该位写入1时，通过GTSECSR寄存器设置为1的通道中的GTPC.PCEN位同时设置为1，并启用周期计数功能。

禁止将SPCE和SPCD位同时设置为1。

SPCD位（周期计数功能同时禁用）

向该位写入1时，通过GTSECSR寄存器设置为1的通道中的GTPC.PCEN位同时设置为0，并且禁用周期计数功能。

禁止将SPCE和SPCD位同时设置为1。

21.2.28 OPSCR : Output Phase Switching Control Register

Base address: GPT_OPS = 0x4016_9A00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	Input Phase Soft Setting These bits set the input phase from software settings. Setting these bits is valid when OPSCR.FB = 1.	R/W
1	VF		R/W
2	WF		R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	U	Input U-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (UF)	R
5	V	Input V-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (VF)	R
6	W	Input W-Phase Monitor This bit monitors the state of the input phase. OPSCR.FB = 0 : External input that are synchronized by PCLKD OPSCR.FB = 1 : Software settings (WF)	R
7	—	This bit is read as 0. The write value should be 0.	R/W
8	EN	Enable Pahse Output Control 0: Do not output (Hi-Z external pin) 1: Output*1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	FB	External Feedback Signal Enable This bit selects the input phase from software settings and external input. 0: Select the external input 1: Select the soft setting (OPSCR.UF, VF, WF)	R/W
17	P	Positive-Phase Output (P) Control 0: Level signal output 1: PWM signal output (PWM of GPT320)	R/W
18	N	Negative-Phase Output (N) Control 0: Level signal output 1: PWM signal output (PWM of GPT320)	R/W
19	INV	Invert Phase Output Control 0: Positive logic (active-high) output 1: Negative logic (active-low) output	R/W
20	RV	Output Phase Rotation Direction Reversal Control 0: Positive rotation 1: Reverse rotation	R/W
21	ALIGN	Input Phase Alignment 0: Input phase aligned to PCLKD 1: Input phase aligned to PWM	R/W

21.2.28 OPSCR：输出相位切换控制寄存器

Base address: GPT_OPS = 0x4016_9A00

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	RV	INV	N	P	FB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	UF	输入相位软设置 这些位通过软件设置设置输入相位。 当OPSCR.FB=1时，设置这些位有效。	R/W
1	VF		R/W
2	WF		R/W
3	—	该位读取为0。写入值应为0。	R/W
4	U	输入U相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由PCLKD同步的外部输入 OPSCR.FB=1：软件设置（UF）	R
5	V	输入V相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由PCLKD同步的外部输入 OPSCR.FB=1：软件设置（VF）	R
6	W	输入W相监视器 该位监控输入相位的状态。 OPSCR.FB=0：由PCLKD同步的外部输入 OPSCR.FB=1：软件设置（WF）	R
7	—	该位读取为0。写入值应为0。	R/W
8	EN	启用相位输出控制 0：不输出（Hi-Z外部引脚）1：输出*1	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	FB	外部反馈信号使能 该位从软件设置和外部输入中选择输入相位。 0：选择外部输入1：选择软设置（OPSCR.UF、VF、WF）	R/W
17	P	正相输出(P)控制 0：电平信号输出1：PWM信号输出（GPT320的PWM）	R/W
18	N	负相输出(N)控制 0：电平信号输出1：PWM信号输出（GPT320的PWM）	R/W
19	INV	反相输出控制 0：正逻辑（高电平有效）输出1：负逻辑（低电平有效）输出	R/W
20	RV	输出相位旋转方向反转控制 0：正转1：反转	R/W
21	ALIGN	输入相位对齐 0：输入相位与PCLKD对齐1：输入相位与PWM对齐	R/W

RA生态工作室

Bit	Symbol	Function	R/W
23:22	—	These bits are read as 0. The write value should be 0.	R/W
25:24	GRP[1:0]	Output Disabled Source Selection 0 0: Select group A output disable source 0 1: Select group B output disable source 1 0: Select group C output disable source 1 1: Select group D output disable source	R/W
26	GODF	Group Output Disable Function 0: This bit function is ignored 1: Group disable clears the OPSCR.EN bit*1	R/W
28:27	—	These bits are read as 0. The write value should be 0.	R/W
29	NFEN	External Input Noise Filter Enable 0: Do not use a noise filter on the external input 1: Use a noise filter on the external input	R/W
31:30	NFCS[1:0]	External Input Noise Filter Clock Selection Noise filter sampling clock setting of the external input. 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF , VF , WF bits (Input Phase Soft Setting)

The UF , VF , WF bits set the input phase from the software settings. When OPSCR.FB bit is 1, these bits are valid. The set value of the UF /VF /WF takes the place of the U/V/W external input.

U, V, W bits (Input Phase Monitor)

When the OPSCR.FB bit is 0, external inputs that are synchronized by PCLKD are monitored by these bits. When the OPSCR.FB bit is 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF , OPSCR.VF , and OPSCR.WF bits.

EN bit (Enable Pahse Output Control)

The EN bit controls the output enable signal output phase (positive phase/reverse phase).

When the OPSCR.EN bit is 1, the signal waveform is output.

When the OPSCR.EN bit is 0, first set OPSCR.FB, OPSCR.UF /VF /WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP[1:0], OPSCR.GODF, OPSCR.NFEN, OPSCR.NFCS. Then, set the bit to 1. Also when OPSCR.GODF is 1 and the signal value selected in the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects one of the level signal output or PWM signal output (PWM of GPT320) for the positive-phase output (GTOUUP pin, GTOVUP pin, GTOWUP pin).

N bit (Negative-Phase Output (N) Control)

The N bit selects one of the level signal output or PWM signal output (PWM of GPT320) for the negative-phase output (GTOULO pin, GTOVLO pin, GTOWLO pin).

INV bit (Invert Phase Output Control)

The INV bit selects one of the positive logic (active-high) output or negative logic (active-low) output for the output phase.

Bit	Symbol	Function	R/W
23:22	—	这些位被读取为0。写入值应为0。	R/W
25:24	GRP[1:0]	输出禁用源选择 0 0: 选择A组输出禁用源选择B组输出禁用 0 1: 源选择C 组输出禁用源选择D组输出禁 1 0: 用源 1 1:	R/W
26	GODF	组输出禁用功能 0：忽略该位功能1：组禁止清除OPSCR.EN位* 1	R/W
28:27	—	这些位被读取为0。写入值应为0。	R/W
29	NFEN	外部输入噪声滤波器启用 0：外部输入不使用噪声滤波器1：外部输入使用 噪声滤波器	R/W
31:30	NFCS[1:0]	外部输入噪声滤波器时钟选择 外部输入的噪声滤波器采样时钟设置。 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64	R/W

注1.当OPSCR.GODF=1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

OPSCR寄存器设置无刷直流电机控制所需的信号波形输出。

UF VF WF位（输入相位软设置）

UF、VF、WF位从软件设置中设置输入相位。当OPSCR.FB位为1时，这些位有效。UFVFWF的设定值代替了UVW外部输入。

U、V、W位（输入相位监视器）

当OPSCR.FB位为0时，由PCLKD同步的外部输入由这些位监控。当。。。的时候
OPSCR.FB位为1，OPSCR.U、OPSCR.V和OPSCR.W位可以读取OPSCR.UF、OPSCR.VF和OPSCR.WF位。

EN位（启用相位输出控制）

EN位控制输出使能信号的输出相位（正相反相）。

当OPSCR.EN位为1时，输出信号波形。

当OPSCR.EN位为0时，先设置OPSCR.FB、OPSCR.UFVFWF（选择软件设置）、OPSCR.PN、OPSCR.INV、OPSCR.RV、OPSCR.ALIGN、OPSCR.GRP[1:0]、OPSCR.GODF、OPSCR.NFEN、OPSCR.NFCS。然后，将该位设置为1。同样，当OPSCR.GODF为1且在OPSCR.GRP[1:0]位中选择的信号值为高时，OPSCR.EN位设置为0。

FB位（外部反馈信号使能）

FB位从软件设置（OPSCR.UF、VF、WF）和霍尔元件等外部输入中选择输入相位。

P位（正相输出(P)控制）

P位选择电平信号输出或PWM信号输出（GPT320的PWM）之一作为正相输出（GTOUUP引脚、GTOVUP引脚、GTOWUP引脚）。

N位（负相输出(N)控制）

N位选择电平信号输出或PWM信号输出（GPT320的PWM）之一作为负相输出（GTOULO引脚、GTOVLO引脚、GTOWLO引脚）。

INV位（反相输出控制）

INV位选择输出相位的正逻辑（高电平有效）输出或负逻辑（低电平有效）输出之一。

RV bit (Output Phase Rotation Direction Reversal Control)

The RV bit reverses the direction of rotation of the motor by inverting the input phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects the PCLKD or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit).

When OPSCR.ALIGN bit is 0, input phase is aligned to PCLKD.

Note: When PWM output is selected (OPSCR.P/N is 1) and the PCLKD input phase is aligned, the PWM pulse can be short-pulsed.

When OPSCR.ALIGN bit is 1, input phase is aligned with PWM output.

GRP[1:0] bit (Output Disabled Source Selection)

The GRP[1:0] bit selects the output disable source.

The GRP bits should be set when GODF bit is 0. If GRP bits select a POEG except for the connected groups, the status of output pin never change to disable.

GODF bit (Group Output Disable Function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP[1:0] bit is high, the OPSCR.EN bit is set to 0.

When OPSCR.GODF bit is 0, this bit is ignored.

The GODF bit should be set when output disable request doesn't occur from POEG.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input. When OPSCR.NFEN bit is 0, a noise filter for the external input is not used.

Note: Please set this bit during the EN bit is 0 to avoid generation of unintentional internal edge caused by switching this bit.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit is 1, noise filter sampling clock setting of the external input is enabled.

1. Set the NFCS[1:0].
2. Wait for 2 cycles.
3. Set the OPSCR.EN bit to 1.

21.3 Operation

21.3.1 Basic Operation

Each channel has a 32-bit and 16-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR controls the count cycle.

When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated GTIOCnA or GTIOCnB can be changed (n = 0 to 9) . GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

21.3.1.1 Counter operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1, and stops counting when the bit is set to 0. The GTCR.CST bit value is changed by the following sources:

RV位（输出相位旋转方向反转控制）

RV位通过反转输入相位来反转电机的旋转方向。

ALIGN位（输入相位对齐）

ALIGN位选择PCLKD或PWM对输入相位进行采样（输入相位在OPSCR.FB位中指定）。

当OPSCR.ALIGN位为0时，输入相位与PCLKD对齐。

Note: WhenPWMoutputisselected(OPSCR.PNis1)andthePCLKDinputphaseisaligned thePWMpulsecanbeshort-pulsed.

当OPSCR.ALIGN位为1时，输入相位与PWM输出对齐。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择输出禁用源。

当GODF位为0时，应设置GRP位。如果GRP位选择除连接组以外的POEG，则输出引脚的状态永远不会变为禁用。

GODF位（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP[1:0]位选择的信号值为高时，OPSCR.EN位设置为0。

当OPSCR.GODF位为0时，该位被忽略。

当POEG没有出现输出禁用请求时，应该设置GODF位。

NFEN位（外部输入噪声滤波器使能）

NFEN位选择外部输入的噪声滤波器。当OPSCR.NFEN位为0时，不使用外部输入的噪声滤波器。

Note: 请在EN位为0期间设置该位，以避免因切换该位而产生意外的内部边沿。

NFCS[1:0]位（外部输入噪声滤波器时钟选择）

NFCS[1:0]位选择外部输入噪声滤波器的时钟。当OPSCR.NFEN位为1时，使能外部输入的噪声滤波器采样时钟设置。

1.设置NFCS[1:0]。

2.等待2个周期。

3.将OPSCR.EN位设置为1。

21.3 Operation

21.3.1 基本操作

每个通道都有一个32位和16位定时器，它们使用计数时钟和硬件源执行周期性计数操作。计数功能提供向上计数和向下计数。GTPR控制计数周期。

当GTCNT计数器值与GTCCRA或GTCCRB中的值匹配时，相关GTIOCnA或GTIOCnB可以更改（n=0到9）。GTCCRA或GTCCRB可用作具有硬件资源的输入捕捉寄存器。

GTCCRC和GTCCRD可以作为GTCCRA的缓冲寄存器。GTCCRE和GTCCRF可以作为GTCCRB的缓冲寄存器。

21.3.1.1 计数器操作

(1) 计数器启动和停止

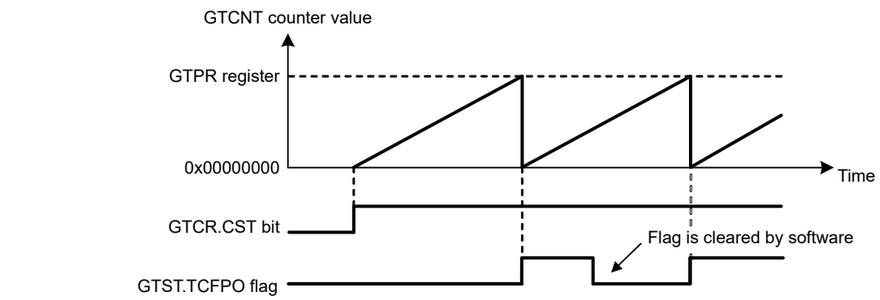
当GTCR.CST设置为1时，每个通道的计数器开始计数操作，并在该位设置为0时停止计数。GTCR.CST位值由以下来源改变：

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.
- Completion of the period count function while the GTPC.ASTP bit is 1.

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with GTUPSR and GTDNSR registers set to 0x00000000. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set set to 1, and the overflow interrupt(GPTn_OVF) is also generated. After GTCNT overflows, up-counting resumes from 0x00000000.

Figure 21.3 shows an example of a periodic count operation in up-counting by the count clock.



Note: The base address of registers are the same.

Figure 21.3 Example of periodic count operation in up-counting by the count clock

Table 21.5 shows an example for setting periodic count operation in up-counting by the count clock.

Table 21.5 Example for setting a periodic count operation in up-counting by the count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.3, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.3, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.3, 0x00000000 is set.
6	Start count operation	Set GTCR.CST to 1 to start count operation.

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with GTUPSR and GTDNSR registers set to 0x00000000. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1, and the underflow interrupt(GPTn_UDF) is also generated. After the GTCNT counter underflows, down-counting resumes from the GTPR value.

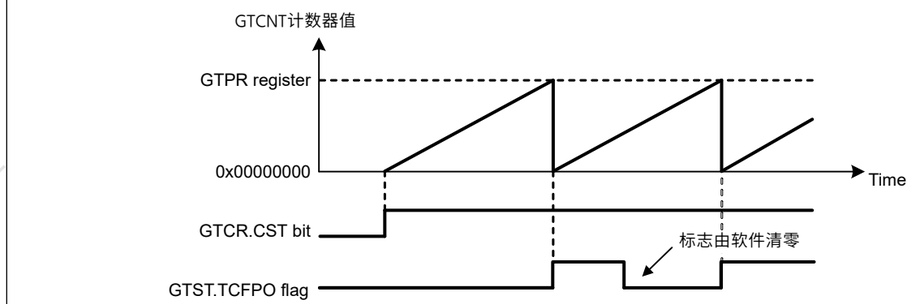
Figure 21.4 shows an example of periodic count operation in down-counting by the count clock.

●写入GTCR寄存器
●当GTSSR.CSTRT位设置为1时，将1写入GTSTR中与GPT通道号相关的位
●当GTPSR.CSTOP位设置为1时，将1写入GTSTP中与GPT通道号相关的位
●GTSSR寄存器中选择的硬件源
●GTPSR寄存器中选择的硬件源。
●GTPC.ASTP位为1时完成周期计数功能。

(2) 计数时钟递增计数中的周期计数操作

当相关的GTCR.CST位设置为1且GTUPSR和GTDNSR寄存器设置为0x00000000时，每个通道中的GTCNT计数器开始向上计数。当GTCNT值从GTPR值变为0（溢出）时，
GTST.TCFPO标志设置为1，并且溢出中断（GPTn_OVF）也产生。GTCNT溢出后，向上计数从0x00000000重新开始。

图21.3显示了计数时钟递增计数中的周期性计数操作的示例。



Note: 寄存器的基地址相同。

Figure 21.3 计数时钟递增计数中的周期计数操作示例

表21.5显示了在计数时钟递增计数中设置周期性计数操作的示例。

Table 21.5 使用计数时钟在递增计数中设置周期性计数操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.3中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.3中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。在图21.3中，设置了0x00000000。
6	开始计数操作	将GTCR.CST设置为1以启动计数操作。

(3) 计数时钟递减计数中的周期计数操作

每个通道中的GTCNT计数器可以通过使用GTUPSR设置GTUDDTYC.UD和
GTDNSR寄存器设置为0x00000000。当GTCNT从0变为GTPR值（下溢）时，GTST.TCFPU置1，同时产生下溢中断（GPTn_UDF）。GTCNT计数器下溢后，从GTPR值开始向下计数。

图21.4显示了计数时钟递减计数中周期性计数操作的示例。

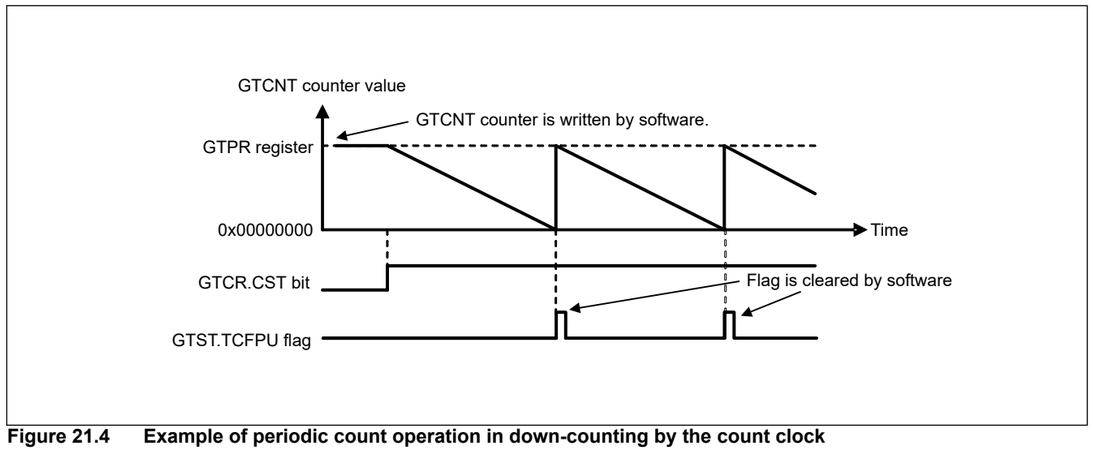


Figure 21.4 Example of periodic count operation in down-counting by the count clock

Table 21.6 shows an example for setting periodic count operation in down-counting by the count clock.

Table 21.6 Example for setting periodic count operation in down-counting by count clock

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.4, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction with the GTUDDTYC register. In Figure 21.4, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.4, the GTPR value is set.
6	Start count operation	Set GTCR.CST to 1 to start count operation.

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior when up-counting using hardware sources is the same as when up-counting by the count clock.

When GTCR.CST bit is set to 1 to count up using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized by the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count up with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 21.5 shows an example of an event count operation in up-counting by a hardware resource (the rising edge of GTETRGA pin input).

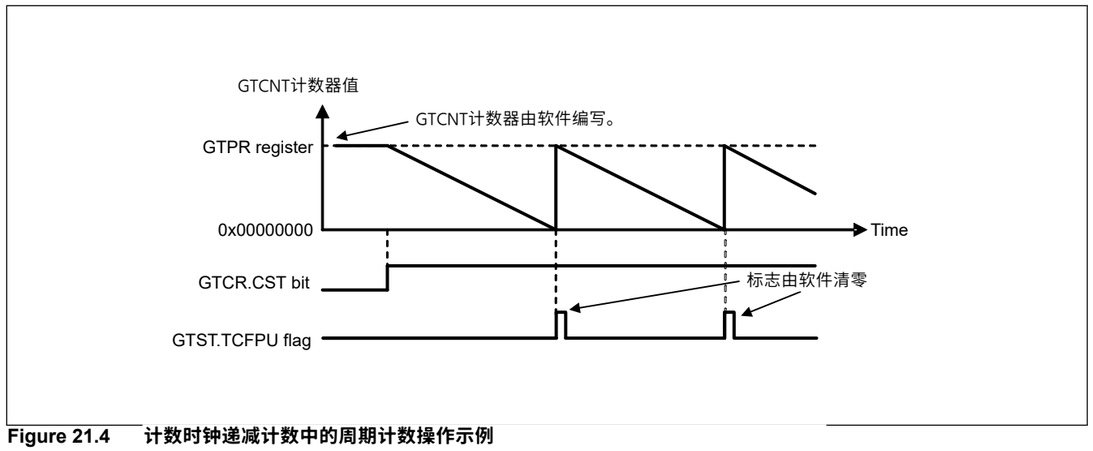


Figure 21.4 计数时钟递减计数中的周期计数操作示例

表21.6显示了在计数时钟的递减计数中设置周期性计数操作的示例。

Table 21.6 计数时钟递减计数中设置周期计数操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.4中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向。 在图21.4中，在GTUDDTYC[1:0]中设置10b后，在GTUDDTYC[1:0]中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.4中，设置了GTPR值。
6	开始计数操作	将GTCR.CST设置为1以启动计数操作。

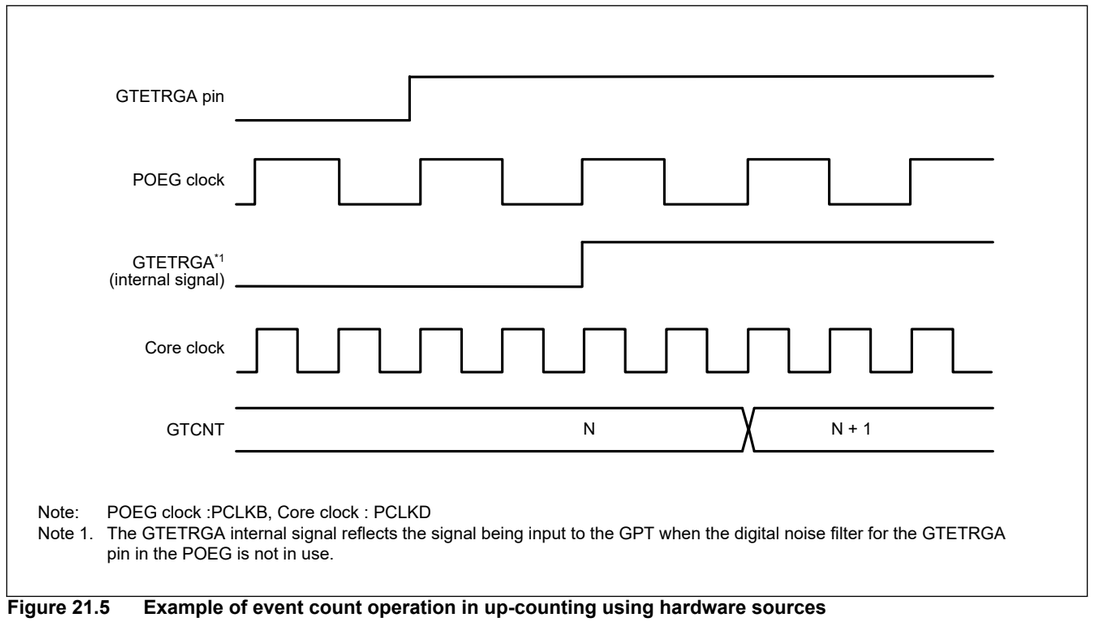
(4) 使用硬件源的递增计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTUPSR中设置的硬件源执行递增计数。

当GTUPSR设置为使能时，在GTCR.TPCS[3:0]中选择的计数时钟和在
GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则
GTCNT计数器值不会改变。使用硬件源递增计数时的溢出行为与使用计数时钟递增计数时的溢出行为相同。

当GTCR.CST位设置为1以使用硬件源进行计数时，计数操作被启用。GTCR.CST设置为1后，计数器无法按GTCR.TPCS[3:0]中指定的1个时钟周期向上计数，因为计数操作与GTCR.TPCS[3:0]中选择的计数时钟同步。将GTCR.TPCS[3:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟向上计数。

图21.5显示了一个硬件资源递增计数中的事件计数操作示例（上升沿
GTETRGA pin input).



Note: POEG clock :PCLKB, Core clock : PCLKD
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 21.5 Example of event count operation in up-counting using hardware sources

Table 21.7 shows an example for setting event count operation in up-counting by a hardware source.

Table 21.7 Example for setting an event count operation in up-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-up source with the GTUPSR register.
2	Set cycle	Set the cycle in GTPR.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set GTCR.CST to 1 to start count operation.

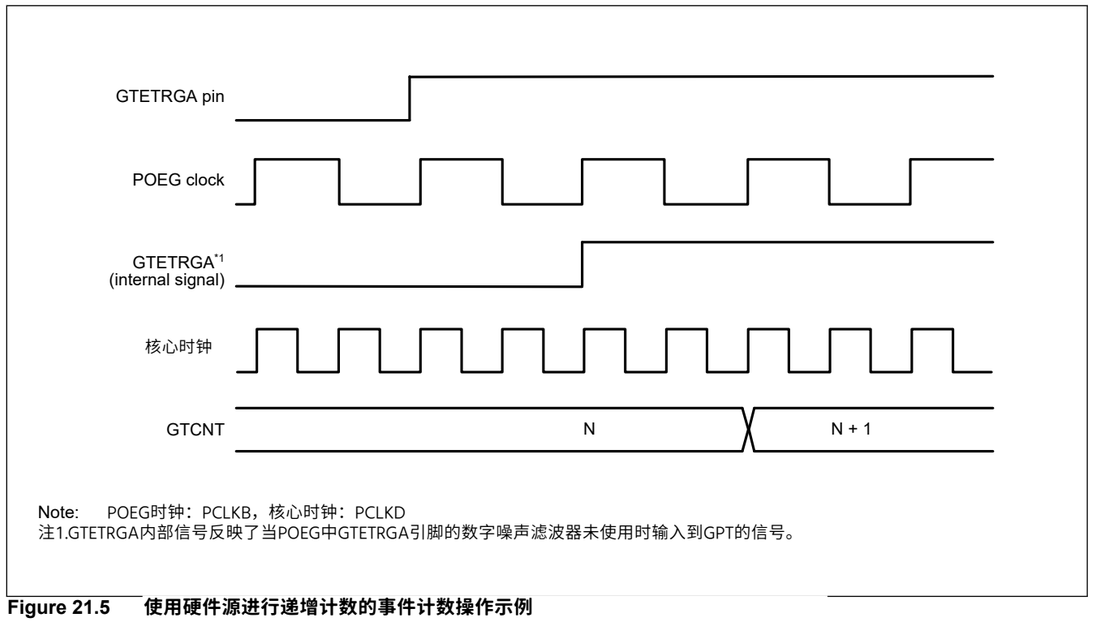
(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[3:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The underflow behavior when down-counting using hardware sources is the same as when down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[3:0] because the count operation is synchronized with the count clock selected in GTCR.TPCS[3:0]. Set GTCR.TPCS[3:0] to 000b to count down with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 21.6 shows an example of a event count operation in down-counting by a hardware resource (rising edge of GTETRGA pin).



Note: POEG时钟：PCLKB，核心时钟：PCLKD
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.5 使用硬件源进行递增计数的事件计数操作示例

表21.7显示了通过硬件源在递增计数中设置事件计数操作的示例。

Table 21.7 使用硬件源在递增计数中设置事件计数操作的示例

No.	步骤名称	Description
1	设置计数源	使用GTUPSR寄存器选择递增计数源。
2	设置周期	在GTPR中设置循环。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	开始计数操作	将GTCR.CST设置为1以启动计数操作。

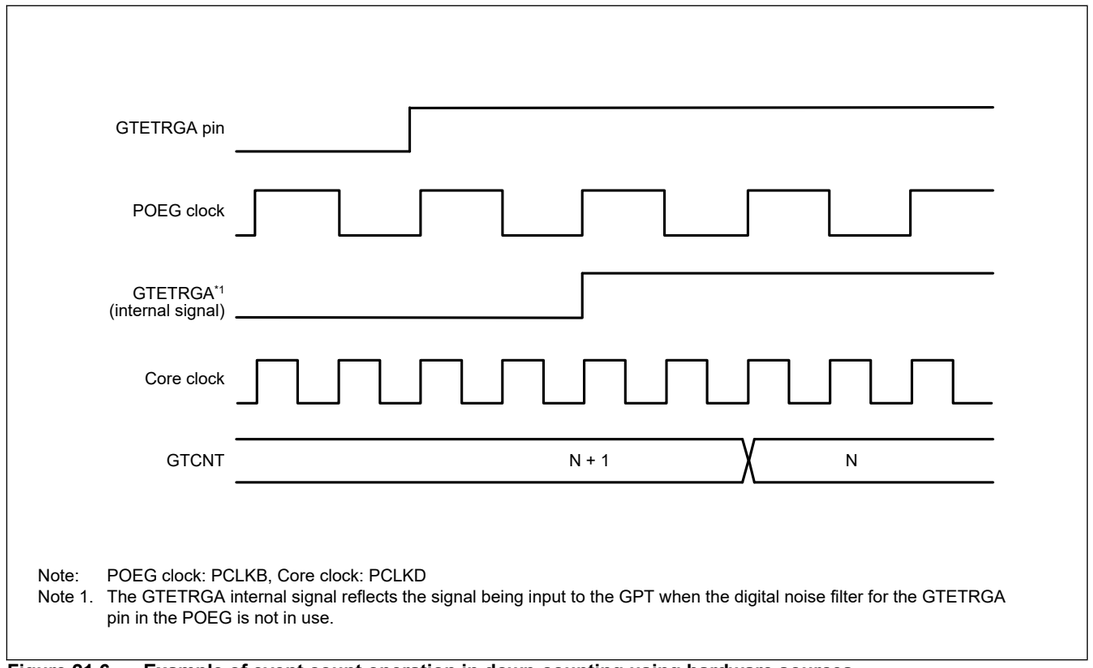
(5) 使用硬件源的递减计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTDNSR中设置的硬件源进行递减计数。

当GTDNSR设置为使能时，在GTCR.TPCS[3:0]中选择的计数时钟和在
GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则
GTCNT计数器值不会改变。使用硬件源向下计数时的下溢行为与使用计数时钟向下计数时相同。

当GTCR.CST位设置为1以使用硬件源进行递减计数时，启用计数操作。在GTCR.CST设置为1后，计数器无法按照GTCR.TPCS[3:0]中的规定向下计数1个时钟周期，因为计数操作与GTCR.TPCS[3:0]中选择的计数时钟同步。将GTCR.TPCS[3:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟递减计数。

图21.6显示了一个事件计数操作的例子，通过硬件资源进行递减计数（上升沿
GTETRGA pin).



Note: POEG clock: PCLKB, Core clock: PCLKD
Note 1. The GTETRGA internal signal reflects the signal being input to the GPT when the digital noise filter for the GTETRGA pin in the POEG is not in use.

Figure 21.6 Example of event count operation in down-counting using hardware sources

Table 21.8 shows an example for setting a periodic count operation in down-counting using a hardware resource.

Table 21.8 Example for setting an event count operation in down-counting using hardware sources

No.	Step Name	Description
1	Set count source	Select the counting-down source with the GTDNSR register.
2	Set cycle	Set the cycle in GTPR.
3	Set initial value for counter	Set the initial value in the GTCNT counter.
4	Start count operation	Set GTCR.CST to 1 to start count operation.

(6) Counter clear operation

The counter of each channel is cleared by following sources:

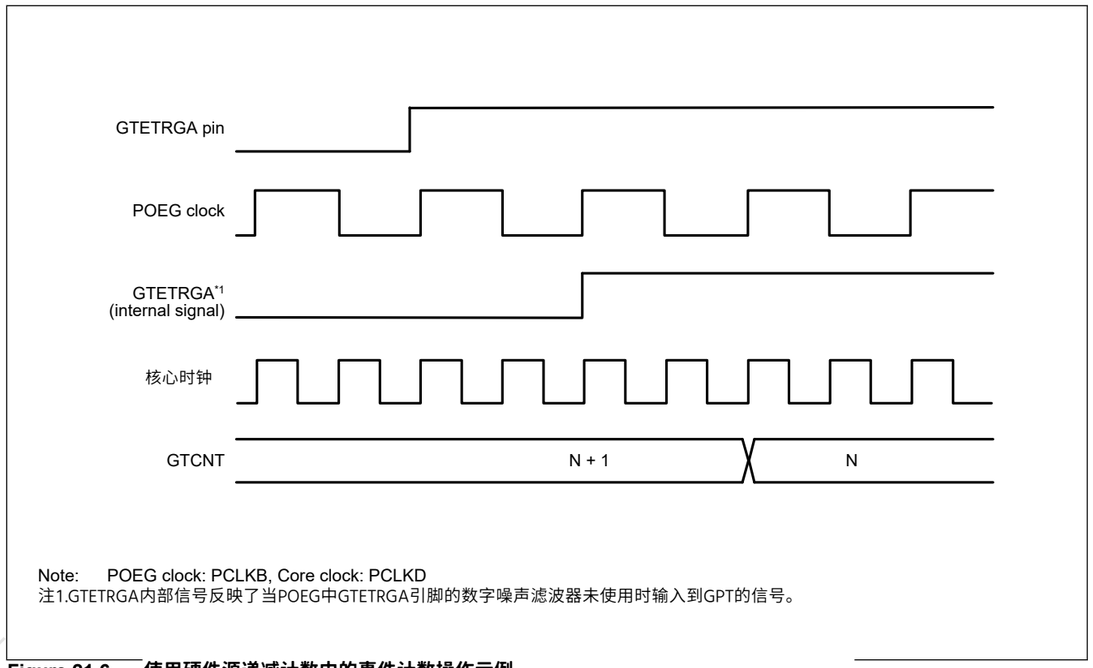
- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST is 1) or not (GTCR.CST is 0).

When the count direction flag is set as decrement (GTST.TCUF flag = 0) in saw-wave mode selected with GTCR.MD[2:0] bits, the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

When not in saw waves mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources are performed.

In event count operation when at least 1 bit in the GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately to synchronize with PCLKD. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[3:0].



Note: POEG clock: PCLKB, Core clock: PCLKD
注1.GTETRGA内部信号反映了当POEG中GTETRGA引脚的数字噪声滤波器未使用时输入到GPT的信号。

Figure 21.6 使用硬件源递减计数中的事件计数操作示例

表21.8显示了使用硬件资源在递减计数中设置周期性计数操作的示例。

Table 21.8 使用硬件源在递减计数中设置事件计数操作的示例

No.	步骤名称	Description
1	设置计数源	使用GTDNSR寄存器选择倒计时源。
2	设置周期	在GTPR中设置循环。
3	设置计数器的初始值	在GTCNT计数器中设置初始值。
4	开始计数操作	将GTCR.CST设置为1以启动计数操作。

(6) 计数器清零操作

每个通道的计数器由以下来源清零：

- ●将0写入GTCNT寄存器
- ●当GTCSR.CCLR位设置为1时，将1写入GTCLR中与GPT通道号相关的位
- ●GTCSR寄存器中选择的硬件源。

计数操作期间禁止写入GTCNT寄存器。GTCNT计数器可以通过向GTCLR写入1和硬件源的清除请求来清除，无论GTCNT正在计数（GTCR.CST为1）还是不计数（GTCR.CST为0）。

在使用GTCR.MD[2:0]位选择的锯齿波模式下，当计数方向标志设置为递减（GTST.TCUF标志=0）时，GTCNT寄存器在写入1时设置为GTPR寄存器的值GTCLR寄存器和硬件源清除时执行。

当不处于锯齿波模式和递减计数时，当向GTCLR寄存器写入1和执行硬件源清零时，GTCNT寄存器设置为0。

在GTUPSR或GTDNSR中至少有1位设置为1的事件计数操作中，清除源发生后，立即执行写入GTCLR寄存器和通过硬件源清除以与PCLKD同步。如果使用其他设置，则清除与GTCR.TPCS[3:0]中选择的计数器时钟同步。

21.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock, including the event count. At the same time, the GPT can output low, high, or toggled output from the associated GTIOCnA or GTIOCnB output pin (n = 0 to 9). In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the cycle end which is determined by GTPR.

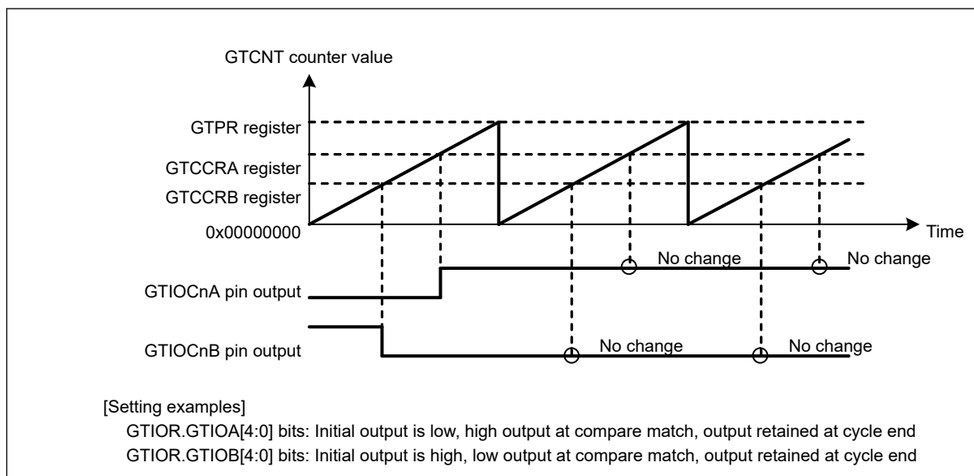
The cycle end is:

- For saw waves in up-counting – when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting – when GTCNT changes from 0 to GTPR value (underflow)
- For saw waves – when the GTCNT counter is cleared
- For triangle waves – when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 21.7 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOCnA pin by a GTCCRA compare match, and low is output from the GTIOCnB pin by a GTCCRB compare match. The pin level does not change when the specified level and pin level match.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is low, high output at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is high, low output at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 21.7 Example of low output and high output operation

Table 21.9 shows an example for setting low output and high output operation.

Table 21.9 Example for setting low output and high output operation (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.7, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.7, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.

21.3.1.2 比较匹配的波形输出

比较匹配意味着GTCNT计数器值与GTCCRA或GTCCRB的值匹配。当比较匹配发生时，比较匹配标志与计数时钟同步生成，包括事件计数。同时，GPT可以从相关的GTIOCnA或GTIOCnB输出引脚（n=0到9）输出低电平、高电平或翻转输出。此外，GTIOCnA或GTIOCnB引脚输出可以是低电平、高电平或在周期结束时切换，由下式确定

GTPR.

循环结束为：

●对于递增计数中的锯齿波 当GTCNT从GTPR值变为0时（溢出）

●对于向下计数中的锯齿波 当GTCNT从0变为GTPR值时（下溢）

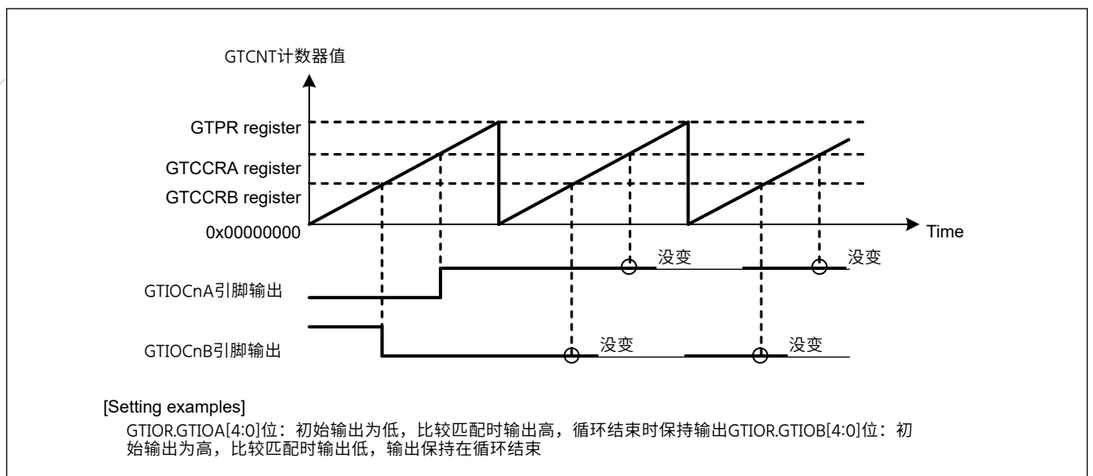
●对于锯齿波 当GTCNT计数器清零时

●对于三角波——当GTCNT从0变为1（波谷）时。

(1) 低输出和高输出

图21.7显示了通过GTCCRA和GTCCRB比较匹配的低输出和高输出操作示例。

在本例中，GTCNT计数器进行递增计数，设定为通过GTCCRA比较匹配从GTIOCnA引脚输出高电平，通过GTCCRB比较匹配从GTIOCnB引脚输出低电平。当指定电平和引脚电平匹配时，引脚电平不会改变。



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为低，比较匹配时输出高，循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为高，比较匹配时输出低，输出保持在循环结束

Note: 寄存器的基地址相同。

Figure 21.7 低输出和高输出操作示例

表21.9显示了设置低输出和高输出操作的示例。

Table 21.9 设置低输出和高输出操作的示例(1of2)

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.7中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.7中，在GTUDDTYC[1:0]中设置了11b后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。

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Table 21.9 Example for setting low output and high output operation (2 of 2)

No.	Step Name	Description
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure Figure 21.7, GTIOA[4:0] = 00010b, GTIOB[4:0] = 10001b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set compare match value	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set GTCR.CST to 1 to start count operation.

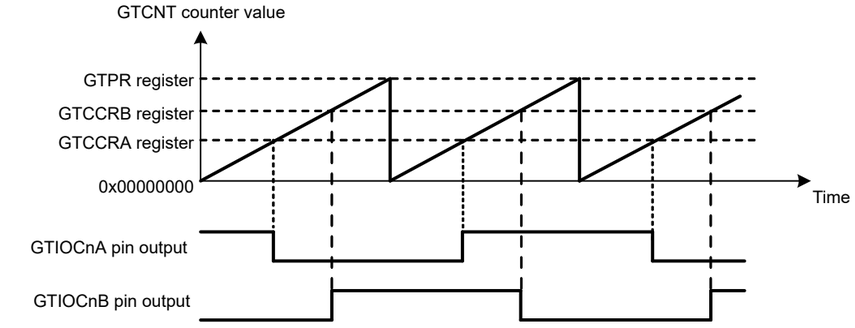
Note: n: 0 to 9
m: A, B

(2) Toggled output

Figure 21.8 and Figure 21.9 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB.

In Figure 21.8, the GTCNT counter performs up-counting, and settings are made so that the GTIOCnA pin output by a GTCCRA compare match and GTIOCnB pin output by a GTCCRB compare match are toggled.

In Figure 21.9, the GTCNT counter performs up-counting, and settings are made so that a GTCCRA compare match toggles the GTIOCnA pin output level and a cycle end toggles the GTIOCnB pin output level.



[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output toggled at compare match, output retained at cycle end

Note: The base address of registers are the same.

Figure 21.8 Example of toggled output operation (1)

Table 21.9 设置低输出和高输出操作的示例(2of2)

No.	步骤名称	Description
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.7中，GTIOA[4:0]=00010b，GTIOB[4:0]=10001b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配值	在GTCCRA和GTCCRB寄存器中设置比较匹配值。
9	开始计数操作	将GTCR.CST设置为1以启动计数操作。

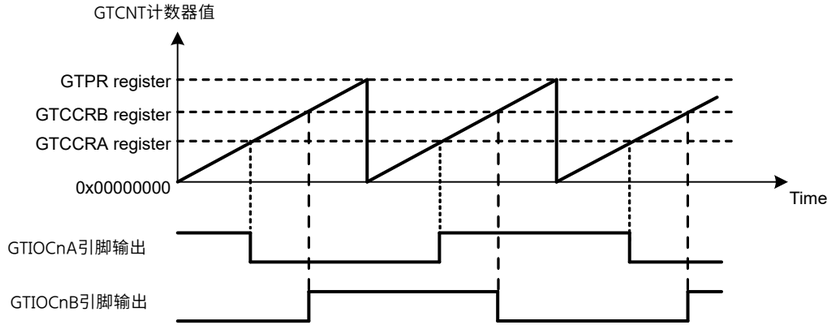
Note: n: 0 to 9
m: A, B

(2) Toggled output

图21.8和图21.9通过GTCCRA和GTCCRB的比较匹配显示了切换输出操作的示例。

在图21.8中，GTCNT计数器进行递增计数，并进行设置以使GTIOCnA引脚输出GTCCRA比较匹配和GTCCRB比较匹配的GTIOCnB引脚输出被切换。

在图21.9中，GTCNT计数器执行递增计数，并进行设置，以便GTCCRA比较匹配切换GTIOCnA引脚输出电平，循环结束切换GTIOCnB引脚输出电平。



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为高电平，在比较匹配时触发输出，在循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为低电平，在比较匹配时触发输出，输出保持在循环结束

Note: 寄存器的基地址相同。

Figure 21.8 切换输出操作示例(1)

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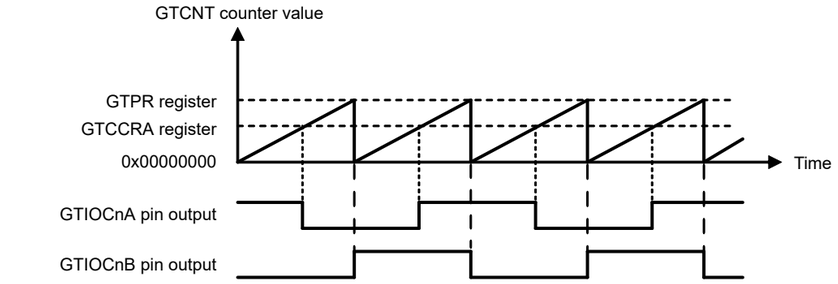


[Setting examples]
GTIOR.GTIOA[4:0] bits: Initial output is high, output toggled at compare match, output retained at cycle end
GTIOR.GTIOB[4:0] bits: Initial output is low, output retained at compare match, output toggled at cycle end

Note: The base address of registers are the same.

Figure 21.9 Example of toggled output operation (2)

Figure 21.15 shows an example for setting toggled output operation.

Table 21.10 Example for setting toggled output operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.8 and Figure 21.9, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.8 and Figure 21.9, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.8, GTIOA[4:0] = 10011b, GTIOB[4:0] = 00011b in Figure 21.9, GTIOA[4:0] = 10011b, GTIOB[4:0] = 01100b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set compare match value	Set compare match values in the GTCCRA and GTCCRB registers.
9	Start count operation	Set GTCR.CST to 1 to start count operation.

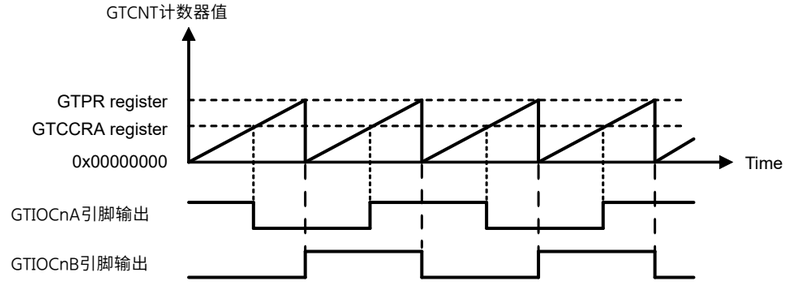
Note: n: 0 to 9
m: A, B

21.3.1.3 Input capture function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 21.10 shows an example of the input capture function.

In this example, the GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTCCRA at both edges of the GTIOCnA input pin and to GTCCRB on the rising edge of the GTIOCnB input pin.



[Setting examples]
GTIOR.GTIOA[4:0]位：初始输出为高电平，在比较匹配时切换输出，在循环结束时保持输出GTIOR.GTIOB[4:0]位：初始输出为低电平，在比较匹配时保持输出，输出在循环结束时切换循环结束

Note: 寄存器的基地址相同。

Figure 21.9 切换输出操作示例(2)

图21.15显示了设置切换输出操作的示例。

Table 21.10 设置切换输出操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.8和图21.9中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。在图21.8和图21.9中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.8中，GTIOA[4:0]=10011b，GTIOB[4:0]=00011b在图21.9中，GTIOA[4:0]=10011b，GTIOB[4:0] = 01100b.
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配值	在GTCCRA和GTCCRB寄存器中设置比较匹配值。
9	开始计数操作	将GTCR.CST设置为1以启动计数操作。

Note: n: 0 to 9
m: A, B

21.3.1.3 输入捕捉功能

在检测到在GTICASR和GTICBSR中设置的硬件源时，可以将GTCNT计数器值传输到GTCCRA或GTCCRB。

图21.10显示了输入捕获函数的示例。

在本例中，GTCNT计数器通过计数时钟进行递增计数，并设置为在GTIOCnA输入引脚的两个边沿对GTCCRA执行输入捕捉，在GTIOCnB输入引脚的上升沿对GTCCRB执行输入捕捉。

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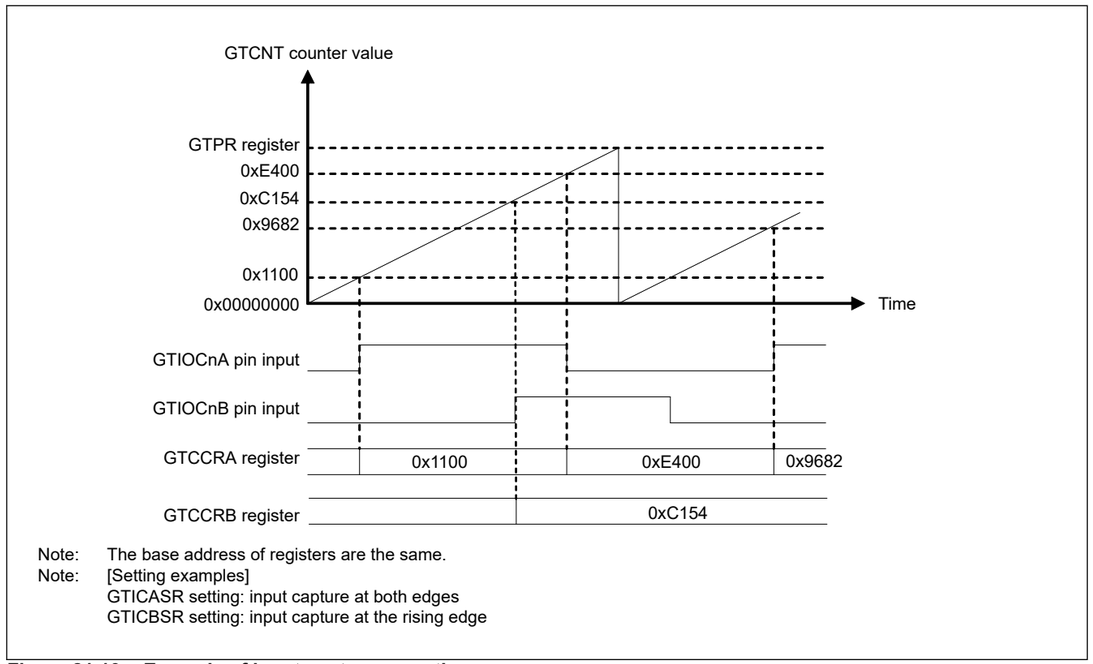


Note: The base address of registers are the same.
Note: [Setting examples]
GTICASR setting: input capture at both edges
GTICBSR setting: input capture at the rising edge

Figure 21.10 Example of input capture operation

Table 21.11 and Table 21.14 shows the example for setting an input capture operation with count operation by the count clock.

Table 21.11 Example for setting input capture operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.10, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.10, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select the input capture source in GTICASR and GTICBSR. In Figure 21.10, GTICASR = 0x00000F00, GTICBSR = 0x00003000.
7	Start count operation	Set GTCR.CST to 1 to start count operation.

21.3.2 Buffer Operation

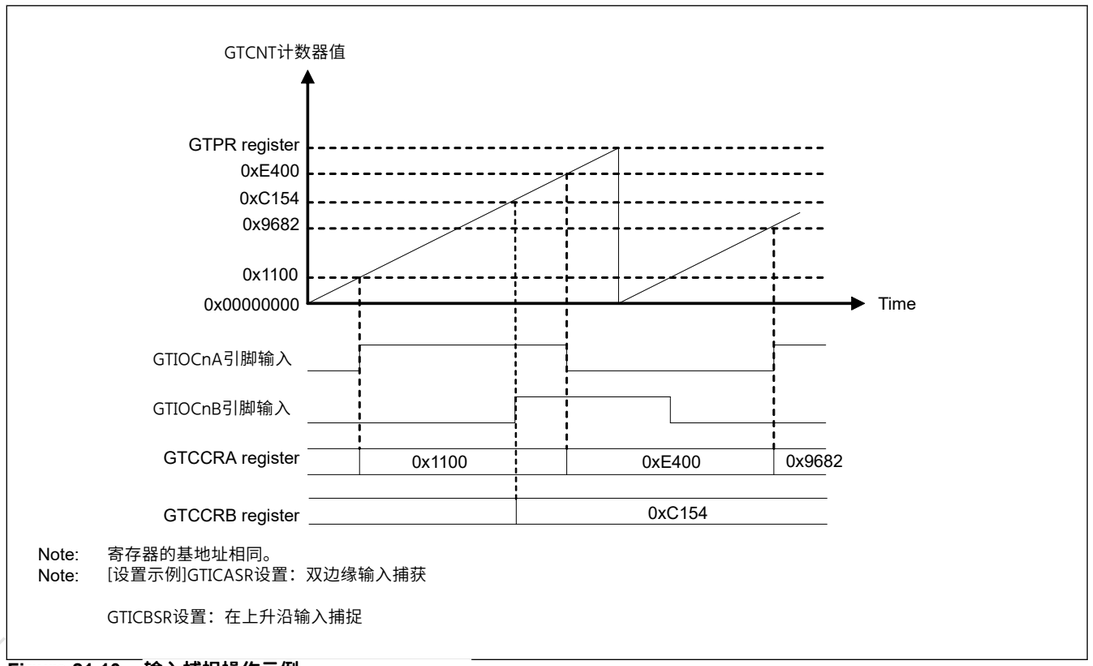
The following buffer operations can be set with GTBER:

- GTPR and GTPBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF

21.3.2.1 GTPR register buffer operation

GTPBR can function as a buffer register for GTPR.

The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.



Note: 寄存器的基地址相同。
Note: [设置示例]GTICASR设置：双边缘输入捕获
GTICBSR设置：在上升沿输入捕捉

Figure 21.10 输入捕捉操作示例

表21.11和表21.14显示了使用计数时钟设置计数操作的输入捕捉操作的示例。

Table 21.11 设置输入捕捉操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.10中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.10中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	选择输入捕捉源	在GTICASR和GTICBSR中选择输入捕获源。 在图21.10中，GTICASR=0x00000F00，GTICBSR=0x00003000。
7	开始计数操作	将GTCR.CST设置为1以启动计数操作。

21.3.2 缓冲操作

可以使用GTBER设置以下缓冲区操作：

- GTPR and GTPBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF

21.3.2.1 GTPR寄存器缓冲操作

GTPBR可以作为GTPR的缓冲寄存器。

缓冲区传输在锯齿波模式或事件计数中的上溢（向上计数期间）或下溢（向下计数期间）以及三角波模式的波谷处执行。

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in CTCSR register)
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR.CCLRn bit is set to 1, n = 0 to 9).

To set GTPR to function as a buffer, set the GTBER.PR bit to 1. To set GTPR not to function as a buffer, set the GTBER.PR bit to 0.

Figure 21.11 to Figure 21.13 show examples of GTPR buffer operation and Table 21.12 shows an example for setting GTPR buffer operation.

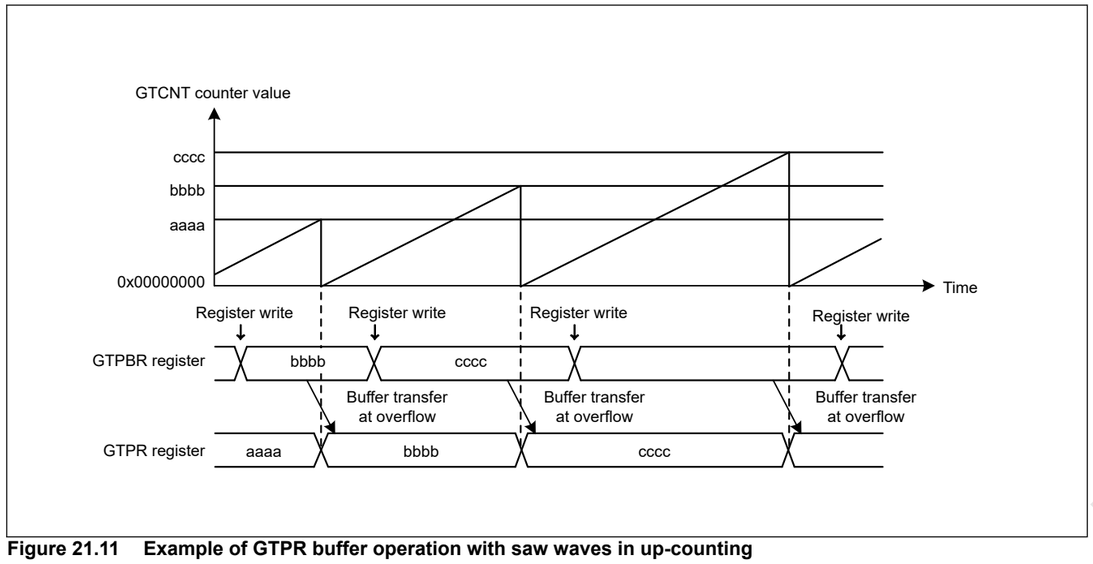


Figure 21.11 Example of GTPR buffer operation with saw waves in up-counting

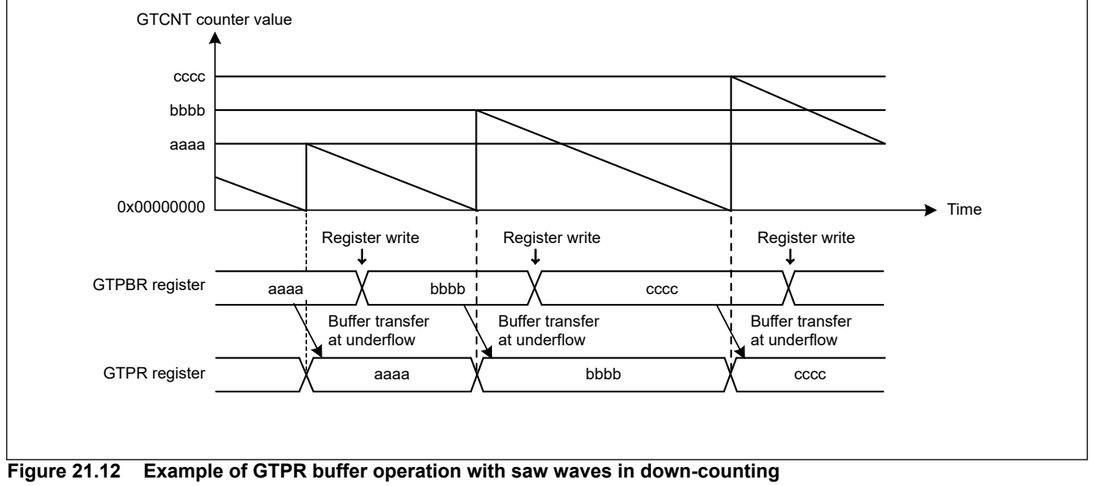


Figure 21.12 Example of GTPR buffer operation with saw waves in down-counting

在锯齿波模式或事件计数中，当计数期间发生以下计数器清零操作时，将执行缓冲区传输：

●通过硬件源清除（清除源在CTCSR寄存器中选择）
●软件清零（当GTCSR.CCLR位为1且GTCLR.CCLRn位设置为1时，n=0至9）。

要将GTPR设置为缓冲区，请将GTBER.PR位设置为1。要将GTPR设置为不作为缓冲区，请将GTBER.PR位设置为0。

图21.11至图21.13显示了GTPR缓冲区操作的示例，表21.12显示了设置GTPR缓冲区操作的示例。

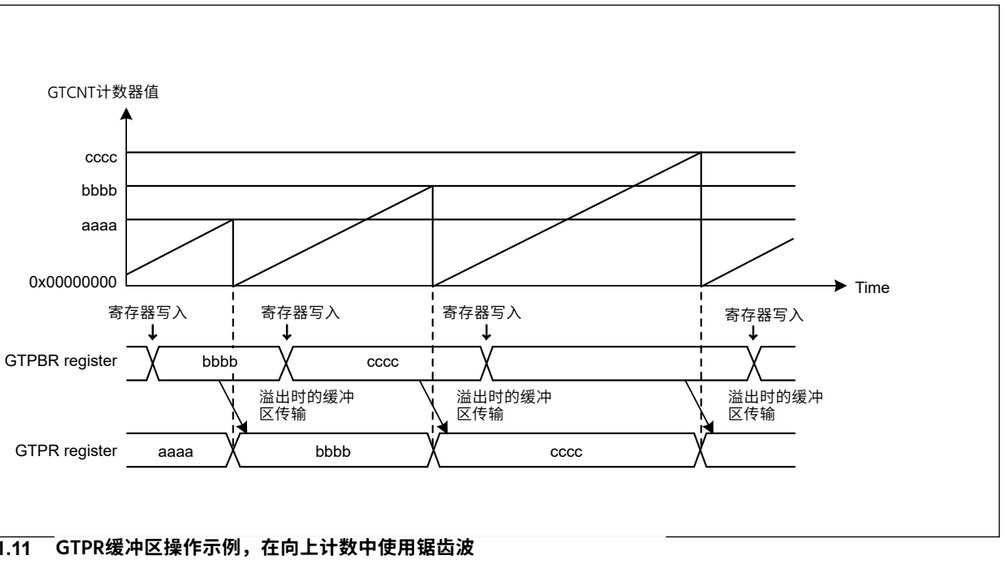


Figure 21.11 GTPR缓冲区操作示例，在向上计数中使用锯齿波

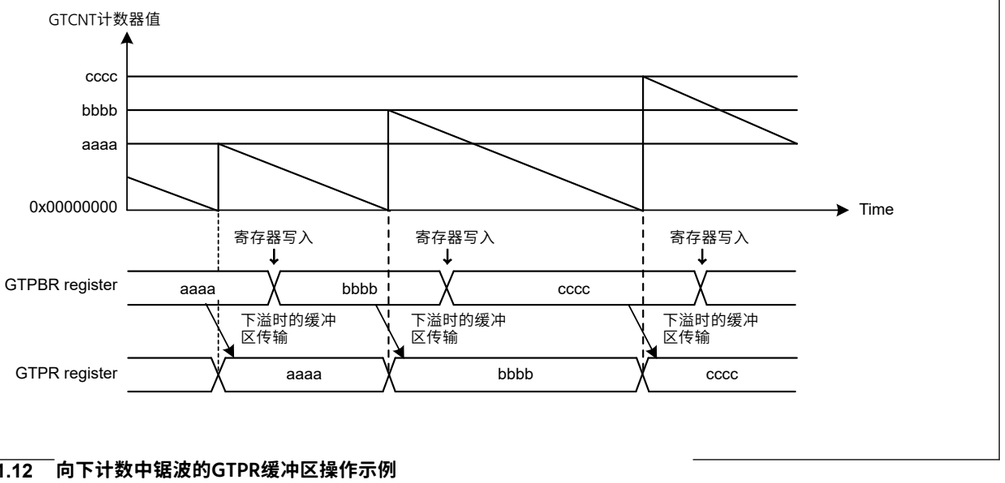


Figure 21.12 向下计数中锯波的GTPR缓冲区操作示例

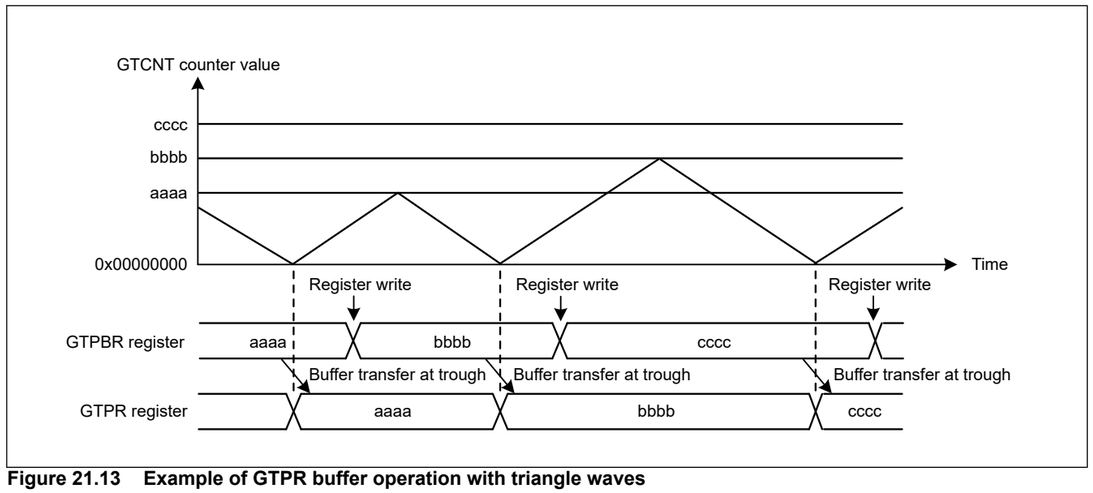


Figure 21.13 Example of GTPR buffer operation with triangle waves

Table 21.12 Example for setting GTPR buffer operation

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.11 and Figure 21.12, 000b (saw-wave PWM mode) is set, and in Figure 21.13, 100b (triangle-wave PWM mode 1) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.11, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting). In Figure 21.12, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set buffer operation	Set buffer operation with GTBER.PR[1:0]. In Figure 21.11, Figure 21.12, and Figure 21.13, PR[1:0] = 01b.
7	Set buffer value	For buffer operation, set a value in one cycle after the current cycle in GTPBR.
8	Start count operation	Set GTCR.CST to 1 to start count operation.
9	Set buffer value for each cycle	For buffer operation, set a value in one cycle after the current cycle in GTPBR.

21.3.2.2 Buffer operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. To set GTCCRA or GTCCRB to not function as a buffer, set 00b.

(1) When GTCCRA or GTCCRB functions as an output compare register

Buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear

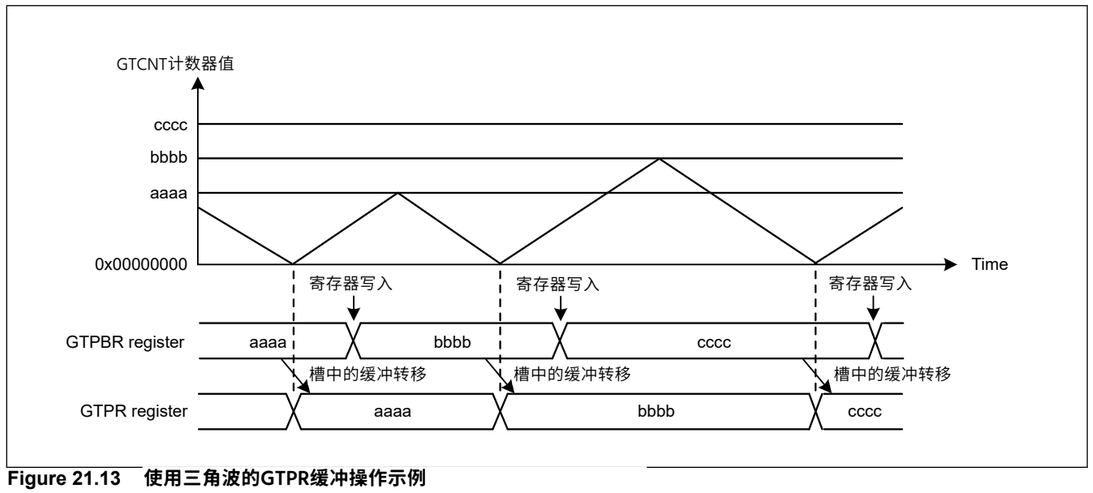


Figure 21.13 使用三角波的GTPR缓冲操作示例

Table 21.12 设置GTPR缓冲区操作的示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.11和图21.12中，设置了000b（锯齿波PWM模式），在图21.13中，设置了100b（三角波PWM模式1）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.11中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。 在图21.12中，在GTUDDTYC[1:0]中设置10b后，在GTUDDTYC[1:0]中设置00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置缓冲操作	使用GTBER.PR[1:0]设置缓冲区操作。在图21.11、图21.12和图21.13中，PR[1:0]=01b。
7	设置缓冲区值	对于缓冲操作，在GTPBR中的当前周期之后的一个周期内设置一个值。
8	开始计数操作	将GTCR.CST设置为1以启动计数操作。
9	为每个周期设置缓冲区值	对于缓冲操作，在GTPBR中的当前周期之后的一个周期内设置一个值。

21.3.2.2 GTCCRA和GTCCRB的缓冲操作

GTCCRC可以作为GTCCRA缓冲寄存器，GTCCRD可以作为GTCCRC缓冲寄存器（GTCCRA的双缓冲寄存器）。同样，GTCCRE可以作为GTCCRB缓冲寄存器，GTCCRF可以作为GTCCRE缓冲寄存器（GTCCRB的双缓冲寄存器）。

要将GTCCRA或GTCCRB设置为双缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为10b或11b。
对于单缓冲操作，设置01b。要将GTCCRA或GTCCRB设置为不用作缓冲区，请设置00b。

(1) 当GTCCRA或GTCCRB用作输出比较寄存器时

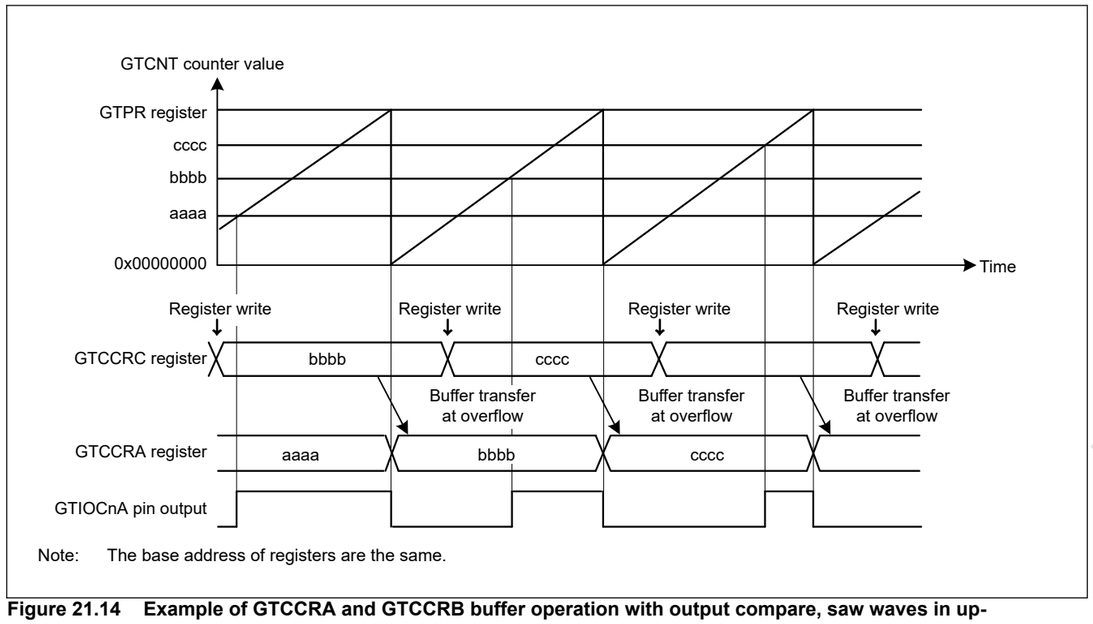
缓冲区传输发生在以下情况：

- 上溢或下溢的缓冲区传输
  在锯齿波模式或事件计数操作中，在溢出（向上计数期间）或下溢（向下计数期间）时执行缓冲区传输。在三角波模式中，缓冲区传输在波谷（三角波PWM模式1）或波峰和波谷（三角波PWM模式2）处执行。
- 通过计数器清除缓冲区传输

In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources similar to the case shown in section 21.3.2.1. GTPR register buffer operation.
In triangle-wave mode, buffer transfer is not performed by the counter clear.

- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfer are performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode.
  Additionally buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3.

Figure 21.14 to Figure 21.16 show examples of GTCCRA and GTCCRB buffer operation and Table 21.13 shows an example for setting GTCCRA and GTCCRB buffer operation.



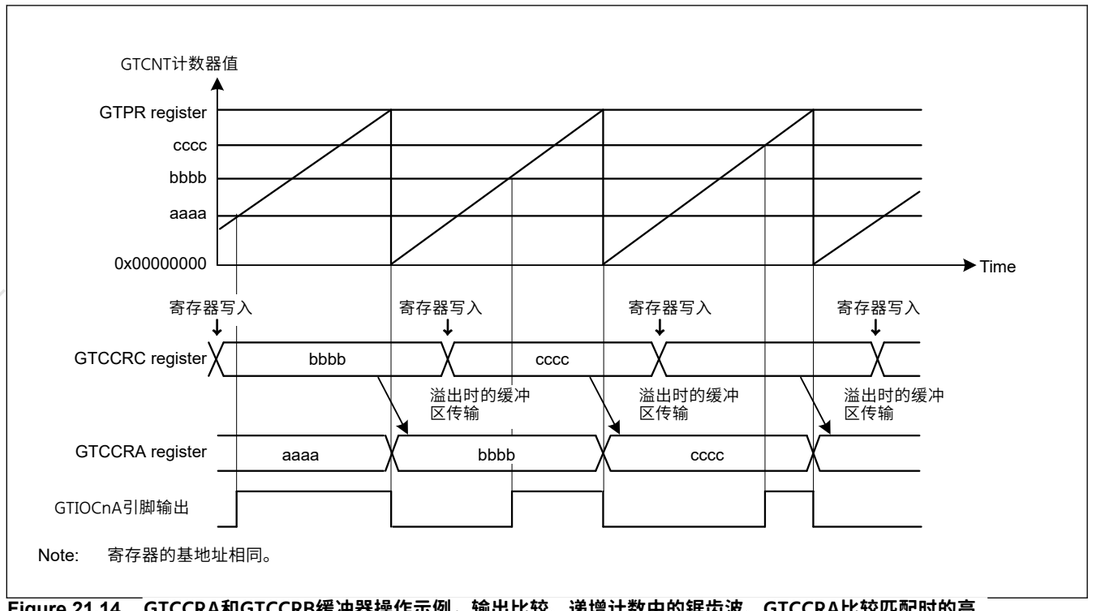
Note: The base address of registers are the same.

Figure 21.14 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, and low output at cycle end

在锯齿波模式或事件计数操作中，在计数期间，缓冲区传输（与向上计数期间的溢出或向下计数期间的下溢相同）由计数器清零源执行，类似于章节中所示的情况21.3.2.1。GTPR寄存器缓冲操作。在三角波模式下，计数器清零不执行缓冲区传输。

●强制缓冲转移
当GTBER.CCRSWT位在计数操作停止时设置为1时，在锯齿波模式、事件计数操作和三角波模式下强制执行GTCCRA和GTCCRB寄存器缓冲传输。此外，从GTCCRD寄存器到临时寄存器A以及从GTCCRF寄存器到临时寄存器B的缓冲区传输是在锯齿波一次性脉冲模式或三角波PWM模式3中执行的。

图21.14至图21.16显示了GTCCRA和GTCCRB缓冲操作的示例，表21.13显示了设置GTCCRA和GTCCRB缓冲操作的示例。



Note: 寄存器的基地址相同。

Figure 21.14 GTCCRA和GTCCRB缓冲器操作示例，输出比较、递增计数中的锯齿波、GTCCRA比较匹配时的高输出和周期结束时的低输出

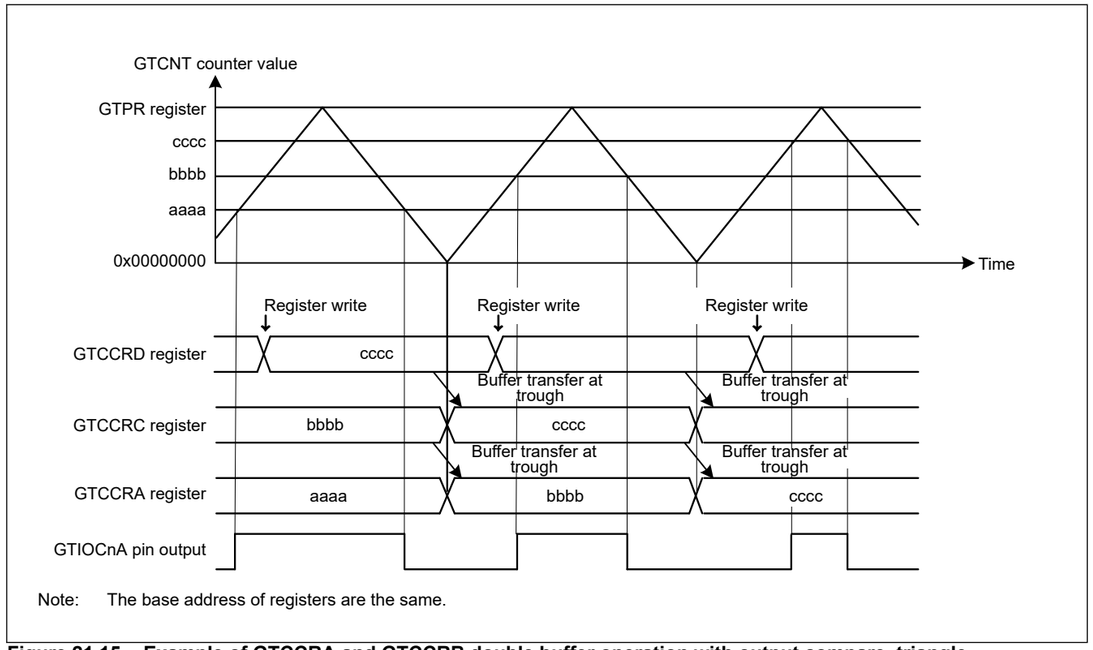


Figure 21.15 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end

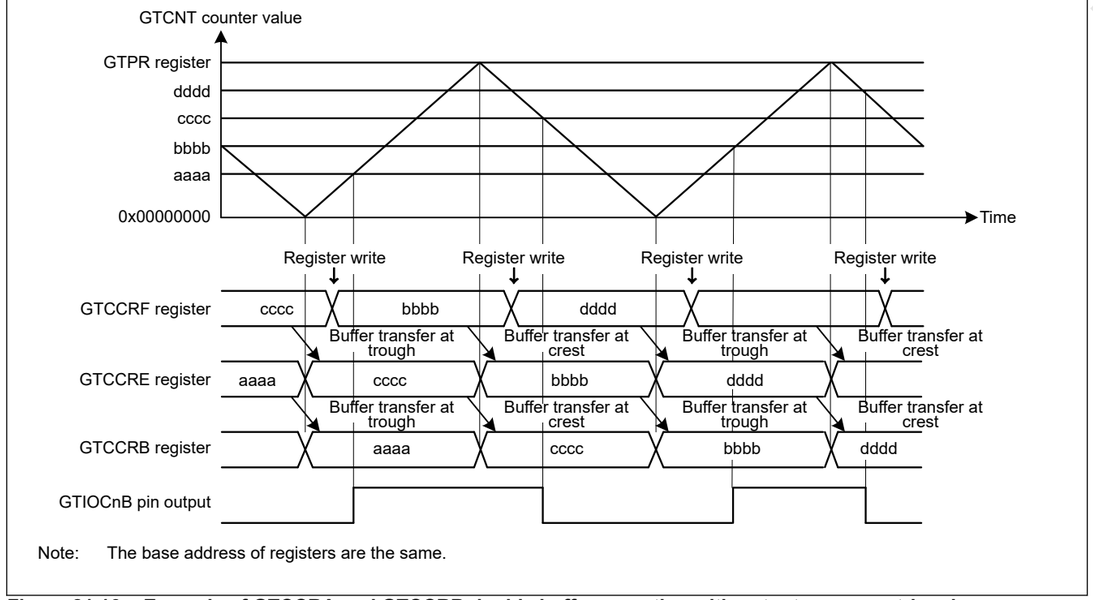


Figure 21.16 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end

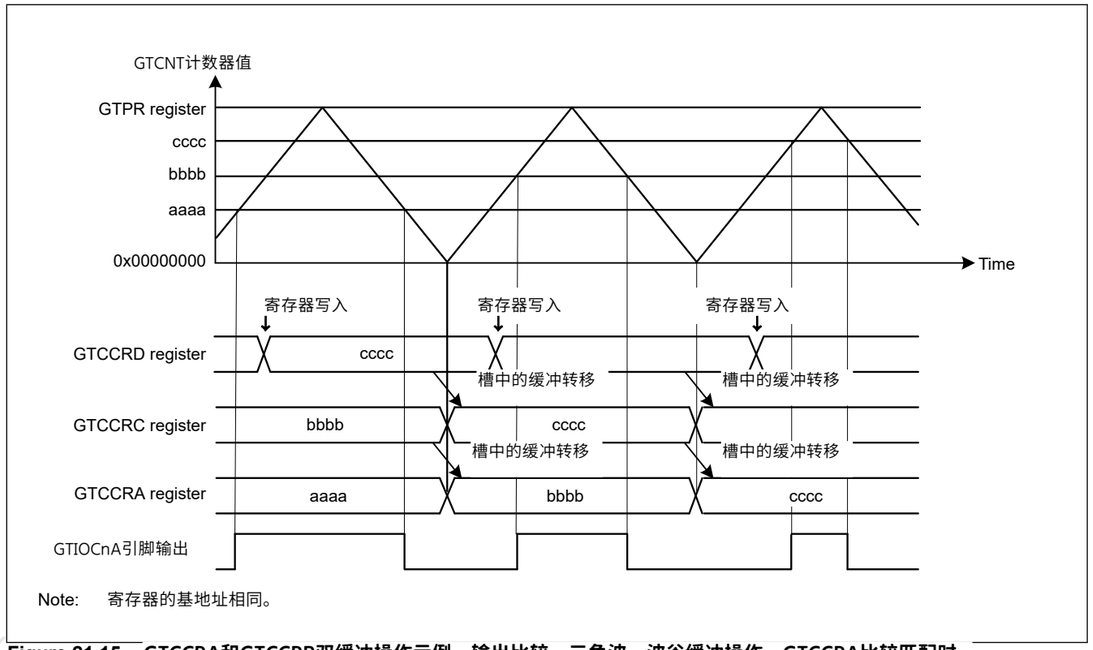


Figure 21.15 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷缓冲操作、GTCCRA比较匹配时切换输出、循环结束时保留输出

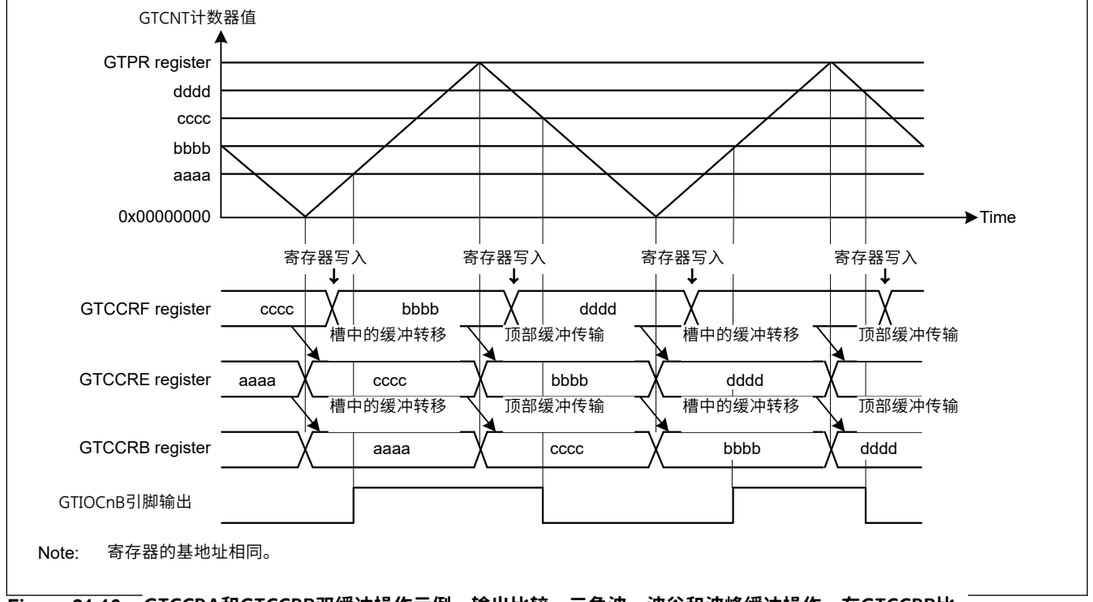


Figure 21.16 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷和波峰缓冲操作、在GTCCRB比较匹配时切换输出以及在周期结束时保留输出

Table 21.13 Example for setting GTCCRA and GTCCRB buffer operation for output compare

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.14, 000b (saw-wave PWM mode) is set, in Figure 21.15, 100b (triangle-wave PWM mode 1) is set, and in Figure 21.16, 101b (triangle-wave PWM mode 2) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.14, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.14, GTIOA[4:0] = 00110b, in Figure 21.15, GTIOA[4:0] = 00011b, and in Figure 21.16, GTIOB[4:0] = 00011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 21.14, CCRA[1:0] = 01b, in Figure 21.15, CCRA[1:0] = 1xb, and in Figure 21.16, CCRB[1:0] = 1xb.
9	Set compare match value	Set the GTIOCnA pin transition in GTCCRA and GTIOCnB pin transition in the GTCCRB.
10	Set buffer value	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRD and GTCCRF, respectively.
11	Start count operation	Set GTCR.CST to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA and GTIOCnB pins transitions in 1 cycle after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or half cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA and GTIOCnB pins transitions in 2 cycles after the current cycle (in saw-wave mode or triangle-wave mode with buffer transfer at trough or crest) or 1 cycle after the current cycle (in triangle-wave mode with buffer transfer at both trough and crest) in GTCCRD and GTCCRF, respectively.

Note: n: 0 to 9
m: A, B

(2) When GTCCRA or GTCCRB functions as an input capture register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 21.17 and Figure 21.18 show examples of GTCCRA and GTCCRB buffer operation and Table 21.14 shows an example for setting GTCCRA and GTCCRB buffer operation.

Table 21.13 为输出比较设置GTCCRA和GTCCRB缓冲操作的示例

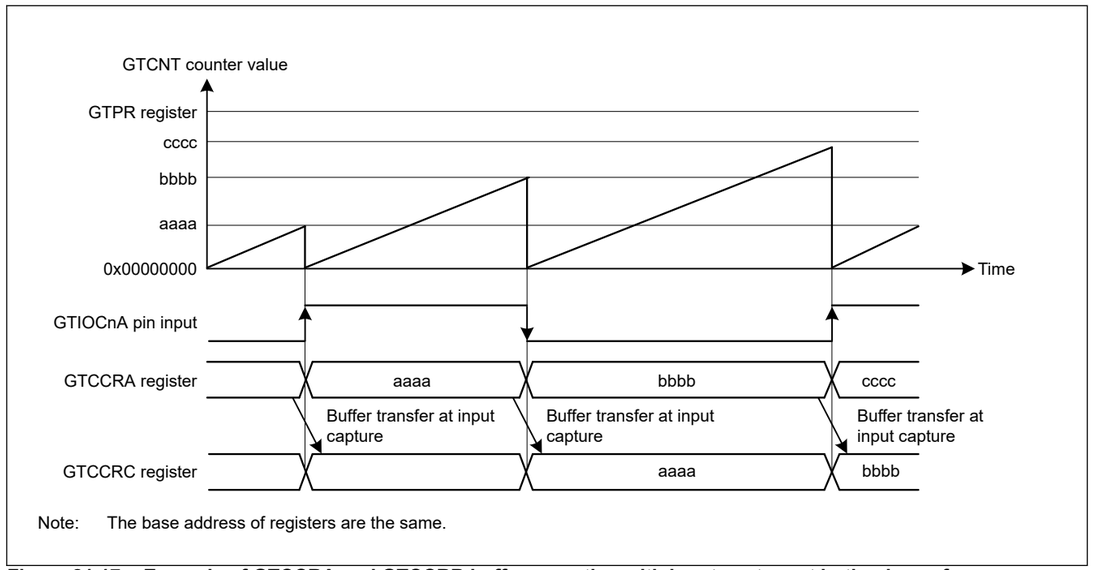
No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.14中，设置了000b（锯齿波PWM模式），在图21.15中，设置了100b（三角波PWM模式1），在图21.16中，设置了101b（三角波PWM模式2）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.14中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.14中，GTIOA[4:0]=00110b，在图21.15中，GTIOA[4:0]=00011b，在图21.16中，GTIOB[4:0] = 00011b.
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图21.14中，CCRA[1:0]=01b，在图21.15中，CCRA[1:0]=1xb，在图21.16中，CCRB[1:0] = 1xb.
9	设置比较匹配值	在GTCCRA中设置GTIOCnA引脚转换，在GTCCRB中设置GTIOCnB引脚转换。
10	设置缓冲区值	对于缓冲操作，设置GTIOCnA和GTIOCnB引脚在当前周期后1个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的半个周期（在三角波模式分别在GTCCRC和GTCCRE中的波谷和波峰处进行缓冲区传输。 对于双缓冲操作，还设置GTIOCnA和GTIOCnB引脚在当前周期后的2个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的1个周期（在三角形–在GTCCRD和GTCCRF中分别具有波谷和波峰缓冲传输的波模式。
11	开始计数操作	将GTCR.CST设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲操作，设置GTIOCnA和GTIOCnB引脚在当前周期后1个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的半个周期（在三角波模式分别在GTCCRC和GTCCRE中的波谷和波峰处进行缓冲区传输。 对于双缓冲操作，还设置GTIOCnA和GTIOCnB引脚在当前周期后的2个周期（在锯齿波模式或在波谷或波峰处缓冲传输的三角波模式）或当前周期后的1个周期（在三角形–在GTCCRD和GTCCRF中分别具有波谷和波峰缓冲传输的波模式。

Note: n: 0 to 9
m: A, B

(2) 当GTCCRA或GTCCRB用作输入捕捉寄存器时

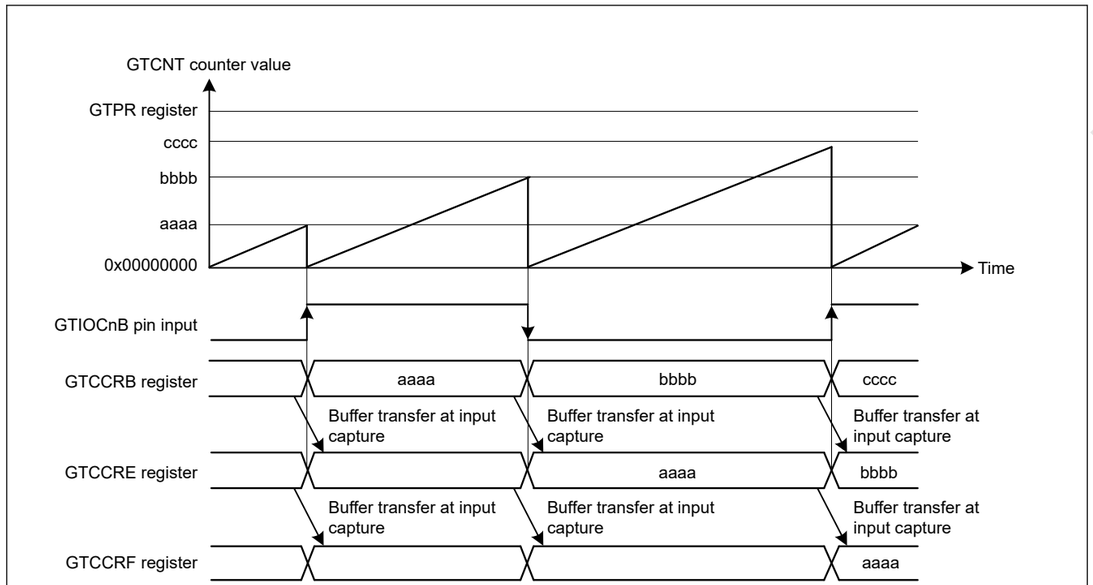
当产生输入捕捉时，GTCNT计数器值被传送到GTCCRA和GTCCRB并存储
GTCCRA和GTCCRB寄存器值被传送到缓冲寄存器。在输入捕捉操作中，缓冲区传输不是由计数器清零来执行的。

图21.17和图21.18显示了GTCCRA和GTCCRB缓冲操作的示例，表21.14显示了设置GTCCRA和GTCCRB缓冲操作的示例。



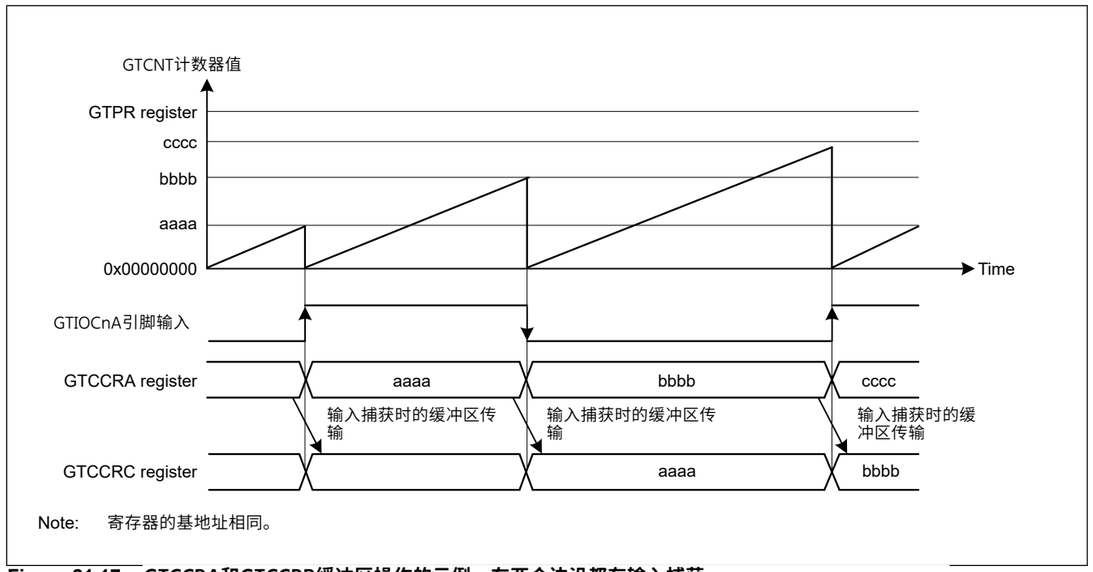
Note: The base address of registers are the same.

Figure 21.17 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOCnA input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnA input



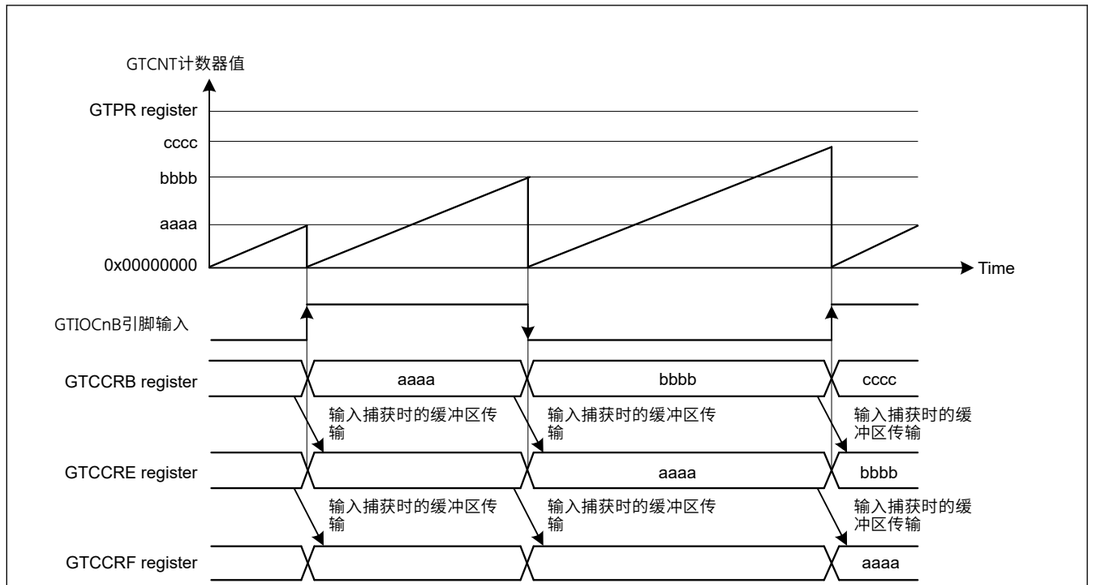
Note: The base address of registers are the same.

Figure 21.18 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOCnB input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOCnB input



Note: 寄存器的基地址相同。

Figure 21.17 GTCCRA和GTCCRB缓冲区操作的示例，在两个边沿都有输入捕获GTIOCnA输入，递增计数中的锯齿波，并且GTCNT计数器在GTIOCnA input



Note: 寄存器的基地址相同。

Figure 21.18 GTCCRA和GTCCRB双缓冲操作示例，在两个边沿进行输入捕获GTIOCnB输入，递增计数中的锯齿波，GTCNT计数器在两个边缘清零GTIOCnB input

Table 21.14 Example for setting GTCCRA and GTCCRB buffer operation for input capture

No.	Step Name	Description
1	Set operating mode and counter clear sources	Set the operating mode with GTCR.MD[2:0] and count clear source with GTCSR. In Figure 21.17, MD[2:0] = 000b (saw-wave PWM mode) and GTCSR = 0x00000F00, and in Figure 21.18, MD[2:0] = 000b (saw-wave PWM mode) and GTCSR = 0x0000F000.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.17, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Select input capture source	Select input capture source in the GTICASR register and GTICBSR register. In Figure 21.17, GTICASR = 0x00000F00, and in Figure 21.18, GTICBSR = 0x0000F000.
7	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 21.17, CCRA[1:0] = 01b, and in Figure 21.18, CCRB = 1xb.
8	Start count operation	Set GTCR.CST to 1 to start count operation.

21.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA pin or GTIOCnB pin (n = 0 to 9) by a compare match between the GTCNT counter and GTCCRA or GTCCRB.

By setting GTDTCR and GTDVU, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

21.3.3.1 Saw-Wave PWM Mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0 to 9) when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

Figure 21.19 shows an example of saw-wave PWM mode operation, and Table 21.15 shows an example for setting saw-wave PWM mode.

Table 21.14 为输入捕捉设置GTCCRA和GTCCRB缓冲操作的示例

No.	步骤名称	Description
1	设置操作模式和计数器清除源	用GTCR.MD[2:0]设置工作模式，用GTCSR计数清源。 在图21.17中，MD[2:0]=000b（锯齿波PWM模式）和GTCSR=0x00000F00，并且在图21.18，MD[2:0]=000b（锯齿波PWM模式）和GTCSR=0x0000F000。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.17中，在GTUDDTYC[1:0]中设置了11b后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	选择输入捕捉源	在GTICASR寄存器和GTICBSR寄存器中选择输入捕捉源。 在图21.17中，GTICASR=0x00000F00，在图21.18中，GTICBSR=0x0000F000。
7	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图21.17中，CCRA[1:0]=01b，在图21.18中，CCRB=1xb。
8	开始计数操作	将GTCR.CST设置为1以启动计数操作。

21.3.3 PWM输出工作模式

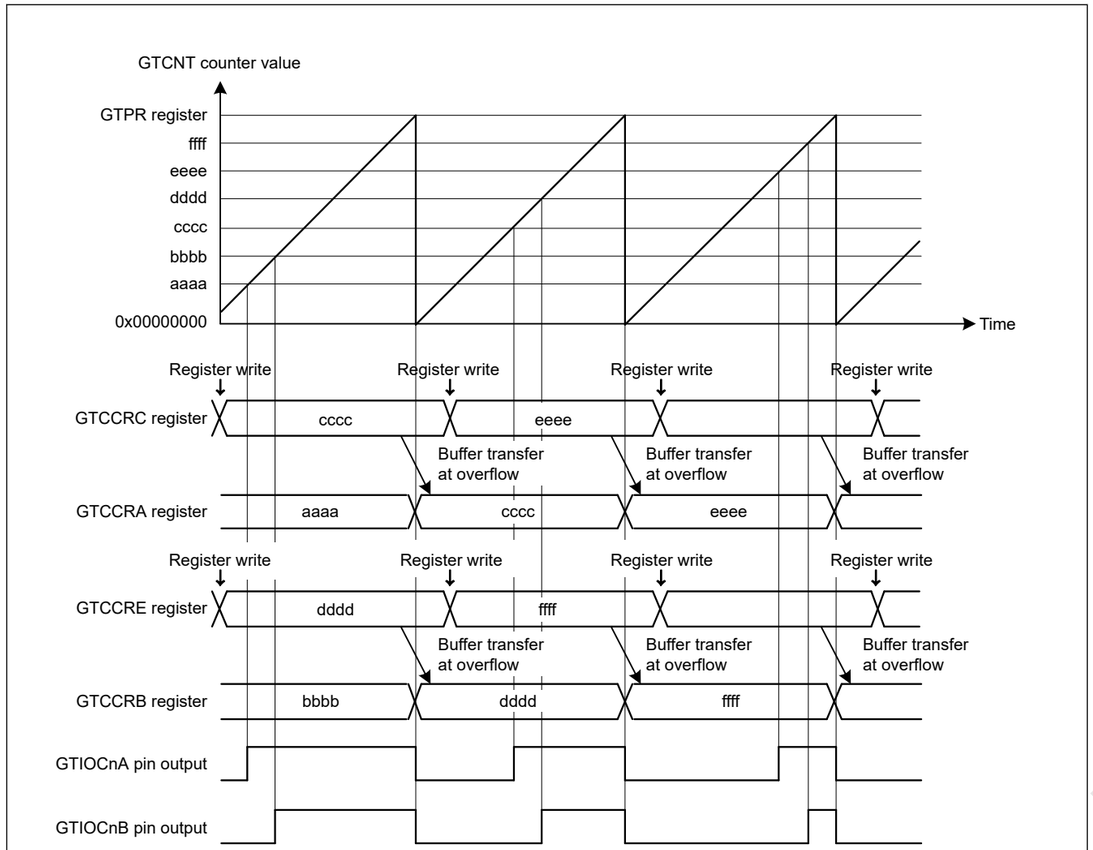
通过GPT之间的比较匹配，GPT可以将PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0到9）。GTCNT计数器和GTCCRA或GTCCRB。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

21.3.3.1 Saw-Wave PWM Mode

在锯齿波PWM模式下，GTCNT通过设置GTPR的周期来执行锯齿波（半波）操作，当GTCCRA或GTCCRB比较时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0至9）匹配发生。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

图21.19显示了锯波PWM模式操作的示例，表21.15显示了设置锯波PWM模式的示例。

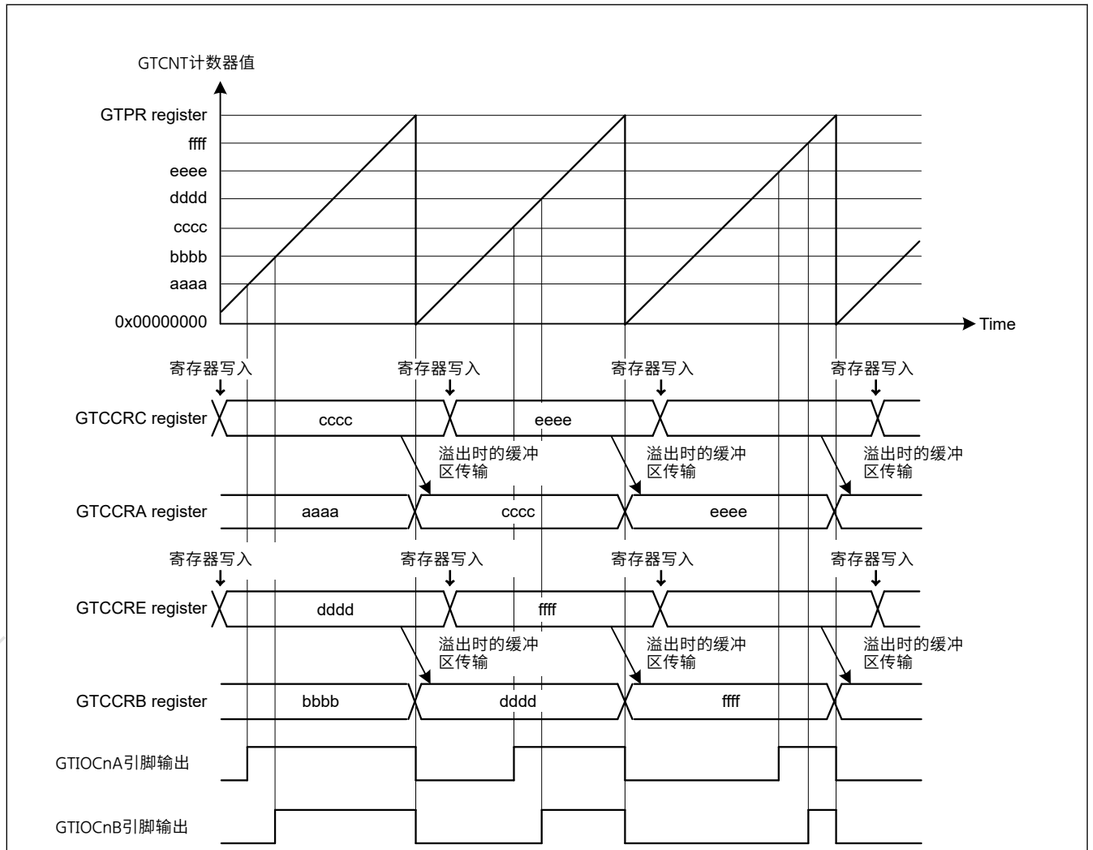


Note: The base address of registers are the same.

Figure 21.19 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end

Table 21.15 Example for setting saw-wave PWM mode (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.19, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.19, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.19, GTIOA[4:0] = 00110b and GTIOB[4:0] = 00110b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 21.19, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
9	Set compare match value	Set the GTIOCnA pin transition in GTCCRA and GTIOCnB pin transition in GTCCRB.



Note: 寄存器的基地址相同。

Figure 21.19 具有递增计数、缓冲操作、高输出的锯齿波PWM模式操作示例 GTCCRAGTCCRB比较匹配，循环结束时输出低

Table 21.15 设置锯齿波PWM模式的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。在图21.19中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.19中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.19中，GTIOA[4:0]=00110b和GTIOB[4:0]=00110b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。在图21.19中，CCRA[1:0]=01b和CCRB[1:0] = 01b.
9	设置比较匹配值	在GTCCRA中设置GTIOCnA引脚转换，在GTCCRB中设置GTIOCnB引脚转换。

Table 21.15 Example for setting saw-wave PWM mode (2 of 2)

No.	Step Name	Description
10	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.
11	Start count operation	Set GTCR.CST to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.

Note: n: 0 to 9
m: A, B

21.3.3.2 Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR, the GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0 to 9) at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.20 shows an example of saw-wave one-shot pulse mode operation, and Table 21.16 shows an example for setting saw-wave one-shot pulse mode.

Table 21.15 设置锯齿波PWM模式的示例(2of2)

No.	步骤名称	Description
10	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。
11	开始计数操作	将GTCR.CST设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

Note: n: 0 to 9
m: A, B

21.3.3.2 锯波单发脉冲模式

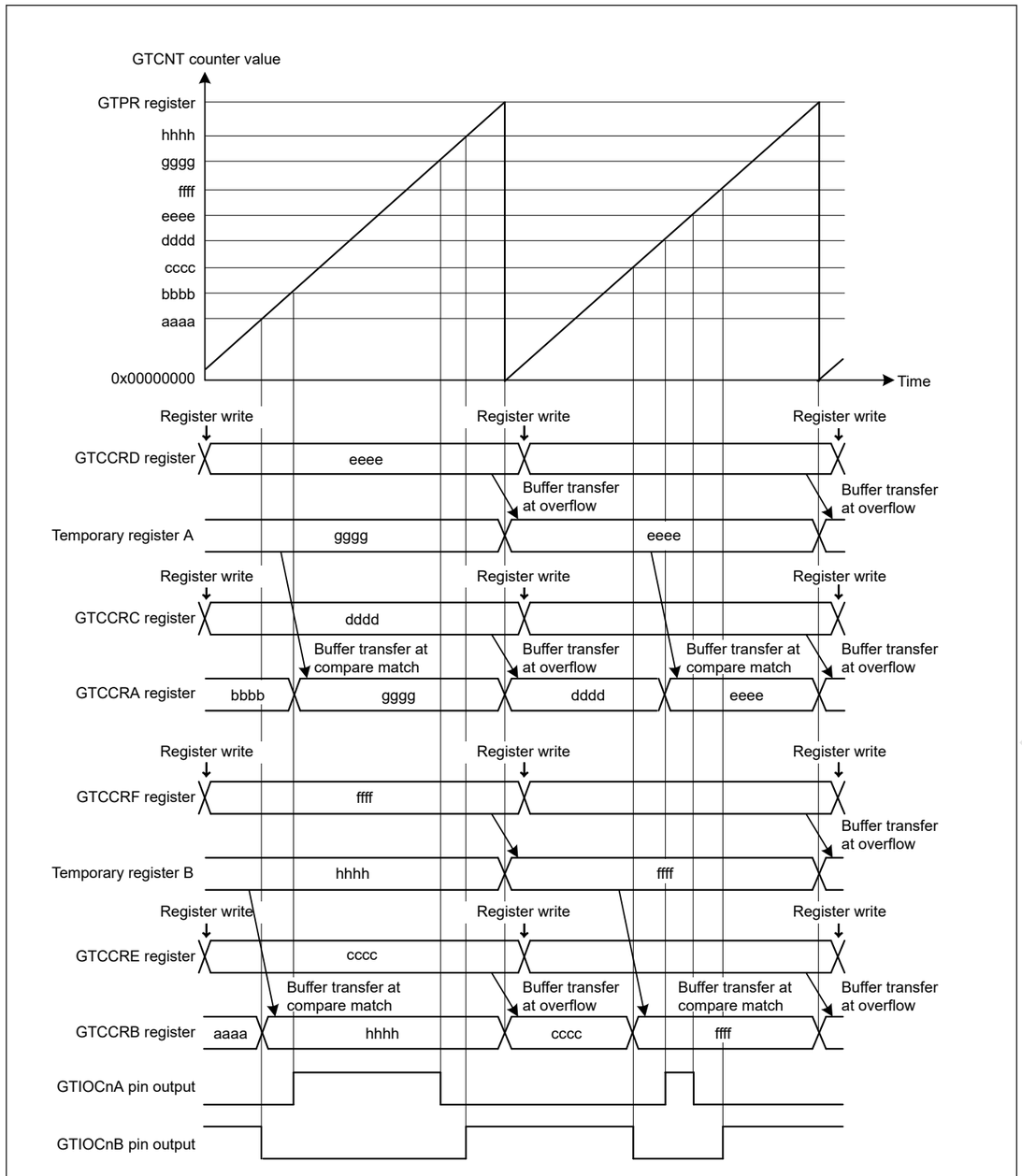
锯齿波单次脉冲模式是在GTPR中设置周期，GTCNT计数器执行锯齿波（半波）操作并将PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0到9)在GTCCRA或GTCCRB的比较匹配中，缓冲区操作固定。

锯波单次脉冲模式中的缓冲操作不同于通常的缓冲操作。缓冲区传输从以下位置执行：

- ●GTCCRC到GTCCRA在循环结束
- ●循环结束时GTCCRE到GTCCRB
- ●GTCCRD在循环结束时到临时寄存器A
- ●GTCCRF在循环结束时到临时寄存器B
- ●GTCCRA比较匹配时到GTCCRA的临时寄存器A
- ●GTCCRB比较匹配时的临时寄存器B到GTCCRB。

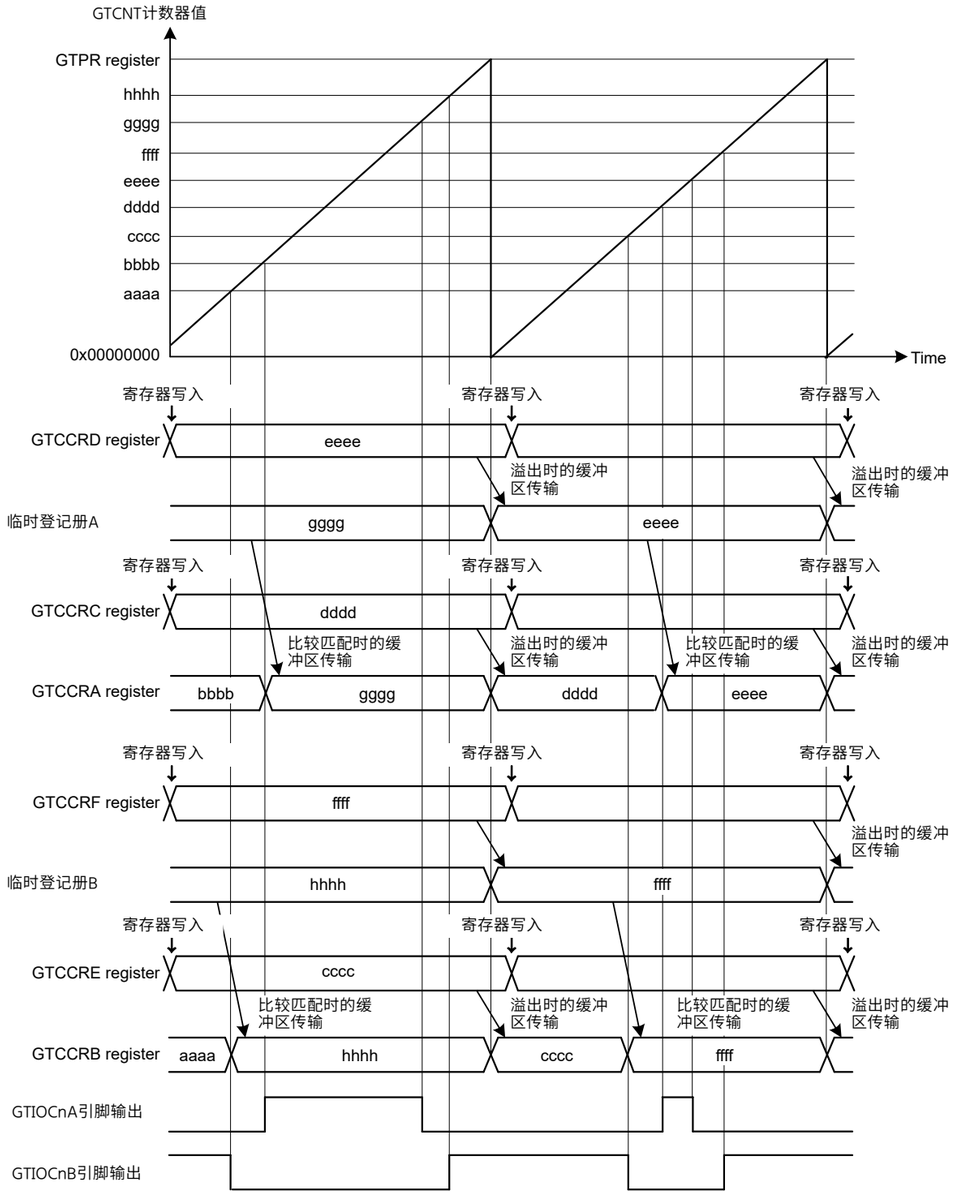
引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，以进行比较匹配和循环结束。当GTBER.CCRSWT位在计数操作停止时设置为1时，缓冲区被强制从GTCCRD寄存器传送到临时寄存器A，并从GTCCRF寄存器传送到临时寄存器B。通过设置GTDTCR和GTDVU，比较匹配值带有死区时间的负相位波形可以自动设置为GTCCRB。

图21.20显示了锯齿波单次脉冲模式操作的示例，表21.16显示了设置锯齿波单次脉冲模式的示例。



Note: The base address of registers are the same.

Figure 21.20 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end



Note: 寄存器的基地址相同。

Figure 21.20 具有递增计数、低输出的锯齿波单次脉冲模式操作示例 GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB比较匹配，并在循环结束时保留输出

Table 21.16 Example setting for saw-wave one-shot pulse mode

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.20, 001b (saw-wave one-shot pulse mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.20, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.20, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set compare match value	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
9	Set forcible buffer transfer	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly.
10	Set buffer value	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
11	Start count operation	Set GTCR.CST to 1 to start count operation.
12	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin transition in one cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.

Note: n: 0 to 9
m: A, B

21.3.3.3 Triangle-wave PWM mode 1 (32-bit transfer at trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0 to 9) when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.21 shows an example of a triangle-wave PWM mode 1 operation, and Table 21.17 shows an example for setting a triangle-wave PWM mode 1.

Table 21.16 锯波单发脉冲模式设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.20中，设置了001b（锯波单次脉冲模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.20中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.20中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配值	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换，在GTCCRE和GTCCRF中设置GTIOCnB引脚转换。
9	设置强制缓冲区传输	将GTBER.CCRSWT设置为1以强制传输缓冲寄存器数据。
10	设置缓冲区值	对于缓冲操作，将GTIOCnA引脚转换设置为在当前周期后的一个周期内GTCCRC和GTCCRD以及GTCCRE和GTCCRF中的GTIOCnB引脚转换。
11	开始计数操作	将GTCR.CST设置为1以启动计数操作。
12	为每个周期设置缓冲区值	对于缓冲操作，将GTIOCnA引脚转换设置为在当前周期后的一个周期内GTCCRC和GTCCRD以及GTCCRE和GTCCRF中的GTIOCnB引脚转换。

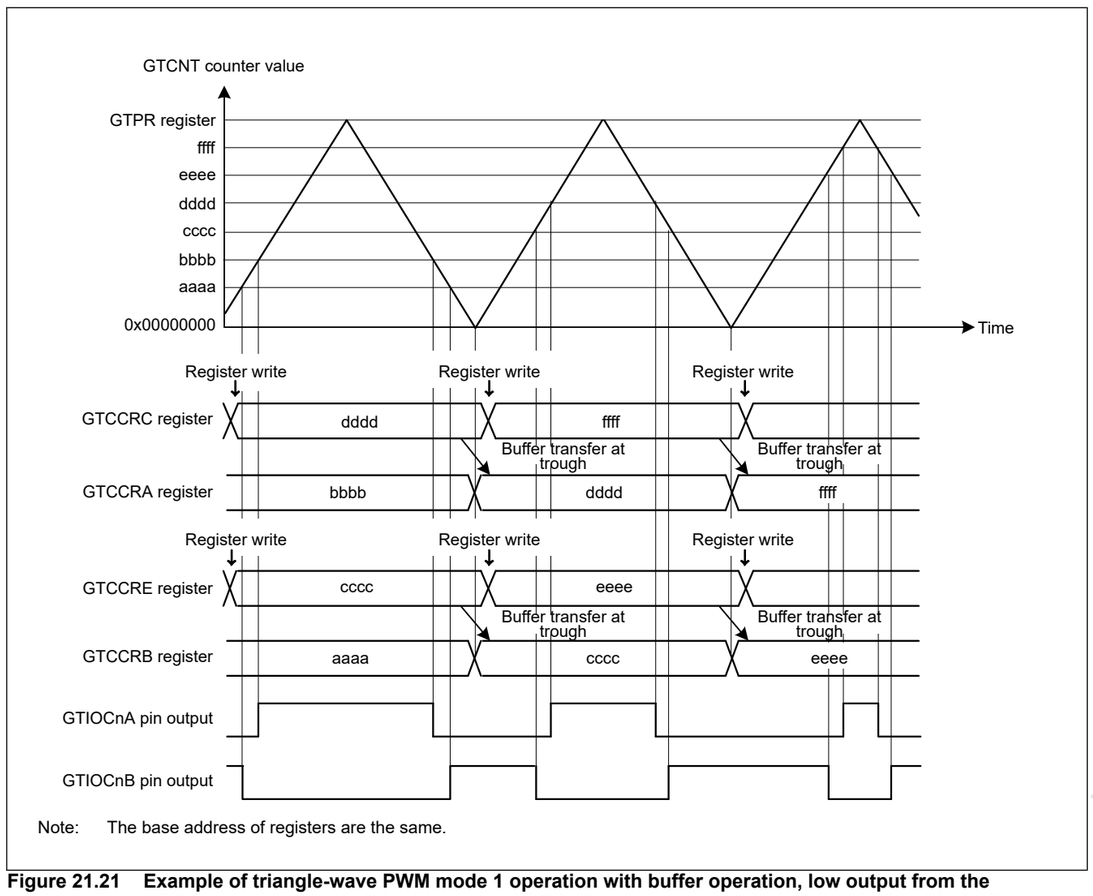
Note: n: 0 to 9
m: A, B

21.3.3.3 三角波PWM模式1（波谷32位传输）

三角波PWM模式1是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0至9）。在槽中进行缓冲转移。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图21.21显示了三角波PWM模式1操作的示例，表21.17显示了设置三角波PWM模式1的示例。

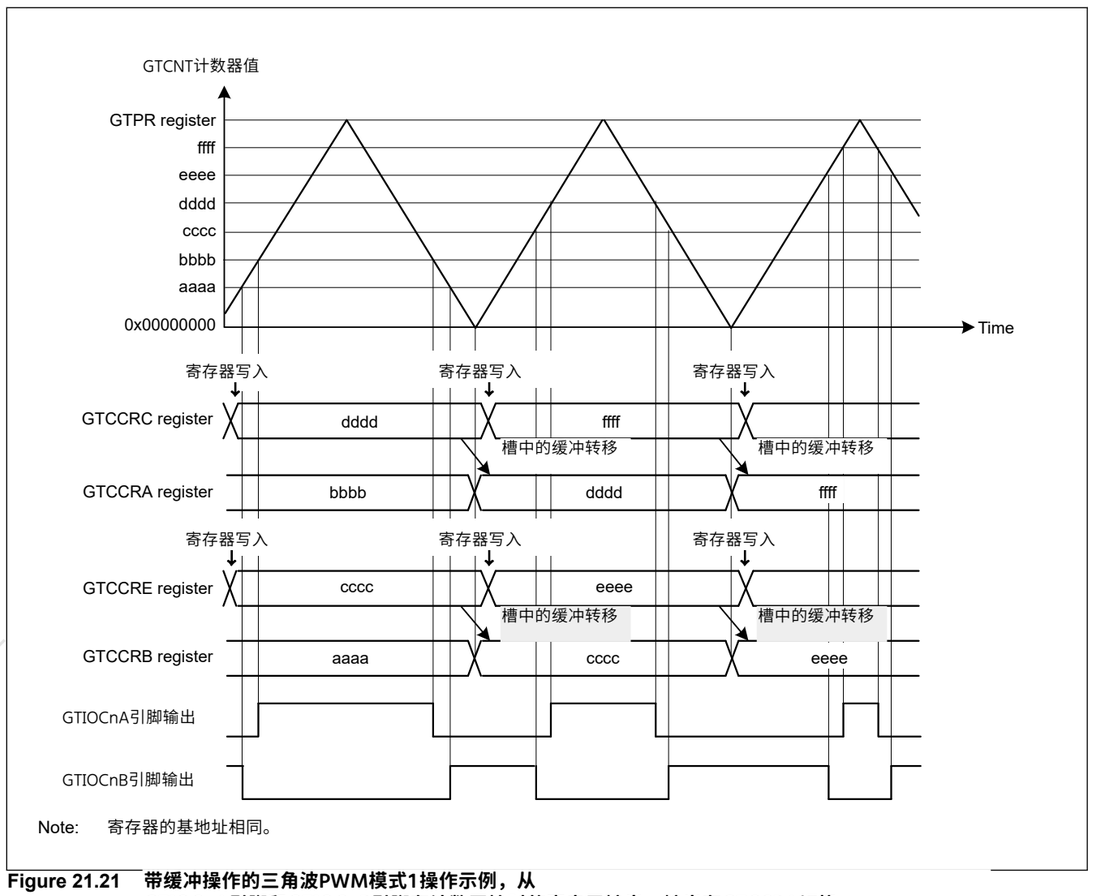


Note: The base address of registers are the same.

Figure 21.21 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB register compare match, and output retained at cycle end

Table 21.17 Example setting for triangle-wave PWM mode 1 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.21, 100b (triangle-wave PWM mode 1) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.21, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 21.21, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
8	Set compare match value	Set the GTIOCnA pin and GTIOCnB pin transitions in GTCCRA and GTCCRB, respectively.
9	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.



Note: 寄存器的基地址相同。

Figure 21.21 带缓冲操作的三角波PWM模式1操作示例，从GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB寄存器比较匹配，并在循环结束时保留输出

Table 21.17 三角波PWM模式1的设置示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.21中，设置了100b（三角波PWM模式1）。
2	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.21中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图21.21中，CCRA[1:0]=01b和CCRB[1:0]=01b。
8	设置比较匹配值	分别在GTCCRA和GTCCRB中设置GTIOCnA引脚和GTIOCnB引脚转换。
9	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

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Table 21.17 Example setting for triangle-wave PWM mode 1 (2 of 2)

No.	Step Name	Description
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value for each cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 2 cycles after the current cycle in GTCCRD and GTCCRF, respectively.

Note: n: 0 to 9
m: A, B

21.3.3.4 Triangle-wave PWM mode 2 (32-bit transfer at crest and trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0 to 9) when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.22 shows an example of triangle-wave PWM mode 2 operation, and Table 21.18 shows an example for setting triangle-wave PWM mode 2.

Table 21.17 三角波PWM模式1(2of2)的示例设置

No.	步骤名称	Description
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。
11	为每个周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的2个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

Note: n: 0 to 9
m: A, B

21.3.3.4 三角波PWM模式2（波峰和波谷32位传输）

与三角波PWM模式1类似，在三角波PWM模式2中，周期在GTPR中设置。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0至9）。缓冲转移在波峰和波谷进行。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图21.22显示了三角波PWM模式2操作的示例，表21.18显示了设置三角波PWM模式2的示例。

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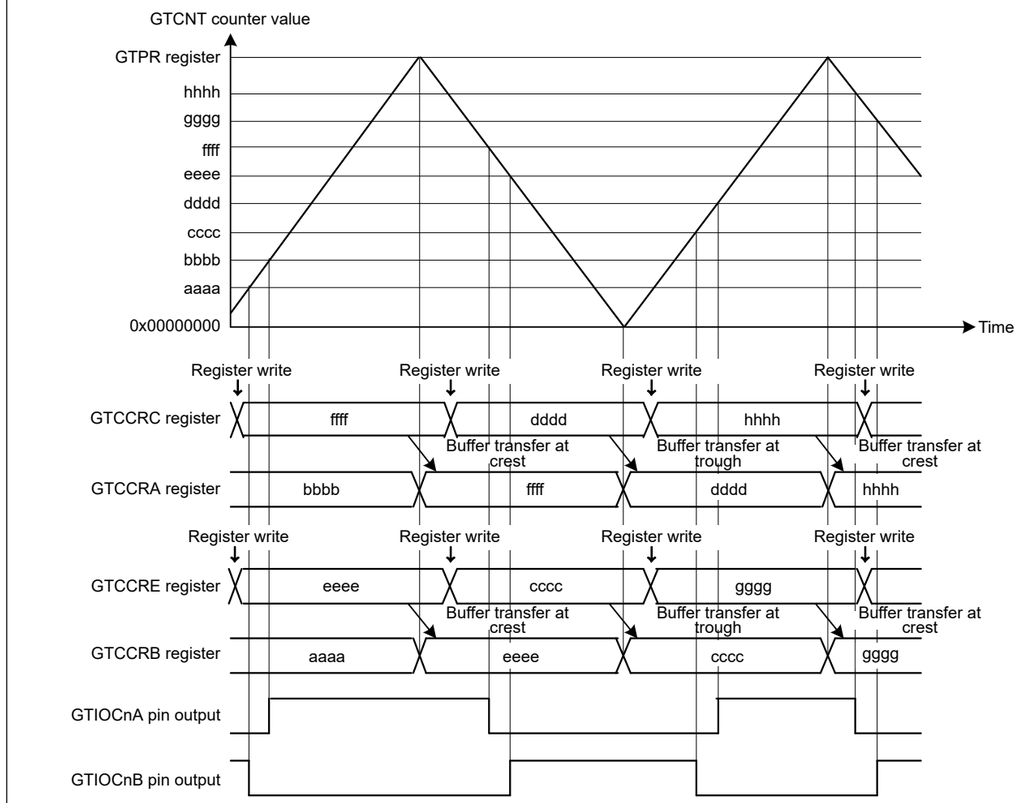
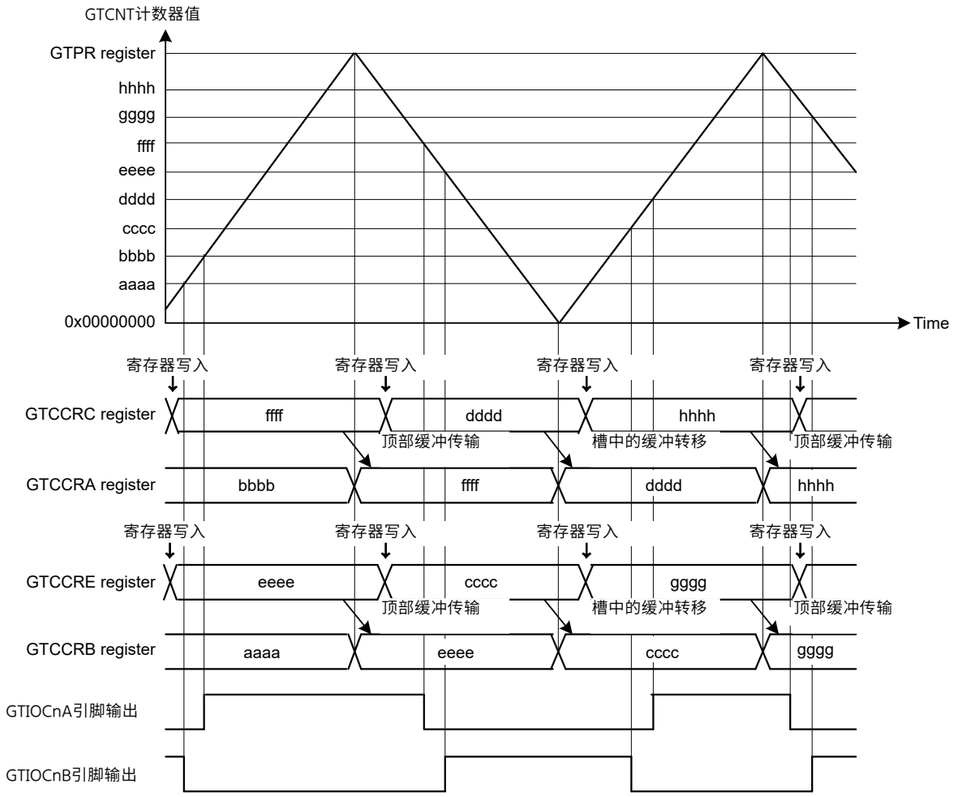


Note: The base address of registers are the same.

Figure 21.22 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/ GTCCRB compare match, and output retained at cycle end

Table 21.18 Example for setting triangle-wave PWM mode 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.22, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.22, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation	Set buffer operation with CCRA and CCRB in GTBER. In Figure 21.22, CCRA[1:0] = 01b and CCRB[1:0] = 01b.
8	Set compare match value	Set the GTIOCnA pin and GTIOCnB pin transitions in GTCCRA and GTCCRB, respectively.



Note: 寄存器的基地址相同。

Figure 21.22 带缓冲操作的三角波PWM模式2操作示例，从GTIOCnA引脚和GTIOCnB引脚在计数开始时的高电平输出，输出在GTCCRA切换GTCCRB比较匹配，并在循环结束时保留输出

Table 21.18 设置三角波PWM模式2的示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.22中，设置了101b（三角波PWM模式2）。
2	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.22中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	设置缓冲操作	在GTBER中使用CCRA和CCRB设置缓冲区操作。 在图21.22中，CCRA[1:0]=01b和CCRB[1:0]=01b。
8	设置比较匹配值	分别在GTCCRA和GTCCRB中设置GTIOCnA引脚和GTIOCnB引脚转换。

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Table 21.18 Example for setting triangle-wave PWM mode 2 (2 of 2)

No.	Step Name	Description
9	Set buffer value	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in half cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF, respectively.
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value for each half cycle	For buffer operation, set the GTIOCnA pin and GTIOCnB pin transitions in half cycle after the current cycle in GTCCRC and GTCCRE, respectively. For double buffer operation, also set the GTIOCnA pin and GTIOCnB pin transitions in 1 cycle after the current cycle in GTCCRD and GTCCRF, respectively.

Note: n: 0 to 9
m: A, B

21.3.3.5 Triangle-wave PWM mode 3 (64-bit transfer at trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA pin or GTIOCnB pin (n = 0 to 9) at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from the following:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggled output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR and GTDVU, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.23 shows an example of triangle-wave PWM mode 3 operation, and Table 21.19 shows an example for setting triangle-wave PWM mode 3.

Table 21.18 设置三角波PWM模式2的示例(2of2)

No.	步骤名称	Description
9	设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的半个周期中设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。
11	为每个半周期设置缓冲区值	对于缓冲操作，分别在GTCCRC和GTCCRE中的当前周期之后的半个周期中设置GTIOCnA引脚和GTIOCnB引脚转换。对于双缓冲器操作，还分别在GTCCRD和GTCCRF中的当前周期之后的1个周期内设置GTIOCnA引脚和GTIOCnB引脚转换。

Note: n: 0 to 9
m: A, B

21.3.3.5 三角波PWM模式3（波谷64位传输）

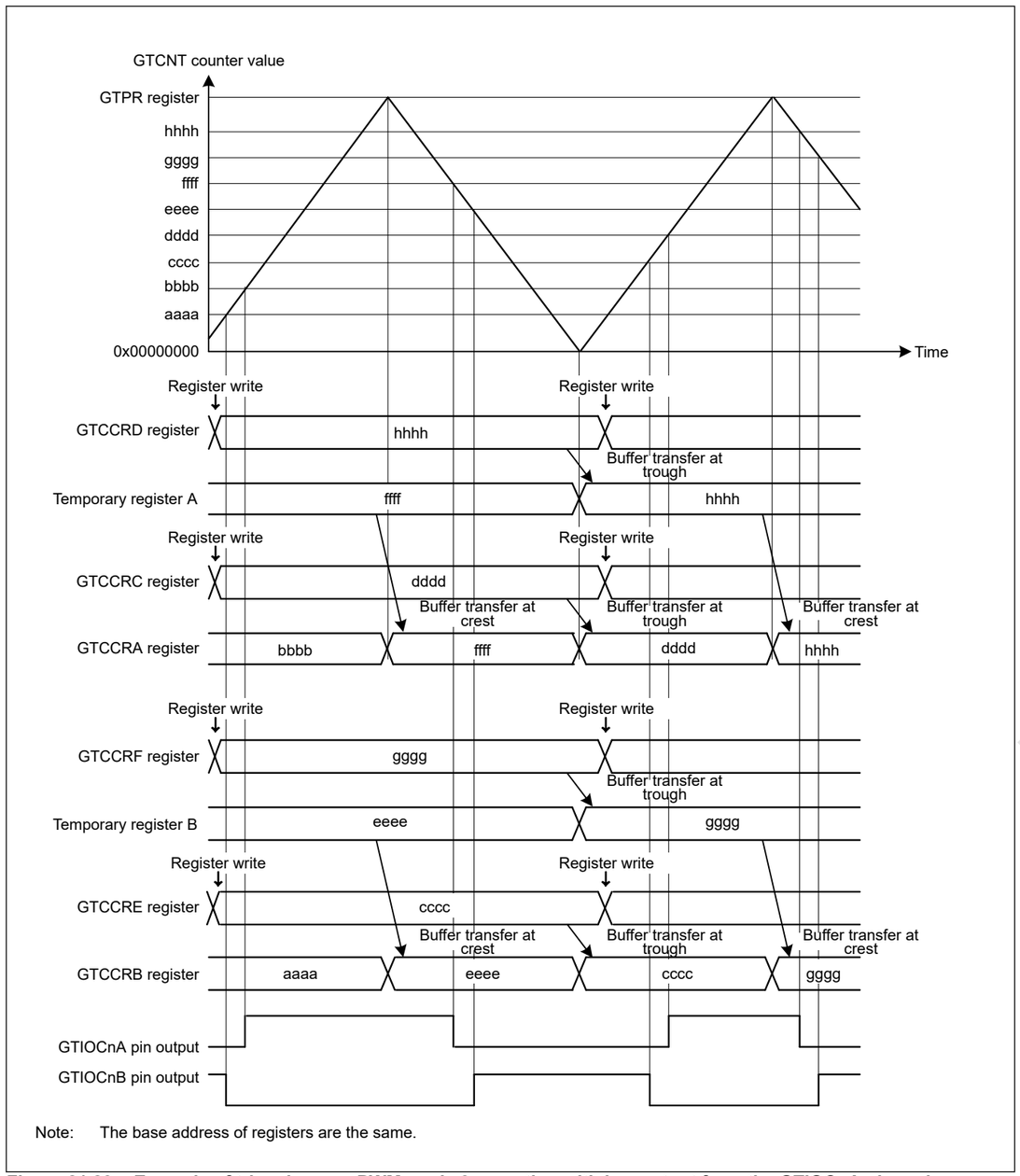
三角波PWM模式3是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，在固定缓冲器操作的GTCCRA或GTCCRB比较匹配时，PWM波形输出到GTIOCnA引脚或GTIOCnB引脚（n=0至9）。三角波PWM模式3中的缓冲操作与通常的缓冲操作不同。缓冲区传输从以下位置执行：

●GTCCRC到GTCCRA处于低谷
●GTCCRE至GTCCRB处于低谷
●GTCCRD到谷底临时寄存器A
●GTCCRF到波谷的临时寄存器B
●顶部为GTCCRA的临时寄存器A
●在顶部的GTCCRB临时寄存器B。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR和GTDVU，可以自动将带死区时间的反相波形的比较匹配值设置为GTCCRB。

图21.23显示了三角波PWM模式3操作的示例，表21.19显示了设置三角波PWM模式3的示例。

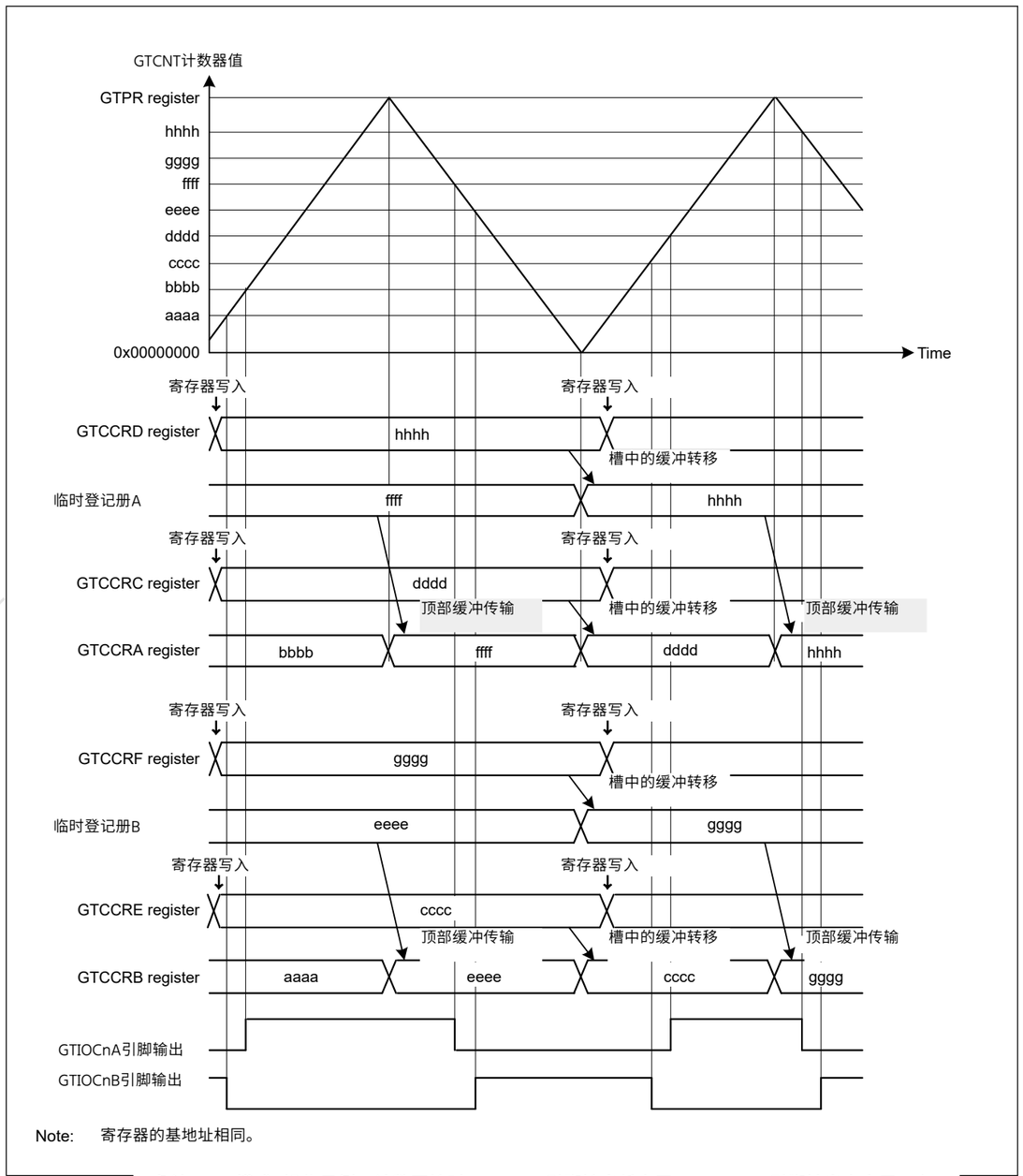


Note: The base address of registers are the same.

Figure 21.23 Example of triangle-wave PWM mode 3 operation with low output from the GTIOCnA pin and high output from the GTIOCnB pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end

Table 21.19 Example setting for triangle-wave PWM mode 3 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.23, 110b (triangle-wave PWM mode 3) is set.



Note: 寄存器的基地址相同。

Figure 21.23 三角波PWM模式3操作示例，计数开始时GTIOCnA引脚输出低电平，GTIOCnB引脚输出高电平，在GTCCRAGTCCRB比较匹配时切换输出，并在周期结束时保持输出

Table 21.19 三角波PWM模式3的设置示例（1of2）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.23中，设置了110b（三角波PWM模式3）。

Table 21.19 Example setting for triangle-wave PWM mode 3 (2 of 2)

No.	Step Name	Description
2	Select count clock	Select the count clock with GTCR.TPCS[3:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.23, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set compare match value	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
8	Set forcible buffer transfer	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly.
9	Set buffer value	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.
10	Start count operation	Set GTCR.CST to 1 to start count operation.
11	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD and the GTIOCnB pin transition in GTCCRE and GTCCRF.

Note: n: 0 to 9
m: A, B

21.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time value (GTDVU value) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB. In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCRA = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 21.7.3. GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B). The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers that are used for calculating the automatic dead time value are updated.

When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 21.20.

The adjusted value for the negative waveform is set for GTCCRB automatically.

The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

Table 21.20 Adjustment of the Waveform Change Point When a Dead-Time Error Occurs

Mode	Count Direction	Period	Condition for Dead Time Error	Change Point of the Positive-Phase Waveform after Adjustment	Change Point of the Negative-Phase Waveform after Adjustment
Sawtooth-wave one-shot pulse mode	Up-counting	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
	Down-counting	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVU < 0	GTDVU	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVU < 0	GTDVU	0

Figure 21.24 to Figure 21.27 show examples of automatic dead time setting function operation. Table 21.21 and Table 21.22 show the setting examples.

Table 21.19 三角波PWM模式3(2of2)的示例设置

No.	步骤名称	Description
2	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.23中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	设置比较匹配值	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换，在GTCCRE和GTCCRF中设置GTIOCnB引脚转换。
8	设置强制缓冲区传输	将GTBER.CCRSWT设置为1以强制传输缓冲寄存器数据。
9	设置缓冲区值	在GTCCRC和GTCCRD中的当前周期和GTCCRE和GTCCRF中的GTIOCnB引脚转换之后的1个周期内设置GTIOCnA引脚转换。
10	开始计数操作	将GTCR.CST设置为1以启动计数操作。
11	为每个周期设置缓冲区值	在GTCCRC和GTCCRD中的当前周期和GTCCRE和GTCCRF中的GTIOCnB引脚转换之后的1个周期内设置GTIOCnA引脚转换。

Note: n: 0 to 9
m: A, B

21.3.4 自动死区时间设置功能

通过设置GTDTCR，可以自动将正波形的比较匹配值（GTCCRA值）和指定死区时间值（GTDVU值）得到的负波形与死区时间的比较匹配值设置为GTCCRB。自动死区时间设置功能可用于锯波单次脉冲模式和所有三角形PWM modes.

使用自动死区时间设置功能时，禁止写入GTCCRB。超出周期的死区时间设置也被禁止。自动死区时间设置的值可以从GTCCRB中读取。在三角波模式下，当设置GTCCRA=0或GTCCRA≥GTCCRA时，死区时间超出周期时，输出保护功能保持输出电平。详见21.7.3节。GTIOCnm引脚输出否定控制（n=0到9，m=A，B）。当用于计算自动死区时间值的寄存器被更新时，在下一个时钟周期计数时执行GTCCRB的自动死区时间值设置。

当出现死区时间错误时，调整正负波形的比较匹配值以生成具有死区时间的波形，如表21.20所示。

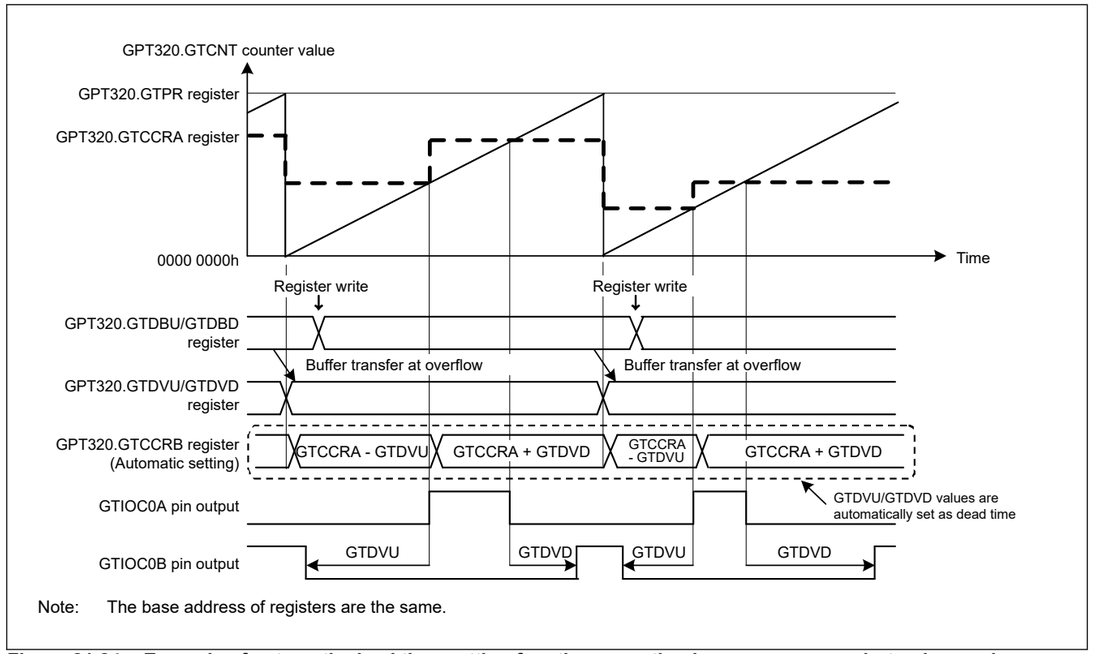
负波形的调整值自动为GTCCRB设置。

正波形的调整值用作内部信号，而不是为GTCCRA设置的。

Table 21.20 发生死区错误时波形变化点的调整

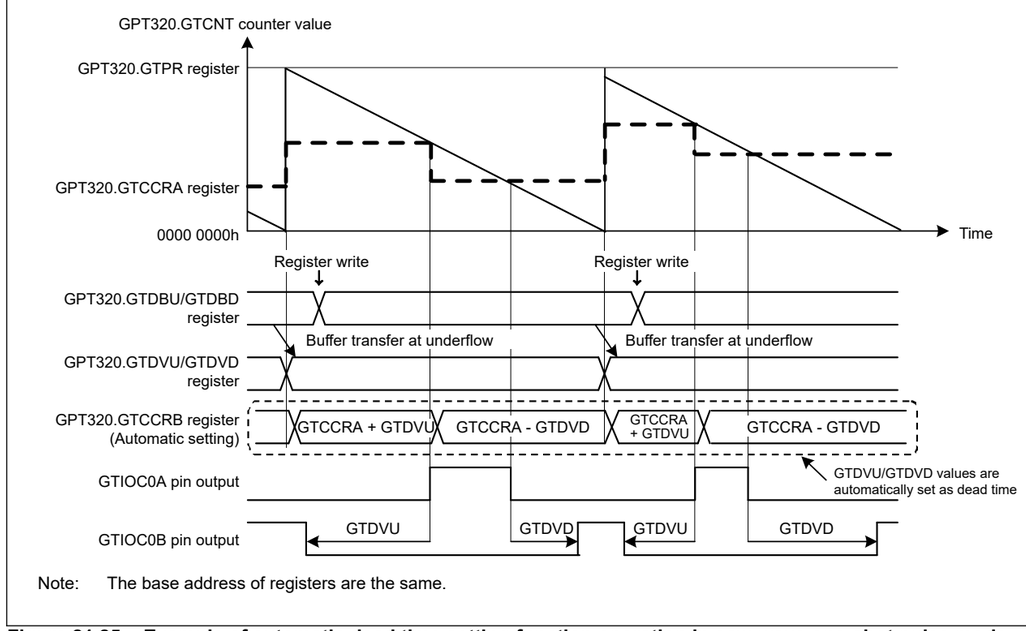
Mode	Count Direction	Period	死区时间错误的条件	变化点 正相波形后 Adjustment	变化点 后的负相位波形 Adjustment
锯齿波单发脉冲模式	Up-counting	上半场	GTCCRA - GTDVU < 0	GTDVU	0
		下半场	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
	Down-counting	上半场	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		下半场	GTCCRA - GTDVU < 0	GTDVU	0
Triangle-wave PWM mode 1/2/3	Up-counting	(First half)	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down-counting	(Second half)	GTCCRA - GTDVU < 0	GTDVU	0

图21.24至图21.27显示了自动死区时间设置功能操作的示例。表21.21和表21.22显示了设置示例。



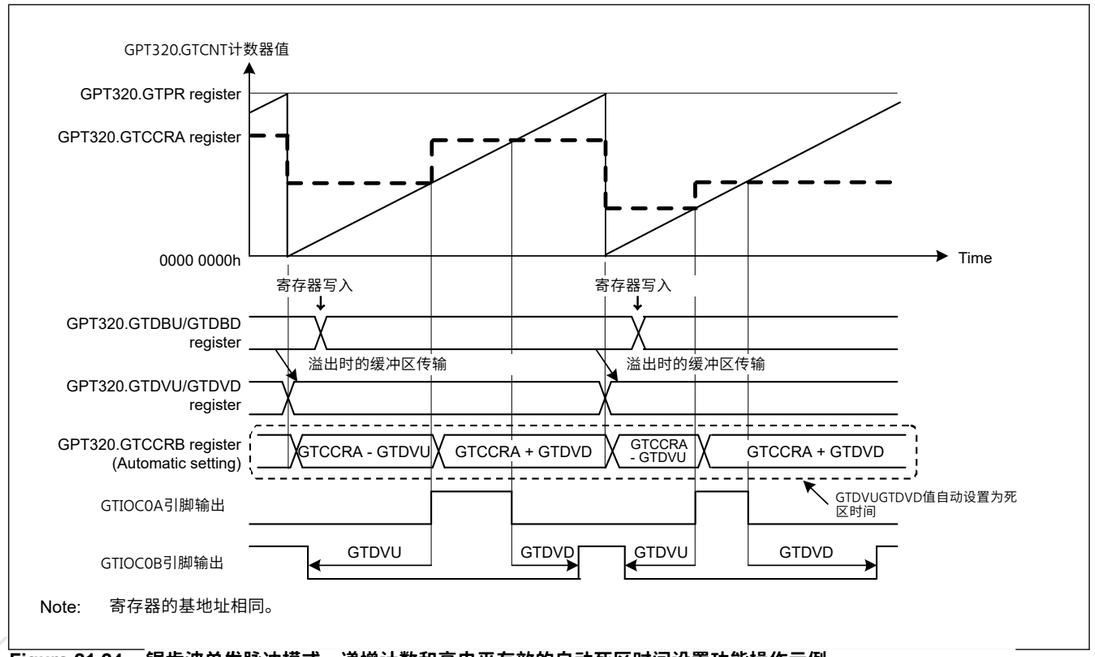
Note: The base address of registers are the same.

Figure 21.24 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, up-counting, and active-high



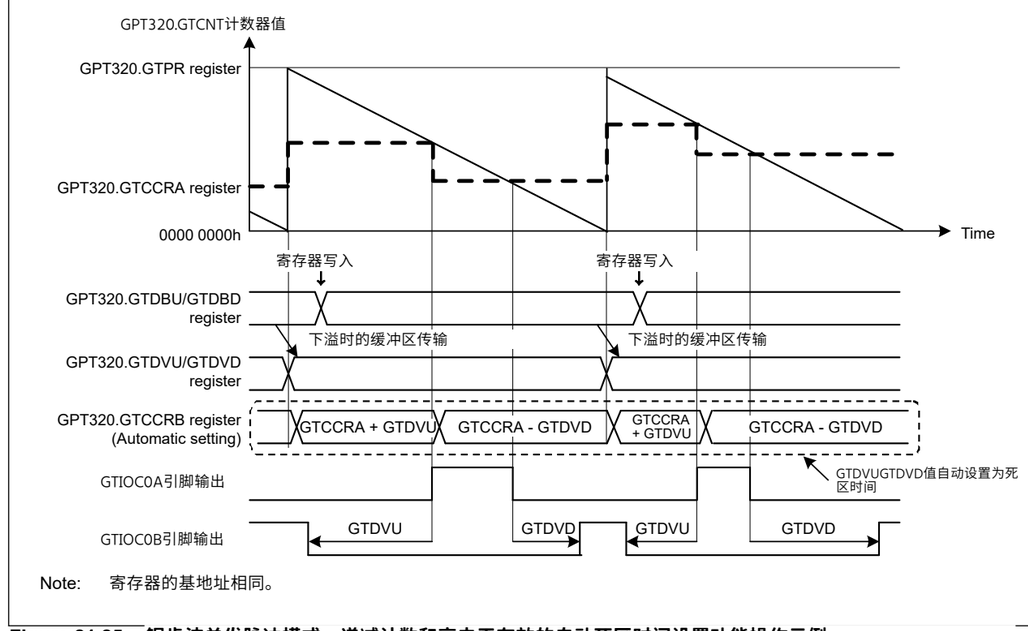
Note: The base address of registers are the same.

Figure 21.25 Example of automatic dead time setting function operation in saw-wave one-shot pulse mode, down-counting, and active-high



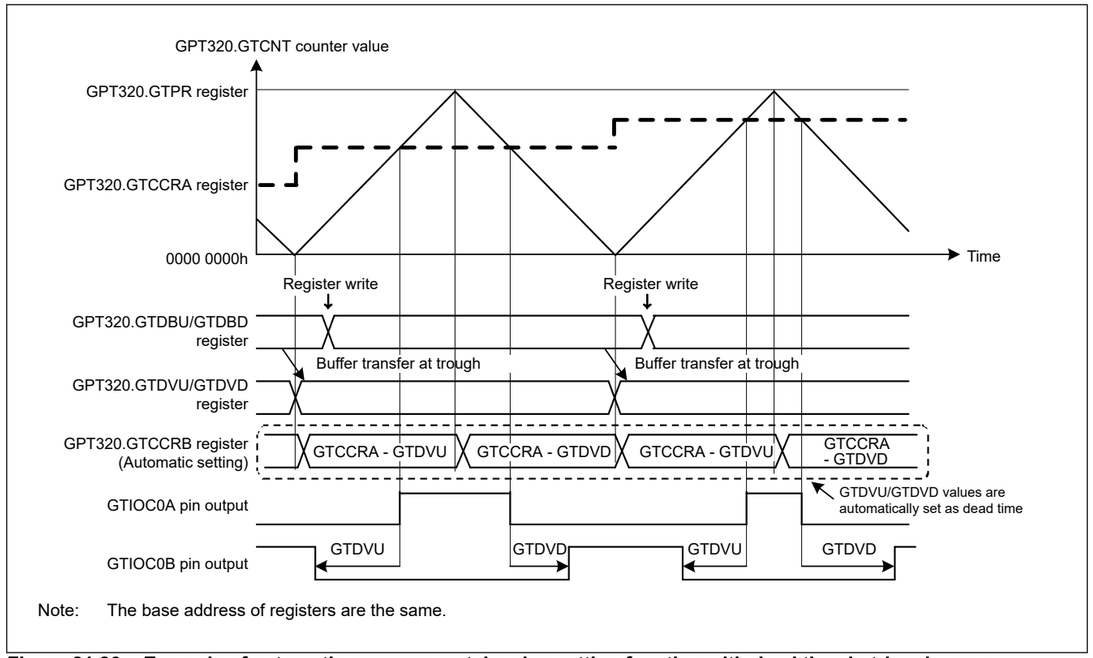
Note: 寄存器的基地址相同。

Figure 21.24 锯齿波单发脉冲模式、递增计数和高电平有效的自动死区时间设置功能操作示例



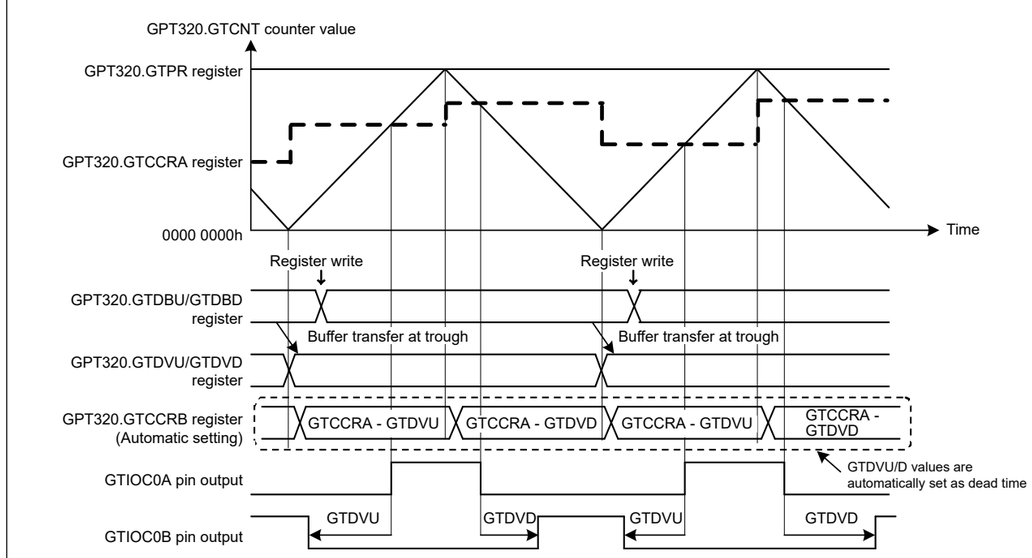
Note: 寄存器的基地址相同。

Figure 21.25 锯齿波单发脉冲模式、递减计数和高电平有效的自动死区时间设置功能操作示例



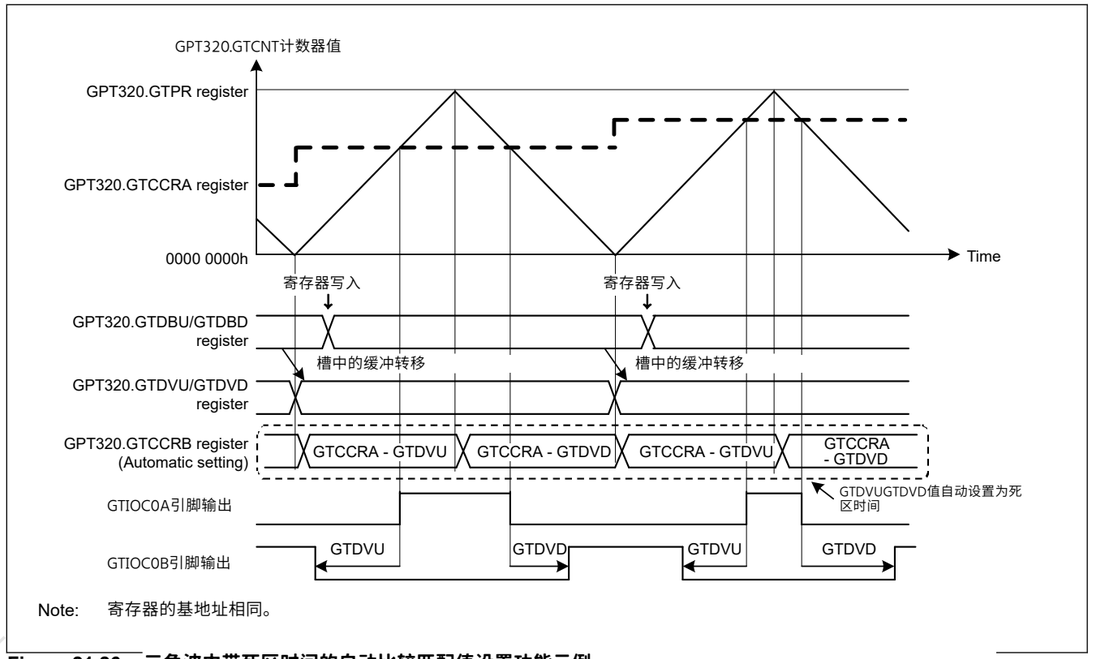
Note: The base address of registers are the same.

Figure 21.26 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 1, and active-high



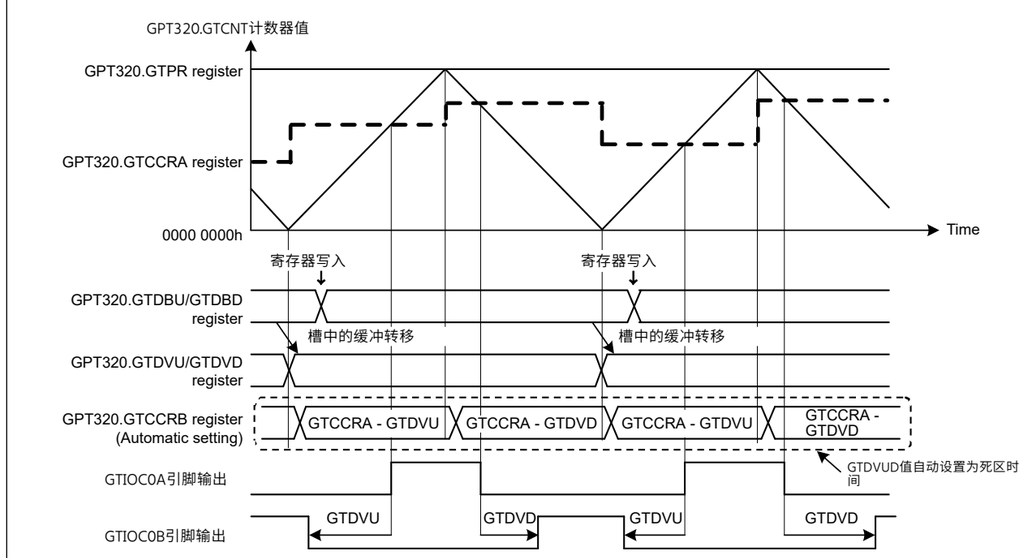
Note: The base address of registers are the same.

Figure 21.27 Example of automatic compare-match value setting function with dead time in triangle-wave PWM mode 2 or 3, and active-high



Note: 寄存器的基地址相同。

Figure 21.26 三角波中带死区时间的自动比较匹配值设置功能示例 PWM模式1，高电平有效



Note: 寄存器的基地址相同。

Figure 21.27 三角波中带死区时间的自动比较匹配值设置功能示例 PWM模式2或3，高电平有效

Table 21.21 Example setting for automatic dead time setting function in saw-wave one-shot pulse mode, and triangle-wave PWM mode 3

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.24 and Figure 21.25, 001b (saw-wave one-shot pulse mode) is set. In Figure 21.27, 110b (triangle-wave PWM mode 3) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.24, 01b is set after 11b is set in GTUDDTYC[1:0] (up count). In Figure 21.25, 00b is set after 10b is set in GTUDDTYC[1:0] (down count).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter.
6	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.24, Figure 21.26, and Figure 21.27, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
7	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
8	Set buffer value for compare match	Set the GTIOCnA pin transition immediately after the count start in GTCCRC and GTCCRD.
9	Set forcible buffer transfer for compare match	Set GTBER.CCRSWT to 1 to transfer buffer register data forcibly to GTCCRA.
10	Set buffer value for compare match	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD.
11	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
12	Set dead time value	Set the dead time value in GTDVU.
13	Start count operation	Set GTCR.CST to 1 to start count operation.
14	Set buffer value for each cycle	Set the GTIOCnA pin transition in 1 cycle after the current cycle in GTCCRC and GTCCRD.

Note: n: 0 to 9
m: A, B

Table 21.22 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2 (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.26, 100b (triangle-wave PWM mode 1) is set. In Figure 21.27, 101b (triangle-wave PWM mode 2) is set.
2	Select count clock	Select the count clock with GTCR.TPCS[3:0].
3	Set cycle	Set the cycle in GTPR.
4	Set initial value for counter	Set the initial value in the GTCNT counter.
5	Set GTIOCnm pin function	Set the GTIOCnm pin function with GTIOA[4:0] and GTIOB[4:0] in GTIOR. In Figure 21.26 and Figure 21.27, GTIOA[4:0] = 00011b and GTIOB[4:0] = 10011b.
6	Enable GTIOCnm pin output	Set to enable the GTIOCnm pin output with OAE and OBE in GTIOR.
7	Set buffer operation for compare match	Set buffer operation with CCRA in GTBER.
8	Set compare match value	Set the GTIOCnA pin transition in GTCCRA.
9	Set buffer value for compare match	For buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC. For double buffer operation, also set the GTIOCnA pin transition in 2 cycles after the current cycle (in triangle-wave PWM mode 1) or 1 cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRD.
10	Set automatic dead time setting function	Set GTDTCR.TDE to 1 to enable the automatic dead time setting function.
11	Set dead time value	Set the dead time value in GTDVU.
12	Start count operation	Set GTCR.CST to 1 to start count operation.

Table 21.21 锯齿波一次性脉冲模式和三角波PWM模式3中自动死区时间设置功能的设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。在图21.24和图21.25中，设置了001b（锯波单发脉冲模式）。在图21.27中，设置了110b（三角波PWM模式3）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.24中，在GTUDDTYC[1:0]中设置了11b之后设置了01b（向上计数）。在图21.25中，在GTUDDTYC[1:0]中设置了10b之后设置了00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。
6	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.24、图21.26和图21.27中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
7	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
8	设置比较匹配的缓冲区值	在GTCCRC和GTCCRD中计数开始后立即设置GTIOCnA引脚转换。
9	为比较匹配设置强制缓冲区传输	将GTBER.CCRSWT设置为1以强制将缓冲寄存器数据传输到GTCCRA。
10	设置比较匹配的缓冲区值	在GTCCRC和GTCCRD中的当前周期之后的1个周期内设置GTIOCnA引脚转换。
11	设置自动死区时间设置功能	将GTDTCR.TDE设置为1以启用自动死区时间设置功能。
12	设置死区时间值	在GTDVU中设置死区时间值。
13	开始计数操作	将GTCR.CST设置为1以启动计数操作。
14	为每个周期设置缓冲区值	在GTCCRC和GTCCRD中的当前周期之后的1个周期内设置GTIOCnA引脚转换。

Note: n: 0 to 9
m: A, B

Table 21.22 三角波PWM模式1或2(1of2)中自动死区时间设置功能的设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。在图21.26中，设置了100b（三角波PWM模式1）。在图21.27中，设置了101b（三角波PWM模式2）。
2	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
3	设置周期	在GTPR中设置循环。
4	设置计数器的初始值	在GTCNT计数器中设置初始值。
5	设置GTIOCnm引脚功能	使用GTIOR中的GTIOA[4:0]和GTIOB[4:0]设置GTIOCnm引脚功能。 在图21.26和图21.27中，GTIOA[4:0]=00011b和GTIOB[4:0]=10011b。
6	启用GTIOCnm引脚输出	设置为在GTIOR中使用OAE和OBE启用GTIOCnm引脚输出。
7	为比较匹配设置缓冲区操作	在GTBER中使用CCRA设置缓冲区操作。
8	设置比较匹配值	在GTCCRA中设置GTIOCnA引脚转换。
9	设置比较匹配的缓冲区值	对于缓冲操作，在GTCCRC中将GTIOCnA引脚转换设置为当前周期后的1个周期（三角波PWM模式1）或当前周期后的半个周期（三角波PWM模式2）。对于双缓冲器操作，在GTCCRD中还设置GTOCnA引脚在当前周期后2个周期（三角波PWM模式1）或当前周期后1个周期（三角波PWM模式2）。
10	设置自动死区时间设置功能	将GTDTCR.TDE设置为1以启用自动死区时间设置功能。
11	设置死区时间值	在GTDVU中设置死区时间值。
12	开始计数操作	将GTCR.CST设置为1以启动计数操作。

Table 21.22 Example setting for automatic dead time setting function in triangle-wave PWM mode 1 or 2 (2 of 2)

No.	Step Name	Description
13	Set buffer value for each cycle	When the compare match register is used for buffer operation, set the GTIOCnA pin transition in 1 cycle after the current cycle (in triangle-wave PWM mode 1) or half cycle after the current cycle (in triangle-wave PWM mode 2) in GTCCRC.

Note: n: 0 to 9
m: A, B

21.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation stops and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation stops, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change even though the UD bit in GTUDDTYC is modified during the count operation. Similarly, even though the GTUDDTYC.UD bit is modified while the count operation stops and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected in the count cycle during up-counting and the GTPR value after the start of down-counting is reflected in the count cycle during down-counting.

Figure 21.28 shows an example of count direction changing function operation.

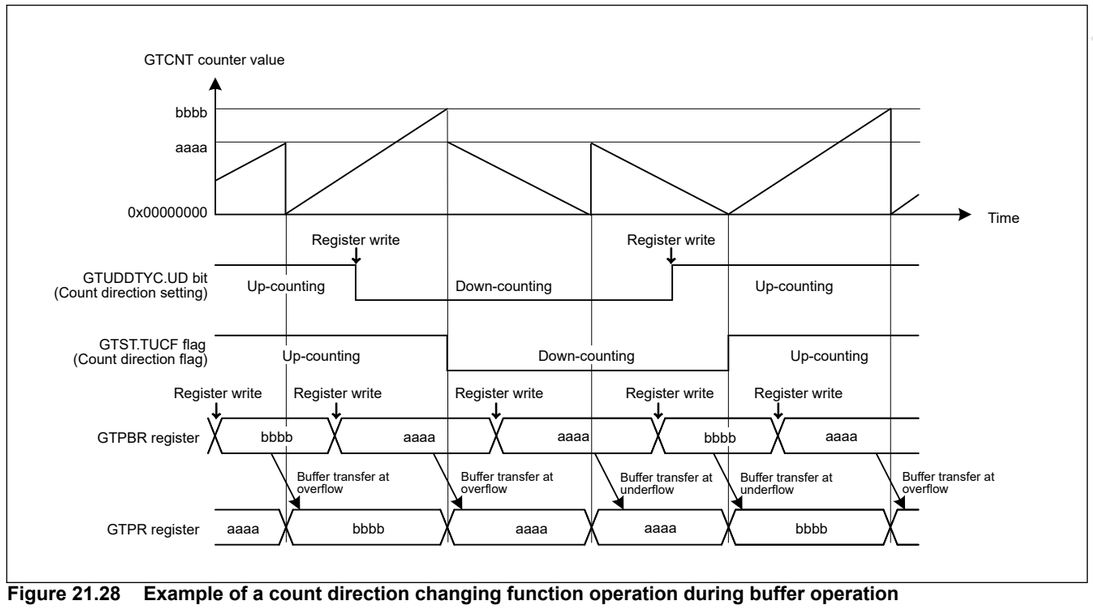


Figure 21.28 Example of a count direction changing function operation during buffer operation

21.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCnA pin and the GTIOCnB pin (n = 0 to 9) are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

Table 21.22 三角波PWM模式1或2(2of2)中自动死区时间设置功能的设置示例

No.	步骤名称	Description
13	为每个周期设置缓冲区值	当比较匹配寄存器用于缓冲操作时，在GTCCRC中设置GTIOCnA引脚在当前周期后1个周期（三角波PWM模式1）或当前周期后半个周期（三角波PWM模式2）.

Note: n: 0 to 9
m: A, B

21.3.5 计数方向改变功能

GTCNT计数器的计数方向可以通过修改GTUDDTYC中的UD位来改变。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC中的UD位，则计数方向会在溢出（在向上计数期间修改时）或下溢（在向下计数期间修改时）改变。如果在计数操作停止时修改GTUDDTYC.UD位且GTUDDTYC.UDF位为0，则GTUDDTYC.UD位的修改不会反映在计数开始时，并且计数方向会在上溢或下溢时改变。如果在计数操作停止时UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

在三角波模式下，即使在计数操作期间修改GTUDDTYC中的UD位，计数方向也不会改变。同样，即使在计数操作停止且GTUDDTYC.UDF位为0时修改GTUDDTYC.UD位，GTUDDTYC.UD位的值也不会反映到计数操作中。如果在计数操作停止时将GTUDDTYC.UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

如果在锯齿波计数操作期间计数方向发生变化，则加计数开始后的GTPR值反映在加计数期间的计数周期中，而减计数开始后的GTPR值反映在计数周期中在向下计数期间。

图21.28显示了计数方向改变功能操作的示例。

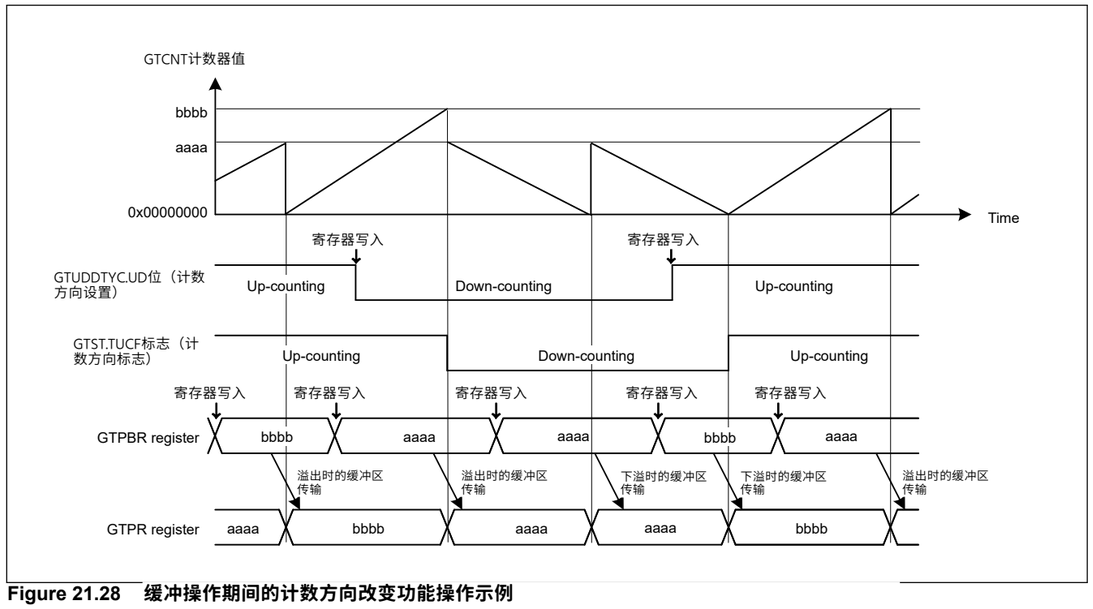


Figure 21.28 缓冲操作期间的计数方向改变功能操作示例

21.3.6 输出占空比0%和100%的功能

GTIOCnA引脚和GTIOCnB引脚（n=0至9）的输出占空比通过更改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位。

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is set to 1 while the count operation is stopped, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected an underflow.

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation stops and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0% or 100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCnA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCnB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 21.23 shows the values of GTIOCnA and GTIOCnB pin output at cycle end.

Table 21.23 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	—	0	0	0	0
10 (high output at cycle end)	—	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 21.29 shows an example of output duty 0% and 100% function.

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映在溢出（在向上计数期间修改时）或下溢（在向下期间修改时-数数）。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在上溢或下溢时发生变化。如果在计数操作停止时GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位设置为1，则

GTUDDTYC.OADTY位或当时的GTUDDTYC.OBDTY位值反映在计数开始时。

在三角波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映为下溢。

如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在下溢时发生变化。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为1时修改了GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比修改将反映在计数开始时。

在执行0%或100%占空比操作时，GPT在内部继续：

- ●执行比较匹配操作
- ●设置比较匹配标志
- ●输出中断
- ●执行缓冲操作。

当控制从0%或100%占空比设置更改为比较匹配时，周期结束时GTIOCnA引脚的输出值由GTIOR.GTIOA[3:2]和GTUDDTYC.OADTYR决定。周期结束时GTIOCnB引脚的输出值由GTIOR.GTIOB[3:2]和GTUDDTYC.OBDTYR决定。

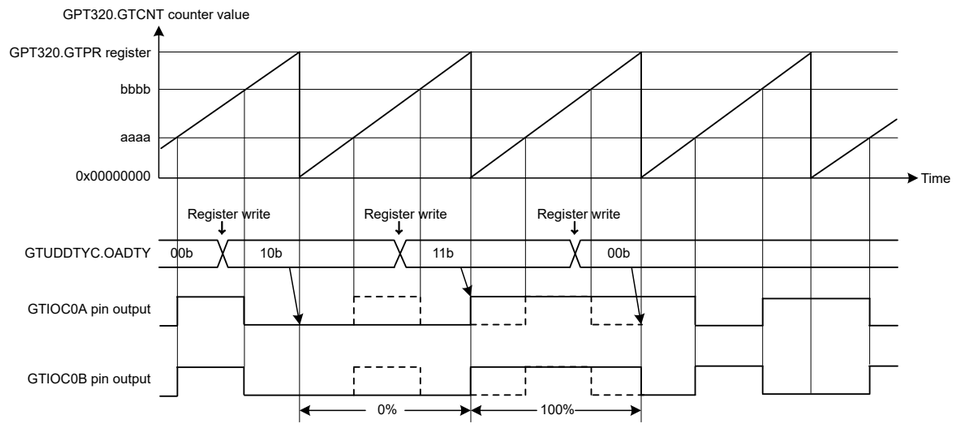
当GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为01b时，输出引脚在周期结束时输出低电平。什么时候GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为10b，输出引脚在周期结束时输出高电平。

GTUDDTYC.OADTYR当GTIOR.GTIOm[3:2]设置为00b（在循环结束时保持输出）或GTIOR.GTIOm[3:2]设置时，选择作为在循环结束时切换的输出保留对象的值到11b（输出在循环结束时切换）。表21.23显示了循环结束时GTIOCnA和GTIOCnB引脚输出的值。

Table 21.23 释放0%或100%占空比设置后的输出值(m=A B)

GTIOR.GTIOm[3:2]	比较被0%或100%占空比设置屏蔽的循环结束时的匹配值	GTUDDTYC.OmDTYR在占空比0%设置		GTUDDTYC.OmDTYR占空比100%设置	
		0	1	0	1
00（循环结束时保留输出）	0	0	0	1	0
	1	0	1	1	1
01（循环结束时输出低）	—	0	0	0	0
10（循环结束时的高输出）	—	1	1	1	1
11（循环结束时切换输出）	0	1	1	0	1
	1	1	0	0	0

图21.29显示了输出占空比0%和100%功能的示例。



Note: The base address of registers are the same.

Note: [Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits:	00011b initial low output, output toggled at compare match, output retained at cycle end
GPT320.GTUDDTYC.OADTYR bit:	0b The function selected by GTIOA[3:2] is applied to the output value when the duty cycle is set after release from 0 to 100% duty-cycle setting.
GPT320.GTIOR.GTIOB[4:0] bits:	00011b initial low output, output toggled at compare match, output retained at cycle end
GPT320.GTUDDTYC.OBDTYR bit:	1 The function of GTIOB[3:2] is applied to the compare match output value which is masked after 0 or 100% duty setting release.

Figure 21.29 Example of output duty 0% and 100% function

21.3.7 Hardware Count Start/Count Stop and Clear Operation

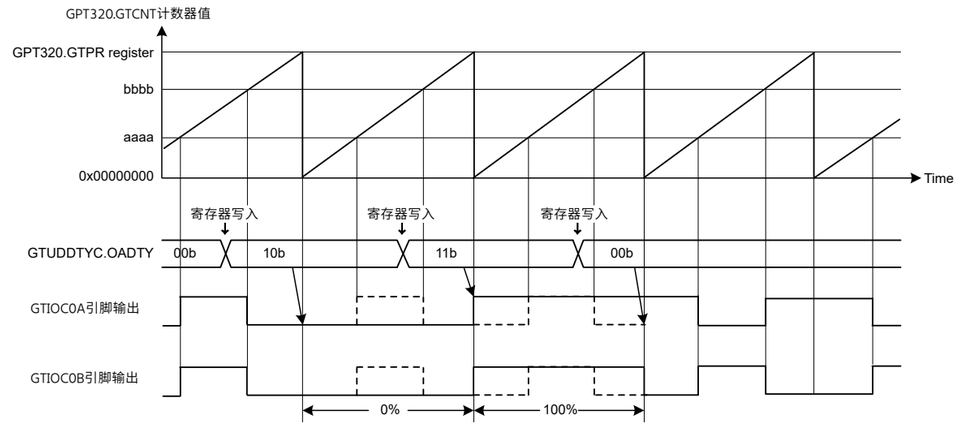
The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCnA and GTIOCnB pin input (n = 0 to 9).

21.3.7.1 Hardware Start Operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 21.30 shows an example of a count start operation by a hardware source. Table 21.24 shows the setting example.



Note: 寄存器的基地址相同。

Note: [Setting examples]

GPT320.GTIOR.GTIOA[4:0] bits:	00011b初始低输出，在比较匹配时切换输出，在循环结束时保持输出
GPT320.GTUDDTYC.OADTYR bit:	0b在从0到100%占空比设置释放后，当占空比设置时，由GTIOA[3:2]选择的功能应用于输出值。
GPT320.GTIOR.GTIOB[4:0] bits:	00011b初始低输出，在比较匹配时切换输出，在循环结束时保持输出
GPT320.GTUDDTYC.OBDTYR bit:	1GTIOB[3:2]的功能应用于在0或100%占空比设置释放后被屏蔽的比较匹配输出值。

Figure 21.29 输出占空比0%和100%功能示例

21.3.7 硬件计数开始计数停止和清除操作

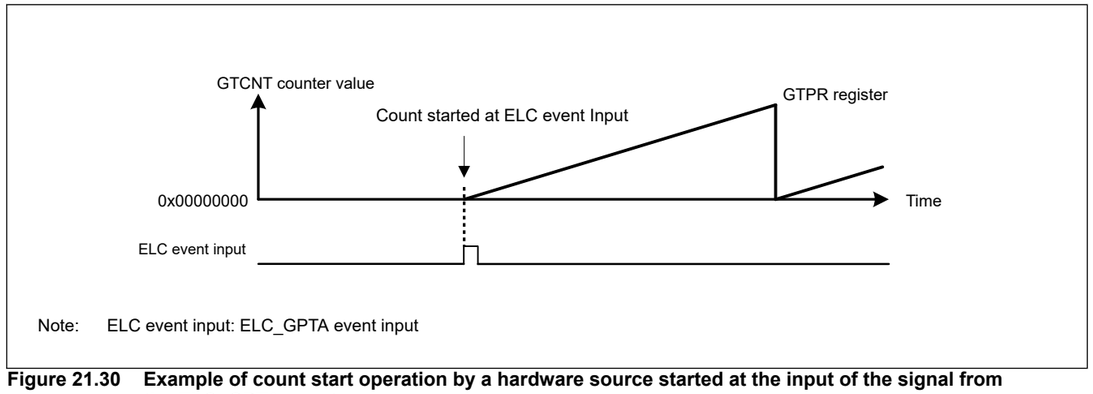
GTCNT计数器可以由以下硬件源启动、停止或清除：

- 外部触发输入
- ELC事件输入
- GTIOCnA和GTIOCnB引脚输入（n=0到9）。

21.3.7.1 硬件启动操作

GTCNT计数器可以通过使用GTSSR选择硬件源来启动。

图21.30显示了一个硬件源的计数开始操作示例。表21.24显示了设置示例。



Note: ELC event input: ELC_GPTA event input

Figure 21.30 Example of count start operation by a hardware source started at the input of the signal from the ELC_GPTA event

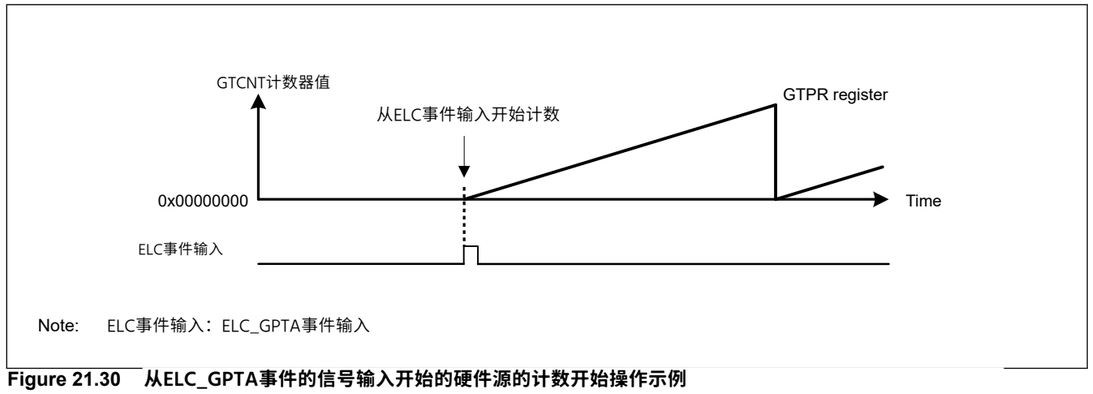
Table 21.24 Example setting for count start operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.30, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.30, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.30, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register. In Figure 21.30, GTSSR.SSELCA = 1
7	Set hardware source operation	Set operation of the hardware source selected by GTSSR register and start counting. In Figure 21.30, the ELC_GPTA event input operation is set.

21.3.7.2 Hardware stop operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR.

Figure 21.31 shows an example of a count stop operation by a hardware source. Table 21.25 shows the setting example. In this example, the count operation stops at the ELC_GPTA event input and restarts at the ELC_GPTB event input.



Note: ELC事件输入：ELC_GPTA事件输入

Figure 21.30 从ELC_GPTA事件的信号输入开始的硬件源的计数开始操作示例

Table 21.24 硬件源的计数开始操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.30中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.30中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.30中，设置了0x00000000。
6	设置硬件计数开始	在GTSSR寄存器中选择启动计数操作的硬件源。 在图21.30中，GTSSR.SSELCA=1
7	设置硬件源操作	设置GTSSR寄存器选择的硬件源的操作并开始计数。 在图21.30中，设置了ELC_GPTA事件输入操作。

21.3.7.2 硬件停止操作

GTCNT计数器可以通过使用GTPSR选择硬件源来停止。

图21.31显示了一个硬件源的计数停止操作示例。表21.25显示了设置示例。在此示例中，计数操作在ELC_GPTA事件输入处停止，并在ELC_GPTB事件输入处重新开始。

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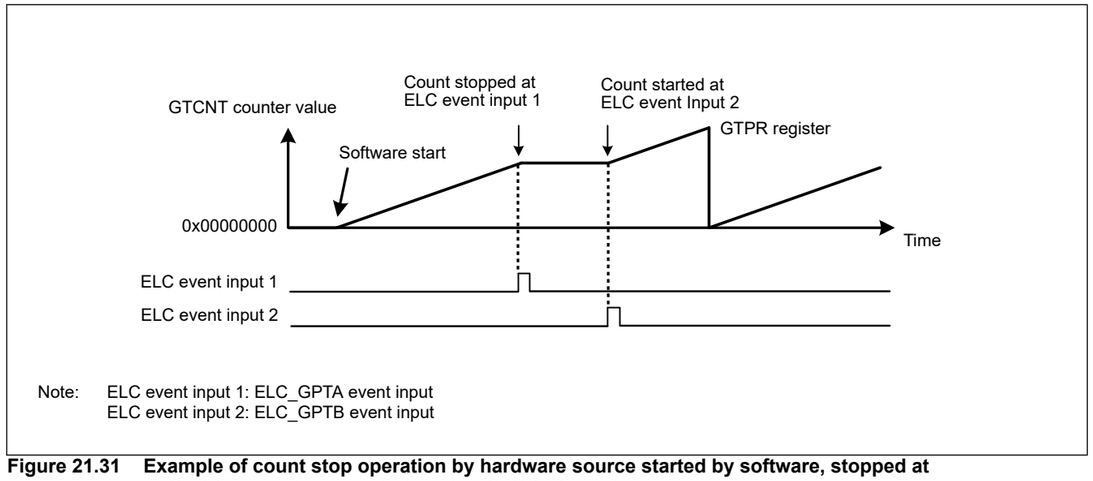


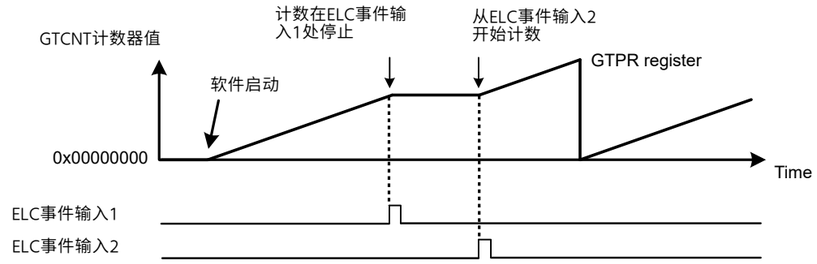
Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 21.31 Example of count stop operation by hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

Table 21.25 Example setting for count stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.31, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.31, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.31, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register, and wait for count start by the hardware source. In Figure 21.31, GTSSR.SSELCB = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 21.31, GTPSR.PSELCA = 1.
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR register or GTPSR register, and start or stop counting. In Figure 21.31, ELC_GPTA input operation and ELC_GPTB input operation are set.

Figure 21.32 shows an example of a count start/stop operation by a hardware source. Table 21.26 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.



Note: ELC事件输入1：ELC_GPTA事件输入ELC事
件输入2：ELC_GPTB事件输入

Figure 21.31 由软件启动的硬件源的计数停止操作示例，停止于ELC_GPTA输入，并在ELC_GPTB输入处重新启动

Table 21.25 硬件源的计数停止操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.31中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.31中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.31中，设置了0x00000000。
6	设置硬件计数开始	在GTSSR寄存器中选择一个开始计数操作的硬件源，等待硬件源开始计数。在图21.31中，GTSSR.SSELCB=1。
7	设置硬件计数停止	在GTPSR寄存器中选择一个停止计数操作的硬件源，等待硬件源停止计数。在图21.31中，GTPSR.PSELCA=1。
8	设置硬件源操作	设置在GTSSR寄存器或GTPSR寄存器中选择的硬件源的操作，并开始或停止计数。在图21.31中，设置了ELC_GPTA输入操作和ELC_GPTB输入操作。

图21.32显示了一个硬件源的计数开始停止操作示例。表21.26显示了设置示例。
在本例中，计数器在外部触发输入GTETRGA的高电平期间运行。

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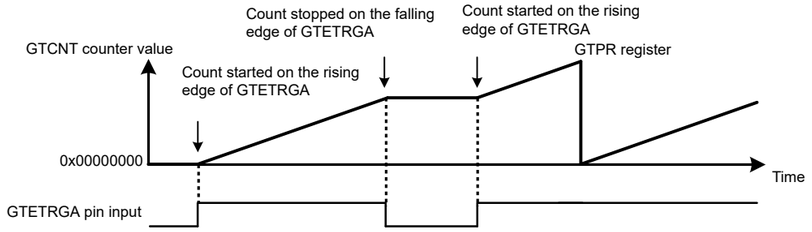


Figure 21.32 Example of count start/stop operation by a hardware source started on the rising edge of GTETRGA pin input, and stopped on the falling edge of GTETRGA pin input

Table 21.26 Example setting for count start/stop operation by a hardware source

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.32, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.32, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in GTPR.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.32, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with GTSSR register and wait for count start by the hardware source. In Figure 21.32, GTSSR.SSGTRGAR = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation with GTPSR register and wait for count stop by the hardware source. In Figure 21.32, GTPSR.PSGTRGAF = 1.
8	Set hardware source operation	Set operation of the hardware source selected in GTSSR or GTPSR and start or stop counting. In Figure 21.32, the GTETRGA pin operation is set.

21.3.7.3 Hardware clear operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 9) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 21.33 and Figure 21.34 show examples of the GTCNT counter clearing operation by a hardware source. Table 21.27 shows the setting example. In this example, the GTCNT counter starts at the ELC_GPTA input, and the counter stops and clears at the ELC_GPTB input.

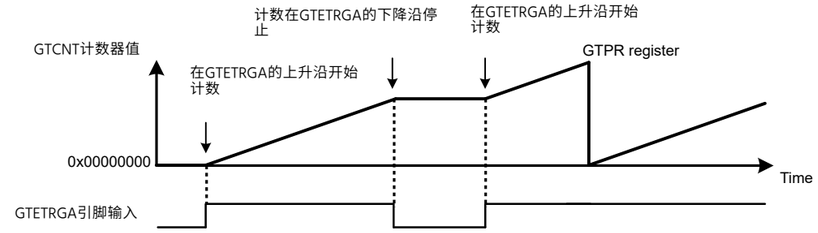


Figure 21.32 由硬件源在上升沿开始的计数开始停止操作示例 GTETRGA引脚输入，并在GTETRGA引脚输入的下降沿停止

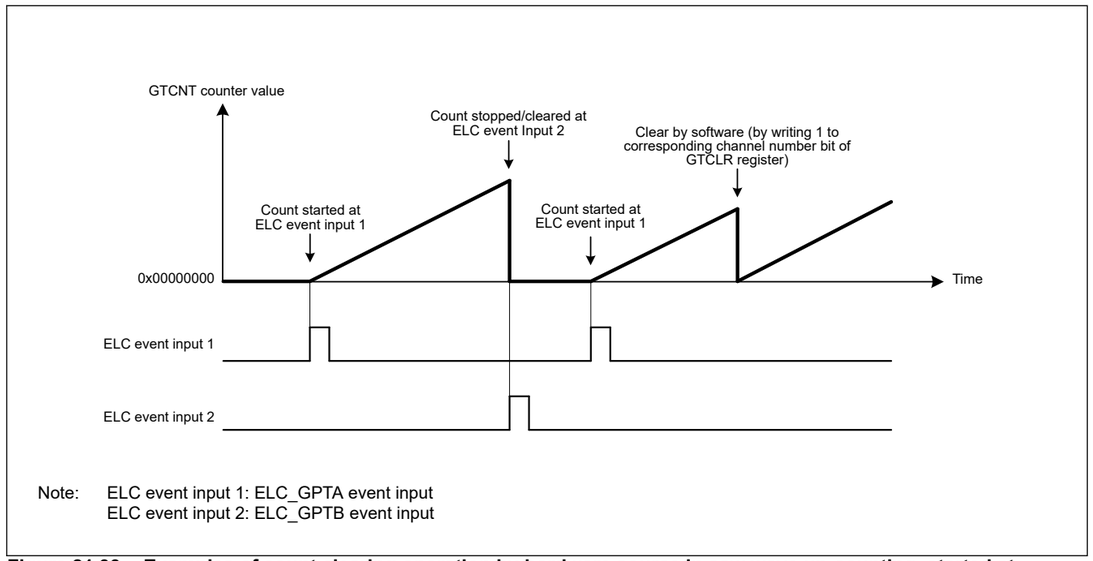
Table 21.26 硬件源的计数开始停止操作设置示例

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.32中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.32中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR中设置循环。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.32中，设置了0x00000000。
6	设置硬件计数开始	使用GTSSR寄存器选择开始计数操作的硬件源，并等待硬件源开始计数。在图21.32中，GTSSR.SSGTRGAR=1。
7	设置硬件计数停止	使用GTPSR寄存器选择停止计数操作的硬件源，并等待硬件源停止计数。在图21.32中，GTPSR.PSGTRGAF=1。
8	设置硬件源操作	设置在GTSSR或GTPSR中选择的硬件源的操作并开始或停止计数。 在图21.32中，设置了GTETRGA引脚操作。

21.3.7.3 硬件清除操作

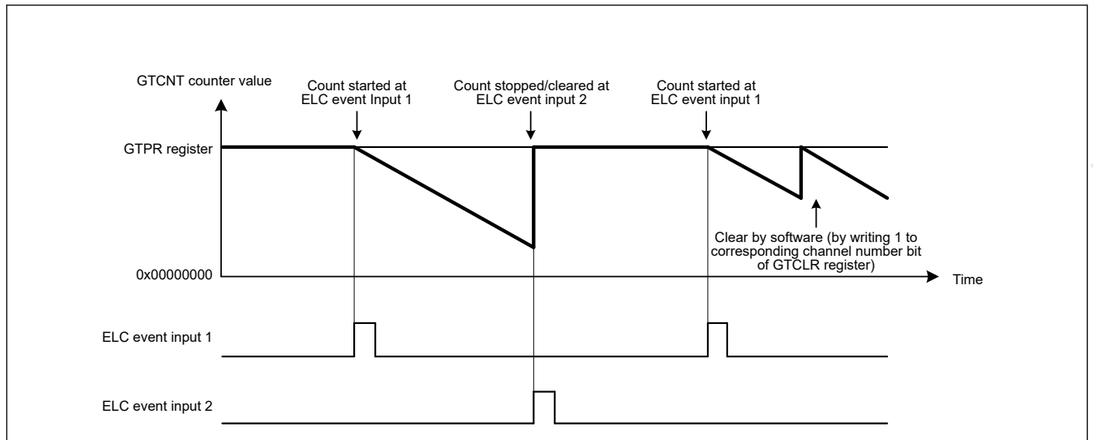
GTCNT计数器可以通过使用GTCSR选择硬件源来清除。GPTn_OVFGPTn_UDF(n=0to9)中断（上溢下溢中断）不会在GTCNT计数器被硬件或软件清零时产生。

图21.33和图21.34显示了通过硬件源清除GTCNT计数器操作的示例。表21.27显示了设置示例。在本例中，GTCNT计数器在ELC_GPTA输入处开始，计数器在ELC_GPTB输入处停止并清零。



Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 21.33 Examples of count clearing operation by hardware source in saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

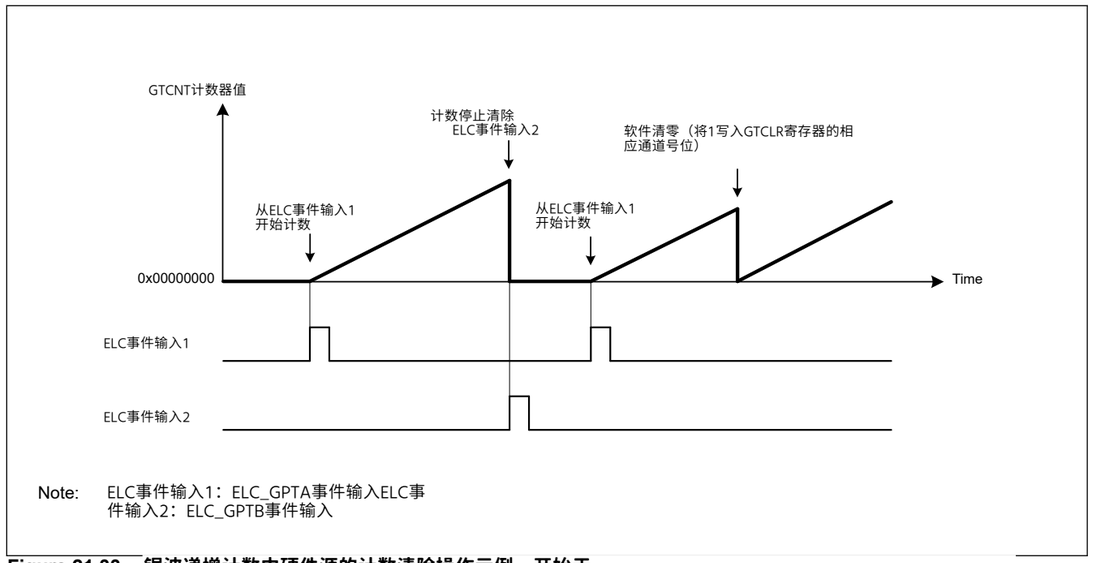


Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 21.34 Examples of count clearing operation by hardware source in saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

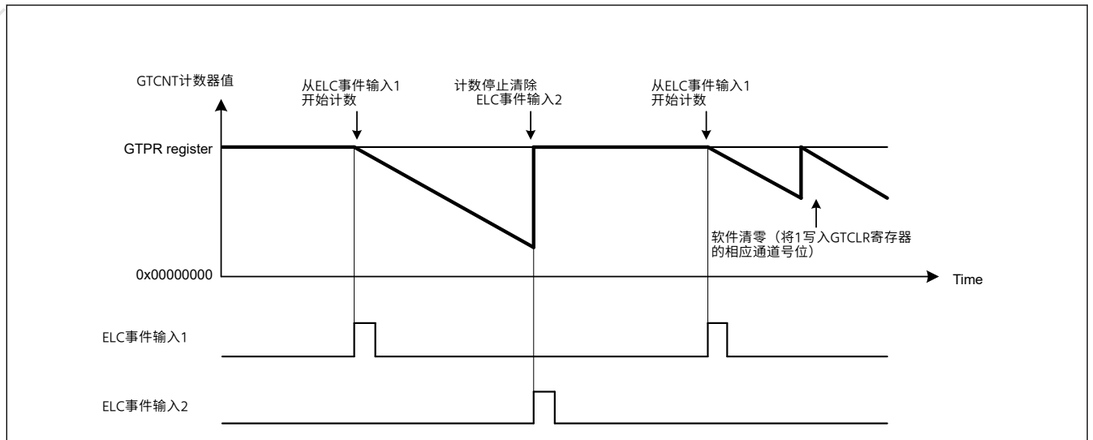
Table 21.27 Example setting for count clearing operation by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.33 and Figure 21.34, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register. In Figure 21.33, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting). In Figure 21.34, after 10b is set in GTUDDTYC[1:0], 00b is set in GTUDDTYC[1:0] (down-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].



Note: ELC事件输入1：ELC_GPTA事件输入ELC事
件输入2：ELC_GPTB事件输入

Figure 21.33 锯波递增计数中硬件源的计数清除操作示例，开始于ELC_GPTA输入，并在ELC_GPTB输入处停止清除



Note: ELC事件输入1：ELC_GPTA事件输入ELC事
件输入2：ELC_GPTB事件输入

Figure 21.34 锯波递减计数中硬件源的计数清除操作示例，从ELC_GPTA输入开始，在ELC_GPTB输入停止清除

Table 21.27 通过硬件源进行计数清除操作的示例设置（2个中的1个）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.33和图21.34中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下）。 在图21.33中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。 在图21.34中，在GTUDDTYC[1:0]中设置了10b后，在GTUDDTYC[1:0]中设置了00b（向下计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。

Table 21.27 Example setting for count clearing operation by a hardware source (2 of 2)

No.	Step Name	Description
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter. In Figure 21.33, 0x00000000 is set. In Figure 21.34, the GTPR value is set.
6	Set hardware count start	Select a hardware source for starting count operation in GTSSR register and wait for count start by the hardware source. In Figure 21.33 and Figure 21.34, GTSSR.SSELCA = 1.
7	Set hardware count stop	Select a hardware source for stopping count operation in GTPSR register and wait for count stop by the hardware source. In Figure 21.33 and Figure 21.34, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation in GTCSR register and wait for count clear by the hardware source. In Figure 21.33 and Figure 21.34, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in GTSSR register, GTPSR Register or GTCSR register and start, stop or clear counting. In Figure 21.33 and Figure 21.34, the ELC_GPTA input and ELC_GPTB input are set.

The GPTn_OVF/GPTn_UDF (n = 0 to 9) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 21.35 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 9) interrupt.

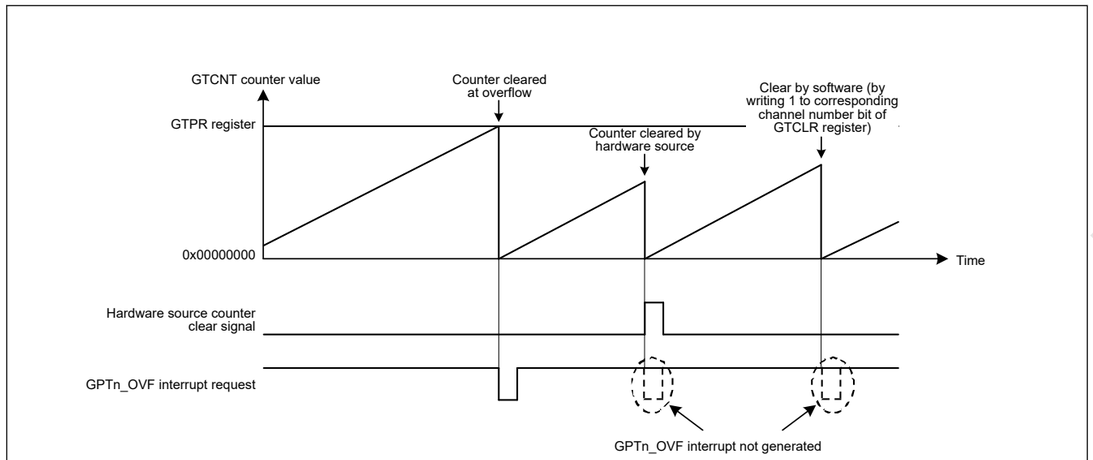


Figure 21.35 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 9) interrupt

21.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

21.3.8.1 Synchronized operation by software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

Figure 21.36 shows an example of a simultaneous start, stop, and clear by software. Figure 21.37 shows an example of phase start operation by software.

Table 21.27 通过硬件源进行计数清除操作的示例设置(2of2)

No.	步骤名称	Description
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值。 在图21.33中，设置了0x00000000。在图21.34中，设置了GTPR值。
6	设置硬件计数开始	在GTSSR寄存器中选择一个开始计数操作的硬件源，等待硬件源开始计数。在图21.33和图21.34中，GTSSR.SSELCA=1。
7	设置硬件计数停止	在GTPSR寄存器中选择一个停止计数操作的硬件源，等待硬件源停止计数。在图21.33和图21.34中，GTPSR.PSELCB=1。
8	设置硬件计数清除	在GTCSR寄存器中选择清除计数操作的硬件源，等待硬件源清除计数。在图21.33和图21.34中，GTCSR.CSELCB=1。
9	设置硬件源操作	设置在GTSSR寄存器、GTPSR寄存器或GTCSR寄存器中选择的硬件源的操作以及开始、停止或清除计数。在图21.33和图21.34中，设置了ELC_GPTA输入和ELC_GPTB输入。

GPTn_OVFGPTn_UDF（n=0到9）中断（溢出下溢中断）不会在计数器被硬件源或软件清零时产生。

图21.35显示了通过硬件源清除计数器和GPTn_OVF（n=0到9）中断之间的关系。

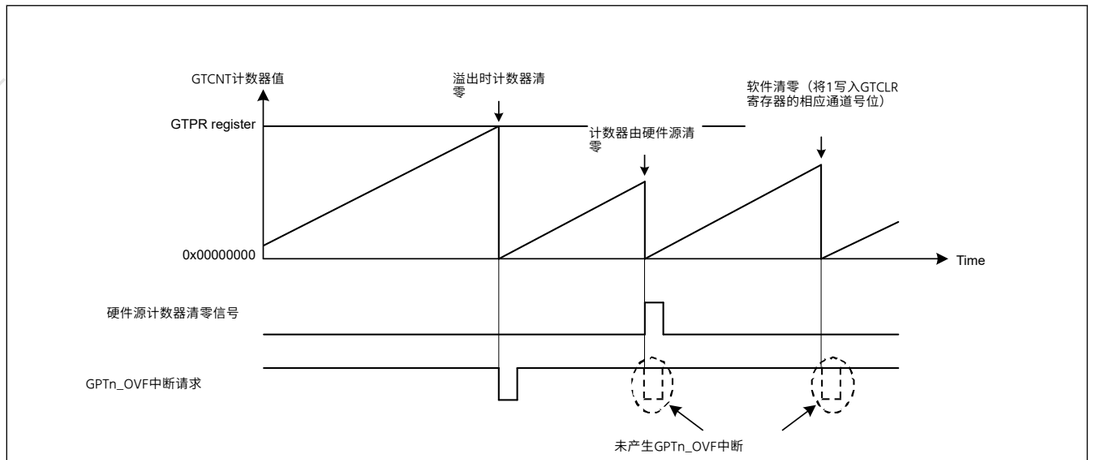


Figure 21.35 硬件源计数器清零与GPTn_OVF(n=0to9)中断的关系

21.3.8 同步操作

可以对通道进行同步操作，例如同步启动、停止和清除操作。

21.3.8.1 软件同步操作

通过将相关的GTSTR、GTSTP或GTCLR位同时设置为1，可以在多个通道上启动、停止和清除GTCNT计数器。

通过在GTCNT计数器中设置初始值并设置相关的
GTSTR位同时为1。

图21.36显示了通过软件同时启动、停止和清除的示例。图21.37显示了通过软件进行相位启动操作的示例。

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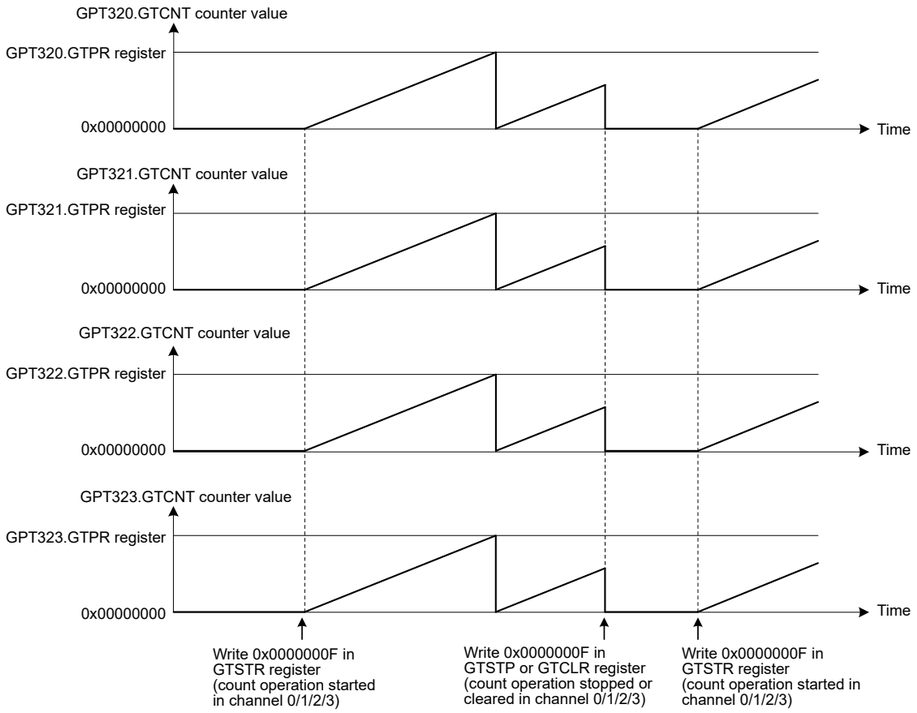


Figure 21.36 Example of a simultaneous start, stop, and clear by software with the same count cycle (GTPR register value)

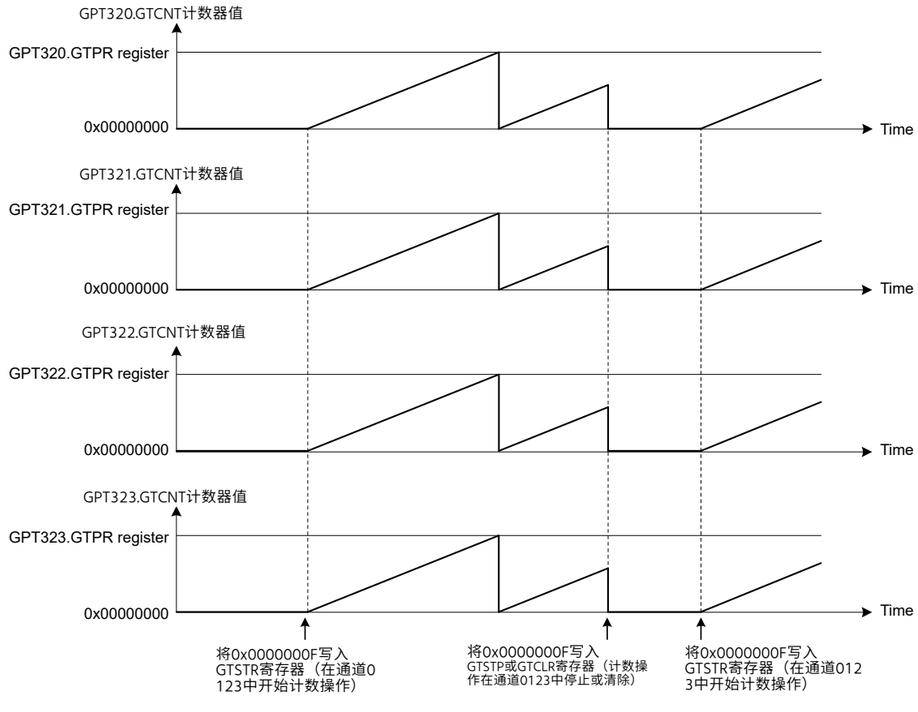


Figure 21.36 使用相同计数周期（GTPR寄存器值）的软件同时启动、停止和清除的示例

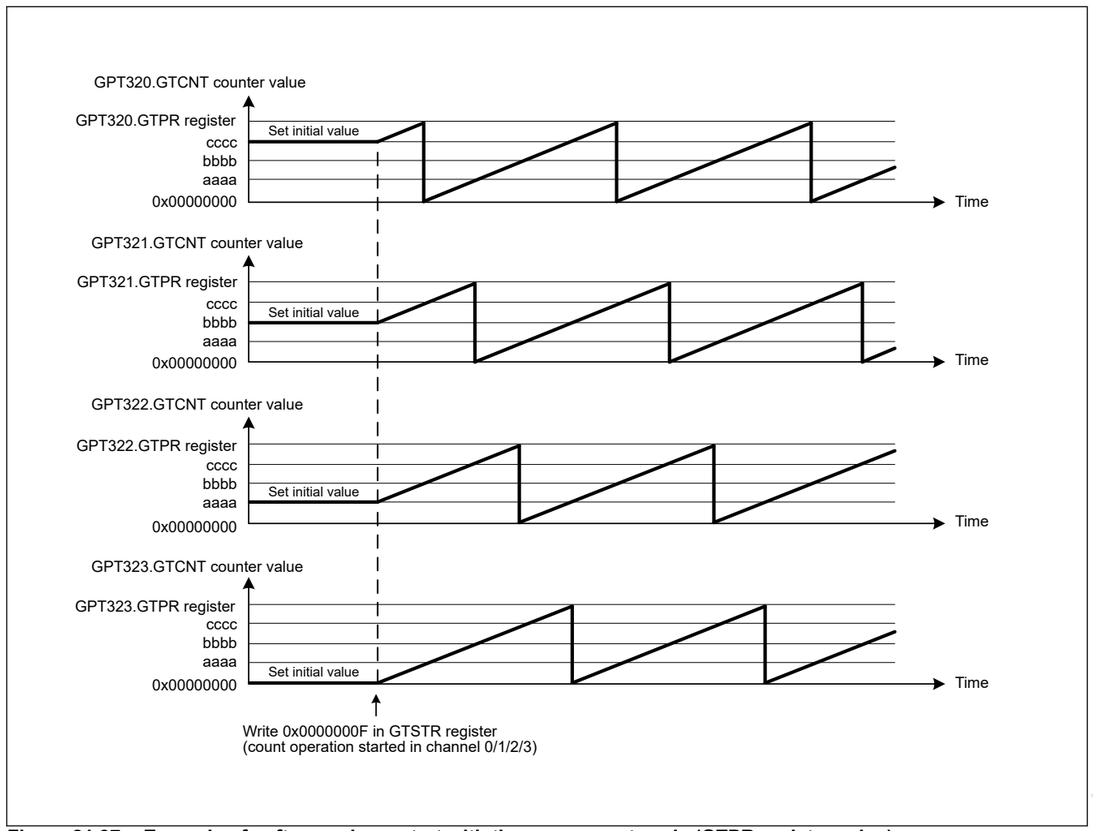


Figure 21.37 Example of software phase start with the same count cycle (GTPR register value)

21.3.8.2 Synchronized operation by hardware

The counters for multiple channels can be started, stopped, and cleared simultaneously by the following hardware sources. Hardware sources that can cause a synchronized operation are external trigger input and ELC event input. Synchronized operations through GTIOCnA and GTIOCnB pin input are possible by setting an ELC event due to input capture as a hardware source (n = 0 to 9).

Figure 21.38 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Table 21.28 shows the setting example.

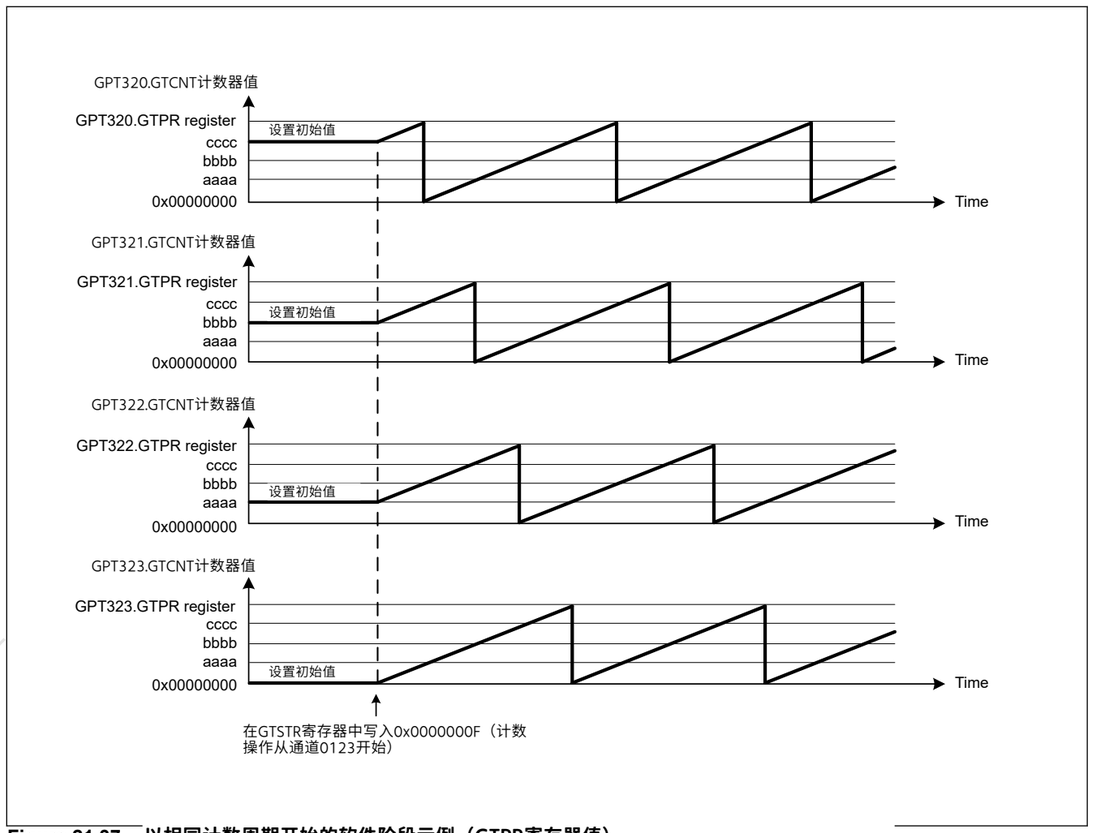
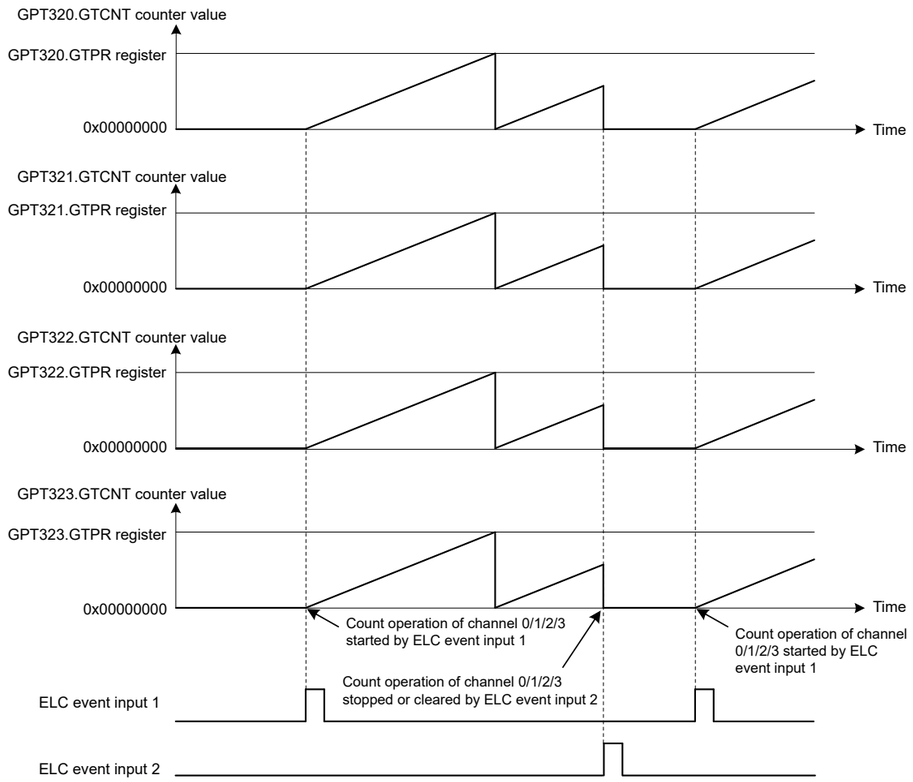


Figure 21.37 以相同计数周期开始的软件阶段示例（GTPR寄存器值）

21.3.8.2 硬件同步操作

多个通道的计数器可以通过以下硬件源同时启动、停止和清除。
可以导致同步操作的硬件源是外部触发输入和ELC事件输入。通过将输入捕获引起的ELC事件设置为硬件源（n=0到9），可以通过GTIOCnA和GTIOCnB引脚输入进行同步操作。

图21.38显示了一个硬件源同时启动、停止和清除操作的示例。表21.28显示了设置示例。

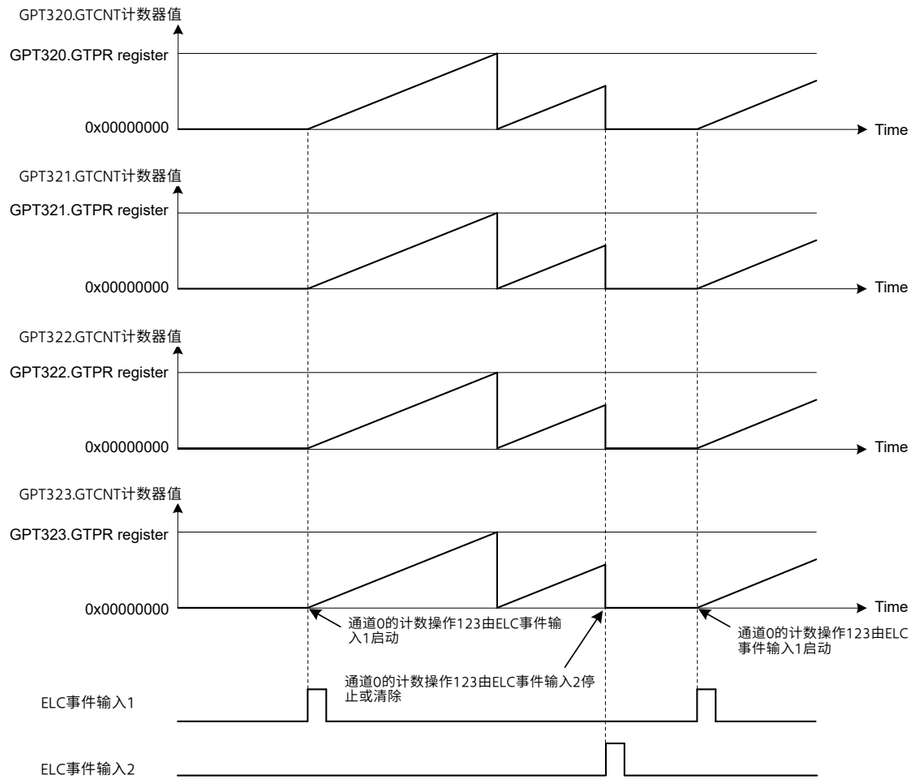


Note: ELC event input 1: ELC_GPTA event input
ELC event input 2: ELC_GPTB event input

Figure 21.38 Example of a simultaneous start, stop, and clear by a hardware source with the same count cycle (GTPR register value)

Table 21.28 Example setting for simultaneous start by a hardware source (1 of 2)

No.	Step Name	Description
1	Set operating mode	Set the operating mode with GTCR.MD[2:0]. In Figure 21.38, 000b (saw-wave PWM mode) is set.
2	Set count direction	Select the count direction (up or down) with the GTUDDTYC register In Figure 21.38, after 11b is set in GTUDDTYC[1:0], 01b is set in GTUDDTYC[1:0] (up-counting).
3	Select count clock	Select the count clock with GTCR.TPCS[3:0].
4	Set cycle	Set the cycle in the GTPR register.
5	Set initial value for counter	Set the initial value in the GTCNT counter In Figure 21.38, 0x00000000 is set.
6	Set hardware count start	Select a hardware source for starting count operation with GTSSR register and wait for count start by the hardware source. In Figure 21.38, GTSSR.SSELCA = 1.



Note: ELC事件输入1：ELC_GPTA事件输入ELC事件输入2：ELC_GPTB事件输入

Figure 21.38 具有相同计数周期（GTPR寄存器值）的硬件源同时启动、停止和清除的示例

Table 21.28 通过硬件源同时启动的示例设置（2个中的1个）

No.	步骤名称	Description
1	设置操作模式	使用GTCR.MD[2:0]设置操作模式。 在图21.38中，设置了000b（锯齿波PWM模式）。
2	设置计数方向	使用GTUDDTYC寄存器选择计数方向（向上或向下） 在图21.38中，在GTUDDTYC[1:0]中设置了11b之后，在GTUDDTYC[1:0]中设置了01b（向上计数）。
3	选择计数时钟	使用GTCR.TPCS[3:0]选择计数时钟。
4	设置周期	在GTPR寄存器中设置周期。
5	设置计数器的初始值	在GTCNT计数器中设置初始值 在图21.38中，设置了0x00000000。
6	设置硬件计数开始	使用GTSSR寄存器选择开始计数操作的硬件源，并等待硬件源开始计数。在图21.38中，GTSSR.SSELCA=1。

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Table 21.28 Example setting for simultaneous start by a hardware source (2 of 2)

No.	Step Name	Description
7	Set hardware count stop	Select a hardware source for stopping count operation with GTPSR register and wait for count stop by the hardware source In Figure 21.38, GTPSR.PSELCB = 1.
8	Set hardware count clear	Select a hardware source for clearing count operation with GTCSR register and wait for count clear by the hardware source In Figure 21.38, GTCSR.CSELCB = 1.
9	Set hardware source operation	Set operation of the hardware source selected in GTSSR or GTPSR or GTCSR and start or stop or clear counting In Figure 21.38, ELC_GPTA input and ELC_GPTB input are set.

21.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 10 × 2 phases of linked PWM waveforms for a maximum of GPT × 10 channels.

Figure 21.39 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

Table 21.28 通过硬件源同时启动的示例设置(2of2)

No.	步骤名称	Description
7	设置硬件计数停止	使用GTPSR寄存器选择停止计数操作的硬件源并等待硬件源停止计数在图21.38中，GTPSR.PSELCB=1。
8	设置硬件计数清除	使用GTCSR寄存器选择清除计数操作的硬件源，等待硬件源清除计数在图21.38中，GTCSR.CSELCB=1。
9	设置硬件源操作	设置在GTSSR或GTPSR或GTCSR中选择的硬件源的操作以及开始或停止或清除计数在图21.38中，设置了ELC_GPTA输入和ELC_GPTB输入。

21.3.9 PWM输出操作示例

(1) 同步PWM输出

GPT为最多GPT×10个通道输出10×2相链接的PWM波形。

图21.39显示了一个示例，其中4个通道在锯齿波PWM模式下执行同步操作并输出8相PWM波形。GTIOCnA设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCnB设置为输出低作为初始值，在GTCCRB比较匹配时输出高，在循环结束时输出低。

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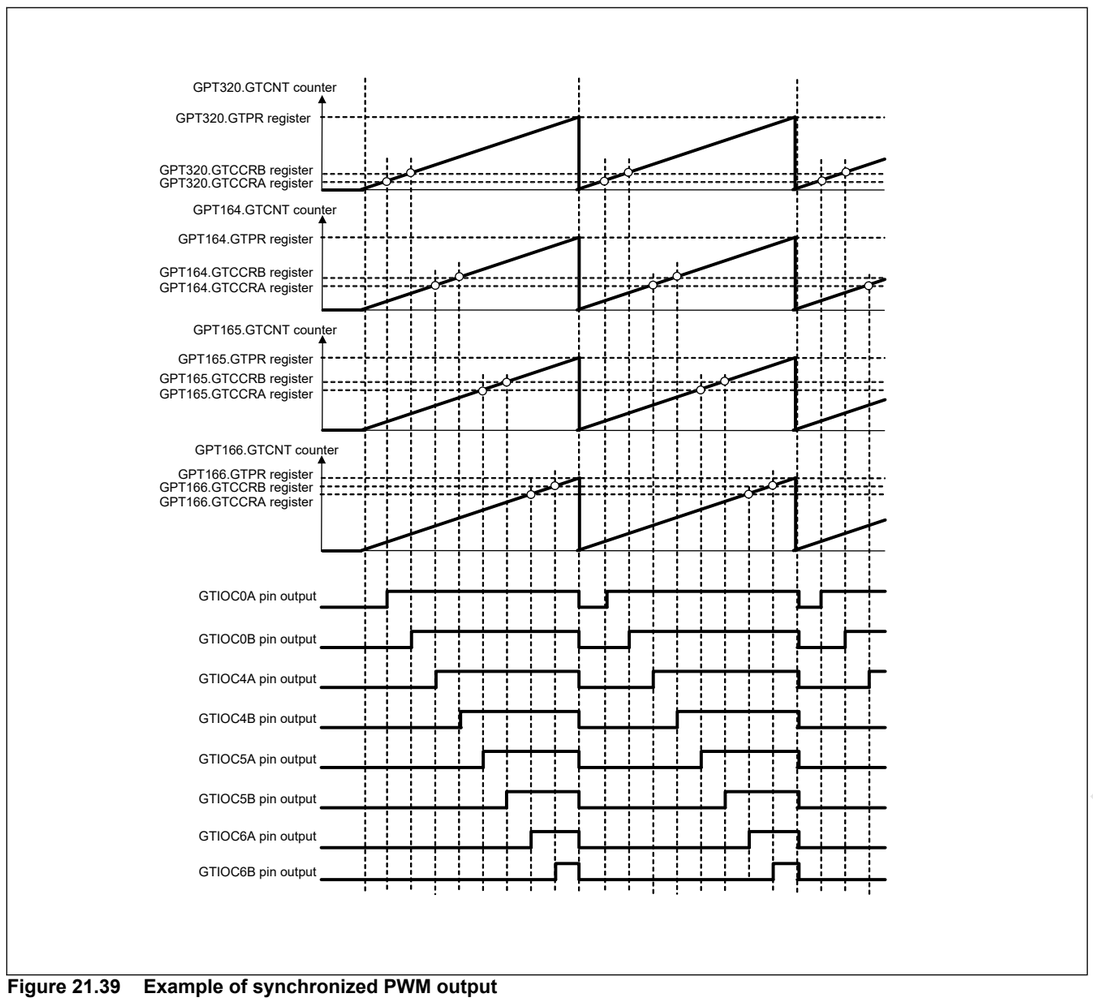

Figure 21.39 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 21.40 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

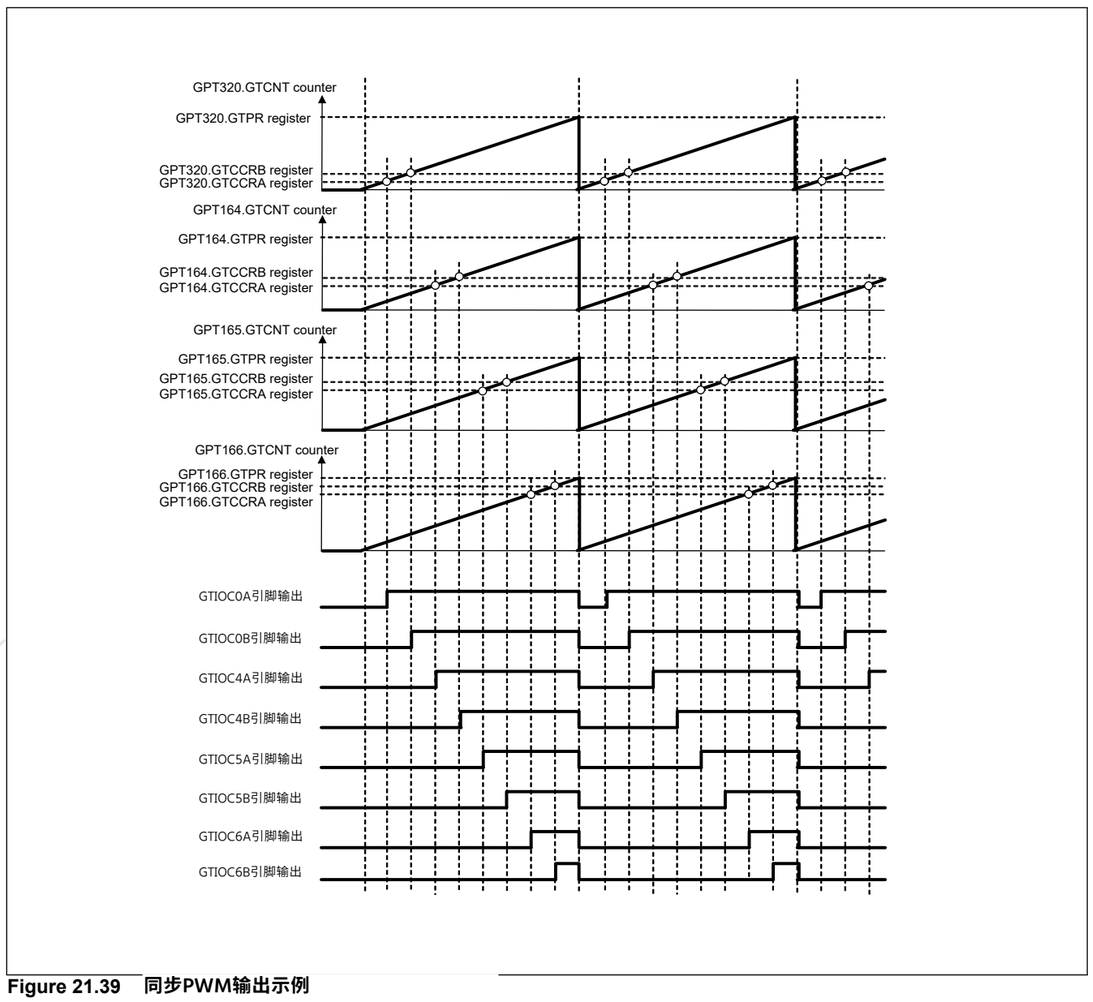

Figure 21.39 同步PWM输出示例

(2) 三相锯齿波互补PWM输出

图21.40显示了一个示例，其中三个通道在锯齿波PWM模式下执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在周期结束时输出低。GTIOCnB引脚设置为输出高作为初始值，在GTCCRB比较匹配时输出低，在周期结束时输出高。

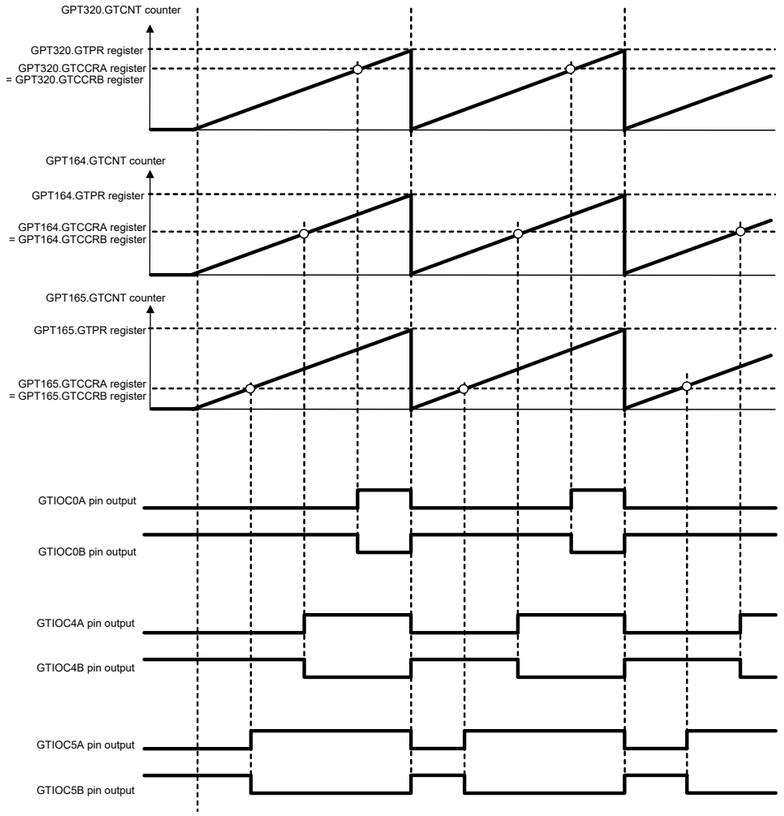

Figure 21.40 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 21.41 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTIOCnB compare match, and retains the output at the cycle end.

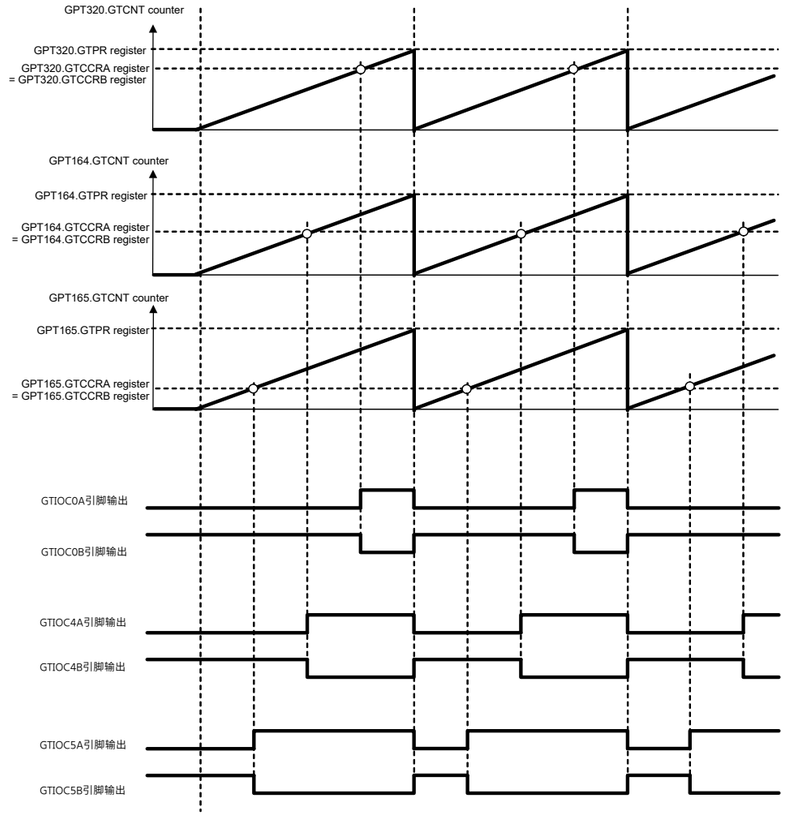

Figure 21.40 三相锯齿波互补PWM输出示例

(3) 具有自动死区时间设置的三相锯齿波互补PWM输出

图21.41显示了一个示例，其中三个通道在具有自动死区时间设置的锯齿波一次性脉冲模式下执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTIOCnB比较匹配时切换输出，并在周期结束时保持输出。

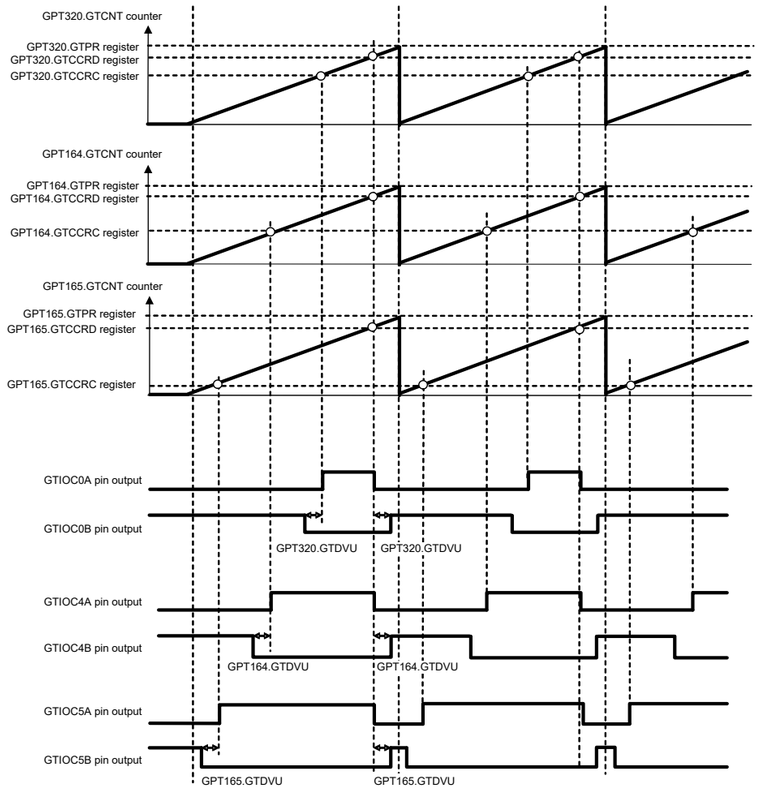

Figure 21.41 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 21.42 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

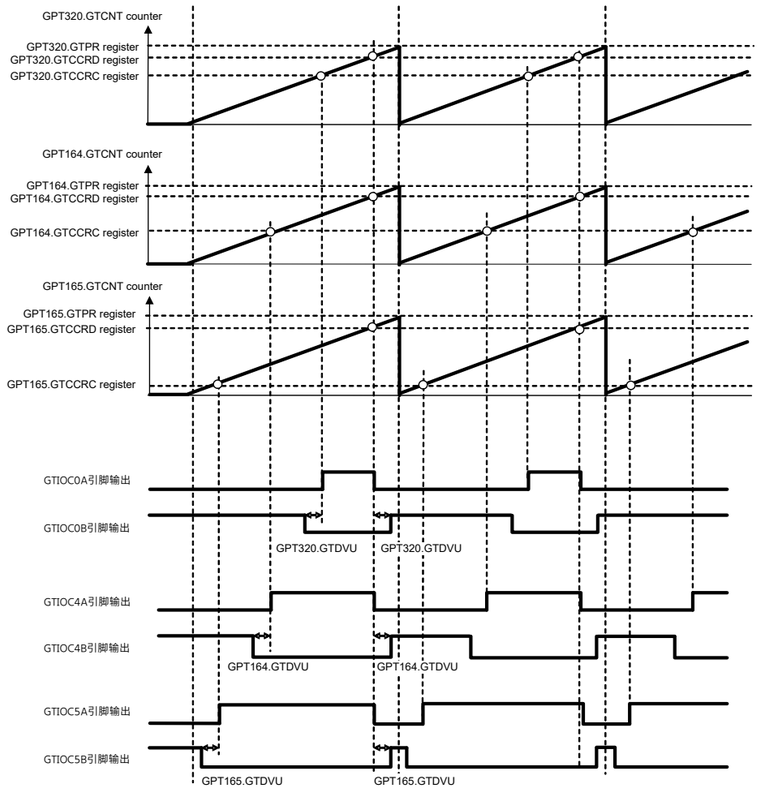

Figure 21.41 具有自动死区时间设置的三相锯齿波互补PWM输出示例

(4) 三相三角波互补PWM输出

图21.42显示了一个示例，其中三个通道在三角波PWM模式1中执行同步操作并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

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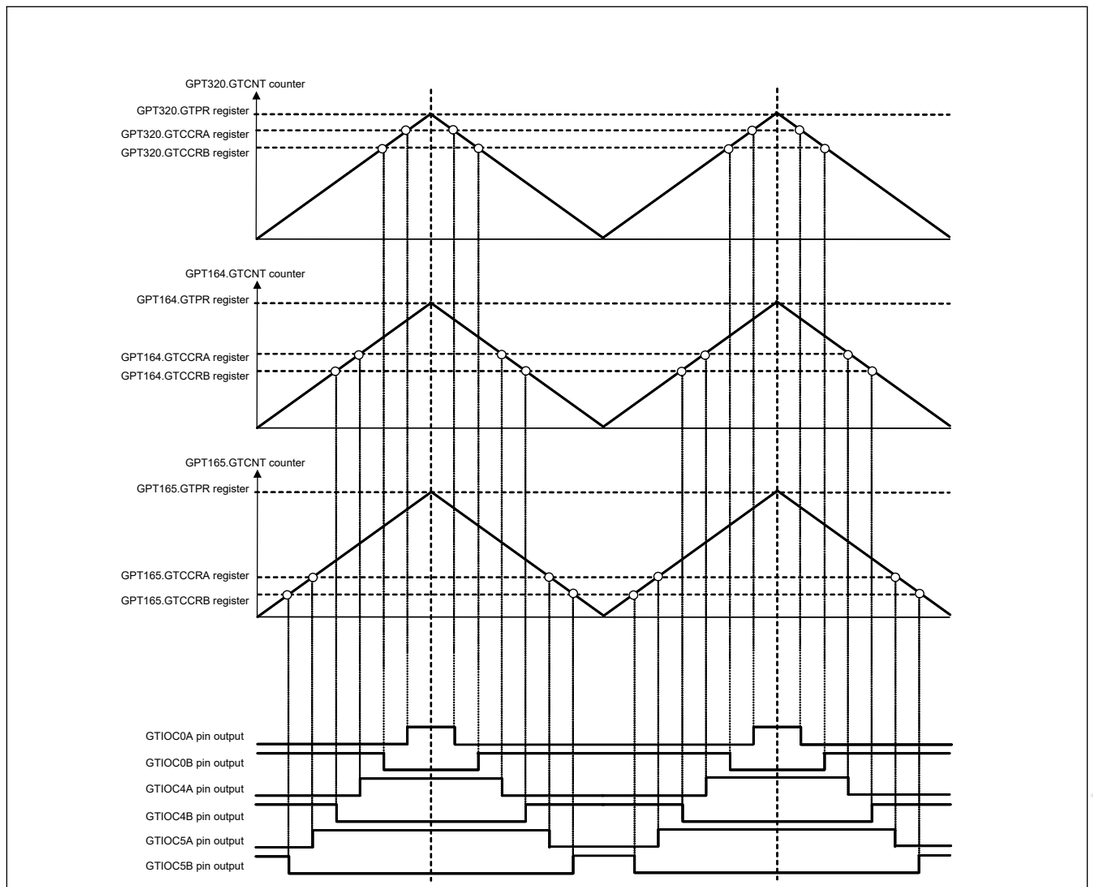

Figure 21.42 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 21.43 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

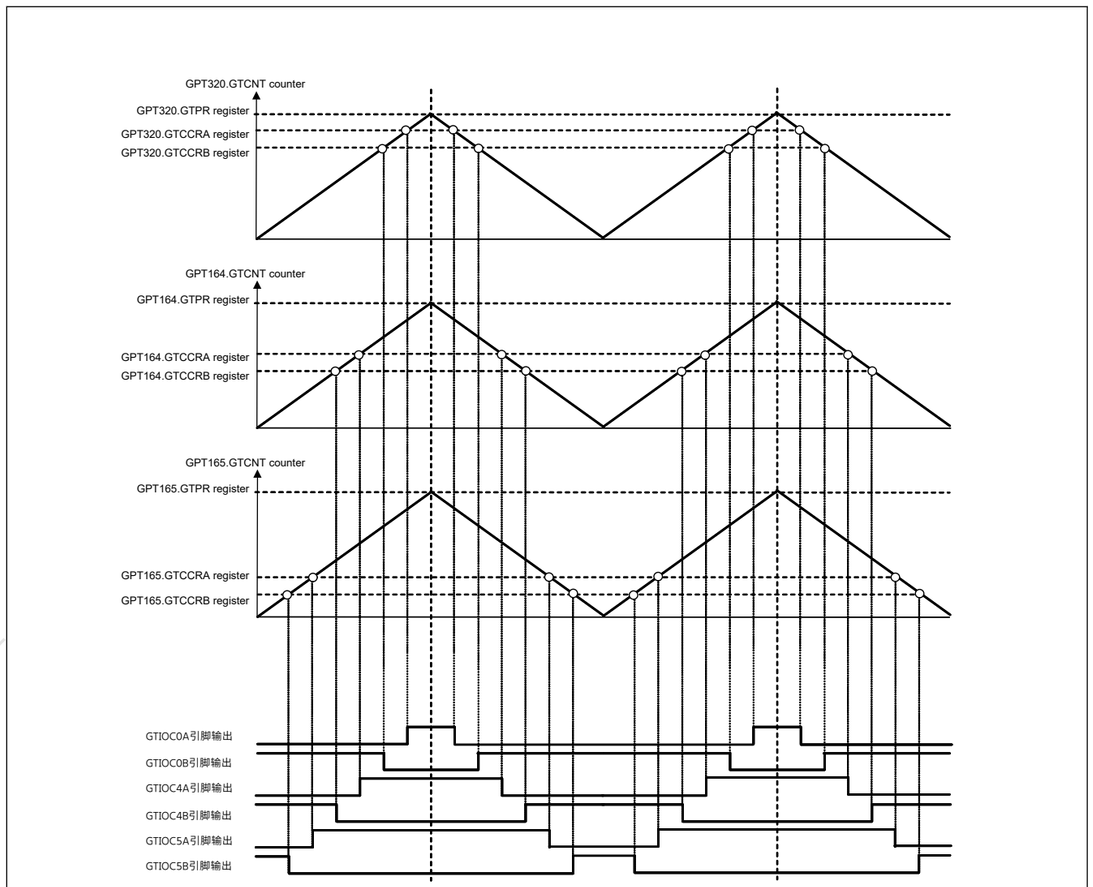

Figure 21.42 三相三角波互补PWM输出示例

(5) 具有自动死区时间设置的三相三角波互补PWM输出

图21.43显示了一个示例，其中三个通道在三角波PWM模式1下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCnA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCnB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

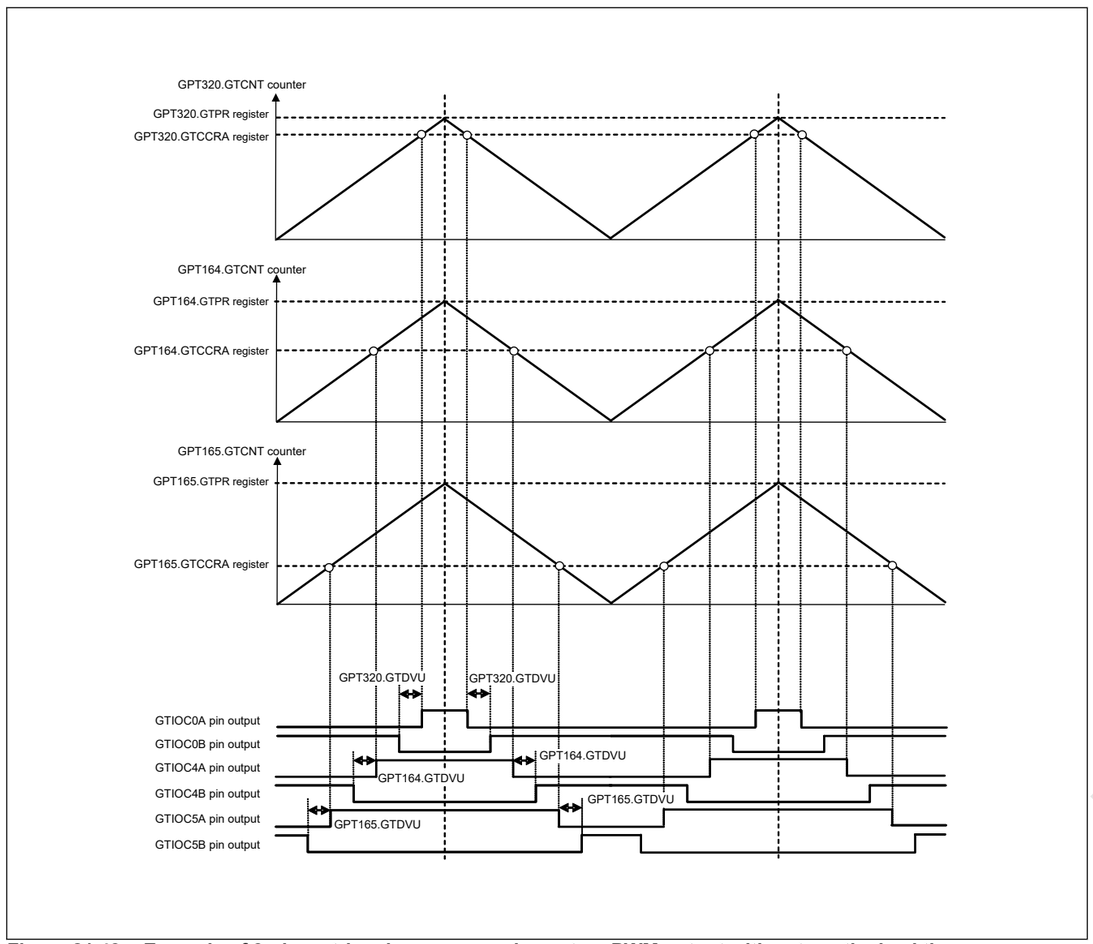

Figure 21.43 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 21.44 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCnA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCnB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

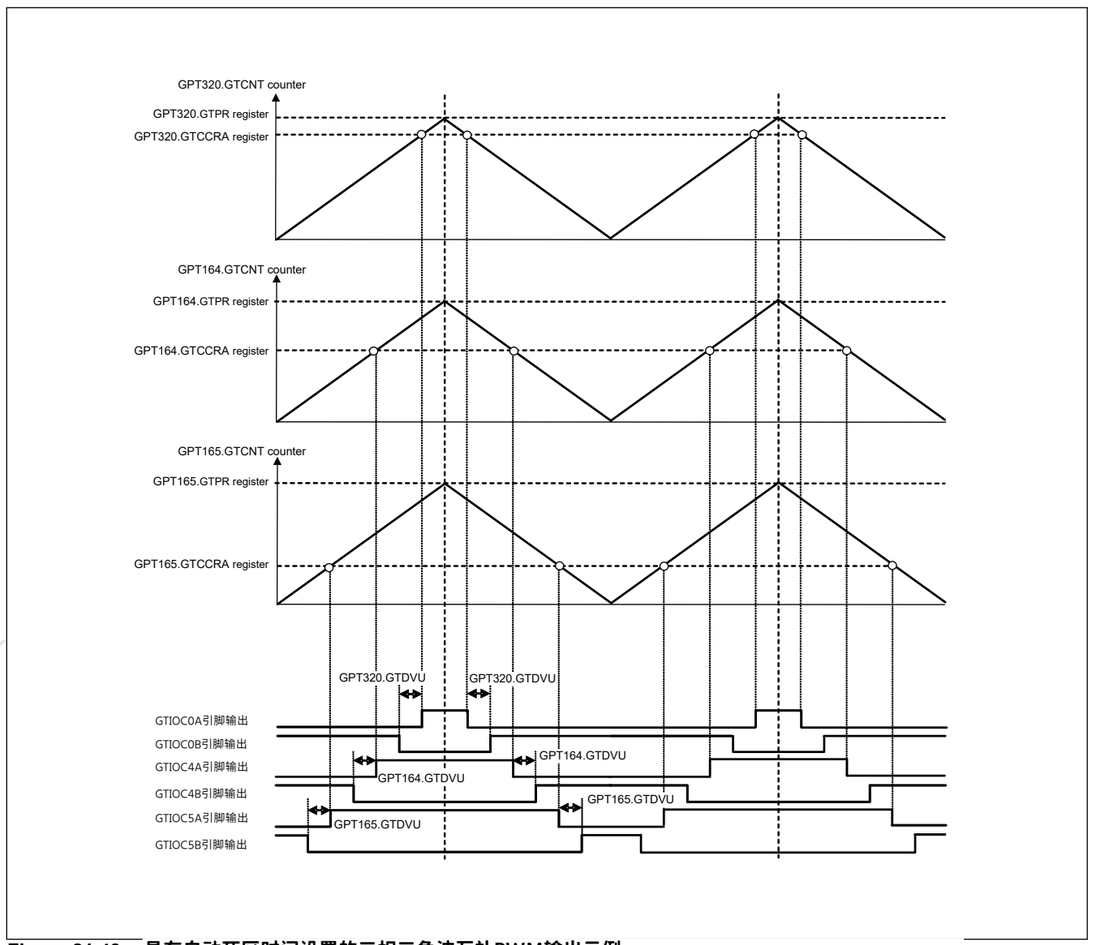

Figure 21.43 具有自动死区时间设置的三相三角波互补PWM输出示例

(6) 具有自动死区时间设置的三相不对称三角波互补PWM输出

图21.44显示了一个示例，其中三个通道在三角波PWM模式3下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCnA设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在循环结束时保留输出。GTIOCnB设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在循环结束时保留输出。

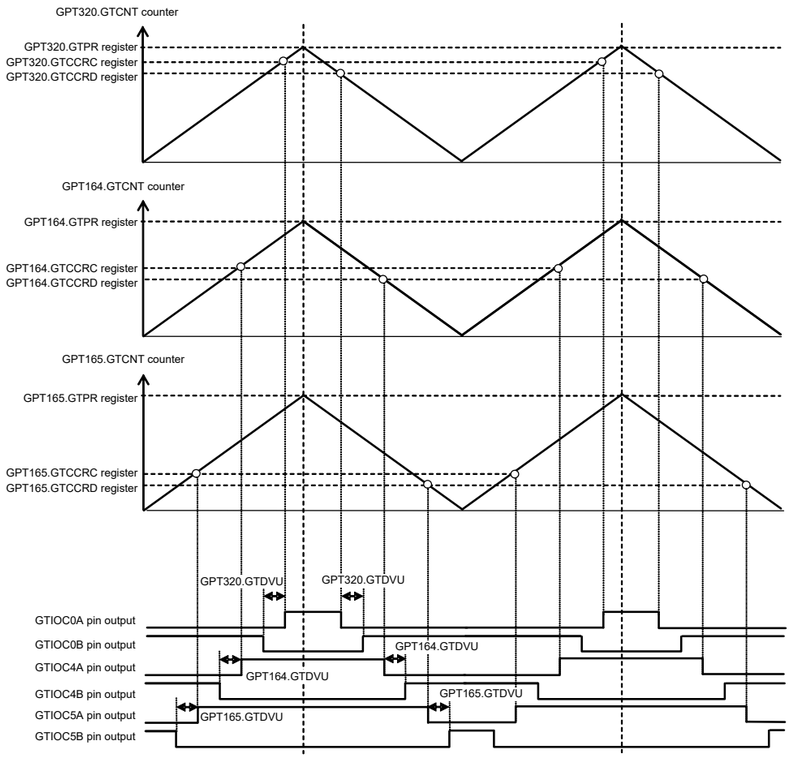

Figure 21.44 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

21.3.10 Period Count Function

By setting the GTPC register, the end of period can be counted.

The number of period to be counted should be set into the GTPC.PCNT counter when the GTPC.PCEN bit is 0. When the PCEN bit is 1, the PCNT counter can be read, but writing is disabled. When the PCEN bit is 1, down-counting is perfoemed at the end of period. When the PCNT counter is 1 at the end of period, it becomes 0 and counting is stopped to finish the period count function. At that time, the GTST.PCF flag is set, and the period count function finish interrupt request GPTn_PC is generated. When the GTPC.ASTP bit is 1, the GTCNT counter is also stopped at the same time that the period count function is finished.

When the GTCNT counter is stopped while period count function is enabled, the PCNT counter keeps its value. When the GTCNT counter restarts counting and the PCEN bit is 1, the PCNT counter restarts down-counting from the hold value.

When the PCEN bit is changed from 0 to 1 while the PCNT counter is 0 and the ASTP bit is 1, the GTCNT counter is stopped at the count clock immidiately after that.

When either GTSECR.SPCE bit or GTSECR.SPCD bit is set to 1, the PCEN bit in the channels set to 1 by the GTSECSR register is simultaneously set the value to enable or disable the period count function for multiple channels.

Figure 21.45 and Figure 21.46 show examples of PWM cycle count function.

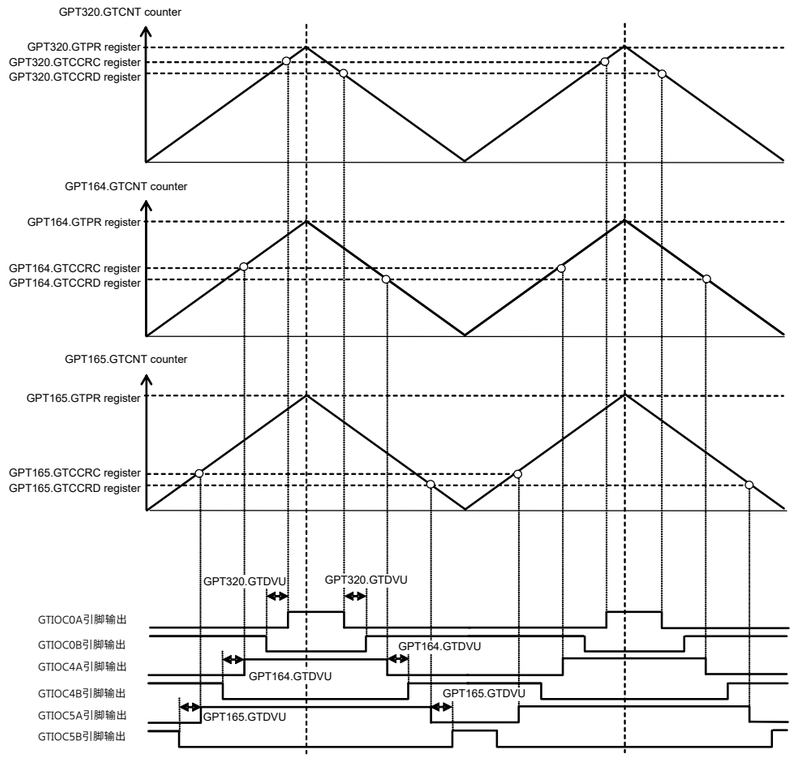

Figure 21.44 具有自动死区时间设置的三相不对称三角波互补PWM输出示例

21.3.10 周期计数功能

通过设置GTPC寄存器，可以计算周期结束。

当GTPC.PCEN位为0时，要计数的周期数应设置到GTPC.PCNT计数器中。当PCEN位为1，可以读取PCNT计数器，但禁止写入。当PCEN位为1时，在周期结束时进行递减计数。当PCNT计数器在周期结束时为1时，它变为0并停止计数以完成周期计数功能。此时，GTST.PCF标志置位，产生周期计数功能完成中断请求GPTn_PC。当GTPC.ASTP位为1时，GTCNT计数器也在周期计数功能完成的同时停止。

当GTCNT计数器停止而周期计数功能使能时，PCNT计数器保持其值。当。。。的时候GTCNT计数器重新开始计数且PCEN位为1，PCNT计数器重新从保持值开始向下计数。

当PCNT计数器为0且ASTP位为1时PCEN位从0变为1时，GTCNT计数器立即停止在计数时钟处。

当GTSECR.SPCE位或GTSECR.SPCD位设置为1时，通过GTSECSR寄存器设置为1的通道中的PCEN位同时设置该值以启用或禁用多个通道的周期计数功能。

图21.45和图21.46显示了PWM周期计数功能的示例。

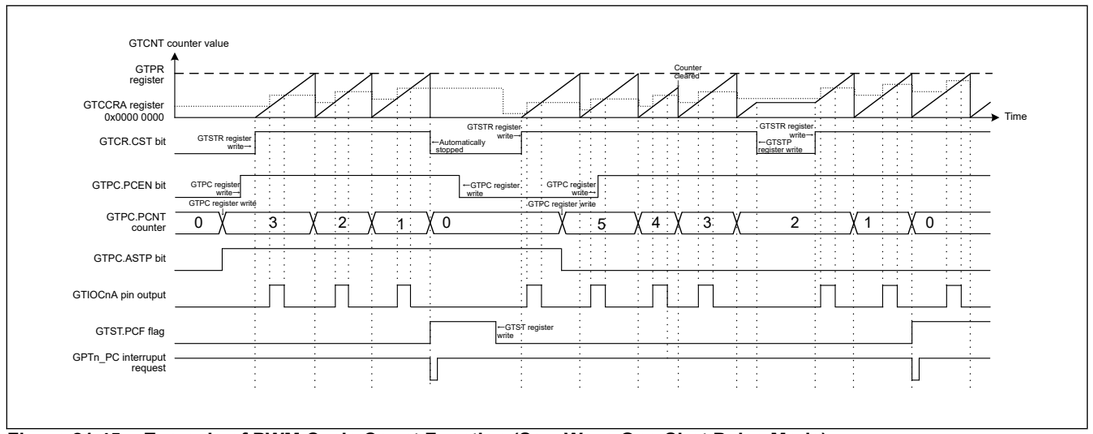

Figure 21.45 Example of PWM Cycle Count Function (Saw-Wave One-Shot Pulse Mode)

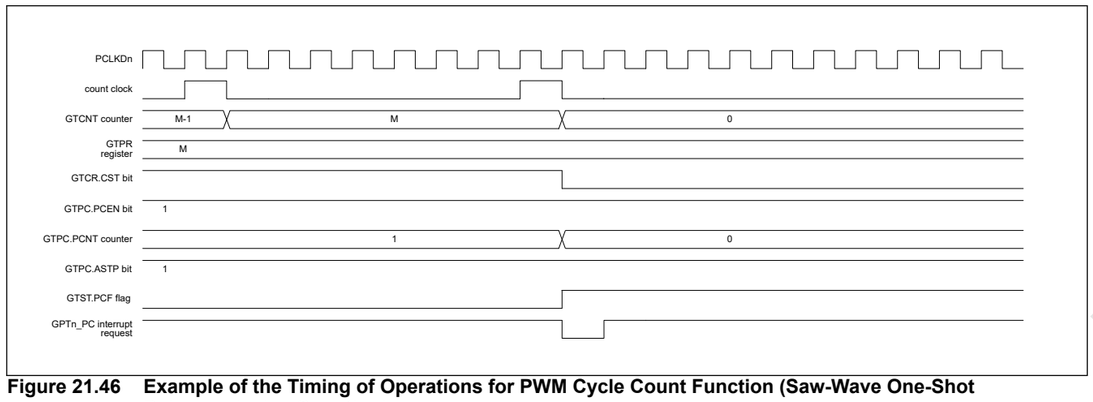

Figure 21.46 Example of the Timing of Operations for PWM Cycle Count Function (Saw-Wave One-Shot Pulse mode, Up-Counting)

21.3.11 Phase Counting Function

The phase difference between the GTIOCnA and GTIOCnB pin (n = 0 to 9) inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCnA and GTIOCnB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 21.3.1.1. Counter operation.

Figure 21.47 to Figure 21.56 show an example of phase counting modes 1 to 5 operation when the GTIOCnA, GTIOCnB pins are used. Table 21.29 to Table 21.38 show conditions of up-counting or down-counting and list settings for the GTUPSR and GTDNSR registers which is correspoinding to Figure 21.47 to Figure 21.56.

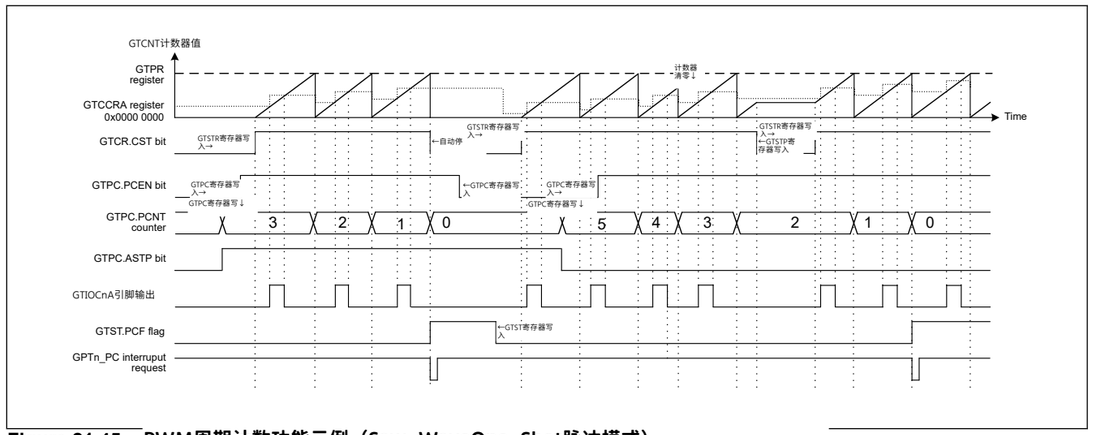

Figure 21.45 PWM周期计数功能示例（Saw-WaveOne-Shot脉冲模式）

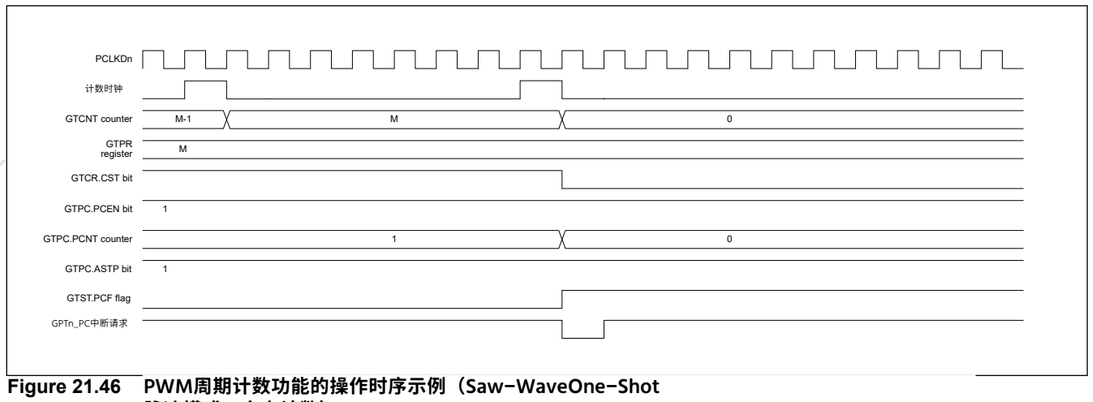

Figure 21.46 PWM周期计数功能的操作时序示例（Saw-WaveOne-Shot脉冲模式，向上计数）

21.3.11 相位计数功能

检测到GTIOCnA和GTIOCnB引脚（n=0到9）输入之间的相位差，并且相关的GTCNT向上计数或向下计数。可检测的相位差可与在GTUPSR和GTDNSR寄存器中设置的GTIOCnA和GTIOCnB引脚输入的边沿和电平之间的关系进行任何组合。有关计数操作的详细信息，请参阅第21.3.1.1节。柜台操作。

图21.47至图21.56显示了使用GTIOCnA、GTIOCnB引脚时相位计数模式1至5操作的示例。表21.29至表21.38显示了向上计数或向下计数的条件，并列出了GTUPSR和GTDNSR寄存器的设置，对应于图21.47至图21.56。

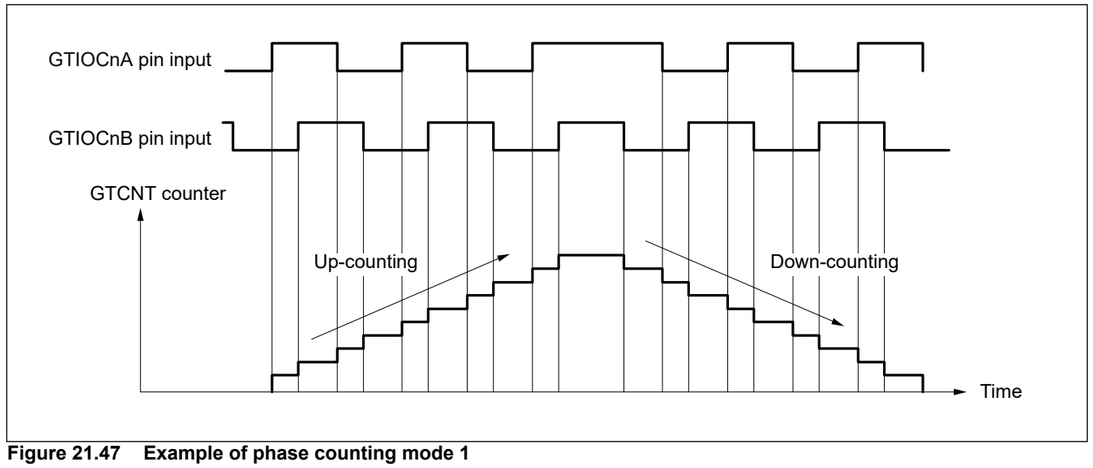

Figure 21.47 Example of phase counting mode 1

Table 21.29 Conditions of up-counting/down-counting in phase counting mode 1

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

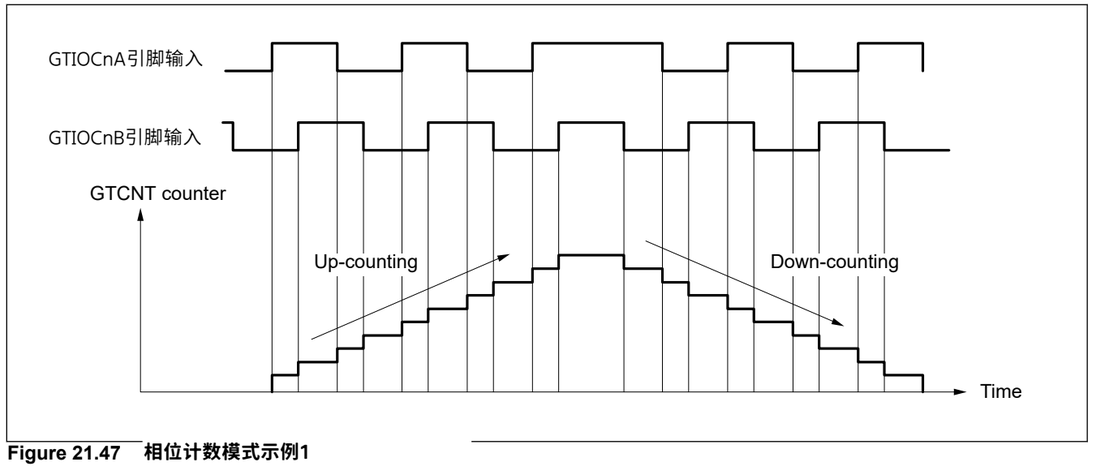

Figure 21.47 相位计数模式示例1

Table 21.29 相位计数模式加减计数条件1

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0x00006900 GTDNSR = 0x00009600
Low	↓		
↑	Low		
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High		
↓	Low		

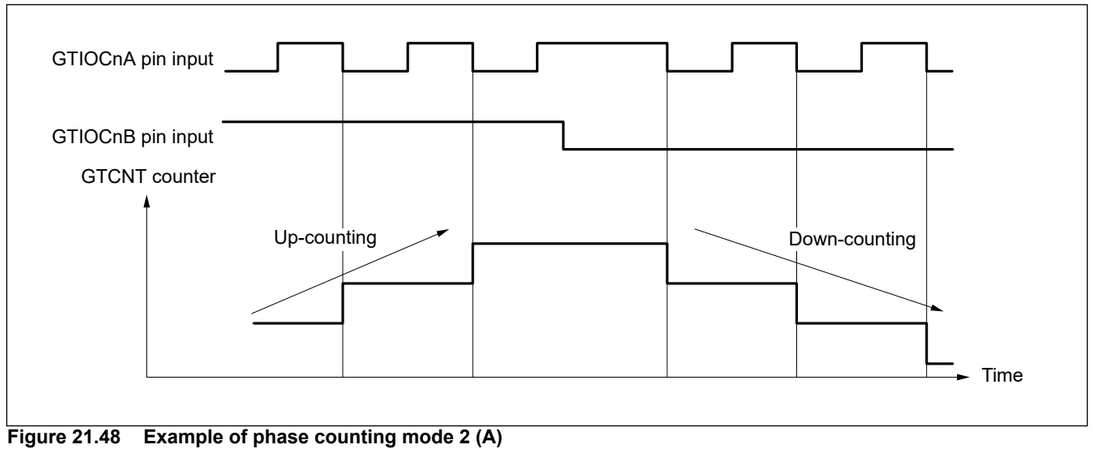

Figure 21.48 Example of phase counting mode 2 (A)

Table 21.30 Conditions of up-counting/down-counting in phase counting mode 2 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High		
↓	Low	Down-counting	

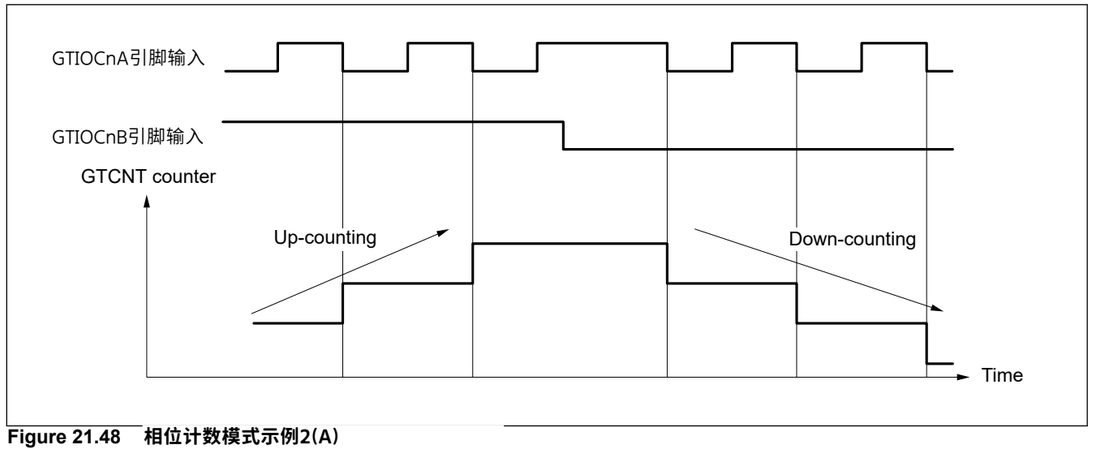

Figure 21.48 相位计数模式示例2(A)

Table 21.30 相位计数模式2(A)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000800 GTDNSR = 0x00000400
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High		
↓	Low	Down-counting	

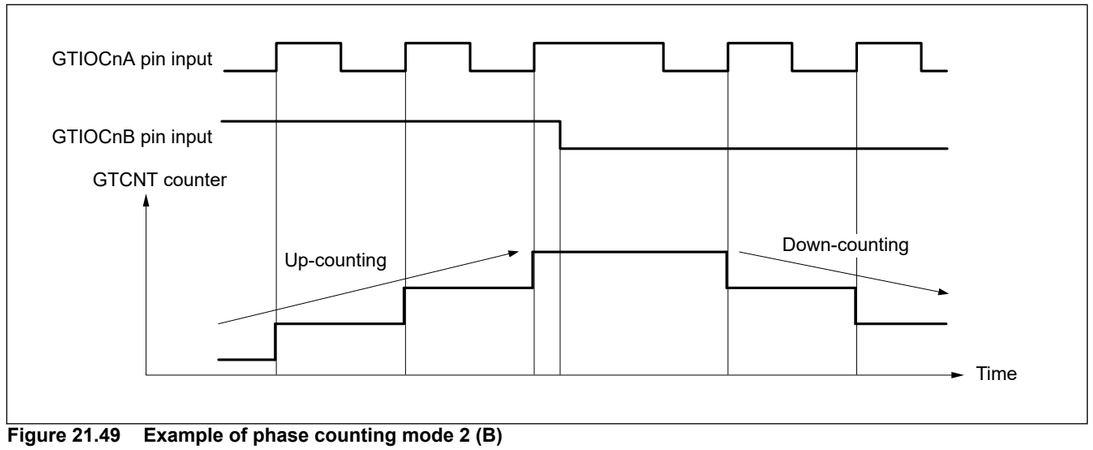

Figure 21.49 Example of phase counting mode 2 (B)

Table 21.31 Conditions of up-counting/down-counting in phase counting mode 2 (B)

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	Not counting	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

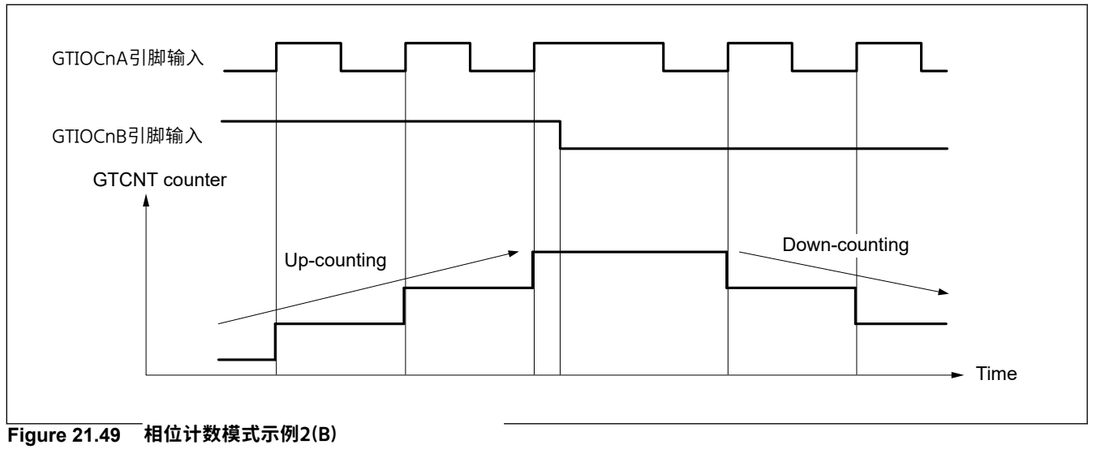

Figure 21.49 相位计数模式示例2(B)

Table 21.31 相位计数模式2(B)加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000200 GTDNSR = 0x00000100
Low	↓		
↑	Low	Down-counting	
↓	High	不算数	
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	不算数	

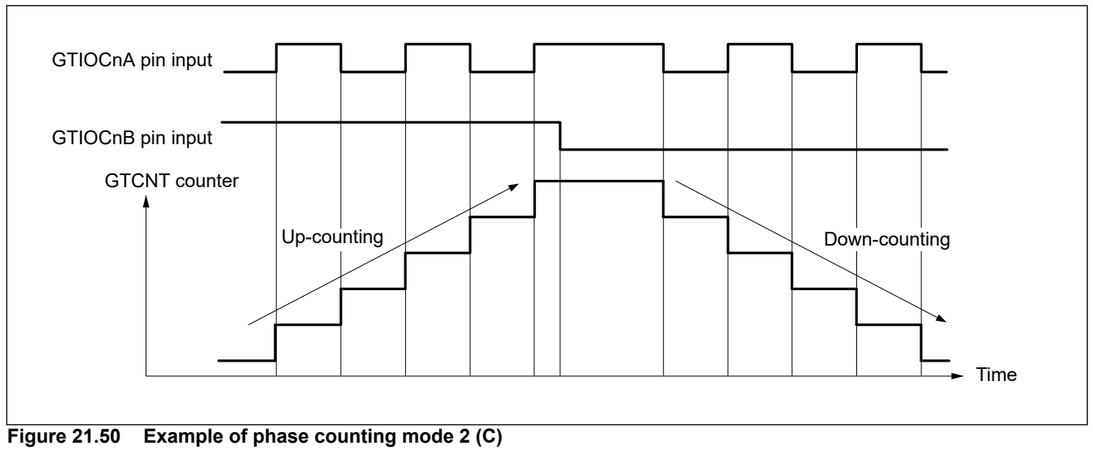

Figure 21.50 Example of phase counting mode 2 (C)

Table 21.32 Conditions of up-counting/down-counting in phase counting mode 2 (C)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	Not counting	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

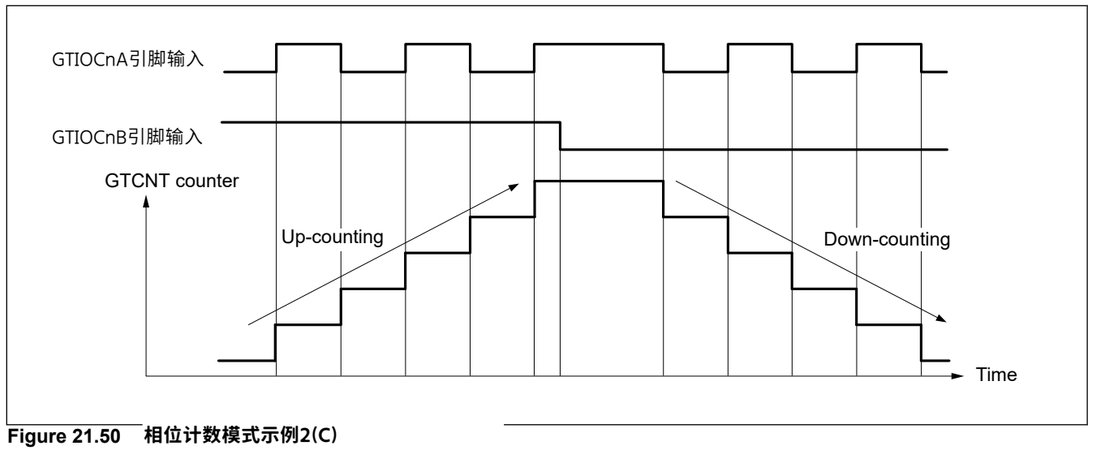

Figure 21.50 相位计数模式示例2(C)

Table 21.32 相位计数模式2(C)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000A00 GTDNSR = 0x00000500
Low	↓		
↑	Low	Down-counting	
↓	High	Up-counting	
High	↓	不算数	
Low	↑		
↑	High	Up-counting	
↓	Low	Down-counting	

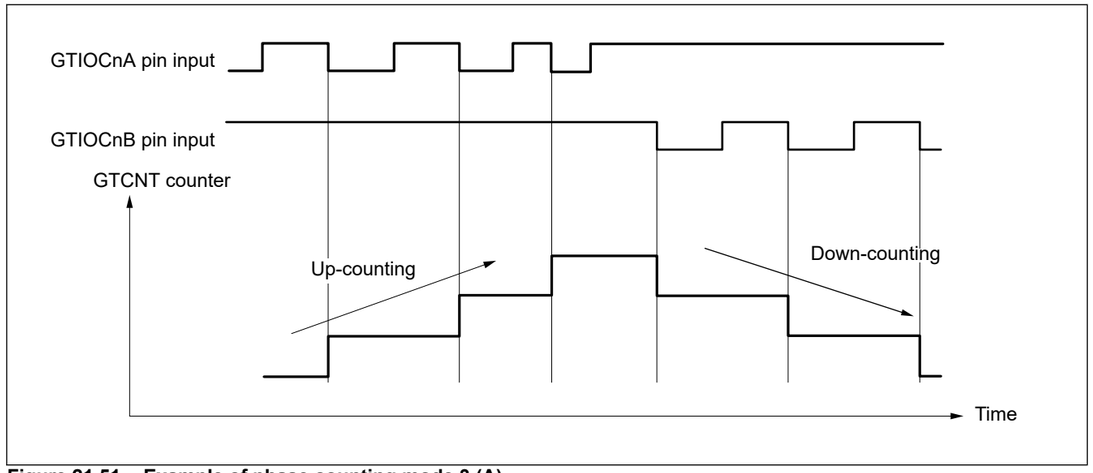

Figure 21.51 Example of phase counting mode 3 (A)

Table 21.33 Conditions of up-counting/down-counting in phase counting mode 3 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Not counting	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High		
↓	Low		

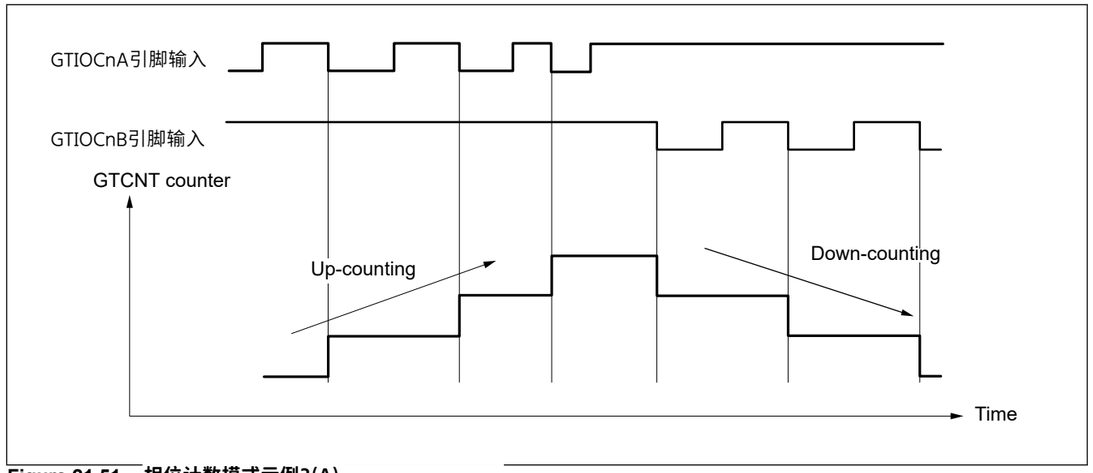

Figure 21.51 相位计数模式示例3(A)

Table 21.33 相位计数模式3(A)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	不算数	GTUPSR = 0x00000800 GTDNSR = 0x00008000
Low	↓		
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	不算数	
↑	High		
↓	Low		

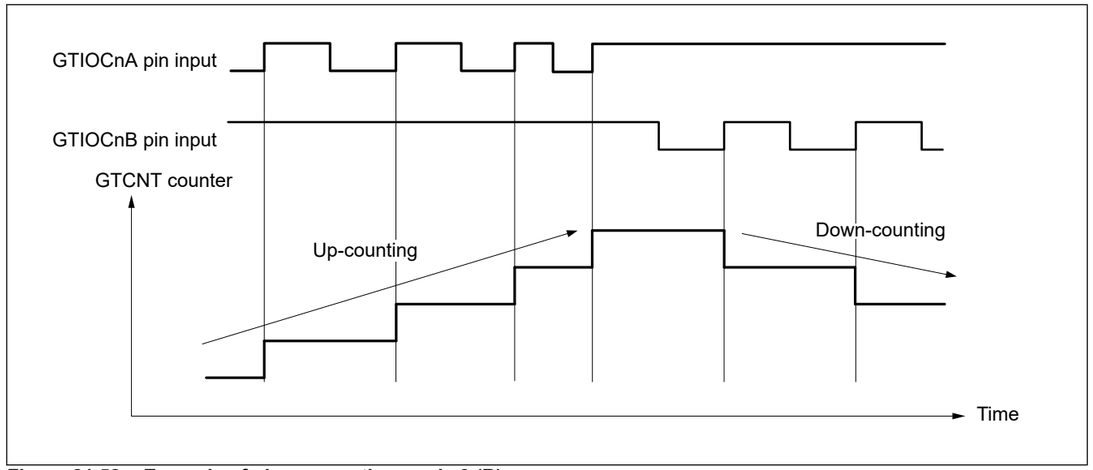

Figure 21.52 Example of phase counting mode 3 (B)

Table 21.34 Conditions of up-counting/down-counting in phase counting mode 3 (B)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	Not counting	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	Not counting	

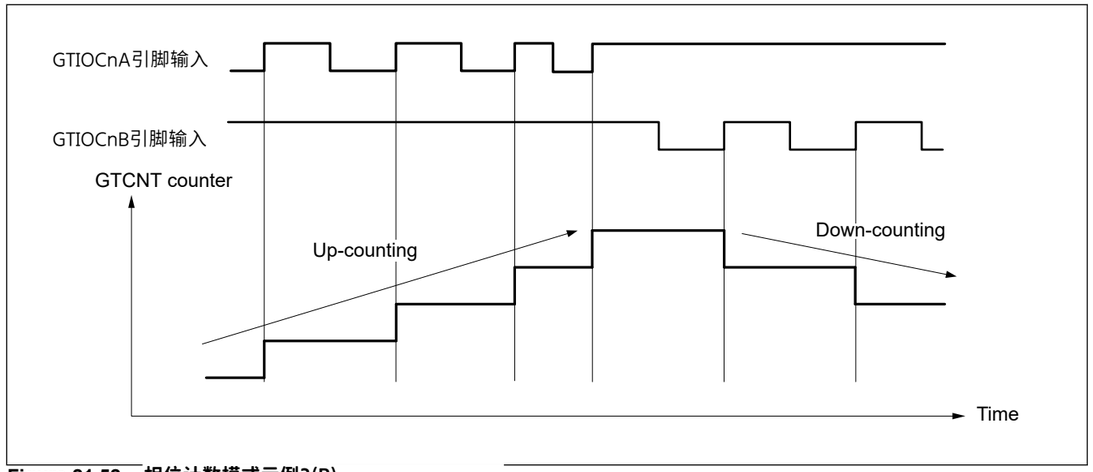

Figure 21.52 相位计数模式示例3(B)

Table 21.34 相位计数模式3(B)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0x00000200 GTDNSR = 0x00002000
Low	↓	不算数	
↑	Low		
↓	High		
High	↓		
Low	↑		
↑	High	Up-counting	
↓	Low	不算数	

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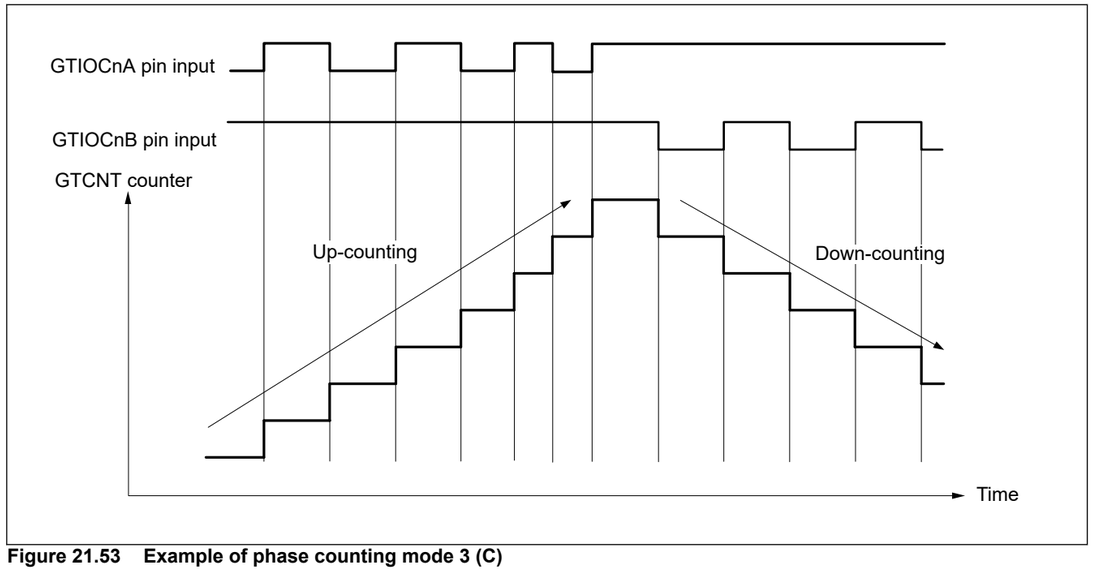

Figure 21.53 Example of phase counting mode 3 (C)

Table 21.35 Conditions of up-counting/down-counting in phase counting mode 3 (C)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	Not counting	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	Not counting	
↑	High	Up-counting	
↓	Low	Not counting	

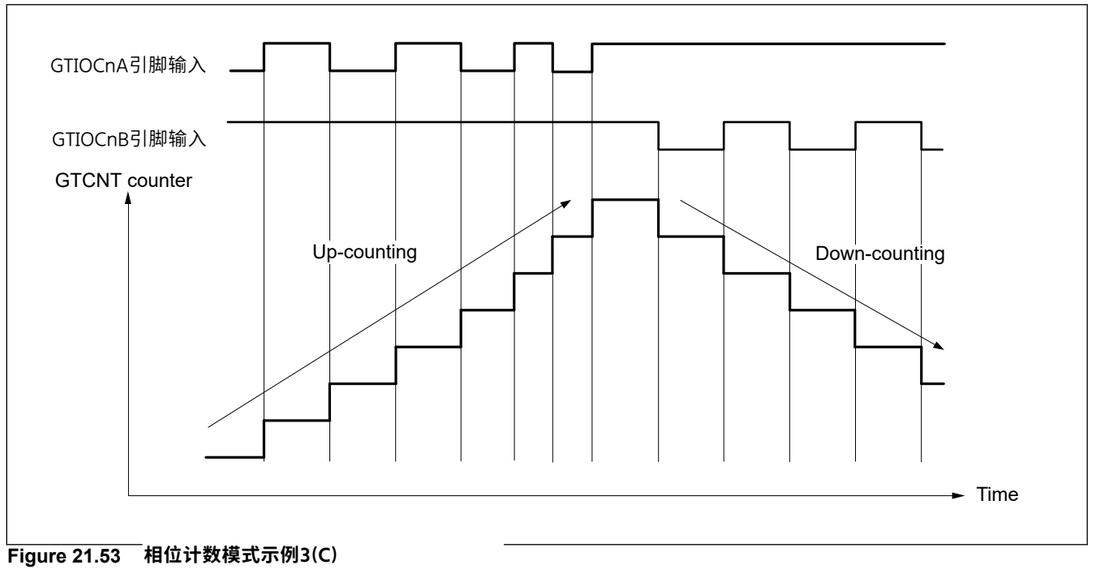

Figure 21.53 相位计数模式示例3(C)

Table 21.35 相位计数模式3(C)加减计数条件

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Down-counting	GTUPSR = 0x00000A00 GTDNSR = 0x0000A000
Low	↓	不算数	
↑	Low		
↓	High	Up-counting	
High	↓	Down-counting	
Low	↑	不算数	
↑	High	Up-counting	
↓	Low	不算数	

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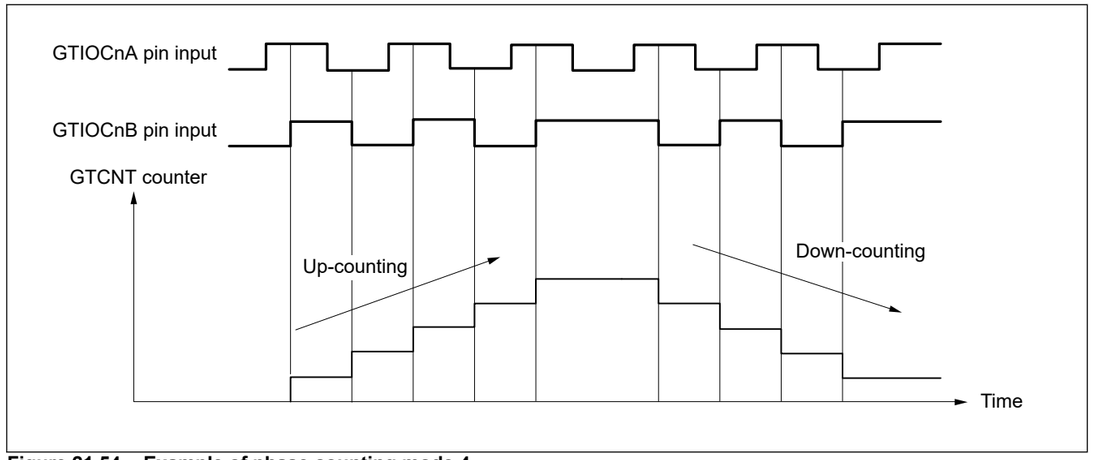

Figure 21.54 Example of phase counting mode 4

Table 21.36 Conditions of up-counting/down-counting in phase counting mode 4

↑ : Rising edge

↓ : Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	Not counting	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	Not counting	
↓	Low		

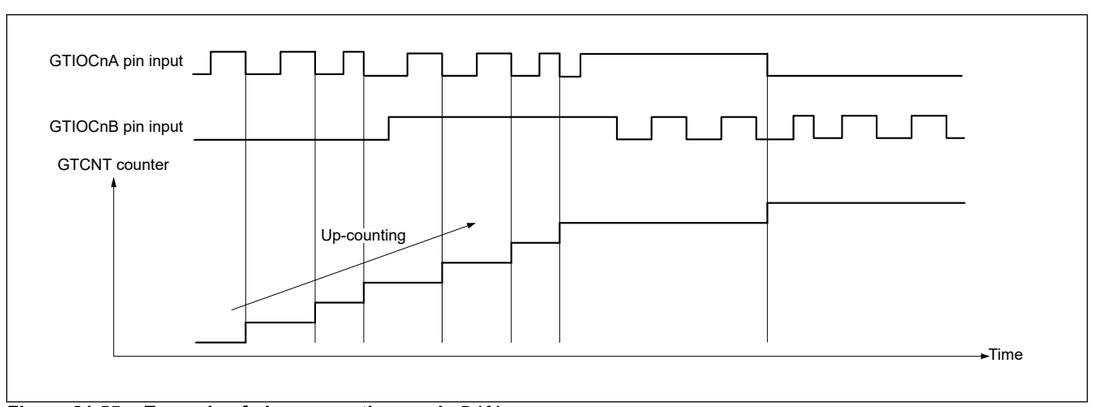

Figure 21.55 Example of phase counting mode 5 (A)

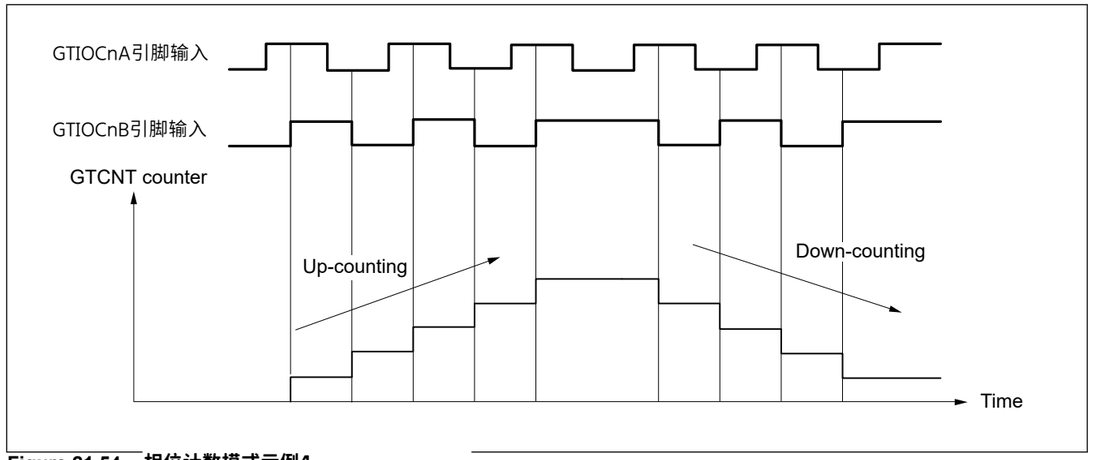

Figure 21.54 相位计数模式示例4

Table 21.36 相位计数方式4加减计数条件

↑ :上升沿

↓ :下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High	↑	Up-counting	GTUPSR = 0x00006000 GTDNSR = 0x00009000
Low	↓		
↑	Low	不算数	
↓	High		
High	↓	Down-counting	
Low	↑		
↑	High	不算数	
↓	Low		

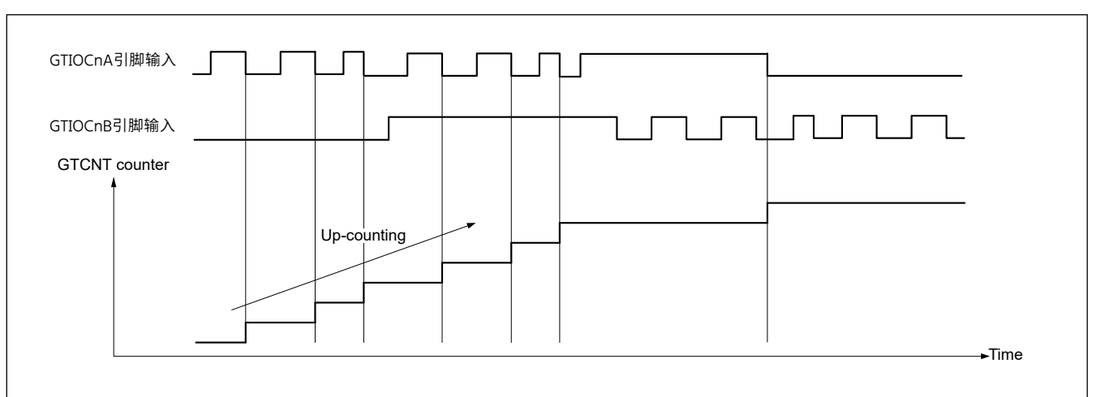

Figure 21.55 相位计数模式示例5(A)

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Table 21.37 Conditions of up-counting/down-counting in phase counting mode 5 (A)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High		Not counting	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low			
	Low		
	High	Up-counting	
High		Not counting	
Low			
	High		
	Low	Up-counting	

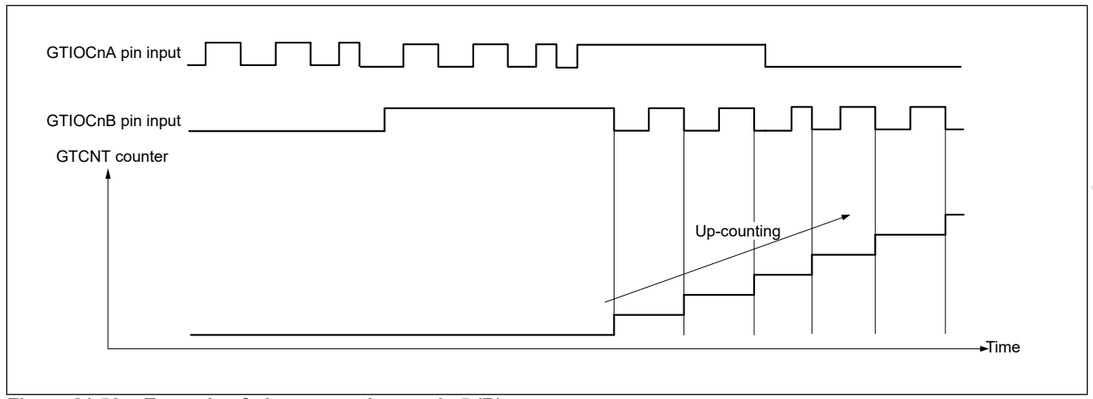


Figure 21.56 Example of phase counting mode 5 (B)

Table 21.37 相位计数模式下加减计数条件5（A）

:上升沿

:下降沿

GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High		不算数	GTUPSR = 0x00000C00 GTDNSR = 0x00000000
Low			
	Low		
	High	Up-counting	
High		不算数	
Low			
	High		
	Low	Up-counting	

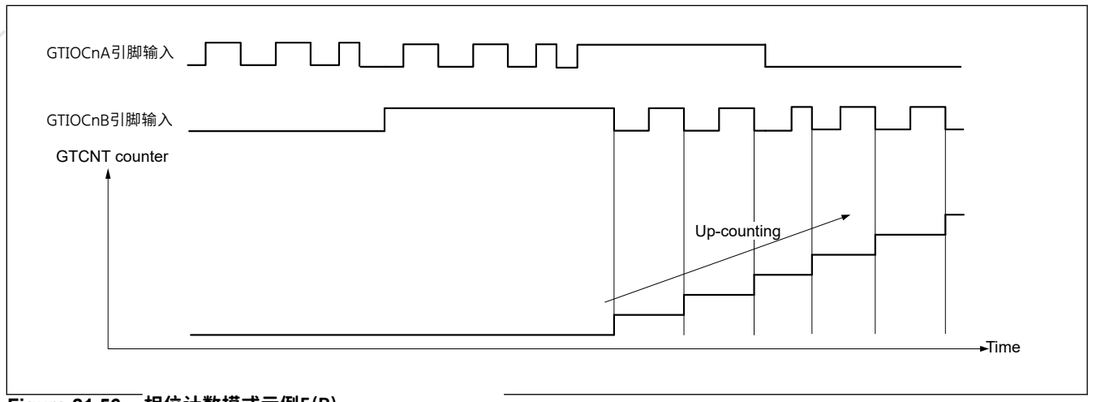


Figure 21.56 相位计数模式示例5(B)

Table 21.38 Conditions of up-counting/down-counting in phase counting mode 5 (B)

: Rising edge

: Falling edge

GTIOCnA pin input	GTIOCnB pin input	Operation	Register setting
High		Not counting	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low		Up-counting	
	Low	Not counting	
	High		
High		Up-counting	
Low		Not counting	
	High		
	Low		

21.3.12 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT320.GTIOC0A.

Figure 21.57 shows the conceptual diagram of GPT_OPS control flow.

Table 21.38 相位计数模式下加减计数条件5(B)

:上升沿

:下降沿

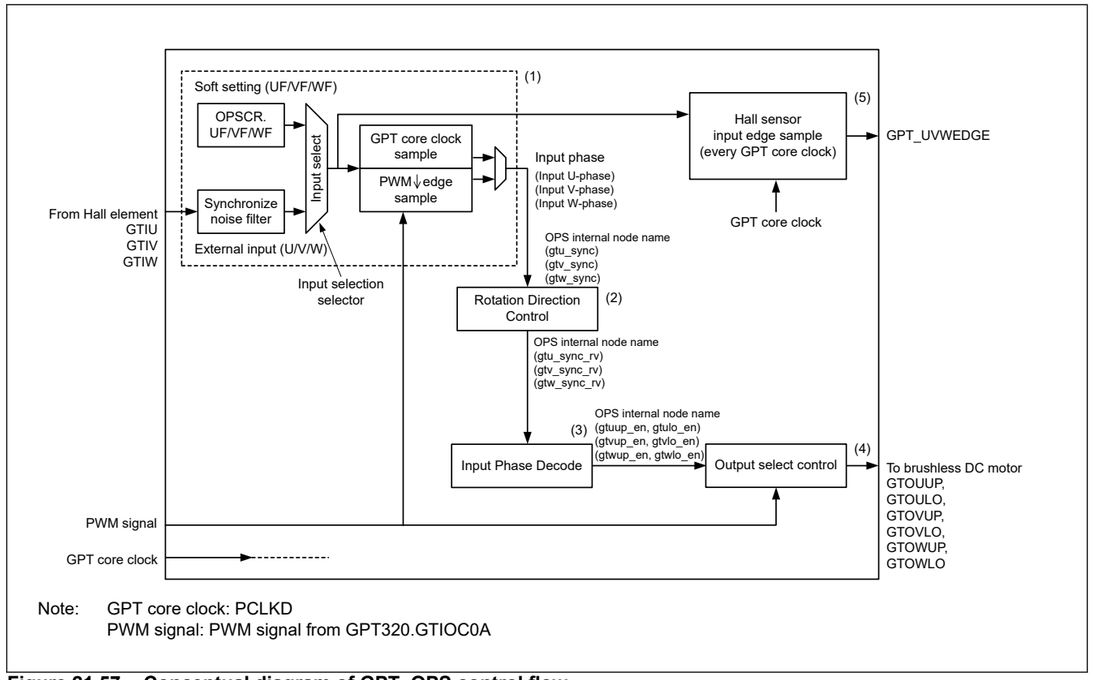
GTIOCnA引脚输入	GTIOCnB引脚输入	Operation	注册设置
High		不算数	GTUPSR = 0x0000C000 GTDNSR = 0x00000000
Low		Up-counting	
	Low	不算数	
	High		
High		Up-counting	
Low		不算数	
	High		
	Low		

21.3.12 输出相位切换(GPT_OPS)

GPT_OPS提供使用输出相位切换控制轻松控制无刷直流电机运行的功能
Register (OPSCR).

GPT_OPS输出用于斩波控制的PWM信号或6相电机控制的每一相（U正相负相、V正相负相、W正相负相）的电平信号。该功能使用软件设置的软设置值（OPSCR.UF、VF、WF）或霍尔元件检测到的外部信号，GPT320.GTIOC0A的PWM波形。

图21.57显示了GPT_OPS控制流程的概念图。

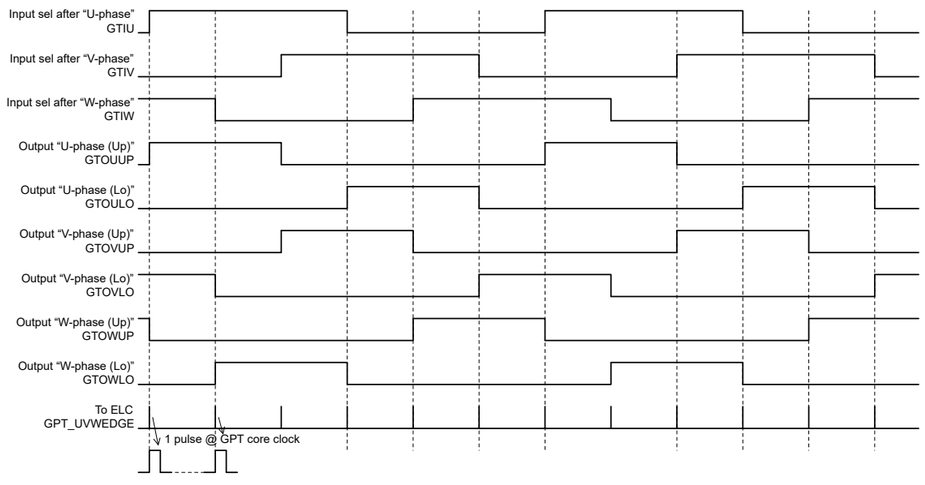


Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT320.GTIOC0A

Figure 21.57 Conceptual diagram of GPT_OPS control flow

Figure 21.58 shows a 6-phase level signals output example of a GPT_OPS operation.

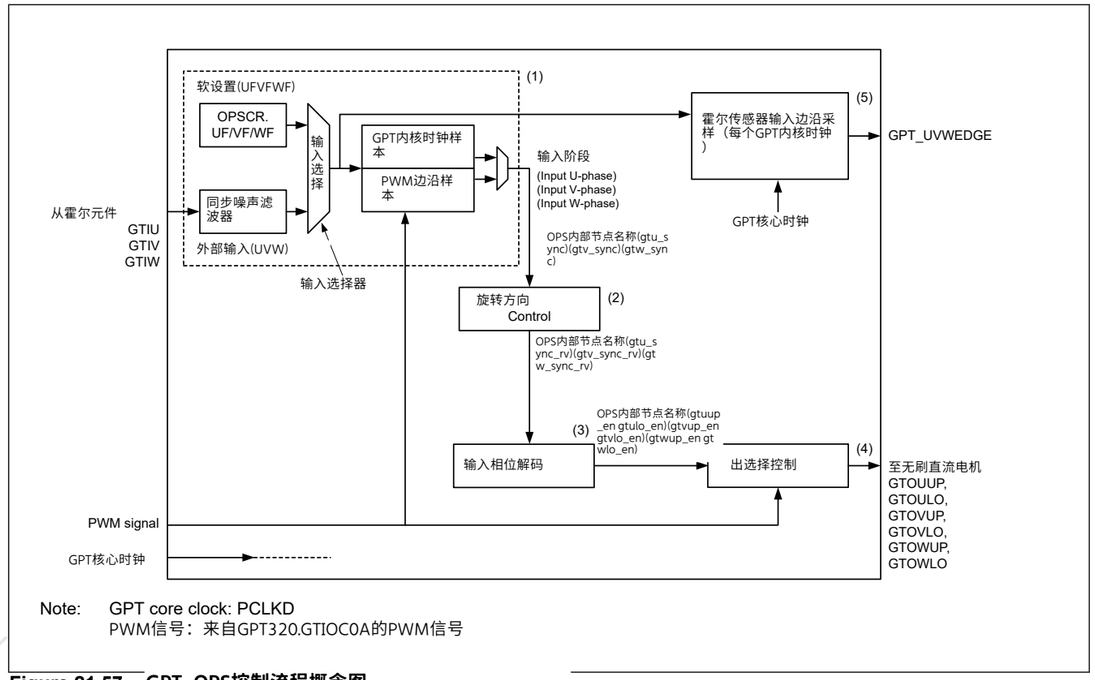
The GPT_UVWEDGE signal in Figure 21.58 is the Hall sensor input edge to ELC output.



Note: Register settings : OPSCR.ALIGN = 0, OPSCR.EN = 1, OPSCR.P = 0, OPSCR.N = 0, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD

Figure 21.58 Example of 6-phase level output operation

Figure 21.59 shows a 6-phase PWM output example of a GPT_OPS operation with chopper control.

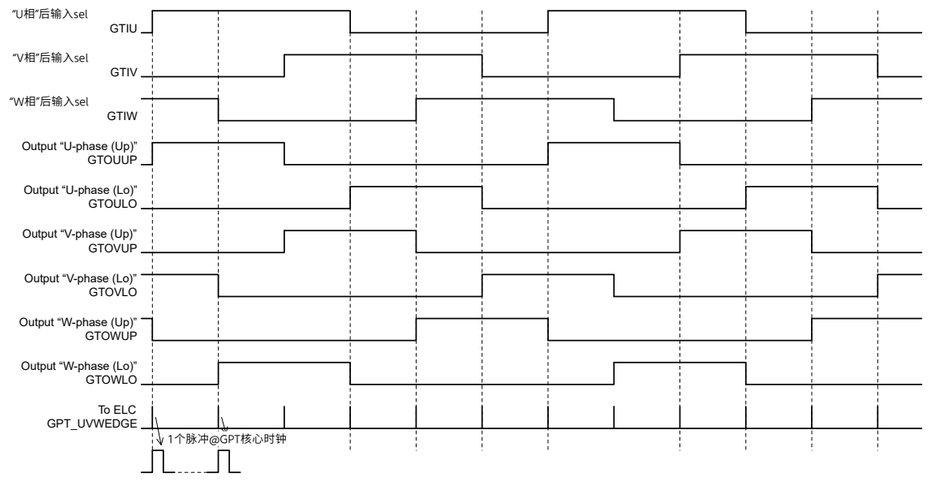


Note: GPT core clock: PCLKD
PWM信号：来自GPT320.GTIOC0A的PWM信号

Figure 21.57 GPT_OPS控制流程概念图

图21.58显示了GPT_OPS操作的6相电平信号输出示例。

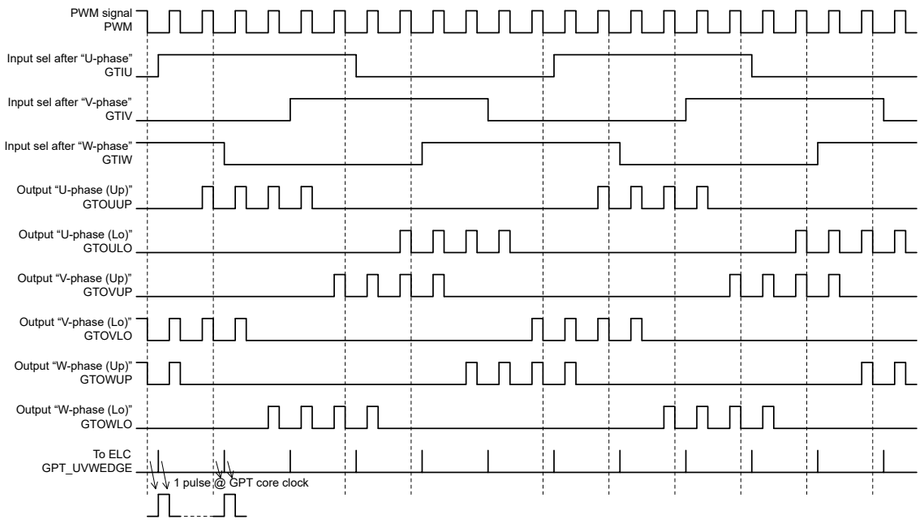
图21.58中的GPT_UVWEDGE信号是霍尔传感器输入边沿到ELC输出。



Note: 寄存器设置：OPSCR.ALIGN=0 OPSCR.EN=1 OPSCR.P=0 OPSCR.N=0 OPSCR.INV=0 OPSCR.RV=0
Note: GPT core clock: PCLKD

Figure 21.58 6相电平输出动作示例

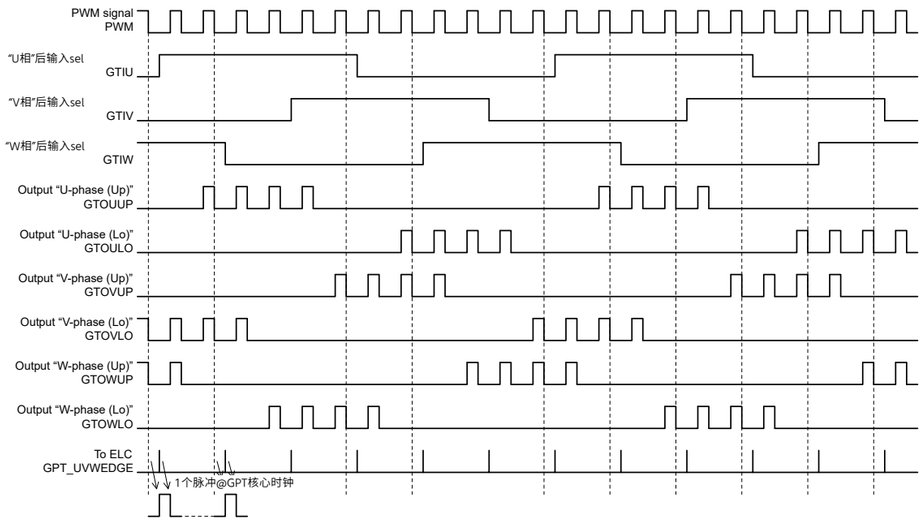
图21.59显示了带斩波器控制的GPT_OPS操作的6相PWM输出示例。



Note: Register settings : OPSCR.ALIGN = 1, OPSCR.EN = 1, OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT320.GTIOC0A

Figure 21.59 Example of 6-phase PWM output operation with chopper control

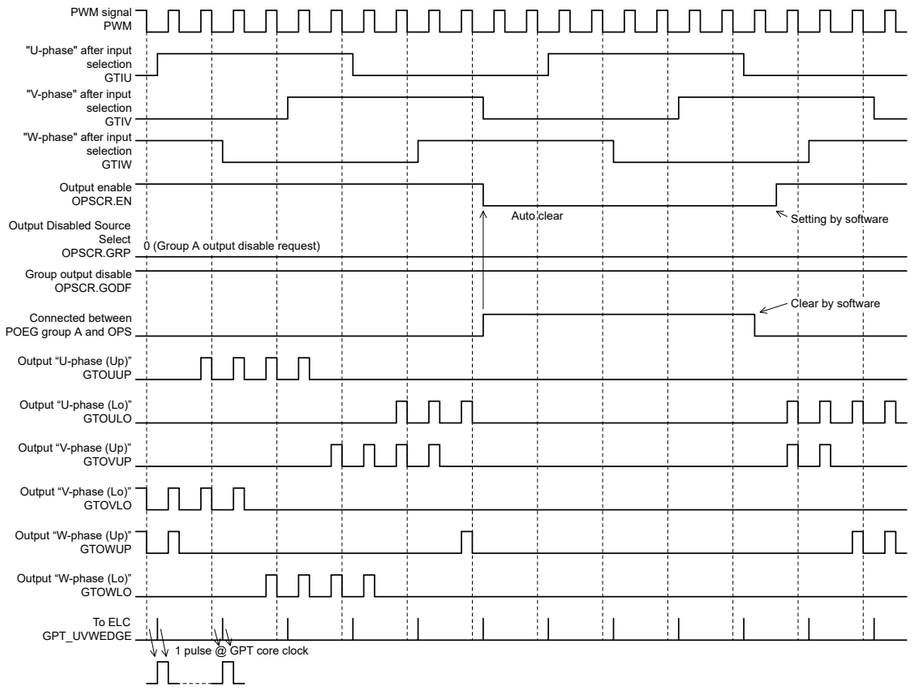
Figure 21.60 shows a 6-phase PWM output example of an output disable control operation.



Note: 寄存器设置：OPSCR.ALIGN=1 OPSCR.EN=1 OPSCR.P=1 OPSCR.N=1 OPSCR.INV=0 OPSCR.RV=0
Note: GPT core clock: PCLKD
PWM信号：来自GPT320.GTIOC0A的PWM信号

Figure 21.59 带斩波器控制的6相PWM输出操作示例

图21.60显示了输出禁用控制操作的6相PWM输出示例。



Note: Register settings : OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0, OPSCR.RV = 0
Note: GPT core clock: PCLKD
PWM signal: PWM signal from GPT320.GTIOC0A

Figure 21.60 Example of group output disable control operation

21.3.12.1 Input selection and synchronization of external input signal

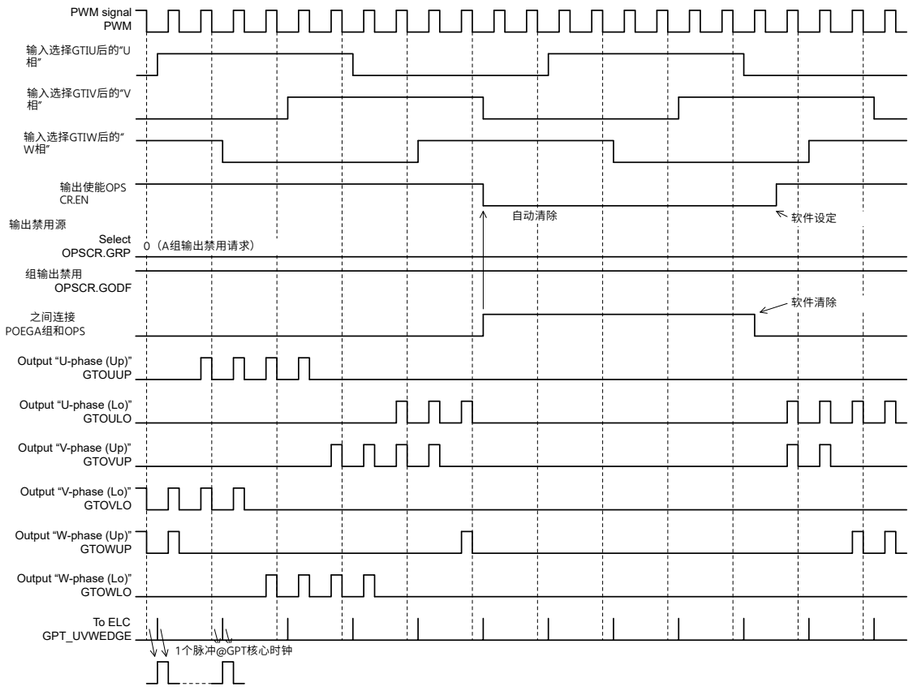
In the GPT_OPS control flow conceptual diagram shown in Figure 21.57, (1) is a selection of input phase from the software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit is 0, select the external input. Enable the input signal after synchronization with the GPT core clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT320.GTIOC0A) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.FB bit is 1, select the soft setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT320.GTIOC0A) using falling edge sampling with OPSCR.ALIGN bit set to 1.

When OPSCR.ALIGN bit is 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit set to 0 or OPSCR.FB bit set to 1. However, there are cases where the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before/just after) is shortened.

Table 21.39 shows the input selection process and setting of associated OPSCR bits.



Note: 寄存器设置：OPSCR.P=1 OPSCR.N=1 OPSCR.INV=0 OPSCR.RV=0
Note: GPT core clock: PCLKD
PWM信号：来自GPT320.GTIOC0A的PWM信号

Figure 21.60 组输出禁用控制操作示例

21.3.12.1 外部输入信号的输入选择和同步

在图21.57所示的GPT_OPS控制流程概念图中，(1)是通过OPSCR.FB位从软件设置和外部输入中选择输入相位。

当OPSCR.FB位为0时，选择外部输入。与GPT内核时钟(PCLKD)同步后启用输入信号。执行噪声过滤（可选）后，使用下降沿采样将外部输入设置为PWM的输入相位（GPT320.GTIOC0A的PWM），并将OPSCR.ALIGN位设置为1。

当OPSCR.FB位为1时，选择软设置（OPSCR.UF、VF、WF）与PWM的输入相位值（PWM的GPT320.GTIOC0A)使用下降沿采样，并将OPSCR.ALIGN位设置为1。

当OPSCR.ALIGN位为0时，GPT_OPS以PCLKD同步的输入相位运行，其中OPSCR.FB位设置为0或OPSCR.FB位设置为1。但是，输出UVW相位的PWM脉冲宽度存在某些情况（PWM输出模式）的开关时间（就在之前）被缩短了。

表21.39显示了输入选择过程和相关OPSCR位的设置。

Table 21.39 Input selection processing method

Register OPSCR		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD synchronization + falling edge sample)	Input Phase Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD synchronization + through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of falling edge sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD synchronization)	

21.3.12.2 Input sampling

The OPSCR.U, V, W bits indicate the PCLKD sampling results of the input selected in the OPSCR.FB bit.

When OPSCR.FB bit is 0 and after synchronization with the GPT core clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits indicate the sampling results of the external input. When OPSCR.FB bit is 1, OPSCR.U, V, W bits are the value (OPSCR.UF, VF, WF) of the soft setting.

21.3.12.3 Input phase decode

In the GPT_OPS control flow conceptual diagram shown in Figure 21.57, (3) enables the 6-phase signals by decoding the input phase selected in the OPSCR.FB bit.

Table 21.40 shows the decode table of input phase when OPSCR.RV bit is 0.

Table 21.40 Decode table of input phase (OPSCR.RV = 0)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

Table 21.41 Decode table of input phase (OPSCR.RV = 1) (1 of 2)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	0

Table 21.39 输入选择处理方法

Register OPSCR		输入相位采样方式的选择（UVW-phase）	同步输入输出选择过程（GPT_OPS内部节点名）
FB bit	对齐位		
0	1	PWM下降沿采样的外部输入（PCLKD同步+下降沿采样）	输入相位 Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	PCLKD同步输出端的外部输入（PCLKD同步+直通模式）	
1	1	PWM下降沿采样的软件设置（下降沿采样的OPSCR.UF、VF、WF）	
	0	软件设置值选择（=OPSCR.UFVFWF值）（=PCLKD同步）	

21.3.12.2 输入采样

OPSCR.U、V、W位指示在OPSCR.FB位中选择的输入的PCLKD采样结果。

当OPSCR.FB位为0并与GPT内核时钟(PCLKD)和噪声过滤（可选）同步后，OPSCR.U、V、W位表示外部输入的采样结果。当OPSCR.FB位为1时，OPSCR.U、V、W位为软设置的值（OPSCR.UF、VF、WF）。

21.3.12.3 输入相位解码

在图21.57所示的GPT_OPS控制流程概念图中，(3)通过解码在OPSCR.FB位中选择的输入相位来启用6相位信号。

表21.40为OPSCR.RV位为0时的输入相位解码表。

Table 21.40 输入相位解码表(OPSCR.RV=0)

输入相位(UVW)（GPT_OPS内部节点名称）			6-phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

Table 21.41 输入相位解码表(OPSCR.RV=1)(1of2)

输入相位(UVW)（GPT_OPS内部节点名称）			6-phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	0	1	1	0	0	0
1	0	0	0	1	0	0	1	0
1	1	0	0	0	0	1	1	0

Table 21.41 Decode table of input phase (OPSCR.RV = 1) (2 of 2)

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1
0	0	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

21.3.12.4 Rotation Direction Control

In the GPT_OPS control flow conceptual diagram shown in Figure 21.57, (2) controls the direction of rotation of a 3-phase motor using the OPSCR.RV bit.

When the rotation direction is reverse (RV bit = 1), the input phase is inverted.

Table 21.42 shows the assigned output phases based on the OPSCR.RV bit setting (before and after rotation direction control).

Table 21.42 Rotation Direction Control Method

Reversal of Direction of Rotation Using Output Phases as Specified in OPSCR Register	Output of Rotation Direction Control [U/V/W (Positive/Negative)] (GPT_OPS Internal Node Name after Control)					
OPSCR.RV bit	(gtuup_ren)	(gtulo_ren)	(gtvup_ren)	(gtvlo_ren)	(gtwup_ren)	(gtwlo_ren)
0	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)
1	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)

21.3.12.5 Output selection control

In the GPT_OPS control flow conceptual diagram in Figure 21.57, (4) represents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P and OPSCR.N bits can select from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to a positive logic or negative logic by the OPSCR. INV bit.

Table 21.43 and Table 21.44 show the output selection control method using the OPSCR register bit.

Table 21.43 Output selection control method (positive phase) (1 of 2)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output

Table 21.41 输入相位解码表(OPSCR.RV=1)(2of2)

输入相位(UVW)（GPT_OPS内部节点名称）			6-phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
Input U-Phase	Input V-Phase	Input W-Phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	0	0	1
0	0	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

21.3.12.4 旋转方向控制

在图21.57所示的GPT_OPS控制流程概念图中，(2)使用OPSCR.RV位控制三相电机的旋转方向。

当旋转方向为反向时（RV位=1），输入相位反转。

表21.42显示了基于OPSCR.RV位设置（旋转方向控制之前和之后）分配的输出相位。

Table 21.42 旋转方向控制方式

使用输出相位反转旋转方向 在OPSCR中指定Register	旋转方向控制输出[UVW（正负）] (GPT_OPS控制后的内部节点名称)					
OPSCR.RV bit	(gtuup_ren)	(gtulo_ren)	(gtvup_ren)	(gtvlo_ren)	(gtwup_ren)	(gtwlo_ren)
0	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)
1	U-phase (Up) (gtuup_en)	U-phase (Lo) (gtulo_en)	W-phase (Up) (gtwup_en)	W-phase (Lo) (gtwlo_en)	V-phase (Up) (gtvup_en)	V-phase (Lo) (gtvlo_en)

21.3.12.5 输出选择控制

在图21.57的GPT_OPS控制流程概念图中，(4)表示通过设置OPSCR寄存器位来选择输出波形。

对于输出选择，以下位是相关的：

- ●OPSCR.EN位控制是输出6相输出，还是停止
- ●OPSCR.P和OPSCR.N位可以选择输出相位的电平信号或PWM信号（斩波器输出）
- ●输出相的极性可以通过OPSCR设置为正逻辑或负逻辑。INV位。

表21.43和表21.44显示了使用OPSCR寄存器位的输出选择控制方法。

Table 21.43 输出选择控制方式（正相）（1of2）

使能相位输出控制	正相输出(P)控制	反相输出控制	输出端口名称（正相=向上）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS→0输出

Table 21.43 Output selection control method (positive phase) (2 of 2)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
1	0	0	Level signal (gtuup_ren) (gtvup_ren) (gtwup_ren)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_ren) (~gtvup_ren) (~gtwup_ren)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_ren) (PWM & gtvup_ren) (PWM & gtwup_ren)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_ren)) (~(PWM & gtvup_ren)) (~(PWM & gtwup_ren))	PWM Output Mode (Positive phase) (Negative logic)

Table 21.44 Output selection control method (negative phase)

Enable-phase output control	Positive-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN	OPSCR.N	OPSCR.INV	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS → 0 output
1	0	0	Level signal (gtulo_ren) (gtvlo_ren) (gtwlo_ren)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_ren) (~gtvlo_ren) (~gtwlo_ren)	Level Output Mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_ren) (PWM & gtvlo_ren) (PWM & gtwlo_ren)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_ren)) (~(PWM & gtvlo_ren)) (~(PWM & gtwlo_ren))	PWM Output Mode (Negative phase) (Negative logic)

21.3.12.6 Output selection control (group output disable function)

When OPSCR.GODF is 1 and the signal value selected by the OPSCR.GRP bit is high (output disable request), the group output-disable function asynchronously sets the output to Hi-Z. When an output-disable request is generated, the OPSCR.EN bit is cleared to 0. For the return, set the OPSCR.EN bit to 1 after clearing the output disable request by software.

To ensure output-disable control, use the POEG_GROUPn (n = A to D) interrupt to clear the flag in the POE or check that the OPSCR.EN bit is 0 and then clear the flag. For an example of the operation of group output disable control, see Figure 21.60.

Table 21.43 输出选择控制方式（正相）（2of2）

使能相位输出控制	正相输出(P)控制	反相输出控制	输出端口名称（正相=向上）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.P	OPSCR.INV	GTOUUP GTOVUP GTOWUP	Mode
1	0	0	电平信号(gtuup_ren)(gtvup_ren)(gtwup_ren)	电平输出模式（正相）（正逻辑）
1	0	1	电平信号(~gtuup_ren)(~gtvup_ren)(~gtwup_ren)	电平输出模式（正相）（负逻辑）
1	1	0	PWM signal (PWM & gtuup_ren) (PWM & gtvup_ren) (PWM & gtwup_ren)	PWM输出模式（正相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtuup_ren)) (~(PWM & gtvup_ren)) (~(PWM & gtwup_ren))	PWM输出模式（正相）（负逻辑）

Table 21.44 输出选择控制方式（负相）

使能相位输出控制	正相输出(N)控制	反相输出控制	输出端口名称（负相=Lo）（输出选择内部节点分配）	
OPSCR.EN	OPSCR.N	OPSCR.INV	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS→0输出
1	0	0	电平信号(gtulo_ren)(gtvlo_ren)(gtwlo_ren)	电平输出模式（负相）（正逻辑）
1	0	1	电平信号(~gtulo_ren)(~gtvlo_ren)(~gtwlo_ren)	电平输出模式（负相）（负逻辑）
1	1	0	PWM signal (PWM & gtulo_ren) (PWM & gtvlo_ren) (PWM & gtwlo_ren)	PWM输出模式（负相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtulo_ren)) (~(PWM & gtvlo_ren)) (~(PWM & gtwlo_ren))	PWM输出模式（负相）（负逻辑）

21.3.12.6 输出选择控制（组输出禁用功能）

当OPSCR.GODF为1且OPSCR.GRP位选择的信号值为高电平（输出禁用请求）时，组输出禁用功能异步将输出设置为Hi-Z。产生输出禁止请求时，OPSCR.EN位清零。返回时，请在软件清除输出禁止请求后将OPSCR.EN位设置为1。

为确保输出禁用控制，请使用POEG_GROUPn（n=A到D）中断清除POE中的标志或检查OPSCR.EN位是否为0，然后清除标志。组输出禁用控制的操作示例见图21.60。

21.3.12.7 Event Link Controller (ELC) output

In the GPT_OPS control flow conceptual diagram shown in Figure 21.57, (5) outputs the Hall sensor input signal edge to the ELC.

The Hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase of the input phase is short in duration, the Hall sensor edge input signal is not output at that time.

When the OPSCR.FB bit is 0, the Hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit is 1, the Hall sensor input edge signal is the logical OR of the edge of the soft setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 21.58 to Figure 21.60 for examples of the output signal to the ELC.

21.3.12.8 GPT_OPS start operation setting flow

Table 21.45 Example setting of GPT_OPS start operation

No.	Step Name	Description
1	GPT320 operation mode setting	GPT320.GTIOC0A set the PWM output operation mode of the saw-wave or triangle-wave. For details, see section 21.3.3. PWM Output Operating Mode.
2	Counting of GPT320	Start the count operation of GPT320, and outputs a PWM waveform.
3	GPT_OPS input data set (only software setting is selected)	Set software setting to OPSCR.UF, VF, and WF bits.
4	Noise filter settings of GPT_OPS external input (only external input is selected)	When using a noise filter, set the sampling clock of the noise filter by OPSCR.NFCS[1:0] bits. Then the noise filter is enabled if OPSCR.NFEN = 1.
5	GPT_OPS input phase selection setting/input phase alignment setting	Select the input phase from the external input or software setting by OPSCR.FB bit. Select the alignment of the input phase by OPSCR.ALIGN bit.
6	Setting the GPT_OPS output phase	Set the level output/PWM output of the positive/negative phase output by OPSCR.P/OPSCR.N bit. Set the positive logic/negative logic of the output phase by OPSCR.INV bit. Set the rotation direction by OPSCR.RV bit
7	GPT_OPS setting the group output disable function	Set the selection of output disable source by OPSCR.GRP bit. Perform the setting of on/off of the group output disable function by OPSCR.GODF bit.
8	GPT_OPS Working	Setting the OPSCR.EN = 1 outputs the 6-phase output to drive the brushless DC motor from the GPT_OPS.

21.3.13 Inter Channel Logical Operation Function

The logical operation function between compare match outputs can be performed.

Figure 21.61 shows the block diagram of inter channel logical operation.

To prevent hazard to the GPT output, the signal after logical operation is latched with PCLKD. After latching, the output disable control is performed.

When the logical operation function which causes the delay of 1 PCLKD is selected, the output enable signal is also delayed with 1 PCLKD and input to the output disable control.

When the same signal (C = A or D = B) to operate logical function AND, OR, EXOR and NOR is selected, C or D is treated as 1. In the case of GTIOCnA pin output, when A of same channel is selected for C, the result of AND is A, the result of OR is 1, the result of EXOR is NOT A, and the result of NOR is 0.

21.3.12.7 事件链接控制器(ELC)输出

在图21.57所示的GPT_OPS控制流程概念图中，(5)将霍尔传感器输入信号沿输出到ELC。

霍尔传感器输入边沿信号是在PCLKD采样的每个U相V相W相输入的上升沿和下降沿信号的逻辑或。也就是说，如果输入相的U相V相W相中的每一个的高电平时段持续时间短，则此时不输出霍尔传感器边沿输入信号。

当OPSCR.FB位为0时，霍尔传感器输入边沿信号为在PCLKD采样的外部输入相位边沿信号的逻辑或。

当OPSCR.FB位为1时，霍尔传感器输入边沿信号为软设置边沿的逻辑或（OPSCR.UF，VF，WF）在PCLKD采样。

有关ELC的输出信号示例，请参见图21.58至图21.60。

21.3.12.8 GPT_OPS启动操作设置流程

Table 21.45 GPT_OPS启动操作的示例设置

No.	步骤名称	Description
1	GPT320操作模式设置	GPT320.GTIOC0A设置PWM输出工作模式为锯齿波或三角波。 详见21.3.3节。PWM输出工作模式。
2	GPT320的计数	启动GPT320的计数操作，并输出一个PWM波形。
3	GPT_OPS输入数据集（仅选择软件设置）	将软件设置设置为OPSCR.UF、VF和WF位。
4	噪声滤波器设置 GPT_OPS外部输入（仅选择外部输入）	使用噪声滤波器时，通过OPSCR.NFCS[1:0]位设置噪声滤波器的采样时钟。 如果OPSCR.NFEN=1，则启用噪声滤波器。
5	GPT_OPS输入相位选择设置 输入相位对齐设置	通过OPSCR.FB位从外部输入或软件设置中选择输入相位。 通过OPSCR.ALIGN位选择输入相位的对齐方式。
6	设置GPT_OPS输出阶段	通过OPSCR.POPSCR.N位设置正负相输出的电平输出PWM输出。 通过OPSCR.INV位设置输出相位的正逻辑负逻辑。通过OPSCR.RV位设置旋转方向
7	GPT_OPS设置组输出禁用功能	通过OPSCR.GRP位设置输出禁用源的选择。 通过OPSCR.GODF位执行组输出禁用功能的开关设置。
8	GPT_OPS Working	设置OPSCR.EN=1输出6相输出来驱动直流无刷电机 GPT_OPS.

21.3.13 通道间逻辑运算功能

可以执行比较匹配输出之间的逻辑运算功能。

图21.61显示了通道间逻辑操作的框图。

为防止对GPT输出造成危害，逻辑运算后的信号由PCLKD锁存。锁存后，执行输出禁用控制。

Whenthelogicaloperationfunctionwhichcausesthedelayof1PCLKDisselected theoutputenablesignalisalsodelayed with1PCLKDandinputtotheoutputdisablecontrol.

Whenthesamesignal(C=AorD=B)tooperatelogicalfunctionAND OR EXORandNORisselected CorDistreatedas1.Inthe caseofGTIOCnApinoutput whenAofsamechannelisselected对于C，AND的结果是A，OR的结果是1，EXOR的结果是NOTA，NOR的结果是0。

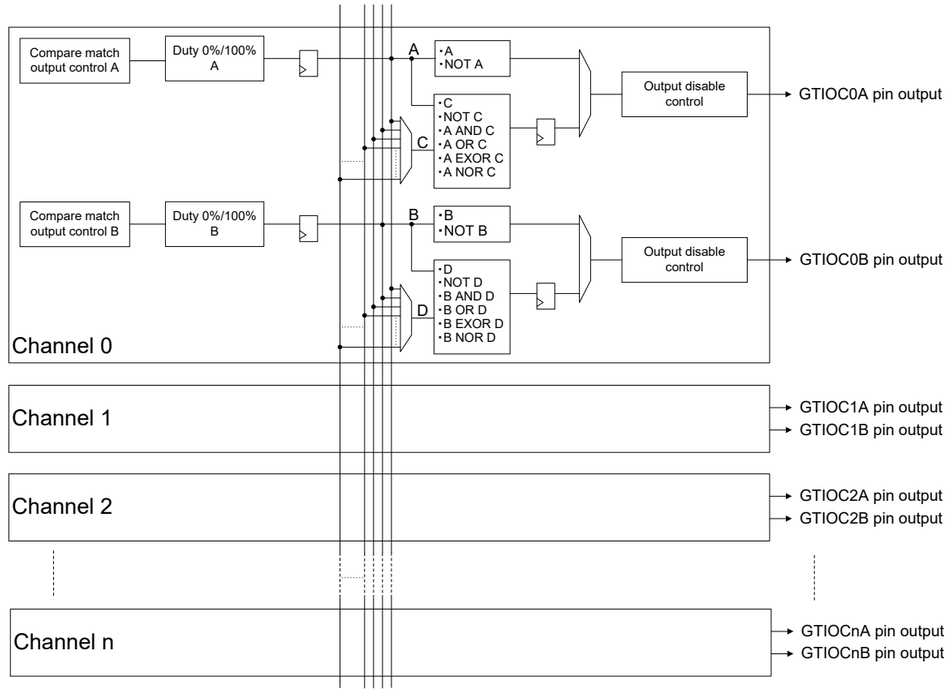


Figure 21.61 Block Diagram of Inter Channel Logical Operation

Figure 21.62 shows an example of inter channel logical operation.

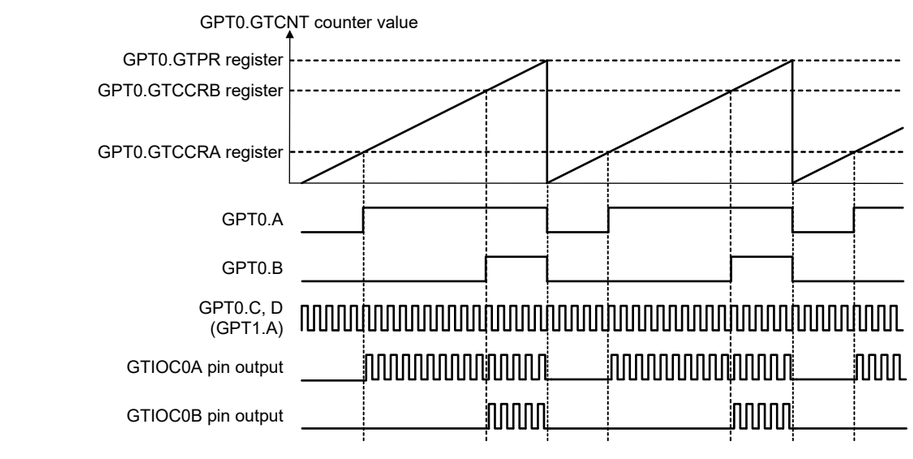


Figure 21.62 Example of Inter Channel Logical Operation

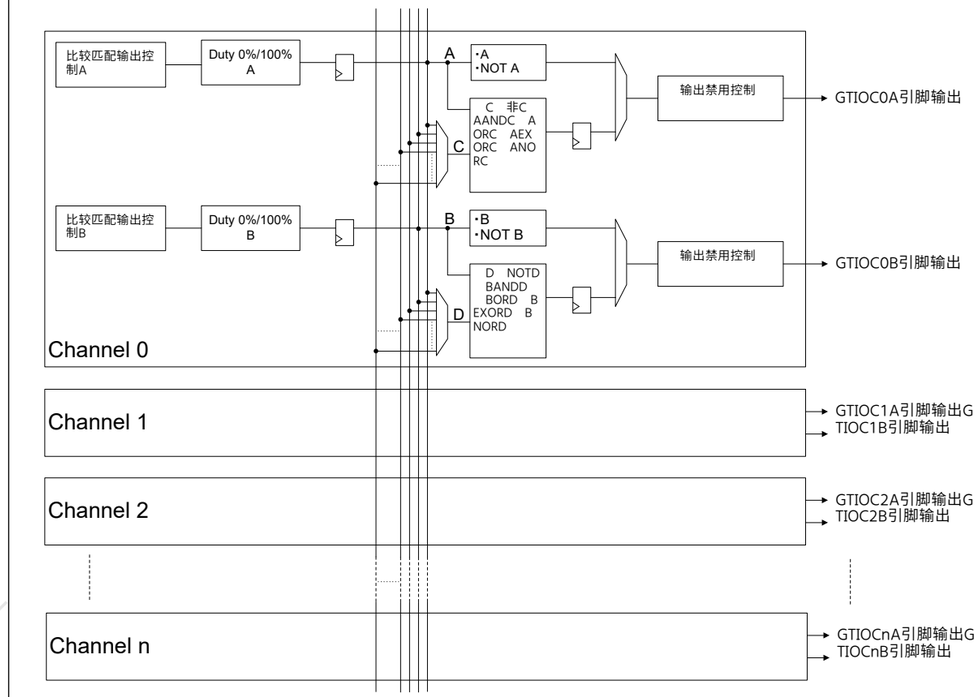


Figure 21.61 通道间逻辑操作框图

图21.62显示了通道间逻辑操作的示例。

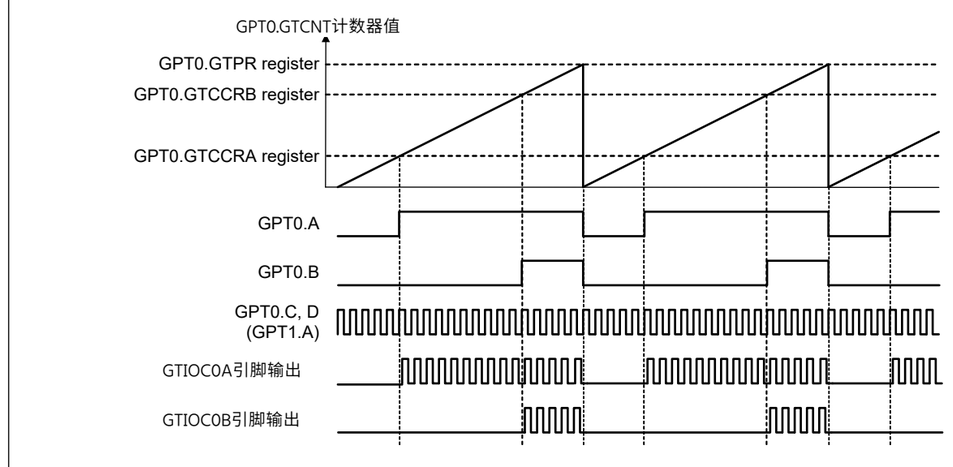


Figure 21.62 通道间逻辑运算示例

21.4 Interrupt Sources

21.4.1 Interrupt Sources

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTCNT counter overflow (GTPR compare match)/underflow.
- period count function finish

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. The Interrupt Controller Unit can change the relative channel priorities. However, the priority within a channel is fixed. For details, see section 13, Interrupt Controller Unit (ICU).

Table 21.46 lists the GPT interrupt sources.

Table 21.46 Interrupt sources

Channel	Name	Interrupt source	Interrupt flag	DTC activation
n = 0 to 3	GPTn_CCMPA	GPT32n.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT32n.GTCCRE compare match	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT32n.GTCCRF compare match	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT32n.GTCNT overflow (GPT32m.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_PC	Period count function finish (n = 0, 1)	GTST[31] (PCF)	Possible
n = 4 to 9	GPTn_CCMPA	GPT16n.GTCCRA input capture/compare match	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT16n.GTCCRB input capture/compare match	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT16n.GTCCRC compare match	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT16n.GTCCRD compare match	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT16n.GTCCRE compare match	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT16n.GTCCRF compare match	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT16n.GTCNT overflow (GPT320.GTPR compare match)	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT16n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_PC	Period count function finish (n = 4 to 6)	GTST[31] (PCF)	Possible

(1) GPTn_CCMPA interrupt (n = 0 to 9)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRA register.

(2) GPTn_CCMPB interrupt (n = 0 to 9)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register

21.4 中断源

21.4.1 中断源

GPT提供以下中断源：

●GTCCR输入捕捉比较匹配

●GTCNT计数器上溢（GTPR比较匹配）下溢。

●周期计数功能完成

每个中断源都有自己的状态标志。当一个中断源信号产生时，相关的状态标志在GTST设置为1。GTST中相关的状态标志可以通过写入0来清除。如果标志设置和标志清除同时发生，标志清除优先于标志设置。这些标志由内部状态自动更新。中断控制器单元可以改变相关的通道优先级。但是，通道内的优先级是固定的。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

表21.46列出了GPT中断源。

Table 21.46 中断源

Channel	Name	中断源	中断标志	DTC activation
n = 0 to 3	GPTn_CCMPA	GPT32n.GTCCRA输入捕捉比较匹配	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT32n.GTCCRB输入捕捉比较匹配	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT32n.GTCCRC比较匹配	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT32n.GTCCRD比较匹配	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT32n.GTCCRE比较匹配	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT32n.GTCCRF比较匹配	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT32n.GTCNT溢出（GPT32m.GTPR比较匹配）	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT32n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_PC	周期计数功能完成(n=0 1)	GTST[31] (PCF)	Possible
n = 4 to 9	GPTn_CCMPA	GPT16n.GTCCRA输入捕捉比较匹配	GTST[0] (TCFA)	Possible
	GPTn_CCMPB	GPT16n.GTCCRB输入捕捉比较匹配	GTST[1] (TCFB)	Possible
	GPTn_CMPC	GPT16n.GTCCRC比较匹配	GTST[2] (TCFC)	Possible
	GPTn_CMPD	GPT16n.GTCCRD比较匹配	GTST[3] (TCFD)	Possible
	GPTn_CMPE	GPT16n.GTCCRE比较匹配	GTST[4] (TCFE)	Possible
	GPTn_CMPF	GPT16n.GTCCRF比较匹配	GTST[5] (TCFF)	Possible
	GPTn_OVF	GPT16n.GTCNT溢出（GPT320.GTPR比较匹配）	GTST[6] (TCFPO)	Possible
	GPTn_UDF	GPT16n.GTCNT underflow	GTST[7] (TCFPU)	Possible
	GPTn_PC	周期计数功能完成（n=4到6）	GTST[31] (PCF)	Possible

(1) GPTn_CCMPA中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRA寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRA寄存器匹配

●当GTCCRA寄存器用作输入捕捉寄存器时，输入捕捉信号导致GTCNT计数器值传送到GTCCRA寄存器。

(2) GPTn_CCMPB中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRB寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRB寄存器匹配

- When the GTCCRB register functions as an input capture register, the input-capture signal causes transfer of the GTCNT counter value to the GTCCRB register.

(3) GPTn_CMPC interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(4) GPTn_CMPD interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(5) GPTn_CMPE interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRE register functions as a compare match register, the GTCNT counter value matches with the GTCCRE register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register).

(6) GPTn_CMPF interrupt (n = 0 to 9)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value matches with the GTCCRF register.

A compare match is not performed and therefore, an interrupt is not requested in the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register).

(7) GPTn_OVF interrupt (n = 0 to 9)

An interrupt request is generated in the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (the GTCNT changes from GTPR to GTPR-1)

●当GTCCRB寄存器用作输入捕捉寄存器时，输入捕捉信号导致GTCNT计数器值传送到GTCCRB寄存器。

(3) GPTn_CMPC中断（n=0到9）

在以下情况下会产生中断请求：

●GTCCRC寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRC寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=01b 10b 11b（使用GTCCRC寄存器进行缓冲操作）。

(4) GPTn_CMPD中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRD寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRD寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRA[1:0]=10b 11b（使用GTCCRD寄存器进行缓冲操作）。

(5) GPTn_CMPE中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRE寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRE寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=01b 10b 11b（使用GTCCRE寄存器进行缓冲操作）。

(6) GPTn_CMPF中断（n=0到9）

在以下情况下会产生中断请求：

●当GTCCRF寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRF寄存器匹配。

不执行比较匹配，因此在以下情况下不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)

●GTBER.CCRB[1:0]=10b 11b（使用GTCCRF寄存器进行缓冲操作）。

(7) GPTn_OVF中断（n=0到9）

在以下情况下会产生中断请求：

●在锯齿波模式下，溢出时允许中断请求（在向上计数期间，当GTCNT计数器值从GTPR变为0时）

●在三角波模式下，在波峰处启用中断请求（GTCNT从GTPR变为GTPR-1）

- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(8) GPTn_UDF interrupt (n = 0 to 9)

An interrupt request is generated in the following conditions.

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (the GTCNT changes from 0 to 1)
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

About Interrupt signals and interrupt status flags, see section 21.2.16. GTST : General PWM Timer Status Register.

(9) GPTn_PC Interrupt (n = 0, 1, 4 to 6)

When the GTPC.PCEN bit is 1 and the GTPC.PCNT counter is 1, an interrupt request is generated at the end of cycle.

21.4.2 DMAC and DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 13, Interrupt Controller Unit (ICU), section 16, DMA Controller (DMAC), and section 17, Data Transfer Controller (DTC).

21.5 Operations Linked by ELC

21.5.1 Event Signal Output to ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the Event Link Controller (ELC).

The GPT has the following ELC event signals:

- Generation of compare match and input capture A interrupt (GPTn_CCMPA)
- Generation of compare match and input capture B interrupt (GPTn_CCMPB)
- Generation of compare match C interrupt (GPTn_CMPC)
- Generation of compare match D interrupt (GPTn_CMPD)
- Generation of compare match E interrupt (GPTn_CMPE)
- Generation of compare match F interrupt (GPTn_CMPF)
- Generation of overflow interrupt (GPTn_OVF)
- Generation of underflow interrupt (GPTn_UDF)
- Finish of period count function (GPTm_PC)

Note: n = 0 to 9
m = 0, 1, 4 to 6

21.5.2 Event Signal Inputs from ELC

The GPT can perform the following operations in response to a maximum of 8 events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down-counting
- Input capture.

See section 18, Event Link Controller (ELC) for the connection between the ELC and the event signal input.

21.6 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than 3 sampling cycles.

●在硬件源的计数中，发生了溢出（GTCNT在向上计数中从GTPR变为0）。

(8) GPTn_UDF中断（n=0到9）

在以下情况下会产生中断请求。

●在锯齿波模式下，下溢时允许中断请求（在向下计数期间，当GTCNT计数器值从0变为GTPR时）

●在三角波模式下，在波谷处启用中断请求（GTCNT由0变为1）

●在硬件源的计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

关于中断信号和中断状态标志，请参见第21.2.16节。GTST：通用PWM定时器状态寄存器。

(9) GPTn_PC中断（n=0、1、4到6）

当GTPC.PCEN位为1且GTPC.PCNT计数器为1时，在周期结束时产生中断请求。

21.4.2 DMAC和DTC激活

DMAC和DTC可以通过每个通道中的中断来激活。有关详细信息，请参见第13节，中断控制器单元(ICU)，第16节，DMA控制器(DMAC)，和第17节，数据传输控制器(DTC)。

21.5 由ELC链接的操作

21.5.1 事件信号输出到ELC

当GPT的中断请求信号被事件链接控制器(ELC)用作事件信号时，GPT可以执行与预先设置的另一个模块链接的操作。

GPT具有以下ELC事件信号：

●产生比较匹配和输入捕捉A中断(GPTn_CCMPA)
●产生比较匹配和输入捕捉B中断(GPTn_CCMPB)
●产生比较匹配C中断(GPTn_CMPC)
●产生比较匹配D中断(GPTn_CMPD)
●产生比较匹配E中断(GPTn_CMPE)
●产生比较匹配F中断(GPTn_CMPF)
●产生溢出中断（GPTn_OVF）
●产生下溢中断（GPTn_UDF）
●周期计数功能完成（GPTm_PC）

Note: n = 0 to 9
m = 0, 1, 4 to 6

21.5.2 来自ELC的事件信号输入

GPT可以执行以下操作以响应来自ELC的最多8个事件：

●开始计数、停止计数、清计数
- Up-counting, down-counting
●输入捕捉。

有关ELC和事件信号输入之间的连接，请参见第18节，事件链接控制器(ELC)。

21.6 噪音过滤功能

用于GPT的输入捕捉和霍尔传感器输入的每个引脚都配备了噪声滤波器。噪声滤波器以采样时钟对输入信号进行采样，并去除长度小于3个采样周期的脉冲。

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 21.63 shows the timing of noise filtering.

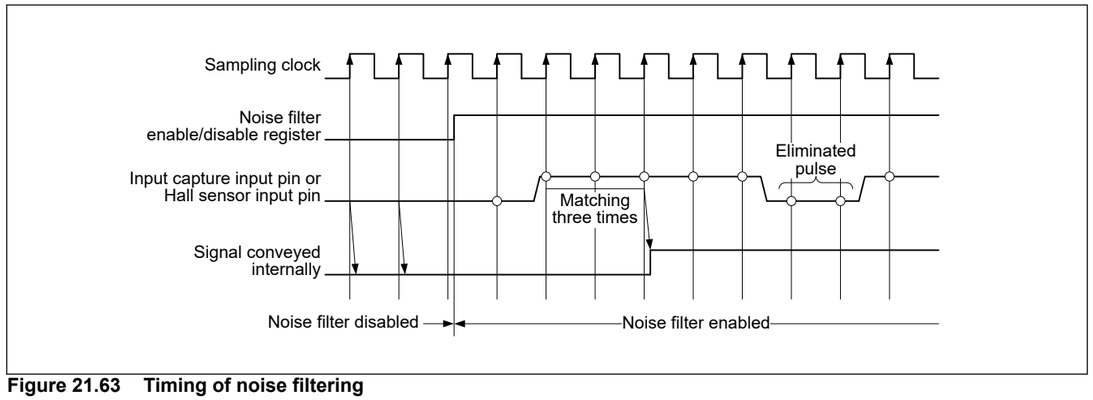


Figure 21.63 Timing of noise filtering

If noise filtering is enabled, the input capture operation or output phase switching operation is performed on the edges of the noise filtered signal after a delay of a sampling interval × 2 + PCLKD at the shortest. This is due to the noise filtering for the input capture input or hall sensor input.

21.7 Protection Function

21.7.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU, GTICLF, GTPC.

Every bit in registers GTSTR, GTSTP and GTCLR which can update the corresponding registers in other channels and can be updated by any of the corresponding registers in other channels conversely, can be protected by setting the GTWP.STRWP, STPWP, and CLRWP bits, respectively, per channel.

Likewise, writing to the GTSECSR and GTSECR registers, which can control all channels by writing to the GTSECSR and GTSECR registers of a given channel, can by enabled or disabled by the setting of the GTWP.CMNWP bit.

Protection using the GTWP register is only for write operations by the CPU. This protection does not cover updates to registers that occur in association with CPU writes.

21.7.2 Disabling of Buffer Operation

If the timing of the buffer register write is delayed relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD[1] and BD[0] bit settings. Specifically, buffer transfer can be temporarily disabled even though a buffer transfer condition is generated during buffer register write.

0 can be set simultaneously by setting the GTSECR register for multiple channels which were set by the GTSECSR register.

Figure 21.64 shows an example of operation for disabling buffer operation.

噪声过滤器功能包括为每个引脚启用和禁用噪声过滤器以及为每个通道设置采样时钟。

图21.63显示了噪声过滤的时序。

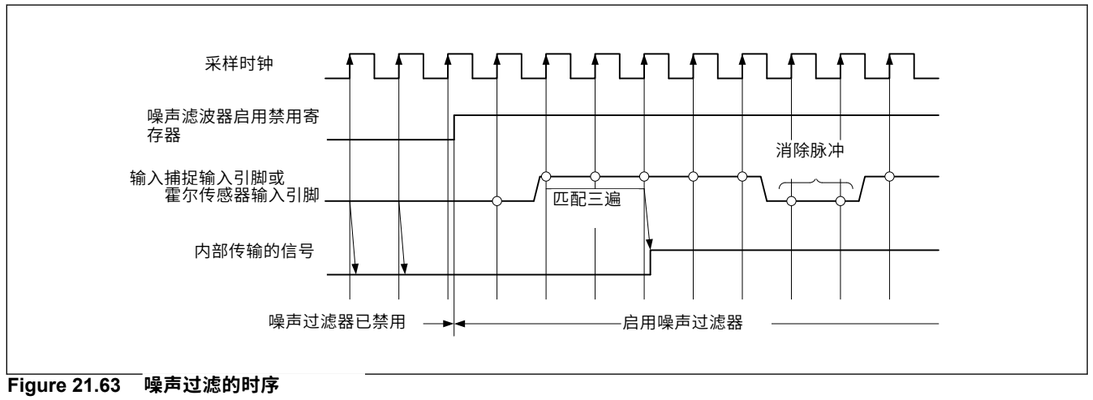


Figure 21.63 噪声过滤的时序

如果噪声过滤使能，输入捕捉操作或输出相位切换操作在最短采样间隔×2+PCLKD的延迟后对噪声过滤信号的边沿执行。这是由于输入捕捉输入或霍尔传感器输入的噪声过滤。

21.7 保护功能

21.7.1 寄存器的写保护

为了防止寄存器被意外修改，可以通过设置以通道为单位对寄存器进行写保护
GTWP.WP。可以为以下寄存器设置写保护：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTDTCR, GTDVU, GTICLF, GTPC.

寄存器GTSTR、GTSTP和GTCLR中的每个位可以更新其他通道中的相应寄存器，反之也可以由其他通道中的任何相应寄存器更新，可以分别通过设置GTWP.STRWP、STPWP和CLRWP位来保护 每个频道。

同样，写入GTSECSR和GTSECR寄存器，它们可以通过写入GTSECSR和
给定通道的GTSECR寄存器可以通过设置GTWP.CMNWP位来启用或禁用。

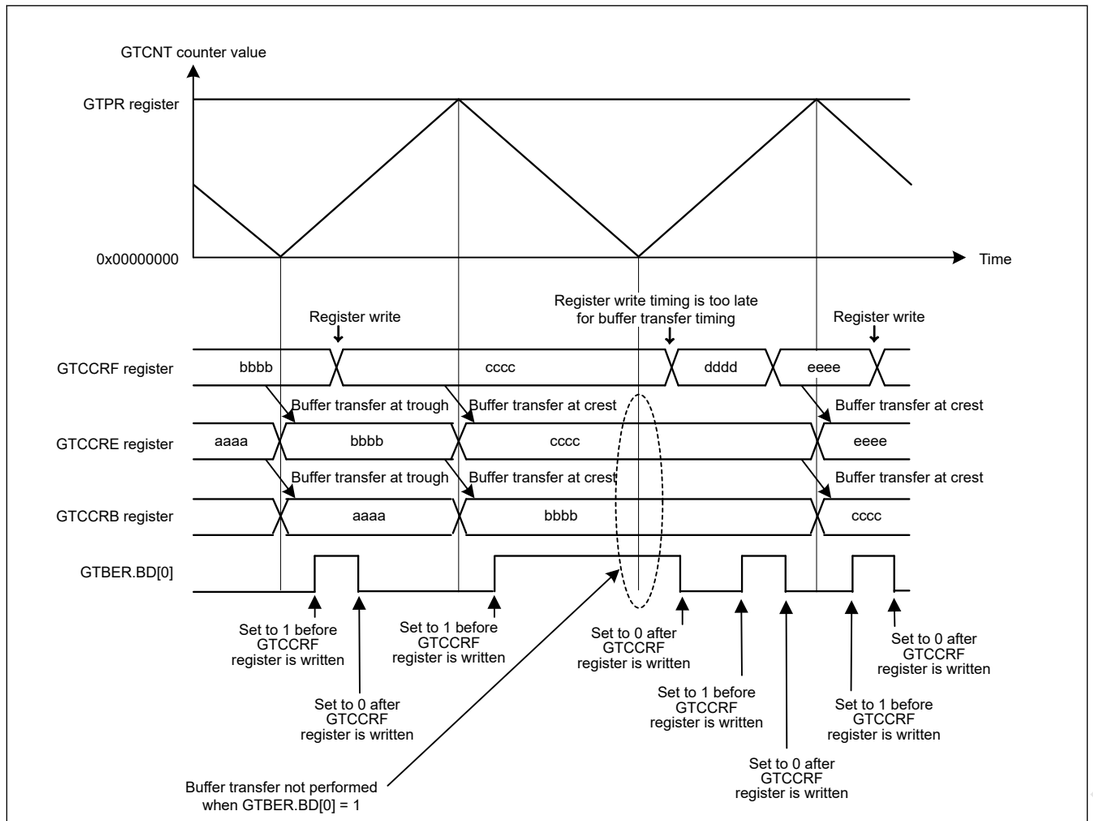
使用GTWP寄存器的保护仅适用于CPU的写操作。此保护不涵盖与CPU写入相关的寄存器更新。

21.7.2 禁用缓冲区操作

如果缓冲寄存器写入的时序相对于缓冲传输的时序延迟，则可以通过GTBER.BD[1]和BD[0]位设置暂停缓冲操作。具体来说，即使在缓冲寄存器写入期间产生了缓冲传送条件，也可以暂时禁用缓冲传送。

0可以通过设置GTSECSR寄存器为由GTSECSR寄存器设置的多个通道同时设置。

图21.64显示了禁用缓冲区操作的操作示例。



Note: The base address of registers are the same.

Figure 21.64 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

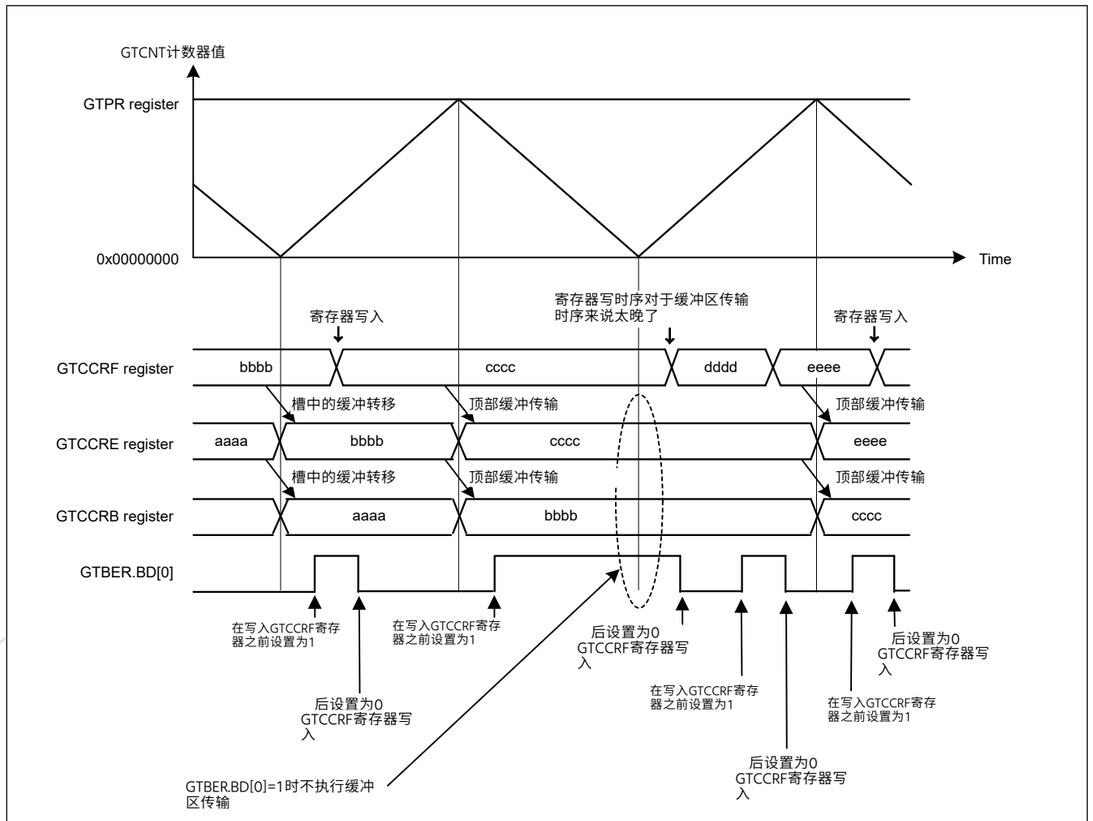
21.7.2.1 Simultaneous Control of Buffer Operations of Multiple Channels

The GTBER.BD bit can be set by writing directly to the GTBER register per channel or by making settings in the GTSECR register for multiple channels that have already set in the GTSECSR register.

Follow the procedure below to simultaneously set the GTBER.BD bits of multiple channels.

1. Select the channels for simultaneously setting by the GTSECSR register
   Set the GTSECSR register so that the values at the bit positions for the corresponding channels for simultaneously setting of the GTBER.BD bits become 1. All GTSECSR registers can be updated by writing to the GTSECSR register of any channel.
2. Simultaneously set the GTBER.BD bits by updating the GTSECR register
   In the GTSECR register, set the operation of the GTBER.BD bits (enabling or disabling of buffer operation) which are to be simultaneously set. Writing to a GTSECR register from any channel updates the GTBER.BD bits in all channels corresponding to the bits set as 1 in the GTSECSR register, in accordance with the value of the GTSECR register.

Figure 21.65 show examples of simultaneously controlling the enabling or disabling of buffer operation for multiple channels.



Note: 寄存器的基地址相同。

Figure 21.64 三角波缓冲操作、双缓冲操作、波谷和波峰缓冲转移的禁用操作示例

21.7.2.1 多通道缓冲操作的同时控制

GTBER.BD位可以通过直接写入每个通道的GTBER寄存器或通过在GTSECR寄存器中为已在GTSECSR寄存器中设置的多个通道进行设置来设置。

按照以下步骤同时设置多个通道的GTBER.BD位。

1.通过GTSECSR寄存器选择同时设置的通道
设置GTSECSR寄存器，使用于同时设置GTBER.BD位的相应通道的位位置的值变为1。通过写入任何通道的GTSECSR寄存器，可以更新所有GTSECSR寄存器。

2.通过更新GTSECR寄存器同时设置GTBER.BD位
在GTSECR寄存器中，设置要同时设置的GTBER.BD位的操作（启用或禁用缓冲区操作）。根据GTSECR寄存器的值，从任何通道写入GTSECR寄存器会更新与GTSECSR寄存器中设置为1的位相对应的所有通道中的GTBER.BD位。

图21.65显示了同时控制多个通道的缓冲区操作的启用或禁用的示例。

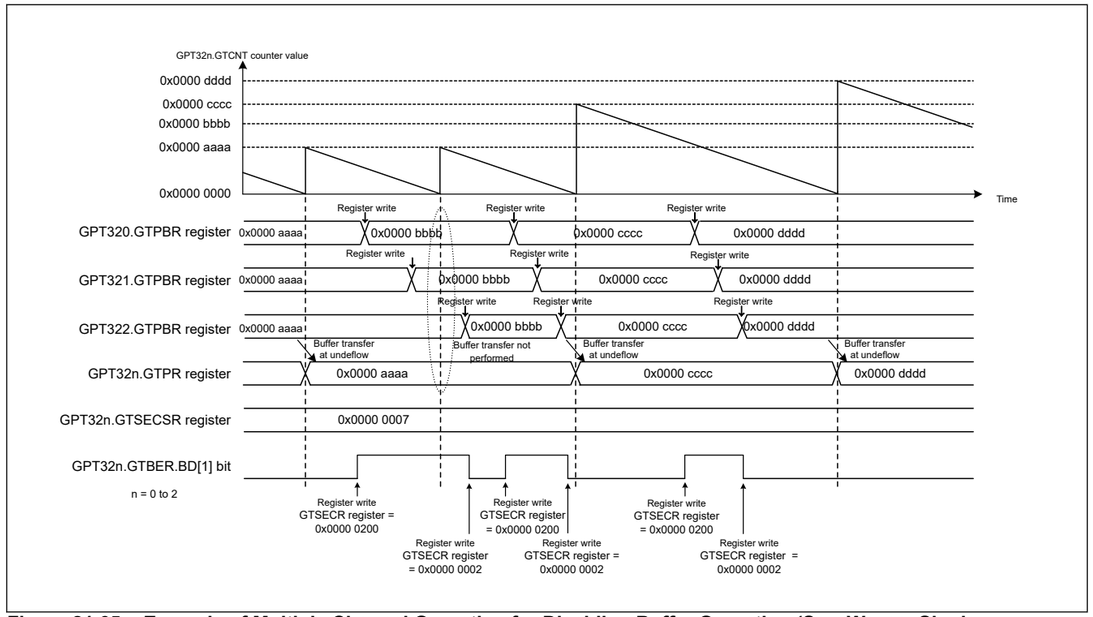


Figure 21.65 Example of Multiple Channel Operation for Disabling Buffer Operation (Saw Waves, Single Buffer Operation)

21.7.3 GTIOCnm Pin Output Negate Control (n = 0 to 9, m = A, B)

For protection from system failure, the output disable control that changes the GTIOCnm pin output value forcibly is provided for GTIOCnm pin output by the request of output disable from POEG. Output protection is required when the same output level being on the GTIOCnA and GTIOCnB pins is detected. GPT detects this condition and generates output disable requests to POEG according to the setting of the output disable request permission bits, such as GTINTAD.GRPABH, GTINTAD.GRPABL. After the POEG receives output disable requests from each channel and calculates external input using an OR operation, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCnA pin and the GTIOCnB pin) out of 4 output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is set based on the GTIOR.OADF[1:0] bits for the GTIOCnA pin and the GTIOR.OBDF[1:0] setting for the GTIOCnB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request.

When event count is performed or when the output disable state should be released immediately without waiting for end of cycle, GTIOR.OADF[1:0] should be set to 00b (for GTIOCnA pin) or GTIOR.OBDF[1:0] should be set to 00b (for the GTIOCnB pin).

Figure 21.66 shows an example of the GTIOCnm pin output disable control operation.（n = 0 to 9, m = A, B）

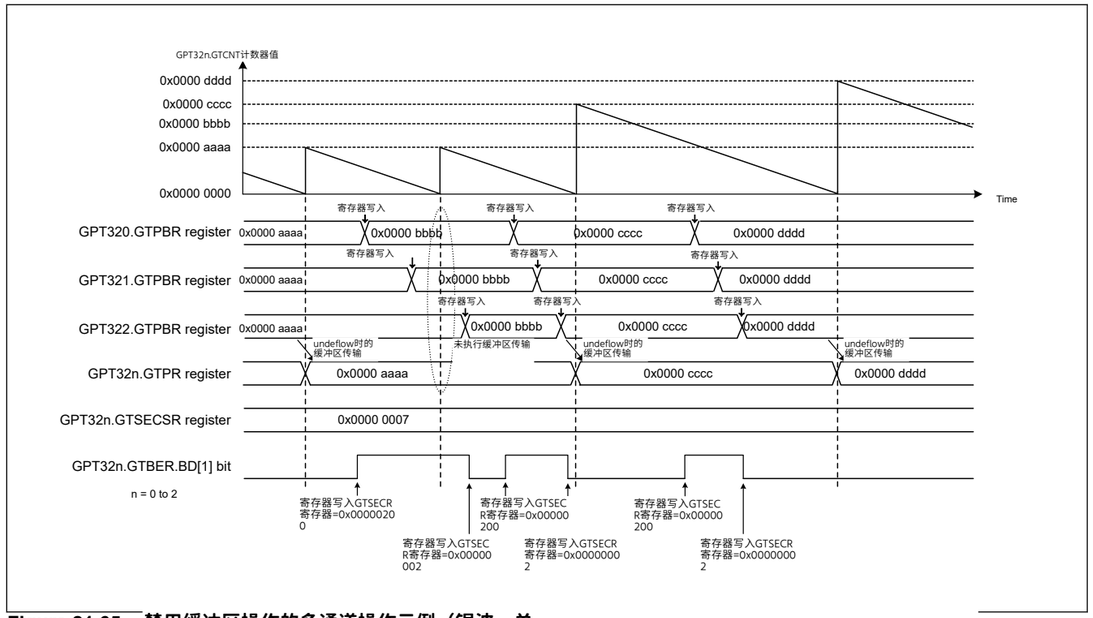


Figure 21.65 禁用缓冲区操作的多通道操作示例（锯波，单Buffer Operation)

21.7.3 GTIOCnm引脚输出负控制（n=0到9，m=A，B）

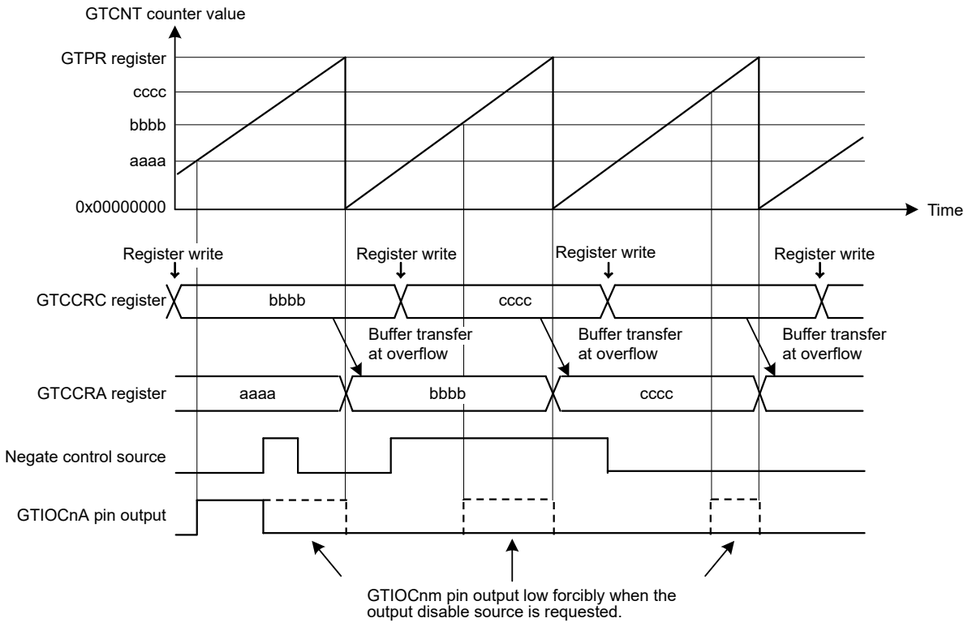
为防止系统故障，根据POEG的输出禁用请求，为GTIOCnm引脚输出提供强制改变GTIOCnm引脚输出值的输出禁用控制。当检测到GTIOCnA和GTIOCnB引脚上的输出电平相同时，需要输出保护。GPT检测到这种情况并根据输出禁用请求许可位的设置，如GTINTAD.GRPABH、GTINTAD.GRPABL向POEG生成输出禁用请求。在POEG接收到来自每个通道的输出禁用请求并使用OR运算计算外部输入后，POEG向GPT生成输出禁用请求。

通过设置GTINTAD.GRP[1:0]，在POEG产生的4个输出禁止请求中选择一个输出禁止信号（代表GTIOCnA引脚和GTIOCnB引脚的共享输出禁止请求信号）。通过读取GTST.ODF位来监控所选禁用输出请求的状态。输出禁用期间的输出电平根据GTIOCnA引脚的GTIOR.OADF[1:0]位和GTIOCnB引脚的GTIOR.OBDF[1:0]设置来设置。

通过从POEG生成输出禁用请求异步执行对输出禁用状态的更改。通过终止输出禁用请求，在循环结束时执行输出禁用状态的释放。

当执行事件计数或应立即释放输出禁用状态而不等待周期结束时，应将GTIOR.OADF[1:0]设置为00b（对于GTIOCnA引脚）或GTIOR.OBDF[1:0]应设置为设置为00b（对于GTIOCnB引脚）。

图21.66显示了GTIOCnm引脚输出禁用控制操作的示例。（n=0到9，m=A，B）



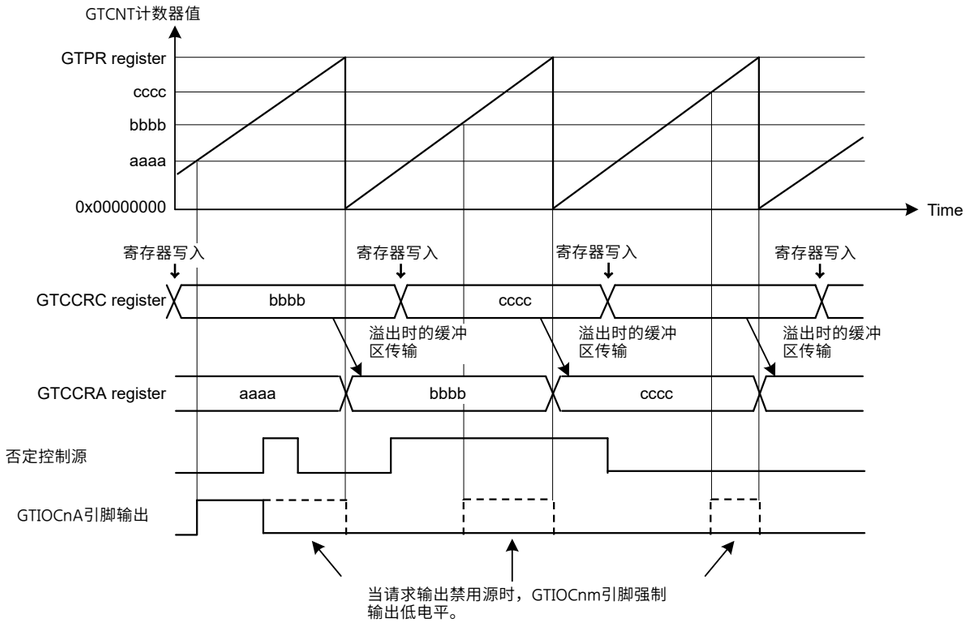
Note: The base address of registers are the same.

Figure 21.66 Example of GTIOCnm pin output disable control operation in saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable (n = 0 to 9, m = A, B)

21.8 Initialization Method of Output Pins

21.8.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.



Note: 寄存器的基地址相同。

Figure 21.66 GTIOCnm引脚输出禁用控制操作示例在锯齿波递增计数、缓冲器操作、有效电平1、GTCCRA比较匹配时的高输出、周期结束时的低输出和输出禁用时的低输出（n=0到9，m=A B）

21.8 输出管脚的初始化方法

21.8.1 复位后的引脚设置

GPT寄存器在复位时被初始化。通过PmnPFS寄存器选择端口引脚功能，设置GTIOR.OAE和GTIOR.OBE位，并将GPT功能输出到外部引脚后开始计数。

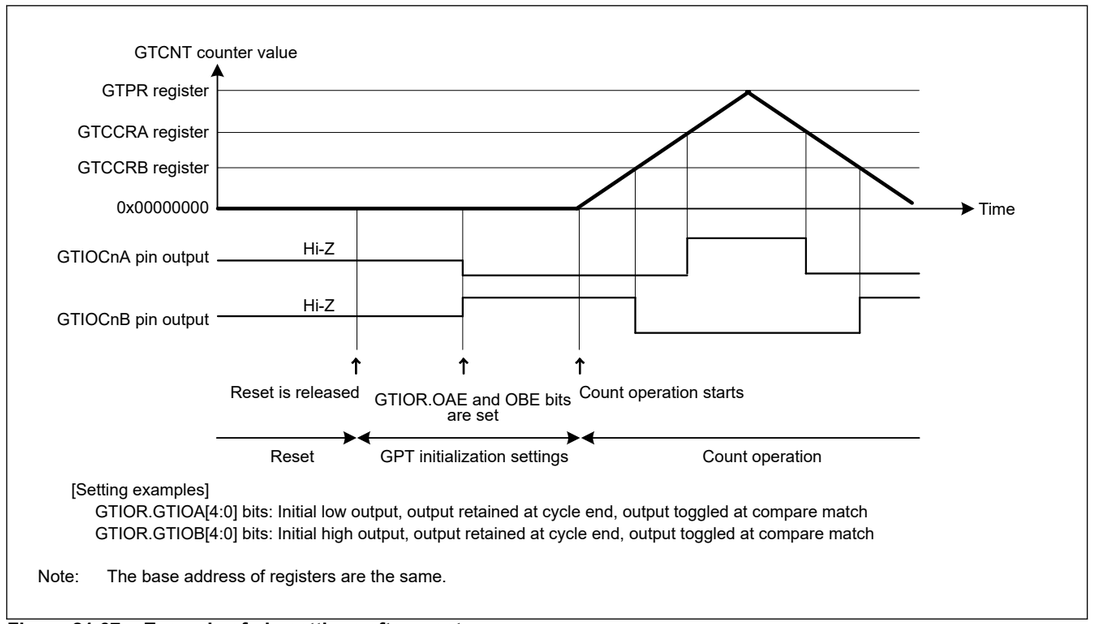


Figure 21.67 Example of pin settings after reset

21.8.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR registers and PmnPFS.PMR bit of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0, and the control bit associated with the pin in the PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

If the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting is resumed, operation continues from where it stopped. If counting is stopped, the registers must be initialized before counting starts.

21.9 Usage Notes

21.9.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

21.9.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy all of the following conditions:

- GTDVU < GTCCRA
- 0 < GTCCRA < GTPR

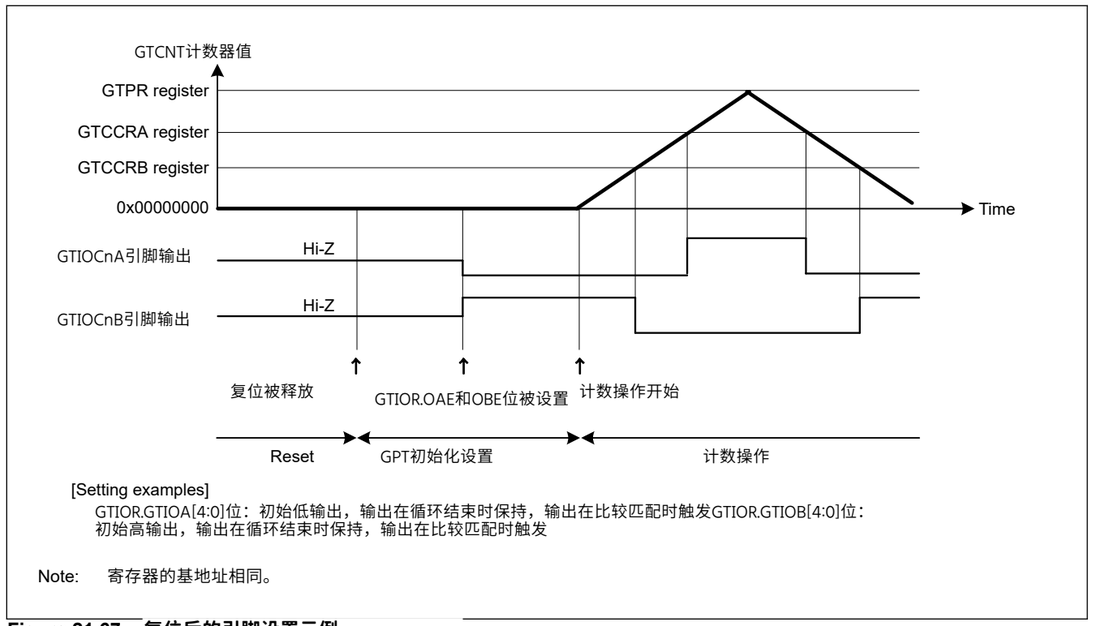


Figure 21.67 复位后的引脚设置示例

21.8.2 由于操作过程中的错误而导致的引脚初始化

如果在GPT操作过程中发生错误，可以在引脚初始化之前进行以下四种引脚处理：

●将GTIOR中的OAHLD和OBHLD位设置为1，并在计数停止时保留输出

●将GTIOR中的OAHLD和OBHLD位设置为0，在GTIOR中的OADFLT和OBDFLT指定任意输出值，并在计数停止时输出任意值

●通过预先设置IO端口的PDR、PODR寄存器和PmnPFS.PMR位，将引脚设置为输出任意值作为通用输出端口。将GTIOR中的OAE和OBE位设置为0，并将与PMR中的引脚相关的控制位设置为0，以允许在发生错误时从设置为通用输出端口的引脚输出任意值。

●使用POEG功能将输出驱动为高阻抗状态。

如果进行了自动死区时间设置，则在计数停止后将GTDTCR.TDE位清零。当计数停止时，只有被GPT外部源改变的寄存器的值会改变。如果重新开始计数，则从停止处继续操作。如果停止计数，则必须在计数开始前初始化寄存器。

21.9 使用说明

21.9.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用GPT操作。GPT在重置后最初停止。
释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

21.9.2 比较匹配操作期间的GTCCRn设置（n=A到F）

(1) 在三角波PWM模式下进行自动死区时间设置时

GTCCRA寄存器必须满足以下所有条件：

- GTDVU < GTCCRA
- 0 < GTCCRA < GTPR

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB is 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, the correct output waveforms with secured dead time may not be obtained.

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVU

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF must be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

21.9.3 Setting Range for GTCNT Counter

The GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

21.9.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[3:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock that is selected in GTCR.TPCS[3:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored, resulting in situations in which an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

21.9.5 Priority Order of Each Event

(1) GTCNT register

Table 21.47 shows a priority order of events updating the GTCNT register.

(2) 在三角波PWM模式下未进行自动死区时间设置时

GTCCRA寄存器必须设置在0<GTCCRA<GTPR的范围内。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。当GTCCRA>GTPR时，不发生比较匹配。

同样，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当GTCCRB为0或GTCCRB=GTPR满足时，才会在周期内发生比较匹配。当GTCCRB>GTPR时，不发生比较匹配。

(3) 在锯波单发脉冲模式下进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足这些限制，则可能无法获得具有安全死区时间的正确输出波形。

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVU

(4) 在锯波单发脉冲模式下未进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0

同样，必须设置GTCCRE和GTCCRF以满足以下限制。如果不满足限制，则不会发生两个比较匹配，并且无法执行脉冲输出。

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) 在锯齿波PWM模式下

GTCCRA寄存器必须设置为0<GTCCRA<GTPR。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRA>GTPR，则不会发生比较匹配。

类似地，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRB>GTPR，则不会发生比较匹配。

21.9.3 GTCNT计数器的设置范围

GTCNT计数器寄存器的设置范围必须为0≤GTCNT≤GTPR。

21.9.4 启动和停止GTCNT计数器

通过GTCR.CST位启动和停止GTCNT计数器的控制时序与在GTCR.TPCS[3:0]中选择的计数时钟同步。当GTCR.CST更新时，GTCNT计数器在GTCR.TPCS[3:0]中选择的计数时钟后开始停止。因此，在GTCNT计数器实际启动之前产生的事件将被忽略，从而导致在GTCR.CST设置为0之后接受事件或发生中断的情况。

21.9.5 每个事件的优先顺序

(1) GTCNT register

表21.47显示了更新GTCNT寄存器的事件的优先顺序。

Table 21.47 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (writing to GTCNT/GTCLR)	High
Clear by hardware sources set in GTCSR	↑
Count up or down by hardware sources set in GTUPSR/GTDNSR	↑
Count operation	Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change. When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), the writing by CPU has priority over the starting/stopping by hardware sources.

In case that stop by the period count function conflicts with start by the CPU writing (GTCR register writing/GTSTR register writing), the period count function is finished with setting the GTST.PCF flag. The CST bit is not changed and the GTCNT continues to count.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. When there is a conflict between updating the GTCR.CST bit and reading by the CPU (reading from GTCR/GTSTR/GTSTP registers), pre-update data is read.

(3) GTCCRm registers (m = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to the GTCCRm registers, the writing to GTCCRm registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. When there is a conflict between updating the GTCCRm registers and reading by the CPU, pre-update data is read.

(4) GTPR registers

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

Table 21.47 更新GTCNT的源的优先顺序

源更新GTCNT	优先顺序
CPU写入（写入GTCNTGTCLR）	High
由GTCSR中设置的硬件源清除	↑
通过GTUPSRGTDNSR中设置的硬件源进行向上或向下计数	↑
计数操作	Low

如果硬件源的递增计数和递减计数同时发生，GTCNT计数器值不会改变。
当更新GTCNT寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(2) GTCR.CST bit

当GTSSRGTPSR寄存器中设置的硬件源启动停止与CPU写入（写入GTCRGTSTRGTSTP寄存器）发生冲突时，CPU写入优先于硬件源启动停止。

如果周期计数功能停止与CPU写入启动（GTCR寄存器写入GTSTR寄存器写入）发生冲突，则周期计数功能通过设置GTST.PCF标志结束。CST位不变，GTCNT继续计数。

当GTSSR寄存器中设置的硬件源启动和GTPSR寄存器中设置的硬件源停止之间存在冲突时，GTCR.CST位的值不会改变。当更新GTCR.CST位与CPU读取（从GTCRGTSTRGTSTP寄存器读取）之间存在冲突时，将读取更新前数据。

(3) GTCCRm寄存器（m=A到F）

当输入捕捉缓冲区传输操作与写入GTCCRm寄存器之间存在冲突时，写入GTCCRm寄存器优先于输入捕捉缓冲区传输操作。当输入捕获与CPU写入计数器寄存器或硬件源更新计数器寄存器之间存在冲突时，将捕获更新前的计数器值。当更新GTCCRm寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(4) GTPR registers

当缓冲区传输操作与写入GTPR寄存器之间存在冲突时，写入GTPR寄存器优先于缓冲区传输操作。当更新GTPR寄存器与CPU读取发生冲突时，读取更新前的数据。

22. Low Power Asynchronous General Purpose Timer (AGT)

22.1 Overview

The low power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 22.1 lists the AGT specifications, Figure 22.1 shows a block diagram, and Table 22.2 lists the I/O pins.

Table 22.1 AGT specifications

Parameter		Description
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Number of Channels		16 bits × 6 channels (AGTn (n = 0 to 5))
Count source (operating clock)*2	Timer mode	PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d, AGTSCLK/d (d = 1, 2, 4, 8, 16, 32, 64, or 128), or underflow signal of AGTn (n = 0, 2, 4) selectable.*1
	Pulse output mode	
	Pulse width measurement mode	
	Pulse period measurement mode	
	Event counting mode	External event input
Interrupt and Event Link function		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input pin (AGTIOn) completes in pulse width measurement mode – When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode. • Compare match A event signal – When the values of AGT register and AGTCMA register matched (compare match A function enabled). • Compare match B event signal – When the values of AGT regsiter and AGTCMB register matched (compare match B function enabled). • Return from Snooze mode or Software Standby mode can be performed with AGTn_AGTI, AGTn_AGTCMAI, or AGTn_AGTCMBI (n = 1, 3)*3
Selectable functions		• Compare match function One or two of the AGT Compare Match A register and AGT Compare Match B register is selectable.
TrustZone Filter		Security attribution can be set for each channels

Note 1. AGTn (n = 0, 2, 4) cannot use underflow signal. AGTn (n = 1, 3, 5) connects directly with the underflow event signal from the AGTn (n = 0, 2, 4) timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.
Note 3. In details, see section 10, Low Power Modes.

22. 低功耗异步通用定时器(AGT)

22.1 Overview

低功耗异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。该定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。

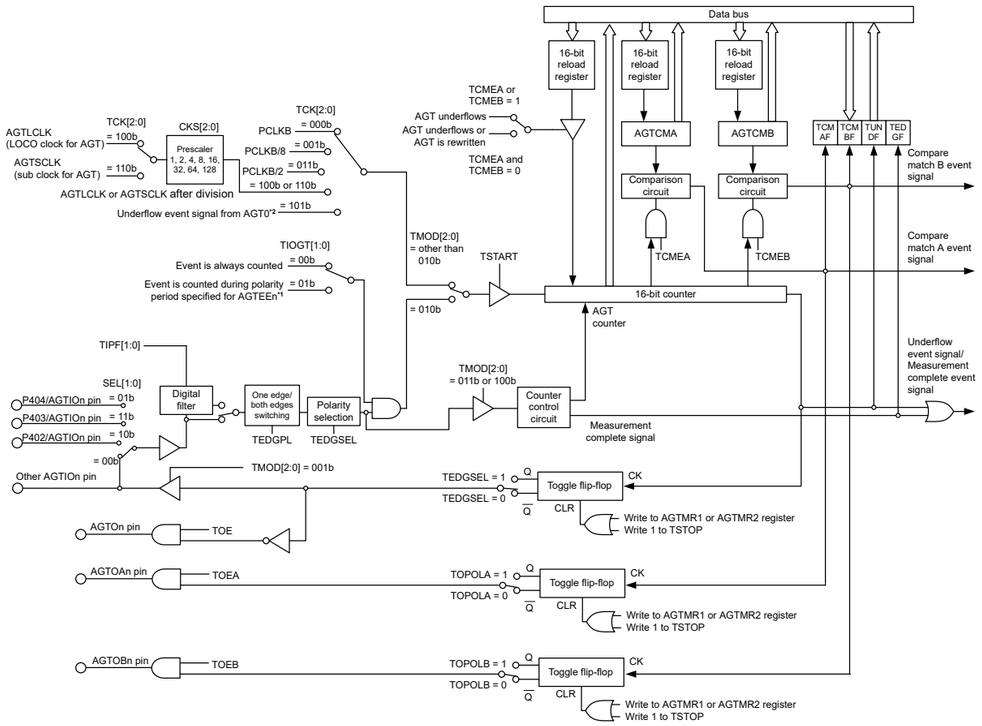
表22.1列出了AGT规格，图22.1显示了框图，表22.2列出了IO引脚。

Table 22.1 AGT specifications

Parameter		Description
操作模式	定时器模式	计数源被计数
	脉冲输出方式	计数源被计数并在每次定时器下溢时反转输出
	事件计数器模式	计算外部事件
	脉宽测量模式	测量外部脉冲宽度
	脉冲周期测量模式	测量外部脉冲周　　期
通道数		16位×6通道(AGTn(n=0到5))
计数源（工作时钟）*2	定时器模式	PCLKB、PCLKB2、PCLKB8、AGTLCLKd、AGTSCLKd（d=1、2、4、8、16、32、64或128）或AGTn的下溢信号（n=0、2、4）可选。*1
	脉冲输出方式	
	脉宽测量模式	
	脉冲周期测量模式	
	事件计数模式	外部事件输入
中断和事件链接功能		• 下溢事件信号或测量完成事件信号 – 当计数器下溢时 – 在脉冲宽度测量模式下，外部输入引脚(AGTIOn)的有效宽度测量完成时 – 在脉冲周期测量模式下输入外部输入引脚(AGTIOn)的设置边沿时。 • 比较匹配A事件信号 – 当AGT寄存器和AGTCMA寄存器的值匹配时（比较匹配A功能启用）。 • 比较匹配B事件信号 – 当AGT寄存器和AGTCMB寄存器的值匹配时（比较匹配B功能启用）。 • 从贪睡模式或软件待机模式返回可以通过 AGTn_AGTI, AGTn_AGTCMAI, or AGTn_AGTCMBI (n = 1, 3)*3
可选择的功能		• 比较匹配功能AGT比较匹配A寄存器和AGT比较匹配中的一个或两个 B寄存器是可选的。
TrustZone Filter		可以为每个通道设置安全属性

注1.AGTn(n=0 2 4)不能使用下溢信号。AGTn(n=1 3 5)直接连接来自AGTn(n=0 2 4)定时器的下溢事件信号。

注2.满足外设模块时钟（PCLKB）的频率≥计数源时钟的频率。
注3.详细信息请参见第10节，低功耗模式。



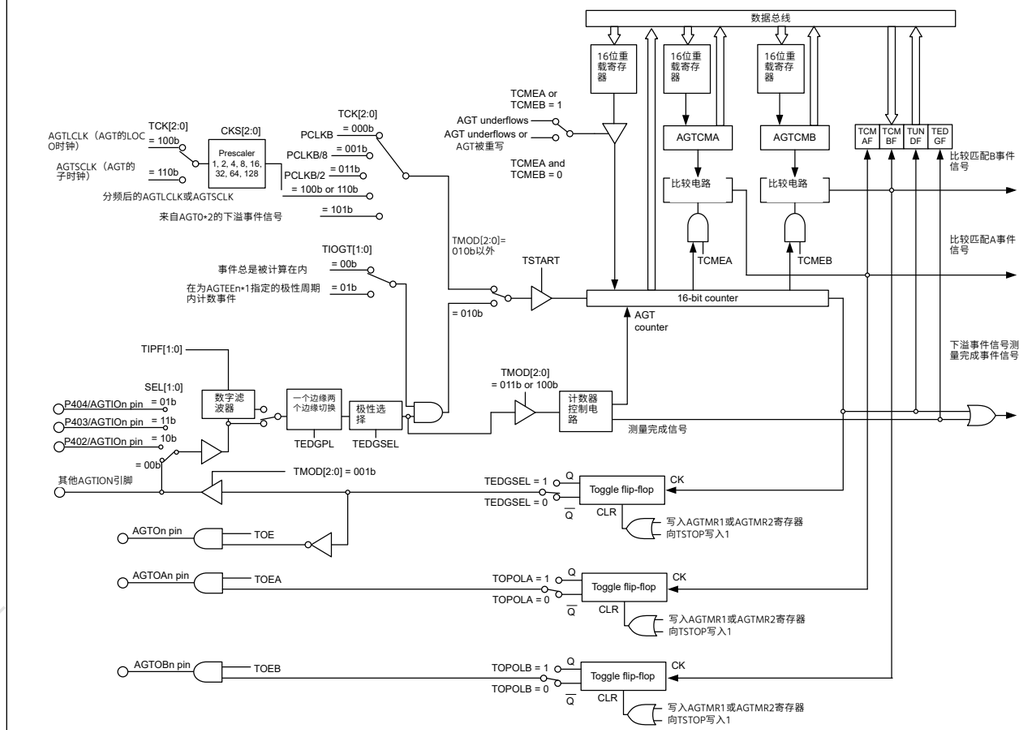
Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGTn (n = 0, 2, 4) cannot use AGTn (n = 0, 2, 4) underflow event. AGTn (n = 1, 3, 5) uses the underflow of AGTn (n = 0, 2, 4).

Figure 22.1 AGT block diagram

Table 22.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input enable for AGT
AGTIOn	Input/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOAn	Output	Compare match A output for AGT
AGTOBn	Output	Compare match B output for AGT

Note: Channel number: n = 0 to 5
Note: P402, P403, P404 can only be used as input.



注1.可以通过AGTISR寄存器中的EEPS位选择极性。
注2.AGTn(n=0 2 4)不能使用AGTn(n=0 2 4)下溢事件。AGTn(n=1 3 5)使用AGTn(n=0 2 4)的下溢。

Figure 22.1 AGT框图

Table 22.2 AGT I/O pins

引脚名称	I/O	Function
AGTEEn	Input	AGT的外部事件输入使能
AGTIOn	Input/output	AGT的外部事件输入和脉冲输出
AGTOn	Output	AGT的脉冲输出
AGTOAn	Output	比较AGT的匹配A输出
AGTOBn	Output	比较AGT的匹配B输出

Note: 通道号：n=0到5
Note: P402、P403、P404只能用作输入。

RA生态工作室

22.2 Register Descriptions

22.2.1 AGT : AGT Counter Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16-bit counter and reload register Setting range : 0x0000 to 0xFFFF	R/W

AGTn.AGT is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 22.3.1. Reload Register and Counter Rewrite Operation.

When 1 is written to the TSTOP bit in the AGTCR register, AGT counter is forcibly stopped and set to 0xFFFF.

When the TCK[2:0] bits setting in the AGTMR1 register are a value other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0x0000, a request signal to the ICU, the DTC, the DMAC, and the ELC is generated once immediately after the count starts. The AGTOn, AGTIOn pin output are toggled.

When the AGT register is set to 0x0000 in event counter mode, regardless of the value of TCK[2:0] bits, a request signal to the ICU, the DTC, the DMAC, and the ELC is generated once immediately after the count starts.

In addition, the AGTOn pin output is toggled even during a period other than the specified count period. When the AGT register is set to 0x0001 or more, a request signal is generated each time AGT underflows.

22.2.2 AGTCMA : AGT Compare Match A Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16-bit compare match A data is stored.*1 Setting range : 0x0000 to 0xFFFF	R/W

Note 1. Set the AGTCMA register to 0xFFFF when compare match A is not used.

The **AGTCMA** register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 22.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

22.2 注册说明

22.2.1 AGT:AGT计数器寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16位计数器和重载寄存器设置范 围：0x0000到0xFFFF	R/W

AGTn.AGT是一个16位寄存器。写入值写入重载寄存器，读取值从计数器中读取。

重载寄存器和计数器的状态根据AGTCR寄存器和TCMEA中的TSTART位改变
AGTCMSR寄存器中的TCMEB位。详见22.3.1节。重载寄存器和计数器重写操作。

当AGTCR寄存器的TSTOP位写入1时，AGT计数器被强制停止并设置为0xFFFF。

当AGTMR1寄存器中的TCK[2:0]位设置为001b(PCLKB8)或011b(PCLKB2)以外的值时，如果
AGT寄存器设置为0x0000，在计数开始后立即生成一次对ICU、DTC、DMAC和ELC的请求信号。AGTO
n、AGTIOn引脚输出被切换。

当AGT寄存器在事件计数器模式下设置为0x0000时，无论TCK[2:0]位的值如何，都会在计数开始后立即生成一次对ICU、DTC、DMAC和ELC的请求信号.

此外，即使在指定计数周期以外的周期内，AGTOn引脚输出也会切换。当AGT寄存器设置为0x0001或更大时，每次AGT下溢时都会产生一个请求信号。

22.2.2 AGTCMA:AGT比较匹配A寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16位比较匹配A数据被存储。*1 设置范围：0x0000到0xFFFF	R/W

注1.不使用比较匹配A时，将AGTCMA寄存器设置为0xFFFF。

AGTCMA寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器A的状态根据AGTCR寄存器中的TSTART位而改变。详见22.3.2节。重载寄存器和AGT比较匹配AB寄存器重写操作。

22.2.3 AGTCMB : AGT Compare Match B Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	16-bit compare match B data is stored.*1 Setting range : 0x0000 to 0xFFFF	R/W

Note 1. Set the AGTCMB register to 0xFFFF when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change according to the TSTART bit in the AGTCR register. For details, see section 22.3.2. Reload Register and AGT Compare Match A/B Register Rewrite Operation.

22.2.4 AGTCR : AGT Control Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT Count Start*2 0: Count stops 1: Count starts	R/W
1	TCSTF	AGT Count Status Flag*2 0: Count stopped 1: Count in progress	R
2	TSTOP	AGT Count Forced Stop*1 0: Writing is invalid 1: The count is forcibly stopped	W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TEDGF	Active Edge Judgment Flag 0: No active edge received 1: Active edge received	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	Compare Match A Flag 0: No match 1: Match	R/(W)*3
7	TCMBF	Compare Match B Flag 0: No match 1: Match	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART bit and TCSTF flag are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART bit and TCSTF flag, see section 22.4.1. Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

22.2.3 AGTCMB:AGT比较匹配B寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
15:0	n/a	存储16位比较匹配B数据。*1 设置范围：0x0000到0xFFFF	R/W

注1.不使用比较匹配B时，将AGTCMB寄存器设置为0xFFFF。

AGTCMB寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器B的状态根据AGTCR寄存器中的TSTART位而改变。详见22.3.2节。重载寄存器和AGT比较匹配AB寄存器重写操作。

22.2.4 AGTCR:AGT控制寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTART	AGT计数开始*2 0：计数停止1 ：计数开始	R/W
1	TCSTF	AGT计数状态标志*2 0：计数停止1：计数中	R
2	TSTOP	AGTCount强制停止*1 0：写入无效1：强制停止计数	W
3	—	该位读取为0。写入值应为0。	R/W
4	TEDGF	主动边缘判断标志 0：未收到有效边沿1：收到有效边沿	R/(W)*3
5	TUNDF	Underflow Flag 0: No underflow 1: Underflow	R/(W)*3
6	TCMAF	比较匹配标志 0：不匹配1 ：匹配	R/(W)*3
7	TCMBF	比较匹配B标志 0：不匹配1 ：匹配	R/(W)*3

注1.当1（强制停止计数）写入TSTOP位时，TSTART位和TCSTF标志同时初始化。脉冲输出电平也被初始化。读取值为0。

注2.有关使用TSTART位和TCSTF标志的信息，请参阅第22.4.1节。计数操作启动和停止控制。
注3.只能写入0来清除标志。

TSTART bit (AGT Count Start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF flag is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF flag is set to 0 (count stops) in synchronization with the count source. For details, see section 22.4.1. Count Operation Start and Stop Control.

TCSTF flag (AGT Count Status Flag)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT Count Forced Stop)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

TEDGF flag (Active Edge Judgment Flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input pin (AGTIOn) is complete in pulse width measurement mode
- When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode.

[Clearing condition]

- When 0 is written to this flag by software.

TUNDF flag (Underflow Flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare Match A Flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare Match B Flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

TSTART位（AGT计数开始）

通过向TSTART位写入1开始计数操作，通过写入0停止计数操作。当TSTART位设置为1（计数开始）时，TCSTF标志设置为1（计数进行中）与计数源同步。此外，在TSTART位写入0后，TCSTF标志与计数源同步设置为0（计数停止）。详见22.4.1节。计数操作启动和停止控制。

TCSTF标志（AGT计数状态标志）

TCSTF标志指示AGT计数状态。

[Setting condition]

●当TSTART位写入1时（TCSTF标志设置为1，与计数源同步）。

[Clearing conditions]

●TSTART位写入0时（TCSTF标志设置为0与计数源同步）

●TSTOP位写入1时。

TSTOP位（AGT计数强制停止）

向TSTOP位写入1时，强制停止计数。读取值为0。

TEDGF标志（活动边缘判断标志）

TEDGF标志表示检测到有效边沿。

[Setting condition]

●在脉冲宽度测量模式下，外部输入引脚(AGTIOn)的有效宽度测量完成时

●在脉冲周期测量模式下输入外部输入引脚(AGTIOn)的设置边沿时。

[Clearing condition]

●当软件向该标志写入0时。

TUNDF flag (Underflow Flag)

TUNDF标志指示计数器下溢。

[Setting condition]

●当计数器下溢时。

[Clearing condition]

●当软件向该标志写入0时。

TCMAF标志（比较匹配A标志）

TCMAF标志表示检测到比较匹配A。

[Setting condition]

●当AGT寄存器中的值与AGTCMA寄存器中的值匹配时。

[Clearing condition]

●当软件向该标志写入0时。

TCMBF标志（比较匹配B标志）

TCMBF标志表示检测到比较匹配B。

[Setting condition]

●当AGT寄存器中的值与AGTCMB寄存器中的值匹配时。

[Clearing condition]

●当软件向该标志写入0时。

22.2.5 AGTMR1 : AGT Mode Register 1

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	Operating Mode*3 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Others: Setting prohibited	R/W
3	TEDGPL	Edge Polarity*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	Count Source*1 *2 *5 *7 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified by CKS[2:0] bits in the AGTMR2 register 1 0 1: Underflow event signal from AGTn (n = 0, 2, 4)*6 1 1 0: Divided clock AGTSCLK specified by CKS[2:0] bits in the AGTMR2 register Others: Setting prohibited	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, AGTOAn, and AGTOBn. For details on the output level at initialization, see section 22.2.7. AGTIOC : AGT I/O Control Register.

Note 1. When event counter mode is selected, the external input pin (AGTIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.

Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).

Note 3. The operating mode can only be changed when the count is stopped while both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.

Note 4. The TEDGPL bit is enabled only in event counter mode.

Note 5. To run AGT in Software Standby and Deep Software Standby mode, select AGTLCLK or AGTSCLK (TCK[2:0] = 100b, 110b).

Note 6. AGTn (n = 0, 2, 4) cannot use AGTn (n = 0, 2, 4) underflow (setting prohibited). AGTn (n = 1, 3, 5) uses the AGTn (n = 0, 2, 4) underflow.

Note 7. Do not change the TCK[2:0] bits when the CKS[2:0] bits in the AGTMR2 register is not 000b. First, change the CKS[2:0] bits in the AGTMR2 register to 000b. Then change the TCK[2:0] bits and wait for one cycle of the count source.

22.2.6 AGTMR2 : AGT Mode Register 2

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

22.2.5 AGTMR1：AGT模式寄存器1

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TMOD[2:0]	操作模式*3 000：定时器模式001：脉冲输出模式01 0：事件计数器模式011：脉冲宽度测量 模式100：脉冲周期测量模式 其他：禁止设置	R/W
3	TEDGPL	边缘极性*4 0: Single-edge 1: Both-edge	R/W
6:4	TCK[2:0]	计数源*1*2*5*7 000:PCLKB001:PCLKB8011:PCLKB2100:分频时钟AGTLCLK由AGTMR2寄存器中的CKS[2:0]位指定101:来自AGTn(n=0)的下溢事件信号 2 4)*6 110：由AGTMR2寄存器中的CKS[2:0]位指定的分频时钟AGTSCLK 其他：禁止设置	R/W
7	—	该位读取为0。写入值应为0。	R/W

Note: 对AGTMR1寄存器的写访问初始化了AGTOn、AGTIOn、AGTOAn和AGTOBn的输出。有关初始化时的输出电平的详细信息，请参阅第22.2.7节。AGTIOC：AGTIO控制寄存器。

注意1.选择事件计数器模式时，无论设置如何
TCK[2:0] bits.

注2.在计数操作期间不要切换计数源。只有当TSTART位和TCSTF标志都在
AGTCR寄存器设置为0（计数停止）。

注3.只有在AGTCR寄存器中的TSTART位和TCSTF标志都设置为0（计数停止）时停止计数才能更改操作模式。请勿在计数操作期间更改操作模式。

注4.TEDGPL位仅在事件计数器模式下启用。

注5.要在软件待机和深度软件待机模式下运行AGT，请选择AGTLCLK或AGTSCLK(TCK[2:0]=100b 110b)。注6.AGTn(n=0 2 4)不能使用AGTn(n=0 2 4)下溢（禁止设置）。AGTn(n=1 3 5)使用AGTn(n=0 2 4)下溢。

注7.当AGTMR2寄存器中的CKS[2:0]位不是000b时，不要更改TCK[2:0]位。首先，更改CKS[2:0]位
AGTMR2寄存器到000b。然后改变TCK[2:0]位并等待计数源的一个周期。

22.2.6 AGTMR2:AGT模式寄存器2

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	LPM	—	—	—	—	CKS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK or AGTSCLK Count Source Clock Frequency Division Ratio*1 *2 *3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	LPM	Low Power Mode 0: Normal mode 1: Low power mode	R/W

Note 1. Do not rewrite the CKS[2:0] bits during count operation. Only rewrite the CKS[2:0] bits when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. When count source is AGTLCLK or AGTSCLK, the switch of CKS[2:0] bits is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] bits are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] bits are set to 000b, and wait for 1 cycle of the count source.

CKS[2:0] bit (AGTLCLK or AGTSCLK Count Source Clock Frequency Division Ratio)

CKS[2:0] bits select the Count Source Clock Frequency Division Ratio for AGTLCLK or AGTSCLK.

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set this bit to 1 to operate in low power.

When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- When reading from the AGT register, read AGT register twice. Only the second reading of data is valid.
- When writing to the AGT, AGTCMA, AGTCMB, and AGTCR register, allow at least 2 cycles of the count source clock when writing to the register.
- When confirm the value written to the AGT, AGTCMA, AGTCMB, and AGTCR registers.
  - When the count operation is stopped; after writing data, it can be read in the next cycle.
  - When the count operation is operating; after writing data, it can be written 4 cycles after the count source clock.

Figure 22.2 shows the flow of how to write LPM bit

Bit	Symbol	Function	R/W
2:0	CKS[2:0]	AGTLCLK或AGTSCLK计数源时钟分频比*1*2*3 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	LPM	低功耗模式 0：正常模式1：低功耗模式	R/W

注1.在计数操作期间不要重写CKS[2:0]位。仅当AGTCR寄存器中的TSTART位和TCSTF标志都设置为0（计数停止）时才重写CKS[2:0]位。

注2.当计数源为AGTLCLK或AGTSCLK时，CKS[2:0]位的切换有效。
注3.当CKS[2:0]位不是000b时，不要切换AGTMR1寄存器中的TCK[2:0]位。在CKS[2:0]位设置为000b后，切换AGTMR1寄存器中的TCK[2:0]位，并等待计数源的1个周期。

CKS[2:0]位（AGTLCLK或AGTSCLK计数源时钟分频比）

CKS[2:0]位选择AGTLCLK或AGTSCLK的计数源时钟分频比。

LPM位（低功耗模式）

LPM位设置低功耗操作，这会影响对某些AGT寄存器的访问。将此位设置为1以在低功耗下运行。

该位为1时，禁止访问以下寄存器：

- AGT/AGTCMA/AGTCMB/AGTCR.

该位由1变为0后，对寄存器的第一次访问受到如下约束：

●读取AGT寄存器时，读取AGT寄存器两次。只有第二次读取数据是有效的。

●写入AGT、AGTCMA、AGTCMB和AGTCR寄存器时，写入寄存器时至少允许计数源时钟的2个周期。

●确认写入AGT、AGTCMA、AGTCMB、AGTCR寄存器的值时。
当计数操作停止时；写入数据后，可以在下一个周期读取。
当计数操作正在运行时；写入数据后，可在计数源时钟后4个周期写入。

图22.2显示如何写入LPM位的流程

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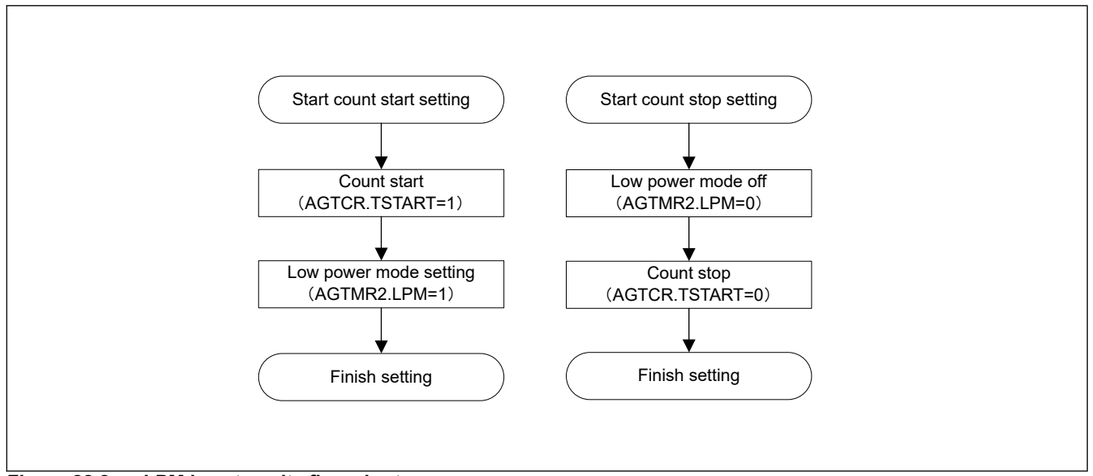

Figure 22.2 LPM how to write flow chart

22.2.7 AGTIOC : AGT I/O Control Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	I/O Polarity Switch Function varies depending on the operating mode (see Table 22.3 and Table 22.4).	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	TOE	AGTOn pin Output Enable 0: AGTOn pin output disabled 1: AGTOn pin output enabled	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	TIPF[1:0]	Input Filter*3 These bits specifies the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value. 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32	R/W
7:6	TIOGT[1:0]	Count Control*1 *2 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn pin Others: Setting prohibited	R/W

Note 1. When AGTEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. TIOGT[1:0] bits are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby and Deep Software Standby mode, the digital filter function cannot be used.

TEDGSEL bit (I/O Polarity Switch)

The TEDGSEL bit switches the AGTOn pin output polarity and the AGTIOn pin input/output edge and polarity.

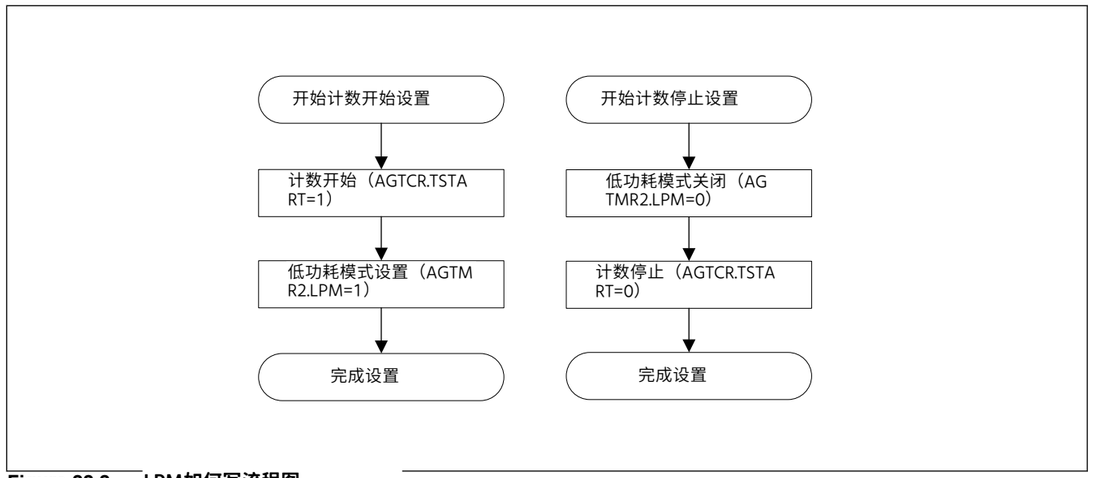

Figure 22.2 LPM如何写流程图

22.2.7 AGTIOC:AGTIO控制寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDG SEL
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TEDGSEL	IO极性开关 功能因操作模式而异（参见表22.3和表22.4）。	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	TOE	AGTOn引脚输出使能 0：禁止AGTOn引脚输出1：使能AGTOn引脚输出	R/W
3	—	该位读取为0。写入值应为0。	R/W
5:4	TIPF[1:0]	输入滤波器*3 这些位指定AGTIOn输入的滤波器采样频率。如果对AGTIOn引脚的输入进行采样并且值连续匹配3次，则将该值作为输入值。 00：无滤波器01：滤波器在PCLKB1采样0：滤波器在PCLKB8采样 11：滤波器在PCLKB32采样	R/W
7:6	TIOGT[1:0]	计数控制*1*2 00：始终计数事件01：在为AGTEEn引脚指定的极性周期内计数事件 其他：禁止设置	R/W

注1.使用AGTEEn引脚时，可以通过AGTISR寄存器中的EEPS位选择计数事件的极性。
注2.TIOGT[1:0]位仅在事件计数器模式下启用。
注3.在软件待机和深度软件待机模式期间执行事件计数器模式操作时，不能使用数字滤波器功能。

TEDGSEL位（IO极性开关）

TEDGSEL位切换AGTOn引脚输出极性和AGTIon引脚输入输出边沿和极性。

In pulse output mode, it only controls polarity of the AGTOn pin output and AGTIOn pin output. AGTOn pin output and AGTIOn pin output are initialized when the AGTMR1 register is written or the TSTOP bit in the AGTCR register is written with 1.

TOE bit (AGTOn pin Output Enable)

The TOE bit selects whether the AGTOn pin output is disabled or enabled.

TIPF[1:0] bits (Input Filter)

The TIPF[1:0] bits specify the sampling frequency of the AGTIOn pin input filter. When the input to the AGTIOn pin is sampled and the values match three times in succession, the value is regarded as the input value.

TIOGT[1:0] bits (Count Control)

The TIOGT[1:0] bits control the event count.

Table 22.3 AGTIOn pin I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) i.e. inverted output 1: Output is started at low (initialization level: low). i.e. normal output
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured.
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Note: When the TOE bit is 0, the pin state is Hi-Z.

Table 22.4 AGTOn pin output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initial level: low): Normal output 1: Output is started at high (initial level: high): Inverted output

Note: When the TOE bit is 0, a value according to the set value of the TEDGSEL bit in the pulse output mode is output.

22.2.8 AGTISR : AGT Event Pin Select Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	EEPS	AGTEEn Polarity Selection 0: An event is counted during the low-level period 1: An event is counted during the high-level period	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

EEPS bit (AGTEEn Polarity Selection)

The EEPS bit selects the polarity of events to be counted.

在脉冲输出模式下，它只控制AGTOn引脚输出和AGTIOn引脚输出的极性。AGTOn引脚输出和当AGTMR1寄存器被写入或AGTCR寄存器中的TSTOP位被写入1时，AGTIOn引脚输出被初始化。

TOE位（AGTOn引脚输出使能）

TOE位选择是禁用还是启用AGTOn引脚输出。

TIPF[1:0] bits (Input Filter)

TIPF[1:0]位指定AGTIOn引脚输入滤波器的采样频率。当AGTIOn引脚的输入被采样并且值连续匹配3次时，该值被认为是输入值。

TIOGT[1:0] bits (Count Control)

TIOGT[1:0]位控制事件计数。

Table 22.3 AGTIOn引脚IO边沿和极性切换

操作模式	Function
定时器模式	不曾用过
脉冲输出方式	0：输出从高开始（初始化电平：高），即反相输出1：输出从低开始（初始化电平：低）。即正常输出
事件计数器模式	0：上升沿计数1：下降沿计数。
脉宽测量模式	0：测量低电平宽度1：测量高电平宽度。
脉冲周期测量模式	0：从一个上升沿测量到下一个上升沿1：从一个下降沿测量到下一个下降沿。

Note: 当TOE位为0时，引脚状态为Hi-Z。

Table 22.4 AGTOn引脚输出极性切换

操作模式	Function
所有模式	0：低电平开始输出（初始电平：低电平）：正常输出1：高电平开始输出（初始电平：高电平）：反相输出

Note: TOE位为0时，输出与脉冲输出模式下的TEDGSEL位的设定值对应的值。

22.2.8 AGTISR:AGT事件引脚选择寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	EEPS	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	EEPS	AGTEEn极性选择 0：在低电平期间计数一个事件1：在高电平期间计数一个事件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

EEPS位（AGTEEn极性选择）

EEPS位选择要计数的事件的极性。

22.2.9 AGTCMSR : AGT Compare Match Function Select Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT Compare Match A Register Enable*1 *2 0: AGT Compare match A register disabled 1: AGT Compare match A register enabled	R/W
1	TOEA	AGTOAn Pin Output Enable*1 *2 0: AGTOAn pin output disabled 1: AGTOAn pin output enabled	R/W
2	TOPOLA	AGTOAn Pin Polarity Select*1 *2 0: AGTOAn pin output is started on low. i.e. normal output 1: AGTOAn pin output is started on high. i.e. inverted output	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	TCMEB	AGT Compare Match B Register Enable*1 *2 0: Compare match B register disabled 1: Compare match B register enabled	R/W
5	TOEB	AGTOBn Pin Output Enable*1 *2 0: AGTOBn pin output disabled 1: AGTOBn pin output enabled	R/W
6	TOPOLB	AGTOBn Pin Polarity Select*1 *2 0: AGTOBn pin output is started on low. i.e. normal output 1: AGTOBn pin output is started on high. i.e. inverted output	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART bit and TCSTF flag in the AGTCR register are set to 0 (count stops).
Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.

22.2.10 AGTIOSEL : AGT Pin Select Register

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	SEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

22.2.9 AGTCMSR:AGT比较匹配功能选择寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCMEA	AGT比较匹配A寄存器使能*1*2 0：禁用AGT比较匹配A寄存器1：启用AGT比较匹配A寄存器	R/W
1	TOEA	AGTOAn引脚输出使能*1*2 0：禁止AGTOAn引脚输出1：使能AGTOAn引脚输出	R/W
2	TOPOLA	AGTOAn引脚极性选择*1*2 0：AGTOAn引脚输出低电平启动。即正常输出1：AGTOAn引脚输出以高电平启动。即反相输出	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	TCMEB	AGT比较匹配B寄存器使能*1*2 0：比较匹配B寄存器禁用1：比较匹配B寄存器启用	R/W
5	TOEB	AGTOBn引脚输出使能*1*2 0：AGTOBn引脚输出禁止1：AGTOBn引脚输出使能	R/W
6	TOPOLB	AGTOBn引脚极性选择*1*2 0：AGTOBn引脚输出低电平启动。即正常输出1：AGTOBn引脚输出以高电平启动。即反相输出	R/W
7	—	该位读取为0。写入值应为0。	R/W

注1.在计数操作期间不要重写AGCTMSR寄存器。只有在TSTART位和AGTCR寄存器中的TCSTF标志设置为0（计数停止）。
注2.在脉冲宽度测量模式或脉冲周期测量模式下不要设置为1。

22.2.10 AGTIOSEL:AGT引脚选择寄存器

Base address: AGTn = 0x400E_8000 + 0x0100 × n (n = 0 to 5)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TIES	—	—	SEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

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Bit	Symbol	Function	R/W
1:0	SEL[1:0]	AGTIOn Pin Select*1 0 0: Select Pm/AGTIO as AGTIO. Pm/AGTIO can not be used as AGTIO input pin in Deep Software Standby mode. (m = 100, 301, 407, and 705 (AGT0), m = 204 and 400 (AGT1), m = 103 (AGT2), m = 600(AGT3).) 0 1: Select P404/AGTIO as AGTIO P404/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P404/AGTIOn is input only. It cannot be used for output. 1 0: Select P402/AGTIO as AGTIO P402/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P402/AGTIOn is input only. It cannot be used for output. 1 1: Select P403/AGTIO as AGTIO. P403/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P403/AGTIOn is input only. It cannot be used for output.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	TIES	AGTIOn Pin Input Enable 0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. You must set the Pin Function Select Register. See section 19, I/O Ports.

The AGTIOSEL register sets the AGTIOn pin when using the AGTIOn pin in Deep Software Standby mode and Software Standby mode.

SEL[1:0] bits (AGTIOn Pin Select)

The SEL[1:0] bits select the AGTIOn pin function.

TIES bit (AGTIOn Pin Input Enable)

The TIES bit enables or disables an external event input.

22.3 Operation

22.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA or TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit and TCMEB bit are 0 (AGT compare match A/B register are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or the TCMEB bit is 1 (AGT compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 22.3 and Figure 22.4 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

Bit	Symbol	Function	R/W
1:0	SEL[1:0]	AGTION引脚选择*1 00：选择PmAGTIO作为AGTIO。PmAGTIO在深度软件待机模式下不能用作AGTIO输入引脚。（m=100、301、407和705(AGT0)，m=204和400(AGT1)，m=103(AGT2)，m=600(AGT3)。） 01：选择P404AGTIO作为AGTIOP404AGTIO可在深度软件待机模式下用作AGTIO输入引脚。P404AGTION仅为输入。它不能用于输出。 10：选择P402AGTIO作为AGTIOP402AGTIO可以在深度软件待机模式下用作AGTIO输入引脚。P402AGTIOn仅为输入。它不能用于输出。 11：选择P403AGTIO作为AGTIO。P403AGTIO可用作深度软件待机模式下的AGTIO输入引脚。P403AGTION仅为输入。它不能用于输出。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	TIES	AGTION引脚输入使能 0：在软件待机模式下禁用外部事件输入1：在软件待机模式下启用外部事件输入	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

注1.您必须设置引脚功能选择寄存器。请参阅第19节，IO端口。

当在深度软件待机模式和软件中使用AGTIOn引脚时，AGTIOSEL寄存器设置AGTIOn引脚待机模式。

SEL[1:0]位（AGTION引脚选择）

SEL[1:0]位选择AGTIOn引脚功能。

TIES位（AGTION引脚输入使能）

TIES位启用或禁用外部事件输入。

22.3 Operation

22.3.1 重载寄存器和计数器重写操作

无论操作模式如何，对重载寄存器和计数器的重写操作的时序根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEA或TCMEB位的值而有所不同。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和计数器。当TSTART位为1（计数开始）且TCMEA位和TCMEB位为0（AGT比较匹配AB寄存器无效）时，将值与计数源同步写入重载寄存器，然后写入计数器与下一个计数源同步。当TSTART位为1（计数开始）且TCMEA位或TCMEB位为1（AGT比较匹配A寄存器或比较匹配B寄存器有效）时，值与计数源同步写入重载寄存器，然后与计数器的下溢同步到计数器。

图22.3和图22.4显示了使用TSTART位值和TCMEATCMEB位值进行重写操作的时序。

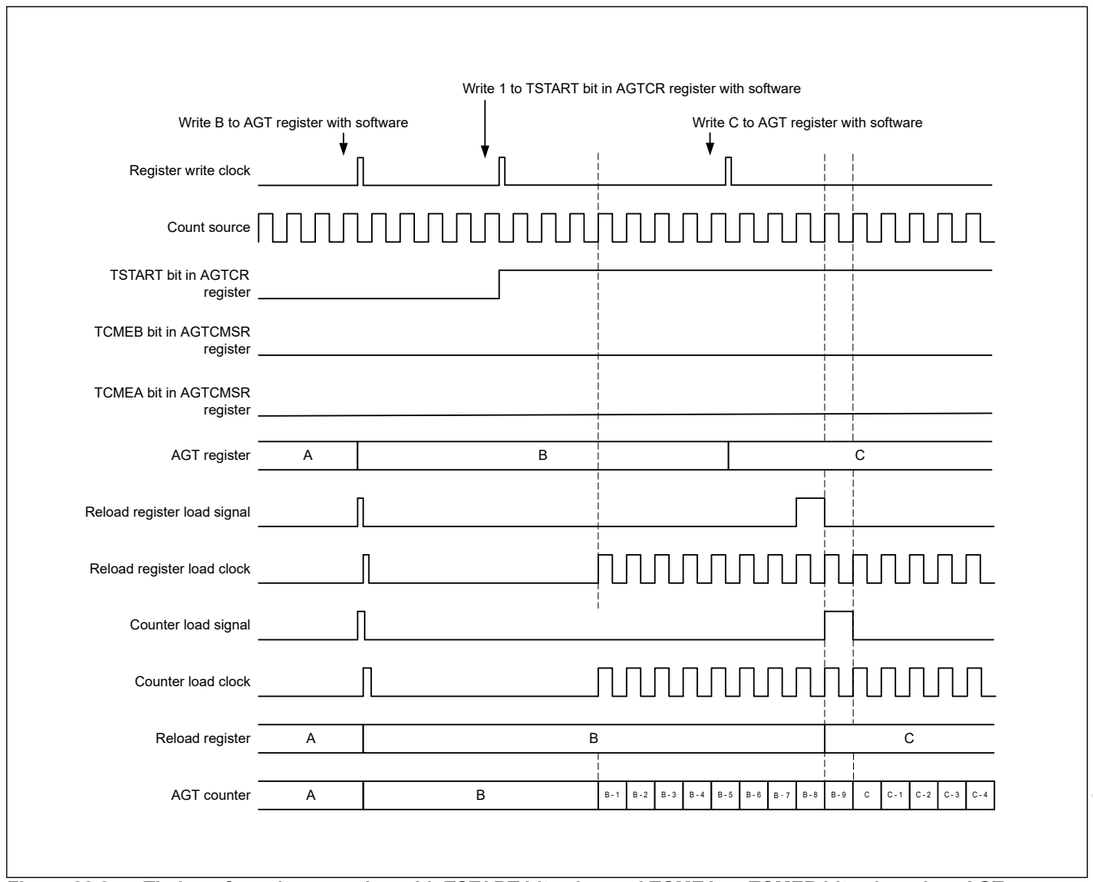

Figure 22.3 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is invalid

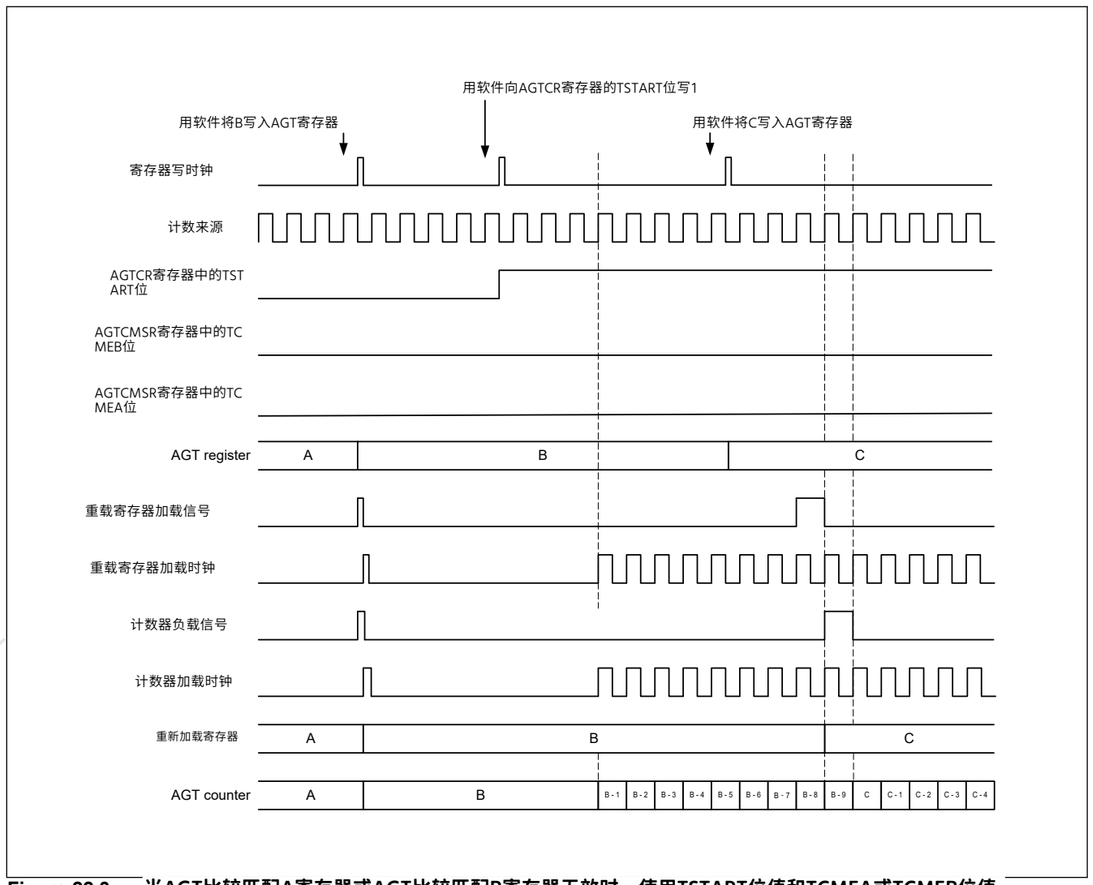

Figure 22.3 当AGT比较匹配A寄存器或AGT比较匹配B寄存器无效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

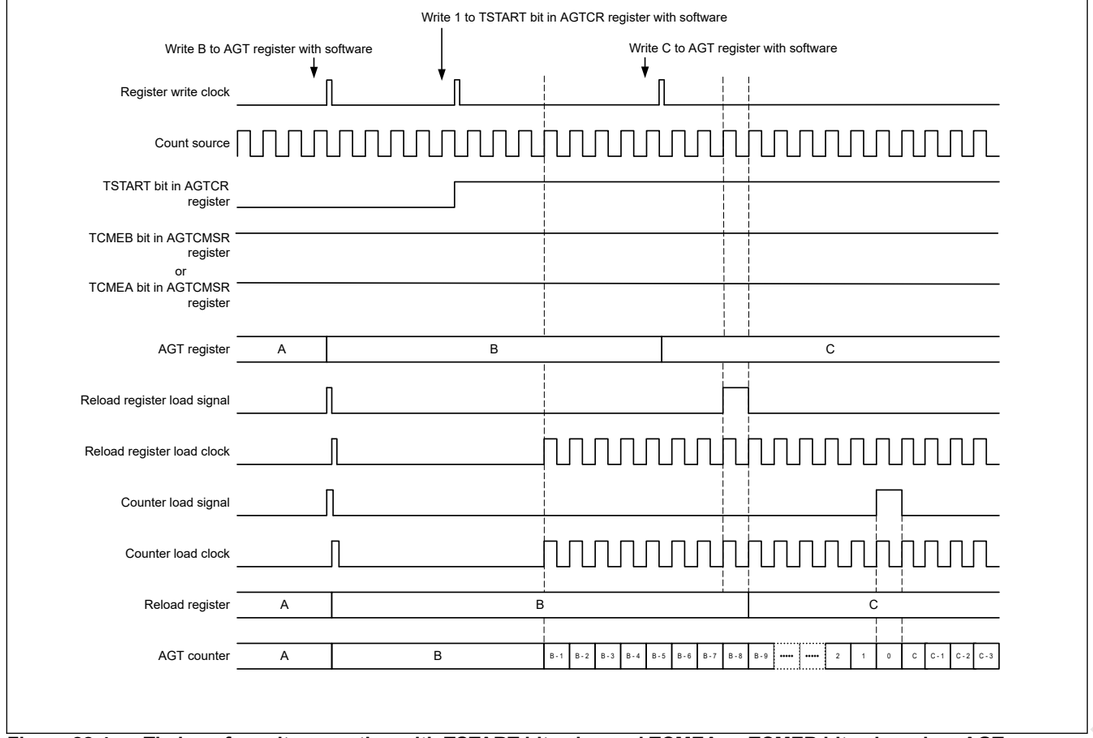

Figure 22.4 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when AGT compare match A register or AGT compare match B register is valid

22.3.2 Reload Register and AGT Compare Match A/B Register Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and AGT compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and AGT compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 22.5 shows the timing of rewrite operation with TSTART bit value for compare register A. AGT Compare register B is of the same timing as AGT compare register A.

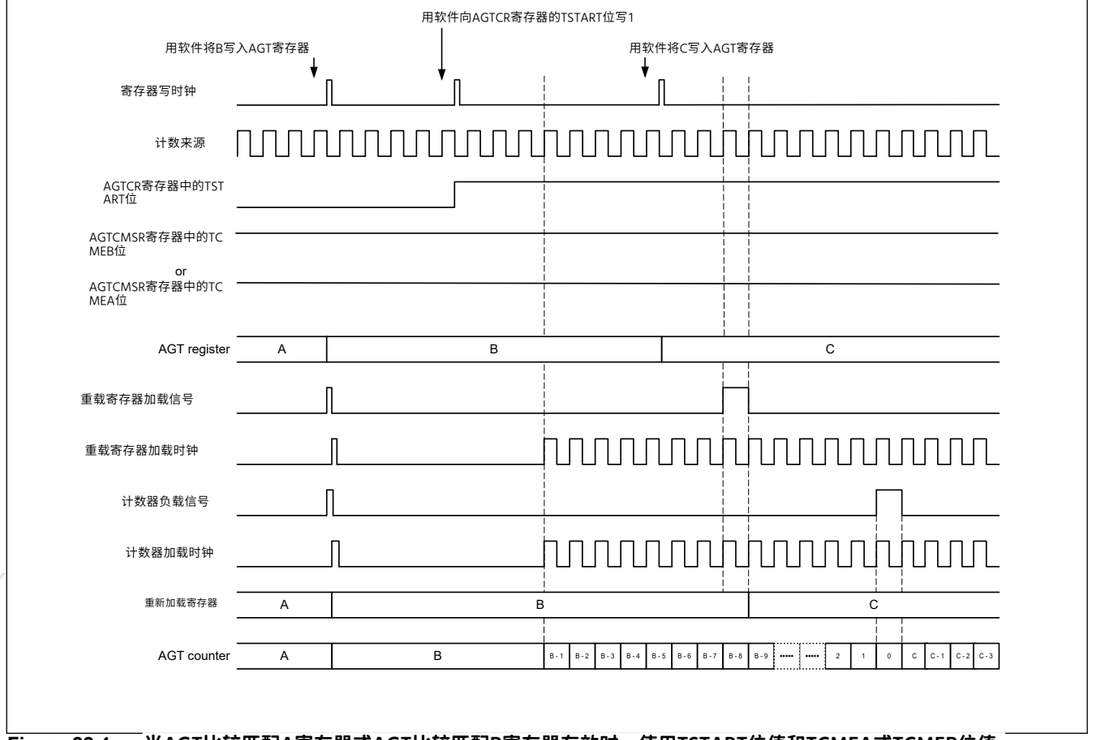

Figure 22.4 当AGT比较匹配A寄存器或AGT比较匹配B寄存器有效时，使用TSTART位值和TCMEA或TCMEB位值进行重写操作的时序

22.3.2 重载寄存器和AGT比较匹配AB寄存器重写操作

不管操作模式如何，对重载寄存器和AGT比较寄存器AB的重写操作的时序取决于AGTCR寄存器中TSTART位的值。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和AGT比较寄存器AB。当TSTART位为1（计数开始）时，该值同步写入重载寄存器计数源，然后与计数器的下溢同步到比较寄存器。

图22.5显示了比较寄存器A的TSTART位值的重写操作时序。AGT比较寄存器B与AGT比较寄存器A的时序相同。

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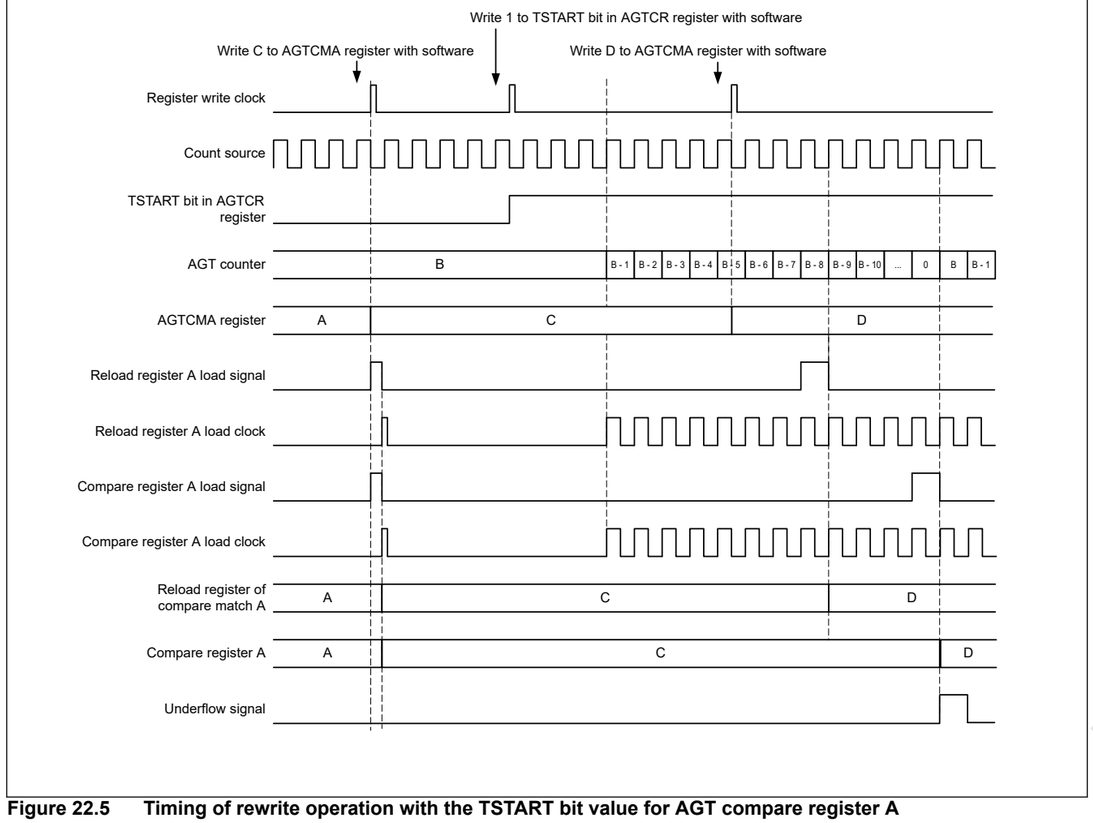


Figure 22.5 Timing of rewrite operation with the TSTART bit value for AGT compare register A

22.3.3 Timer Mode

In this mode, the AGT counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x0000 and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 22.6 shows the operation example in timer mode.

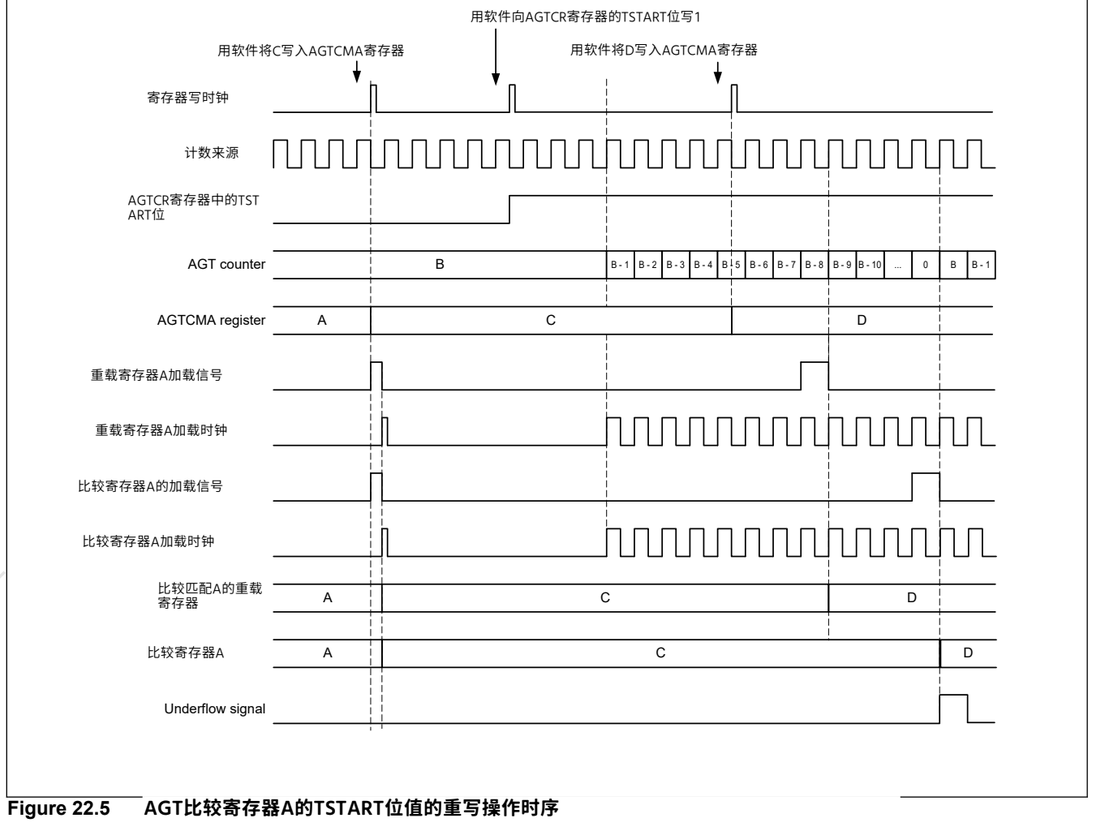


Figure 22.5 AGT比较寄存器A的TSTART位值的重写操作时序

22.3.3 定时器模式

在此模式下，AGT计数器按AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。
在定时器模式下，计数值在计数源的每个上升沿减1。当计数值达到0x0000并输入下一个计数源时，发生下溢并产生中断请求。

图22.6显示了定时器模式下的操作示例。

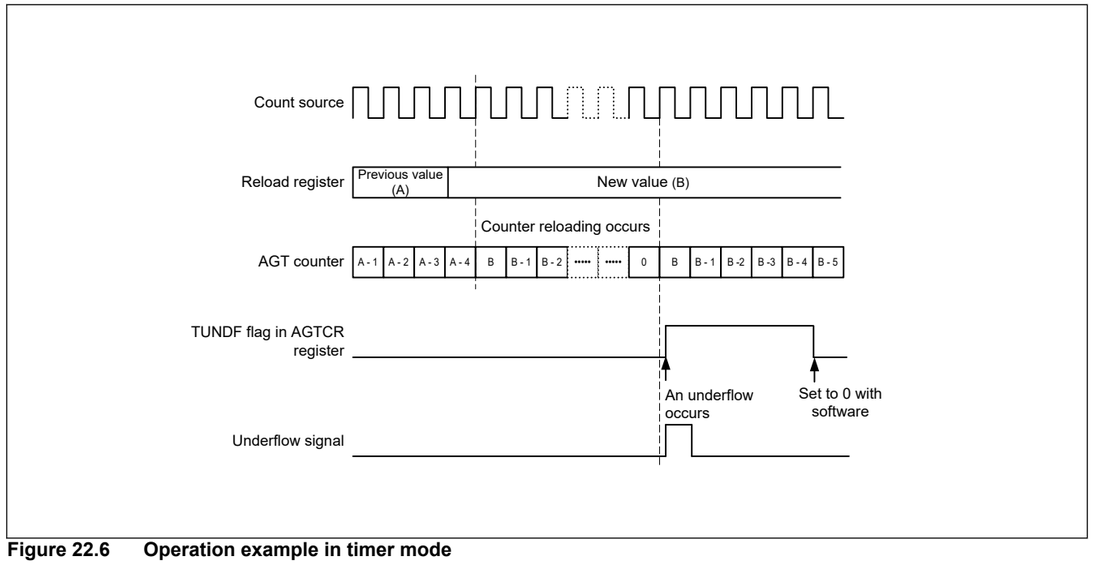


Figure 22.6 Operation example in timer mode

22.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and the output level of the AGTIOn and AGTOn pins inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0x0000 and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 22.7 shows the operation example in pulse output mode.

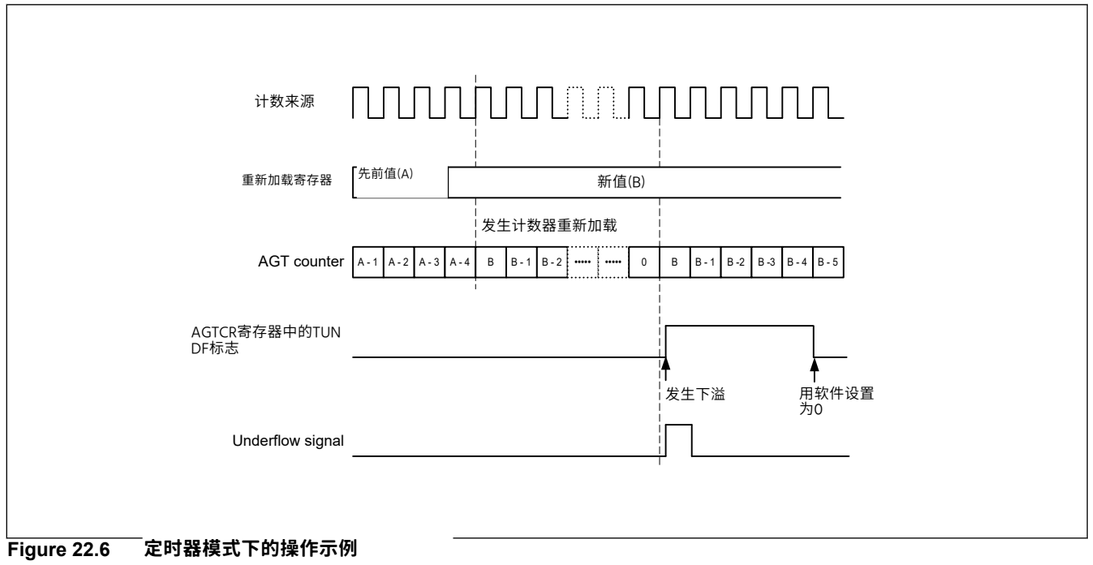


Figure 22.6 定时器模式下的操作示例

22.3.4 脉冲输出方式

在脉冲输出模式下，计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减，并且每次发生下溢时反转AGTIOn和AGTOn引脚的输出电平。

在脉冲输出模式下，计数值在计数源的每个上升沿减1。当计数值达到0x0000并输入下一个计数源时，发生下溢并产生中断请求。此外，可以从AGTIOn和AGTOn引脚输出脉冲。每次发生下溢时，输出电平都会反转。AGTOn引脚的脉冲输出可通过AGTIOC寄存器中的TOE位停止。可以通过AGTIOC寄存器中的TEDGSEL位选择输出电平。

图22.7显示了脉冲输出模式下的操作示例。

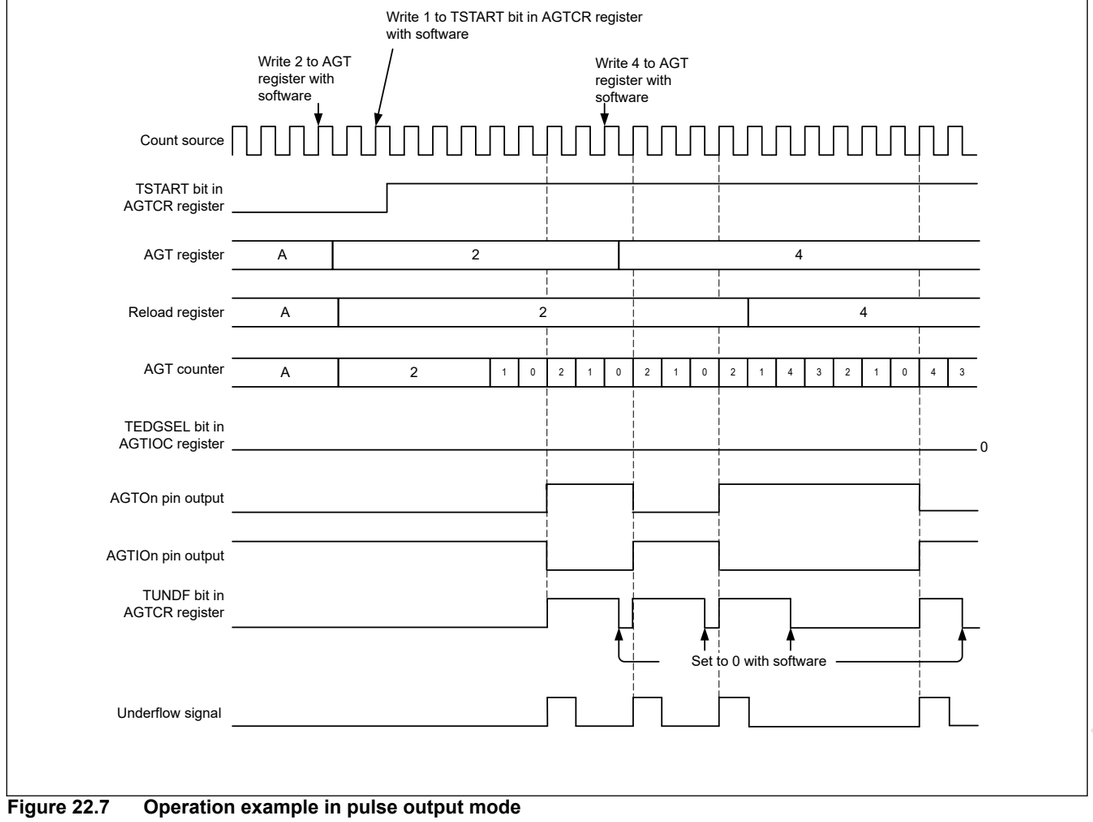


Figure 22.7 Operation example in pulse output mode

22.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal (count source) input to the AGTIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC register and AGTISR registers. In addition, the filter function for theAGTIOn pin input can be specified with bits TIPF[1:0] in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 22.8 shows the operation example in event counter mode.

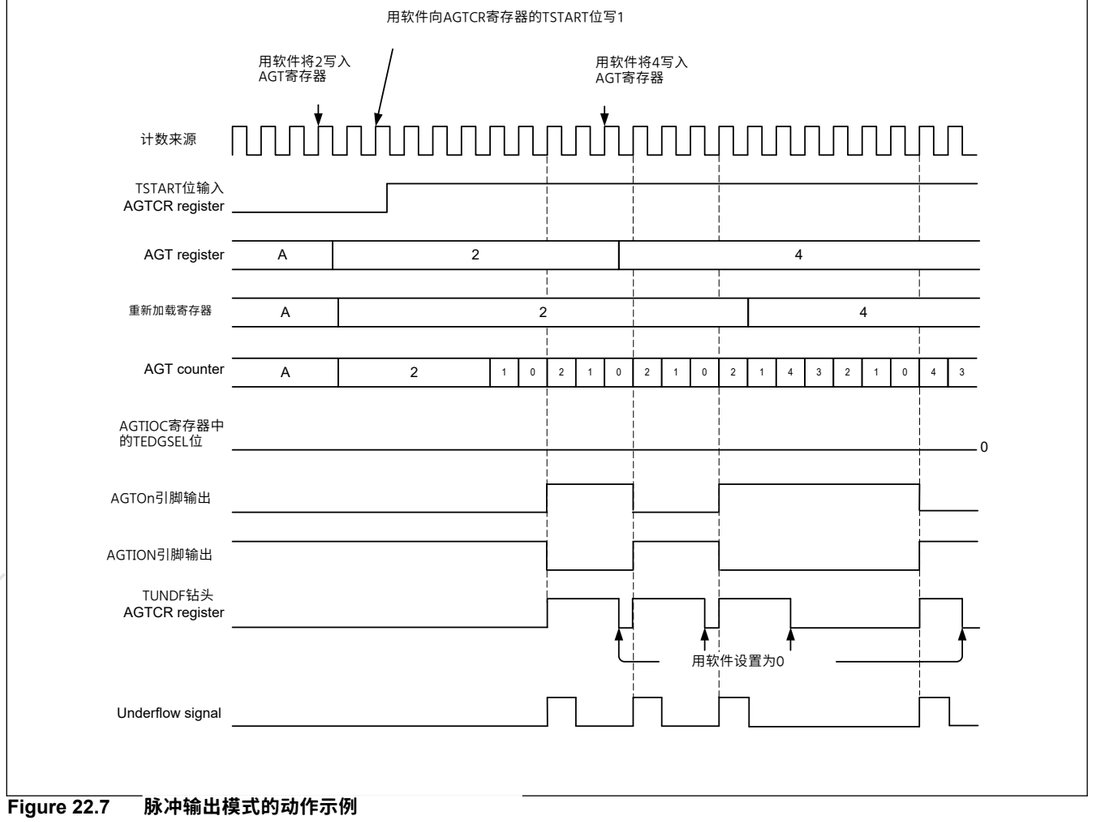


Figure 22.7 脉冲输出模式的动作示例

22.3.5 事件计数器模式

在事件计数器模式下，计数器由输入到AGTIOn引脚的外部事件信号（计数源）递减。可以使用AGTIOC寄存器和AGTISR寄存器中的TIOGT[1:0]位设置计数事件的各种周期。此外，AGTIOn引脚输入的过滤功能可通过AGTIOC寄存器中的位TIPF[1:0]指定。即使在事件计数器模式下，也可以切换AGTOn引脚的输出。

图22.8显示了事件计数器模式下的操作示例。

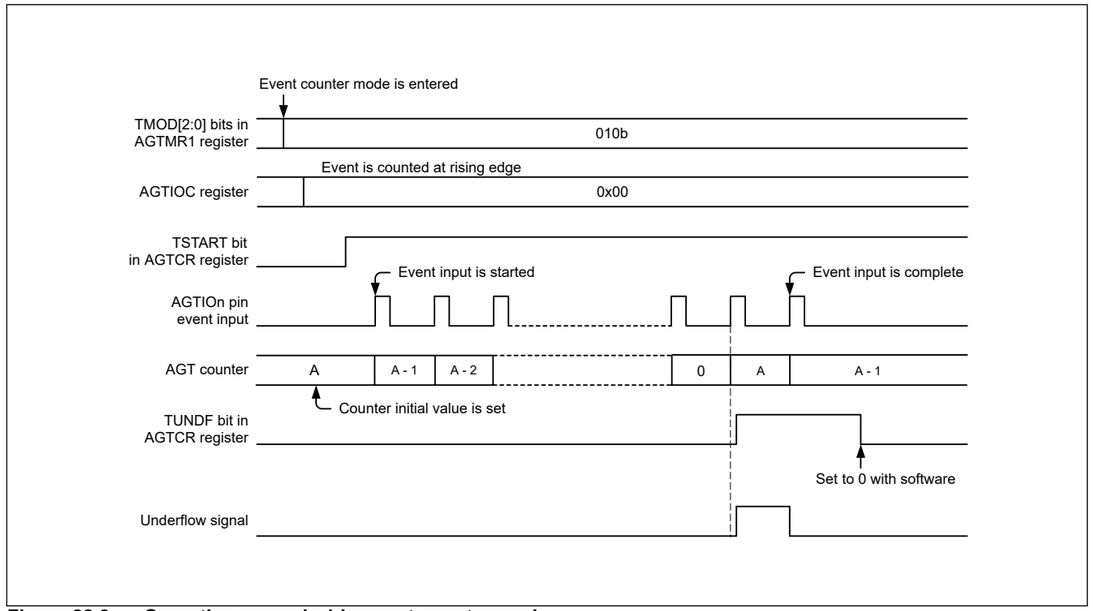
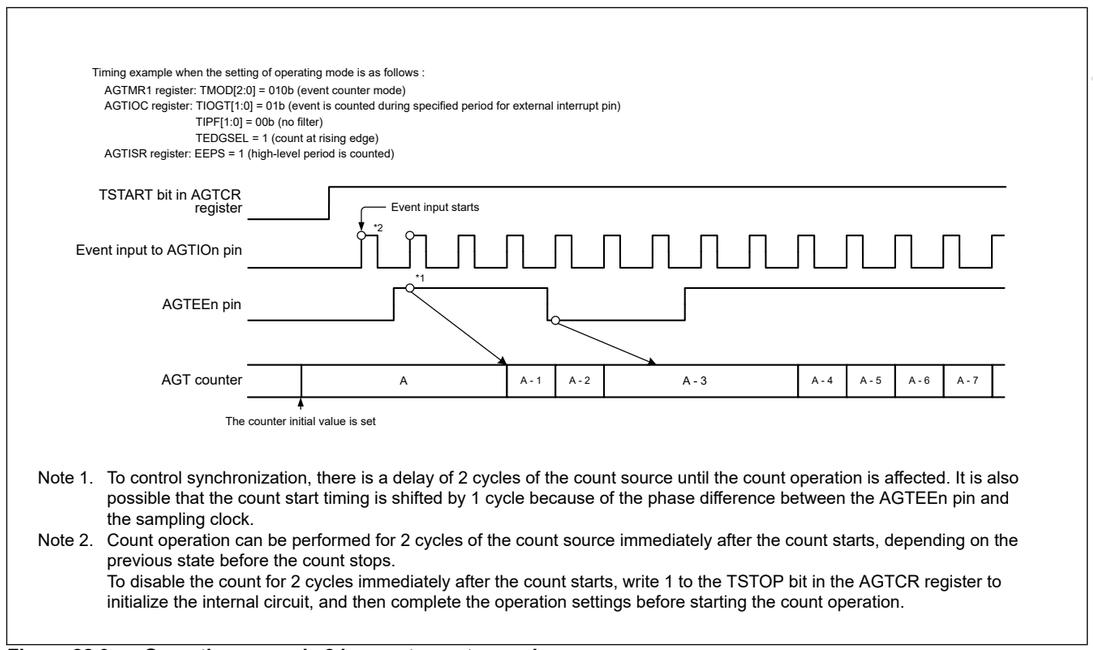


Figure 22.8 Operation example 1 in event counter mode

Figure 22.9 shows an operation example for counting during the specified period in event counter mode (TIOGT[1:0] bits in the AGTIOC register are set to 01b).



Note 1. To control synchronization, there is a delay of 2 cycles of the count source until the count operation is affected. It is also possible that the count start timing is shifted by 1 cycle because of the phase difference between the AGTEEn pin and the sampling clock.

Note 2. Count operation can be performed for 2 cycles of the count source immediately after the count starts, depending on the previous state before the count stops.
To disable the count for 2 cycles immediately after the count starts, write 1 to the TSTOP bit in the AGTCR register to initialize the internal circuit, and then complete the operation settings before starting the count operation.

Figure 22.9 Operation example 2 in event counter mode

22.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by the

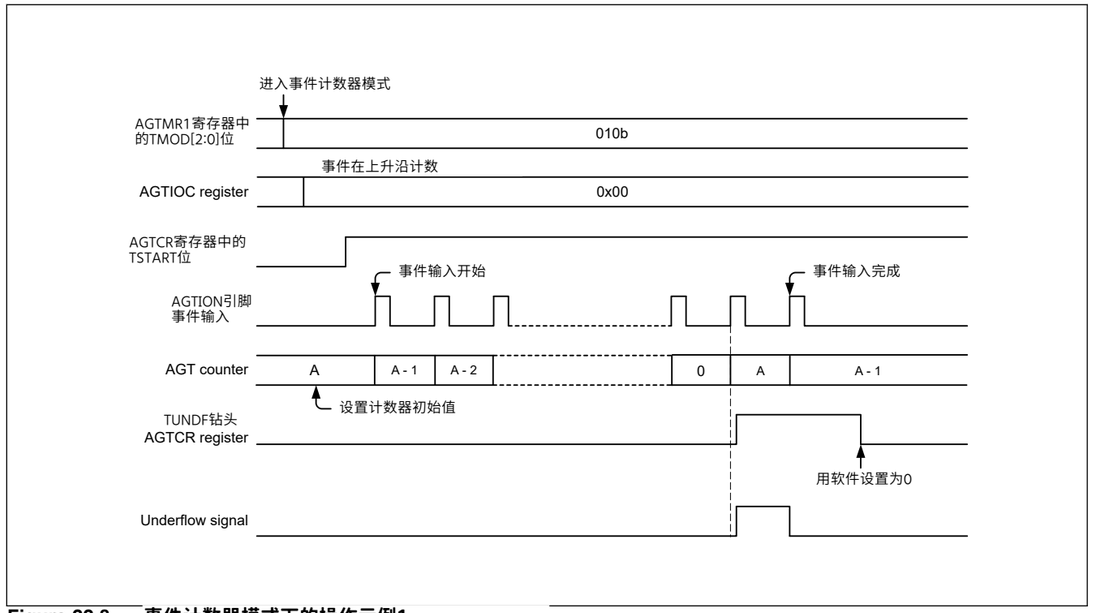
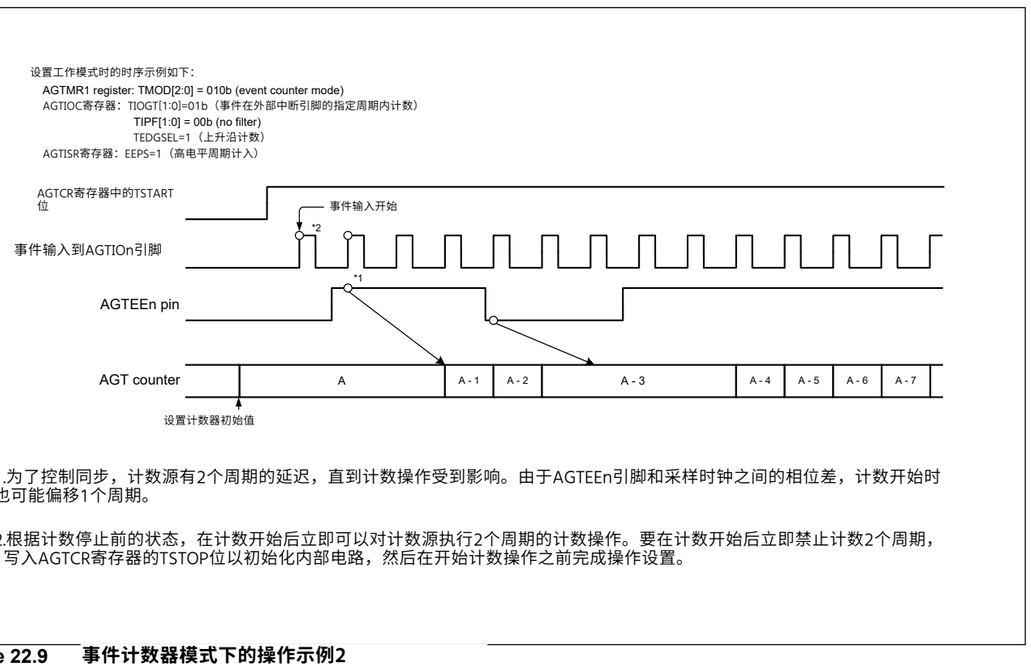


Figure 22.8 事件计数器模式下的操作示例1

图22.9显示了在事件计数器模式下在指定周期内进行计数的操作示例（AGTIOC寄存器中的TIOGT[1:0]位设置为01b）。



注1.为了控制同步，计数源有2个周期的延迟，直到计数操作受到影响。由于AGTEEn引脚和采样时钟之间的相位差，计数开始时间也可能偏移1个周期。

注2.根据计数停止前的状态，在计数开始后立即可以对计数源执行2个周期的计数操作。要在计数开始后立即禁止计数2个周期，将1写入AGTCR寄存器的TSTOP位以初始化内部电路，然后在开始计数操作之前完成操作设置。

Figure 22.9 事件计数器模式下的操作示例2

22.3.6 脉冲宽度测量模式

在脉冲宽度测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲宽度。当AGTIOC寄存器中的TEDGSEL位指定的电平输入到AGTIOn引脚时，计数器递减

count source selected with the TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 22.10 shows the operation example in pulse width measurement mode.

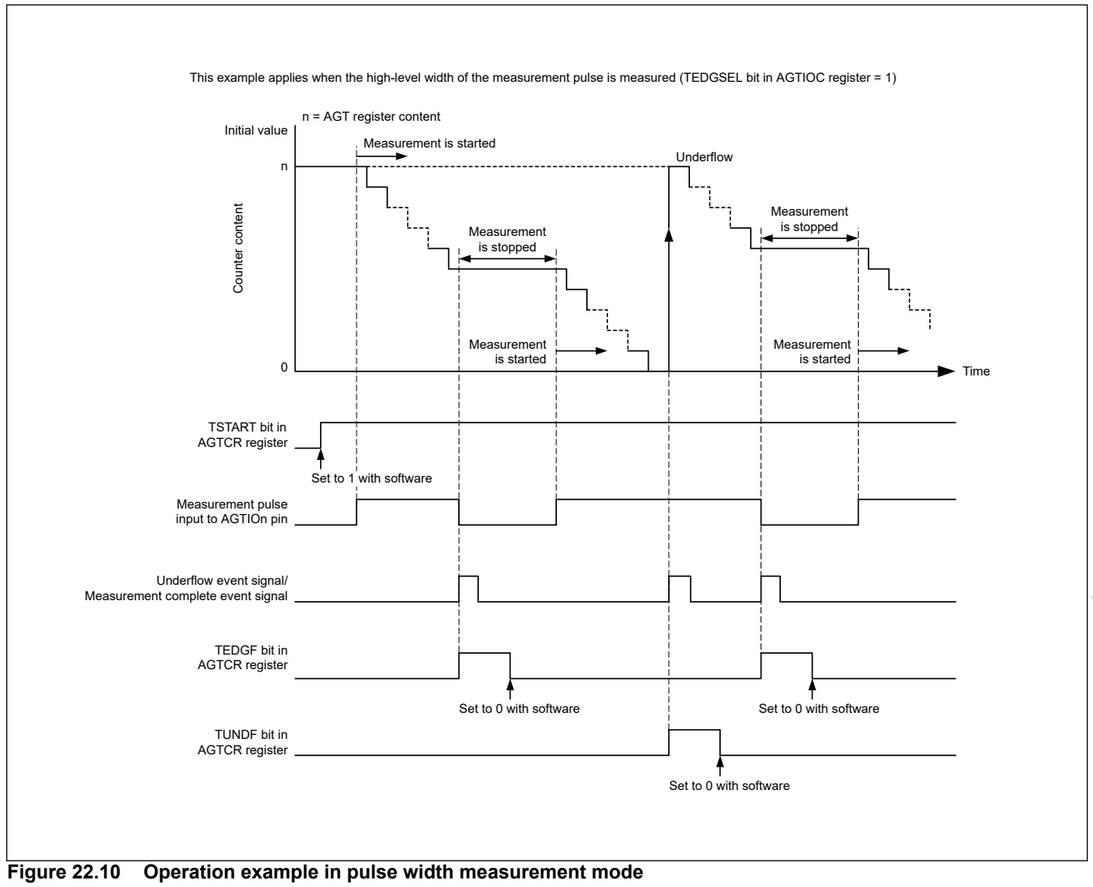


Figure 22.10 Operation example in pulse width measurement mode

22.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with TCK[2:0] bits in the AGTMR1 register. When a pulse with the period specified by the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF flag in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 22.4.6. How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF flag in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 22.11 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input might be ignored.

通过AGTMR1寄存器中的TCK[2:0]位选择计数源。当AGTIOn引脚上的指定电平结束时，计数器停止，AGTCR寄存器中的TEDGF位设置为1（接收到有效沿），并产生中断请求。通过在计数器停止时读取计数值来执行脉冲宽度数据的测量。此外，当测量期间计数器下溢时，AGTCR寄存器中的TUNDF位设置为1，并产生中断请求。

图22.10显示了脉宽测量模式下的操作示例。

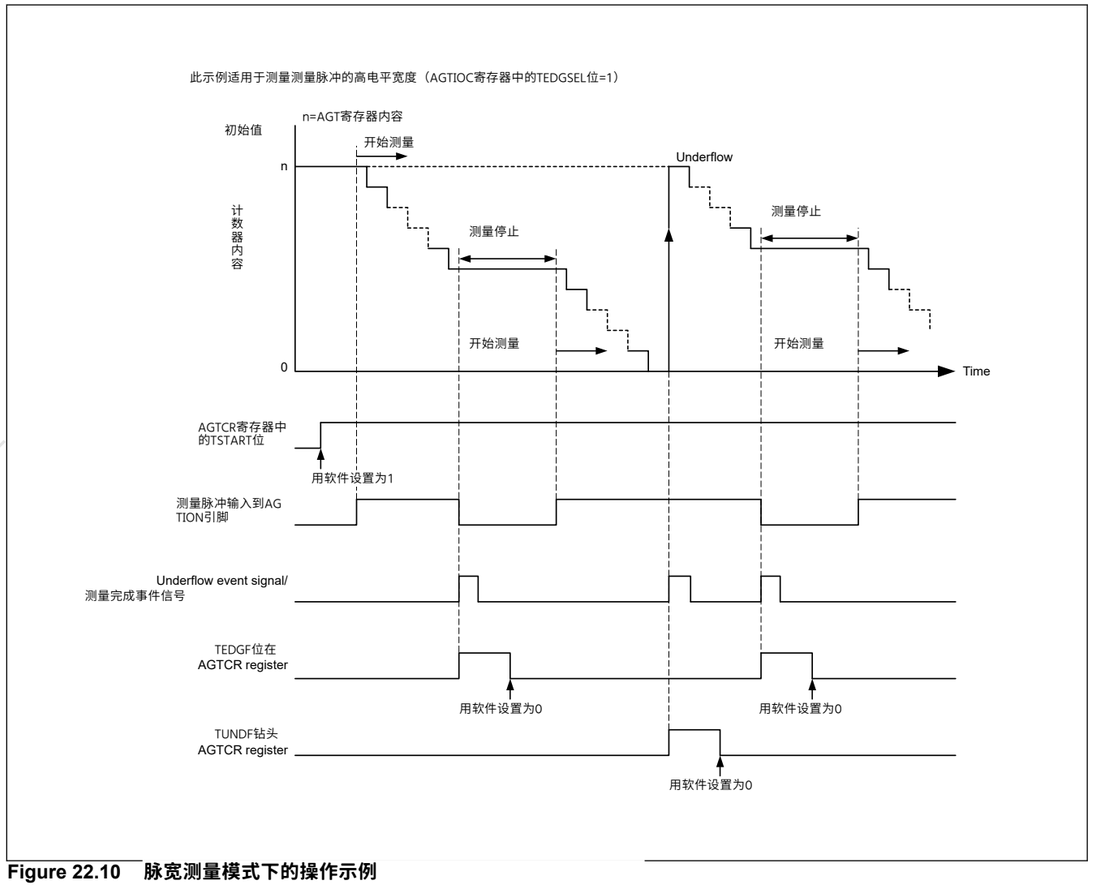


Figure 22.10 脉宽测量模式下的操作示例

22.3.7 脉冲周期测量模式

在脉冲周期测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲周期。计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTIOC寄存器中TEDGSEL位指定周期的脉冲输入到AGTIOn引脚时，计数值在计数源的上升沿传送到读出缓冲器。重载寄存器中的值在下一个上升沿加载到计数器。同时，AGTCR寄存器中的TEDGF标志设置为1（接收到有效沿）并产生中断请求。此时读取读出缓冲器（AGT寄存器），与重载值的差值（见22.4.6.如何计算事件数、脉冲宽度和脉冲周期）是输入脉冲的周期数据。周期数据被保留，直到读出缓冲器被读取。当计数器下溢时，AGTCR寄存器中的TUNDF标志设置为1（下溢）并产生中断请求。

图22.11显示了脉冲周期测量模式下的操作示例。

仅测量周期长于计数源周期两倍的输入脉冲。此外，低电平和高电平宽度都必须长于计数源的周期。如果输入比这些条件短的脉冲周期，输入可能会被忽略。

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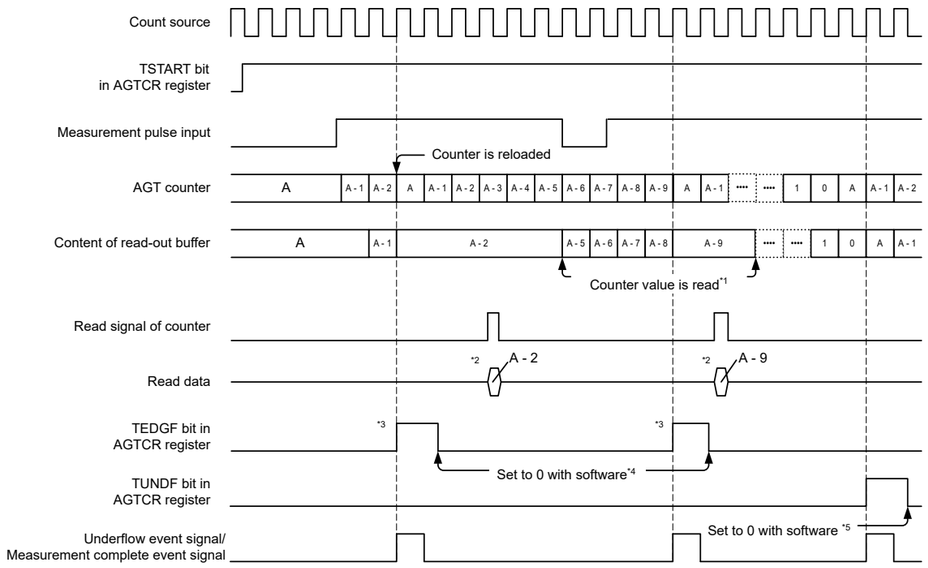


This example applies when the initial value of the AGT register is set to A, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF flag is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF flag in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF flag in the AGTCR register with an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF flag in the AGTCR register with an 8-bit memory manipulation instruction.

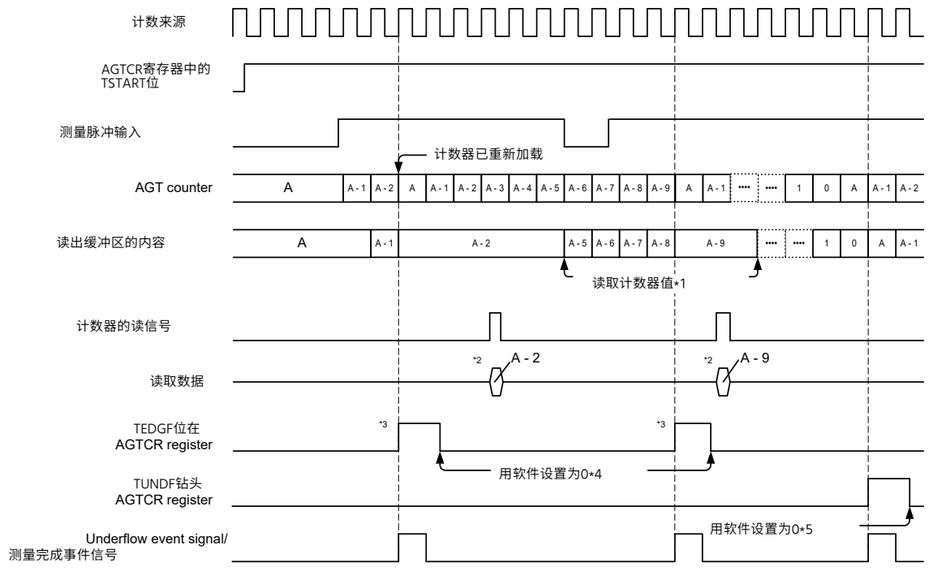
Figure 22.11 Operation example in pulse period measurement mode

22.3.8 Compare Match function

The compare match function detects matches (compare match) between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA or TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected with the TCK[2:0] bits in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF flag in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When the compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 22.3.1. Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOAn, AGTOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 22.12 shows the operation example in compare match mode.



此示例适用于将AGT寄存器的初始值设置为A，将AGTIOC寄存器中的TEDGSEL位设置为0，并测量从一个上升沿到下一个测量脉冲沿的周期。

注1.从TEDGF标志设置为1（接收到有效边沿）到输入下一个有效边沿期间，必须执行从AGT寄存器的读取。读出缓冲器的内容一直保留到AGT寄存器被读取。如果在输入有效边沿之前未读取，则保留前一周期的测量结果。

注2.在脉冲周期测量模式下读取AGT寄存器时，会读取读出缓冲区的内容。
注3.当输入测量脉冲的有效边沿，然后输入外部脉冲的设置边沿时，AGTCR寄存器中的TEDGF标志设置为1（接收到有效边沿）。

注4.要使用软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TEDGF标志。注5.要通过软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TUNDF标志。

Figure 22.11 脉冲周期测量模式下的操作示例

22.3.8 比较匹配功能

比较匹配功能检测AGTCMA或AGTCMB寄存器的内容与AGT寄存器的内容之间的匹配（比较匹配）。该功能在AGTCMSR寄存器中的TCMEA或TCMEB位为1时使能（比较匹配A寄存器或比较匹配B寄存器有效）。计数器按AGTMR1寄存器中TCK[2:0]位选择的计数源递减，当AGT和AGTCMA或AGTCMB的值匹配时，AGTCR寄存器中的TCMAFTCMBF标志设置为1（匹配），并产生中断请求。

当比较匹配功能启用时，对重载寄存器和计数器的重写操作的时序不同。请参阅第22.3.1节。重载寄存器和计数器重写操作了解详情。此外，AGTOAn、AGTOBn引脚的输出电平通过匹配和下溢反转。输出电平可以选择与

AGTCMSR寄存器中的TOPOLA或TOPOLB位。

图22.12显示了比较匹配模式下的操作示例。

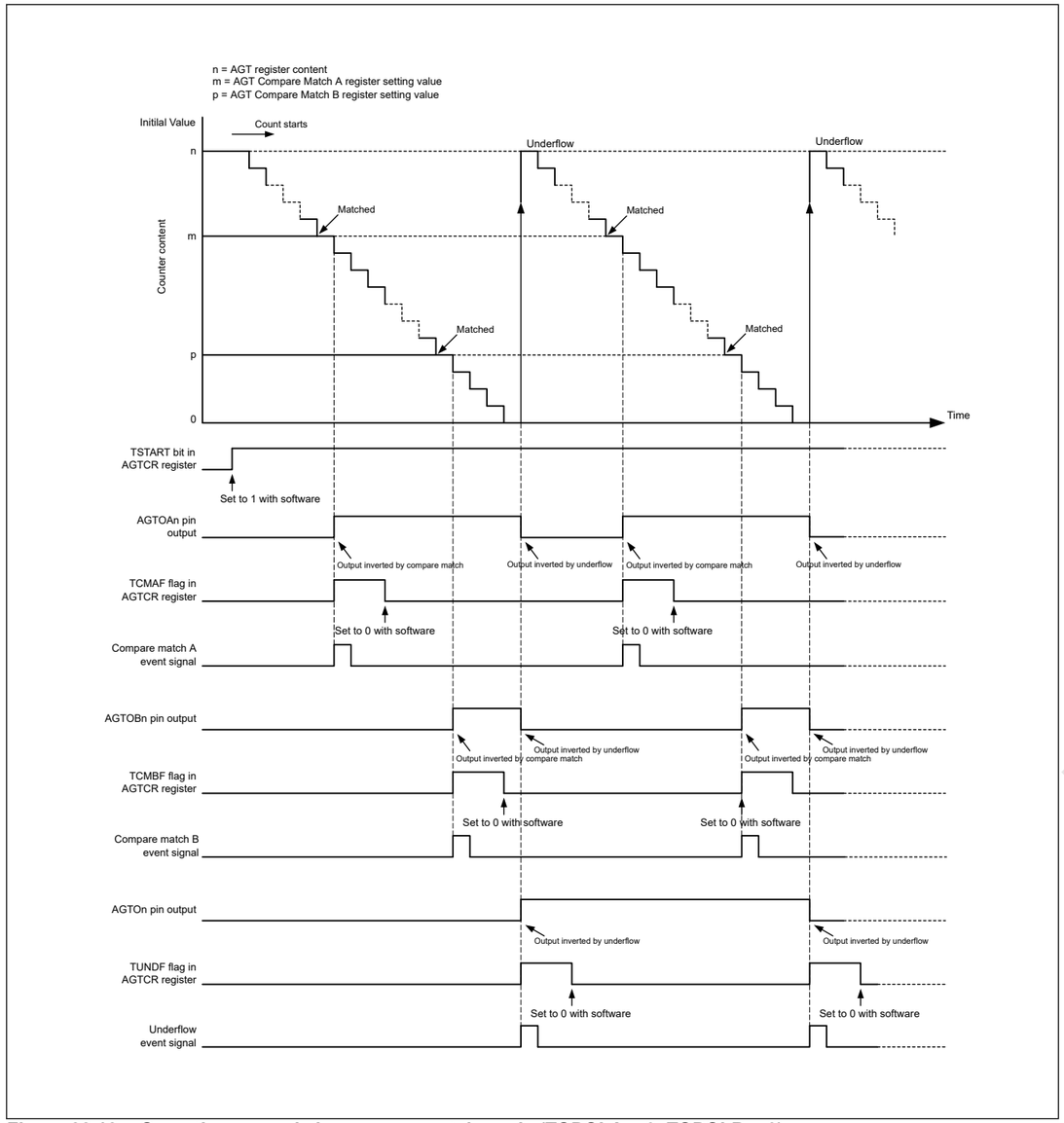


Figure 22.12 Operation example in compare match mode (TOPOLA = 0, TOPOLB = 0)

22.3.9 Output Settings for Each Mode

Table 22.5 to Table 22.8 list the states of pins AGTOn, AGTIOn, AGTOAn, and AGTOBn pins in each mode.

Table 22.5 AGTOn pin setting

Operating mode	AGTIOC register		AGTOn pin output
	TOE bit	TEDGSEL bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

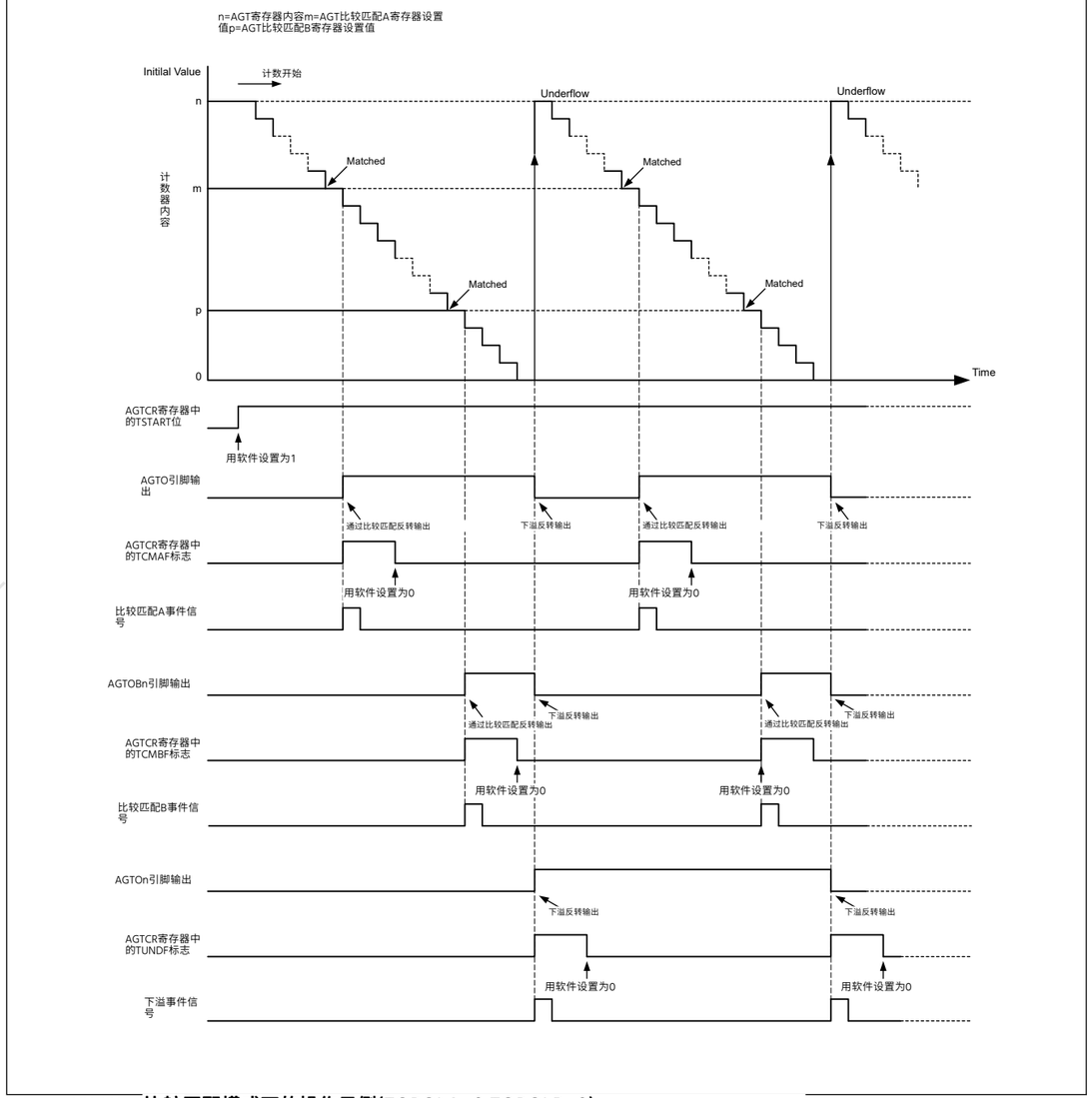


Figure 22.12 比较匹配模式下的操作示例(TOPOLA=0 TOPOLB=0)

22.3.9 每种模式的输出设置

表22.5至表22.8列出了每种模式下引脚AGTOn、AGTIOn、AGTOAn和AGTOBn引脚的状态。

Table 22.5 AGTOn引脚设置

操作模式	AGTIOC register		AGTOn引脚输出
	脚趾位	TEDGSEL bit	
所有模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用

Table 22.6 AGTIOn pin setting

Operating mode	AGTIOC register TEDGSEL bit	AGTIOn pin I/O
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 22.7 AGTOAn pin setting

Operating mode	AGTCMSR register TOEA bit	AGTCMSR register TOPOLA bit	AGTOAn pin output
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 22.8 AGTOBn pin setting

Operating mode	AGTCMSR register TOEB bit	AGTCMSR register TOPOLB bit	AGTOBn pin output
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

22.3.10 Standby Mode

The AGT can operate in Software Standby and Deep Software Standby mode. Set it to Software Standby or Deep Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 22.9 and Table 22.10 show the setting that can be used in Software Standby and Deep Software Standby mode.

Table 22.6 AGTIOn引脚设置

操作模式	AGTIOC register TEDGSEL bit	AGTIOn pin I/O
定时器模式	0 or 1	Input (not used)
脉冲输出方式	1	正常输出
	0	反相输出
事件计数器模式	0 or 1	Input
脉宽测量模式		
脉冲周期测量模式		

Table 22.7 AGTO引脚设置

操作模式	AGTCMSR register TOEA bit	AGTCMSR register TOPOLA bit	AGTO引脚输出
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

Table 22.8 AGTOBn引脚设置

操作模式	AGTCMSR register TOEB bit	AGTCMSR register TOPOLB bit	AGTOBn引脚输出
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

22.3.10 待机模式

AGT可以在软件待机和深度软件待机模式下运行。将其设置为软件待机或深度软件计数操作开始的待机模式（TSTART=1，TCSTF=1）。

表22.9和表22.10显示了可在软件待机和深度软件待机模式下使用的设置。

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Table 22.9 Usable settings in Software Standby and Deep Software Standby mode (AGTn (n = 0, 2, 4)*2)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	—
Event counter mode	—	AGTIOn*1	—
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—

Note: —: invalid
Note 1. When using the AGTIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.
Note 2. AGT4 cannot operate in Deep Software Standby mode.

Table 22.10 Usable settings in Software Standby and Deep Software Standby mode (AGTn (n = 1, 3, 5)*3)

Operating mode	AGTMR1.TCK[2:0]	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • Compare match A/B
Event counter mode	—	AGTIOn*2	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • Active edge

Note: —: invalid
Note: Release of Software Standby or Deep Software Standby mode is only AGT1.
Note: Compare match A/B is resurgence factor of CPU from Software Standby mode.
Note 1. Only when AGTn (n = 0, 2, 4) operates in Table 22.9
Note 2. When using the AGTIOn pin for external event input in Software Standby mode, set AGTIOSEL.TIES = 1.
Note 3. AGT5 cannot operate in Deep Software Standby mode.

22.3.11 Interrupt Sources

The AGTn has three interrupt sources as listed in Table 22.11.

Table 22.11 AGT interrupt sources

Name	Interrupt source	DMAC/DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input pin (AGTIOn) is complete in pulse width measurement mode • When the set edge of the external input pin (AGTIOn) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	• When the values of AGT register and AGTCMA register match	Possible
AGTn_AGTCMBI	• When the values of AGT register and AGTCMB register match	Possible

Note: Channel number (n = 0 to 5)

22.3.12 Event Signal Output to ELC

The AGT uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGT outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 18, Event Link Controller (ELC).

Table 22.9 软件待机和深度软件待机模式下的可用设置(AGTn(n=0 2 4)*2)

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 110b	AGTLCLK or AGTSCLK	—
脉冲输出方式	100b or 110b	AGTLCLK or AGTSCLK	—
事件计数器模式	—	AGTIOn*1	—
脉宽测量模式	100b or 110b	AGTLCLK or AGTSCLK	—
脉冲周期测量模式	100b or 110b	AGTLCLK or AGTSCLK	—

Note: —: invalid
注1.在软件待机模式下将AGTIOn引脚用于外部事件输入时，设置AGTIOSEL.TIES=1。
注2.AGT4不能在深度软件待机模式下运行。

Table 22.10 软件待机和深度软件待机模式下的可用设置(AGTn(n=1 3 5)*3)

操作模式	AGTMR1.TCK[2:0]	工作时钟	CPU的中兴系数
定时器模式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • 比较匹配AB
脉冲输出方式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • 比较匹配AB
事件计数器模式	—	AGTIOn*2	• Underflow • 比较匹配AB
脉宽测量模式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • 主动边缘
脉冲周期测量模式	100b or 110b or 101b*1	AGTLCLK or AGTSCLK or AGTn (n = 0, 2, 4) underflow	• Underflow • 主动边缘

Note: —: invalid
Note: 软件待机或深度软件待机模式的释放只有AGT1。
Note: 比较匹配AB是CPU从软件待机模式中恢复的因素。
注1.仅当AGTn(n=0 2 4)在表22.9中运行时
注2.在软件待机模式下将AGTIOn引脚用于外部事件输入时，设置AGTIOSEL.TIES=1。
注3.AGT5不能在深度软件待机模式下运行。

22.3.11 中断源

AGTn有表22.11中列出的三个中断源。

Table 22.11 AGT中断源

Name	中断源	DMAC/DTC activation
AGTn_AGTI	• 当计数器下溢时 • 在脉冲宽度测量模式下完成外部输入引脚(AGTIOn)的有效宽度测量时 • 在脉冲周期测量模式下输入外部输入引脚(AGTIOn)的设置边沿时。	Possible
AGTn_AGTCMAI	• 当AGT寄存器和AGTCMA寄存器的值匹配时	Possible
AGTn_AGTCMBI	• 当AGT寄存器和AGTCMB寄存器的值匹配时	Possible

Note: 通道号（n=0到5）

22.3.12 事件信号输出到ELC

AGT使用事件链接控制器(ELC)使用中断请求信号作为事件信号执行到指定模块的链接操作。AGT输出比较匹配A、比较匹配B和下溢测量完成信号作为事件信号。有关详细信息，请参阅第18节，事件链接控制器(ELC)。

22.4 Usage Notes

22.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 22.1) is set to other than the event counter mode, or the count source is set to other than AGTn underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT other than the TCSTF flag until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 3 cycles of the count source. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGT. Other than the TCSTF flag until this bit is set to 0.

- When the operating mode (see Table 22.1) is set to event counter mode, or the count source is set to AGT1 underflow event signal (TCK[2:0] = 101b):
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 2 PCLKB cycles. Do not access the registers associated with AGT other than the TCSTF flag until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 2 PCLKB cycles. When the TCSTF flag is set to 0, the count is stopped. Do not access the registers associated with AGT other than the TCSTF flag until this bit is set to 0.

22.4.2 Access to Counter Register

When the TSTART bit and TCSTF flag in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

22.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, AGTCMSR and AGTIOC) can be changed only when the count is stopped with both the TSTART bit and TCSTF flag set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of TEDGF, TUNDF, TCMAF, and TCMBF flags are undefined. Before starting the count, write 0 to the following flags:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

22.4.4 Output pin setting

When using the AGTOn, AGTIOn, AGTOAn, or AGTOBn as an output pin, set up the Operation and determine the initial output values. Then set an output mode in the port register.

When using the AGTIOn as an input pin in pulse width measurement mode or pulse period measurement mode, set up the Operation and start count operation. Then start to enter external events from the AGTIOn pin. Invalidate the first measurement and validate the second and later completed measurements.

22.4.5 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting TIPF[1:0] bits and when the TEDGSEL bit in the AGTIOC register changes.

22.4.6 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end

22.4 使用说明

22.4.1 计数操作启动和停止控制

●当操作模式（见表22.1）设置为非事件计数器模式，或计数源设置为非AGTn下溢事件信号（TCK[2:0]=101b）时：

在计数停止期间将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在计数源的3个周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGT相关的寄存器，而不是TCSTF标志。

在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志在计数源的3个周期内保持为1。当TCSTF标志设置为0时，停止计数。不要访问与AGT关联的寄存器。除TCSTF标志外，直到该位设置为0。

●当工作模式（见表22.1）设置为事件计数器模式，或计数源设置为AGT1下溢事件信号（TCK[2:0]=101b）时：

在停止计数时将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在2个PCLKB周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGT相关的寄存器，而不是TCSTF标志。

在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志保持1持续2
PCLKB周期。当TCSTF标志设置为0时，停止计数。不要访问与相关的寄存器
AGT不是TCSTF标志，直到该位设置为0。

22.4.2 访问计数器寄存器

当AGTCR寄存器中的TSTART位和TCSTF标志都为1（计数开始）时，连续写入AGT寄存器时，在两次写入之间至少允许计数源时钟的3个周期。

22.4.3 更改模式时

与AGT操作模式相关的寄存器（AGTMR1、AGTMR2、AGTIOC、AGTISR、AGTCMSR和AGTIOC）只有在TSTART位和TCSTF标志都设置为0（计数停止）时停止计数时才能更改。在计数操作期间不要更改这些寄存器。

当与AGT工作模式相关的寄存器发生变化时，TEDGF、TUNDF、TCMAF和
TCMBF标志未定义。在开始计数之前，将0写入以下标志：

●TEDGF（未收到有效边沿）

- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

22.4.4 输出引脚设置

当使用AGTOn、AGTIOn、AGTOAn或AGTOBn作为输出引脚时，设置操作并确定初始输出值。然后在端口寄存器中设置一个输出模式。

在脉冲宽度测量模式或脉冲周期测量模式下使用AGTIOn作为输入引脚时，设置
操作并开始计数操作。然后开始从AGTIOn引脚输入外部事件。使第一次测量无效并验证第二次和以后
完成的测量。

22.4.5 数字滤波器

使用数字滤波器时，在设置TIPF[1:0]位后以及AGTIOC寄存器中的TEDGSEL位发生变化时，在数字滤波器时钟的5个周期内不要启动定时器操作。

22.4.6 如何计算事件编号、脉冲宽度和脉冲周期

●在事件计数器模式下，事件编号以数学方式表示如下：
事件编号=计数器的初始值[AGT寄存器]活动事件结束的计数器值

- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1.

22.4.7 When Count is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

22.4.8 When Selecting AGTn (n = 0, 2, 4) Underflow as the Count Source

Operate according to the following procedures described in this section when selecting the underflow event signal as the count source.

(1) Procedure for starting operation

1. Set AGT.
2. Start the count operation of AGTn (n = 1, 3, 5).
3. Start the count operation of AGTn (n = 0, 2, 4).

(2) Procedure for stopping operation

1. Stop the count operation of AGTn (n = 0, 2, 4).
2. Stop the count operation of AGTn (n = 1, 3, 5).
3. Stop the count source clock of AGTn (n = 1, 3, 5) (write 000b in the AGTMR1.TCK[2:0] bits).

22.4.9 Module-stop function

AGT operation can be disabled or enabled using Module Stop Control Register D (MSTPCRD) and Module Stop Control Register E (MSTPCRE). The AGT module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes

22.4.10 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTIO, AGTEE, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

●在脉冲宽度测量模式下，脉冲宽度以数学方式表示如下：
脉冲宽度=停止测量的计数器值下一个停止测量的计数器值

●在脉冲周期测量模式下，输入脉冲周期的数学表达式如下：
输入脉冲周期=（计数器初始值[AGT寄存器]读出缓冲器的读取值）+1。

22.4.7 当计数被TSTOP位强制停止时

计数器被AGTCR寄存器中的TSTOP位强制停止后，在计数源的1个周期内不要访问以下IO寄存器：

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

22.4.8 选择AGTn(n=0 2 4)下溢作为计数源时

选择下溢事件信号作为计数源时，请按照本节所述的以下步骤进行操作。

(1) 开始运行的步骤

1. Set AGT.
2.启动AGTn(n=1 3 5)的计数操作。
3.启动AGTn(n=0 2 4)的计数操作。

(2) 停止运行的步骤

1.停止AGTn(n=0 2 4)的计数操作。
2.停止AGTn(n=1 3 5)的计数操作。
3.停止AGTn(n=1 3 5)的计数源时钟（将000b写入AGTMR1.TCK[2:0]位）。

22.4.9 Module-stop function

可以使用模块停止控制寄存器D(MSTPCRD)和模块停止控制来禁用或启用AGT操作
寄存器E(MSTPCRE)。AGT模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式

22.4.10 切换源时钟时

当通过改变SCKSCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。因此，当使用AGTIO、AGTEE或两者输入作为外部事件输入时，不应切换时钟源。如果在使用外部事件输入时切换时钟源，请将输入脉冲宽度延长4个切换源时钟周期的时钟周期。

23. Realtime Clock (RTC)

23.1 Overview

The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

The sub-clock oscillator or LOCO can be selected as the count source of the time counters. The RTC uses a 128-Hz clock acquired by dividing the count source by a prescaler. Year, month, date, day-of-week, a.m. /p.m. (in 12-hour mode), hour, minute, second, or 32-bit binary is counted by 1/128 second.

Table 23.1 lists the RTC specifications, Figure 23.1 shows a block diagram, and Table 23.2 lists the I/O pins.

Table 23.1 RTC specifications

Parameter	Specifications
Count mode	Calendar count mode/binary count mode
Count source*1	Sub-clock (XCIN) or LOCO
Clock and calendar functions	• Calendar count mode – Year, month, date, day of week, hour, minute, second are counted, BCD display – 12 hours/24 hours mode switching function – 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute) – Automatic adjustment function for leap years • Binary count mode – Count seconds in 32 bits, binary display • Shared by both modes – Start/stop function – The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz) – Clock error correction function – Clock (1-Hz/64-Hz) output
Interrupts	• Alarm interrupt (RTC_ALM) – As an alarm interrupt condition, selectable for comparison with the following: – Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected – Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (RTC_PRD) – 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (RTC_CUP) – An interrupt is generated at either of the following conditions: • When a carry from the 64-Hz counter to the second counter is generated. • When the 64-Hz counter is changed and the R64CNT register is read at the same time. (32-KHz count mode is only for 64-Hz counter reading) • Return from Software Standby or Deep Software Standby mode mode can be performed by an alarm interrupt or periodic interrupt
Time capture function	• Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or the 32-bit binary counter value is captured. • Interrupt can be generated when the edge of the time capture event input is detected. The time capture event input pin and IRQ are shared.
Event link function	Periodic event output (RTC_PRD)
TrustZone filter	Security attribution can be set

Note 1. The frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source should be satisfied.

23. 实时时钟(RTC)

23.1 Overview

实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。

可以选择子时钟振荡器或LOCO作为时间计数器的计数源。RTC使用一个128-Hz时钟，通过预分频器将计数源分频获得。年、月、日、星期、上午、下午（在12小时模式下）时、分、秒或32位二进制按1128秒计数。

表23.1列出了RTC规格，图23.1显示了框图，表23.2列出了IO引脚。

Table 23.1 RTC specifications

Parameter	Specifications
计数模式	日历计数模式二进制计数模式
计数来源*1	副时钟(XCIN)或LOCO
时钟和日历功能	• 日历计数模式 – 年、月、日、星期、时、分、秒计数，BCD显示 – 12小时24小时模式切换功能 – 30秒调整功能（小于30的数字向下取整为00秒，大于等于30秒向上取整为1分钟） – 闰年自动调整功能 • 二进制计数模式 – 以32位计算秒数，二进制显示 • 两种模式共享 – Start/stop function – 亚秒数字以二进制单位显示（1Hz、2Hz、4Hz、8Hz、16Hz、32Hz或64Hz） – 时钟纠错功能 – 时钟(1-Hz64-Hz)输出
Interrupts	• 闹钟中断(RTC_ALM) – 作为报警中断条件，可选择用于与以下比较： – 日历计数模式：可选择年、月、日、星期、小时、分钟或秒 – 二进制计数方式：32位二进制计数器的每一位 • 周期性中断(RTC_PRD) – 可以选择2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒作为中断周期。 • 进位中断(RTC_CUP) – 在以下任一情况下都会产生中断： • 当产生从64-Hz计数器到第二个计数器的进位时。 • 当64-Hz计数器改变并同时读取R64CNT寄存器时。（32-KHz计数模式仅适用于64-Hz计数器读数） • 从软件待机或深度软件待机模式模式中返回可以通过警报中断或周期性中断来执行
时间捕捉功能	• 当检测到时间捕捉事件输入引脚的边沿时，可以捕捉时间。对于每个事件输入，都会捕获月、日、小时、分钟和秒，或者捕获32位二进制计数器值。 • 当检测到时间捕捉事件输入的边沿时可以产生中断。时间捕捉事件输入引脚和IRQ是共享的。
事件链接功能	周期性事件输出(RTC_PRD)
TrustZone filter	可设置安全属性

注1.外围模块时钟（PCLKB）的频率≥计数源的频率应满足。

RA生态工作室

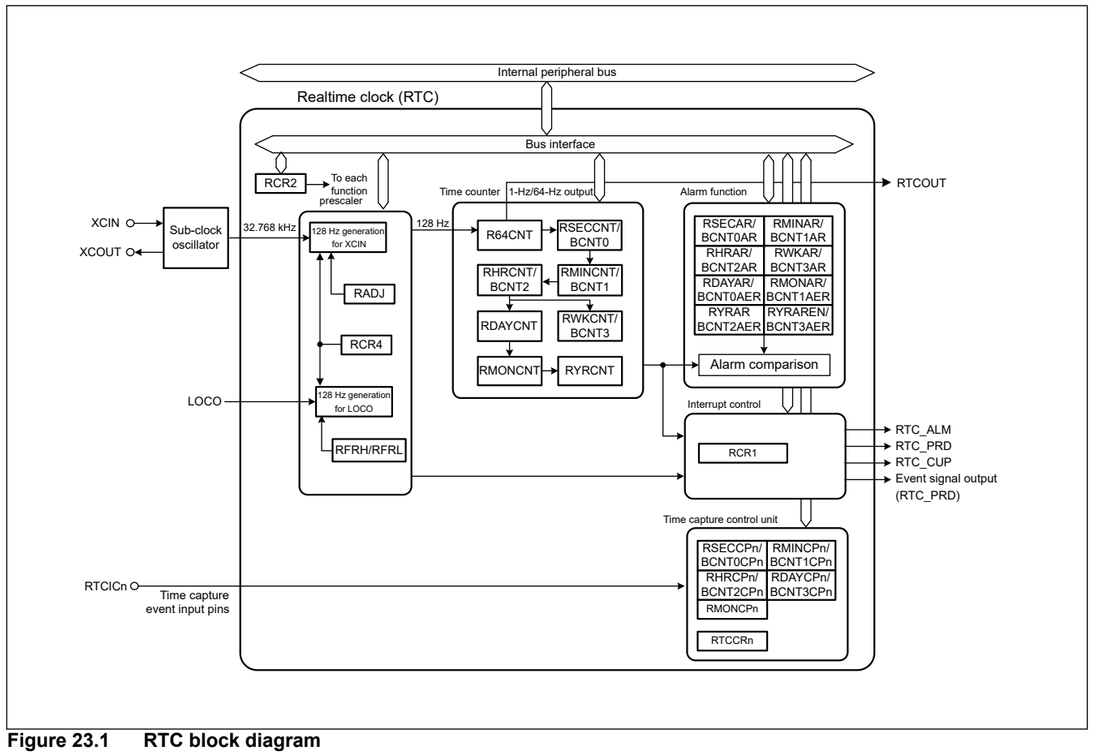


Figure 23.1 RTC block diagram

Table 23.2 RTC I/O pins

Pin name	I/O	Description
XCIN	Input	Connect a 32.768-kHz crystal to these pins
XCOUT	Output	
RTCOUT	Output	This pin is used to output a 1-Hz/64-Hz waveform, but not in Deep Software Standby mode
RTCICn (n = 0 to 2)	Input	Time capture event input pins RTCICn can be controlled by the VBTICTLR register. For more information, see section 11, Battery Backup Function and section 19, I/O Ports.

23.2 Register Descriptions

Write or read from the RTC registers as described in section 23.6.5. Notes on Writing to and Reading from Registers.

If the value in an RTC register after a reset is given as x (undefined bits) in the list, it is not initialized by a reset. When RTC enters the reset state or a low power state during counting operations, for example, while the RCR2.START bit is 1, the year, month, day of the week, date, hours, minutes, seconds, and 64-Hz counters continue to operate.

Note: A reset generated while writing to a register might destroy the register value. In addition, do not allow the MCU to enter Software Standby or Deep Software Standby mode immediately after setting any of these registers. For details, see section 23.6.4. Transitions to Low Power Modes after Setting Registers.

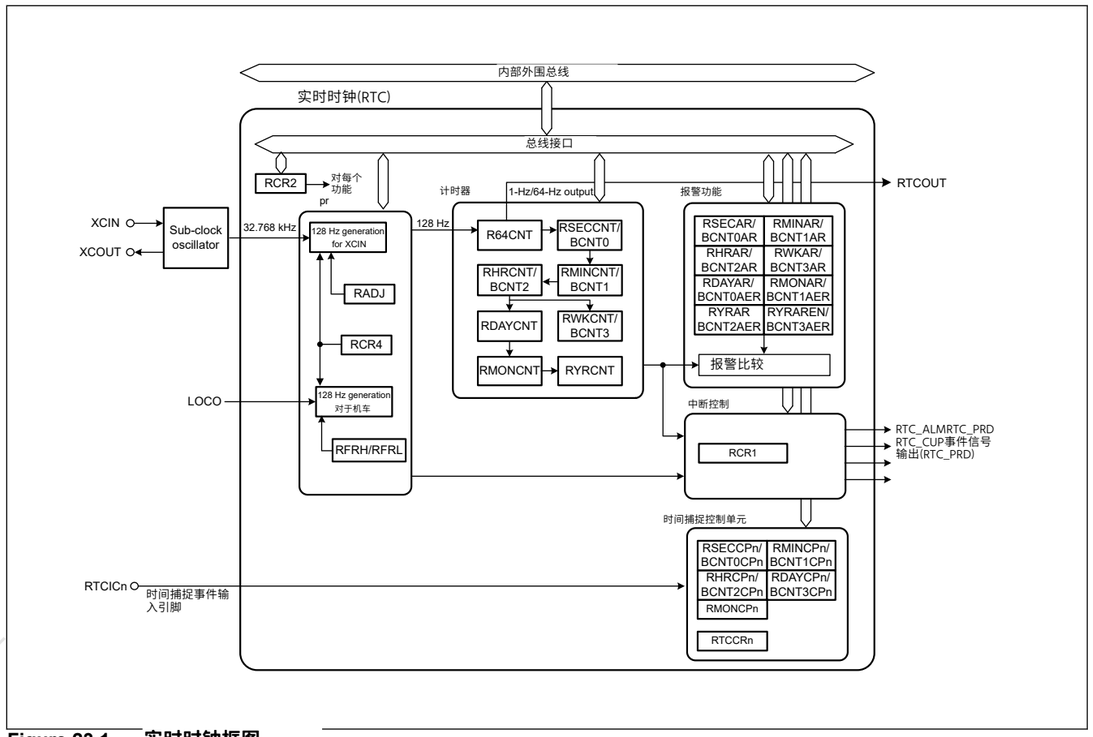


Figure 23.1 实时时钟框图

Table 23.2 RTC I/O pins

引脚名称	I/O	Description
XCIN	Input	将32.768kHz晶振连接到这些引脚
XCOUT	Output	
RTCOUT	Output	此引脚用于输出1-Hz64-Hz波形，但在DeepSoftware中不使用待机模式
RTCICn (n = 0 to 2)	Input	时间捕捉事件输入引脚 RTCICn可由VBTICTLR寄存器控制。有关详细信息，请参阅第11节，电池备份功能和第19节，IO端口。

23.2 注册说明

如第23.6.5节所述，从RTC寄存器写入或读取。关于写入和读取寄存器的注意事项。

如果复位后RTC寄存器中的值在列表中以x（未定义位）的形式给出，则它不会被复位初始化。当RTC在计数操作期间进入复位状态或低功耗状态时，例如，当RCR2.START位为1时，年、月、星期、日期、小时、分钟、秒和64-Hz计数器继续经营。

Note: 写入寄存器时产生的复位可能会破坏寄存器值。此外，不要让MCU在设置任何这些寄存器后立即进入软件待机或深度软件待机模式。详见23.6.4节。设置寄存器后转换到低功耗模式。

23.2.1 R64CNT : 64-Hz Counter

Base address: RTC = 0x4008_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
Value after reset:	0	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
0	F64HZ	64-Hz Flag This bit indicates the 64-Hz state of the sub-second digit.	R
1	F32HZ	32-Hz Flag This bit indicates the 32-Hz state of the sub-second digit.	R
2	F16HZ	16-Hz Flag This bit indicates the 16-Hz state of the sub-second digit.	R
3	F8HZ	8-Hz Flag This bit indicates the 8-Hz state of the sub-second digit.	R
4	F4HZ	4-Hz Flag This bit indicates the 4-Hz state of the sub-second digit.	R
5	F2HZ	2-Hz Flag This bit indicates the 2-Hz state of the sub-second digit.	R
6	F1HZ	1-Hz Flag This bit indicates the 1-Hz state of the sub-second digit.	R
7	—	This bit is read as 0.	R

The R64CNT counter is used in both calendar count mode and binary count mode The 64-Hz counter (R64CNT) generates the period for a second by counting up periods of the 128-Hz clock. The state in the sub-second range can be confirmed by reading this counter.

This counter is set to 0x00 by an RTC software reset or an execution of a 30-second adjustment. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.2 RSECCNT : Second Counter (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1-Second Count Counts from 0 to 9 every second. When a carry is generated, 1 is added to the tens place.	R/W
6:4	SEC10[2:0]	10-Second Count Counts from 0 to 5 for 60-second counting.	R/W
7	—	The read value is undefined. The write value should be 0.	R/W

The RSECCNT counter sets and counts the BCD-coded second value. It counts the carries generated once per second in the 64-Hz counter.

The setting range is decimal 00 to 59. The RTC does not operate normally if any other value is set. Before writing to this register, you must stop the count operation using the START bit in RCR2.

23.2.1 R64CNT : 64-Hz Counter

Base address: RTC = 0x4008_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
重置后的值:	0	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
0	F64HZ	64-Hz标志该位指示亚秒数字的64-Hz状态。	R
1	F32HZ	32-Hz标志该位指示亚秒数字的32-Hz状态。	R
2	F16HZ	16-Hz标志该位指示亚秒数位的16-Hz状态。	R
3	F8HZ	8-Hz标志该位指示亚秒数位的8-Hz状态。	R
4	F4HZ	4-Hz标志该位指示亚秒数位的4-Hz状态。	R
5	F2HZ	2-Hz标志该位指示亚秒数字的2-Hz状态。	R
6	F1HZ	1-Hz标志该位指示亚秒数字的1-Hz状态。	R
7	—	该位读为0。	R

R64CNT计数器用于日历计数模式和二进制计数模式。64-Hz计数器(R64CNT)通过向上计数128-Hz时钟的周期来产生一秒的周期。亚秒范围内的状态可以通过读取该计数器来确认。

该计数器通过RTC软件复位或执行30秒调整设置为0x00。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.2 RSECCNT:第二个计数器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SEC10[2:0]			SEC1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1-SecondCount每秒从0计数到9。产生进位时，十位加1。	R/W
6:4	SEC10[2:0]	10秒计数从0计数到5以进行60秒计数。	R/W
7	—	读取值未定义。写入值应为0。	R/W

RSECCNT计数器设置并计算BCD编码的第二个值。它对64-Hz计数器中每秒生成一次的进位进行计数。

设置范围为十进制00到59。如果设置任何其他值，RTC将无法正常工作。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。

To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.3 RMINCNT : Minute Counter (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1-Minute Count Counts from 0 to 9 every minute. When a carry is generated, 1 is added to the tens place.	R/W
6:4	MIN10[2:0]	10-Minute Count Counts from 0 to 5 for 60-minute counting.	R/W
7	—	The read value is undefined. The write value should be 0.	R/W

The RMINCNT counter sets and counts the BCD-coded minute value. It counts the carries generated once every minute in the second counter.

A value from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.4 RHRCNT : Hour Counter (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1-Hour Count Counts from 0 to 9 once per hour. When a carry is generated, 1 is added to the tens place.	R/W
5:4	HR10[1:0]	10-Hour Count Counts from 0 to 2 once per carry from the ones place.	R/W
6	PM	AM/PM select for time counter setting. 0: AM 1: PM	R/W
7	—	The read value is undefined. The write value should be 0.	R/W

The RHRCNT counter sets and counts the BCD-coded hour value. It counts the carries generated once per hour in the minute counter. The specifiable time differs based on the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 – from 00 to 11 (in BCD).
- When the RCR2.HR24 bit is 1 – from 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. The PM bit is only enabled when the RCR2.HR24 bit is 0.

Otherwise, the setting in the PM bit has no effect. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.3 RMINCNT：分钟计数器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1分钟计数每分钟从0计数到9。产生进位时，十位加1。	R/W
6:4	MIN10[2:0]	10分钟计数从0到5计数60分钟。	R/W
7	—	读取值未定义。写入值应为0。	R/W

RMINCNT计数器设置并计算BCD编码的分钟值。它对第二个计数器中每分钟产生一次的进位进行计数。

可以指定从00到59的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.4 RHRCNT：小时计数器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1小时计数每小时从0计数到9次。产生进位时，十位加1。	R/W
5:4	HR10[1:0]	10小时计数从0到2计数一次，每次从一个位置进行。	R/W
6	PM	AMPM选择时间计数器设置。 0: AM 1: PM	R/W
7	—	读取值未定义。写入值应为0。	R/W

RHRCNT计数器设置并计算BCD编码的小时值。它在分钟计数器中计算每小时生成一次的进位。可指定的时间因小时模式位(RCR2.HR24)中的设置而异：

- 当RCR2.HR24位为0时——从00到11（以BCD表示）。
- 当RCR2.HR24位为1时 从00到23（以BCD表示）。

如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。PM位仅在RCR2.HR24位为0时启用。

否则，PM位中的设置无效。要读取此计数器，请按照第23.3.5节中的程序进行。阅读64-Hz计数器和时间。

23.2.5 RWKCNT : Day-of-Week Counter (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Counting 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited	R/W
7:3	—	The read values are undefined. The write value should be 0.	R/W

The RWKCNT counter sets and counts in the coded day-of-week value. It counts the carries generated once per day in the hour counter. A value from 0 through 6 can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.6 BCNTn : Binary Counter n (n = 0 to 3) (in Binary Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNT[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNT[7:0]	Binary Counter	R/W

BCNTn is a read/write 8-bit register to access BCNT[31:0] that is a 32-bit binary counter. BCNT3 is assigned to the BCNT[31:24] bits, BCNT2 is assigned to the BCNT[23:16] bits, BCNT1 is assigned to the BCNT[15:8] bits, and BCNT0 is assigned to the BCNT[7:0] bits. BCNTn performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.7 RDAYCNT : Day Counter

Base address: RTC = 0x4008_3000

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	0	0	x	x	x	x	x	x

23.2.5 RWKCNT：星期计数器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Counting 000：星期日001：星期一010：星期二011：星期三100：星期四101：星期五110：星期六111：禁止设置	R/W
7:3	—	读取的值未定义。写入值应为0。	R/W

RWKCNT计数器在编码的星期值中设置和计数。它计算小时计数器中每天生成一次的进位。可以指定从0到6的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.6 BCNTn：二进制计数器n（n=0到3）（在二进制计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x02 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNT[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNT[7:0]	二进制计数器	R/W

BCNTn是一个读写8位寄存器，用于访问BCNT[31:0]，它是一个32位二进制计数器。BCNT3分配给BCNT[31:24]位，BCNT2分配给BCNT[23:16]位，BCNT1分配给BCNT[15:8]位，BCNT0分配给BCNT[7:0]]位。BCNTn通过64-Hz计数器每秒生成的进位执行计数操作。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.7 RDAYCNT:日计数器

Base address: RTC = 0x4008_3000

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	0	0	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1-Day Count Counts from 0 to 9 once per day. When a carry is generated, 1 is added to the tens place.	R/W
5:4	DATE10[1:0]	10-Day Count Counts from 0 to 3 once per carry from the ones place.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

The RDAYCNT counter is used in calendar count mode to set and count the BCD-coded date value. It counts the carries generated once per day in the hour counter. The count operation depends on the month and whether the year is a leap year. Leap years are determined according to whether the year counter (RYRCNT) value is divisible by 400, 100, and 4.

A value from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. When specifying a value, the range of specifiable days depends on the month and whether the year is a leap year. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.8 RMONCNT : Month Counter

Base address: RTC = 0x4008_3000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MON10	MON1[3:0]			
Value after reset:	0	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1-Month Count Counts from 0 to 9 once per month. When a carry is generated, 1 is added to the tens place.	R/W
4	MON10	10-Month Count Counts from 0 to 1 once per carry from the ones place.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The RMONCNT counter is used in calendar count mode to set and count the BCD-coded month value. It counts the carries generated once per month in the date counter.

A value from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.9 RYRCNT : Year Counter

Base address: RTC = 0x4008_3000

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	1-Year Count Counts from 0 to 9 once per year. When a carry is generated, 1 is added to the tens place.	R/W

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1天计数每天从0计数到9次。产生进位时，十位加1。	R/W
5:4	DATE10[1:0]	10天计数从0到3计数一次，每次从一个位置进行。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

RDAYCNT计数器用于日历计数模式以设置和计数BCD编码的日期值。它计算小时计数器中每天生成一次的进位。计数操作取决于月份以及年份是否为闰年。闰年根据年份计数器(RYRCNT)值是否可被400、100和4整除来确定。

可以指定从01到31的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。指定值时，可指定天数的范围取决于月份以及年份是否为闰年。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.8 RMONCNT:月计数器

Base address: RTC = 0x4008_3000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MON10	MON1[3:0]			
重置后的值:	0	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1个月计数每月一次从0计数到9。产生进位时，十位加1。	R/W
4	MON10	10-MonthCount从0到1计数一次，每次进位。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

RMONCNT计数器用于日历计数模式以设置和计数BCD编码的月份值。它在日期计数器中计算每月生成一次的进位。

可以指定从01到12的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.9 RYRCNT:年计数器

Base address: RTC = 0x4008_3000

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	1年计数每年从0计数到9次。产生进位时，十位加1。	R/W

Bit	Symbol	Function	R/W
7:4	YR10[3:0]	10-Year Count Counts from 0 to 9 once per carry from ones place. When a carry is generated in the tens place, 1 is added to the hundreds place.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

The RYRCNT counter is used in calendar count mode to set and count the BCD-coded year value. It counts the carries generated once per year in the month counter.

A value from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.

23.2.10 RSECAR : Second Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1 Second Value for the ones place of seconds.	R/W
6:4	SEC10[2:0]	10 Seconds Value for the tens place of seconds.	R/W
7	ENB	ENB 0: Do not compare register value with RSECCNT counter value 1: Compare register value with RSECCNT counter value	R/W

RSECAR is an alarm register associated with the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, the RSECAR value is compared with the RSECCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RSECAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

Bit	Symbol	Function	R/W
7:4	YR10[3:0]	10-YearCount从0到9计数一次，每次从一个位置进位。当十位产生进位时，百位加1。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

RYRCNT计数器在日历计数模式下用于设置和计数BCD编码的年份值。它计算月份计数器中每年生成一次的进位。

可以指定从00到99（BCD格式）的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第23.3.5节中的程序进行。读取64-Hz计数器和时间。

23.2.10 RSCAR：第二个警报寄存器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	SEC10[2:0]			SEC1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1秒个位的秒值。	R/W
6:4	SEC10[2:0]	10秒十位秒的值。	R/W
7	ENB	ENB 0：不将寄存器值与RSECCNT计数器值进行比较1：将寄存器值与RSECCNT计数器值进行比较	R/W

RSCAR是与BCD编码的第二个计数器RSECCNT相关的警报寄存器。当ENB位设置为1时，RSCAR值与RSECCNT值进行比较。从下面的报警寄存器中，只有那些选择与设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RSCAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

23.2.11 RMINAR : Minute Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1 Minute Value for the ones place of minutes.	R/W
6:4	MIN10[2:0]	10 Minutes Value for the tens place of minutes.	R/W
7	ENB	ENB 0: Do not compare register value with RMINCNT counter value 1: Compare register value with RMINCNT counter value	R/W

RMINAR is an alarm register associated with the BCD-coded minute counter RMINCNT. When the ENB bit is set to 1, the RMINAR value is compared with the RMINCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RMINAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

23.2.12 RHRAR : Hour Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1 Hour Value for the ones place of hours.	R/W
5:4	HR10[1:0]	10 Hours Value for the tens place of hours.	R/W
6	PM	AM/PM select for alarm setting. 0: AM 1: PM	R/W

23.2.11 RMINAR：分钟报警寄存器（日历计数模式）

Base address: RTC = 0x4008_3000

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	分钟的个位的1分钟值。	R/W
6:4	MIN10[2:0]	十位分钟的10分钟值。	R/W
7	ENB	ENB 0：不将寄存器值与RMINCNT计数器值进行比较1：将寄存器值与RMINCNT计数器值进行比较	R/W

RMINAR是一个与BCD编码的分钟计数器RMINCNT相关的报警寄存器。当ENB位设置为1时，RMINAR值与RMINCNT值进行比较。从下面的报警寄存器中，只有那些选择与设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RMINAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

23.2.12 RHRAR：小时报警寄存器（日历计数模式）

Base address: RTC = 0x4008_3000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1小时值的个数。	R/W
5:4	HR10[1:0]	十位小时的10小时值。	R/W
6	PM	AMPM选择闹钟设置。 0: AM 1: PM	R/W

Bit	Symbol	Function	R/W
7	ENB	ENB 0: Do not compare register value with RHRCNT counter value 1: Compare register value with RHRCNT counter value	R/W

RHRAR is an alarm register associated with the BCD-coded hour counter RHRCNT. When the ENB bit is set to 1, the RHRAR value is compared with the RHRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 – From 00 to 11 (in BCD).
- When the RCR2.HR24 bit is 1 – From 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. When the RCR2.HR24 bit is 0, you must set the PM bit. When the RCR2.HR24 bit is 1, the setting in the PM bit has no effect. This register is set to 0x00 by an RTC software reset.

23.2.13 RWKAR : Day-of-Week Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x16

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Setting 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited	R/W
6:3	—	The read values are undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with RWKCNT counter value 1: Compare register value with RWKCNT counter value	R/W

RWKAR is an alarm register associated with the coded day-of-week counter RWKCNT. When the ENB bit is set to 1, the RWKAR value is compared with the RWKCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR

Bit	Symbol	Function	R/W
7	ENB	ENB 0：不将寄存器值与RHRCNT计数器值进行比较1：将寄存器值与RHRCNT计数器值进行比较	R/W

RHRAR是一个与BCD编码的小时计数器RHRCNT相关的警报寄存器。当ENB位设置为1时，RHRAR值与RHRCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可指定的时间根据小时模式位(RCR2.HR24)中的设置而有所不同：

●当RCR2.HR24位为0时 从00到11（以BCD表示）。

●当RCR2.HR24位为1时 从00到23（BCD格式）。

如果指定的值超出此范围，则RTC将无法正确运行。当RCR2.HR24位为0时，必须设置PM位。当RCR2.HR24位为1时，PM位中的设置无效。该寄存器通过RTC软件复位设置为0x00。

23.2.13 RWKAR：星期报警寄存器（日历计数模式）

Base address: RTC = 0x4008_3000

Offset address: 0x16

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
2:0	DAYW[2:0]	Day-of-Week Setting 000：星期日001：星期一010：星期二011：星期三100：星期四101：星期五110：星期六111：禁止设置	R/W
6:3	—	读取的值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RWKCNT计数器值进行比较1：将寄存器值与RWKCNT计数器值进行比较	R/W

RWKAR是与编码的星期计数器RWKCNT相关的警报寄存器。当ENB位设置为1时，RWKAR值与RWKCNT值进行比较。从下面的报警寄存器中，只有那些选择与设置为1的ENB位与相关计数器进行比较：

- RSECAR

- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RWKAR values from 0 through 6 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

23.2.14 BCNTnAR : Binary Counter n Alarm Register (n = 0 to 3) (in Binary Count Mode)

Base address: RTC = 0x4008_3000
Offset address: 0x10 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNTAR							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNTAR	Alarm register associated with the 32-bit binary counter	R/W

BCNTnAR is a read/write alarm register associated with the 32-bit binary counter. BCNT3AR is assigned to the BCNTAR[31:24] bits, BCNT2AR is assigned to the BCNTAR[23:16] bits, BCNT1AR is assigned to the BCNTAR[15:8] bits, and BCNT0AR is assigned to the BCNTAR[7:0]. This register is set to 0x00 by an RTC software reset.

23.2.15 RDAYAR : Date Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000
Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1 Day Value for the ones place of days.	R/W
5:4	DATE10[1:0]	10 Days Value for the tens place of days.	R/W
6	—	The read value is undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with RDAYCNT counter value 1: Compare register value with RDAYCNT counter value	R/W

RDAYAR is an alarm register associated with the BCD-coded date counter RDAYCNT. When the ENB bit is set to 1, the RDAYAR value is compared with the RDAYCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR

- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从0到6（以BCD表示）的RWKAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

23.2.14 BCNTnAR：二进制计数器n报警寄存器（n=0到3）（在二进制计数模式下）

Base address: RTC = 0x4008_3000
Offset address: 0x10 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCNTAR							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	BCNTAR	与32位二进制计数器关联的报警寄存器	R/W

BCNTnAR是一个与32位二进制计数器相关的读写报警寄存器。BCNT3AR分配给BCNTAR[31:24]位，BCNT2AR分配给BCNTAR[23:16]位，BCNT1AR分配给BCNTAR[15:8]位，BCNT0AR分配给BCNTAR[7:0]。该寄存器通过RTC软件复位设置为0x00。

23.2.15 RDAYAR:日期报警寄存器（日历计数模式）

Base address: RTC = 0x4008_3000
Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1天的个位数的值。	R/W
5:4	DATE10[1:0]	10天十位天的价值。	R/W
6	—	读取值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RDAYCNT计数器值进行比较1：将寄存器值与RDAYCNT计数器值进行比较	R/W

RDAYAR是一个与BCD编码日期计数器RDAYCNT相关的报警寄存器。当ENB位设置为1时，将RDAYAR值与RDAYCNT值进行比较。从下面的报警寄存器中，只有那些选择与
设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR

- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RDAYAR values from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

23.2.16 RMONAR : Month Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x1A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1 Month Value for the ones place of months.	R/W
4	MON10	10 Months Value for the tens place of months.	R/W
6:5	—	The read values are undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with RMONCNT counter value 1: Compare register value with RMONCNT counter value	R/W

RMONAR is an alarm register associated with the BCD-coded month counter RMONCNT. When the ENB bit is set to 1, the RMONAR value is compared with the RMONCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The RMONAR values from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x00 by an RTC software reset.

23.2.17 RYRAR : Year Alarm Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到31（以BCD表示）的RDAYAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

23.2.16 RMONAR：月报警寄存器（日历计数模式）

Base address: RTC = 0x4008_3000

Offset address: 0x1A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	MON10	MON1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1月份的个位数的月份值。	R/W
4	MON10	10个月十位月份的值。	R/W
6:5	—	读取的值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RMONCNT计数器值进行比较1：将寄存器值与RMONCNT计数器值进行比较	R/W

RMONAR是一个与BCD编码月份计数器RMONCNT相关的报警寄存器。当ENB位设置为1时，RMONAR值与RMONCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到12（以BCD表示）的RMONAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x00。

23.2.17 RYRAR：年警报寄存器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	1 Year Value for the ones place of years.	R/W
7:4	YR10[3:0]	10 Years Value for the tens place of years.	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

RYRAR is an alarm register associated with the BCD-coded year counter RYRCNT. The RYRAR values from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is set to 0x0000 by an RTC software reset.

23.2.18 RYRAREN : Year Alarm Enable Register (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
6:0	—	The read values are undefined. The write value should be 0.	R/W
7	ENB	ENB 0: Do not compare register value with the RYRCNT counter value 1: Compare register value with the RYRCNT counter value	R/W

When the ENB bit in the RYRAREN register is set to 1, the RYRAR value is compared with the RYRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

23.2.19 BCNTnAER : Binary Counter n Alarm Enable Register (n = 0, 1) (in Binary Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x18 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	YR1[3:0]	年的个位的1年值。	R/W
7:4	YR10[3:0]	10年十位年份的值。	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

RYRAR是一个与BCD编码年份计数器RYRCNT相关联的警报寄存器。可以指定从00到99（BCD格式）的RYRAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位设置为0x0000。

23.2.18 RYRAREN:年警报启用寄存器（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB	—	—	—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
6:0	—	读取的值未定义。写入值应为0。	R/W
7	ENB	ENB 0：不将寄存器值与RYRCNT计数器值进行比较1：将寄存器值与RYRCNT计数器值进行比较	R/W

当RYRAREN寄存器中的ENB位设置为1时，RYRAR值与RYRCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。该寄存器通过RTC软件复位设置为0x00。

23.2.19 BCNTnAER:二进制计数器n报警使能寄存器(n=0 1)(以二进制计数 Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x18 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	Setting the alarm enable associated with the 32-bit binary counter	R/W

BCNTnAER is a read/write register for setting the alarm enable (BCNTAER) associated with the 32-bit binary counter. BCNT3AER is assigned to the BCNTAER.ENB[31:24] bits, BCNT2AER register is assigned to the BCNTAER.ENB[23:16] bits, BCNT1AER is assigned to the BCNTAER.ENB[15:8] bits, and BCNT0AER is assigned to the BCNTAER.ENB[7:0] bits. The binary counter (BCNT[31:0]) associated with the BCNTAER.ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

23.2.20 BCNT2AER : Binary Counter 2 Alarm Enable Register (in Binary Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ENB[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	Setting the alarm enable associated with the 32-bit binary counter	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

BCNT2AER is a read/write register for setting the alarm enable (BCNTAER) associated with the 32-bit binary counter. BCNT3AER is assigned to the BCNTAER.ENB[31:24] bits, BCNT2AER register is assigned to the BCNTAER.ENB[23:16] bits, BCNT1AER is assigned to the BCNTAER.ENB[15:8] bits, and BCNT0AER is assigned to the BCNTAER.ENB[7:0] bits. The binary counter (BCNT[31:0]) associated with the BCNTAER.ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

23.2.21 BCNT3AER : Binary Counter 3 Alarm Enable Register (in Binary Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	Setting the alarm enable associated with the 32-bit binary counter	R/W

BCNT3AER is a read/write register for setting the alarm enable (BCNTAER) associated with the 32-bit binary counter. BCNT3AER is assigned to the BCNTAER.ENB[31:24] bits, BCNT2AER register is assigned to the BCNTAER.ENB[23:16] bits, BCNT1AER is assigned to the BCNTAER.ENB[15:8] bits, and BCNT0AER is assigned to the BCNTAER.ENB[7:0] bits. The binary counter (BCNT[31:0]) associated with the BCNTAER.ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is set to 0x00 by an RTC software reset.

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	设置与32位二进制计数器关联的警报启用	R/W

BCNTnAER是一个读写寄存器，用于设置与32位二进制计数器相关的报警使能(BCNTAER)。BCNT3AER分配给BCNTAER.ENB[31:24]位，BCNT2AER寄存器分配给BCNTAER.ENB[23:16]位，BCNT1AER分配给BCNTAER.ENB[15:8]位，BCNT0AER分配给BCNTAER.ENB[7:0]位。与设置为1的BCNTAER.ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR)进行比较，当全部匹配时，与RTC_ALM中断设置为1。该寄存器通过RTC软件复位设置为0x00。

23.2.20 BCNT2AER：二进制计数器2报警使能寄存器（在二进制计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	ENB[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	设置与32位二进制计数器关联的警报启用	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

BCNT2AER是一个读写寄存器，用于设置与32位二进制计数器相关的报警使能(BCNTAER)。BCNT3AER分配给BCNTAER.ENB[31:24]位，BCNT2AER寄存器分配给BCNTAER.ENB[23:16]位，BCNT1AER分配给BCNTAER.ENB[15:8]位，BCNT0AER分配给BCNTAER.ENB[7:0]位。与设置为1的BCNTAER.ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR)进行比较，当全部匹配时，与RTC_ALM中断设置为1。该寄存器通过RTC软件复位设置为0x00。

23.2.21 BCNT3AER：二进制计数器3报警使能寄存器（在二进制计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x1E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ENB[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	ENB[7:0]	设置与32位二进制计数器关联的警报启用	R/W

BCNT3AER是一个读写寄存器，用于设置与32位二进制计数器相关的报警使能(BCNTAER)。BCNT3AER分配给BCNTAER.ENB[31:24]位，BCNT2AER寄存器分配给BCNTAER.ENB[23:16]位，BCNT1AER分配给BCNTAER.ENB[15:8]位，BCNT0AER分配给BCNTAER.ENB[7:0]位。与设置为1的BCNTAER.ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR)进行比较，当全部匹配时，与RTC_ALM中断设置为1。该寄存器通过RTC软件复位设置为0x00。

23.2.22 RCR1 : RTC Control Register 1

Base address: RTC = 0x4008_3000

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PES[3:0]				RTCOS	PIE	CIE	AIE
Value after reset:	x	x	x	x	0	x	0	x

Bit	Symbol	Function	R/W
0	AIE	Alarm Interrupt Enable 0: Disable alarm interrupt requests 1: Enable alarm interrupt requests	R/W
1	CIE	Carry Interrupt Enable 0: Disable carry interrupt requests 1: Enable carry interrupt requests	R/W
2	PIE	Periodic Interrupt Enable 0: Disable periodic interrupt requests 1: Enable periodic interrupt requests	R/W
3	RTCOS	RTCOUT Output Select 0: Outputs 1 Hz on RTCOUT 1: Outputs 64 Hz RTCOUT	R/W
7:4	PES[3:0]	Periodic Interrupt Select 0x6: Generate periodic interrupt every 1/256 second*1 0x7: Generate periodic interrupt every 1/128 second 0x8: Generate periodic interrupt every 1/64 second 0x9: Generate periodic interrupt every 1/32 second 0xA: Generate periodic interrupt every 1/16 second 0xB: Generate periodic interrupt every 1/8 second 0xC: Generate periodic interrupt every 1/4 second 0xD: Generate periodic interrupt every 1/2 second 0xE: Generate periodic interrupt every 1 second 0xF: Generate periodic interrupt every 2 seconds Others: Do not generate periodic interrupts	R/W

Note 1. When LOCO is selected (RCR4.RCKSEL = 1) while PES[3:0] = 0x6, a periodic interrupt is generated every 1/128 second.

The RCR1 register is used in both calendar count mode and binary count mode. Bits AIE, PIE, and PES[3:0] are updated synchronously with the count source. When the RCR1 register is modified, check that all the bits are updated before proceeding.

AIE bit (Alarm Interrupt Enable)

The AIE bit enables or disables alarm interrupt requests.

If the times indicated in the counters and alarm settings match in Deep Software Standby mode, the MCU returns from the regardless of the AIE bit value.

CIE bit (Carry Interrupt Enable)

The CIE bit enables or disables interrupt requests when a carry to the RSECCNT/BCNT0 register occurs, or when a carry to the 64-Hz counter (R64CNT) occurs while reading the 64-Hz counter.

PIE bit (Periodic Interrupt Enable)

The PIE bit enables or disabled a periodic interrupt.

If the periods indicated in the counters and PES[3:0] settings match in Deep Software Standby mode, the MCU returns from the regardless of the PIE bit value.

23.2.22 RCR1:RTC控制寄存器1

Base address: RTC = 0x4008_3000

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PES[3:0]				RTCOS	PIE	CIE	AIE
重置后的值:	x	x	x	x	0	x	0	x

Bit	Symbol	Function	R/W
0	AIE	报警中断使能 0：禁用报警中断请求1：启用报警中断请求	R/W
1	CIE	进位中断使能 0：禁止进位中断请求1：使能进位中断请求	R/W
2	PIE	周期性中断使能 0：禁用周期性中断请求1：启用周期性中断请求	R/W
3	RTCOS	RTCOUT输出选择 0：在RTCOUT上输出1Hz1：输出64HzRTCOUT	R/W
7:4	PES[3:0]	周期性中断选择 0x6：每1256秒产生周期性中断*1 0x7：每1128秒产生周期中断0x8：每164秒产生周期中断0x9：每132秒产生周期中断0xA：每116秒产生周期中断0xB：每18秒产生周期中断0xC：产生周期中断每14秒0xD：每12秒产生周期性中断0xE：每1秒产生周期性中断0xF：每2秒产生周期性中断 其他：不产生周期性中断	R/W

注意1.选择LOCO（RCR4.RCKSEL=1）时，PES[3：0]=0x6时，每1128秒都会生成周期性中断。

RCR1寄存器用于日历计数模式和二进制计数模式。AIE、PIE和PES[3:0]位与计数源同步更新。修改RCR1寄存器时，在继续之前检查所有位是否都已更新。

AIE位（报警中断允许）

AIE位启用或禁用警报中断请求。

如果计数器和警报设置中指示的时间在深度软件待机模式下匹配，则MCU从不考虑AIE位值返回。

CIE位（进位中断使能）

当发生对RSECCNTBCNT0寄存器的进位，或在读取64-Hz计数器时发生对64-Hz计数器(R64CNT)的进位时，CIE位启用或禁用中断请求。

PIE位（周期性中断使能）

PIE位启用或禁用周期性中断。

如果计数器中指示的周期和PES[3:0]设置在深度软件待机模式下匹配，则MCU将从无论PIE位值如何返回。

RA生态工作室

RTCOS bit (RTCOUT Output Select)

The RTCOS bit selects the RTCOUT output period. The RTCOS bit must be rewritten while the count operation is stopped (RCR2.START = 0) and the RTCOUT output is disabled (RCR2.RTCOE = 0). When RTCOUT is output to an external pin, the RCR2.RTCOE bit must be enabled.

PES[3:0] bits (Periodic Interrupt Select)

The PES[3:0] bits specify the period for the periodic interrupt. A periodic interrupt is generated with the period specified in these bits.

23.2.23 RCR2 : RTC Control Register 2 (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START	Start 0: Stop prescaler and time counter 1: Operate prescaler and time counter normally	R/W
1	RESET	RTC Software Reset 0: In writing: Invalid (writing 0 has no effect). In reading: Normal time operation in progress, or an RTC software reset has completed. 1: In writing: Initialize the prescaler and target registers for RTC software reset*1. In reading: RTC software reset in progress.	R/W
2	ADJ30	30-Second Adjustment 0: In writing: Invalid (writing 0 has no effect). In reading: Normal time operation in progress, or 30-second adjustment has completed. 1: In writing: Execute 30-second adjustment. In reading: 30-second adjustment in progress.	R/W
3	RTCOE	RTCOUT Output Enable 0: Disable RTCOUT output 1: Enable RTCOUT output	R/W
4	AADJE	Automatic Adjustment Enable*2*3 0: Disable automatic adjustment 1: Enable automatic adjustment	R/W
5	AADJP	Automatic Adjustment Period Select*2*3 0: The RADJ.ADJ[5:0] setting from the count value of the prescaler every minute. 1: The RADJ.ADJ[5:0] setting value is adjusted from the coun tvalue of the prescaler every 10 seconds.	R/W
6	HR24	Hours Mode*3 0: Operate RTC in 12-hour mode 1: Operate RTC in 24-hour mode	R/W
7	CNTMD	Count Mode Select*4 0: Calendar count mode 1: Binary count mode	R/W

Note 1. R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RTCCRn, RSECCPn, RMINCPn, RHRCPn, RDAYCPn, RMONCPn, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.
Note 3. When rewriting this bit, confirm that the value has been rewritten before performing the following processing. See section 23.6.5. Notes on Writing to and Reading from Registers for notes on register writing/reading.
Note 4. When rewriting this bit, confirm that the value has been rewritten before performing the following processing.

RTCOS位（RTCOUT输出选择）

RTCOS位选择RTCOUT输出周期。当计数操作停止(RCR2.START=0)并且RTCOUT输出被禁用(RCR2.RTCOE=0)时，必须重写RTCOS位。当RTCOUT输出到外部引脚时，必须使能RCR2.RTCOE位。

PES[3:0]位（周期性中断选择）

PES[3:0]位指定周期性中断的周期。以这些位中指定的周期生成周期性中断。

23.2.23 RCR2：RTC控制寄存器2（日历计数模式）

Base address: RTC = 0x4008_3000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
重置后的值：	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START	Start 0：停止预分频器和时间计数器1：正常运行预分频器和时间计数器	R/W
1	RESET	RTC软件复位 0：写入中：无效（写入0无效）。 读取中：正常时间操作正在进行，或RTC软件复位已完成。 1：书面：初始化RTC软件复位的预分频器和目标寄存器*1。读取中：RTC软件正在复位。	R/W
2	ADJ30	30-Second Adjustment 0：写入中：无效（写入0无效）。 读数中：正常时间操作正在进行，或30秒调整已完成。 1：书面：执行30秒调整。 阅读中：正在进行30秒调整。	R/W
3	RTCOE	RTCOUT输出使能 0：禁用RTCOUT输出1：启用RTCOUT输出	R/W
4	AADJE	自动调整启用*2*3 0：禁用自动调整1：启用自动调整	R/W
5	AADJP	自动调整周期选择*2*3 0：RADJ.ADJ[5:0]设置来自每分钟预分频器的计数值。1：RADJ.ADJ[5:0]设置值每10秒从预分频器的计数值调整一次。	R/W
6	HR24	小时模式*3 0：以12小时模式运行RTC1：以24小时模式运行RTC	R/W
7	CNTMD	计数模式选择*4 0：日历计数模式1：二进制计数模式	R/W

Note 1. R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RTCCRn, RSECCPn, RMINCPn, RHRCPn, RDAYCPn, RMONCPn, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
注意2.选择机车时，该位的设置被禁用。
注3.改写该位时，请确认该值已被改写，然后再进行以下处理。请参阅第23.6.5节。NotesonWritetoandReadingfromRegisters有关寄存器写入读取的说明。
注4.改写该位时，请确认该值已被改写，然后再进行以下处理。

RA生态工作室

The RCR2 register is related to hours mode, automatic adjustment function, enabling RTCOUT output, 30-second adjustment, RTC software reset, and controlling count operation.

START bit (Start)

The START bit stops or restarts the prescaler or time counter operation. This bit is updated in synchronization with the next cycle of the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software. When 1 is written to this bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. Check that this bit is 0 before proceeding.

ADJ30 bit (30-Second Adjustment)

The ADJ30 bit is for 30-second adjustment.

When 1 is written to the ADJ30 bit, the RSECCNT value of 30 seconds or less is rounded down to 00 second and the value of 30 seconds or more is rounded up to 1 minute.

The 30-second adjustment is performed in synchronization with the count source. When 1 is written to this bit, the ADJ30 bit is automatically set to 0 after the 30-second adjustment completes. If 1 is written to the ADJ30 bit, check that the bit is 0 before proceeding. When the 30-second adjustment is performed, the prescaler and R64CNT are also reset. The ADJ30 bit is set to 0 by an RTC software reset.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time.

When RTCOUT is to be output from an external pin, enable the RTCOE bit and set up the port control for the pin.

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit.

The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit.

The AADJP bit is set to 0 by an RTC software reset.

HR24 bit (Hours Mode)

The HR24 bit specifies whether the RTC operates in 12- or 24-hour mode.

Use the START bit to stop counting before changing the value of the HR24 bit. Do not stop counting (write 0 to the START bit) and change the value of the HR24 bit at the same time.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated in synchronization with the count source. However, the count mode switches only after the RTC software reset. (Bit switches before RTC reset, mode switches after RTC reset.)

For details on initial settings, see section 23.3.1. Outline of Initial Settings of Registers after Power On.

RCR2寄存器与小时模式、自动调整功能、启用RTCOUT输出、30秒调整、RTC软件复位和控制计数操作有关。

开始位（开始）

START位停止或重新启动预分频器或时间计数器操作。该位与计数源的下一个周期同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。当向该位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。在继续之前检查该位是否为0。

ADJ30 bit (30-Second Adjustment)

ADJ30位用于30秒调整。

向ADJ30位写入1时，30秒以下的RSECCNT值向下舍入为00秒，30秒以上的值向上舍入为1分钟。

30秒调整与计数源同步进行。向该位写入1时，30秒调整完成后ADJ30位自动设置为0。如果将1写入ADJ30位，请在继续之前检查该位是否为0。当执行30秒调整时，预分频器和R64CNT也被复位。RTC软件复位将ADJ30位设置为0。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。

当RTCOUT要从外部引脚输出时，使能RTCOE位并设置引脚的端口控制。

ADJE位（自动调整使能）

AADJE位控制（启用或禁用）自动调整。

在更改ADJE位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。

RTC软件复位将ADJE位设置为0。

AADJP位（自动调整周期选择）

AADJP位选择自动调整周期。

在更改AADJP位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。

AADJP位通过RTC软件复位设置为0。

HR24 bit (Hours Mode)

HR24位指定RTC是在12小时还是24小时模式下运行。

在更改HR24位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改HR24位的值。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式还是二进制计数模式下运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新。但是，计数模式仅在RTC软件复位后切换。（RTC复位前位切换，RTC复位后模式切换。）

有关初始设置的详细信息，请参阅第23.3.1节。上电后寄存器的初始设置概要。

23.2.24 RCR2 : RTC Control Register 2 (in Binary Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START	Start 0: Stop the 32-bit binary counter, 64-Hz counter, and prescaler 1: Operate the 32-bit binary counter, 64-Hz counter, and prescaler normally	R/W
1	RESET	RTC Software Reset 0: In writing: Invalid (writing 0 has no effect). In reading: Normal time operation in progress, or an RTC software reset has completed. 1: In writing: Initialize the prescaler and target registers for RTC software reset*1. In reading: RTC software reset in progress.	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	RTCOE	RTCOUT Output Enable 0: Disable RTCOUT output 1: Enable RTCOUT output	R/W
4	AADJE	Automatic Adjustment Enable*2*3 0: Disable automatic adjustment 1: Enable automatic adjustment	R/W
5	AADJP	Automatic Adjustment Period Select*2*3 0: Add or subtract RADJ.ADJ [5:0] bits from prescaler count value every 32 seconds 1: Add or subtract RADJ.ADJ [5:0] bits from prescaler countvalue every 8 seconds.	R/W
6	—	The read value is undefined. The write value should be 0.	R/W
7	CNTMD	Count Mode Select*4 0: Calendar count mode 1: Binary count mode	R/W

Note 1. R64CNT, BCNTnAR, BCNTnAER, RADJ, RTCCRn, BCNTnCPm, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.
Note 3. When rewriting this bit, confirm that the value has been rewritten before performing the following processing. See section 23.6.5. Notes on Writing to and Reading from Registers for notes on register writing/reading.
Note 4. When rewriting this bit, confirm that the value has been rewritten before performing the following processing.

RCR2 in the binary count mode is a register related to the automatic correction function, RTCOUT output enable, RTC software reset, and count mode control.

START bit (Start)

The START bit stops or restarts the prescaler or counter (clock) operation. This bit is updated in synchronization with the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software. When 1 is written to this bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. When 1 is written to the RESET bit, check that the bit is 0 before proceeding.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time. When an RTCOUT signal is to be output from an external pin, enable the port control in addition to setting this bit.

23.2.24 RCR2：RTC控制寄存器2（二进制计数模式）

Base address: RTC = 0x4008_3000

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
重置后的值：	x	x	x	x	0	0	0	x

Bit	Symbol	Function	R/W
0	START	Start 0：停止32位二进制计数器、64-Hz计数器和预分频器1：正常操作32位二进制计数器、64-Hz计数器和预分频器	R/W
1	RESET	RTC软件复位 0：写入中：无效（写入0无效）。 读取中：正常时间操作正在进行，或RTC软件复位已完成。 1：书面：初始化RTC软件复位的预分频器和目标寄存器*1。读取中：RTC软件正在复位。	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	RTCOE	RTCOUT输出使能 0：禁用RTCOUT输出1：启用RTCOUT输出	R/W
4	AADJE	自动调整启用*2*3 0：禁用自动调整1：启用自动调整	R/W
5	AADJP	自动调整周期选择*2*3 0：每32秒从预分频器计数值加或减RADJ.ADJ[5:0]位1：每8秒从预分频器计数值加或减RADJ.ADJ[5:0]位。	R/W
6	—	读取值未定义。写入值应为0。	R/W
7	CNTMD	计数模式选择*4 0：日历计数模式1：二进制计数模式	R/W

Note 1. R64CNT, BCNTnAR, BCNTnAER, RADJ, RTCCRn, BCNTnCPm, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
注意2.选择机车时，该位的设置被禁用。
注3.改写该位时，请确认该值已被改写，然后再进行以下处理。请参阅第23.6.5节。
NotesonWritetoandReadingfromRegisters有关寄存器写入读取的说明。
注4.改写该位时，请确认该值已被改写，然后再进行以下处理。

二进制计数模式下的RCR2是与自动校正功能、RTCOUT输出使能、RTC软件复位和计数模式控制相关的寄存器。

开始位（开始）

START位停止或重新启动预分频器或计数器（时钟）操作。该位与计数源同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。当向该位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。当向RESET位写入1时，在继续之前检查该位是否为0。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。当要从外部引脚输出RTCOUT信号时，除了设置该位外，还启用端口控制。

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit. The AADJE bit is set to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Correction period can be selected from 32 second units or 8 second units in binary count mode.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit. The AADJP bit is set to 0 by an RTC software reset.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated in synchronization with the count source. However, the count mode switches only after the RTC software reset. (Bit switches before RTC reset, mode switches after RTC reset.)

For details on initial settings, see section 23.3.1. Outline of Initial Settings of Registers after Power On .

23.2.25 RCR4 : RTC Control Register 4

Base address: RTC = 0x4008_3000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RCKSEL
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RCKSEL	Count Source Select 0: Sub-clock oscillator is selected 1: LOCO is selected	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The RCR4 register is used in both calendar count mode and binary count mode.

RCKSEL bit (Count Source Select)

The RCKSEL bit selects the count source from the sub-clock oscillator and LOCO.

The RCKSEL bit is only used in normal operation mode. When the RCKSEL bit is set to 0, the time is counted with the sub-clock oscillator. When the bit is set to 1, the time is counted with LOCO.

For details on count source setting, see section 23.3.1. Outline of Initial Settings of Registers after Power On and section 23.3.2. Clock and Count Mode Setting Procedure. The count source must be selected only once before specifying the initial settings of the RTC registers at power on.

23.2.26 RFRL : Frequency Register L

Base address: RTC = 0x4008_3000

Offset address: 0x2C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFC[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

ADJE位（自动调整使能）

AADJE位控制（启用或禁用）自动调整。

在更改ADJE位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。RTC软件复位将ADJE位设置为0。

AADJP位（自动调整周期选择）

AADJP位选择自动调整周期。

在二进制计数模式下，校正周期可以从32秒单位或8秒单位中选择。

在更改AADJP位的值之前，将正负位(RADJ.PMADJ[1:0])设置为00b（不执行调整）。AADJP位通过RTC软件复位设置为0。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式还是二进制计数模式下运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新。但是，计数模式仅在RTC软件复位后切换。（RTC复位前位切换，RTC复位后模式切换。）

有关初始设置的详细信息，请参阅第23.3.1节。上电后寄存器的初始设置概要。

23.2.25 RCR4:RTC控制寄存器4

Base address: RTC = 0x4008_3000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RCKSEL
重置后的值:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RCKSEL	计数源选择 0：选择副时钟振荡器1：选择LOCO	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

RCR4寄存器用于日历计数模式和二进制计数模式。

RCKSEL位（计数源选择）

RCKSEL位从副时钟振荡器和LOCO中选择计数源。

RCKSEL位仅用于正常操作模式。当RCKSEL位设置为0时，时间由副时钟振荡器计数。当该位设置为1时，时间以LOCO计数。

有关计数源设置的详细信息，请参阅第23.3.1节。上电后寄存器的初始设置概要和第23.3.2节。时钟和计数模式设置程序。在上电时指定RTC寄存器的初始设置之前，必须只选择一次计数源。

23.2.26 RFRL:频率寄存器L

Base address: RTC = 0x4008_3000

Offset address: 0x2C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFC[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	RFC[15:0]	Frequency Comparison Value Write 0x00FF to this register when using the LOCO.	R/W

RFRL is a register for controlling the prescaler when LOCO is selected.

The RTC time counter operates on a 128-Hz clock signal as the base clock. Therefore, when LOCO is selected, LOCO is divided by the prescaler to generate a 128-Hz clock signal. Set the frequency comparison value in the RFC[15:0] bits to generate a 128-Hz clock from the LOCO frequency. Before writing to RFC[15:0] after a cold start, write 0x0000 to the RFRH register.

A value from 0x0007 through 0x01FF can be specified as the frequency comparison value. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2. The operating frequency of the peripheral module clock and the LOCO should be such that the peripheral module clock is ≥ LOCO.

Calculation method of frequency comparison value:

RFC[15:0] = (LOCO clock frequency) / 128 - 1

When the LOCO frequency is 32.768 kHz, the RFRL register should be set to 0x00FF.

23.2.27 RFRH : Frequency Register H

Base address: RTC = 0x4008_3000

Offset address: 0x2A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RFC16	Write 0 before writing to the RFRL register after a cold start.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

Before writing to RFRHL.RFC[15:0] after a cold start, write 0x0000 to the RFRH register.

23.2.28 RADJ : Time Error Adjustment Register

Base address: RTC = 0x4008_3000

Offset address: 0x2E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PMADJ[1:0]		ADJ[5:0]					
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
5:0	ADJ[5:0]	Adjustment Value These bits specify the adjustment value from the prescaler.	R/W
7:6	PMADJ[1:0]	Plus-Minus 0 0: Do not perform adjustment. 0 1: Adjustment is performed by the addition to the prescaler 1 0: Adjustment is performed by the subtraction from the prescaler 1 1: Setting prohibited.	R/W

The RADJ register is used in both calendar count mode and binary count mode. Adjustment is performed by the addition to or subtraction from the prescaler or 64-Hz counter. If the Automatic Adjustment Enable (RCR2.AADJE) bit is 0, adjustment

Bit	Symbol	Function	R/W
15:0	RFC[15:0]	频率比较值 使用LOCO时将0x00FF写入该寄存器。	R/W

RFRL是一个寄存器，用于在选择LOCO时控制预分频器。

RTC时间计数器以128-Hz时钟信号作为基本时钟运行。Therefore whenLOCOisselected LOCOisdividedbythepr escalertogeneratea128-Hzclocksignal.设置RFC[15:0]位中的频率比较值以从LOCO频率生成128-Hz时钟。在冷启动后写入RFC[15:0]之前，将0x0000写入RFRH寄存器。

从0x0007到0x01FF的值可以指定为频率比较值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必通过设置RCR2中的START位来停止计数操作。外围模块时钟和LOCO的工作频率应使外围模块时钟≥LOCO。

频率比较值的计算方法：

RFC[15:0] = (LOCO clock frequency) / 128 - 1

当LOCO频率为32.768kHz时，RFRL寄存器应设置为0x00FF。

23.2.27 RFRH:频率寄存器H

Base address: RTC = 0x4008_3000

Offset address: 0x2A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	RFC16	在冷启动后写入RFRL寄存器之前写入0。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

在冷启动后写入RFRHL.RFC[15:0]之前，将0x0000写入RFRH寄存器。

23.2.28 RADJ:时间误差调整寄存器

Base address: RTC = 0x4008_3000

Offset address: 0x2E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PMADJ[1:0]		ADJ[5:0]					
重置后的值:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
5:0	ADJ[5:0]	调整值 这些位指定来自预分频器的调整值。	R/W
7:6	PMADJ[1:0]	Plus-Minus 00：不进行调整。01：通过预分频器1的加法进行调整0：通过预分频器1的减法进行调整1：禁止设置。	R/W

RADJ寄存器用于日历计数模式和二进制计数模式。通过对预分频器或64-Hz计数器进行加法或减法来执行调整。如果自动调整启用(RCR2.AADJE)位为0，则调整

is performed when writing to the RADJ. If the RCR2.AADJE bit is 1, adjustment is performed in the interval specified in the Automatic Adjustment Period Select (RCR2.AADJP) bit.

The current adjustment by software (disabling automatic adjustment) may be invalid if the following adjustment value is specified within 320 cycles of the count source after the register setting. To perform adjustment consecutively, wait for 320 cycles or more of the count source after the register setting, then specify the next adjustment value.

RADJ is updated in synchronization with the count source. When RADJ is modified, check that all the bits are updated before continuing with more processing. This register is set to 0x00 by an RTC software reset. The setting of this register is enabled only when the sub-clock oscillator is selected. When LOCO is selected, adjustment is not performed.

ADJ[5:0] bits (Adjustment Value)

The ADJ[5:0] bits specify the adjustment value (number of sub-clock cycles) from the prescaler.

PMADJ[1:0] bits (Plus-Minus)

The PMADJ[1:0] bits select whether the clock is set ahead or back depending on the error-adjustment value set in the ADJ[5:0] bits.

23.2.29 RTCCRn : Time Capture Control Register n (n = 0 to 2)

Base address: RTC = 0x4008_3000

Offset address: 0x40 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCEN	—	TCNF[1:0]		—	TCST	TCCT[1:0]	
Value after reset:	x	0	x	x	0	x	x	x

Bit	Symbol	Function	R/W
1:0	TCCT[1:0]	Time Capture Control 0 0: Do not detect events 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges	R/W
2	TCST	Time Capture Status 0: No event detected 1: Event detected*1	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	TCNF[1:0]	Time Capture Noise Filter Control 0 0: Turn noise filter off 0 1: Setting prohibited 1 0: Turn noise filter on (count source) 1 1: Turn noise filter on (count source by divided by 32)	R/W
6	—	These bits are read as 0. The write value should be 0.	R/W
7	TCEN	Time Capture Event Input Pin Enable 0: Disable the RTCICn pin as the time capture event input pin 1: Enable the RTCICn pin as the time capture event input pin	R/W

Note 1. Indicates that an event is detected. Writing 1 to this bit has no effect. Writing 0 sets this bit to 0.

The RTCCRn register is used both in calendar count mode and in binary count mode. RTCCR0, RTCCR1, and RTCCR2 control the RTCIC0, RTCIC1, and RTCIC2 pins, respectively.

RTCCRn is updated in synchronization with the count source. When RTCCRn is modified, check that all the bits except the TCST bit are updated before continuing with additional processing. This register is cleared to 0x00 by an RTC software reset. When RTCICm is used as the time capture pin, VBTICTLR.VCHnIEN (n = 0 to 2) must be set to 1.

TCCT[1:0] bits (Time Capture Control)

The TCCT[1:0] bits control the edge detection of the time capture event input pins, RTCIC0, RTCIC1, and RTCIC2. The detection edge is selectable. The TCCT[1:0] bits must be set while the VBTICTLR.VCHnIEN bit is 1.

在写入RADJ时执行。如果RCR2.AADJE位为1，则在自动调整周期选择(RCR2.AADJP)位指定的间隔内执行调整。

如果在寄存器设置后的计数源的320个周期内指定了以下调整值，则通过软件进行的当前调整（禁用自动调整）可能无效。要连续执行调整，请在寄存器设置后等待计数源的320个或更多周期，然后指定下一个调整值。

RADJ与计数源同步更新。修改RADJ后，在继续进行更多处理之前检查所有位是否已更新。该寄存器通过RTC软件复位设置为0x00。该寄存器的设置仅在选择了副时钟振荡器时启用。选择LOCO时，不进行调整。

ADJ[5:0] bits (Adjustment Value)

ADJ[5:0]位指定来自预分频器的调整值（子时钟周期数）。

PMADJ[1:0] bits (Plus-Minus)

PMADJ[1:0]位根据在
ADJ[5:0] bits.

23.2.29 RTCCRn:时间捕捉控制寄存器n(n=0to2)

Base address: RTC = 0x4008_3000

Offset address: 0x40 + 0x02 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TCEN	—	TCNF[1:0]		—	TCST	TCCT[1:0]	
重置后的值：	x	0	x	x	0	x	x	x

Bit	Symbol	Function	R/W
1:0	TCCT[1:0]	时间捕捉控制 00：不检测事件01：检测 上升沿10：检测下降沿11 ：检测两个沿	R/W
2	TCST	时间捕捉状态 0：未检测到事件1： 检测到事件*1	R/W
3	—	该位读取为0。写入值应为0。	R/W
5:4	TCNF[1:0]	时间捕捉噪声滤波器控制 00：关闭噪声过滤器01：设置禁止10：打开噪声过滤器 （计数源）11：打开噪声过滤器（计数源除以32）	R/W
6	—	这些位被读取为0。写入值应为0。	R/W
7	TCEN	时间捕捉事件输入引脚使能 0：禁止RTCICn引脚作为时间捕捉事件输入引脚1：使能RTCICn 引脚作为时间捕捉事件输入引脚	R/W

注1.表示检测到事件。向该位写入1无效。写入0将该位设置为0。

RTCCRn寄存器用于日历计数模式和二进制计数模式。RTCCR0、RTCCR1和RTCCR2分别控制RTCIC0、RTCIC1和RTCIC2引脚。

RTCCRn与计数源同步更新。当RTCCRn被修改时，检查除
TCST位在继续进行附加处理之前被更新。RTC软件复位将该寄存器清零为0x00。当RTCICm用作时间捕捉引脚时，VBTICTLR.VCHnIEN(n=0to2)必须设置为1。

TCCT[1:0]位（时间捕捉控制）

TCCT[1:0]位控制时间捕捉事件输入引脚RTCIC0、RTCIC1和RTCIC2的边沿检测。检测边缘是可选的。当VBTICTLR.VCHnIEN位为1时，必须设置TCCT[1:0]位。

TCST bit (Time Capture Status)

The TCST bit indicates that an event on the time capture event input pins, RTCIC0, RTCIC1, and RTCIC2, was detected. When the TCST bit is 0, no event is detected. When the TCST bit is 1, this bit indicates that an event was detected on the associated pin and the capture register is valid. When multiple events are detected, the capture time for the first event is retained.

The event is detected only during count operation (RCR2.START bit = 1). Before reading the capture register, make sure that this bit is set to 1.

Set the TCST bit while the TCCT[1:0] bits are 00b (no event is detected). The TCST bit is set to 0 in synchronization with the count source. When the TCST bit is set to 0, check that the bit is updated before continuing with additional processing.

TCNF[1:0] bits (Time Capture Noise Filter Control)

The TCNF[1:0] bits control the noise filter of the time capture event input pins (RTCIC0, RTCIC1, and RTCIC2).

When the noise filter is on, the count source divided by 1 or divided by 32 is selectable. In this case, when the input level on the time capture event input pin matches three consecutive times at the set sampling period, the input level is determined.

Set the TCNF[1:0] bits while the TCCT[1:0] bits are 00b (no event is detected). When the noise filter is used, set the TCNF[1:0] bits, wait for 3 cycles of the specified sampling period, then set the TCCT[1:0] bits. Set the TCNF[1:0] bits when the VBTICTLR.VCHnIEN bit is 1.

TCEN bit (Time Capture Event Input Pin Enable)

The TCEN bit enables or disables the time capture event input pins RTCIC0, RTCIC1, and RTCIC2. When the functions of the time capture event input pins are multiplexed, set VBTICTLR first. If the TCEN bit is set to 0, also set the TCCT[1:0] bits to 00b.

section 23.2.29. RTCCRn : Time Capture Control Register n (n = 0 to 2) lists the conditions for enabling the RTCICn pin. Before setting this bit to 1, be sure to set the count source setting bit (RCR4.RCKSEL), RTC time capture event enable bit (RCPE.RTCEN), port control setting bits (PmnPFS.PDR, and PmnPFS.PMR). For details on the port control setting bits (PmnPFS.PDR and PmnPFS.PMR), see section 19, I/O Ports.

23.2.30 RSECCPn : Second Capture Register n (n = 0 to 2) (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x52 + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1-Second Capture Capture value for the ones place of seconds.	R
6:4	SEC10[2:0]	10-Second Capture Capture value for the tens place of seconds.	R
7	—	The read value is undefined.	R

RSECCPn is a read-only register that captures the RSECCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RSECCP0, RSECCP1, and RSECCP2 registers, respectively. This register is cleared to 0x00 by an RTC software reset. Before reading from this register, the time capture event detection should be stopped using the RTCCRn.TCCT[1:0] bits.

TCST位（时间捕捉状态）

TCST位指示检测到时间捕捉事件输入引脚RTCIC0、RTCIC1和RTCIC2上的事件。当TCST位为0时，未检测到任何事件。当TCST位为1时，该位表示在相关引脚上检测到事件并且捕捉寄存器有效。当检测到多个事件时，将保留第一个事件的捕获时间。

仅在计数操作期间检测到事件（RCR2.START位=1）。在读取捕获寄存器之前，请确保该位设置为1。

当TCCT[1:0]位为00b（未检测到事件）时，设置TCST位。TCST位与计数源同步设置为0。当TCST位设置为0时，在继续进行其他处理之前检查该位是否已更新。

TCNF[1:0]位（时间捕捉噪声滤波器控制）

TCNF[1:0]位控制时间捕捉事件输入引脚（RTCIC0、RTCIC1和RTCIC2）的噪声滤波器。

当噪声滤波器打开时，计数源除以1或除以32是可选的。在这种情况下，当时间捕捉事件输入引脚上的输入电平在设置的采样周期内连续匹配3次时，确定输入电平。

当TCCT[1:0]位为00b（未检测到事件）时，设置TCNF[1:0]位。使用噪声滤波器时，设置TCNF[1:0]位，等待指定采样周期的3个周期，然后设置TCCT[1:0]位。当VBTICTLR.VCHnIEN位为1时，设置TCNF[1:0]位。

TCEN位（时间捕捉事件输入引脚使能）

TCEN位启用或禁用时间捕捉事件输入引脚RTCIC0、RTCIC1和RTCIC2。当时间捕捉事件输入引脚的功能复用时，首先设置VBTICTLR。如果TCEN位设置为0，也将TCCT[1:0]位设置为00b。

第23.2.29节。RTCCRn：时间捕捉控制寄存器n（n=0到2）列出了启用RTCICn引脚的条件。在将此位设置为1之前，请务必设置计数源设置位(RCR4.RCKSEL)、RTC时间捕捉事件使能位(RCPE.RTCEN)、端口控制设置位(PmnPFS.PDR和PmnPFS.PMR)。有关端口控制设置位（PmnPFS.PDR和PmnPFS.PMR）的详细信息，请参阅第19节，IO端口。

23.2.30 RSCCPn：第二个捕捉寄存器n（n=0到2）（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x52 + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SEC10[2:0]			SEC1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	SEC1[3:0]	1秒捕获捕获秒的个位的值。	R
6:4	SEC10[2:0]	10秒捕获十位秒的捕获值。	R
7	—	读取值未定义。	R

RSCCPn是一个只读寄存器，当检测到时间捕捉事件时，它会捕捉RSECCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在RSCCP0、RSCCP1和RSCCP2寄存器，分别。RTC软件复位将该寄存器清零为0x00。在读取该寄存器之前，应使用RTCCRn.TCCT[1:0]位停止时间捕捉事件检测。

23.2.31 RMINCPn : Minute Capture Register n (n = 0 to 2) (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x54 + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1-Minute Capture Capture value for the ones place of minutes.	R
6:4	MIN10[2:0]	10-Minute Capture Capture value for the tens place of minutes.	R
7	—	The read value is undefined.	R

RMINCPn is a read-only register that captures the RMINCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RMINCP0, RMINCP1, and RMINCP2 registers, respectively.

This register is cleared to 0x00 by an RTC software reset. Before reading from this register, the time capture event detection should be stopped using the RTCCRn.TCCT[1:0] bits.

23.2.32 RHRCPn : Hour Capture Register n (n = 0 to 2) (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x56 + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1-Hour Capture Capture value for the ones place of hours	R
5:4	HR10[1:0]	10-Hour Capture Capture value for the tens place of hours	R
6	PM	PM 0: AM 1: PM	R
7	—	The read value is undefined.	R

RHRCPn is a read-only register that captures the RHRCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RHRCP0, RHRCP1, and RHRCP2 registers, respectively.

The PM bit is only enabled when the RCR2.HR24 bit is 0 (in 12-hour mode).

This register is cleared to 0x00 by an RTC software reset. Before reading from this register, you must stop the time capture event detection using the RTCCRn.TCCT[1:0] bits.

23.2.31 RMINCPn：分钟捕捉寄存器n（n=0到2）（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x54 + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MIN1[3:0]	1-MinuteCapture以分钟为单位的捕获值。	R
6:4	MIN10[2:0]	10分钟捕获十位分钟的捕获值。	R
7	—	读取值未定义。	R

RMINCPn是一个只读寄存器，它在检测到时间捕捉事件时捕捉RMINCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在RMINCP0、RMINCP1和RMINCP2寄存器，分别。

RTC软件复位将该寄存器清零为0x00。在读取该寄存器之前，应使用RTCCRn.TCCT[1:0]位停止时间捕捉事件检测。

23.2.32 RHRCPn：小时捕捉寄存器n（n=0到2）（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x56 + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	HR1[3:0]	1-HourCapture以小时为单位的捕获值	R
5:4	HR10[1:0]	10-HourCapture十位小时的捕获值	R
6	PM	PM 0: AM 1: PM	R
7	—	读取值未定义。	R

RHRCPn是一个只读寄存器，它在检测到时间捕捉事件时捕捉RHRCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在RHRCP0、RHRCP1和RHRCP2寄存器，分别。

PM位仅在RCR2.HR24位为0时启用（在12小时模式下）。

RTC软件复位将该寄存器清零为0x00。在读取该寄存器之前，您必须使用RTCCRn.TCCT[1:0]位停止时间捕捉事件检测。

23.2.33 RDAYCPn : Date Capture Register n (n = 0 to 2) (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x5A + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1-Day Capture Capture value for the ones place of days.	R
5:4	DATE10[1:0]	10-Day Capture Capture value for the tens place of days.	R
7:6	—	The read value is undefined.	R

RDAYCPn is a read-only register that captures the RDAYCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RDAYCP0, RDAYCP1, and RDAYCP2 registers, respectively.

This register is cleared to 0x00 by an RTC software reset. Before reading from this register, the time capture event detection should be stopped using the RTCCRn.TCCT[1:0] bits.

23.2.34 RMONCPn : Month Capture Register n (n = 0 to 2) (in Calendar Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x5C + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MON10	MON1[3:0]			
Value after reset:	0	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1-Month Capture Capture value for the ones place of months.	R
4	MON10	10-Month Capture Capture value for the tens place of months.	R
7:5	—	These bits are read as 0.	R

RMONCPn is a read-only register that captures the RMONCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RMONCP0, RMONCP1, and RMONCP2 registers, respectively.

This register is cleared to 0x00 by an RTC software reset. Before reading from this register, the time capture event detection should be stopped using the RTCCRn.TCCT[1:0] bits.

23.2.33 RDAYCPn：日期捕捉寄存器n（n=0到2）（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x5A + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	DATE1[3:0]	1天捕获捕获天数的值。	R
5:4	DATE10[1:0]	10天捕获十位天的捕获值。	R
7:6	—	读取值未定义。	R

RDAYCPn是一个只读寄存器，它在检测到时间捕捉事件时捕捉RDAYCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间分别存储在RDAYCP0、RDAYCP1和RDAYCP2寄存器中。

RTC软件复位将该寄存器清零为0x00。在读取该寄存器之前，应使用RTCCRn.TCCT[1:0]位停止时间捕捉事件检测。

23.2.34 RMONCPn：月份捕捉寄存器n（n=0到2）（在日历计数模式下）

Base address: RTC = 0x4008_3000

Offset address: 0x5C + 0x10 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	MON10	MON1[3:0]			
重置后的值：	0	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
3:0	MON1[3:0]	1-MonthCapture捕获月份个位数的值。	R
4	MON10	10个月捕获捕获十个月份的值。	R
7:5	—	这些位读为0。	R

RMONCPn是一个只读寄存器，它在检测到时间捕捉事件时捕捉RMONCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间分别存储在RMONCP0、RMONCP1和RMONCP2寄存器中。

RTC软件复位将该寄存器清零为0x00。在读取该寄存器之前，应使用RTCCRn.TCCT[1:0]位停止时间捕捉事件检测。

23.2.35 BCNTnCPm : BCNTn Capture Register m (n= 0 to 3, m = 0 to 2) (in Binary Count Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x52 + 0x10 × m (BCNT0CPm)
0x54 + 0x10 × m (BCNT1CPm)
0x56 + 0x10 × m (BCNT2CPm)
0x5A + 0x10 × m (BCNT3CPm)

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	x	x	x	x	x	x	x	x

BCNTnCPm is a read-only register that captures the BCNTn value when a time capture event is detected. BCNT3CPm is assigned to the BCNTCPm[31:24] bits, BCNT2CPm is assigned to the BCNTCPm[23:16] bits, BCNT1CPm is assigned to the BCNTCPm[15:8] bits and BCNT0CPm is assigned to the BCNTCPm[7:0] bits. The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the BCNTnCP0, BCNTnCP1, and BCNTnCP2 registers, respectively.

This register is cleared to 0x00 by an RTC software reset. Before reading from this register, you must stop the time capture event detection using the RTCCRn.TCCT[1:0] bits.

23.3 Operation

23.3.1 Outline of Initial Settings of Registers after Power On

After the power is turned on, perform the initial settings for the clock, count mode, time error adjustment, time, alarm, interrupts, and time capture.

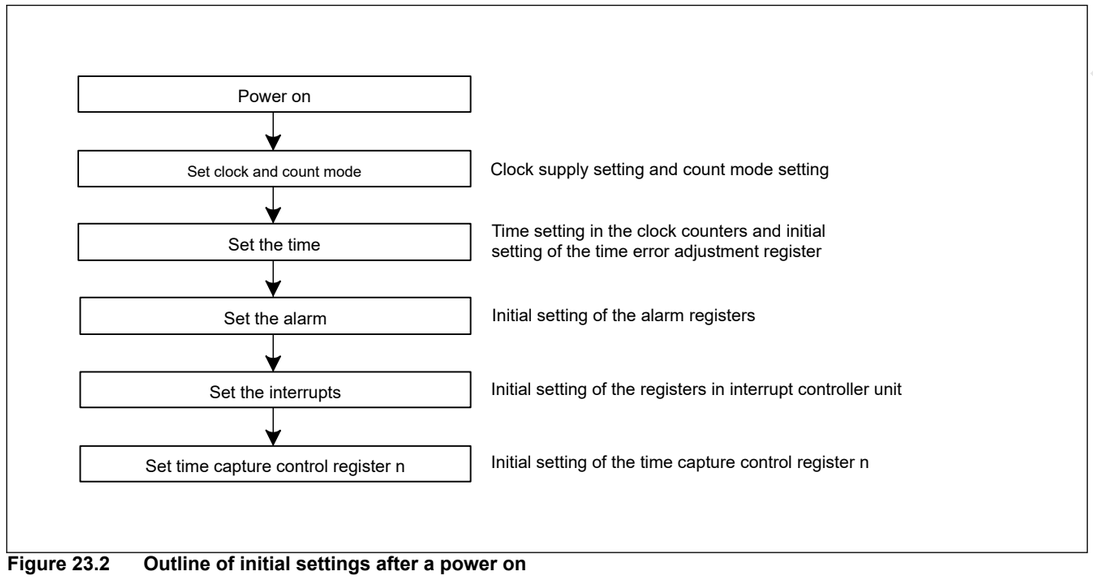


Figure 23.2 Outline of initial settings after a power on

23.3.2 Clock and Count Mode Setting Procedure

Figure 23.3 shows how to set the clock and the count mode.

23.2.35 BCNTnCPm:BCNTn捕捉寄存器m(n=0to3 m=0to2)(以二进制计数 Mode)

Base address: RTC = 0x4008_3000

Offset address: 0x52 + 0x10 × m (BCNT0CPm)
0x54 + 0x10 × m (BCNT1CPm)
0x56 + 0x10 × m (BCNT2CPm)
0x5A + 0x10 × m (BCNT3CPm)

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	x	x	x	x	x	x	x	x

BCNTnCPm是一个只读寄存器，它在检测到时间捕捉事件时捕捉BCNTn值。BCNT3CPm分配给BCNTCPm[31:24]位，BCNT2CPm分配给BCNTCPm[23:16]位，BCNT1CPm分配给BCNTCPm[15:8]位，BCNT0CPm分配给BCNTCPm[7:0]位。RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间分别存储在BCNTnCP0、BCNTnCP1和BCNTnCP2寄存器中。

RTC软件复位将该寄存器清零为0x00。在读取该寄存器之前，您必须使用RTCCRn.TCCT[1:0]位停止时间捕捉事件检测。

23.3 Operation

23.3.1 上电后寄存器的初始设置概要

上电后，对时钟、计数方式、时间误差调整、时间、闹钟、中断、时间捕捉进行初始设置。

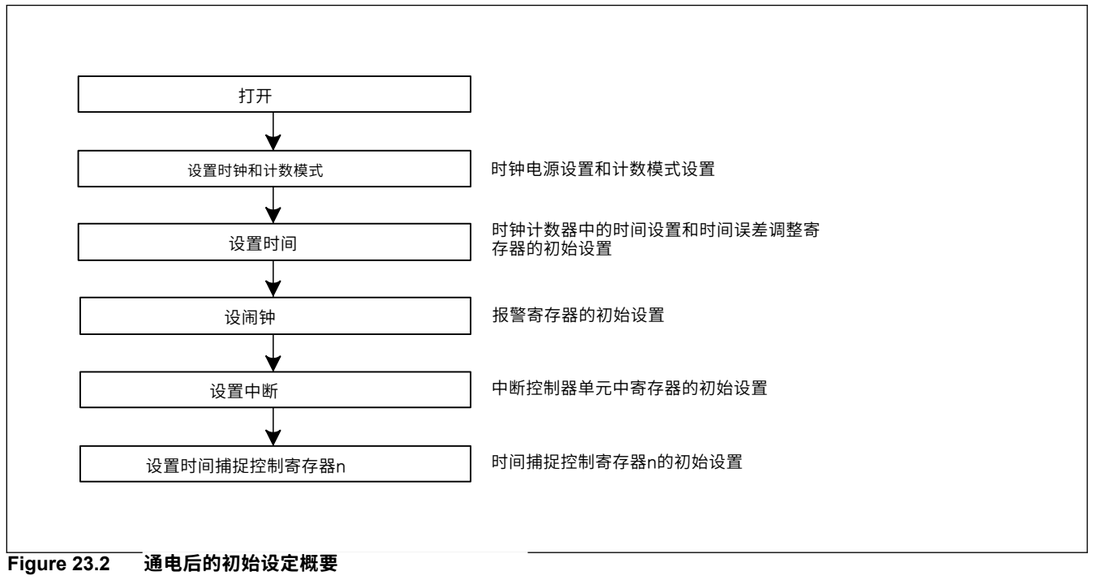
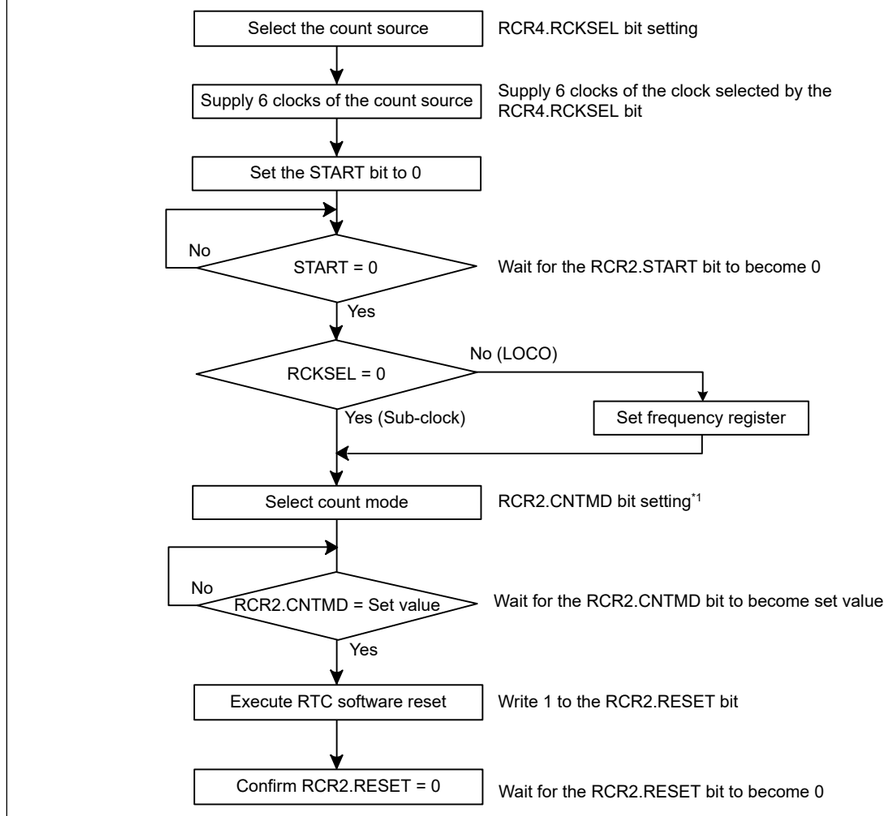


Figure 23.2 通电后的初始设定概要

23.3.2 时钟和计数模式设置程序

图23.3显示了如何设置时钟和计数模式。

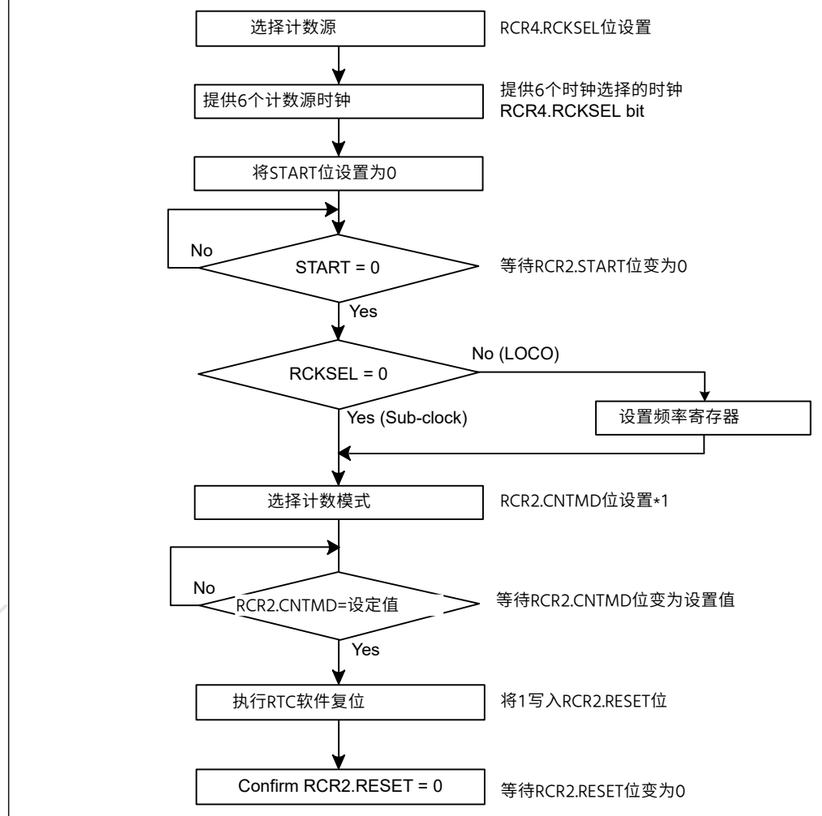


Note 1. This step is not required if the count mode is concurrently set by setting the START bit to 0. A value associated with the count mode setting must be written to the RCR2.CNTMD bit.

Figure 23.3 Clock and count mode setting procedure

23.3.3 Setting the Time

Figure 23.4 shows how to set the time.

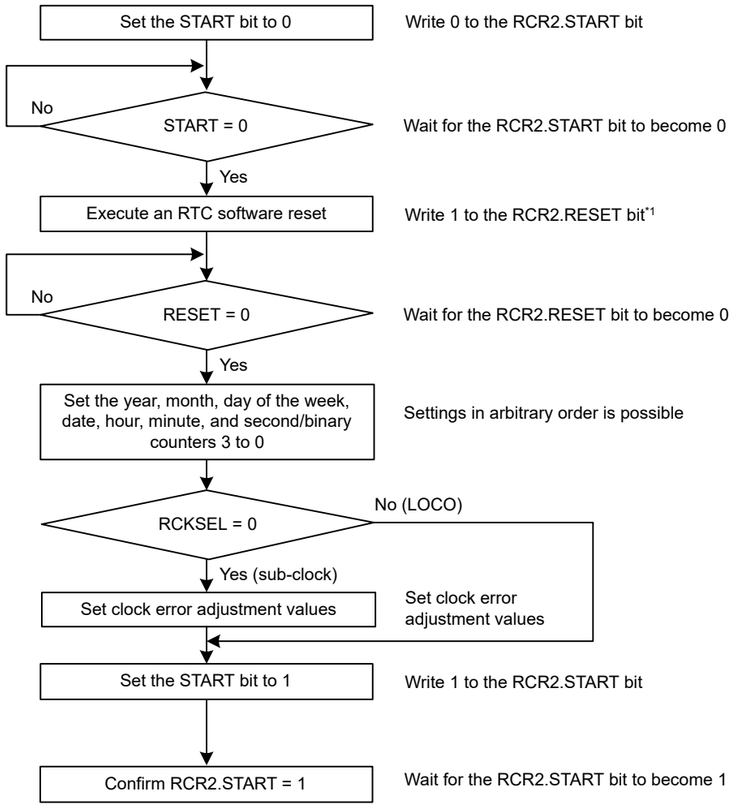


注1.如果通过将START位设置为0同时设置计数模式，则不需要此步骤。必须将与计数模式设置相关的值写入RCR2.CNTMD位。

Figure 23.3 时钟和计数模式设置程序

23.3.3 设置时间

图23.4显示了如何设置时间。

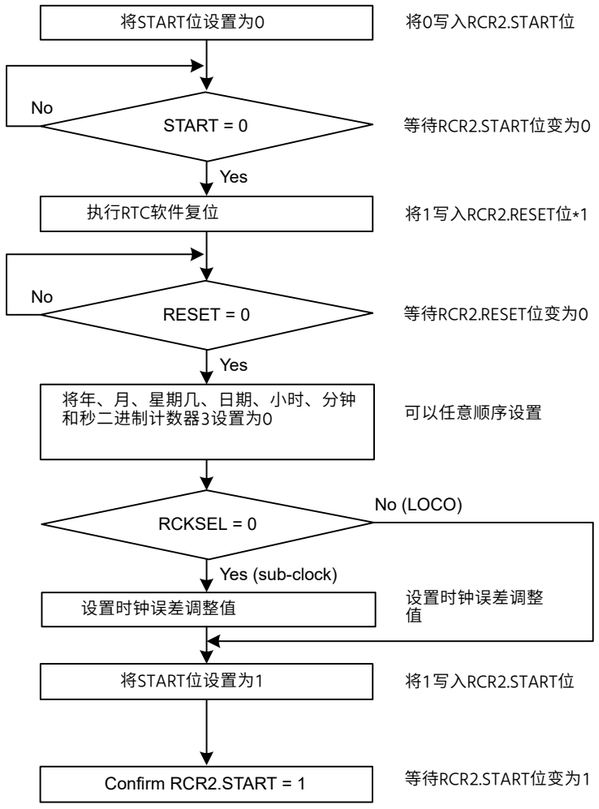


Note 1. This step can be omitted in initial settings after power-on because an RTC software reset is executed in the clock setting procedure that is performed during initial settings at power-on.
Note 2. Set in any order.

Figure 23.4 Setting the time

23.3.4 30-Second Adjustment

Figure 23.5 shows how to execute a 30-second adjustment.



注1.上电后初始设置中可以省略此步骤，因为在上电初始设置期间执行的时钟设置过程中执行RTC软件复位。

注2.按任意顺序设置。

Figure 23.4 设定时间

23.3.4 30-Second Adjustment

图23.5显示了如何执行30秒的调整。

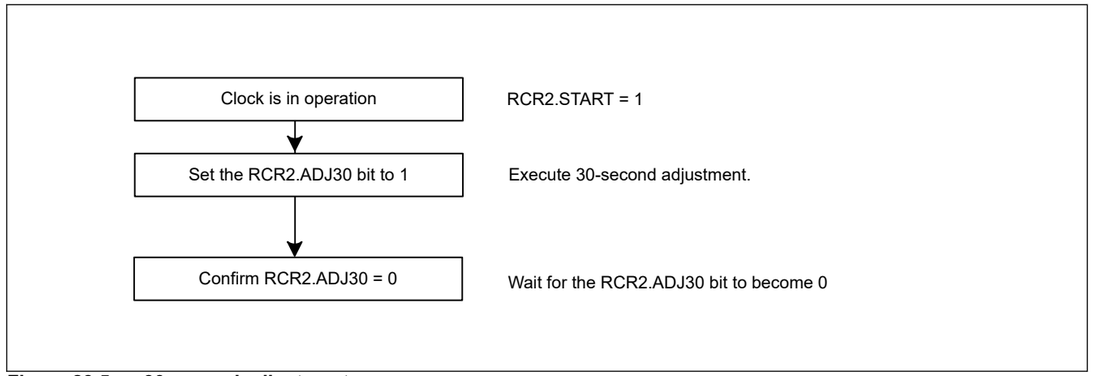


Figure 23.5 30-second adjustment

23.3.5 Reading 64-Hz Counter and Time

Figure 23.6 shows how to read a 64-Hz counter and time.

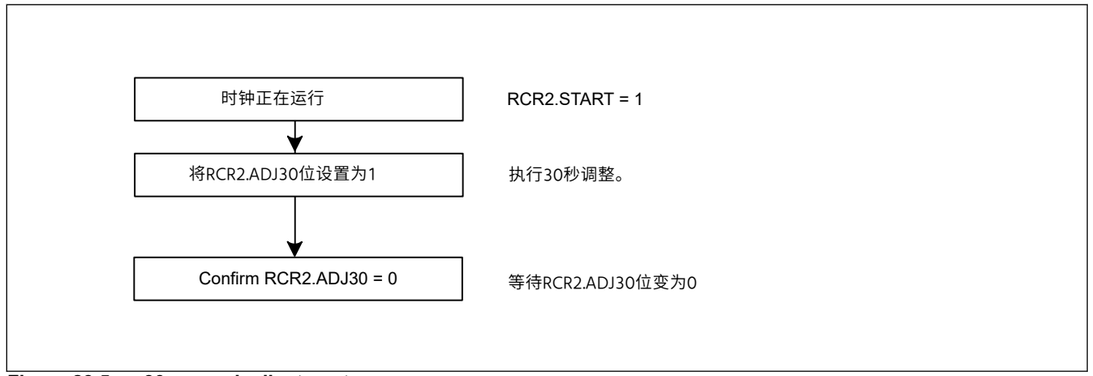


Figure 23.5 30-second adjustment

23.3.5 读取64-Hz计数器和时间

图23.6显示了如何读取64-Hz计数器和时间。

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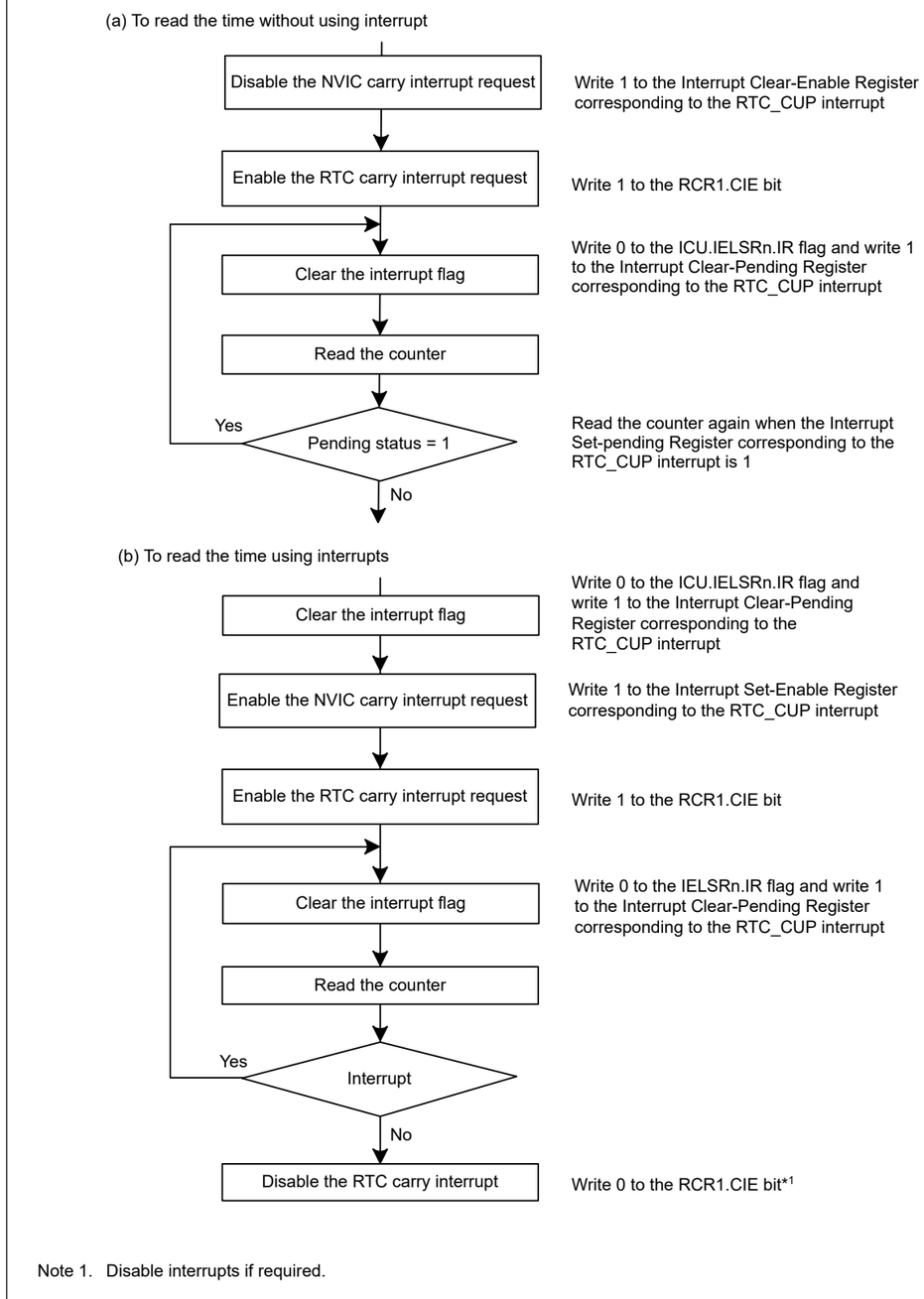
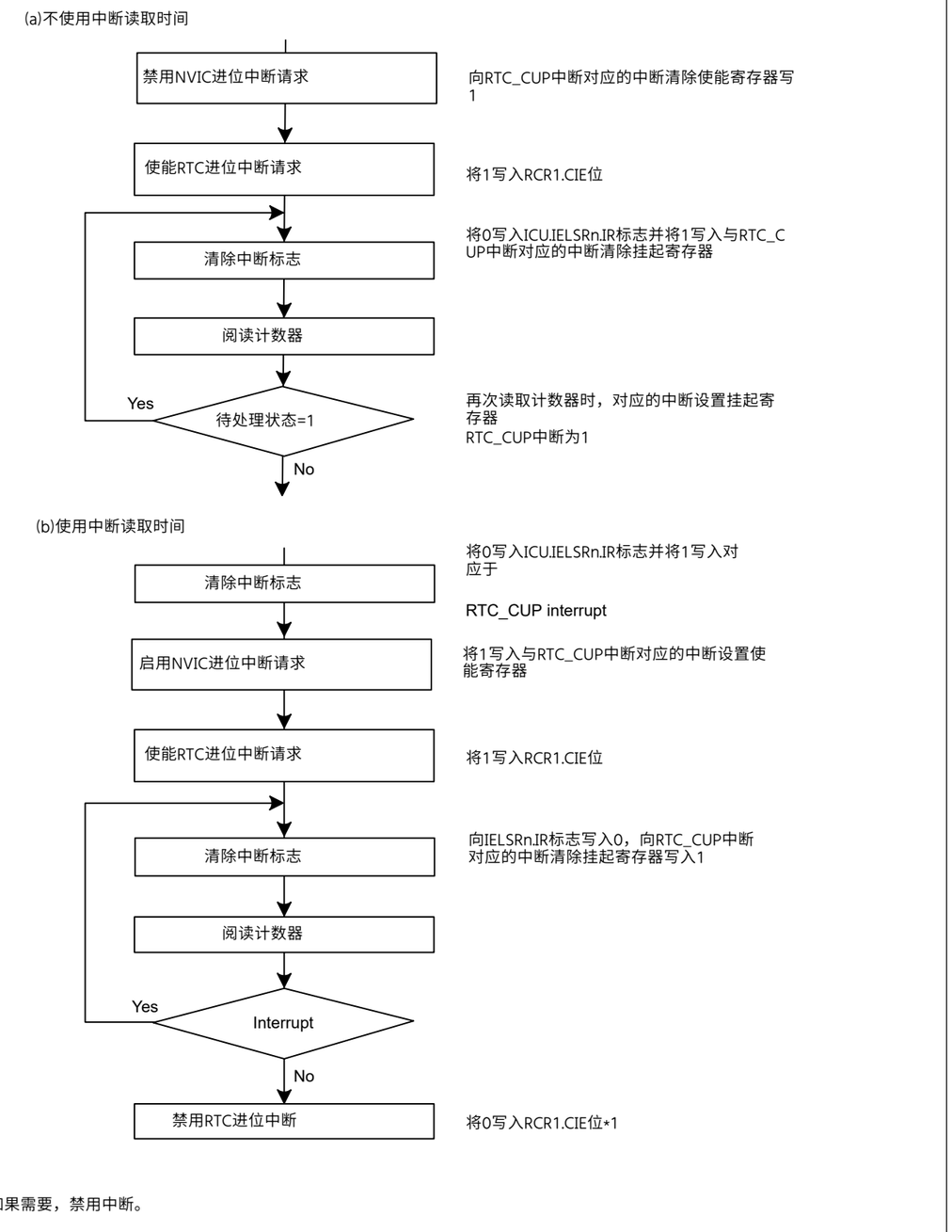


Note 1. Disable interrupts if required.

Figure 23.6 Reading time

If a carry occurs while the 64-Hz counter and time are read, the correct time is not obtained, therefore they must be read again. The procedure for reading the time without using interrupts is shown in (a) in Figure 23.6, and the procedure using carry interrupts is shown in (b). To keep the program simple, method (a) should be used in most cases.



注1.如果需要，禁用中断。

Figure 23.6 阅读时间

如果在读取64-Hz计数器和时间时发生进位，则无法获得正确的时间，因此必须再次读取它们。不使用中断读取时间的过程如图23.6(a)所示，使用进位中断的过程如图23.6所示。为保持程序简单，在大多数情况下应使用方法(a)。

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23.3.6 Alarm Function

Figure 23.7 shows how to use the alarm function.

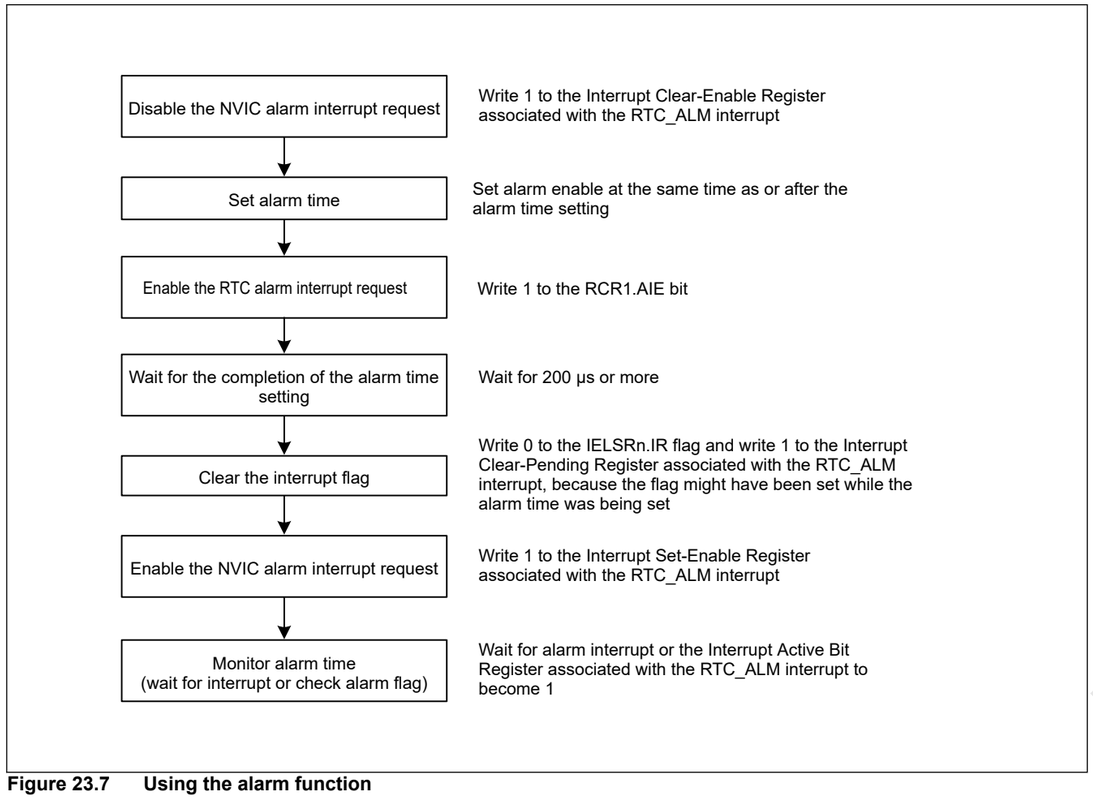


Figure 23.7 Using the alarm function

In calendar count mode, an alarm can be generated by any one of year, month, date, day-of-week, hour, minute or second, or any combination of those. Write 1 to the ENB bit in the alarm registers involved in the alarm setting, and set the alarm time in the lower bits. Write 0 to the ENB bit in registers not involved in the alarm setting.

In binary count mode, an alarm can be generated in any bit combination of 32 bits. Write 1 to the ENB bit of the Alarm Enable register associated with the target bit of the alarm, and set the alarm time in the alarm register. For bits that are not the target of the alarm, write 0 to the ENB bit of the Alarm Enable register.*1

For any of the ENB[31:0] bits that are set to 1, the bits in the corresponding positions in the binary counter (BCNT[31:0]) are compared with the values of the corresponding bits in the binary alarm registers*1. When all such bits match, the IR flag associated with the RTC_ALM interrupt is set to 1 and the corresponding bits in the Interrupt Set-Pending/Clear-Pending Registers are set to 1. Alarm detection can be confirmed by reading the Interrupt Set-Pending Register associated with the RTC_ALM interrupt, but an interrupt should be used in most cases. If 1 is set in the Interrupt Set-Enable Register associated with the RTC_ALM interrupt, an alarm interrupt is generated in the event of the alarm, enabling the alarm to be detected.

Writing 0 sets the IELSRn.IR flag associated with the RTC_ALM interrupt to 0. If interrupt is enabled, the Interrupt Set-Pending/Clear-Pending Register associated with the RTC_ALM interrupt is cleared automatically after exiting the interrupt handler. Otherwise, write 1 to the Interrupt Clear-Pending Register associated with the RTC_ALM interrupt to clear it.

When the counter and the alarm time match in a low power state, the MCU returns from the low power state.

Note 1. For any bits in the ENB bits that are set to 1, the values in the corresponding positions in the alarm registers from the following registers are compared with the corresponding bits of the counted values.

Counter registers: RSECCNT, RMINCNT, RHRCNT, RWKCNT, RDAYCNT, RMONCNT, RYRCNT

Alarm registers: RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAREN

23.3.6 报警功能

图23.7显示了如何使用报警功能。

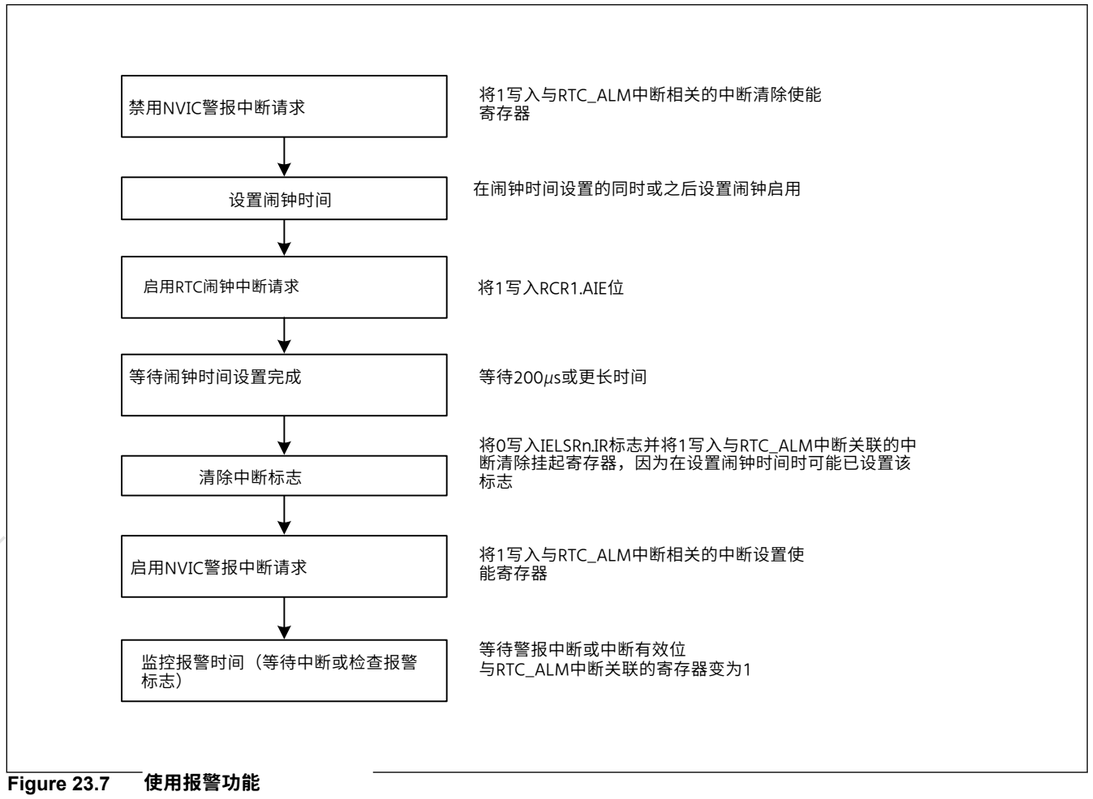


Figure 23.7 使用报警功能

在日历计数模式下，可以通过年、月、日、星期、小时、分钟或秒中的任何一个或它们的任意组合来生成警报。将1写入涉及闹钟设置的闹钟寄存器的ENB位，并在低位设置闹钟时间。将0写入与报警设置无关的寄存器中的ENB位。

在二进制计数模式下，可以以32位的任意位组合产生报警。将1写入闹钟的ENB位与报警的目标位相关联的使能寄存器，并在报警寄存器中设置报警时间。对于不是警报目标的位，将0写入警报启用寄存器的ENB位。*1

对于任何设置为1的ENB[31:0]位，二进制计数器(BCNT[31:0])中相应位置的位与二进制报警寄存器中相应位的值进行比较*1.当所有这些位匹配时，与RTC_ALM中断相关的IR标志设置为1，并且中断设置挂起清除挂起寄存器中的相应位设置为1。可以通过读取中断设置挂起寄存器来确认警报检测与RTC_ALM中断相关联，但在大多数情况下应使用中断。如果在与RTC_ALM中断相关的中断设置使能寄存器中设置为1，则在发生警报时会产生警报中断，从而能够检测到警报。

写入0将与RTC_ALM中断关联的IELSRn.IR标志设置为0。如果启用中断，则中断设置与RTC_ALM中断关联的PendingClear-Pending寄存器在退出中断处理程序后自动清除。否则，将1写入与RTC_ALM中断相关的中断清除挂起寄存器以将其清除。

当计数器和闹钟时间在低功耗状态下匹配时，MCU从低功耗状态返回。

注1.对于设置为1的ENB位中的任何位，将以下寄存器中警报寄存器中相应位置的值与计数值的相应位进行比较。

Counter registers: RSECCNT, RMINCNT, RHRCNT, RWKCNT, RDAYCNT, RMONCNT, RYRCNT

Alarm registers: RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAREN

23.3.7 Procedure for Disabling Alarm Interrupt

Figure 23.8 shows the procedure for disabling the enabled alarm interrupt request.

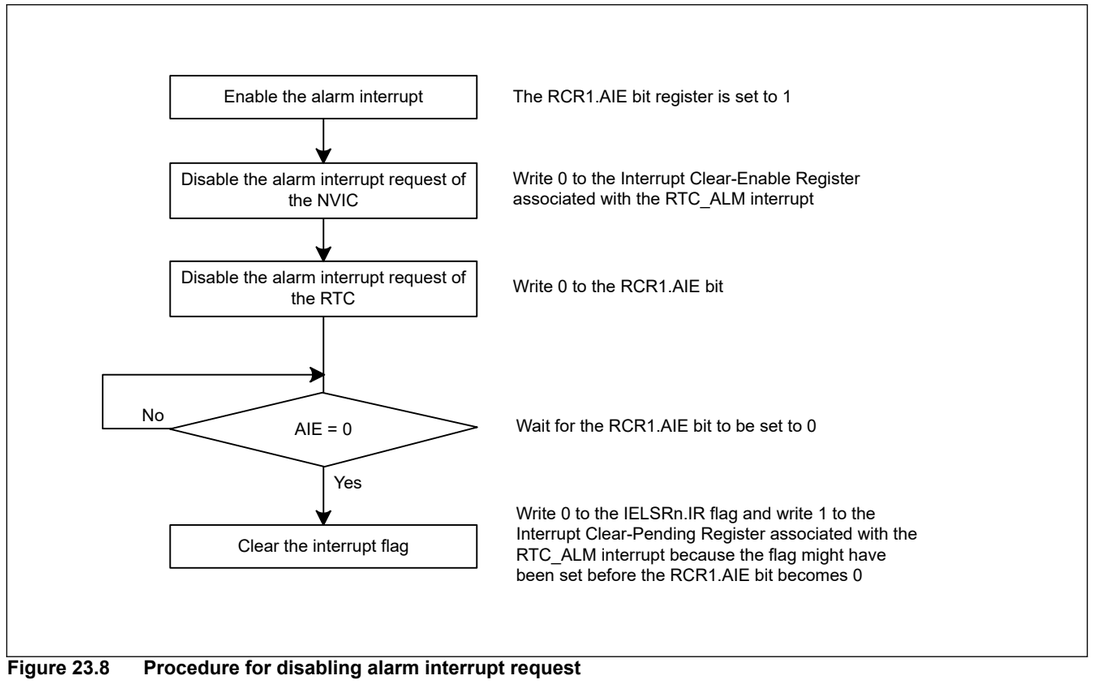


Figure 23.8 Procedure for disabling alarm interrupt request

23.3.8 Time Error Adjustment Function

The time error adjustment function is used to correct errors, running fast or slow, in the time caused by variation in the precision of oscillation by the sub-clock oscillator. Because 32768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low.

The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software

Use the RCR2.AADJE bit to select automatic adjustment or adjustment by software.

23.3.8.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1.

Automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJP bit elapses.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32769 clock cycles. The RTC is meant to run at 32768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

23.3.7 禁用警报中断的步骤

图23.8显示了禁用启用的警报中断请求的过程。

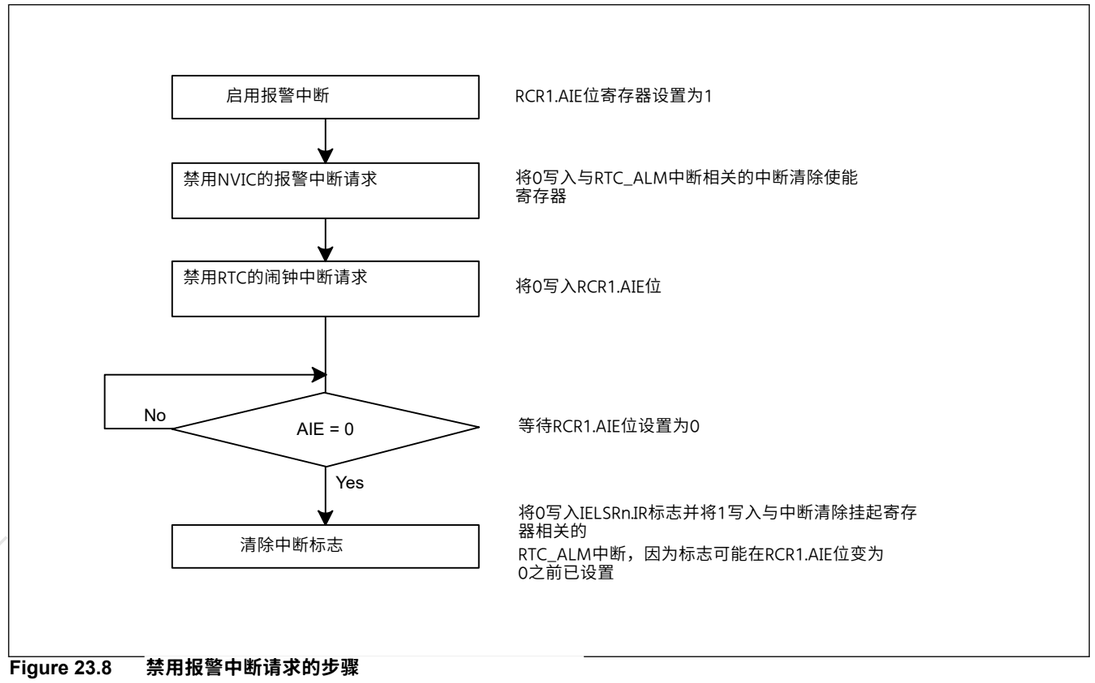


Figure 23.8 禁用报警中断请求的步骤

23.3.8 时间误差调整功能

时间误差调整功能用于校正子时钟振荡器振荡精度变化引起的时间误差，运行速度快或慢。由于在选择子时钟振荡器时，子时钟振荡器的32768个周期构成1秒的操作，因此如果子时钟频率高，则时钟运行快，如果子时钟频率低，则时钟运行慢。

时间误差调整功能包括：

- 自动调整
- 软件调整

使用RCR2.AADJE位选择自动调整或软件调整。

23.3.8.1 自动调整

通过将RCR2.AADJE位设置为1来启用自动调整。

自动调整是每次经过RCR2.AADJP位选择的调整周期后，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) 示例1：运行在32.769kHz的子时钟振荡器

调整程序

当副时钟振荡器以32.769kHz运行时，每32769个时钟周期经过1秒。RTC旨在以32768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每分钟快60个时钟周期，因此调整可以采取将时钟每分钟调回60个周期的形式。

Register settings when RCR2.CNTMD = 0:

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 60 (0x3C)

(2) Example 2: Sub-clock oscillator running at 32.766 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.766 kHz, 1 second elapses every 32766 clock cycles. The RTC is meant to run at 32768 clock cycles, so the clock runs slow by 2 clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings when RCR2.CNTMD = 0:

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 20 (0x14)

(3) Example 3: Sub-clock oscillator running at 32.764 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.764 kHz, 1 second elapses on 32764 clock cycles. Because the RTC operates for 32768 clock cycles as 1 second, the clock is delayed for 4 clock cycles per second. In 8 seconds, the delay is 32 clock cycles, therefore correction can be made by advancing the clock 32 clock cycles every 8 seconds.

Register settings when RCR2.CNTMD = 1:

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 32 (0x20)

23.3.8.2 Adjustment by software

Enable adjustment by software by setting the RCR2.AADJE bit to 0. Adjustment by software is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register on execution of a write instruction to the RADJ register.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32769 clock cycles. The RTC is meant to run at 32768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 1 clock cycle per second, so adjustment can take the form of setting the clock back by 1 cycle every second.

Register settings

- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 1 (0x10)
  This is written to the RADJ register once per 1-second interrupt.

23.3.8.3 Procedure to change the mode of adjustment

When changing the mode of adjustment, change the value of the AADJE bit in RCR2 after setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

To change adjustment by software to automatic adjustment:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 1 (automatic adjustment is enabled).

RCR2.CNTMD=0时的寄存器设置：

- RCR2.AADJP = 0 (adjustment every minute)
- ●RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 60 (0x3C)

(2) 示例2：以32.766kHz运行的子时钟振荡器

调整程序

当子时钟振荡器以32.766kHz运行时，每32766个时钟周期经过1秒。RTC旨在以32768个时钟周期运行，因此时钟每秒运行2个时钟周期。时钟上的时间每10秒慢20个时钟周期，因此调整可以采取将时钟每10秒向前设置20个周期的形式。

RCR2.CNTMD=0时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- ●RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 20 (0x14)

(3) 示例3：以32.764kHz运行的子时钟振荡器

调整程序

当副时钟振荡器以32.764kHz运行时，32764个时钟周期经过1秒。由于RTC以1秒为单位运行32768个时钟周期，因此时钟每秒延迟4个时钟周期。在8秒内，延迟为32个时钟周期，因此可以通过每8秒将时钟提前32个时钟周期来进行校正。

RCR2.CNTMD=1时的寄存器设置：

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- ●RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 32 (0x20)

23.3.8.2 软件调整

通过将RCR2.AADJE位设置为0来启用软件调整。软件调整是在对RADJ寄存器执行写指令时，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) 示例1：运行在32.769kHz的子时钟振荡器

调整程序

当副时钟振荡器以32.769kHz运行时，每32769个时钟周期经过1秒。RTC旨在以32768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每秒快1个时钟周期，因此调整可以采取将时钟每秒调回1个周期的形式。

注册设置

- ●RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 1 (0x10)
  每1秒中断一次将其写入RADJ寄存器。

23.3.8.3 更改调整模式的程序

改变调整模式时，将RADJ.PMADJ[1:0]位设置为00b后改变RCR2中的AADJE位的值（不进行调整）。

将软件调整改为自动调整：

1.将RADJ.PMADJ[1:0]位设置为00b（不进行调整）。

2.将RCR2.AADJE位设置为1（启用自动调整）。

3. Use the RCR2.AADJP bit to select the period of adjustment.
4. In RADJ, set the PMADJ[1:0] bits for addition or subtraction and the ADJ[5:0] bits to the value for use in time error adjustment.

To change automatic adjustment to adjustment by software:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 0 (adjustment by software is enabled).
3. Proceed with the adjustment by setting the RADJ.PMADJ[1:0] bits for addition or subtraction and the RADJ.ADJ[5:0] bits to the value for use in time error adjustment at the wanted time. After that, the time is adjusted every time a value is written to the RADJ register.

23.3.8.4 Procedure to stop adjustment

Stop the adjustment by setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

23.3.9 Capturing the time

The RTC is capable of storing the month, date, hour, minute and second/binary counters 3 to 0 by detecting an edge of a signal on a time capture event input pin in calendar count mode or binary count mode .

A noise filter can also be used on a time capture event input pin. If the noise filter is enabled, the RTCCRn.TCST bit is set to 1 when the input level on the pin matches three times.

The noise filter can be switched on or off for each of the time capture event input pins.Set VBTICTLR.VCHnIEN (n = 0 to 2) to 1 to enable the RTCICn input. Operation when the noise filter is off is shown in Figure 23.9 and operation when the noise filter is on is shown in Figure 23.10.

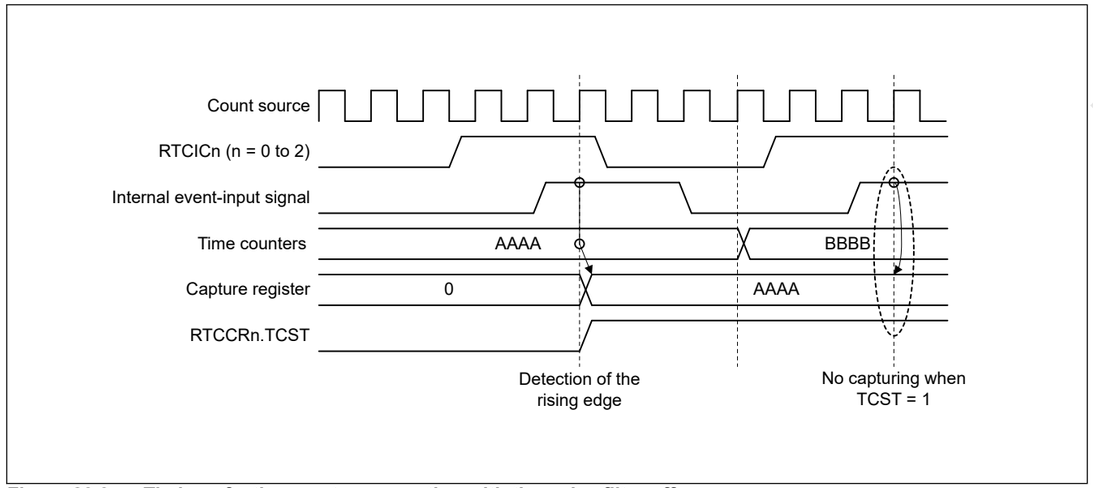


Figure 23.9 Timing of a time capture operation with the noise filter off

3.使用RCR2.AADJP位选择调整周期。

4.在RADJ中，将PMADJ[1:0]位设置为加法或减法，并将ADJ[5:0]位设置为用于时间误差调整的值。

将自动调整更改为软件调整：

1.将RADJ.PMADJ[1:0]位设置为00b（不进行调整）。

2.将RCR2.AADJE位设置为0（启用软件调整）。

3.通过将RADJ.PMADJ[1:0]位设置为加法或减法并将RADJ.ADJ[5:0]位设置为在所需时间用于时间误差调整的值，继续进行调整。之后，每次将值写入RADJ寄存器时都会调整时间。

23.3.8.4 停止调整的程序

通过将RADJ.PMADJ[1:0]位设置为00b来停止调整（不执行调整）。

23.3.9 捕捉时间

通过在日历计数模式或二进制计数模式下检测时间捕捉事件输入引脚上的信号沿，RTC能够存储月、日、小时、分钟和秒二进制计数器3到0。

噪声滤波器也可用于时间捕捉事件输入引脚。如果启用噪声滤波器，则当引脚上的输入电平匹配3次时，RTCCRn.TCST位设置为1。

可以为每个时间捕捉事件输入引脚打开或关闭噪声滤波器。将VBTICTLR.VCHnIEN（n=0到2）设置为1以启用RTCICn输入。噪声滤波器关闭时的操作如图23.9所示，噪声滤波器打开时的操作如图23.10所示。

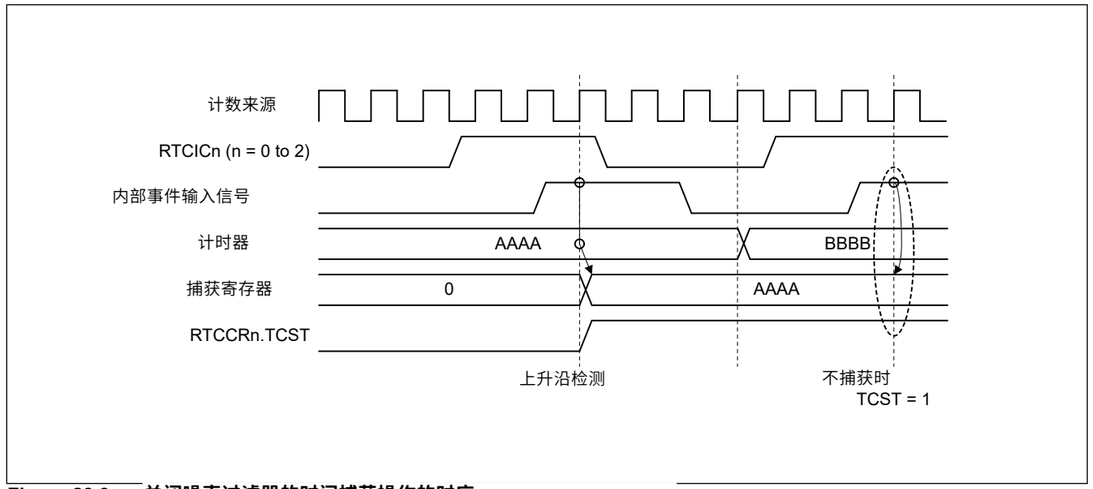


Figure 23.9 关闭噪声过滤器的时间捕获操作的时序

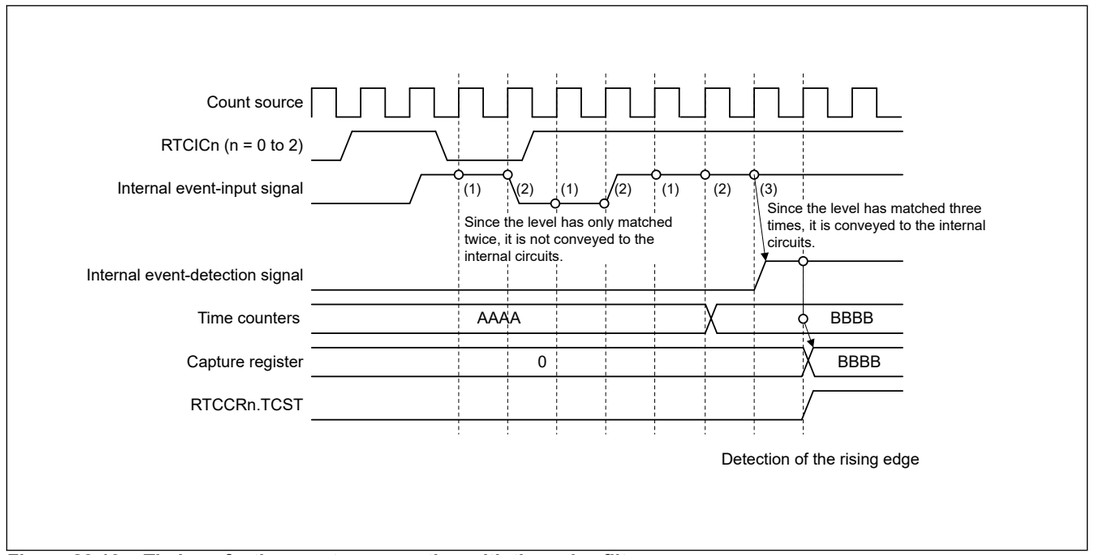


Figure 23.10 Timing of a time capture operation with the noise filter on

23.4 Interrupt Sources

The RTC has three interrupt sources, as listed in Table 23.3.

Table 23.3 RTC interrupt sources

Name	Interrupt source
RTC_ALM	Alarm interrupt
RTC_PRD	Periodic interrupt
RTC_CUP	Carry interrupt

(1) Alarm interrupt (RTC_ALM)

This interrupt is generated based on the comparison result between the alarm registers and RTC counters. For details, see section 23.3.6. Alarm Function.

Because there is a possibility that the interrupt flag might be set to 1 when the settings of the alarm registers match the clock counters, wait for the alarm time settings to be confirmed and clear the IELSRn.IR flag and the interrupt Set-Pending Register associated with the RTC_ALM interrupt to 0 again after modifying values of the alarm registers. After the interrupt flag for the alarm interrupt is set to 1 and the state is returned to mismatching of the alarm registers and clock counters, the flag is not 1 again until there is another match or the values of the alarm registers are modified again.

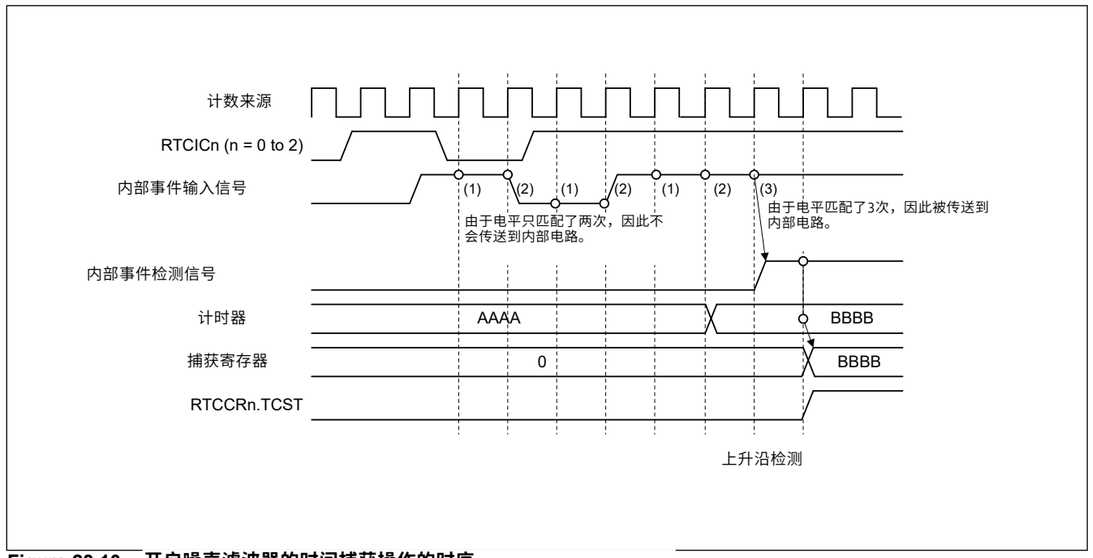


Figure 23.10 开启噪声滤波器的时间捕获操作的时序

23.4 中断源

RTC具有三个中断源，如表23.3中所列。

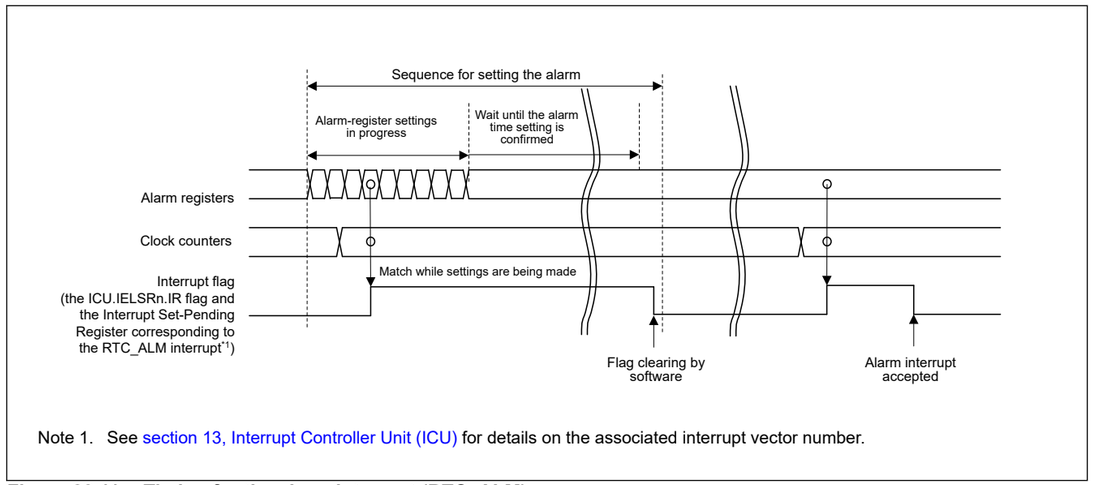
Table 23.3 RTC中断源

Name	中断源
RTC_ALM	报警中断
RTC_PRD	周期性中断
RTC_CUP	进位中断

(1) 闹钟中断(RTC_ALM)

该中断是根据闹钟寄存器和RTC计数器之间的比较结果产生的。详见23.3.6节。报警功能。

因为当闹钟寄存器的设置与时钟计数器匹配时中断标志可能被设置为1，请等待闹钟时间设置被确认并清除IELSRn.IR标志和相关的中断设置挂起寄存器修改闹钟寄存器的值后，RTC_ALM中断再次为0。报警中断的中断标志置1并返回报警寄存器和时钟计数器不匹配状态后，该标志不再为1，直到再次匹配或再次修改报警寄存器的值。



Note 1. See section 13, Interrupt Controller Unit (ICU) for details on the associated interrupt vector number.

Figure 23.11 Timing for the alarm interrupt (RTC_ALM)

(2) Periodic interrupt (RTC_PRD)

This interrupt is generated at intervals of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second. The interrupt interval can be selected in the RCR1.PES[3:0] bits.

(3) Carry interrupt (RTC_CUP)

This interrupt is generated when a carry to the second counter/binary counter 0 occurred or a carry to the R64CNT counter occurred during read access to the 64-Hz counter.

Figure 23.12 shows the timing of the carry interrupt (RTC_CPU).

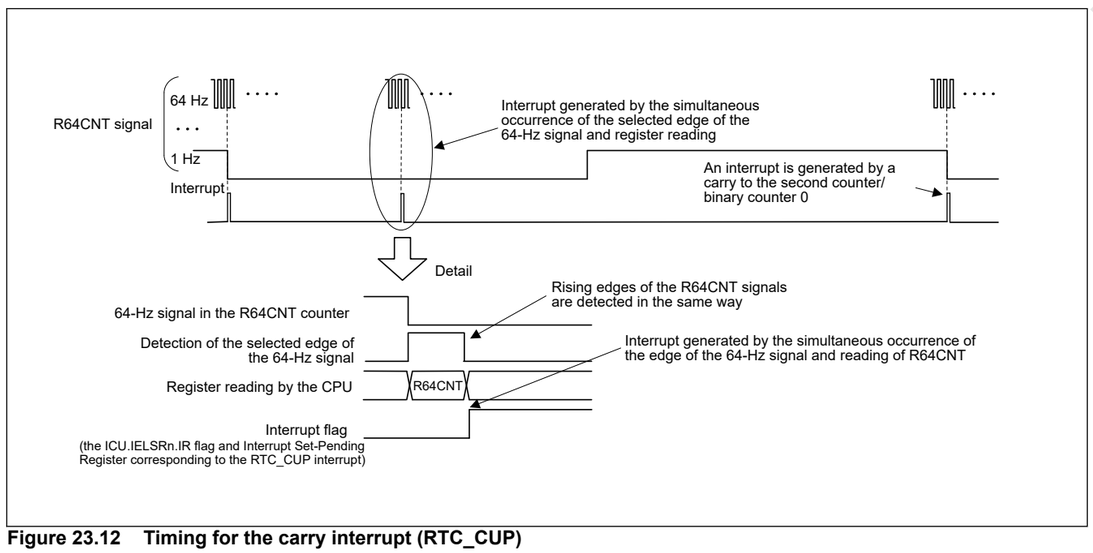
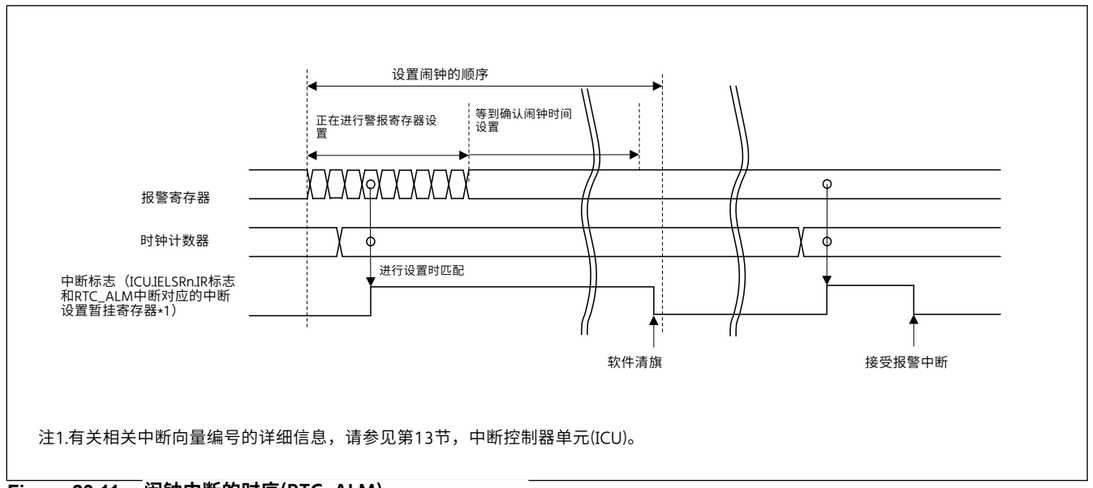


Figure 23.12 Timing for the carry interrupt (RTC_CUP)

23.5 Event Link Output

The RTC generates periodic event output (RTC_PRD) event signal for the ELC that can be used to initiate operations by other modules selected in advance.



注1.有关相关中断向量编号的详细信息，请参见第13节，中断控制器单元(ICU)。

Figure 23.11 闹钟中断的时序(RTC_ALM)

(2) 周期性中断(RTC_PRD)

此中断以2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒的间隔生成。可以在RCR1.PES[3:0]位中选择中断间隔。

(3) 进位中断(RTC_CUP)

当第二个计数器二进制计数器0的进位发生或在对64-Hz计数器的读访问期间发生对R64CNT计数器的进位时，将产生此中断。

图23.12显示了进位中断(RTC_CPU)的时序。

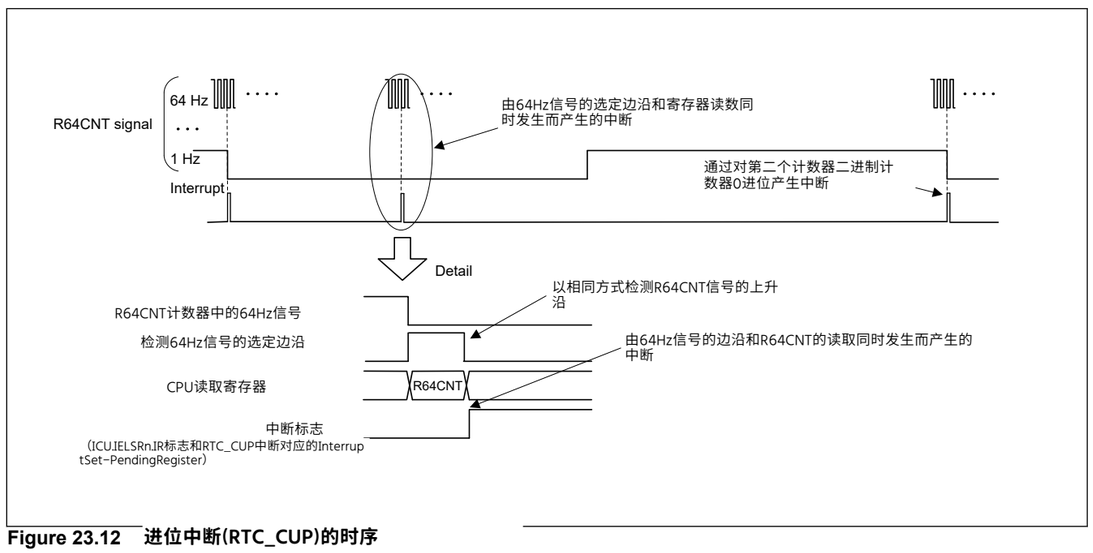


Figure 23.12 进位中断(RTC_CUP)的时序

23.5 事件链接输出

RTC为ELC生成周期性事件输出(RTC_PRD)事件信号，该信号可用于启动预先选择的其他模块的操作。

The periodic event signal is output at the interval selected from 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, and 2 seconds by setting the RCR1.PES[3:0] bits.

The event generation period immediately after the event generation is selected is not guaranteed.

Note: If event linking from the RTC is used, only set the ELC after setting the RTC, for example initialization and time settings. Setting the RTC after the ELC can lead to output of unexpected event signals.

23.5.1 Interrupt Handling and Event Linking

The RTC has a bit to enable or disable periodic interrupts. An interrupt request signal is output to the CPU when an interrupt source is generated while the associated enable bit is enabled.

In contrast, an event link output signal is sent to other modules as an event signal through the ELC when an interrupt source is generated, regardless of the setting of the associated interrupt enable bit.

Note: Although alarm and periodic interrupts can still be output during Software Standby or Deep Software Standby mode, the periodic event signals for the ELC are not output.

23.6 Usage Notes

23.6.1 Register Writing during Counting

The following registers should not be written to during counting, that is, while the RCR2.START bit is 1:

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL

The counter should be stopped before writing to any of these registers.

23.6.2 Use of Periodic Interrupts

Figure 23.13 shows the procedure for using periodic interrupts.

The generation and period of the periodic interrupt can be changed by setting the RCR1.PES[3:0] bits. However, because the prescaler R64CNT and RSECCNT/BCNT0 are used to generate interrupts, the interrupt period is not guaranteed immediately after setting the RCR1.PES[3:0] bits.

In addition, any of the following operation can affect the interrupt period:

- Stopping/restarting or resetting counter operation
- Reset by RTC software
- 30-second adjustment by changing the RCR2 value

When the time error adjustment function is used, the interrupt generation period after adjustment is added or subtracted based on the adjustment value.

通过设置RCR1.PES[3:0，以从1256、1128、164、132、116、18、14、12、1和2秒中选择的间隔输出周期性事件信号]位。

不保证选择事件生成后的事件生成周期。

Note: 如果使用来自RTC的事件链接，请仅在设置RTC后设置ELC，例如初始化和时间设置。在ELC之后设置RTC会导致意外事件信号的输出。

23.5.1 中断处理和事件链接

RTC有一个位来启用或禁用周期性中断。当相关使能位使能时产生中断源时，将向CPU输出中断请求信号。

相反，当产生中断源时，事件链接输出信号作为事件信号通过ELC发送到其他模块，而不管相关中断使能位的设置如何。

Note: 尽管在软件待机或深度软件待机模式下仍可输出警报和周期性中断，但不会输出ELC的周期性事件信号。

23.6 使用说明

23.6.1 计数期间的寄存器写入

计数期间不应写入以下寄存器，即RCR2.START位为1时：

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL

在写入任何这些寄存器之前，应停止计数器。

23.6.2 使用周期性中断

图23.13显示了使用周期性中断的过程。

可以通过设置RCR1.PES[3:0]位来更改周期性中断的产生和周期。但是，因为预分频器R64CNT和RSECCNTBCNT0用于产生中断，所以在设置RCR1.PES[3:0]位后不能立即保证中断周期。

此外，以下任何操作都会影响中断周期：

- ●停止重新启动或重置计数器操作
- ●RTC软件复位
- ●通过改变RCR2值进行30秒调整

使用时间误差调整功能时，根据调整值加减调整后的中断产生周期。

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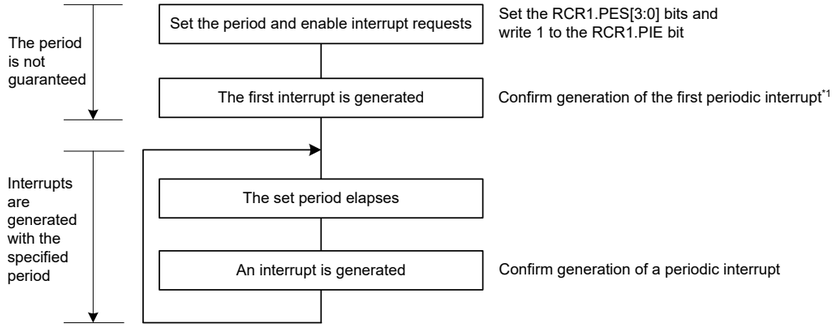


Note 1. When an interrupt generation period changes while the periodic interrupt is used, an interrupt might be generated at the completion of the setting. If the interrupt is generated immediately after the setting, the period is not guaranteed for two interrupts including the current interrupt.

Figure 23.13 Using the periodic interrupt function

23.6.3 RTCOUT (1-Hz/64-Hz) Clock Output

Stopping/restarting or resetting counter operation, reset by RTC software, and the 30-second adjustment by changing the RCR2 value affects the period of RTCOUT (1-Hz/64-Hz) output. When the time error adjustment function is used, the period of RTCOUT (1-Hz/64-Hz) output after adjustment is added or subtracted based on the adjustment value.

23.6.4 Transitions to Low Power Modes after Setting Registers

A transition to a low power state (Software Standby mode, Deep Software Standby mode, or battery backup state) during a write to an RTC register might corrupt the value of the register. After setting the register, confirm that the setting is in place before initiating a transition to a low power state.

23.6.5 Notes on Writing to and Reading from Registers

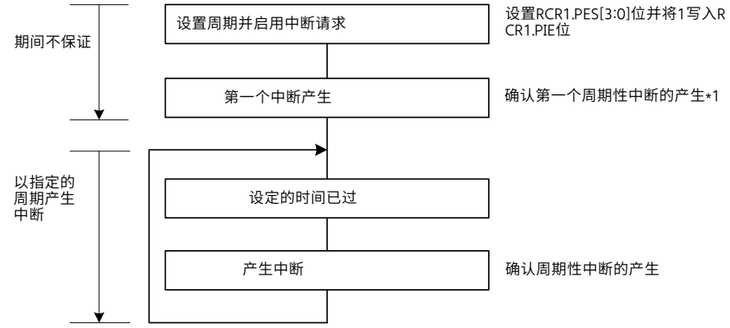
- When reading a counter register such as the second counter after writing to the counter register, follow the procedure in section 23.3.5. Reading 64-Hz Counter and Time.
- The value written to the count registers, alarm registers, year alarm enable register, bits RCR2.AADJE, AADJP, and HR24, RCR4 register, or frequency register is reflected when fourth read operations are performed after writing.
- The values written to the RCR1.CIE, RCR1.RTCOS, and RCR2.RTCOE bits can be read immediately after writing.
- To read the value from the timer counter after returning from a reset or a period in Software Standby mode, Deep Software Standby mode, or battery backup state, wait for 1/128 second while the clock is operating (RCR2.START bit = 1).
- After a reset is generated, write to the RTC register after 6 cycles of the count source clock have elapsed.

23.6.6 Changing the Count Mode

When changing the count mode (calendar count mode/binary count mode), set the RCR2.START bit to 0, stop the counting operation, then start it again from the initial setting. For details on the initial setting, see section 23.3.1. Outline of Initial Settings of Registers after Power On.

23.6.7 Initialization Procedure When the RTC Is Not to Be Used

Registers in the RTC are not initialized by a reset. Depending on the initial state, the generation of an unintentional interrupt request or operation of the counter might lead to increased power consumption.



注1.当使用周期性中断时中断产生周期发生变化时，可能会在设置完成时产生中断。如果设置后立即产生中断，则不保证包括当前中断在内的两次中断的周期。

Figure 23.13 使用周期性中断功能

23.6.3 RTCOUT(1-Hz64-Hz)时钟输出

停止重新启动或重置计数器操作，通过RTC软件重置，并通过更改30秒调整RCR2值影响RTCOUT(1-Hz64-Hz)输出的周期。使用时间误差调整功能时，调整后的RTCOUT（1-Hz64-Hz）输出的周期根据调整值加减。

23.6.4 设置寄存器后转换到低功耗模式

在写入RTC寄存器期间转换到低功耗状态（软件待机模式、深度软件待机模式或电池备份状态）可能会损坏寄存器的值。设置寄存器后，在开始转换到低功耗状态之前确认设置到位。

23.6.5 关于写入和读取寄存器的注意事项

●在写入计数器寄存器后读取第二个计数器等计数器寄存器时，请按照第23.3.5节。读取64-Hz计数器和时间。

●写入计数寄存器、报警寄存器、年报警使能寄存器、RCR2.AADJE、AADJP位和HR24、RCR4寄存器或频率寄存器的值在写入后执行第四次读操作时反映。

●写入RCR1.CIE、RCR1.RTCOS和RCR2.RTCOE位的值可在写入后立即读取。

●要在软件待机模式下从复位或一段时间返回后从定时器计数器读取值，Deep软件待机模式或电池备份状态在时钟运行时等待1128秒（RCR2.START位=1）。

●产生复位后，经过6个计数源时钟周期后写入RTC寄存器。

23.6.6 更改计数模式

当改变计数模式（日历计数模式二进制计数模式）时，将RCR2.START位设置为0，停止计数操作，然后从初始设置重新开始。有关初始设置的详细信息，请参阅第23.3.1节。上电后寄存器的初始设置概要。

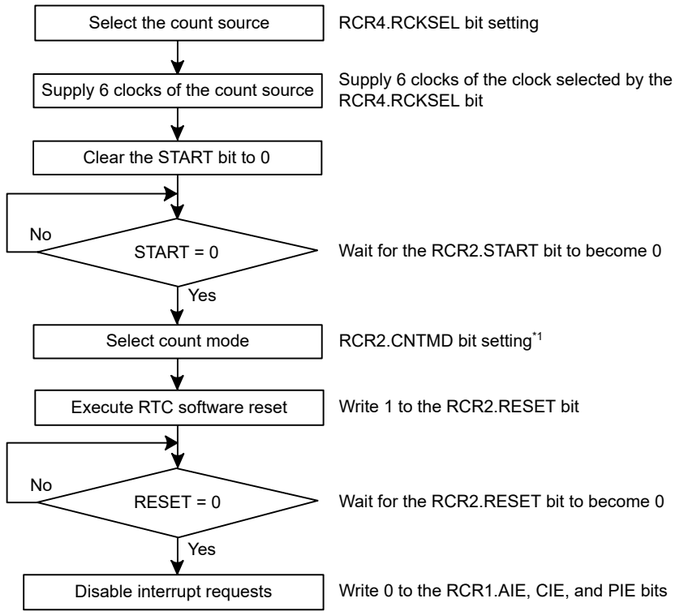
23.6.7 不使用RTC时的初始化程序

RTC中的寄存器不会因复位而初始化。根据初始状态，意外中断请求的生成或计数器的操作可能会导致功耗增加。

For applications that do not require a realtime clock, initialize the registers by following the initialization procedure shown in Figure 23.14.

Alternatively, when the sub-clock oscillator is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (sub-clock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock oscillator. To stop the sub-clock oscillator, write 1 to the SOSCCR.SOSTP bit.

For details on the setting of the SOSCCR.SOSTP bit, see section 8, Clock Generation Circuit.



Note 1. This step is not necessary if the count mode is concurrently set by setting the START bit to 0.

Figure 23.14 Initialization procedure

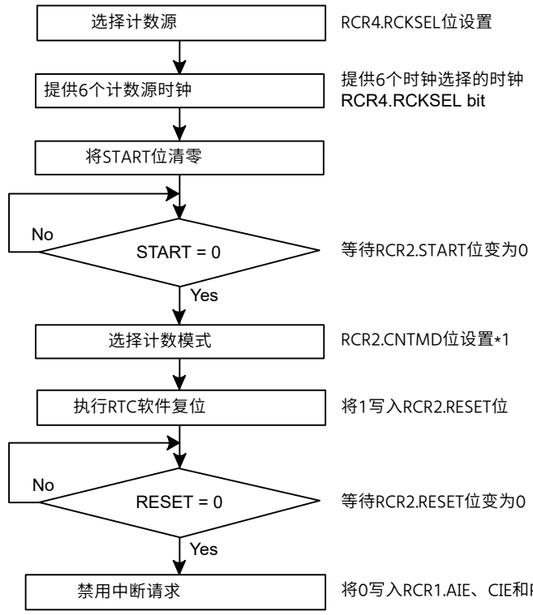
23.6.8 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. If the RTC periodical interrupt or RTC periodical event output was generated at this time, the interrupt or event is invalid.

对于不需要实时时钟的应用程序，按照图23.14所示的初始化过程初始化寄存器。

或者，当副时钟振荡器不用作系统时钟或实时时钟时，可以通过向RCR4.RCKSEL位写入0（选择副时钟振荡器）并停止副时钟振荡器来停止计数器。要停止副时钟振荡器，向SOSCCR.SOSTP位写入1。

有关SOSCCR.SOSTP位设置的详细信息，请参见第8节，时钟生成电路。



注1.如果通过将START位设置为0同时设置计数模式，则不需要此步骤。

Figure 23.14 初始化程序

23.6.8 切换源时钟时

当通过改变SCKSCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。如果此时产生了RTC周期性中断或RTC周期性事件输出，则该中断或事件无效。

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24. Watchdog Timer (WDT)

24.1 Overview

The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.

Table 24.1 lists the WDT specifications and Figure 24.1 shows a block diagram.

Table 24.1 WDT specifications

Parameter	Specifications
Count source*1	Peripheral clock (PCLKB)
Clock division ratio	Division by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Auto start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register • Only secure developer can select Auto-start mode or Register-start mode
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output
TrustZone Filter	Security attribution can be set

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

24. 看门狗定时器(WDT)

24.1 Overview

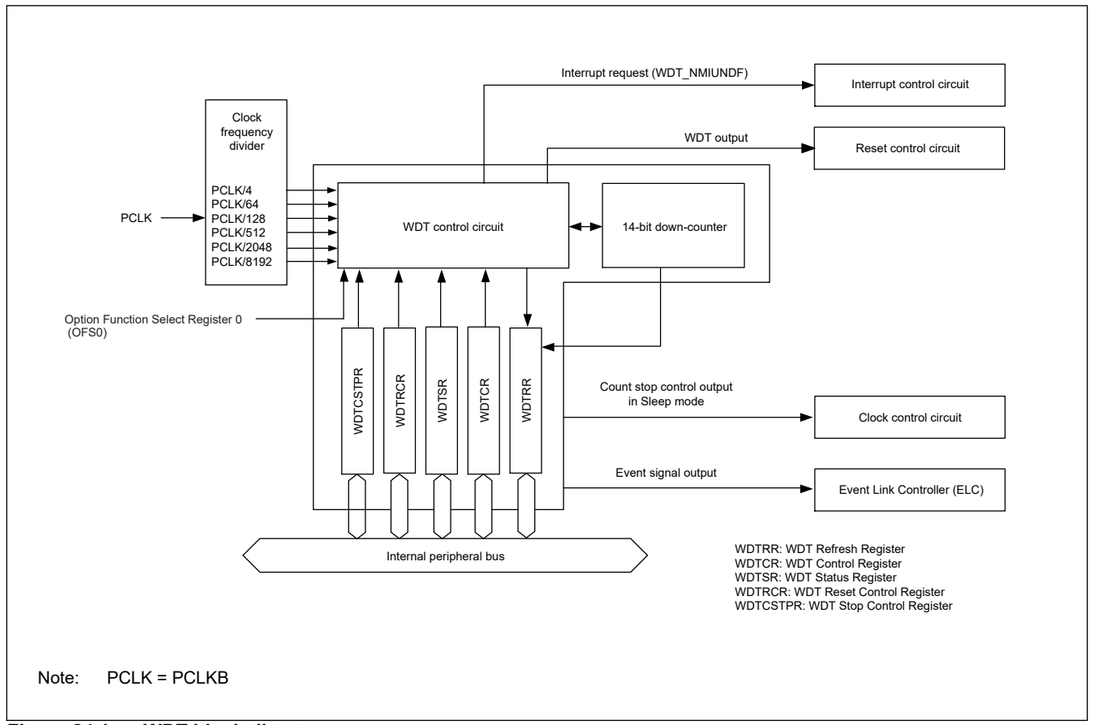
看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。

表24.1列出了WDT规范，图24.1显示了框图。

Table 24.1 WDT specifications

Parameter	Specifications
计数来源*1	外设时钟(PCLKB)
时钟分频比	除以4、64、128、512、2048或8192
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	• 自动启动模式：复位后或发生下溢或刷新错误后自动开始计数 • 寄存器启动模式：通过写入WDTRR寄存器以刷新开始计数 • 只有安全的开发人员可以选择自动启动模式或注册启动模式
停止计数器的条件	• 复位（递减计数器和其他寄存器恢复初始值） • 计数器下溢或产生刷新错误
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
看门狗定时器复位源	• Down-counter underflows • 刷新允许时间之外的刷新（刷新错误）
Non-maskable interrupt/interrupt sources	• Down-counter underflows • 刷新允许时间之外的刷新（刷新错误）
读取计数器值	递减计数器的值可以通过WDTSR寄存器读取
事件链接功能（输出）	• 递减计数器下溢事件输出 • 刷新错误事件输出
输出信号（内部信号）	• 复位输出 • 中断请求输出 • 休眠模式计数停止控制输出
TrustZone Filter	可设置安全属性

注1.满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。



Note: PCLK = PCLKB

Figure 24.1 WDT block diagram

24.2 Register Descriptions

24.2.1 WDTRR : WDT Refresh Register

Base address: WDT = 0x4008_3400

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

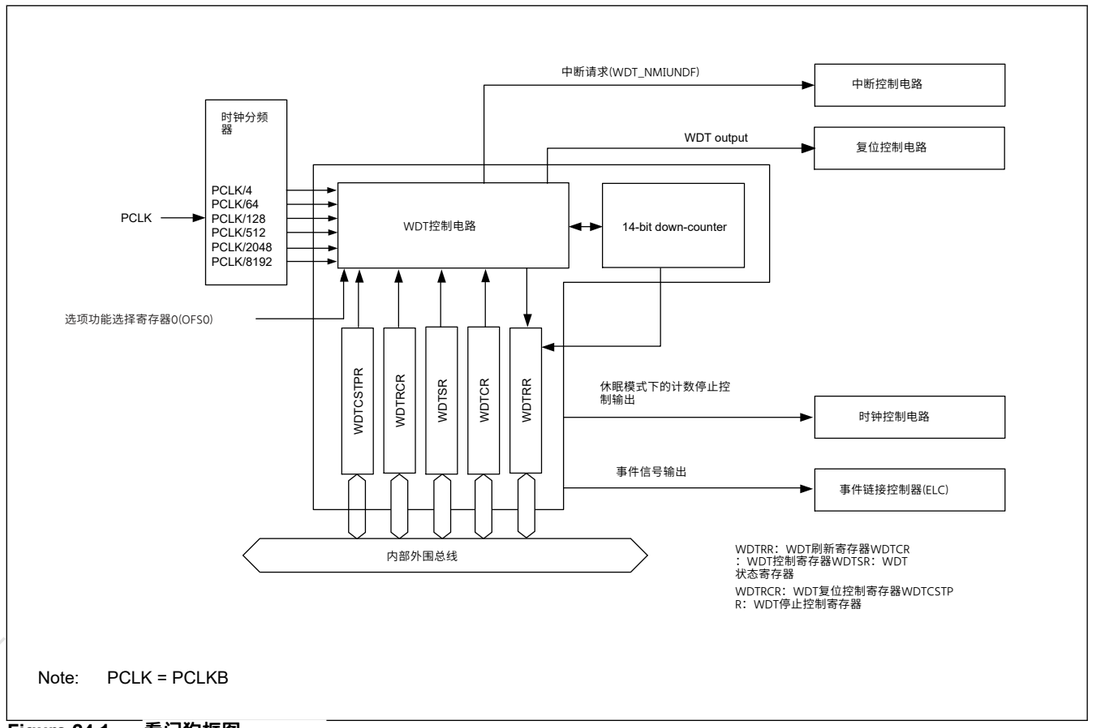
Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register.	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 0x00 and then writing 0xFF to WDTRR register (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected by setting the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in the Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected by setting the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 24.3.3. Refresh Operation.



Note: PCLK = PCLKB

Figure 24.1 看门狗框图

24.2 注册说明

24.2.1 WDTRR:WDT刷新寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x00

Bit position:	7							0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	通过写入0x00然后将0xFF写入该寄存器来刷新递减计数器。	R/W

WDTRR寄存器刷新WDT的递减计数器。

WDT的递减计数器通过在允许刷新期间内写入0x00然后将0xFF写入WDTRR寄存器（刷新操作）来刷新。

递减计数器刷新后，在自动启动模式下，它从通过设置选项功能选择寄存器0中的WDT超时周期选择位(OFS0.WDTTOPS[1:0])选择的值开始递减计数。在寄存器启动模式下，倒计时从通过设置WDT控制寄存器中的超时周期选择位(WDTCR.TOPS[1:0])选择的值开始。

写入0x00时，读取值为0x00。写入0x00以外的值时，读取的值为0xFF。有关刷新操作的详细信息，请参阅第24.3.3节。刷新操作。

24.2.2 WDTCR : WDT Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	Timeout Period Select 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
7:4	CKS[3:0]	Clock Division Ratio Select 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 Others: Setting prohibited	R/W
9:8	RPES[1:0]	Window End Position Select 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (do not specify window end position).	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W
13:12	RPSS[1:0]	Window Start Position Select 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (do not specify window start position).	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

The WDTCR register is used to set the clock division ratio, and window start and end positions for refresh, and the timeout period until the down-counter underflows in register start mode.

Some constraints apply to writes to the WDTCR register. For details, see section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in the Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made in the OFS0 register. For details, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the number of PCLKB cycles until the counter underflows.

Table 24.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

24.2.2 WDTCR:WDT控制寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
重置后的值：	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Function	R/W
1:0	TOPS[1:0]	超时时间选择 0 0: 1024 cycles (0x03FF) 0 1: 4096 cycles (0x0FFF) 1 0: 8192 cycles (0x1FFF) 1 1: 16384 cycles (0x3FFF)	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
7:4	CKS[3:0]	时钟分频比选择 0x1: PCLKB/4 0x4: PCLKB/64 0xF: PCLKB/128 0x6: PCLKB/512 0x7: PCLKB/2048 0x8: PCLKB/8192 其他：禁止设置	R/W
9:8	RPES[1:0]	窗口结束位置选择 00：75%01：50%10：25%11：0%（不指定 窗口结束位置）。	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W
13:12	RPSS[1:0]	窗口起始位置选择 00：25%01：50%10：75%11：100%（不指定 窗口起始位置）。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

WDTCR寄存器用于设置时钟分频比、刷新的窗口开始和结束位置，以及在寄存器开始模式下直到递减计数器下溢的超时时间。

一些限制适用于写入WDTCR寄存器。详见24.3.2节。控制对WDTCR的写入，WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，禁用WDTCR寄存器中的设置，启用选项功能选择寄存器0(OFS0)中的设置。WDTCR寄存器的设置也可以在OFS0寄存器中进行。详见24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

TOPS[1:0]位（超时周期选择）

TOPS[1:0]位从1024、4096、8192和16384个周期中选择超时周期，直到递减计数器下溢的周期，以CKS[3:0]位中指定的分频时钟为1个周期.向下计数器刷新后，CKS[3:0]和TOPS[1:0]位的组合决定了PCLKB周期数，直到计数器下溢。

表24.2列出了CKS[3:0]和TOPS[1:0]位设置、超时时间和
PCLKB cycles.

Table 24.2 Timeout period settings

CKS[3:0] bits	TOPS[1:0] bits	Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the PCLKB divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, this allows the WDT to be configured to a count period between 4096 and 134217728 PCLKB clock cycles.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the value for the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window end position is set to 0%.

Table 24.3 lists the counter values for the window start and end positions, and Figure 24.2 shows the refresh-permitted period set in the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 24.2 超时时间设置

CKS[3:0] bits	TOPS[1:0] bits	时钟分频比	超时时间（周期数）	PCLKB时钟周期
0x1	00b	PCLKB/4	1024	4096
	01b		4096	16384
	10b		8192	32768
	11b		16384	65536
0x4	00b	PCLKB/64	1024	65536
	01b		4096	262144
	10b		8192	524288
	11b		16384	1048576
0xF	00b	PCLKB/128	1024	131072
	01b		4096	524288
	10b		8192	1048576
	11b		16384	2097152
0x6	00b	PCLKB/512	1024	524288
	01b		4096	2097152
	10b		8192	4194304
	11b		16384	8388608
0x7	00b	PCLKB/2048	1024	2097152
	01b		4096	8388608
	10b		8192	16777216
	11b		16384	33554432
0x8	00b	PCLKB/8192	1024	8388608
	01b		4096	33554432
	10b		8192	67108864
	11b		16384	134217728

CKS[3:0]位（时钟分频比选择）

CKS[3:0]位指定用于递减计数器的时钟的分频比。分频比可以从PCLKB除以4、64、128、512、2048和8192中选择。结合TOPS[1:0]位设置，这允许将WDT配置为4096和134217728个PCLKB时钟周期。

RPES[1:0]位（窗口结束位置选择）

RPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口起始位置的值（窗口起始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

RPSS[1:0]位（窗口起始位置选择）

RPSS[1:0]位指定指示允许刷新周期的窗口起始位置。可以为窗口起始位置选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置设置为小于或等于窗口结束位置的值，则窗口结束位置设置为0%。

表24.3列出了窗口开始和结束位置的计数器值，图24.2显示了在RPSS[1:0]、RPES[1:0]和TOPS[1:0]位中设置的允许刷新周期。

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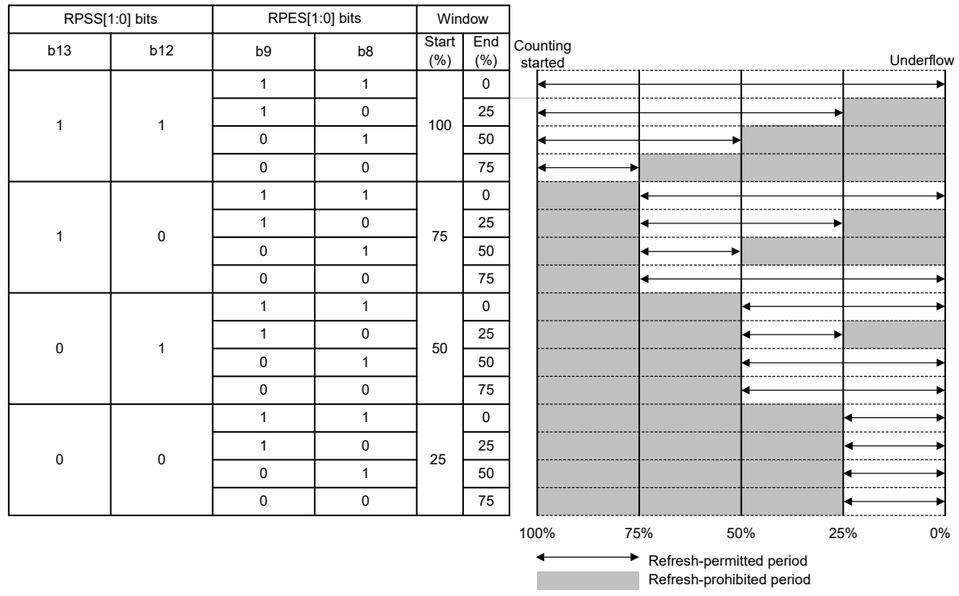
Table 24.3 Relationship between the timeout period and window start and end counter values

TOPS[1:0]	Timeout period		Window start and end counter value			
	Cycles	Counter value	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 24.2 RPSS[1:0] and RPES[1:0] bits setting and refresh-permitted period

24.2.3 WDTSR : WDT Status Register

Base address: WDT = 0x4008_3400

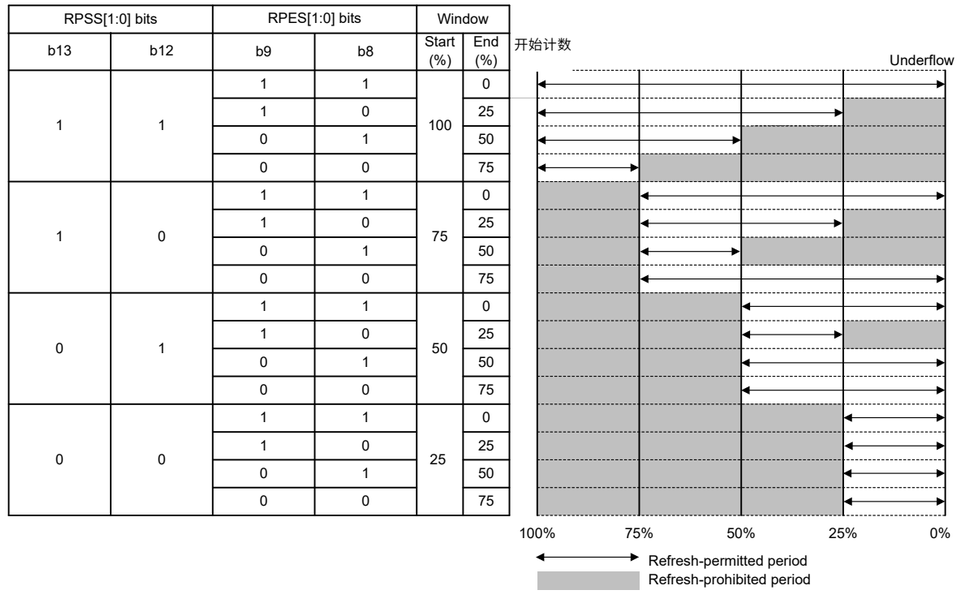
Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1

Table 24.3 超时时间与窗口开始和结束计数器值之间的关系

TOPS[1:0]	超时时间		窗口开始和结束计数器值			
	Cycles	计数器值	100%	75%	50%	25%
00b	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
01b	4096	0x0FFF	0x0FFF	0x0BFF	0x07FF	0x03FF
10b	8192	0x1FFF	0x1FFF	0x17FF	0x0FFF	0x07FF
11b	16384	0x3FFF	0x3FFF	0x2FFF	0x1FFF	0x0FFF



Note: 如果窗口结束设置≥窗口开始设置，则窗口结束设置设置为0%。

Figure 24.2 RPSS[1:0]和RPES[1:0]位设置和允许刷新周期

24.2.3 WDTSR:WDT状态寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-Counter Value 递减计数器计数的值	R
14	UNDFF	Underflow Flag 0：未发生下溢1：发生下溢	R/W*1

Bit	Symbol	Function	R/W
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The WDTSR register indicates the counter value of the down-counter and the status of whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the counter. A value of 1 indicates that the down counter underflowed. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred, indicating that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

24.2.4 WDTRCR : WDT Reset Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
15	REFEF	刷新错误标志 0：未发生刷新错误1：发生刷新错误	R/W*1

注1.只能写入0来清除标志。

WDTSR寄存器指示递减计数器的计数值以及递减计数器是否发生下溢或刷新错误的状态。

CNTVAL[13:0] bits (Down-Counter Value)

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认计数器是否发生下溢。值1表示递减计数器下溢。将0写入标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+1)个PCLKB周期。此外，在下溢后的(N+1)个PCLKB周期内忽略标志的清除。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

REFEF标志（刷新错误标志）

读取REFEF标志，确认是否发生刷新错误，表示在禁止期间进行了刷新操作。值1表示发生了刷新错误。将0写入标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+1)个PCLKB周期。此外，在刷新错误后的(N+1)个PCLKB周期内，标志的清除将被忽略。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0x1, N = 4
- When WDTCR.CKS[3:0] = 0x4, N = 64
- When WDTCR.CKS[3:0] = 0xF, N = 128
- When WDTCR.CKS[3:0] = 0x6, N = 512
- When WDTCR.CKS[3:0] = 0x7, N = 2048
- When WDTCR.CKS[3:0] = 0x8, N = 8192

24.2.4 WDTRCR:WDT复位控制寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RSTIRQS	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	RSTIRQS	Reset Interrupt Request Select 0: Enable non-maskable interrupt request or interrupt request output 1: Enable reset output	R/W

The WDTRCR register controls reset output by a WDT down-counter underflow or interrupt request output.

Some constraints apply to writes to the WDTRCR register. For details, see section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTRCR register can also be made for the OFS0 register. For details, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

24.2.5 WDTCSTPR : WDT Count Stop Control Register

Base address: WDT = 0x4008_3400

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	SLCSTP	WDT Count Stop Control Register 0: Disable count stop 1: Stop count on transition to Sleep mode	R/W

The WDTCSTPR register controls whether to stop the WDT counter in a low power mode. Some constraints apply to writes to the WDTCSTPR register. For details, see section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in the Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (WDT Count Stop Control Register)

The SLCSTP bit selects whether to stop counting on transition to Sleep mode, Snooze, or Software Standby mode.

24.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 24.3.8. Association between Option Function Select Register 0 (OFS0) and WDT Registers.

24.3 Operation

24.3.1 Count Operation in each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting starts with a refresh by writing to the register.

In auto start mode, counting automatically starts after a release from the reset state according to the settings in the Option Function Select register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the WDTRR register after the respective registers are set after a release from the reset state.

Bit	Symbol	Function	R/W
7	RSTIRQS	复位中断请求选择 0：使能不可屏蔽中断请求或中断请求输出1：使能复位输出	R/W

WDTRCR寄存器通过WDT递减计数器下溢或中断请求输出控制复位输出。

一些限制适用于写入WDTRCR寄存器。详见24.3.2节。控制写入WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTRCR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。WDTRCR寄存器的设置也可以对OFS0寄存器进行。详见24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

24.2.5 WDTCSTPR:WDT计数停止控制寄存器

Base address: WDT = 0x4008_3400

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SLCSTP	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	SLCSTP	WDT计数停止控制寄存器 0：禁用计数停止1：转换到睡眠模式时停止计数	R/W

WDTCSTPR寄存器控制是否在低功耗模式下停止WDT计数器。一些限制适用于写入WDTCSTPR寄存器。详见24.3.2节。控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

在自动启动模式下，WDTCSTPR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。也可以对OFS0寄存器进行WDTCSTPR寄存器的设置。详见24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

SLCSTP位（WDT计数停止控制寄存器）

SLCSTP位选择在转换到休眠模式、贪睡或软件待机模式时是否停止计数。

24.2.6 选项功能选择寄存器0(OFS0)

有关OFS0寄存器的信息，请参见第24.3.8节。选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

24.3 Operation

24.3.1 每种启动模式下的计数操作

WDT有两种启动模式：

●自动启动模式，从复位状态释放后自动开始计数

●寄存器启动模式，通过写入寄存器，从刷新开始计数。

在自动启动模式下，根据选项中的设置从复位状态释放后自动开始计数
功能选择闪存中的寄存器0(OFS0)。

在寄存器启动模式下，在从复位状态释放后，在设置各个寄存器后，通过写入WDTRR寄存器，从刷新开始计数。

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register.

When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

When the register start mode is selected, the setting for the OFS0 register is disabled while the settings for the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

24.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected and the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

After the reset state is released, set the following to Sleep mode in the WDTCSTPR register:

- Clock division ratio
- Window start and end positions
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transitions to Sleep mode in the WDTCSTPR register

Refresh the down-counter to start counting down from the value set in the Timeout Period Selection bits (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs the reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). Non-maskable interrupt requests or interrupt requests can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 24.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b)

通过设置OFS0寄存器中的WDT启动模式选择位(OFS0.WDTSTRT)来选择自动启动模式或寄存器启动模式。

选择自动启动模式后，WDT控制寄存器（WDTCR）中的设置，WDTRESET控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）在启用OFS0寄存器中的设置时被禁用。

选择寄存器启动模式时，在WDT控件的设置时禁用OFS0寄存器的设置
使能寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

24.3.1.1 注册启动模式

当WDT启动模式选择位(OFS0.WDTSTRT)为1时，选择寄存器启动模式并启用WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

释放复位状态后，在WDTCSTPR寄存器中将以下内容设置为休眠模式：

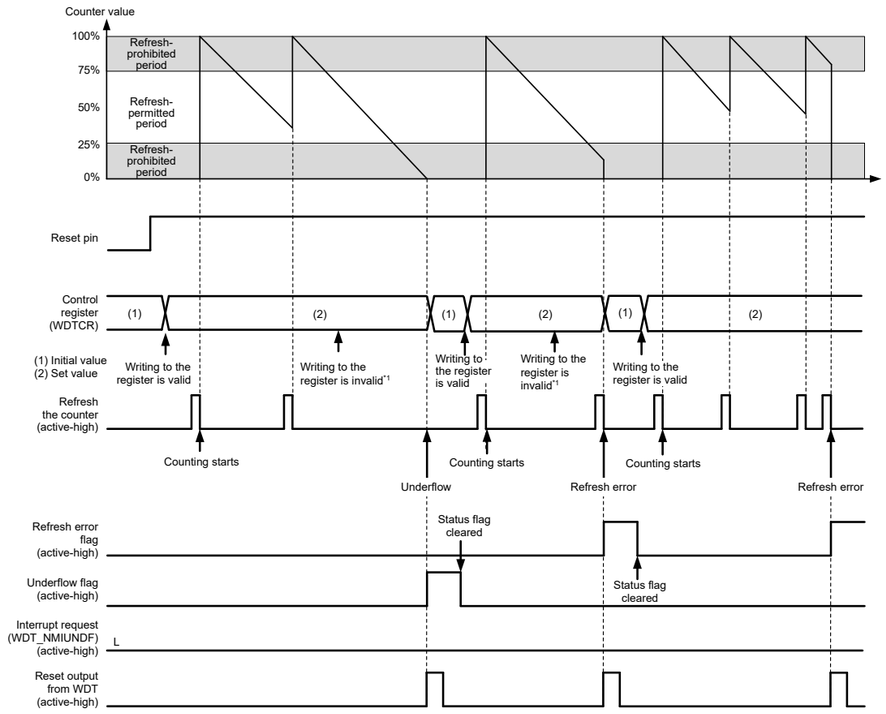
- ●时钟分频比
- ●窗口开始和结束位置
- ●WDTCR寄存器中的超时时间
- ●WDTRCR寄存器中的复位输出或中断请求输出
- ●WDTCSTPR寄存器中转换到休眠模式期间的计数器停止控制

刷新递减计数器以从超时周期选择位(WDTCR.TOPS[1:0])中设置的值开始递减计数。

此后，只要在可刷新期间刷新了计数器，则每次刷新计数器时都会重置计数器中的值，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果由于程序失控导致递减计数器无法刷新而导致递减计数器下溢，或者由于计数器在刷新允许时间之外刷新而发生刷新错误，则WDT输出复位信号或非可屏蔽中断请求中断请求(WDT_NMIUNDF)。可以在WDT复位中断请求选择位(WDTRCR.RSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断 允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图24.3显示了以下条件下的操作示例：

- ●寄存器启动模式（OFS0.WDSTSTRT=1）
- ●启用复位输出(WDTRCR.RSTIRQS=1)
- ●窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)
- ●窗口结束位置为25%(WDTCR.RPES[1:0]=10b)



Note: See section 24.3.2. Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.
Reset pin = RES

Figure 24.3 Operation example in register start mode

24.3.1.2 Auto start mode

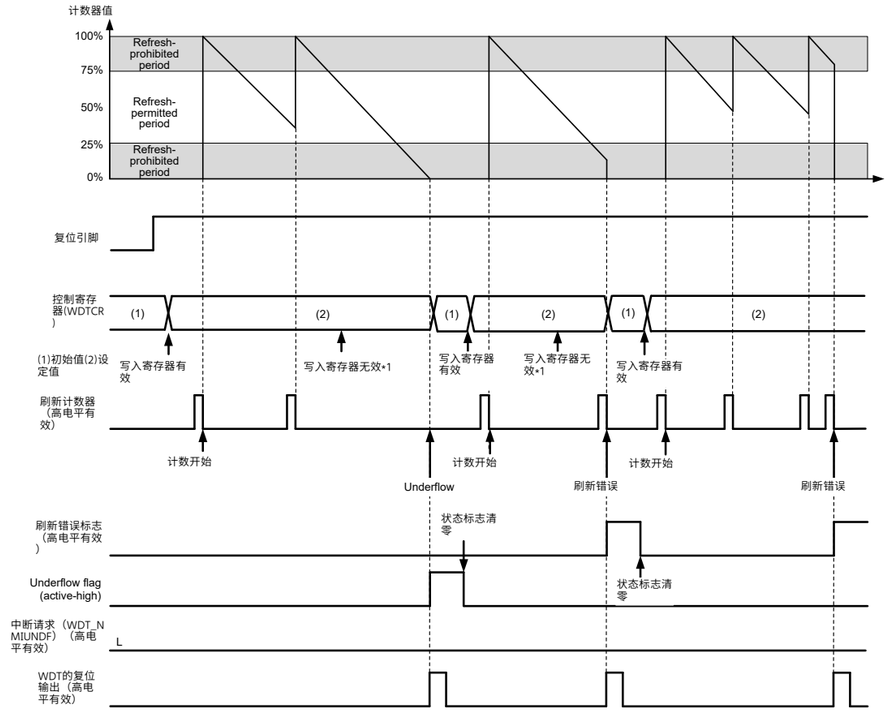
When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected, the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control during transition to Sleep mode

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and counting down continues. The WDT does not output the reset signal as long as the counting continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to a



Note: 请参阅第24.3.2节。控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。
复位引脚=RES

Figure 24.3 寄存器启动模式下的操作示例

24.3.1.2 自动启动模式

当WDT启动模式选择位置（OFS0.WDTSTSTRT）中的选项功能选择寄存器0（OFS0）为0时，选择了自动启动模式，WDT控制寄存器（WDTCR）（WDTCR），WDTRESETRESETCONTROMCONTROL寄存器（WDTRCR）和WDTCountCountCountCountCount停止控制寄存器(WDTCSTPR)被禁用，而OFS0寄存器中的设置被启用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
WDT registers:

- ●时钟分频比
- ●窗口开始和结束位置
- ●超时时间
- ●复位输出或中断请求
- ●转换到睡眠模式期间的计数器停止控制

当复位状态解除时，递减计数器自动从WDT中设置的值开始递减计数
超时周期选择位(OFS0.WDTTOPS[1:0])。

此后，只要在可刷新期间刷新了计数器，则每次刷新计数器时都会重置计数器中的值，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果递减计数器下溢，因为递减计数器的刷新是不可能的，因为

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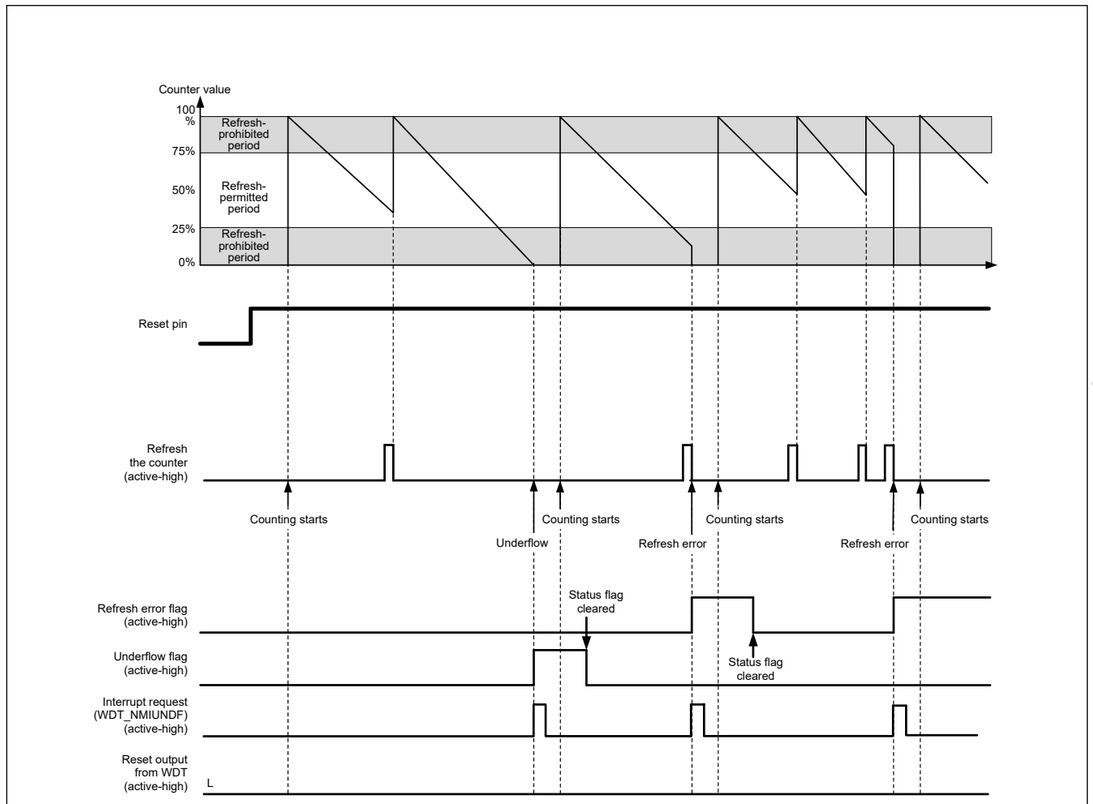
runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT outputs the reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected by setting the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/ Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 24.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.WDTRSTIRQS = 0)
- The window start position is 75% (OFS0.WDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.WDTRPES[1:0] = 10b)



Note: Reset pin = RES

Figure 24.4 Operation example in auto start mode

24.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once between the release from the reset state and the first refresh operation.

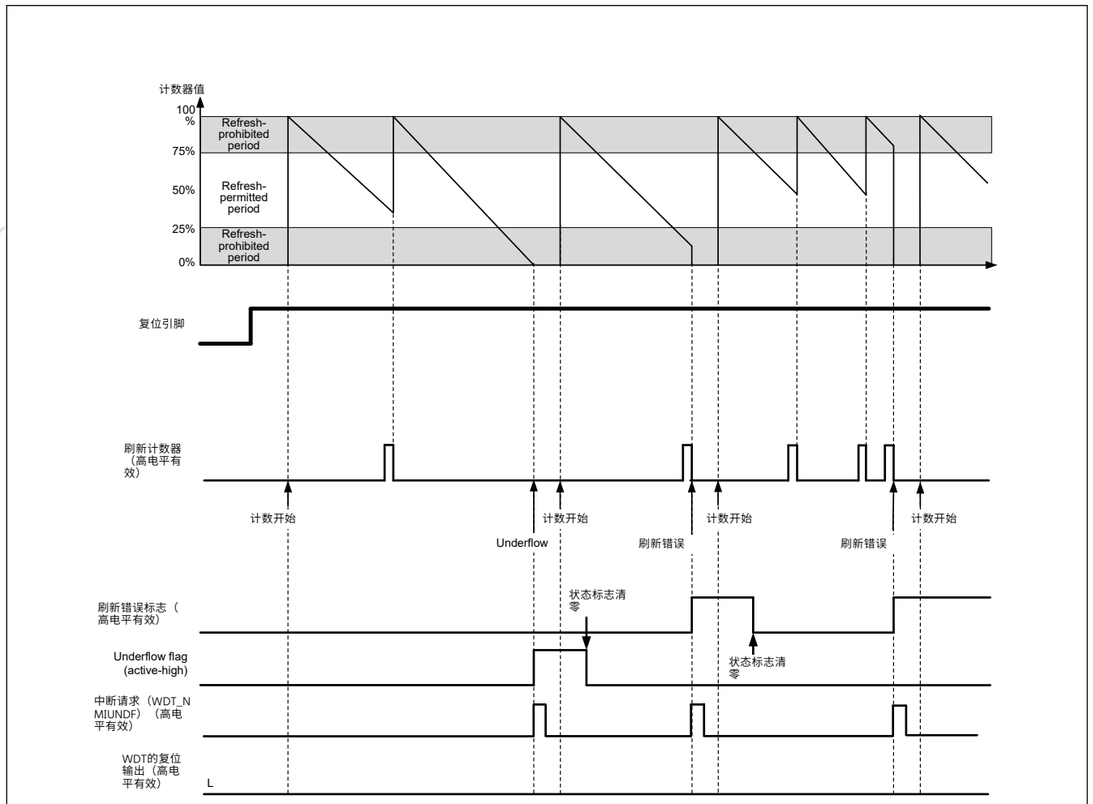
如果程序失控或由于刷新允许刷新周期之外的刷新而发生刷新错误，则WDT输出复位信号或不可屏蔽中断请求中断请求(WDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期。超时时间的值在递减计数器中设置并重新开始计数。

通过设置WDT复位中断请求选择位(OFS0.WDTRSTIRQS)可以选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断 允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图24.4显示了以下条件下的操作示例（不可屏蔽中断）：

- ●自动启动模式（OFS0.WDTSTRT=0）
- ●使能不可屏蔽中断请求输出（OFS0.WDTRSTIRQS=0）
- ●窗口起始位置为75%(OFS0.WDTRPSS[1:0]=10b)
- ●窗口结束位置为25%(OFS0.WDTRPES[1:0]=10b)



Note: 复位引脚=RES

Figure 24.4 自动启动模式下的操作示例

24.3.2 控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入

写入WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)或WDT计数停止控制在从复位状态释放到第一次刷新操作之间，寄存器(WDTCSTPR)是可能的。

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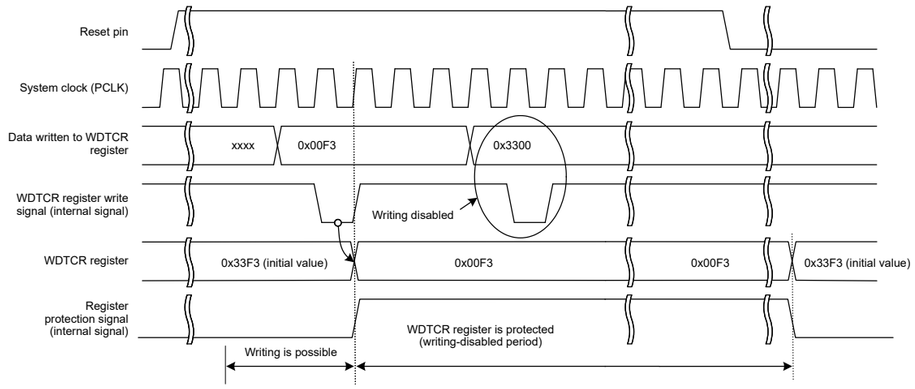
After a refresh (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR register, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR register against subsequent write attempts. This protection is released by the reset source of the WDT. With other reset sources, the protection is not released.

Figure 24.5 shows control waveforms produced in response to writing to the WDTCR.



Note: PCLK = PCLKB
Reset pin = RES

Figure 24.5 Control waveforms produced in response to writes to the WDTCR register

24.3.3 Refresh Operation

The down-counter is refreshed and starts counting operation on a write of the values 0x00 and 0xFF to the WDT Refresh Register (WDTRR). If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 0x00 and 0xFF to the WDTRR register.

Correct refreshing is also performed when a register other than WDTRR is accessed or WDTRR is read between writing 0x00 and writing 0xFF to WDTRR. Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by the 0xFF write. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from WDTRR → 0xFF

[Example write sequences that are invalid for refreshing the counter]

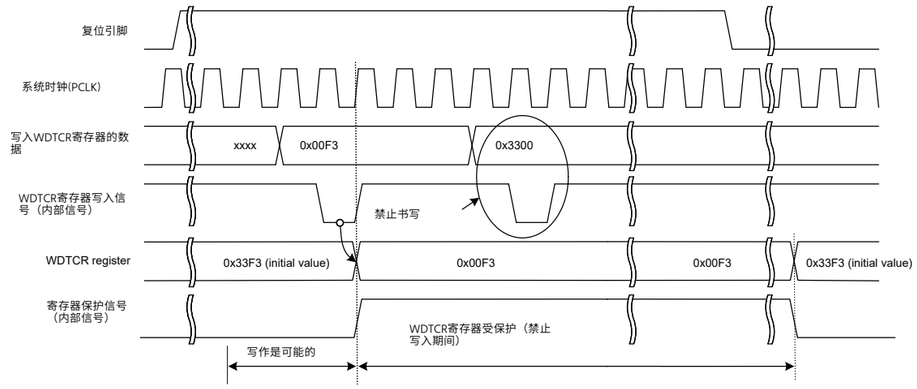
- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)
- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF

After 0xFF is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing 0xFF to WDTRR 4 count cycles before the down-counter underflows.

Figure 24.6 shows the WDT refresh-operation waveforms when the clock division ratio is PCLKB/64.

在刷新（计数开始）或写入WDTCR、WDTRCR或WDTCSTPR寄存器后，WDT变为1以保护WDTCR、WDTRCR和WDTCSTPR寄存器免受后续写入尝试。该保护由WDT的复位源解除。使用其他复位源时，不会解除保护。

图24.5显示了响应写入WDTCR产生的控制波形。



Note: PCLK=PCLKB复位引脚=RES

Figure 24.5 响应写入WDTCR寄存器而产生的控制波形

24.3.3 刷新操作

向下计数器刷新并在将值0x00和0xFF写入WDT刷新时开始计数操作寄存器(WDTRR)。如果在0x00之后写入0xFF以外的值，则不刷新递减计数器。如果写入无效值，则在向WDTRR寄存器写入0x00和0xFF时会恢复正确刷新。

在写入0x00和写入0xFF到WDTRR之间访问WDTRR以外的寄存器或读取WDTRR时，也会执行正确刷新。刷新计数器的写入必须在允许刷新的周期内进行，这由0xFF写入决定。因此，即使在可刷新期间外写入0x00，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

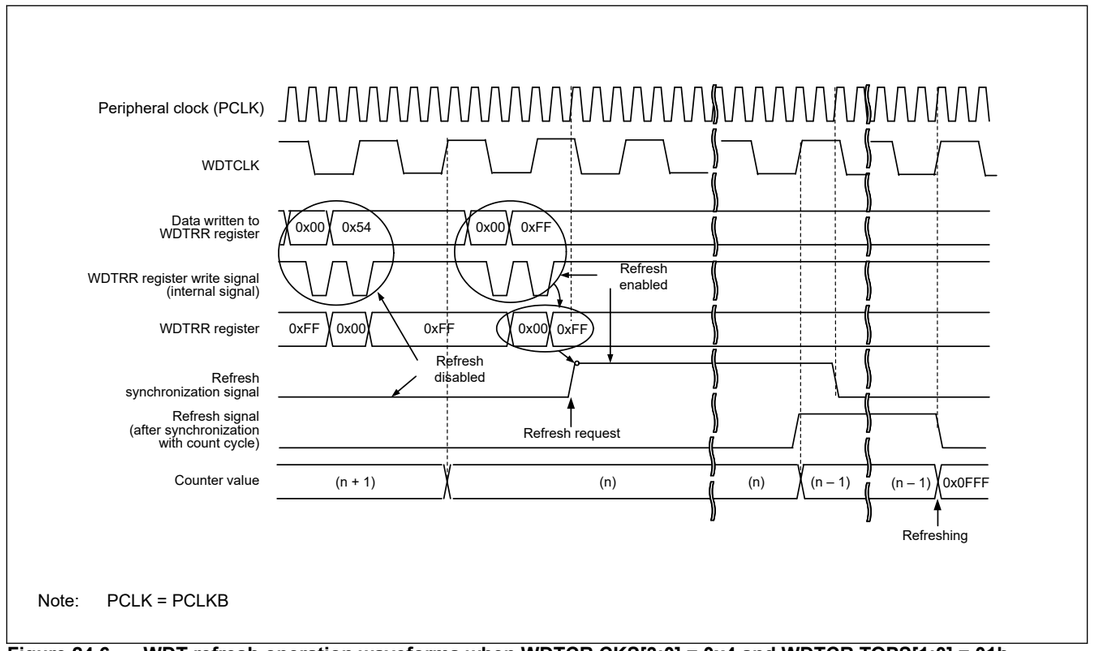
- 0x00 → 0xFF
- 0x00 ((n–1)th time) → 0x00 (nth time) → 0xFF
- ●0x00→访问另一个寄存器或从WDTRR读取→0xFF

[对刷新计数器无效的示例写入序列]

- ●0x23（0x00以外的值）→0xFF
- ●0x00→0x54（0xFF以外的值）
- ●0x00→0xAA（0x00和0xFF以外的值）→0xFF

将0xFF写入WDT刷新寄存器(WDTRR)后，刷新递减计数器最多需要4个信号周期进行计数。为满足此要求，请在递减计数器下溢之前的4个计数周期内将0xFF写入WDTRR。

图24.6显示了时钟分频比为PCLKB64时的WDT刷新操作波形。



Note: PCLK = PCLKB

Figure 24.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

Note: When setting the refresh time, consider the oscillation accuracy of the clock sources of the PCLKB and WDTCLK. Set values which ensure that refreshing is possible even when the frequency varies in the range of error of the oscillation accuracy.

24.3.4 Status Flags

The refresh error (WDTSR.REFEF) and underflow (WDTSR.UNDFF) flags retain the source of the interrupt request from the WDT. After a release from the interrupt request generation, read the WDTSR.REFEF and WDTSR.UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit. Writing 1 has no effect. Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the next interrupt request from the WDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 24.2.3. WDTSR : WDT Status Register.

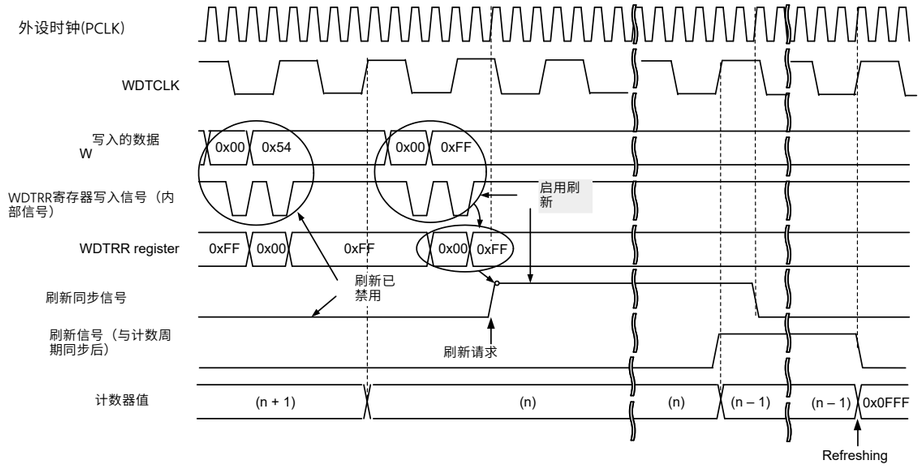
24.3.5 Reset Output

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up again and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

24.3.6 Interrupt Sources

When the Reset Interrupt Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt (WDT_NMIUNDF) signal is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 13, Interrupt Controller Unit (ICU).



Note: PCLK = PCLKB

Figure 24.6 WDTCR.CKS[3:0]=0x4和WDTCR.TOPS[1:0]=01b时的WDT刷新操作波形

Note: 设置刷新时间时，要考虑PCLKB和WDTCLK时钟源的振荡精度。设定即使频率在振荡精度的误差范围内变化也能进行刷新的值。

24.3.4 状态标志

刷新错误(WDTSR.REFEF)和下溢(WDTSR.UNDFF)标志保留来自WDT的中断请求源。释放中断请求生成后，读取WDTSR.REFEF和WDTSR.UNDFF标志以检查中断源。对于每个标志，写入0会清除该位。写1无效。保持状态标志不变不会影响操作。如果在WDT发出下一个中断请求时未清除标志，则清除较早的中断源并写入新的中断源。关于从各标志写入0到反映其值的时间段，请参阅第24.2.3节。WDTSR：WDT状态寄存器。

24.3.5 复位输出

当复位中断选择位(WDTRCR.RSTIRQS)在寄存器启动模式下设置为1时，或当WDT复位时在自动启动模式下，选项功能选择寄存器0(OFS0)中的中断请求选择位(OFS0.WDTRSTIRQS)设置为1，当递减计数器中的下溢或刷新错误发生时，在1个周期计数内输出复位信号.

在寄存器启动模式下，递减计数器被初始化（所有位设置为0）并在输出复位信号后停止在该状态。复位状态解除并重新启动程序后，再次设置计数器，并通过刷新再次开始倒计时。在自动启动模式下，复位状态解除后自动开始倒计时。

24.3.6 中断源

当在寄存器启动模式下复位中断选择位(WDTRCR.RSTIRQS)设置为0或WDT复位时在自动启动模式下，选项功能选择寄存器0(OFS0)中的中断请求选择位(OFS0.WDTRSTIRQS)设置为0，当计数器下溢或发生刷新错误时，将产生中断(WDT_NMIUNDF)信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

Table 24.4 WDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DMAC or DTC
WDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

24.3.7 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value. The read value of the down-counter might differ from the actual count by one.

Figure 24.7 shows the processing for reading the WDT down-counter value when the clock division ratio is PCLKB/64.

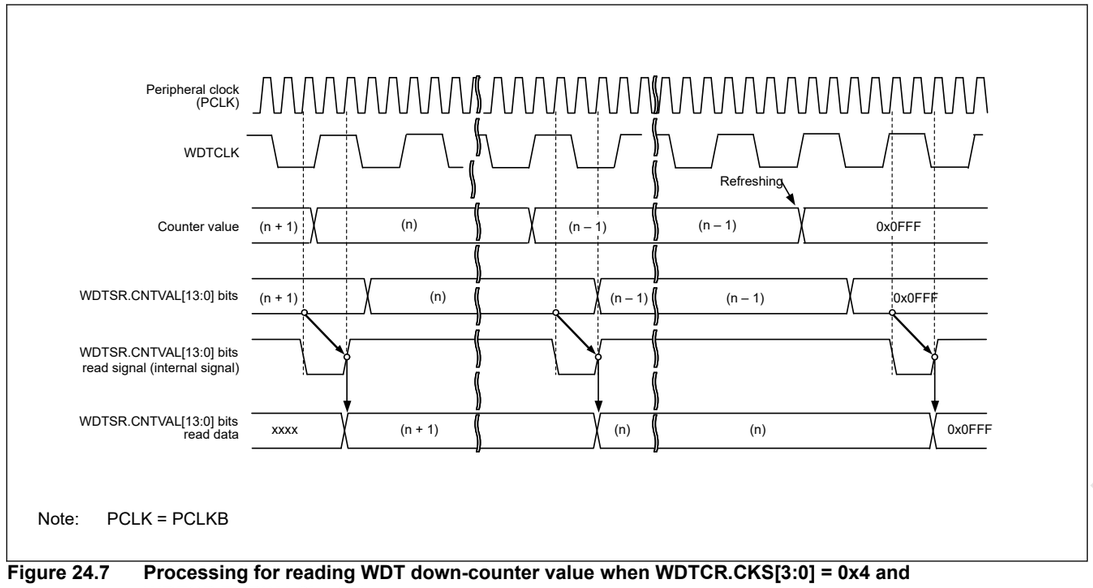


Figure 24.7 Processing for reading WDT down-counter value when WDTCR.CKS[3:0] = 0x4 and WDTCR.TOPS[1:0] = 01b

24.3.8 Association between Option Function Select Register 0 (OFS0) and WDT Registers

Table 24.5 lists the association between the Option Function Select Register 0 (OFS0) used in auto start mode, and the registers used in register start mode. For details on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

Table 24.5 Association between Option Function Select Register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period selection	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio selection	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position selection	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position selection	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output selection	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep or Snooze mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

Table 24.4 WDT中断源

Name	中断源	对CPU的中断	启动DMAC或DTC
WDT_NMIUNDF	• Down-counter underflow • 刷新错误	Possible	不可能

24.3.7 读取递减计数器值

WDT将计数器值存储在WDT状态寄存器的递减计数器值位(WDTSR.CNTVAL[13:0])中。检查这些位以获得计数器值。递减计数器的读取值可能与实际计数相差1。

图24.7显示了在时钟分频比为PCLKB64时读取WDT递减计数器值的处理。

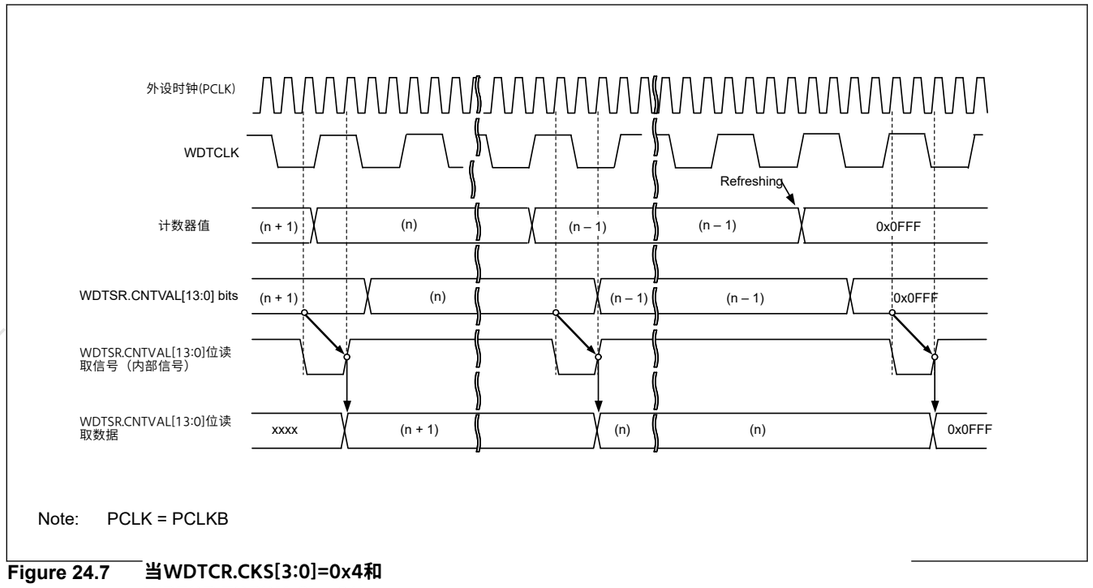


Figure 24.7 当WDTCR.CKS[3:0]=0x4和WDTCR.TOPS[1:0] = 01b

24.3.8 选项功能选择寄存器0(OFS0)和WDT之间的关联 Registers

表24.5列出了用于自动启动模式的选项功能选择寄存器0(OFS0)和用于寄存器启动模式的寄存器之间的关联。有关选项功能选择寄存器0(OFS0)的详细信息，请参见第6.2.1节。OFS0：选项功能选择寄存器0。

Table 24.5 选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联

控制目标	Function	OFS0寄存器（在自动启动模式下启用）OFS0.WDTSTRT=0	WDT寄存器（在寄存器启动模式下启用）OFS0.WDTSTRT=1
Down-counter	超时时间选择	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	时钟分频比选择	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	窗口起始位置选择	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	窗口结束位置选择	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
复位输出或中断请求输出	复位输出或中断请求输出选择	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
计数停止	睡眠或贪睡模式计数停止控制	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

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24.4 Output to the Event Link Controller (ELC)

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow and refresh error. An event signal is output regardless of the setting of the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) in register start mode or auto start mode. An event signal can also be output when the next interrupt source is generated while the Refresh Error flag (WDTSR.REFEF) or Underflow flag (WDTSR.UNDFF) is 1. For details, see section 18, Event Link Controller (ELC).

24.5 Usage Notes

24.5.1 ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x53 to ICU Event Link Setting Register n (ICU.IELSRn) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x53).

24.4 输出到事件链接控制器(ELC)

当ELC将中断请求信号用作事件信号时，WDT能够对先前指定的模块进行链接操作。事件信号由计数器下溢和刷新错误输出。在寄存器启动模式或自动启动模式下，无论复位中断请求选择位(WDTRCR.RSTIRQS)的设置如何，都会输出事件信号。当刷新错误标志(WDTSR.REFEF)或下溢标志(WDTSR.UNDFF)为1时，也可以在产生下一个中断源时输出事件信号。有关详细信息，请参阅第18节，事件链接控制器(ELC)。

24.5 使用说明

24.5.1 ICU事件链接设置寄存器n(IELSRn)设置

当启用WDT复位断言(OFS0.WDTRSTIRQS=0或WDTRCR.RSTIRQS=0)或启用事件链接操作(ELSRn.ELS[8:0])时，禁止将0x53设置为ICU事件链接设置寄存器n(ICU.IELSRn)=0x53)。

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25. Independent Watchdog Timer (IWDT)

25.1 Overview

The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The IWDT functions differ from those of the WDT in the following respects:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support register start mode

Table 25.1 lists the IWDT specifications and Figure 25.1 shows a block diagram.

Table 25.1 IWDT specifications

Parameter	Description
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Counting automatically starts after a reset • Only secure developer can start the IWDT
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically).
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading the counter value	The down-counter value can be read by the IWDTSR register
Event link function	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the Independent Watchdog Timer (OFS0.IWDTTOPS[1:0] bits) • Window start position in the Independent Watchdog Timer (OFS0.IWDTRPSS[1:0] bits) • Window end position in the Independent Watchdog Timer (OFS0.IWDTRPES[1:0] bits) • Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit).
TrustZone Filter	Security attribution can be set

Note 1. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

25. 独立看门狗定时器(IWDT)

25.1 Overview

独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT提供复位MCU或生成不可屏蔽中断或下溢中断的功能。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。

IWDT的功能与WDT的功能有以下不同：

●分频IWDT专用时钟（IWDTCLK）用作计数源（不受PCLKB影响）

●IWDT不支持寄存器启动方式

表25.1列出了IWDT规范，图25.1显示了框图。

Table 25.1 IWDT specifications

Parameter	Description
计数来源*1	IWDT-dedicated clock (IWDTCLK)
时钟分频比	除以1、16、32、64、128或256
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	• 复位后自动开始计数 • 只有安全的开发人员才能启动IWDT
停止计数器的条件	• 复位（递减计数器和其他寄存器恢复初始值） • 计数器下溢或产生刷新错误（计数自动重新开始）。
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
重置输出源	• Down-counter underflows • 在允许刷新的期限之外刷新（刷新错误）。
Non-maskable interrupt/interrupt sources	• Down-counter underflows • 在允许刷新的期限之外刷新（刷新错误）。
读取计数器值	递减计数器的值可以通过IWDTSR寄存器读取
事件链接功能	• 递减计数器下溢事件输出 • 刷新错误事件输出。
输出信号（内部信号）	• 复位输出 • 中断请求输出 • 休眠模式计数停止控制输出。
自动启动模式	可配置为以下触发器：● 复位后的时钟分频比（OFS0.IWDTCKS[3:0]位） • 独立看门狗定时器的超时周期（OFS0.IWDTTOPS[1:0]位） • 独立看门狗定时器中的窗口起始位置（OFS0.IWDTRPSS[1:0]位） • 独立看门狗定时器中的窗口结束位置（OFS0.IWDTRPES[1:0]位） • 复位输出或中断请求输出（OFS0.IWDTRSTIRQS位） • 转换到休眠模式、软件待机模式或贪睡模式时的减计数停止功能（OFS0.IWDTSTPCL位）。
TrustZone Filter	可设置安全属性

注1.满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。

总线接口和寄存器使用PCLKB运行，14位计数器和控制电路使用IWDTCLK运行。

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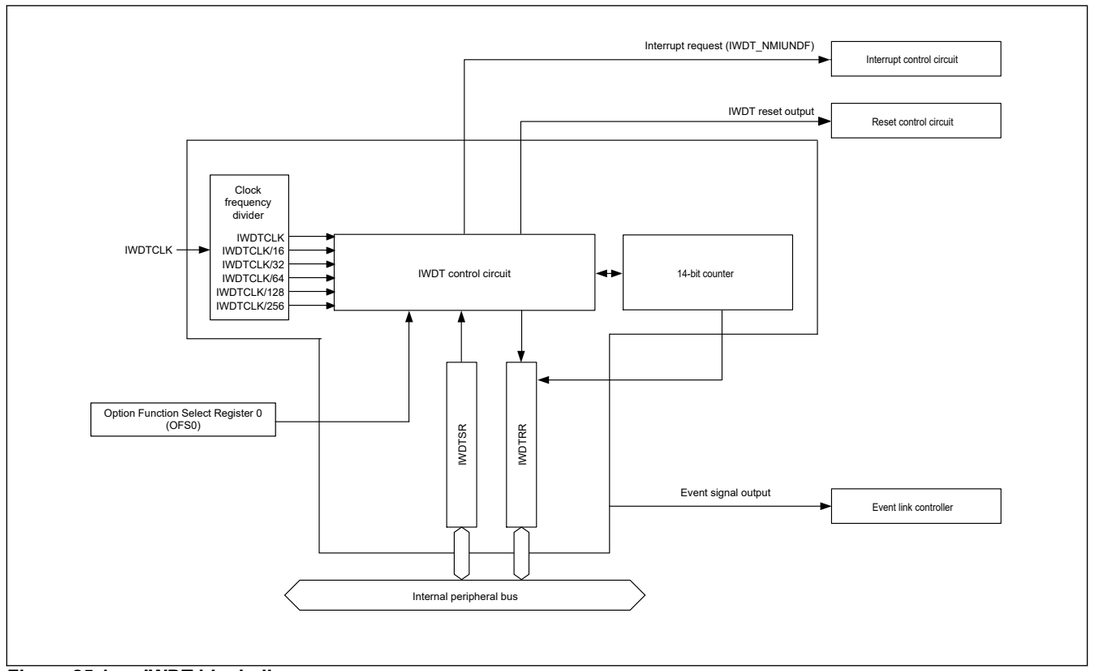


Figure 25.1 IWDT block diagram

25.2 Register Descriptions

25.2.1 IWDTRR : IWDT Refresh Register

Base address: IWDT = 0x4008_3200

Offset address: 0x00

Bit position:	7							0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	The down-counter is refreshed by writing 0x00 and then writing 0xFF to this register	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 0x00 and then writing 0xFF to IWDTRR (refresh operation) within the refresh-permitted period. After the down-counter is refreshed, it starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]) in the Option Function Select Register 0 (OFS0).

When 0x00 is written, the read value is 0x00. When a value other than 0x00 is written, the read value is 0xFF. For details of the refresh operation, see section 25.3.2. Refresh Operation.

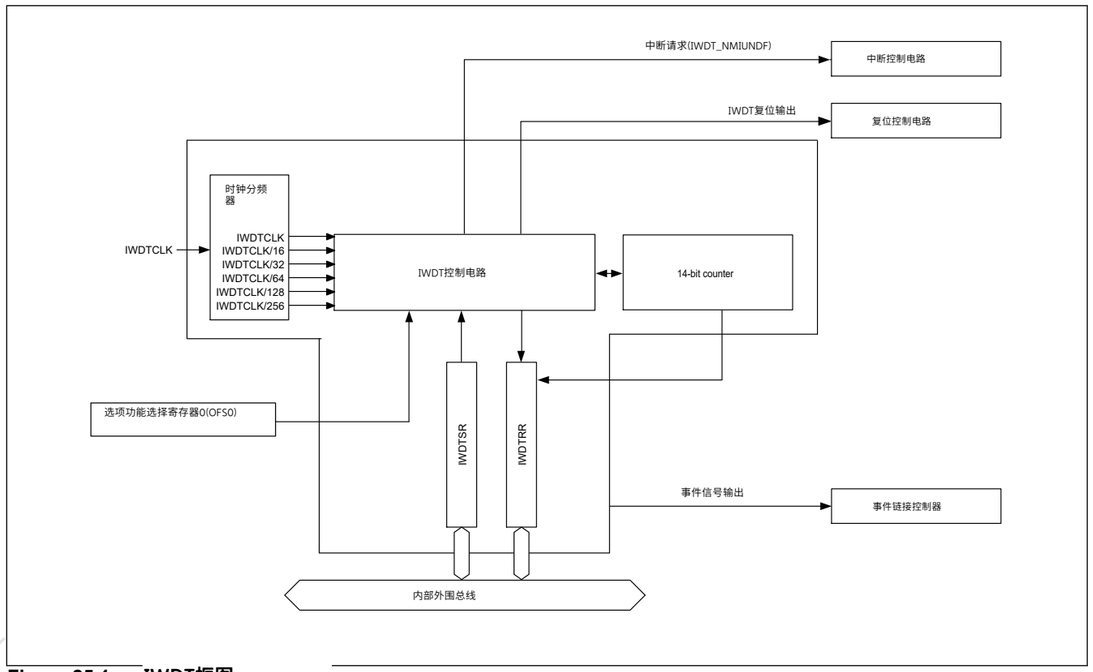


Figure 25.1 IWDT框图

25.2 注册说明

25.2.1 IWDTRR:IWDT刷新寄存器

Base address: IWDT = 0x4008_3200

Offset address: 0x00

Bit position:	7							0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	通过写入0x00然后将0xFF写入该寄存器来刷新递减计数器	R/W

IWDTRR寄存器刷新IWDT的递减计数器。IWDT的递减计数器通过在允许刷新的周期内写入0x00然后将0xFF写入IWDTRR（刷新操作）来刷新。递减计数器刷新后，它从选项功能选择寄存器0(OFS0)的IWDT超时周期选择位(OFS0.IWDTTOPS[1:0])中选择的值开始递减计数。

写入0x00时，读取值为0x00。写入0x00以外的值时，读取的值为0xFF。有关刷新操作的详细信息，请参阅第25.3.2节。刷新操作。

25.2.2 IWDTSR : IWDT Status Register

Base address: IWDT = 0x4008_3200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value Value counted by the down-counter	R
14	UNDFF	Underflow Flag 0: No underflow occurred 1: Underflow occurred	R/W*1
15	REFEF	Refresh Error Flag 0: No refresh error occurred 1: Refresh error occurred	R/W*1

Note 1. Only 0 can be written to clear the flag.

The IWDTSR register indicates the counter value of the down-counter and whether an underflow or refresh error occurred in the down-counter.

CNTVAL[13:0] bits (Down-counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. The value 1 indicates that the down-counter underflowed. Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred. This indicates that a refresh operation was performed during a prohibited period. The value 1 indicates that a refresh error occurred. Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N + 2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of this flag is ignored for (N + 2) IWDTCLK cycles following a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128

25.2.2 IWDTSR:IWDT状态寄存器

Base address: IWDT = 0x4008_3200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	REFEF	UNDFF	CNTVAL[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
13:0	CNTVAL[13:0]	Down-counter Value 递减计数器计数的值	R
14	UNDFF	Underflow Flag 0：未发生下溢1：发生下溢	R/W*1
15	REFEF	刷新错误标志 0：未发生刷新错误1：发生刷新错误	R/W*1

注1.只能写入0来清除标志。

IWDTSR寄存器指示递减计数器的计数值以及递减计数器是否发生下溢或刷新错误。

CNTVAL[13:0] bits (Down-counter Value)

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认递减计数器中是否发生下溢。值1表示递减计数器下溢。将0写入UNDFF标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在下溢后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128
- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

REFEF标志（刷新错误标志）

读取REFEF标志以确认是否发生刷新错误。这表示在禁止期间执行了刷新操作。值1表示发生了刷新错误。将0写入REFEF标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在刷新错误后的(N+2)个IWDTCLK周期内，该标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When OFS0.IWDTCKS[3:0] = 0x0, N = 1
- When OFS0.IWDTCKS[3:0] = 0x2, N = 16
- When OFS0.IWDTCKS[3:0] = 0x3, N = 32
- When OFS0.IWDTCKS[3:0] = 0x4, N = 64
- When OFS0.IWDTCKS[3:0] = 0xF, N = 128

- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

25.2.3 OFS0 : Option Function Select Register 0

For information on the Option Function Select Register 0 (OFS0), see section 6.2.1. OFS0 : Option Function Select Register 0.

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, that is, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified in the IWDTCKS[3:0] bits as 1 cycle.

After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 25.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 25.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, the IWDT can be configured to a count period between 128 and 524,288 IWDTCLK cycles.

- When OFS0.IWDTCKS[3:0] = 0x5, N = 256.

25.2.3 OFS0：选项功能选择寄存器0

有关选项功能选择寄存器0(OFS0)的信息，请参见第6.2.1节。OFS0：选项功能选择寄存器0。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位选择超时周期，即从128、512、1024或2048个周期到递减计数器下溢的周期，采用IWDTCKS[3:0]位中指定的分频时钟作为1个周期。

向下计数器刷新后，IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定了在计数器下溢之前的IWDTCLK周期数。

表25.2列出了IWDTCKS[3:0]和IWDTTOPS[1:0]位设置、超时周期和IWDTCLK周期数之间的关系。

Table 25.2 超时时间设置

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		时钟分频比	超时时间（周期数）	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1024	1024
				1	1		2048	2048
0	0	1	0	0	0	IWDTCLK/16	128	2048
				0	1		512	8192
				1	0		1024	16384
				1	1		2048	32768
0	0	1	1	0	0	IWDTCLK/32	128	4096
				0	1		512	16384
				1	0		1024	32768
				1	1		2048	65536
0	1	0	0	0	0	IWDTCLK/64	128	8192
				0	1		512	32768
				1	0		1024	65536
				1	1		2048	131072
1	1	1	1	0	0	IWDTCLK/128	128	16384
				0	1		512	65536
				1	0		1024	131072
				1	1		2048	262144
0	1	0	1	0	0	IWDTCLK/256	128	32768
				0	1		512	131072
				1	0		1024	262144
				1	1		2048	524288

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于递减计数器的时钟分频比。分频比可以从IWDT专用时钟(IWDTCLK)除以1、16、32、64、128和256中选择。结合IWDTTOPS[1:0]位设置，可以将IWDT配置为计数128到524 288个IWDTCLK周期之间的周期。

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

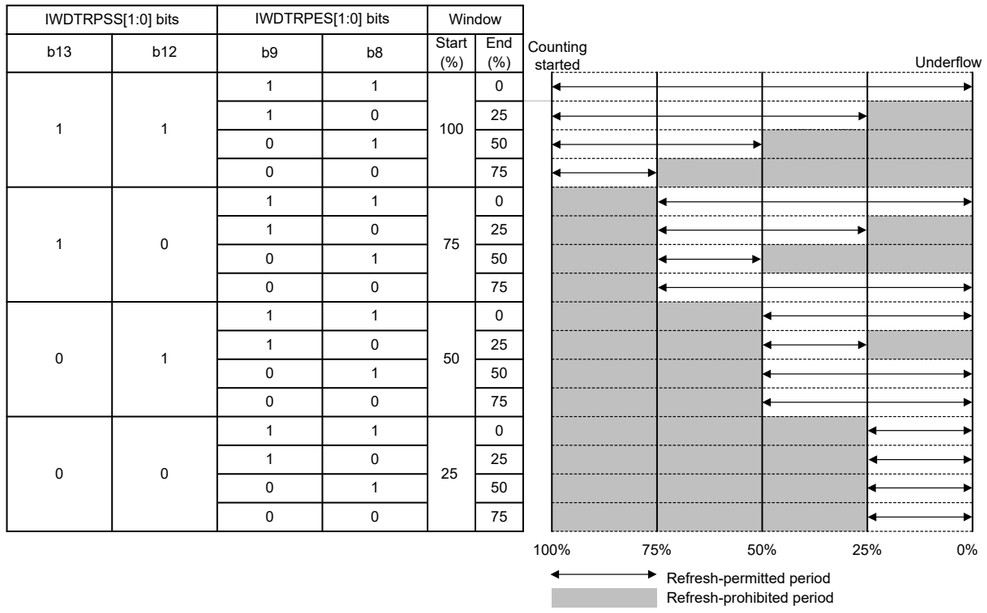
IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the window end position. If the window start position is less than or equal to the window end position, the window end position is set to 0%.

Table 25.3 lists the counter values for the window start and end positions, and Figure 25.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 25.3 Relationship between the timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 25.2 IWDTRPSS[1:0] and IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurs. Setting 1 selects reset output. Setting 0 selects non-maskable interrupt or interrupt.

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口开始位置的值（窗口开始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

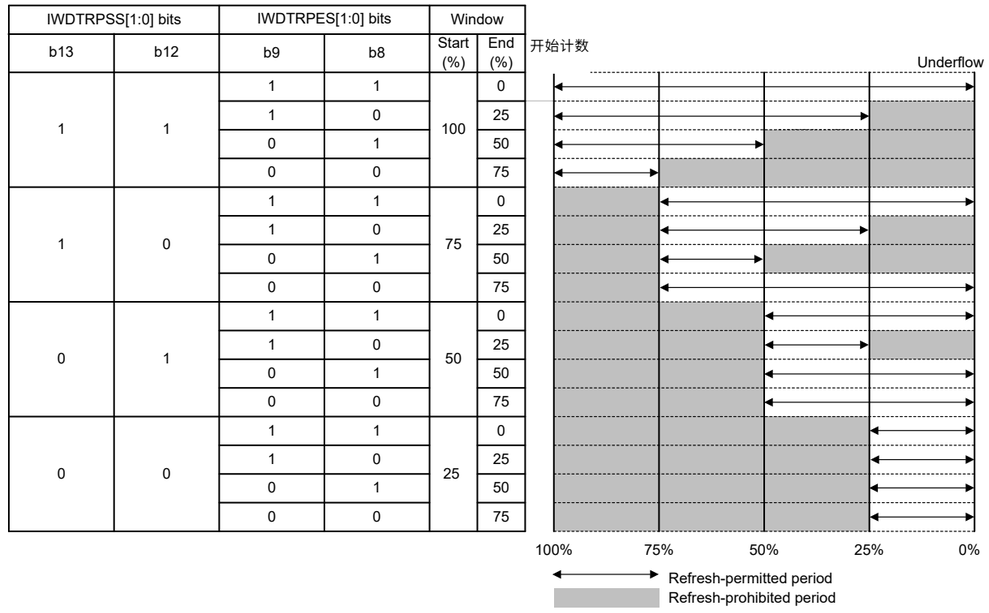
IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定指示刷新允许周期的窗口起始位置。可以为窗口起始位置选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置小于或等于窗口结束位置，则窗口结束位置设置为0%。

表25.3列出了窗口开始和结束位置的计数器值，图25.2显示了在IWDTRPSS[1:0]、IWDTRPES[1:0]和IWDTTOPS[1:0]位中设置的允许刷新周期。

Table 25.3 超时时间与窗口开始和结束计数器值之间的关系

IWDTTOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
b1	b0	Cycles	计数器值	100%	75%	50%	25%
0	0	128	0x007F	0x007F	0x005F	0x003F	0x001F
0	1	512	0x01FF	0x01FF	0x017F	0x00FF	0x007F
1	0	1024	0x03FF	0x03FF	0x02FF	0x01FF	0x00FF
1	1	2048	0x07FF	0x07FF	0x05FF	0x03FF	0x01FF



Note: 如果窗口结束设置≥窗口开始设置，则窗口结束设置设置为0%。

Figure 25.2 IWDTRPSS[1:0]和IWDTRPES[1:0]位设置和允许刷新周期

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位指定发生下溢或刷新错误时的行为。设置1选择复位输出。
设置0选择不可屏蔽中断或中断。

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit selects whether to stop counting on transition to Sleep, Snooze, or Software Standby mode.

25.3 Operation

25.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) in the Option Function Select Register 0 is 0, auto start mode is selected, otherwise the IWDT is disabled.

Within the reset state, the setting values for the following in the Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio (OFS0.IWDTCKS[3:0])
- Window start and end positions (OFS0.IWDTRPSS[1:0], OFS0.IWDTRPES[1:0])
- Timeout period (OFS0.IWDTTOPS[1:0])
- Reset output or interrupt request (OFS0.IWDTRSTIRQS)

When the reset state is released, the counter automatically starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashed or because a refresh error occurred when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, the value of the timeout period is set in the down-counter and counting starts. The reset output or interrupt request output can be selected with the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected with the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 25.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.IWDTRSTIRQS = 0)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位选择在转换到休眠、贪睡或软件待机模式时是否停止计数。

25.3 Operation

25.3.1 自动启动模式

当IWDT启动模式选择位置（OFS0.IWDTSTRT）中的选项函数选择寄存器0为0时，选择了自动启动模式，否则IWDT将被禁用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下设置值在
IWDT registers:

- ●时钟分频比（OFS0.IWDTCKS[3:0]）
- ●窗口开始和结束位置（OFS0.IWDTRPSS[1:0]、OFS0.IWDTRPES[1:0]）
- ●超时周期（OFS0.IWDTOPS[1:0]）
- ●复位输出或中断请求（OFS0.IWDTRSTIRQS）

解除复位状态后，计数器自动从IWDT中选择的值开始倒计时
超时周期选择位(OFS0.IWDTOPS[1:0])。

之后，只要程序继续正常运行，并且在允许刷新的时间内刷新计数器，每次刷新计数器并继续递减计数时，计数器中的值都会被复位。只要此过程继续，IWDT就不会输出复位信号。但是，如果由于程序崩溃或在刷新允许周期之外尝试刷新时发生刷新错误而导致计数器下溢，则IWDT将置位复位信号或不可屏蔽中断请求中断请求(IWDT_NMIUNDF)。

在产生复位信号或不可屏蔽中断请求中断请求后，计数器在计数1个周期后重新加载超时周期，超时周期的值设置在递减计数器中并开始计数。可以通过IWDT复位中断请求选择位(OFS0.IWDTRSTIRQS)选择复位输出或中断请求输出。可以使用IWDT下溢刷新错误中断 允许位(NMIER.IWDTEN)选择不可屏蔽的中断请求或中断请求。

图25.3显示了以下条件下的操作示例：

- ●自动启动模式（OFS0.IWDTSTRT=0）
- ●使能不可屏蔽中断请求输出（OFS0.IWDTRSTIRQS=0）
- ●窗口起始位置为75%(OFS0.IWDTRPSS[1:0]=10b)
- ●窗口结束位置为25%(OFS0.IWDTRPES[1:0]=10b)。

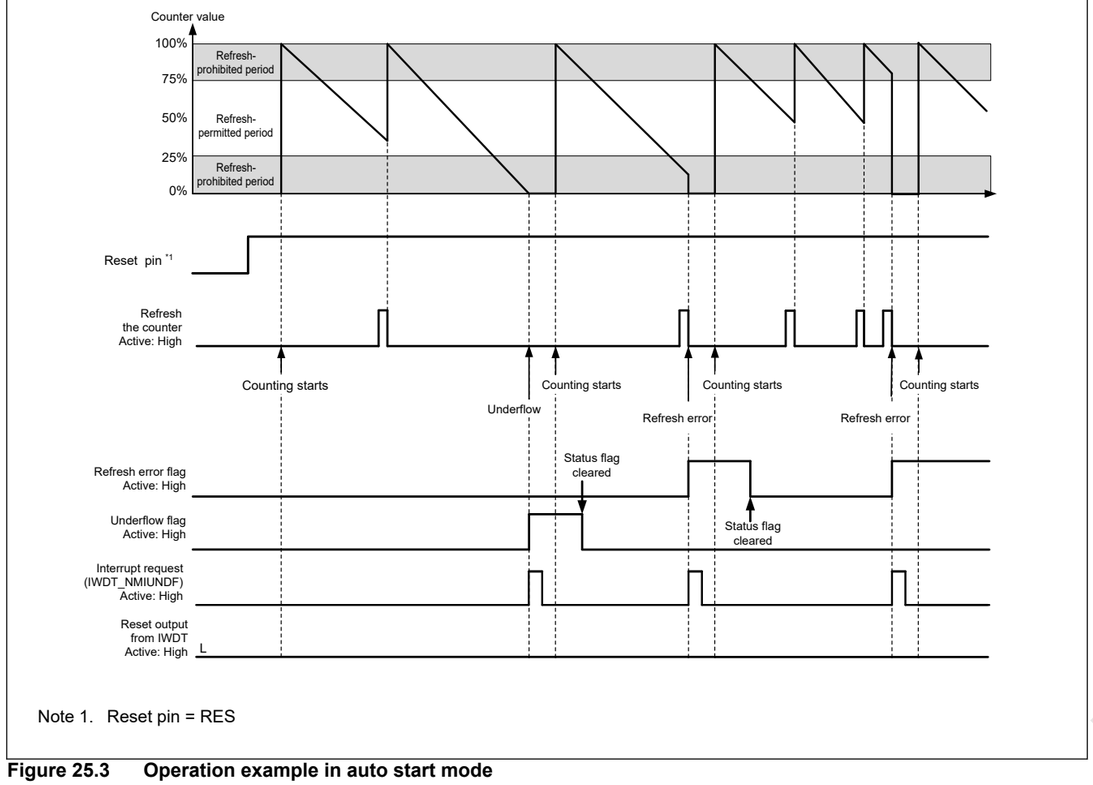


Figure 25.3 Operation example in auto start mode

25.3.2 Refresh Operation

The down-counter is refreshed and operation starts (counting is started by refreshing) by writing the values 0x00 and 0xFF to the IWDT Refresh Register (IWDTRR). If a value other than 0xFF is written after 0x00, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 0x00 and 0xFF to the IWDTRR.

When writes are made in the order of 0x00 (first time) → 0x00 (second time), and if 0xFF is written after that, the writing order 0x00 → 0xFF is satisfied. Writing 0x00 ((n - 1)th time) →0x00 (nth time) → 0xFF is valid, and the refresh is performed correctly. Even when the first value written before 0x00 is not 0x00, correct refreshing is performed as long as the operation contains the write sequence of 0x00 → 0xFF.

Correct refreshing is also performed regardless of whether a register other than IWDTRR is accessed or IWDTRR is read between writing 0x00 and writing 0xFF to IWDTRR. Writes to refresh the counter must be made within the refresh-permitted period. Whether writing is done within the refresh-permitted period is determined when 0xFF is written. For this reason, correct refreshing is performed even when 0x00 is written outside the refresh-permitted period.

[Example write sequences that are valid to refresh the counter]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- 0x00 → access to another register or read from IWDTRR → 0xFF.

[Example write sequences that are not valid to refresh the counter]

- 0x23 (a value other than 0x00) → 0xFF
- 0x00 → 0x54 (a value other than 0xFF)

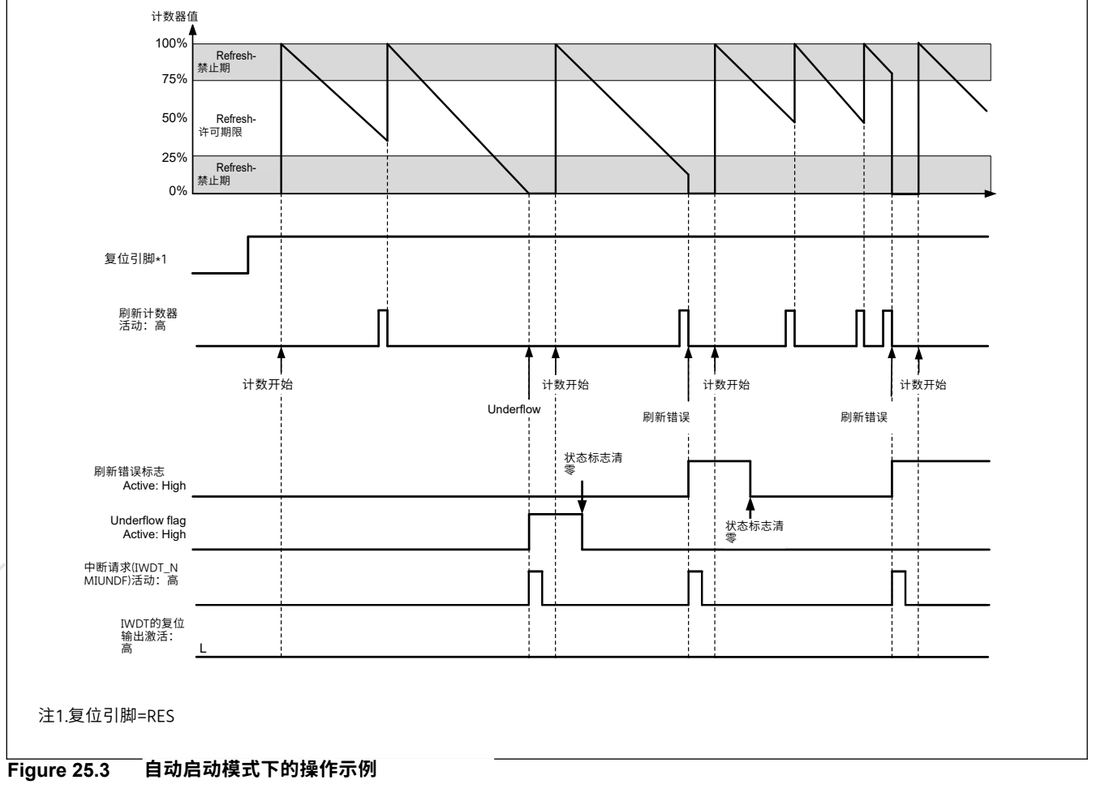


Figure 25.3 自动启动模式下的操作示例

25.3.2 刷新操作

通过将值0x00和0xFF写入IWDT刷新寄存器(IWDTRR)来刷新递减计数器并开始操作（通过刷新开始计数）。如果在0x00之后写入0xFF以外的值，则不刷新递减计数器。如果写入无效值，则在向IWDTRR写入0x00和0xFF时会恢复正确刷新。

当以0x00（第一次）→0x00（第二次）的顺序进行写入时，如果在此之后写入0xFF，则满足写入顺序0x00→0xFF。写入0x00((n1)次)→0x00(n次)→0xFF有效，刷新正确。即使在0x00之前写入的第一个值不是0x00时，只要操作包含0x00→0xFF的写入序列，就会执行正确的刷新。

无论在写入0x00和写入0xFF到IWDTRR之间是否访问IWDTRR以外的寄存器或读取IWDTRR，也会执行正确刷新。刷新计数器的写入必须在允许刷新的期限内进行。在写入0xFF时确定是否在可刷新周期内完成写入。因此，即使在可刷新期间外写入0x00，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

- 0x00 → 0xFF
- 0x00 ((n - 1)th time) → 0x00 (nth time) → 0xFF
- ●0x00→访问另一个寄存器或从IWDTRR读取→0xFF。

[对刷新计数器无效的示例写入序列]

- ●0x23（0x00以外的值）→0xFF
- ●0x00→0x54（0xFF以外的值）

- 0x00 → 0xAA (0x00 and a value other than 0xFF) → 0xFF.

After 0xFF is written to the IWDTRR register, refreshing the counter requires up to 4 cycles of the signal for counting (the IWDT-Dedicated Clock Frequency Division Ratio Select bits (OFS0.IWDTCKS[3:0]) to determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 cycle for counting. To meet this requirement, writing 0xFF to the IWDTRR must be completed 4 count cycles before the end of the refresh-permitted period or a down-counter underflow. The value of the counter can be checked with the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 0x1FFF, even if 0x00 is written to IWDTRR before 0x1FFF is reached at (0x2002, for example), refreshing occurs if 0xFF is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 0x1FFF
- When the window end position is set to 0x1FFF, refreshing occurs if 0x2003 (4 count cycles before 0x1FFF) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR
- When the refresh-permitted period continues until count 0x0000, refreshing can be performed immediately before an underflow. In this case, if 0x0003 (4 count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 0x00 → 0xFF to IWDTRR, no underflow occurs and refreshing is performed.

Figure 25.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

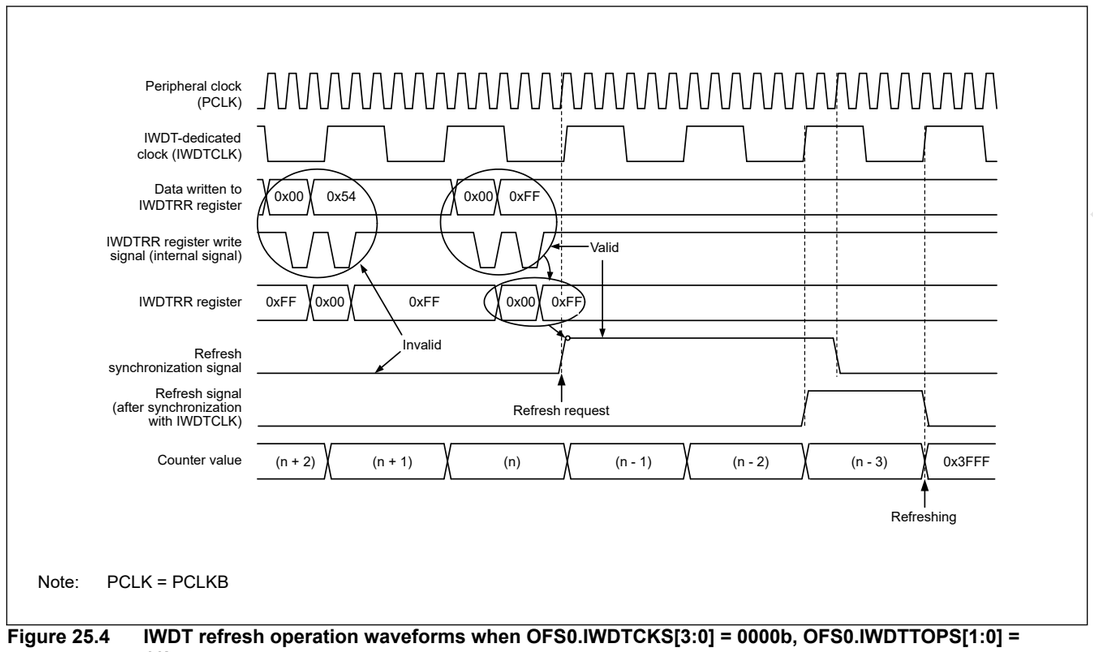


Figure 25.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

25.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the interrupt request from the IWDT. Therefore, after a release from the interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared at the time of the next interrupt request from the IWDT, the earlier interrupt source is cleared and the new interrupt source is written. For the time period between when 0 is written in each flag and when its value is reflected, see section 25.2.2. IWDTSR : IWDT Status Register.

●0x00→0xAA（0x00和0xFF以外的值）→0xFF。

将0xFF写入IWDTRR寄存器后，刷新计数器需要最多4个周期的信号计数（IWDT专用时钟分频比选择位（OFS0.IWDTCKS[3:0]）来确定IWDT专用时钟(IWDTCLK)占1个周期用于计数。为满足此要求，必须在刷新允许周期结束或递减计数器下溢之前4个计数周期完成向IWDTRR写入0xFF。可以使用计数器位(IWDTSR.CNTVAL[13:0])检查计数器。

[Example refreshing timings]

●当窗口起始位置设置为0x1FFF时，即使在到达0x1FFF之前将0x00写入IWDTRR（例如0x2002），如果在IWDTSR.CNTVAL[13:0]位的值达到0x1FFF后将0xFF写入IWDTRR，则会发生刷新

●当窗口结束位置设置为0x1FFF时，如果在将0x00→0xFF写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0x2003（0x1FFF之前的4个计数周期）或更大的值，则会发生刷新

●当刷新允许周期持续到计数0x0000时，可以在下溢之前立即执行刷新。在这种情况下，如果在将0x00→0xFF写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0x0003（下溢前的4个计数周期）或更大的值，则不会发生下溢并执行刷新。

图25.4显示了当PCLKB>IWDTCLK且时钟分频比为时的IWDT刷新操作波形
IWDTCLK.

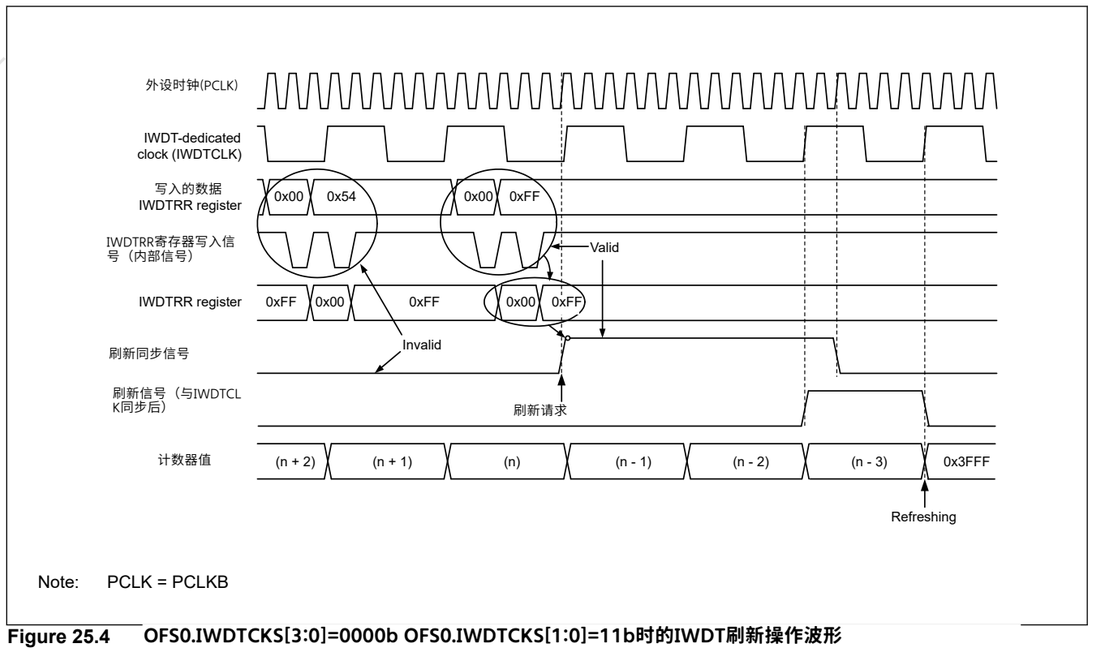


Figure 25.4 OFS0.IWDTCKS[3:0]=0000b OFS0.IWDTCKS[1:0]=11b时的IWDT刷新操作波形

25.3.3 状态标志

刷新错误(IWDTSR.REFEF)和下溢(IWDTSR.UNDFF)标志保留来自IWDT的中断请求源。因此，在中断请求生成释放后，读取IWDTSR.REFEF和UNDFF标志以检查中断源。对于每个标志，写入0清除该位，写入1无效。

保持状态标志不变不会影响操作。如果在IWDT发出下一个中断请求时未清除标志，则清除较早的中断源并写入新的中断源。关于从各标志写入0到反映其值的时间段，请参阅第25.2.2节。IWDTSR：IWDT状态寄存器。

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25.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the counter or a refresh error occurs. Counting down automatically starts after the reset output.

25.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 0, an interrupt (IWDT_NMIUNDF) signal occurs when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 13, Interrupt Controller Unit (ICU).

Table 25.4 IWDT interrupt source

Name	Interrupt source	Interrupt to CPU	Start DMAC or DTC
IWDT_NMIUNDF	• Down-counter underflow • Refresh error	Possible	Not possible

25.3.6 Reading the Down-Counter Value

As the counter is a IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT Status Register. Check these bits to obtain the counter value indirectly.

Reading the counter value requires multiple PCLKB clock cycles (up to 4 clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 25.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

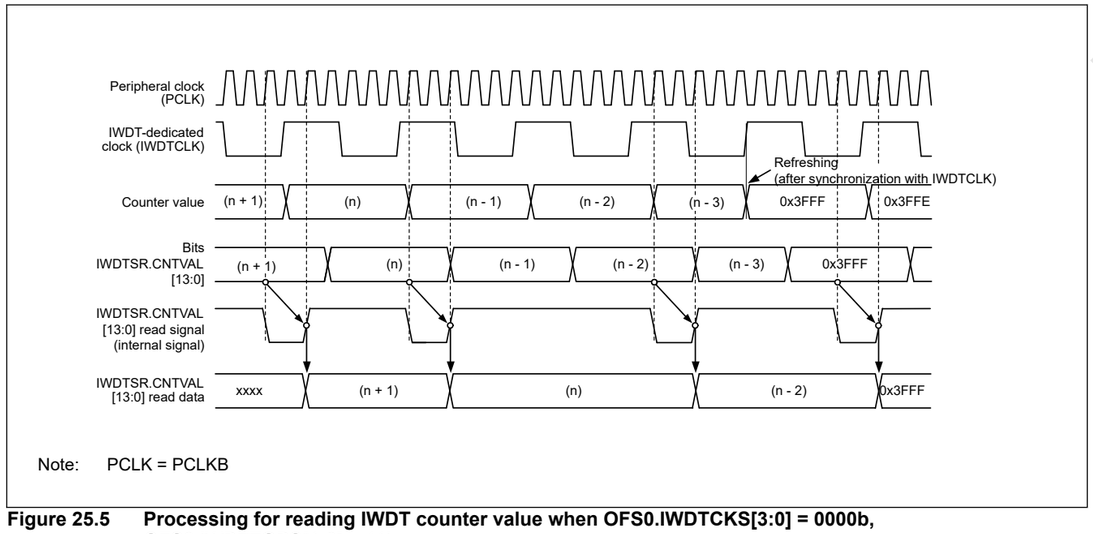

Figure 25.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b, OFS0.IWDTTOPS[1:0] = 11b

25.4 Output to the Event Link Controller (ELC)

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the event link controller (ELC). The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting of the OFS0.IWDTRSTIRQS bit. An event signal can also be output at generation of the next interrupt source while the Refresh Error flag (IWDTSR.REFEF) or Underflow flag (IWDTSR.UNDFF) is 1. For details, see section 18, Event Link Controller (ELC).

25.3.4 复位输出

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）的位置为1时，当计数器中的下流或刷新错误发生时，将输出重置信号。复位输出后自动开始倒计时。

25.3.5 中断源

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项函数选择寄存器0（OFS0）设置为0时，当计数器中的下流或刷新错误发生时，会发生中断（IWDT_NMIUNDF）信号。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

Table 25.4 IWDT中断源

Name	中断源	对CPU的中断	启动DMAC或DTC
IWDT_NMIUNDF	• Down-counter underflow • 刷新错误	Possible	不可能

25.3.6 读取递减计数器值

由于计数器是IWDT专用时钟(IWDTCLK)，因此无法直接读取计数器值。IWDT将计数器值与外设时钟(PCLKB)同步，并将其存储在IWDT状态寄存器的递减计数器值位(IWDTSR.CNTVAL[13:0])中。检查这些位以间接获得计数器值。

读取计数器值需要多个PCLKB时钟周期（最多4个时钟周期），读取的计数器值可能与实际计数器值相差一个计数值。

图25.5显示了当PCLKB>IWDTCLK且时钟分频比为IWDTCLK时读取IWDT计数器值的处理。

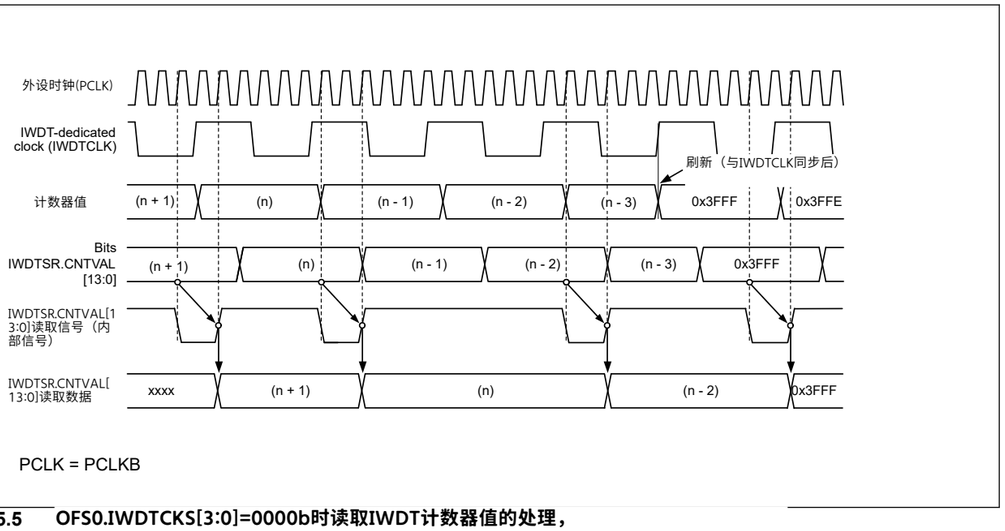

Figure 25.5 OFS0.IWDTCKS[3:0]=0000b时读取IWDT计数器值的处理，OFS0.IWDTTOPS[1:0] = 11b

25.4 输出到事件链接控制器(ELC)

当中断请求信号被事件链接控制器(ELC)用作事件信号时，IWDT能够对指定模块进行链接操作。事件信号由计数器下溢或刷新错误输出。

无论OFS0.IWDTRSTIRQS位的设置如何，都会输出事件信号。当刷新错误标志(IWDTSR.REFEF)或下溢标志(IWDTSR.UNDFF)为1时，也可以在生成下一个中断源时输出事件信号。有关详细信息，请参阅第18节，事件链接控制器(ELC)。

25.5 Usage Notes

25.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

25.5.2 Clock Division Ratio Setting

Satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

25.5.3 Constraints on the ICU Event Link Setting Register n (IELSRn) Setting

Setting 0x52 to ICU Event Link Setting Register n (IELSRn.IELS[8:0]) is prohibited when enabling the IWDT reset assertion (OFS0.IWDTRSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x52).

25.5 使用说明

25.5.1 刷新操作

在配置刷新时间时，请考虑给定PCLKB和IWDTCLK精度的误差范围的变化。
设置确保可以刷新的值。

25.5.2 时钟分频比设置

满足外设模块时钟（PCLKB）的频率≥4×（分频后的计数时钟源的频率）。

25.5.3 ICU事件链接设置寄存器n(IELSRn)设置的约束

当启用IWDT复位断言(OFS0.IWDTRSTIRQS=0)或启用事件链接操作(ELSRn.ELS[8:0]=0x52）。

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26. Ethernet MAC Controller (ETHERC)

26.1 Overview

The MCU provides a one-channel Ethernet Controller (ETHERC) compliant with the Ethernet or IEEE802.3 Media Access Control (MAC) layer protocol. Each ETHERC channel has one channel of the MAC layer interface. Connecting the MCU to the physical layer LSI (PHY-LSI) allows transmission and reception of frames compliant with the Ethernet/IEEE802.3 standard. The ETHERC is connected to the Ethernet DMA Controller (EDMAC), so data can be transferred without using the CPU.

Table 26.1 lists the ETHERC specifications, Figure 26.1 shows the configuration, and Table 26.2 lists the I/O pins.

Figure 26.2 and Figure 26.3 show examples connections of the MCU to an external PHY-LSI.

Table 26.1 ETHERC specifications

Parameter	Specifications
Number of channels	One channel
Protocol	Flow control compliant with IEEE802.3x
Data transmission/reception	Frames compliant with the Ethernet/IEEE802.3 standard can be transmitted and received
Bit rate	Supports 10 Mbps and 100 Mbps
Operation modes	Supports full-duplex and half-duplex modes
Interfaces	Media Independent Interface (MII), Reduced Media Independent Interface (RMII), compliant with the IEEE802.3u standard
Functions	• Magic Packet™ detection • Wake-on-LAN (WOL) signal output

26. 以太网MAC控制器(ETHERC)

26.1 Overview

MCU提供符合以太网或IEEE802.3媒体访问的单通道以太网控制器(ETHERC)
控制(MAC)层协议。每个ETHERC通道都有一个MAC层接口通道。将MCU连接到物理层LSI(PHY-LSI)允许发送和接收符合以太网IEEE802.3标准的帧。ETHERC连接到以太网DMA控制器(EDMAC)，因此可以在不使用CPU的情况下传输数据。

表26.1列出了ETHERC规范，图26.1显示了配置，表26.2列出了IO引脚。

图26.2和图26.3显示了MCU与外部PHY-LSI的连接示例。

Table 26.1 ETHERC specifications

Parameter	Specifications
通道数	一个频道
Protocol	符合IEEE802.3x的流量控制
Data transmission/reception	可以发送和接收符合以太网IEEE802.3标准的帧
比特率	支持10Mbps和100Mbps
操作模式	支持全双工和半双工模式
Interfaces	媒体独立接口(MII)、精简媒体独立接口(RMII)，符合IEEE802.3u standard
Functions	• MagicPacket 检测 • 网络唤醒(WOL)信号输出

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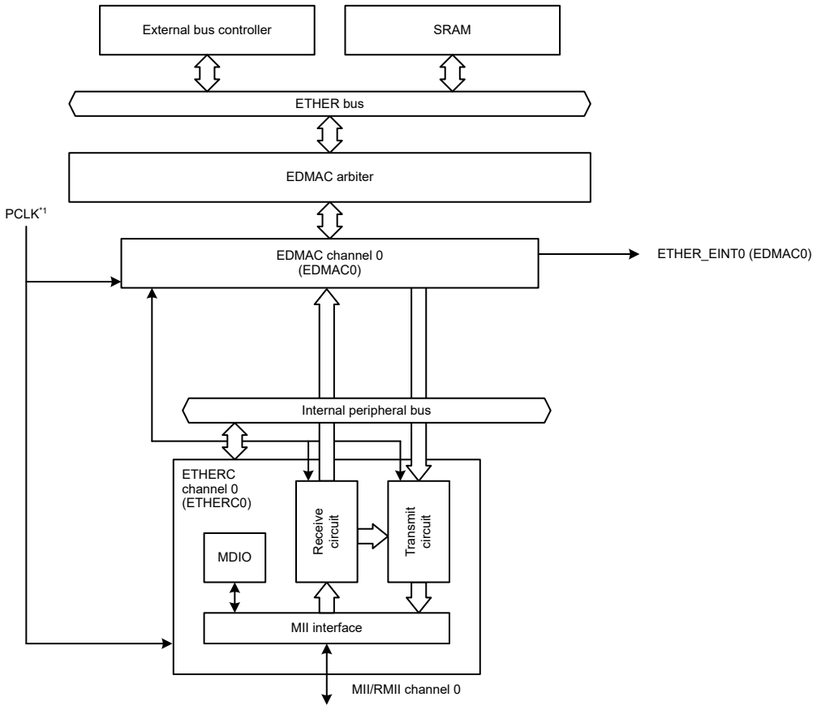
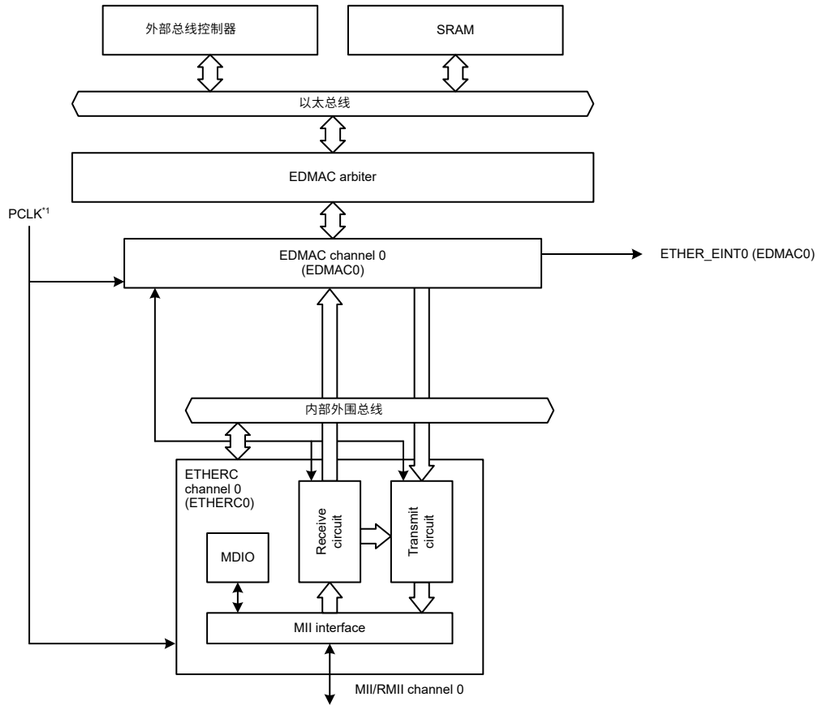


Note 1. PCLK: PCLKA
When using the ETHERC, 12.5 MHz ≤ PCLK ≤ 100 MHz.

Figure 26.1 ETHERC configuration



Note 1. PCLK: PCLKA
使用ETHERC时，12.5MHz≤PCLK≤100MHz。

Figure 26.1 ETHERC configuration

Table 26.2 ETHERC I/O pins (1 of 2)

Operating mode	Pin name	I/O	Description
MII	ET0_TX_CLK *1	Input	Transmit clock Timing reference signal for outputting the ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER signals.
	ET0_RX_CLK *1	Input	Receive clock Timing reference signal for inputting the ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER signals.
	ET0_TX_EN *1	Output	Transmit data valid This signal indicates that valid transmit data was output on pins ET0_ETXD3 to ET0_ETXD0.
	ET0_ETXD3 to ET0_ETXD0 *1	Output	4-bit transmit data
	ET0_TX_ER *1	Output	Transmit error This signal notifies the PHY-LSI that an error occurred during transmission.
	ET0_RX_DV *1	Input	Receive data valid This signal indicates that valid receive data is on pins ET0_ERXD3 to ET0_ERXD0.
	ET0_ERXD3 to ET0_ERXD0 *1	Input	4-bit receive data
	ET0_RX_ER *1	Input	Receive error This signal indicates that there is an error in a frame that is being transferred from the PHY-LSI to the ETHERC.
	ET0_CRS *1	Input	Carrier sense
	ET0_COL *1	Input	Collision detection signal
	ET0_MDC *1	Output	Management data clock Reference clock signal for transfer of information on the ET0_MDIO pin.
	ET0_MDIO *1	I/O	Management data Input/Output Bidirectional data signal for exchanging management data with the PHY-LSI.
	ET0_LINKSTA	Input	Link status input from the PHY-LSI
	ET0_EXOUT	Output	General output pin
	ET0_WOL	Output	Wake-on-LAN. This signal indicates that a Magic Packet was received

Table 26.2 ETHERCIO引脚（2个中的1个）

操作模式	引脚名称	I/O	Description
MII	ET0_TX_CLK *1	Input	发送时钟 用于输出ET0_TX_EN、ET0_ETXD3到ET0_ETXD0和ET0_TX_ER信号的时序参考信号。
	ET0_RX_CLK *1	Input	接收时钟 将ET0_RX_DV、ET0_ERXD3输入到 ET0_ERXD0和ET0_RX_ER信号。
	ET0_TX_EN *1	Output	传输数据有效 该信号表明有效的发送数据在引脚上输出 ET0_ETXD3 to ET0_ETXD0.
	ET0_ETXD3 to ET0_ETXD0 *1	Output	4位传输数据
	ET0_TX_ER *1	Output	传输错误该信号通知PHY-LSI在传输过程中发生错误。
	ET0_RX_DV *1	Input	接收数据有效 该信号表明有效的接收数据在引脚ET0_ERXD3到 ET0_ERXD0.
	ET0_ERXD3 to ET0_ERXD0 *1	Input	4位接收数据
	ET0_RX_ER *1	Input	接收错误 该信号表示从PHY-LSI传输到ETHERC的帧中存在错误。
	ET0_CRS *1	Input	载体感
	ET0_COL *1	Input	碰撞检测信号
	ET0_MDC *1	Output	管理数据时钟 用于在ET0_MDIO引脚上传输信息的参考时钟信号。
	ET0_MDIO *1	I/O	管理数据输入输出 双向数据信号，用于与管理数据交换 PHY-LSI.
	ET0_LINKSTA	Input	来自PHY-LSI的链路状态输入
	ET0_EXOUT	Output	通用输出引脚
	ET0_WOL	Output	局域网唤醒。该信号表示收到了一个魔术包

Table 26.2 ETHERC I/O pins (2 of 2)

Operating mode	Pin name	I/O	Description
RMII	REF50CK0 *2	Input	Reference clock Timing reference signal for the RMII0_TXD_EN, RMII0_TXD1 to RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1 to RMII0_RXD0, and RMII0_RX_ER pins.
	RMII0_TXD_EN *2	Output	Transmit data valid This signal indicates that valid transmit data was output on the RMII0_TXD1 and RMII0_TXD0 pins.
	RMII0_TXD1 to RMII0_TXD0 *2	Output	2-bit transmit data
	RMII0_CRS_DV *2	Input	Carrier sense/receive data valid This signal indicates that valid receive data is on the RMII0_RXD1 and RMII0_RXD0 pins.
	RMII0_RXD1 to RMII0_RXD0 *2	Input	2-bit receive data
	RMII0_RX_ER *2	Input	Receive error This signal indicates that there is an error in a frame that is being transferred from the PHY-LSI to the ETHERC. See the note in section 26.5.2. Input to RMII0_RX_ER Pin While RMII Is Selected.
	ET0_MDC *2	Output	Management data clock Reference clock signal for transfer of information on the ET0_MDIO pin
	ET0_MDIO *2	I/O	Management data Input/Output Bidirectional data signal for exchanging management data with the PHY-LSI.
	ET0_LINKSTA	Input	Link status input from the PHY-LSI.
	ET0_EXOUT	Output	General output pin
	ET0_WOL	Output	Wake-on-LAN. This signal indicates that a Magic Packet was received.

Note 1. MII signal compliant with IEEE802.3u.
Note 2. RMII signal compliant with IEEE802.3u.

Table 26.2 ETHERCIO引脚（2个中的2个）

操作模式	引脚名称	I/O	Description
RMII	REF50CK0 *2	Input	参考时钟 RMII0_TXD_EN、RMII0_TXD1的时序参考信号 RMII0_TXD0、RMII0_CRS_DV、RMII0_RXD1至RMII0_RXD0，以及 RMII0_RX_ER pins.
	RMII0_TXD_EN *2	Output	传输数据有效 该信号表示有效的传输数据已输出到 RMII0_TXD1和RMII0_TXD0引脚。
	RMII0_TXD1 to RMII0_TXD0 *2	Output	2位传输数据
	RMII0_CRS_DV *2	Input	载波侦听接收数据有效 该信号表示有效的接收数据在RMII0_RXD1和RMII0_RXD0引脚上。
	RMII0_RXD1 to RMII0_RXD0 *2	Input	2位接收数据
	RMII0_RX_ER *2	Input	接收错误 该信号表示从PHY-LSI传输到ETHERC的帧中存在错误。请参阅第26.5.2节中的注释。选择RMII时输入到RMII0_RX_ER引脚。
	ET0_MDC *2	Output	管理数据时钟 用于在ET0_MDIO引脚上传输信息的参考时钟信号
	ET0_MDIO *2	I/O	管理数据输入输出 双向数据信号，用于与管理数据交换 PHY-LSI.
	ET0_LINKSTA	Input	来自PHY-LSI的链路状态输入。
	ET0_EXOUT	Output	通用输出引脚
	ET0_WOL	Output	局域网唤醒。该信号表示收到了一个魔术包。

注1.符合IEEE802.3u的MII信号。
注2.RMII信号符合IEEE802.3u。

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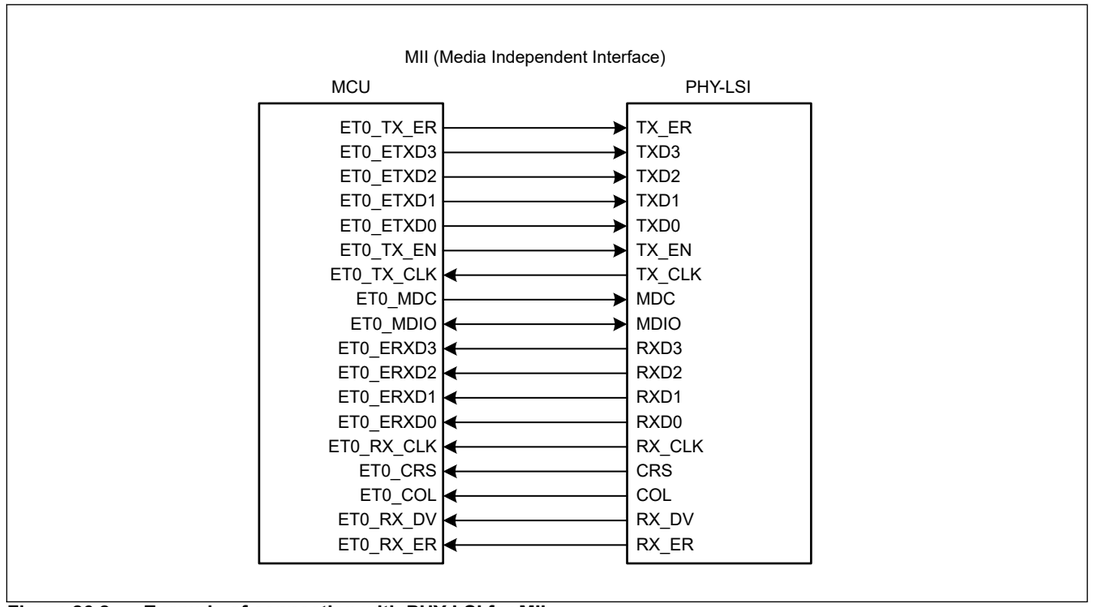


Figure 26.2 Example of connection with PHY-LSI for MII

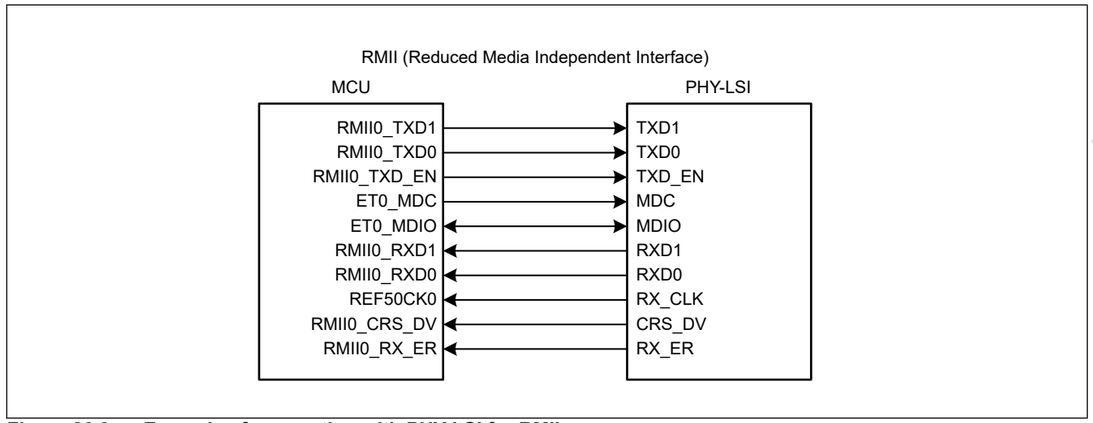


Figure 26.3 Example of connection with PHY-LSI for RMII

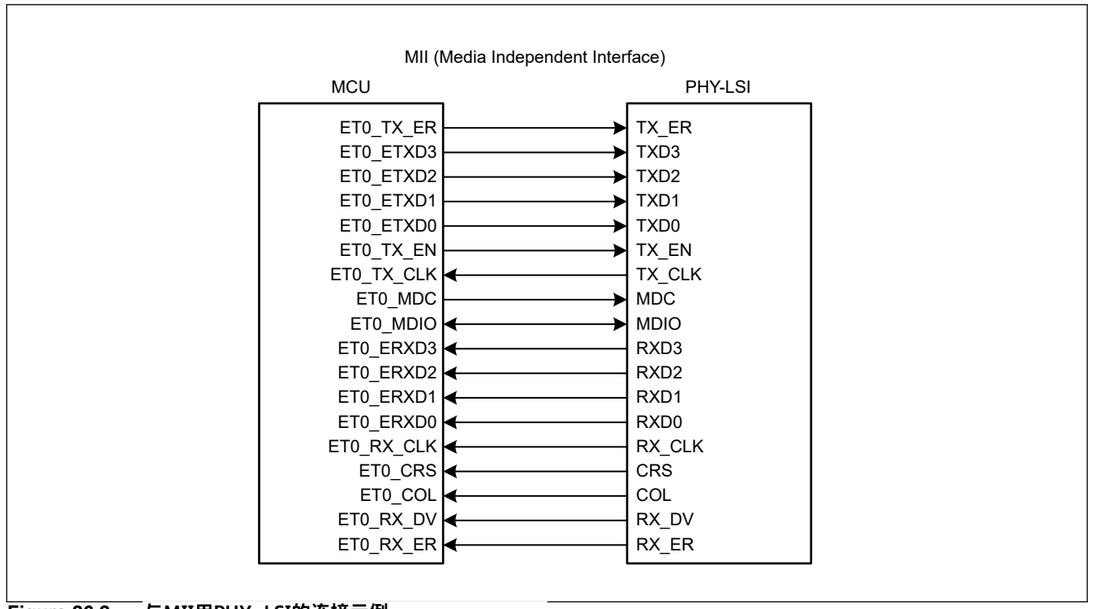


Figure 26.2 与MII用PHY-LSI的连接示例

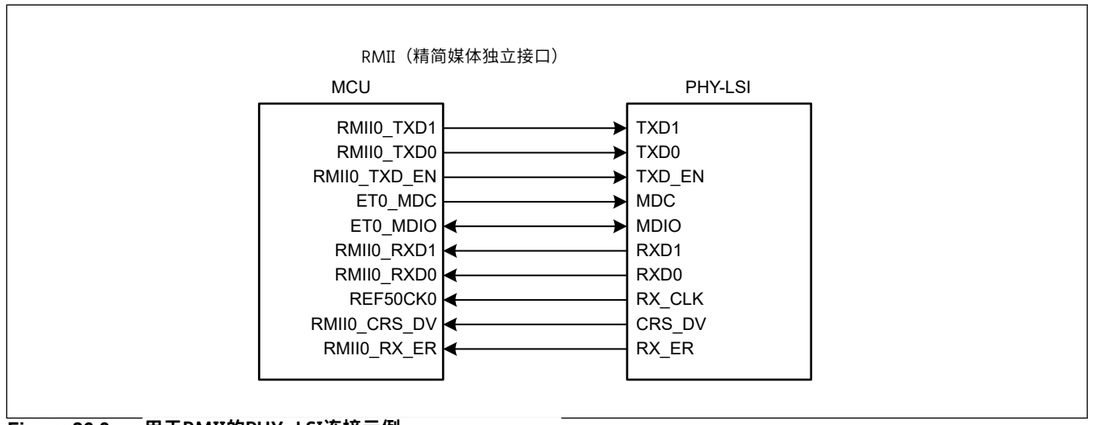


Figure 26.3 用于RMII的PHY-LSI连接示例

26.2 Register Descriptions

26.2.1 ECMR : ETHERC Mode Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	TPC	ZPF	PFR	RXF	TXF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PRCEF	—	—	MPDE	—	—	RE	TE	—	ILB	RTM	DM	PRM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRM	Promiscuous Mode 0: Disable promiscuous mode 1: Enable promiscuous mode.	R/W
1	DM	Duplex Mode 0: Half-duplex mode 1: Full-duplex mode.	R/W
2	RTM	Bit Rate 0: 10 Mbps 1: 100 Mbps.	R/W
3	ILB	Internal Loopback Mode 0: Perform normal data transmission or reception 1: Loop data back in the ETHERC when full-duplex mode is selected.	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W
5	TE	Transmission Enable 0: Disable transmit function 1: Enable transmit function.	R/W
6	RE	Reception Enable 0: Disable receive function 1: Enable receive function.	R/W
8:7	—	These bits are read as 0. The write value should be 0.	R/W
9	MPDE	Magic Packet Detection Enable 0: Disable Magic Packet detection 1: Enable Magic Packet detection.	R/W
11:10	—	These bits are read as 0. The write value should be 0.	R/W
12	PRCEF	CRC Error Frame Receive Mode 0: Notify EDMAC of a CRC error 1: Do not notify EDMAC of a CRC error.	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
16	TXF	Transmit Flow Control Operating Mode 0: Disable automatic PAUSE frame transmission (PAUSE frame is not automatically transmitted) 1: Enable automatic PAUSE frame transmission (PAUSE frame is automatically transmitted as required).	R/W
17	RXF	Receive Flow Control Operating Mode 0: Disable PAUSE frame detection 1: Enable PAUSE frame detection.	R/W

26.2 注册说明

26.2.1 ECMR:ETHERC模式寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	TPC	ZPF	PFR	RXF	TXF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PRCEF	—	—	MPDE	—	—	RE	TE	—	ILB	RTM	DM	PRM
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PRM	混杂模式 0：禁用混杂模式1：启用混杂模式。	R/W
1	DM	双工模式 0: Half-duplex mode 1: Full-duplex mode.	R/W
2	RTM	比特率 0: 10 Mbps 1: 100 Mbps.	R/W
3	ILB	内部环回模式 0：执行正常的数据发送或接收1：选择全双工模式时，在ETHERC中环回数据。	R/W
4	—	该位读取为0。写入值应为0。	R/W
5	TE	传输使能 0：关闭发送功能1：开启发送功能。	R/W
6	RE	接收启用 0：关闭接收功能1：开启接收功能。	R/W
8:7	—	这些位被读取为0。写入值应为0。	R/W
9	MPDE	魔术包检测启用 0：禁用魔包检测1：启用魔包检测。	R/W
11:10	—	这些位被读取为0。写入值应为0。	R/W
12	PRCEF	CRC错误帧接收模式 0：通知EDMACCRC错误1：不通知EDMACCRC错误。	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W
16	TXF	传输流控制操作模式 0：禁用自动暂停帧传输（暂停帧不自动传输） 1：启用自动暂停帧传输（PAUSE帧根据需要自动发送）。	R/W
17	RXF	接收流控制操作模式 0：禁用PAUSE帧检测1：启用PAUSE帧检测。	R/W

Bit	Symbol	Function	R/W
18	PFR	PAUSE Frame Receive Mode 0: Do not transfer PAUSE frame to the EDMAC 1: Transfer PAUSE frame to the EDMAC.	R/W
19	ZPF	0 Time PAUSE Frame Enable 0: Do not use PAUSE frames that containing a pause_time parameter of 0 1: Use PAUSE frames that containing a pause_time parameter of 0.	R/W
20	TPC	PAUSE Frame Transmit 0: Transmit PAUSE frame even during a PAUSE period 1: Do not transmit PAUSE frame during a PAUSE period.	R/W
31:21	—	These bits are read as 0. The write value should be 0.	R/W

The ECMR register controls ETHERC operation. Except for the TE and RE bits, set the bits in this register during initialization after a reset. When rewriting this register outside the initialization process, set the EDMAC0.EDMR.SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again.

PRM bit (Promiscuous Mode)

When the PRM bit is set to 1, the ETHERC operates in promiscuous mode, where all Ethernet frames are received. In promiscuous mode, the ETHERC receives all valid frames regardless of whether the address matches the destination or broadcast address, and regardless of the multicast bit setting.

RTM bit (Bit Rate)

The RTM bit sets the bit rate when the RMII is selected.

ILB bit (Internal Loopback Mode)

When the ILB bit is set to 1, transmit frames can be looped back in the MCU. Set the DM bit to 1 (full-duplex mode) to perform a loopback test.

TE bit (Transmission Enable)

When the TE bit is set to 1, the ETHERC transmit function is enabled. When the TE bit is set to 0, the transmit function is disabled after the frame being processed is completely transmitted.

RE bit (Reception Enable)

When the RE bit is set to 1, the ETHERC receive function is enabled. When the RE bit is set to 0, the receive function is disabled after the frame being processed is completely received.

PRCEF bit (CRC Error Frame Receive Mode)

When the PRCEF bit is set to 1, the EDMAC is not notified that a CRC error has occurred even when the error is detected in a receive frame. Accordingly, the EDMAC0.EESR.CERF flag and RFS0 bit in receive descriptor 0 (RD0) do not set to 1.

ZPF bit (0 Time PAUSE Frame Enable)

When the ZPF bit is 1, a PAUSE frame with a pause_time parameter of 0 is transmitted when a PAUSE frame transmit request is canceled before the PAUSE time of the previously transmitted PAUSE frame has elapsed. After the PAUSE frame containing the pause_time parameter of 0 is received, the ETHERC is ready for transmission.

When the ZPF bit is 0, even if the PAUSE frame transmit request from the receive FIFO is canceled, the next PAUSE frame is not transmitted until the PAUSE time of the previously transmitted PAUSE frame has elapsed. When a PAUSE frame containing a pause_time parameter of 0 is received, it is discarded.

Bit	Symbol	Function	R/W
18	PFR	PAUSE帧接收模式 0：不向EDMAC传输PAUSE帧1：向EDMAC传输PAUSE帧。	R/W
19	ZPF	0时间PAUSE帧启用 0：不使用包含pause_time参数为0的PAUSE帧1：使用包含pause_time参数为0的PAUSE帧。	R/W
20	TPC	PAUSE帧发送 0：即使在PAUSE期间也发送PAUSE帧1：在PAUSE期间不发送PAUSE帧。	R/W
31:21	—	这些位被读取为0。写入值应为0。	R/W

ECMR寄存器控制ETHERC操作。除TE和RE位外，在复位后初始化期间设置此寄存器中的位。在初始化过程之外重写该寄存器时，将EDMAC0.EDMR.SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。

PRM bit (Promiscuous Mode)

当PRM位设置为1时，ETHERC以混杂模式运行，其中接收所有以太网帧。在混杂模式下，ETHERC接收所有有效帧，无论地址是否匹配目标地址或广播地址，也无论多播位设置如何。

RTM bit (Bit Rate)

选择RMII时，RTM位设置了比特率。

ILB bit (Internal Loopback Mode)

当ILB位设置为1时，发送帧可以在MCU中环回。将DM位设置为1（全双工模式）以执行环回测试。

TE位（传输使能）

当TE位设置为1时，使能ETHERC发送功能。当TE位设置为0时，正在处理的帧发送完毕后，发送功能被禁用。

RE位（接收使能）

当RE位设置为1时，使能ETHERC接收功能。当RE位设置为0时，接收功能在正在处理的帧被完全接收后被禁用。

PRCEF位（CRC错误帧接收模式）

当PRCEF位设置为1时，即使在接收帧中检测到错误，也不通知EDMAC发生CRC错误。因此，接收描述符0(RD0)中的EDMAC0.EESR.CERF标志和RFS0位不会设置为1。

ZPF位（0时间暂停帧启用）

当ZPF位为1时，如果在先前发送的PAUSE帧的PAUSE时间过去之前取消PAUSE帧发送请求，则发送一个pause_time参数为0的PAUSE帧。在接收到包含pause_time参数为0的PAUSE帧后，ETHERC准备好传输。

当ZPF位为0时，即使来自接收FIFO的PAUSE帧发送请求被取消，直到前一个发送的PAUSE帧的PAUSE时间过去后，下一个PAUSE帧才会发送。当接收到包含pause_time参数为0的PAUSE帧时，将其丢弃。

26.2.2 RFLR : Receive Frame Maximum Length Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x08

Bit position:	31											11																	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFL[11:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	RFL[11:0]	Receive Frame Maximum Length The set value becomes the maximum frame length. The minimum value that can be set is 1,518 bytes, and the maximum value that can be set is 2,048 bytes. Values less than 1,518 bytes are regarded as 1,518 bytes, and values larger than 2,048 bytes are regarded as 2,048 bytes.	R/W
31:12	—	These bits are read as 0. The write value should be 0.	R/W

The RFLR register specifies the maximum frame length that can be received by the MCU. Set the length in bytes. Do not rewrite this register while the ECMR.RE bit is 1 (receive function enabled).

RFL[11:0] bits (Receive Frame Maximum Length)

The RFL[11:0] bits set the frame length to be checked. The frame length is the number of bytes in a field, extending from the destination address to the frame check sequence [FCS] of the received frame. When this length exceeds the RFL[11:0] bit value, the EDMAC is notified of a frame-too-long error, and the excess data is discarded.

26.2.3 ECSR : ETHERC Status Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	BFR	PSRTO	—	LCHNG	MPD	ICD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICD	False Carrier Detect Flag 0: PHY-LSI has not detected a false carrier on the line 1: PHY-LSI detected a false carrier on the line.	R/W*1
1	MPD	Magic Packet Detect Flag 0: Magic Packet not detected 1: Magic Packet detected.	R/W*1
2	LCHNG	Link Signal Change Flag 0: Change in the ET0_LINKSTA signal not detected 1: Change in the ET0_LINKSTA signal detected (high to low, or low to high).	R/W*1
3	—	This bit is read as 0. The write value should be 0.	R/W
4	PSRTO	PAUSE Frame Retransmit Over Flag 0: PAUSE frame retransmit count has not reached the upper limit 1: PAUSE frame retransmit count reached the upper limit.	R/W*1

26.2.2 RFLR:接收帧最大长度寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x08

Bit position:	31											11																	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFL[11:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	RFL[11:0]	接收帧最大长度 设定值成为最大帧长。可设置的最小值为1 518字节，可设置的最大值为2 048字节。小于1 518字节的值被视为1 518字节，大于2 048字节的值被视为2 048字节。	R/W
31:12	—	这些位被读取为0。写入值应为0。	R/W

RFLR寄存器指定MCU可以接收的最大帧长度。以字节为单位设置长度。当ECMR.RE位为1（启用接收功能）时不要重写该寄存器。

RFL[11:0]位（接收帧最大长度）

RFL[11:0]位设置要检查的帧长度。帧长度是一个字段中的字节数，从目标地址延伸到接收帧的帧校验序列[FCS]。当此长度超过RFL[11:0]位值时，EDMAC会收到帧太长错误的通知，并丢弃多余的数据。

26.2.3 ECSR：ETHERC状态寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	BFR	PSRTO	—	LCHNG	MPD	ICD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICD	错误载波检测标志 0：PHY-LSI未检测到线路上的虚假载波1：PHY-LSI检测到线路上的虚假载波。	R/W*1
1	MPD	魔术包检测标志 0：未检测到魔术包1：检测到魔术包。	R/W*1
2	LCHNG	链路信号变化标志 0：未检测到ET0_LINKSTA信号变化1：检测到ET0_LINKSTA信号变化（从高到低，或从低到高）。	R/W*1
3	—	该位读取为0。写入值应为0。	R/W
4	PSRTO	PAUSE帧重传标志 0：PAUSE帧重传计数未达到上限1：PAUSE帧重传计数达到上限。	R/W*1

Bit	Symbol	Function	R/W
5	BFR	Continuous Broadcast Frame Reception Flag 0: Continuous reception of broadcast frames not detected 1: Continuous reception of broadcast frames detected.	R/W*1
31:6	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Write 1 to clear the flag.

The ECSR register indicates the status of the ETHERC. When any flag in the ECSR register is set to 1 while the associated bit in the ECSIPR register is 1 (interrupt enabled), the EDMAC0.EESR.ECI flag is set to 1.

ICD flag (False Carrier Detect Flag)

The ICD flag indicates that the PHY-LSI has detected a false carrier on the line. The flag is set to 1 when a receive error signal shown in Figure 26.11 is received from the PHY-LSI. The information might not be correct when signals input from the PHY-LSI change faster than software recognizes the change. Check the timing of the PHY-LSI.

LCHNG flag (Link Signal Change Flag)

The LCHNG flag indicates that the ET0_LINKSTA signal input from the PHY-LSI has changed from high to low, or from low to high. Check the PSR.LMON flag for the current link status. See section 26.5.1. Preventing the LCHNG Flag from Erroneously Setting to 1 for more information.

PSRTO flag (PAUSE Frame Retransmit Over Flag)

The PSRTO flag indicates that the number of retransmissions reached the value set in the TPAUSER register when retransmitting a PAUSE frame while automatic PAUSE frame transmission is enabled.

26.2.4 ECSIPR : ETHERC Interrupt Enable Register

Base address: ETHERC0 = 0x4011 4100

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	BFSIPR	PSRTOIP	—	LCHNGIP	MPDIP	ICDIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICDIP	False Carrier Detect Interrupt Enable 0: Disable interrupt notification 1: Enable interrupt notification.	R/W
1	MPDIP	Magic Packet Detect Interrupt Enable 0: Disable interrupt notification 1: Enable interrupt notification.	R/W
2	LCHNGIP	LINK Signal Change Interrupt Enable 0: Disable interrupt notification 1: Enable interrupt notification.	R/W
3	—	These bits are read as 0. The write value should be 0.	R/W
4	PSRTOIP	PAUSE Frame Retransmit Over Interrupt Enable 0: Disable interrupt notification 1: Enable interrupt notification.	R/W
5	BFSIPR	Continuous Broadcast Frame Reception Interrupt Enable 0: Disable interrupt notification 1: Enable interrupt notification.	R/W

Bit	Symbol	Function	R/W
5	BFR	连续广播帧接收标志 0：未检测到连续接收广播帧1：检测到连续接收广播帧。	R/W*1
31:6	—	这些位被读取为0。写入值应为0。	R/W

注1.写1清除标志。

ECSR寄存器指示ETHERC的状态。当ECSR寄存器中的任何标志设置为1且ECSIPR寄存器中的相关位为1（允许中断）时，EDMAC0.EESR.ECI标志设置为1。

ICD标志（错误载波检测标志）

ICD标志表示PHY-LSI检测到线路上的错误载波。当从PHY-LSI接收到图26.11所示的接收错误信号时，该标志设置为1。当来自PHY-LSI的信号输入变化快于软件识别变化的速度时，该信息可能不正确。检查PHY-LSI的时序。

LCHNG标志（链路信号变化标志）

LCHNG标志表示从PHY-LSI输入的ET0_LINKSTA信号已由高变为低，或由低变为高。检查当前链接状态的PSR.LMON标志。请参阅第26.5.1节。防止LCHNG标志错误地设置为1以获取更多信息。

PSRTO标志（暂停帧重传结束标志）

PSRTO标志表示在启用自动PAUSE帧传输时重传PAUSE帧时重传次数达到TPAUSER寄存器中设置的值。

26.2.4 ECSIPR:ETHERC中断使能寄存器

Base address: ETHERC0 = 0x4011 4100

Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	BFSIPR	PSRTOIP	—	LCHNGIP	MPDIP	ICDIP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICDIP	假载波检测中断使能 0：禁用中断通知1：启用中断通知。	R/W
1	MPDIP	魔术包检测中断使能 0：禁用中断通知1：启用中断通知。	R/W
2	LCHNGIP	LINK信号变化中断使能 0：禁用中断通知1：启用中断通知。	R/W
3	—	这些位被读取为0。写入值应为0。	R/W
4	PSRTOIP	PAUSE帧重传中断使能 0：禁用中断通知1：启用中断通知。	R/W
5	BFSIPR	连续广播帧接收中断使能 0：禁用中断通知1：启用中断通知。	R/W

Bit	Symbol	Function	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

The ECSIPR register selects whether to notify the EDMAC of the status indicated in the ECSR register. Each bit is associated with the flag with the same bit number in the ECSR register.

26.2.5 PIR : PHY Interface Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
0	MDC	MII/RMII Management Data Clock This value is output from the ET0_MDC pin to supply the management data clock to the MII or RMII.	R/W
1	MMD	MII/RMII Management Mode 0: Read 1: Write.	R/W
2	MDO	MII/RMII Management Data-Out This value is output from the ET0_MDIO pin when the MMD bit is 1 (write), and not when MMD is 0 (read).	R/W
3	MDI	MII/RMII Management Data-In This bit indicates the level of the ET0_MDIO pin. The write value should be 0.	R
31:4	—	These bits are read as 0. The write value should be 0.	R/W

The PIR register accesses registers in the PHY-LSI through the MII or RMII. The management clock and management data are controlled by software. See section 26.3.4. Accessing the MII and RMII Registers for details on accessing the MII and RMII registers.

26.2.6 PSR : PHY Status Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x28

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LMON
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	LMON	ET0_LINKSTA Pin Status Flag The link status can be read by connecting the link signal output from the PHY-LSI to the ET0_LINKSTA pin. For details on the polarity, see the specifications of the connected PHY-LSI.	R
31:1	—	This bit is read as 0.	R

The PSR register monitors interface signals from the PHY-LSI.

Bit	Symbol	Function	R/W
31:6	—	这些位被读取为0。写入值应为0。	R/W

ECSIPR寄存器选择是否将ECSR寄存器中指示的状态通知EDMAC。每个位都与ECSR寄存器中具有相同位号的标志相关联。

26.2.5 PIR:PHY接口寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
0	MDC	MIIRMII管理数据时钟 该值从ET0_MDC引脚输出，为MII或RMII提供管理数据时钟。	R/W
1	MMD	MIIRMII管理模式 0：读取1 ：写入。	R/W
2	MDO	MII/RMII Management Data-Out 该值在MMD位为1（写入）时从ET0_MDIO引脚输出，而不是在 MMD is 0 (read).	R/W
3	MDI	MII/RMII Management Data-In 该位指示ET0_MDIO引脚的电平。写入值应为0。	R
31:4	—	这些位被读取为0。写入值应为0。	R/W

PIR寄存器通过MII或RMII访问PHY-LSI中的寄存器。管理时钟和管理数据由软件控制。请参阅第26.3.4节。访问MII和RMII寄存器以获取有关访问MII和RMII寄存器的详细信息。

26.2.6 PSR：物理状态寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x28

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LMON
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	LMON	ET0_LINKSTA引脚状态标志 通过将PHY-LSI输出的链路信号连接到 ET0_LINKSTA引脚。有关极性的详细信息，请参阅所连接PHY的规格 LSI.	R
31:1	—	该位读为0。	R

PSR寄存器监视来自PHY-LSI的接口信号。

26.2.7 RDMLR : Random Number Generation Counter Upper Limit Setting Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x40

Bit position:	31												19												0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RMD[19:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
19:0	RMD[19:0]	Random Number Generation Counter 0x00000: Normal operation 0x00001 to 0xFFFFF: Setting prohibited.	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The RDMLR register specifies the maximum value for the counter used in the random number generator. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled).

26.2.8 IPGR : Interpacket Gap Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x50

Bit position:	31																								4	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IPG[4:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0			

Bit	Symbol	Function	R/W
4:0	IPG[4:0]	Interpacket Gap 0x00: 16 bit times 0x01: 20 bit times ⋮ 0x14: 96 bit times (initial value) ⋮ 0x1F: 140 bit times.	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

The IPGR register specifies the interpacket gap (IPG) value. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled). See section 26.3.6. Adjusting Transmission Efficiency by Changing the IPG for details on the IPG.

26.2.9 APR : Automatic PAUSE Frame Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x54

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

26.2.7 RDMLR：随机数生成计数器上限设置寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x40

Bit position:	31												19												0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RMD[19:0]												
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
19:0	RMD[19:0]	随机数生成计数器0x00000：正常操作0 x00001至0xFFFFF：禁止设置。	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

RDMLR寄存器指定随机数发生器中使用的计数器的最大值。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。

26.2.8 IPGR：包间间隙寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x50

Bit position:	31																								4	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IPG[4:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0			

Bit	Symbol	Function	R/W
4:0	IPG[4:0]	Interpacket Gap 0x00：16位时间0 x01：20位时间 ⋮ 0x14：96位时间（初始值） ⋮ 0x1F：140位时间。	R/W
31:5	—	这些位被读取为0。写入值应为0。	R/W

IPGR寄存器指定包间间隙(IPG)值。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。请参阅第26.3.6节。通过更改IPG调整传输效率，了解IPG的详细信息。

26.2.9 APR：自动暂停帧寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x54

Bit position:	31															15															0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AP[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	AP[15:0]	Automatic PAUSE Time Setting These bits set the value of the pause_time parameter for PAUSE frames that are automatically transmitted. Transmission is not performed until a period equal to the set value multiplied by 512 bit times has elapsed.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The APR register specifies the PAUSE time for PAUSE frames that are automatically transmitted. The value set in the APR register is used for the pause_time parameter of the PAUSE frame. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled).

26.2.10 MPR : Manual PAUSE Frame Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x58

Bit position:	31															15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MP[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	MP[15:0]	Manual PAUSE Time Setting These bits set the value of the pause_time parameter for PAUSE frames that are manually transmitted. Transmission is not performed until the set value multiplied by 512 bit times has elapsed. The read value is undefined.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The MPR register specifies the PAUSE time for PAUSE frames that are manually transmitted. The value set in the MPR register is used for the pause_time parameter of the PAUSE frame. When a value is set to this register, a PAUSE frame is transmitted. Rewrite this register while the ECMR.TE bit is 1 (transmit function enabled).

26.2.11 RFCF : Received PAUSE Frame Counter

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x60

Bit position:	31																								7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPAUSE[7:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RPAUSE[7:0]	Received PAUSE Frame Count Number of received PAUSE frames.	R
31:8	—	This bit is read as 0.	R

The RFCF register is a counter that indicates the number of received PAUSE frames. The counter is reset after this register is read.

Bit	Symbol	Function	R/W
15:0	AP[15:0]	自动暂停时间设置 这些位为自动传输的PAUSE帧设置pause_time参数的值。在等于设置值乘以512位时间的周期过去之前，不执行传输。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

APR寄存器指定自动发送的暂停帧的暂停时间。APR寄存器中设置的值用于PAUSE帧的pause_time参数。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。

26.2.10 MPR：手动暂停帧寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x58

Bit position:	31															15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MP[15:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
15:0	MP[15:0]	手动暂停时间设置 这些位为手动传输的PAUSE帧设置pause_time参数的值。在设定值乘以512位时间之前，不执行传输。读取值未定义。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

MPR寄存器指定手动发送的暂停帧的暂停时间。MPR寄存器中设置的值用于PAUSE帧的pause_time参数。当一个值被设置到这个寄存器时，一个暂停帧被发送。当ECMR.TE位为1（启用发送功能）时重写该寄存器。

26.2.11 RFCF:接收暂停帧计数器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x60

Bit position:	31																								7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RPAUSE[7:0]						
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RPAUSE[7:0]	接收暂停帧计数 接收到的暂停帧数。	R
31:8	—	该位读为0。	R

RFCF寄存器是一个计数器，用于指示接收到的PAUSE帧的数量。读取该寄存器后计数器复位。

26.2.12 TPAUSER : PAUSE Frame Retransmit Count Setting Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x64

Bit position:	31																15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TPAUSE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TPAUSE[15:0]	Automatic PAUSE Frame Retransmit Setting 0x0000 0: Number of retransmissions is unlimited 0x0000 1: Maximum number of retransmissions is 1 ⋮ ⋮ 0xFFFF F: Maximum number of retransmissions is 65,535.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The TPAUSECR register selects the maximum number of times a PAUSE frame is automatically transmitted. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled).

26.2.13 TPAUSECR : PAUSE Frame Retransmit Counter

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x68

Bit position:	31																								7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXP[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXP[7:0]	PAUSE Frame Retransmit Count Number of times a PAUSE frame was retransmitted.	R
31:8	—	These bits are read as 0.	R

The TPAUSECR register is a counter that indicates the number of times a PAUSE frame was automatically retransmitted. The counter is reset after this register is read.

26.2.14 BCFRR : Broadcast Frame Receive Count Setting Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x6C

Bit position:	31																15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

26.2.12 TPAUSER：暂停帧重传计数设置寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x64

Bit position:	31																15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TPAUSE[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TPAUSE[15:0]	自动暂停帧重传设置 0x0000 0: 重传次数不限 0x0000 1: 最大重传次数为1 ⋮ ⋮ 0xFFFF F: 最大重传次数为65 535。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

TPAUSECR寄存器选择自动发送暂停帧的最大次数。当ECMR.TE位为1（启用发送功能）时不要重写该寄存器。

26.2.13 TPAUSECR:暂停帧重传计数器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x68

Bit position:	31																								7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXP[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXP[7:0]	PAUSE帧重传计数 重传PAUSE帧的次数。	R
31:8	—	这些位读为0。	R

TPAUSECR寄存器是一个计数器，指示暂停帧自动重传的次数。
读取该寄存器后计数器复位。

26.2.14 BCFRR:广播帧接收计数设置寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0x6C

Bit position:	31																15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BCF[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	BCF[15:0]	Broadcast Frame Continuous Receive Count Setting 0x0000 Number of reception is unlimited : 0x0001 Receive 1 frame. : ⋮ 0xFFFF Receive 65,535 frames. :	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The BCFRR register specifies the number of times broadcast frames can be received continuously. When the number of received frames exceeds the BCF[15:0] bit value, the excess broadcast frames are discarded. Do not rewrite this register while the EMCR.RE bit is 1 (receive function enabled).

26.2.15 MAHR : MAC Address Upper Bit Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xC0

Bit position:	31																												0
Bit field:	MAHR[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	MAHR[31:0]	MAC Address Upper Bit See the following.	R/W

The MAHR register specifies the upper 32 bits ([47:16]) of the 48-bit MAC address. For example, if the MAC address is 01-23-45-67-89-AB, set the register to 0x01234567.

Set the MAHR register during initialization after a reset. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled). When rewriting this register, set the EDMAC0.EDMR.SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again.

26.2.16 MALR : MAC Address Lower Bit Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xC8

Bit position:	31															15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MALR[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	MALR[15:0]	MAC Address Lower Bit These bits set the lower 16 bits of the MAC address.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The MALR register specifies the lower 16 bits of the 48-bit MAC address. For example, if the MAC address is 01-23-45-67-89-AB, set the register to 0x000089AB.

Set the MALR register during initialization after a reset. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled). When rewriting this register, set the EDMAC0.EDMR.SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again.

Bit	Symbol	Function	R/W
15:0	BCF[15:0]	广播帧连续接收计数设置 0x0000 接待人数不限 : 0x0001 接收1帧。 : ⋮ 0xFFFF 接收65 535帧。 :	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

BCFRR寄存器指定可以连续接收广播帧的次数。当接收到的帧数超过BCF[15:0]位值时，多余的广播帧将被丢弃。当EMCR.RE位为1（启用接收功能）时，请勿重写此寄存器。

26.2.15 MAHR:MAC地址高位寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xC0

Bit position:	31																												0
Bit field:	MAHR[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	MAHR[31:0]	MAC地址高位 请参阅以下内容。	R/W

MAHR寄存器指定48位MAC地址的高32位([47:16])。例如，如果MAC地址为01-23-45-67-89-AB，则将寄存器设置为0x01234567。

在复位后初始化期间设置MAHR寄存器。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。重写该寄存器时，将EDMAC0.EDMR.SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。

26.2.16 MALR:MAC地址低位寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xC8

Bit position:	31															15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MALR[15:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	MALR[15:0]	MAC地址低位 这些位设置MAC地址的低16位。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

MALR寄存器指定48位MAC地址的低16位。例如，如果MAC地址为01-23-45-67-89-AB，则将寄存器设置为0x000089AB。

在复位后初始化期间设置MALR寄存器。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。重写该寄存器时，将EDMAC0.EDMR.SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。

26.2.17 TROCR : Transmit Retry Over Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xD0

Bit position:	31																													0
Bit field:	TROCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TROCR[31:0]	Transmit Retry Over Counter See the following.	R/W

The TROCR register is a counter that indicates the number of frames that failed to be retransmitted. The register value is incremented by 1 when a frame fails to be retransmitted 15 times. The counter stops when the register value becomes 0xFFFF_FFFF. Writing any value to the TROCR register clears the counter value to 0.

26.2.18 CDCR : Late Collision Detect Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xD4

Bit position:	31																													0
Bit field:	CDCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CDCR[31:0]	Late Collision Detect Counter See the following.	R/W

The CDCR register is a counter that indicates the number of late collisions that are detected after transmission starts. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the CDCR register clears the counter value to 0.

26.2.19 LCCR : Lost Carrier Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xD8

Bit position:	31																													0
Bit field:	LCCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	LCCR[31:0]	Lost Carrier Counter See the following.	R/W

The LCCR register is a counter that indicates the number of times a loss of carrier is detected during frame transmission.

When the register value becomes 0xFFFF FFFF, the counter stops. Writing any value to the LCCR register clears the counter value to 0.

26.2.17 TROCR：通过计数器发送重试寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xD0

Bit position:	31																													0
Bit field:	TROCR[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TROCR[31:0]	计数器传输重试 请参阅以下内容。	R/W

TROCR寄存器是一个计数器，用于指示重传失败的帧数。当一帧重传15次失败时，寄存器值加1。当寄存器值变为0xFFFF_FFFF时，计数器停止。向TR OCR寄存器写入任何值都会将计数器值清除为0。

26.2.18 CDCR：后期冲突检测计数器寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xD4

Bit position:	31																													0
Bit field:	CDCR[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CDCR[31:0]	后期碰撞检测计数器 请参阅以下内容。	R/W

CDCR寄存器是一个计数器，用于指示在传输开始后检测到的后期冲突数。当寄存器值变为0xFFFF_FFFF时，计数器停止。向CDCR寄存器写入任何值都会将计数器值清零。

26.2.19 LCCR:LostCarrierCounterRegister

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xD8

Bit position:	31																													0
Bit field:	LCCR[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	LCCR[31:0]	遗失承运人柜台 请参阅以下内容。	R/W

LCCR寄存器是一个计数器，用于指示在帧传输期间检测到载波丢失的次数。

当寄存器值变为0xFFFFFFFF时，计数器停止。向LCCR寄存器写入任何值都会将计数器值清零。

26.2.20 CNDCR : Carrier Not Detect Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xDC

Bit position:	31																													0
Bit field:	CNDCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CNDCR[31:0]	Carrier Not Detect Counter See the following.	R/W

The CNDCR register is a counter that indicates the number of times a carrier is not detected during preamble transmission. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the CNDCR register clears the counter value to 0.

26.2.21 CEFCR : CRC Error Frame Receive Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xE4

Bit position:	31																													0
Bit field:	CEFCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CEFCR[31:0]	CRC Error Frame Receive Counter See the following.	R/W

The CEFCR register is a counter that indicates the number of received frames in which a CRC error was detected. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the CEFCR register clears the counter value to 0.

26.2.22 FRECR : Frame Receive Error Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xE8

Bit position:	31																													0
Bit field:	FRECR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FRECR[31:0]	Frame Receive Error Counter See the following.	R/W

The FRECR register is a counter that indicates the number of times a frame receive error has occurred. The PHY-LSI notifies the ETHERC of the frame receive error using the ET0_RX_ER pin. The FRECR register increments each time the ET0_RX_ER pin goes high. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the FRECR register clears the counter value to 0.

26.2.20 CNDCR:载波未检测计数器寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xDC

Bit position:	31																													0
Bit field:	CNDCR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CNDCR[31:0]	运营商未检测计数器 请参阅以下内容。	R/W

CNDCR寄存器是一个计数器，指示在前导码传输期间未检测到载波的次数。
当寄存器值变为0xFFFF_FFFF时，计数器停止。向CNDCR寄存器写入任何值都会将计数器值清除为0。

26.2.21 CEFCR:CRC错误帧接收计数器寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xE4

Bit position:	31																													0
Bit field:	CEFCR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CEFCR[31:0]	CRC错误帧接收计数器 请参阅以下内容。	R/W

CEFCR寄存器是一个计数器，用于指示检测到CRC错误的接收帧数。当寄存器值变为0xFFFF_FFFF时，计数器停止。向CEFCR寄存器写入任何值都会将计数器值清零。

26.2.22 FRECR:帧接收错误计数器寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xE8

Bit position:	31																													0
Bit field:	FRECR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FRECR[31:0]	帧接收错误计数器 请参阅以下内容。	R/W

FRECR寄存器是一个计数器，用于指示帧接收错误发生的次数。PHY-LSI使用ET0_RX_ER引脚将帧接收错误通知ETHERC。每次ET0_RX_ER引脚变高时，FRECR寄存器都会递增。当寄存器值变为0xFFFF_FFFF时，计数器停止。
将任何值写入

FRCR寄存器将计数器值清零。

26.2.23 TSFRCR : Too-Short Frame Receive Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xEC

Bit position:	31																													0
Bit field:	TSFRCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TSFRCR[31:0]	Too-Short Frame Receive Counter See the following.	R/W

The TSFRCR register is a counter that indicates the number of times a short frame that is shorter than 64 bytes was received. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the TSFRCR register clears the counter value to 0.

26.2.24 TLFRCR : Too-Long Frame Receive Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xF0

Bit position:	31																													0
Bit field:	TLFRCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TLFRCR[31:0]	Too-Long Frame Receive Counter See the following.	R/W

Note: The TLFRCR register does not increment when a frame is received with an alignment error. In this case, the RFCR register increments.

The TLFRCR register is a counter that indicates the number of times a long frame that is longer than the RFLR register value was received. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the TLFRCR register clears the counter value to 0.

26.2.25 RFCR : Received Alignment Error Frame Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xF4

Bit position:	31																													0
Bit field:	RFCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RFCR[31:0]	Received Alignment Error Frame Counter See the following.	R/W

The RFCR register is a counter that indicates the number of times a frame was received with an alignment error, meaning that it is not an integral number of octets. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the RFCR register clears the counter value to 0.

26.2.23 TSFRCR:Too-ShortFrameReceiveCounterRegister

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xEC

Bit position:	31																													0
Bit field:	TSFRCR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TSFRCR[31:0]	帧接收计数器过短 请参阅以下内容。	R/W

TSFRCR寄存器是一个计数器，用于指示接收到短于64字节的短帧的次数。当寄存器值变为0xFFFF_FFFF时，计数器停止。向TSFRCR寄存器写入任何值都会将计数器值清除为0。

26.2.24 TLFRCR:Too-LongFrameReceiveCounterRegister

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xF0

Bit position:	31																													0
Bit field:	TLFRCR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	TLFRCR[31:0]	帧接收计数器过长 请参阅以下内容。	R/W

Note: 当接收到有对齐错误的帧时，TLFRCR寄存器不会增加。在这种情况下，RFCR寄存器递增。

TLFRCR寄存器是一个计数器，用于指示接收到长于RFLR寄存器值的长帧的次数。当寄存器值变为0xFFFF_FFFF时，计数器停止。向TLFRCR寄存器写入任何值都会将计数器值清零。

26.2.25 RFCR：接收对齐错误帧计数器寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xF4

Bit position:	31																													0
Bit field:	RFCR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RFCR[31:0]	接收对齐错误帧计数器 请参阅以下内容。	R/W

RFCR寄存器是一个计数器，指示接收到的帧出现对齐错误的次数，这意味着它不是八位字节的整数。当寄存器值变为0xFFFF_FFFF时，计数器停止。向RFCR寄存器写入任何值都会将计数器值清除为0。

26.2.26 MAFCR : Multicast Address Frame Receive Counter Register

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xF8

Bit position:	31																													0
Bit field:	MAFCR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	MAFCR[31:0]	Multicast Address Frame Receive Counter See the following.	R/W

The MAFCR register is a counter that indicates the number of times a frame with the multicast address set was received. When the register value becomes 0xFFFF_FFFF, the counter stops. Writing any value to the MAFCR register clears the counter value to 0.

26.3 Operation

This section provides an overview of the ETHERC operations. ETHERC supports the flow control compliant with IEEE802.3x, and can transmit and receive PAUSE frames.

26.3.1 Transmission

The ETHERC transmitter assembles the transmit data into a frame and outputs it to the MII or RMII when a transmit request is received from the EDMAC. The frame transmitted through the MII or RMII is transmitted on the line by the PHY-LSI.

Figure 26.4 shows the state transitions of the ETHERC transmitter.

26.2.26 MAFCR:多播地址帧接收计数器寄存器

Base address: ETHERC0 = 0x4011_4100

Offset address: 0xF8

Bit position:	31																													0
Bit field:	MAFCR[31:0]																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	MAFCR[31:0]	组播地址帧接收计数器 请参阅以下内容。	R/W

MAFCR寄存器是一个计数器，用于指示接收到设置了多播地址的帧的次数。当寄存器值变为0xFFFF_FFFF时，计数器停止。向MAFCR寄存器写入任何值都会将计数器值清除为0。

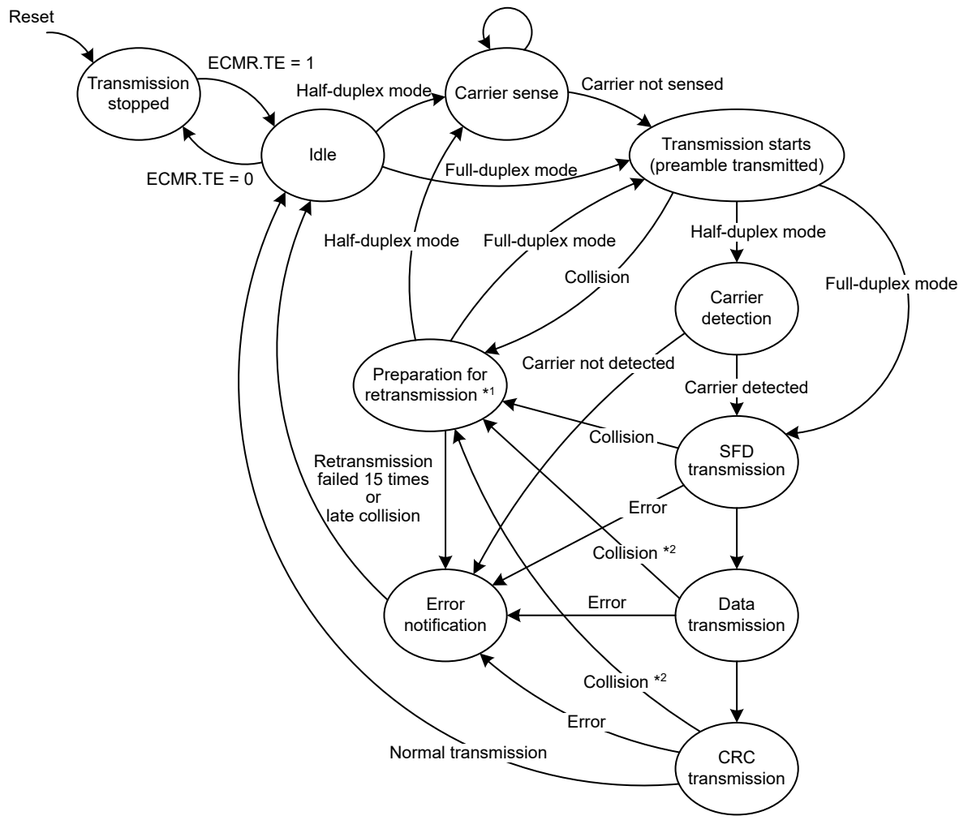
26.3 Operation

本节概述了ETHERC操作。ETHERC支持符合以下标准的流量控制IEEE802.3x，可收发PAUSE帧。

26.3.1 Transmission

ETHERC发送器将发送数据组装成一个帧，并在收到来自EDMAC的发送请求时将其输出到MII或RMII。通过MII或RMII传输的帧由PHYLSI在线路上传输。

图26.4显示了ETHERC发送器的状态转换。

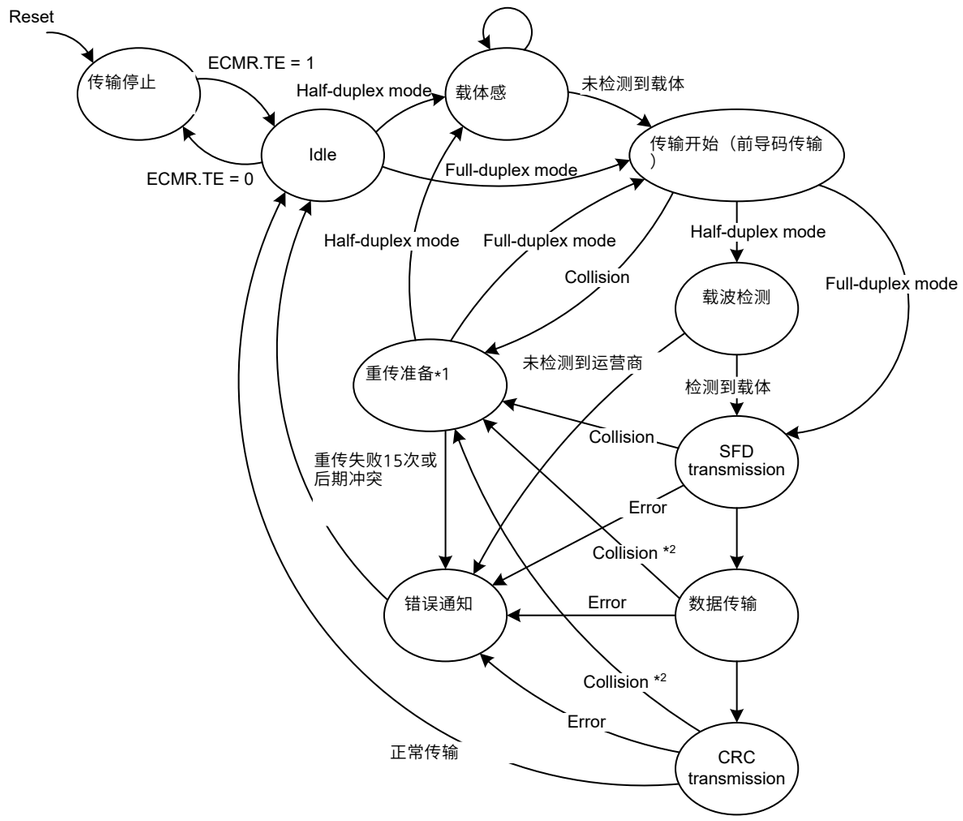


Note 1. Preparation for retransmission after a collision is detected includes transmitting a jam signal and adjusting transmission time intervals using the backoff algorithm.
Note 2. Preparation for retransmission is performed only when a collision is detected within 512 bit times after preamble transmission starts. When a collision is detected after 512 bit times, only a jam signal is transmitted and processing using the backoff algorithm is not performed.

Figure 26.4 ETHERC transmitter state transitions

The ETHERC transmitter state transitions are as follows:

1. When the ECMR.TE bit is set to 1, the ETHERC enters the transmit idle state.
2. When a transmit request is received from the EDMAC, the ETHERC enters the carrier sense state. The ETHERC waits for the interpacket gap and then transmits a preamble to the MII or RMII. When full-duplex mode is selected, carrier sensing is not required, so the ETHERC transmits a preamble immediately after receiving a transmit request from the EDMAC.
3. The ETHERC transmits the Start Frame Delimiter (SFD), transmit data, and CRC sequentially. When the transmission completes successfully, the ETHERC notifies the EDMAC of successful completion, and the EDMAC sets the EDMAC0.EESR.TC flag to 1. When a late collision or loss of carrier is detected during data transmission, the ETHERC stops the transmission and notifies the EDMAC of the error.
4. After the time specified as the interpacket gap has elapsed, the ETHERC enters the idle state and continues the transmission when transmit data remains.



注1：检测到冲突后重传的准备工作包括传输阻塞信号和使用退避算法调整传输时间间隔。

注2.只有在前导码后512比特时间内检测到冲突时，才进行重传准备
传输开始。当在512位时间后检测到冲突时，仅传输阻塞信号，并且不执行使用退避算法的处理。

Figure 26.4 ETHERC发送器状态转换

ETHERC发送器状态转换如下：

1.当ECMR.TE位设置为1时，ETHERC进入发送空闲状态。

2.当收到来自EDMAC的发送请求时，ETHERC进入载波侦听状态。ETHERC等待包间间隙，然后将前同步码发送到MII或RMII。Whenfull-duplexmodeisselected carriersensingisnotrequired sotheETHERCtransmitsapreambleimmediatelyafterreceivingatransmitrequestfromtheEDMAC.

3.ETHERC依次传输起始帧定界符（SFD）、传输数据和CRC。当传输成功完成时，ETHERC通知EDMAC成功完成，EDMAC将EDMAC0.EESR.TC标志设置为1。当在数据传输过程中检测到延迟冲突或载波丢失时，ETHERC停止传输并通知错误的EDMAC。

4.指定的包间间隙时间过去后，ETHERC进入空闲状态，并在传输数据剩余时继续传输。

26.3.2 Reception

The ETHERC receiver separates the frame input from the MII or RMII into the preamble, SFD, receive data, and CRC, and transmits only the receive data (destination address, source address, type/length, data/LLC). Figure 26.5 shows the state transitions of the ETHERC receiver.

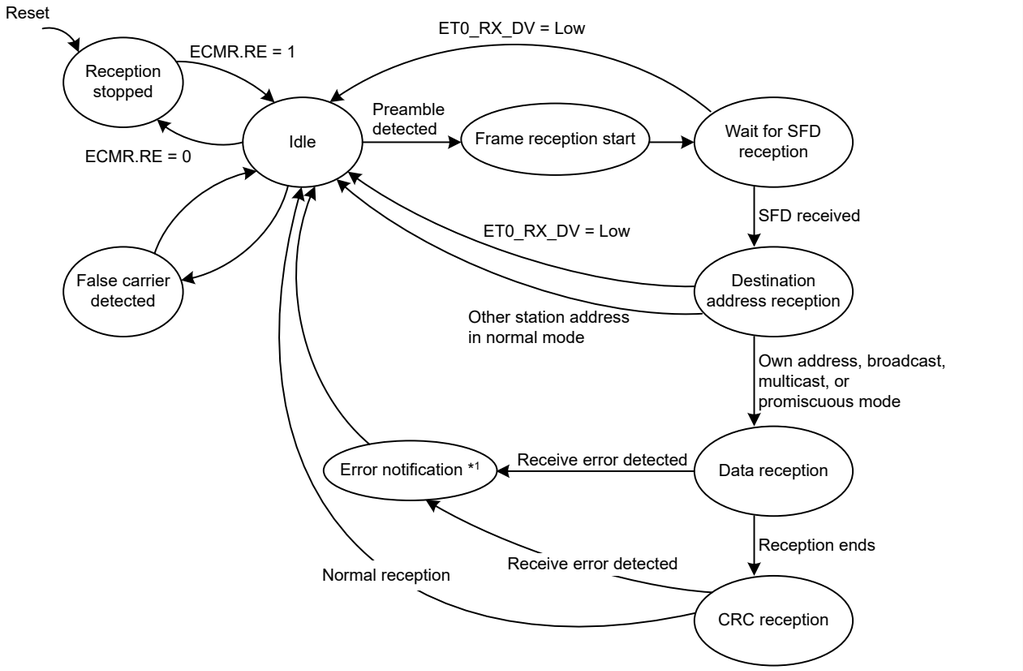


Figure 26.5 ETHERC receiver state transitions

The ETHERC receiver state transitions are as follows:

1. When the ECMR.RE bit is set to 1, the ETHERC enters the receive idle state.
2. When the SFD following the preamble of the receive packet is detected, the ETHERC starts reception. If the received SFD is invalid, the ETHERC discards the frame.
3. In normal mode, the ETHERC starts data reception when the destination address of the receive frame is the address of the MCU or the receive frame is a broadcast or multicast frame. In promiscuous mode, the ETHERC starts data reception regardless of the receive frame type.
4. After receiving data from the MII or RMII, the ETHERC performs a CRC check. The ETHERC notifies the EDMAC of the CRC check result. After the received data is transferred to the receive buffer, the CRC check result is written back to the receive descriptor as status. The result is also reflected in the EDMAC0.EESR.CERF flag.
5. When the ECMR.RE bit is 1 after one frame is received, the ETHERC prepares to receive the next frame.

26.3.2 Reception

ETHERC接收器将从MII或RMII输入的帧分离为前导码、SFD、接收数据和CRC，并仅发送接收数据（目标地址、源地址、类型长度、数据LLC）。图26.5显示了ETHERC接收器的状态转换。

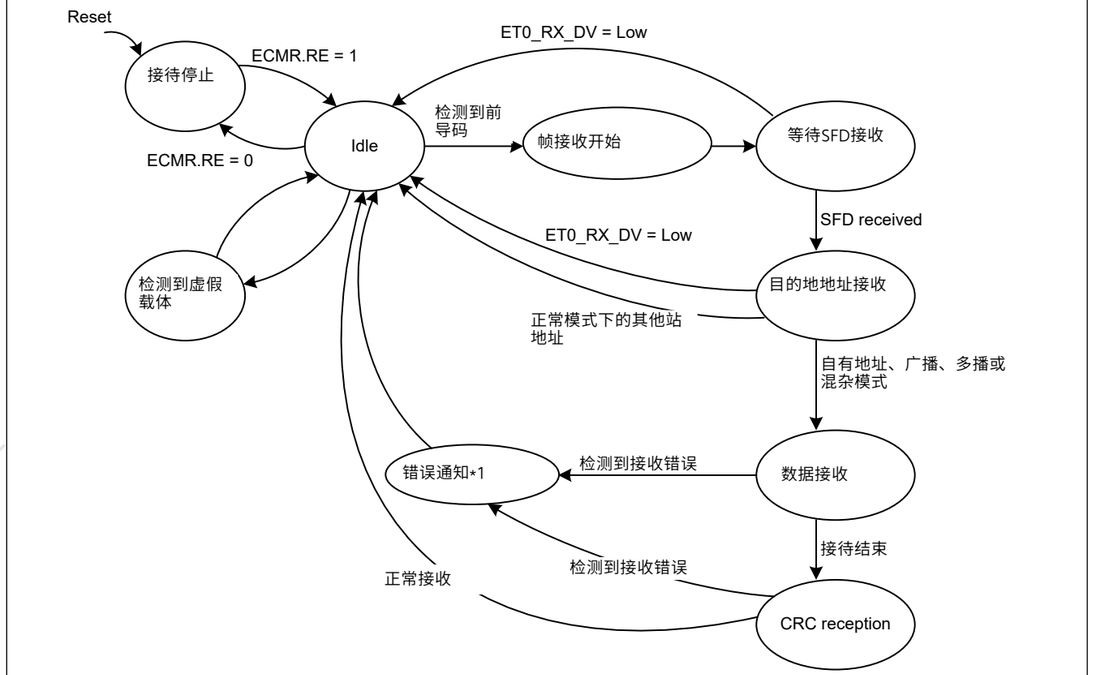


Figure 26.5 ETHERC接收器状态转换

ETHERC接收器状态转换如下：

1.当ECMR.RE位设置为1时，ETHERC进入接收空闲状态。

2.当检测到接收包前导码后面的SFD时，ETHERC开始接收。如果接收到的SFD无效，则ETHERC丢弃该帧。

3.普通模式下，当接收帧的目的地址为MCU地址或接收帧为广播或组播帧时，ETHERC开始数据接收。在混杂模式下，无论接收帧类型如何，ETHERC都会开始数据接收。

4.ETHERC接收到来自MII或RMII的数据后，进行CRC校验。ETHERC将CRC校验结果通知给EDMAC。接收到的数据传送到接收缓冲区后，CRC校验结果作为状态写回接收描述符。结果也反映在EDMAC0.EESR.CERF标志中。

5.当接收到一帧后ECMR.RE位为1时，ETHERC准备接收下一帧。

26.3.3 Frame Timing

26.3.3.1 MII frame timing

Figure 26.6 to Figure 26.11 show the MII frame timing.

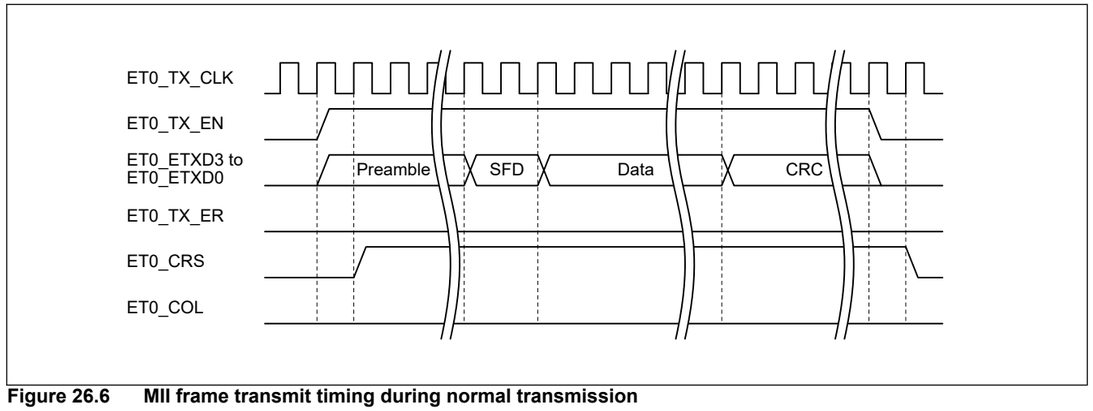


Figure 26.6 MII frame transmit timing during normal transmission

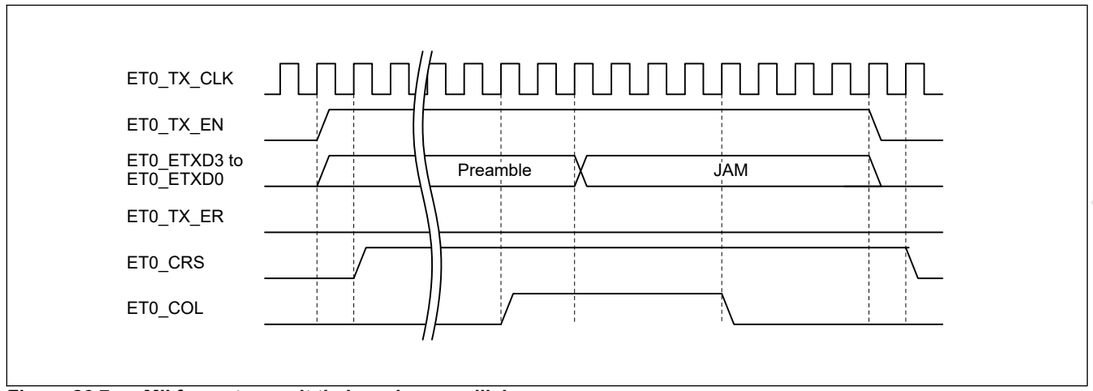


Figure 26.7 MII frame transmit timing when a collision occurs

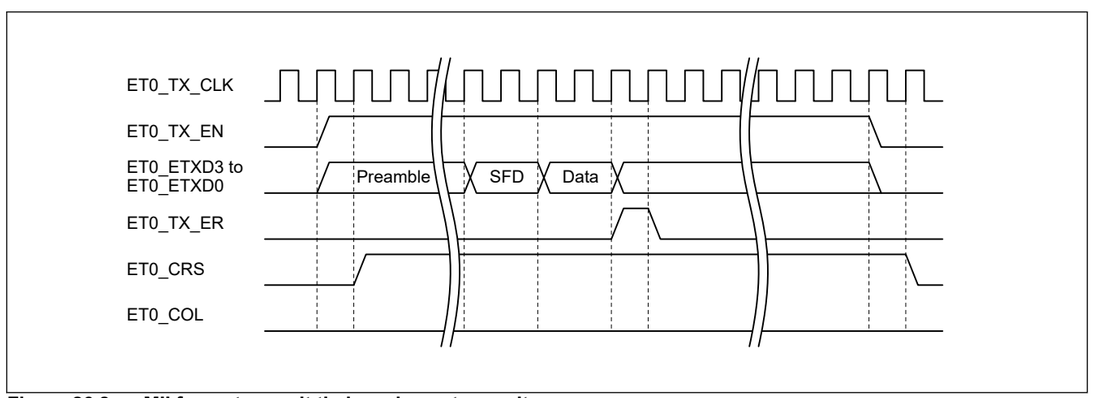


Figure 26.8 MII frame transmit timing when a transmit error occurs

26.3.3 帧时序

26.3.3.1 MII帧时序

图26.6至图26.11显示了MII帧时序。

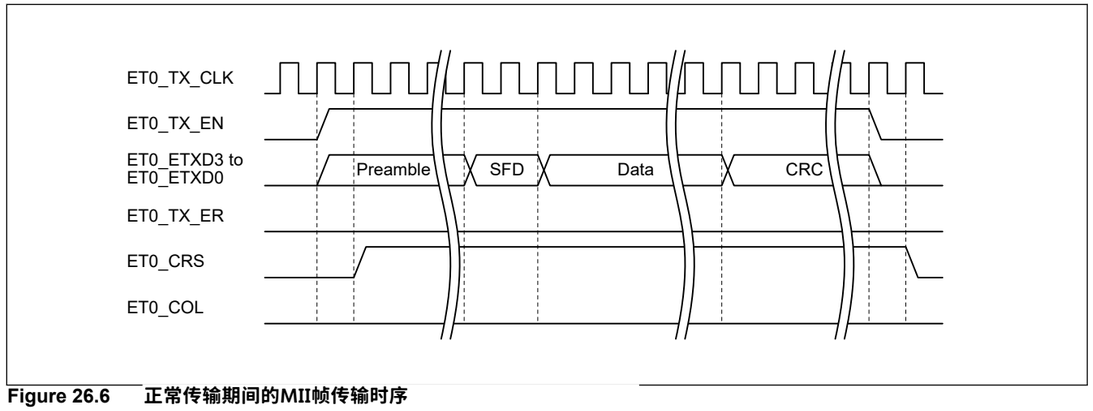


Figure 26.6 正常传输期间的MII帧传输时序

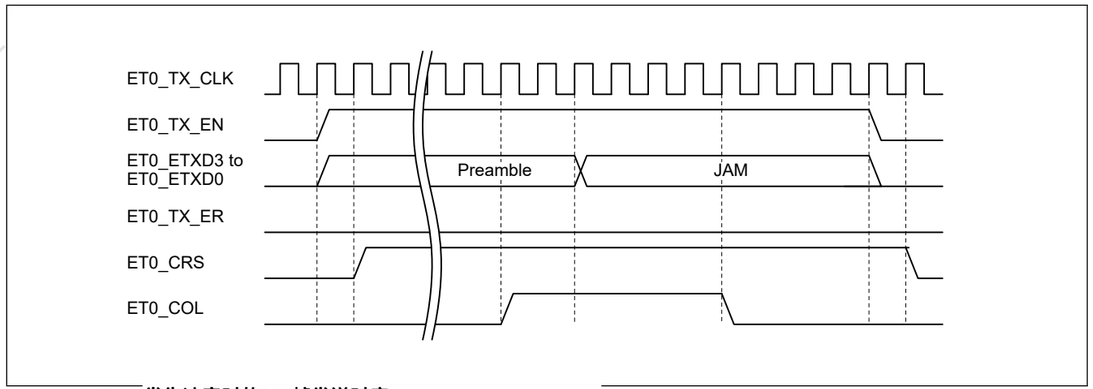


Figure 26.7 发生冲突时的MII帧发送时序

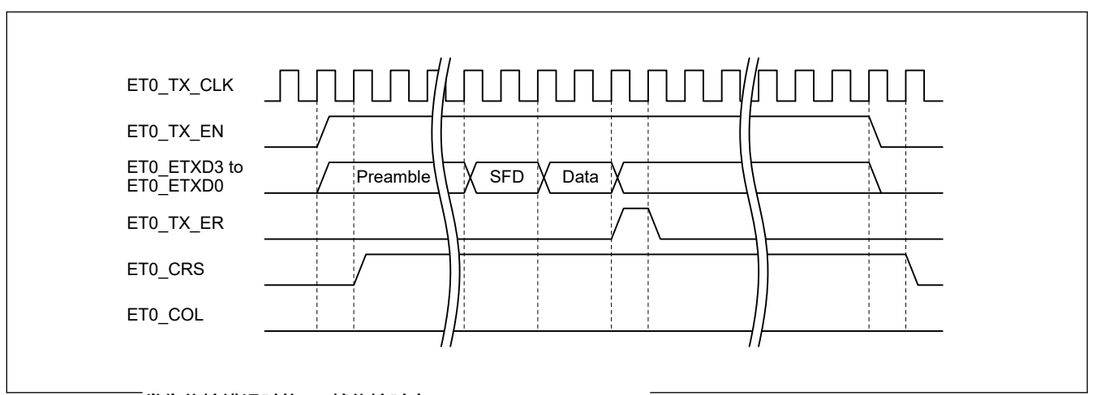


Figure 26.8 发生传输错误时的MII帧传输时序

RA生态工作室

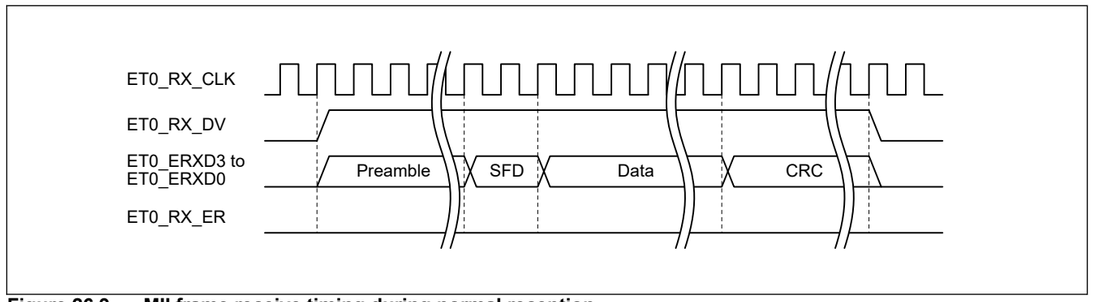


Figure 26.9 MII frame receive timing during normal reception

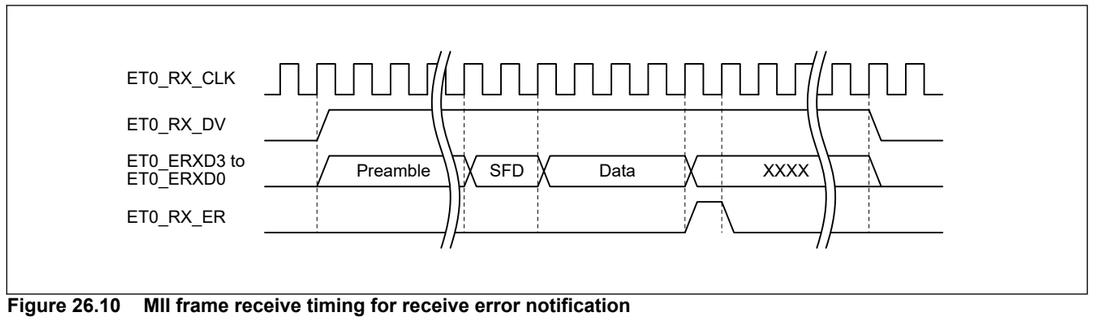


Figure 26.10 MII frame receive timing for receive error notification

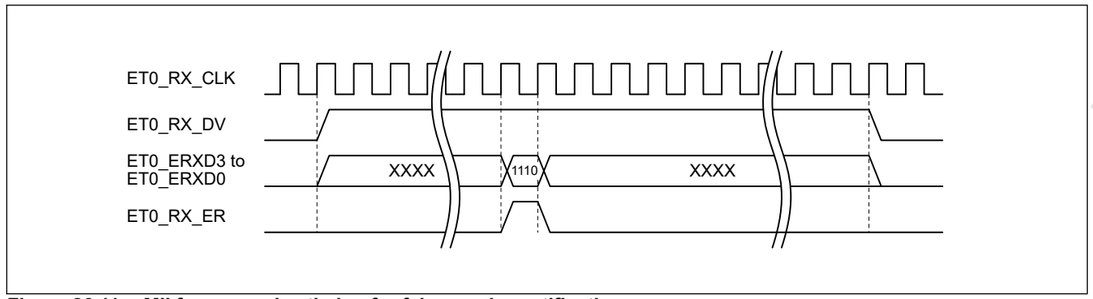


Figure 26.11 MII frame receive timing for false carrier notification

26.3.3.2 RMII frame timing

Figure 26.12 to Figure 26.14 show the RMII frame timing.

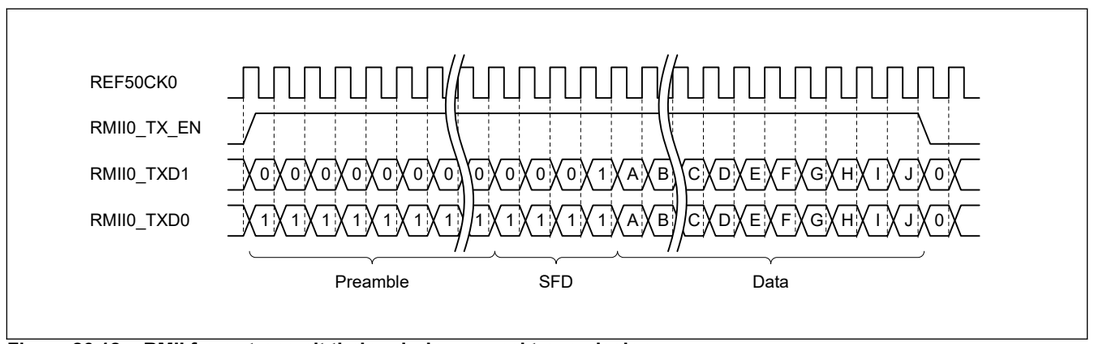


Figure 26.12 RMII frame transmit timing during normal transmission

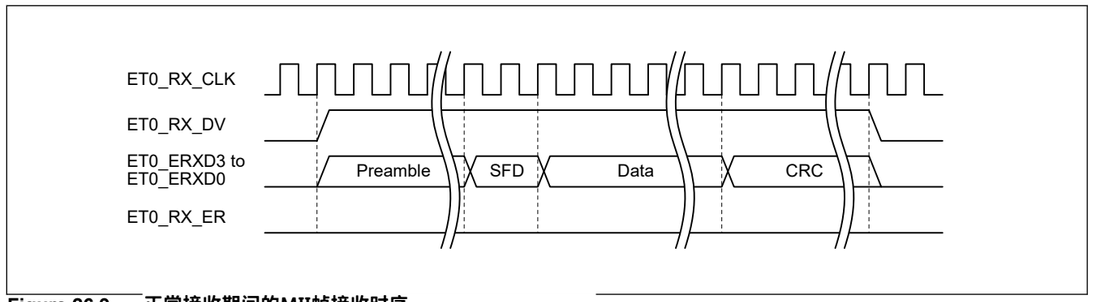


Figure 26.9 正常接收期间的MII帧接收时序

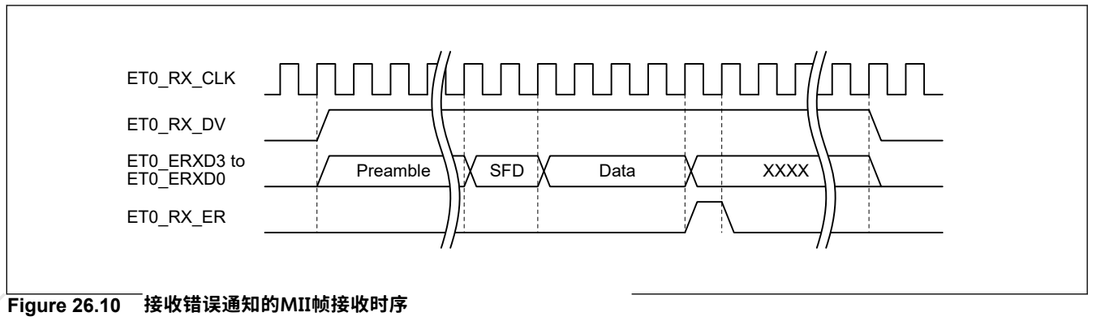


Figure 26.10 接收错误通知的MII帧接收时序

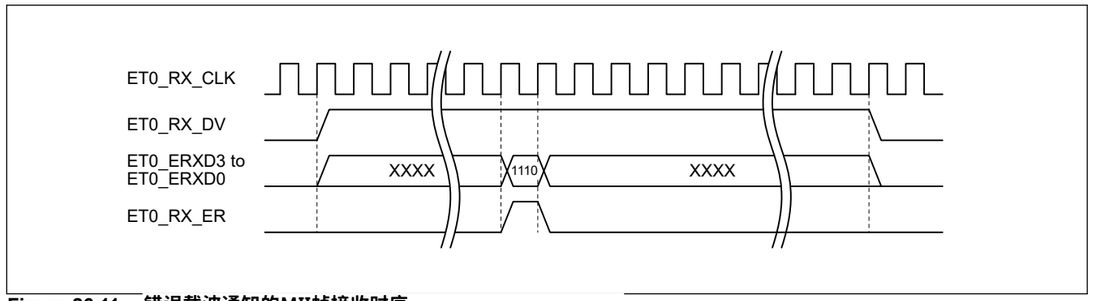


Figure 26.11 错误载波通知的MII帧接收时序

26.3.3.2 RMII帧时序

图26.12至图26.14显示了RMII帧时序。

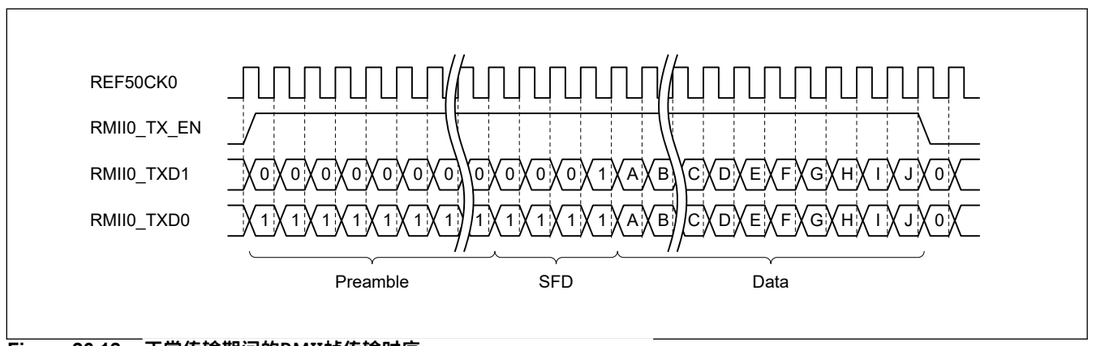


Figure 26.12 正常传输期间的RMII帧传输时序

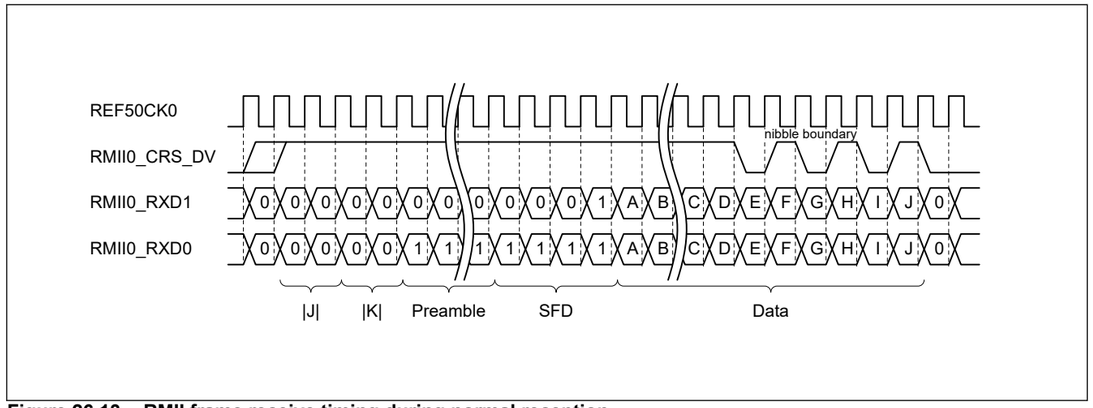


Figure 26.13 RMII frame receive timing during normal reception

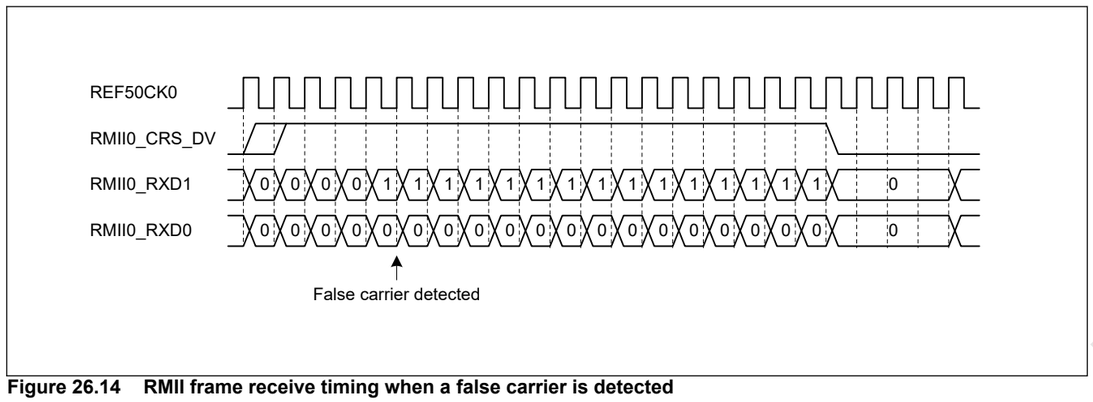


Figure 26.14 RMII frame receive timing when a false carrier is detected

26.3.4 Accessing the MII and RMII Registers

Use the PIR register to access the MII and RMII registers in the PHY-LSI. Serial data in the MII and RMII management frame format is transmitted and received through the ET0_MDC and ET0_MDIO pins controlled by software.

26.3.4.1 MII and RMII management frame format

Table 26.3 lists the MII and RMII management frame formats.

Table 26.3 MII and RMII management frame formats

Access type	MII and RMII management frame							
Parameter	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Number of bits	32	2	2	5	5	2	16	1
Read	1…1	01	10	00001	RRRRR	Z0	DDDDDDDD DDDDDDDD	Z
Write	1…1	01	01	00001	RRRRR	10	DDDDDDDD DDDDDDDD	Z

Note: PRE (preamble): Send 32 consecutive 1s.
ST (start of frame): Send 01b.
OP (operation code): Send 10b for read or 01b for write.
PHYAD (PHY address): Up to 32 PHY-LSIs can be connected to one MAC. PHY-LSIs are selected with these 5 bits. When the PHY-LSI address is 1, send 0x01.

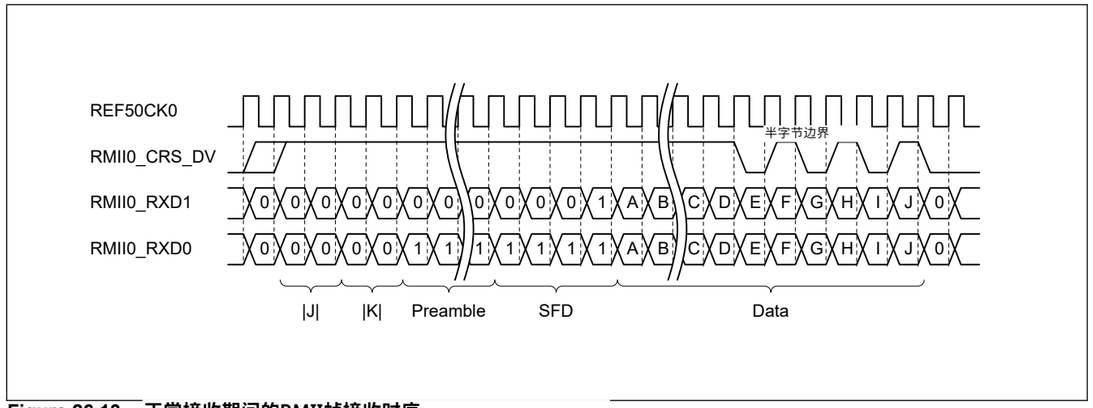


Figure 26.13 正常接收期间的RMII帧接收时序

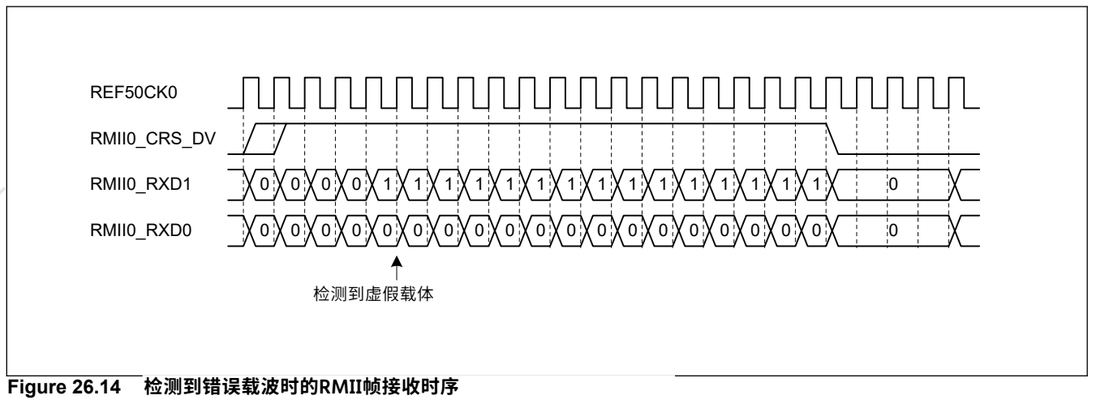


Figure 26.14 检测到错误载波时的RMII帧接收时序

26.3.4 访问MII和RMII寄存器

使用PIR寄存器访问PHY-LSI中的MII和RMII寄存器。MII和RMII管理帧格式的串行数据通过软件控制的ET0_MDC和ET0_MDIO引脚发送和接收。

26.3.4.1 MII和RMII管理帧格式

表26.3列出了MII和RMII管理帧格式。

Table 26.3 MII和RMII管理帧格式

访问类型	MII和RMII管理框架							
Parameter	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
位数	32	2	2	5	5	2	16	1
Read	1…1	01	10	00001	RRRRR	Z0	DDDDDDDD DDDDDDDD	Z
Write	1…1	01	01	00001	RRRRR	10	DDDDDDDD DDDDDDDD	Z

Note: PRE（前导码）：发送32个连续的1。
ST（帧开始）：发送01b。
OP（操作码）：发送10b读或01b写。
PHYAD（PHY地址）：一个MAC最多可以连接32个PHY-LSI。使用这5位选择PHY-LSI。当PHY LSI地址为1，发送0x01。

REGAD (register address): One register is selected from up to 32 registers in the PHY-LSI. When the register address is 1, send 0x01.
TA (turnaround): Use 2-bit turnaround time to avoid contention between the register address and data during a read operation. Send 10b during a write operation. Release the bus for 1 bit during a read operation (Z is output).
(This is indicated as Z0 because 0 is output from the PHY-LSI on the next clock cycle.)
DATA (data): 16-bit data. Sequentially send or receive starting from the MSB.
IDLE (IDLE condition): Wait time before inputting the next MII or RMII management format. Release the bus during a write operation (Z is output). No control is required, because a bus was already released during a read operation.

26.3.4.2 MII and RMII register access procedure

Access to the MII and RMII registers includes writing data in 1-bit units, reading data in 1-bit units, and releasing the bus. Figure 26.15 to Figure 26.18 show examples of the MII and RMII register access timing. The access timing differs with the PHY-LSI type.

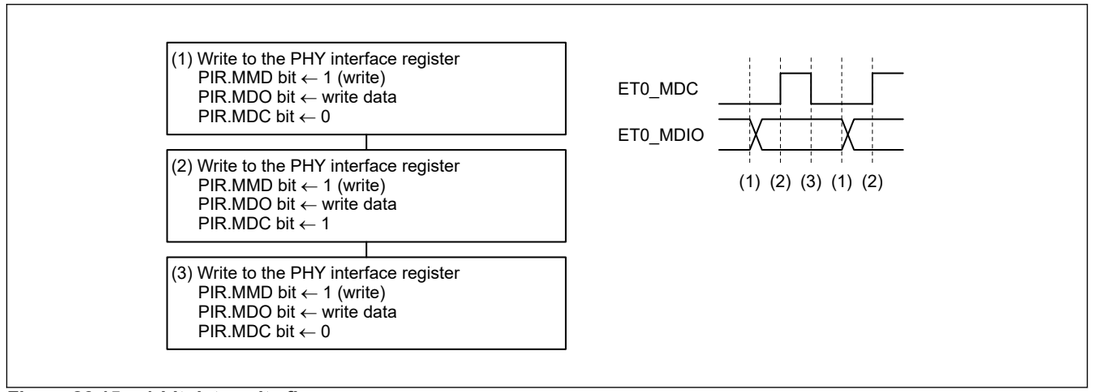


Figure 26.15 1-bit data write flow

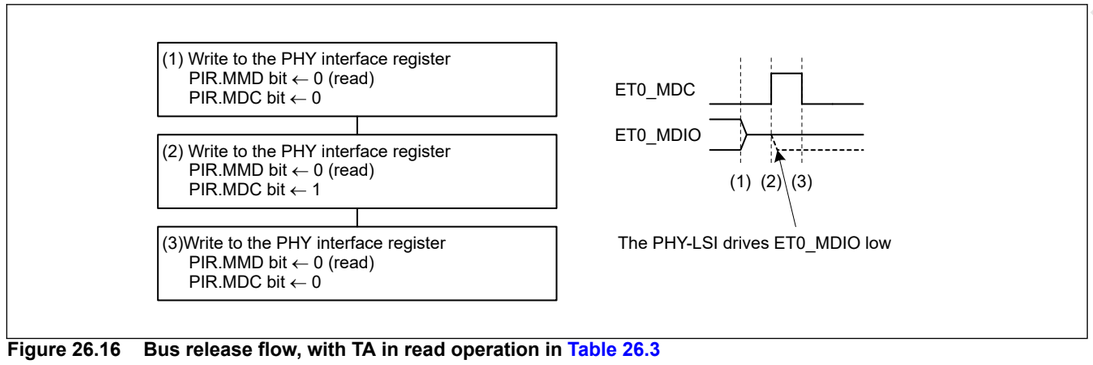


Figure 26.16 Bus release flow, with TA in read operation in Table 26.3

REGAD（寄存器地址）：从PHY-LSI的最多32个寄存器中选择一个寄存器。当寄存器地址为1时，发送0x01。TA（周转）：使用2位周转时间来避免读取操作期间寄存器地址和数据之间的争用。在写操作期间发送10b。在读操作期间释放总线1位（Z为输出）。（这表示为Z0，因为在下一个时钟周期从PHY-LSI输出0。）DATA（数据）：16位数据。从MSB开始顺序发送或接收。

IDLE（IDLE条件）：输入下一个MII或RMII管理格式前的等待时间。在写操作期间释放总线（Z为输出）。不需要控制，因为在读取操作期间总线已被释放。

26.3.4.2 MII和RMII寄存器访问过程

对MII和RMII寄存器的访问包括以1位为单位写入数据、以1位为单位读取数据以及释放总线。
图26.15至图26.18显示了MII和RMII寄存器访问时序的示例。访问时间不同
PHY-LSI type.

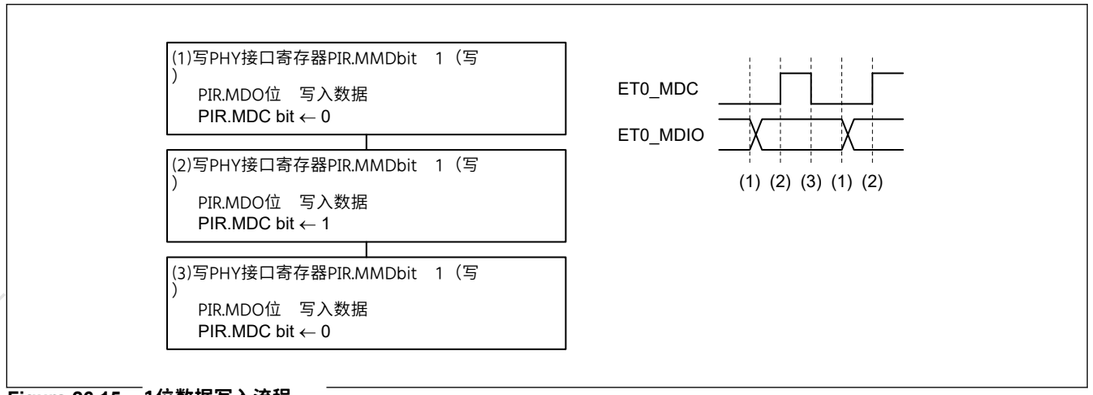


Figure 26.15 1位数据写入流程

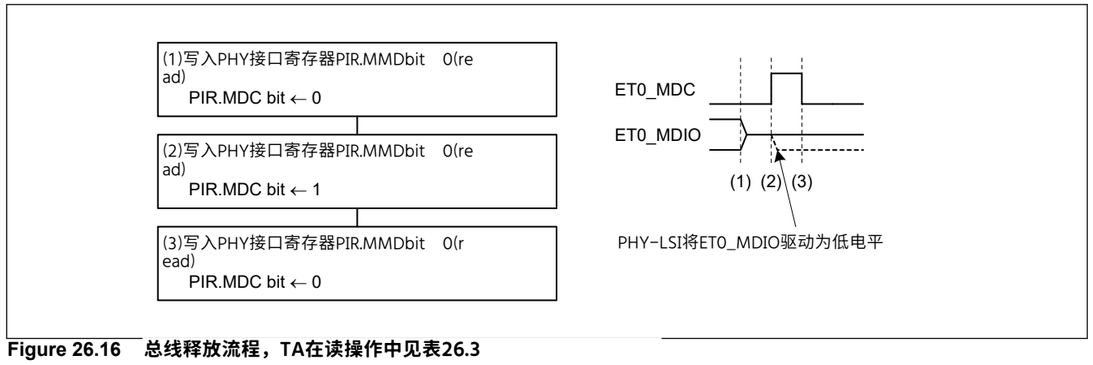


Figure 26.16 总线释放流程，TA在读操作中见表26.3

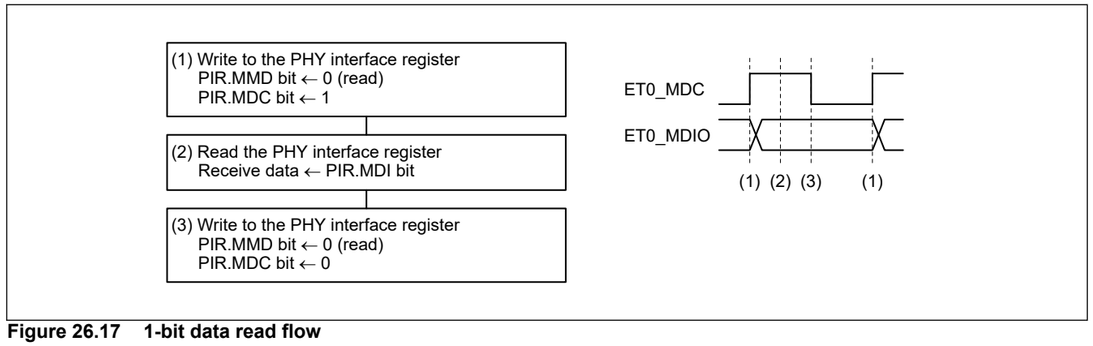


Figure 26.17 1-bit data read flow

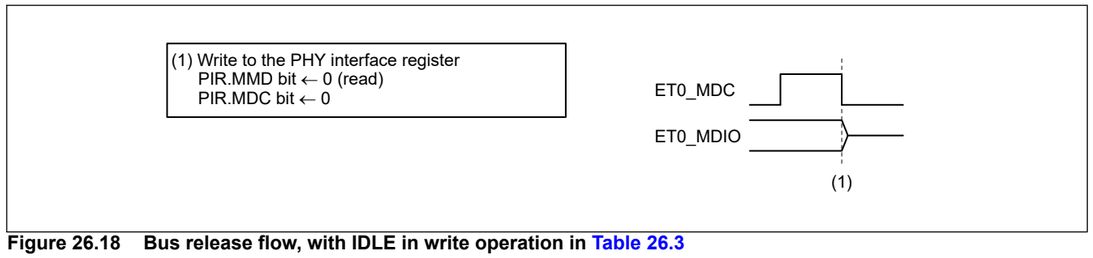


Figure 26.18 Bus release flow, with IDLE in write operation in Table 26.3

26.3.5 Magic Packet Detection

The ETHERC supports Wake-on-LAN (WOL). WOL is a function to detect a Magic Packet transmitted from a host device or other device, and to wake the MCU from a low power mode such as Sleep. When the ETHERC detects a Magic Packet, it outputs high on the ET0_WOL pin. Write 1 to the EDMAC0.EDMR.SWR bit to drive the ET0_WOL pin low.

Because a Magic Packet is transmitted in broadcast mode, it is received regardless of the destination MAC address selected in the format. The ETHERC outputs high on the ET0_WOL pin only when the destination MAC address matches its own MAC address. See the technical documentation provided by Advanced Micro Devices, Inc., for details on the Magic Packet.

To use WOL in the MCU, use the procedure in the following example:

1. Configure the ICU to disable ETHER_EINT0 interrupt requests.
2. Set the ECMR.MPDE bit to 1 to enable Magic Packet detection, and set the ECMR.RE bit to 1 to enable reception.
3. Set the ECSIPR.MPDIP bit to 1 to enable notification of Magic Packet detection interrupts.
4. Set the EDMAC0.EESIPR.ECIIP bit to 1 to enable ETHERC status register source interrupts.
5. Configure the ICU to enable ETHER_EINT0 interrupt requests.
6. Change the CPU operating mode to Sleep mode or place unused peripherals in the module-stop state, as required.
7. When a Magic Packet is detected, an interrupt request is sent to the CPU. High is output on the ET0_WOL pin to notify peripheral devices that the Magic Packet was detected.

26.3.5.1 Constraints on Magic Packet detection

The ETHERC receives packets, including broadcast packets, even when waiting to receive a Magic Packet. This means that receive data might already be stored in the receive FIFO of the EDMAC when a Magic Packet is detected. Also, flags in the ECSR and EDMAC0.EESR registers might have changed. When returning to normal operation after detecting a Magic Packet, set the EDMAC0.EDMR.SWR bit to 1 to reset the ETHERC and EDMAC.

26.3.6 Adjusting Transmission Efficiency by Changing the IPG

The IPG is a non-transmit period between transmit frames. The ETHERC can change the value of the IPG to increase or decrease transmission efficiency based on the value set in the IPGR register. Typical values are specified in the IEEE802.3 standard. When changing the setting, confirm that all devices in the same network operate normally.

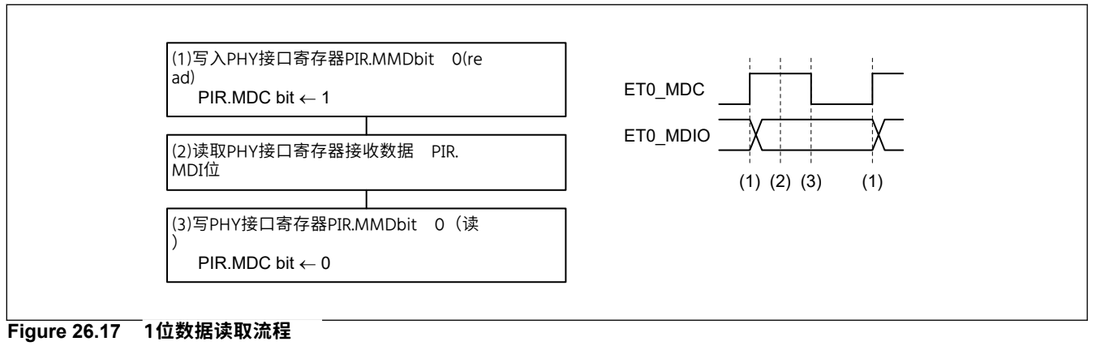


Figure 26.17 1位数据读取流程

Figure 26.18 总线释放流程，IDLE写操作见表26.3

26.3.5 魔术包检测

ETHERC支持网络唤醒(WOL)。WOL是一种检测从主机设备或其他设备发送的魔术包，并将MCU从低功耗模式（例如睡眠）唤醒的功能。当ETHERC检测到一个魔术包时，它在ET0_WOL引脚上输出高电平。将1写入EDMAC0.EDMR.SWR位以将ET0_WOL引脚驱动为低电平。

因为MagicPacket以广播模式传输，所以无论格式中选择的目标MAC地址如何，都会接收到它。仅当目标MAC地址与其自己的MAC地址匹配时，ETHERC才会在ET0_WOL引脚上输出高电平。有关MagicPacket的详细信息，请参阅AdvancedMicroDevices Inc.提供的技术文档。

要在MCU中使用WOL，请使用以下示例中的过程：

1.将ICU配置为禁用ETHER_EINT0中断请求。

2.将ECMR.MPDE位设置为1以启用魔术包检测，并将ECMR.RE位设置为1以启用接收。

3.将ECSIPR.MPDIP位设置为1以启用魔术包检测中断通知。

4.将EDMAC0.EESIPR.ECIIP位设置为1以启用ETHERC状态寄存器源中断。

5.配置ICU以启用ETHER_EINT0中断请求。

6.根据需要将CPU工作模式更改为休眠模式或将未使用的外设置于模块停止状态。

7.当检测到MagicPacket时，向CPU发送中断请求。ET0_WOL引脚上输出高电平以通知外围设备检测到魔术包。

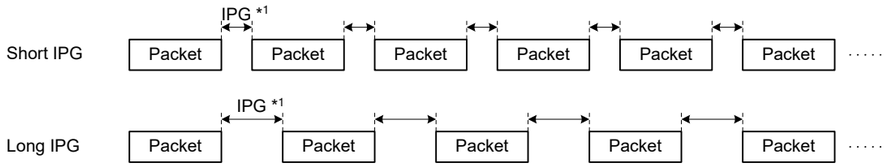
26.3.5.1 魔术包检测的约束

ETHERC接收数据包，包括广播数据包，即使在等待接收魔术数据包时也是如此。这意味着当检测到魔术包时，接收数据可能已经存储在EDMAC的接收FIFO中。此外，ECSR和EDMAC0.EESR寄存器中的标志可能已更改。检测到魔法后恢复正常运行时

数据包，将EDMAC0.EDMR.SWR位设置为1以复位ETHERC和EDMAC。

26.3.6 改变IPG调整传输效率

IPG是传输帧之间的非传输周期。ETHERC可以根据IPGR寄存器中设置的值改变IPG的值来提高或降低传输效率。典型值在IEEE802.3标准中指定。更改设置时，请确认同一网络中的所有设备都正常运行。



Note 1. The IPG may be longer than the set value depending on the condition of the line or system bus.

Figure 26.19 Differences in transmission efficiency based on changes in the IPG

26.3.7 Flow Control

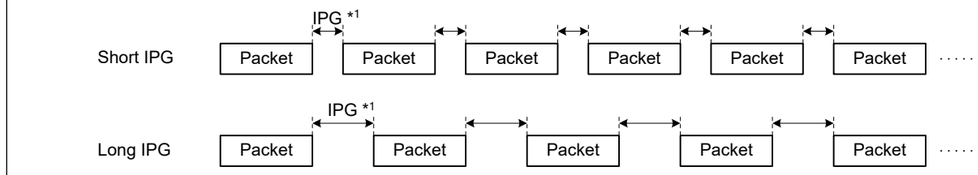
The ETHERC can perform flow control compliant with IEEE802.3x in full-duplex mode, and the receiver and transmitter can be set independently. PAUSE frames can be transmitted automatically or manually.

26.3.7.1 Automatic PAUSE frame transmission

When the ECMR.TXF bit is set to 1, automatic PAUSE frame transmission is enabled. A PAUSE frame is automatically transmitted by a PAUSE frame transmit request from the EDMAC. The APR.AP[15:0] bit value is used for the pause_time parameter of the PAUSE frame.

When a PAUSE frame is transmitted, if the EDMAC is still requesting PAUSE frame transmission after the PAUSE time elapses, a PAUSE frame is transmitted again. The maximum number of PAUSE frame retransmissions can be set in the TPAUSER.TPAUSE[15:0] bits. If the maximum number of retransmissions is reached, subsequent PAUSE frames are not transmitted.

Figure 26.20 shows the procedure for setting up automatic PAUSE frame transmission.



Note 1. 根据线路或系统总线的情况，IPG可能会比设定值长。

Figure 26.19 基于IPG变化的传输效率差异

26.3.7 流量控制

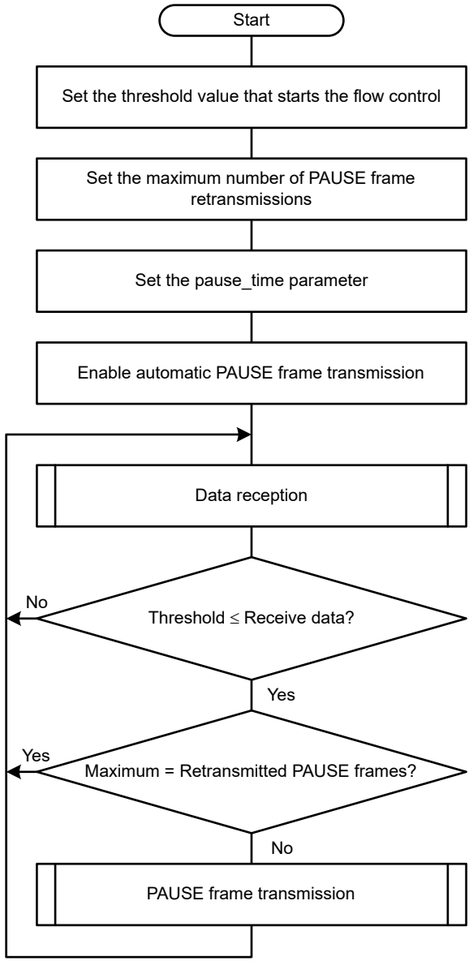
ETHERC可以在全双工模式下进行符合IEEE802.3x的流量控制，接收端和发送端可以独立设置。PAUSE帧可以自动或手动传输。

26.3.7.1 自动暂停帧传输

当ECMR.TXF位设置为1时，启用自动暂停帧传输。PAUSE帧由来自EDMAC的PAUSE帧发送请求自动发送。APR.AP[15:0]位值用于PAUSE帧的pause_time参数。

当发送暂停帧时，如果在暂停时间过去后EDMAC仍在请求暂停帧发送，则再次发送暂停帧。PAUSE帧重传的最大次数可以在TPAUSER.TPAUSE[15:0]位中设置。如果达到最大重传次数，则不传输后续PAUSE帧。

图26.20显示了设置自动暂停帧传输的过程。

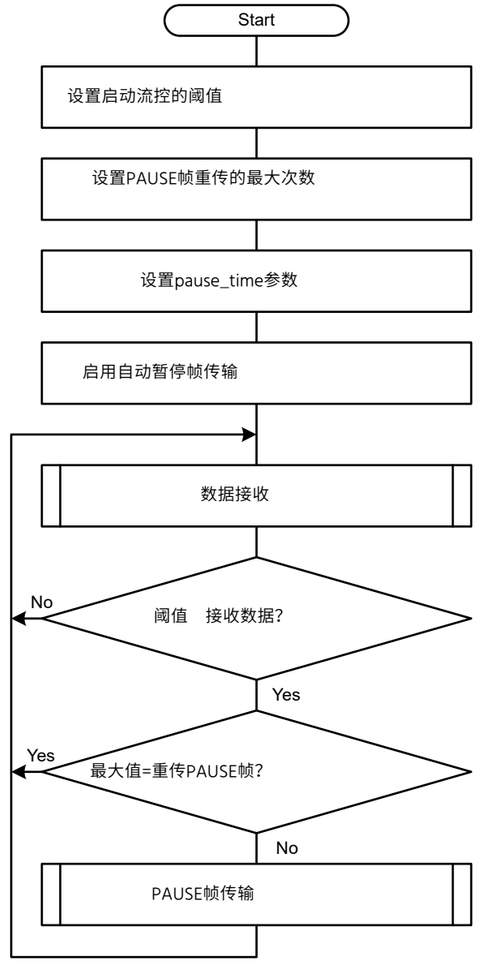


1. Set the threshold value in the EDMAC0.FCFTR.RFDO[2:0] bits or EDMAC0.FCFTR.RFFO[2:0] bits.
2. Set the maximum number of automatic PAUSE frame retransmissions in the TPAUSER.TPAUSE[15:0] bits.
3. Set the pause_time parameter of the automatic PAUSE frame in the APR.AP[15:0] bits.
4. Set the ECMR.TXF bit to 1.
5. Set the ECMR.RE bit to 1.
6. Check whether the amount of receive FIFO data or the number of received frames reached the threshold.
7. Check whether the number of automatic PAUSE frame retransmissions reached the threshold.

Figure 26.20 Example procedure for setting up automatic PAUSE frame transmission

26.3.7.2 Manual PAUSE frame transmission

A PAUSE frame can be manually transmitted at any time. When the software writes the pause_time parameter of the PAUSE frame to the MPR.MP[15:0] bits, the ETHERC transmits a PAUSE frame once. To transmit a PAUSE frame more than once, write to the MPR.MP[15:0] bits for each transmission.



1.在EDMAC0.FCFTR.RFDO[2:0]位或EDMAC0.FCFTR.RFFO[2:0]位中设置阈值。2.在TPAUSER.TPAUSE[15:0]位中设置自动暂停帧重传的最大次数。3.在APR.AP[15:0]位中设置自动PAUSE帧的pause_time参数。4.将ECMR.TXF位设置为1。5.将ECMR.RE位设置为1。6.检查接收FIFO数据量或接收帧数是否达到阈值。7.检查自动暂停帧重传次数是否达到阈值。

Figure 26.20 设置自动暂停帧传输的示例过程

26.3.7.2 手动暂停帧传输

PAUSE帧可以随时手动发送。当软件写入的pause_time参数
PAUSE帧到MPR.MP[15:0]位，ETHERC发送一个PAUSE帧一次。要多次传输PAUSE帧，请在每次传输时写入MPR.MP[15:0]位。

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26.3.7.3 PAUSE frame reception

When the ECMR.RXF bit is set to 1, PAUSE frame detection is enabled. After a PAUSE frame is received, the ETHERC completes transmission of the current frame and waits for the PAUSE time of the received PAUSE frame to elapse before it can transmit the next frame. The ETHERC also increments the RFCF.RPAUSE[7:0] bit value.

However, while waiting for the PAUSE time to elapse, if a PAUSE frame that contains a pause_time parameter of 0 is received and the ECMR.ZPF bit is 1, the ETHERC becomes ready to transmit immediately.

26.4 Interrupts

When a flag in the ECSR register sets to 1 and the associated bit in the ECSIPR register is 1, the ETHERC notifies the EDMAC of the interrupt source status. After receiving the notification, the EDMAC sets the EDMAC0.EESR.ECI flag to 1. When the EDMAC0.EESIPR.ECIIP bit is 1, the EDMAC sends an ETHER_EINT0 interrupt request to the CPU.

For details, see section 27, Ethernet DMA Controller (EDMAC).

26.5 Usage Notes

26.5.1 Preventing the LCHNG Flag from Erroneously Setting to 1

The ECSR.LCHNG flag might set to 1 even when the input level of the ET0_LINKSTA pin remains the same. In this case, high level is input to the ET0_LINKSTA pin when setting the PFS.PmnPFS register to assign the ET0_LINKSTA signal to a port, or when releasing the ETHERC and EDMAC software reset using the EDMAC0.EDMR.SWR bit. The ECSR.LCHNG flag is sets to 1 because the ET0_LINKSTA signal in the ETHERC is fixed low level regardless of the input level to the external pin if the MPC does not assign the ET0_LINKSTA signal or during an ETHERC and EDMAC software reset.

To avoid erroneously generating a link signal change interrupt, clear the ECSR.LCHNG flag, and then set the ECSIPR.LCHNGIP bit to 1.

26.5.2 Input to RMII0_RX_ER Pin While RMII Is Selected

When the width of a reception error signal received from the PHY-LSI is only 1 cycle of the REF50CK0 clock (50 MHz) while the RMII is selected, the signal is not recognized as an error signal.

26.5.3 Collision Occurrence in Half-Duplex Mode

Transmission might start and communication might collide within 21 clock cycles (50 MHz) from reception in halfduplex mode.

26.3.7.3 暂停帧接收

当ECMR.RXF位设置为1时，启用PAUSE帧检测。接收到PAUSE帧后，ETHERC完成当前帧的传输，并等待接收到的PAUSE帧的PAUSE时间过去，然后才能传输下一帧。ETHERC还会增加RFCF.RPAUSE[7:0]位的值。

然而，在等待PAUSE时间过去时，如果接收到包含pause_time参数为0的PAUSE帧并且ECMR.ZPF位为1，则ETHERC立即准备好发送。

26.4 Interrupts

当ECSR寄存器中的标志设置为1并且ECSIPR寄存器中的相关位为1时，ETHERC通知中断源状态的EDMAC。收到通知后，EDMAC将EDMAC0.EESR.ECI标志设置为1。
当EDMAC0.EESIPR.ECIIP位为1时，EDMAC向CPU发送一个ETHER_EINT0中断请求。

有关详细信息，请参阅第27节，以太网DMA控制器(EDMAC)。

26.5 使用说明

26.5.1 防止LCHNG标志错误设置为1

即使ET0_LINKSTA引脚的输入电平保持不变，ECSR.LCHNG标志也可能设置为1。在这种情况下，当设置PFS.PmnPFS寄存器以将ET0_LINKSTA信号分配给端口时，或使用EDMAC0.EDMR.SWR位释放ETHERC和EDMAC软件复位时，高电平输入到ET0_LINKSTA引脚。ECSR.LCHNG标志设置为1，因为如果MPC未分配ET0_LINKSTA信号或在ETHERC和EDMAC软件复位期间，无论外部引脚的输入电平如何，ETHERC中的ET0_LINKSTA信号都是固定的低电平。

为避免错误地生成链接信号更改中断，请清除ECSR.LCHNG标志，然后设置ECSIPR.LCHNGIP位为1。

26.5.2 选择RMII时输入到RMII0_RX_ER引脚

选择RMII时，如果从PHY-LSI接收到的接收错误信号的宽度仅为REF50CK0时钟(50MHz)的1个周期，则该信号不会被识别为错误信号。

26.5.3 半双工模式下的冲突发生

在半双工模式下，从接收开始的21个时钟周期(50MHz)内，传输可能会开始并且通信可能会发生冲突。

27. Ethernet DMA Controller (EDMAC)

27.1 Overview

The MCU provides one channel for the Ethernet DMA Controller (EDMAC) for the Ethernet Controller (ETHERC) .

The EDMAC controls most of the transmit and receive buffer management for communications. This reduces the load on the CPU and allows efficient data transmission and reception. The data transfers are controlled according to the information referred to as descriptors, in memory. EDMAC0 controls data transmission and reception for ETHERC0.

Table 27.1 lists the EDMAC specifications and Figure 27.1 shows the configuration. Figure 27.2 shows the configuration of descriptors and the transmit and receive buffers in memory.

Table 27.1 EDMAC specifications

Parameter	Specifications
Data transmission and reception	• Controls data transmission and reception according to descriptors • Supports single buffer frame transmission and reception (1 buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)
Functions	• Minimizes system bus occupancy time using block transfer (32-byte units) • Writes back the transmit or receive frame state to descriptors • Inserts padding in receive data
Module-stop function	Module-stop state can be set to reduce power consumption

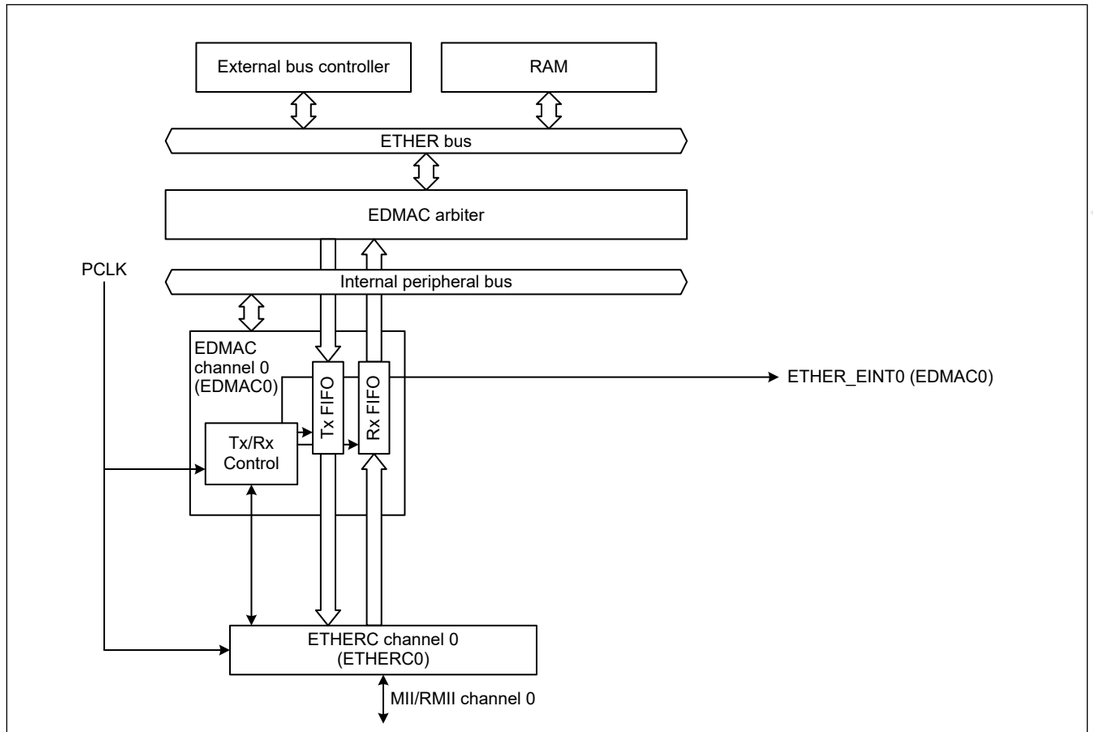


Figure 27.1 EDMAC configuration

27. 以太网DMA控制器(EDMAC)

27.1 Overview

MCU为以太网控制器(ETHERC)的以太网DMA控制器(EDMAC)提供一个通道。

EDMAC控制大部分用于通信的发送和接收缓冲区管理。这减少了CPU的负载并允许高效的数据传输和接收。数据传输是根据内存中称为描述符的信息进行控制的。EDMAC0控制ETHERC0的数据传输和接收。

表27.1列出了EDMAC规范，图27.1显示了配置。图27.2显示了描述符的配置以及内存中的发送和接收缓冲区。

Table 27.1 EDMAC specifications

Parameter	Specifications
数据传输和接收	• 根据描述符控制数据的发送和接收 • 支持单缓冲帧发送和接收（每帧1个缓冲区）和多缓冲区帧发送和接收（每帧多个缓冲区）
Functions	• 使用块传输（32字节单位）最小化系统总线占用时间 • 将发送或接收帧状态写回描述符 • 在接收数据中插入填充
Module-stop function	可设置模块停止状态以降低功耗

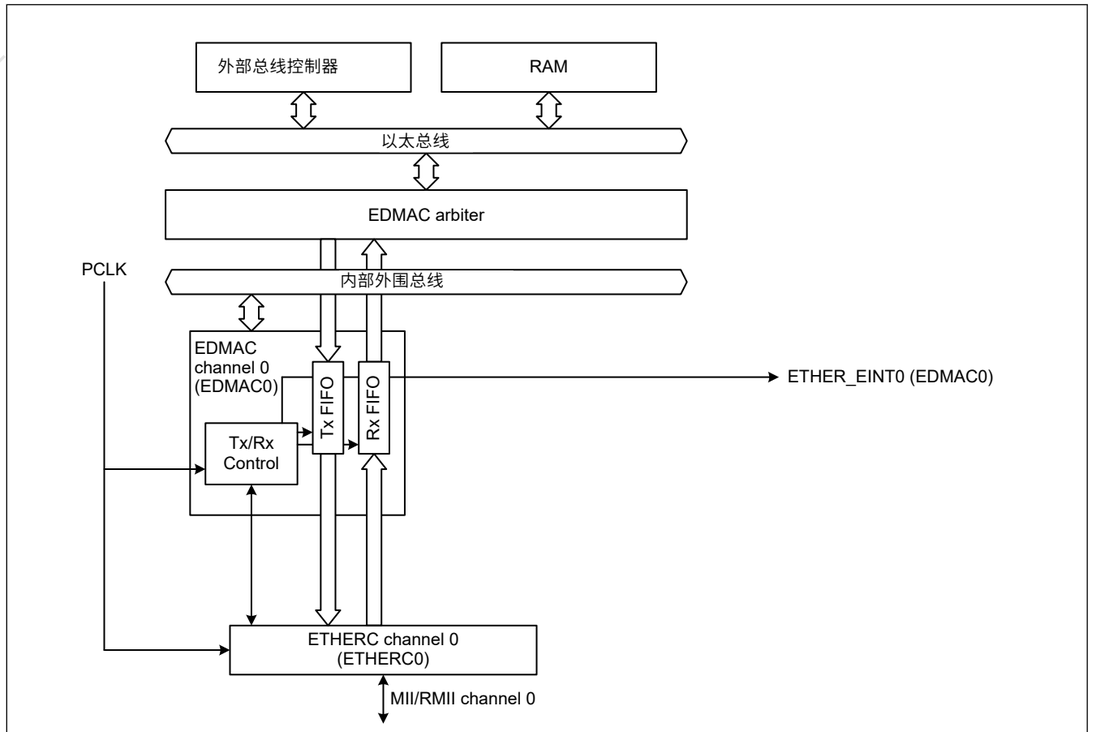


Figure 27.1 EDMAC configuration

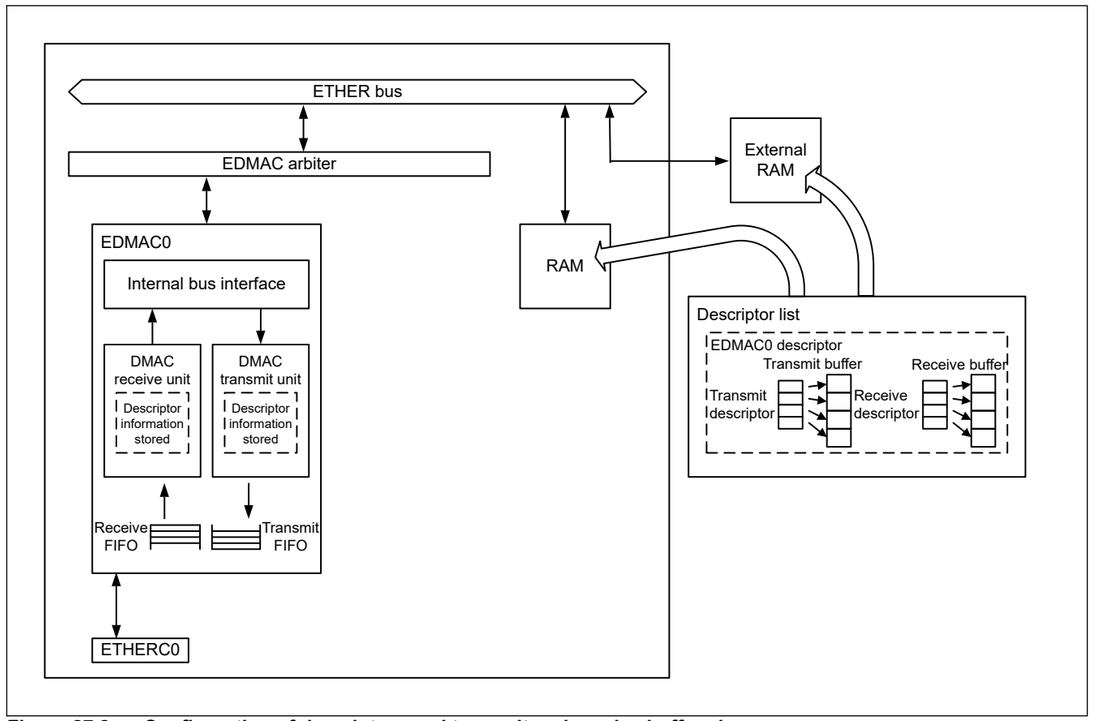


Figure 27.2 Configuration of descriptors and transmit and receive buffers in memory

27.2 Register Descriptions

27.2.1 EDMR : EDMAC Mode Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	DE	DL[1:0]		—	—	—	SWR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWR	Software Reset When 1 is written, the associated channels of the EDMAC and ETHERC are reset. The TDLAR, RDLAR, RMFCR, TFUCR, and RFOCR registers are not reset with this bit.The read value is 0.	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
5:4	DL[1:0]	Transmit/Receive Descriptor Length 0 0: 16 bytes 0 1: 32 bytes 1 0: 64 bytes 1 1: 16 bytes.	R/W

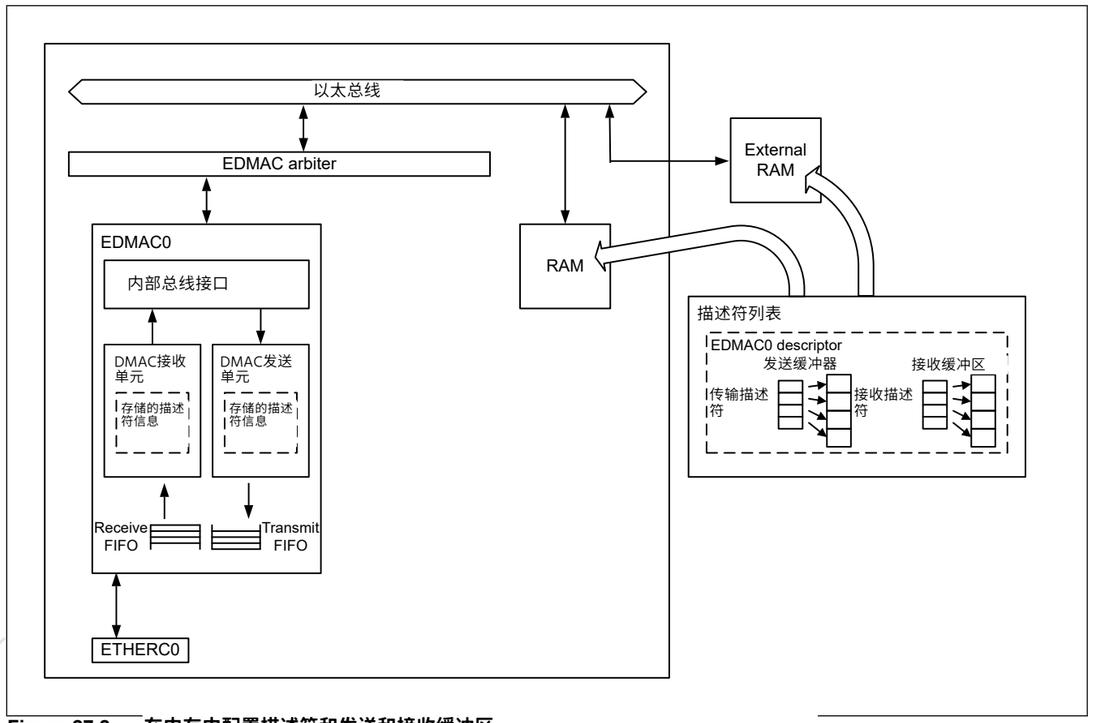


Figure 27.2 在内存中配置描述符和发送和接收缓冲区

27.2 注册说明

27.2.1 EDMR:EDMAC模式寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	DE	DL[1:0]		—	—	—	SWR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SWR	软件复位 当写入1时，EDMAC和ETHERC的相关通道被复位。 TDLAR、RDLAR、RMFCR、TFUCR和RFOCR寄存器不会用该位复位。读取值为0。	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
5:4	DL[1:0]	发送接收描述符长度 0 0: 16 bytes 0 1: 32 bytes 1 0: 64 bytes 1 1: 16 bytes.	R/W

Bit	Symbol	Function	R/W
6	DE	Big Endian Mode/Little Endian Mode*1 0: Big endian mode 1: Little endian mode.	R/W
31:7	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This setting applies to data for the transmit and receive buffers. It does not apply to transmit and receive descriptors and registers.

The EDMR register controls EDMAC operation. Set the EDMR register during initialization process after a reset. When rewriting this register outside of the initialization process, set the SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again. If the ETHERC and EDMAC are reset during data transmission or reception, abnormal data might be sent on the line. Do not rewrite this register while the ETHERC transmit or receive function is enabled. It takes 64 cycles of the peripheral module clock (PCLKA) to initialize the ETHERC and EDMAC. Complete the initialization before accessing registers in the ETHERC and EDMAC.

27.2.2 EDTRR : EDMAC Transmit Request Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x08

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TR	Transmit Request When 1 is written, the EDMAC reads the associated descriptor and transmits frames where the TD0.TACT bit is 1. The TR bit clears to 0 after all the valid frames are transmitted. Writing 0 to this bit has no effect.	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The EDTRR register controls EDMAC transmission. After the EDMAC transmits one frame, it reads the next descriptor. When the TD0.TACT bit in the descriptor is 1, the EDMAC continues transmission. When the TD0.TACT bit is 0, the EDMAC sets the TR bit to 0 and stops transmission.

27.2.3 EDRRR : EDMAC Receive Request Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x10

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RR	Receive Request 0: Disable the receive function*1 1: Read receive descriptor and enable the receive function.	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. If the receive function is disabled during frame reception, write-back to the receive descriptor is not performed successfully. Subsequent pointers for reading a receive descriptor become abnormal and the EDMAC cannot operate normally. In this case, to enable the EDMAC receive function again, execute a software reset by setting the EDMR.SWR bit to 1. To disable the EDMAC receive function without resetting the EDMAC, set the ETHERC0.ECMR.RE bit to 0. After the EDMAC completes reception and write-back to the receive descriptor is confirmed, set the RR bit to 0.

The EDRRR register controls EDMAC reception. When the RR bit sets to 1, the EDMAC reads the receive descriptor.

Bit	Symbol	Function	R/W
6	DE	大端模式小端模式*1 0：大端模式1：小端模式。	R/W
31:7	—	这些位被读取为0。写入值应为0。	R/W

注1.此设置适用于发送和接收缓冲区的数据。它不适用于发送和接收描述符和寄存器。

EDMR寄存器控制EDMAC操作。在复位后的初始化过程中设置EDMR寄存器。在初始化过程之外重写该寄存器时，将SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。如果ETHERC和EDMAC在数据传输或接收过程中被复位，可能会在线路上发送异常数据。在启用ETHERC发送或接收功能时不要重写该寄存器。初始化ETHERC和EDMAC需要64个外围模块时钟(PCLKA)周期。在访问ETHERC和EDMAC中的寄存器之前完成初始化。

27.2.2 EDTRR:EDMAC发送请求寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x08

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TR	发送请求 写入1时，EDMAC读取相关描述符并发送TD0.TACT位为1的帧。发送完所有有效帧后，TR位清零。向该位写入0无效。	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

EDTRR寄存器控制EDMAC传输。EDMAC传输一帧后，读取下一个描述符。
当描述符中的TD0.TACT位为1时，EDMAC继续传输。当TD0.TACT位为0时，
EDMAC将TR位设置为0并停止传输。

27.2.3 EDRRR:EDMAC接收请求寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x10

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RR	接收请求 0：关闭接收功能*1 1：读取接收描述符并启用接收功能。	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

注1.如果在帧接收期间禁用接收功能，则无法成功执行对接收描述符的回写。
后续读取接收描述符的指针异常，EDMAC不能正常工作。在这种情况下，要再次启用EDMAC接收功能，通过将EDMR.SWR位设置为1来执行软件复位。要禁用EDMAC接收功能而不重置EDMAC，请将ETHERC0.ECMR.RE位设置为0。EDMAC完成接收并确认回写到接收描述符，将RR位设置为0。

EDRRR寄存器控制EDMAC接收。当RR位设置为1时，EDMAC读取接收描述符。

When the RD0.RACT bit is 1, the EDMAC waits for a receive request from the ETHERC. When the EDMAC has received data for the receive buffer size, it reads the next descriptor and waits to receive a frame. If the RD0.RACT bit is 0, the EDMAC sets the RR bit to 0 and stops reception.

27.2.4 TDLAR : Transmit Descriptor List Start Address Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x18

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	—	These bits specify the start address of the transmit descriptor list. Set the start address according to the descriptor length selected in the EDMR.DL[1:0] bits. ● 16-byte boundary: Lower 4 bits = 0000b ● 32-byte boundary: Lower 5 bits = 00000b ● 64-byte boundary: Lower 6 bits = 000000b.	R/W

The TDLAR register specifies the start address of the transmit descriptor list. Align each descriptor on the associated boundary to the descriptor length selected in the EDMR.DL[1:0] bits. Do not rewrite the TDLAR register during transmission. Rewrite the TDLAR register while the EDTRR.TR bit is 0.

27.2.5 RDLAR : Receive Descriptor List Start Address Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x20

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	—	The start address of the receive descriptor list is set. Set the start address according to the descriptor length selected in the EDMR.DL[1:0] bits. ● 16-byte boundary: Lower 4 bits = 0000b ● 32-byte boundary: Lower 5 bits = 00000b ● 64-byte boundary: Lower 6 bits = 000000b.	R/W

The RDLAR register specifies the start address of the receive descriptor list. Allocate each descriptor on the associated boundary to the descriptor length selected in the EDMR.DL[1:0] bits. Do not rewrite the RDLAR register during reception. Rewrite the RDLAR register while the EDRRR.RR bit is 0.

当RD0.RACT位为1时，EDMAC等待来自ETHERC的接收请求。当EDMAC接收到接收缓冲区大小的数据时，它会读取下一个描述符并等待接收帧。如果RD0.RACT位为0，则EDMAC将RR位设置为0并停止接收。

27.2.4 TDLAR:发送描述符列表起始地址寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x18

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	—	这些位指定发送描述符列表的起始地址。根据在EDMR.DL[1:0]位中选择的描述符长度设置起始地址。● 16字节边界：低4位=0000b ● 32字节边界：低5位=00000b ● 64字节边界：低6位=000000b。	R/W

TDLAR寄存器指定发送描述符列表的起始地址。将相关边界上的每个描述符与在EDMR.DL[1:0]位中选择的描述符长度对齐。发送期间不要重写TDLAR寄存器。在EDTRR.TR位为0时重写TDLAR寄存器。

27.2.5 RDLAR:接收描述符列表起始地址寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x20

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	—	设置接收描述符列表的起始地址。根据在EDMR.DL[1:0]位中选择的描述符长度设置起始地址。● 16字节边界：低4位=0000b ● 32字节边界：低5位=00000b ● 64字节边界：低6位=000000b。	R/W

RDLAR寄存器指定接收描述符列表的起始地址。将相关边界上的每个描述符分配给在EDMR.DL[1:0]位中选择的描述符长度。接收期间不要重写RDLAR寄存器。在EDRRR.RR位为0时重写RDLAR寄存器。

27.2.6 EESR : ETHERC/EDMAC Status Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	TWB	—	—	—	TABT	RABT	RFCOF	ADE	ECI	TC	TDE	TFUF	FR	RDE	RFOF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CND	DLC	CD	TRO	RMAF	—	—	RRF	RTLF	RTSF	PRE	CERF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CERF	CRC Error Flag 0: CRC error not detected 1: CRC error detected.	R/W
1	PRE	PHY-LSI Receive Error Flag 0: PHY-LSI receive error not detected 1: PHY-LSI receive error detected.	R/W
2	RTSF	Frame-Too-Short Error Flag 0: Frame-too-short error not detected 1: Frame-too-short error detected.	R/W
3	RTLF	Frame-Too-Long Error Flag 0: Frame-too-long error not detected 1: Frame-too-long error detected.	R/W
4	RRF	Alignment Error Flag 0: Alignment error not detected 1: Alignment error detected.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	RMAF	Multicast Address Frame Receive Flag 0: Multicast address frame not received 1: Multicast address frame received.	R/W
8	TRO	Transmit Retry Over Flag 0: Transmit retry-over condition not detected 1: Transmit retry-over condition detected.	R/W
9	CD	Late Collision Detect Flag 0: Late collision not detected 1: Late collision detected during frame transmission.	R/W
10	DLC	Loss of Carrier Detect Flag 0: Loss of carrier not detected 1: Loss of carrier detected during frame transmission.	R/W
11	CND	Carrier Not Detect Flag 0: Carrier detected when transmission started 1: Carrier not detected during preamble transmission.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	RFOF	Receive FIFO Overflow Flag 0: No overflow occurred 1: Overflow occurred.	R/W
17	RDE	Receive Descriptor Empty Flag 0: EDMAC detected that the receive descriptor valid bit (RD0.RACT) is 1 1: EDMAC detected that the receive descriptor valid bit (RD0.RACT) is 0.	R/W

27.2.6 EESR：ETHERCEDMAC状态寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x28

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	TWB	—	—	—	TABT	RABT	RFCOF	ADE	ECI	TC	TDE	TFUF	FR	RDE	RFOF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CND	DLC	CD	TRO	RMAF	—	—	RRF	RTLF	RTSF	PRE	CERF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CERF	CRC错误标志 0：未检测到CRC错误1： 检测到CRC错误。	R/W
1	PRE	PHY-LSI接收错误标志 0：未检测到PHY-LSI接收错误1：检测 到PHY-LSI接收错误。	R/W
2	RTSF	帧太短错误标志 0：未检测到帧太短错误1：检测到帧 太短错误。	R/W
3	RTLF	帧过长错误标志 0：未检测到帧过长错误1：检测到帧 过长错误。	R/W
4	RRF	对齐错误标志 0：未检测到对齐错误1：检测 到对齐错误。	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	RMAF	组播地址帧接收标志 0：未收到组播地址帧1：收到组播地址 帧。	R/W
8	TRO	发送重试标志 0：未检测到发送重试条件1：检测到发送重 试条件。	R/W
9	CD	后期碰撞检测标志 0：未检测到后期冲突1：在帧传输期间检测到后期冲 突。	R/W
10	DLC	载波检测标志丢失 0：未检测到载波丢失1：在帧传输过程中检测到载波 丢失。	R/W
11	CND	运营商未检测标志 0：传输开始时检测到载波1：前导传输期间未检测到 载波。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
16	RFOF	接收FIFO溢出标志 0：未发生溢出1：发生 溢出。	R/W
17	RDE	接收描述符空标志 0：EDMAC检测到接收描述符有效位（RD0.RACT）为11：EDMAC检测到 接收描述符有效位（RD0.RACT）为0。	R/W

Bit	Symbol	Function	R/W
18	FR	Frame Receive Flag 0: Frame not received 1: Frame received and update of the receive descriptor is complete.	R/W
19	TFUF	Transmit FIFO Underflow Flag 0: No underflow occurred 1: Underflow occurred.	R/W
20	TDE	Transmit Descriptor Empty Flag 0: EDMAC detected that the transmit descriptor valid bit (TD0.TACT) is 1 1: EDMAC detected that the transmit descriptor valid bit (TD0.TACT) is 0.	R/W
21	TC	Frame Transfer Complete Flag 0: Transfer not complete or no transfer requested 1: All frames indicated in the transmit descriptor were completely transferred to the transmit FIFO.	R/W
22	ECI	ETHERC Status Register Source Flag 0: ETHERC status interrupt source not detected 1: ETHERC status interrupt source detected.	R*1
23	ADE	Address Error Flag 0: Invalid memory address not detected (normal operation) 1: Invalid memory address detected.*2	R/W
24	RFCOF	Receive Frame Counter Overflow Flag 0: Receive frame counter did not overflow 1: Receive frame counter overflowed.	R/W
25	RABT	Receive Abort Detect Flag 0: Frame reception not aborted or no reception requested 1: Frame reception aborted.	R/W
26	TABT	Transmit Abort Detect Flag 0: Frame transmission not aborted or no transmission requested. 1: Frame transmission aborted.	R/W
29:27	—	These bits are read as 0. The write value should be 0.	R/W
30	TWB	Write-Back Complete Flag 0: Write-back not complete or no transmission requested 1: Write-back to the transmit descriptor completed.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. The ECI flag is read-only. When the source in the ECSR register is cleared, the ECI flag is also cleared.
Note 2. When an address error is detected, the EDMAC halts the process. To resume operation, set the EDMR.SWR bit to 1 (resetting the EDMAC and ETHERC), and then reconfigure the EDMAC and ETHERC.

The EESR register indicates the ETHERC and EDMAC communication status. Each flag in the EESR register can be output as an interrupt request signal (ETHER_EINT0) from the EDMAC. Writing 1 clears all of the flags except ECI to 0. Writing 0 does not affect any of the flag values. The interrupt sources are enabled by setting the associated bits in the EESIPR register.

CERF flag (CRC Error Flag)

The CERF flag sets to 1 when an error is detected while checking the frame check sequence (FCS) field of the receive frame.

PRE flag (PHY-LSI Receive Error Flag)

The PRE flag indicates that the RX_ER signal output from the PHY-LSI is high.

RTSF flag (Frame-Too-Short Error Flag)

The RTSF flag indicates that a received frame is less than 64 bytes.

RTLF flag (Frame-Too-Long Error Flag)

The RTLF flag indicates that a received frame is greater than the upper limit of the receive frame length set in the ETHERC0.RFLR register. The excess data is discarded.

Bit	Symbol	Function	R/W
18	FR	帧接收标志 0：未接收到帧1：接收到帧并且接收描述符的更新完成。	R/W
19	TFUF	发送FIFO下溢标志 0：未发生下溢1：发生下 溢。	R/W
20	TDE	发送描述符空标志 0：EDMAC检测到发送描述符有效位（TD0.TACT）为11：EDMAC检测到发 送描述符有效位（TD0.TACT）为0。	R/W
21	TC	帧传输完成标志 0：传输未完成或未请求传输1：传输描述符中指示的所有帧都已完全传输到传输FIF O。	R/W
22	ECI	ETHERC状态寄存器源标志 0：未检测到ETHERC状态中断源1：检测到ETHER C状态中断源。	R*1
23	ADE	地址错误标志 0：未检测到无效内存地址（正常操作）1：检测到无效内存 地址。*2	R/W
24	RFCOF	接收帧计数器溢出标志 0：接收帧计数器未溢出1：接收帧计数器 溢出。	R/W
25	RABT	接收中止检测标志 0：未中止帧接收或未请求接收1：中止帧接收。	R/W
26	TABT	发送中止检测标志 0：帧传输未中止或未请求传输。1：帧传输中止。	R/W
29:27	—	这些位被读取为0。写入值应为0。	R/W
30	TWB	回写完成标志 0：回写未完成或未请求传输1：对传输描述符的回写完成 。	R/W
31	—	该位读取为0。写入值应为0。	R/W

注1.ECI标志是只读的。当ECSR寄存器中的源被清零时，ECI标志也被清零。
注2.当检测到地址错误时，EDMAC停止该过程。要恢复操作，请将EDMR.SWR位设置为1（复位
EDMAC和ETHERC），然后重新配置EDMAC和ETHERC。

EESR寄存器指示ETHERC和EDMAC通信状态。EESR寄存器中的每个标志都可以作为中断请求信号（ETHER_EINT0）从EDMAC输出。写入1会将除ECI之外的所有标志清除为0。写入0不会影响任何标志值。通过设置ESIPR寄存器中的相关位来启用中断源。

CERF标志（CRC错误标志）

当在检查接收帧的帧校验序列(FCS)字段时检测到错误时，CERF标志设置为1。

PRE标志（PHY-LSI接收错误标志）

PRE标志表示从PHY-LSI输出的RX_ER信号为高电平。

RTSF标志（帧太短错误标志）

RTSF标志表示接收到的帧小于64字节。

RTLF标志（帧过长错误标志）

RTLF标志表示接收到的帧大于设置的接收帧长度的上限
ETHERC0.RFLR寄存器。多余的数据被丢弃。

RA生态工作室

RRF flag (Alignment Error Flag)

The RRF flag indicates that a frame is not an integral number of octets. The last word that is not an integral number of octets is not transferred.

RMAF flag (Multicast Address Frame Receive Flag)

The RMAF flag indicates that a multicast frame was received.

TRO flag (Transmit Retry Over Flag)

The TRO flag indicates that a collision occurred again during the 15th retry of frame transmission.

CD flag (Late Collision Detect Flag)

The CD flag indicates that a late collision was detected during frame transmission.

DLC flag (Loss of Carrier Detect Flag)

The DLC flag indicates that a loss of carrier was detected during frame transmission.

CND flag (Carrier Not Detect Flag)

The CND flag sets to 1 when a carrier is not detected during preamble transmission.

RFOF flag (Receive FIFO Overflow Flag)

The RFOF flag indicates that the receive FIFO overflowed during frame reception.

RDE flag (Receive Descriptor Empty Flag)

The RDE flag indicates that the read receive descriptor is invalid. When this flag sets to 1, set the RD0.RACT bit in the receive descriptor to 1 and set the EDRRR.RR bit to 1 to resume reception.

FR flag (Frame Receive Flag)

The FR flag indicates that a frame was received and the receive descriptor was updated. The FR flag sets to 1 every time a frame is received.

TFUF flag (Transmit FIFO Underflow Flag)

The TFUF flag indicates that no data remains in the transmit FIFO during frame transmission. Incomplete data is sent to the line.

TDE flag (Transmit Descriptor Empty Flag)

The TDE flag indicates that the TD0.TACT bit of the transmit descriptor is 0 while the previous transmit descriptor indicates that the frame is not complete (TD0.TFP[1:0] bits are 10b or 00b) in multi-buffer frame transmission. As a result, an incomplete frame might be sent.

When this flag sets to 1, perform a software reset and then set the EDTRR.TR bit to 1 to resume transmission. Transmission starts from the address stored in the TDLAR register.

TC flag (Frame Transfer Complete Flag)

The TC flag indicates that all the data specified in the transmit descriptor was transmitted from the ETHERC. This flag is set to 1 when one frame was transmitted in a single-buffer frame transmission or when the last data of a frame is transmitted in multi-buffer frame transmission and the TD0.TACT bit in the next transmit descriptor is 0. After frame transmission is complete, the EDMAC writes the transfer status back to the descriptor.

ECI flag (ETHERC Status Register Source Flag)

The ECI flag is set to 1 when an interrupt request is generated by the ECSR register.

ADE flag (Address Error Flag)

The ADE flag indicates that the memory address that the EDMAC tried to use for transfer is invalid.

RFCOF flag (Receive Frame Counter Overflow Flag)

The RFCOF flag indicates that the next frame reception started while the number of frames stored in the receive FIFO reached the maximum number of frames (16 frames). The received frame is discarded while the RFCOF flag is 1.

RRF标志（对齐错误标志）

RRF标志表明一个帧不是整数个八位字节。不是整数八位字节的最后一个字不被传送。

RMAF标志（多播地址帧接收标志）

RMAF标志指示接收到多播帧。

TRO标志（传输重试结束标志）

TRO标志表示在第15次帧传输重试期间再次发生冲突。

CD标志（后期碰撞检测标志）

CD标志表示在帧传输期间检测到后期冲突。

DLC标志（载波丢失检测标志）

DLC标志表示在帧传输期间检测到载波丢失。

CND标志（载波未检测标志）

当在前导码传输期间未检测到载波时，CND标志设置为1。

RFOF标志（接收FIFO溢出标志）

RFOF标志表示接收FIFO在帧接收期间溢出。

RDE标志（接收描述符空标志）

RDE标志指示读取的接收描述符无效。当该标志设置为1时，将接收描述符中的RD0.RACT位设置为1，并将EDRRR.RR位设置为1以恢复接收。

FR标志（帧接收标志）

FR标志表示接收到一个帧并且接收描述符已更新。每次接收到一帧时，FR标志设置为1。

TFUF flag (Transmit FIFO Underflow Flag)

TFUF标志表示在帧传输期间没有数据保留在传输FIFO中。不完整的数据被发送到线路。

TDE标志（传输描述符空标志）

TDE标志表示发送描述符的TD0.TACT位为0，而前一个发送描述符表示在多缓冲帧传输中该帧未完成（TD0.TFP[1:0]位为10b或00b）。因此，可能会发送不完整的帧。

当该标志设置为1时，执行软件复位，然后将EDTRR.TR位设置为1以恢复传输。传输从存储在TDLAR寄存器中的地址开始。

TC标志（帧传输完成标志）

TC标志表示发送描述符中指定的所有数据都是从ETHERC发送的。当在单缓冲帧传输中传输一帧或在多缓冲帧传输中传输一帧的最后一个数据并且下一个传输描述符中的TD0.TACT位为0时，此标志设置为1。传输完成后，EDMAC将传输状态写回描述符。

ECI标志（ETHERC状态寄存器源标志）

当ECSR寄存器产生中断请求时，ECI标志设置为1。

ADE标志（地址错误标志）

ADE标志表示EDMAC尝试用于传输的内存地址无效。

RFCOF标志（接收帧计数器溢出标志）

RFCOF标志表示在接收FIFO中存储的帧数达到最大帧数（16帧）时开始下一帧接收。当RFCOF标志为1时，接收到的帧被丢弃。

RA生态工作室

RABT flag (Receive Abort Detect Flag)

The RABT flag indicates that the ETHERC aborted frame reception because of a CRC error, PHY-LSI receive error, frame-too-short error, frame-too-long error, or other errors.

TABT flag (Transmit Abort Detect Flag)

The TABT flag indicates that the ETHERC aborted frame transmission because of transmit retry over, loss of carrier, no carrier detection, or other errors.

TWB flag (Write-Back Complete Flag)

The TWB flag indicates the EDMAC completed writing back to the descriptor after frame transmission. This flag is set to 1 after each frame transmission when the TRIMD.TIM bit is 0. It only sets to 1 when the TRIMD.TIS bit is 1.

27.2.7 EESIPR : ETHERC/EDMAC Status Interrupt Enable Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	TWBIP	—	—	—	TABTIP	RABTIP	RFCOFIP	ADEIP	ECIIP	TCIP	TDEIP	TFUFIP	FRIP	RDEIP	RFOFIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CNDIP	DLCIP	CDIP	TROIP	RMAFIP	—	—	RRFIP	RTLFIP	RTSFIP	PREIP	CERFIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CERFIP	CRC Error Interrupt Request Enable 0: Disable CRC error interrupt requests 1: Enable CRC error interrupt requests.	R/W
1	PREIP	PHY-LSI Receive Error Interrupt Request Enable 0: Disable PHY-LSI receive error interrupt requests 1: Enable PHY-LSI receive error interrupt requests.	R/W
2	RTSFIP	Frame-Too-Short Error Interrupt Request Enable 0: Disable frame-too-short error interrupt requests 1: Enable frame-too-short error interrupt requests.	R/W
3	RTLFIP	Frame-Too-Long Error Interrupt Request Enable 0: Disable frame-too-long error interrupt requests 1: Enable frame-too-long error interrupt requests.	R/W
4	RRFIP	Alignment Error Interrupt Request Enable 0: Disable alignment error interrupt requests 1: Enable alignment error interrupt requests.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	RMAFIP	Multicast Address Frame Receive Interrupt Request Enable 0: Disable multicast address frame receive interrupt requests 1: Enable multicast address frame receive interrupt requests.	R/W
8	TROIP	Transmit Retry Over Interrupt Request Enable 0: Disable transmit retry over interrupt requests 1: Enable transmit retry over interrupt requests.	R/W
9	CDIP	Late Collision Detect Interrupt Request Enable 0: Disable late collision detected interrupt requests 1: Enable late collision detected interrupt requests.	R/W
10	DLCIP	Loss of Carrier Detect Interrupt Request Enable 0: Disable loss of carrier detected interrupt requests 1: Enable loss of carrier detected interrupt requests.	R/W

RABT标志（接收中止检测标志）

RABT标志指示ETHERC由于CRC错误、PHY-LSI接收错误、帧太短错误、帧太长错误或其他错误而中止帧接收。

TABT标志（发送中止检测标志）

TABT标志指示ETHERC由于传输重试、载波丢失、未检测到载波或其他错误而中止帧传输。

TWB标志（回写完成标志）

TWB标志表示EDMAC在帧传输后完成写回描述符。当TRIMD.TIM位为0时，此标志在每帧传输后设置为1。仅当TRIMD.TIS位为1时设置为1。

27.2.7 ESIPR：ETHERCEDMAC状态中断使能寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x30

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	TWBIP	—	—	—	TABTIP	RABTIP	RFCOFIP	ADEIP	ECIIP	TCIP	TDEIP	TFUFIP	FRIP	RDEIP	RFOFIP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CNDIP	DLCIP	CDIP	TROIP	RMAFIP	—	—	RRFIP	RTLFIP	RTSFIP	PREIP	CERFIP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CERFIP	CRC错误中断请求使能 0：禁用CRC错误中断请求1：启用CRC错误中断请求。	R/W
1	PREIP	PHY-LSI接收错误中断请求使能 0：禁止PHY-LSI接收错误中断请求1：使能PHY-LSI接收错误中断请求。	R/W
2	RTSFIP	帧太短错误中断请求使能 0：禁用帧太短错误中断请求1：启用帧太短错误中断请求。	R/W
3	RTLFIP	帧过长错误中断请求使能 0：禁用帧过长错误中断请求1：启用帧过长错误中断请求。	R/W
4	RRFIP	对齐错误中断请求启用 0：禁用对齐错误中断请求1：启用对齐错误中断请求。	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	RMAFIP	多播地址帧接收中断请求使能 0：禁止组播地址帧接收中断请求1：使能组播地址帧接收中断请求。	R/W
8	TROIP	通过中断请求启用发送重试 0：禁止发送重试中断请求1：启用发送重试中断请求。	R/W
9	CDIP	后期冲突检测中断请求使能 0：禁用后期冲突检测中断请求1：启用后期冲突检测中断请求。	R/W
10	DLCIP	载波丢失检测中断请求使能 0：禁用检测到载波丢失中断请求1：启用检测到载波丢失中断请求。	R/W

Bit	Symbol	Function	R/W
11	CNDIP	Carrier Not Detect Interrupt Request Enable 0: Disable carrier not detected interrupt requests 1: Enable carrier not detected interrupt requests.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	RFOFIP	Receive FIFO Overflow Interrupt Request Enable 0: Disable overflow interrupt requests 1: Enable overflow interrupt requests.	R/W
17	RDEIP	Receive Descriptor Empty Interrupt Request Enable 0: Disable receive descriptor empty interrupt requests 1: Enable receive descriptor empty interrupt requests.	R/W
18	FRIP	Frame Receive Interrupt Request Enable 0: Disable frame reception interrupt requests 1: Enable frame reception interrupt requests.	R/W
19	TFUFIP	Transmit FIFO Underflow Interrupt Request Enable 0: Disable underflow interrupt requests 1: Enable underflow interrupt requests.	R/W
20	TDEIP	Transmit Descriptor Empty Interrupt Request Enable 0: Disable transmit descriptor empty interrupt requests 1: Enable transmit descriptor empty interrupt requests.	R/W
21	TCIP	Frame Transfer Complete Interrupt Request Enable 0: Disable frame transmission complete interrupt requests 1: Enable frame transmission complete interrupt requests.	R/W
22	ECIIP	ETHERC Status Register Source Interrupt Request Enable 0: Disable ETHERC status interrupt requests 1: Enable ETHERC status interrupt requests.	R/W
23	ADEIP	Address Error Interrupt Request Enable 0: Disable address error interrupt requests 1: Enable address error interrupt requests.	R/W
24	RFCOFIP	Receive Frame Counter Overflow Interrupt Request Enable 0: Disable receive frame counter overflow interrupt requests 1: Enable receive frame counter overflow interrupt requests.	R/W
25	RABTIP	Receive Abort Detect Interrupt Request Enable 0: Disable receive abort detected interrupt requests 1: Enable receive abort detected interrupt requests.	R/W
26	TABTIP	Transmit Abort Detect Interrupt Request Enable 0: Disable transmit abort detected interrupt requests 1: Enable transmit abort detected interrupt requests.	R/W
29:27	—	These bits are read as 0. The write value should be 0.	R/W
30	TWBIP	Write-Back Complete Interrupt Request Enable 0: Disable write-back complete interrupt requests 1: Enable write-back complete interrupt requests.	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

The EESIPR register enables interrupt requests associated with bits in the EESR register. When a bit in this register is 1, the associated interrupt request is enabled.

Bit	Symbol	Function	R/W
11	CNDIP	载波未检测中断请求使能 0：禁用未检测到载波中断请求1：启用未检测到载波中断请求。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
16	RFOFIP	接收FIFO溢出中断请求使能 0：禁止溢出中断请求1：使能溢出中断请求。	R/W
17	RDEIP	接收描述符空中断请求使能 0：禁用接收描述符空中断请求1：启用接收描述符空中断请求。	R/W
18	FRIP	帧接收中断请求使能 0：禁止帧接收中断请求1：允许帧接收中断请求。	R/W
19	TFUFIP	发送FIFO下溢中断请求使能 0：禁止下溢中断请求1：允许下溢中断请求。	R/W
20	TDEIP	发送描述符空中断请求使能 0：禁止发送描述符空中断请求1：使能发送描述符空中断请求。	R/W
21	TCIP	帧传输完成中断请求使能 0：禁止帧发送完成中断请求1：允许帧发送完成中断请求。	R/W
22	ECIIP	ETHERC状态寄存器源中断请求使能 0：禁止ETHERC状态中断请求1：使能ETHERC状态中断请求。	R/W
23	ADEIP	地址错误中断请求使能 0：禁止地址错误中断请求1：允许地址错误中断请求。	R/W
24	RFCOFIP	接收帧计数器溢出中断请求使能 0：禁止接收帧计数器溢出中断请求1：使能接收帧计数器溢出中断请求。	R/W
25	RABTIP	接收中止检测中断请求使能 0：禁用接收中止检测到中断请求1：启用接收中止检测到中断请求。	R/W
26	TABTIP	发送中止检测中断请求使能 0：禁止发送中止检测到中断请求1：使能发送中止检测到中断请求。	R/W
29:27	—	这些位被读取为0。写入值应为0。	R/W
30	TWBIP	回写完成中断请求使能 0：禁止回写完成中断请求1：使能回写完成中断请求。	R/W
31	—	该位读取为0。写入值应为0。	R/W

ESIPR寄存器启用与EESR寄存器中的位相关的中断请求。当该寄存器中的某个位为1时，相关的中断请求被使能。

27.2.8 TRSCER : ETHERC/EDMAC Transmit/Receive Status Copy Enable Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	RMAFCE	—	—	RRFCE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	RRFCE	RRF Flag Copy Enable 0: Reflect the EESR.RRF flag status in the RD0.RFE bit of the receive descriptor 1: Do not reflect the EESR.RRF flag status in the RD0.RFE bit of the receive descriptor.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	RMAFCE	RMAF Flag Copy Enable 0: Reflect the EESR.RMAF flag status in the RD0.RFE bit of the receive descriptor 1: Do not reflect the EESR.RMAF flag status in the RD0.RFE bit of the receive descriptor.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TRSCER register selects whether the receive status indicated in the EESR.RMAF and RRF flags is reflected in the RFE bit of the receive descriptor as a summary. The bits in this register are associated with bits in the EESR register that have the same number. When the RMAFCE or RRFCE bit is set to 0, the associated receive status is reflected in the RFE bit. When the RMAFCE or RRFCE bit is set to 1, the associated receive status is not reflected.

27.2.9 RMFCR : Missed-Frame Counter Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x40

Bit position:	31	15	0
Bit field:	—	MFC[15:0]	
Value after reset:	0	0	0

Bit	Symbol	Function	R/W
15:0	MFC[15:0]	Missed-Frame Counter These bits indicate the number of frames that are discarded and not transferred to the receive buffer during reception.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The RMFCR register indicates that the number of frames that could not be stored in the receive FIFO and so were discarded during reception. When the receive FIFO overflows, it stops receiving data, and the rest of frames are discarded. At the same time, the RMFCR register value is incremented. When the RMFCR register value reaches 0xFFFF, count-up is halted. Writing any value to the RMFCR register clears the counter value to 0.

For frames that are not completely received, after data in the receive FIFO is transferred to the receive buffer, the RACT bit in the receive descriptor 0 (RD0) clears to 0 (descriptor disabled), the RFS9 bit sets to 1 (receive FIFO overflowed), and the EESR.RFOF flag is set to 1 (overflow detected).

27.2.8 TRSCER：ETHERCEDMAC发送接收状态复制使能寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	RMAFCE	—	—	RRFCE	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	RRFCE	RRF标志复制启用 0：在接收描述符的RD0.RFE位中反映EESR.RRF标志状态1：在接收描述符的RD0.RFE位中不反映EESR.RRF标志状态。	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	RMAFCE	RMAF标志复制启用 0：在接收描述符的RD0.RFE位中反映EESR.RMAF标志状态1：在接收描述符的RD0.RFE位中不反映EESR.RMAF标志状态。	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TRSCER寄存器选择是否将EESR.RMAF和RRF标志中指示的接收状态作为摘要反映在接收描述符的RFE位中。该寄存器中的位与EESR寄存器中具有相同编号的位相关联。当RMAFCE或RRFCE位设置为0时，相关的接收状态反映在RFE位中。当RMAFCE或RRFCE位设置为1时，不反映相关的接收状态。

27.2.9 RMFCR:漏帧计数器寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x40

Bit position:	31	15	0
Bit field:	—	MFC[15:0]	
重置后的值：	0	0	0

Bit	Symbol	Function	R/W
15:0	MFC[15:0]	Missed-Frame Counter 这些位指示在接收期间被丢弃且未传输到接收缓冲区的帧数。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

RMFCR寄存器指示无法存储在接收FIFO中并因此在接收期间被丢弃的帧数。当接收FIFO溢出时，它停止接收数据，其余帧被丢弃。同时，RMFCR寄存器值递增。当RMFCR寄存器值达到0xFFFF时，停止向上计数。向RMFCR寄存器写入任何值都会将计数器值清零。

对于未完全接收的帧，接收FIFO中的数据传输到接收缓冲区后，接收描述符0（RD0）中的RACT位清为0（描述符禁用），RFS9位设置为1（接收FIFO溢出），并且EESR.RFOF标志设置为1（检测到溢出）。

27.2.10 TFTR : Transmit FIFO Threshold Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x48

Bit position:	31																			10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TFT[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	TFT[10:0]	Transmit FIFO Threshold 0x000: Store-and-forward mode 0x001 to 0x00C: Setting prohibited 0x00D to 0x200: The threshold is the set value multiplied by 4. 0x201 to 0x7FF: Setting prohibited Example: TFT[10:0] = 0x00D : 52 bytes TFT[10:0] = 0x040 : 256 bytes TFT[10:0] = 0x100 : 1024 bytes TFT[10:0] = 0x200 : 2048 bytes	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: When starting transmission before one frame data is completely written, take care to prevent an underflow. To prevent a transmit underflow, Renesas recommends using the initial value (store-and-forward mode).

The TFTR register specifies the transmit FIFO threshold at which the first transmission starts. The actual threshold is the set value multiplied by 4.

The ETHERC starts transmission when the amount of data in the transmit FIFO exceeds the number of bytes set in this register, when the transmit FIFO is full, or when one frame of data is completely written. Set the TFTR register while the EDTRR.TR bit is 0.

27.2.11 FDR : FIFO Depth Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TFD[4:0]					—	—	—	RFD[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	RFD[4:0]	Receive FIFO Depth 0x0F: 4096 bytes Others: settings prohibited	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
12:8	TFD[4:0]	Transmit FIFO Depth 0x07: 2048 bytes Others: settings prohibited	R/W
31:13	—	These bits are read as 0. The write value should be 0.	R/W

27.2.10 TFTR：发送FIFO阈值寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x48

Bit position:	31																			10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TFT[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	TFT[10:0]	发送FIFO阈值 0x000: Store-and-forward mode 0x001 to 0x00C: 禁止设定阈值为设定值乘以4。 0x00D to 0x200: 0x201 to 0x7FF: 禁止设定 Example: TFT[10:0] = 0x00D : 52 bytes TFT[10:0] = 0x040 : 256 bytes TFT[10:0] = 0x100 : 1024 bytes TFT[10:0] = 0x200 : 2048 bytes	R/W
31:11	—	这些位被读取为0。写入值应为0。	R/W

Note: 在完全写入一帧数据之前开始传输时，请注意防止下溢。为防止发送下溢，瑞萨推荐使用初始值（存储转发模式）。

TFTR寄存器指定第一次发送开始时的发送FIFO阈值。实际阈值是设定值乘以4。

当发送FIFO中的数据量超过此寄存器中设置的字节数、发送FIFO已满或一帧数据被完全写入时，ETHERC开始发送。当EDTRR.TR位为0时设置TFTR寄存器。

27.2.11 FDR：FIFO深度寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TFD[4:0]					—	—	—	RFD[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

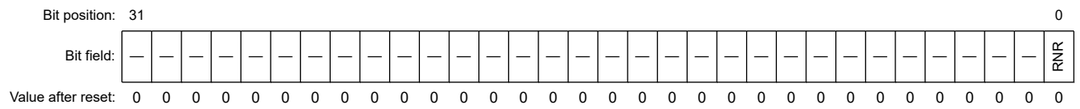
Bit	Symbol	Function	R/W
4:0	RFD[4:0]	接收FIFO深度 0x0F: 4096 bytes 其他：禁止设置	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
12:8	TFD[4:0]	发送FIFO深度 0x07: 2048 bytes 其他：禁止设置	R/W
31:13	—	这些位被读取为0。写入值应为0。	R/W

The FDR register specifies the transmit and receive FIFO depths. Set this register to 0x0000_070F before starting transmission and reception.

27.2.12 RMCR : Receive Method Control Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x58



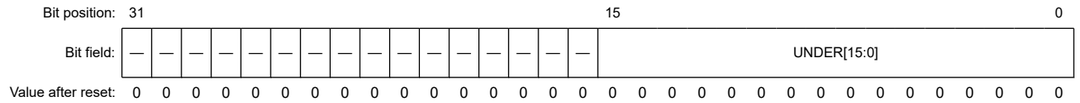
Bit	Symbol	Function	R/W
0	RNR	Receive Request Reset 0: EDRRR.RR bit (receive request bit) is cleared to 0 when one frame is received 1: EDRRR.RR bit (receive request bit) is not cleared to 0 when one frame is received.	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The RMCR register specifies how to control the EDRRR.RR bit when receiving a frame. When the RNR bit is 0, the EDRRR.RR bit clears to 0 when one frame is received, so it must be set to 1 by software to receive the subsequent frame. When the RNR bit is 1, the EDRRR.RR bit does not clear to 0 when one frame is received, and the EDMAC reads the next receive descriptor and continues frame reception. Renesas recommends setting the RNR bit to 1 when receiving data continuously. Set the RMCR register while the EDRRR.RR bit is 0.

27.2.13 TFUCR : Transmit FIFO Underflow Counter

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x64



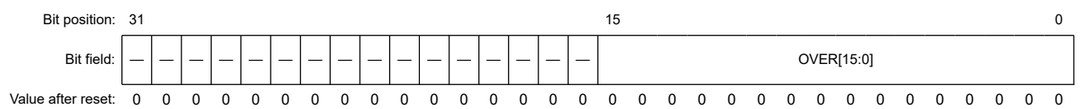
Bit	Symbol	Function	R/W
15:0	UNDER[15:0]	Transmit FIFO Underflow Count These bits indicate how many times the transmit FIFO underflows. The counter stops when the counter value reaches 0xFFFF.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The TFUCR register indicates how many times the transmit FIFO underflows. Writing any value to the TFUCR register clears the counter value to 0.

27.2.14 RFOCR : Receive FIFO Overflow Counter

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x68

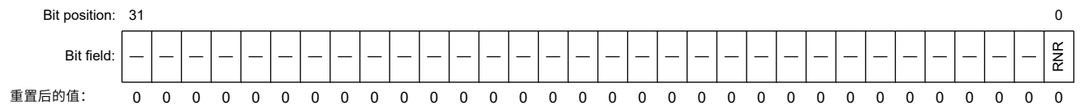


FDR寄存器指定发送和接收FIFO深度。在开始发送和接收之前将此寄存器设置为0x0000_070F。

27.2.12 RMCR:接收方法控制寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x58



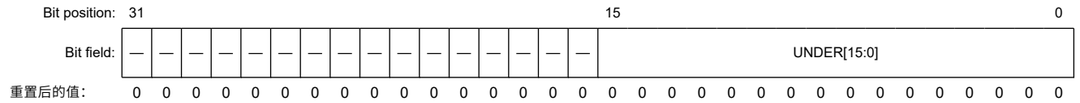
Bit	Symbol	Function	R/W
0	RNR	接收请求重置 0：当接收一帧时，EDRRR.RR位（接收请求位）清零1：当接收一帧时，EDRRR.RR位（接收请求位）不清零。	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

RMCR寄存器指定接收帧时如何控制EDRRR.RR位。当RNR位为0时，
EDRRR.RR位在接收到一帧后清为0，因此必须通过软件设置为1才能接收后续帧。
当RNR位为1时，接收到一帧时EDRRR.RR位不清为0，EDMAC读取下一个接收描述符并继续帧接收。Renesas建议在连续接收数据时将RNR位设置为1。当EDRRR.RR位为0时设置RMCR寄存器。

27.2.13 TFUCR：发送FIFO下溢计数器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x64



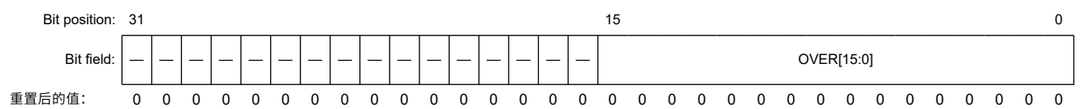
Bit	Symbol	Function	R/W
15:0	UNDER[15:0]	发送FIFO下溢计数 这些位指示发送FIFO下溢的次数。当计数器值达到0xFFFF时，计数器停止。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

TFUCR寄存器指示发送FIFO下溢的次数。向TFUCR寄存器写入任何值都会将计数器值清零。

27.2.14 RFOCR:接收FIFO溢出计数器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x68



Bit	Symbol	Function	R/W
15:0	OVER[15:0]	Receive FIFO Overflow Count These bits indicate how many times the receive FIFO overflows. The counter stops when the counter value reaches 0xFFFF.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The RFOCR register indicates how many times the receive FIFO overflows. Writing any value to the RFOCR register clears the counter value to 0.

27.2.15 IOSR : Independent Output Signal Setting Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x6C

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ELB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ELB	External Loopback Mode 0: Output low on the ET0_EXOUT pin 1: Output high on the ET0_EXOUT pin.	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

The IOSR register selects the output level of the ETHERC external output pin (ET0_EXOUT) in external loopback mode. The ELB bit value is output on the ET0_EXOUT pin, which can be used to set loopback mode for the PHY-LSI.

To use the loopback function of the PHY-LSI through this register, you must connect the PHY-LSI to the ET0_EXOUT pin.

27.2.16 FCFTR : Flow Control Start FIFO Threshold Setting Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x70

Bit position:	31												18	16													2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RFFO[2:0]		—	—	—	—	—	—	—	—	—	—	—	—	RFDO[2:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	RFDO[2:0]	Receive FIFO Data PAUSE Output Threshold 0 0 0: When 224 (256 to 32) bytes of data is stored in the receive FIFO 0 0 1: When 480 (512 to 32) bytes of data is stored in the receive FIFO ⋮ 1 1 0: When 1760 (1792 to 32) bytes of data is stored in the receive FIFO 1 1 1: When 2016 (2048 to 32) bytes of data is stored in the receive FIFO.	R/W
15:3	—	These bits are read as 0. The write value should be 0.	R/W
18:16	RFFO[2:0]	Receive FIFO Frame PAUSE Output Threshold 0 0 0: When 2 receive frames are stored in the receive FIFO 0 0 1: When 4 receive frames are stored in the receive FIFO 0 1 0: When 6 receive frames are stored in the receive FIFO ⋮ 1 1 0: When 14 receive frames are stored in the receive FIFO 1 1 1: When 16 receive frames are stored in the receive FIFO.	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The FCFTR register specifies the ETHERC flow control. Set the threshold to automatically transmit a PAUSE frame.

Bit	Symbol	Function	R/W
15:0	OVER[15:0]	接收FIFO溢出计数 这些位指示接收FIFO溢出的次数。 当计数器值达到0xFFFF时，计数器停止。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

RFOCR寄存器指示接收FIFO溢出的次数。向RFOCR寄存器写入任何值都会将计数器值清零。

27.2.15 IOSR：独立输出信号设置寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x6C

Bit position:	31																													0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ELB
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ELB	外部环回模式 0：ET0_EXOUT引脚输出低电平1：ET0_ EXOUT引脚输出高电平。	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

IOSR寄存器选择外部环回模式下ETHERC外部输出引脚(ET0_EXOUT)的输出电平。
ELB位值在ET0_EXOUT引脚上输出，可用于设置PHY-LSI的环回模式。
要通过该寄存器使用PHY-LSI的环回功能，您必须将PHY-LSI连接到ET0_EXOUT引脚。

27.2.16 FCFTR:流控制启动FIFO阈值设置寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x70

Bit position:	31												18	16													2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	RFFO[2:0]		—	—	—	—	—	—	—	—	—	—	—	—	RFDO[2:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
2:0	RFDO[2:0]	接收FIFO数据暂停输出阈值 000：接收FIFO中存储224（256到32）字节数据时001：接收FIFO中存 储480（512到32）字节数据时 ⋮ 110：当1760（1792到32）字节数据存储在接收FIFO中时111：当2016（ 2048到32）字节数据存储在接收FIFO中时。	R/W
15:3	—	这些位被读取为0。写入值应为0。	R/W
18:16	RFFO[2:0]	接收FIFO帧暂停输出阈值 000：接收FIFO中存储2个接收帧时001：接收FIFO中存储4个 接收帧时010：接收FIFO中存储6个接收帧时 ⋮ 110：接收FIFO中存储14个接收帧时111：接收FIFO中存储16个 接收帧时。	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

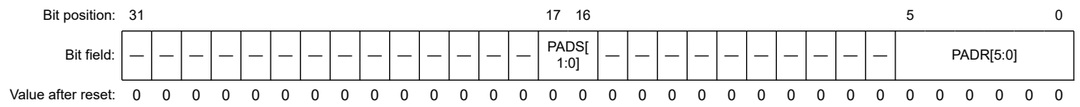
FCFTR寄存器指定ETHERC流控制。设置阈值以自动发送PAUSE帧。

The threshold can be set using the data size (RFDO[2:0] bits) and the number of frames (RFFO[2:0] bits) stored in the receive FIFO. Flow control starts when the stored data size or the number of stored frames reaches its threshold.

27.2.17 RPADIR : Receive Data Padding Insert Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x78



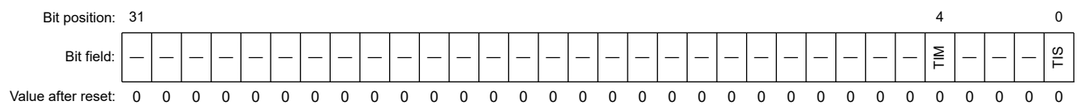
Bit	Symbol	Function	R/W
5:0	PADR[5:0]	Padding Slot 0x00: Insert padding at the head of received data 0x01: Insert padding between the 1st and 2nd bytes of received data ⋮ 0x3E: Insert padding between the 62nd and 63rd bytes of received data 0x3F: Insert padding between the 63rd and 64th bytes of received data.	R/W
15:6	—	These bits are read as 0. The write value should be 0.	R/W
17:16	PADS[1:0]	Padding Size 0 0: Do not insert padding Others: settings prohibited	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The RPADIR register specifies insertion of padding for received data. The padding value is 0x00. Set the EDMR.SWR bit to 1 to reset before rewriting the PRADIR register.

27.2.18 TRIMD : Transmit Interrupt Setting Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x7C



Bit	Symbol	Function	R/W
0	TIS	Transmit Interrupt Enable 0: Disable transmit interrupts 1: Enable transmit Interrupts. Set the EESR.TWB flag to 1 in the mode selected in the TIM bit to report an interrupt.	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	TIM	Transmit Interrupt Mode 0: Select transmission complete interrupt mode, where an interrupt occurs when a frame is transmitted 1: Select write-back complete interrupt mode, where an interrupt occurs when write-back to the transmit descriptor is complete while the TWBI bit is 1.	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

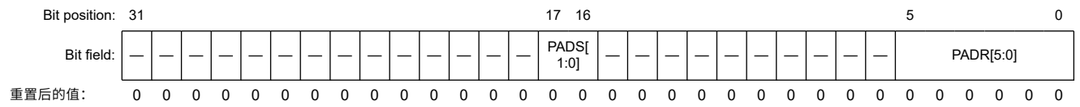
The TRIMD register specifies the transmit interrupt mode and enables or disables transmit interrupts. When the condition selected in this register is satisfied, the EESR.TWB flag sets to 1, and an interrupt request is output when the EESIPR.TWBIP bit is 1.

可以使用存储在接收FIFO中的数据大小（RFDO[2:0]位）和帧数（RFFO[2:0]位）来设置阈值。当存储的数据大小或存储的帧数达到其阈值时，流量控制开始。

27.2.17 RPADIR:接收数据填充插入寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x78



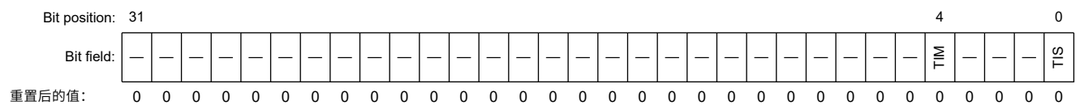
Bit	Symbol	Function	R/W
5:0	PADR[5:0]	填充槽 0x00：在接收数据的头部插入填充0x01：在接收数据的第1和第2个字节之间插入填充 ⋮ 0x3E：在接收数据的第62和63字节之间插入填充0x3F：在接收数据的第63和第64字节之间插入填充。	R/W
15:6	—	这些位被读取为0。写入值应为0。	R/W
17:16	PADS[1:0]	填充尺寸 00：不插入填充 其他：禁止设置	R/W
31:18	—	这些位被读取为0。写入值应为0。	R/W

RPADIR寄存器指定为接收到的数据插入填充。填充值是0x00。在重写PRADIR寄存器之前，将EDMR.SWR位设置为1以复位。

27.2.18 TRIMD：发送中断设置寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0x7C



Bit	Symbol	Function	R/W
0	TIS	发送中断使能 0：禁用发送中断1：启用发送中断。 在TIM位选择的模式下将EESR.TWB标志设置为1以报告中断。	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	TIM	发送中断模式 0：选择传输完成中断模式，传输一帧时发生中断 1：选择回写完成中断模式，当TWBI位为1时，当回写发送描述符完成时产生中断。	R/W
31:5	—	这些位被读取为0。写入值应为0。	R/W

TRIMD寄存器指定发送中断模式并启用或禁用发送中断。当满足此寄存器中选择的条件时，EESR.TWB标志设置为1，并且当ESIPR.TWBIP位为1时输出中断请求。

27.2.19 RBWAR : Receive Buffer Write Address Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xC8

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	The RBWAR register indicates the last address that the EDMAC wrote data to, when writing to the receive buffer.	R

The RBWAR register indicates the last address that the EDMAC wrote data to, when writing to the receive buffer. Check the contents of this register to identify the address in the receive buffer to which the EDMAC is writing data to. The address that the EDMAC is outputting to the receive buffer might not match the read value of the RBWAR register during data reception. The RBWAR register is read-only. Do not write to this register.

27.2.20 RDFAR : Receive Descriptor Fetch Address Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xCC

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	The RDFAR register indicates the start address of the last fetched receive descriptor when the EDMAC is fetching descriptor information from the receive descriptor.	R

The RDFAR register indicates the start address of the last fetched receive descriptor when the EDMAC is fetching descriptor information from the receive descriptor. Check the contents of this register to identify which receive descriptor information the EDMAC is using for active processing. The address of the receive descriptor that the EDMAC is fetching might not match the read value of the RDFAR register during data reception. The RDFAR register is read-only.

Do not write to this register.

27.2.21 TBRAR : Transmit Buffer Read Address Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xD4

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	The TBRAR register indicates the last address from which the EDMAC read data, when reading data from the transmit buffer.	R

The TBRAR register indicates the last address from which the EDMAC read data, when reading data from the transmit buffer. Check the contents of this register to identify which address in the transmit buffer the EDMAC is reading from.

The address that the EDMAC is outputting to the transmit buffer might not match the read value of the TBRAR register.

27.2.19 RBWAR：接收缓冲区写地址寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xC8

Bit position:	31																												0
Bit field:																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	当写入接收缓冲区时，RBWAR寄存器指示EDMAC写入数据的最后一个地址。	R

当写入接收缓冲区时，RBWAR寄存器指示EDMAC写入数据的最后一个地址。检查该寄存器的内容以确定EDMAC正在向其写入数据的接收缓冲区中的地址。在数据接收期间，EDMAC输出到接收缓冲区的地址可能与RBWAR寄存器的读取值不匹配。RBWAR寄存器是只读的。不要写入该寄存器。

27.2.20 RDFAR:接收描述符获取地址寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xCC

Bit position:	31																												0
Bit field:																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	当EDMAC从接收描述符中获取描述符信息时，RDFAR寄存器指示最后获取的接收描述符的起始地址。	R

当EDMAC从接收描述符中获取描述符信息时，RDFAR寄存器指示最后获取的接收描述符的起始地址。检查该寄存器的内容以确定EDMAC正在使用哪些接收描述符信息进行主动处理。EDMAC正在获取的接收描述符的地址可能与数据接收期间RDFAR寄存器的读取值不匹配。RDFAR寄存器是只读的。

不要写入该寄存器。

27.2.21 TBRAR:发送缓冲区读地址寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xD4

Bit position:	31																												0
Bit field:																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	当从发送缓冲区读取数据时，TBRAR寄存器指示EDMAC读取数据的最后地址。	R

当从发送缓冲区读取数据时，TBRAR寄存器指示EDMAC读取数据的最后地址。检查该寄存器的内容以确定EDMAC正在从发送缓冲区中的哪个地址读取。

EDMAC输出到发送缓冲区的地址可能与TBRAR寄存器的读取值不匹配。

The TBRAR register is read-only. Do not write to this register.

27.2.22 TDFAR : Transmit Descriptor Fetch Address Register

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xD8

Bit	Symbol	Function	R/W
31:0	n/a	The TDFAR register indicates the start address of the last fetched transmit descriptor when the EDMAC is fetching the descriptor information from the transmit descriptor.	R

The TDFAR register indicates the start address of the last fetched transmit descriptor when the EDMAC is fetching the descriptor information from the transmit descriptor. Check the contents of this register to identify which transmit descriptor information the EDMAC is using for active processing. The address of transmit descriptor that the EDMAC fetches might not match the read value of the TDFAR register. The TDFAR is read only. Do not write to this register.

27.3 Operation

The EDMAC transfers data according to the information written in the descriptor. Two descriptors are provided: transmit and receive. A descriptor includes the buffer size, address, and transmit or receive status. The EDMAC transmits or receives data continuously by using sequentially arranged descriptors.

27.3.1 Descriptor Lists and Data Buffers

To transfer data using the EDMAC, create the transmit and receive descriptor lists in memory, set the start address of the transmit descriptor list in the TDLAR register, and set the start address of the receive descriptor list in the RDLAR register. Also, the transmit and receive buffers associated with each descriptor are required.

Align the descriptor list on the appropriate address boundary according to the descriptor length set in the EDMR.DL[1:0] bits. The transmit buffer can be aligned on a word boundary, halfword boundary, or byte boundary. When the valid transmit buffer size is 16 bytes or less, align it on a 32-byte boundary. When the valid transmit buffer size is larger than 16bytes, the transmit buffer setting on not aligned 32-byte boundary is permitted. However EDMAC0 might read the transmit buffer aligned on 32-byte boundary, therefore, initialize the transmit buffer area at the beginning of 32 byte-boundary where the transmit buffer set in. Align the receive buffer on a 32-byte boundary. Set different addresses for the transmit and receive descriptors and buffers for EDMAC0.

27.3.1.1 Transmit descriptor

Figure 27.3 shows the relationship between a transmit descriptor and transmit buffer. A transmit descriptor consists of TD0 to TD2. The transmit frame and transmit buffer configuration can be specified as one buffer per frame (single-buffer frame transmission) or multiple buffers per frame (multi-buffer frame transmission) by setting the transmit descriptor.

TBRAR寄存器是只读的。不要写入该寄存器。

27.2.22 TDFAR:发送描述符获取地址寄存器

Base address: EDMAC0 = 0x4011_4000

Offset address: 0xD8

Bit	Symbol	Function	R/W
31:0	n/a	当EDMAC从发送描述符中获取描述符信息时，TDFAR寄存器指示最后获取的发送描述符的起始地址。	R

当EDMAC从发送描述符中获取描述符信息时，TDFAR寄存器指示最后获取的发送描述符的起始地址。检查该寄存器的内容以确定EDMAC正在使用哪些传输描述符信息进行主动处理。EDMAC获取的发送描述符地址可能与TDFAR寄存器的读取值不匹配。TDFAR是只读的。不要写入该寄存器。

27.3 Operation

EDMAC根据描述符中写入的信息传输数据。提供了两个描述符：发送和接收。描述符包括缓冲区大小、地址和发送或接收状态。EDMAC通过使用顺序排列的描述符连续发送或接收数据。

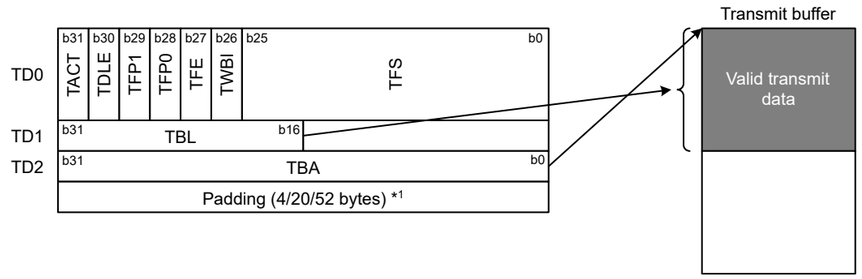
27.3.1 描述符列表和数据缓冲区

要使用EDMAC传输数据，在内存中创建发送和接收描述符列表，在TDLAR寄存器中设置发送描述符列表的起始地址，在RDLAR寄存器中设置接收描述符列表的起始地址。此外，还需要与每个描述符关联的发送和接收缓冲区。

根据在EDMR.DL[1:0]位中设置的描述符长度将描述符列表对齐在适当的地址边界上。发送缓冲区可以在字边界、半字边界或字节边界上对齐。当有效发送缓冲区大小为16字节或更少时，将其对齐在32字节边界上。当有效传输缓冲区大小大于16字节时，允许在未对齐的32字节边界上设置传输缓冲区。然而，EDMAC0可能会读取对齐在32字节边界上的传输缓冲区，因此，在设置传输缓冲区的32字节边界的开头初始化传输缓冲区。将接收缓冲区对齐在32字节边界上。为EDMAC0的发送和接收描述符和缓冲区设置不同的地址。

27.3.1.1 传输描述符

图27.3显示了发送描述符和发送缓冲区之间的关系。发送描述符由TD0到TD2组成。通过设置传输描述符，可以将传输帧和传输缓冲区配置指定为每帧一个缓冲区（单缓冲区帧传输）或每帧多个缓冲区（多缓冲区帧传输）。



Note 1. The padding size is determined by the descriptor length (16/32/64 bytes).

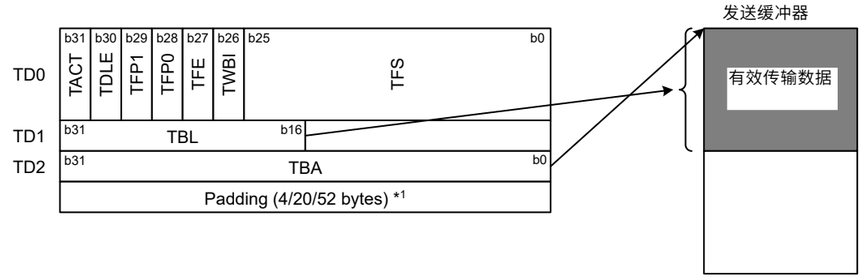
Figure 27.3 Relationship between transmit descriptor and transmit buffer

(1) Transmit descriptor 0 (TD0)

Note: Bits for write-back are underlined.

Bit	Symbol	Function	R/W
25:0	TFS	Transmit Frame Status Set all bits to 0 when creating a descriptor. After write-back, the bits indicate the following: TFS25 to TFS9: Reserved TFS8: Transmit abort was detected (value is equivalent to the EESR.TABT flag) TFS7 to TFS4: Reserved TFS3: No carrier was detected (value is equivalent to the EESR.CND flag) TFS2: Loss of carrier was detected (value is equivalent to the EESR.DLC flag) TFS1: Late collision during transmission was detected (value is equivalent to the EESR.CD flag) TFS0: Transmit retry over (value is equivalent to the EESR.TRO flag). When a bit sets to 1, it indicates that the associated error occurred during frame transmission. When any of the TFS bits sets to 1, the TFE bit also is set to 1. When any of bits TFS3 to TFS0 is set to 1, TFS8 is also set to 1.	R/W
26	TWBI	Write-Back Complete Interrupt Enable 0: Do not generate interrupt when write-back to this descriptor is complete 1: Generate interrupt when write-back to this descriptor is complete.	R/W
27	TFE	Transmit Frame Error 0: Frame transmission is successfully complete 1: Error occurred during frame transmission (transmission aborted).	R/W
29:28	TFP[1:0]	Transmit Frame Position 0 0: Transmit buffer indicated in this descriptor is the middle of a transmit frame (frame information is incomplete) 0 1: Transmit buffer indicated in this descriptor is the end of a transmit frame (frame information is complete) 1 0: Transmit buffer indicated in this descriptor is the head of a transmit frame (frame information is incomplete) 1 1: Transmit buffer indicated in this descriptor is all of a transmit frame (one buffer per frame).	R/W
30	TDLE	Transmit Descriptor List End When this bit is 1, it indicates that this descriptor is the last in the descriptor list.	R/W
31	TACT	Transmit Descriptor Valid This bit indicates that this descriptor is valid.	R/W

TD0 specifies the transmit frame settings and indicates the status after transmission.



注1.填充大小由描述符长度（163264字节）决定。

Figure 27.3 发送描述符和发送缓冲区的关系

(1) 发送描述符0(TD0)

Note: 用于回写的位带有下划线。

Bit	Symbol	Function	R/W
25:0	TFS	发送帧状态 创建描述符时将所有位设置为0。回写后，这些位指示以下内容： TFS25 to TFS9: Reserved TFS8: 检测到发送中止（值等同于EESR.TABT标志） TFS7 to TFS4: Reserved TFS3: 未检测到载体（值等同于EESR.CND标志） TFS2: 检测到载波丢失（值相当于EESR.DLC标志） TFS1: 检测到传输过程中的后期冲突（值等于EESR.CD flag) TFS0: 传输重试结束（值相当于EESR.TRO标志）。 当某个位设置为1时，表示在帧传输期间发生了相关错误。当任何TFS位设置为1时，TFE位也设置为1。当任何位TFS3到TFS0设置为1时，TFS8也设置为1。	R/W
26	TWBI	回写完成中断使能 0：回写该描述符完成时不产生中断1：回写该描述符完成时产生中断。	R/W
27	TFE	传输帧错误 0：帧传输成功完成1：帧传输过程中发生错误（传输中止）。	R/W
29:28	TFP[1:0]	发送帧位置 00：此描述符中指示的传输缓冲区是传输帧的中间（帧信息不完整） 01：此描述符中指示的发送缓冲区是发送帧的结尾（帧信息完整） 10：此描述符中指示的传输缓冲区是传输帧的头部（帧信息不完整） 11：此描述符中指示的传输缓冲区是一个传输帧的全部（每帧一个缓冲区）。	R/W
30	TDLE	传输描述符列表结束 当该位为1时，表示该描述符是描述符列表中的最后一个。	R/W
31	TACT	传输描述符有效 该位指示该描述符有效。	R/W

TD0指定传输帧设置并指示传输后的状态。

TFE bit (Transmit Frame Error)

When the TFE bit is 1, it indicates that any of the TFS bits is 1.

TFP[1:0] bits (Transmit Frame Position)

The TFP[1:0] bits indicate which part of a transmit frame corresponds to the transmit buffer indicated in this descriptor. The TFP[1:0] and TD1.TBL bit settings must be logically consistent in the previous and next descriptors.

TACT bit (Transmit Descriptor Valid)

The TACT bit indicates that this descriptor is valid. The TACT bit is set to 1 by software. This bit clears to 0 when the transmit frame is transferred or when the transmission is aborted.

(2) Transmit descriptor 1 (TD1)

Bit	Symbol	Function	R/W
15:0	—	The read value is 0. The write value should be 0.	R/W
31:16	TBL	Transmit Buffer Length Specifies the valid byte length of the associated transmit buffer. Set a value equal to or greater than 1.	R/W

TD1 specifies the valid byte length of the transmit buffer.

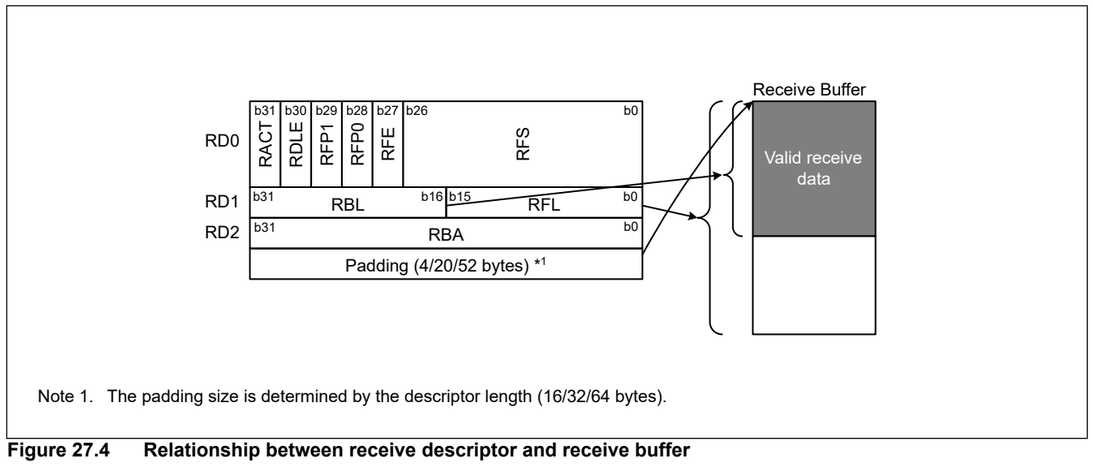
(3) Transmit descriptor 2 (TD2)

Bit	Symbol	Function	R/W
31:0	TBA	Transmit Buffer Address Specifies the start address of the transmit buffer. When the TD1.TBL bit value is 1 to 16 bytes, align it on a 32-byte boundary.	R/W

TD2 specifies the start address of the transmit buffer.

27.3.1.2 Receive descriptor

Figure 27.4 shows the relationship between a receive descriptor and receive buffer. The receive frame and receive buffer configuration can be specified as one buffer per frame (single-buffer frame transmission) or multiple buffers per frame (multi-buffer frame transmission) by setting the receive descriptor. If the receive buffer length (RBL) is set to 0, the operation indicated in the descriptor is not guaranteed.



Note 1. The padding size is determined by the descriptor length (16/32/64 bytes).

Figure 27.4 Relationship between receive descriptor and receive buffer

TFE位（发送帧错误）

当TFE位为1时，表示任何TFS位为1。

TFP[1:0]位（发送帧位置）

TFP[1:0]位指示发送帧的哪一部分对应于该描述符中指示的发送缓冲区。
TFP[1:0]和TD1.TBL位设置在前一个和下一个描述符中必须在逻辑上一致。

TACT位（发送描述符有效）

TACT位指示该描述符是有效的。TACT位由软件设置为1。该位清零时
传输帧或传输中止时。

(2) 传输描述符1(TD1)

Bit	Symbol	Function	R/W
15:0	—	读取值为0。写入值应为0。	R/W
31:16	TBL	发送缓冲区长度 指定相关传输缓冲区的有效字节长度。设置一个等于或大于1的值。	R/W

TD1指定发送缓冲区的有效字节长度。

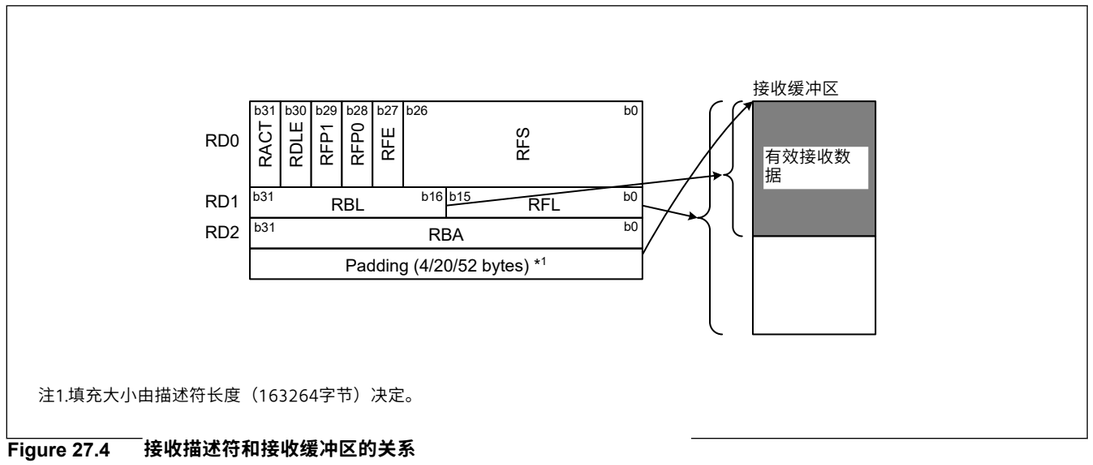
(3) 传输描述符2(TD2)

Bit	Symbol	Function	R/W
31:0	TBA	发送缓冲区地址 指定发送缓冲区的起始地址。当TD1.TBL位值为1到16字节时，将其对齐在32字节边界上。	R/W

TD2指定发送缓冲区的起始地址。

27.3.1.2 接收描述符

图27.4显示了接收描述符和接收缓冲区之间的关系。通过设置接收描述符，可以将接收帧和接收缓冲区配置指定为每帧一个缓冲区（单缓冲区帧传输）或每帧多个缓冲区（多缓冲区帧传输）。如果接收缓冲区长度(RBL)设置为0，则无法保证描述符中指示的操作。



注1.填充大小由描述符长度（163264字节）决定。

Figure 27.4 接收描述符和接收缓冲区的关系

(1) Receive descriptor 0 (RD0)

Note: Bits for write-back are underlined.

Bit	Symbol	Function	R/W
26:0	RFS	Receive Frame Status Set all bits to 0 when creating a descriptor. After write-back, the bits indicate the following: RFS26 to RFS10: Reserved RFS9: Receive FIFO overflow (value is equivalent to the EESR.RFOF flag) RFS8: Receive abort was detected (value is equivalent to the EESR.RABT flag) RFS7: Multicast address frame was received (value is equivalent to the EESR.RMAF flag) RFS6 and RFS5: Reserved RFS4: Alignment error was detected (value is equivalent to the EESR.RRF flag) RFS3: Frame-too-long error (value is equivalent to the EESR.RTLF flag) RFS2: Frame-too-short error (value is equivalent to the EESR.RTSF flag) RFS1: PHY-LSI receive error (value is equivalent to the EESR.PRE flag) RFS0: CRC error (value is equivalent to the EESR.CERF flag). When a bit sets to 1, it indicates that the associated error occurred during frame reception. When any of the RFS bits sets to 1, the RFE bit also sets to 1. Set the TRSCER register to select whether bits RFS7 and RFS4 are reflected in the RFE bit. When any of bits RFS3 to RFS0 sets to 1, RFS8 also sets to 1.	R/W
27	RFE	Receive Frame Error 0: No error occurred in the received frame 1: Error occurred in the received frame.	R/W
29:28	RFP[1:0]	Receive Frame Position 0 0: Receive buffer indicated in this descriptor is the middle of a receive frame (frame information is incomplete) 0 1: Receive buffer indicated in this descriptor is the end of a receive frame (frame information is complete) 1 0: Receive buffer indicated in this descriptor is the head of a receive frame (frame information is incomplete) 1 1: Receive buffer indicated in this descriptor is all of a receive frame (one buffer per frame).	R/W
30	RDLE	Receive Descriptor List End When this bit is 1, it indicates that this descriptor is the last in the descriptor list.	R/W
31	RACT	Receive Descriptor Valid Indicates that this descriptor is valid.	R/W

RD0 indicates the receive frame status.

RFE bit (Receive Frame Error)

When the RFE bit is 1, it indicates that any of the RFS 7 bits is 1. Set the TRSCER register to select whether the RFS and RFS4 bits of EDMAC0 are reflected in the RFE bit.

RFP[1:0] bits (Receive Frame Position)

The RFP[1:0] bits indicate which part of a receive frame corresponds to the receive buffer indicated in this descriptor.

RACT bit (Receive Descriptor Valid)

The RACT bit indicates that this descriptor is valid. The RACT bit is set to 1 by software. This bit clears to 0 when all the data is transferred to the receive buffer indicated in RD2 or when the receive buffer becomes full.

(1) 接收描述符0(RD0)

Note: 用于回写的位带有下划线。

Bit	Symbol	Function	R/W
26:0	RFS	接收帧状态 创建描述符时将所有位设置为0。回写后，这些位指示以下内容： RFS26 to RFS10: Reserved RFS9: 接收FIFO溢出（值相当于EESR.RFOF标志） RFS8: 检测到接收中止（值等同于EESR.RABT标志） RFS7: 收到多播地址帧（值相当于EESR.RMAF标志） RFS6 and RFS5: Reserved RFS4: 检测到对齐错误（值相当于EESR.RRF标志） RFS3: 帧太长错误（值相当于EESR.RTLF标志） RFS2: 帧太短错误（值相当于EESR.RTSF标志） RFS1: PHY-LSI接收错误（值相当于EESR.PRE标志） RFS0: CRC错误（值等同于EESR.CERF标志）。 当某个位设置为1时，表示在帧接收期间发生了相关错误。当任何RFS位设置为1时，RFE位也设置为1。设置TRSCER寄存器以选择位RFS7和RFS4是否反映在RFE位中。当RFS3到RFS0的任何位设置为1时，RFS8也设置为1。	R/W
27	RFE	接收帧错误 0：接收帧未发生错误1：接收帧发生错误 。	R/W
29:28	RFP[1:0]	接收帧位置 00：此描述符中指示的接收缓冲区是接收帧的中间（帧信息不完整） 01：此描述符中指示的接收缓冲区是接收帧的结尾（帧信息完整） 10：此描述符中指示的接收缓冲区是接收帧的头部（帧信息不完整） 11：此描述符中指示的接收缓冲区是一个接收帧的全部（每帧一个缓冲区）。	R/W
30	RDLE	接收描述符列表结束 当该位为1时，表示该描述符是描述符列表中的最后一个。	R/W
31	RACT	接收描述符有效 表示此描述符有效。	R/W

RD0指示接收帧状态。

RFE位（接收帧错误）

当RFE位为1时，表示RFS7位中的任何一个为1。设置TRSCER寄存器以选择是否RFS和EDMAC0的RFS4位反映在RFE位中。

RFP[1:0]位（接收帧位置）

RFP[1:0]位指示接收帧的哪一部分对应于该描述符中指示的接收缓冲区。

RACT位（接收描述符有效）

RACT位指示该描述符是有效的。RACT位由软件设置为1。当所有数据传输到RD2中指示的接收缓冲区或接收缓冲区已满时，该位清0。

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(2) Receive descriptor 1 (RD1)

Bit	Symbol	Function	R/W
15:0	RFL	Receive Frame Length Specifies the length (number of bytes) of the receive frame stored in the buffer. This does not include the number of bytes for padding set in the RPADIR register. These bits are written back to the descriptor associated with the end of a frame.	R/W
31:16	RBL	Receive Buffer Length Specifies the byte length of the associated receive buffer. Set an integral multiple of 32 as the buffer length.	R/W

Note: Bits for write-back are underlined.

RD1 specifies the receive buffer length. When reception is complete, the receive frame length is written back.

(3) Receive descriptor 2 (RD2)

Bit	Symbol	Function	R/W
31:0	RBA	Receive Buffer Address Specifies the start address of the receive buffer. Align the buffer address on a 32-byte boundary.	R/W

RD2 specifies the start address of the receive buffer.

27.3.2 Transmission

When the EDTRR.TR bit is set to 1 while the ETHERC0.ECMR.TE bit is 1, the EDMAC reads the descriptor following the previously used descriptor in the transmit descriptor list (or the descriptor indicated in the TDLAR register after a reset). When the TACT bit is 1 in the transmit descriptor (TD0), the EDMAC sequentially reads transmit data from the start address of the transmit buffer indicated in transmit descriptor 2 (TD2) and transfers it to the ETHERC through the transmit FIFO. The ETHERC creates a transmit frame and starts transmission to the MII or RMII. When all data indicated in the TD1.TBL bit is transferred, write-back is performed based on the TD0.TFP[1:0] bit setting as follows:

- When the TD0.TFP[1:0] bits are 00b or 10b (frame is incomplete), the TD0.TACT bit is written back
- When the TD0.TFP[1:0] bits are 01b or 11b (frame is complete), the TD0.TACT, TD0.TFS, and TD0.TFE bits are written back.

When the TD0.TACT bit in the read descriptor is 1, the EDMAC continues reading descriptors and transmit frames. When the TD0.TACT bit in the read descriptor is 0, the EDMAC sets the EDTRR.TR bit to 0 and stops transmission.

(2) 接收描述符1(RD1)

Bit	Symbol	Function	R/W
15:0	RFL	接收帧长度 指定存储在缓冲区中的接收帧的长度（字节数）。这不包括RPADIR寄存器中设置的填充字节数。这些位被写回与帧结束相关的描述符。	R/W
31:16	RBL	接收缓冲区长度 指定相关接收缓冲区的字节长度。设置32的整数倍作为缓冲区长度。	R/W

Note: 用于回写的位带有下划线。

RD1指定接收缓冲区长度。当接收完成时，接收帧长度被写回。

(3) 接收描述符2(RD2)

Bit	Symbol	Function	R/W
31:0	RBA	接收缓冲区地址 指定接收缓冲区的起始地址。在32字节边界上对齐缓冲区地址。	R/W

RD2指定接收缓冲区的起始地址。

27.3.2 Transmission

当EDTRR.TR位设置为1而ETHERC0.ECMR.TE位为1时，EDMAC读取发送描述符列表中先前使用的描述符之后的描述符（或复位后TDLAR寄存器中指示的描述符）。当发送描述符(TD0)中的TACT位为1时，EDMAC从发送描述符2(TD2)中指示的发送缓冲区的起始地址顺序读取发送数据，并通过发送FIFO将其传输到ETHERC。ETHERC创建一个传输帧并开始传输到MII或RMII。当所有数据显示在

传输TD1.TBL位，根据TD0.TFP[1:0]位设置执行回写，如下所示：

●当TD0.TFP[1:0]位为00b或10b（帧不完整）时，TD0.TACT位被回写

●当TD0.TFP[1:0]位为01b或11b（帧完成）时，TD0.TACT、TD0.TFS和TD0.TFE位被写回。

当读取描述符中的TD0.TACT位为1时，EDMAC继续读取描述符并发送帧。当读描述符中的TD0.TACT位为0时，EDMAC将EDTRR.TR位设置为0并停止传输。

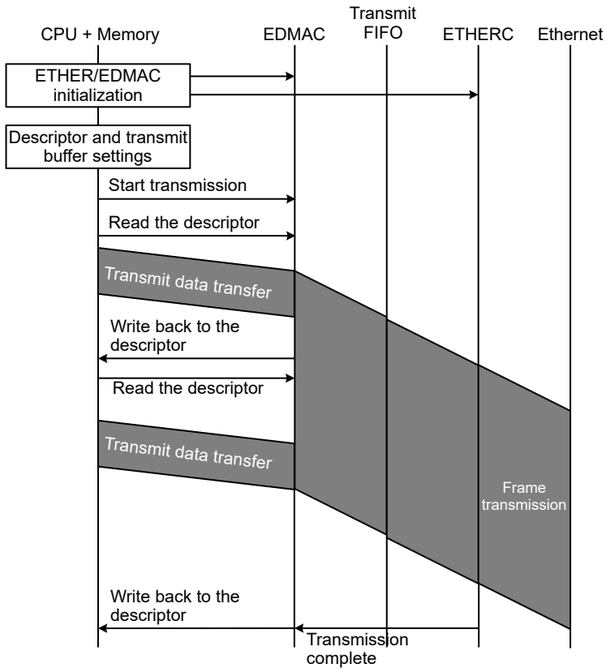

Figure 27.5 Example of transmission flow

27.3.3 Reception

When the EDRRR.RR bit is set to 1 while the ETHERC0.ECMR.RE bit is 1, the EDMAC reads the receive descriptor following the previously used descriptor (or the descriptor indicated in the RDLAR register after a reset) and then waits for reception. When the RD0.RACT bit is 1, if the data stored in the receive FIFO is 32 bytes or more, or if the end byte of the frame is stored in the receive buffer, the EDMAC transfers data from the receive FIFO to the receive buffer indicated in receive descriptor 2 (RD2).

If the data length of the received frame is longer than the buffer length set in the RBL bit in receive descriptor 1 (RD1), the EDMAC writes back 10b or 00b to the RD0.RFP[1:0] bits and 0 to the RD0.RACT bit when the receive buffer becomes full, and then the EDMAC reads the next data. After that, the EDMAC transfers data to another receive buffer.

When the frame reception is complete or when the frame reception is aborted by an error, the EDMAC writes back 11b or 01b to the RD0.RFP[1:0] bits, 0 to the RD0.RACT bit, and the receive frame length to the RD1.RFL bit. When the RMCR.RNR bit is 1, the EDMAC reads the next descriptor and waits for reception. When the RNR bit is 0, the EDMAC sets the EDRRR.RR bit to 0 and stops reception.

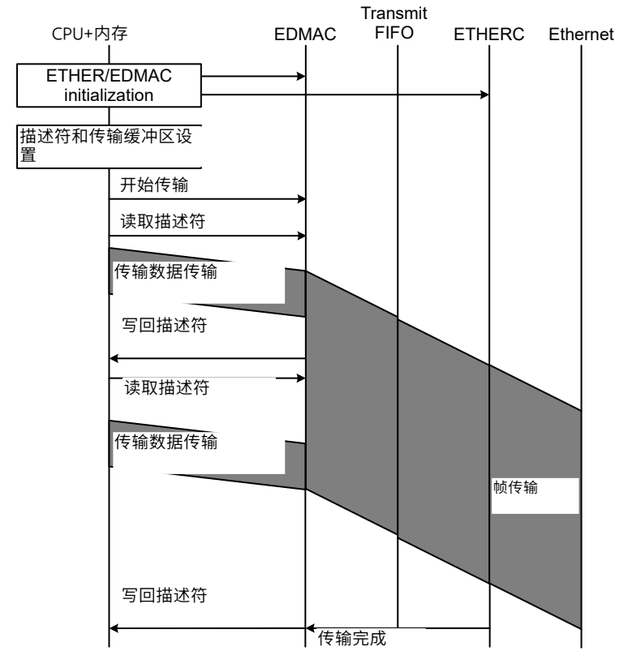

Figure 27.5 传输流程示例

27.3.3 Reception

当EDRRR.RR位设置为1而ETHERC0.ECMR.RE位为1时，EDMAC读取先前使用的描述符（或复位后RDLAR寄存器中指示的描述符）之后的接收描述符，然后等待接收.当RD0.RACT位为1时，如果接收FIFO中存储的数据为32字节或更多，或者如果帧的结束字节存储在接收缓冲区中，则EDMAC将数据从接收FIFO传输到接收缓冲区在接收描述符2(RD2)中指示。

如果接收帧的数据长度大于接收描述符1(RD1)中RBL位中设置的缓冲区长度，则
当接收缓冲器变满时，EDMAC将10b或00b写回RD0.RFP[1:0]位，并将0写回RD0.RACT位，然后EDMAC读取下一个数据。之后，EDMAC将数据传输到另一个接收缓冲区。

当帧接收完成或帧接收因错误而中止时，EDMAC将11b或01b写回RD0.RFP[1:0]位，将0写回RD0.RACT位，并将接收帧长度写入RD1.RFL位。当RMCR.RNR位为1时，EDMAC读取下一个描述符并等待接收。当RNR位为0时，EDMAC将EDRRR.RR位设置为0并停止接收。

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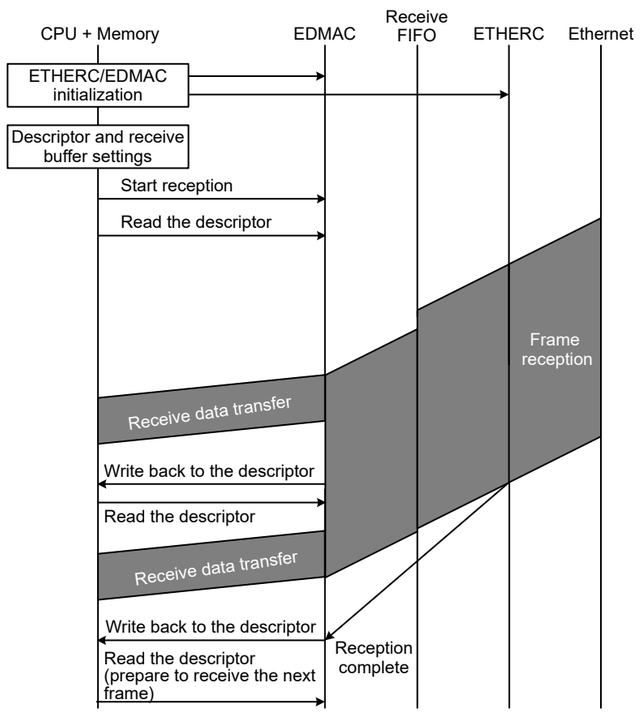

Figure 27.6 Example of reception flow

27.3.4 Multi-Buffer Frame Transmission

27.3.4.1 Error processing while transmitting multi-buffer frame

If an error occurs during multi-buffer frame transmission, the EDMAC performs the processing shown in Figure 27.7. In the figure, when the TACT bit of transmit descriptor 0 (TD0) is 0, the descriptor indicates that all data in the buffer is successfully transmitted. When the TACT bit is 1, the descriptor indicates that data in the buffer is not yet transmitted. If a frame transmit error*1 occurs in the head or at the middle of the frame while the TD0.TACT bit is 1, the EDMAC stops data transmission from the transmit FIFO and EDMAC data transfer, and sets the TD0.TACT bit to 0.

After that, the EDMAC reads the next descriptor to see if the descriptor indicates the middle of the frame (TD0.TFP[1:0] bits are 00b) or the end of the frame (TD0.TFP[1:0] bits are 01b). When the descriptor indicates the middle of the frame, the EDMAC sets the TD0.TACT bit to 0 and reads the next descriptor. When the descriptor indicates the end of the frame, in addition to setting the TD0.TACT bit to 0, the EDMAC also writes back to the TD0.TFE and TD0.TFS bits.

After an error occurs, data in the buffer is not transmitted until write-back to the descriptor for the end of the frame. When the associated transmit error interrupt is enabled in the EESIPR register, an interrupt request is generated immediately after write-back to the descriptor for the end of the frame.

Note 1. A transmit retry-over condition, late collision, or loss of carrier is detected, or a carrier is not detected.

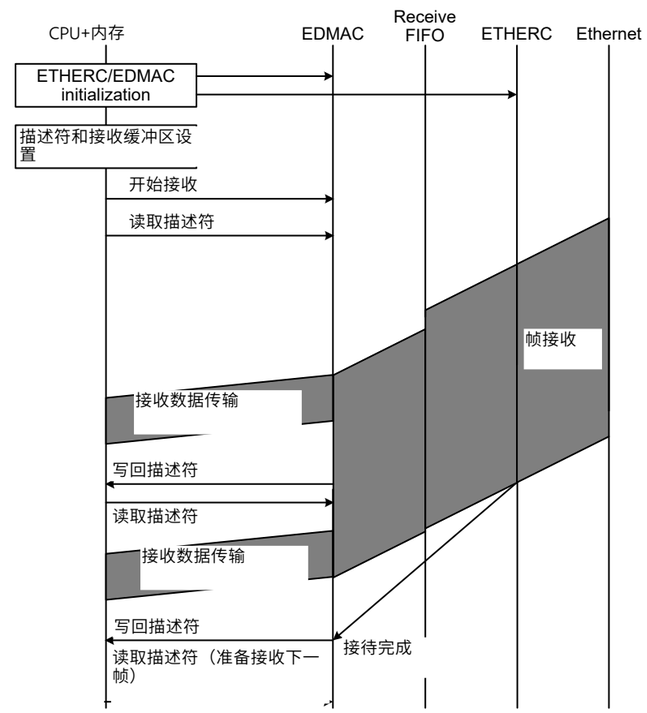

Figure 27.6 接收流程示例

27.3.4 多缓冲区帧传输

27.3.4.1 传输多缓冲帧时的错误处理

如果在多缓冲帧传输过程中发生错误，EDMAC将执行图27.7所示的处理。图中，当发送描述符0（TD0）的TACT位为0时，描述符表示缓冲区中的所有数据都发送成功。当TACT位为1时，描述符指示缓冲区中的数据尚未传输。如果在TD0.TACT位为1时在帧的开头或中间发生帧发送错误*1，则EDMAC停止从发送FIFO和EDMAC数据传输的数据传输，并将TD0.TACT位设置为0.

之后，EDMAC读取下一个描述符，看描述符是表示帧中间（TD0.TFP[1:0]位为00b）还是帧结束（TD0.TFP[1:0]位为01b)。当描述符指示帧的中间时，EDMAC将TD0.TACT位设置为0并读取下一个描述符。当描述符指示帧结束时，除了将TD0.TACT位设置为0外，EDMAC还写回TD0.TFE和TD0.TFS位。

发生错误后，缓冲区中的数据不会传输，直到写回帧结束的描述符。当在ESIPR寄存器中使能相关的发送错误中断时，在帧结束写回描述符后立即生成中断请求。

注1.检测到传输重试条件、延迟冲突或载波丢失，或未检测到载波。

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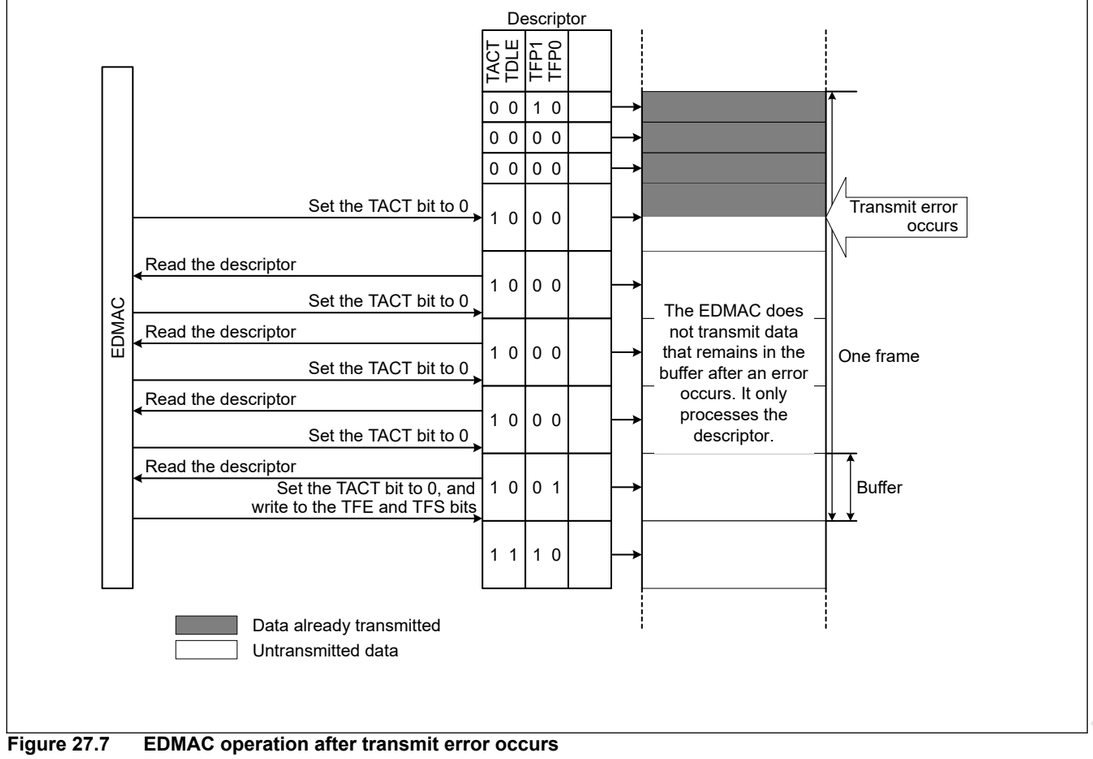

Figure 27.7 EDMAC operation after transmit error occurs

27.3.4.2 Error processing while receiving multi-buffer frame

If an error occurs during multi-buffer frame reception, the EDMAC performs the processing shown in Figure Figure 27.8. In the figure, when the RACT bit of receive descriptor 0 (RD0) is 0, the descriptor indicates that data was successfully received in the buffer. When the RACT bit is 1, the descriptor indicates that data is not yet received in the buffer. If a frame receive error*1 occurs, the EDMAC stops receiving new data, but it transfers data that is already stored in the receive FIFO to the receive buffer.

When the receive buffer becomes full during transfer, the EDMAC sets the RACT bit to 0 and the RFP[1:0] bits to 10b or 00b and reads the next descriptor. After all data in the receive FIFO is transferred, the EDMAC writes back the status to the descriptor.

When the associated receive error interrupt is enabled in the EESIPR register, an interrupt request is generated immediately after write-back to the descriptor. When there is a request to receive a new frame, the EDMAC continues reception using the descriptor following the descriptor where the error occurred.

Note 1. A CRC error, PHY-LSI receive error, frame-too-short error, frame-too-long error, or alignment error is detected.

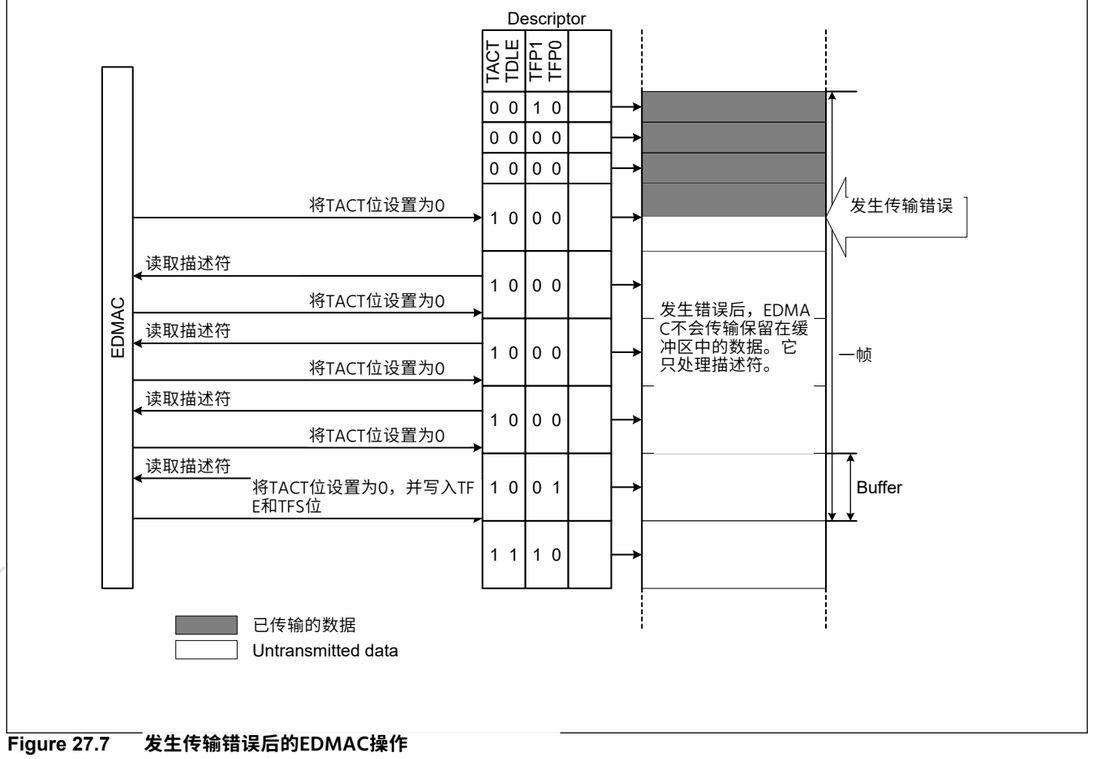

Figure 27.7 发生传输错误后的EDMAC操作

27.3.4.2 接收多缓冲帧时的错误处理

如果在多缓冲区帧接收过程中发生错误，EDMAC将执行图27.8所示的处理。图中，当接收描述符0（RD0）的RACT位为0时，描述符表示缓冲区成功接收到数据。当RACT位为1时，描述符指示缓冲区中尚未接收到数据。如果发生帧接收错误*1，EDMAC将停止接收新数据，但会将已存储在接收FIFO中的数据传输到接收缓冲区。

当接收缓冲区在传输过程中变满时，EDMAC将RACT位设置为0，并将RFP[1:0]位设置为10b或00b并读取下一个描述符。接收FIFO中的所有数据传输完毕后，EDMAC将状态写回描述符。

当在ESIPR寄存器中启用相关的接收错误中断时，在写回描述符后立即生成中断请求。当有接收新帧的请求时，EDMAC使用发生错误的描述符之后的描述符继续接收。

注1.检测到CRC错误、PHY-LSI接收错误、帧太短错误、帧太长错误或对齐错误。

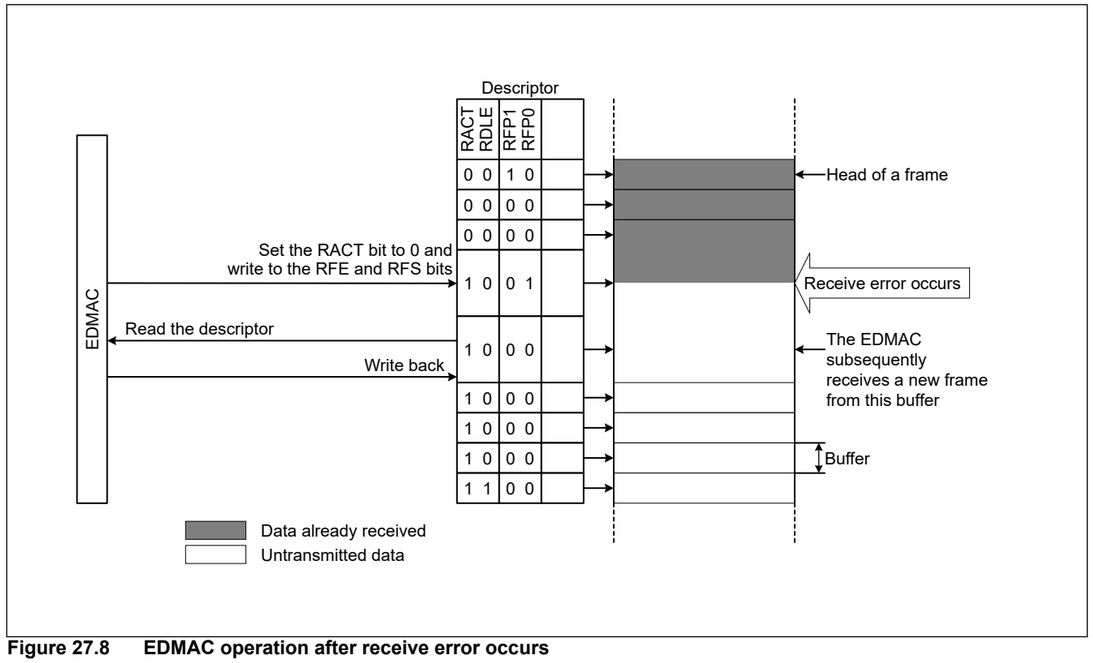

Figure 27.8 EDMAC operation after receive error occurs

27.3.5 Bus Transfer Error

Bus transfer error occurs with the slave TrustZone filter error, the master MPU error, the slave bus error or the illegal address access error. When the bus transfer error is detected, the EDMAC halts the process and EESR.ADE bit is set to 1.

Bus transfer error can be output as an interrupt request signal (ETHER_EINT0). The slave TrustZone error and the master MPU error can be output as NMI. When ETHER_EINT0 and NMI are generated, NMI always responds first. Figure 27.9 and Figure 27.10 show the processing for the bus error in NMI handler and ETHER_EINT0 handler.

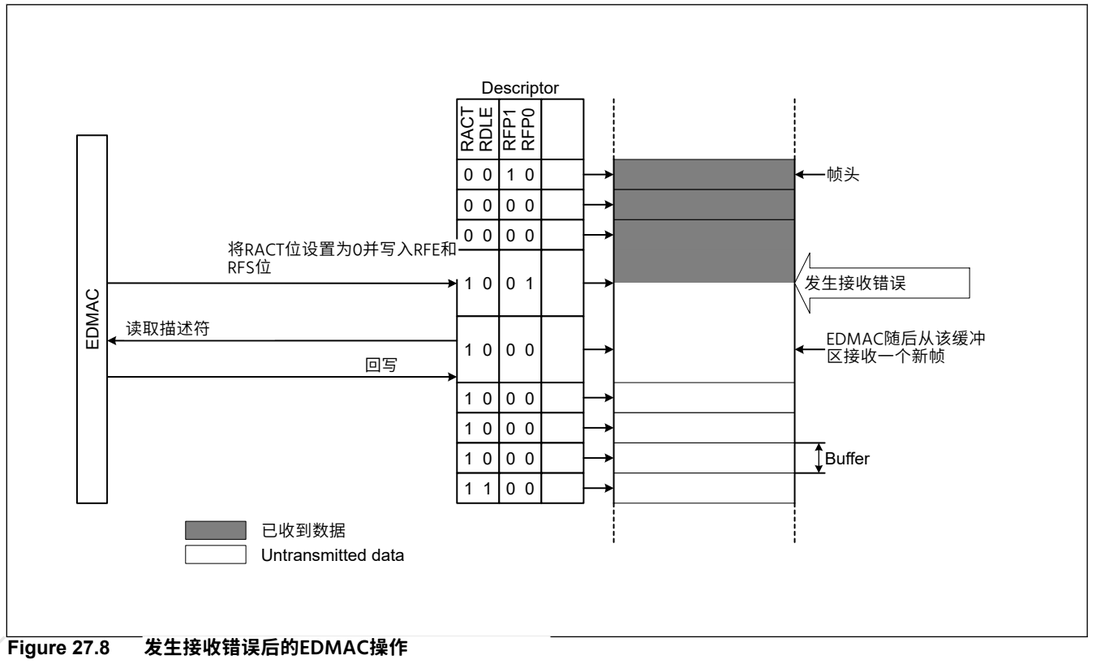

Figure 27.8 发生接收错误后的EDMAC操作

27.3.5 总线传输错误

总线传输错误与从属TrustZone过滤器错误、主控MPU错误、从属总线错误或非法地址访问错误一起发生。当检测到总线传输错误时，EDMAC将停止该过程并将EESR.ADE位设置为1。

总线传输错误可以作为中断请求信号(ETHER_EINT0)输出。从站TrustZone错误和主站MPU错误可以作为NMI输出。当ETHER_EINT0和NMI生成时，NMI总是首先响应。图27.9和图27.10显示了NMI处理程序和ETHER_EINT0处理程序中的总线错误处理。

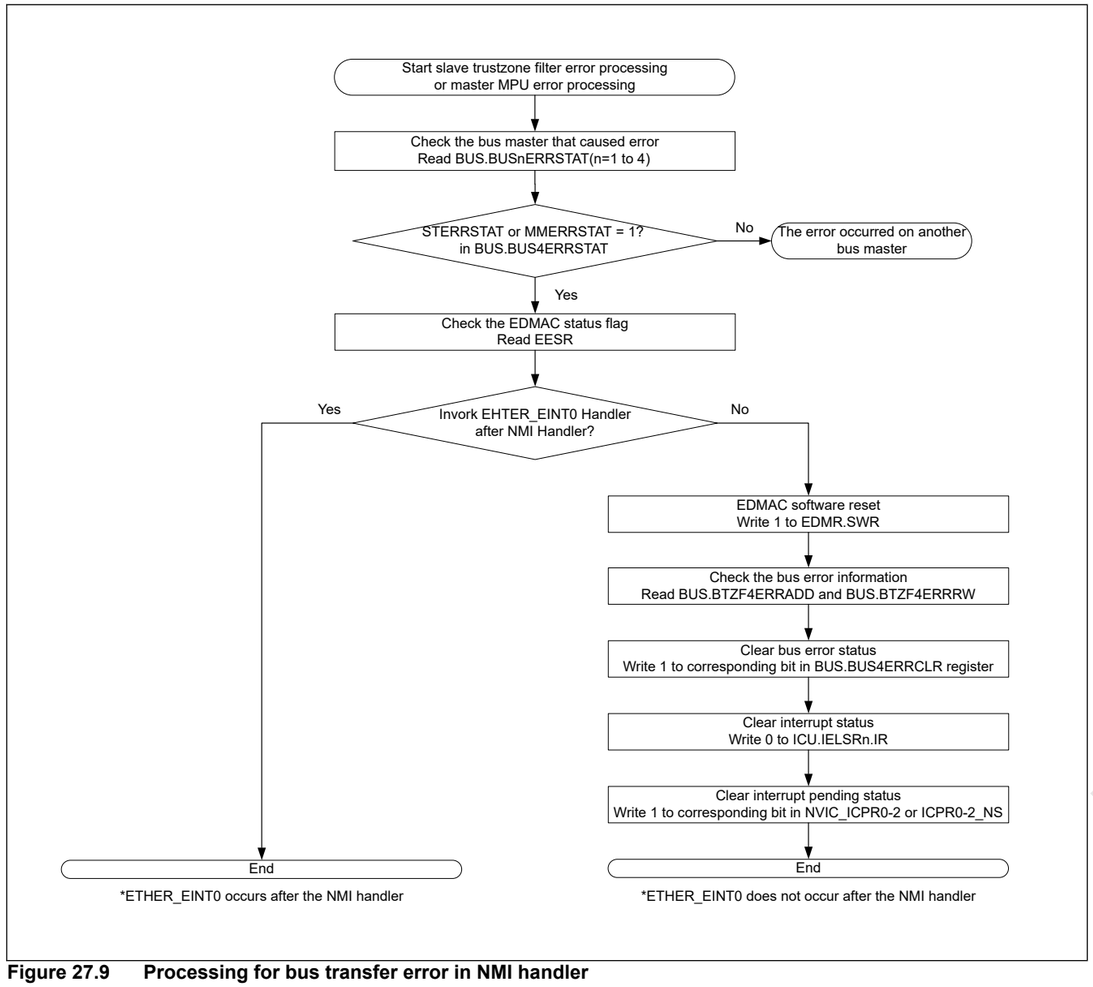

Figure 27.9 Processing for bus transfer error in NMI handler

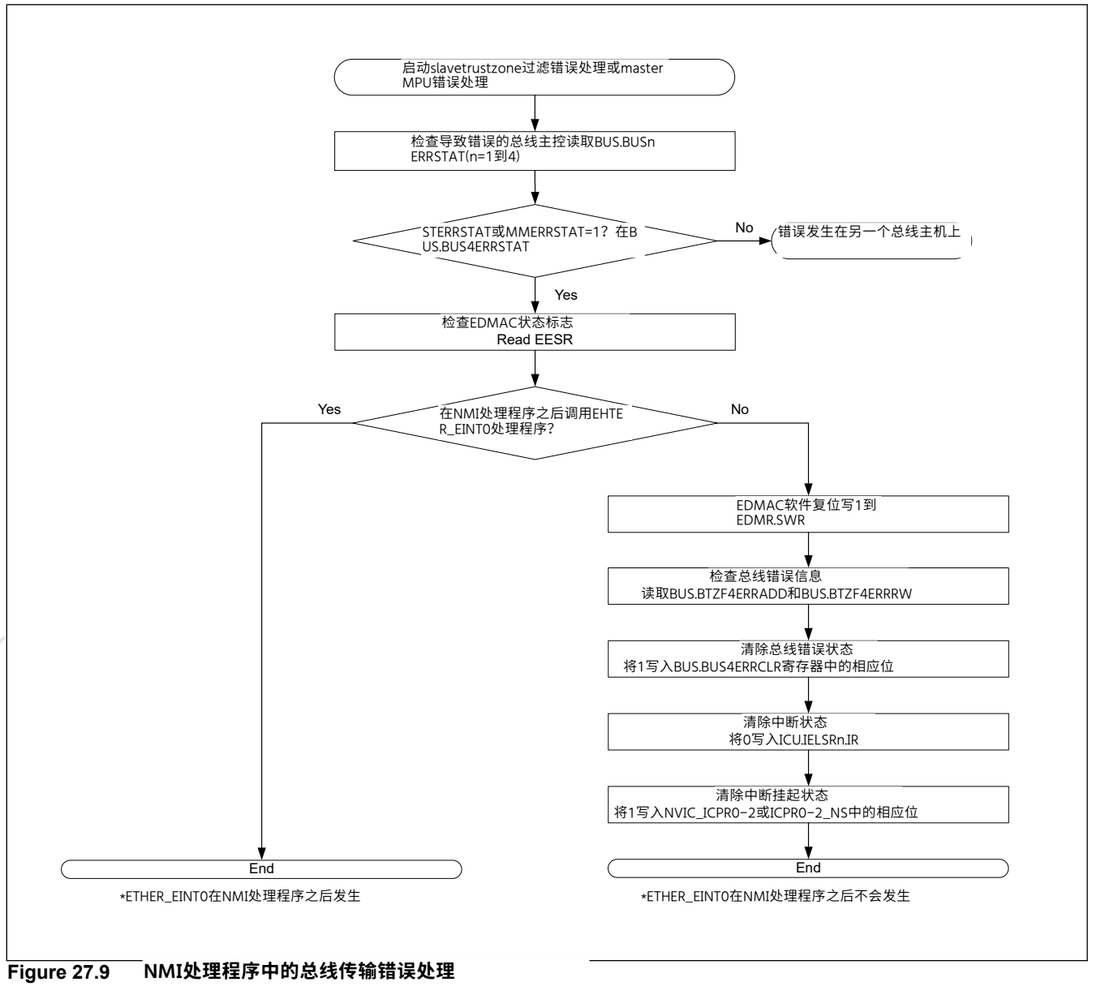

Figure 27.9 NMI处理程序中的总线传输错误处理

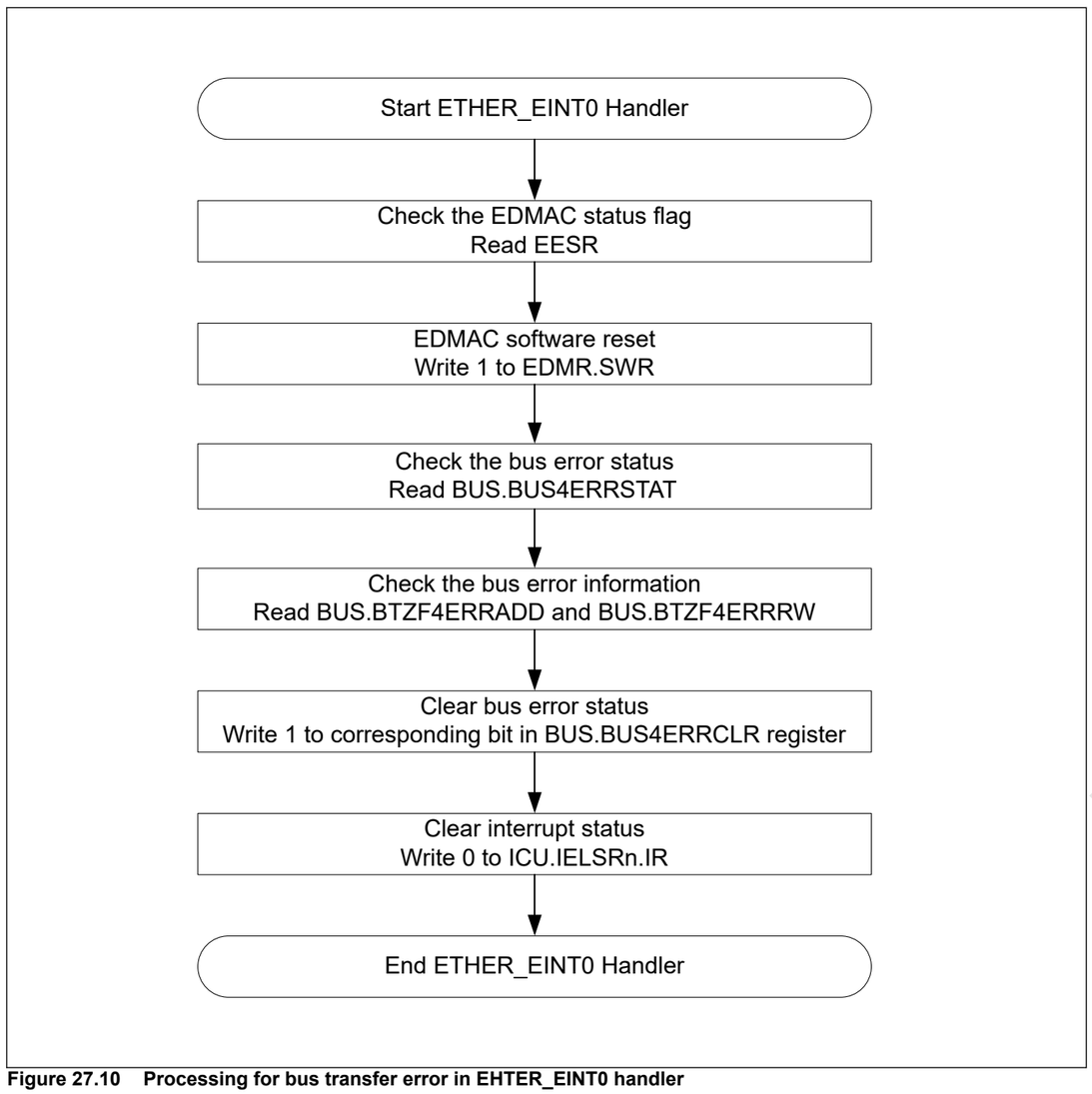

Figure 27.10 Processing for bus transfer error in EHTER_EINT0 handler

27.4 Interrupts

When any of the status flags in the EESR register sets to 1 while the associated interrupt request enable bit in the EESIPR register is 1, EDMAC0 issues an ETHER_EINT0 interrupt request.

27.5 Usage Notes

27.5.1 Settings for the Module-Stop Function

The following bit in Module Stop Control Register B (MSTPCRB) enables or disables EDMAC module operation:

- The MSTPB15 bit in enables or disables ETHERC0 and EDMAC0 operation

The modules are initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

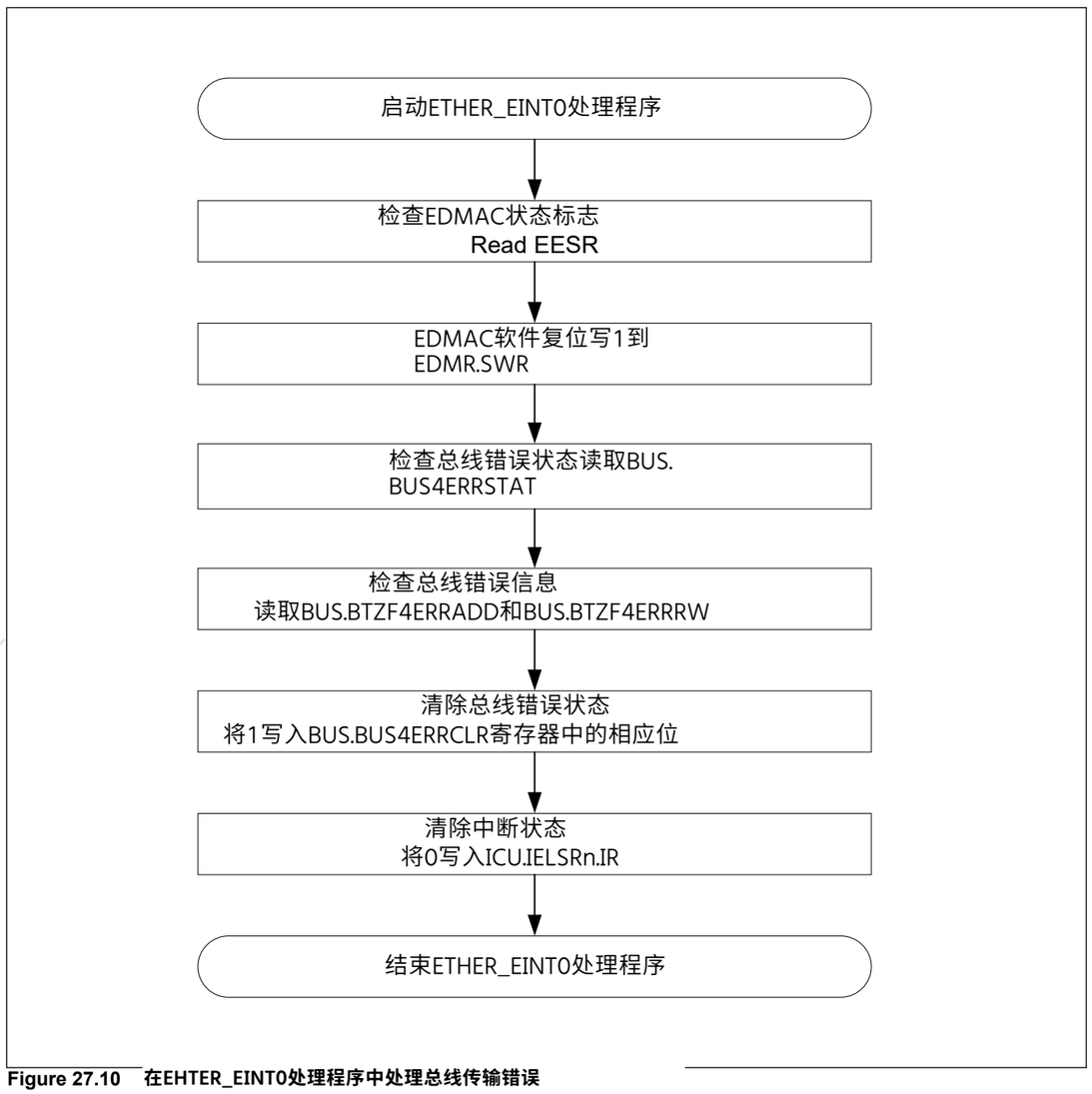

Figure 27.10 在EHTER_EINT0处理程序中处理总线传输错误

27.4 Interrupts

当EESR寄存器中的任何状态标志设置为1且ESIPR寄存器中相关的中断请求使能位为1时，EDMAC0发出ETHER_EINT0中断请求。

27.5 使用说明

27.5.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)中的以下位启用或禁用EDMAC模块操作：

●MSTPB15位启用或禁用ETHERC0和EDMAC0操作

模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

27.5.2 Stopping the EDMAC during Operation

When stopping EDMAC operation by using a Software Standby mode or the module-stop function while the EDMAC is running, confirm that the EDTRR.TR and EDRRR.RR bits are 0. If the EDMAC is stopped while the EDTRR.TR or EDRRR.RR bit is 1, data for the frame that is being transmitted or received might not be complete, and EDMAC operation after exiting Software Standby mode or the module-stop state is not guaranteed.

27.5.2 在运行期间停止EDMAC

在EDMAC运行时使用软件待机模式或模块停止功能停止EDMAC操作时，请确认EDTRR.TR和EDRRR.RR位为0。如果在EDTRR.TR或EDRRR.RR时停止EDMAC位为1，正在发送或接收的帧的数据可能不完整，并且无法保证退出软件待机模式或模块停止状态后的EDMAC操作。

RA生态工作室

28. USB 2.0 Full-Speed Module (USBFS)

28.1 Overview

The USB 2.0 Full-Speed module (USBFS) operates as a host or device controller compliant with the Universal Serial Bus (USB) specification revision 2.0. The host controller supports USB 2.0 full-speed and low-speed transfers, and the device controller supports USB 2.0 full-speed transfers. The USBFS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification

The USBFS has FIFO buffer for data transfers, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or the communication requirements for your system.

Table 28.1 lists the USBFS specifications, Figure 28.1 shows a block diagram, and Table 28.2 lists the I/O pins.

Table 28.1 USBFS specifications

Parameter	Specifications
Features	• USB Device Controller (UDC) and USB 2.0 transceiver supporting host controller, device controller, and On-The-Go (OTG) functions (one channel) • Host and device controller can be switched by software • Self-power or bus power mode selectable • Revision 1.2 of battery charging specification is supported
	Host controller features: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Communications with multiple peripheral devices connected through a single hub
	Device controller features: • Full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation
Supported transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• FIFO buffer for USB communication • Up to 10 pipes selectable, including the Default Control Pipe (DCP) • Pipes 1 to 9 assignable to any endpoint number
	Transfer conditions specifiable for each pipe: • Pipe 0: Control transfer with 64-byte single buffer • Pipes 1 and 2: Selectable to bulk transfer with 64-byte double buffer or isochronous transfer with 256-byte double buffer • Pipes 3 to 5: Bulk transfer with 64-byte double buffer • Pipes 6 to 9: Interrupt transfer with 64-byte single buffer
Other features	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Automatic clearing of the FIFO buffer after the data for the pipe specified in the DnFIFO port (n = 0, 1) is read (DCLRM) • NAK setting function for response PID generated on transfer end (SHTNAK) • On-chip pull-up and pull-down resistors for D+ and D– • Compliance with Battery Charging Class Specification Revision 1.2
Module-stop function	Module-stop state can be set
TrustZone Filter	Security attribution can be set

Note 1. Low-speed transfer (1.5 Mbps) is not supported.

28. USB2.0全速模块(USBFS)

28.1 Overview

USB2.0全速模块(USBFS)作为主机或设备控制器运行，符合通用串行总线(USB)规范修订版2.0。主机控制器支持USB2.0全速和低速传输，设备控制器支持USB2.0全速传输。USBFS具有内部USB收发器并支持USB2.0规范中定义的所有传输类型

USBFS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或系统的通信要求，可以将任何端点编号分配给管道1到9。

表28.1列出了USBFS规范，图28.1显示了框图，表28.2列出了IO引脚。

Table 28.1 USBFS specifications

Parameter	Specifications
Features	• USB设备控制器(UDC)和USB2.0收发器，支持主机控制器、设备控制器和On-The-Go(OTG)功能（一个通道） • 主机和设备控制器可通过软件切换 • 自供电或总线供电模式可选 • 支持电池充电规范1.2版
	主机控制器特点：● 全速传输(12Mbps)和低速传输(1.5Mbps) • SOF和数据包传输的自动调度 • 同步和中断传输的可编程间隔 • 与通过单个集线器连接的多个外围设备进行通信
	设备控制器特点：● 2 Mbps)*1 • 控制转移级控制功能 • 设备状态控制功能 • SET_ADDRESS请求的自动响应功能 • SOF插值
支持的传输类型	• 控制转移 • 批量传输 • 中断传输 • Isochronous transfer
管道配置	• 用于USB通信的FIFO缓冲区 • 最多可选择10个管道，包括默认控制管道(DCP) • 管道1到9可分配给任何端点编号
	可为每根管道指定传输条件：● 管道0：使用64字节单缓冲区进行控制传输 • 管道1和2：可选择使用64字节双缓冲区 进行批量传输或使用256字节双缓冲区 进行同步传输 • 管道3到5：使用64字节双缓冲区 进行批量传输 • 管道6到9：使用64字节单缓冲区的中断传输
其它功能	• 使用事务计数的接收端函数 • 更改BRDY中断事件通知时间(BFRE)的函数 • 读取DnFIFO端口(n=0 1)中指定管道的数据后自动清除FIFO缓冲区(DCLRM) • 传输结束时产生的响应PID的NAK设置功能（SHTNAK） • 用于D+和D 的片上上拉和下拉电阻 • 符合电池充电类规范修订版1.2
Module-stop function	模块停止状态可设置
TrustZone Filter	可设置安全属性

注1.不支持低速传输(1.5Mbps)。

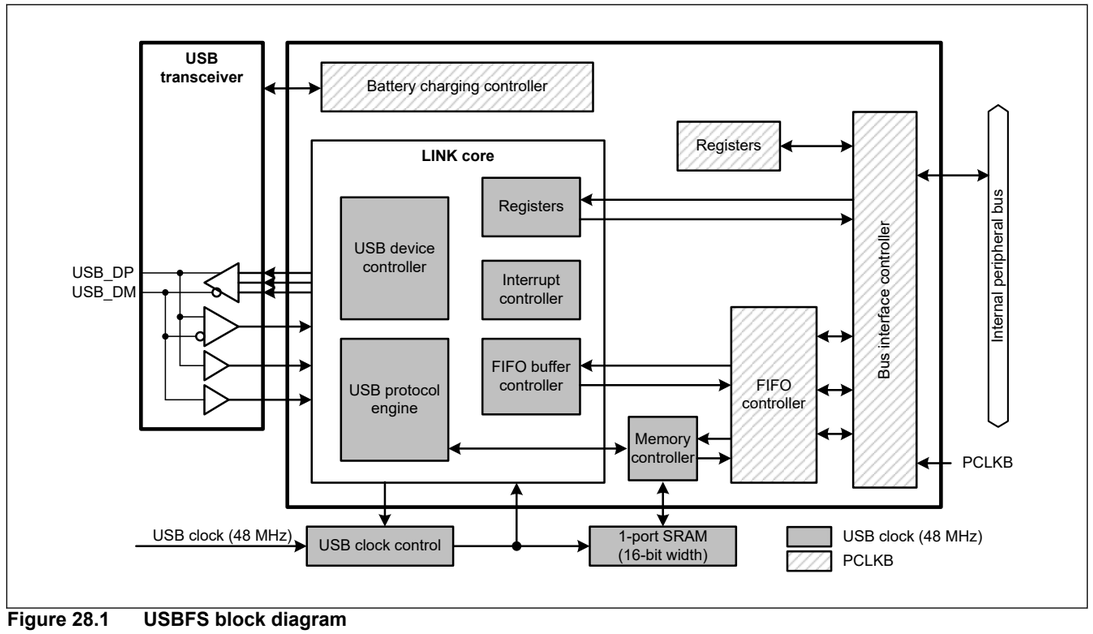

Figure 28.1 USBFS block diagram

Table 28.2 USBFS pin configuration

Functoin	Pin name	I/O	Description
USBFS	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip.
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip.
	USB_OVRCURA, USB_OVRCURB	Input	External overcurrent detection signals should be connected to these pins. VBUS comparator signals should be connected to these pins when the OTG power supply chip is connected.
	USB_ID	Input	MicroAB connector ID input signal should be connected to this pin during operation in OTG mode.
	VCC_USB	Input	Power supply pins.
	VSS_USB	Input	Ground pins.

28.2 Register Descriptions

28.2.1 SYSCFG : System Configuration Control Register

Base address: USBFS = 0x4009_0000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKE	—	—	—	DCFM	DRPD	DPRPU	—	—	—	USBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

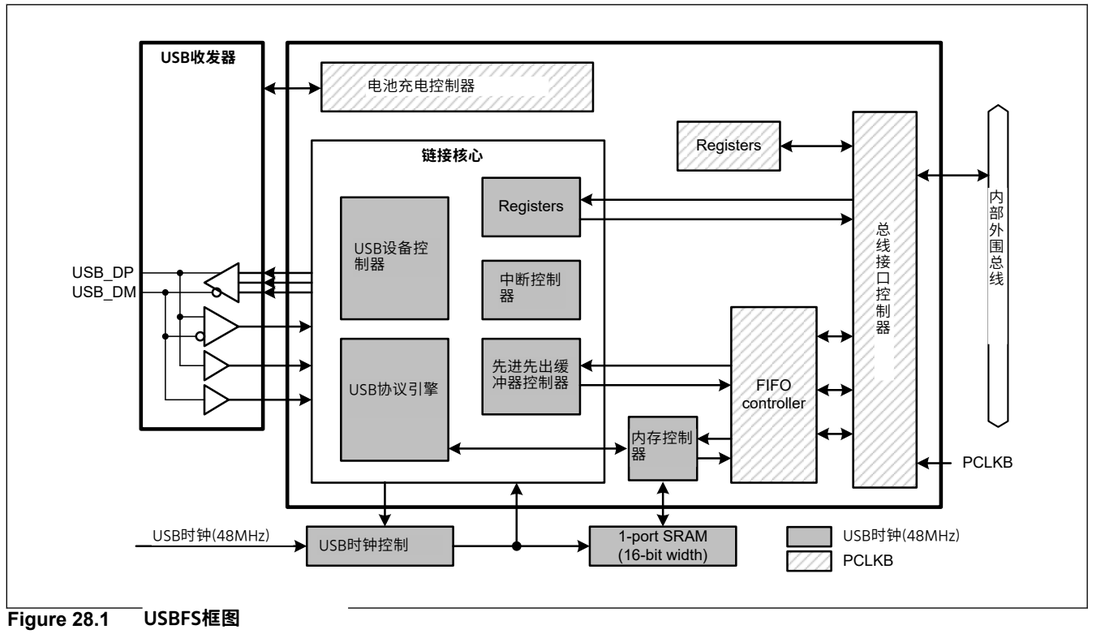

Figure 28.1 USBFS框图

Table 28.2 USBFS引脚配置

Functoin	引脚名称	I/O	Description
USBFS	USB_DP	I/O	USB片上收发器的D+IO引脚。该引脚应连接到USB总线的D+引脚。
	USB_DM	I/O	D USB片上收发器的IO引脚。该引脚应连接到USB总线的D 引脚。
	USB_VBUS	Input	USB电缆连接监视器引脚。该引脚应连接到USB总线的VBUS。当USB模块作为功能控制器运行时，可以检测VBUS引脚状态（连接或断开）。
	USB_EXICEN	Output	用于外部电源(OTG)芯片的低功耗控制信号。
	USB_VBUSEN	Output	VBUS(5V)为外部供电芯片供电使能信号。
	USB_OVRCURA, USB_OVRCURB	Input	外部过流检测信号应连接到这些引脚。连接OTG电源芯片时，应将VBUS比较器信号连接到这些引脚。
	USB_ID	Input	MicroAB连接器ID输入信号应在操作期间连接到此引脚 OTG mode.
	VCC_USB	Input	电源引脚。
	VSS_USB	Input	接地引脚。

28.2 注册说明

28.2.1 SYSCFG：系统配置控制寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKE	—	—	—	DCFM	DRPD	DPRPU	—	—	—	USBE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	USBE	USBFS Operation Enable 0: Disable 1: Enable	R/W
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
4	DPRPU	D+ Line Resistor Control 0: Disable line pull-up 1: Enable line pull-up	R/W
5	DRPD	D+/D– Line Resistor Control 0: Disable line pull-down 1: Enable line pull-down	R/W
6	DCFM	Controller Function Select 0: Select device controller 1: Select host controller	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
9:8	—	These bits are read as 0. The write value should be 0.	R/W
10	SCKE	USB Clock Enable 0: Stop clock supply to the USBFS 1: Enable clock supply to the USBFS	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

Note: After writing 1 to the SCKE bit, read it to confirm that it is set to 1.

USBE bit (USBFS Operation Enable)

The USBE bit enables or disables operation of the USBFS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 28.3. Only change this bit while the SCKE bit is 1. In host controller mode, this bit must be set to 1 after setting the DRPD bit to 1, eliminating SYSSTS0.LNST[1:0] flags chattering, and confirming that the USB bus state is stable.

Table 28.3 Registers initialized by writing 0 to the SYSCFG.USBE bit

Selected function	Register	Bit	Remarks
Device controller	SYSSTS0	LNST[1:0]	Value is saved in host controller mode
	DVSTCTR0	RHST[2:0]	—
	INTSTS0	DVSQ[2:0]	Value is saved in host controller mode
	USBADDR	USBADDR[6:0]	Value is saved in host controller mode
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	Value is saved in host controller mode
	USBVAL	WVALUE[15:0]	Value is saved in host controller mode
	USBINDX	WINDEX[15:0]	Value is saved in host controller mode
	USBLENG	WLENTUH[15:0]	Value is saved in host controller mode
Host controller	DVSTCTR0	RHST[2:0]	—
	FRMNUM	FRNM[10:0]	Value is saved in device controller mode

DPRPU bit (D+ Line Resistor Control)

The DPRPU bit enables or disables pulling up the D+ line in device controller mode.

When the DPRPU bit is set to 1 in device controller mode, the USBFS pulls up the D+ line to notify the USB host that it attached. Changing the DPRPU bit from 1 to 0 releases the pull-up, thereby notifying the USB host that it detached.

Set this bit to 1 in device controller mode and to 0 in host controller mode.

Bit	Symbol	Function	R/W
0	USBE	USBFS操作启用 0：禁用1 ：启用	R/W
2:1	—	这些位被读取为0。写入值应为0。	R/W
3	—	该位读取为0。写入值应为0。	R/W
4	DPRPU	D+线路电阻控制 0：禁用线路上拉1： 启用线路上拉	R/W
5	DRPD	D+D 线路电阻控制 0：禁用线下拉1：启用线 下拉	R/W
6	DCFM	控制器功能选择 0：选择设备控制器1：选 择主机控制器	R/W
7	—	该位读取为0。写入值应为0。	R/W
9:8	—	这些位被读取为0。写入值应为0。	R/W
10	SCKE	USB时钟使能 0：停止向USBFS提供时钟1：使能向U SBFS提供时钟	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W

Note: 将1写入SCKE位后，读取它以确认其设置为1。

USBE位（USBFS操作使能）

USBE位启用或禁用USBFS的操作。

将USBE位从1更改为0会初始化表28.3中列出的位。仅在SCKE位为1时更改该位。在主机控制器模式下，必须在将DRPD位设置为1后将该位设置为1，消除SYSSTS0.LNST[1:0]标志抖动，并确认USB总线状态是稳定的。

Table 28.3 通过向SYSCFG.USBE位写入0来初始化寄存器

所选功能	Register	Bit	Remarks
设备控制器	SYSSTS0	LNST[1:0]	值以主机控制器模式保存
	DVSTCTR0	RHST[2:0]	—
	INTSTS0	DVSQ[2:0]	值以主机控制器模式保存
	USBADDR	USBADDR[6:0]	值以主机控制器模式保存
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	值以主机控制器模式保存
	USBVAL	WVALUE[15:0]	值以主机控制器模式保存
	USBINDX	WINDEX[15:0]	值以主机控制器模式保存
	USBLENG	WLENTUH[15:0]	值以主机控制器模式保存
主机控制器	DVSTCTR0	RHST[2:0]	—
	FRMNUM	FRNM[10:0]	值保存在设备控制器模式中

DPRPU位（D+线路电阻控制）

DPRPU位启用或禁用在设备控制器模式下上拉D+线。

当DPRPU位在设备控制器模式下设置为1时，USBFS拉高D+线以通知USB主机它已连接。将DPRPU位从1更改为0会释放上拉电阻，从而通知USB主机它已分离。

在设备控制器模式下将此位设置为1，在主机控制器模式下设置为0。

DRPD bit (D+/D– Line Resistor Control)

TheDRPD bit enables or disables pulling down D+ and D– lines in host controller mode.

Set this bit to 1 in host controller mode and to 0 in device controller mode.

DCFM bit (Controller Function Select)

The DCFM bit selects the host or device function of the USBFS.

Only change this bit when the DPRPU and DRPD bits are both 0.

SCKE bit (USB Clock Enable)

The SCKE bit stops or enables the 48-MHz clock supply to the USBFS.

When this bit is 0, only SYSCFG is permitted to be read from and written to; the other registers related to the USB should not be read from or written to.

28.2.2 SYSSTS0 : System Configuration Status Register 0

Base address: USBFS = 0x4009_0000

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
Value after reset:	x	x	0	0	0	0	0	0	0	0	0	0	0	x	0	0

Bit	Symbol	Function	R/W
1:0	LNST[1:0]	USB Data Line Status Monitor Indicates the status of the USB data lines, see Table 28.4	R
2	IDMON	External ID0 Input Pin Monitor 0: USB_ID pin is low 1: USB_ID pin is high	R
4:3	—	These bits are read as 0.	R
5	SOFEA	Active Monitor When the Host Controller Is Selected 0: SOF output stopped 1: SOF output operating	R
6	HTACT	USB Host Sequencer Status Monitor 0: Host sequencer completely stopped 1: Host sequencer not completely stopped	R
13:7	—	These bits are read as 0.	R
15:14	OVCMON[1:0]	External USB_OVRCURA/ USB_OVRCURB Input Pin Monitor OVCMON[1] indicates the USB_OVRCURA pin status. OVCMON[0] indicates the USB_OVRCURB pin status.	R

Note: The values of the OVCMON[1:0] and IDMON bits depend on the status of the USB_OVRCURA, USB_OVRCURB, and USB_ID pins.

LNST[1:0] bits (USB Data Line Status Monitor)

The LNST[1:0] bits indicate the state of the USB data lines, D+ and D–. For details, see Table 28.4.

In device controller mode, read the LNST[1:0] bits after connection processing (SYSCFG.DPRPU bit = 1). In host controller mode, read them after enabling pull-down of the lines (SYSCFG.DRPD bit = 1).

Table 28.4 Status of the USB data bus lines (D+ and D–) (1 of 2)

LNST[1:0] bits	During full-speed operation	During low-speed operation
00b	SE0	SE0
01b	J-State	K-State

DRPD位（D+D 线路电阻控制）

DRPD位启用或禁用在主机控制器模式下下拉D+和D 线。

在主机控制器模式下将此位设置为1，在设备控制器模式下设置为0。

DCFM位（控制器功能选择）

DCFM位选择USBFS的主机或设备功能。

仅当DPRPU和DRPD位都为0时更改该位。

SCKE位（USB时钟使能）

SCKE位停止或启用向USBFS提供48MHz时钟。

该位为0时，只允许读写SYSCFG；不应读取或写入与USB相关的其他寄存器。

28.2.2 SYSSTS0：系统配置状态寄存器0

Base address: USBFS = 0x4009_0000

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
重置后的值：	x	x	0	0	0	0	0	0	0	0	0	0	0	x	0	0

Bit	Symbol	Function	R/W
1:0	LNST[1:0]	USB数据线状态监视器 指示USB数据线的状态，见表28.4	R
2	IDMON	外部ID0输入引脚监视器 0：USB_ID引脚为低电平 1：USB_ID引脚为高电平	R
4:3	—	这些位读为0。	R
5	SOFEA	选择主机控制器时的活动监视器 0：SOF输出停止1：SOF输出工作	R
6	HTACT	USB主机定序器状态监视器 0：主机定序器完全停止1：主机定序器未完全停止	R
13:7	—	这些位读为0。	R
15:14	OVCMON[1:0]	外部USB_OVRCURAUSB_OVRCURB输入引脚监视器 OVCMON[1]指示USB_OVRCURA引脚状态。OVCMON[0]表示USB_OVRCURB引脚状态。	R

Note: OVCMON[1:0]和IDMON位的值取决于USB_OVRCURA、USB_OVRCURB和USB_ID引脚的状态。

LNST[1:0]位（USB数据线状态监视器）

LNST[1:0]位指示USB数据线D+和D−的状态。详见表28.4。

在设备控制器模式下，在连接处理后读取LNST[1:0]位（SYSCFG.DPRPU位=1）。在主机控制器模式下，在启用线路下拉后读取它们（SYSCFG.DRPD位=1）。

Table 28.4 USB数据总线的状态（D+和D ）（1of2）

LNST[1:0] bits	全速运行期间	低速运转时
00b	SE0	SE0
01b	J-State	K-State

Table 28.4 Status of the USB data bus lines (D+ and D–) (2 of 2)

LNST[1:0] bits	During full-speed operation	During low-speed operation
10b	K-State	J-State
11b	SE1	SE1

SOFEA bit (Active Monitor When the Host Controller Is Selected)

The SOFEA bit is used in host controller mode to check whether the output of the last SOF is complete when the USBFS is suspended because of a 0 setting to the DVSTCTR0.UACT bit.

In host controller mode, check that both the HTACT and SOFEA bits are 0 before setting the SYSCFG.USBE bit to 0 to stop the USBFS or setting the SYSCFG.SCKE bit to 0 to stop the clock signal supply during communication.

HTACT bit (USB Host Sequencer Status Monitor)

The HTACT bit is set to 0 when the host sequencer of the USBFS is completely stopped.

In host controller mode, check that the HTACT bit is 0 before setting the DVSTCTR0.UACT bit to 0 to place the USBFS in the suspended state or setting the SCKE bit to 0 to stop the clock signal supply during communication.

OVCMON[1:0] bits (External USB_OVRCURA/ USB_OVRCURB Input Pin Monitor)

The OVCMON[1:0] bits indicate the status of the overcurrent signals from an external power supply IC.

28.2.3 DVSTCTR0 : Device State Control Register 0

Base address: USBFS = 0x4009_0000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	RHST[2:0]	USB Bus Reset Status 0 0 0: In host controller mode: Communication speed indeterminate (powered state or no connection) In device controller mode: Communication speed indeterminate 0 0 1: In host controller mode: Low-speed connection In device controller mode: USB bus reset in progress 0 1 0: In host controller mode: Full-speed connection In device controller mode: USB bus reset in progress or full-speed connection 0 1 1: Setting prohibited Others: In host controller mode: USB bus reset in progress In device controller mode: Setting prohibited	R
3	—	These bits are read as 0. The write value should be 0.	R/W
4	UACT	USB Bus Enable 0: Disable downstream port (disable SOF transmission) 1: Enable downstream port (enable SOF transmission)	R/W
5	RESUME	Resume Output 0: Do not output resume signal 1: Output resume signal	R/W
6	USBRST	USB Bus Reset Output 0: Do not output USB bus reset signal 1: Output USB bus reset signal	R/W
7	RWUPE	Wakeup Detection Enable 0: Disable downstream port remote wakeup 1: Enable downstream port remote wakeup	R/W

Table 28.4 USB数据总线的状态（D+和D ）（2之2）

LNST[1:0] bits	全速运行期间	低速运转时
10b	K-State	J-State
11b	SE1	SE1

SOFEA位（选择主机控制器时的主动监视器）

SOFEA位在主机控制器模式下用于检查当USBFS由于DVSTCTR0.UACT位设置为0而暂停时最后一个SOF的输出是否完成。

在主机控制器模式下，在将SYSCFG.USBE位设置为0以停止USBFS或将SYSCFG.SCKE位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT和SOFEA位是否都为0。

HTACT位（USB主机定序器状态监视器）

当USBFS的主机定序器完全停止时，HTACT位设置为0。

在主机控制器模式下，在将DVSTCTR0.UACT位设置为0以将USBFS置于挂起状态或将SCKE位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT位是否为0。

OVCMON[1:0]位（外部USB_OVRCURAUSB_OVRCURB输入引脚监视器）

OVCMON[1:0]位指示来自外部电源IC的过流信号的状态。

28.2.3 DVSTCTR0：设备状态控制寄存器0

Base address: USBFS = 0x4009_0000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	RHST[2:0]	USB总线复位状态 000：在主机控制器模式下：通信速度不确定（通电状态或无连接）在设备控制器模式下：通信速度不确定 001：在主控制器模式下：低速连接 在设备控制器模式下：正在进行USB总线复位 010：在主控制器模式下：全速连接 在设备控制器模式下：USB总线正在复位或全速连接 011：禁止设定 其他：在主机控制器模式下：USB总线复位正在进行中 在设备控制器模式下：禁止设置	R
3	—	这些位被读取为0。写入值应为0。	R/W
4	UACT	USB总线启用 0：禁用下行端口（禁用SOF传输）1：启用下行端口（启用SOF传输）	R/W
5	RESUME	恢复输出 0：不输出恢复信号1：输出恢复信号	R/W
6	USBRST	USB总线复位输出 0：不输出USB总线复位信号1：输出USB总线复位信号	R/W
7	RWUPE	唤醒检测启用 0：禁用下游端口远程唤醒1：启用下游端口远程唤醒	R/W

Bit	Symbol	Function	R/W
8	WKUP	Wakeup Output 0: Do not output remote wakeup signal 1: Output remote wakeup signal	R/W
9	VBUSEN	USB_VBUSEN Output Pin Control 0: Output low on external USB_VBUSEN pin 1: Output high on external USB_VBUSEN pin	R/W
10	EXICEN	USB_EXICEN Output Pin Control 0: Output low on external USB_EXICEN pin 1: Output high on external USB_EXICEN pin	R/W
11	HNPBTOA	Host Negotiation Protocol (HNP) Control Use this bit when switching from device B to device A in OTG mode. If the HNPBTOA bit is 1, the internal function control remains in the Suspend state until the HNP processing ends even if SYSCFG.DPRPU = 0 or SYSCFG.DCFM = 1.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

The USBFS controller does not support low-speed connections in device controller mode. When this value is read, abnormal connection processing must be executed in higher level application software.

RHST[2:0] bits (USB Bus Reset Status)

RHST[2:0] bits indicate the status of the USB bus reset.

In host controller mode, writing 1 to the USBRST bit causes the RHST[2:0] bits to set to 100b. When 0 is written to the USBRST bit and the USBFS ends the SE0 state, the RHST[2:0]bits update to a new value.

In device controller mode, if the USBFS detects a USB bus reset, the RHST[2:0] bits indicate 010b if the DPRPU bit is 1, and a DVST interrupt is generated.

UACT bit (USB Bus Enable)

When set to 1 in host controller mode, the UACT bit enables USB bus operation by controlling SOF packet transmission to the USB bus in addition to data and reception. The USBFS starts SOF packet output within one frame period after the UACT bit is set to 1. When UACT is set to 0, the USBFS enters the idle state after the SOF packet output.

The USBFS sets the UACT bit to 0 on any of the following conditions:

- A DTCH interrupt is detected during communication (when UACT = 1)
- An EOFERR interrupt is detected during communication (when UACT = 1)

Always write 1 to the UACT bit at the end of the USB bus reset processing (writing 0 to the USBRST bit) or at the end of resume processing from the suspended state (writing 0 to the RESUME bit).

In device controller mode, always set this bit to 0.

RESUME bit (Resume Output)

The RESUME bit controls the resume signal output in host controller mode.

When this bit is set to 1, the USBFS drives the USB port to the K-state and outputs the resume signal. The USBFS sets the bit to 1 on detection of a remote wakeup signal while the RWUPE bit is 1 and in the USB Suspend state.

The USBFS continues outputting the K-state while the RESUME bit is 1, until the bit is cleared to 0 by software. The RESUME bit must be 1 (resume period) for the time defined in the USB 2.0 specification. Only set this bit to 1 while the interface is in the Suspend state. Write 1 to the UACT bit simultaneously with the end of the resume processing (writing 0 to the RESUME bit).

Always set this bit to 0 in device controller mode.

USBRST bit (USB Bus Reset Output)

The USBRST bit controls the output of the USB bus signal in host controller mode. When this bit set to 1, the USBFS drives the USB port to the SE0 state to reset the USB bus. The USBFS continues outputting SE0 while the USBRST bit is 1, until the bit is cleared to 0 by software. The USBRST bit must be 1 (USB bus reset period) for the time defined in the USB 2.0 specification. Writing 1 to the USBRST bit during communication (UACT = 1) or during resume processing (RESUME

Bit	Symbol	Function	R/W
8	WKUP	唤醒输出 0：不输出远程唤醒信号1：输出远程唤醒信号	R/W
9	VBUSEN	USB_VBUSEN输出引脚控制 0：外部USB_VBUSEN引脚输出低电平1：外部USB_VBUSEN引脚输出高电平	R/W
10	EXICEN	USB_EXICEN输出引脚控制 0：外部USB_EXICEN引脚输出低电平1：外部USB_EXICEN引脚输出高电平	R/W
11	HNPBTOA	主机协商协议(HNP)控制 在OTG模式下从设备B切换到设备A时使用该位。如果HNPBTOA位为1，即使SYSCFG.DPRPU=0或SYSCFG.DCFM=1，内部功能控制仍保持暂停状态直到HNP处理结束。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W

USBFS控制器不支持设备控制器模式下的低速连接。当读取此值时，必须在更高级别的应用软件中执行异常连接处理。

RHST[2:0]位（USB总线复位状态）

RHST[2:0]位指示USB总线复位的状态。

在主机控制器模式下，将1写入USBRST位会导致RHST[2:0]位设置为100b。当0被写入USBRST位和USBFS结束SE0状态，RHST[2:0]位更新为新值。

在设备控制器模式下，如果USBFS检测到USB总线复位，如果DPRPU位为1，则RHST[2:0]位指示010b，并产生DVST中断。

UACT位（USB总线使能）

在主机控制器模式下设置为1时，UACT位通过控制向USB总线发送SOF数据包以及数据和接收来启用USB总线操作。USBFS在UACT位设置为1后的一帧周期内开始SOF数据包输出。当UACT设置为0时，USBFS在SOF数据包输出后进入空闲状态。

USBFS在以下任何条件下将UACT位设置为0：

●通信期间检测到DTCH中断（当UACT=1时）

●通信期间检测到EOFERR中断（当UACT=1时）

在USB总线复位处理结束（将0写入USBRST位）或从挂起状态恢复处理结束（将0写入RESUME位）时，始终向UACT位写入1。

在设备控制器模式下，始终将此位设置为0。

RESUME位（恢复输出）

RESUME位控制主机控制器模式下的恢复信号输出。

当该位设置为1时，USBFS将USB端口驱动到K状态并输出恢复信号。当RWUPE位为1且处于USB挂起状态时，USBFS在检测到远程唤醒信号时将该位设置为1。

当RESUME位为1时，USBFS继续输出K状态，直到该位被软件清除为0。这在USB2.0规范中定义的时间内，RESUME位必须为1（恢复周期）。仅当接口处于挂起状态时将此位设置为1。在恢复处理结束的同时向UACT位写入1（向RESUME位写入0）。

在设备控制器模式下始终将此位设置为0。

USBRST位（USB总线复位输出）

USBRST位控制主机控制器模式下USB总线信号的输出。当该位设置为1时，USBFS将USB端口驱动到SE0状态以复位USB总线。当USBRST位为1时，USBFS继续输出SE0，直到该位被软件清零。在USB2.0规范中定义的时间内，USBRST位必须为1（USB总线复位周期）。通信期间(UACT=1)或恢复处理期间(RESUME)向USBRST位写入1

= 1) prevents the USBFS from starting USB bus reset processing until both the UACT and RESUME bits become 0. Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (writing 0 to the USBRST bit).

Always set this bit to 0 in device controller mode.

RWUPE bit (Wakeup Detection Enable)

The RWUPE bit enables or disables remote wakeup signals (resume signals) from downstream peripheral devices in host controller mode. When this bit is set to 1, the USBFS detects a remote wakeup signal (K-state for 2.5 µs) from a downstream peripheral device, and performs resume processing, driving the K-state. When the RWUPE bit is set to 0, the USBFS ignores remote wakeup signals (K-states) from peripheral devices connected to the USB port.

Do not stop the internal clock when the RWUPE bit is 1, even in the Suspend state (SYSCFG.SCKE bit must be set to 1).

Always set this bit to 0 in device controller mode.

WKUP bit (Wakeup Output)

The WKUP bit enables or disables remote wakeup signals (resume signals) to the USB bus in device controller mode.

The USBFS controls the output timing of the remote wakeup signals. When this bit is set to 1, the USBFS clears it to 0 after outputting the K-state for 10 ms. The USB 2.0 specification specifies that the USB bus idle state must be kept for 5 ms or longer before a remote wakeup signal is sent. If the USBFS writes 1 to the WKUP bit immediately after detecting the Suspend state, the K-state is output after 2 ms.

Only write 1 to the WKUP bit when the device is in the Suspend state (INTSTS0.DVSQ[2:0] = 1xxb) and the USB host enables the remote wakeup signal (RWUPE = 1). Do not stop the internal clock while this bit is 1, even in the Suspend state (SYSCFG.SCKE bit must be set to 1).

Always set this bit to 0 in host controller mode.

HNPBTOA bit (Host Negotiation Protocol (HNP) Control)

TheHNPBTOA bit is used when switching from device B to device A while in OTG mode.

If the HNPBTOA bit is 1, the internal function control maintains the Suspend state until HNP processing ends, even if the SYSCFG.DPRPU bit is set to 0 or the SYSCFG.DCFM bit is set to 1. Resume interrupts (RESM) are not generated even if a falling edge of D+ is detected.

The HNP processing ends when a host attach event is detected, because of a pull-up by the initiating party, or the HNPBTOA bit is cleared to 0 by software because the HNP processing times out.

28.2.4 CFIFO/CFIFOL : CFIFO Port Register

Base address: USBFS = 0x4009_0000

Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FIFOPORT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FIFOPORT[15:0]*1	FIFO Port Read receive data from the FIFO buffer or write transmit data to the FIFO buffer by accessing these bits	R/W

Note 1. The valid bits depend on the MBW settings (CFIFOSEL.MBW) and BIGEND settings (CFIFOSEL.BIGEND) in the associated port selection register. See Table 28.5 and Table 28.6.

Three FIFO ports are available:

- CFIFO
- D0FIFO
- D1FIFO

=1)防止USBFS开始USB总线复位处理，直到UACT和RESUME位都变为0。在USB总线复位处理结束的同时向UACT位写入1（向USBRST位写入0）。

在设备控制器模式下始终将此位设置为0。

RHUPE位（唤醒检测使能）

在主机控制器模式下，RWUPE位启用或禁用来自下游外围设备的远程唤醒信号（恢复信号）。当该位设置为1时，USBFS检测到来自下游外围设备的远程唤醒信号（K状态持续2.5µs），并执行恢复处理，驱动K状态。当RHUPE位设置为0时，USBFS忽略来自连接到USB端口的外围设备的远程唤醒信号（K状态）。

当RHUPE位为1时不要停止内部时钟，即使处于挂起状态（SYSCFG.SCKE位必须设置为1）。

在设备控制器模式下始终将此位设置为0。

WKUP bit (Wakeup Output)

WKUP位在设备控制器模式下启用或禁用到USB总线的远程唤醒信号（恢复信号）。

USBFS控制远程唤醒信号的输出时序。当该位设置为1时，USBFS在输出K状态10ms后将其清除为0。USB2.0规范规定，在发送远程唤醒信号之前，USB总线空闲状态必须保持5ms或更长时间。如果USBFS在检测到Suspend状态后立即向WKUP位写入1，则在2ms后输出K-state。

仅当设备处于挂起状态（INTSTS0.DVSQ[2:0]=1xxb）且USB主机使能远程唤醒信号（RWUPE=1）时向WKUP位写入1。当该位为1时不要停止内部时钟，即使处于挂起状态（SYSCFG.SCKE位必须设置为1）。

在主机控制器模式下始终将此位设置为0。

HNPBTOA位（主机协商协议(HNP)控制）

在OTG模式下从设备B切换到设备A时使用HNPBTOA位。

如果HNPBTOA位为1，内部功能控制保持暂停状态直到HNP处理结束，即使SYSCFG.DPRPU位设置为0或SYSCFG.DCFM位设置为1。不产生恢复中断(RESM)即使检测到D+的下降沿。

当检测到主机连接事件时，HNP处理结束，因为发起方的上拉，或者
由于HNP处理超时，HNPBTOA位由软件清零。

28.2.4 CFIFOCFIFOL:CFIFO端口寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FIFOPORT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FIFOPORT[15:0]*1	FIFO Port 通过访问这些位从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区	R/W

注1.有效位取决于相关端口选择寄存器中的MBW设置(CFIFOSEL.MBW)和BIGEND设置(CFIFOSEL.BIGEND)。请参见表28.5和表28.6。

三个FIFO端口可用：

- CFIFO
- D0FIFO
- D1FIFO

Each FIFO port is configured with:

- A port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR)

Each FIFO port has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port
- Access to the FIFO buffer for DMA or DTC transfers is through the D0FIO or D1FIFO port
- The D0FIFO and D1FIFO ports can also be accessed by the CPU
- When using functions specific to the FIFO port, such as the DMA or DTC transfer function, you cannot change the pipe number selected in the CURPIPE[3:0] bits of the port selection register
- Registers configuring a FIFO port do not affect other FIFO ports
- The same pipe must not be assigned to two or more FIFO ports
- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU

FIFOPORT[15:0] bits (FIFO Port)

When the FIFOPORT[15:0] bit is accessed, the USBFS reads the received data from the FIFO buffer or writes the transmit data to the FIFO buffer. The FIFO port register can be accessed only when the FRDY bit in the associated port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

The valid bits in the FIFO port register depend on the MBW and BIGEND settings in the port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL). See Table 28.5 and Table 28.6.

Table 28.5 Endian operation in 16-bit access

CFIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 28.6 Endian operation in 8-bit access

CFIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	Access prohibited*1	N + 0 data
1	Access prohibited*1	N + 0 data

Note 1. Writing to or reading from these areas is not allowed.

28.2.5 DnFIFO/DnFIFOL : DnFIFO Port Register (n = 0, 1)

Base address: USBFS = 0x4009_0000

Offset address: 0x018 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FIFOPORT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FIFOPORT[15:0]*1	FIFO Port Read receive data from the FIFO buffer or write transmit data to the FIFO buffer by accessing these bits	R/W

每个FIFO端口配置有：

●一个端口寄存器（CFIFO、D0FIFO或D1FIFO），用于处理从FIFO缓冲区读取数据并将数据写入FIFO缓冲区

●端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL），用于选择分配给FIFO端口的管道

●一个端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）

每个FIFO端口具有以下约束：

●通过CFIFO端口访问DCP控制传输的FIFO缓冲区

●通过D0FIO或D1FIFO端口访问DMA或DTC传输的FIFO缓冲区

●D0FIFO和D1FIFO端口也可以被CPU访问

●当使用特定于FIFO端口的功能时，例如DMA或DTC传输功能，您不能更改在端口选择寄存器的CURPIPE[3:0]位中选择的管道号

●配置FIFO端口的寄存器不会影响其他FIFO端口

●不能将同一管道分配给两个或多个FIFO端口

●有两种FIFO缓冲区状态，一种授予CPU访问权限，另一种授予串行接口引擎(SIE)。当SIE有访问权限时，CPU不能访问FIFO缓冲区

FIFOPORT[15:0] bits (FIFO Port)

当访问FIFOPORT[15:0]位时，USBFS从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。只有当相关端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）中的FRDY位为1时，才能访问FIFO端口寄存器。

FIFO端口寄存器中的有效位取决于端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）中的MBW和BIGEND设置。请参见表28.5和表28.6。

Table 28.5 16位访问中的字节序操作

CFIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 28.6 8位访问中的字节序操作

CFIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	禁止访问*1	N + 0 data
1	禁止访问*1	N + 0 data

注1.不允许对这些区域进行写入或读取。

28.2.5 DnFIFODnFIFOL:DnFIFO端口寄存器(n=0 1)

Base address: USBFS = 0x4009_0000

Offset address: 0x018 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FIFOPORT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	FIFOPORT[15:0]*1	FIFO Port 通过访问这些位从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区	R/W

Note 1. The valid bits depend on the MBW settings (CFIFOSEL.MBW, D0FIFOSEL.MBW, and D1FIFOSEL.MBW) and BIGEND settings (CFIFOSEL.BIGEND, D0FIFOSEL.BIGEND, and D1FIFOSEL.BIGEND) in the associated port selection register. See Table 28.7 and Table 28.8.

Three FIFO ports are available:

- CFIFO
- D0FIFO
- D1FIFO

Each FIFO port is configured with:

- A port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR)

Each FIFO port has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port
- Access to the FIFO buffer for DMA or DTC transfers is through the D0FIO or D1FIFO port
- The D0FIFO and D1FIFO ports can also be accessed by the CPU
- When using functions specific to the FIFO port, such as the DMA or DTC transfer function, you cannot change the pipe number selected in the CURPIPE[3:0] bits of the port selection register
- Registers configuring a FIFO port do not affect other FIFO ports
- The same pipe must not be assigned to two or more FIFO ports
- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU

FIFOPORT[15:0] bits (FIFO Port)

When the FIFOPORT bit is accessed, the USBFS reads the received data from the FIFO buffer or writes the transmit data to the FIFO buffer. The FIFO port register can be accessed only when the FRDY bit in the associated port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

The valid bits in the FIFO port register depend on the MBW and BIGEND settings in the port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL). See Table 28.7 and Table 28.8.

Table 28.7 Endian operation in 16-bit access

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 28.8 Endian operation in 8-bit access

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	Access prohibited*1	N + 0 data
1	Access prohibited*1	N + 0 data

Note 1. Writing to or reading from these areas is not allowed.

注1.有效位取决于相关端口选择寄存器中的MBW设置（CFIFOSEL.MBW、D0FIFOSEL.MBW和D1FIFOSEL.MBW）和BIGEND设置（CFIFOSEL.BIGEND、D0FIFOSEL.BIGEND和D1FIFOSEL.BIGEND）。请参见表28.7和表28.8。

三个FIFO端口可用：

- CFIFO
- D0FIFO
- D1FIFO

每个FIFO端口配置有：

●一个端口寄存器（CFIFO、D0FIFO或D1FIFO），用于处理从FIFO缓冲区读取数据并将数据写入FIFO缓冲区

●端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL），用于选择分配给FIFO端口的管道

●一个端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）

每个FIFO端口具有以下约束：

●通过CFIFO端口访问DCP控制传输的FIFO缓冲区

●通过D0FIO或D1FIFO端口访问DMA或DTC传输的FIFO缓冲区

●D0FIFO和D1FIFO端口也可以被CPU访问

●当使用特定于FIFO端口的功能时，例如DMA或DTC传输功能，您不能更改在端口选择寄存器的CURPIPE[3:0]位中选择的管道号

●配置FIFO端口的寄存器不会影响其他FIFO端口

●不能将同一管道分配给两个或多个FIFO端口

●有两种FIFO缓冲区状态，一种授予CPU访问权限，另一种授予串行接口引擎(SIE)。当SIE有访问权限时，CPU不能访问FIFO缓冲区

FIFOPORT[15:0] bits (FIFO Port)

当访问FIFOPORT位时，USBFS从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。只有当相关端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）中的FRDY位为1时，才能访问FIFO端口寄存器。

FIFO端口寄存器中的有效位取决于端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）中的MBW和BIGEND设置。请参见表28.7和表28.8。

Table 28.7 16位访问中的字节序操作

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 28.8 8位访问中的字节序操作

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	禁止访问*1	N + 0 data
1	禁止访问*1	N + 0 data

注1.不允许对这些区域进行写入或读取。

28.2.6 CFIFOSEL : CFIFO Port Select Register

Base address: USBFS = 0x4009_0000

Offset address: 0x020

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	CFIFO Port Access Pipe Specification 0x0: Default Control Pipe 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3 0x4: Pipe 4 0x5: Pipe 5 0x6: Pipe 6 0x7: Pipe 7 0x8: Pipe 8 0x9: Pipe 9 Others: Setting prohibited	R/W
4	—	This bit is read as 0. The write value should be 0. This bit is read as 0. The write value should be 0.	R/W
5	ISEL	CFIFO Port Access Direction When DCP Is Selected 0: Select reading from the FIFO buffer 1: Select writing to the FIFO buffer	R/W
7:6	—	These bits are read as 0. The write value should be 0. These bits are read as 0. The write value should be 0.	R/W
8	BIGEND	CFIFO Port Endian Control 0: Little endian 1: Big endian	R/W
9	—	This bit is read as 0. The write value should be 0.	R/W
10	MBW	CFIFO Port Access Bit Width 0: 8-bit width 1: 16-bit width	R/W
13:11	—	These bits are read as 0. The write value should be 0.	R/W
14	REW	Buffer Pointer Rewind 0: Do not rewind buffer pointer 1: Rewind buffer pointer	W*1
15	RCNT	Read Count Mode 0: The DTLN[8:0] bits (CFIFOCTR.DTLN[8:0], D0FIFOCTR.DTLN[8:0], D1FIFOCTR.DTLN[8:0]) are cleared when all receive data is read from the CFIFO. In double buffer mode, the DTLN[8:0] value is cleared when all data is read from only a single plane. 1: The DTLN[8:0] bits are decremented each time the receive data is read from the CFIFO.	R/W

Note 1. Only 0 can be read.

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (CFIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number to use for reading or writing data through the CFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

28.2.6 CFIFOSEL:CFIFO端口选择寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x020

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	CFIFO端口访问管道规范 0x0：默认控制管道0x1：管道10x2：管道20x3：管道30x4：管道40x5：管道50x6：管道60x7：管道70x8：管道80x9：管道9 其他：禁止设置	R/W
4	—	该位读取为0。写入值应为0。该位读取为0。写入值应为0。	R/W
5	ISEL	选择DCP时的CFIFO端口访问方向 0：选择从FIFO缓冲区读取1：选择写入FIFO缓冲区	R/W
7:6	—	这些位读取为0。写入值应为0。这些位读取为0。写入值应为0。	R/W
8	BIGEND	CFIFO端口字节序控制 0：小端1：大端	R/W
9	—	该位读取为0。写入值应为0。	R/W
10	MBW	CFIFO端口访问位宽 0: 8-bit width 1: 16-bit width	R/W
13:11	—	这些位被读取为0。写入值应为0。	R/W
14	REW	缓冲区指针倒带 0：不倒回缓冲区指针1：倒回缓冲区指针	W*1
15	RCNT	读取计数模式 0：DTLN[8:0]位（CFIFOCTR.DTLN[8:0]、D0FIFOCTR.DTLN[8:0]、D1FIFOCTR.DTLN[8:0]）在所有接收数据从先进先出。在双缓冲模式下，当仅从单个平面读取所有数据时，清除DTLN[8:0]值。 1：每次从CFIFO读取接收数据时，DTLN[8:0]位递减。	R/W

注1.只能读取0。

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（CFIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过CFIFO端口读取或写入数据的管道编号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

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During FIFO buffer access, even when an attempt is made to change the CURPIPE[3:0] setting, the current access setting is retained until access is complete.

ISEL bit (CFIFO Port Access Direction When DCP Is Selected)

After writing a new value to the ISEL bit with the DCP as the selected pipe, read the ISEL bit to check that the written value agrees with the read value before proceeding to the next process. Set the ISEL and CURPIPE[3:0] bits simultaneously.

MBW bit (CFIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the CFIFO port.

When the selected pipe is receiving, set the CURPIPE[3:0] and MBW bits simultaneously. After a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit to 16-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering, this setting enables re-reading of the currently-read FIFO buffer plane from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

28.2.7 DnFIFOSEL : DnFIFO Port Select Register (n = 0, 1)

Base address: USBFS = 0x4009_0000

Offset address: 0x028 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	FIFO Port Access Pipe Specification 0x0: Default Control Pipe 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3 0x4: Pipe 4 0x5: Pipe 5 0x6: Pipe 6 0x7: Pipe 7 0x8: Pipe 8 0x9: Pipe 9 Others: Setting prohibited	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	BIGEND	FIFO Port Endian Control 0: Little endian 1: Big endian	R/W
9	—	This bit is read as 0. The write value should be 0.	R/W
10	MBW	FIFO Port Access Bit Width 0: 8-bit width 1: 16-bit width	R/W

在FIFO缓冲区访问期间，即使尝试更改CURPIPE[3:0]设置，当前访问设置也会保留，直到访问完成。

ISEL位（选择DCP时的CFIFO端口访问方向）

在以DCP作为选定管道的情况下将新值写入ISEL位后，读取ISEL位以检查写入的值是否与读取的值一致，然后再进行下一个过程。同时设置ISEL和CURPIPE[3:0]位。

MBW位（CFIFO端口访问位宽度）

MBW位指定访问CFIFO端口的位宽。

当所选管道正在接收时，同时设置CURPIPE[3:0]和MBW位。在写入这些位开始从FIFO缓冲区读取数据后，在读取所有数据之前不要更改这些位。

当所选管道正在传输时，位宽不能从8位更改为16位，同时数据正在写入FIFO缓冲区。

即使选择了16位宽度，也可以通过字节访问控制写入奇数个字节。

REW位（缓冲区指针倒带）

REW位指定是否倒回缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在双缓冲中，此设置允许从第一个条目重新读取当前读取的FIFO缓冲区平面。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将REW位设置为1之前，请务必检查FRDY位是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

28.2.7 DnFIFOSEL:DnFIFO端口选择寄存器(n=0 1)

Base address: USBFS = 0x4009_0000

Offset address: 0x028 + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	FIFO端口访问管道规范 0x0：默认控制管道0x1：管道10x2：管道20x3：管道30x4：管道40x5：管道50x6：管道60x7：管道70x8：管道80x9：管道9 其他：禁止设置	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	BIGEND	FIFO端口字节序控制 0：小端1：大端	R/W
9	—	该位读取为0。写入值应为0。	R/W
10	MBW	FIFO端口访问位宽 0: 8-bit width 1: 16-bit width	R/W

Bit	Symbol	Function	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
12	DREQE	DMA/DTC Transfer Request Enable 0: Disable DMA/DTC transfer request 1: Enable DMA/DTC transfer request	R/W
13	DCLRM	Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read 0: Disable auto buffer clear mode 1: Enable auto buffer clear mode	R/W
14	REW	Buffer Pointer Rewind 0: Do not rewind buffer pointer 1: Rewind buffer pointer	W
15	RCNT	Read Count Mode 0: Clear DTLN[8:0] bits in (CFIFOCTR.DTLN[8:0], D0FIFOCTR.DTLN[8:0], D1FIFOCTR.DTLN[8:0]) when all receive data is read from DnFIFO (after read of a single plane in double buffer mode) 1: Decrement DTLN[8:0] bits each time receive data is read from DnFIFO	R/W

The same pipe must not be specified in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected. The pipe number must not be changed while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number to use for reading or writing data through the DnFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, even when an attempt is made to change the CURPIPE[3:0] setting, the current access setting is retained until access is complete.

MBW bit (FIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the DnFIFO port.

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. Set the CURPIPE[3:0] and MBW bits simultaneously.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit to 16-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

DREQE bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. To enable DMA or DTC transfer requests, set this bit to 1 after setting the CURPIPE[3:0] bits. To change the CURPIPE[3:0] setting, first set this bit to 0.

DCLRM bit (Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read)

The DCLRM bit enables or disables automatic FIFO buffer clearing after data in the selected pipe is read.

When this bit is set to 1, on receiving a zero-length packet while the FIFO buffer assigned to the selected pipe is empty, or when reading of a received short packet is complete while the PIPECFG.BFRE bit is 1, the USBFS sets the BCLR bit in the FIFO port control register to 1.

When using the USBFS with the SOFCFG.BRDYM bit set to 1, set this bit to 0.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering, this setting enables re-reading of the currently-read FIFO buffer plane from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the bit to 1, be sure to check that the FRDY bit is 1.

Bit	Symbol	Function	R/W
11	—	该位读取为0。写入值应为0。	R/W
12	DREQE	DMADTC传输请求启用 0：禁用DMADTC传输请求1：启用DM ADTC传输请求	R/W
13	DCLRM	读取指定管道数据后访问的自动缓冲存储器清除模式 0：禁用自动缓冲区清除模式1： 启用自动缓冲区清除模式	R/W
14	REW	缓冲区指针倒带 0：不倒回缓冲区指针1：倒回 缓冲区指针	W
15	RCNT	读取计数模式 0：清除（CFIFOCTR.DTLN[8:0]、D0FIFOCTR.DTLN[8:0]、D1FIFOCTR.DTLN[8:0])当从DnFIFO中读取所有接收数据时（在双缓冲模式下读取单个平面后） 1：每次从DnFIFO读取接收数据时，递减DTLN[8:0]位	R/W

不能在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。启用DMA或DTC传输时，不得更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过DnFIFO端口读取或写入数据的管道编号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，即使尝试更改CURPIPE[3:0]设置，当前访问设置也会保留，直到访问完成。

MBW位（FIFO端口访问位宽度）

MBW位指定访问DnFIFO端口的位宽。

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。同时设置CURPIPE[3:0]和MBW位。

当所选管道正在传输时，位宽不能从8位更改为16位，同时数据正在写入FIFO缓冲区。

即使选择了16位宽度，也可以通过字节访问控制写入奇数个字节。

DREQE位（DMADTC传输请求使能）

DREQE位启用或禁用DMA或DTC传输请求的发出。要启用DMA或DTC传输请求，请在设置CURPIPE[3:0]位后将此位设置为1。要更改CURPIPE[3:0]设置，首先将该位设置为0。

DCLRM位（读取指定管道数据后访问的自动缓冲存储器清除模式）

在读取所选管道中的数据后，DCLRM位启用或禁用自动FIFO缓冲区清除。

当该位设置为1时，在分配给所选管道的FIFO缓冲区为空时接收到零长度数据包，或在PIPECFG.BFRE位为1时完成读取接收到的短数据包时，USBFS设置FIFO端口控制寄存器中的BCLR位为1。

当使用SOFCFG.BRDYM位设置为1的USBFS时，将此位设置为0。

REW位（缓冲区指针倒带）

REW位指定是否倒回缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在双缓冲中，此设置允许从第一个条目重新读取当前读取的FIFO缓冲区平面。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将该位设置为1之前，请务必检查FRDY位是否为1。

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

The RCNT bit specifies the read mode for the value in the CFIFOCTR.DTLN bit. When accessing DnFIFO with the PIPECFG.BFRE bit set to 1, set the RCNT bit to 0.

28.2.8 CFIFOCTR : CFIFO Port Control Register

Base address: USBFS = 0x4009_0000

Offset address: 0x022

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DTLN[8:0]	Receive Data Length Indicates the receive data length. The meaning of the values differs depending on the RCNT bit setting in the port select register. For details, see the description of the DTLN[8:0] bits.	R
12:9	—	These bits are read as 0. The write value should be 0.	R/W
13	FRDY	FIFO Port Ready 0: FIFO port access disabled 1: FIFO port access enabled	R
14	BCLR	CPU Buffer Clear 0: No operation 1: Clear FIFO buffer on the CPU side	W
15	BVAL	Buffer Memory Valid Flag 0: Invalid (writing 0 has no effect) 1: Writing ended	R/W

The CFIFOCTR, D0FIFOCTR, and D1FIFOCTR registers correspond to the CFIFO, D0FIFO, and D1FIFO buffers.

DTLN[8:0] bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the receive data.

While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the DnFIFOSEL.RCNT bit (n = 0, 1), as follows:

- RCNT = 0

  The USBFS sets the DTLN[8:0] bits to indicate the length of the receive data until the CPU or DMA/DTC has read all of the received data from a single FIFO buffer plane.

  While the PIPECFG.BFRE bit = 1, the USBFS retains the length of the receive data until the BCLR bit is set to 1, even after all the data is read.

- RCNT = 1

  The USBFS decrements the value indicated in the DTLN[8:0] bits each time data is read from the FIFO buffer. The value is decremented by 1 when MBW = 0, and by 2 when MBW = 1.

  The USBFS sets these bits to 0 when all the data is read from one FIFO buffer plane. In double buffer mode, if data is received in one FIFO buffer plane before all of the data is read from the other plane, the USBFS sets these bits to indicate the length of the receive data in the former plane when all of the data is read from the latter plane.

FRDY bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU or DMA/DTC.

In the following cases, the USBFS sets the FRDY bit to 1 but data cannot be read through the FIFO port because there is no data to be read:

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

RCNT位指定CFIFOCTR.DTLN位中值的读取模式。当使用DnFIFO访问PIPECFG.BFRE位设置为1，将RCNT位设置为0。

28.2.8 CFIFOCTR:CFIFO端口控制寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x022

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DTLN[8:0]	接收数据长度 表示接收数据长度。 这些值的含义因端口选择寄存器中的RCNT位设置而异。有关详细信息，请参见DTLN[8:0]位的说明。	R
12:9	—	这些位被读取为0。写入值应为0。	R/W
13	FRDY	FIFO端口就绪 0：禁止FIFO端口访问1：使能FIFO端口访问	R
14	BCLR	CPU缓冲区清除 0：无操作1：清除CPU端的FIFO缓冲区	W
15	BVAL	缓冲存储器有效标志 0：无效（写入0无效）1：写入结束	R/W

CFIFOCTR、D0FIFOCTR和D1FIFOCTR寄存器对应于CFIFO、D0FIFO和D1FIFO缓冲区。

DTLN[8:0]位（接收数据长度）

DTLN[8:0]位指示接收数据的长度。

在读取FIFO缓冲区时，DTLN[8:0]位指示不同的值，具体取决于DnFIFOSEL.RCNT位(n=0 1)，如下所示：

- RCNT = 0

  USBFS设置DTLN[8:0]位以指示接收数据的长度，直到CPU或DMADTC从单个FIFO缓冲区平面读取所有接收数据。

  当PIPECFG.BFRE位=1时，USBFS将保留接收数据的长度，直到BCLR位设置为1，即使在读取所有数据之后也是如此。

- RCNT = 1

  每次从FIFO缓冲区读取数据时，USBFS都会递减DTLN[8:0]位中指示的值。当MBW=0时该值减1，当MBW=1时该值减2。

  当从一个FIFO缓冲平面读取所有数据时，USBFS将这些位设置为0。在双缓冲模式下，如果在一个FIFO缓冲平面中的数据在从另一个平面读取所有数据之前接收到数据，则USBFS设置这些位以指示在读取所有数据时在前一个平面中接收数据的长度从后一个平面。

FRDY位（FIFO端口就绪）

FRDY位指示FIFO端口是否可以被CPU或DMADTC访问。

在以下情况下，USBFS将FRDY位设置为1，但由于没有数据可读取，因此无法通过FIFO端口读取数据：

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit = 1

In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer on the CPU side for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBFS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBFS to clear the FIFO buffer regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is transmitting, if 1 is written to the BVAL flag and the BCLR bit simultaneously, the USBFS clears the data that is already written, enabling transmission of a zero-length packet.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY bit in the FIFO port control register is 1 (set by the USBFS).

BVAL flag (Buffer Memory Valid Flag)

Set the BVAL flag to 1 when data is completely written to the FIFO buffer on the CPU side for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set this flag to 1 in the following cases:

- To transmit a short packet, set this flag to 1 after data is written
- To transmit a zero-length packet, set this flag to 1 before data is written to the FIFO buffer

The USBFS then switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

When data of the maximum packet size is written for the pipe in continuous transfer mode, the USBFS sets the BVAL flag to 1 and switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBFS). When the selected pipe is receiving, do not set the BVAL flag to 1.

28.2.9 DnFIFOCTR : DnFIFO Port Control Register (n = 0, 1)

Base address: USBFS = 0x4009_0000

Offset address: 0x02A + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DTLN[8:0]	Receive Data Length Indicates the receive data length. The meaning of the values differs depending on the RCNT bit setting in the port select register. For details, see the description of the DTLN[8:0] bits.	R
12:9	—	These bits are read as 0. The write value should be 0.	R/W
13	FRDY	FIFO Port Ready 0: FIFO port access disabled 1: FIFO port access enabled	R
14	BCLR	CPU Buffer Clear 0: No operation 1: Clear FIFO buffer on the CPU side	R/W*1

●当分配给所选管道的FIFO缓冲区为空时，接收到一个长度为零的数据包

●PIPECFG.BFRE位=1时接收到一个短数据包并完全读取数据

在这些情况下，将BCLR位设置为1以清除FIFO缓冲区，并启用下一个数据的发送和接收。

BCLR位（CPU缓冲区清除）

将BCLR位设置为1以清除所选管道的CPU端的FIFO缓冲区。

当分配给所选管道的FIFO缓冲区设置为双缓冲区模式时，USBFS仅清除
即使两个平面都已启用读取，也有FIFO缓冲区。

当DCP为选定管道时，将BCLR位设置为1允许USBFS清除FIFO缓冲区，而不管CPU或SIE是否具有访问权限。要在SIE具有访问权限时清除缓冲区，请将DCPCTR.PID[1:0]位设置为00b（NAK响应），然后再将BCLR位设置为1。

当所选管道正在传输时，如果同时向BVAL标志和BCLR位写入1，则USBFS会清除已写入的数据，从而可以传输零长度数据包。

当所选管道不是DCP时，仅在FIFO端口控制寄存器中的frdy位为1（由USBF设置）时，仅将1个写入BCLR位。

BVAL标志（缓冲存储器有效标志）

当数据完全写入CPU端的FIFO缓冲区时，将BVAL标志设置为1，用于在
CURPIPE[3:0].

当所选管道正在传输时，在以下情况下将此标志设置为1：

●要发送一个短包，在数据写入后将此标志设置为1

●要发送零长度数据包，请在数据写入FIFO缓冲区之前将此标志设置为1

然后USBFS将FIFO缓冲区从CPU端切换到SIE端，从而启用传输。

当在连续传输模式下为管道写入最大数据包大小的数据时，USBFS将BVAL标志设置为1，并将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

仅在FRDY位为1（由USBFS设置）时将1写入BVAL标志。当所选管道正在接收时，不要将BVAL标志设置为1。

28.2.9 DnFIFOCTR:DnFIFO端口控制寄存器(n=0 1)

Base address: USBFS = 0x4009_0000

Offset address: 0x02A + 0x4 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DTLN[8:0]	接收数据长度 表示接收数据长度。 这些值的含义因端口选择寄存器中的RCNT位设置而异。有关详细信息，请参见DTLN[8:0]位的说明。	R
12:9	—	这些位被读取为0。写入值应为0。	R/W
13	FRDY	FIFO端口就绪 0：禁止FIFO端口访问1：使能FIFO端口访问	R
14	BCLR	CPU缓冲区清除 0：无操作1：清除CPU端的FIFO缓冲区	R/W*1

Bit	Symbol	Function	R/W
15	BVAL	Buffer Memory Valid Flag 0: Invalid (writing 0 has no effect) 1: Writing ended	R/W

Note 1. Only 0 can be read.

The CFIFOCTR, D0FIFOCTR, and D1FIFOCTR registers correspond to the CFIFO, D0FIFO, and D1FIFO buffers.

DTLN[8:0] bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the receive data.

While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the DnFIFOSEL.RCNT bit (n = 0, 1), as follows:

- RCNT = 0

  The USBFS sets the DTLN[8:0] bits to indicate the length of the receive data until the CPU or DMA/DTC has read all of the received data from a single FIFO buffer plane.

  While the PIPECFG.BFRE bit = 1, the USBFS retains the length of the receive data until the BCLR bit is set to 1, even after all the data is read.

- RCNT = 1

  The USBFS decrements the value indicated in the DTLN[8:0] bits each time data is read from the FIFO buffer. The value is decremented by 1 when MBW = 0, and by 2 when MBW = 1.

  The USBFS sets these bits to 0 when all the data is read from one FIFO buffer plane. In double buffer mode, if data is received in one FIFO buffer plane before all of the data is read from the other plane, the USBFS sets these bits to indicate the length of the receive data in the former plane when all of the data is read from the latter plane.

FRDY bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU or DMA/DTC.

In the following cases, the USBFS sets the FRDY bit to 1 but data cannot be read through the FIFO port because there is no data to be read:

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit = 1

In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer on the CPU side for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBFS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBFS to clear the FIFO buffer regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is transmitting, if 1 is written to the BVAL flag and the BCLR bit simultaneously, the USBFS clears the data that is already written, enabling transmission of a zero-length packet.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY bit in the FIFO port control register is 1 (set by the USBFS).

BVAL flag (Buffer Memory Valid Flag)

Set the BVAL flag to 1 when data is completely written to the FIFO buffer on the CPU side for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set this flag to 1 in the following cases:

- To transmit a short packet, set this flag to 1 after data is written

Bit	Symbol	Function	R/W
15	BVAL	缓冲存储器有效标志 0：无效（写入0无效）1：写入结束	R/W

注1.只能读取0。

CFIFOCTR、D0FIFOCTR和D1FIFOCTR寄存器对应于CFIFO、D0FIFO和D1FIFO缓冲区。

DTLN[8:0]位（接收数据长度）

DTLN[8:0]位指示接收数据的长度。

在读取FIFO缓冲区时，DTLN[8:0]位指示不同的值，具体取决于DnFIFOSEL.RCNT位(n=0 1)，如下所示：

- RCNT = 0

  USBFS设置DTLN[8:0]位以指示接收数据的长度，直到CPU或DMADTC从单个FIFO缓冲区平面读取所有接收数据。

  当PIPECFG.BFRE位=1时，USBFS将保留接收数据的长度，直到BCLR位设置为1，即使在读取所有数据之后也是如此。

- RCNT = 1

  每次从FIFO缓冲区读取数据时，USBFS都会递减DTLN[8:0]位中指示的值。当MBW=0时该值减1，当MBW =1时该值减2。

  当从一个FIFO缓冲平面读取所有数据时，USBFS将这些位设置为0。在双缓冲模式下，如果在一个FIFO缓冲平面中的数据在从另一个平面读取所有数据之前接收到数据，则USBFS设置这些位以指示在读取所有数据时在前一个平面中接收数据的长度从后一个平面。

FRDY位（FIFO端口就绪）

FRDY位指示FIFO端口是否可以被CPU或DMADTC访问。

在以下情况下，USBFS将FRDY位设置为1，但由于没有数据可读取，因此无法通过FIFO端口读取数据：

●当分配给所选管道的FIFO缓冲区为空时，接收到一个长度为零的数据包

●PIPECFG.BFRE位=1时接收到一个短数据包并完全读取数据

在这些情况下，将BCLR位设置为1以清除FIFO缓冲区，并启用下一个数据的发送和接收。

BCLR位（CPU缓冲区清除）

将BCLR位设置为1以清除所选管道的CPU端的FIFO缓冲区。

当分配给所选管道的FIFO缓冲区设置为双缓冲区模式时，USBFS仅清除
即使两个平面都已启用读取，也有FIFO缓冲区。

当DCP为选定管道时，将BCLR位设置为1允许USBFS清除FIFO缓冲区，而不管CPU或SIE是否具有访问权限。要在SIE具有访问权限时清除缓冲区，请将DCPCTR.PID[1:0]位设置为00b（NAK响应），然后再将BCLR位设置为1。

当所选管道正在传输时，如果同时向BVAL标志和BCLR位写入1，则USBFS会清除已写入的数据，从而可以传输零长度数据包。

当所选管道不是DCP时，仅在FIFO端口控制寄存器中的frdy位为1（由USBF设置）时，仅将1个写入BCLR位。

BVAL标志（缓冲存储器有效标志）

当数据完全写入CPU端的FIFO缓冲区时，将BVAL标志设置为1，用于在
CURPIPE[3:0].

当所选管道正在传输时，在以下情况下将此标志设置为1：

●要发送一个短包，在数据写入后将此标志设置为1

- To transmit a zero-length packet, set this flag to 1 before data is written to the FIFO buffer

The USBFS then switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

When data of the maximum packet size is written for the pipe in continuous transfer mode, the USBFS sets the BVAL flag to 1 and switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBFS). When the selected pipe is receiving, do not set the BVAL flag to 1.

28.2.10 INTENB0 : Interrupt Enable Register 0

Base address: USBFS = 0x4009_0000

Offset address: 0x030

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	BRDYE	Buffer Ready Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
9	NRDYE	Buffer Not Ready Response Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
10	BEMPE	Buffer Empty Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
11	CTRE	Control Transfer Stage Transition Interrupt Enable *1 0: Disable interrupt request 1: Enable interrupt request	R/W
12	DVSE	Device State Transition Interrupt Enable *1 0: Disable interrupt request 1: Enable interrupt request	R/W
13	SOFE	Frame Number Update Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
14	RSME	Resume Interrupt Enable*1 0: Disable interrupt request 1: Enable interrupt request	R/W
15	VBSE	VBUS Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W

Note 1. The RSME, DVSE, and CTRE bits can only be set to 1 in device controller mode. Do not set these bits to 1 in host controller mode.

When a status flag in the INTSTS0 register sets to 1 and the associated interrupt request enable bit setting in theINTENB0 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB0 register setting, the status flag in the INTSTS0 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB0 register is switched from 0 to 1 while the associated status flag in the INTSTS0 register is set to 1, a USBFS interrupt is requested.

●要发送零长度数据包，请在数据写入FIFO缓冲区之前将此标志设置为1

然后USBFS将FIFO缓冲区从CPU端切换到SIE端，从而启用传输。

当在连续传输模式下为管道写入最大数据包大小的数据时，USBFS将BVAL标志设置为1，并将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

仅在FRDY位为1（由USBFS设置）时将1写入BVAL标志。当所选管道正在接收时，不要将BVAL标志设置为1。

28.2.10 INTENB0:中断使能寄存器0

Base address: USBFS = 0x4009_0000

Offset address: 0x030

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
8	BRDYE	缓冲区就绪中断使能 0：禁止中断请求1：允许中断请求	R/W
9	NRDYE	缓冲区未就绪响应中断使能 0：禁止中断请求1：允许中断请求	R/W
10	BEMPE	缓冲区空中断使能 0：禁止中断请求1：允许中断请求	R/W
11	CTRE	控制传输级转换中断使能*1 0：禁止中断请求1：允许中断请求	R/W
12	DVSE	设备状态转换中断使能*1 0：禁止中断请求1：允许中断请求	R/W
13	SOFE	帧号更新中断使能 0：禁止中断请求1：允许中断请求	R/W
14	RSME	恢复中断使能*1 0：禁止中断请求1：允许中断请求	R/W
15	VBSE	VBUS中断使能 0：禁止中断请求1：允许中断请求	R/W

注1.RSME、DVSE和CTRE位只能在设备控制器模式下设置为1。不要在主机控制器模式下将这些位设置为1。

当INTSTS0寄存器中的状态标志设置为1并且INTENB0寄存器中相关的中断请求使能位设置为1时，USBFS发出USBFS中断请求。

无论INTENB0寄存器设置如何，INTSTS0寄存器中的状态标志都会设置为1，以响应满足相关条件的状态变化。

当INTENB0寄存器中的中断请求使能位从0切换到1时，而相关的状态标志在INTSTS0寄存器设置为1，请求USBFS中断。

RA生态工作室

28.2.11 INTENB1 : Interrupt Enable Register 1

Base address: USBFS = 0x4009_0000

Offset address: 0x032

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PDDETINTE	PDDETINT Detection Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	SACKE	Setup Transaction Normal Response Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
5	SIGNE	Setup Transaction Error Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
6	EOFERRE	EOF Error Detection Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
10:7	—	These bits are read as 0. The write value should be 0.	R/W
11	ATTCHE	Connection Detection Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
12	DTCHE	Disconnection Detection Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
13	—	This bit is read as 0. The write value should be 0.	R/W
14	BCHGE	USB Bus Change Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
15	OVRCRE	Overcurrent Input Change Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W

Note: The bits in INTENB1 can only be set to 1 in host controller mode. Do not set these bits to 1 in device controller mode.

INTENB1 specifies the interrupt masks in host controller mode and for the setup transaction.

When a status flag in the INTSTS1 register sets to 1 and the associated interrupt request enable bit setting in theINTENB1 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB1 register setting, the status flag in the INTSTS1 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB1 register is switched from 0 to 1 while the associated status flag in the INTSTS1 register is set to 1, a USBFS interrupt is requested.

Do not enable interrupts in device controller mode.

28.2.11 INTENB1：中断使能寄存器1

Base address: USBFS = 0x4009_0000

Offset address: 0x032

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PDDETINTE	PDDETINT检测中断请求使能 0：禁止中断请求1：允许中断请求	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	SACKE	设置事务正常响应中断使能 0：禁止中断请求1：允许中断请求	R/W
5	SIGNE	设置事务错误中断使能 0：禁止中断请求1：允许中断请求	R/W
6	EOFERRE	EOF错误检测中断使能 0：禁止中断请求1：允许中断请求	R/W
10:7	—	这些位被读取为0。写入值应为0。	R/W
11	ATTCHE	连接检测中断使能 0：禁止中断请求1：允许中断请求	R/W
12	DTCHE	断线检测中断使能 0：禁止中断请求1：允许中断请求	R/W
13	—	该位读取为0。写入值应为0。	R/W
14	BCHGE	USB总线变化中断使能 0：禁止中断请求1：允许中断请求	R/W
15	OVRCRE	过流输入变化中断使能 0：禁止中断请求1：允许中断请求	R/W

Note: INTENB1中的位只能在主机控制器模式下设置为1。不要在设备控制器模式下将这些位设置为1。

INTENB1指定主机控制器模式和设置事务的中断掩码。

当INTSTS1寄存器中的状态标志设置为1并且INTENB1寄存器中相关的中断请求使能位设置为1时，USBFS发出USBFS中断请求。

无论INTENB1寄存器设置如何，INTSTS1寄存器中的状态标志都会设置为1，以响应满足相关条件的状态更改。

当INTENB1寄存器中的中断请求使能位从0切换到1时，而相关的状态标志在INTSTS1寄存器设置为1，请求USBFS中断。

不要在设备控制器模式下启用中断。

28.2.12 BRDYENB : BRDY Interrupt Enable Register

Base address: USBFS = 0x4009_0000

Offset address: 0x036

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BRDYE	BRDY Interrupt Enable for Pipe 0 0: Disable interrupt request 1: Enable interrupt request	R/W
1	PIPE1BRDYE	BRDY Interrupt Enable for Pipe 1 0: Disable interrupt request 1: Enable interrupt request	R/W
2	PIPE2BRDYE	BRDY Interrupt Enable for Pipe 2 0: Disable interrupt request 1: Enable interrupt request	R/W
3	PIPE3BRDYE	BRDY Interrupt Enable for Pipe 3 0: Disable interrupt request 1: Enable interrupt request	R/W
4	PIPE4BRDYE	BRDY Interrupt Enable for Pipe 4 0: Disable interrupt request 1: Enable interrupt request	R/W
5	PIPE5BRDYE	BRDY Interrupt Enable for Pipe 5 0: Disable interrupt request 1: Enable interrupt request	R/W
6	PIPE6BRDYE	BRDY Interrupt Enable for Pipe 6 0: Disable interrupt request 1: Enable interrupt request	R/W
7	PIPE7BRDYE	BRDY Interrupt Enable for Pipe 7 0: Disable interrupt request 1: Enable interrupt request	R/W
8	PIPE8BRDYE	BRDY Interrupt Enable for Pipe 8 0: Disable interrupt request 1: Enable interrupt request	R/W
9	PIPE9BRDYE	BRDY Interrupt Enable for Pipe 9 0: Disable interrupt request 1: Enable interrupt request	R/W
15:10	—	This bit is read as 0. The write value should be 0.	R/W

The BRDYENB register enables or disables the INTSTS0.BRDY bit to be set to 1 when a BRDY interrupt is detected for each pipe.

When a status flag in the BRDYSTS register sets to 1 and the associated PIPEnBRDYE bit (n = 0 to 9) setting in theBRDYENB register is 1, the INTSTS0.BRDY flag sets to 1. In this case, if the BRDYE bit in INTENB0 is 1, the USBFS generates a BRDY interrupt request. While at least one PIPEnBRDY bit indicates 1, the USB generates the BRDY interrupt request when the associated interrupt request enable bit in the BRDYENB register is changed from 0 to 1 by software.

28.2.12 BRDYENB:BRDY中断使能寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x036

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BRDYE	管道0的BRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
1	PIPE1BRDYE	管道1的BRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
2	PIPE2BRDYE	管道2的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
3	PIPE3BRDYE	管道3的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
4	PIPE4BRDYE	管道4的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
5	PIPE5BRDYE	管道5的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
6	PIPE6BRDYE	管道6的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
7	PIPE7BRDYE	管道7的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
8	PIPE8BRDYE	管道8的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
9	PIPE9BRDYE	管道9的BRDY中断启用 0：禁止中断请求1：允许中断请求	R/W
15:10	—	该位读取为0。写入值应为0。	R/W

当检测到每个管道的BRDY中断时，BRDYENB寄存器启用或禁用INTSTS0.BRDY位以设置为1。

当BRDYSTS寄存器中的状态标志设置为1并且BRDYENB寄存器中相关的PIPEnBRDYE位（n=0到9）设置为1时，INTSTS0.BRDY标志设置为1。在这种情况下，如果INTENB0中的BRDYE位为1、USBFS产生一个BRDY中断请求。当至少一个PIPEnBRDY位指示1时，当BRDYENB寄存器中相关的中断请求使能位由软件从0变为1时，USB产生BRDY中断请求。

RA生态工作室

28.2.13 NRDYENB : NRDY Interrupt Enable Register

Base address: USBFS = 0x4009_0000

Offset address: 0x038

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0NRDYE	NRDY Interrupt Enable for Pipe 0 0: Disable interrupt request 1: Enable interrupt request	R/W
1	PIPE1NRDYE	NRDY Interrupt Enable for Pipe 1 0: Disable interrupt request 1: Enable interrupt request	R/W
2	PIPE2NRDYE	NRDY Interrupt Enable for Pipe 2 0: Disable interrupt request 1: Enable interrupt request	R/W
3	PIPE3NRDYE	NRDY Interrupt Enable for Pipe 3 0: Disable interrupt request 1: Enable interrupt request	R/W
4	PIPE4NRDYE	NRDY Interrupt Enable for Pipe 4 0: Disable interrupt request 1: Enable interrupt request	R/W
5	PIPE5NRDYE	NRDY Interrupt Enable for Pipe 5 0: Disable interrupt request 1: Enable interrupt request	R/W
6	PIPE6NRDYE	NRDY Interrupt Enable for Pipe 6 0: Disable interrupt request 1: Enable interrupt request	R/W
7	PIPE7NRDYE	NRDY Interrupt Enable for Pipe 7 0: Disable interrupt request 1: Enable interrupt request	R/W
8	PIPE8NRDYE	NRDY Interrupt Enable for Pipe 8 0: Disable interrupt request 1: Enable interrupt request	R/W
9	PIPE9NRDYE	NRDY Interrupt Enable for Pipe 9 0: Disable interrupt request 1: Enable interrupt request	R/W
15:10	—	This bit is read as 0. The write value should be 0.	R/W

The NRDYENB register enables or disables the INTSTS0.NRDY bit to be set to 1 when a NRDY interrupt is detected for each pipe.

When a status flag in the NRDYSTS register sets to 1 and the associated PIPEnNRDYE (n = 0 to 9) bit setting in theNRDYENB register is 1, the INTSTS0.NRDY flag sets to 1. In this case, if the NRDYE bit in INTENB0 is 1, the USBFS generates a NRDY interrupt request. While at least one PIPEnNRDY bit indicates 1, the USBFS generates the NRDY interrupt request when the associated interrupt request enable bit in the NRDYENB register is changed from 0 to 1 by software.

28.2.13 NRDYENB:NRDY中断使能寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x038

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0NRDYE	管道0的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
1	PIPE1NRDYE	管道1的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
2	PIPE2NRDYE	管道2的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
3	PIPE3NRDYE	管道3的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
4	PIPE4NRDYE	管道4的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
5	PIPE5NRDYE	管道5的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
6	PIPE6NRDYE	管道6的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
7	PIPE7NRDYE	管道7的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
8	PIPE8NRDYE	管道8的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
9	PIPE9NRDYE	管道9的NRDY中断使能 0：禁止中断请求1：允许中断请求	R/W
15:10	—	该位读取为0。写入值应为0。	R/W

当检测到每个管道的NRDY中断时，NRDYENB寄存器启用或禁用INTSTS0.NRDY位设置为1。

当NRDYSTS寄存器中的状态标志设置为1并且NRDYENB寄存器中相关的PIPEnNRDYE（n=0到9）位设置为1时，INTSTS0.NRDY标志设置为1。在这种情况下，如果INTENB0中的NRDYE位为1、USBFS产生一个NRDY中断请求。当至少一个PIPEnNRDY位指示1时，USBFS生成

当NRDYENB寄存器中的相关中断请求使能位由软件从0变为1时，发出NRDY中断请求。

28.2.14 BEMPENB : BEMP Interrupt Enable Register

Base address: USBFS = 0x4009_0000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BEMPE	BEMP Interrupt Enable for Pipe 0 0: Disable interrupt request 1: Enable interrupt request	R/W
1	PIPE1BEMPE	BEMP Interrupt Enable for Pipe 1 0: Disable interrupt request 1: Enable interrupt request	R/W
2	PIPE2BEMPE	BEMP Interrupt Enable for Pipe 2 0: Disable interrupt request 1: Enable interrupt request	R/W
3	PIPE3BEMPE	BEMP Interrupt Enable for Pipe 3 0: Disable interrupt request 1: Enable interrupt request	R/W
4	PIPE4BEMPE	BEMP Interrupt Enable for Pipe 4 0: Disable interrupt request 1: Enable interrupt request	R/W
5	PIPE5BEMPE	BEMP Interrupt Enable for Pipe 5 0: Disable interrupt request 1: Enable interrupt request	R/W
6	PIPE6BEMPE	BEMP Interrupt Enable for Pipe 6 0: Disable interrupt request 1: Enable interrupt request	R/W
7	PIPE7BEMPE	BEMP Interrupt Enable for Pipe 7 0: Disable interrupt request 1: Enable interrupt request	R/W
8	PIPE8BEMPE	BEMP Interrupt Enable for Pipe 8 0: Disable interrupt request 1: Enable interrupt request	R/W
9	PIPE9BEMPE	BEMP Interrupt Enable for Pipe 9 0: Disable interrupt request 1: Enable interrupt request	R/W
15:10	—	This bit is read as 0. The write value should be 0.	R/W

The BEMPENB register enables or disables the INTSTS0.BEMP bit to be set to 1 when a BEMP interrupt is detected for each pipe.

When a status flag in the BEMPSTS register sets to 1 and the associated PIPEnBEMPE (n = 0 to 9) bit setting in the BEMPENB register is 1, the INTSTS0.BEMP flag sets to 1. In this case, if the BEMPE bit in INTENB0 is 1, the USBFS generates a BEMP interrupt request. While at least one PIPEnBEMP bit indicates 1, the USBFS generates the BEMP interrupt request when the associated interrupt request enable bit in the BEMPENB register is changed from 0 to 1 by software.

28.2.14 BEMPENB:BEMP中断使能寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BEMPE	管道0的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
1	PIPE1BEMPE	管道1的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
2	PIPE2BEMPE	管道2的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
3	PIPE3BEMPE	管道3的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
4	PIPE4BEMPE	管道4的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
5	PIPE5BEMPE	管道5的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
6	PIPE6BEMPE	管道6的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
7	PIPE7BEMPE	管道7的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
8	PIPE8BEMPE	管道8的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
9	PIPE9BEMPE	管道9的BEMP中断启用 0：禁止中断请求1：允许中断请求	R/W
15:10	—	该位读取为0。写入值应为0。	R/W

当检测到每个管道的BEMP中断时，BEMPENB寄存器启用或禁用INTSTS0.BEMP位设置为1。

当BEMPSTS寄存器中的状态标志设置为1并且BEMPENB寄存器中相关的PIPEnBEMPE（n=0到9）位设置为1时，INTSTS0.BEMP标志设置为1。在这种情况下，如果INTENB0中的BEMPE位为1，USBFS产生一个BEMP中断请求。当至少一个PIPEnBEMP位指示1时，当BEMPENB寄存器中相关的中断请求使能位由软件从0变为1时，USBFS产生BEMP中断请求。

28.2.15 SOFCFG : SOF Output Configuration Register

Base address: USBFS = 0x4009_0000

Offset address: 0x03C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	EDGESTS	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	EDGESTS	Edge Interrupt Output Status Monitor*1 Indicates 1 during the edge processing of an edge interrupt output signal.	R
5	—	This bit is read as 0. The write value should be 0.	R/W
6	BRDYM	BRDY Interrupt Status Clear Timing 0: Clear BRDY flag by software 1: Clear BRDY flag by the USBFS through a data read from the FIFO buffer or data write to the FIFO buffer	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
8	TRNENSEL	Transaction-Enabled Time Select*1 0: Not low-speed communication 1: Low-speed communication	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Confirm that the EDGESTS flag is 0 before stopping the clock supply to the USBFS.

EDGESTS bit (Edge Interrupt Output Status Monitor)

The EDGESTS bit indicates 1 during the edge processing of an edge interrupt output signal. Confirm that this bit is 0 before stopping the clock supply to the USBFS.

BRDYM bit (BRDY Interrupt Status Clear Timing)

The BRDYM bit specifies how the BRDY interrupt status flags for the pipes are cleared.

TRNENSEL bit (Transaction-Enabled Time Select)

When the USB port is in use for full- or low-speed communications, the TRNENSEL bit specifies the timing with which the USBFS issues tokens in a frame (transaction-enabled time).

Set this bit to 1 when a low-speed device is connected. The bit is only valid in host controller mode. Set this bit to 0 in device controller mode.

28.2.16 INTSTS0 : Interrupt Status Register 0

Base address: USBFS = 0x4009_0000

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	VINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	x	0	0	0	0	x	0	0	x	0	0	0	0

28.2.15 SOFCFG:SOF输出配置寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x03C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	EDGESTS	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	EDGESTS	边沿中断输出状态监视器*1 在边沿中断输出信号的边沿处理期间表示1。	R
5	—	该位读取为0。写入值应为0。	R/W
6	BRDYM	BRDY中断状态清除时序 0：软件清除BRDY标志1：USBFS通过从FIFO缓冲区读取数据或向FIFO缓冲区写入数据清除BRDY标志	R/W
7	—	该位读取为0。写入值应为0。	R/W
8	TRNENSEL	事务启用时间选择*1 0：非低速通讯1：低速通讯	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.在停止向USBFS提供时钟之前，请确认EDGESTS标志为0。

EDGESTS位（边缘中断输出状态监视器）

在边沿中断输出信号的边沿处理期间，EDGESTS位指示1。在停止向USBFS提供时钟之前，请确认该位为0。

BRDYM位（BRDY中断状态清除时序）

BRDYM位指定如何清除管道的BRDY中断状态标志。

TRNENSEL位（事务使能时间选择）

当USB端口用于全速或低速通信时，TRNENSEL位指定
USBFS在一个帧中发布令牌（事务启用时间）。

当连接了低速设备时，将此位设置为1。该位仅在主机控制器模式下有效。在设备控制器模式下将此位设置为0。

28.2.16 INTSTS0：中断状态寄存器0

Base address: USBFS = 0x4009_0000

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	VINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
重置后的值:	0	0	0	x	0	0	0	0	x	0	0	x	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CTSQ[2:0]	Control Transfer Stage 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error	R
3	VALID	USB Request Reception 0: Setup packet not received 1: Setup packet received	R/W
6:4	DVSQ[2:0]	Device State Indicates the device state. 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state Others: Suspend state	R
7	VBSTS	VBUS Input Status 0: USB_VBUS pin is low 1: USB_VBUS pin is high	R
8	BRDY	Buffer Ready Interrupt Status 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R
9	NRDY	Buffer Not Ready Interrupt Status 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R
10	BEMP	Buffer Empty Interrupt Status 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R
11	CTRT	Control Transfer Stage Transition Interrupt Status*2 0: No control transfer stage transition interrupt occurred 1: Control transfer stage transition interrupt occurred	R/W*1
12	DVST	Device State Transition Interrupt Status*2 0: No device state transition interrupt occurred 1: Device state transition interrupt occurred	R/W*1
13	SOFR	Frame Number Refresh Interrupt Status 0: No SOF interrupt occurred 1: SOF interrupt occurred	R/W*1
14	RESM	Resume Interrupt Status*2 *3 0: No resume interrupt occurred 1: Resume interrupt occurred	R/W*1
15	VBINT	VBUS Interrupt Status*3 0: No VBUS interrupt occurred 1: VBUS interrupt occurred	R/W*1

Note: The value of the DVST bit is 0 when the MCU is reset and 1 after a USB bus reset.
Note: The value of the VBSTS bit is 1 when the USB_VBUS pin is high and 0 when the USB_VBUS pin is low.
Note: The value of the DVSQ[2:0] bits is 000b when the MCU is reset and 001b after a USB bus reset.
Note 1. To clear the VBINT, RESM, SOFR, DVST, CTRT, or VALID bits, write 0 only to the bits to be cleared. Write 1 to the other bits. Do not write 0 to the status bits indicating 0.
Note 2. The status of the RESM, DVST, and CTRT bits are changed only in device controller mode. Set the associated interrupt enable bits to 0 (disabled) in host controller mode.
Note 3. The USBFS detects a change in the status indicated in the VBINT andRESM bits even while the clock supply is stopped (SCKE bit = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status by software.

CTSQ[2:0] bits (Control Transfer Stage)

In host controller mode, the read value of the CTSQ[2:0] bits is invalid.

Bit	Symbol	Function	R/W
2:0	CTSQ[2:0]	控制转移阶段 000：空闲或设置阶段001：控制读取数据阶段010：控制读取状态阶段011：控制写入数据阶段100：控制写入状态阶段101：控制写入（无数据）状态阶段110：控制传输顺序错误	R
3	VALID	USB请求接收 0：未收到设置包1：收到设置包	R/W
6:4	DVSQ[2:0]	设备状态 指示设备状态。 000：通电状态001：默认状态010：地址状态011：配置状态 其他：暂停状态	R
7	VBSTS	VBUS输入状态 0：USB_VBUS引脚为低电平1：USB_VBUS引脚为高电平	R
8	BRDY	缓冲区就绪中断状态 0：未发生BRDY中断1：发生BRDY中断	R
9	NRDY	缓冲区未就绪中断状态 0：未发生NRDY中断1：发生NRDY中断	R
10	BEMP	缓冲区空中断状态 0：未发生BEMP中断1：发生BEMP中断	R
11	CTRT	控制传输阶段转换中断状态*2 0：未发生控制转移阶段转换中断1：发生控制转移阶段转换中断	R/W*1
12	DVST	设备状态转换中断状态*2 0：未发生设备状态转换中断1：发生设备状态转换中断	R/W*1
13	SOFR	帧号刷新中断状态 0：未发生SOF中断1：发生SOF中断	R/W*1
14	RESM	恢复中断状态*2*3 0：未发生恢复中断1：发生恢复中断	R/W*1
15	VBINT	VBUS中断状态*3 0：未发生VBUS中断1：发生VBUS中断	R/W*1

Note: DVST位的值在MCU复位时为0，在USB总线复位后为1。
Note: 当USB_VBUS引脚为高电平时VBSTS位的值为1，当USB_VBUS引脚为低电平时为0。
Note: DVSQ[2:0]位的值在MCU复位时为000b，在USB总线复位后为001b。
注1.要清除VBINT、RESM、SOFR、DVST、CTRT或VALID位，只需将0写入要清除的位。将1写入其他位。不要将0写入指示0的状态位。

注2.RESM、DVST和CTRT位的状态仅在设备控制器模式下更改。在主机控制器模式下，将相关的中断使能位设置为0（禁用）。

注3.即使在时钟供应停止（SCKE位=0）时，USBFS也会检测到VBINT和RESM位指示的状态变化，并在相关中断请求位为1时请求中断。在之前启用时钟供应通过软件清除状态。

CTSQ[2:0]位（控制传输级）

在主机控制器模式下，CTSQ[2:0]位的读取值无效。

RA生态工作室

VALID bit (USB Request Reception)

In host controller mode, the read value of the VALID bit is invalid.

DVSQ[2:0] bits (Device State)

The DVSQ[2:0] bits are initialized by a USB bus reset. In host controller mode, the read value is invalid.

BRDY flag (Buffer Ready Interrupt Status)

The BRDY flag indicates the BRDY interrupt status.

The USBFS sets the BRDY bit to 1 when it detects a BRDY interrupt status (PIPEnBRDY = 1, n = 0 to 9) on at least one pipe for which BRDY interrupts are enabled (BRDYENB.PIPEnBRDYE = 1).

For the conditions that cause the PIPEnBRDY status to be asserted, see section 28.3.3.1. BRDY interrupt.

The USBFS sets the BRDY bit to 0 when the software writes 0 to all of the PIPEnBRDY bits associated with the PIPEnBRDYE bits that are set to 1. Writing 0 to the BRDY flag in the software does not clear the flag.

NRDY flag (Buffer Not Ready Interrupt Status)

The NRDY flag indicates the NRDY interrupt status.

The USBFS sets the NRDY bit to 1 when it detects a NRDY interrupt status (PIPEnNRDY = 1, n = 0 to 9) on at least one pipe for which NRDY interrupts are enabled (NRDYENB.PIPEnNRDYE = 1).

For the conditions that cause the PIPEnNRDY status to be asserted, see section 28.3.3.2. NRDY interrupt.

The USBFS sets the NRDY bit to 0 when the software writes 0 to all of the PIPEnNRDY bits associated with the PIPEnNRDYE bits that are set to 1. Writing 0 to the NRDY flag in the software does not clear the flag.

BEMP flag (Buffer Empty Interrupt Status)

The BEMP flag indicates the BEMP interrupt status.

The USBFS sets the BEMP bit to 1 when it detects a BEMP interrupt status (PIPEnBEMP = 1, n = 0 to 9) on at least one pipe for which BEMP interrupts are enabled (BEMPENB.PIPEnBEMPE = 1).

For the conditions that cause the PIPEnBEMP status to be asserted, see section 28.3.3.3. BEMP interrupt.

The USBFS sets the BEMP bit to 0 when the software writes 0 to all of the PIPEnBEMP bits associated with the PIPEnBEMPE bits that are set to 1. Writing 0 to the BEMP flag in the software does not clear the flag.

CTRT flag (Control Transfer Stage Transition Interrupt Status)

In device controller mode, the USBFS updates the value of the CTSQ[2:0] bits and sets the CTRT flag to 1 on detecting a transition in the control transfer stage. When a control transfer stage transition interrupt occurs, clear the CTRT flag before the USBFS detects the next control transfer stage transition.

Values read from the CTRT flag in host controller mode are invalid.

DVST flag (Device State Transition Interrupt Status)

In device controller mode, the USBFS updates the value of the DVSQ[2:0] bits and sets the DVST flag to 1 on detecting a change in the device state. When a device state transition interrupt occurs, clear theDVST flag before the USBFS detects the next device state transition.

Values read from the DVST flag in host controller mode are invalid.

SOFR flag (Frame Number Refresh Interrupt Status)

In host controller mode, the USBFS sets the SOFR flag to 1 on updating the frame number when the DVSTCTR0.UACT bit is set to 1 by software. A SOFR interrupt is detected every 1 ms.

In device controller mode, the USBFS sets the SOFR flag to 1 on updating the frame number. A frame number refresh interrupt is detected every 1 ms.

The USBFS can detect an SOFR interrupt through the internal interpolation function even when a corrupted SOF packet is received from the USB host.

有效位（USB请求接收）

在主机控制器模式下，VALID位的读取值无效。

DVSQ[2:0] bits (Device State)

DVSQ[2:0]位由USB总线复位初始化。在主机控制器模式下，读取的值无效。

BRDY标志（缓冲区就绪中断状态）

BRDY标志指示BRDY中断状态。

当USBFS在至少一个启用了BRDY中断(BRDYENB.PIPEnBRDYE=1)的管道上检测到BRDY中断状态(PIPEnBRDY=1 n=0到9)时，将BRDY位设置为1。

有关导致PIPEnBRDY状态被断言的条件，请参见第28.3.3.1节。BRDY中断。

当软件将0写入与
设置为1的PIPEnBRDYE位。在软件中将0写入BRDY标志不会清除该标志。

NRDY标志（缓冲区未就绪中断状态）

NRDY标志指示NRDY中断状态。

当USBFS在至少一个启用了NRDY中断(NRDYENB.PIPEnNRDYE=1)的管道上检测到NRDY中断状态(PIPEnNRDY=1 n=0到9)时，将NRDY位设置为1。

有关导致PIPEnNRDY状态被断言的条件，请参见第28.3.3.2节。NRDY中断。

USBFS将NRDY位设置为0，当软件将0写入与
设置为1的PIPEnNRDYE位。在软件中将0写入NRDY标志不会清除该标志。

BEMP标志（缓冲区空中断状态）

BEMP标志指示BEMP中断状态。

当USBFS在至少一个启用了BEMP中断(BEMPENB.PIPEnBEMPE=1)的管道上检测到BEMP中断状态(PIPEnBEMP=1 n=0到9)时，将BEMP位设置为1。

有关导致PIPEnBEMP状态被断言的条件，请参见第28.3.3.3节。BEMP中断。

当软件将0写入与
PIPEnBEMPE位设置为1。在软件中将0写入BEMP标志不会清除该标志。

CTRT标志（控制传输阶段转换中断状态）

在设备控制器模式下，USBFS更新CTSQ[2:0]位的值，并在检测到控制传输阶段的转换时将CTRT标志设置为1。当控制传输阶段转换中断发生时，在USBFS检测到下一个控制传输阶段转换之前清除CTRT标志。

在主机控制器模式下从CTRT标志读取的值无效。

DVST标志（设备状态转换中断状态）

在设备控制器模式下，USBFS更新DVSQ[2:0]位的值，并在检测到设备状态发生变化时将DVST标志设置为1。当设备状态转换中断发生时，在USBFS检测到下一个设备状态转换之前清除DVST标志。

在主机控制器模式下从DVST标志读取的值无效。

SOFR标志（帧号刷新中断状态）

在主机控制器模式下，当软件将DVSTCTR0.UACT位设置为1时，USBFS在更新帧号时将SOFR标志设置为1。每1ms检测一次SOFR中断。

在设备控制器模式下，USBFS在更新帧号时将SOFR标志设置为1。每1ms检测一次帧号刷新中断。

即使从USB主机接收到损坏的SOF数据包，USBFS也可以通过内部插值功能检测SOFR中断。

RESM flag (Resume Interrupt Status)

In device controller mode, the USBFS sets the RESM flag to 1 on detecting the falling edge of the signal on the USB_DP pin in the Suspend state (DVSQ[2:0] = 1xxb). Values read from the RESM flag in host controller mode are invalid.

VBINT flag (VBUS Interrupt Status)

The USBFS sets the VBINT flag to 1 on detecting a level change (high to low or low to high) in the USB_VBUS pin input value. The USBFS sets the VBSTS flag to indicate the USB_VBUS pin input value. When a VBUS interrupt occurs, eliminate transient elements by reading the VBSTS flag at least three times through software processing and check that the values read are the same.

28.2.17 INTSTS1 : Interrupt Status Register 1

Base address: USBFS = 0x4009_0000

Offset address: 0x042

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PDDETINT*1	PDDET Detection Interrupt Status Flag 0: No PDDET interrupt occurred 1: PDDET interrupt occurred	R/W*2
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	SACK	Setup Transaction Normal Response Interrupt Status 0: No SACK interrupt occurred 1: SACK interrupt occurred	R/W*3
5	SIGN	Setup Transaction Error Interrupt Status 0: No SIGN interrupt occurred 1: SIGN interrupt occurred	R/W*3
6	EOFERR	EOF Error Detection Interrupt Status 0: No EOFERR interrupt occurred 1: EOFERR interrupt occurred	R/W*3
10:7	—	These bits are read as 0. The write value should be 0.	R/W
11	ATTCH	ATTCH Interrupt Status 0: No ATTCH interrupt occurred 1: ATTCH interrupt occurred	R/W*3
12	DTCH	USB Disconnection Detection Interrupt Status 0: No DTCH interrupt occurred 1: DTCH interrupt occurred	R/W*3
13	—	This bit is read as 0. The write value should be 0.	R/W
14	BCHG	USB Bus Change Interrupt Status*4 0: No BCHG interrupt occurred 1: BCHG interrupt occurred	R/W*3
15	OVRCR	Overcurrent Input Change Interrupt Status*4 0: No OVRCR interrupt occurred 1: OVRCR interrupt occurred	R/W*3

Note 1. The USBFS detects a change in the status in the PDDETINT, OVRCR or BCHG bit even when the clock supply is stopped (SYSCFG.SCKE = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply (SYSCFG.SCKE = 1) before clearing the status through software. No other interrupts can be detected while the clock supply is stopped (SYSCFG.SCKE bit = 0).
Note 2. To clear the bits in the INTSTS1 register, write 0 only to the bits to be cleared. Write 1 to the other bits.
Note 3. To clear the bits in INTSTS1, write 0 only to the bits to be cleared. Write 1 to the other bits.
Note 4. The USBFS detects a change in the status in the OVRCR or BCHG bit even when the clock supply is stopped (SYSCFG.SCKE = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply (SYSCFG.SCKE = 1) before

RESM标志（恢复中断状态）

在设备控制器模式下，USBFS在检测到处于挂起状态(DVSQ[2:0]=1xxb)的USB_DP引脚上的信号下降沿时将RESM标志设置为1。在主机控制器模式下从RESM标志读取的值无效。

VBINT标志（VBUS中断状态）

USBFS在检测到USB_VBUS引脚输入值的电平变化（从高到低或从低到高）时将VBINT标志设置为1。USBFS设置VBSTS标志以指示USB_VBUS引脚输入值。当发生VBUS中断时，通过软件处理至少3次读取VBSTS标志来消除瞬态元素，并检查读取的值是否相同。

28.2.17 INTSTS1：中断状态寄存器1

Base address: USBFS = 0x4009_0000

Offset address: 0x042

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PDDETINT*1	PDDET检测中断状态标志 0：未发生PDDET中断1：发生PDDET中断	R/W*2
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	SACK	设置事务正常响应中断状态 0：未发生SACK中断1：发生SACK中断	R/W*3
5	SIGN	设置事务错误中断状态 0：未发生SIGN中断1：发生SIGN中断	R/W*3
6	EOFERR	EOF错误检测中断状态 0：未发生EOFERR中断1：发生EOFERR中断	R/W*3
10:7	—	这些位被读取为0。写入值应为0。	R/W
11	ATTCH	ATTCH中断状态 0：未发生ATTCH中断1：发生ATTCH中断	R/W*3
12	DTCH	USB断线检测中断状态 0：未发生DTCH中断1：发生DTCH中断	R/W*3
13	—	该位读取为0。写入值应为0。	R/W
14	BCHG	USB总线更改中断状态*4 0：未发生BCHG中断1：发生BCHG中断	R/W*3
15	OVRCR	过电流输入变化中断状态*4 0：未发生OVRCR中断1：发生OVRCR中断	R/W*3

注1.即使停止时钟供应(SYSCFG.SCKE=0)，USBFS也会检测到PDDETINT、OVRCR或BCHG位的状态变化，并在相关中断请求位为1时请求中断。使能在通过软件清除状态之前提供时钟（SYSCFG.SCKE=1）。停止提供时钟（SYSCFG.SCKE位=0）时，不会检测到其他中断。

注2.要清除INTSTS1寄存器中的位，只需将0写入要清除的位。将1写入其他位。
注3.要清除INTSTS1中的位，只需将0写入要清除的位。将1写入其他位。
注4.即使停止时钟供应(SYSCFG.SCKE=0)，USBFS也会检测到OVRCR或BCHG位的状态变化，并在相关中断请求位为1时请求中断。使能时钟供应(SYSCFG.SCKE=1)之前

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clearing the status through the software. No other interrupts can be detected while the clock supply is stopped (SYSCFG.SCKE bit = 0).

INTSTS1 is used to confirm the status of each interrupt in host controller mode. Only enable the status change interrupts indicated in the bits in INTSTS1 in host controller mode.

PDDETINT flag (PDDET Detection Interrupt Status Flag)

The USBFS sets the PDDETINT flag to 1 on detecting a level change (high to low or low to high) in the PDDET pin input value. When the PDDETINT interrupt is generated, perform debouncing by reading the BCCTRL1.PDDETSTS flag at least three times through software processing and checking that the values read are the same.

SACK flag (Setup Transaction Normal Response Interrupt Status)

The SACK flag indicates the status of the setup transaction normal response interrupt in host controller mode.

The USBFS detects the SACK interrupt and sets this flag to 1 when an ACK response is returned from a peripheral device during the setup transactions issued by the USBFS. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

Values read from the SACK flag in device controller mode are invalid.

SIGN flag (Setup Transaction Error Interrupt Status)

The SIGN flag indicates the status of setup transaction error interrupts in host controller mode.

The USBFS detects the SIGN interrupt and sets this flag to 1 when an ACK response is not returned from a peripheral device three consecutive times during the setup transactions issued by the USBFS. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions:

- Timeout is detected by the USBFS when the peripheral device has returned no response
- A corrupted ACK packet is received
- A handshake other than ACK (NAK, NYET, or STALL) is received

Values read from the SIGN flag in device controller mode are invalid.

EOFERR flag (EOF Error Detection Interrupt Status)

The EOFERR flag indicates the status of EOF error detection interrupts in host controller mode.

The USBFS detects the EOFERR interrupt and sets this flag to 1 on detecting that communication did not complete at the EOF2 timing defined in the USB 2.0 specification. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

After detecting the EOFERR interrupt, the USBFS controls the hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt was detected to 0
- Puts the port in which the EOFERR interrupt occurred into the idle state

The software must terminate all pipes in which communications are being carried out and re-enumerate the USB port.

Values read from the EOFERR flag in device controller mode are invalid.

ATTCH flag (ATTCH Interrupt Status)

The ATTCH flag indicates the status of USB attach detection interrupts in host controller mode.

The USBFS detects the ATTCH interrupt and sets this flag to 1 on detecting a J- or K-state on the full- or low-speed signal level for 2.5 µs. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects the ATTCH interrupt on any of the following conditions.

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs

Values read from the ATTCH flag in device controller mode are invalid.

通过软件清除状态。停止提供时钟（SYSCFG.SCKE位=0）时，不会检测到其他中断。

INTSTS1用于确认主机控制器模式下每个中断的状态。仅在主机控制器模式下启用INTSTS1位中指示的状态更改中断。

PDDETINT标志（PDDET检测中断状态标志）

USBFS在检测到PDDET引脚输入值的电平变化（从高到低或从低到高）时将PDDETINT标志设置为1。当产生PDDETINT中断时，通过软件处理至少3次读取BCCTRL1.PDDETSTS标志并检查读取的值是否相同来执行去抖动。

SACK标志（设置事务正常响应中断状态）

SACK标志指示主机控制器模式下设置事务正常响应中断的状态。

在USBFS发出的设置事务期间，当外围设备返回ACK响应时，USBFS检测到SACK中断并将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

在设备控制器模式下从SACK标志读取的值无效。

SIGN标志（设置事务错误中断状态）

SIGN标志指示主机控制器模式下设置事务错误中断的状态。

在USBFS发出的设置事务期间，如果外围设备连续3次没有返回ACK响应，则USBFS检测到SIGN中断并将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

当三个连续的设置事务发生以下任何响应条件时，USBFS检测到SIGN中断：

●当外围设备没有返回响应时，USBFS检测到超时
●收到损坏的ACK数据包
●收到ACK（NAK、NYET或STALL）以外的握手

在设备控制器模式下从SIGN标志读取的值无效。

EOFERR标志（EOF错误检测中断状态）

EOFERR标志指示主机控制器模式下EOF错误检测中断的状态。

USBFS检测到EOFERR中断，并在检测到通信未在USB2.0规范中定义的EOF2时序完成时将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

检测到EOFERR中断后，USBFS对硬件进行如下控制，而不考虑相关的中断使能位设置：

●将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
●将发生EOFERR中断的端口置于空闲状态

软件必须终止正在执行通信的所有管道并重新枚举USB端口。

在设备控制器模式下从EOFERR标志读取的值无效。

ATTCH标志（ATTCH中断状态）

ATTCH标志指示主机控制器模式下USB连接检测中断的状态。

USBFS检测到ATTCH中断，并在检测到全速或低速信号电平上的JorK状态持续2.5µs时将此标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS在以下任何条件下检测ATTCH中断。

●K-state、SE0或SE1变为J-state，J-state持续2.5µs
●J-state、SE0或SE1变为K-state，K-state持续2.5µs

在设备控制器模式下从ATTCH标志读取的值无效。

DTCH flag (USB Disconnection Detection Interrupt Status)

The DTCH flag indicates the status of USB disconnection detection interrupts in host controller mode.

The USBFS detects the DTCH interrupt and sets this flag to 1 on detecting a USB bus detach event. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects bus detach events based on the USB 2.0 specification.

After detecting the DTCH interrupt, the USBFS controls hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt was detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state

The software must terminate all pipes in which communications are being carried out and invoke the wait state for attaching to the USB port (waiting for ATTCH interrupt generation).

Values read from the DTCH flag in device controller mode are invalid.

BCHG flag (USB Bus Change Interrupt Status)

The BCHG flag indicates the status of USB bus change interrupts in host controller mode.

The USBFS detects the BCHG interrupt and sets this flag to 1 when a change in the full- or low-speed signal level occurs on the USB port. This includes any change from J-state, K-state, or SE0 to J-state, K-state, or SE0. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS sets the LNST[1:0] flags to indicate the input state of the USB port. When a BCHG interrupt occurs, eliminate transient elements by repeat reading the LNST[1:0] flags by software until the same value is read at least three times.

Change in the USB bus state can be detected while the internal clock is stopped.

Values read from the BCHG flag in device controller mode are invalid.

OVRCR flag (Overcurrent Input Change Interrupt Status)

The OVRCR flag indicates the status of USB_OVRCURA and USB_OVRCURB input pin change interrupts.

The USBFS detects the OVRCR interrupt and sets this flag to 1 when a change (high to low or low to high) occurs in at least one of the input values to the USB_OVRCURA and USB_OVRCURB pins. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

28.2.18 BRDYSTS : BRDY Interrupt Status Register

Base address: USBFS = 0x4009_0000

Offset address: 0x046

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BRDY	BRDY Interrupt Status for Pipe 0 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
1	PIPE1BRDY	BRDY Interrupt Status for Pipe 1 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
2	PIPE2BRDY	BRDY Interrupt Status for Pipe 2*2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1

DTCH标志（USB断线检测中断状态）

DTCH标志指示主机控制器模式下USB断开检测中断的状态。

USBFS检测到DTCH中断并在检测到USB总线分离事件时将此标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS根据USB2.0规范检测总线分离事件。

检测到DTCH中断后，USBFS对硬件进行如下控制，而不管相关的中断使能位设置如何：

●将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0

●将发生DTCH中断的端口置于空闲状态

软件必须终止正在执行通信的所有管道并调用等待状态以连接到USB端口（等待ATTCH中断生成）。

在设备控制器模式下从DTCH标志读取的值无效。

BCHG标志（USB总线更改中断状态）

BCHG标志指示主机控制器模式下USB总线更改中断的状态。

当USB端口上发生全速或低速信号电平变化时，USBFS检测到BCHG中断并将该标志设置为1。这包括从J-state、K-state或SE0到J-state、K-state或SE0的任何更改。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS设置LNST[1:0]标志以指示USB端口的输入状态。当发生BCHG中断时，通过软件重复读取LNST[1:0]标志来消除瞬态元素，直到至少读取相同的值3次。

当内部时钟停止时，可以检测到USB总线状态的变化。

在设备控制器模式下从BCHG标志读取的值无效。

OVRCR标志（过流输入变化中断状态）

OVRCR标志指示USB_OVRCURA和USB_OVRCURB输入引脚变化中断的状态。

当USB_OVRCURA和USB_OVRCURB引脚的至少一个输入值发生变化（从高到低或从低到高）时，USBFS检测到OVRCR中断并将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

28.2.18 BRDYSTS:BRDY中断状态寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x046

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BRDY	管道0*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
1	PIPE1BRDY	管道1*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
2	PIPE2BRDY	管道2*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1

Bit	Symbol	Function	R/W
3	PIPE3BRDY	BRDY Interrupt Status for Pipe 3*2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
4	PIPE4BRDY	BRDY Interrupt Status for Pipe 4 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
5	PIPE5BRDY	BRDY Interrupt Status for Pipe 5 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
6	PIPE6BRDY	BRDY Interrupt Status for Pipe 6*2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
7	PIPE7BRDY	BRDY Interrupt Status for Pipe 7 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
8	PIPE8BRDY	BRDY Interrupt Status for Pipe 8 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
9	PIPE9BRDY	BRDY Interrupt Status for Pipe 9 *2 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*1
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated in the bits in BRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.
Note 2. When the SOFCFG.BRDYM bit is set to 0, clear BRDY interrupts before accessing the FIFO.

28.2.19 NRDYSTS : NRDY Interrupt Status Register

Base address: USBFS = 0x4009_0000
Offset address: 0x048

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0NRDY	NRDY Interrupt Status for Pipe 0 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
1	PIPE1NRDY	NRDY Interrupt Status for Pipe 1 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
2	PIPE2NRDY	NRDY Interrupt Status for Pipe 2 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
3	PIPE3NRDY	NRDY Interrupt Status for Pipe 3 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
4	PIPE4NRDY	NRDY Interrupt Status for Pipe 4 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1

Bit	Symbol	Function	R/W
3	PIPE3BRDY	管道3*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
4	PIPE4BRDY	管道4*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
5	PIPE5BRDY	管道5*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
6	PIPE6BRDY	管道6*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
7	PIPE7BRDY	管道7*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
8	PIPE8BRDY	管道8*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
9	PIPE9BRDY	管道9*2的BRDY中断状态 0：未发生BRDY中断1：发生BRDY中断	R/W*1
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.当SOFCFG.BRDYM位设置为0时，要清除BRDYSTS中位指示的状态，只需将0写入要清除的位。将1写入其他位。

注2.当SOFCFG.BRDYM位设置为0时，在访问FIFO之前清除BRDY中断。

28.2.19 NRDYSTS:NRDY中断状态寄存器

Base address: USBFS = 0x4009_0000
Offset address: 0x048

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0NRDY	管道0的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
1	PIPE1NRDY	管道1的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
2	PIPE2NRDY	管道2的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
3	PIPE3NRDY	管道3的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
4	PIPE4NRDY	管道4的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1

Bit	Symbol	Function	R/W
5	PIPE5NRDY	NRDY Interrupt Status for Pipe 5 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
6	PIPE6NRDY	NRDY Interrupt Status for Pipe 6 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
7	PIPE7NRDY	NRDY Interrupt Status for Pipe 7 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
8	PIPE8NRDY	NRDY Interrupt Status for Pipe 8 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
9	PIPE9NRDY	NRDY Interrupt Status for Pipe 9 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R/W*1
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated in the bits in NRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

28.2.20 BEMPSTS : BEMP Interrupt Status Register

Base address: USBFS = 0x4009_0000

Offset address: 0x04A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9 BEMP	PIPE8 BEMP	PIPE7 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BEMP	BEMP Interrupt Status for Pipe 0 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
1	PIPE1BEMP	BEMP Interrupt Status for Pipe 1 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
2	PIPE2BEMP	BEMP Interrupt Status for Pipe 2 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
3	PIPE3BEMP	BEMP Interrupt Status for Pipe 3 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
4	PIPE4BEMP	BEMP Interrupt Status for Pipe 4 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
5	PIPE5BEMP	BEMP Interrupt Status for Pipe 5 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
6	PIPE6BEMP	BEMP Interrupt Status for Pipe 6 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
7	PIPE7BEMP	BEMP Interrupt Status for Pipe 7 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1

Bit	Symbol	Function	R/W
5	PIPE5NRDY	管道5的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
6	PIPE6NRDY	管道6的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
7	PIPE7NRDY	管道7的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
8	PIPE8NRDY	管道8的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
9	PIPE9NRDY	管道9的NRDY中断状态 0：未发生NRDY中断1：发生NRDY中断	R/W*1
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.要清除NRDYSTS中位中指示的状态，请仅将0写入要清除的位。将1写入其他位。

28.2.20 BEMPSTS:BEMP中断状态寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x04A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PIPE9 BEMP	PIPE8 BEMP	PIPE7 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PIPE0BEMP	管道0的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
1	PIPE1BEMP	管道1的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
2	PIPE2BEMP	管道2的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
3	PIPE3BEMP	管道3的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
4	PIPE4BEMP	管道4的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
5	PIPE5BEMP	管道5的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
6	PIPE6BEMP	管道6的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
7	PIPE7BEMP	管道7的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1

Bit	Symbol	Function	R/W
8	PIPE8BEMP	BEMP Interrupt Status for Pipe 8 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
9	PIPE9BEMP	BEMP Interrupt Status for Pipe 9 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R/W*1
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated in the bits in BEMPSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

28.2.21 FRMNUM : Frame Number Register

Base address: USBFS = 0x4009_0000

Offset address: 0x04C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FRNM[10:0]	Frame Number Latest frame number.	R
13:11	—	These bits are read as 0. The write value should be 0.	R/W
14	CRCE	Receive Data Error 0: No error occurred 1: Error occurred	R/W*1
15	OVRN	Overrun/Underrun Detection Status 0: No error occurred 1: Error occurred	R/W*1

Note 1. To clear the status, write 0 only to the bits to be cleared. Write 1 to the other bits.

FRNM[10:0] flags (Frame Number)

The USBFS sets the FRNM[10:0] flags to indicate the latest frame number, which is updated every 1 ms, when an SOF packet is issued or received.

CRCE flag (Receive Data Error)

The CRCE flag sets to 1 when a CRC error or bit stuffing error occurs during isochronous transfer. On detecting a CRC error in host controller mode, the USBFS generates an internal NRDY interrupt.

To clear the CRCE flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

OVRN flag (Overrun/Underrun Detection Status)

The OVRN flag sets to 1 when an overrun or underrun error occurs during isochronous transfer. To clear the flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

In host controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the time to issue an OUT token comes before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the time to issue an IN token comes when no FIFO buffer planes are empty

In device controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the IN token is received before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the OUT token is received when no FIFO buffer planes are empty

Bit	Symbol	Function	R/W
8	PIPE8BEMP	管道8的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
9	PIPE9BEMP	管道9的BEMP中断状态 0：未发生BEMP中断1：发生BEMP中断	R/W*1
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.要清除BEMPSTS中位指示的状态，请仅将0写入要清除的位。将1写入其他位。

28.2.21 FRMNUM:帧号寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x04C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRN	CRCE	—	—	—	FRNM[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FRNM[10:0]	帧号 最新帧号。	R
13:11	—	这些位被读取为0。写入值应为0。	R/W
14	CRCE	接收数据错误 0：未发生错误1：发生错误	R/W*1
15	OVRN	OverrunUnderrun检测状态 0：未发生错误1：发生错误	R/W*1

注1.要清除状态，只需将0写入要清除的位。将1写入其他位。

FRNM[10:0] flags (Frame Number)

USBFS设置FRNM[10:0]标志以指示最新的帧号，该帧号每1ms更新一次，当发出或接收SOF数据包时。

CRCE标志（接收数据错误）

当同步传输期间发生CRC错误或位填充错误时，CRCE标志设置为1。在主机控制器模式下检测到CRC错误时，USBFS会生成内部NRDY中断。

要清除CRCE标志，向其写入0，同时向FRMNUM寄存器中的其他位写入1。

OVRN标志（溢出欠载检测状态）

当同步传输期间发生溢出或欠载错误时，OVRN标志设置为1。要清除该标志，请向其写入0，同时向FRMNUM寄存器中的其他位写入1。

在主机控制器模式下，OVRN标志在以下任何条件下设置为1：

●对于传输同步管道，发出OUT令牌的时间是在所有传输数据写入FIFO缓冲区之前

●对于接收同步管道，在没有FIFO缓冲平面为空时发出IN令牌

在设备控制器模式下，OVRN标志在以下任何条件下设置为1：

●对于传输同步管道，在所有传输数据写入FIFO缓冲区之前接收到IN令牌

●对于接收同步管道，当没有FIFO缓冲平面为空时接收OUT令牌

RA生态工作室

28.2.22 DVCHGR : Device State Change Register

Base address: USBFS = 0x4009_0000

Offset address: 0x04E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0. The write value should be 0.	R/W
15	DVCHG	Device State Change 0: Disable writes to the USBADDR.STSRECOV[3:0] and USBADDR.USBADDR[6:0] bits 1: Enable writes to the USBADDR.STSRECOV[3:0] and USBADDR.USBADDR[6:0] bits	R/W

For details, see section 28.3.1.5. Release from deep software standby mode because of USB suspend/resume interrupts.

28.2.23 USBADDR : USB Address Register

Base address: USBFS = 0x4009_0000

Offset address: 0x050

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	STSRECOV[3:0]				—	USBADDR[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	USBADDR[6:0]	USB Address In device controller mode, these bits indicate the USB address assigned by the host when the USBFS processed the SET_ADDRESS request successfully.	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
11:8	STSRECOV[3:0]	Status Recovery 0x4: Recovery in device controller mode: Setting prohibited Recovery in host controller mode: Return to the low-speed state (bits DVSTCTR0.RHST[2:0] = 001b) 0x8: Recovery in device controller mode: Setting prohibited Recovery in host controller mode: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b) 0x9: Recovery in device controller mode: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 001b (default state) Recovery in host controller mode: Setting prohibited 0xA: Recovery in device controller mode: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 010b (address state) Recovery in host controller mode: Setting prohibited 0xB: Recovery in device controller mode: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 011b (configured state) Recovery in host controller mode: Setting prohibited Others: Setting prohibited	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

USBADDR[6:0] bits (USB Address)

In device controller mode, the USBADDR[6:0] flags indicate the USB address received when the USBFS processed a SetAddress request successfully. The USBFS sets the USBADDR[6:0] bits to 0x00 on detecting a USB bus reset.

28.2.22 DVCHGR:设备状态改变寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x04E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位被读取为0。写入值应为0。	R/W
15	DVCHG	设备状态更改 0：禁止写入USBADDR.STSRECOV[3:0]和USBADDR.USBADDR[6:0]位 1：允许写入USBADDR.STSRECOV[3:0]和USBADDR.USBADDR[6:0]位	R/W

有关详细信息，请参阅第28.3.1.5节。由于USB挂起恢复中断而从深度软件待机模式中释放。

28.2.23 USBADDR:USB地址寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x050

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	STSRECOV[3:0]				—	USBADDR[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	USBADDR[6:0]	USB地址 在设备控制器模式下，这些位指示USBFS成功处理SET_ADDRESS请求时主机分配的USB地址。	R/W
7	—	该位读取为0。写入值应为0。	R/W
11:8	STSRECOV[3:0]	状态恢复 0x4：设备控制器模式下的恢复：在主机控制器模式下设置禁止恢复： 返回低速状态（位DVSTCTR0.RHST[2:0]=001b） 0x8：设备控制器模式下的恢复：在主机控制器模式下设置禁止恢复： 返回全速状态（位DVSTCTR0.RHST[2:0]=010b） 0x9：设备控制器模式下的恢复： 返回全速状态（位DVSTCTR0.RHST[2:0]=010b），位INTSTS0.DVSQ[2:0] = 001b (default state) 主机控制器模式下的恢复：禁止设置 0xA：设备控制器模式下的恢复： 返回全速状态（位DVSTCTR0.RHST[2:0]=010b），位INTSTS0.DVSQ[2:0] = 010b (address state) 主机控制器模式下的恢复：禁止设置 0xB：设备控制器模式下的恢复： 返回全速状态（位DVSTCTR0.RHST[2:0]=010b），位INTSTS0.DVSQ[2:0] = 011b (configured state) 主机控制器模式下的恢复：禁止设置 其他：禁止设置	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W

USBADDR[6:0] bits (USB Address)

在设备控制器模式下，USBADDR[6:0]标志指示当USBFS处理一个SetAddress请求成功。USBFS在检测到USB总线复位时将USBADDR[6:0]位设置为0x00。

Writing to these bits is enabled while the DVCHGR.DVCHG bit is set to 1. On recovering from a USB power shut-off, the operation can resume from the USB address set before the software shut-off.

In host controller mode, the USBADDR[6:0] bits are invalid.

STSRECOV[3:0] bits (Status Recovery)

Use the STSRECOV[3:0] bits to resume the state of the internal sequencer on recovering from USB power shut-off. For details, see section 28.3.1.5. Release from deep software standby mode because of USB suspend/resume interrupts.

Writing to these bits is enabled while the DVCHGR.DVCHG bit is set to 1.

28.2.24 USBREQ : USB Request Type Register

Base address: USBFS = 0x4009_0000

Offset address: 0x054

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	BMREQUESTTYPE[7:0]	Request Type USB request bmRequestType value	R/W*1
15:8	BREQUEST[7:0]	Request USB request bRequest value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

USBREQ stores setup requests for control transfers.

In device controller mode, the USBREQ stores the received bRequest and bmRequestType values. In host controller mode, it sets to the bRequest and bmRequestType values to be transmitted.

USBREQ is initialized by a USB bus reset.

BMREQUESTTYPE[7:0] bits (Request Type)

The BMREQUESTTYPE[7:0] bits hold the bmRequestType value of USB requests.

- In host controller mode:

  Set these bits to the value of the USB request data in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:

  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

BREQUEST[7:0] bits (Request)

The BREQUEST[7:0] bits store bRequest value of the USB request.

- In host controller mode:

  Set these bits to the value of the USB request data in setup transmission transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:

  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

当DVCHGR.DVCHG位设置为1时，允许写入这些位。从USB电源关闭恢复后，操作可以从软件关闭前设置的USB地址恢复。

在主机控制器模式下，USBADDR[6:0]位无效。

STSRECOV[3:0] bits (Status Recovery)

使用STSRECOV[3:0]位在从USB电源关闭恢复时恢复内部定序器的状态。有关详细信息，请参阅第28.3.1.5节。由于USB挂起恢复中断而从深度软件待机模式中释放。

当DVCHGR.DVCHG位设置为1时，可以写入这些位。

28.2.24 USBREQ:USB请求类型寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x054

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	BMREQUESTTYPE[7:0]	请求类型 USB请求bmRequestType值	R/W*1
15:8	BREQUEST[7:0]	Request USB请求bRequest值	R/W*1

注1.在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

USBREQ存储控制传输的设置请求。

在设备控制器模式下，USBREQ存储接收到的bRequest和bmRequestType值。在主机控制器模式下，它设置为要传输的bRequest和bmRequestType值。

USBREQ由USB总线复位初始化。

BMREQUESTTYPE[7:0] bits (Request Type)

BMREQUESTTYPE[7:0]位保存USB请求的bmRequestType值。

●在主机控制器模式下：

在传输设置事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：

这些位指示接收设置事务中USB请求数据的值。写入位无效。

BREQUEST[7:0] bits (Request)

BREQUEST[7:0]位存储USB请求的bRequest值。

●在主机控制器模式下：

在设置传输事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：

这些位指示接收设置事务中USB请求数据的值。写入位无效。

28.2.25 USBVAL : USB Request Value Register

Base address: USBFS = 0x4009_0000

Offset address: 0x056

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WVALUE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WVALUE[15:0]	Value USB request wValue value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

In device controller mode, USBVAL stores the received wValue value. In host controller mode, it sets to the wValue value to be transmitted is set.

USBVAL is initialized by a USB bus reset.

WVALUE[15:0] bits (Value)

The WVALUE[15:0] bits store wValue value of the USB request.

- In host controller mode:

  Set these bits to the value of the wValue field in USB requests of transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:

  These bits indicate the wValue value of USB requests in reception setup transactions. Writing to the bits has no effect.

28.2.26 USBINDX : USB Request Index Register

Base address: USBFS = 0x4009_0000

Offset address: 0x058

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WINDEX[15:0]	Index USB request wIndex value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

USBINDX stores setup requests for control transfers.

In device controller mode, it stores the received wIndex value. In host controller mode, it sets to the wIndex value to be transmitted.

USBINDX is initialized by a USB bus reset.

WINDEX[15:0] bits (Index)

The WINDEX[15:0] bits hold the wIndex value of a USB request.

- In host controller mode:

28.2.25 USBVAL:USB请求值寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x056

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WVALUE[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WVALUE[15:0]	Value USB请求wValue值	R/W*1

注1.在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

在设备控制器模式下，USBVAL存储接收到的wValue值。在主机控制器模式下，它设置为要传输的wValue值。

USBVAL由USB总线复位初始化。

WVALUE[15:0] bits (Value)

WVALUE[15:0]位存储USB请求的wValue值。

●在主机控制器模式下：

将这些位设置为USB传输设置事务请求中wValue字段的值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：

这些位指示接收设置事务中USB请求的wValue值。写入位无效。

28.2.26 USBINDX:USB请求索引寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x058

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WINDEX[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WINDEX[15:0]	Index USB请求wIndex值	R/W*1

注1.在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

USBINDX存储控制传输的设置请求。

在设备控制器模式下，它存储接收到的wIndex值。在主机控制器模式下，它设置为要传输的wIndex值。

USBINDX由USB总线复位初始化。

WINDEX[15:0] bits (Index)

WINDEX[15:0]位保存USB请求的wIndex值。

●在主机控制器模式下：

Set these bits to the wIndex value in USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:

  These bits indicate the wIndex value in USB requests received in reception setup transactions. Writing to the bits has no effect.

28.2.27 USBLENG : USB Request Length Register

Base address: USBFS = 0x4009_0000

Offset address: 0x05A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WLENTUH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WLENTUH[15:0]	Length USB request wLength value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

USBLENG stores setup requests for control transfers.

In device controller mode, the value of wLength that is received is stored. In host controller mode, the value of wLength to be transmitted is set.

USBLENG is initialized by a USB bus reset.

WLENTUH[15:0] bits (Length)

The WLENTUH[15:0]bits hold the wLength value of a USB request.

- In host controller mode:

  Set these bits to the wLength value in USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:

  These bits indicate the wLength value in USB requests received in reception setup transactions. Writing to the bits has no effect.

28.2.28 DCPCFG : DCP Configuration Register

Base address: USBFS = 0x4009_0000

Offset address: 0x05C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	DIR	Transfer Direction*1 0: Data receiving direction 1: Data transmitting direction	R/W

在传输设置事务中将这些位设置为USB请求中的wIndex值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：

这些位指示在接收设置事务中收到的USB请求中的wIndex值。写入位无效。

28.2.27 USBLENG:USB请求长度寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x05A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WLENTUH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WLENTUH[15:0]	Length USB请求wLength值	R/W*1

注1.在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

USBLENG存储控制传输的设置请求。

在设备控制器模式下，存储接收到的wLength的值。在主机控制器模式下，设置要传输的wLength的值。

USBLENG由USB总线复位初始化。

WLENTUH[15:0] bits (Length)

WLENTUH[15:0]位保存USB请求的wLength值。

●在主机控制器模式下：

在传输设置事务中将这些位设置为USB请求中的wLength值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：

这些位指示在接收设置事务中收到的USB请求中的wLength值。写入位无效。

28.2.28 DCPCFG:DCP配置寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x05C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	DIR	传输方向*1 0：数据接收方向1：数据发送方向	R/W

Bit	Symbol	Function	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	SHTNAK	Pipe Disabled at End of Transfer*1 0: Keep pipe open after transfer ends 1: Disable pipe after transfer ends	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set this bit while the PID is NAK. Before setting this bit, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

DIR bit (Transfer Direction)

In host controller mode, the DIR bit sets the transfer direction of the data stage and status stage for control transfers. In device controller mode, set the DIR bit to 0.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change PID to NAK on transfer end when the selected pipe is receiving. It is only valid when the selected pipe is receiving.

When the SHTNAK bit is 1, the USBFS changes the DCPCTR.PID[1:0] bits for the DCP to NAK on determining that a transfer has ended. The USBFS determines transfer end on the following condition:

- A short packet, including a zero-length packet, is successfully received.

28.2.29 DCPMAXP : DCP Maximum Packet Size Register

Base address: USBFS = 0x4009_0000
Offset address: 0x05E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	MXPS[6:0]	Maximum Packet Size*1 Maximum data payload specification (maximum packet size) for the DCP	R/W
11:7	—	These bits are read as 0. The write value should be 0.	R/W
15:12	DEVSEL[3:0]	Device Select*2 0x0: Address 0000b 0x1: Address 0001b 0x2: Address 0010b 0x3: Address 0011b 0x4: Address 0100b 0x5: Address 0101b Others: Setting prohibited	R/W

Note 1. Only set the MXPS[6:0] bits while PID is NAK. Before setting these bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary. After the MXPS[6:0] bits are set and the DCP is set to the CURPIPE[3:0] bits in a port select register, clear the buffer by setting the BCLR bit in the port control register to 1.
Note 2. Only set the DEVSEL[3:0] bits while PID is NAK and the DCPCTR.SUREQ bit is 0. Before setting these bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

MXPS[6:0] bits (Maximum Packet Size)

The MXPS[6:0] bits specify the maximum data payload (maximum packet size) for the DCP. The initial value is 0x40 (64 bytes). Set the bits to a USB 2.0-compliant value. Do not write to the FIFO buffer or set PID = BUF whileMXPS[6:0] is set to 0.

Bit	Symbol	Function	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	SHTNAK	传输结束时管道禁用*1 0：传输结束后保持管道打开1：传输结束后禁用管道	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当PID为NAK时设置该位。在设置该位之前，请检查DCPCTR.PBUSY位是否为0，然后更改DCPCTR.PID[1:0]位用于DCP从BUF到NAK。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。

DIR位（传输方向）

在主机控制器模式下，DIR位设置控制传输的数据阶段和状态阶段的传输方向。在设备控制器模式下，将DIR位设置为0。

SHTNAK位（传输结束时禁用管道）

SHTNAK位指定当所选管道正在接收时，是否在传输结束时将PID更改为NAK。仅在所选管道正在接收时有效。

当SHTNAK位为1时，USBFS在确定传输已结束时将DCPCR.PID[1:0]位更改为DCP为NAK。USBFS在以下条件下确定传输结束：

●成功接收到短报文，包括零长度报文。

28.2.29 DCPMAXP:DCP最大数据包大小寄存器

Base address: USBFS = 0x4009_0000
Offset address: 0x05E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
重置后的值：	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	MXPS[6:0]	最大数据包大小*1 DCP的最大数据有效负载规范（最大数据包大小）	R/W
11:7	—	这些位被读取为0。写入值应为0。	R/W
15:12	DEVSEL[3:0]	设备选择*2 0x0: Address 0000b 0x1: Address 0001b 0x2: Address 0010b 0x3: Address 0011b 0x4: Address 0100b 0x5: Address 0101b 其他：禁止设置	R/W

注1.仅在PID为NAK时设置MXPS[6:0]位。在设置这些位之前，请检查DCPCTR.PBUSY位是否为0，然后将DCP的DCPCTR.PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。在设置MXPS[6:0]位并将DCP设置为端口选择寄存器中的CURPIPE[3:0]位后，通过将端口控制寄存器中的BCLR位设置为1来清除缓冲区。

注2.仅在PID为NAK且DCPCTR.SUREQ位为0时设置DEVSEL[3:0]位。在设置这些位之前，请检查DCPCTR.PBUSY位为0，然后将DCPCR.PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。

MXPS[6:0]位（最大数据包大小）

MXPS[6:0]位指定DCP的最大数据有效载荷（最大数据包大小）。初始值为0x40（64字节）。将这些位设置为符合USB2.0的值。当MXPS[6:0]设置为0时，不要写入FIFO缓冲区或设置PID=BUF。

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target peripheral device for a control transfer. Set up the device address in the associated DEVADDn (n = 0 to 5) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0000b.

28.2.30 DCPCTR : DCP Control Register

Base address: USBFS = 0x4009_0000

Offset address: 0x060

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	SUREQ	—	—	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	Response PID 0 0: NAK response 0 1: BUF response (depends on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
2	CCPL	Control Transfer End Enable 0: Disable control transfer completion 1: Enable control transfer completion	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	PBUSY	Pipe Busy 0: DCP not used for the USB bus 1: DCP in use for the USB bus	R
6	SQMON	Sequence Toggle Bit Monitor 0: DATA0 1: ATA1	R
7	SQSET	Sequence Toggle Bit Set*2 Sets the sequence toggle bit in DCP transfers. This bit is read as 0. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1	R/W*1
8	SQCLR	Sequence Toggle Bit Clear*2 Clears the sequence toggle bit in DCP transfers. This bit is read as 0. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0	R/W*1
10:9	—	These bits are read as 0. The write value should be 0.	R/W
11	SUREQCLR	SUREQ Bit Clear Clears the SUREQ bit in host controller mode. This bit is read as 0. 0: Invalid (writing 0 has no effect) 1: Clear SUREQ to 0	R/W
13:12	—	These bits are read as 0. The write value should be 0.	R/W
14	SUREQ	Setup Token Transmission Sets up token transmission in host controller mode. 0: Invalid (writing 0 has no effect) 1: Transmit setup packet	R/W
15	BSTS	Buffer Status 0: Buffer access disabled 1: Buffer access enabled	R

DEVSEL[3:0] bits (Device Select)

在主机控制器模式下，DEVSEL[3:0]位指定目标外围设备的地址以进行控制传输。首先在相关的DEVADDn（n=0到5）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0000b。

28.2.30 DCPCTR:DCP控制寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x060

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	SUREQ	—	—	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	响应PID 00：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应	R/W
2	CCPL	控制传输结束使能 0：禁止控制传输完成1：使能控制传输完成	R/W
4:3	—	这些位被读取为0。写入值应为0。	R/W
5	PBUSY	管道忙 0：USB总线不使用DCP1：USB总线使用DCP	R
6	SQMON	序列切换位监视器 0: DATA0 1: ATA1	R
7	SQSET	序列切换位设置*2 设置DCP传输中的序列切换位。 该位读为0。 0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1	R/W*1
8	SQCLR	序列切换位清除*2 清除DCP传输中的序列切换位。 该位读为0。 0：无效（写0无效）1：清除下一笔交易的期望值到DATA0	R/W*1
10:9	—	这些位被读取为0。写入值应为0。	R/W
11	SUREQCLR	SUEQ位清零 在主机控制器模式下清除SUREQ位。 该位读为0。 0：无效（写0无效）1：清除SUREQ为0	R/W
13:12	—	这些位被读取为0。写入值应为0。	R/W
14	SUREQ	设置令牌传输 在主机控制器模式下设置令牌传输。 0：无效（写0无效）1：发送设置包	R/W
15	BSTS	缓冲区状态 0：禁止缓冲区访问1：允许缓冲区访问	R

Note 1. This bit is read as 0.
Note 2. Only set the SQSET and SQCLR bits while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

PID[1:0] bits (Response PID)

The PID[1:0] bits control the USB response type during control transfers.

In host controller mode, to change the PID[1:0] setting from NAK to BUF:

- When the transmitting direction is set:
  a. Write all of the transmit data to the FIFO buffer while the DVSTCTR0.UACT bit is 1 and PID is NAK.
  b. Set PID[1:0] bits to 01b (BUF).
     The USBFS then executes the OUT transaction.
- When the receiving direction is set:
  a. Check that the FIFO buffer is empty (or empty the buffer) while the DVSTCTR0.UACT bit is 1 and PID is NAK.
  b. Set PID[1:0] bits to 01b (BUF).
     The USBFS then executes the IN transaction.

The USBFS changes the PID[1:0] setting as follows:

- When the PID[1:0] bits are set to BUF (01b) by software and the USBFS has received data exceeding MaxPacketSize, the USBFS sets the PID[1:0] to STALL (11b)
- When a reception error, such as a CRC error, is detected three times consecutively, the USBFS sets thePID[1:0] bits to NAK (00b)
- On receiving the STALL handshake, the USBFS sets PID[1:0] to STALL (11b)

In device controller mode, the USBFS changes the PID[1:0] setting as follows:

- On receiving a setup packet, the USBFS sets PID[1:0] to NAK (00b). The USBFS then sets the INTSTS0.VALID flag to 1, and the PID[1:0] setting cannot be changed until the software clears the VALID flag to 0.
- When the PID[1:0] bits are set to BUF (01b) by software and the USBFS has received data exceeding MaxPacketSize, the USBFS sets PID[1:0] to STALL (11b)
- On detecting a control transfer sequence error, the USBFS sets PID[1:0] to STALL (1xb)
- On detecting a USB bus reset, the USBFS sets PID[1:0] to NAK

The USBFS does not check the PID[1:0] setting while processing a SET_ADDRESS request.

The PID[1:0] bits are initialized by a USB bus reset.

CCPL bit (Control Transfer End Enable)

In device controller mode, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed. When the bit is set to 1 by software while the associated PID[1:0] bits are set to BUF, the USBFS completes the control transfer status stage.

During control read transfers, the USBFS transmits the ACK handshake in response to the OUT transaction from the USB host. During control write or no-data control transfers, it transmits the zero-length packet in response to the IN transaction from the USB host. On detecting a SET_ADDRESS request, the USBFS operates in auto response mode from the setup stage up to status stage completion regardless of the CCPL bit setting.

The USBFS changes the CCPL bit from 1 to 0 on receiving a new setup packet. The software cannot write 1 to the bit while the INTSTS0.VALID bit is 1. The bit is initialized by a USB bus reset.

In host controller mode, always write 0 to the CCPL bit.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether DCP is used for the transaction when USBFS changes the PID[1:0] bits from BUF to NAK. The USBFS changes the PBUSY bit from 0 to 1 on start of a USB transaction for the selected pipe. It changes the PBUSY bit from 1 to 0 on completion of one transaction.

注1.该位读为0。
注2.仅在PID为NAK时设置SQSET和SQCLR位。在设置这些位之前，请检查PBUSY位是否为0，然后将DCP的PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。

PID[1:0] bits (Response PID)

PID[1:0]位在控制传输期间控制USB响应类型。

在主机控制器模式下，要将PID[1:0]设置从NAK更改为BUF：

●设置传输方向时：

a. 当DVSTCTR0.UACT位为1且PID为NAK时，将所有发送数据写入FIFO缓冲区。

湾。将PID[1:0]位设置为01b(BUF)。

然后USBFS执行OUT事务。

●设置接收方向时：

a. 在DVSTCTR0.UACT位为1且PID为NAK时检查FIFO缓冲区是否为空（或清空缓冲区）。

湾。将PID[1:0]位设置为01b(BUF)。

然后USBFS执行IN事务。

USBFS更改PID[1:0]设置如下：

●当PID[1:0]位被软件设置为BUF(01b)并且USBFS接收到超过MaxPacketSize的数据时，USBFS将PID[1:0]设置为STALL(11b)

●当连续3次检测到接收错误（例如CRC错误）时，USBFS将PID[1:0]位设置为NAK(00b)

●在接收到STALL握手时，USBFS将PID[1:0]设置为STALL(11b)

在设备控制器模式下，USBFS将PID[1:0]设置更改如下：

●在接收到设置数据包时，USBFS将PID[1:0]设置为NAK(00b)。然后USBFS将INTSTS0.VALID标志设置为1，并且在软件将VALID标志清除为0之前无法更改PID[1:0]设置。

●当PID[1:0]位被软件设置为BUF(01b)并且USBFS接收到超过MaxPacketSize的数据时，USBFS将PID[1:0]设置为STALL(11b)

●在检测到控制传输序列错误时，USBFS将PID[1:0]设置为STALL(1xb)

●在检测到USB总线复位时，USBFS将PID[1:0]设置为NAK

USBFS在处理SET_ADDRESS请求时不检查PID[1:0]设置。

PID[1:0]位由USB总线复位初始化。

CCPL位（控制传输结束使能）

在设备控制器模式下，将CCPL位设置为1可以完成控制传输的状态阶段。当该位由软件设置为1且相关的PID[1:0]位设置为BUF时，USBFS完成控制传输状态阶段。

在控制读取传输期间，USBFS发送ACK握手以响应来自USB主机的OUT事务。在控制写入或无数据控制传输期间，它传输零长度数据包以响应来自USB主机的IN事务。在检测到SET_ADDRESS请求时，USBFS从设置阶段到状态阶段完成以自动响应模式运行，无论CCPL位设置如何。

USBFS在接收到新的设置数据包时将CCPL位从1更改为0。当INTSTS0.VALID位为1时，软件无法向该位写入1。该位由USB总线复位初始化。

在主机控制器模式下，始终将0写入CCPL位。

PBUSY bit (Pipe Busy)

PBUSY位指示当USBFS将PID[1:0]位从BUF更改为NAK时是否使用DCP进行事务处理。USBFS在所选管道的USB事务开始时将PBUSY位从0更改为1。它改变了

PBUSY位在一个事务完成时从1变为0。

After PID is set to NAK by software, the value in the PBUSY bit indicates whether changes to pipe settings can proceed.

For details, see section 28.3.4.1. Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Monitor)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

The USBFS toggles the bit on normal completion of the transaction. It does not toggle the bit, however, when a DATAPID mismatch occurs during a transfer in the receiving direction.

In device controller mode, the USBFS sets the SQMON bit to 1 (specifies DATA1 as the expected value) on successful reception of the setup packet.

In device controller mode, the USBFS does not reference this bit during IN or OUT transactions at the status stage, and it does not toggle the bit on normal completion.

SQSET bit (Sequence Toggle Bit Set)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR bit (Sequence Toggle Bit Clear)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer. It is read as 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR bit (SUREQ Bit Clear)

In host controller mode, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The bit is read as 0.

If transfer stops while the SUREQ bit is set to 1 in a setup transaction, set the SUREQCLR bit to 1 by software. This is not necessary at the end of a normal setup transaction, because the USBFS automatically clears the SUREQ bit to 0.

Only control the SUREQ bit through the SUREQCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a bus disconnection was detected.

In device controller mode, always write 0 to this bit.

SUREQ bit (Setup Token Transmission)

In host controller mode, setting the SUREQ bit to 1 triggers the USBFS to transmit the setup packet. After completing the setup transaction process, the USBFS generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0. The USBFS also clears the SUREQ bit to 0 when the software sets the SUREQCLR bit to 1.

Before setting the SUREQ bit to 1, set the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the target USB request in the setup transaction. Also check that the PID[1:0] bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not change the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is complete (SUREQ bit = 1). Write 1 to the SUREQ bit only when transmitting the setup token. Otherwise, write 0.

In device controller mode, always write 0 to this bit.

BSTS flag (Buffer Status)

The BSTS flag indicates the status of access to the DCP FIFO buffer. The meaning of this flag varies as follows depending on the CFIFOSEL.ISEL setting:

- When ISEL = 0, the bit indicates whether receive data can be read from the buffer
- When ISEL = 1, the bit indicates whether transmit data can be written to the buffer

在软件将PID设置为NAK后，PBUSY位中的值指示是否可以继续对管道设置进行更改。

详见28.3.4.1节。管道控制寄存器切换程序。

SQMON位（序列切换位监视器）

SQMON位指示DCP传输期间下一个事务的序列切换位的预期值。

USBFS在事务正常完成时切换该位。但是，当在接收方向的传输过程中发生DATAPID不匹配时，它不会切换该位。

在设备控制器模式下，USBFS在成功接收到设置数据包时将SQMON位设置为1（指定DATA1作为预期值）。

在设备控制器模式下，USBFS在状态阶段的IN或OUT事务期间不引用该位，并且它不会在正常完成时切换该位。

SQSET位（序列切换位设置）

SQSET位将DATA1指定为DCP传输期间下一个事务的序列切换位的预期值。

不要同时将SQCLR和SQSET位设置为1。

SQCLR位（序列翻转位清除）

SQCLR位将DATA0指定为DCP传输期间下一个事务的序列切换位的预期值。读为0。

不要同时将SQCLR和SQSET位设置为1。

SUREQCLR bit (SUREQ Bit Clear)

在主机控制器模式下，将SUREQCLR位设置为1会将SUREQ位清除为0。该位被读取为0。

如果在设置事务中将SUREQ位设置为1时传输停止，则通过软件将SUREQCLR位设置为1。这在正常设置事务结束时不是必需的，因为USBFS会自动将SUREQ位清除为0。

当DVSTCTR0.UACT位为0时，仅通过SUREQCLR位控制SUREQ位。当UACT为0时，由于检测到总线断开，通信停止或没有传输发生。

在设备控制器模式下，始终向该位写入0。

SURESQ位（设置令牌传输）

在主机控制器模式下，将SUREQ位设置为1会触发USBFS发送设置数据包。完成设置事务处理后，USBFS产生SACK或SIGN中断并将SUREQ位清零。当软件将SUREQCLR位设置为1时，USBFS也将SUREQ位清零。

在将SUREQ位设置为1之前，将DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX和USBLENG适当地在设置事务中传输目标USB请求。还要检查DCP的PID[1:0]位是否设置为NAK。将SUREQ位设置为1后，在设置事务完成（SUREQ位=1）之前，不要更改DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX或USBLENG。仅在发送设置令牌时向SUREQ位写入1。否则，写0。

在设备控制器模式下，始终向该位写入0。

BSTS flag (Buffer Status)

BSTS标志指示访问DCPFIFO缓冲区的状态。根据CFIFOSEL.ISEL设置，该标志的含义如下：

- ISEL=0时，该位指示是否可以从缓冲区读取接收数据
- ISEL=1时，该位指示发送数据是否可以写入缓冲区

28.2.31 PIPESEL : Pipe Window Select Register

Base address: USBFS = 0x4009_0000

Offset address: 0x064

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PIPESEL[3:0]	Pipe Window Select 0x0: No pipe selected 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3 0x4: Pipe 4 0x5: Pipe 5 0x6: Pipe 6 0x7: Pipe 7 0x8: Pipe 8 0x9: Pipe 9 Others: Setting prohibited	R/W
15:4	—	These bits are read as 0. The write value should be 0.	R/W

Set pipes 1 to 9 using the PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN registers (n = 0 to 9).

After selecting the pipe in the PIPESEL register, pipe functions must be set in the associated PIPECFG, PIPEMAXP, and PIPEPERI registers. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set independently of the pipe selection in this register.

PIPESEL[3:0] bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number associated with the PIPECFG, PIPEMAXP, and PIPEPERI registers used for data writing and reading. Selecting a pipe number in the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI associated with the selected pipe number.

When PIPESEL[3:0] = 0000b, 0 is read from all of the bits in PIPECFG, PIPEMAXP, and PIPEPERI. Writing to these bits has no effect.

28.2.32 PIPECFG : Pipe Configuration Register

Base address: USBFS = 0x4009_0000

Offset address: 0x068

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	EPNUM[3:0]	Endpoint Number*1 Specifies the endpoint number for the selected pipe. Setting 0000b indicates that the pipe is not used.	R/W
4	DIR	Transfer Direction*2 *3 0: Receiving direction 1: Transmitting direction	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W

28.2.31 PIPESEL:管道窗口选择寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x064

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PIPESEL[3:0]	管道窗口选择 0x0：未选择管道0x1：管道10x2：管道20x3：管道30x4：管道40x5：管道50x6：管道60x7：管道70x8：管道80x9：管道9 其他：禁止设置	R/W
15:4	—	这些位被读取为0。写入值应为0。	R/W

使用PIPESEL、PIPECFG、PIPEMAXP、PIPEPERI、PIPEnCTR、PIPEnTRE和PIPEnTRN寄存器（n=0到9）设置管道1到9。

在PIPESEL寄存器中选择管道后，必须在相关的PIPECFG、PIPEMAXP和PIPEPERI寄存器。PIPEnCTR、PIPEnTRE和PIPEnTRN可以独立于该寄存器中的管道选择进行设置。

PIPESEL[3:0]位（管道窗口选择）

PIPESEL[3:0]位选择与用于数据写入和读取的PIPECFG、PIPEMAXP和PIPEPERI寄存器相关的管道编号。在PIPESEL[3:0]位中选择一个管道编号允许写入和读取与所选管道编号相关的PIPECFG、PIPEMAXP和PIPEPERI。

当PIPESEL[3:0]=0000b时，从PIPECFG、PIPEMAXP和PIPEPERI中的所有位读取0。写入这些位无效。

28.2.32 PIPECFG:管道配置寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x068

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	EPNUM[3:0]	端点编号*1 指定选定管道的端点编号。设置0000b表示不使用管道。	R/W
4	DIR	传输方向*2*3 0：接收方向1：发送方向	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	SHTNAK	Pipe Disabled at End of Transfer*1 0: Continue pipe operation after transfer ends 1: Disable pipe after transfer ends	R/W
8	—	This bit is read as 0. The write value should be 0.	R/W
9	DBLB	Double Buffer Mode*2 *3 0: Single buffer 1: Double buffer	R/W
10	BFRE	BRDY Interrupt Operation Specification*2 *3 0: Generate BRDY interrupt on transmitting or receiving data 1: Generate BRDY interrupt on completion of reading data	R/W
13:11	—	These bits are read as 0. The write value should be 0.	R/W
15:14	TYPE[1:0]	Transfer Type*1 0 0: Pipe not used 0 1: Pipes 1 and 2: Bulk transfer Pipes 3 to 5: Bulk transfer Pipes 6 to 9: Setting prohibited 1 0: Pipes 1 and 2: Setting prohibited Pipes 3 to 5: Setting prohibited Pipes 6 to 9: Interrupt transfer 1 1: Pipes 1 and 2: Isochronous transfer Pipes 3 to 5: Setting prohibited Pipes 6 to 9: Setting prohibited	R/W

Note 1. Only set the TYPE[1:0], SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 2. Only set the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 3. To change the BFRE, DBLB, or DIR bits after completing USB communication on the selected pipe, in addition to the constraints described in Note 2, write 1 and 0 to the PIPEnCTR.ACLRM bit continuously through the software and clear the FIFO buffer assigned to the pipe.

PIPECFG specifies the transfer type, FIFO buffer access direction, and endpoint numbers for pipes 1 to 9. It also selects single or double buffer mode, and whether to continue or disable pipe operation at the end of transfer.

EPNUM[3:0] bits (Endpoint Number)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe. Setting 0000b indicates the pipe not used.

Set these bits so that the combination of the DIR and EPNUM[3:0] settings is different from those for other pipes. The EPNUM[3:0] bits can be set to 0000b for all pipes.

DIR bit (Transfer Direction)

The DIR bit specifies the transfer direction for the selected pipe.

When the software sets this bit to 0, the USBFS uses the selected pipe for receiving. When the software sets this bit to 1, the USBFS uses the selected pipe for transmitting.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change the PIPEnCTR.PID[1:0] bits to 00b (NAK) at the end of transfer when the selected pipe is set in the receiving direction. The bit is valid for pipes 1 to 5 in the receiving direction.

When the software sets this bit to 1 for a receiving pipe, the USBFS changes the associated PIPEnCTR.PID[1:0] bits to 00b (NAK) on determining the transfer end. The USBFS determines that the transfer has ended on the following conditions:

- A short packet data (including a zero-length packet) was successfully received
- The transaction counter is used and the number of packets specified for the transaction counter are successfully received

Bit	Symbol	Function	R/W
7	SHTNAK	传输结束时管道禁用*1 0：传输结束后继续管道操作1：传输结束后禁用管道	R/W
8	—	该位读取为0。写入值应为0。	R/W
9	DBLB	双缓冲模式*2*3 0：单缓冲区1：双缓冲区	R/W
10	BFRE	BRDY中断操作规范*2*3 0：发送或接收数据时产生BRDY中断1：读取数据完成时产生BRDY中断	R/W
13:11	—	这些位被读取为0。写入值应为0。	R/W
15:14	TYPE[1:0]	传输类型*1 00：未使用管道01：管道1和2：批量传输管道3到5：批量传输 管道6至9：禁止设置 10：管道1和2：设置禁止管道3至5：设置禁止管道6至9：中断传输 11：管道1和2：同步传输管道3至5：禁止设置管道6至9：禁止设置	R/W

注1.PID为NAK时，仅设置TYPE[1:0]、SHTNAK和EPNUM[3:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

注2.仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置BFRE、DBLB和DIR位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

注3.要在选定管道上完成USB通信后更改BFRE、DBLB或DIR位，除了注2中描述的约束外，通过软件连续向PIPEnCTR.ACLRM位写入1和0并清除FIFO分配给管道的缓冲区。

PIPECFG指定管道1到9的传输类型、FIFO缓冲区访问方向和端点编号。它还选择单缓冲区或双缓冲区模式，以及在传输结束时是继续还是禁用管道操作。

EPNUM[3:0] bits (Endpoint Number)

EPNUM[3:0]位指定所选管道的端点号。设置0000b表示管道未使用。

设置这些位，以便DIR和EPNUM[3:0]设置的组合不同于其他管道的设置。这对于所有管道，EPNUM[3:0]位可以设置为0000b。

DIR位（传输方向）

DIR位指定所选管道的传输方向。

当软件将此位设置为0时，USBFS使用所选管道进行接收。当软件将该位设置为1时，USBFS使用选定的管道进行传输。

SHTNAK位（传输结束时禁用管道）

SHTNAK位指定当所选管道设置为接收方向时，是否在传输结束时将PIPEnCTR.PID[1:0]位更改为00b(NAK)。该位对接收方向的管道1到5有效。

当软件将该位设置为1用于接收管道时，USBFS在确定传输结束时将相关的PIPEnCTR.PID[1:0]位更改为00b(NAK)。USBFS在以下条件下确定传输已结束：

- 成功接收短包数据（包括零长度包）
- 使用事务计数器，成功接收事务计数器指定的包数

DBLB bit (Double Buffer Mode)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe. The bit is valid for pipes 1 to 5.

BFRE bit (BRDY Interrupt Operation Specification)

The BFRE bit specifies the BRDY interrupt generation timing from the USBFS to the CPU for the selected pipe.

When the software sets the BFRE bit to 1 and the selected pipe is in the receiving direction, the USBFS detects the transfer completion and generates the BRDY interrupt on reading the packet.

When a BRDY interrupt is generated with this setting, the software must write 1 to the BCLR bit in the port control register. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.

When the BFRE bit is set to 1 by software and the selected pipe is in the transmitting direction, the USBFS does not generate the BRDY interrupt. For details, see section 28.3.3.1. BRDY interrupt.

TYPE[1:0] bits (Transfer Type)

The TYPE[1:0] bits specify the transfer type for the pipe selected in the PIPESEL.PIPESEL[3:0] bits. Before setting PID to BUF and starting USB communication on the selected pipe, set the TYPE[1:0] bits to a value other than 00b.

28.2.33 PIPEMAXP : Pipe Maximum Packet Size Register

Base address: USBFS = 0x4009_0000

Offset address: 0x06C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	MXPS[8:0]	Maximum Packet Size*1 • Pipes 1 and 2 1 byte (0x001) to 256 bytes (0x100) (Bit [9] not supported.) • Pipes 3 to 5 8 bytes (0x008), 16 bytes (0x010), 32 bytes (0x020), 64 bytes (0x040) (Bits [9:7] and [2:0] not supported.) • Pipes 6 to 9 1 byte (0x001) to 64 bytes (0x040) (Bits [9:7] not supported.)	R/W
11:9	—	These bits are read as 0. The write value should be 0.	R/W
15:12	DEVSEL[3:0]	Device Select*2 0x0: Address 0000b 0x1: Address 0001b 0x2: Address 0010b 0x3: Address 0011b 0x4: Address 0100b 0x5: Address 0101b Others: Setting prohibited	R/W

Note: The value of the MXPS[8:0] bits is 0x000 when no pipe is selected in the PIPESEL.PIPESEL[3:0] bits and 0x040 when a pipe is selected.

Note 1. Only set the MXPS[8:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 2. Only set the DEVSEL[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00b (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PIPEMAXP specifies the maximum packet size for pipes 1 to 9.

DBLB位（双缓冲模式）

DBLB位为所选管道使用的FIFO缓冲区选择单缓冲区模式或双缓冲区模式。该位对管道1到5有效。

BFRE位（BRDY中断操作规范）

BFRE位为所选管道指定从USBFS到CPU的BRDY中断生成时序。

当软件将BFRE位设置为1且所选管道处于接收方向时，USBFS检测到传输完成并在读取数据包时产生BRDY中断。

当使用该设置产生BRDY中断时，软件必须将1写入端口控制寄存器中的BCLR位。
在将1写入BCLR位之前，分配给所选管道的FIFO缓冲区不会用于接收。

当BFRE位由软件设置为1且所选管道处于发送方向时，USBFS不会产生BRDY中断。详见28.3.3.1节。BRDY中断。

TYPE[1:0] bits (Transfer Type)

TYPE[1:0]位指定在PIPESEL.PIPESEL[3:0]位中选择的管道的传输类型。设置PID之前BUF并在所选管道上启动USB通信，将TYPE[1:0]位设置为00b以外的值。

28.2.33 PIPEMAXP:管道最大数据包大小寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x06C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	MXPS[8:0]	最大数据包大小*1 • 管道1和2 1字节(0x001)到256字节(0x100)（不支持位[9]。） • 管道3至5 8字节(0x008)、16字节(0x010)、32字节(0x020)、64字节(0x040)（不支持位[9:7]和[2:0]。） • 管道6至9 1字节(0x001)到64字节(0x040)（不支持位[9:7]。）	R/W
11:9	—	这些位被读取为0。写入值应为0。	R/W
15:12	DEVSEL[3:0]	设备选择*2 0x0: Address 0000b 0x1: Address 0001b 0x2: Address 0010b 0x3: Address 0011b 0x4: Address 0100b 0x5: Address 0101b 其他：禁止设置	R/W

Note: ThevalueoftheMXPS[8:0]bitsis0x000whennopipeisselectedinthePIPESEL.PIPESEL[3:0]bitsand0x040whenapipeisselected.

注1.仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置MXPS[8:0]位。
在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

注2.仅在PID为NAK时设置DEVSEL[3:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00b(NAK)，则无需通过软件检查PBUSY位。

PIPEMAXP指定管道1到9的最大数据包大小。

MXPS[8:0] bits (Maximum Packet Size)

The MXPS[8:0] bits specify the maximum data payload (maximum packet size) for the selected pipe.

Set these bits to the appropriate value for each transfer type based on the USB 2.0 specification. When MXPS[8:0] = 0, do not write to the FIFO buffer or set PID to BUF. These writes have no effect.

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target device for USB communication. Set up the device address in the associated DEVADDn (n = 0 to 5) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0x2, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0x0.

28.2.34 PIPEPERI : Pipe Cycle Control Register

Base address: USBFS = 0x4009_0000

Offset address: 0x06E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	IITV[2:0]*1	Interval Error Detection Interval Specifies the interval error detection timing for the selected pipe as the n-th power of 2 of the frame timing	R/W
11:3	—	These bits are read as 0. The write value should be 0.	R/W
12	IFIS	Isochronous IN Buffer Flush 0: Do not flush buffer 1: Flush buffer	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set the IITV[2:0] bits while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PIPEPERI selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfers, and sets the interval error detection interval for pipes 1 to 9.

IITV[2:0] bits (Interval Error Detection Interval)

To change the IITV[2:0] bits to another value after they are set and USB communication is performed, set the PIPEnCTR.PID[1:0] bits to 00b (NAK) and then set the PIPEnCTR.ACLRM bit to 1 to initialize the interval timer.

The IITV[2:0] bits are not provided for pipes 3 to 5. Write 000b to bit positions of the IITV[2:0] bits associated with pipes 3 to 5.

IFIS bit (Isochronous IN Buffer Flush)

The IFIS bit specifies whether to flush the buffer when the pipe selected in the PIPESEL.PIPESEL[3:0] bits is used for isochronous IN transfers.

In device controller mode when the selected pipe is for isochronous IN transfers, the USBFS automatically clears the FIFO buffer if the USBFS fails to receive the IN token from the USB host within the interval set in theIITV[2:0] bits in terms of frames.

When double buffering is specified (PIPECFG.DBLB = 1), the USBFS only clears the data in the previously used plane.

The USBFS clears the FIFO buffer on receiving the SOF packet immediately after the frame in which the USBFS expected to receive the IN token. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time the SOF packet is expected to be received by using the internal interpolation function.

In host controller mode, set the IITV[2:0] bits to 000b.

MXPS[8:0]位（最大数据包大小）

MXPS[8:0]位指定所选管道的最大数据有效负载（最大数据包大小）。

根据USB2.0规范将这些位设置为每种传输类型的适当值。当MXPS[8:0]=0时，不要写入FIFO缓冲区或将PID设置为BUF。这些写入没有效果。

DEVSEL[3:0] bits (Device Select)

在主机控制器模式下，DEVSEL[3:0]位指定USB通信的目标设备的地址。首先在相关的DEVADDn（n=0到5）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0x2，首先设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0x0。

28.2.34 PIPEPERI:管道循环控制寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x06E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	IITV[2:0]*1	间隔错误检测间隔 将所选管道的间隔错误检测时间指定为帧时间的2的n次方	R/W
11:3	—	这些位被读取为0。写入值应为0。	R/W
12	IFIS	同步IN缓冲区刷新 0：不刷新缓冲区1： 刷新缓冲区	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W

注1.仅在PID为NAK时设置IITV[2:0]位。在设置这些位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

PIPEPERI选择在同步IN传输期间发生间隔错误时是否刷新缓冲区，并设置管道1到9的间隔错误检测间隔。

IITV[2:0]位（间隔错误检测间隔）

要在设置IITV[2:0]位并在执行USB通信后将其更改为另一个值，请设置PIPEnCTR.PID[1:0]位为00b(NAK)，然后将PIPEnCTR.ACLRM位设置为1以初始化间隔定时器。

不为管道3到5提供IITV[2:0]位。将000b写入与管道3到5相关联的IITV[2:0]位的位位置。

IFIS位（同步IN缓冲区刷新）

IFIS位指定当在PIPESEL.PIPESEL[3:0]位中选择的管道用于同步IN传输时是否刷新缓冲区。

在设备控制器模式下，当所选管道用于同步IN传输时，如果USBFS未能在IITV[2:0]位（以帧为单位）设置的间隔内从USB主机接收IN令牌，则USBFS自动清除FIFO缓冲区.

当指定双缓冲时（PIPECFG.DBLB=1），USBFS只清除先前使用的平面中的数据。

在USBFS预期接收IN令牌的帧之后，USBFS在接收到SOF数据包后立即清除FIFO缓冲区。即使SOF数据包损坏，FIFO缓冲区也会在预期接收SOF数据包时使用内部插值功能清除。

在主机控制器模式下，将IITV[2:0]位设置为000b。

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Set the IITV[2:0] bits to 000b when the selected pipe is not used for isochronous transfers.

28.2.35 PIPEnCTR : PIPEn Control Registers (n = 1 to 5)

Base address: USBFS = 0x4009_0000

Offset address: 0x070 + 0x2 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	Response PID 0 0: NAK response 0 1: BUF response (depends buffer state) 1 0: STALL response 1 1: STALL response	R/W
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	PBUSY	Pipe Busy 0: Pipe n not in use for the transaction 1: Pipe n in use for the transaction	R
6	SQMON	Sequence Toggle Bit Confirmation 0: DATA0 1: DATA1	R
7	SQSET	Sequence Toggle Bit Set*2 Sets the sequence toggle bit for pipe n. This bit is read as 0. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1	R/W*1
8	SQCLR	Sequence Toggle Bit Clear*2 Clears the sequence toggle bit for pipe n. This bit is read as 0. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0	R/W*1
9	ACLRM	Auto Buffer Clear Mode*3 0: Disable 1: Enable (initialize all buffers)	R/W
10	ATREPM	Auto Response Mode*2 0: Disable auto response mode 1: Enable auto response mode	R/W
13:11	—	These bits are read as 0. The write value should be 0.	R/W
14	INBUFM	Transmit Buffer Monitor 0: No data to be transmitted is in the FIFO buffer 1: Data to be transmitted is in the FIFO buffer	R
15	BSTS	Buffer Status 0: Buffer access by the CPU disabled 1: Buffer access by the CPU enabled	R

Note 1. Only 0 can be read.

Note 2. Only set the ATREPM bit or write 1 to the SQCLR or SQSETbit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSYbit through the software is not necessary.

Note 3. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PIPEnCTR can be set for any pipe selection in the PIPESEL register.

当所选管道不用于同步传输时，将IITV[2:0]位设置为000b。

28.2.35 PIPEnCTR:PIPEn控制寄存器(n=1到5)

Base address: USBFS = 0x4009_0000

Offset address: 0x070 + 0x2 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	响应PID 00：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应	R/W
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	PBUSY	管道忙 0：管道n未用于事务1：管道n正在用于事务	R
6	SQMON	序列切换位确认 0: DATA0 1: DATA1	R
7	SQSET	序列切换位设置*2 设置管道n的序列切换位。 该位读为0。 0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1	R/W*1
8	SQCLR	序列切换位清除*2 清除管道n的序列切换位。 该位读为0。 0：无效（写0无效）1：清除下一笔交易的期望值到DATA0	R/W*1
9	ACLRM	自动缓冲区清除模式*3 0：禁用1：启用（初始化所有缓冲区）	R/W
10	ATREPM	自动响应模式*2 0：禁用自动响应模式1：启用自动响应模式	R/W
13:11	—	这些位被读取为0。写入值应为0。	R/W
14	INBUFM	发送缓冲区监视器 0：FIFO缓冲区中没有要发送的数据1：FIFO缓冲区中没有要发送的数据	R
15	BSTS	缓冲区状态 0：禁止CPU访问缓冲区1：允许CPU访问缓冲区	R

注1.只能读取0。

注2.PID为NAK时，仅设置ATREPM位或向SQCLR或SQSET位写入1。在设置这些位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

注3.仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。在设置该位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

PIPEnCTR可以为PIPESEL寄存器中的任何管道选择设置。

PID[1:0] bits (Response PID)

The PID[1:0]bits specify the response type for the next transaction on the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USB transfer. Table 28.9 and Table 28.10 show the basic operations of the USBFS (when there are no errors in the communication packets) based on the PID[1:0] bit setting.

After changing the PID[1:0] setting from BUF to NAK through the software during USB communication on the selected pipe, check that the PBUSY bit is 1 to see if USB transfer on the pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through the software is not necessary.

The USBFS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBFS sets PID to NAK on recognizing completion of the transfer when the selected pipe is in the receiving direction and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software
- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBFS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBFS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode

To specify the response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, set 00b (NAK) and then 01b (BUF)

Table 28.9 Operation of the USBFS based on the PID[1:0] setting in host controller mode

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
00b (NAK)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens
01b (BUF)	Bulk or interrupt	Does not depend on the setting	Issues tokens when the DVSTCTR0.UACT bit is 1 and the FIFO buffer associated with the selected pipe is ready for transmission and reception. Does not issue tokens when the DVSTCTR0.UACT bit is 0 or the FIFO buffer associated with the selected pipe is not ready for transmission or reception.
	Isochronous	Does not depend on the setting	Issues tokens regardless of the status of the FIFO buffer associated with the selected pipe.
10b (STALL) or 11b (STALL)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens.

Table 28.10 Operation of the USBFS based on the PID[1:0] setting in device controller mode (1 of 2)

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
00b (NAK)	Bulk or interrupt	Does not depend on the setting	Returns NAK in response to the token from the USB host
	Isochronous	Does not depend on the setting	Returns nothing in response to the token from the USB host

PID[1:0] bits (Response PID)

PID[1:0]位指定所选管道上下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联的管道进行USB传输。表28.9和表28.10显示了基于PID[1:0]位设置的USBFS的基本操作（当通信数据包中没有错误时）。

在选定管道上进行USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以查看管道上的USB传输是否真正进入了NAK状态。如果USBFS将PID[1:0]位更改为NAK，则无需通过软件检查PBUSY位。

USBFS在以下情况下更改PIPEnCTR.PID[1:0]设置：

- 当所选管道处于接收方向并且所选管道的PIPECFG.SHTNAK位由软件设置为1时，USBFS在识别到传输完成时将PID设置为NAK
- USBFS在接收到负载超过所选管道的最大数据包大小的数据包时将PID设置为STALL(11b)
- USBFS在设备控制器模式下检测到USB总线复位时将PID设置为NAK
- USBFS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK
- USBFS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)

要指定响应类型，请按如下方式设置PID[1:0]位：

- 要从NAK(00b)转换到STALL，设置10b
- 要从BUF(01b)转换到STALL，设置11b
- 要从STALL(11b)转换为NAK，请设置10b，然后设置00b
- 要从STALL转换到BUF，请设置00b(NAK)，然后设置01b(BUF)

Table 28.9 USBFS在主机控制器模式下基于PID[1:0]设置的操作

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
00b (NAK)	不依赖于设置	不依赖于设置	不发行代币
01b (BUF)	批量或中断	不依赖于设置	当DVSTCTR0.UACT位为1并且与所选管道关联的FIFO缓冲区已准备好进行发送和接收时，发出令牌。当DVSTCTR0.UACT位为0或 与所选管道关联的FIFO缓冲区尚未准备好进行发送或接收。
	Isochronous	不依赖于设置	无论与所选管道关联的FIFO缓冲区的状态如何，都会发出令牌。
10b (STALL) or 11b (STALL)	不依赖于设置	不依赖于设置	不发行代币。

Table 28.10 基于设备控制器模式下的PID[1:0]设置的USBFS操作（1of2）

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
00b (NAK)	批量或中断	不依赖于设置	返回NAK以响应来自USB主机的令牌
	Isochronous	不依赖于设置	响应来自USB主机的令牌，不返回任何内容

Table 28.10 Operation of the USBFS based on the PID[1:0] setting in device controller mode (2 of 2)

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
01b (BUF)	Bulk	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Interrupt	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Bulk or interrupt	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the FIFO buffer associated with the selected pipe is ready for transmission. Otherwise, returns NAK.
	Isochronous	Receiving direction (DIR = 0)	Receives data in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, discards the data.
	Isochronous	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the associated FIFO buffer is ready for transmission. Otherwise, transmits a zero-length packet.
10b (STALL) or 11b (STALL)	Bulk or interrupt	Does not depend on the setting	Returns STALL in response to the token from the USB host
	Isochronous	Does not depend on the setting	Returns nothing in response to the token from the USB host

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is being used for the current transaction.

The USBFS changes the PBUSY bit from 0 to 1 on start of the USB transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible. For details, see section 28.3.4.1. Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

When the selected pipe is not the isochronous transfer type, the USBFS toggles the SQMON flag on successful completion of the transaction. However, the USBFS does not toggle the SQMON flag when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through the software causes the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction on the selected pipe. The USBFS clears the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through the software causes the USBFS to clear the expected value of the sequence toggle bit for the next transaction on the selected pipe to DATA0. The USBFS clears the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 28.11 shows the data cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which this processing is required.

Table 28.11 Data cleared by the USBFS when ACLRM = 1 (1 of 2)

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe (two FIFO buffers in double buffer mode)	When initializing the selected pipe

Table 28.10 基于设备控制器模式下的PID[1:0]设置的USBFS操作（2之2）

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
01b (BUF)	Bulk	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK以响应来自USB主机的OUT令牌
	Interrupt	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK以响应来自USB主机的OUT令牌
	批量或中断	发射方向(DIR=1)	传输数据以响应来自USB主机的令牌，如果与所选管道关联的FIFO缓冲区已准备好进行传输。否则，返回NAK。
	Isochronous	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据以响应来自USB主机的OUT令牌。否则，丢弃数据。
	Isochronous	发射方向(DIR=1)	如果关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，发送零长度数据包。
10b (STALL) or 11b (STALL)	批量或中断	不依赖于设置	返回STALL以响应来自USB主机的令牌
	Isochronous	不依赖于设置	响应来自USB主机的令牌，不返回任何内容

PBUSY bit (Pipe Busy)

PBUSY位指示所选管道是否正在用于当前事务。

USBFS在所选管道的USB事务开始时将PBUSY位从0更改为1，并更改PBUSY位在一个事务完成时从1变为0。

在PID设置为NAK后，通过软件读取PBUSY位可以检查是否可以更改管道设置。详见28.3.4.1节。管道控制寄存器切换程序。

SQMON位（序列切换位确认）

SQMON位指示所选管道的下一个事务的序列切换位的预期值。

当所选管道不是同步传输类型时，USBFS在事务成功完成时切换SQMON标志。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBFS不会切换SQMON标志。

SQSET位（序列切换位设置）

通过软件将SQSET位设置为1会导致USBFS将DATA1设置为所选管道上下一个事务的序列切换位的预期值。USBFS将SQSET位清0。

SQCLR位（序列翻转位清除）

通过软件将SQCLR位设置为1会导致USBFS将所选管道上下一个事务的序列切换位的预期值清除为DATA0。USBFS将SQCLR位清0。

ACLRM位（自动缓冲区清除模式）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。要完全清除分配给所选管道的FIFO缓冲区中的数据，请向ACLRM位连续写入1和0。

表28.11显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 28.11 当ACLRM=1(1of2)时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	FIFO缓冲区中的所有数据分配给选定的管道（两个双缓冲模式下的FIFO缓冲）	初始化选定管道时

Table 28.11 Data cleared by the USBFS when ACLRM = 1 (2 of 2)

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value
3	Internal flags related to the PIPECFG.BFRE bit	When changing the PIPECFG.BFRE setting
4	FIFO buffer toggle control	When changing the PIPECFG.DBLB setting
5	Internal flags related to the transaction count	When forcing the transaction count function to terminate

ATREPM bit (Auto Response Mode)

The ATREPM bit enables or disables auto response mode for the selected pipe.

This bit can be set to 1 in device controller mode when the selected pipe is the bulk transfer type. When the bit is set to 1, the USBFS responds to the token from the USB host as follows:

- When the selected pipe is set for bulk IN transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 1):
  a. When the ATREPM bit = 1 and PID = BUF, the USBFS transmits a zero-length packet in response to the IN token.
  b. The USBFS updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USBFS receives ACK from the USB host. In a single transaction, the IN token is received, a zero-length packet is transmitted, and then ACK is received. The USBFS does not generate the BRDY or BEMP interrupt.
- When the selected pipe is set for bulk OUT transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 0):
  When the ATREPM bit = 1 and PID = BUF, the USBFS returns NAK in response to the OUT token and generates an NRDY interrupt.

For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode. When the selected pipe uses isochronous transfer, always set this bit to 0.

In host controller mode, always set the ATREPM bit to 0.

INBUFM bit (Transmit Buffer Monitor)

The INBUFM bit indicates the FIFO buffer status for the selected pipe in the transmitting direction.

When the selected pipe is set in the transmitting direction (PIPECFG.DIR = 1), the USBFS sets this bit to 1 when the CPU or DMA/DTC completes writing data to at least one FIFO buffer plane.

The USBFS sets this bit to 0 when the USBFS completes transmission of the data from the FIFO buffer plane to which all the data is written. In double buffer mode (PIPECFG.DBLB = 1), the USBFS sets the INBUFM bit to 0 when the USBFS completes transmission of the data from the two FIFO buffer planes before the CPU or DMA/DTC completes writing data to one FIFO buffer plane.

The INBUFM bit indicates the same value as the BSTS bit when the selected pipe is in the receiving direction (PIPECFG.DIR = 0).

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 28.12.

Table 28.11 当ACLRM=1(2of2)时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时
3	与PIPECFG.BFRE位相关的内部标志	更改PIPECFG.BFRE设置时
4	FIFO缓冲区切换控制	更改PIPECFG.DBLB设置时
5	与事务计数相关的内部标志	强制事务计数函数终止时

ATREPM位（自动响应模式）

ATREPM位启用或禁用所选管道的自动响应模式。

当所选管道为批量传输类型时，该位可以在设备控制器模式下设置为1。当该位设置为1时，USBFS响应来自USB主机的令牌，如下所示：

●Whentheselectedpipeissetforbulk INtransfers(PIPECFG.TYPE[1:0]=01bandPIPECFG.DIR=1):

a. 当ATREPM位=1且PID=BUF时，USBFS发送一个长度为零的数据包以响应IN令牌。

湾。每次USBFS从USB主机接收到ACK时，USBFS都会更新（允许切换）序列切换位(DATA-PID)。在单个事务中，收到IN令牌，发送零长度数据包，然后收到ACK。USBFS不会产生BRDY或BEMP中断。

●当所选管道设置为批量OUT传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=0）：

当ATREPM位=1且PID=BUF时，USBFS返回NAK以响应OUT令牌并生成一个
NRDY interrupt.

对于自动响应模式下的USB通信，当FIFO缓冲区为空时，将ATREPM位设置为1。在自动响应模式下的USB通信期间不要写入FIFO缓冲区。当所选管道使用同步传输时，始终将此位设置为0。

在主机控制器模式下，始终将ATREPM位设置为0。

INBUFM位（发送缓冲区监视器）

INBUFM位指示发送方向上所选管道的FIFO缓冲区状态。

当所选管道设置为发送方向(PIPECFG.DIR=1)时，当CPU或DMADTC完成将数据写入至少一个FIFO缓冲区平面时，USBFS将该位设置为1。

当USBFS完成从写入所有数据的FIFO缓冲区平面传输数据时，USBFS将该位设置为0。在双缓冲模式(PIPECFG.DBLB=1)下，当USBFS在CPU或DMADTC完成将数据写入一个FIFO缓冲层之前完成从两个FIFO缓冲层的数据传输时，USBFS将INBUFM位设置为0。

当所选管道处于接收方向时（PIPECFG.DIR=0），INBUFM位指示与BSTS位相同的值。

BSTS bit (Buffer Status)

BSTS位指示所选管道的FIFO缓冲区状态。

BSTS位的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表28.12所示。

Table 28.12 BSTS bit operation

DIR value	BFRE value	DCLRM value	BSTS bit function
0	0	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
		1	Setting prohibited
	1	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 when the software sets the BCLR bit in the port control register to 1 after the data read is complete
		1	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
1	0	0	Sets to 1 when transmit data can be written to the FIFO buffer, and clears to 0 on completion of data write
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

28.2.36 PIPEnCTR : PIPEn Control Registers (n = 6 to 9)

Base address: USBFS = 0x4009_0000

Offset address: 0x07A + 0x2 × (n - 6)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	Response PID 0 0: NAK response 0 1: BUF response (depends buffer state) 1 0: STALL response 1 1: STALL response	R/W
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	PBUSY	Pipe Busy 0: Pipe n not in use for the transaction 1: Pipe n in use for the transaction	R
6	SQMON	Sequence Toggle Bit Confirmation 0: DATA0 1: DATA1	R
7	SQSET	Sequence Toggle Bit Set*1 Sets the sequence toggle bit for pipe n. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA0	W
8	SQCLR	Sequence Toggle Bit Clear*1 Clears the sequence toggle bit for pipe n. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0	W
9	ACLRM	Auto Buffer Clear Mode*2 0: Disable 1: Enable (all buffers initialized)	R/W
14:10	—	These bits are read as 0. The write value should be 0.	R/W
15	BSTS	Buffer Status 0: Buffer access disabled 1: Buffer access enabled	R

Table 28.12 BSTS位操作

方向值	BFRE value	DCLRM value	BSTS位功能
0	0	0	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
		1	禁止设定
	1	0	接收数据可以从FIFO缓冲区读取时设置为1，当数据读取完成后软件将端口控制寄存器中的BCLR位设置为1时清除为0
		1	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
1	0	0	当发送数据可以写入FIFO缓冲区时设置为1，并在数据写入完成时清除为0
		1	禁止设定
	1	0	禁止设定
		1	禁止设定

28.2.36 PIPEnCTR:PIPEn控制寄存器(n=6到9)

Base address: USBFS = 0x4009_0000

Offset address: 0x07A + 0x2 × (n - 6)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	响应PID 00：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应	R/W
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	PBUSY	管道忙 0：管道n未用于事务1：管道n正在用于事务	R
6	SQMON	序列切换位确认 0: DATA0 1: DATA1	R
7	SQSET	序列切换位设置*1 设置管道n的序列切换位。 0：无效（写0无效）1：将下一笔交易的期望值设置为DATA0	W
8	SQCLR	序列切换位清除*1 清除管道n的序列切换位。 0：无效（写0无效）1：清除下一笔交易的期望值到DATA0	W
9	ACLRM	自动缓冲区清除模式*2 0：禁用1：启用（所有缓冲区已初始化）	R/W
14:10	—	这些位被读取为0。写入值应为0。	R/W
15	BSTS	缓冲区状态 0：禁止缓冲区访问1：允许缓冲区访问	R

Note 1. Only write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00b (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 2. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00b (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PID[1:0] bits (Response PID)

The PID[1:0]bits specify the response type for the next transaction of the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USB transfer. Table 28.9 and Table 28.10 show the basic operation (when there are no errors in the transmitted and received packets) of the USBFS depending on the PID[1:0] setting.

After changing the PID[1:0] setting from BUF to NAK through the software during USB communication on the selected pipe, check that the PBUSY bit is 1 to see if USB transfer on the selected pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through the software is not necessary.

The USBFS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBFS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBFS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode

To specify each response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, set 00b (NAK) and then 01b (BUF)

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is being used for the current transaction.

The USBFS changes the PBUSY bit from 0 to 1 on start of the USB transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

The USBFS toggles the SQMON bit on successful completion of the transaction. However, the USBFS does not toggle the SQMON bit when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through the software causes the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction on the selected pipe. The USBFS sets the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through the software causes the USBFS to clear the expected value of the sequence toggle bit for the next transaction on the selected pipe to DATA0. The USBFS sets the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

注1.PID为NAK时，仅向SQCLR或SQSET位写入1。在设置这些位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00b(NAK)，则无需通过软件检查PBUSY位。

注2.仅在PID为NAK时和在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。在设置该位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00b(NAK)，则无需通过软件检查PBUSY位。

PID[1:0] bits (Response PID)

PID[1:0]位指定所选管道的下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联的管道进行USB传输。表28.9和表28.10显示了取决于PID[1:0]设置的USBFS的基本操作（在发送和接收的数据包中没有错误时）。

在选定管道上进行USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以查看选定管道上的USB传输是否真正进入了NAK状态。如果USBFS将PID[1:0]位更改为NAK，则无需通过软件检查PBUSY位。

USBFS在以下情况下更改PIPEnCTR.PID[1:0]设置：

●USBFS在接收到负载超过所选管道的最大数据包大小的数据包时将PID设置为STALL(11b)

●USBFS在设备控制器模式下检测到USB总线复位时将PID设置为NAK

●USBFS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK

●USBFS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)

要指定每种响应类型，请按如下方式设置PID[1:0]位：

●要从NAK(00b)转换到STALL，设置10b

●要从BUF(01b)转换到STALL，设置11b

●要从STALL(11b)转换为NAK，请设置10b，然后设置00b

●要从STALL转换到BUF，请设置00b(NAK)，然后设置01b(BUF)

PBUSY bit (Pipe Busy)

PBUSY位指示所选管道是否正在用于当前事务。

USBFS在所选管道的USB事务开始时将PBUSY位从0更改为1，并更改PBUSY位在一个事务完成时从1变为0。

在PID设置为NAK后，通过软件读取PBUSY位可以检查是否可以更改管道设置。

SQMON位（序列切换位确认）

SQMON位指示所选管道的下一个事务的序列切换位的预期值。

USBFS在事务成功完成时切换SQMON位。但是，USBFS不会切换SQMON位，当在接收方向的传输过程中发生DATA-PID不匹配时。

SQSET位（序列切换位设置）

通过软件将SQSET位设置为1会导致USBFS将DATA1设置为所选管道上下一个事务的序列切换位的预期值。USBFS将SQSET位设置为0。

SQCLR位（序列翻转位清除）

通过软件将SQCLR位设置为1会导致USBFS将所选管道上下一个事务的序列切换位的预期值清除为DATA0。USBFS将SQCLR位设置为0。

ACLRM位（自动缓冲区清除模式）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。要完全清除分配给所选管道的FIFO缓冲区中的数据，请向ACLRM位连续写入1和0。

Table 28.13 shows the data cleared by writing 1 and 0 continuously to the ACLRM bit and the cases in which this processing is required.

Table 28.13 Data cleared by the USBFS when ACLRM = 1

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe	When initializing the selected pipe
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value
3	Internal flags related to the PIPECFG.BFRE bit	When changing the PIPECFG.BFRE setting
4	Internal flags related to the transaction count	When forcing the transaction count function to terminate

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 28.12.

28.2.37 PIPEnTRE : PIPEn Transaction Counter Enable Register (n = 1 to 5)

Base address: USBFS = 0x4009_0000

Offset address: 0x090 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	TRCLR	Transaction Counter Clear 0: Invalid (writing 0 has no effect) 1: Clear counter value	R/W
9	TRENB	Transaction Counter Enable 0: Disable transaction counter 1: Enable transaction counter	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note: Set each bit in PIPEnTRE while PID is NAK. Before setting these bits after changing the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

TRCLR bit (Transaction Counter Clear)

When the TRCLR bit sets to 1, the USBFS clears the value of the transaction counter associated with the selected pipe and then sets the TRCLR bit to 0.

TRENB bit (Transaction Counter Enable)

The TRENB bit enables or disables the transaction counter.

For receiving pipes, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through the software allows the USBFS to control hardware on having received the number of packets equal to the TRNCNT[15:0] setting, as follows:

- When the PIPECFG.SHTNAK bit is 1, the USBFS changes the PID bits to NAK for the associated pipe on having received the number of packets equal to the TRNCNT[15:0] setting
- When the PIPECFG.BFRE bit is 1, the USBFS asserts the BRDY interrupt on having received the number of packets equal to the TRNCNT[15:0] setting and then reading the last received data

表28.13显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 28.13 ACLRM=1时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	分配给所选管道的FIFO缓冲区中的所有数据	初始化选定管道时
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时
3	与PIPECFG.BFRE位相关的内部标志	更改PIPECFG.BFRE设置时
4	与事务计数相关的内部标志	强制事务计数函数终止时

BSTS bit (Buffer Status)

BSTS位指示所选管道的FIFO缓冲区状态。

BSTS位的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表28.12所示。

28.2.37 PIPEnTRE:PIPEn事务计数器使能寄存器(n=1到5)

Base address: USBFS = 0x4009_0000

Offset address: 0x090 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
8	TRCLR	交易计数器清除 0：无效（写0无效）1：清除计数器值	R/W
9	TRENB	事务计数器启用 0：禁用事务计数器1：启用事务计数器	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

Note: 当PID为NAK时，设置PIPEnTRE中的每个位。在将所选管道的PIPEnCTR.PID[1:0]位从BUF更改为NAK之后设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0。但是，如果PID[1:0]位更改为NAK通过USBFS，无需通过软件检查PBUSY位。

TRCLR位（事务计数器清零）

当TRCLR位设置为1时，USBFS清除与所选管道关联的事务计数器的值，然后将TRCLR位设置为0。

TRENB位（事务计数器使能）

TRENB位启用或禁用事务计数器。

对于接收管道，在设置接收管道的总包数后，将TRENB位设置为1 PIPEnTRN.TRNCNT[15:0]位通过软件允许USBFS在接收到等于TRNCNT[15:0]设置的数据包数量时控制硬件，如下所示：

●当PIPECFG.SHTNAK位为1时，USBFS在接收到等于TRNCNT[15:0]设置的数据包数时将关联管道的PID位更改为NAK

●当PIPECFG.BFRE位为1时，USBFS在接收到等于TRNCNT[15:0]设置的数据包数量并读取最后接收到的数据时断言BRDY中断

For transmitting pipes, set the TRENB bit to 0.

When the transaction counter is not used, set this bit to 0. When the transaction counter is used, set the TRNCNT[15:0] bits before setting this bit to 1. Set this bit to 1 before receiving the first packet to be counted by the transaction counter.

28.2.38 PIPEnTRN : PIPEn Transaction Counter Register (n = 1 to 5)

Base address: USBFS = 0x4009_0000

Offset address: 0x092 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TRNCNT[15:0]	Transaction Counter When written to, this bit specifies the total packets (number of transactions) to be received by the selected pipe. When read from, when PIPEnTRE.TRENB is 0, this bit indicates the specified number of transactions. When PIPEnTRE.TRENB is 1, this bit indicates the current transaction count.	R/W

The PIPEnTRN registers retain their settings during a USB bus reset.

TRNCNT[15:0] bits (Transaction Counter)

The USBFS increments the value of the TRNCNT[15:0] bits by 1 when all of the following conditions are satisfied on receiving the packet:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[9:0] setting

The USBFS clears the value of the TRNCNT[15:0] bits to 0 when any of the following conditions are satisfied:

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[9:0] setting

Both of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The USBFS received a short packet

Both of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The PIPEnTRE.TRCLR bit was set to 1 by software

For transmitting pipes, set the TRNCNT[15:0] bits to 0. When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.

Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is only enabled when the PIPEnTRE.TRENB bit is 0. To set the number of transactions to be transferred, set the TRCLR bit to 1 to clear the current counter value before setting the PIPEnTRE.TRENB bit to 1.

对于传输管道，将TRENB位设置为0。

当不使用事务计数器时，将该位设置为0。当使用事务计数器时，将该位设置为1之前设置TRNCNT[15:0]位。在接收第一个要计数的数据包之前将该位设置为1由交易柜台。

28.2.38 PIPEnTRN:PIPEn事务计数器寄存器(n=1到5)

Base address: USBFS = 0x4009_0000

Offset address: 0x092 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TRNCNT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TRNCNT[15:0]	事务计数器写入时，该位指定所选管道要接收的总数据包（事务数）。读取时，当PIPEnTRE.TRENB为0时，该位指示指定的事务数。当PIPEnTRE.TRENB为1时，该位指示当前事务计数。	R/W

PIPEnTRN寄存器在USB总线复位期间保留其设置。

TRNCNT[15:0] bits (Transaction Counter)

当接收到数据包时满足以下所有条件时，USBFS将TRNCNT[15:0]位的值加1：

●PIPEnTRE.TRENB位=1

●(TRNCNT[15:0]设定值≠当前计数器值+1)收到数据包

●接收数据包的有效载荷与PIPEMAXP.MXPS[9:0]设置一致

当满足以下任一条件时，USBFS将TRNCNT[15:0]位的值清零：

满足以下所有条件：

●PIPEnTRE.TRENB位=1

●(TRNCNT[15:0]setvalue=currentcountervalue+1)收到数据包

●接收数据包的有效载荷与PIPEMAXP.MXPS[9:0]设置一致

满足以下两个条件：

●PIPEnTRE.TRENB位=1

●USBFS收到一个短数据包

满足以下两个条件：

●PIPEnTRE.TRENB位=1

●PIPEnTRE.TRCLR位由软件设置为1

对于传输管道，将TRNCNT[15:0]位设置为0。当不使用事务计数器时，将TRNCNT[15:0]位设置为0。

仅当PIPEnTRE.TRENB位为0时才使能将要传输的事务数设置到TRNCNT[15:0]位。要设置要传输的事务数，请将TRCLR位设置为1以清除当前计数器将PIPEnTRE.TRENB位设置为1之前的值。

28.2.39 BCCTRL1 : Battery Charging Control Register 1

Base address: USBFS = 0x4009_0000

Offset address: 0x0B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CHGDETSTS	PDDETSTS	—	—	CHGDETE	PDDETE	VDPSRCE	VDMSRCE	IDPSRCE	RPDME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPDME	D- Line Pull-down Control 0: Disable D- Line Pull-down 1: Enable D- Line Pull-down	R/W
1	IDPSRCE	D+ Line IDPSRC Output Control 0: Stopped 1: 10 µA output	R/W
2	VDMSRCE	D- Line VDMSRC (0.6 V) Output Control 0: Stopped 1: 0.6 V output	R/W
3	VDPSRCE	D+ Line VDPSRC (0.6 V) Output Control 0: Stopped 1: 0.6 V output	R/W
4	PDDETE	D+ Line 0.6 V Input Detection Control 0: Disable detection 1: Enable detection	R/W
5	CHGDETE	D- Line 0.6 V Input Detection Control 0: Disable detection 1: Enable detection	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	PDDETSTS	D+ Line 0.6 V Input Detection Status Flag This Flag is valid when PDDETE = 1. 0: Not detected 1: Detected	R
9	CHGDETSTS	D- Line 0.6 V Input Detection Status Flag This flag is valid when CHGDETE = 1. 0: Not detected 1: Detected	R
31:10	—	These bits are read as 0. The write value should be 0.	R/W

RPDME bit (D- Line Pull-down Control)

In device controller operation, set this bit to 1 to perform Data Contact Detect. In the Battery Charging Specification Revision 1.2, there are two methods to handle Data Contact Detect; the method realized by software wait and the method to contact the data line by hardware. The RPDME bit adopts the latter method. When RPDME = 1, the USBFS controls D- line pull-down.

IDPSRCE bit (D+ Line IDPSRC Output Control)

In device controller operation, set this bit to 1 to perform Data Contact Detect. In the Battery Charging Specification Revision 1.2, there are two methods to handle Data Contact Detect; the method realized by software wait and the method to contact the data line by hardware. The IDPSRCE bit adopts the latter method. When IDPSRCE = 1, the USBFS enables the IDP_SRC circuit

28.2.39 BCCTRL1：电池充电控制寄存器1

Base address: USBFS = 0x4009_0000

Offset address: 0x0B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CHGDETSTS	PDDETSTS	—	—	CHGDETE	PDDETE	VDPSRCE	VDMSRCE	IDPSRCE	RPDME
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPDME	D- Line Pull-down Control 0：禁用DLine下拉1：启用DLine下拉	R/W
1	IDPSRCE	D+线IDPSRC输出控制 0：停止1：10µA输出	R/W
2	VDMSRCE	DLineVDMSRC(0.6V)输出控制 0：停止1：0.6V输出	R/W
3	VDPSRCE	D+线VDPSRC(0.6V)输出控制 0：停止1：0.6V输出	R/W
4	PDDETE	D+线0.6V输入检测控制 0：禁用检测1：启用检测	R/W
5	CHGDETE	DLine0.6V输入检测控制 0：禁用检测1：启用检测	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
8	PDDETSTS	D+线0.6V输入检测状态标志 该标志在PDDETE=1时有效。 0：未检测到1：检测到	R
9	CHGDETSTS	DLine0.6V输入检测状态标志 该标志在CHGDETE=1时有效。 0：未检测到1：检测到	R
31:10	—	这些位被读取为0。写入值应为0。	R/W

RPDME bit (D- Line Pull-down Control)

在设备控制器操作中，将此位设置为1以执行数据接触检测。在电池充电规范中修订版1.2，有两种方法来处理DataContactDetect；软件等待实现的方法和硬件连接数据线的方法。RPDME比特采用后一种方法。当RPDME=1时，USBFS控制Dline下拉。

IDPSRCE位（D+线IDPSRC输出控制）

在设备控制器操作中，将此位设置为1以执行数据接触检测。在电池充电规范中修订版1.2，有两种方法来处理DataContactDetect；软件等待实现的方法和硬件连接数据线的方法。IDPSRCE位采用后一种方法。当IDPSRCE=1时，USBFS使能IDP_SRC电路

VDMSRCE bit (D- Line VDMSRC (0.6 V) Output Control)

In host controller operation, during Primary Detection, this bit controls VDMSRC (0.6 V) output from the USB_DM pin.

In device controller operation, during Secondary Detection, this bit controls VDMSRC (0.6 V) output from the USB_DM pin.

VDPSRCE bit (D+ Line VDPSRC (0.6 V) Output Control)

In device controller operation, if Primary Detection is executed, this bit controls VDPSRC (0.6 V) output from the USB_DP pin.

PDDETE bit (D+ Line 0.6 V Input Detection Control)

When the PDDETE bit is set to 1, the following states can be detected.

In host controller operation, during Primary Detection, VDPSRC (0.6 V) is input to the USB_DP pin from a peripheral device.

In device controller operation, during Secondary Detection, VDPSRC (0.6 V) output from the USBFS to the USB_DM pin is input to the USB_DP pin via the host.

CHGDETE bit (D- Line 0.6 V Input Detection Control)

In device controller operation, the following can be detected when the CHGDETE bit is set to 1.

During Primary Detection, VDMSRC (0.6 V) is input to the USB_DM pin from the host.

During Primary Detection, VDPSRC (0.6 V) output from the USBFS to the USB_DP pin is input to the USB_DM pin via the USB host.

PDDETSTS flag (D+ Line 0.6 V Input Detection Status Flag)

The PDDETSTS flag is enabled when the PDDETE bit is 1. The PDDETSTS flag becomes 1 under the following conditions.

In host controller operation, during Primary Detection, VDPSRC (0.6V) is input to the USB_DP pin from a peripheral device.

In device controller operation, during Secondary Detection, the VDMSRC (0.6V) output from the USBFS to the USB_DM pin is input to the USB_DP pin via the host.

CHGDETSTS flag (D- Line 0.6 V Input Detection Status Flag)

In device controller operation, this flag is enabled when the CHGDETE bit is 1. The CHGDETSTS flag becomes 1 under the following conditions.

During Primary Detection, VDMSRC (0.6V) is input to the USB_DM pin from the USB host.

During Primary Detection, the VDPSRC (0.6V) output from the USBFS to the USB_DP pin is input to the USB_DM pin via the USB host.

28.2.40 BCCTRL2 : Battery Charging Control Register 2

Base address: USBFS = 0x4009_0000

Offset address: 0x0B4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PHYDET[1:0]		—	—	—	—	BATCHGE	DCPMODE	—	—	—	—	—	—
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

VDMSRCE位（DLineVDMSRC(0.6V)输出控制）

在主机控制器操作中，在主检测期间，该位控制USB_DM引脚的VDMSRC(0.6V)输出。

在设备控制器操作中，在辅助检测期间，该位控制USB_DM引脚的VDMSRC(0.6V)输出。

VDPSRCE位（D+线VDPSRC(0.6V)输出控制）

在设备控制器操作中，如果执行PrimaryDetection，该位控制USB_DP引脚的VDPSRC(0.6V)输出。

PDDETE位（D+线0.6V输入检测控制）

当PDDETE位设置为1时，可以检测到以下状态。

在主机控制器操作中，在初级检测期间，VDPSRC(0.6V)从外围设备输入到USB_DP引脚。

在设备控制器操作中，在二次检测期间，从USBFS到USB_DM引脚的VDPSRC(0.6V)输出通过主机输入到USB_DP引脚。

CHGDETE位（DLine0.6V输入检测控制）

在设备控制器操作中，当CHGDETE位设置为1时，可以检测到以下情况。

在主要检测期间，VDMSRC(0.6V)从主机输入到USB_DM引脚。

在初级检测期间，从USBFS到USB_DP引脚的VDPSRC(0.6V)输出通过USB主机输入到USB_DM引脚。

PDDETSTS标志（D+线0.6V输入检测状态标志）

当PDDETE位为1时，使能PDDETSTS标志。在以下条件下，PDDETSTS标志变为1。

在主机控制器操作中，在初级检测期间，VDPSRC(0.6V)从外围设备输入到USB_DP引脚。

在设备控制器操作中，在二次检测期间，从USBFS到USB_DM引脚的VDMSRC(0.6V)输出通过主机输入到USB_DP引脚。

CHGDETSTS标志（DLine0.6V输入检测状态标志）

在设备控制器操作中，当CHGDETE位为1时启用该标志。在以下条件下，CHGDETSTS标志变为1。

在初级检测期间，VDMSRC(0.6V)从USB主机输入到USB_DM引脚。

在初级检测期间，从USBFS到USB_DP引脚的VDPSRC(0.6V)输出通过USB主机输入到USB_DM引脚。

28.2.40 BCCTRL2：电池充电控制寄存器2

Base address: USBFS = 0x4009_0000

Offset address: 0x0B4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PHYDET[1:0]		—	—	—	—	BATCHGE	DCPMODE	—	—	—	—	—	—
重置后的值：	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	DCPMODE	Dedicated Charging Port (DCP) Mode Control In host controller mode, setting this bit to 1 connects the D+ line and D- line. If USBFS is configured as DCP, this bit should be set to 1 before driving VBUS. In device controller mode, this bit should be set to 0. 0: Disable DCP 1: Enable DCP	R/W
7	BATCHGE	Battery Charging Enable 0: Disable Battery Charging 1: Enable Battery Charging	R/W
11:8	—	These bits are read as 0. The write value should be 0.	R/W
13:12	PHYDET[1:0]	Detect Sensitivity Adjustment Adjusts the detect sensitivity of Portable Device and Charging D- Port Initial value is 10b, but need to be set 01b.	R/W
31:14	—	These bits are read as 0. The write value should be 0.	R/W

28.2.41 DEVADDn : Device Address n Configuration Register (n = 0 to 5)

Base address: USBFS = 0x4009_0000

Offset address: 0x0D0 + 0x2 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
7:6	USBSPD[1:0]	Transfer Speed of Communication Target Device 0 0: Do not use DEVADDn 0 1: Low-speed 1 0: Full-speed 1 1: Setting prohibited	R/W
15:8	—	These bits are read as 0. The write value should be 0.	R/W

The DEVADDn register specifies the transfer speed of the peripheral device that is the communication target for pipes 0 to 9.

In host controller mode, set all DEVADDn bits before starting communication to any pipes. Only change the bits in DEVADDn when no valid pipes are using the bit settings. A valid pipe is defined as one that satisfies both of the following conditions:

- DEVADDn is selected in the DEVSEL[3:0] bits
- The PID[1:0] bits are set to BUF for the selected pipe, or the selected pipe is the DCP with the DCPCTR.SUREQ bit set to 1

In device controller mode, set all bits in this register to 0.

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

TheUSBSPD[1:0] bits specify the USB transfer speed of the target peripheral device. Set these bits to 10b when a full-speed device is connected through the hub. In host controller mode, the USBFS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	DCPMODE	专用充电端口(DCP)模式控制 在主机控制器模式下，将此位设置为1连接D+线和Dline。如果USBFS配置为DCP，则该位应在驱动VBUS之前设置为1。在设备控制器模式下，该位应设置为0。 0：禁用DCP1： 启用DCP	R/W
7	BATCHGE	电池充电启用 0：禁用电池充电1：启用电 池充电	R/W
11:8	—	这些位被读取为0。写入值应为0。	R/W
13:12	PHYDET[1:0]	检测灵敏度调整 调整便携式设备和充电DPort的检测灵敏度 初始值为10b，但需要设置为01b。	R/W
31:14	—	这些位被读取为0。写入值应为0。	R/W

28.2.41 DEVADDn：器件地址n配置寄存器（n=0到5）

Base address: USBFS = 0x4009_0000

Offset address: 0x0D0 + 0x2 × n

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
7:6	USBSPD[1:0]	通信目标设备的传输速度 00：不使用DEVADDn01： 低速10：全速11：禁止设 置	R/W
15:8	—	这些位被读取为0。写入值应为0。	R/W

DEVADDn寄存器指定作为管道0到9的通信目标的外围设备的传输速度。

在主机控制器模式下，在开始与任何管道通信之前设置所有DEVADDn位。仅更改中的位DEVADDn当没有有效管道使用位设置时。有效管道被定义为同时满足以下两个条件的管道：

●DEVADDn在DEVSEL[3:0]位中选择

●所选管道的PID[1:0]位设置为BUF，或者所选管道是DCPCTR.SUREQ位设置为1的DCP

在设备控制器模式下，将此寄存器中的所有位设置为0。

USBSPD[1:0]位（通信目标设备的传输速度）

USBSPD[1:0]位指定目标外围设备的USB传输速度。当通过集线器连接全速设备时，将这些位设置为10b。在主机控制器模式下，USBFS根据USBSPD[1:0]设置生成数据包。在设备控制器模式下，将这些位设置为00b。

28.2.42 PHYSECTRL : PHY Single-ended Receiver Control Register

Base address: USBFS = 0x4009_0000

Offset address: 0x0F4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	CNEN	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	CNEN	Single-ended Receiver Enable 0: Single-ended receiver operation is disabled 1: Single-ended receiver operation is enabled	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

CNEN bit (Single-ended Receiver Enable)

Setting the CNEN bit to 1 enables single-ended receiver operation. Set this bit to 1 when perform the hardware-based Data Contact Detection using the battery charging function in device controller mode.

28.2.43 DPUSR0R : Deep Software Standby USB Transceiver Control/Pin Monitor Register

Base address: USBFS = 0x4009_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBSTS0	—	DOVCB0	DOVCA0	—	—	DM0	DP0
Value after reset:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	x	x

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	FIXPHY0	DRPD0	—	RPUE0	SRPC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRPC0*1	USB Single-ended Receiver Control 0: Disable input through DP and DM inputs 1: Enable input through DP and DM inputs	R/W
1	RPUE0*1	DP Pull-Up Resistor Control 0: Disable DP pull-up resistor 1: Enable DP pull-up resistor	R/W
2	—	These bits are read as 0. The write value should be 0.	R/W
3	DRPD0*1	D+/D- Pull-Down Resistor Control 0: Disable DP/DM pull-down resistor 1: Enable DP/DM pull-down resistor	R/W
4	FIXPHY0	USB Transceiver Output Fix 0: Fix outputs in Normal mode and on return from Deep Software Standby mode 1: Fix outputs on transition to Deep Software Standby mode	R/W
15:5	—	These bits are read as 0. The write value should be 0.	R/W
16	DP0	USB D+ Input Indicates D+ input signal on the USBFS side	R

28.2.42 PHYSECTRL:PHY单端接收器控制寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x0F4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	CNEN	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	CNEN	单端接收器使能 0：禁止单端接收器操作1：使能单端接收器操作	R/W
31:5	—	这些位被读取为0。写入值应为0。	R/W

CNEN位（单端接收器使能）

将CNEN位设置为1可启用单端接收器操作。执行基于硬件的数据时将此位设置为1
在设备控制器模式下使用电池充电功能进行接触检测。

28.2.43 DPUSR0R:DeepSoftwareStandbyUSBTransceiverControlPinMonitor Register

Base address: USBFS = 0x4009_0000

Offset address: 0x400

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBSTS0	—	DOVCB0	DOVCA0	—	—	DM0	DP0
重置后的值:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	x	x

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	FIXPHY0	DRPD0	—	RPUE0	SRPC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRPC0*1	USB单端接收器控制 0：通过DP和DM输入禁用输入1：通过DP和DM输入启用输入	R/W
1	RPUE0*1	DP上拉电阻控制 0：禁用DP上拉电阻1：启用DP上拉电阻	R/W
2	—	这些位被读取为0。写入值应为0。	R/W
3	DRPD0*1	D+D下拉电阻控制 0：禁用DPDM下拉电阻1：启用DPDM下拉电阻	R/W
4	FIXPHY0	USB收发器输出修复 0：在正常模式和从深度软件待机模式返回时修复输出1：在转换到深度软件待机模式时修复输出	R/W
15:5	—	这些位被读取为0。写入值应为0。	R/W
16	DP0	USBD+输入 指示USBFS侧的D+输入 信号	R

Bit	Symbol	Function	R/W
17	DM0	USB D- Input Indicates D– input signal on the USBFS side	R
19:18	—	These bits are read as 0. The write value should be 0.	R/W
20	DOVCA0	USB OVRCURA Input Indicates OVRCURA input signal on the USBFS side	R
21	DOVCB0	USB OVRCURB Input Indicates OVRCURB input signal on the USBFS side	R
22	—	The read value is undefined. The write value should be 0.	R/W
23	DVBSTS0	USB VBUS Input Indicates VBUS input signal on the USBFS side	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use this bit during operation in Deep Software Standby mode. For details, see section 28.3.1.5. Release from deep software standby mode because of USB suspend/resume interrupts.

SRPC0 bit (USB Single-ended Receiver Control)

The SRPC0 bit controls the D+ and D- inputs of the USB transceiver. In host controller mode, set this bit to 1. In device controller mode, set this bit to 0 when disconnected, set to 1 when suspended. This bit is only valid when the FIXPHY0 bit is 1.

FIXPHY0 bit (USB Transceiver Output Fix)

The FIXPHY0 bit keeps the outputs of the USB transceiver disabled.

28.2.44 DPUSR1R : Deep Software Standby USB Suspend/Resume Interrupt Register

Base address: USBFS = 0x4009_0000

Offset address: 0x404

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBINT0	—	DOVRCRB0	DOVRCRA0	—	—	DMINT0	DPINT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	DVBSE0	—	DOVRCRBE0	DOVRCRAE0	—	—	DMINTE0	DPINTE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DPINTE0	USB DP Interrupt Enable/Clear 0: Disable recovery from Deep Software Standby mode by DP input 1: Enable recovery from Deep Software Standby mode by DP input	R/W
1	DMINTE0	USB DM Interrupt Enable/Clear 0: Disable recovery from Deep Software Standby mode by DM input 1: Enable recovery from Deep Software Standby mode by DM input	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DOVRCRAE0	USB OVRCURA Interrupt Enable/Clear 0: Disable recovery from Deep Software Standby mode by OVRCURA input 1: Enable recovery from Deep Software Standby mode by OVRCURA input	R/W
5	DOVRCRBE0	USB OVRCURB Interrupt Enable/Clear 0: Disable recovery from Deep Software Standby mode by OVRCURB input 1: Enable recovery from Deep Software Standby mode by OVRCURB input	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
17	DM0	USB D- Input 指示USBFS侧的D 输入信号	R
19:18	—	这些位被读取为0。写入值应为0。	R/W
20	DOVCA0	USBOVRCURA输入 指示USBFS侧的OVRCURA输入信号	R
21	DOVCB0	USBOVRCURB输入 指示USBFS侧的OVRCURB输入信号	R
22	—	读取值未定义。写入值应为0。	R/W
23	DVBSTS0	USBVBUS输入 指示USBFS侧的VBUS输入信号	R
31:24	—	这些位被读取为0。写入值应为0。	R/W

注1.在深度软件待机模式下操作期间使用该位。有关详细信息，请参阅第28.3.1.5节。由于USB挂起恢复中断而从深度软件待机模式中释放。

SRPC0位（USB单端接收器控制）

SRPC0位控制USB收发器的D+和D输入。在主机控制器模式下，将此位设置为1。在设备控制器模式下，断开连接时将此位设置为0，暂停时设置为1。该位仅在FIXPHY0位为1时有效。

FIXPHY0位（USB收发器输出修复）

FIXPHY0位保持禁用USB收发器的输出。

28.2.44 DPUSR1R:深度软件待机USB暂停恢复中断寄存器

Base address: USBFS = 0x4009_0000

Offset address: 0x404

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBINT0	—	DOVRCRB0	DOVRCRA0	—	—	DMINT0	DPINT0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	DVBSE0	—	DOVRCRBE0	DOVRCRAE0	—	—	DMINTE0	DPINTE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DPINTE0	USBDP中断使能清除 0：禁止通过DP输入从深度软件待机模式恢复1：允许通过DP输入从深度软件待机模式恢复	R/W
1	DMINTE0	USBDM中断使能清除 0：禁止通过DM输入从深度软件待机模式恢复1：允许通过DM输入从深度软件待机模式恢复	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	DOVRCRAE0	USBOVRCURA中断使能清除 0：通过OVRCURA输入禁止从深度软件待机模式恢复1：通过OVRCURA输入允许从深度软件待机模式恢复	R/W
5	DOVRCRBE0	USBOVRCURB中断使能清除 0：通过OVRCURB输入禁用从深度软件待机模式恢复1：通过OVRCURB输入从深度软件待机模式启用恢复	R/W
6	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	DVBSE0	USB VBUS Interrupt Enable/Clear 0: Disable recovery from Deep Software Standby mode by VBUS input 1: Enable recovery from Deep Software Standby mode by VBUS input	R/W
15:8	—	T These bits are read as 0. The write value should be 0. .	R/W
16	DPINT0	USB DP Interrupt Source Recovery 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of DP	R
17	DMINT0	USB DM Interrupt Source Recovery 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of DM input	R
19:18	—	This bit is read as 0. The write value should be 0.	R/W
20	DOVRCRA0	USB OVRCURA Interrupt Source Recovery 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of OVRCURA input	R
21	DOVRCRB0	USB OVRCURB Interrupt Source Recovery 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of OVRCURB input	R
22	—	This bit is read as 0. The write value should be 0.	R/W
23	DVBINT0	USB VBUS Interrupt Source Recovery 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of VBUS input	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

DPINTE0 bit (USB DP Interrupt Enable/Clear)

The DPINTE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the DP input of the USBFS. Writing 0 to this bit while the DPINT0 bit is 1 sets the DPINT0 bit to 0.

DMINTE0 bit (USB DM Interrupt Enable/Clear)

The DMINTE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the DM input of the USBFS. Writing 0 to this bit while the DMINT0 bit is 1 clears the DMINT0 bit to 0.

DOVRCRAE0 bit (USB OVRCURA Interrupt Enable/Clear)

The DOVRCRAE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the OVRCURA input of the USBFS. Writing 0 to this bit while the DOVRCRA0 bit is 1 clears the DOVRCRA0 bit to 0.

DOVRCRBE0 bit (USB OVRCURB Interrupt Enable/Clear)

The DOVRCRBE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the OVRCURB input of the USBFS. Writing 0 to this bit while the DOVRCRB0 bit is 1 clears the DOVRCRB0 bit to 0.

DVBSE0 bit (USB VBUS Interrupt Enable/Clear)

The DVBSE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the VBUS input of the USBFS. Writing 0 to this bit while the DVBINT0 bit is 1 clears the DVBINT0 bit to 0.

DPINT0 bit (USB DP Interrupt Source Recovery)

The DPINT0 bit indicates that the system has returned from Deep Software Standby mode because of the DP input of the USBFS. This recovery is only enabled when the DPINTE0 bit is 1. Writing 0 to the DPINTE0 bit while this bit is 1 clears this bit to 0.

DMINT0 bit (USB DM Interrupt Source Recovery)

The DMINT0 bit indicates that the system has returned from Deep Software Standby mode because of the DM input of the USBFS. This recovery is only enabled when the DMINTE0 bit is 1. Writing 0 to the DMINTE0 bit while this bit is 1 clears this bit to 0.

Bit	Symbol	Function	R/W
7	DVBSE0	USBVBUS中断使能清除 0：禁止通过VBUS输入从深度软件待机模式恢复1：使能通过VBUS输入从深度软件待机模式恢复	R/W
15:8	—	T这些位被读取为0。写入值应为0。	R/W
16	DPINT0	USBDP中断源恢复 0：系统尚未从深度软件待机模式中恢复1：系统由于DP从深度软件待机模式中恢复	R
17	DMINT0	USBDM中断源恢复 0：系统尚未从深度软件待机模式中恢复1：系统由于DM输入而从深度软件待机模式中恢复	R
19:18	—	该位读取为0。写入值应为0。	R/W
20	DOVRCRA0	USBOVRCURA中断源恢复 0：系统尚未从深度软件待机模式中恢复1：系统由于OVRCURA输入而从深度软件待机模式中恢复	R
21	DOVRCRB0	USBOVRCURB中断源恢复 0：系统尚未从深度软件待机模式中恢复1：系统由于OVRCURB输入而从深度软件待机模式中恢复	R
22	—	该位读取为0。写入值应为0。	R/W
23	DVBINT0	USBVBUS中断源恢复 0：系统尚未从深度软件待机模式中恢复1：系统由于VBUS输入而从深度软件待机模式中恢复	R
31:24	—	这些位被读取为0。写入值应为0。	R/W

DPINTE0位（USBDP中断使能清除）

DPINTE0位启用或禁用触发从深度软件待机模式恢复由DP输入USBFS。当DPINT0位为1时向该位写入0会将DPINT0位设置为0。

DMINTE0位（USBDM中断使能清除）

DMINTE0位启用或禁用触发从深度软件待机模式恢复由DM输入USBFS。当DMINT0位为1时向该位写入0会将DMINT0位清除为0。

DOVRCRAE0位（USBOVRCURA中断使能清除）

DOVRCRAE0位通过USBFS的OVRCURA输入启用或禁用从深度软件待机模式恢复的触发。当DOVRCRA0位为1时向该位写入0会将DOVRCRA0位清除为0。

DOVRCRBE0位（USBOVRCURB中断使能清除）

DOVRCRBE0位通过USBFS的OVRCURB输入启用或禁用从深度软件待机模式恢复的触发。当DOVRCRB0位为1时向该位写入0会将DOVRCRB0位清除为0。

DVBSE0位（USBVBUS中断使能清除）

DVBSE0位通过VBUS输入启用或禁用从深度软件待机模式恢复的触发USBFS。当DVBINT0位为1时向该位写入0会将DVBINT0位清除为0。

DPINT0位（USBDP中断源恢复）

由于USBFS的DP输入，DPINT0位指示系统已从深度软件待机模式返回。此恢复仅在DPINTE0位为1时启用。当该位为1时向DPINTE0位写入0将该位清除为0。

DMINT0位（USBDM中断源恢复）

由于USBFS的DM输入，DMINT0位指示系统已从深度软件待机模式返回。此恢复仅在DMINTE0位为1时启用。当该位为1时向DMINTE0位写入0会将该位清除为0。

DOVRCRA0 bit (USB OVRCURA Interrupt Source Recovery)

The DOVRCRA0 bit indicates that the system has returned from Deep Software Standby mode because of the OVRCURA input of the USBFS. This recovery is only enabled when the DOVRCRAE0 bit is 1. Writing 0 to the DOVRCRAE0 bit while this bit is 1 clears this bit to 0.

DOVRCRB0 bit (USB OVRCURB Interrupt Source Recovery)

The DOVRCRB0 bit indicates that the system has returned from Deep Software Standby mode because of the OVRCURB input of the USBFS. This recovery is only enabled when the DOVRCRBE0 bit is 1. Writing 0 to the DOVRCRBE0 bit while this bit is 1 clears this bit to 0.

DVBINT0 bit (USB VBUS Interrupt Source Recovery)

The DVBINT0 bit indicates that the system has returned from Deep Software Standby mode because of the VBUS input of the USBFS. This recovery is only enabled when the DVBSE0 bit is 1. Writing 0 to the DVBSE0 bit while this bit is 1 clears this bit to 0.

28.3 Operation

28.3.1 System Control

This section describes register settings required for initializing the USBFS and controlling power consumption.

28.3.1.1 Setting data to the USBFS registers

Setting the SYSCFG.USBE bit to 1 after starting the clock supply (SYSCFG.SCKE bit = 1) enables and starts USBFS operation.

28.3.1.2 Selecting the controller function

The USBFS can operate as either a host or device controller.

Use the SYSCFG.DCFM bit to select one of these USBFS functions. The DCFM bit must be changed in the initial settings immediately after a reset or in the D+ pull-up-disabled state (SYSCFG.DPRPU bit = 0) and D+ and D– pull-down-disabled state (SYSCFG.DRPD bit = 0).

28.3.1.3 Controlling the USB data bus using resistors

The USBFS provides pull-up and pull-down resistors for the D+ and D– lines. Pull these lines up or down by setting the SYSCFG.DPRPU and DRPD bits.

In device controller mode, confirm that connection to the USB host is made, and then set the SYSCFG.DPRPU bit to 1 and pull up the D+ line (in full-speed communication).

When the SYSCFG.DPRPU bit is set to 0 during communication with a PC, the USBFS disables the pull-up resistor of the USB data line, thereby notifying the USB host of disconnection.

In host controller mode, set the SYSCFG.DRPD bit to 1 to pull down the D+ and D– lines.

Table 28.14 USB data bus resistor control

SYSCFG register settings		USB data bus control		
DRPD bit	DPRPU bit	D–	D+	Function
0	0	Open	Open	When resistors not used
0	1	Open	Pull-up	When operating as a device controller at full-speed
1	0	Pull-down	Pull-down	When operating as a host controller
1	1	—	—	Setting prohibited

28.3.1.4 Example external connection circuits

Figure 28.2 shows an example OTG connection in the self-powered system. The USBFS controls the pull-up resistor of the D+ line and the pull-down resistor of D+ and D- lines. Select pull-up and pull-down for the lines in the SYSCFG.DPRPU

DOVRCRA0位（USBOVRCURA中断源恢复）

由于USBFS的OVRCURA输入，DOVRCRA0位指示系统已从深度软件待机模式返回。此恢复仅在DOVRCRAE0位为1时启用。当此位为1时向DOVRCRAE0位写入0会将该位清除为0。

DOVRCRB0位（USBOVRCURB中断源恢复）

DOVRCRB0位指示由于USBFS的OVRCURB输入，系统已从深度软件待机模式返回。此恢复仅在DOVRCRBE0位为1时启用。当此位为1时向DOVRCRBE0位写入0会将该位清除为0。

DVBINT0位（USBVBUS中断源恢复）

由于USBFS的VBUS输入，DVBINT0位指示系统已从深度软件待机模式返回。此恢复仅在DVBSE0位为1时启用。当该位为1时将0写入DVBSE0位可将该位清除为0。

28.3 Operation

28.3.1 系统控制

本节介绍初始化USBFS和控制功耗所需的寄存器设置。

28.3.1.1 将数据设置到USBFS寄存器

启动时钟供应（SYSCFG.SCKE位=1）后将SYSCFG.USBE位设置为1启用并启动USBFS操作。

28.3.1.2 选择控制器功能

USBFS可以作为主机或设备控制器运行。

使用SYSCFG.DCFM位选择这些USBFS功能之一。DCFM位必须在复位后立即更改为初始设置或在D+上拉禁用状态（SYSCFG.DPRPU位=0）和D+和D 下拉禁用状态（SYSCFG.DRPD位=0））。

28.3.1.3 使用电阻控制USB数据总线

USBFS为D+和D−线提供上拉和下拉电阻。通过设置
SYSCFG.DPRPU和DRPD位。

在设备控制器模式下，确认与USB主机的连接已建立，然后将SYSCFG.DPRPU位设置为1并拉高D+线（全速通信）。

当SYSCFG.DPRPU位在与PC通信期间设置为0时，USBFS禁用上拉电阻
USB数据线，从而通知USB主机断开。

在主机控制器模式下，将SYSCFG.DRPD位设置为1以拉低D+和D−线。

Table 28.14 USB数据总线电阻控制

SYSCFG寄存器设置		USB数据总线控制		
DRPD bit	DPRPU bit	D–	D+	Function
0	0	Open	Open	不使用电阻时
0	1	Open	Pull-up	作为设备控制器全速运行时
1	0	Pull-down	Pull-down	作为主机控制器运行时
1	1	—	—	禁止设定

28.3.1.4 外部连接电路示例

图28.2显示了自供电系统中的示例OTG连接。USBFS控制的上拉电阻
D+线和D+和Dlines的下拉电阻。为SYSCFG.DPRPU中的行选择上拉和下拉

and SYSCFG.DRPD bits. In device controller mode, the pull-up resistor of USB data line is disabled if SYSCFG.DPRPU bit is set to 0 while communicating with the USB host. The USBFS can use this to notify the USB host of a device disconnect.

和SYSCFG.DRPD位。在设备控制器模式下，如果在与USB主机通信时将SYSCFG.DPRPU位设置为0，则禁用USB数据线的上拉电阻。USBFS可以使用它来通知USB主机设备断开连接。

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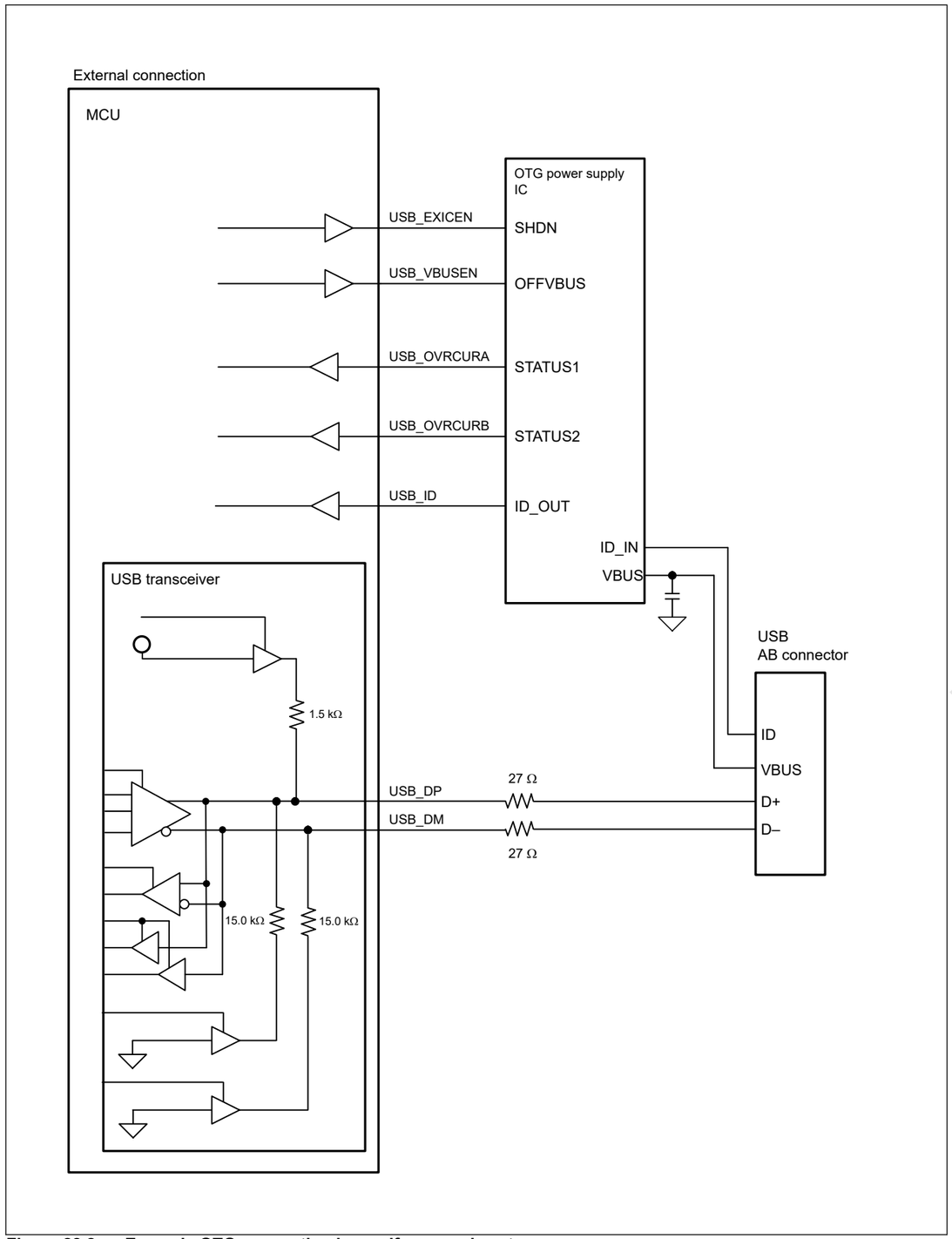


Figure 28.2 Example OTG connection in a self-powered system

Figure 28.3 shows an example device connection in a self-powered system.

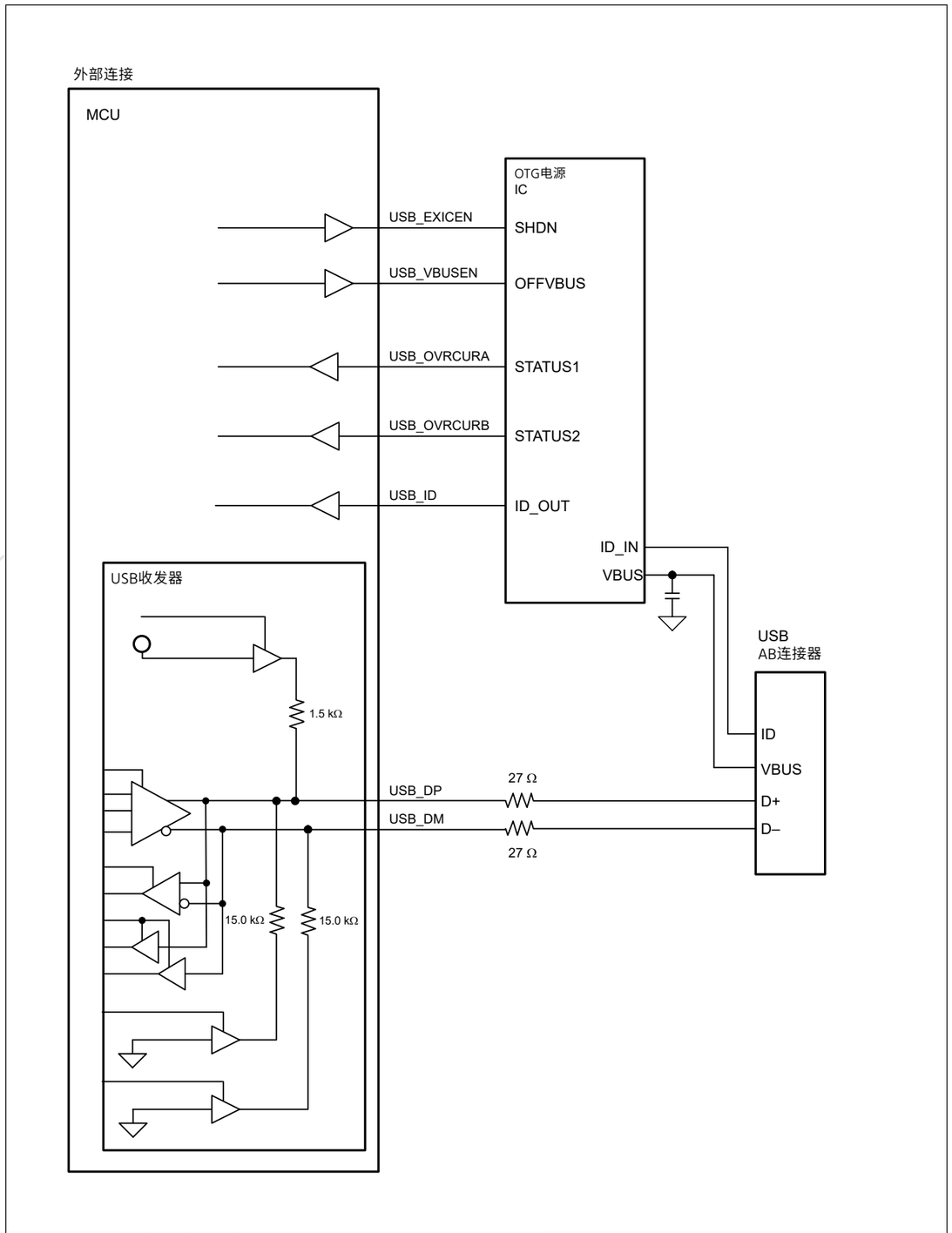
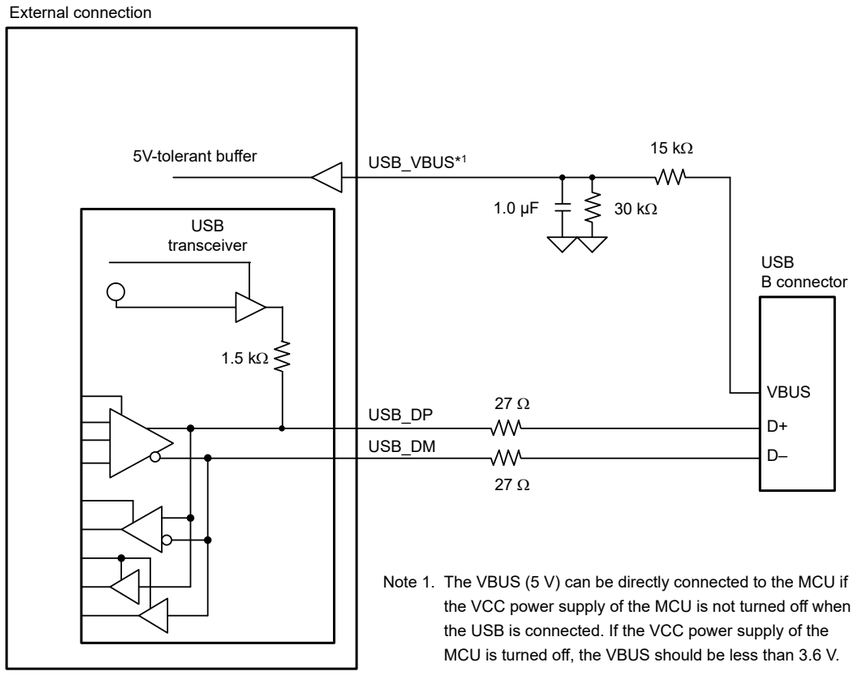


Figure 28.2 自供电系统中的示例OTG连接

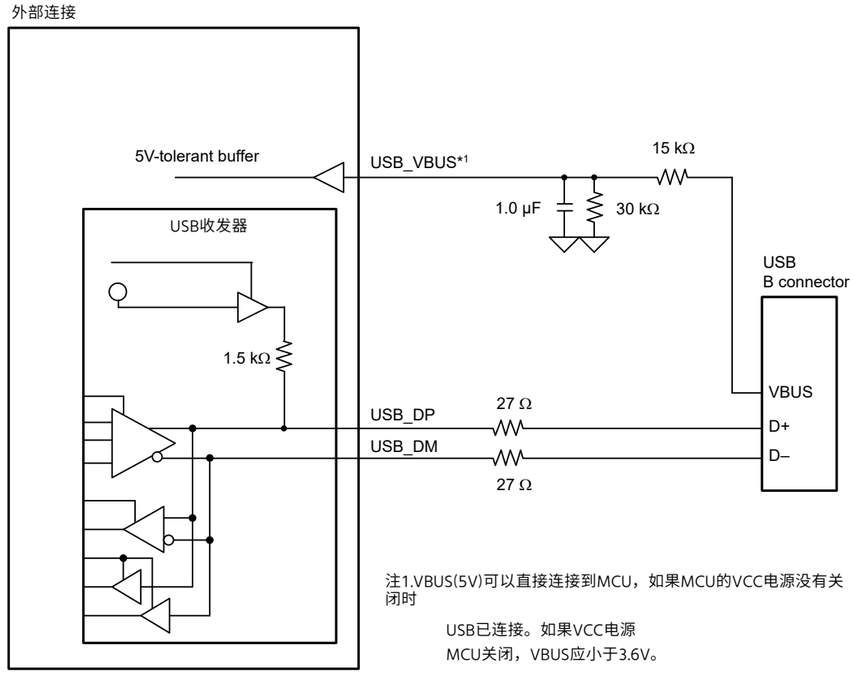
图28.3显示了自供电系统中的示例设备连接。



Note 1. The VBUS (5 V) can be directly connected to the MCU if the VCC power supply of the MCU is not turned off when the USB is connected. If the VCC power supply of the MCU is turned off, the VBUS should be less than 3.6 V.

Figure 28.3 Example device connection in a self-powered system

Figure 28.4 shows an example host connection.



注1.VBUS(5V)可以直接连接到MCU，如果MCU的VCC电源没有关闭时

USB已连接。如果VCC电源
MCU关闭，VBUS应小于3.6V。

Figure 28.3 自供电系统中的示例设备连接

图28.4显示了一个示例主机连接。

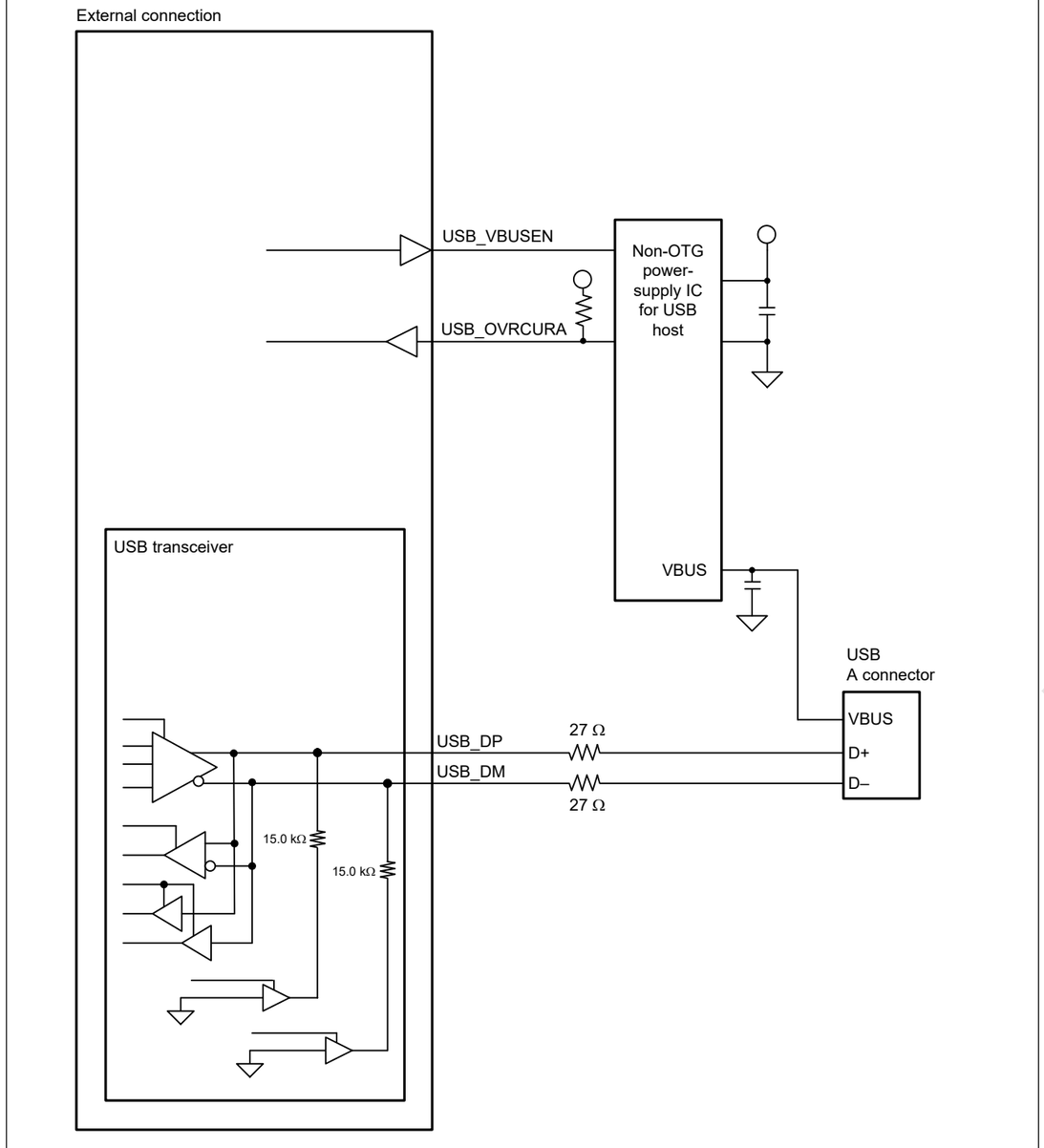


Figure 28.4 Example host connection

Figure 28.5 shows an example device connection in a bus-powered system.

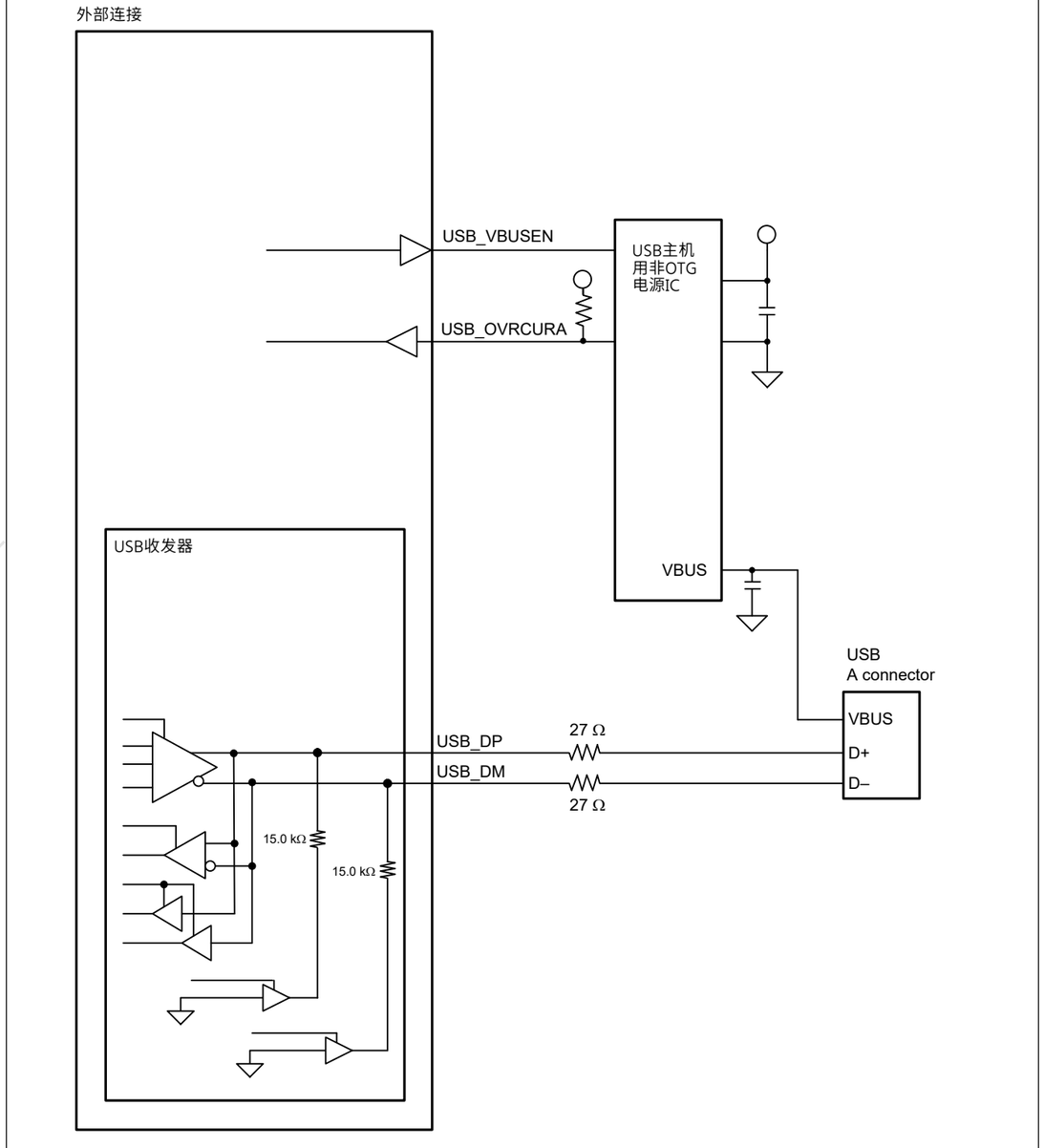


Figure 28.4 主机连接示例

图28.5显示了总线供电系统中的示例设备连接。

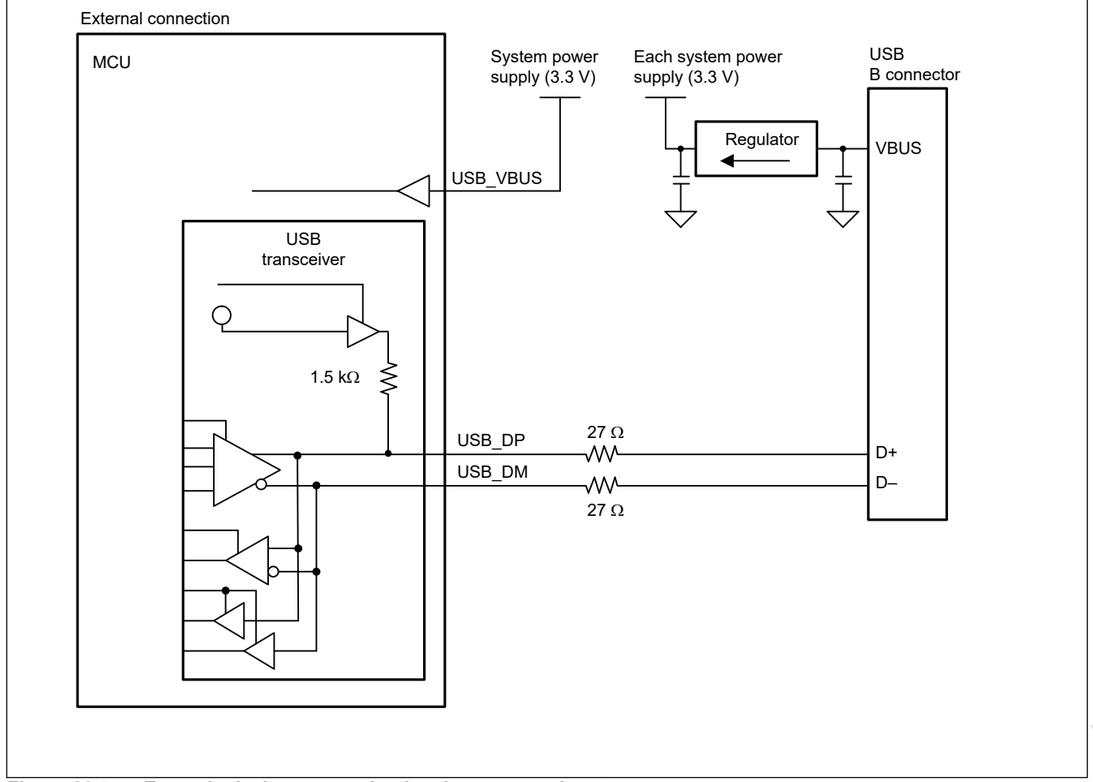


Figure 28.5 Example device connection in a bus-powered state

Figure 28.6 shows an example of functional connection of the USB connector with Battery Charging Rev 1.2 supported.

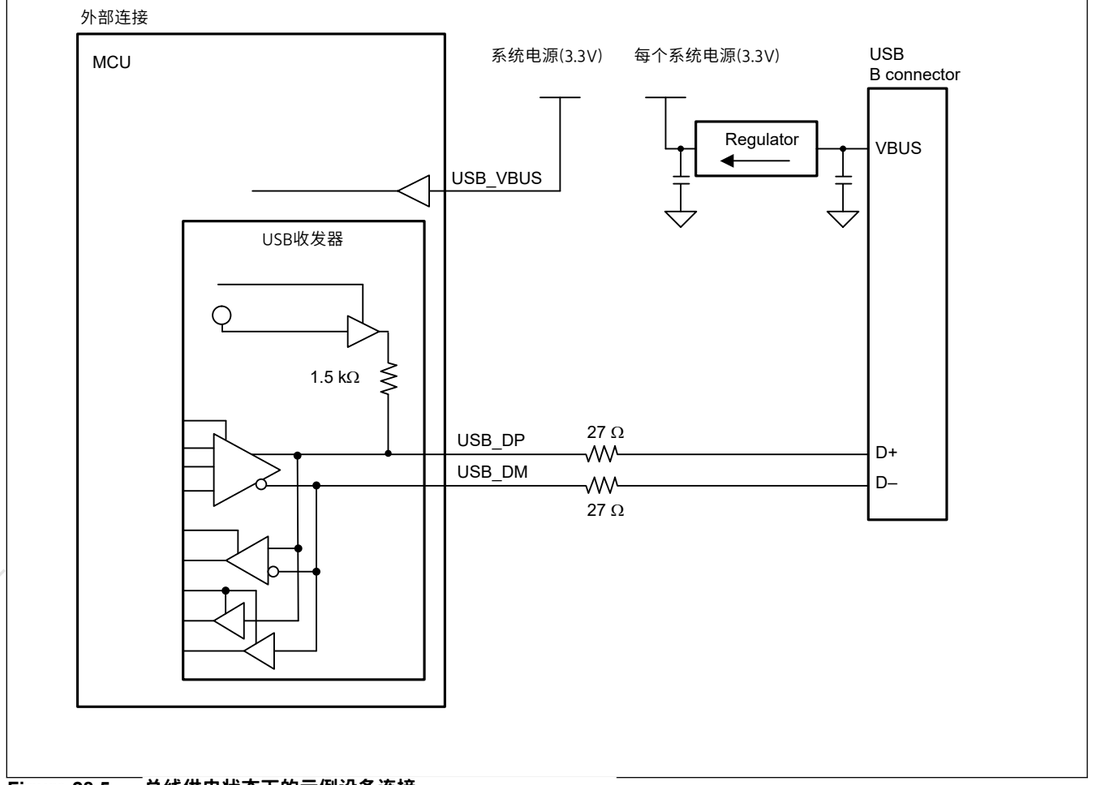


Figure 28.5 总线供电状态下的示例设备连接

图28.6显示了支持电池充电Rev1.2的USB连接器的功能连接示例。

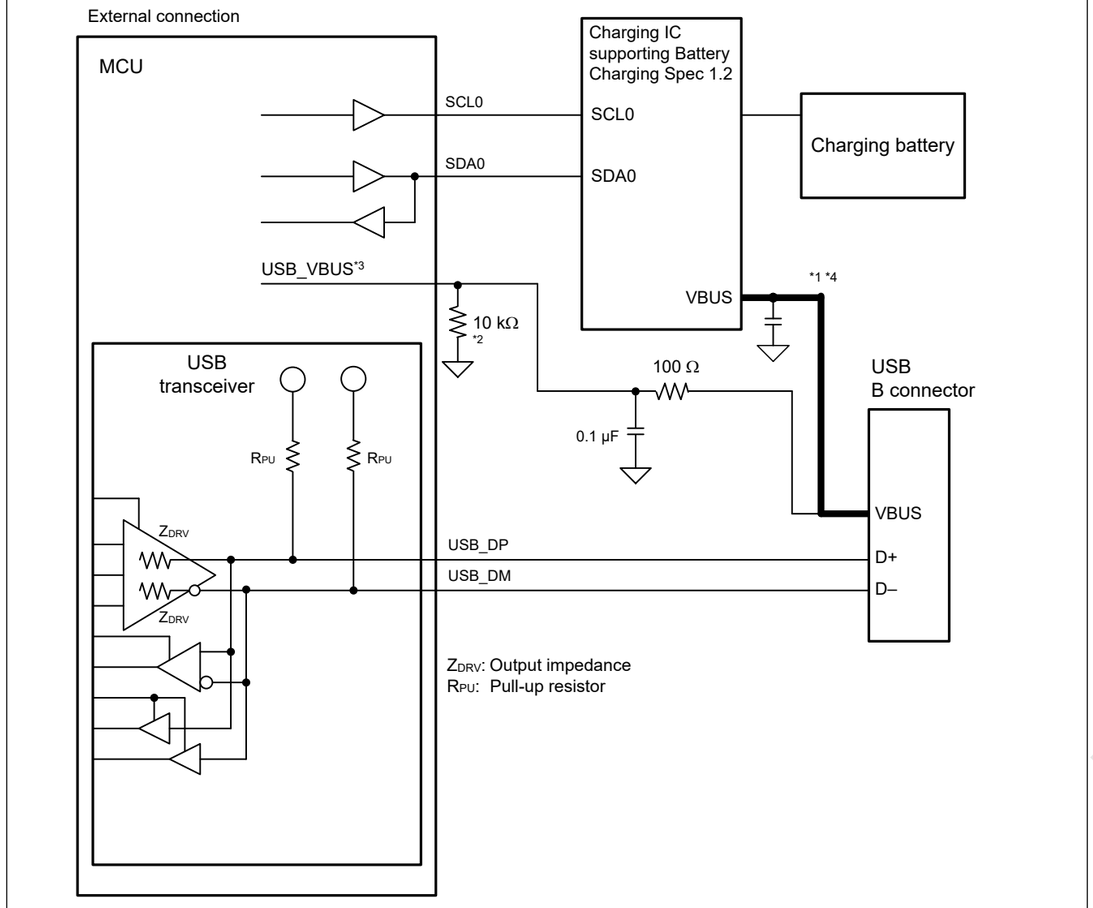


Figure 28.6 Example of functional connection with Battery Charging Rev 1.2 supported

The examples of external circuits given in this section are simplified circuits, and their operation in every system is not guaranteed.

28.3.1.5 Release from deep software standby mode because of USB suspend/resume interrupts

Deep Software Standby mode can be canceled by a USB suspend/resume interrupt. USB suspend/resume interrupts are detected by the USB resume detecting unit, which controls and monitors the USB I/O pins to detect the interrupts.

Figure 28.7 shows a schematic diagram of the connection between the USB resume detecting unit and the USB I/O pins.

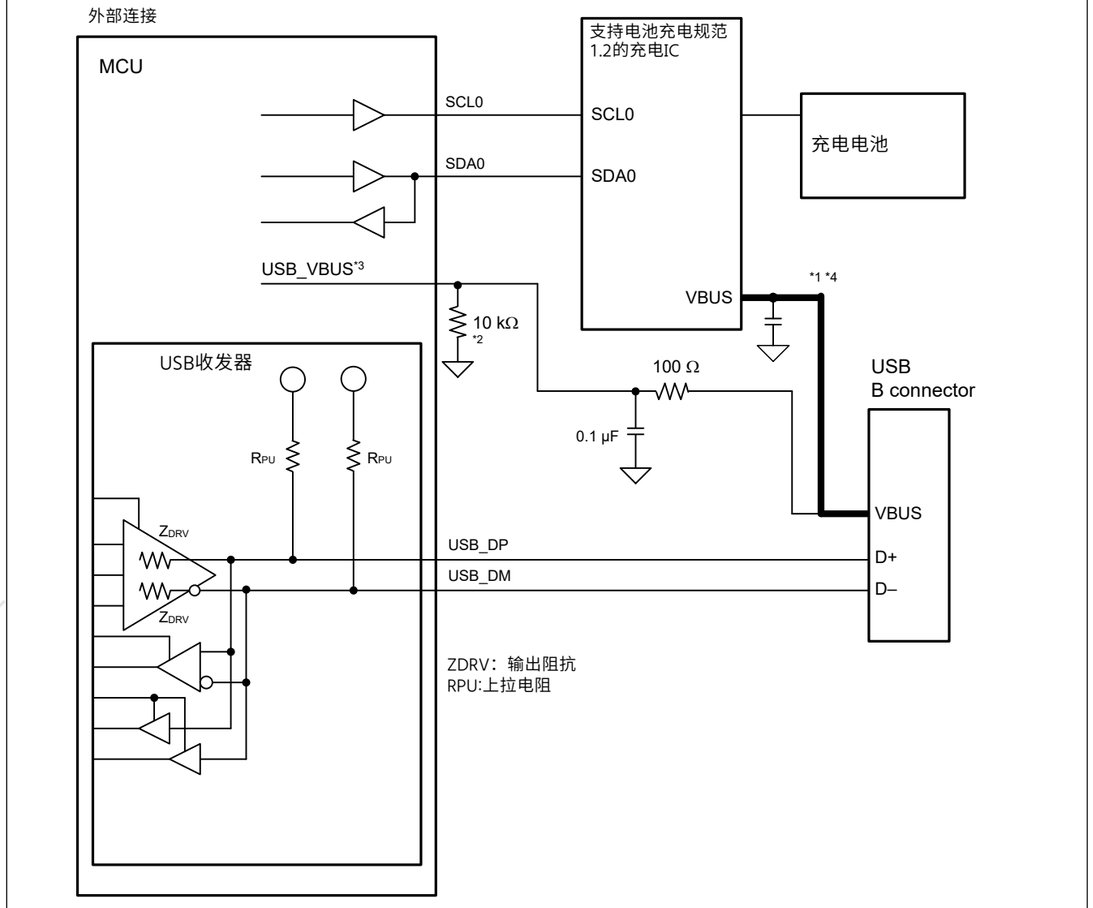


Figure 28.6 支持电池充电版本1.2的功能连接示例

本节中给出的外部电路示例是简化电路，不保证它们在每个系统中的操作。

28.3.1.5 由于USB挂起恢复中断而从深度软件待机模式中释放

深度软件待机模式可以通过USB挂起恢复中断来取消。USB暂停恢复中断由USB恢复检测单元检测，该单元控制和监视USBIO引脚以检测中断。

图28.7显示了USB恢复检测单元与USBIO引脚之间的连接示意图。

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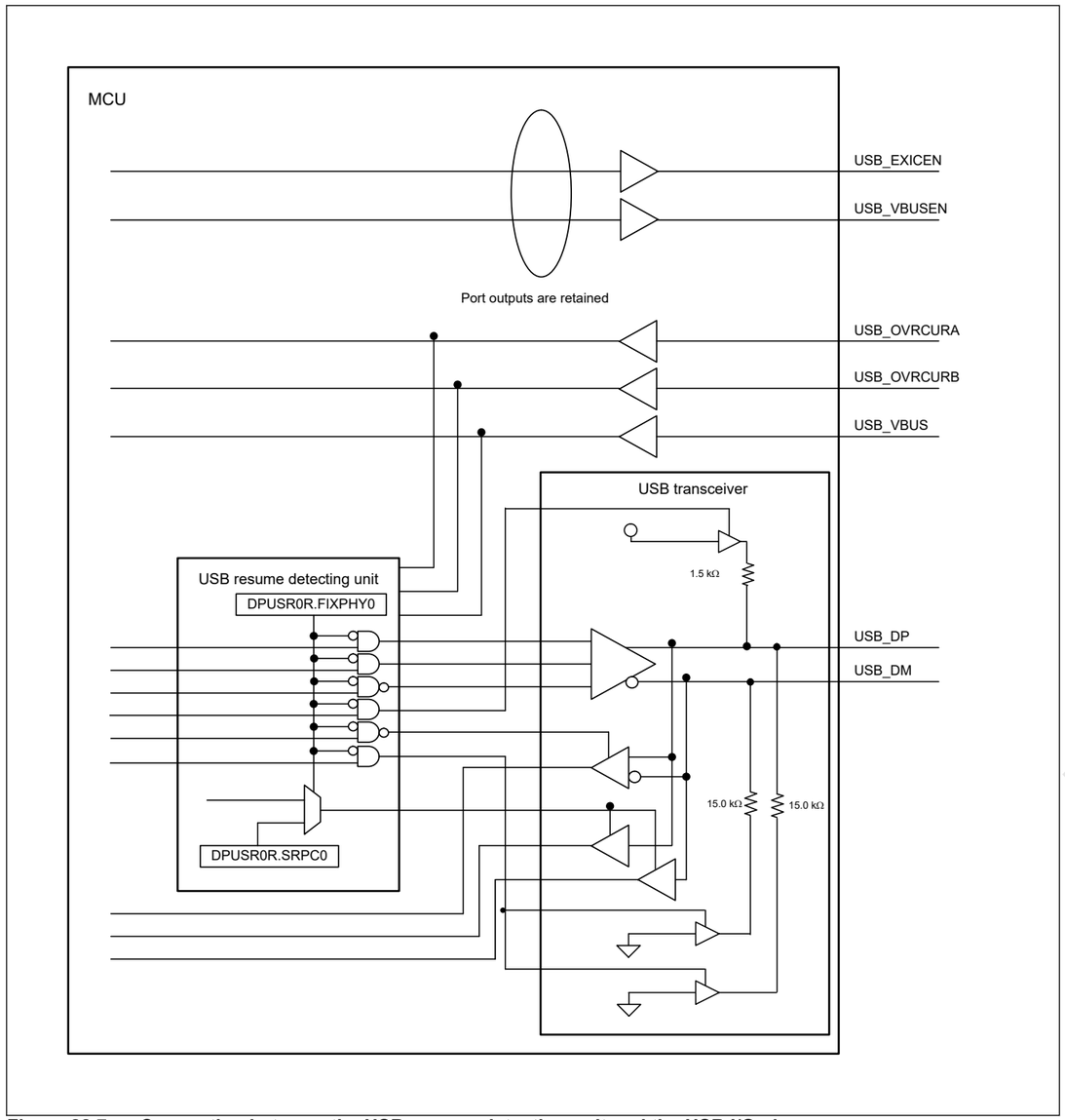

Figure 28.7 Connection between the USB resume detecting unit and the USB I/O pins

Table 28.15 shows the USB suspend and resume interrupt sources and their associated I/O pins.

Table 28.15 USB suspend and resume interrupt sources and their associated I/O pins

USB operating mode	Source	Pin name
Device, OTG	Resume	USB_DP
Host, OTG	Attach or detach	USB_DP, USB_DM
Device	Attach or detach	USB_VBUS
Host	Overcurrent detection	USB_OVRCURA
OTG	Overcurrent detection	USB_OVRCURA, USB_OVRCURB

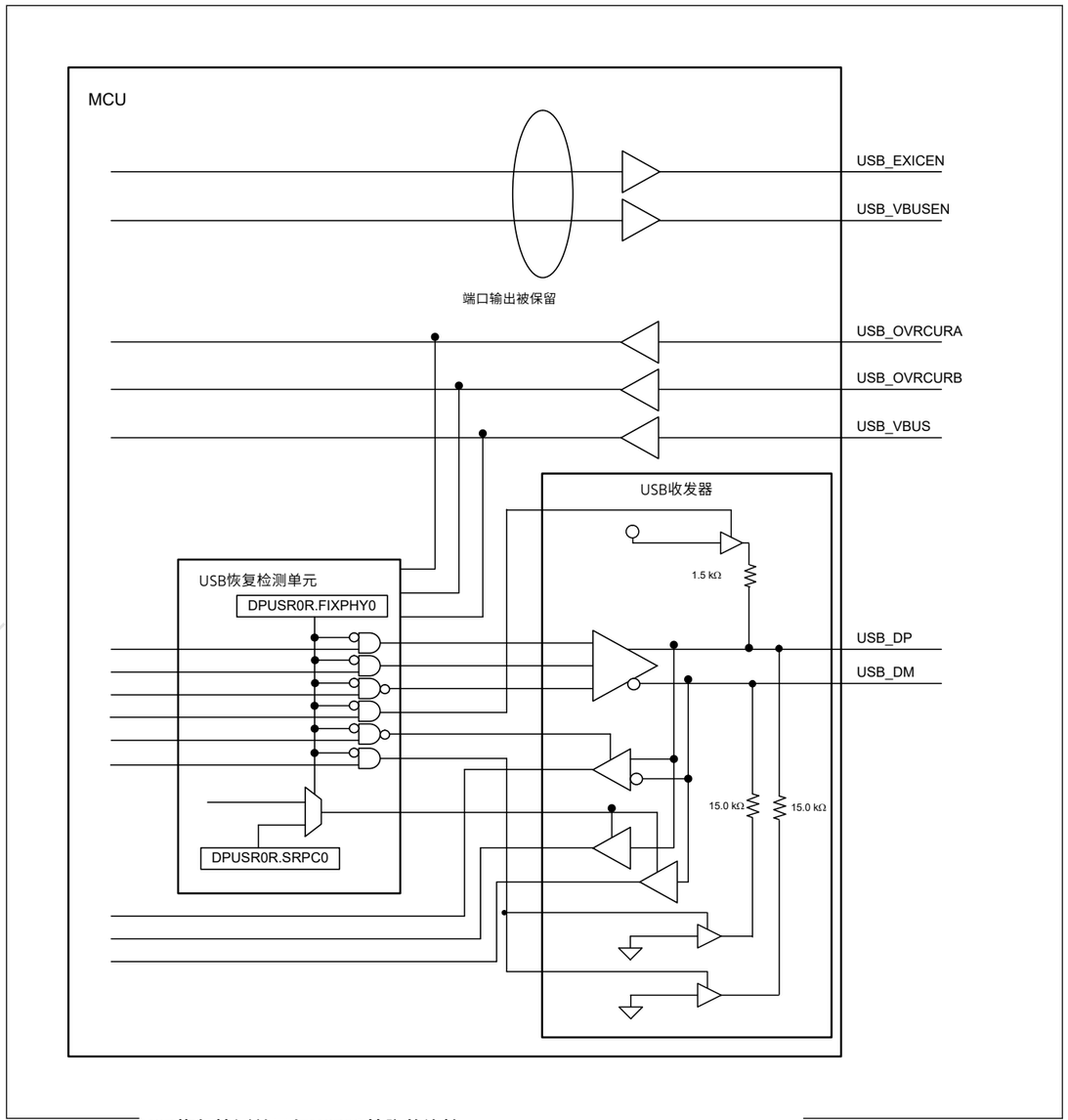

Figure 28.7 USB恢复检测单元与USBIO管脚的连接

表28.15显示了USB挂起和恢复中断源及其相关的IO引脚。

Table 28.15 USB挂起和恢复中断源及其相关的IO引脚

USB操作模式	Source	引脚名称
Device, OTG	Resume	USB_DP
Host, OTG	连接或分离	USB_DP, USB_DM
Device	连接或分离	USB_VBUS
Host	Overcurrent detection	USB_OVRCURA
OTG	Overcurrent detection	USB_OVRCURA, USB_OVRCURB

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Figure 28.8 shows the flow for setting the USBFS when entering Deep Software Standby mode from either host or device controller mode. Figure 28.9 shows the flow for setting the USBFS when canceling Deep Software Standby mode from host controller mode. Figure 28.10 shows the flow for setting the USBFS when canceling Deep Software Standby mode from device controller mode.

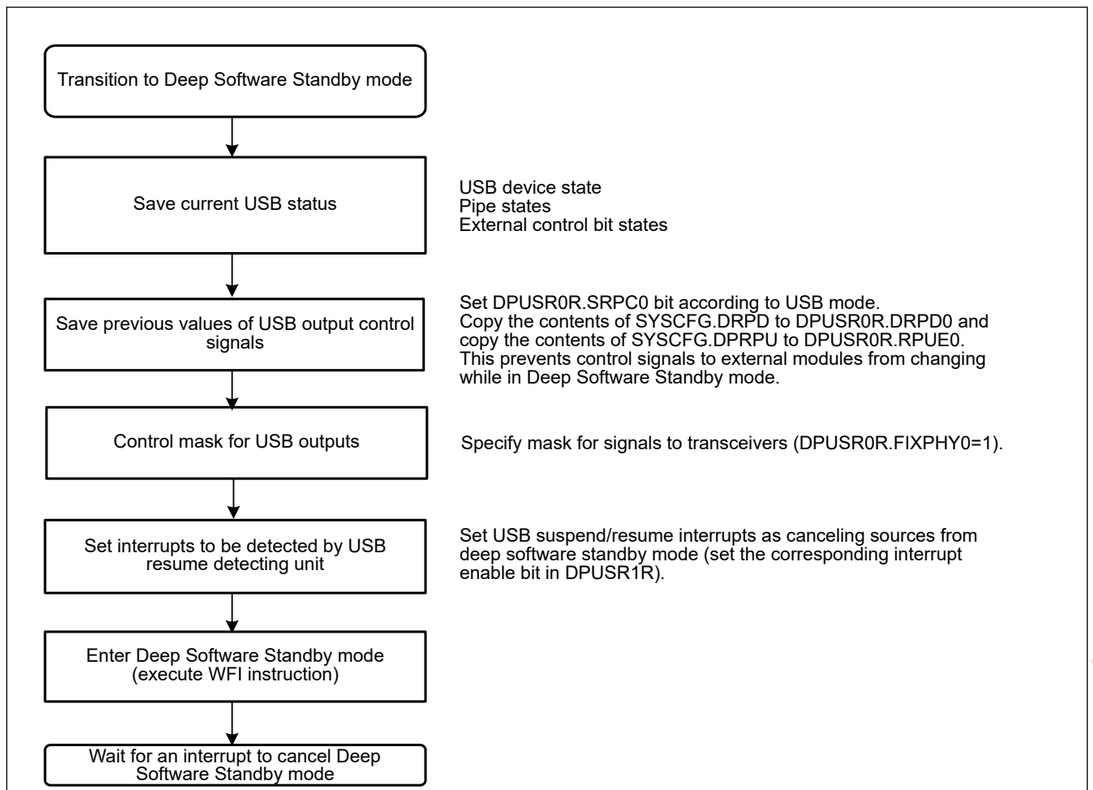

Figure 28.8 USBFS setup flow for transition to Deep Software Standby mode as host or device controller

图28.8显示了从主机或设备控制器模式进入深度软件待机模式时设置USBFS的流程。图28.9显示了从主机控制器模式取消深度软件待机模式时设置USBFS的流程。图28.10显示了从设备控制器模式取消深度软件待机模式时设置USBFS的流程。

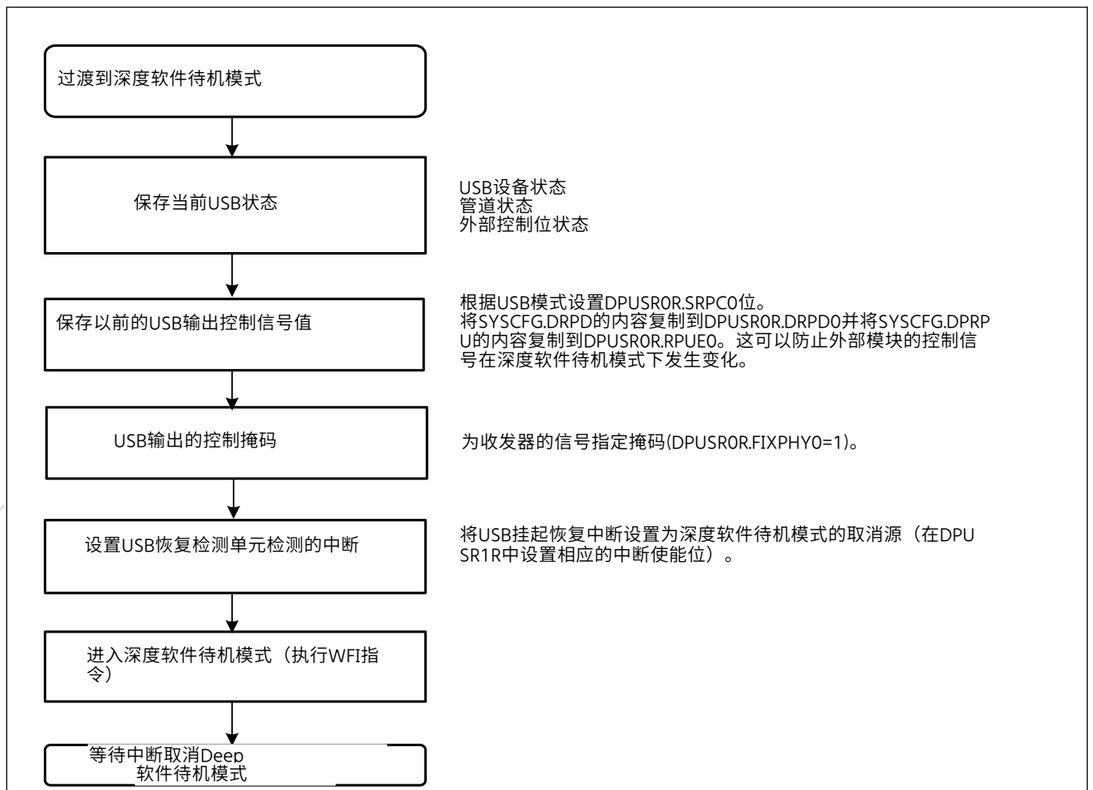

Figure 28.8 作为主机或设备控制器转换到深度软件待机模式的USBFS设置流程

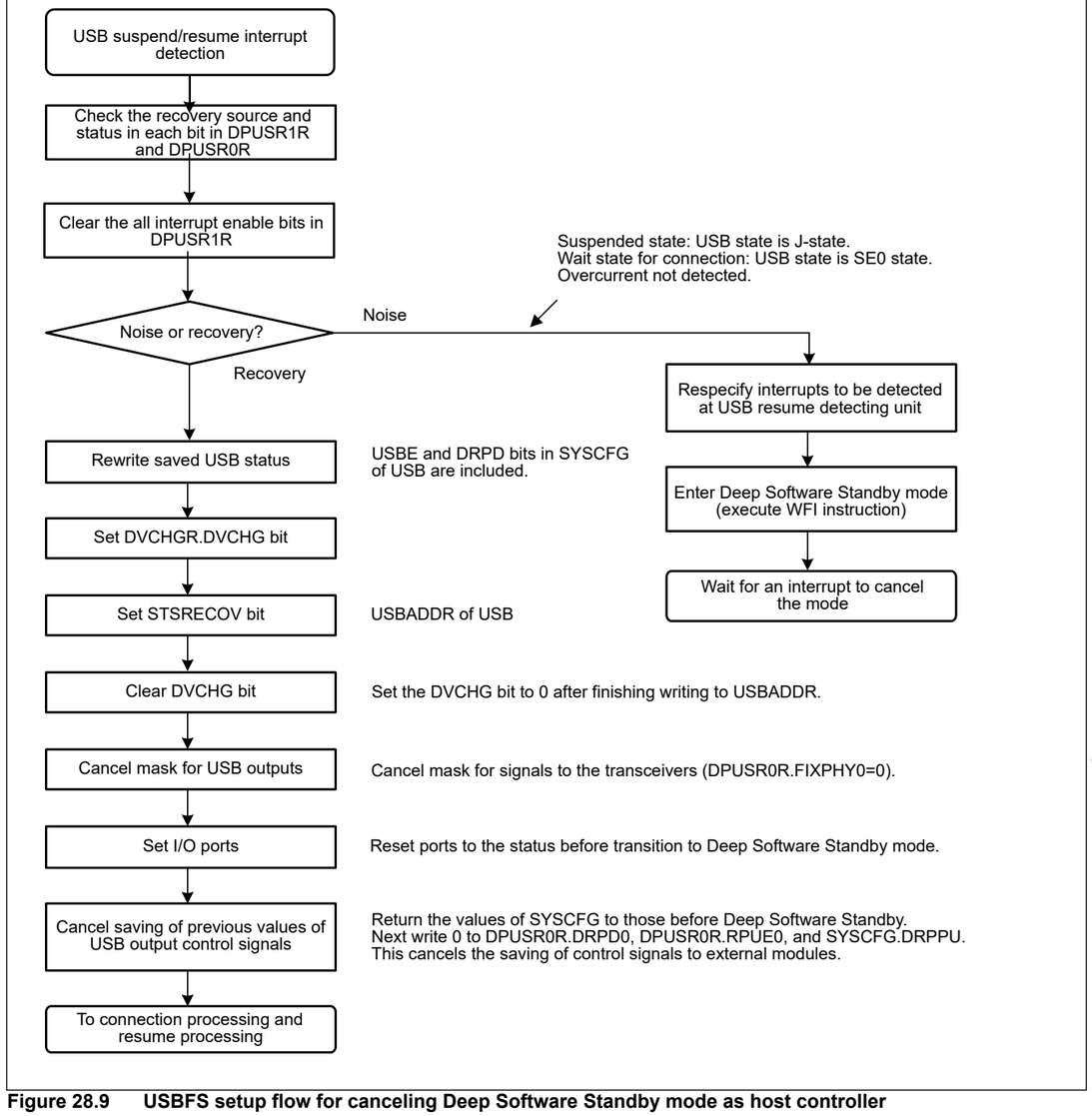

Figure 28.9 USBFS setup flow for canceling Deep Software Standby mode as host controller

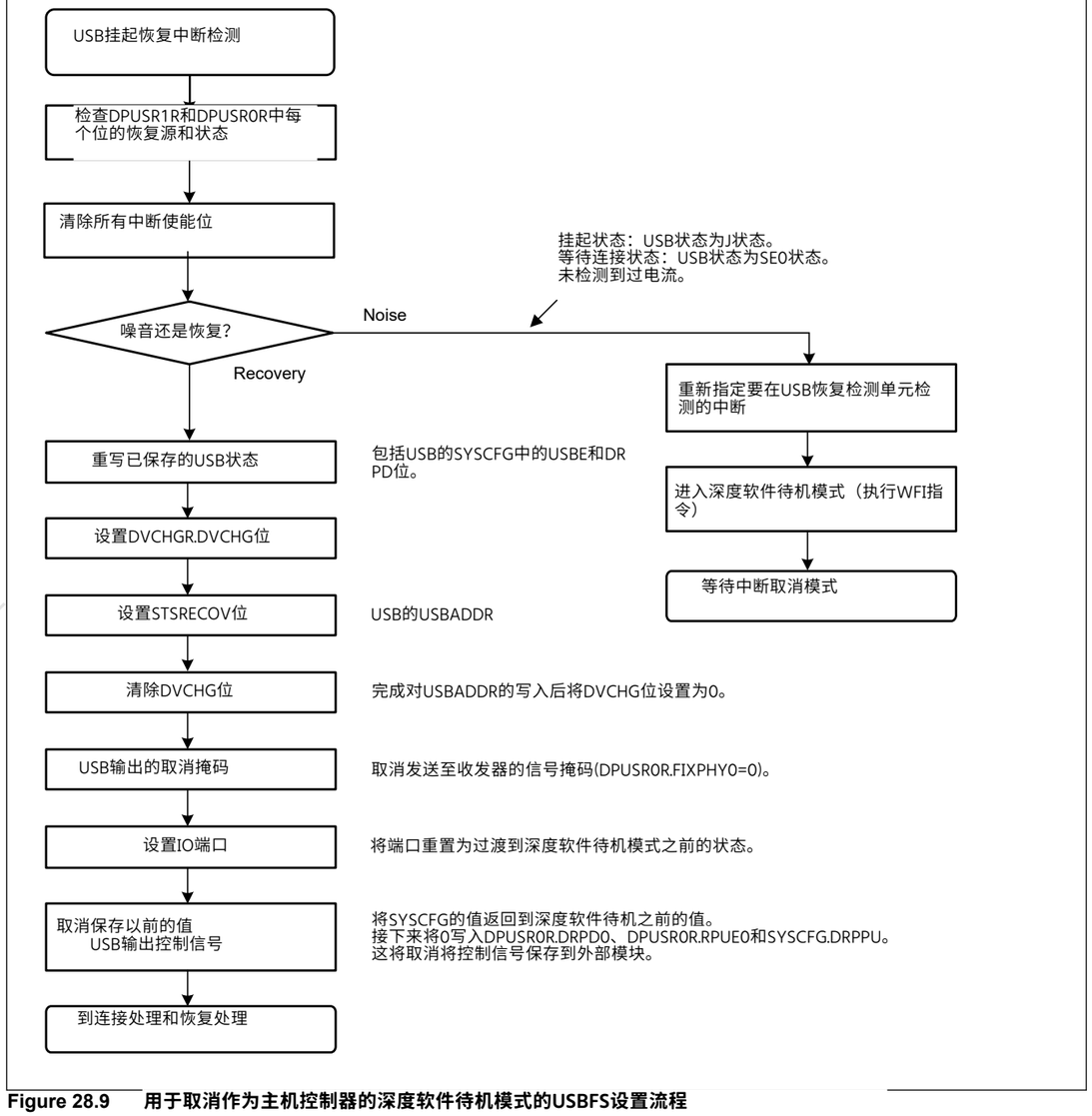

Figure 28.9 用于取消作为主机控制器的深度软件待机模式的USBFS设置流程

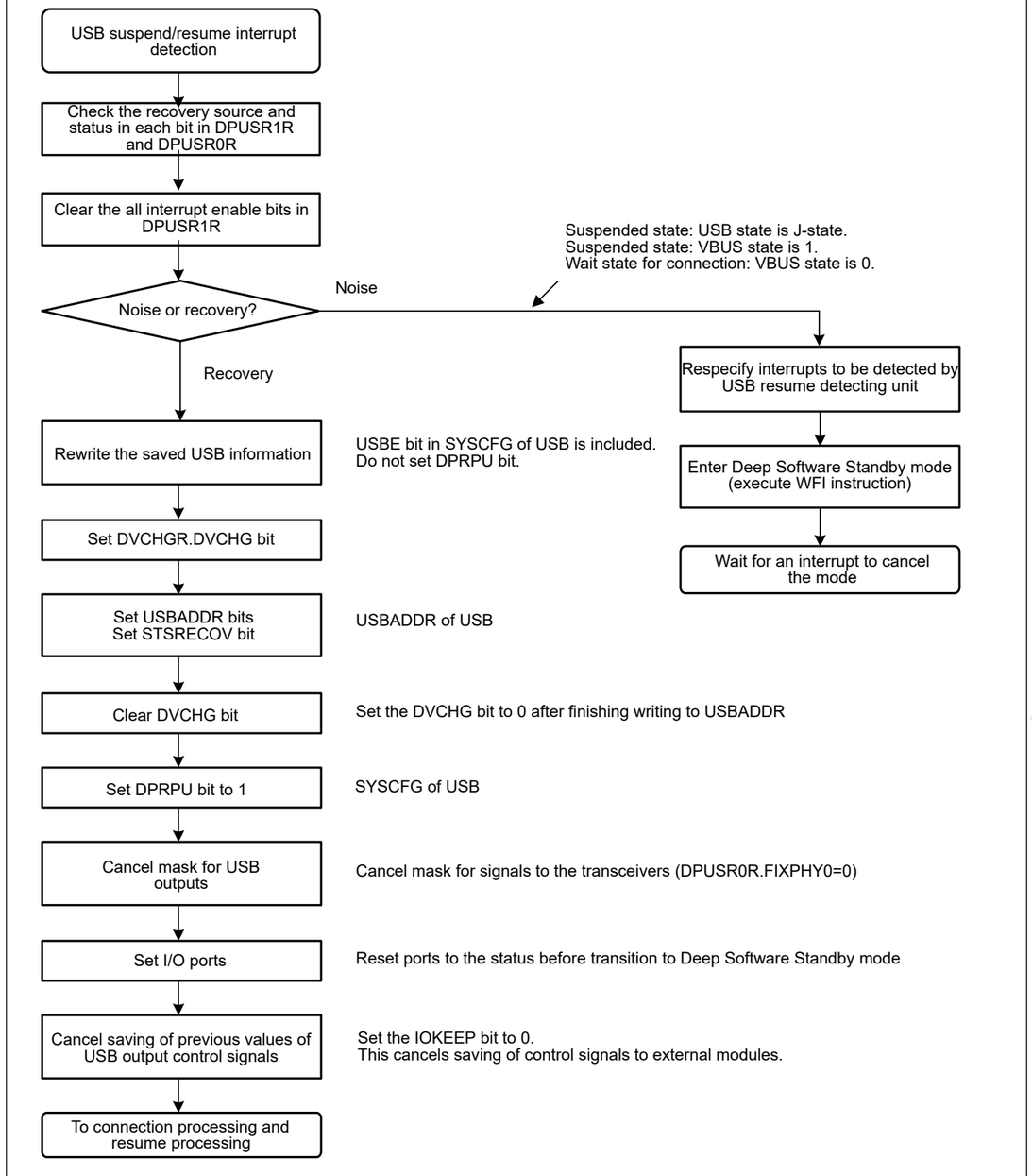

Figure 28.10 USBFS setup flow for canceling Deep Software Standby mode as device controller

28.3.2 Interrupts

Table 28.16 lists the interrupt sources in the USBFS. When an interrupt generation condition is satisfied and the interrupt output is enabled using the associated interrupt enable register, a USBFS interrupt request is issued to the Interrupt Controller Unit (ICU) and an USBFS interrupt is generated.

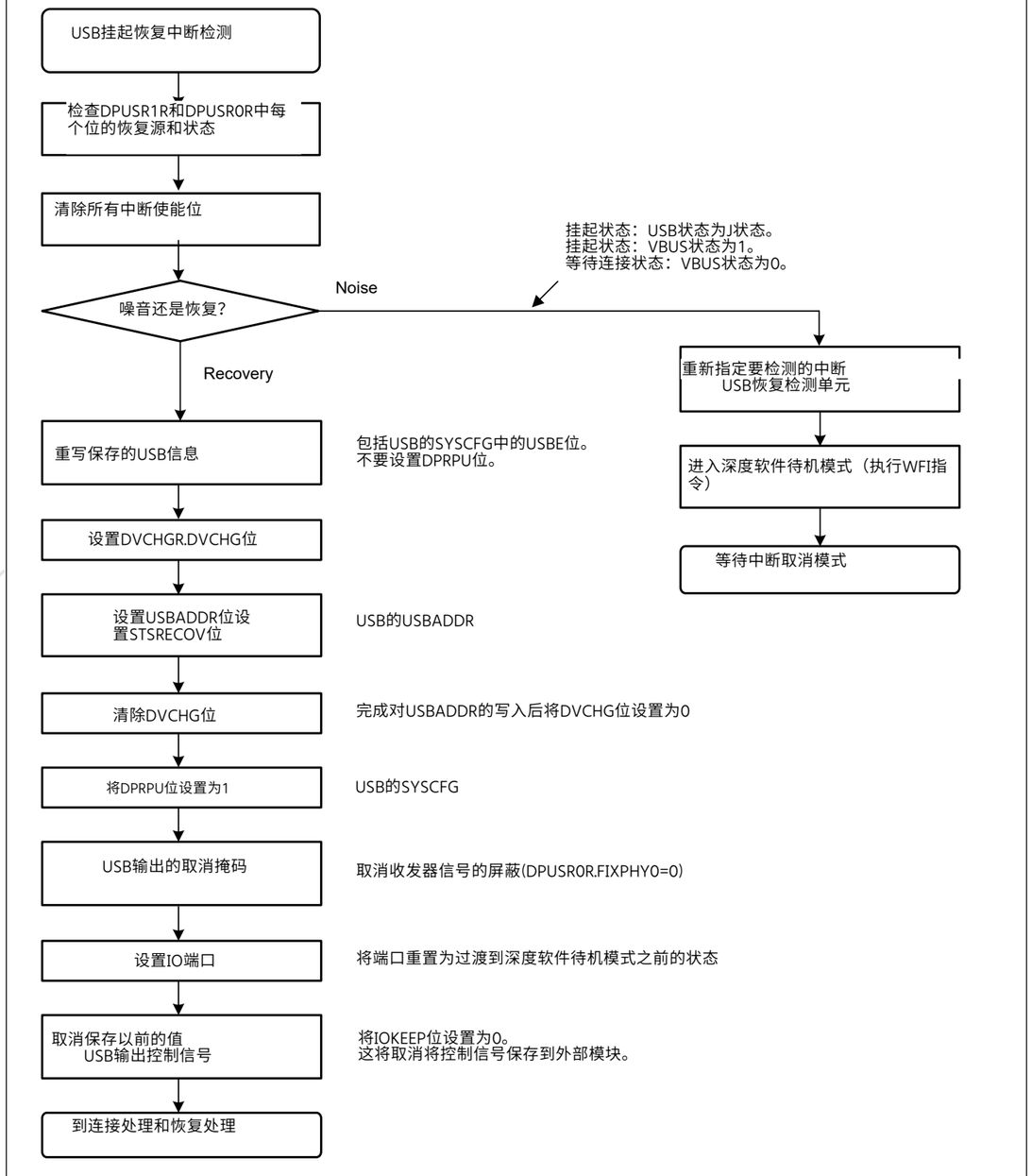

Figure 28.10 用于取消作为设备控制器的深度软件待机模式的USBFS设置流程

28.3.2 Interrupts

表28.16列出了USBFS中的中断源。当满足中断生成条件并使用相关的中断使能寄存器启用中断输出时，将向中断控制器单元(ICU)发出USBFS中断请求并生成USBFS中断。

Table 28.16 Interrupt sources (1 of 2)

Bit to be set to 1	Name	Interrupt source	Applicable controller function	Status flag
VBINT	VBUS interrupt	• A change in the state of the USB_VBUS input pin was detected (low to high or high to low)	Host or device*1	INTSTS0.VBSTS
RESM	Resume interrupt	• A change in the state of the USB bus was detected in the Suspend state (J-state to K-state or J-state to SE0)	Device	—
SOFR	Frame number update interrupt	In host controller mode: • An SOF packet with a different frame number was transmitted In device controller mode: • An SOF packet with a different frame number was received	Host or device	—
DVST	Device state transition interrupt	• One of the following device state transitions was detected: – USB bus reset was detected – Suspend state was detected – SET_ADDRESS request was received – SET_CONFIGURATION request was received	Device	INTSTS0.DVSQ[2:0]
CTRT	Control transfer stage transition interrupt	• A control transfer stage transition was detected because of one of the following: – Setup stage completed – Control write transfer status stage transition occurred – Control read transfer status stage transition occurred – Control transfer completed – Control transfer sequence error occurred	Device	INTSTS0.CTSQ[2:0]
BEMP	Buffer empty interrupt	• The buffer is empty after all FIFO buffer data was transmitted • A packet larger than the maximum packet size was received	Host or device	BEMPSTS.PIPEnBEMP
NRDY	Buffer not ready interrupt	In host controller mode • A STALL response was received from the peripheral device in response to the issued token • The response from the peripheral device in response to the issued token was not received successfully (no response three times consecutively or packet reception error three times consecutively) • An overrun or underrun error occurred during isochronous transfer In device controller mode • NAK was returned for an IN or OUT token while the PID[1:0] bits were set to 01b (BUF) • A CRC error or bit stuffing error occurred during data reception in isochronous transfer • An overrun or underrun occurred during data reception in isochronous transfer	Host or device	NRDYSTS.PIPEnNRDY
BRDY	Buffer ready interrupt	• The buffer is ready (readable or writable state)	Host or device	BRDYSTS.PIPEnBRDY
OVRCR	Overcurrent input change interrupt	• USB_OVRCURA or USB_OVRCURB input pin state change was detected (low to high or high to low)	Host	INTSTS1.OVRCR
BCHG	Bus change interrupt	• USB bus state change was detected	Host or device	SYSSTS0.LNST[1:0]
DTCH	Disconnect detection during full-speed operation	Peripheral device disconnect was detected in full-speed operation	Host	DVSTCTR0.RHST[2:0]
ATTCH	Device connect detection interrupt	• J-state or K-state was detected on the USB bus for 2.5 µs continuously This interrupt can be used to check whether peripheral devices are connected	Host	—

Table 28.16 中断源(1of2)

要设置为1的位	Name	中断源	适用控制器功能	状态标志
VBINT	VBUS interrupt	• 检测到USB_VBUS输入引脚的状态发生变化（从低到高或从高到低）	主机或设备*1	INTSTS0.VBSTS
RESM	恢复中断	• 检测到USB总线的状态发生变化 挂起状态（J状态到K状态或J状态到SE0）	Device	—
SOFR	帧号更新中断	在主机控制器模式下： 在设备控制器模式下传输了具有不同帧号的SOF数据包：● 接收到具有不同帧号的SOF数据包	主机或设备	—
DVST	设备状态转换中断	• 检测到以下设备状态转换之一： – 检测到USB总线复位 – 检测到挂起状态 – 收到SET_ADDRESS请求 – 已收到SET_CONFIGURATION请求	Device	INTSTS0.DVSQ[2:0]
CTRT	控制转移阶段转换中断	• 由于以下原因之一，检测到控制转移阶段转换： – 设置阶段完成 – 发生控制写传输状态阶段转换 – 发生控制读取传输状态阶段转换 – 控制转移完成 – 发生控制传输序列错误	Device	INTSTS0.CTSQ[2:0]
BEMP	缓冲区空中断	• 传输完所有FIFO缓冲区数据后缓冲区为空 • 接收到大于最大数据包大小的数据包	主机或设备	BEMPSTS.PIPEnBEMP
NRDY	缓冲区未就绪中断	在主机控制器模式下● 从外围设备接收到一个STALL响应以响应颁发的令牌 • 外围设备对下发令牌的响应未成功接收（连续3次无响应或连续3次报文接收错误） ●同步传输期间发生溢出或欠载错误在设备控制器模式下● 为IN或OUT令牌返回NAK，而PID[1:0]位设置为01b(BUF) • 同步传输中的数据接收过程中发生CRC错误或位填充错误 • 同步传输的数据接收过程中发生溢出或欠载	主机或设备	NRDYSTS.PIPEnNRDY
BRDY	缓冲区就绪中断	• 缓冲区就绪（可读或可写状态）	主机或设备	BRDYSTS.PIPEnBRDY
OVRCR	过流输入变化中断	• 检测到USB_OVRCURA或USB_OVRCURB输入引脚状态变化（从低到高或从高到低）	Host	INTSTS1.OVRCR
BCHG	总线变化中断	• 检测到USB总线状态更改	主机或设备	SYSSTS0.LNST[1:0]
DTCH	全速运行时断线检测	全速运行时检测到外围设备断开	Host	DVSTCTR0.RHST[2:0]
ATTCH	设备连接检测中断	• 在USB总线上连续检测到J状态或K状态2.5µs 这个中断可以用来检查外围设备是否连接	Host	—

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Table 28.16 Interrupt sources (2 of 2)

Bit to be set to 1	Name	Interrupt source	Applicable controller function	Status flag
EOFERR	EOF error detection interrupt	• An EOF error was detected for a peripheral device	Host	—
SACK	Setup normal interrupt	• A setup transaction normal response (ACK) was received	Host	—
SIGN	Setup error interrupt	• A setup transaction error (no response or ACK packet corruption) was detected three consecutive times	Host	—
PDDETINT	Portable Device detection interrupt	• Portable Device connection was detected	Host	BCCTRL1.PDDETSTS

Note 1. Although this interrupt can be generated in host controller mode, it is not usually used in this mode.

Figure 28.11 shows the circuits related to the USBFS interrupts.

Table 28.16 中断源（2个中的2个）

要设置为1的位	Name	中断源	适用控制器功能	状态标志
EOFERR	EOF错误检测中断	• 检测到外围设备的EOF错误	Host	—
SACK	设置正常中断	• 收到设置事务正常响应(ACK)	Host	—
SIGN	设置错误中断	• 连续3次检测到设置事务错误（无响应或ACK数据包损坏）	Host	—
PDDETINT	便携式设备检测中断	• 检测到便携式设备连接	Host	BCCTRL1.PDDETSTS

注1.虽然该中断可以在主机控制器模式下产生，但通常不用于该模式。

图28.11显示了与USBFS中断相关的电路。

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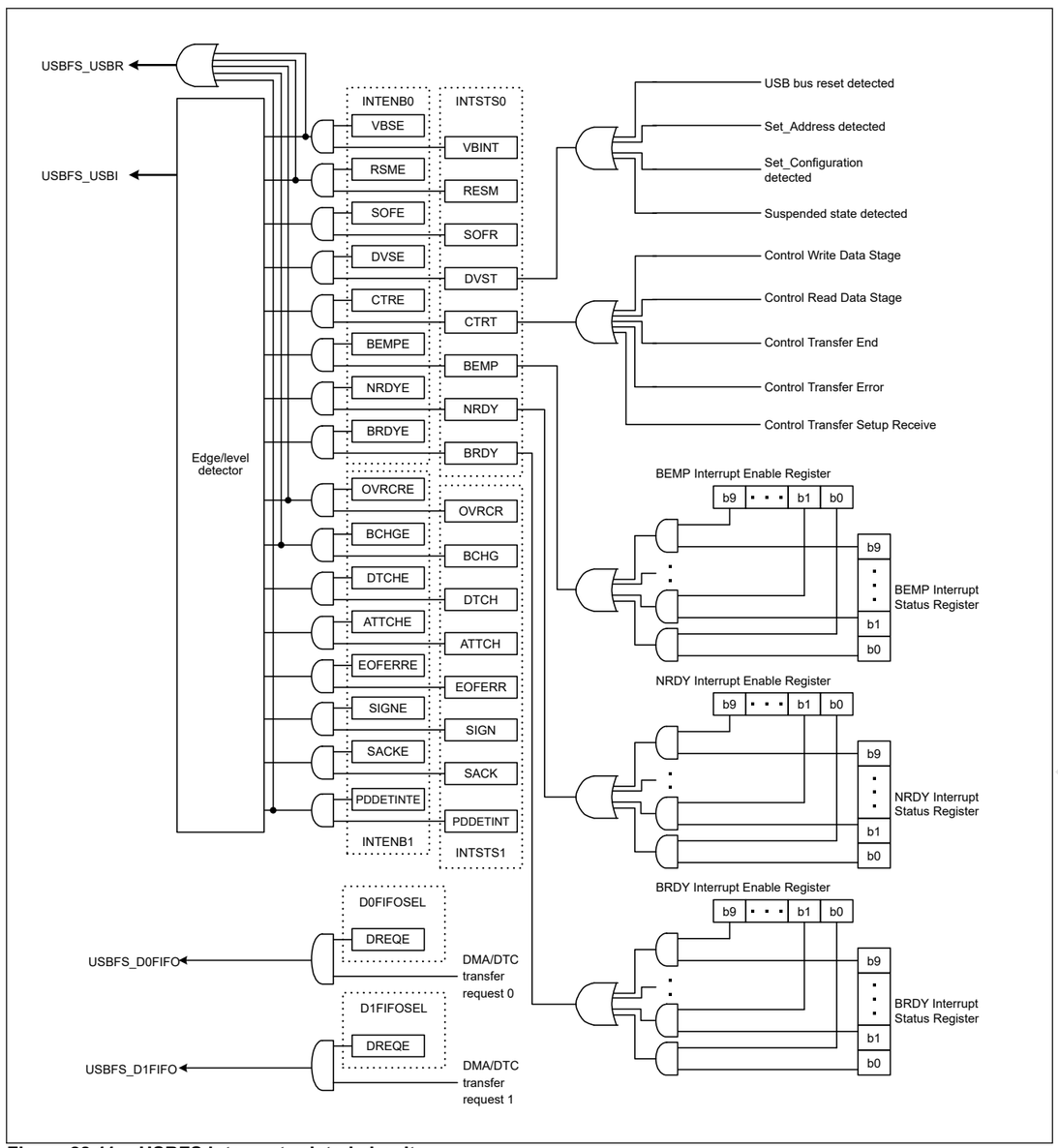

Figure 28.11 USBFS interrupt-related circuits

Table 28.17 shows the interrupts generated by the USBFS.

Table 28.17 USBFS interrupts (1 of 2)

Interrupt name	Interrupt status flag	DTC activation	DMAC activation	Priority
USBFS_D0FIFO	DMA transfer request 0	Possible	Possible	High
USBFS_D1FIFO	DMA transfer request 1	Possible	Possible	

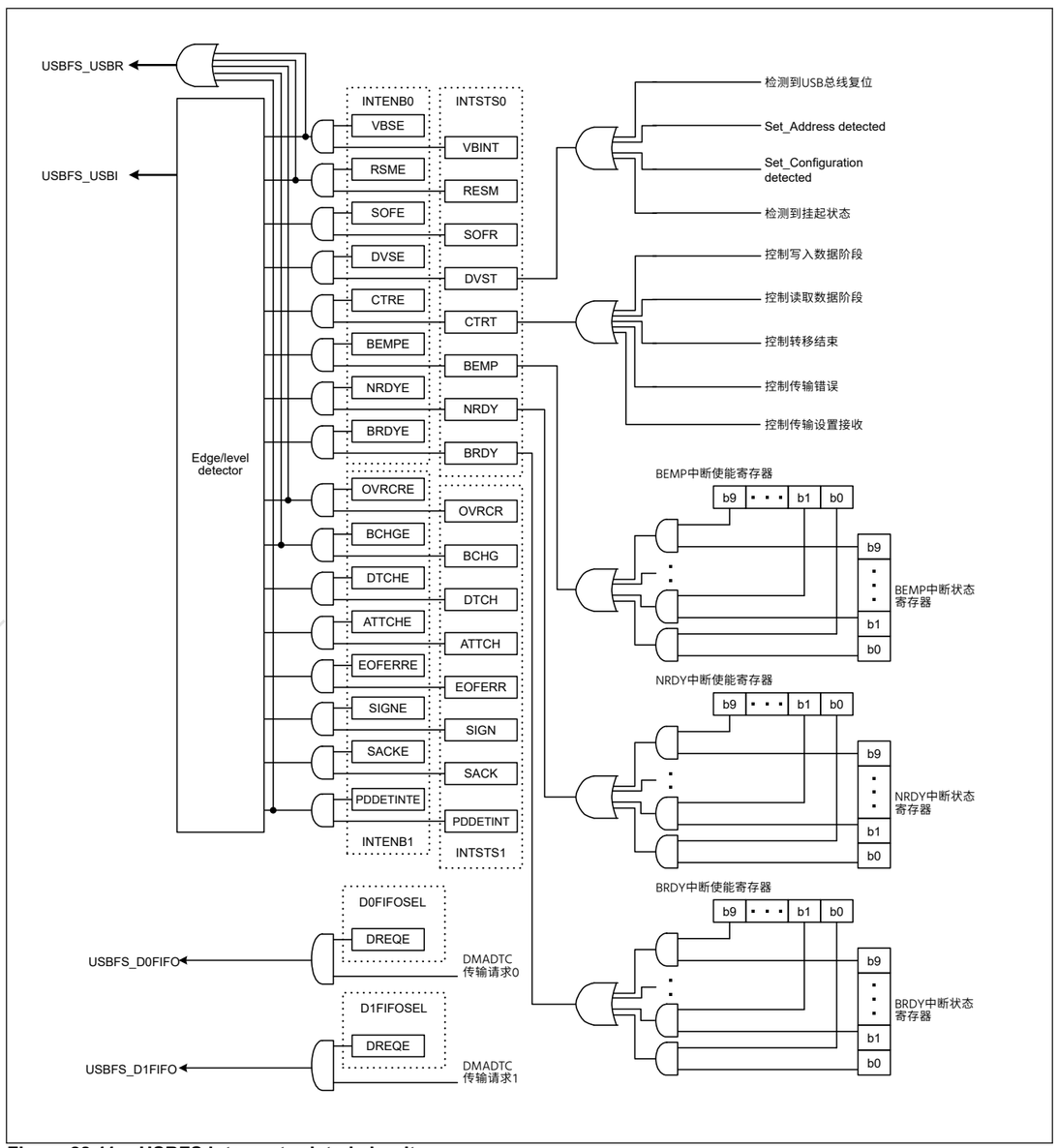

Figure 28.11 USBFS interrupt-related circuits

表28.17显示了USBFS产生的中断。

Table 28.17 USBFS中断(1of2)

中断名称	中断状态标志	DTC activation	DMAC activation	Priority
USBFS_D0FIFO	DMA传输请求0	Possible	Possible	High
USBFS_D1FIFO	DMA传输请求1	Possible	Possible	

Table 28.17 USBFS interrupts (2 of 2)

Interrupt name	Interrupt status flag	DTC activation	DMAC activation	Priority
USBFS_USBI	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent input change interrupt, bus change interrupt, disconnect detection interrupt during full-speed operation, device connect detection interrupt, EOF error detection interrupt, normal setup operation interrupt, setup error interrupt, and Portable Device detection interrupt	Not possible	Not possible	Low
USBFS_USBR	VBUS interrupt, resume interrupt, overcurrent input change interrupt, bus change interrupt, and Portable Device detection interrupt	Not possible	Not possible	—

28.3.3 Interrupt Descriptions

28.3.3.1 BRDY interrupt

The BRDY interrupt is generated in both host and device controller modes. This section describes the conditions in which the USBFS sets the associated bit in BRDYSTS to 1. Under these conditions, the USBFS generates a BRDY interrupt if the software has set the bit in BRDYENB associated with the given pipe to 1 and the INTENB0.BRDYE bit to 1.

The conditions for generating and clearing the BRDY interrupt depend on the SOFCFG.BRDYM and PIPECFG.BFRE settings for each pipe as follows:

(1) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.

On any of the following conditions, the USBFS generates an internal BRDY interrupt request trigger and sets the BRDYSTS.PIPEnBRDY bit associated with the selected pipe to 1.

For transmitting pipes

- When the DIR bit is changed from 0 to 1 by software
- When packet transmission is complete for a pipe while write-access from the CPU to the FIFO buffer for the pipe is disabled (when the BSTS bit is read as 0)
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is complete
- When the hardware flushes the buffer of the pipe for isochronous transfers
- When 1 is written to the PIPEnCTR.ACLRM bit, which causes the FIFO buffer to transition from the write-disabled to write-enabled state

No request trigger is generated for the DCP, that is, during data transmission for control transfers.

For receiving pipes

- When packet reception is successfully complete, enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the given pipe is disabled (when the BSTS bit is read as 0). No request trigger is generated for transactions in which a DATA-PID mismatch has occurred.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode. No request trigger is generated until completion of reading data from the currently-read FIFO buffer, even if reception by the other FIFO buffer is complete.

In device controller mode, the BRDY interrupt is not generated in the status stage of control transfers. The PIPEBRDY interrupt status of the selected pipe can be set to 0 by writing 0 to the associated PIPEnBRDY bit through software. In this case, the other PIPEBRDY bit should be set to 1.

Clear the BRDY status before accessing the FIFO buffer.

Table 28.17 USBFS中断（2个中的2个）

中断名称	中断状态标志	DTC activation	DMAC activation	Priority
USBFS_USBI	VBUS中断、恢复中断、帧号更新中断、设备状态转换中断、控制传输阶段转换中断、缓冲区空中断、缓冲区未就绪中断、缓冲区就绪中断、过流输入改变中断、总线改变中断、满时断开检测中断速度操作、设备连接检测中断、EOF错误检测中断、正常设置操作中断、设置错误中断和便携式设备检测中断	不可能	不可能	Low
USBFS_USBR	VBUS中断、恢复中断、过流输入变化中断、总线变化中断和便携式设备检测中断	不可能	不可能	—

28.3.3 中断说明

28.3.3.1 BRDY interrupt

在主机和设备控制器模式下都会产生BRDY中断。本节描述USBFS将BRDYSTS中的相关位设置为1的条件。在这些条件下，如果软件将BRDYENB中与给定管道相关的位设置为1并且INTENB0.BRDYE位，USBFS将生成BRDY中断为1。

产生和清除BRDY中断的条件取决于每个管道的SOFCFG.BRDYM和PIPECFG.BFRE设置，如下所示：

(1) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=0时

通过这些设置，BRDY中断指示FIFO端口可访问。

在以下任何一种情况下，USBFS都会产生一个内部BRDY中断请求触发器并设置BRDYSTS.PIPEnBRDY位与所选管道相关联为1。

用于传输管道

●DIR位由软件从0变为1时

●当一个管道的数据包传输完成而从CPU到该管道的FIFO缓冲区的写访问被禁用时（当BSTS位被读取为0时）

●双缓冲模式下，当一个FIFO缓冲区完成向另一个FIFO缓冲区写入数据时为空时

●直到向当前写入的FIFO缓冲区写入数据完成，才会产生请求触发，即使传输到另一个FIFO缓冲区已完成

●当硬件刷新管道缓冲区以进行同步传输时

●当PIPEnCTR.ACLRM位写入1时，导致FIFO缓冲区从写禁止状态转变为写使能状态

没有为DCP生成请求触发，即在控制传输的数据传输期间。

用于接收管道

●当数据包接收成功完成时，允许读取FIFO缓冲区，同时禁止CPU对给定管道的FIFO缓冲区的读取访问（当BSTS位被读取为0时）。对于发生DATA-PID不匹配的事务，不会生成请求触发器。

●当一个FIFO缓冲区在双缓冲区模式下从另一个FIFO缓冲区读取数据完成后使能读取。在从当前读取的FIFO缓冲区读取数据完成之前，不会生成请求触发，即使其他FIFO缓冲区的接收已完成。

在设备控制器模式下，在控制传输的状态阶段不会产生BRDY中断。通过软件将0写入相关的PIPEnBRDY位，可以将所选管道的PIPEBRDY中断状态设置为0。在这种情况下，另一个PIPEBRDY位应设置为1。

在访问FIFO缓冲区之前清除BRDY状态。

(2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1

With these settings, the USBFS generates a BRDY interrupt on completion of reading all data for a single transfer using the receiving pipe, and sets the bit in BRDYSTS associated with the pipe to 1.

On any of the following conditions, the USBFS determines that the last data for a single transfer was received.

- When a short packet including a zero-length packet is received
- When the PIPEn transaction counter register (PIPEnTRN) is used and the number of packets specified in the PIPEnTRN.TRNCNT[15:0] bits are completely received

When the data is completely read after any of these conditions is satisfied, the USBFS determines that all data for a single transfer is completely read.

When a zero-length packet is received while the FIFO buffer is empty, the USBFS determines that all data for a single transfer is completely read when the FRDY bit in the FIFO port control register is 1 and the DTLN[8:0] bits are 0. In this case, to start the next transfer, write 1 to the BCLR bit in the associated port control register through the software. With these settings, the USBFS does not detect a BRDY interrupt for the transmitting pipe.

The PIPEBRDY interrupt status of a pipe can be set to 0 by writing 0 to the associated BRDYSTS.PIPEnBRDY bit through the software. In this case, 1s must be written to the PIPEBRDY bits for the other pipes.

In this mode, do not change the PIPECFG.BFRE bit setting until all data for a single transfer is processed. When it is necessary to change the PIPECFG.BFRE bit before completion of processing, all FIFO buffers for the pipe must be cleared using the PIPEnCTR.ACLRM bit.

(3) When SOFCFG.BRDYM = 1 and PIPECFG.BFRE = 0

With these settings, the BRDYSTS.PIPEnBRDY values are linked to the BSTS bit setting for each pipe. In other words, the BRDY interrupt status bits (PIPEBRDY) are set to 1 or 0 by the USB depending on the FIFO buffer status.

For transmitting pipes

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for write access, and are set to 0 when it is not ready. The BRDY interrupt is not generated for the DCP in the transmitting direction even when it is ready for write access.

For receiving pipes

The BRDY interrupt status bits set to 1 when the FIFO buffer is ready for read access, and set to 0 when all data is read (not ready for read access).

When a zero-length packet is received while the FIFO buffer is empty, the associated bit is set to 1 and the BRDY interrupt is continuously generated until the software writes 1 to BCLR. With this setting, the PIPEnBRDY bit cannot be set to 0 by software.

When the SOFCFG.BRDYM bit is set to 1, set the PIPECFG.BFRE bit for all pipes to 0.

Figure 28.12 shows the timing of BRDY interrupt generation.

(2) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=1时

使用这些设置，USBFS在完成使用接收管道读取单次传输的所有数据时生成BRDY中断，并将BRDYSTS中与管道关联的位设置为1。

在以下任何一种情况下，USBFS都会确定已接收到单次传输的最后一个数据。

●收到包含零长度包的短包时

●当使用PIPEn事务计数器寄存器(PIPEnTRN)并且完全接收到PIPEnTRN.TRNCNT[15:0]位中指定的数据包数量时

当满足其中任何一个条件后数据被完全读取时，USBFS确定单次传输的所有数据都被完全读取。

当FIFO缓冲区为空时接收到零长度数据包时，当FIFO端口控制寄存器中的FRDY位为1且DTLN[8:0]位为0.在这种情况下，要开始下一次传输，通过软件向相关端口控制寄存器中的BCLR位写入1。使用这些设置，USBFS不会检测到传输管道的BRDY中断。

通过软件将0写入相关的BRDYSTS.PIPEnBRDY位，可以将管道的PIPEBRDY中断状态设置为0。在这种情况下，必须将1写入其他管道的PIPEBRDY位。

在此模式下，在处理完单次传输的所有数据之前，不要更改PIPECFG.BFRE位设置。当需要在处理完成之前更改PIPECFG.BFRE位时，必须使用PIPEnCTR.ACLRM位清除管道的所有FIFO缓冲区。

(3) 当SOFCFG.BRDYM=1且PIPECFG.BFRE=0时

通过这些设置，BRDYSTS.PIPEnBRDY值链接到每个管道的BSTS位设置。换句话说，BRDY中断状态位(PIPEBRDY)由USB设置为1或0，具体取决于FIFO缓冲区状态。

用于传输管道

当FIFO缓冲区准备好进行写访问时，BRDY中断状态位设置为1，当它未准备好时设置为0。发送方向上的DCP不会产生BRDY中断，即使它已准备好进行写访问。

用于接收管道

当FIFO缓冲区准备好进行读取访问时，BRDY中断状态位设置为1，并在读取所有数据（未准备好进行读取访问）时设置为0。

当FIFO缓冲区为空时接收到零长度数据包时，相关位设置为1，并且持续产生BRDY中断，直到软件将1写入BCLR。使用此设置，PIPEnBRDY位不能通过软件设置为0。

当SOFCFG.BRDYM位设置为1时，将所有管道的PIPECFG.BFRE位设置为0。

图28.12显示了BRDY中断产生的时序。

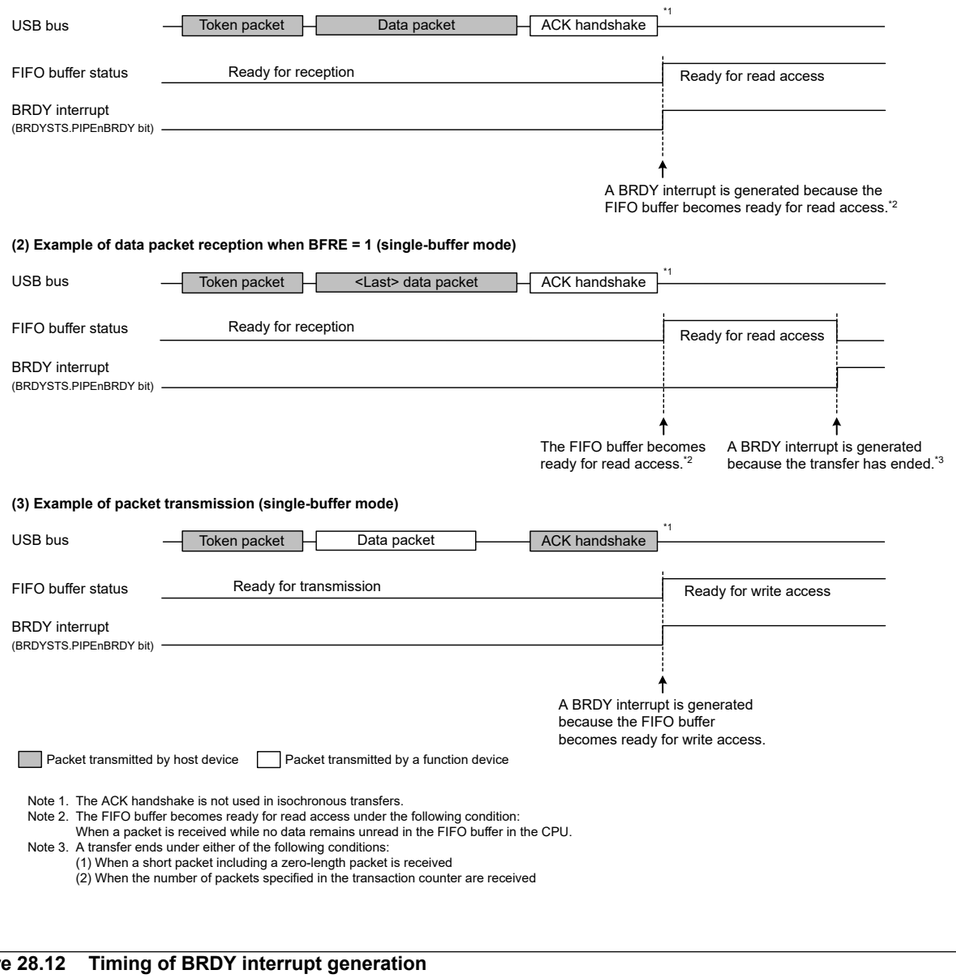

Figure 28.12 Timing of BRDY interrupt generation

The condition for clearing the INTSTS0.BRDY bit depends on the SOFCFG.BRDYM bit setting, as shown in Table 28.18.

Table 28.18 Conditions for clearing the BRDY bit

BRDYM bit	Condition for clearing BRDY bit
0	The USBFS clears the BRDY bit to 0 when all bits in BRDYSTS are set to 0 by software.
1	The USBFS clears the BRDY bit to 0 when the BSTS bits for all pipes have cleared to 0.

28.3.3.2 NRDY interrupt

On generating an internal NRDY interrupt request for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated PIPEnNRDY bit in NRDYSTS to 1. If the associated bit in NRDYENB is set to 1 by software, the USBFS sets the INTSTS0.NRDY bit to 1 and generates a USBFS interrupt.

This section describes the conditions in which the USBFS generates the internal NRDY interrupt request for a given pipe.

The internal NRDY interrupt request is not generated during setup transaction execution in host controller mode. During setup transactions in host controller mode, the SACK or SIGN interrupt is detected.

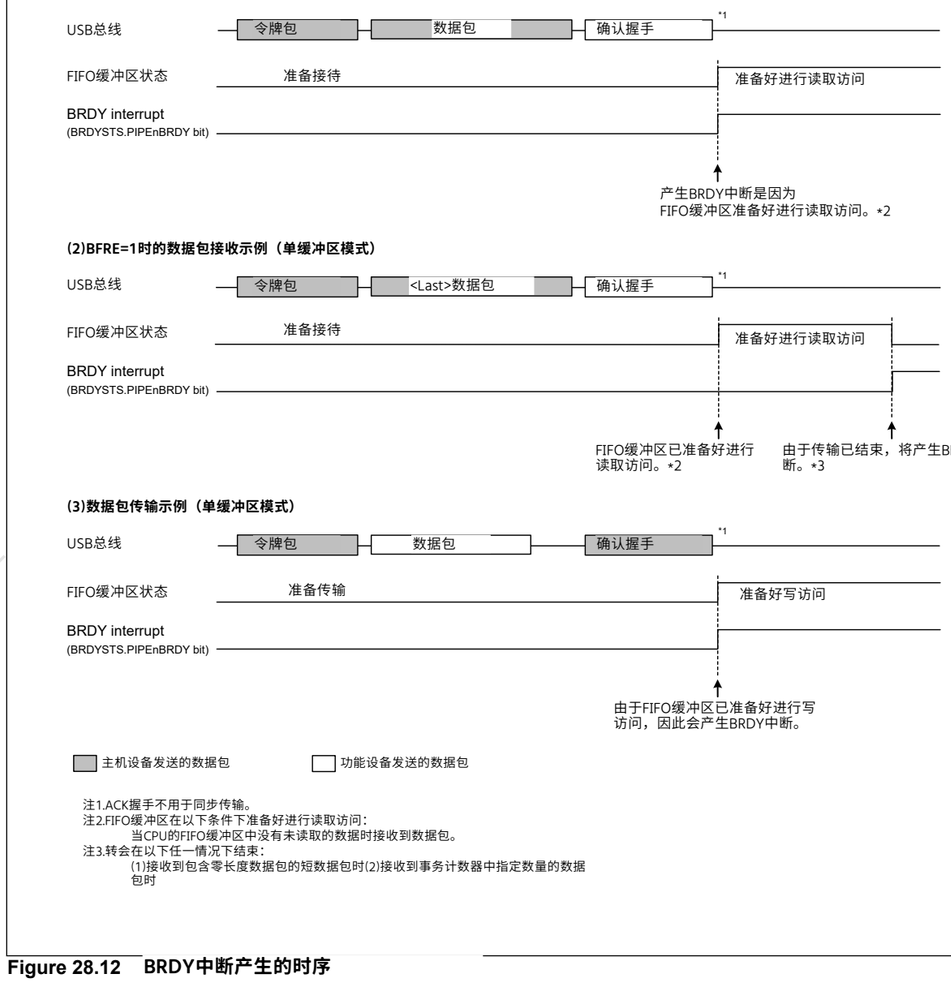

Figure 28.12 BRDY中断产生的时序

清除INTSTS0.BRDY位的条件取决于SOFCFG.BRDYM位设置，如表28.18所示。

Table 28.18 清除BRDY位的条件

BRDYM bit	清除BRDY位的条件
0	当BRDYSTS中的所有位被软件设置为0时，USBFS将BRDY位清零。
1	当所有管道的BSTS位已清零时，USBFS将BRDY位清零。

28.3.3.2 NRDY interrupt

在为PID位由软件设置为BUF的管道生成内部NRDY中断请求时，USBFS将NRDYSTS中的相关PIPEnNRDY位设置为1。如果NRDYENB中的相关位由软件设置为1，则USBFS设置INTSTS0.NRDY位为1并产生USBFS中断。

本节描述USBFS为给定管道生成内部NRDY中断请求的条件。

内部NRDY中断请求在主控制器模式下的设置事务执行期间不会产生。在主机控制器模式下的设置事务期间，检测到SACK或SIGN中断。

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The internal NRDY interrupt request is not generated during status stage execution of the control transfer in device controller mode.

(1) In host controller mode

For transmitting pipes

On any of the following conditions, the USBFS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBFS transmits a zero-length packet following the OUT token and sets the associated NRDYSTS.PIPEnNRDY bit and the FRMNUM.OVRN bit to 1.
- During communications other than setup transactions on pipes not used for isochronous transfers, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device
  - An error is detected in the packet from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the associated PID[1:0] setting for the pipe to NAK
- During communications other than setup transactions, when the STALL handshake is received from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the PID[1:0] setting for the associated pipe to STALL (11b).

For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBFS discards the received data for the IN token and sets the PIPEnNRDY bit associated with the pipe and the OVRN bit to 1. When a packet error is detected in the received data for the IN token, the USBFS also sets the FRMNUM.CRCE bit to 1.
- For non-isochronous transfer pipes, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device for the IN token issued by the USBFS (when timeout is detected before detection of the DATA packet from the peripheral device)
  - An error is detected in the packet from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the associated PID[1:0] setting for the pipe to NAK
- For isochronous transfer pipes, when no response is returned from the peripheral device for the IN token (when timeout is detected before detection of the DATA packet from the peripheral device) or an error is detected in the packet from the peripheral device. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe to 1. The PID[1:0] setting for the pipe is not changed.
- For isochronous transfer pipes, when a CRC error or a bit stuffing error is detected in the received data packet. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe and the CRCE bit to 1.
- When the STALL handshake is received. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe to 1 and changes the PID[1:0] setting for the associated pipe to STALL.

(2) In device controller mode

For transmitting pipes

- When an IN token is received while there is no data to be transmitted in the FIFO buffer. In this case, the USBFS generates a NRDY interrupt request on reception of the IN token and sets the NRDYSTS.PIPEnNRDY bit to 1. For an isochronous transfer pipe in which an interrupt is generated, the USBFS transmits a zero-length packet and sets the FRMNUM.OVRN bit to 1.

For receiving pipes

- When an OUT token is received but there is no space available in the FIFO buffer. For an isochronous transfer pipe in which an interrupt is generated, the USBFS generates a NRDY interrupt request on reception of the OUT token and sets the PIPEnNRDY bit to 1 and OVRN bit to 1. For a non-isochronous transfer pipe in which an interrupt is generated, the USBFS generates a NRDY interrupt request when a NAK handshake is transferred after the data following the OUT token is received, and sets the PIPEnNRDY bit to 1. The NRDY interrupt request is not generated during retransmission

在设备控制器模式下控制传输的状态阶段执行期间，不会产生内部NRDY中断请求。

(1) 在主机控制器模式下

用于传输管道

在以下任何一种情况下，USBFS都会检测到NRDY中断：

●对于同步传输管道，当FIFO缓冲区中没有要传输的数据时发出OUT令牌的时间到来。在这种情况下，USBFS在OUT令牌之后发送一个长度为零的数据包，并将相关的NRDYSTS.PIPEnNRDY位和FRMNUM.OVRN位设置为1。

●在不用于同步传输的管道上的设置事务以外的通信期间，当以下两种情况的任意组合连续发生3次时：

外围设备没有返回响应（当在检测到来自外围设备的握手包之前检测到超时

在来自外围设备的数据包中检测到错误。在这种情况下，USBFS将相关的PIPEnNRDY位设置为1，并将管道的相关PID[1:0]设置更改为NAK

●在设置事务以外的通信期间，当从外围设备接收到STALL握手时。在这种情况下，USBFS将相关的PIPEnNRDY位设置为1，并将相关管道的PID[1:0]设置更改为STALL(11b)。

用于接收管道

●对于同步传输管道，当发出IN令牌的时间到来但FIFO中没有可用空间时
缓冲。在这种情况下，USBFS丢弃接收到的IN令牌数据，并将与管道关联的PIPEnNRDY位和OVRN位设置为1。当在接收到的IN令牌数据中检测到数据包错误时，USBFS也会设置FRMNUM.CRCE位为1。

●对于非等时传输管道，当以下两种情况的任意组合连续出现3次时：

USBFS发出的IN令牌没有从外围设备返回响应（当在检测到来自外围设备的DATA数据包之前检测到超时时）

在来自外围设备的数据包中检测到错误。在这种情况下，USBFS将相关的PIPEnNRDY位设置为1，并将管道的相关PID[1:0]设置更改为NAK

●对于同步传输管道，当外围设备没有返回对IN令牌的响应时（在检测到来自外围设备的DATA数据包之前检测到超时）或在外围设备的数据包中检测到错误。在这种情况下，USBFS将与管道关联的PIPEnNRDY位设置为1。管道的PID[1:0]设置不会更改。

●对于同步传输管道，当在接收到的数据包中检测到CRC错误或比特填充错误时。在这种情况下，USBFS将与管道关联的PIPEnNRDY位和CRCE位设置为1。

●收到STALL握手时。在这种情况下，USBFS将与管道关联的PIPEnNRDY位设置为1，并将关联管道的PID[1:0]设置更改为STALL。

(2) 在设备控制器模式下

用于传输管道

●当接收到一个IN令牌而FIFO缓冲区中没有要传输的数据时。在这种情况下，USBFS
在接收到IN令牌时生成NRDY中断请求并将NRDYSTS.PIPEnNRDY位设置为1。对于产生中断的同步传输管道，USBFS发送一个长度为零的数据包并将FRMNUM.OVRN位设置为1.

用于接收管道

●当接收到OUT令牌但FIFO缓冲区中没有可用空间时。对于产生中断的同步传输管道，USBFS在接收到OUT令牌时产生一个NRDY中断请求，并将PIPEnNRDY位设置为1，并将OVRN位设置为1。USBFS在接收到OUT令牌之后的数据后，在传输NAK握手时产生NRDY中断请求，并将PIPEnNRDY位设置为1。重传期间不产生NRDY中断请求

because of a DATA-PID mismatch. In addition, the NRDY interrupt request is not generated if an error occurs in the DATA packet.

- For isochronous transfer pipes, when a token is not received successfully within an interval frame. In this case, the USBFS generates an NRDY interrupt request when the SOF is received, and sets the PIPEnNRDY bit to 1.

Figure 28.13 shows the timing of NRDY interrupt generation in device controller mode.

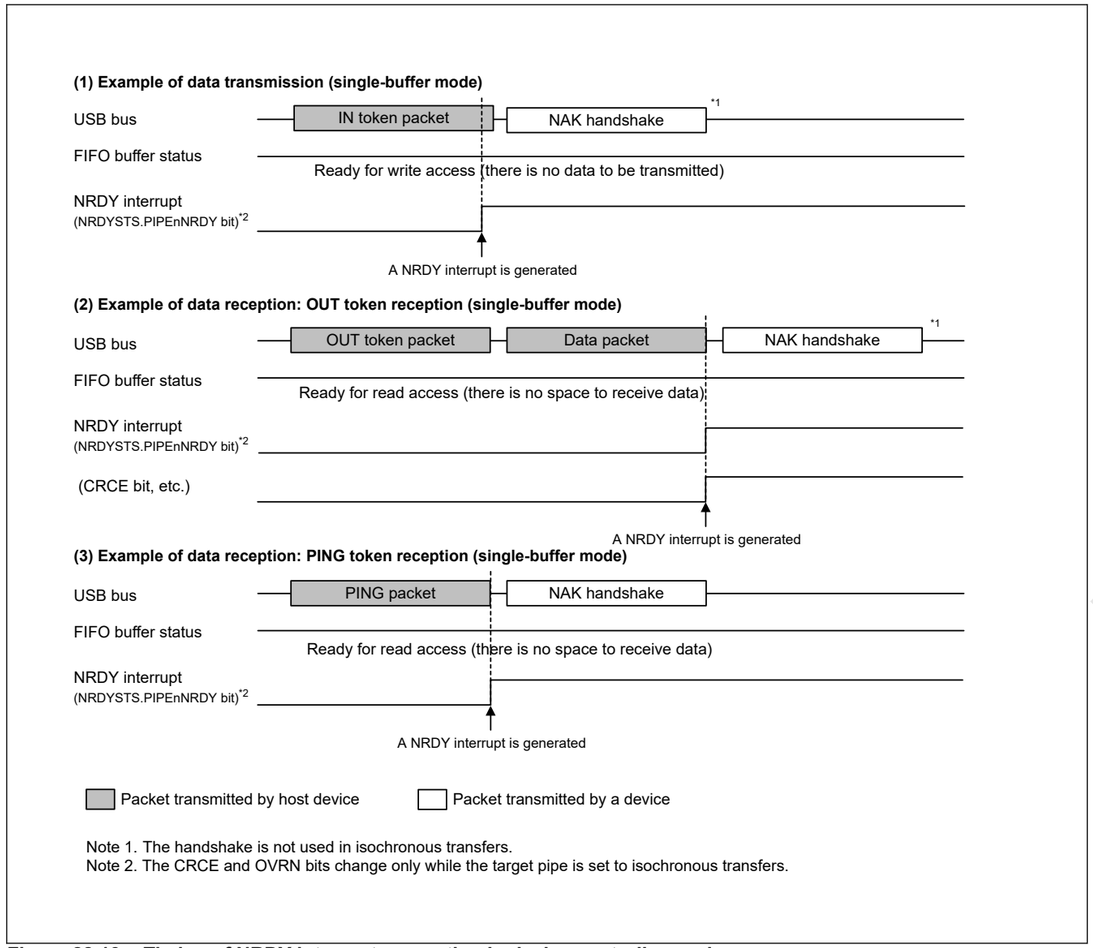

Figure 28.13 Timing of NRDY interrupt generation in device controller mode

28.3.3.3 BEMP interrupt

On detecting a BEMP interrupt for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated BEMPSTS.PIPEnBEMP bit to 1. If the associated bit in BEMPENB is set to 1 by software, the USBFS sets the INTSTS0.BEMP bit to 1 and generates a USBFS interrupt. This section describes the conditions in which the USBFS generates an internal BEMP interrupt request.

(1) For transmitting pipes

When the FIFO buffer of the associated pipe is empty on completion of transmission, including zero-length packet transmission, and in single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for a non-DCP pipe. The internal BEMP interrupt request is not generated in any of the following conditions:

因为DATA-PID不匹配。此外，如果DATA包发生错误，则不会产生NRDY中断请求。

●对于同步传输管道，当在间隔帧内没有成功接收到令牌时。在这种情况下，USBFS在接收到SOF时产生一个NRDY中断请求，并将PIPEnNRDY位设置为1。

图28.13显示了设备控制器模式下NRDY中断产生的时序。

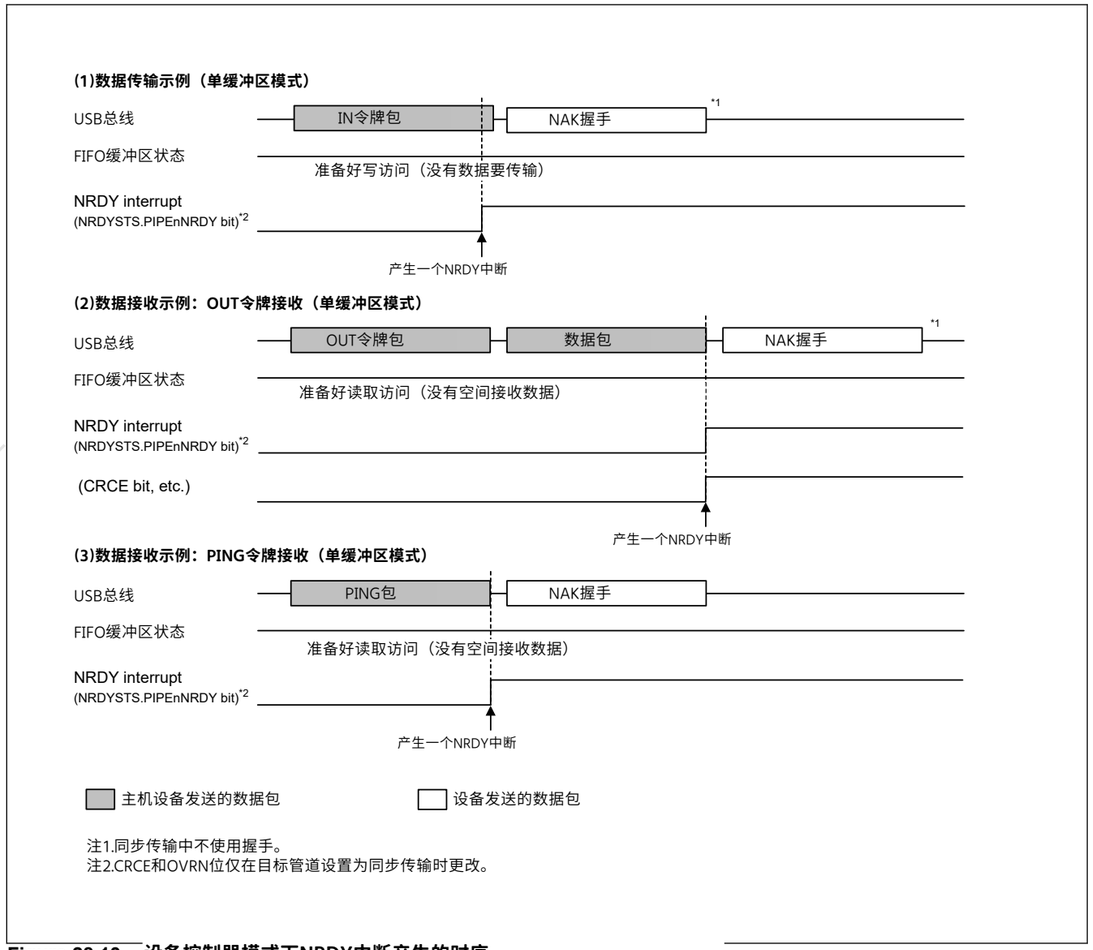

Figure 28.13 设备控制器模式下NRDY中断产生的时序

28.3.3.3 BEMP interrupt

在检测到PID位被软件设置为BUF的管道的BEMP中断时，USBFS将相关的BEMPSTS.PIPEnBEMP位设置为1。如果BEMPENB中的相关位被软件设置为1，USBFS将设置INTSTS0.BEMP位为1并产生USBFS中断。本节介绍USBFS产生内部BEMP中断请求的条件。

(1) 用于传输管道

当相关管道的FIFO缓冲区在传输完成时为空时，包括零长度数据包传输，并且在单缓冲区模式下，内部BEMP中断请求与非DCP管道的BRDY中断同时生成。在以下任何一种情况下都不会产生内部BEMP中断请求：

- When the CPU or DMA/DTC has already started writing data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode
- When the buffer is cleared (emptied) by setting the PIPEnCTR.ACLRM or the BCLR bit to 1 in the port control register
- When an IN transfer (zero-length packet transmission) is performed during the control transfer status stage in device controller mode

(2) For receiving pipes

When a successfully-received data packet size exceeds the specified maximum packet size. In this case, the USBFS generates a BEMP interrupt request, sets the associated BEMPSTS.PIPEnBEMP bit to 1, discards the received data, and changes the associated PID[1:0] setting for the pipe to STALL (11b). The USBFS returns no response in host controller mode, and returns STALL response in device controller mode.

The internal BEMP interrupt request is not generated in any of the following conditions:

- When a CRC error or a bit stuffing error is detected in the received data
- When a setup transaction is being performed:
  - Writing 0 to the BEMPSTS.PIPEnBEMP bit clears the status
  - Writing 1 to the BEMPSTS.PIPEnBEMP bit has no effect

Figure 28.14 shows the timing of BEMP interrupt generation in device controller mode.

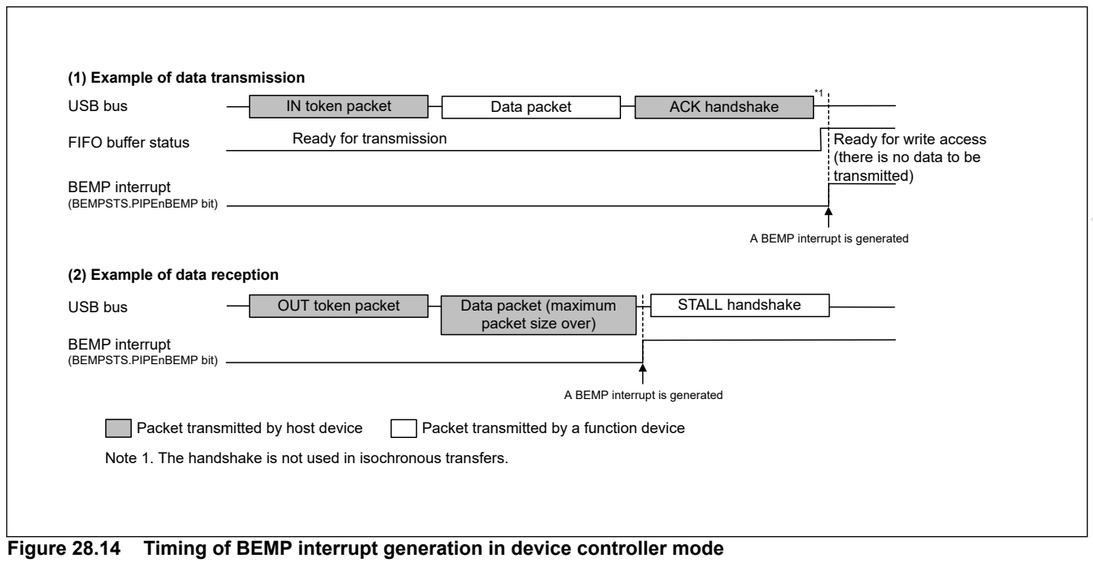

Figure 28.14 Timing of BEMP interrupt generation in device controller mode

28.3.3.4 Device state transition interrupt (device controller mode)

Figure 28.15 shows a diagram of the USBFS device state transitions. The USBFS controls device states and generates device state transition interrupts. However, recovery from the Suspend state (resume signal detection) is detected by means of the resume interrupt. Device state transition interrupts can be enabled or disabled independently in INTENB0. Devices whose states have changed can be checked in the INTSTS0.DVSQ[2:0] bits.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is detected.

The USBFS controls device states, and device state transition interrupts can be generated, only in device controller mode.

●当CPU或DMADTC在双缓冲模式下从一个FIFO缓冲区完成数据传输后已经开始向CPU的FIFO缓冲区写入数据时

●通过将端口控制寄存器中的PIPEnCTR.ACLRM或BCLR位设置为1来清除（清空）缓冲区时

●在设备控制器模式的控制传输状态阶段进行IN传输（零长度包传输）时

(2) 用于接收管道

当成功接收的数据包大小超过指定的最大包大小时。在这种情况下，USBFS生成一个BEMP中断请求，将相关的BEMPSTS.PIPEnBEMP位设置为1，丢弃接收到的数据，并将管道的相关PID[1:0]设置更改为STALL(11b)。USBFS在主机控制器模式下不返回响应，在设备控制器模式下返回STALL响应。

在以下任何一种情况下都不会产生内部BEMP中断请求：

●在接收到的数据中检测到CRC错误或位填充错误时

●执行设置事务时：

将0写入BEMPSTS.PIPEnBEMP位可清除状态

向BEMPSTS.PIPEnBEMP位写入1无效

图28.14显示了设备控制器模式下BEMP中断产生的时序。

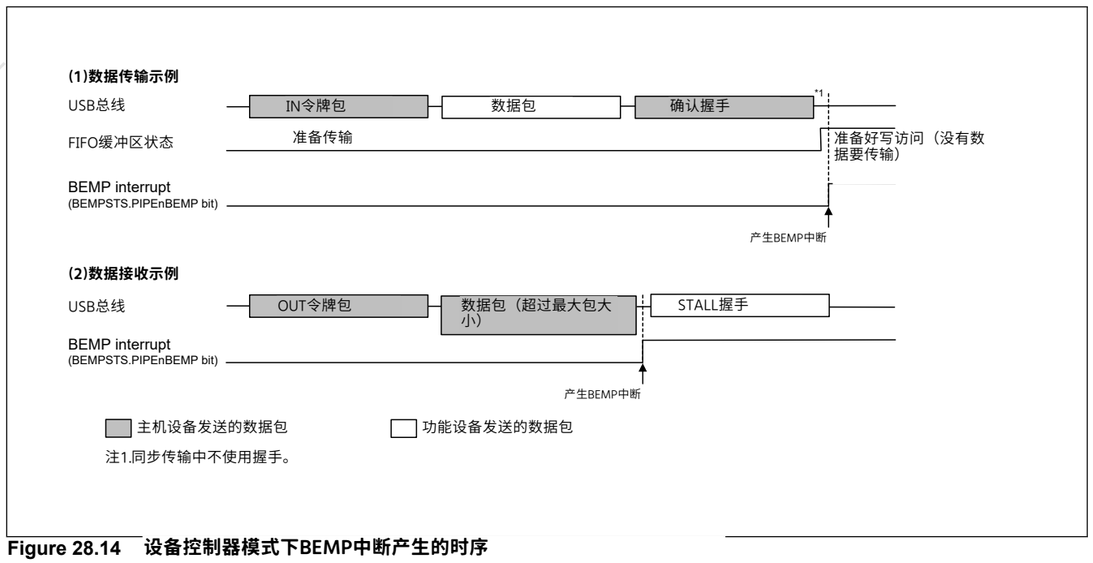

Figure 28.14 设备控制器模式下BEMP中断产生的时序

28.3.3.4 设备状态转换中断（设备控制器模式）

图28.15显示了USBFS设备状态转换的示意图。USBFS控制设备状态并产生设备状态转换中断。但是，从挂起状态的恢复（恢复信号检测）是通过恢复中断来检测的。可以在INTENB0中独立启用或禁用设备状态转换中断。可以在INTSTS0.DVSQ[2:0]位中检查状态已更改的设备。

当转换到默认状态时，检测到USB总线复位后会产生设备状态转换中断。

USBFS控制设备状态，并且只能在设备控制器模式下产生设备状态转换中断。

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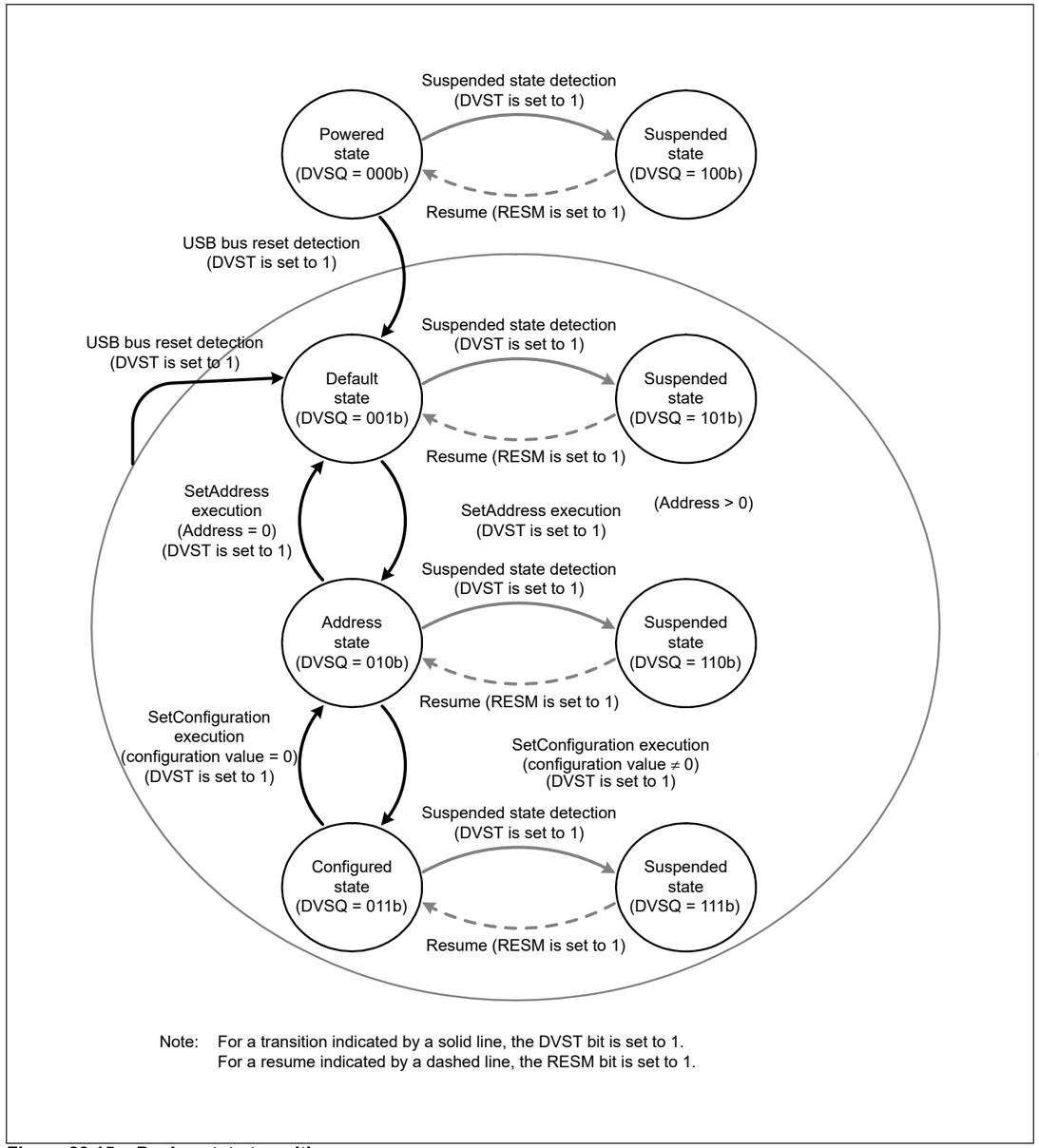


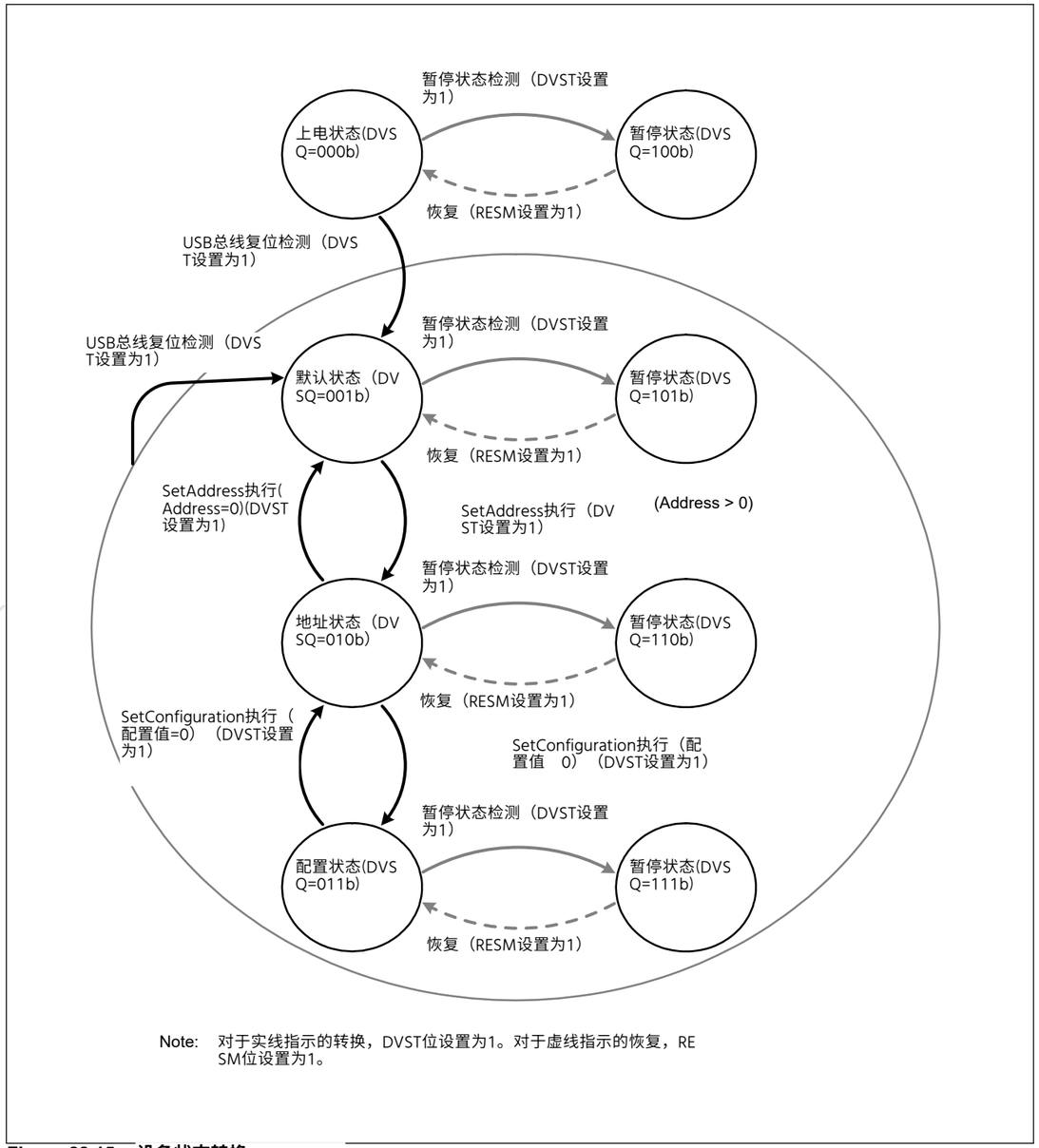
Note: For a transition indicated by a solid line, the DVST bit is set to 1.
For a resume indicated by a dashed line, the RESM bit is set to 1.

Figure 28.15 Device state transitions

28.3.3.5 Control transfer stage transition interrupt (device controller mode)

Figure 28.16 shows a diagram of the control transfer stage transitions of the USBFS. The USBFS controls the control transfer sequence and generates control transfer stage transition interrupts. Control transfer stage transition interrupts can be enabled or disabled independently in INTENB0. Transfer stages that have transitioned can be checked in the INTSTS0.CTSQ[2:0] bits.

Control transfer stage transition interrupts are generated only in device controller mode. This section describes control transfer sequence errors. If an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).



Note: 对于实线指示的转换，DVST位设置为1。对于虚线指示的恢复，RESM位设置为1。

Figure 28.15 设备状态转换

28.3.3.5 控制转移阶段转换中断（设备控制器模式）

图28.16显示了USBFS的控制传输阶段转换图。USBFS控制控制传输序列并产生控制传输阶段转换中断。控制转移阶段转换中断可以在INTENB0中独立启用或禁用。可以在INTSTS0.CTSQ[2:0]位中检查已转换的传输阶段。

控制转移阶段转换中断仅在设备控制器模式下产生。本节描述控制传输序列错误。如果发生错误，则DCPCTR.PID[1:0]位设置为1xb（STALL响应）。

(1) Control read transfer errors

- An OUT token is received but no data is transferred in response to the IN token at the data stage
- An IN token is received at the status stage
- A data packet with DATAPID = DATA0 is received at the status stage

(2) Control write transfer errors

- An IN token is received but no ACK is returned in response to the OUT token at the data stage
- A data packet with DATAPID = DATA0 is received as the first data packet at the data stage
- An OUT token is received at the status stage

(3) Control write no data transfer errors

- An OUT token is received at the status stage

At the control write transfer data stage, if the receive data length exceeds the wLength value of the USB request, it is not recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT = 1), the CTSQ[2:0] = 110b value is saved until the CTRT bit is set to 0, clearing the interrupt status. While CTSQ[2:0] = 110b is being saved, no CTRT interrupt for ending the setup stage is generated, even if a new USB request is received. The USBFS saves the setup stage completion status, and it generates a CTRT interrupt after the interrupt status is cleared by software.

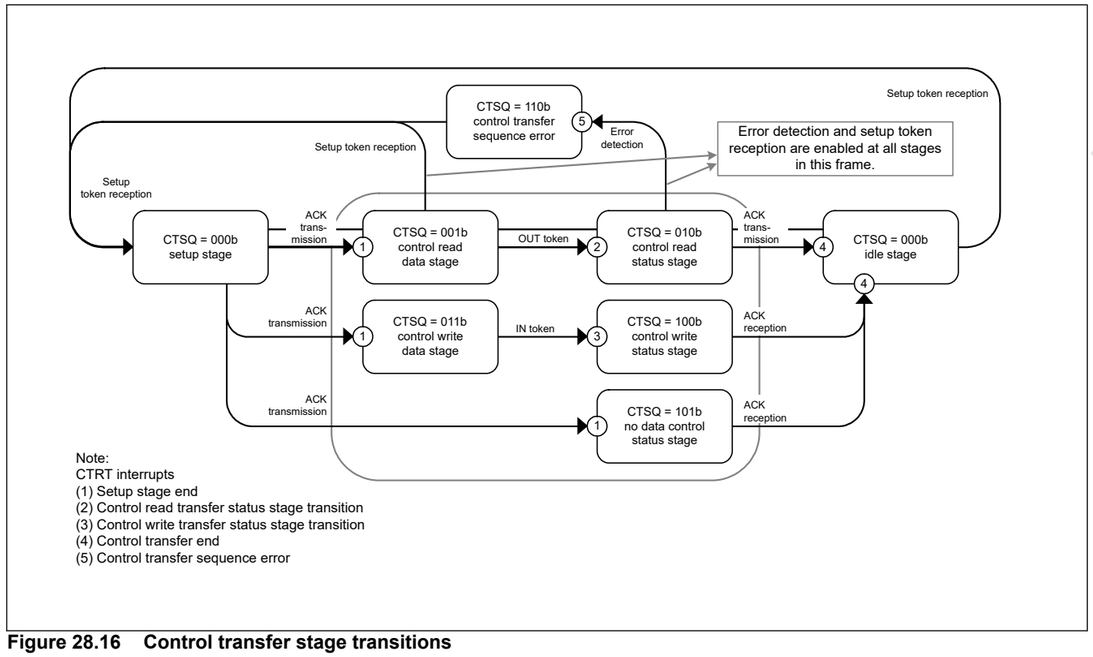


Figure 28.16 Control transfer stage transitions

28.3.3.6 Frame update interrupt

In host controller mode, an interrupt is generated when the frame number is updated.

In device controller mode, an SOFR interrupt is generated when the frame number is updated. The USBFS updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

(1) 控制读取传输错误

●在数据阶段收到一个OUT令牌，但没有传输数据以响应IN令牌

●在状态阶段收到一个IN令牌

●在状态阶段接收到DATAPID=DATA0的数据包

(2) 控制写入传输错误

●在数据阶段收到一个IN令牌，但没有返回ACK响应OUT令牌

●DATAPID=DATA0的数据包作为数据阶段的第一个数据包被接收

●在状态阶段收到一个OUT令牌

(3) 控制写入无数据传输错误

●在状态阶段收到一个OUT令牌

在控制写入传输数据阶段，如果接收数据长度超过USB请求的wLength值，则不被识别为控制传输序列错误。
在控制读取传输状态阶段，除了零长度数据包之外的数据包被一个ACK响应接收并且传输正常结束。

当响应序列错误（INTSTS0.CTRT=1）而发生CTRT中断时，将保存CTSQ[2:0]=110b值，直到CTRT位设置为0，清除中断状态。在保存CTSQ[2:0]=110b时，不会产生用于结束设置阶段的CTRT中断，即使收到新的USB请求也是如此。USBFS保存设置阶段完成状态，软件清除中断状态后产生CTRT中断。

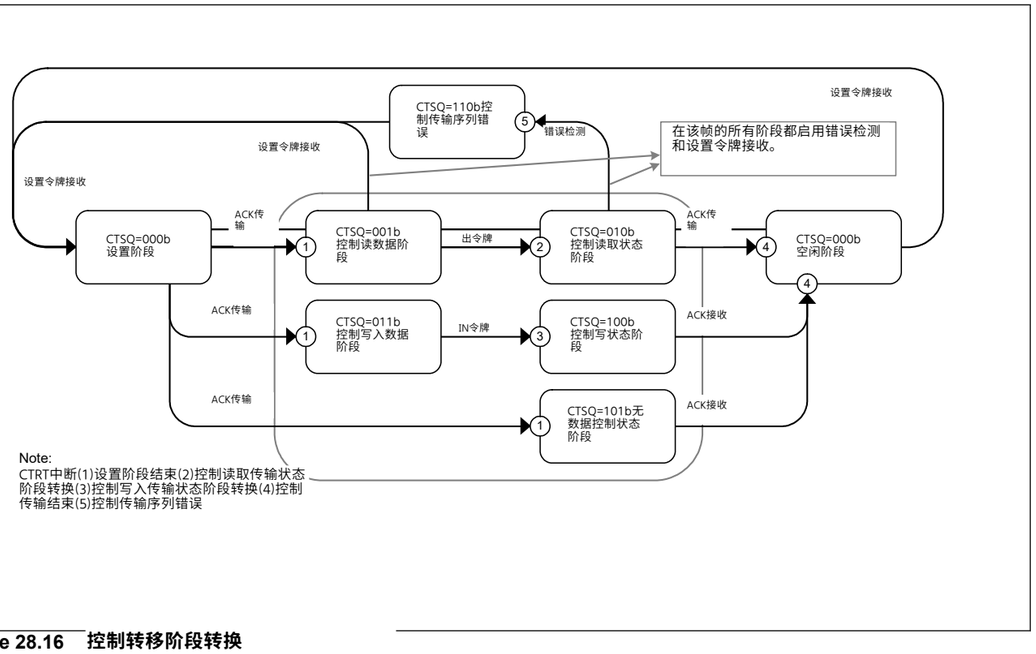


Figure 28.16 控制转移阶段转换

28.3.3.6 帧更新中断

在主机控制器模式下，更新帧号时会产生中断。

在设备控制器模式下，更新帧号时会产生SOFR中断。如果USBFS在全速运行期间检测到新的SOF数据包，则USBFS会更新帧号并生成SOFR中断。

28.3.3.7 VBUS interrupt

When the USB_VBUS pin level changes, a VBUS interrupt is generated. The level of the USB_VBUS pin can be checked with the INTSTS0.VBSTS bit. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. If the system is activated with the host controller connected, the first VBUS interrupt is not generated, because there is no change in the USB_VBUS pin level.

28.3.3.8 Resume interrupt

In device controller mode, a resume interrupt is generated when the device state is the Suspend state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the Suspend state is detected by means of the resume interrupt.

In host controller mode, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

28.3.3.9 OVRCR interrupt

An OVRCR interrupt is generated when the USB_OVRCURA or USB_OVRCURB pin level has changed. The levels of the USB_OVRCURA and USB_OVRCURB pins can be checked in the SYSSTS0.OVCMON[1:0] flags. The external power supply IC can check whether overcurrent is detected using the OVRCR interrupt.

For OTG connections, the OVRCR interrupt allows you to check whether a change is detected in the VBUS comparator.

28.3.3.10 BCHG interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether a peripheral device is connected and can also be used to detect a remote wakeup in host controller mode. The BCHG interrupt is generated in both host and device controller modes.

28.3.3.11 DTCH interrupt

A DTCH interrupt occurs when a USB bus disconnect is detected in host controller mode. The USBFS detects bus disconnects in compliance with the USB 2.0 specification.

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software. The pipes enter the wait state for a bus connection to the port, waiting for an ATTCH interrupt to occur. Regardless of the value set in the associated interrupt enable bit, the USBFS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt is detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state

28.3.3.12 SACK interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet is received from the peripheral device in host controller mode. The SACK interrupt can be used to confirm that the setup transaction is successfully complete.

28.3.3.13 SIGN interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet is not correctly received from the peripheral device three consecutive times in host controller mode. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

28.3.3.14 ATTCH interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 µs in host controller mode. To be more specific, an ATTCH interrupt is detected on any of the following conditions:

- When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 µs
- When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 µs

28.3.3.7 VBUS interrupt

当USB_VBUS引脚电平改变时，会产生VBUS中断。USB_VBUS引脚的电平可以通过INTSTS0.VBSTS位检查。主控制器是连接还是断开可以使用VBUS中断来确认。如果系统在连接主机控制器的情况下激活，则不会产生第一个VBUS中断，因为USB_VBUS引脚电平没有变化。

28.3.3.8 恢复中断

在设备控制器模式下，当设备状态为Suspend状态且USB总线状态发生变化（从J-state到K-state，或从J-state到SE0）时，会产生恢复中断。通过恢复中断检测从挂起状态的恢复。

在主机控制器模式下，不会产生恢复中断。使用BCHG中断来检测USB总线状态的变化。

28.3.3.9 OVRCR interrupt

当USB_OVRCURA或USB_OVRCURB引脚电平发生变化时，会产生OVRCR中断。的水平USB_OVRCURA和USB_OVRCURB引脚可以在SYSSTS0.OVCMON[1:0]标志中检查。外部电源IC可以使用OVRCR中断检查是否检测到过电流。

对于OTG连接，OVRCR中断允许您检查是否在VBUS比较器中检测到变化。

28.3.3.10 BCHG interrupt

当USB总线状态改变时会产生BCHG中断。BCHG中断可用于检测是否连接了外围设备，也可用于检测主机控制器模式下的远程唤醒。BCHG中断在主机和设备控制器模式下产生。

28.3.3.11 DTCH interrupt

当在主机控制器模式下检测到USB总线断开连接时，会发生DTCH中断。USBFS检测符合USB2.0规范的总线断开连接。

在检测到中断时，为相关端口执行通信的所有管道必须由软件终止。管道进入等待状态，等待总线连接到端口，等待ATTCH中断发生。无论相关中断使能位中设置的值如何，USBFS硬件：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态

28.3.3.12 SACK中断

当在主机控制器模式下从外围设备接收到对发送的设置数据包的ACK响应时，将产生SACK中断。SACK中断可用于确认设置事务成功完成。

28.3.3.13 标志中断

在主机控制器模式下，如果连续三次未从外围设备正确接收到已发送的设置数据包的ACK响应，则会产生SIGN中断。SIGN中断可用于检测没有从外围设备发送的ACK响应或ACK数据包的损坏。

28.3.3.14 ATTCH interrupt

在主机控制器模式下，当在USB端口上检测到全速信号电平的J状态或K状态持续2.5µs时，将产生ATTCH中断。更具体地说，在以下任何条件下都会检测到ATTCH中断：

- 当K-state、SE0或SE1变为J-state时，J-state持续2.5µs
- J-state、SE0或SE1变为K-state时，K-state持续2.5µs

28.3.3.15 EOFERR interrupt

An EOFERR interrupt occurs when the USBFS detects that communication is not complete at the EOF2 timing defined in the USB 2.0 specification.

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software, and the port must be re-enumerated. Regardless of the value set in the associated interrupt enable bit, the USBFS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt is detected to 0
- Puts the port in which the EOFERR interrupt is generated into the idle state

28.3.3.16 Portable Device Detection Interrupt

The USBFS sets the INTSTS1.PDDETINT flag to 1 on detecting a portable device and generates the portable device detection interrupt. When the portable device detection interrupt is generated, use software to repeat reading the BCCTRL1.PDDETSTS flag until the same value is read three or more times, and perform debounce processing.

28.3.4 Pipe Control

Table 28.19 lists the pipe settings for the USBFS. USB data transfer is performed through logical pipes that the software associates with endpoints. The USBFS provides 10 pipes that are used for data transfer. Set up the pipes based on your system specifications.

Table 28.19 Pipe settings (1 of 2)

Register name	Bit name	Setting	Notes
DCPCFG PIPECFG	TYPE	Transfer type	Pipes 1 to 9: Settable
	BFRE	BRDY interrupt mode	Pipes 1 to 5: Settable
	DBLB	Double buffer select	Pipes 1 to 5: Settable
	DIR	Transfer direction select	IN or OUT settable
	EPNUM	Endpoint number	Pipes 1 to 9: Settable A value other than 0000b must be set when the pipe is used.
	SHTNAK	Selects disabled state for pipe when transfer ends	Pipes 1 and 2: Settable only for bulk transfers Pipes 3 to 5: Settable
DCPMAXP PIPEMAXP	DEVSEL	Device select	Referenced only in host controller mode.
	MXPS	Maximum packet size	Compliant with the USB 2.0 specification.
PIPEPERI	IFIS	Buffer flush	Pipes 1 and 2: Settable only for isochronous transfers Pipes 3 to 9: Setting disabled
	IITV	Interval counter	Pipes 1 and 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Settable only in host controller mode
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit.
	INBUFM	IN buffer monitor	Available only for pipes 1 to 5.
	SUREQ	Setup request	Settable only for the DCP and controlled in host controller mode
	SUREQCLR	SUREQ clear	Settable only for the DCP and controlled in host controller mode
	ATREPM	Auto response mode	Pipes 1 to 5: Settable only in device controller mode
	ACLRM	Auto buffer clear	Pipes 1 to 9: Settable
	SQCLR	Sequence clear	Clears the data toggle bit
	SQSET	Sequence set	Sets the data toggle bit
	SQMON	Sequence monitor	Monitors the data toggle bit
	PBUSY	Pipe busy status	—
	PID	Response PID	See section 28.3.4.6. Response PID.

28.3.3.15 EOFERR interrupt

当USBFS检测到在USB2.0规范中定义的EOF2时序未完成通信时，将发生EOFERR中断。

在检测到中断时，所有为相关端口执行通信的管道必须由软件终止，并且必须重新枚举该端口。无论相关中断使能位中设置的值如何，USBFS硬件：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将产生EOFERR中断的端口置于空闲状态

28.3.3.16 便携式设备检测中断

USBFS在检测到便携式设备时将INTSTS1.PDDETINT标志设置为1，并生成便携式设备检测中断。当便携式设备检测中断产生时，使用软件重复读取BCCTRL1.PDDETSTS标志，直到读取相同的值3次或更多次，并进行去抖动处理。

28.3.4 管道控制

表28.19列出了USBFS的管道设置。USB数据传输是通过软件与端点关联的逻辑管道执行的。USBFS提供了10个用于数据传输的管道。根据您的系统规格设置管道。

Table 28.19 管道设置(1of2)

注册名称	位名称	Setting	Notes
DCPCFG PIPECFG	TYPE	传输类型	管道1至9：可设置
	BFRE	BRDY中断模式	管道1至5：可设置
	DBLB	双缓冲选择	管道1至5：可设置
	DIR	传输方向选择	输入或输出可设置
	EPNUM	端点编号	管道1至9：可设置 使用管道时，必须设置0000b以外的值。
	SHTNAK	传输结束时为管道选择禁用状态	管道1和2：仅可设置用于批量传输 管道3至5：可设置
DCPMAXP PIPEMAXP	DEVSEL	设备选择	仅在主机控制器模式下引用。
	MXPS	最大数据包大小	符合USB2.0规范。
PIPEPERI	IFIS	缓冲区刷新	管道1和2：仅可设置用于同步传输 管道3到9：设置禁用
	IITV	间隔计数器	管道1和2：仅可设置用于同步传输 管道3到5：禁用设置 管道6到9：仅在主机控制器模式下可设置
DCPCTR PIPEnCTR	BSTS	缓冲状态	对于DCP，接收缓冲器状态和发送缓冲器状态通过ISEL位切换。
	INBUFM	IN缓冲监视器	仅适用于管道1到5。
	SUREQ	设置请求	只能为DCP设置并在主机控制器模式下控制
	SUREQCLR	SUREQ clear	只能为DCP设置并在主机控制器模式下控制
	ATREPM	自动响应模式	管道1到5：仅在设备控制器模式下可设置
	ACLRM	自动缓冲区清除	管道1至9：可设置
	SQCLR	序列清晰	清除数据切换位
	SQSET	序列集	设置数据切换位
	SQMON	序列监视器	监控数据切换位
	PBUSY	管道繁忙状态	—
	PID	响应PID	请参阅第28.3.4.6节。响应PID。

Table 28.19 Pipe settings (2 of 2)

Register name	Bit name	Setting	Notes
PIPEnTRE	TRENB	Transaction counter enable	Pipes 1 to 5: Settable
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Settable
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Settable

28.3.4.1 Pipe control register switching procedures

The following bits in the pipe control registers can be changed only when USB communication is prohibited (PID = NAK).

Do not change the following registers and bits when USB communication is enabled (PID = BUF):

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN

To set these bits when USB communication is enabled (PID = BUF):

1. A request to change the bits in the pipe control register occurs.
2. Set the PID[1:0] bits associated with the pipe to NAK.
3. Wait until the associated PBUSY bit clears to 0.
4. Set the bits in the pipe control register.

The following bits in the pipe control registers can be changed only when the selected pipe information is not set in the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Do not set the following registers when the CURPIPE[3:0] bits are set:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEMAXP and PIPEPERI

To change pipe information, you must set the CURPIPE[3:0] bits in the port select registers to a pipe other than the one to be changed. For the DCP, the buffer must be cleared using the BCLR bit in the Port Control Register after the pipe information is changed.

28.3.4.2 Transfer types

The PIPECFG.TYPE[1:0] bits specify the following transfer types for each pipe:

- DCP: No setting is necessary (fixed at control transfer)
- Pipes 1 and 2: Set to bulk or isochronous transfer
- Pipes 3 to 5: Set to bulk transfer
- Pipes 6 to 9: Set to interrupt transfer

28.3.4.3 Endpoint number

The PIPECFG.EPNUM[3:0] bits are used to set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to 15.

- DCP: No setting is necessary (fixed at endpoint 0)
- Pipes 1 to 9: Select and set the endpoint numbers from 1 to 15 so that the combination of the PIPECFG.DIR and EPNUM[3:0] bits is unique

Table 28.19 管道设置(2of2)

注册名称	位名称	Setting	Notes
PIPEnTRE	TRENB	事务计数器启用	管道1至5：可设置
	TRCLR	当前交易柜台清零	管道1至5：可设置
PIPEnTRN	TRNCNT	交易柜台	管道1至5：可设置

28.3.4.1 管道控制寄存器切换程序

只有当USB通信被禁止(PID=NAK)时，管道控制寄存器中的以下位才能更改。

当启用USB通信(PID=BUF)时，请勿更改以下寄存器和位：

●DCPCFG和DCPMAXP中的位

●DCPCTR中的SQCLR和SQSET位

●PIPECFG、PIPEMAXP和PIPEPERI中的位

●PIPEnCTR中的ATREPM、ACLRM、SQCLR和SQSET位

●PIPEnTRE和PIPEnTRN中的位

要在启用USB通信(PID=BUF)时设置这些位：

1.发生更改管道控制寄存器中的位的请求。

2.将与管道关联的PID[1:0]位设置为NAK。

3.等到相关的PBUSY位清除为0。

4.设置管道控制寄存器中的位。

管道控制寄存器中的以下位只有在所选管道信息未设置时才能更改CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位。

设置CURPIPE[3:0]位时不要设置以下寄存器：

●DCPCFG和DCPMAXP中的位

●PIPECFG、PIPEMAXP和PIPEPERI中的位

要更改管道信息，您必须将端口选择寄存器中的CURPIPE[3:0]位设置为要更改的管道以外的管道。对于DCP，必须在管道信息更改后使用端口控制寄存器中的BCLR位清除缓冲区。

28.3.4.2 传输类型

PIPECFG.TYPE[1:0]位为每个管道指定以下传输类型：

●DCP：无需设置（控制转移时固定）

●管道1和2：设置为批量或同步传输

●管道3到5：设置为批量传输

●管道6到9：设置为中断传输

28.3.4.3 端点编号

PIPECFG.EPNUM[3:0]位用于设置每个管道的端点编号。DCP固定在端点0。其他管道可以设置从端点1到15。

●DCP：无需设置（固定在端点0）

●管道1到9：从1到15选择和设置端点编号，以便PIPECFG.DIR和EPNUM[3:0]位的组合是唯一的

28.3.4.4 Maximum packet size setting

Specify the maximum packet size for each pipe in the DCPMAXP.MXPS[6:0] and PIPEMAXP.MXPS[9:0] bits. The DCP and pipes 1 to 5 can be set to any of the maximum pipe sizes defined in the USB 2.0 specification. For pipes 6 to 9, the maximum packet size is 64 bytes. Set the maximum packet size as follows before starting a transfer (PID = BUF):

- DCP: Set to 8, 16, 32, or 64
- Pipes 1 to 5: Set to 8, 16, 32, or 64 for bulk transfers
- Pipes 1 and 2: Set between 1 and 256 for isochronous transfers
- Pipes 6 to 9: Set between 1 and 64

28.3.4.5 Transaction counter for pipes 1 to 5 in the receiving direction

When the specified number of transactions is complete in the data packet receiving direction, the USBFS recognizes that the transfer ended. Two transaction counters are provided: one is the PIPEnTRN register, which specifies the number of transactions to be executed, and the other is the current counter, which internally counts the number of executed transactions. If the PIPECFG.SHTNAK bit is set to 1, when the current counter value matches the specified number of transactions, the associated PIPEnCTR.PID[1:0] bits are set to NAK and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The data read from PIPEnTRN differs depending on the PIPEnTRE.TRENB setting as follows:

- The TRENB bit = 0: Specified transaction counter value can be read
- The TRENB bit = 1: Current counter value indicating the internally counted number of executed transactions can be read

The following constraints apply when working with the TRCLR bit:

- If the transactions are being counted and PID = BUF, the current counter cannot be cleared
- If there is any data left in the buffer, the current counter cannot be cleared

28.3.4.6 Response PID

Specify the response PID for each pipe in the PID[1:0] bits in DCPCTR and PIPEnCTR. This section describes the USBFS operation with different response PID settings.

(1) Software response PID settings in host controller mode

Select the response PID to specify the execution of transactions as follows:

- NAK setting: Using pipes is disabled and no transactions are executed
- BUF setting: Transactions are executed based on the FIFO buffer state:
  - OUT direction: An OUT token is issued if the FIFO buffer contains transmit data.
  - IN direction: An IN token is issued if the FIFO buffer is not full and can receive data.
- STALL setting: Using pipes is disabled and no transactions are executed

Note: Use the DCPCTR.SUREQ bit to execute setup transactions for the DCP.

(2) Software response PID settings in device controller mode

Select the response PID to respond as follows to transactions from the host:

- NAK setting: A NAK response is returned to all generated transactions
- BUF setting: A response is returned to transactions based on the FIFO buffer
- STALL setting: A STALL response is returned to all generated transactions

Note: For setup transactions, an ACK response is always returned, regardless of the PID[1:0] bits setting, and the USB request is stored in the register.

28.3.4.4 最大数据包大小设置

在DCPMAXP.MXPS[6:0]和PIPEMAXP.MXPS[9:0]位中指定每个管道的最大数据包大小。DCP和管道1到5可以设置为USB2.0规范中定义的任何最大管道尺寸。对于管道6到9，最大数据包大小为64字节。在开始传输之前设置最大数据包大小如下（PID=BUF）：

●DCP：设置为8、16、32或64

●管道1到5：设置为8、16、32或64以进行批量传输

●管道1和2：设置在1和256之间，用于同步传输

●管道6到9：设置在1到64之间

28.3.4.5 接收方向上管道1到5的事务计数器

当在数据包接收方向完成指定数量的事务时，USBFS识别传输结束。提供了两个事务计数器：一个是PIPEnTRN寄存器，指定要执行的事务数，另一个是当前计数器，内部统计执行的事务数。如果PIPECFG.SHTNAK位设置为1，则当当前计数器值与指定的事务数匹配时，相关的PIPEnCTR.PID[1:0]位将设置为NAK，并禁用后续传输。通过PIPEnTRE.TRCLR位初始化事务计数器功能的当前计数器，事务可以从头开始重新计数。从PIPEnTRN读取的数据因PIPEnTRE.TRENB设置而异，如下所示：

●TRENB位=0：可以读取指定的事务计数器值

●TRENB位=1：表示内部计数的已执行事务数的当前计数器值可被读取

使用TRCLR位时适用以下约束：

●如果正在对事务进行计数且PID=BUF，则无法清除当前计数器

●如果缓冲区中还有数据，则无法清除当前计数器

28.3.4.6 响应PID

在DCPCTR和PIPEnCTR的PID[1:0]位中指定每个管道的响应PID。本节介绍具有不同响应PID设置的USBFS操作。

(1) 主机控制器模式下的软件响应PID设置

选择响应PID来指定事务的执行，如下所示：

●NAK设置：禁用使用管道，不执行任何事务

●BUF设置：根据FIFO缓冲区状态执行事务：

OUT方向：如果FIFO缓冲区包含发送数据，则发出OUT令牌。

IN方向：如果FIFO缓冲区未满并且可以接收数据，则发出IN令牌。

●STALL设置：禁止使用管道，不执行任何事务

Note: 使用DCPCTR.SUREQ位执行DCP的设置事务。

(2) 设备控制器模式下的软件响应PID设置

选择响应PID以对来自主机的事务进行如下响应：

●NAK设置：对所有生成的事务返回NAK响应

●BUF设置：根据FIFO缓冲区向事务返回响应

●STALL设置：向所有生成的事务返回STALL响应

Note: 对于设置事务，无论PID[1:0]位设置如何，始终返回ACK响应，并且USB请求存储在寄存器中。

Sections (3) and (4) describe situations in which the USBFS writes to the PID[1:0] bits because of specific transaction results.

(3) Hardware response PID settings in host controller mode

- NAK setting: PID = NAK is set in the following cases, and issuing of tokens is automatically stopped:
  - When a non-isochronous transfer is performed and an NRDY interrupt is generated
    (For details, see section 28.3.3.2. NRDY interrupt.)
  - If a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
  - If transaction counting ends when the SHTNAK bit is set to 1 for bulk transfers
- BUF setting: The USBFS does not write this setting.
- STALL setting: PID = STALL is set in the following cases, and issuing of tokens is automatically stopped:
  - When STALL is received in response to a transmitted token
  - When a received data packet exceeds the maximum packet size

(4) Hardware response PID settings in device controller mode

- NAK setting: PID = NAK is set in the following cases, and a NAK response is returned to transactions:
  - When the setup token is received normally (DCP only)
  - If transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
- BUF setting: There is no BUF writing by the USBFS.
- STALL setting: PID = STALL is set in the following cases, and a STALL response is returned to transactions:
  - When a received data packet exceeds the maximum packet size
  - When a control transfer sequence error is detected (DCP only)

28.3.4.7 Data PID sequence bit

The USBFS automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit toggles on ACK handshake reception. When data is received, the sequence bit toggles on ACK handshake transmission. The SQCLR bit in DCPCTR and the SQSET bit in PIPEnCTR can be used to change the data PID sequence bit.

In device controller mode when control transfers are used, the USBFS automatically sets the sequence bit for stage transitions. DATA1 is returned when the setup stage ends. The sequence bit is not referenced and PID = DATA1 is returned in the status stage. Therefore, no software settings are required. However, in host controller mode when control transfers are used, the sequence bit must be set by software for the stage transitions.

For ClearFeature requests for transmission or reception, the data PID sequence bit must be set by software in both host and device controller modes.

28.3.4.8 Response PID = NAK function

The USBFS provides a function for disabling pipe operation (PID response = NAK) when the final data packet of a transaction is received. The USBFS automatically distinguishes this based on reception of a short packet or the transaction counter. Enable this function by setting the PIPECFG.SHTNAK bit to 1.

When the double buffer mode is being used for the FIFO buffer, using this function enables reception of data packets in transfer units. If pipe operation is disabled, the software must enable the pipe again (PID response = BUF).

The response PID = NAK function can be used only for bulk transfers.

第(3)和(4)节描述了USBFS由于特定事务结果而写入PID[1:0]位的情况。

(3) 主机控制器模式下的硬件响应PID设置

●NAK设置：PID=NAK在以下情况下设置，令牌自动停止发行：
当执行非同步传输并产生NRDY中断时
（有关详细信息，请参阅第28.3.3.2节。NRDY中断。）
如果在PIPECFG.SHTNAK位设置为1以进行批量传输时接收到短数据包
如果在SHTNAK位设置为1以进行批量传输时事务计数结束

●BUF设置：USBFS不写入此设置。

●STALL设置：PID=STALL在以下情况下设置，并且自动停止发行令牌：
当接收到STALL以响应传输的令牌时
当接收到的数据包超过最大包大小时

(4) 设备控制器模式下的硬件响应PID设置

●NAK设置：PID=NAK在以下情况下设置，并向事务返回NAK响应：
正常接收到设置令牌时（仅DCP）
当PIPECFG.SHTNAK位设置为1以进行批量传输时，如果事务计数结束或收到短数据包

●BUF设置：USBFS不写入BUF。

●STALL设置：PID=STALL在以下情况下设置，并向事务返回STALL响应：
当接收到的数据包超过最大包大小时
当检测到控制传输序列错误时（仅限DCP）

28.3.4.7 数据PID序列位

当数据在控制传输数据阶段、批量传输和中断传输成功传输时，USBFS会自动切换数据PID中的序列位。下一个要发送的数据PID的序列位可以通过DCPCTR和PIPEnCTR中的SQMON位来确认。发送数据时，序列位在ACK握手接收时切换。当接收到数据时，序列位在ACK握手传输上切换。DCPCTR中的SQCLR位和PIPEnCTR中的SQSET位可用于更改数据PID序列位。

在使用控制传输的设备控制器模式下，USBFS自动设置阶段转换的序列位。DATA1在设置阶段结束时返回。不引用序列位，在状态阶段返回PID=DATA1。因此，不需要任何软件设置。但是，在使用控制传输的主机控制器模式下，必须由软件设置序列位以进行阶段转换。

对于发送或接收的ClearFeature请求，数据PID序列位必须由软件在主机和设备控制器模式下设置。

28.3.4.8 响应PID=NAK功能

USBFS提供了在接收到事务的最终数据包时禁用管道操作（PID响应=NAK）的功能。USBFS根据收到的短数据包或事务计数器自动区分这一点。通过将PIPECFG.SHTNAK位设置为1来启用此功能。

当FIFO缓冲区使用双缓冲区模式时，使用此功能可以接收以传输为单位的数据包。如果管道操作被禁用，软件必须再次启用管道（PID响应=BUF）。

响应PID=NAK函数只能用于批量传输。

28.3.4.9 Auto response mode

For bulk transfer pipes (1 to 5), when the PIPEnCTR.ATREPM bit is set to 1, a transition is made to auto response mode. During an OUT transfer (PIPECFG.DIR = 0), OUT-NAK mode is invoked, and during an IN transfer (DIR = 1), null auto response mode is invoked.

28.3.4.10 OUT-NAK mode

For bulk OUT transfer pipes, NAK is returned in response to an OUT token, and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To transition from normal mode to OUT-NAK mode, specify OUT-NAK mode while pipe operation is disabled (PID[1:0] = 00b for NAK response). Next enable pipe operation (PID[1:0] = 01b for BUF response), on which OUT-NAK mode becomes valid. If an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is returned to the host.

To transition from OUT-NAK mode to normal mode, cancel OUT-NAK mode while pipe operation is disabled (NAK). Next enable pipe operation (BUF). In normal mode, reception of OUT data is enabled.

28.3.4.11 Null auto response mode

For bulk IN transfer pipes, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To transition from normal mode to null auto response mode, specify null auto response mode while pipe operation is disabled (response PID = NAK). Next enable pipe operation (response PID = BUF) on which null auto response mode becomes valid. Before setting null auto response mode, check that PIPEnCTR.INBUFM = 0, because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, empty the buffer using the PIPEnCTR.ACLRM bit. Do not write data from the FIFO port while a transition to null auto response mode is being made.

To transition from null auto response mode to normal mode, keep pipe operation disabled (response PID = NAK) for the period of the zero-length packet transmission (about 10 µs) before canceling the null auto response mode. In normal mode, data can be written from the FIFO port, so packet transmission to the host is enabled by enabling pipe operation (response PID = BUF).

28.3.5 FIFO Buffer

The USBFS provides a FIFO buffer for data transfers, and it manages the memory area used for each pipe. The FIFO buffer has two states depending on whether the access right is assigned to the system (CPU side) or the USBFS (SIE side).

(1) Buffer status

Table 28.20 and Table 28.21 show the buffer status in the USBFS. The FIFO buffer status can be confirmed using the DCPCTR.BSTS and PIPEnCTR.INBUFM bits. The transfer direction for the FIFO buffer can be specified in either the PIPECFG.DIR or CFIFOSEL.ISEL bit (when DCP is selected).

The INBUFM bit is valid for pipes 0 to 5 in the transmitting direction.

When a transmitting pipe uses double buffering, the software can read the BSTS bit to monitor the FIFO buffer status on the CPU side and the INBUFM bit to monitor the FIFO buffer status on the SIE side. When write access to the FIFO port by the CPU or DMA/DTC is slow and the buffer empty status cannot be determined using the BEMP interrupt, the software can use the INBUFM bit to confirm the end of transmission.

Table 28.20 Buffer status indicated in the BSTS bit

ISEL or DIR	BSTS	FIFO buffer status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet is received. Reading from the FIFO port is allowed. When a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	Transmission has not completed. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	Transmission is complete. CPU write is allowed.

28.3.4.9 自动响应模式

对于批量传输管道（1到5），当PIPEnCTR.ATREPM位设置为1时，将转换到自动响应模式。在OUT传输期间(PIPECFG.DIR=0)，将调用OUT-NAK模式，在IN传输期间(DIR=1)，将调用空自动响应模式。

28.3.4.10 OUT-NAK mode

对于批量OUT传输管道，NAK响应OUT令牌返回，并且当PIPEnCTR.ATREPM位设置为1。要从正常模式转换到OUT-NAK模式，请在禁用管道操作时指定OUT-NAK模式（对于NAK响应，PID[1:0]=00b）。接下来启用管道操作（PID[1:0]=01b用于BUF响应），此时OUT-NAK模式变为有效。如果在禁用管道操作之前立即收到OUT令牌，则正常接收令牌数据，并向主机返回ACK。

要从OUT-NAK模式转换到正常模式，请在禁用管道操作(NAK)时取消OUT-NAK模式。接下来启用管道操作(BUF)。在正常模式下，可以接收OUT数据。

28.3.4.11 空自动响应模式

对于批量IN传输管道，当PIPEnCTR.ATREPM位设置为1时，将连续传输零长度数据包。

要从正常模式转换为空自动响应模式，请在禁用管道操作时指定空自动响应模式（响应PID=NAK）。接下来启用空自动响应模式有效的管道操作（响应PID=BUF）。在设置空自动响应模式之前，请检查PIPEnCTR.INBUFM=0，因为只有在缓冲区为空时才能设置模式。如果INBUFM位为1，则使用PIPEnCTR.ACLRM位清空缓冲区。在转换到空自动响应模式时，不要从FIFO端口写入数据。

要从空值自动响应模式转换到正常模式，在取消空值自动响应模式之前，在零长度数据包传输期间（约10µs）保持管道操作禁用（响应PID=NAK）。在正常模式下，可以从FIFO端口写入数据，因此通过启用管道操作（响应PID=BUF）来启用到主机的数据包传输。

28.3.5 FIFO Buffer

USBFS为数据传输提供FIFO缓冲区，并管理用于每个管道的内存区域。根据访问权限是分配给系统（CPU端）还是USBFS（SIE端），FIFO缓冲区有两种状态。

(1) 缓冲状态

表28.20和表28.21显示了USBFS中的缓冲区状态。FIFO缓冲区状态可以使用确认DCPCTR.BSTS和PIPEnCTR.INBUFM位。FIFO缓冲区的传输方向可以在任一pipecfg.dir或cfifoselisel位（选择DCP时）。

INBUFM位对传输方向的管道0到5有效。

当传输管道使用双缓冲时，软件可以读取BSTS位来监控CPU侧的FIFO缓冲区状态，以及读取INBUFM位来监控SIE侧的FIFO缓冲区状态。当写访问FIFO端口由CPU或DMADTC较慢且无法使用BEMP中断确定缓冲区空状态，软件可以使用INBUFM位确认传输结束。

Table 28.20 BSTS位中指示的缓冲区状态

ISEL或DIR	BSTS	FIFO缓冲区状态
0 (receiving direction)	0	没有接收到数据，或正在接收数据。 禁止从FIFO端口读取。
0 (receiving direction)	1	有接收数据，或接收到零长度数据包。 允许从FIFO端口读取。 当接收到零长度数据包时，无法读取，必须清除缓冲区。
1 (transmitting direction)	0	传输尚未完成。 禁止写入FIFO端口。
1 (transmitting direction)	1	传输完成。 允许CPU写入。

Table 28.21 Buffer status indicated in the INBUFM bit

DIR	INBUFM	FIFO buffer status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	Transmission is complete. There is no data waiting to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

28.3.6 FIFO Buffer Clearing

Table 28.22 shows the methods for clearing the FIFO buffer. The FIFO buffer can be cleared using BCLR bit in the port control register, DnFIFOSEL.DCLRM, or the PIPEnCTR.ACLRM bit.

Single or double buffering can be selected for pipes 1 to 5 in the PIPECFG.DBLB bit.

Table 28.22 Buffer clearing methods

FIFO buffer clearing mode	Clearing FIFO buffer on the CPU side	Mode for automatically clearing the FIFO buffer after reading the specified pipe data	Auto buffer clear mode for discarding all received packets
Register used	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Bit used	BCLR	DCLRM	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid	1: Mode valid 0: Mode invalid

(1) Auto buffer clear mode function

The USBFS discards all received data packets if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet is received, the ACK response is returned to the host controller. The auto buffer clear mode function can only be set in the FIFO buffer reading direction.

Setting the ACLRM bit to 1 and then to 0 clears the FIFO buffer of the selected pipe regardless of the access direction. An access cycle of at least 100 ns is required for the internal hardware sequence processing between ACLRM = 1 and ACLRM = 0.

28.3.7 FIFO Port Functions

Table 28.23 shows the settings for the FIFO port functions. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, set the BVAL flag in the port control register to end writing. To send a zero-length packet, use the BCLR bit to clear the buffer, and then set the BVAL flag to end writing.

In reading, reception of new packets is automatically enabled when all data is read. Data cannot be read when a zero-length packet is received (DTLN[8:0] = 0), so the buffer must be cleared with the BCLR bit. The length of the receive data can be confirmed in the DTLN[8:0] bits in the port control register.

Table 28.23 FIFO port function settings (1 of 2)

Register name	Bit name	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	Selects DTLN[11:0] read mode
	REW	FIFO buffer rewind (re-read, rewrite)
	DCLRM	Automatically clears receive data for a specified pipe after the data is read (only for DnFIFO)
	DREQE	Enables DMA/DTC transfers (only for DnFIFO)
	MBW	FIFO port access bit width
	BIGEND	Selects FIFO port endian
	ISEL	FIFO port access direction (only for DCP)
	CURPIPE	Selects the current pipe

Table 28.21 INBUFM位中指示的缓冲区状态

DIR	INBUFM	FIFO缓冲区状态
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	传输完成。 没有等待传输的数据。
1 (transmitting direction)	1	FIFO端口已将数据写入缓冲区。 有数据要传输。

28.3.6 FIFO缓冲区清除

表28.22显示了清除FIFO缓冲区的方法。可以使用端口控制寄存器中的BCLR位、DnFIFOSEL.DCLRM或PIPEnCTR.ACLRM位清除FIFO缓冲区。

可以在PIPECFG.DBLB位中为管道1到5选择单缓冲或双缓冲。

Table 28.22 缓冲区清除方法

FIFO缓冲区清除模式	清除FIFO缓冲区 CPU端	读取指定管道数据后自动清除FIFO缓冲区的模式	自动缓冲区清除模式，用于丢弃所有接收到的数据包
注册使用	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
使用的位	BCLR	DCLRM	ACLRM
清算条件	通过写1清除	1：模式有效0 ：模式无效	1：模式有效0 ：模式无效

(1) 自动缓冲清除模式功能

如果PIPEnCTR.ACLRM位设置为1，USBFS将丢弃所有接收到的数据包。如果接收到正确的数据包，则向主机控制器返回ACK响应。自动缓冲区清除模式功能只能在FIFO缓冲区读取方向设置。

无论访问方向如何，将ACLRM位设置为1，然后设置为0都会清除所选管道的FIFO缓冲区。ACLRM=1和ACLRM=0之间的内部硬件序列处理需要至少100ns的访问周期。

28.3.7 FIFO端口功能

表28.23显示了FIFO端口功能的设置。在写访问中，在达到最大数据包大小之前写入数据会自动启用数据传输。要在达到最大数据包大小之前启用传输，请设置端口控制寄存器中的BVAL标志以结束写入。要发送零长度数据包，请使用BCLR位清除缓冲区，然后设置BVAL标志以结束写入。

在读取中，当所有数据被读取时，自动启用新数据包的接收。接收到零长度数据包时（DTLN[8:0]=0）无法读取数据，因此必须使用BCLR位清除缓冲区。接收数据的长度可以在端口控制寄存器的DTLN[8:0]位中确认。

Table 28.23 FIFO端口功能设置(1of2)

注册名称	位名称	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	选择DTLN[11:0]读取模式
	REW	FIFO缓冲区倒带（重新读取、重写）
	DCLRM	读取数据后自动清除指定管道的接收数据（仅适用于DnFIFO）
	DREQE	启用DMADTC传输（仅适用于DnFIFO）
	MBW	FIFO端口访问位宽
	BIGEND	选择FIFO端口字节序
	ISEL	FIFO端口访问方向（仅适用于DCP）
	CURPIPE	选择当前管道

Table 28.23 FIFO port function settings (2 of 2)

Register name	Bit name	Description
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	Ends writing to the FIFO buffer
	BCLR	Clears the FIFO buffer on the CPU side
	DTLN	Checks the length of receive data

(1) FIFO port selection

Table 28.24 shows the pipes that can be selected with the different FIFO ports. The pipe to be accessed must be selected in the CURPIPE[3:0] bits in the port select register. After the pipe is selected, the software must check whether the written value can be read correctly from the CURPIPE[3:0] bits. (If the previous pipe number is read, it indicates that the USBFS is modifying the pipe.) Next, the software checks that the FRDY bit in the port control register is 1.

In addition, the software must specify the bus width to be accessed in the MBW bit in the port select register. The FIFO buffer access direction conforms to the PIPECFG.DIR setting. For the DCP only, the ISEL bit in the port select register determines the direction.

Table 28.24 FIFO port access by pipe

Pipe	Access method	Ports that can be used
DCP	CPU access	CFIFO port register
Pipes 1 to 9	CPU access	• CFIFO port register • D0FIFO/D1FIFO port register
	DMA/DTC access	D0FIFO/D1FIFO port register

(2) REW bit

It is possible to temporarily stop access to a pipe currently being accessed, access a different pipe, and then continue processing for the first pipe again. The REW bit in the port select register is used for this processing.

If a pipe is selected in the CURPIPE[3:0] bits in the port select register with the REW bit set to 1, the pointer used for reading from and writing to the FIFO buffer is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with 0 set for the REW bit, data can be read and written in continuation from the previous selection, without the pointer being reset.

To access the FIFO port, the software must check that the FRDY bit in the port control register is 1 after selecting a pipe.

28.3.8 DMA Transfers (D0FIFO and D1FIFO Ports)

(1) Overview of DMA transfers

For pipes 1 to 9, the FIFO port can be accessed using the DMAC. When buffer access for a pipe targeted for DMA transfer is enabled, a DMA transfer request is issued.

Select the unit of transfer to the FIFO port in the DnFIFOSEL.MBW bit, and select the pipe targeted for the DMA transfer in the DnFIFOSEL.CURPIPE[3:0] bits. Do not change the selected pipe during the DMA transfer.

(2) DnFIFO auto clear mode (D0FIFO and D1FIFO port reading direction)

If 1 is set in the DnFIFOSEL.DCLRM bit, the USBFS automatically clears the FIFO buffer of the selected pipe when reading of data from the FIFO buffer is complete.

Table 28.25 shows the packet reception and FIFO buffer clearing processing by software for each of the settings. As shown in the table, the buffer clearing conditions depend on the value set in the PIPECFG.BFRE bit. Using the DnFIFOSEL.DCLRM bit eliminates the need for the buffer to be cleared by software in any situation that requires buffer clearing. This enables DMA transfers without involving software.

The DnFIFO auto clear mode can only be set in the FIFO buffer reading direction.

Table 28.23 FIFO端口功能设置(2of2)

注册名称	位名称	Description
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	结束写入FIFO缓冲区
	BCLR	清除CPU端的FIFO缓冲区
	DTLN	检查接收数据的长度

(1) 先进先出端口选择

表28.24显示了可以使用不同FIFO端口选择的管道。必须在端口选择寄存器的CURPIPE[3:0]位中选择要访问的管道。选择管道后，软件必须检查是否可以从CURPIPE[3:0]位正确读取写入的值。（如果读取了之前的管道号，则表明USBFS正在修改管道。）接下来，软件检查端口控制寄存器中的FRDY位是否为1。

此外，软件必须在端口选择寄存器的MBW位中指定要访问的总线宽度。FIFO缓冲区访问方向符合PIPECFG.DIR设置。仅对于DCP，端口选择寄存器中的ISEL位决定方向。

Table 28.24 通过管道访问FIFO端口

Pipe	访问方法	可以使用的端口
DCP	CPU访问	CFIFO端口寄存器
管道1至9	CPU访问	• CFIFO端口寄存器 • D0FIFOD1FIFO端口寄存器
	DMA/DTC access	D0FIFOD1FIFO端口寄存器

(2) REW位

可以暂时停止对当前正在访问的管道的访问，访问不同的管道，然后再次继续处理第一个管道。端口选择寄存器中的REW位用于此处理。

如果在端口选择寄存器的CURPIPE[3:0]位中选择了一个管道，并且REW位设置为1，则用于读取和写入FIFO缓冲区的指针复位，可以进行读取或写入从第一个字节开始。如果在REW位设置为0的情况下选择管道，则可以从先前的选择继续读取和写入数据，而无需重置指针。

要访问FIFO端口，软件必须在选择管道后检查端口控制寄存器中的FRDY位是否为1。

28.3.8 DMA传输（D0FIFO和D1FIFO端口）

(1) DMA传输概述

对于管道1到9，可以使用DMAC访问FIFO端口。当启用以DMA传输为目标的管道的缓冲区访问时，将发出DMA传输请求。

在DnFIFOSEL.MBW位中选择传输到FIFO端口的单位，并在DnFIFOSEL.CURPIPE[3:0]位中选择DMA传输的目标管道。在DMA传输期间不要更改选定的管道。

(2) DnFIFO自动清除模式（D0FIFO和D1FIFO端口读取方向）

如果DnFIFOSEL.DCLRM位设置为1，USBFS会在从FIFO缓冲区读取数据完成时自动清除所选管道的FIFO缓冲区。

表28.25显示了针对每个设置通过软件进行的数据包接收和FIFO缓冲区清除处理。如表所示，缓冲区清除条件取决于PIPECFG.BFRE位中设置的值。使用DnFIFOSEL.DCLRM位无需在任何需要清除缓冲区的情况下通过软件清除缓冲区。这可以在不涉及软件的情况下实现DMA传输。

DnFIFO自动清除模式只能设置在FIFO缓冲区读取方向。

Table 28.25 Packet reception and FIFO buffer clearing processing by software

Buffer status when packet is received	Register setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	No clearing required	No clearing required	No clearing required	No clearing required
Zero-length packet reception	Clearing required	Clearing required	No clearing required	No clearing required
Normal short packet reception	No clearing required	Clearing required	No clearing required	No clearing required
Transaction count end	No clearing required	Clearing required	No clearing required	No clearing required

28.3.9 Control Transfers Using the DCP

The DCP is used for data transfers in the control transfer data stage. The FIFO buffer of the DCP is a 64-byte single buffer with a fixed area for both control reads and control writes. The FIFO buffer can be accessed only through the CFIFO port.

28.3.9.1 Control transfers in host controller mode

(1) Setup stage

The USQREQ, USBVAL, USBINDX, and USBLENG registers are used to transmit USB requests for setup transactions. Writing the setup packet data to the registers and then writing 1 to the DCPCTR.SUREQ bit transmits the specified data for the setup transaction. On completion of the transaction, the SUREQ bit clears to 0. Do not change these USB request registers while SUREQ = 1.

When an attached function device is detected, the software must issue the first setup transaction for the device using this sequence with the DCPMAXP.DEVSEL[3:0] bits cleared to 0 and the DEVADD0.USBSPD[1:0] bits set appropriately.

When an attached function device is shifted to the Address state, the software must issue setup transactions using this sequence with the assigned USB address set in the DEVSEL[3:0] bits and the bits in DEVADDn corresponding to the specified USB address set appropriately. For example, when PIPEMAXP.DEVSEL[3:0] = 0010b, make appropriate settings in DEVADD2. When PIPEMAXP.DEVSEL[3:0] = 0101b, make appropriate settings in DEVADD5.

When the setup transaction data is sent, an interrupt request is generated based on the response from the peripheral device (SIGN or SACK bit in INTSTS1). This interrupt request allows the software to check the setup transaction result.

A DATA0 data packet (USB request) for the setup transaction is always transmitted regardless of the status of the DCPCTR.SQMON bit.

(2) Data stage

The data stage is used to transfer data using the DCP FIFO buffer.

Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit. Specify the transfer direction in the DCPCFG.DIR bit.

For the first data packet of the data stage, the data PID must be transferred as DATA1. Set data PID = DATA1 in the DCPCTR.SQSET bit and set the PID bits = BUF. Completion of data transfer is detected using the BRDY or BEMP interrupt.

For control write transfers, when the number of data bytes to be sent is an integer multiple of the maximum packet size, the software must send a zero-length packet at the end.

(3) Status stage

The status stage is used for zero-length packet data transfers in the reverse direction of the data stage. As in the data stage, data is transfered using the DCP FIFO buffer. Transactions are executed using the same procedure as the data stage.

Data packets in the status stage must be transmitted and received with the data PID set to DATA1 using the DCPCTR.SQSET bit.

When a zero-length packet is received, check the receive-data length in the CFIFOCTR.DTLN[8:0] bits after a BRDY interrupt is generated, and then clear the FIFO buffer using the BCLR bit.

Table 28.25 通过软件进行数据包接收和FIFO缓冲区清除处理

收到数据包时的缓冲区状态	注册设置			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
缓冲区已满	无需清算	无需清算	无需清算	无需清算
零长度数据包接收	需要清算	需要清算	无需清算	无需清算
正常短包接收	无需清算	需要清算	无需清算	无需清算
交易计数结束	无需清算	需要清算	无需清算	无需清算

28.3.9 使用DCP进行控制传输

DCP用于控制传输数据阶段的数据传输。DCP的FIFO缓冲区是一个64字节的单缓冲区，具有用于控制读取和控制写入的固定区域。FIFO缓冲区只能通过CFIFO端口访问。

28.3.9.1 主机控制器模式下的控制传输

(1) 设置阶段

USQREQ、USBVAL、USBINDX和USBLENG寄存器用于传输设置事务的USB请求。
将设置数据包数据写入寄存器，然后向DCPCTR.SUREQ位写入1，以传输设置事务的指定数据。事务完成后，SUREQ位清除为0。在SUREQ=1时不要更改这些USB请求寄存器。

当检测到连接的功能器件时，软件必须使用此序列为器件发出第一个设置事务，其中DCPMAXP.DEVSEL[3:0]位清零，DEVADD0.USBSPD[1:0]位适当设置。

当连接的功能器件转移到地址状态时，软件必须使用此序列发出设置事务，其中指定的USB地址设置在DEVSEL[3:0]位中，并且DEVADDn中的位对应于指定的USB地址设置适当。例如，当PIPEMAXP.DEVSEL[3:0]=0010b时，在DEVADD2中进行适当的设置。当PIPEMAXP.DEVSEL[3:0]=0101b时，在DEVADD5中进行适当的设置。

发送设置事务数据时，根据外围设备的响应（INTSTS1中的SIGN或SACK位）生成中断请求。该中断请求允许软件检查设置事务结果。

一个DATA0数据包（USB请求）用于设置事务总是被传输，无论状态如何
DCPCTR.SQMON bit.

(2) 数据阶段

数据级用于使用DCPFIFO缓冲区传输数据。

在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。在DCPCFG.DIR位中指定传输方向。

对于数据阶段的第一个数据包，数据PID必须作为DATA1传输。在DCPCTR.SQSET位中设置数据PID=DATA1，并设置PID位=BUF。使用BRDY或BEMP中断检测数据传输的完成。

对于控制写传输，当要发送的数据字节数是最大数据包大小的整数倍时，软件必须在最后发送一个长度为零的数据包。

(3) 状态阶段

状态阶段用于在数据阶段的相反方向上进行零长度分组数据传输。与数据阶段一样，使用DCPFIFO缓冲区传输数据。事务使用与数据阶段相同的过程执行。

状态阶段的数据包必须在数据PID设置为DATA1的情况下使用
DCPCTR.SQSET bit.

当接收到零长度数据包时，在产生BRDY中断后检查CFIFOCTR.DTLN[8:0]位中的接收数据长度，然后使用BCLR位清除FIFO缓冲区。

28.3.9.2 Control transfers in device controller mode

(1) Setup stage

The USBFS sends an ACK response to a normal setup packet for the USBFS. The USBFS operates in the setup stage as follows:

On receiving a new setup packet, the USBFS sets the following bits:

- Sets the INTSTS0.VALID bit to 1
- Sets the DCPCTR.PID[1:0] bits to NAK
- Sets the DCPCTR.CCPL bit to 0

When the USBFS receives a data packet following a setup packet, it stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Before performing the response processing for a control transfer, set the VALID flag to 0. When the VALID bit = 1, PID = BUF cannot be set, and the data stage cannot be terminated.

Using the VALID bit function, the USBFS can suspend a request being processed when it receives a new USB request during a control transfer and return a response to the latest request.

In addition, the USBFS automatically detects the direction bit (bmRequestType bit [8]) and the request data length (wLength) in the received USB request. It distinguishes between control read transfers, control write transfers, and no-data control transfers, and it controls stage transitions. For an incorrect sequence, a sequence error occurs in the control transfer stage transition interrupt, and the interrupt is reported to the software. For a diagram of the stage control by the USBFS, see Figure 28.16.

(2) Data stage

The DCP must be used to execute data transfers for received USB requests. Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit.

If the transfer data is larger than the size of the DCP FIFO buffer, execute the data transfer using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

(3) Status stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to BUF.

After this setting is made, the USBFS automatically executes the status stage based on the data transfer direction determined at the setup stage. The procedure is as follows:

- For control read transfers

  The USBFS receives a zero-length packet from the USB host and transmits an ACK response.
- For control write transfers and no-data control transfers

  The USBFS transmits a zero-length packet and receives an ACK response from the USB host.

(4) Control transfer auto response function

The USBFS automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, a response from the software is necessary.

- bmRequestType is not 00h: Any transfer other than a control write transfer
- wIndex is not 00h: Request error
- wLength is not 00h: Any transfer other than a no-data control transfer
- wValue is larger than 7Fh: Request error
- INTSTS0.DVSQ[2:0] are 011b (Configured state): Control transfer of a device state error

For all requests other than the SET_ADDRESS request, a response is required from the corresponding software.

28.3.9.2 设备控制器模式下的控制传输

(1) 设置阶段

USBFS向USBFS的正常设置数据包发送ACK响应。USBFS在设置阶段运行如下：

在接收到新的设置数据包时，USBFS设置以下位：

- ●将INTSTS0.VALID位设置为1
- ●将DCPCTR.PID[1:0]位设置为NAK
- ●将DCPCTR.CCPL位设置为0

当USBFS在setup数据包之后接收到数据包时，它会将USB请求参数存储在USBREQ中，
USBVAL, USBINDX, and USBLENG.

在执行控制传输的响应处理之前，将VALID标志设置为0。当VALID位=1时，PID=
BUF不能设置，数据阶段不能终止。

使用VALID位功能，USBFS可以在控制传输期间接收到新的USB请求时暂停正在处理的请求，并返回对最新请求的响应。

此外，USBFS会自动检测接收到的USB请求中的方向位（bmRequestTypebit[8]）和请求数据长度（wLength）。它区分控制读取传输、控制写入传输和无数据控制传输，并控制阶段转换。对于不正确的序列，在控制转移阶段转换中断中发生序列错误，并将中断报告给软件。USBFS的阶段控制图见图28.16。

(2) 数据阶段

DCP必须用于执行接收到的USB请求的数据传输。在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。

如果传输数据大于DCPFIFO缓冲区的大小，则使用控制写传输的BRDY中断和控制读传输的BEMP中断执行数据传输。

(3) 状态阶段

通过将DCPCTR.CCPL位设置为1而将DCPCTR.PID[1:0]位设置为BUF来终止控制传输。

完成此设置后，USBFS根据设置阶段确定的数据传输方向自动执行状态阶段。程序如下：

- ●用于控制读取传输

  USBFS从USB主机接收零长度数据包并发送ACK响应。
- ●用于控制写传输和无数据控制传输

  USBFS发送一个长度为零的数据包并接收来自USB主机的ACK响应。

(4) 控制转移自动响应功能

USBFS自动响应正确的SET_ADDRESS请求。如果出现以下任何错误
SET_ADDRESS请求，需要软件的响应。

- ●bmRequestType不是00h：控制写入传输以外的任何传输
- ●wIndexisnot00h：请求错误
- ●wLength不是00h：除无数据控制传输之外的任何传输
- ●wValue大于7Fh：请求错误
- ●INTSTS0.DVSQ[2:0]为011b（已配置状态）：设备状态错误的控制传输

对于除SET_ADDRESS请求之外的所有请求，都需要相应软件的响应。

28.3.10 Bulk Transfers (Pipes 1 to 5)

The FIFO buffer usage (single/double buffer setting) is configurable for bulk transfers. The USBFS provides the following functions for bulk transfers:

- BRDY interrupt function (PIPECFG.BFRE bit), see section 28.3.3.1. BRDY interrupt
- Transaction count function (PIPEnTRE.TRENB, TRCLR, and PIPEnTRN.TRNCNT[15:0] bits), see section 28.3.4.5. Transaction counter for pipes 1 to 5 in the receiving direction
- Response PID = NAK function (PIPECFG.SHTNAK bit), see section 28.3.4.8. Response PID = NAK function
- Auto response mode (PIPEnCTR.ATREPM bit), see section 28.3.4.9. Auto response mode

28.3.11 Interrupt Transfers (Pipes 6 to 9)

In device controller mode, the USBFS performs interrupt transfers based on the timing dictated by the host controller.

In host controller mode, the software can set the timing for issuing tokens using the interval counter.

28.3.11.1 Interval counter for interrupt transfers in host controller mode

Specify the transaction interval for interrupt transfers in the PIPEPERI.IITV[2:0] bits. The USBFS issues interrupt transfer tokens based on this interval.

(1) Counter initialization

The USBFS initializes the interval counter under the following conditions:

- Power-on reset

  This initializes the IITV[2:0] bits.
- FIFO buffer initialization using the PIPEnCTR.ACLRM bit:

  This does not initialize the IITV[2:0] bits, but does initialize the count value. Setting the PIPEnCTR.ACLRM bit to 0 starts counting from the value set in IITV[2:0].

The interval counter is not initialized in the following case:

- USB bus reset or USB suspended

  The IITV[2:0] bits are not initialized. Setting 1 to the DVSTCTR0.UACT bit starts counting from the value saved before entering the USB bus reset state or USB suspend state.

(2) Operation when tokens cannot be transmitted or received even on token generation

No token is generated in the following cases even at token generation time. In these cases, the USBFS tries to execute the transaction in the next interval.

- When the PID is set to NAK or STALL
- When the FIFO buffer is full at token transmit time in the receiving (IN) direction
- When there is no data to be transmitted in the FIFO buffer at token transmit time in the transmitting (OUT) direction

28.3.12 Isochronous Transfers (Pipes 1 and 2)

The USBFS provides the following functions for isochronous transfers:

- Notification of isochronous transfer error
- Interval counter specified in the PIPEPERI.IITV[2:0] bits
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function specified in the PIPEPERI.IFIS bit

28.3.10 批量传输（管道1到5）

FIFO缓冲区使用（单双缓冲区设置）可配置为批量传输。USBFS为批量传输提供以下功能：

●BRDY中断功能（PIPECFG.BFRE位），见28.3.3.1节。BRDY中断

●事务计数函数（PIPEnTRE.TRENB、TRCLR和PIPEnTRN.TRNCNT[15:0]位），参见第28.3.4.5节。接收方向上管道1到5的事务计数器

●响应PID=NAK功能（PIPECFG.SHTNAK位），参见第28.3.4.8节。响应PID=NAK功能

●自动响应模式（PIPEnCTR.ATREPM位），参见第28.3.4.9节。自动响应模式

28.3.11 中断传输（管道6到9）

在设备控制器模式下，USBFS根据主机控制器规定的时序执行中断传输。

在主机控制器模式下，软件可以使用间隔计数器设置发布令牌的时间。

28.3.11.1 主机控制器模式下中断传输的间隔计数器

在PIPEPERI.IITV[2:0]位中指定中断传输的事务间隔。USBFS基于此间隔发出中断传输令牌。

(1) 计数器初始化

USBFS在以下条件下初始化间隔计数器：

- Power-on reset

  这将初始化IITV[2:0]位。

●使用PIPEnCTR.ACLRM位初始化FIFO缓冲区：

这不会初始化IITV[2:0]位，但会初始化计数值。将PIPEnCTR.ACLRM位设置为0从IITV[2:0]中设置的值开始计数。

在以下情况下不初始化间隔计数器：

●USB总线复位或USB挂起

IITV[2:0]位未初始化。将DVSTCTR0.UACT位置1从进入USB总线复位状态或USB挂起状态之前保存的值开始计数。

(2) 即使在生成令牌时也无法发送或接收令牌时的操作

在以下情况下，即使在生成令牌时也不会生成令牌。在这些情况下，USBFS会尝试在下一个时间间隔执行事务。

●当PID设置为NAK或STALL时

●接收(IN)方向的令牌发送时FIFO缓冲区已满时

●在发送（OUT）方向的令牌发送时间，FIFO缓冲区中没有要发送的数据时

28.3.12 同步传输（管道1和2）

USBFS为同步传输提供以下功能：

●同步传输错误通知

●PIPEPERI.IITV[2:0]位中指定的间隔计数器

●同步IN传输数据设置控制（IDLY功能）

●PIPEPERI.IFIS位中指定的同步IN传输缓冲区刷新功能

28.3.12.1 Error detection in isochronous transfers

The USBFS provides a function for detecting the errors described in this section, so that when errors occur in isochronous transfers, they can be controlled by software. Table 28.26 and Table 28.27 show the priority order for errors detected by the USBFS and the associated interrupts.

PID errors

- The PID value of the received packet is invalid.

CRC errors and bit stuffing errors

- A CRC error is found in a received packet or the bit stuffing is illegal.

Maximum packet size exceeded

- The data size of the received packet exceeds the specified maximum packet size.

Overrun and underrun errors

In host controller mode:

- The FIFO buffer is full at token transmit time in the IN (receiving) direction
- There is no data to be sent in the FIFO buffer at token transmit time in the OUT (transmitting) direction

In device controller mode:

- There is no data to be sent in the FIFO buffer at token receive time in the IN (transmitting) direction
- The FIFO buffer is full at token receive time in the OUT (receiving) direction

Interval errors

In device controller mode, the following cases are treated as an interval error:

- Failure to receive an IN token in the interval frame during an isochronous IN transfer
- Failure to receive an OUT token in the interval frame during an isochronous OUT transfer

Table 28.26 Error detection for token transmission and reception

Detection priority	Error	Generated interrupt and status
1	PID error	No interrupts are generated in either host or device controller mode (ignored as a corrupted packet)
2	CRC or bit stuffing error	No interrupts are generated in either host or device controller mode (ignored as a corrupted packet)
3	Overrun or underrun error	An NRDY interrupt is generated to set the FRMNUM.OVRN bit to 1 in both host and device controller modes. In device controller mode, a zero-length packet is transmitted in response to an IN token. No data packets are received in response to OUT token.
4	Interval error	An NRDY interrupt is generated in device controller mode. No interrupt is generated in host controller mode.

Table 28.27 Error detection for data packet reception

Detection priority	Error	Generated interrupt and status
1	PID error	No interrupts are generated (ignored as a corrupted packet)
2	CRC or bit stuffing error	An NRDY interrupt is generated and the FRMNUM.CRCE bit sets to 1 in both host and device controller modes
3	Maximum packet size exceeded error	A BEMP interrupt is generated and the PID[1:0] bits set to STALL in both host and device controller modes

28.3.12.1 同步传输中的错误检测

USBFS提供了检测本节所述的错误的功能，以便在同步传输中发生错误时，可以通过软件进行控制。表28.26和表28.27显示了USBFS检测到的错误和相关中断的优先级顺序。

PID错误

●接收报文的PID值无效。

CRC错误和位填充错误

●收到的报文发现CRC错误或比特填充不合法。

超出最大数据包大小

●接收到的数据包的数据大小超过了指定的最大数据包大小。

溢出和欠载错误

在主机控制器模式下：

●在IN（接收）方向发送令牌时，FIFO缓冲区已满

●在OUT（发送）方向的令牌发送时间，FIFO缓冲区中没有要发送的数据

在设备控制器模式下：

●在IN（发送）方向的令牌接收时间，FIFO缓冲区中没有要发送的数据

●在OUT（接收）方向的令牌接收时间，FIFO缓冲区已满

间隔错误

在设备控制器模式下，以下情况被视为间隔错误：

●等时IN传输期间在间隔帧中接收IN令牌失败

●在等时OUT传输期间未能在间隔帧中接收到OUT令牌

Table 28.26 令牌发送和接收的错误检测

检测优先级	Error	产生的中断和状态
1	PID错误	在主机或设备控制器模式下都不会产生中断（被忽略为损坏的数据包）
2	CRC或位填充错误	在主机或设备控制器模式下都不会产生中断（被忽略为损坏的数据包）
3	溢出或欠载错误	在主机和设备控制器模式下，都会产生一个NRDY中断来将FRMNUM.OVRN位设置为1。在设备控制器模式下，发送一个零长度数据包以响应IN令牌。 没有接收到响应OUT令牌的数据包。
4	间隔误差	在设备控制器模式下会产生一个NRDY中断。在主机控制器模式下不产生中断。

Table 28.27 数据包接收错误检测

检测优先级	Error	产生的中断和状态
1	PID错误	不产生中断（作为损坏的数据包被忽略）
2	CRC或位填充错误	在主机和设备控制器模式下都会产生一个NRDY中断并且FRMNUM.CRCE位设置为1
3	超出最大数据包大小错误	在主机和设备控制器模式下都会产生BEMP中断并且PID[1:0]位设置为STALL

28.3.12.2 DATA-PID

In device controller mode, the USBFS responds to a received PID as follows:

(1) IN direction

- DATA0: Transmitted as data packet PID
- DATA1: Not transmitted
- DATA2: Not transmitted
- mDATA: Not transmitted

(2) OUT direction

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Packets ignored
- mDATA: Packets ignored

28.3.12.3 Interval counter

The isochronous transfer interval can be set in the PIPEPERI.IITV[2:0] bits. In device controller mode, the interval counter enables the functions as shown in Table 28.28. In host controller mode, the USBFS generates the token issuance timing, and the interval counter operation is the same as that for interrupt transfers.

Table 28.28 Interval counter functions in device controller mode

Transfer direction	Function	Conditions for detection
IN	Transmit buffer flush	Failure to receive an IN token successfully in the interval frame during an isochronous IN transfer.
OUT	Notification of no reception of token	Failure to receive an OUT token successfully in the interval frame during an isochronous OUT transfer.

The interval count is performed when an SOF is received or for interpolated SOFs, so the isochronism can be maintained even if an SOF is corrupt. The frame interval can be set to 2^{IITV} frames.

(1) Counter initialization in device controller mode

The USBFS initializes the interval counter under the following conditions:

- Power-on reset

  This initializes the PIPEPERI.IITV[2:0] bits.
- FIFO buffer initialization using the ACLRM bit

  This does not initialize the IITV[2:0] bits, but does initialize the count value.

After the interval counter is initialized, the interval count starts under one of the following conditions when a packet is transferred successfully:

- An SOF is received after data is transmitted in response to an IN token when PID = BUF
- An SOF is received after data is received in response to an OUT token when PID = BUF

The interval counter is not initialized in the following conditions:

- When the PID[1:0] bits are set to NAK or STALL

  This does not stop the interval timer. The USBFS attempts the transaction in the next interval.
- When the USB bus is reset or USBFS is suspended

  This does not initialize the IITV[2:0] bits. When an SOF is received, the interval counter starts counting from the value set before SOF was received.

28.3.12.2 DATA-PID

在设备控制器模式下，USBFS响应接收到的PID如下：

(1) 在方向

●DATA0：作为数据包PID发送
●DATA1：未发送
●DATA2：未传输
●mDATA：不传输

(2) 出方向

●DATA0：作为数据包PID正常接收
●DATA1：作为数据包PID正常接收
●DATA2：忽略的数据包
●mDATA：忽略的数据包

28.3.12.3 间隔计数器

同步传输间隔可以在PIPEPERI.IITV[2:0]位中设置。在设备控制器模式下，间隔计数器启用如表28.28所示的功能。在主机控制器模式下，USBFS产生令牌发布时序，间隔计数器操作与中断传输相同。

Table 28.28 设备控制器模式下的间隔计数器功能

转移方向	Function	检测条件
IN	发送缓冲区刷新	在同步IN传输期间未能在间隔帧中成功接收IN令牌。
OUT	未收到令牌的通知	在同步OUT传输期间未能在间隔帧中成功接收OUT令牌。

间隔计数在接收到SOF时执行或对插值SOF执行，因此即使SOF损坏也可以保持等时性。帧间隔可以设置为2个IITV帧。

(1) 设备控制器模式下的计数器初始化

USBFS在以下条件下初始化间隔计数器：

- Power-on reset

  这将初始化PIPEPERI.IITV[2:0]位。
●使用ACLRM位初始化FIFO缓冲区

  这不会初始化IITV[2:0]位，但会初始化计数值。

间隔计数器初始化后，当数据包传输成功时，间隔计数在以下条件之一开始：

●当PID=BUF时，响应IN令牌传输数据后收到SOF
●当PID=BUF时，接收到响应OUT令牌的数据后接收到SOF

间隔计数器在以下情况下不会初始化：

●当PID[1:0]位设置为NAK或STALL时

  这不会停止间隔计时器。USBFS在下一个间隔尝试事务。
●USB总线复位或USBFS挂起时

  这不会初始化IITV[2:0]位。当接收到SOF时，间隔计数器从接收到SOF之前设置的值开始计数。

(2) Interval counting and transfer control in host controller mode

The USBFS controls the interval between token issuance operations based on the PIPEPERI.IITV[2:0] bits settings. Specifically, the USBFS issues a token for a selected pipe once every 2^{IITV} frames.

The USBFS starts counting the token issuance interval at the frame following the frame in which the PID[1:0] bits are set to BUF by software.

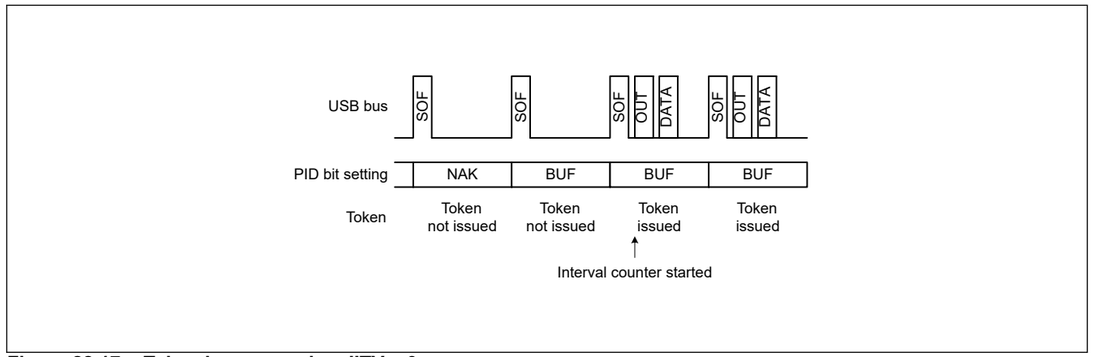


Figure 28.17 Token issuance when IITV = 0

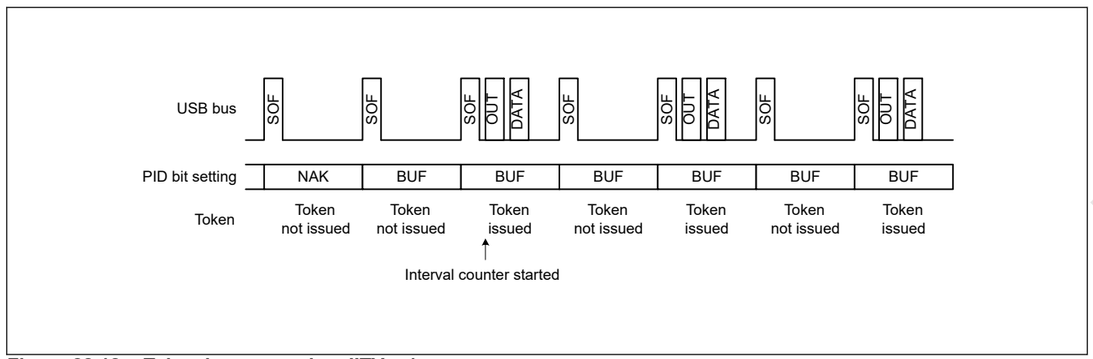


Figure 28.18 Token issuance when IITV = 1

When the selected pipe is set for isochronous transfers, the USBFS performs the following operation in addition to controlling the token issuance interval. The USBFS issues a token even when the NRDY interrupt generation condition is satisfied.

When the selected pipe is for isochronous IN transfers

The USBFS generates an NRDY interrupt when the USBFS issues an IN token but does not successfully receive a packet from a peripheral device (no response or packet error).

The USBFS sets the FRMNUM.OVRN bit to 1, generating an NRDY interrupt, when the time to issue an IN token occurs while the USBFS cannot receive data because the FIFO buffer is full, because the CPU or DMAC/DTC is too slow in reading data from the FIFO buffer.

When the selected pipe is for isochronous OUT transfers

The USBFS sets the OVRN bit to 1, generating an NRDY interrupt and transmitting a zero-length packet, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer, or because the CPU or DMAC/DTC is too slow in writing data to the FIFO buffer.

The token issuance interval is reset on any of the following conditions:

- When the USBFS is reset through a reset pin

  This initializes the IITV[2:0] bits.

(2) 主机控制器模式下的间隔计数和传输控制

USBFS根据PIPEPERI.IITV[2:0]位设置控制令牌发布操作之间的间隔。
具体来说，USBFS每2个IITV帧为所选管道发布一次令牌。

USBFS在PID[1:0]位设置为的帧之后的帧开始计算令牌发布间隔
BUF通过软件。

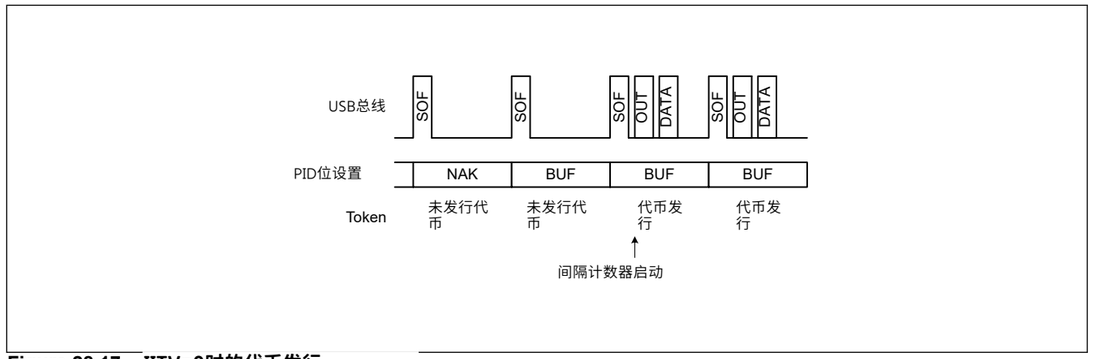


Figure 28.17 IITV=0时的代币发行

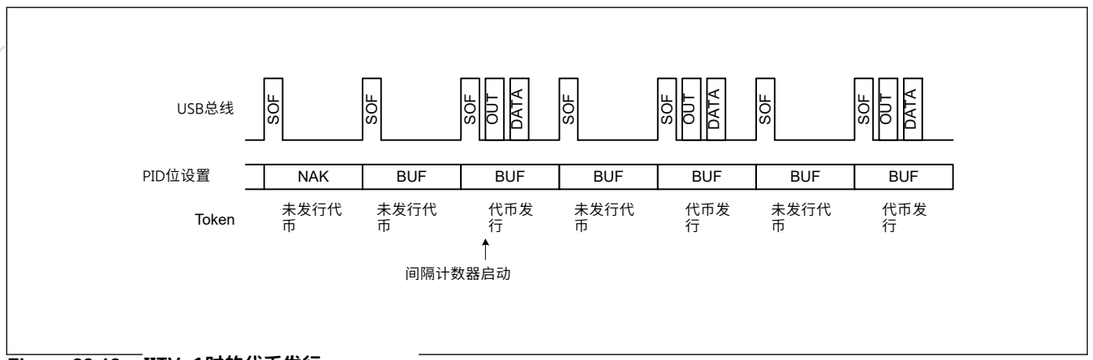


Figure 28.18 IITV=1时的代币发行

当所选管道设置为同步传输时，USBFS除了控制令牌发布间隔外，还执行以下操作。即使满足NRDY中断生成条件，USBFS也会发出令牌。

当所选管道用于同步IN传输时

当USBFS发出IN令牌但未成功接收到来自外围设备的数据包（无响应或数据包错误）时，USBFS会生成NRDY中断。

USBFS将FRMNUM.OVRN位设置为1，产生一个NRDY中断，此时发生发出IN令牌的时间，而USBFS无法接收数据，因为FIFO缓冲区已满，因为CPU或DMACDTC读取数据太慢从FIFO缓冲区。

当所选管道用于同步OUT传输时

USBFS将OVRN位设置为1，产生一个NRDY中断并发送一个长度为零的数据包，当发出OUT令牌的时间到来而FIFO缓冲区中没有要发送的数据时，或者因为CPU或DMACDTC将数据写入FIFO缓冲区太慢。

令牌发行间隔在以下任何条件下重置：

●USBFS通过复位引脚复位时

这将初始化IITV[2:0]位。

- When the PIPEnCTR.ACLRM bit is set to 1 by software

(3) Interval counting and transfer control in device controller mode

When the selected pipe is for isochronous OUT transfers

The USBFS generates an NRDY interrupt when it fails to receive a data packet within the interval set in the PIPEPERI.IITV[2:0] bits.

The USBFS also generates an NRDY interrupt when it fails to receive data because of a CRC error or other errors contained in the data packet or because the FIFO buffer is full.

The NRDY interrupt is generated on SOF packet reception. Even if the SOF packet is corrupted, internal interpolation allows the interrupt to be generated when the SOF packet is received. However, when the IITV bits are set to a value other than 0, the USBFS generates an NRDY interrupt on receiving an SOF packet for every interval after interval counting starts.

When the PID[1:0] bits are set to NAK by software after starting the interval timer, the USBFS does not generate an NRDY interrupt on receiving an SOF packet.

The timing for starting interval counting depend on the IITV[2:0] setting as follows:

- When the IITV[2:0] bits = 0:

  Interval counting starts at the next frame after the software changes the PID[1:0] bits of the selected pipe to BUF.

- When the IITV[2:0] bits ≠ 0:

  Interval counting starts on completion of successful reception of the first data packet after the PID[1:0] bits for the selected pipe are changed to BUF.

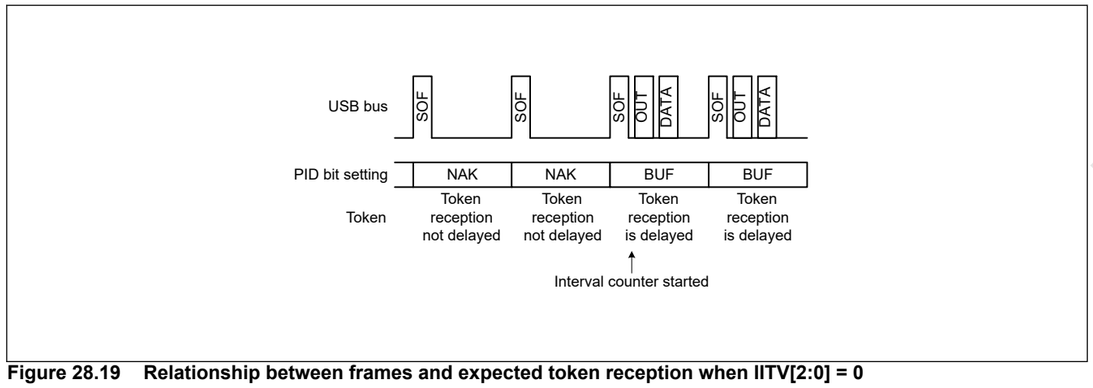


Figure 28.19 Relationship between frames and expected token reception when IITV[2:0] = 0

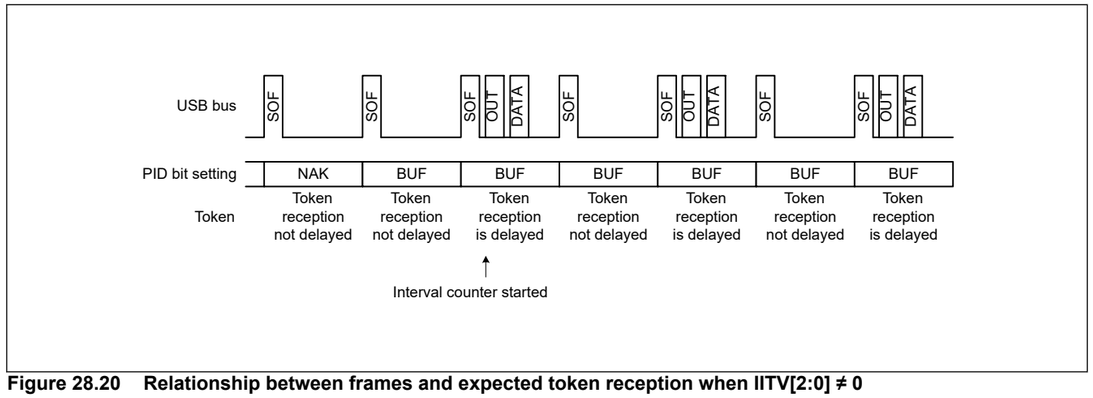


Figure 28.20 Relationship between frames and expected token reception when IITV[2:0] ≠ 0

●PIPEnCTR.ACLRM位由软件设置为1时

(3) 设备控制器模式下的间隔计数和传输控制

当所选管道用于同步OUT传输时

当USBFS在设置的时间间隔内没有接收到数据包时，会产生一个NRDY中断。
PIPEPERI.IITV[2:0] bits.

当由于数据包中包含的CRC错误或其他错误或FIFO缓冲区已满而无法接收数据时，USBFS也会产生NRDY中断。

NRDY中断在SOF数据包接收时产生。即使SOF数据包损坏，内部插值也允许在接收到SOF数据包时产生中断。但是，当IITV位设置为0以外的值时，USBFS会在间隔计数开始后的每个间隔接收到SOF数据包时产生NRDY中断。

当PID[1:0]位在启动间隔定时器后被软件设置为NAK时，USBFS在接收到SOF数据包时不会产生NRDY中断。

开始间隔计数的时间取决于IITV[2:0]设置，如下所示：

●当IITV[2:0]位=0时：

软件将所选管道的PID[1:0]位更改为BUF后，间隔计数从下一帧开始。

●当IITV[2:0]位≠0时：

在所选管道的PID[1:0]位更改为BUF后，成功接收第一个数据包后，间隔计数开始。

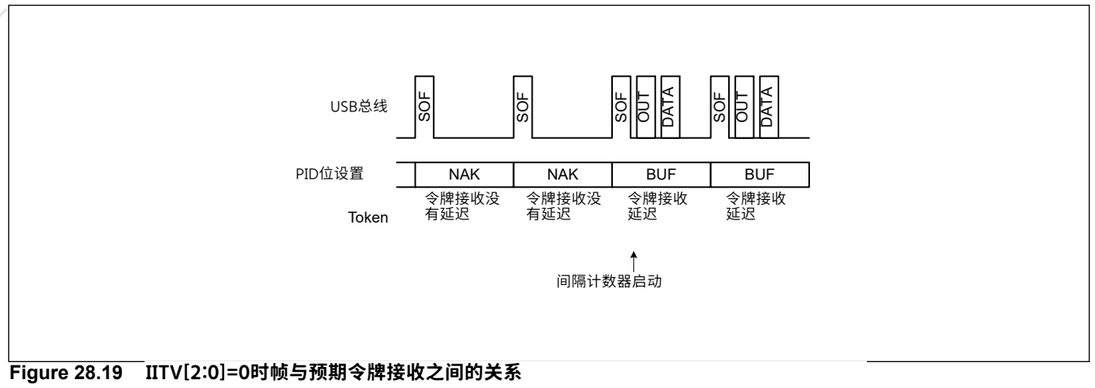


Figure 28.19 IITV[2:0]=0时帧与预期令牌接收之间的关系

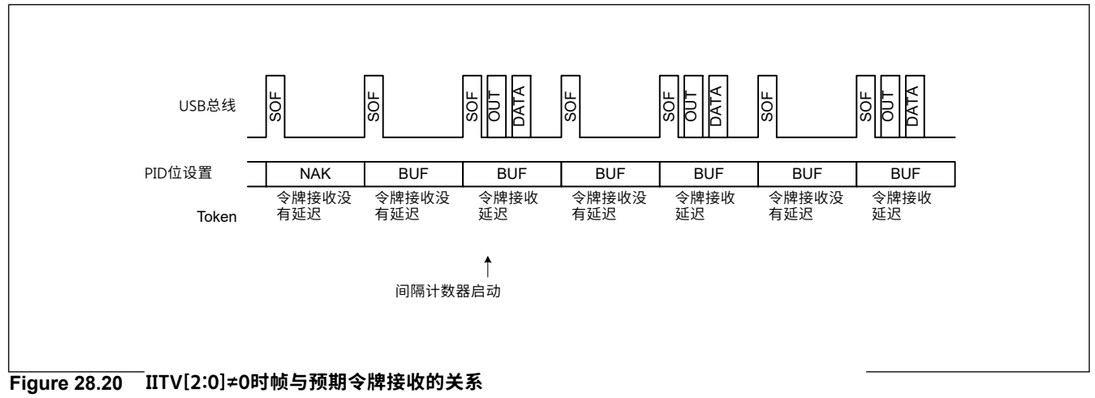


Figure 28.20 IITV[2:0]≠0时帧与预期令牌接收的关系

When the selected pipe is for isochronous IN transfers

The PIPEPERI.IFIS bit must be 1 for this use case. When IFIS = 0, the USBFS transmits a data packet in response to a received IN token regardless of the PIPEPERI.IITV[2:0] setting.

When IFIS is 1 and there is data to be transmitted in the FIFO buffer, the USBFS clears the FIFO buffer when it fails to receive an IN token in the frame at the interval set in the IITV[2:0] bits.

The USBFS also clears the FIFO buffer when it fails to receive an IN token successfully because of a bus error, such as a CRC error, contained in the IN token.

The FIFO buffer is cleared on SOF packet reception. Even if the SOF packet is corrupted, the internal interpolation allows the FIFO buffer to be cleared when the SOF packet is received.

The timing to start interval counting depends on the IITV[2:0] setting, as with OUT transfers.

The interval is counted on any of the following conditions in device controller mode:

- When a hardware reset is applied to the USBFS (which also sets the IITV[2:0] bits to 000b)
- When the PIPEnCTR.ACLRM bit is set to 1 by software
- When the USBFS detects a USB bus reset

(4) Transmit data setup for isochronous transfers in device controller mode

With isochronous data transmission using the USBFS in device controller mode, after data is written to the FIFO buffer, a data packet can be transmitted in the first frame after the SOF packet is detected. This isochronous transfer transmit data setup function can identify the frame that started transmission.

When the double buffering is used, transmission is only enabled for the buffer where data writing was completed first, even after the data write to both buffers is complete. Accordingly, even if multiple IN tokens are received, only the one packet of FIFO buffer data is transmitted.

When the FIFO buffer is ready to transmit data when an IN token is received, the data is transferred and a normal response is returned. However, if the FIFO buffer cannot transmit data, a zero-length packet is transmitted and an underrun error occurs.

Figure 28.21 shows an example transmission using the isochronous transfer transmission data setup function when IITV = 0 (every frame) is set.

当所选管道用于同步IN传输时

对于此用例，PIPEPERI.IFIS位必须为1。当IFIS=0时，无论PIPEPERI.IITV[2:0]设置如何，USBFS都会发送一个数据包以响应接收到的IN令牌。

当IFIS为1且FIFO缓冲区中有数据要发送时，如果USBFS在IITV[2:0]位设置的时间间隔内未能接收到帧中的IN令牌，则清除FIFO缓冲区。

当USBFS由于总线错误（例如
CRC错误，包含在IN令牌中。

FIFO缓冲区在SOF数据包接收时被清除。即使SOF数据包损坏，内部插值也允许在接收到SOF数据包时清除FIFO缓冲区。

开始间隔计数的时间取决于IITV[2:0]设置，与OUT传输一样。

在设备控制器模式下，根据以下任何条件计算间隔：

- 当对USBFS应用硬件复位时（也将IITV[2:0]位设置为000b）
- PIPEnCTR.ACLRM位由软件设置为1时
- 当USBFS检测到USB总线复位时

(4) 设备控制器模式下同步传输的传输数据设置

在设备控制器模式下使用USBFS进行同步数据传输，数据写入FIFO缓冲区后，可在检测到SOF包后的第一帧发送数据包。此同步传输传输数据设置功能可以识别开始传输的帧。

使用双缓冲时，仅对先完成数据写入的缓冲区启用传输，即使在两个缓冲区的数据写入完成后也是如此。因此，即使接收到多个IN令牌，也仅发送一包FIFO缓冲器数据。

当接收到IN令牌时，当FIFO缓冲区准备好传输数据时，将传输数据并返回正常响应。但是，如果FIFO缓冲区无法传输数据，则会传输零长度数据包并发生欠载错误。

图28.21显示了在设置IITV=0（每帧）时使用同步传输传输数据设置功能的示例传输。

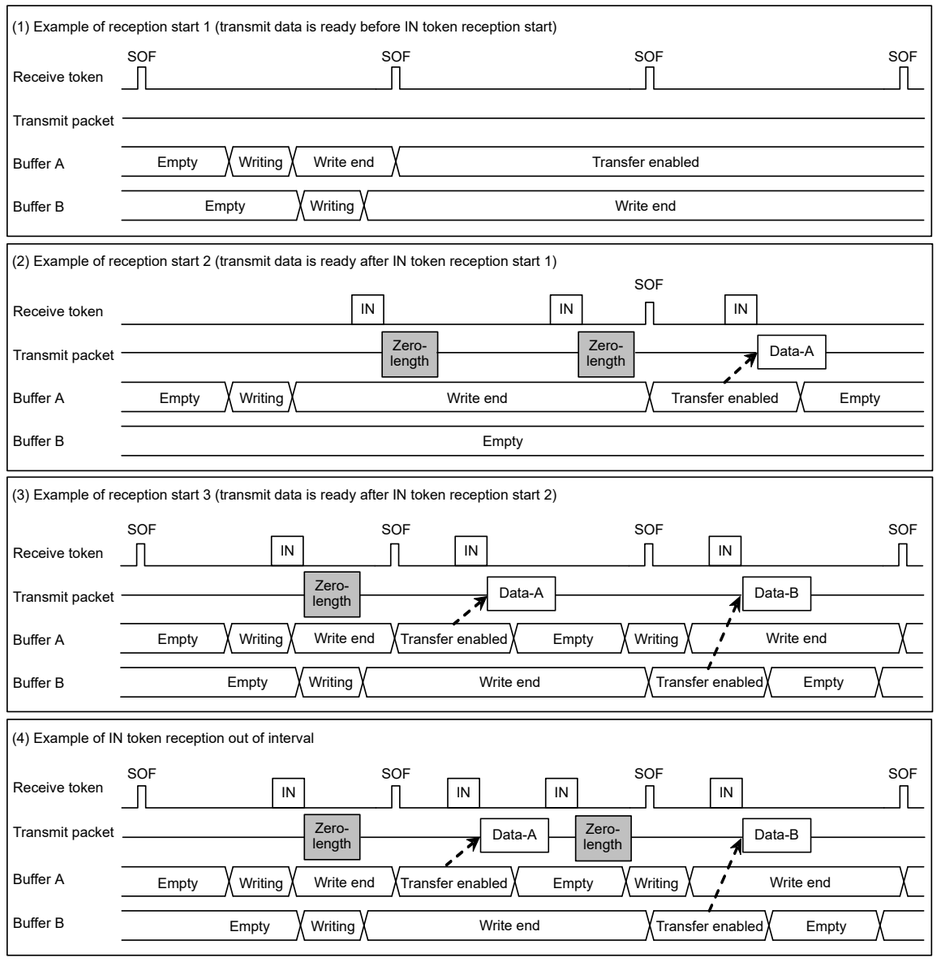


Figure 28.21 Example data setup operation

(5) Transmit buffer flush for isochronous transfers in device controller mode

In device controller mode during isochronous data transmission, if the USBFS receives an SOF packet for the next frame without receiving an IN token in the interval frame, it operates as if the IN token is corrupt and clears the buffer that is enabled for transmission, putting that buffer in the writing enabled state.

When double buffering is used and writing to both buffers is complete, the cleared FIFO buffer is assumed to be the one where the data was transmitted in the interval frame, and transmission is enabled for the FIFO buffer that was not cleared on SOF packet reception.

The timing of the buffer flush function depends on the PIPEPERI.IITV[2:0] setting as follows:

- When IITV = 0:

  The buffer flush operation starts from the first frame after the pipe is enabled.
- When IITV ≠ 0:

  The buffer flush operation starts after the first normal transaction.

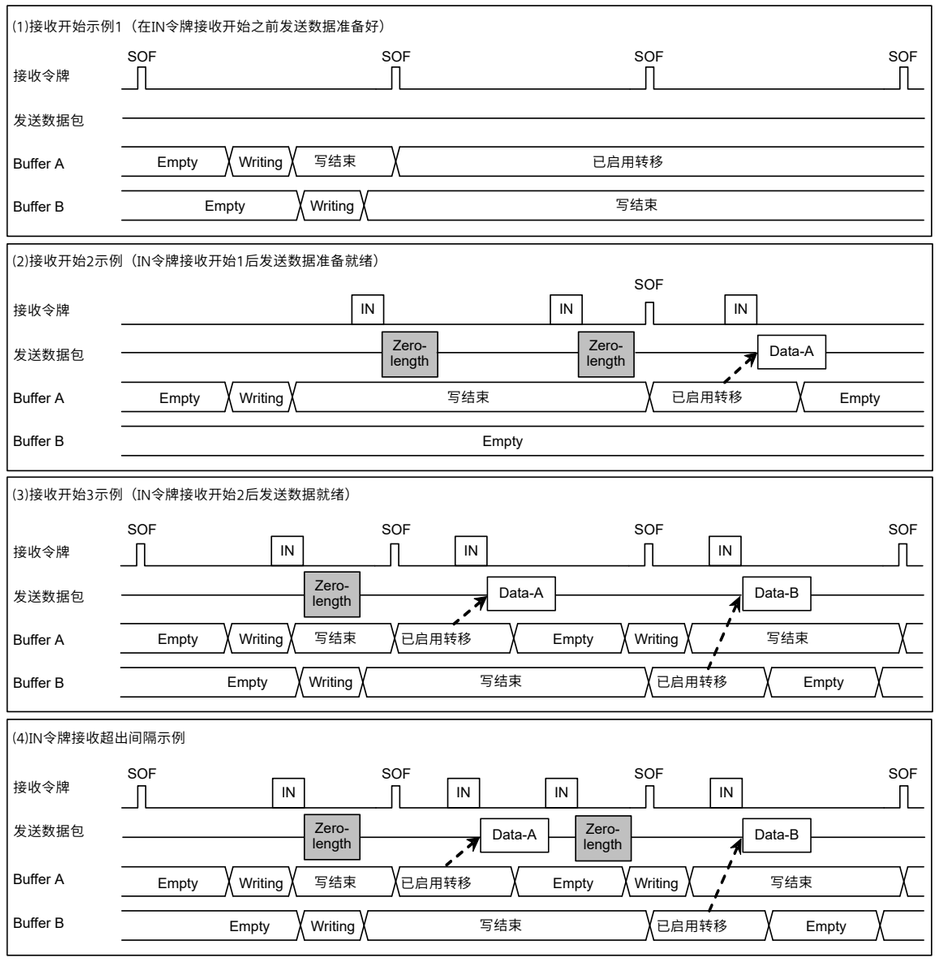


Figure 28.21 示例数据设置操作

(5) 设备控制器模式下同步传输的传输缓冲区刷新

在同步数据传输期间的设备控制器模式下，如果USBFS接收到下一帧的SOF数据包，而在间隔帧中没有接收到IN令牌，则它会像IN令牌损坏一样操作并清除启用传输的缓冲区，将该缓冲区处于写入启用状态。

当使用双缓冲并完成对两个缓冲区的写入时，已清除的FIFO缓冲区被假定为在间隔帧中传输数据的缓冲区，并为接收SOF数据包时未清除的FIFO缓冲区启用传输。

缓冲区刷新功能的时间取决于PIPEPERI.IITV[2:0]设置，如下所示：

- When IITV = 0:

  缓冲区刷新操作从启用管道后的第一帧开始。
- When IITV ≠ 0:

  缓冲区刷新操作在第一个正常事务之后开始。

Figure 28.22 shows an example buffer flush. When an unanticipated token is received before the interval frame, the USBFS sends the write data or a zero-length packet as an underrun error, depending on the data setup status.

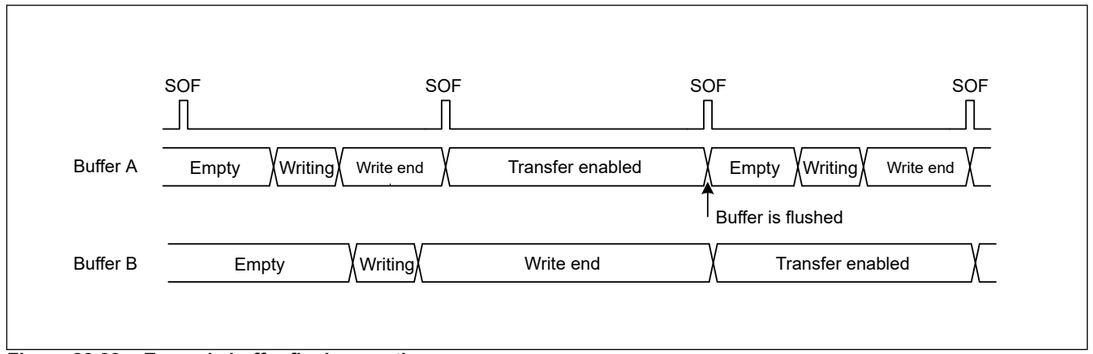


Figure 28.22 Example buffer flush operation

Figure 28.23 shows an example interval error occurrence. There are five types of interval errors, as shown in the figure. An interval error occurs at timing (A), and the buffer flush function is activated.

If an interval error occurs during an IN transfer, the buffer flush function is activated. If it occurs during an OUT transfer, an NRDY interrupt is generated. Use the FRMNUM.OVRN bit to distinguish between this and NRDY interrupts triggered by received packet errors and overrun errors.

For tokens that are shaded in the figure, responses are returned based on the FIFO buffer status.

- IN direction:
  - If the buffer is ready to transfer data, the data is transferred and a normal response is returned
  - If the buffer is not ready to transfer data, a zero-length packet is transmitted and an underrun error occurs
- OUT direction:
  - If the buffer is ready to receive data, the data is received and a normal response is returned
  - If the buffer is not ready to receive data, the received data is discarded and an overrun error occurs

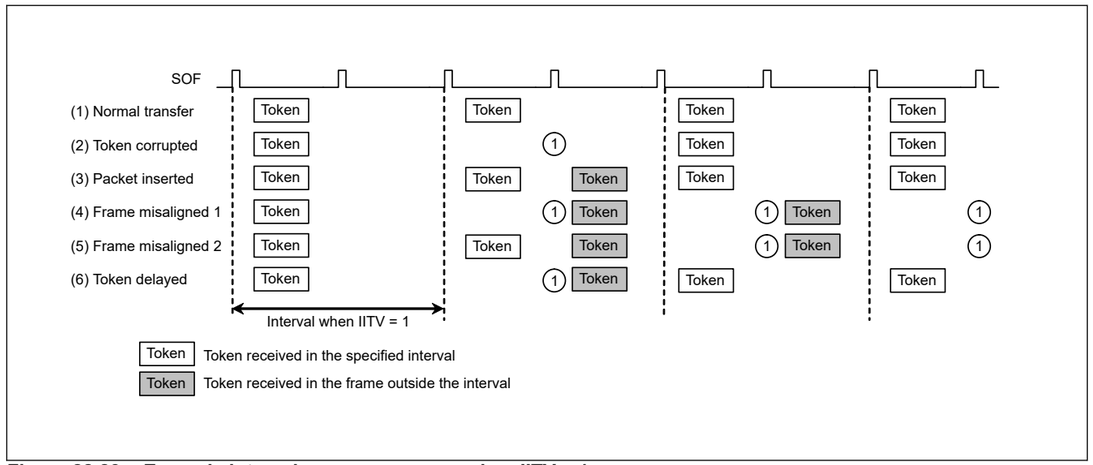


Figure 28.23 Example interval error occurrence when IITV = 1

28.3.13 SOF Interpolation Function

In device controller mode, if packet reception is disabled at intervals of 1 ms because the SOF packet is corrupted or missing, the USBFS interpolates the SOF. SOF interpolation begins when the USBE and SCKE bits in SYSCFG are set to 1 and an SOF packet is received.

图28.22显示了一个示例缓冲区刷新。当在间隔帧之前接收到意外令牌时，USBFS将根据数据设置状态发送写数据或零长度数据包作为欠载错误。

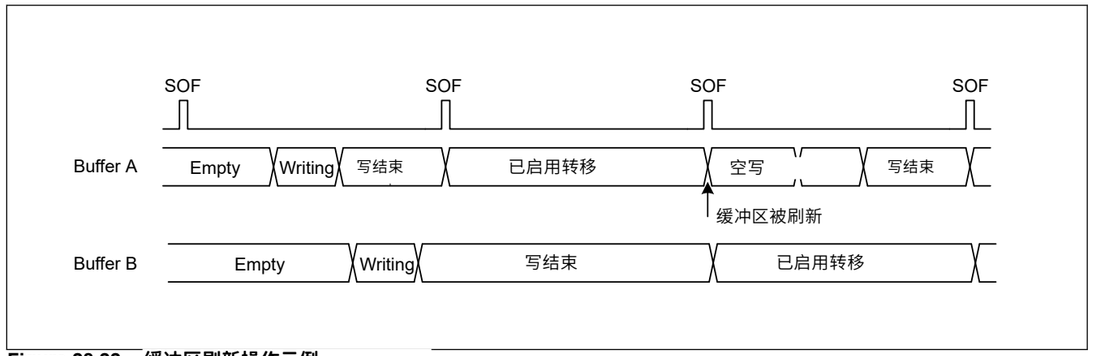


Figure 28.22 缓冲区刷新操作示例

图28.23显示了一个发生间隔错误的示例。如图所示，有五种区间误差。在时间（A）发生间隔错误，缓冲刷新功能被激活。

如果在IN传输期间发生间隔错误，则会激活缓冲区刷新功能。如果它发生在OUT传输期间，则NRDY中断产生。使用FRMNUM.OVRN位来区分此中断和由接收数据包错误和溢出错误触发的NRDY中断。

对于图中带阴影的令牌，根据FIFO缓冲区状态返回响应。

- IN direction:
  如果缓冲区准备好传输数据，则传输数据并返回正常响应
  如果缓冲区未准备好传输数据，则传输零长度数据包并发生欠载错误
- OUT direction:
  如果缓冲区准备好接收数据，则接收数据并返回正常响应
  如果缓冲区没有准备好接收数据，则丢弃接收到的数据并发生溢出错误

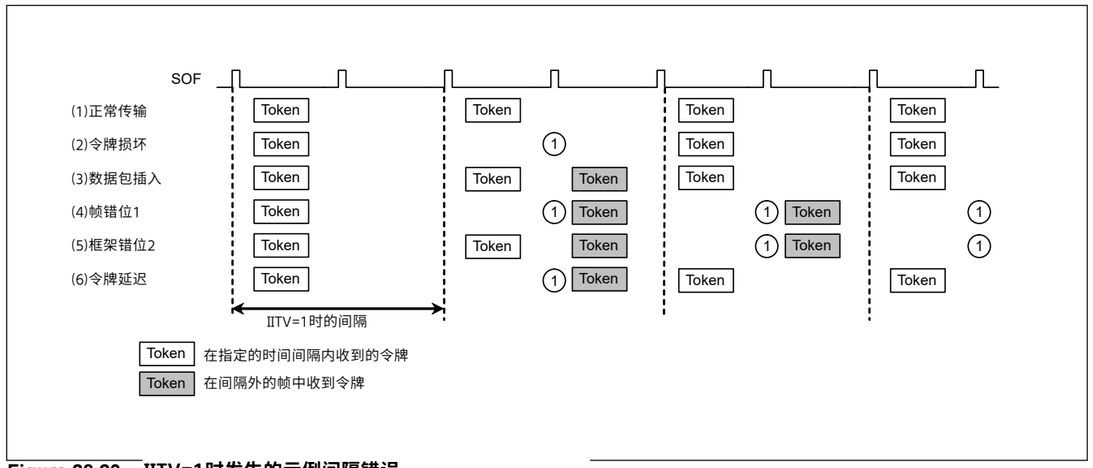


Figure 28.23 IITV=1时发生的示例间隔错误

28.3.13 SOF插值函数

在设备控制器模式下，如果由于SOF数据包损坏或丢失而每隔1ms禁用数据包接收，则USBFS会内插SOF。当SYSCFG中的USBE和SCKE位设置为1并且接收到SOF数据包时，SOF内插开始。

The interpolation function is initialized under the following conditions:

- MCU reset
- USB bus reset
- Suspend state detection

The SOF interpolation operates as follows:

- The interpolation function is not activated until an SOF packet is received
- When the first SOF packet is received, interpolation is performed by counting 1 ms on the 48-MHz internal clock
- When the second and subsequent SOF packets are received, interpolation is performed at the previous reception interval
- Interpolation is not performed in the Suspend state or on reception of a USB bus reset

The USBFS supports the following functions controlled by SOF packet reception. These functions operate normally with SOF interpolation if the SOF packet is missing:

- Updating of the frame number
- SOFR interrupt timing
- Isochronous transfer interval count

If an SOF packet is missing during full-speed operation, the FRMNUM.FRNM[10:0] bits are not updated.

28.3.14 Pipe Schedule

28.3.14.1 Conditions for generating transactions

In host controller mode and when the DVSTCTR0.UACT bit is set to 1, the USBFS generates transactions under the conditions shown in Table 28.29.

Table 28.29 Conditions for generating transactions

Transaction	Conditions for generation				
	DIR	PID	IITV0	Buffer state	SUREQ
Setup	—*1	—*1	—*1	—*1	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	Invalid	Receive area exists	—*1
	OUT	BUF	Invalid	Transmit data exists	—*1
Interrupt transfer	IN	BUF	Valid	Receive area exists	—*1
	OUT	BUF	Valid	Transmit data exists	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. An em dash (—) in the table indicates that the condition is unrelated to the generating of tokens. “Valid” indicates that, for interrupt transfers and isochronous transfers, a transaction is generated only in transfer frames that are based on the interval counter. “Invalid” indicates that a transaction is generated regardless of the interval counter.
Note 2. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.
Note 3. This indicates that a transaction is generated regardless of whether there is any data to be transmitted. If there is no data to be transmitted, however, a zero-length packet is transmitted.

28.3.14.2 Transfer schedule

This section describes the transfer scheduling within a frame of the USBFS. After the USBFS sends an SOF, the transfer is carried out in the following sequence:

1. Execution of periodic transfers:

插值函数在以下条件下初始化：

- MCU reset
- ●USB总线复位
- ●暂停状态检测

SOF插值操作如下：

- ●直到收到SOF数据包才激活插值功能
- ●当接收到第一个SOF数据包时，通过在48-MHz内部时钟上计数1ms执行插值
- ●当接收到第二个和后续的SOF数据包时，按照之前的接收间隔进行插值
- ●在挂起状态或接收到USB总线复位时不执行插值

USBFS支持以下由SOF数据包接收控制的功能。这些功能正常运行
如果SOF数据包丢失，则SOF插值：

- ●更新帧号
- ●SOFR中断时序
- ●同步传输间隔计数

如果在全速运行期间丢失SOF数据包，则不会更新FRMNUM.FRNM[10:0]位。

28.3.14 管道计划

28.3.14.1 产生交易的条件

在主机控制器模式下，当DVSTCTR0.UACT位设置为1时，USBFS在表28.29所示的条件下生成事务。

Table 28.29 产生交易的条件

Transaction	生成条件				
	DIR	PID	IITV0	缓冲状态	SUREQ
Setup	—*1	—*1	—*1	—*1	1 setting
控制传输数据阶段、状态阶段、批量传输	IN	BUF	Invalid	接收区存在	—*1
	OUT	BUF	Invalid	传输数据存在	—*1
中断传输	IN	BUF	Valid	接收区存在	—*1
	OUT	BUF	Valid	传输数据存在	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

注1.表中的破折号(—)表示该条件与令牌的生成无关。“有效”表示，对于中断传输和同步传输，事务仅在基于间隔计数器的传输帧中生成。“无效”表示无论间隔计数器如何都生成事务。

注2.这表示无论是否有接收区域，都会生成一个事务。但是，如果没有接收区域，则丢弃接收到的数据。

注3.这表示无论是否有任何数据要传输，都会产生交易。然而，如果没有要传输的数据，则传输零长度数据包。

28.3.14.2 转移时间表

本节介绍USBFS帧内的传输调度。USBFS发送SOF后，按以下顺序进行传输：

1.定期转账的执行：

A pipe is searched for in the order of pipe 1 → pipe 2 → pipe 6 → pipe 7 → pipe 8 → pipe 9, and then if there is a pipe for which an isochronous or interrupt transfer transaction can be generated, the transaction is generated.

2. Setup transactions for control transfers:

   The DCP is checked, and if a setup transaction is possible, it is sent.

3. Execution of bulk transfers, control transfer data stages, and control transfer status stages:

   A pipe is searched for in the order of DCP → pipe 1 → pipe 2 → pipe 3 → pipe 4 → pipe 5, and then if there is a pipe for which a transaction for a bulk transfer, a control transfer data stage, or a control transfer status stage can be generated, the transaction is generated.

   When a transaction is generated, processing moves to the next pipe transaction regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, step 3 is repeated.

28.3.14.3 Enabling USB communication

Setting the DVSTCTR0.UACT bit to 1 initiates an SOF transmission, and transaction generation is enabled. Setting the UACT bit to 0 stops SOF transmission and the Suspend state is invoked. If the UACT setting is changed from 1 to 0, processing stops after the next SOF is sent.

28.3.15 Battery Charging Detection Processing

The USBFS provides control over the data contact detection processing (D+ line contact checking), primary detection processing (charger detection processing), and secondary detection processing (charger determination processing) as defined in the Battery Charging Specification.

28.3.15.1 Processing in device controller mode

To operate a function device as a battery charging portable device:

1. Start primary detection processing after detecting contact with the D+ and D- lines. The Battery Charging Specification describes two processing methods for Data Contact Detection. The USBFS supports both methods as follows:

   - Software processing

     After a VBINT interrupt or polling of the VBSTS flag indicates a change in the state of the USBFS_VBUS input pin, software controls a wait from 300 to 900 ms. The BCCTRL1.VDPSRCE and CHGDETE bits are then both set to 1 to start primary detection processing.

   - Hardware Processing

     Apply 7 to 13 µA of current to the D+ line to hold the D+ line at the logical high level. This is done to detect the D+ and D- lines going to the logical low level because of pull-down resistors on the host device side when the D+ and D- lines come in contact with those of the host. Monitor the SYSSTS0.LNST[1:0] flags while the PHYSECTRL.CNEN bit, BCCTRL1.RPDME and IDPSRCE bit are set to 1 to see when the level on the D+ line changes from high to low. After detecting a low level on the D+ line, clear the PHYSECTRL.CNEN bit, BCCTRL1.RPDME and IDPSRCE bit to 0 and set both the BCCTRL1.VDPSRCE and CHGDETE bits to 1 to start primary detection processing. The VDPSRCE and CHGDETE bits must be set to 1 simultaneously.

2. After the start of primary detection processing followed by a software-controlled wait of 40 ms, check the BCCTRL1.CHGDETSTS flag. A value of 1 indicates detection of a charger, and secondary detection processing starts.*1

3. To start secondary detection processing, clear the BCCTRL1.VDPSRCE bit to 0, then clear the BCCTRL1.CHGDETE bits to 0 after a software-controlled wait of 20 ms. Next, set both the BCCTRL1.VDMSRCE and PDDETE bits to 1.

4. After the start of secondary detection processing followed by a software-controlled wait of 40 ms, check the BCCTRL1.PDDETSTS flag, and determine the result of the secondary detection processing.

Note 1. In primary detection processing, detection of a voltage above the range from 0.25 to 0.4 V and below the range from 0.8 to 2.0 V on the D-Line indicates that the other device is a host device that supports battery charging (charging downstream port). The BCCTRL1.CHGDETSTS flag in the PHY block only indicates whether the voltage on the D- line is higher than the range from 0.25 to 0.4 V, so add processing as required to read the SYSSTS0.LNST[1:0] flags and confirm that the voltage on the D- line is also below the range from 0.8 to 2.0 V.

Figure 28.24 shows the process flow.

按照管道1→管道2→管道6→管道7→管道8→管道9的顺序查找管道，如果有管道可以生成等时或中断传输事务，则生成事务.

2.为控制转移设置交易：

DCP被检查，如果设置事务是可能的，它被发送。

3、批量传输、控制传输数据阶段、控制传输状态阶段的执行：

按照DCP→管道1→管道2→管道3→管道4→管道5的顺序搜索管道，然后如果有管道需要进行批量传输、控制传输数据阶段或可以生成控制转移状态阶段，生成事务。

生成事务时，无论来自外围设备的响应是ACK还是NAK，处理都会转移到下一个管道事务。如果帧内有时间进行传输，则重复步骤3。

28.3.14.3 启用USB通信

将DVSTCR0.UACT位设置为1启动SOF传输，并启用事务生成。设置
UACT位为0停止SOF传输并调用暂停状态。如果UACT设置从1更改为0，则在发送下一个SOF后处理停止。

28.3.15 电池充电检测处理

USBFS提供对电池充电规范中定义的数据接触检测处理（D+线路接触检查）、一次检测处理（充电器检测处理）和二次检测处理（充电器确定处理）的控制。

28.3.15.1 设备控制器模式下的处理

将功能设备作为电池充电便携式设备操作：

1.检测到与D+和Dlines的接触后开始初级检测处理。电池充电规范描述了数据接触检测的两种处理方法。USBFS支持以下两种方法：

●软件处理

在VBINT中断或VBSTS标志的轮询指示USBFS_VBUS输入引脚的状态发生变化后，软件控制从300到900ms的等待。然后将BCCTRL1.VDPSRCE和CHGDETE位都设置为1以启动主要检测处理。

●硬件处理

向D+线施加7到13µA的电流，以将D+线保持在逻辑高电平。这样做是为了检测D+和Dlines进入逻辑低电平，因为当D+和Dlines与主机的那些接触时，由于主机设备侧的下拉电阻器。在PHYSECTRL.CNEN位、BCCTRL1.RPDME和IDPSRCE位设置为1时监控SYSSTS0.LNST[1:0]标志，以查看D+线上的电平何时从高变为低。检测到D+线上的低电平后，将PHYSECTRL.CNEN位、BCCTRL1.RPDME和IDPSRCE位清除为0，并将BCCTRL1.VDPSRCE和CHGDETE位都设置为1，以启动初级检测处理。VDPSRCE和CHGDETE位必须同时设置为1。

2.主要检测处理开始后，软件控制等待40毫秒后，检查
BCCTRL1.CHGDETSTS标志。值为1表示检测到充电器，并开始二次检测处理。*1

3.要启动二次检测处理，将BCCTRL1.VDPSRCE位清零，然后在软件控制的20ms等待后将BCCTRL1.CHGDETE位清零。接下来，将BCCTRL1.VDMSRCE和PDDETE位都设置为1。

4.二次检测处理开始后，软件控制等待40ms，检查BCCTRL1.PDDETSTS标志，确定二次检测处理的结果。

注1.在初级检测处理中，在D-Line上检测到高于0.25至0.4V范围且低于0.8至2.0V范围的电压表示其他设备是支持电池充电的主机设备（充电下游港口）。PHY模块中的BCCTRL1.CHGDETSTS标志位仅指示Dline上的电压是否高于0.25到0.4V的范围，因此根据需要添加处理以读取SYSSTS0.LNST[1:0]标志位并确认电压Dline上的电压也低于0.8至2.0V的范围。

图28.24显示了处理流程。

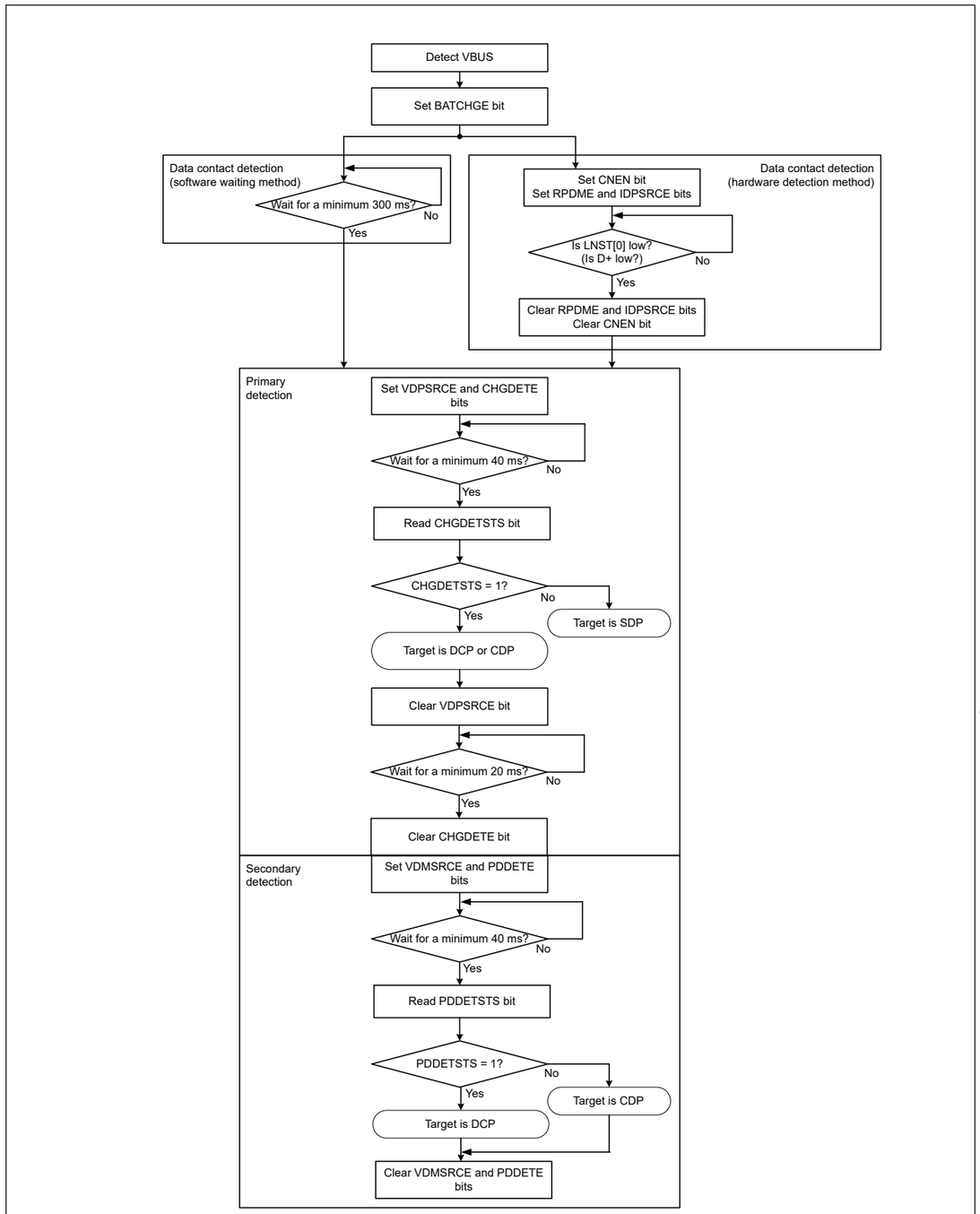


Figure 28.24 Processing flow as portable device

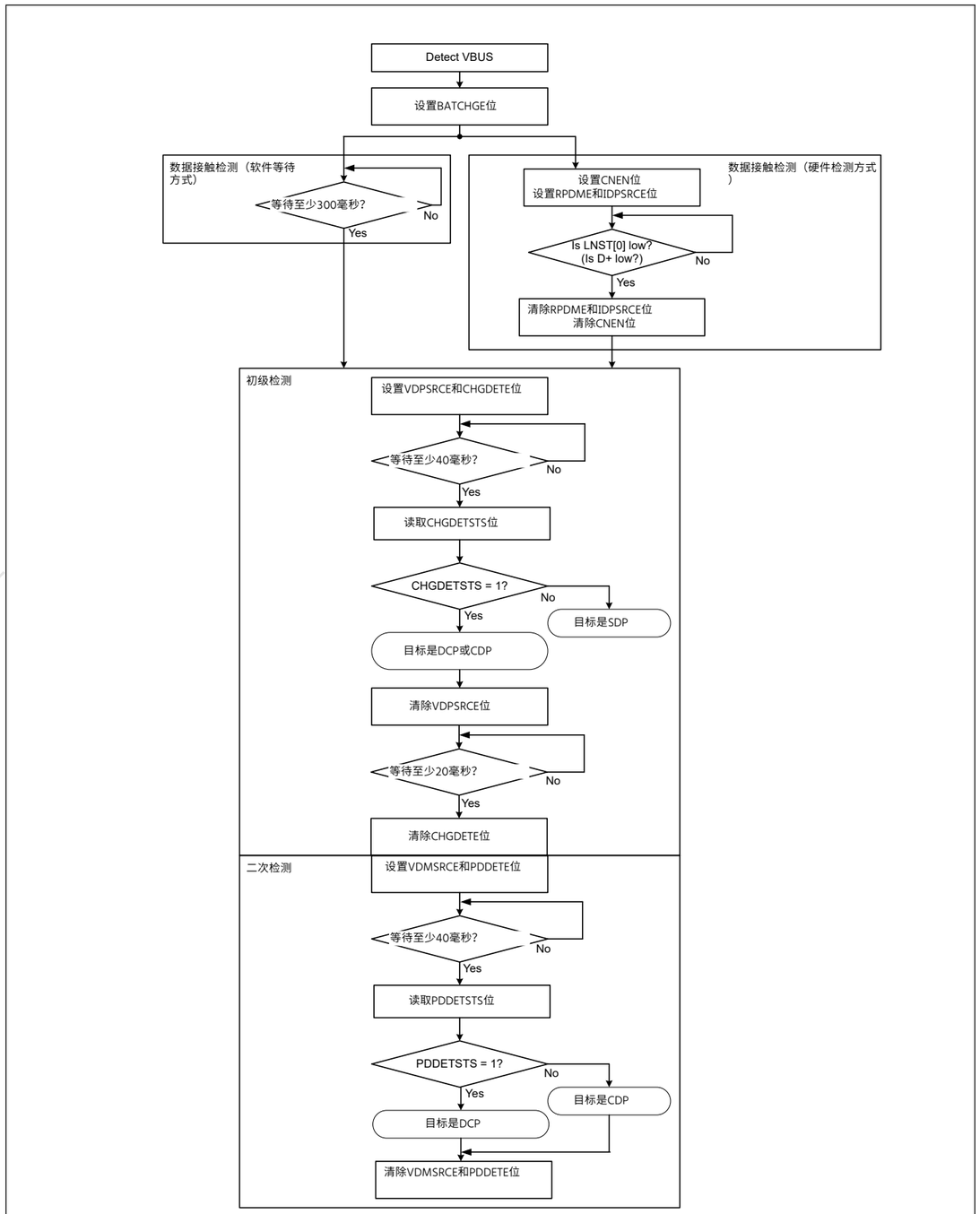


Figure 28.24 作为便携式设备的处理流程

28.3.15.2 Processing in host controller mode

In host controller mode, driving the D- line is required for a portable device to perform primary detection. The USBFS supports the following two primary detection methods:

When using the Portable Device detection function

The D- line is driven when a Portable Device is detected.

1. Start driving the VBUS.
2. Set the BCCTRL1.PDDETE bit to 1 to enable the portable device detection circuit.
3. Monitor the portable device detection signal and start driving the D- line when the level of the portable device detection signal is high.*1
4. Stop driving the D- line when the portable device detection signal is at the low level.*1

Note 1. The PDDETINT interrupt indicates a change in the level of the portable device detection signal, and the current level can be obtained by reading the PDDETSTS flag.

When not using the Portable Device detection function

Regardless of whether or not a Portable Device was detected, drive the D- line after device disconnection is detected, and leave the D- line open after connection is detected. Software handles the timing of a and b.

a. After disconnection is detected, start driving the D- line within 200 ms.

b. After connection is detected, stop driving the D- line within 10 ms.

Figure 28.25 shows the process flow for steps 1. to 4. and Figure 28.26 shows the process flow for steps a. and b., respectively.

28.3.15.2 主机控制器模式下的处理

在主机控制器模式下，便携式设备需要驱动Dline才能执行初级检测。USBFS支持以下两种主要检测方法：

使用便携式设备检测功能时

当检测到便携式设备时驱动Dline。

1.开始驱动VBUS。

2.将BCCTRL1.PDDETE位设置为1以启用便携式设备检测电路。

3.监测便携设备检测信号，当便携设备检测信号为高电平时开始驱动Dline。*1

4、当便携设备检测信号为低电平时，停止驱动Dline。*1

注1.PDDETINT中断表示便携式设备检测信号电平的变化，当前电平可通过读取PDDETSTS标志获得。

不使用便携设备检测功能时

无论是否检测到便携式设备，在检测到设备断开后驱动Dline，在检测到连接后保持Dline处于打开状态。软件处理a和b的时序。

a. 检测到断线后，在200ms内开始驱动Dline。

湾。检测到连接后，请在10ms内停止驱动Dline。

图28.25显示了步骤1.至4.的处理流程，图28.26显示了步骤a的处理流程。和b.，分别。

RA生态工作室

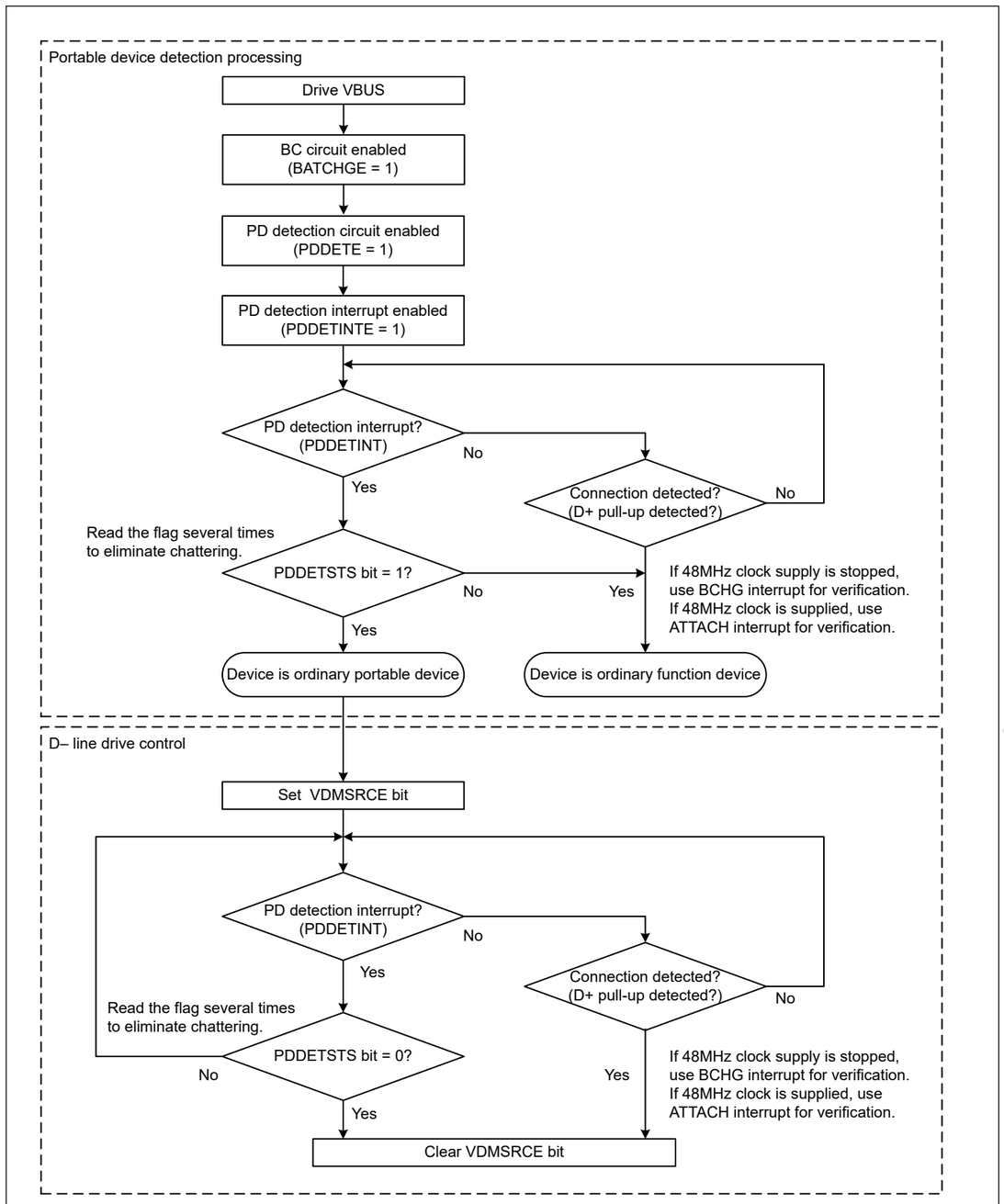


Figure 28.25 Processing flow when using the Portable Device detection function (steps 1. to 4.)

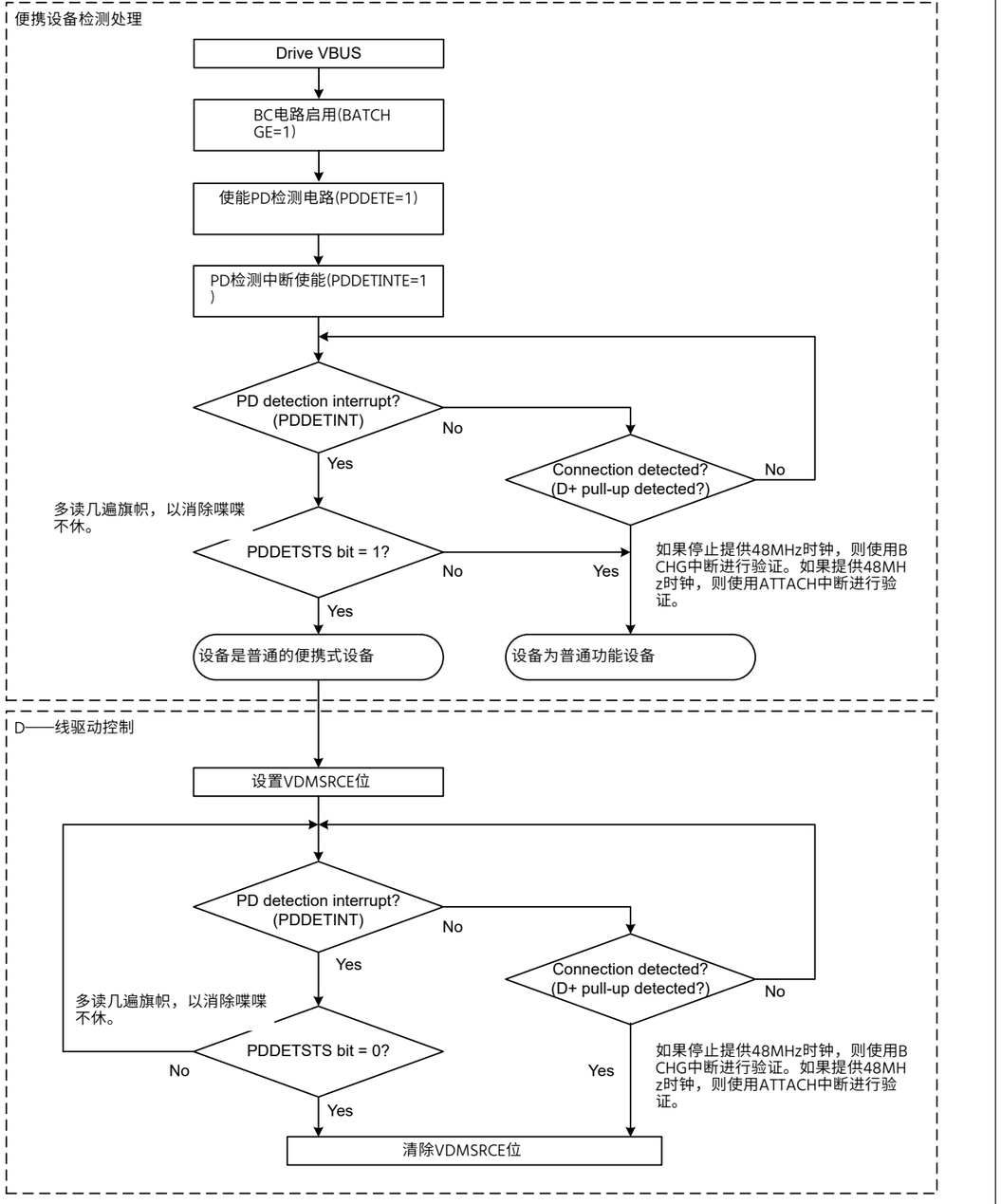


Figure 28.25 使用便携式设备检测功能时的处理流程（步骤1.至4.）

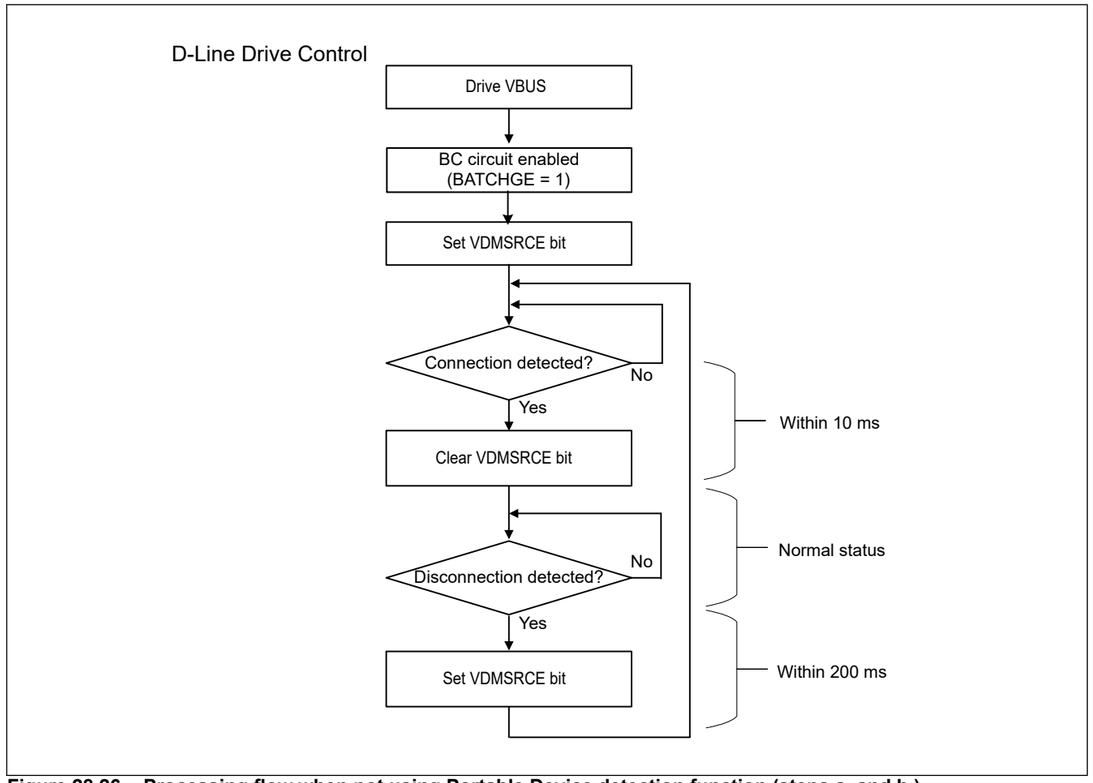


Figure 28.26 Processing flow when not using Portable Device detection function (steps a. and b.)

28.4 Usage Notes

28.4.1 Settings for the Module-Stop State

USBFS operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The USBFS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

28.4.2 Clearing the Interrupt Status Register on Exiting Software Standby Mode

Because the input buffer is always enabled in Software Standby mode, an unexpected interrupt might occur under the following conditions:

- When the interrupt is enabled in Normal mode
- When the interrupt is disabled in Software Standby mode
- When the input level of the pin that cancels software standby is changed in Software Standby mode

These conditions might cause the associated interrupt flag in the Interrupt Status Register to set unexpectedly. After the MCU exits the Software Standby mode, the unexpected interrupt might be sent to the interrupt controller. To avoid this, always clear the INTSTS0 and INTSTS1 registers in the canceling sequence.

28.4.3 Clearing the Interrupt Status Register after Setting Up the Port Function

The input buffer is disabled before the PmnPFS.PSEL and PmnPFS.PMR port is set up, so the internal signal is fixed high or low. The input buffer is enabled after the port is set so that the external pin state is propagated to the MCU. An unexpected interrupt might occur at this time, causing the VBINT and OVRCR bits in INTSTS0 and INTSTS1, or other

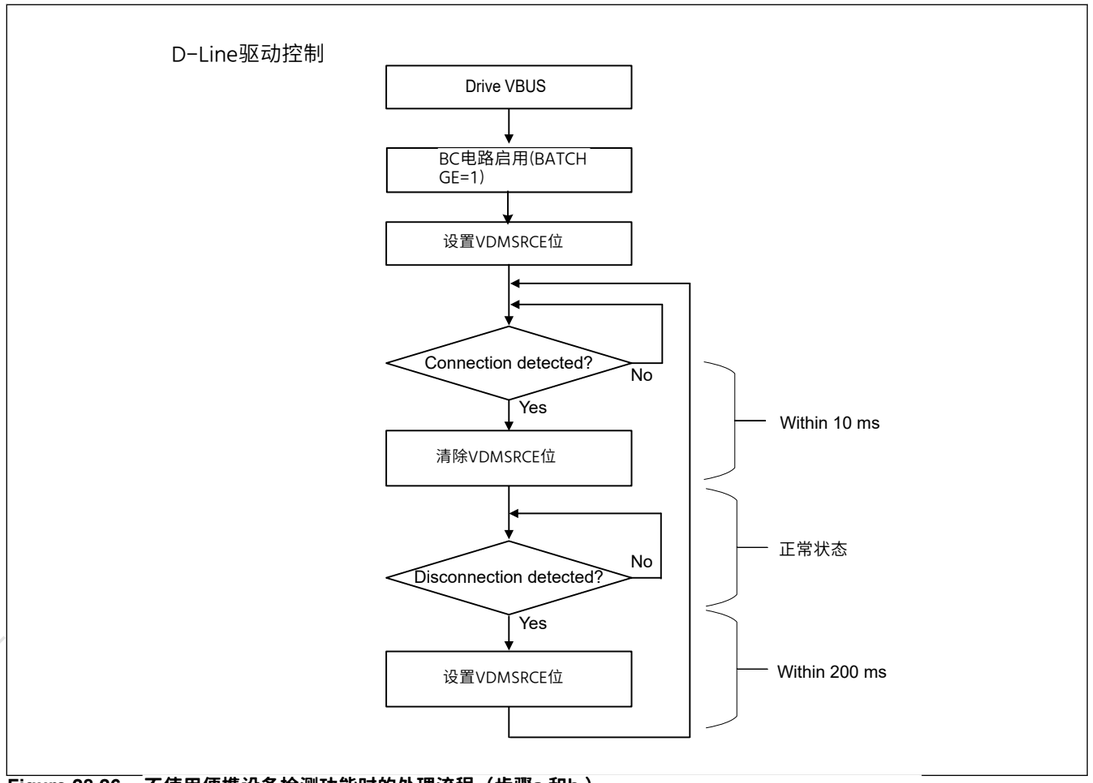


Figure 28.26 不使用便携设备检测功能时的处理流程（步骤a.和b.）

28.4 使用说明

28.4.1 模块停止状态的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用USBFS操作。USBFS在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

28.4.2 退出软件待机模式时清除中断状态寄存器

由于在软件待机模式下始终启用输入缓冲区，因此在以下情况下可能会发生意外中断：

- 在正常模式下使能中断时
- 在软件待机模式下禁用中断时
- 在软件待机模式下，取消软件待机的引脚的输入电平发生变化时

这些情况可能会导致中断状态寄存器中的相关中断标志意外设置。MCU退出软件待机模式后，可能会向中断控制器发送意外中断。为避免这种情况，请始终在取消序列中清除INTSTS0和INTSTS1寄存器。

28.4.3 设置端口功能后清除中断状态寄存器

在设置PmnPFS.PSEL和PmnPFS.PMR端口之前，输入缓冲器被禁用，因此内部信号固定为高电平或低电平。设置端口后启用输入缓冲器，以便将外部引脚状态传播到MCU。此时可能会发生意外中断，导致INTSTS0和INTSTS1中的VBINT和OVRCR位，或其他

interrupt status flags to set to 1. To avoid a malfunction, always clear the INTSTS0 and INTSTS1 registers after setting up the port.

中断状态标志设置为1。为避免故障，请在设置端口后始终清除INTSTS0和INTSTS1寄存器。

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29. USB 2.0 High-Speed Module (USBHS)

29.1 Overview

The MCU provides a USB 2.0 High-Speed Module (USBHS) that operates as a host or a device controller compliant with the Universal Serial Bus (USB) Specification revision 2.0. The host controller supports USB 2.0 high-speed, fullspeed, and low-speed transfers, and the device controller supports USB 2.0 high-speed and full-speed transfers. The USBHS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification.

The USBHS has FIFO buffer for data transfers, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or the communication requirements for your system.

Table 29.1 lists the USBHS specifications, Figure 29.1 shows a block diagram, and Table 29.2 lists the I/O pins.

Table 29.1 USBHS specifications

Parameter	Specifications
Features	• USB Device Controller (UDC) and USB 2.0 transceiver supporting host controller, device controller, and On-The-Go (OTG) functions • Software can switch between host and device controller modes
	Host controller features: • High-speed transfer (480 Mbps), full-speed transfer (12 Mbps), and low-speed transfer (1.5 Mbps) • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Communications with multiple peripheral devices connected through a single hub
	Device controller features: • High-speed transfer (480 Mbps) and full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF complementation
Supported transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Pipe configuration	• FIFO buffer of up to 8.5 KB for USB communications • Up to 10 pipes selectable, including the default control pipe • Programmable pipe configurations • Pipes 1 to 9 assignable to any endpoint number
	Transfer conditions specifiable for each pipe: • Pipe 0: Control transfer with 64-byte single buffer • Pipes 1 and 2: Bulk isochronous transfer continuous transfer mode with programmable buffer size up to 2 KB and optional double buffer • Pipes 3 to 5: Bulk transfer continuous transfer mode with programmable buffer size up to 2 KB and optional double buffer • Pipes 6 to 9: Interrupt transfer with 64-byte single buffer
Other features	• Force-end transfer function using transaction count • Function that changes the BRDY interrupt event notification timing • Automatic clearing of the FIFO buffer after data for the pipe specified in the DnFIFO port (n = 0, 1) is read • NAK setting function for response PID generated on transfer end • On-chip pull-up and pull-down resistors for D+ and D- • Support for Link Power Management (LPM) ECN, including a new Sleep state (the L1 state) • Compliance with Battery Charging Class Specification Revision 1.2 • For power reduction, selectable classic-only mode (CL-only mode) in which operation is only USB 1.1-compliant

29. USB2.0高速模块(USBHS)

29.1 Overview

MCU提供USB2.0高速模块(USBHS)，可作为主机或设备控制器运行，符合通用串行总线(USB)规范修订版2.0。主机控制器支持USB2.0高速、全速和低速传输，设备控制器支持USB2.0高速和全速传输。USBHS具有内部USB收发器，并支持USB2.0规范中定义的所有传输类型。

USBHS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或系统的通信要求，可以将任何端点编号分配给管道1到9。

表29.1列出了USBHS规范，图29.1显示了框图，表29.2列出了IO引脚。

Table 29.1 USBHS specifications

Parameter	Specifications
Features	• USB设备控制器(UDC)和USB2.0收发器，支持主机控制器、设备控制器和On-The-Go(OTG)功能 • 软件可以在主机和设备控制器模式之间切换
	主机控制器特点：● 高速传输(480Mbps)、全速传输(12Mbps)和低速传输(1.5Mbps) • SOF和数据包传输的自动调度 • 同步和中断传输的可编程间隔 • 与通过单个集线器连接的多个外围设备进行通信
	设备控制器特点：● 高速传输(480Mbps)和全速传输(12Mbps) • 控制转移级控制功能 • 设备状态控制功能 • SET_ADDRESS请求的自动响应功能 • SOF complementation
支持的传输类型	• 控制转移 • 批量传输 • 中断传输 • Isochronous transfer
管道配置	• 用于USB通信的高达8.5KB的FIFO缓冲区 • 最多可选择10个管道，包括默认控制管道 • 可编程管道配置 • 管道1到9可分配给任何端点编号
	可为每根管道指定传输条件：● 管道0：使用64字节单缓冲区进行控制传输 • 管道1和2：批量同步传输连续传输模式，可编程缓冲区大小高达2KB和可选的双缓冲区 • 管道3到5：批量传输连续传输模式，可编程缓冲区大小高达2KB和可选的双缓冲区 • 管道6到9：使用64字节单缓冲区的中断传输
其它功能	• 使用事务计数的强制结束传输函数 • 改变BRDY中断事件通知时间的函数 • 读取DnFIFO端口(n=0 1)中指定管道的数据后自动清除FIFO缓冲区 • 传输结束时产生的响应PID的NAK设置功能 • D+和D的片上上拉和下拉电阻 • 支持链路电源管理(LPM)ECN，包括新的睡眠状态（L1状态） • 符合电池充电类规范修订版1.2 • 为了降低功耗，可选择仅经典模式（CL-only模式），其中操作仅兼容USB1.1

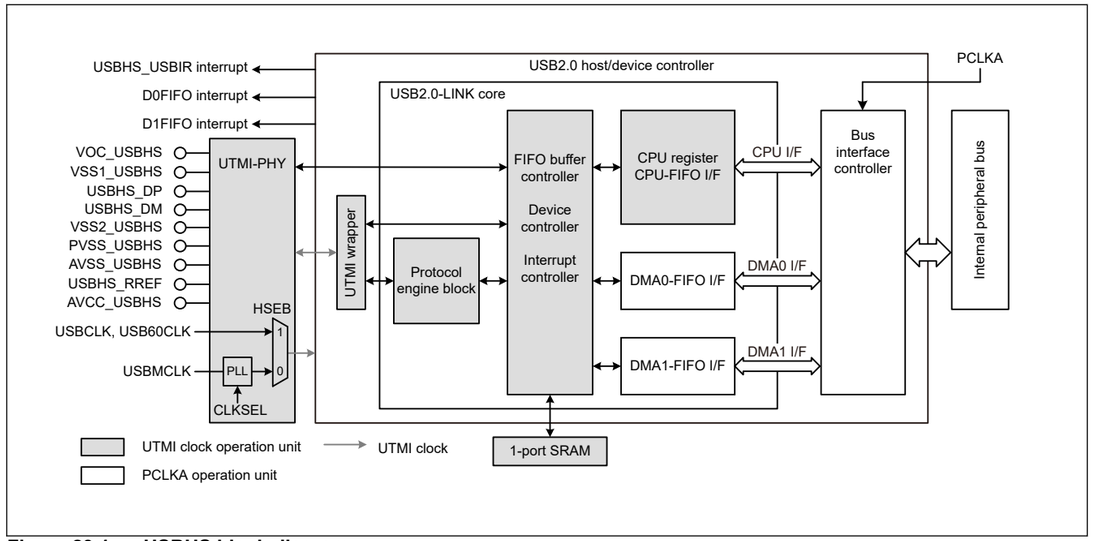

Figure 29.1 USBHS block diagram

Table 29.2 USBHS I/O pins

Pin name	I/O	Function
VCC_USBHS	Input	Power supply pin for the USBHS
VSS1_USBHS VSS2_USBHS	Input	Ground pin for the USBHS
AVCC_USBHS	Input	Analog power supply pin for the USBHS
AVSS_USBHS	Input	Analog ground pin for the USBHS Must be shorted to the PVSS_USBHS pin.
PVSS_USBHS	Input	PLL circuit ground pin for the USBHS Must be shorted to the AVSS_USBHS pin.
USBHS_RREF	I/O	Reference current source pin for the USBHS Must be connected to the AVSS_USBHS pin through a 2.2-kΩ (±1%) resistor.
USBHS_DP	I/O	Input/output pin for the D+ data line of the USB bus
USBHS_DM	I/O	Input/output pin for the D- data line of the USB bus
USBHS_EXICEN	Output	Must be connected to the OTG power supply IC
USBHS_ID	Input	Must be connected to the OTG power supply IC
USBHS_VBUSEN	Output	VBUS power supply enable pin for the USBHS
USBHS_OVRCURA/ USBHS_OVRCURB	Input	Overcurrent pin for the USBHS
USBHS_VBUS	Input	USB cable connection monitor input pin

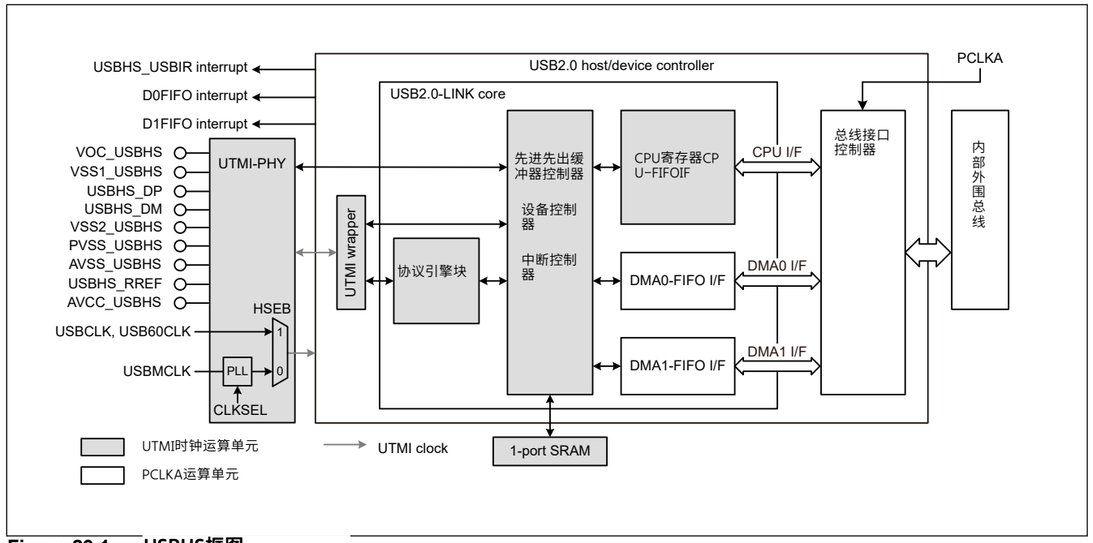

Figure 29.1 USBHS框图

Table 29.2 USBHS I/O pins

引脚名称	I/O	Function
VCC_USBHS	Input	USBHS的电源引脚
VSS1_USBHS VSS2_USBHS	Input	USBHS的接地引脚
AVCC_USBHS	Input	USBHS的模拟电源引脚
AVSS_USBHS	Input	USBHS的模拟接地引脚 必须短接到PVSS_USBHS引脚。
PVSS_USBHS	Input	USBHS的PLL电路接地引脚 必须短接到AVSS_USBHS引脚。
USBHS_RREF	I/O	USBHS的参考电流源引脚 必须通过2.2-kΩ(±1%)电阻连接到AVSS_USBHS引脚。
USBHS_DP	I/O	USB总线D+数据线的输入输出引脚
USBHS_DM	I/O	USB总线Ddata线的输入输出引脚
USBHS_EXICEN	Output	必须接OTG电源IC
USBHS_ID	Input	必须接OTG电源IC
USBHS_VBUSEN	Output	USBHS的VBUS电源使能引脚
USBHS_OVRCURA/ USBHS_OVRCURB	Input	USBHS的过流引脚
USBHS_VBUS	Input	USB线连接显示器输入引脚

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29.2 Register Descriptions

29.2.1 SYSCFG : System Configuration Control Register

Base address: USBHS = 0x4011_1000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CNEN	HSE	DCFM	DRPD	DPRPU	—	—	—	USBE
Value after reset:	x	x	x	x	x	x	x	0	0	0	1	0	x	x	x	0

Bit	Symbol	Function	R/W
0	USBE	USBHS Operation Enable 0: Disable 1: Enable	R/W
3:1	—	The read values are undefined. The write value should be 0.	R/W
4	DPRPU	D+ Line Resistor Control 0: Disable line pull-up 1: Enable line pull-up	R/W
5	DRPD	D+/D- Line Resistor Control 0: Disable line pull-down 1: Enable line pull-down	R/W
6	DCFM	Controller Operation Select 0: Select device controller mode 1: Select host controller mode	R/W
7	HSE	High-Speed Operation Enable 0: Disable Device controller mode: full-speed Host controller mode: full- or low-speed 1: Enable The controller detects the communication speed	R/W
8	CNEN	Single-ended Receiver Enable 0: Disable 1: Enable	R/W
15:9	—	The read values are undefined. The write value should be 0.	R/W

Writing to the SYSCFG register can proceed while the PHY clock is stopped. However, written values are only reflected in the SYSCFG register after the PHY clock is oscillating again.

USBE bit (USBHS Operation Enable)

The USBE bit enables or disables operation of USBHS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 29.3. Only change this bit after specifying the input clock in the PHYSET.CLKSEL[1:0] bits and confirming that the PLLSTA.PLLLOCK flag is 1. In CL-only mode, change the USBE bit after setting the PHYSET.HSEB bit to 1. At that time, the USBCLK must be set to 48 MHz and USB60CLK must be set to 60 MHz. For the clock settings, see section 29.3.3. Supplying the Clock.

In host controller mode, always set this bit to 1 after setting the DRPD bit to 1, eliminating SYSSTS0.LNST[1:0] bit chattering, and confirming that the USB bus state is stable.

29.2 注册说明

29.2.1 SYSCFG：系统配置控制寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CNEN	HSE	DCFM	DRPD	DPRPU	—	—	—	USBE
重置后的值：	x	x	x	x	x	x	x	0	0	0	1	0	x	x	x	0

Bit	Symbol	Function	R/W
0	USBE	USBHS操作使能 0：禁用1 ：启用	R/W
3:1	—	读取的值未定义。写入值应为0。	R/W
4	DPRPU	D+线路电阻控制 0：禁用线路上拉1： 启用线路上拉	R/W
5	DRPD	D+DLine电阻控制 0：禁用线下拉1：启用线 下拉	R/W
6	DCFM	控制器操作选择 0：选择设备控制器模式1：选择 主机控制器模式	R/W
7	HSE	高速操作使能 0: Disable 设备控制器模式：全速 主机控制器模式：全速或低速 1: Enable 控制器检测通讯速度	R/W
8	CNEN	单端接收器使能 0：禁用1 ：启用	R/W
15:9	—	读取的值未定义。写入值应为0。	R/W

当PHY时钟停止时，可以继续写入SYSCFG寄存器。但是，写入的值仅在PHY时钟再次振荡后才会反映在SYSCFG寄存器中。

USBE位（USBHS操作使能）

USBE位启用或禁用USBHS的操作。

将USBE位从1更改为0会初始化表29.3中列出的位。仅在PHYSET.CLKSEL[1:0]位中指定输入时钟并确认PLLSTA.PLLLOCK标志为1后更改该位。在CL-only模式下，将PHYSET.HSEB位设置为1后更改USBE位.此时USBCLK必须设置为48MHz，USB60CLK必须设置为60MHz。有关时钟设置，请参阅第29.3.3节。提供时钟。

在主机控制器模式下，在将DRPD位设置为1后始终将此位设置为1，消除SYSSTS0.LNST[1:0]位抖动，并确认USB总线状态稳定。

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Table 29.3 Bits initialized by writing SYSCFG.USBE = 0

Selected function	Register	Bit	Remarks
Device controller (DCFM = 0)	SYSSTS0	LNST[1:0]	Value is saved in host controller mode
	DVSTCTR0	RHST[2:0]	—
	PL1CTRL1	DVSQ[3:0]	Value is saved in host controller mode
	USBADDR	USBADDR[6:0]	Value is saved in host controller mode
	USBREQ	• BREQUEST[7:0] • BMREQUESTTYPE[7:0]	Value is saved in host controller mode
	USBVAL	WVALUE[15:0]	Value is saved in host controller mode
	USBINDX	WINDEX[15:0]	Value is saved in host controller mode
	USBLENG	WLENTUH[15:0]	Value is saved in host controller mode
Host controller (DCFM = 1)	DVSTCTR0	RHST[2:0]	—
	FRMNUM	FRNM[10:0]	Value is saved in device controller mode
	UFRMNUM	UFRNM[2:0]	Value is saved in device controller mode

DPRPU bit (D+ Line Resistor Control)

The DPRPU bit enables or disables pulling up the D+ line in device controller mode.

When the DPRPU bit is set to 1 in device controller mode, the USBHS pulls up the D+ line to notify the USB host that it attached. Changing the DPRPU bit from 1 to 0 releases the pull-up, thereby notifying the USB host that it detached.

Set this bit to 1 in device controller mode and to 0 in host controller mode.

DRPD bit (D+/D- Line Resistor Control)

The DRPD bit enables or disables pulling down D+ and D- lines in host controller mode.

Set this bit to 1 in host controller mode. Set it to 0 when OTG is not used in device controller mode.

DCFM bit (Controller Operation Select)

The DCFM bit selects the host or device function of the USBHS.

Only change this bit when the DPRPU and DRPD bits are both 0.

HSE bit (High-Speed Operation Enable)

The HSE bit enables or disables high-speed operation.

When this bit is 1, the USBHS operates in high- or full-speed based on the results of the reset handshake.

In host controller mode, setting this bit to 0 allows the USBHS to operate in low- or full-speed. If the DVSTCTR0.RHST[2:0] flags indicate that a low-speed device has attached, set the HSE bit to 0.

In host controller mode, setting this bit to 1 allows the USBHS to operate in high- or full-speed based on the results of the reset handshake. Change the HSE bit after detection of an attach event (ATTCH interrupt) and before the USB bus reset (when DVSTCTR0.USBRST = 1), or after detection of a detach event.

In device controller mode, setting this bit to 0 allows the USBHS to operate in full-speed. Setting the bit to 1 allows the USBHS to perform the reset handshake and then operate in high-speed or full-speed, based on the results.

In device controller mode, only change this bit when the DPRPU bit is 0.

CNEN bit (Single-ended Receiver Enable)

Setting the CNEN bit to 1 enables single-ended receiver operation and selects monitoring of the D+ and D- line states in the SYSSTS0.LNST[1:0] flags. Use this bit to prevent through-current damage that might otherwise be caused during single-ended receiver operation, where the terminals are floating while the USBHS is detached.

In host controller mode, set this bit to 1 after confirming that the PHY clock is being supplied. In device controller mode, set this bit to 1 when the VBUS is detected because of a VBUS interrupt, and set it to 0 when the VBUS line is removed.

Table 29.3 通过写入SYSCFG.USBE=0初始化的位

所选功能	Register	Bit	Remarks
设备控制器(DCFM=0)	SYSSTS0	LNST[1:0]	值以主机控制器模式保存
	DVSTCTR0	RHST[2:0]	—
	PL1CTRL1	DVSQ[3:0]	值以主机控制器模式保存
	USBADDR	USBADDR[6:0]	值以主机控制器模式保存
	USBREQ	• BREQUEST[7:0] • BMREQUESTTYPE[7:0]	值以主机控制器模式保存
	USBVAL	WVALUE[15:0]	值以主机控制器模式保存
	USBINDX	WINDEX[15:0]	值以主机控制器模式保存
	USBLENG	WLENTUH[15:0]	值以主机控制器模式保存
主机控制器(DCFM=1)	DVSTCTR0	RHST[2:0]	—
	FRMNUM	FRNM[10:0]	值保存在设备控制器模式中
	UFRMNUM	UFRNM[2:0]	值保存在设备控制器模式中

DPRPU位（D+线路电阻控制）

DPRPU位启用或禁用在设备控制器模式下上拉D+线。

当DPRPU位在设备控制器模式下设置为1时，USBHS拉高D+线以通知USB主机它已连接。将DPRPU位从1更改为0会释放上拉电阻，从而通知USB主机它已分离。

在设备控制器模式下将此位设置为1，在主机控制器模式下设置为0。

DRPD位（D+DLine电阻控制）

DRPD位在主机控制器模式下启用或禁用下拉D+和Dlines。

在主机控制器模式下将此位设置为1。在设备控制器模式下不使用OTG时将其设置为0。

DCFM位（控制器操作选择）

DCFM位选择USBHS的主机或设备功能。

仅当DPRPU和DRPD位都为0时更改该位。

HSE位（高速操作使能）

HSE位启用或禁用高速操作。

当该位为1时，USBHS根据复位握手的结果以高速或全速运行。

在主机控制器模式下，将该位设置为0允许USBHS以低速或全速运行。如果DVSTCTR0.RHST[2:0]标志表示已连接低速设备，将HSE位设置为0。

在主机控制器模式下，将此位设置为1允许USBHS根据复位握手的结果以高速或全速运行。在检测到附加事件（ATTCH中断）和USB总线复位之前（当DVSTCTR0.USBRST=1时）或检测到分离事件之后，更改HSE位。

在设备控制器模式下，将该位设置为0允许USBHS全速运行。将该位设置为1允许USBHS根据结果执行复位握手，然后以高速或全速运行。

在设备控制器模式下，仅当DPRPU位为0时更改该位。

CNEN位（单端接收器使能）

将CNEN位设置为1可启用单端接收器操作并选择监控D+和Dline状态SYSSTS0.LNST[1:0]标志。使用该位可防止在单端接收器操作期间可能造成的直通电流损坏，其中在USBHS分离时端子处于浮动状态。

在主机控制器模式下，在确认提供PHY时钟后将该位设置为1。在设备控制器模式下，当由于VBUS中断而检测到VBUS时将该位设置为1，并在移除VBUS线时将其设置为0。

29.2.2 BUSWAIT : CPU Bus Wait Register

Base address: USBHS = 0x4011_1000

Offset address: 0x002

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]		
Value after reset:	x	x	0	0	0	0	0	0	x	x	0	0	1	1	1	1

Bit	Symbol	Function	R/W
3:0	BWAIT[3:0]	CPU Bus Access Wait Specification 0x0: 0 waits (2 access cycles) ⋮ 0x2: 2 waits (4 access cycles) ⋮ 0x4: 4 waits (6 access cycles) ⋮ 0xF: 15 waits (17 access cycles) (initial value)	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
7:6	—	The read values are undefined. The write value should be 0.	R/W
13:8	—	These bits are read as 0. The write value should be 0.	R/W
15:14	—	The read values are undefined. The write value should be 0.	R/W

BWAIT[3:0] bits (CPU Bus Access Wait Specification)

The BWAIT[3:0] bits specify the wait time for access to the USBHS registers.

When accessing the registers at addresses in the range beginning at 0x4011_1004, set the cycle time for consecutive access to at least 40.8 ns. The initial value is 0xF (17 cycles), but Renesas recommends that you satisfy this condition by setting the best wait time for the frequency of the CPU clock in your application.

This setting is the same as the wait time for accesses to the FIFO port register. The maximum speed of access to the FIFO port is as follows:

- MBW[1:0] = 10b (32-bit width): Maximum 60 MB/s
- MBW[1:0] = 01b (16-bit width): Maximum 30 MB/s
- MBW[1:0] = 00b (8-bit width): Maximum 15 MB/s

29.2.3 SYSSTS0 : System Configuration Status Register

Base address: USBHS = 0x4011_1000

Offset address: 0x004

Bit position:	15		13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	LNST[1:0]	USB Data Line Status Monitor Flag Indicates the status of the USB data lines. See Table 29.4.	R
2	IDMON	USBHS_ID Pin Monitor Flag 0: USBHS_ID pin is low 1: USBHS_ID pin is high	R
4:3	—	The read values are undefined.	R

29.2.2 BUSWAIT:CPU总线等待寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x002

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]		
重置后的值:	x	x	0	0	0	0	0	0	x	x	0	0	1	1	1	1

Bit	Symbol	Function	R/W
3:0	BWAIT[3:0]	CPU总线访问等待规范 0x0：0次等待（2个访问周期） ⋮ 0x2：2次等待（4个访问周期） ⋮ 0x4：4次等待（6个访问周期） ⋮ 0xF：15次等待（17个访问周期）（初始值）	R/W
5:4	—	这些位被读取为0。写入值应为0。	R/W
7:6	—	读取的值未定义。写入值应为0。	R/W
13:8	—	这些位被读取为0。写入值应为0。	R/W
15:14	—	读取的值未定义。写入值应为0。	R/W

BWAIT[3:0]位（CPU总线访问等待规范）

BWAIT[3:0]位指定访问USBHS寄存器的等待时间。

访问从0x4011_1004开始的地址范围内的寄存器时，将连续访问的周期时间设置为至少40.8ns。初始值为0xF（17个周期），但瑞萨建议您通过在应用程序中为CPU时钟频率设置最佳等待时间来满足此条件。

该设置与访问FIFO端口寄存器的等待时间相同。访问FIFO端口的最大速度如下：

- MBW[1:0] = 10b (32-bit width): Maximum 60 MB/s
- MBW[1:0] = 01b (16-bit width): Maximum 30 MB/s
- MBW[1:0] = 00b (8-bit width): Maximum 15 MB/s

29.2.3 SYSSTS0：系统配置状态寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x004

Bit position:	15		13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
重置后的值:	x	x	x	x	x	x	x	x	x	0	0	x	x	x	x	x

Bit	Symbol	Function	R/W
1:0	LNST[1:0]	USB数据线状态监控标志 指示USB数据线的状态。见表29.4。	R
2	IDMON	USBHS_ID引脚监控标志 0：USBHS_ID引脚为低电平1 ：USBHS_ID引脚为高电平	R
4:3	—	读取的值未定义。	R

Bit	Symbol	Function	R/W
5	SOFEA	SOF Active Monitor Flag While Host Controller Operation Is Selected 0: SOF output stopped 1: SOF output operating	R
6	HTACT	Host Sequencer Status Monitor Flag 0: Host sequencer stopped 1: Host sequencer operating	R
13:7	—	The read values are undefined.	R
15:14	OVCMON[1:0]	External USBHS_OVRCURA/USBHS_O VRCURB Input Pin Monitor Flag OVCMON[1] indicates the USBHS_OVRCURA pin status. OVCMON[0] indicates the USBHS_OVRCURB pin status.	R

LNST[1:0] flags (USB Data Line Status Monitor Flag)

The LNST[1:0] flags indicate the state of the USB data lines, D+ and D-. For details, see Table 29.4.

In device controller mode, read the LNST[1:0] flags after setting the SYSCFG.CNEN and SYSCFG.USBE bits to 1. In host controller mode, read them after setting the SYSCFG.DRPD bit to 1.

When you are checking hardware contacts for the battery charging function in device controller mode, read the LNST[1:0] flags after setting the SYSCFG.DRPD, SYSCFG.CNEN, and BCCTRL.IDPSRCE bits to 1. For details, see section 29.3.15. Battery charging detection processing.

Table 29.4 Status of USB data bus lines (D+ and D-)

LNST[1]	LNST[0]	Low-speed operation (host controller mode only)	Full-speed operation	High-speed operation	Chirp operation
0	0	SE0	SE0	Squelch	Squelch
0	1	K-State	J-State	Unsquelch	Chirp J
1	0	J-State	K-State	Invalid	Chirp K
1	1	SE1	SE1	Invalid	Invalid

Chirp: The reset handshake protocol is being executed when high-speed operation is enabled (HSE bit is 1).
Squelch: SE0 or idle state
Unsquelch: High-speed J-state or high-speed K-state
Chirp J: Chirp J-State
Chirp K: Chirp K-State

SOFEA flag (SOF Active Monitor Flag While Host Controller Operation Is Selected)

The SOFEA flag is used in host controller mode to check whether the output of the last SOF is complete when the USBHS is suspended because of a 0 setting to the DVSTCTR0.UACT bit.

In host controller mode, check that both the HTACT and SOFEA flags are 0 before setting the SYSCFG.USBE bit to 0 to stop the USBHS or setting the LPSTS.SUSPENDM bit to 0 to stop the clock signal supply during communication.

HTACT flag (Host Sequencer Status Monitor Flag)

The HTACT flag clears to 0 when the host sequencer of the USBHS is completely stopped.

In host controller mode, check that the HTACT flag is 0 before setting the DVSTCTR0.UACT bit to 0 to place the USBHS in the Suspend state or setting the LPSTS.SUSPENDM bit to 0 to stop the clock signal supply during communication.

OVCMON[1:0] flags (External USBHS_OVRCURA/USBHS_O VRCURB Input Pin Monitor Flag)

The OVCMON[1:0] flags indicate the status of the overcurrent signals from an external power supply IC.

Bit	Symbol	Function	R/W
5	SOFEA	选择主机控制器操作时的SOF活动监视器标志 0：SOF输出停止1：SOF 输出工作	R
6	HTACT	主机定序器状态监视器标志 0：主机定序器停止1：主机 定序器运行	R
13:7	—	读取的值未定义。	R
15:14	OVCMON[1:0]	外部USBHS_OVRCURAUSBHS_OVRCURB输入管脚监控标志 OVCMON[1]指示USBHS_OVRCURA引脚状态。OVCMON[0]指示USBHS_OVRCURB引脚状态。	R

LNST[1:0]标志（USB数据线状态监控标志）

LNST[1:0]标志指示USB数据线D+和D−的状态。详见表29.4。

在设备控制器模式下，将SYSCFG.CNEN和SYSCFG.USBE位设置为1后读取LNST[1:0]标志。在主机控制器模式下，将SYSCFG.DRPD位设置为1后读取它们。

当您在设备控制器模式下检查电池充电功能的硬件触点时，在将SYSCFG.DRPD、SYSCFG.CNEN和BCCTRL.IDPSRCE位设置为1后读取LNST[1:0]标志。有关详细信息，请参阅第29.3节.15.电池充电检测处理。

Table 29.4 USB数据总线的状态（D+和D−）

LNST[1]	LNST[0]	低速运行（仅主机控制器模式）	Full-speed operation	High-speed operation	啁啾操作
0	0	SE0	SE0	Squelch	Squelch
0	1	K-State	J-State	Unsquelch	Chirp J
1	0	J-State	K-State	Invalid	Chirp K
1	1	SE1	SE1	Invalid	Invalid

Chirp: 当使能高速操作（HSE位为1）时，正在执行复位握手协议。
Squelch: SE0或空闲状态
Unsquelch: High-speed J-state or high-speed K-state
Chirp J: Chirp J-State
Chirp K: Chirp K-State

SOFEA标志（选择主机控制器操作时的SOF活动监视器标志）

SOFEA标志用于主机控制器模式，用于检查当USBHS由于DVSTCTR0.UACT位设置为0而暂停时最后一个SOF的输出是否完成。

在主机控制器模式下，在将SYSCFG.USBE位设置为0以停止USBHS或将LPSTS.SUSPENDM位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT和SOFEA标志是否为0。

HTACT标志（主机定序器状态监视器标志）

当USBHS的主机定序器完全停止时，HTACT标志清零。

在主机控制器模式下，在将DVSTCTR0.UACT位设置为0以将USBHS置于暂停状态或将LPSTS.SUSPENDM位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT标志是否为0。

OVCMON[1:0]标志（外部USBHS_OVRCURAUSBHS_OVRCURB输入引脚监控标志）

OVCMON[1:0]标志指示来自外部电源IC的过流信号的状态。

29.2.4 PLLSTA : PLL Status Register

Base address: USBHS = 0x4011_1000

Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLLLOCK
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Bit	Symbol	Function	R/W
0	PLLLOCK	PLL Lock Flag 0: PLL not locked 1: PLL locked	R
15:1	—	The read values are undefined.	R

PLLLOCK flag (PLL Lock Flag)

The PLLLOCK flag indicates whether the USB-PHY internal PLL is locked. When not using CL-only mode, make sure that the PLL is locked before starting USB communication.

29.2.5 DVSTCTR0 : Device State Control Register 0

Base address: USBHS = 0x4011_1000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
Bit field:	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
Value after reset:	x	x	x	x	0	0	0	0	0	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
2:0	RHST[2:0]	USB Bus Reset Status Flag 0 0 0: Communication speed indeterminate (powered state or no connection) 0 0 1: Host controller mode Low-speed connection Device controller mode USB bus reset in progress or low-speed connection 0 1 0: Host controller mode Full-speed connection Device controller mode USB bus reset in progress or full-speed connection 0 1 1: Host controller mode High-speed connection Device controller mode USB bus reset in progress or high-speed connection 1 x x: Host controller mode USB bus reset in progress Device controller mode Setting prohibited	R
3	—	The read value is undefined. The write value should be 0.	R/W
4	UACT	USB Bus Operation Enable for the Host Controller Operation 0: Disable downstream port (disable SOF or micro-SOF transmission) 1: Enable downstream port (enable SOF or micro-SOF transmission)	R/W
5	RESUME	Resume Signal Output for the Host Controller Operation 0: Do not output resume signal 1: Output resume signal	R/W

29.2.4 PLLSTA：PLL状态寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLLLOCK
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Bit	Symbol	Function	R/W
0	PLLLOCK	PLL锁定标志 0：PLL未锁定1： PLL锁定	R
15:1	—	读取的值未定义。	R

PLLLOCK标志（PLL锁定标志）

PLLLOCK标志指示USB-PHY内部PLL是否被锁定。不使用CL-only模式时，请确保在开始USB通信之前锁定PLL。

29.2.5 DVSTCTR0：设备状态控制寄存器0

Base address: USBHS = 0x4011_1000

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2		0
Bit field:	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
重置后的值：	x	x	x	x	0	0	0	0	0	0	0	0	x	0	0	0

Bit	Symbol	Function	R/W
2:0	RHST[2:0]	USB总线复位状态标志 000：通讯速度不定（通电或无连接）001：上位机模式 Low-speed connection 设备控制器模式 USB总线正在重置或低速连接 010：主机控制器模式 Full-speed connection 设备控制器模式 USB总线正在重置或全速连接 011：主机控制器模式 High-speed connection 设备控制器模式 USB总线正在复位或高速连接 1xx：主机控制器模式 USB总线正在重置 设备控制器模式 禁止设定	R
3	—	读取值未定义。写入值应为0。	R/W
4	UACT	主机控制器操作的USB总线操作使能 0：禁用下行端口（禁用SOF或micro-SOF传输）1：启用下行端口（启用SOF或micro-SOF传输）	R/W
5	RESUME	主机控制器操作的恢复信号输出 0：不输出恢复信号1：输出恢复信号	R/W

Bit	Symbol	Function	R/W
6	USBRST	USB Bus Reset Output for the Host Controller Operation 0: Do not output USB bus reset signal 1: Output USB bus reset signal	R/W
7	RWUPE	Remote Wakeup Detection Enable for the Host Controller Operation 0: Disable downstream port remote wakeup 1: Enable downstream port remote wakeup	R/W
8	WKUP	Remote Wakeup Output for the Device Controller Operation 0: Do not output remote wakeup signal 1: Output remote wakeup signal	R/W
9	VBUSEN	USBHS_VBUSEN Output Pin Control 0: Output low on external USBHS_VBUSEN pin 1: Output high on external USBHS_VBUSEN pin	R/W
10	EXICEN	USBHS_EXICEN Output Pin Control 0: Output low on external USBHS_EXICEN pin 1: Output high on external USBHS_EXICEN pin	R/W
11	HNPBTOA	Host Negotiation Protocol (HNP) Control Use this bit when switching from device B to device A in OTG mode. If the HNPBTOA bit is 1, the internal function control remains in the Suspend state until the HNP processing ends even if SYSCFG.DPRPU = 0 or SYSCFG.DCFM = 1 is set.	R/W
15:12	—	The read values are undefined. The write value should be 0.	R/W

RHST[2:0] flags (USB Bus Reset Status Flag)

The RHST[2:0] flags indicate the USB bus reset status.

In host controller mode, writing 1 to the USBRST bit causes the RHST[2:0] flags to set to 100b. When 0 is written to the USBRST bit and the USBHS ends the SE0 state, the RHST[2:0] flags update to a new value.

In device controller mode, if the USBHS detects a USB bus reset, the RHST[2:0] flags set to 010b if an attach event occurs while the DPRPU bit is 1, and a DVST interrupt is generated.

UACT bit (USB Bus Operation Enable for the Host Controller Operation)

When set to 1 in host controller mode, the UACT bit enables USB bus operation by controlling SOF packet transmission to the USB bus in addition to data and reception. The USBHS starts SOF packet output within one frame period after the this bit is set to 1. If UACT is set to 0, the USBHS enters the idle state after the SOF packet output.

The USBHS sets the bit to 0 on any of the following conditions:

- A DTCH interrupt is detected during communication (while UACT = 1)
- An EOFERR interrupt is detected during communication (while UACT = 1)

Always write 1 to the UACT bit at the end of the USB bus reset processing (on a 0 write to the USBRST bit) or at the end of resume processing from the Suspend state (on a 0 write to the RESUME bit).

The USBHS clears the UACT bit to 0 if it receives an ACK response to an LPM token while the HL1CTRL1.L1REQ bit is set to 1. The USBHS sets the UACT bit to 1 when it finishes resume processing from the L1 state.

In device controller mode, always set this bit to 0.

RESUME bit (Resume Signal Output for the Host Controller Operation)

The RESUME bit controls the resume signal output in host controller mode.When this bit is set to 1, the USBHS drives the USB port to the K-state and outputs the resume signal. The USBHS sets the bit to 1 on detection of a remote wakeup signal while the RWUPE bit is 1 and in the USB suspend state. The USBHS continues outputting the K-state while the RESUME bit is 1, until the bit is cleared to 0 by software. The RESUME bit must be 1 (= resume period) for the time defined in the USB 2.0 specification. Only set this bit to 1 while the interface is in the Suspend state. Write 1 to the UACT bit simultaneously with the end of the resume processing (0 write to the RESUME bit).

Setting the RESUME bit to 1 during transition to the L1 state allows the USBHS to drive the USB port to the K-state and output the resume signal. The USBHS clears the RESUME bit to 0 at the end of the resume period, the value set in the HL1CTRL2.HIRD[3:0] bits.

Always set this bit to 0 in device controller mode.

Bit	Symbol	Function	R/W
6	USBRST	用于主机控制器操作的USB总线复位输出 0：不输出USB总线复位信号1：输出USB总线复位信号	R/W
7	RWUPE	主机控制器操作的远程唤醒检测启用 0：禁用下游端口远程唤醒1：启用下游端口远程唤醒	R/W
8	WKUP	设备控制器操作的远程唤醒输出 0：不输出远程唤醒信号1：输出远程唤醒信号	R/W
9	VBUSEN	USBHS_VBUSEN输出引脚控制 0：外部USBHS_VBUSEN引脚输出低电平1：外部USBHS_VBUSEN引脚输出高电平	R/W
10	EXICEN	USBHS_EXICEN输出引脚控制 0：外部USBHS_EXICEN引脚输出低电平1：外部USBHS_EXICEN引脚输出高电平	R/W
11	HNPBTOA	主机协商协议(HNP)控制 在OTG模式下从设备B切换到设备A时使用该位。如果HNPBTOA位为1，即使设置SYSCFG.DPRPU=0或SYSCFG.DCFM=1，内部功能控制仍保持暂停状态直到HNP处理结束。	R/W
15:12	—	读取的值未定义。写入值应为0。	R/W

RHST[2:0]标志（USB总线复位状态标志）

RHST[2:0]标志指示USB总线复位状态。

在主机控制器模式下，将1写入USBRST位会导致RHST[2:0]标志设置为100b。当0被写入USBRST位和USBHS结束SE0状态，RHST[2:0]标志更新为新值。

在设备控制器模式下，如果USBHS检测到USB总线复位，如果在DPRPU位为1时发生连接事件并产生DVST中断，则RHST[2:0]标志设置为010b。

UACT位（主机控制器操作的USB总线操作使能）

在主机控制器模式下设置为1时，UACT位通过控制向USB总线发送SOF数据包以及数据和接收来启用USB总线操作。USBHS在该位设置为1后的一帧周期内开始SOF数据包输出。如果UACT设置为0，则USBHS在SOF数据包输出后进入空闲状态。

USBHS在以下任何条件下将该位设置为0：

- ●在通信期间检测到DTCH中断（当UACT=1时）
- ●通信期间检测到EOFERR中断（当UACT=1时）

在USB总线复位处理结束时（向USBRST位写入0）或从挂起状态恢复处理结束时（向RESUME位写入0），始终向UACT位写入1。

如果USBHS在HL1CTRL1.L1REQ位设置为1时接收到对LPM令牌的ACK响应，则将UACT位清除为0。USBHS在完成从L1状态恢复处理时将 UACT位设置为1。

在设备控制器模式下，始终将此位设置为0。

RESUME位（主机控制器操作的恢复信号输出）

RESUME位控制主机控制器模式下的恢复信号输出。当该位设置为1时，USBHS将USB端口驱动到K状态并输出恢复信号。当RUPE位为1且处于USB挂起状态时，USBHS在检测到远程唤醒信号时将该位设置为1。当RESUME位为1时，USBHS继续输出K状态，直到该位被软件清零。在USB2.0规范中定义的时间内，RESUME位必须为1（=恢复周期）。仅当接口处于挂起状态时将此位设置为1。在恢复处理结束的同时向UACT位写入1（向RESUME位写入0）。

在转换到L1状态期间将RESUME位设置为1允许USBHS将USB端口驱动到K状态并输出恢复信号。USBHS在恢复周期结束时将RE SUME位清除为0，该值在HL1CTRL2.HIRD[3:0]位中设置。

在设备控制器模式下始终将此位设置为0。

USBRST bit (USB Bus Reset Output for the Host Controller Operation)

The USBRST bit controls the output of the USB bus signal in host controller mode. When this bit set to 1, the USBHS drives the USB port to the SE0 state to reset the USB bus. The USBHS continues outputting SE0 while the USBRST bit is 1, until the bit is cleared to 0 by software. The USBRST bit must be 1 (= USB bus reset period) for the time defined in the USB 2.0 specification. Writing 1 to the USBRST bit during communication (UACT bit = 1) or during resume processing (RESUME bit = 1) prevents the USBHS from starting USB bus reset processing until both the UACT and RESUME bits clear to 0. Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (0 write to the USBRST bit).

Always set this bit to 0 in device controller mode.

RWUPE bit (Remote Wakeup Detection Enable for the Host Controller Operation)

The RWUPE bit enables or disables remote wakeup signals (resume signals) from downstream peripheral devices in host controller mode. When this bit is set to 1, the USBHS detects a remote wakeup signal (K-state for 2.5 µs) from a downstream peripheral device, and it performs resume processing, driving the K-state. When the RWUPE bit is set to 0, the USBHS ignores remote wakeup signals (K-states) from peripheral devices connected to the USB port.

Do not stop the PHY clock while the RWUPE bit is 1, even in the Suspend state (the LPSTS.SUSPENDM bit must be set to 1). Also, do not reset the USB bus (setting USBRST to 1) from the Suspend state. This is prohibited in the USB 2.0 specification.

The RWUPE bit is also used to enable or disable detection of a remote wakeup signal during transition to the L1 state.

Always set this bit to 0 in device controller mode.

WKUP bit (Remote Wakeup Output for the Device Controller Operation)

The WKUP bit enables or disables remote wakeup signals (resume signals) to the USB bus in device controller mode.

The USBHS controls the output timing of the remote wakeup signals. When this bit is set to 1, the USBHS clears it to 0 after outputting the K-state for 10 ms. The USB 2.0 specification dictates that the USB bus idle state must be maintained for 5 ms or longer before a remote wakeup signal is sent. If the USBHS writes 1 to the WKUP bit immediately after detecting the Suspend state, the K-state is output after 2 ms.

Only write 1 to the WKUP bit when the device is in the Suspend state (the PL1CTRL1.DVSQ[3:0] flags are 01xxb) and the USB host enables the remote wakeup signal (RWUPE = 1). Do not stop the PHY clock while this bit is 1, even in the Suspend state (the LPSTS.SUSPENDM bit must be set to 1).

If the WKUP bit is set to 1 during transition to the L1 state, the USBHS outputs the K-state for 50 µs and then clears the bit to 0. Before writing 1 to the bit during the L1 state, check that the PL1CTRL1.DVSQ[3:0] flags are 10xxb.

Always set this bit to 0 in host controller mode.

HNPBTOA bit (Host Negotiation Protocol (HNP) Control)

The HNPBTOA bit is used when switching from device B to device A while in OTG mode.

If the HNPBTOA bit is 1, the internal function control maintains the Suspend state until HNP processing ends, even if the SYSCFG.DPRPU bit is set to 0 or the SYSCFG.DCFM bit is set to 1. Resume interrupts (RESM) are not generated even if a falling edge of D+ is detected.

The HNP processing ends when a host attach event is detected, because of a pull-up by the initiating party, or the HNPBTOA bit is cleared to 0 by software because the HNP processing times out.

29.2.6 TESTMODE : USB Test Mode Register

Base address: USBHS = 0x4011_1000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

USBRST位（用于主机控制器操作的USB总线复位输出）

USBRST位控制主机控制器模式下USB总线信号的输出。当该位设置为1时，USBHS将USB端口驱动到SE0状态以复位USB总线。当USBRST位为1时，USBHS继续输出SE0，直到该位被软件清零。在USB2.0规范中定义的时间内，USBRST位必须为1（=USB总线复位周期）。在通信期间（UACT位=1）或恢复处理期间（RESUME位=1）向USBRST位写入1可防止USBHS开始USB总线复位处理，直到UACT和RESUME位都清零。向UACT位写入1同时结束USB总线复位处理（0写入USBRST位）。

在设备控制器模式下始终将此位设置为0。

RHUPE位（主机控制器操作的远程唤醒检测使能）

在主机控制器模式下，RWUPE位启用或禁用来自下游外围设备的远程唤醒信号（恢复信号）。当该位设置为1时，USBHS检测到来自下游外围设备的远程唤醒信号（K状态持续2.5µs），并执行恢复处理，驱动K状态。当RWUPE位设置为0时，USBHS忽略来自连接到USB端口的外围设备的远程唤醒信号（K状态）。

当RHUPE位为1时不要停止PHY时钟，即使处于挂起状态（LPSTS.SUSPENDM位必须设置为1）。此外，不要将USB总线（将USBRST设置为1）从挂起状态复位。这在USB2.0规范中是禁止的。

RWUPE位还用于在转换到L1状态期间启用或禁用远程唤醒信号的检测。

在设备控制器模式下始终将此位设置为0。

WKUP位（设备控制器操作的远程唤醒输出）

WKUP位在设备控制器模式下启用或禁用到USB总线的远程唤醒信号（恢复信号）。

USBHS控制远程唤醒信号的输出时序。当该位设置为1时，USBHS在输出K状态10ms后将其清除为0。USB2.0规范规定，在发送远程唤醒信号之前，USB总线空闲状态必须保持5ms或更长时间。如果USBHS在检测到Suspend状态后立即向WKUP位写入1，则在2ms后输出K状态。

仅当设备处于挂起状态（PL1CTRL1.DVSQ[3:0]标志为01xxb）时向WKUP位写入1，并且USB主机使能远程唤醒信号(RWUPE=1)。当该位为1时不要停止PHY时钟，即使在挂起状态（LPSTS.SUSPENDM位必须设置为1）。

如果在转换到L1状态期间WKUP位设置为1，则USBHS输出K状态50µs，然后将该位清除为0。在L1状态期间向该位写入1之前，请检查PL1CTRL1.DVSQ[3:0]标志为10xxb。

在主机控制器模式下始终将此位设置为0。

HNPBTOA位（主机协商协议(HNP)控制）

在OTG模式下从设备B切换到设备A时使用HNPBTOA位。

如果HNPBTOA位为1，内部功能控制保持暂停状态直到HNP处理结束，即使SYSCFG.DPRPU位设置为0或SYSCFG.DCFM位设置为1。不产生恢复中断(RESM)即使检测到D+的下降沿。

当检测到主机连接事件时，HNP处理结束，因为发起方的上拉，或者由于HNP处理超时，HNPBTOA位由软件清零。

29.2.6 TESTMODE:USB测试模式寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x00C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Bit	Symbol	Function	R/W
3:0	UTST[3:0]	Test Mode These bits output the USB test signals. See Table 29.5	R/W
15:4	—	The read values are undefined. The write value should be 0.	R/W

UTST[3:0] bits (Test Mode)

Writing values to the UTST[3:0] bits allows the USBHS to output USB test signals in high-speed operation mode. Table 29.5 shows the test mode operation settings.

Table 29.5 Test mode operation settings

Test mode	UTST[3:0] bit setting	
	In device controller mode	In host controller mode
Normal operation	0x0	0x0
Test_J	0x1	0x9
Test_K	0x2	0xA
Test_SE0_NAK	0x3	0xB
Test_Packet	0x4	0xC
Test_Force_Enable	—	0xD
Reserved	0x5 to 0x7	0xE to 0xF

Host controller mode

In host controller mode, these bits can be set after setting the SYSCFG.DRPD bit to 1. After the UTST[3:0] bits are set, the USBHS outputs waveforms to the USB port by setting the DVSTCTR0.UACT bit to 1. The USBHS also performs high-speed termination for the USB port by setting these bits in host controller mode.

To set the UTST[3:0] bits in host controller mode:

1. Reset the hardware.
2. Start supplying the PHY clock, and then set the LPSTS.SUSPENDM bit to 1.
3. Set the SYSCFG.DCFM and SYSCFG.DRPD bits to 1. (Setting the SYSCFG.HSE bit to 1 is not required.)
4. Set the SYSCFG.USBE bit to 1.
5. Set the UTST[3:0] bits based on the test requirements.
6. Set the DVSTCTR0.UACT bit to 1.

Assuming the initial steps (1) to (6) are already complete, to change the UTST[3:0] bits in host controller mode:

1. Set the DVSTCTR0.UACT and SYSCFG.USBE bits to 0.
2. Set the SYSCFG.USBE bit to 1.
3. Set the UTST[3:0] bits based on the test requirements.
4. Set the DVSTCTR0.UACT bit to 1.

When the UTST[3:0] bits are set to 1011b (Test_SE0_NAK), the USBHS does not output SOF packets to ports for which the DVSTCTR0.UACT bit is set to 1.

When the UTST[3:0] bits are set to 1101b (Test_Force_Enable), the USBHS outputs SOF packets to ports for which the DVSTCTR0.UACT bit is set to 1. In this test mode, the USBHS does not control the hardware related to attach detection, even if it detects a high-speed detach event (DTCH interrupt).

Before setting the UTST[3:0] bits, set the PID[1:0] bits of all pipe control registers to 00b (NAK response). To return to normal USB communication after setting a test mode, issue a hardware reset.

Bit	Symbol	Function	R/W
3:0	UTST[3:0]	测试模式 这些位输出USB测试信号。见表29.5	R/W
15:4	—	读取的值未定义。写入值应为0。	R/W

UTST[3:0] bits (Test Mode)

将值写入UTST[3:0]位允许USBHS在高速操作模式下输出USB测试信号。表29.5显示了测试模式操作设置。

Table 29.5 测试模式操作设置

测试模式	UTST[3:0]位设置	
	在设备控制器模式下	在主机控制器模式下
普通手术	0x0	0x0
Test_J	0x1	0x9
Test_K	0x2	0xA
Test_SE0_NAK	0x3	0xB
Test_Packet	0x4	0xC
Test_Force_Enable	—	0xD
Reserved	0x5 to 0x7	0xE to 0xF

主机控制器模式

在主机控制器模式下，可以在将SYSCFG.DRPD位设置为1后设置这些位。设置UTST[3:0]位后，USBHS通过将DVSTCTR0.UACT位设置为1将波形输出到USB端口。USBHS还通过在主机控制器模式下设置这些位来执行USB端口的高速端接。

在主机控制器模式下设置UTST[3:0]位：

1.重置硬件。

2.开始提供PHY时钟，然后将LPSTS.SUSPENDM位设置为1。

3.将SYSCFG.DCFM和SYSCFG.DRPD位设置为1。（不需要将SYSCFG.HSE位设置为1。）

4.将SYSCFG.USBE位设置为1。

5.根据测试要求设置UTST[3:0]位。

6.将DVSTCTR0.UACT位设置为1。

假设初始步骤(1)到(6)已经完成，在主机控制器模式下更改UTST[3:0]位：

1.将DVSTCTR0.UACT和SYSCFG.USBE位设置为0。

2.将SYSCFG.USBE位设置为1。

3.根据测试要求设置UTST[3:0]位。

4.将DVSTCTR0.UACT位设置为1。

当UTST[3:0]位设置为1011b(Test_SE0_NAK)时，USBHS不会将SOF数据包输出到DVSTCTR0.UACT位设置为1的端口。

当UTST[3:0]位设置为1101b(Test_Force_Enable)时，USBHS将SOF数据包输出到DVSTCTR0.UACT位设置为1。在此测试模式下，USBHS不控制与连接检测相关的硬件，即使它检测到高速分离事件（DTCH中断）。

在设置UTST[3:0]位之前，将所有管道控制寄存器的PID[1:0]位设置为00b（NAK响应）。要在设置测试模式后返回正常USB通信，请发出硬件复位。

Device controller mode

In device controller mode, set these bits using a SetFeature request from the USB host during high-speed communication. The USBHS does not enter the Suspend state while these bits are 0001b to 0100b. To return to normal USB communication after setting a test mode, issue a hardware reset.

29.2.7 CFIFO/ CFIFOL/ CFIFOH/ CFIFOLL/ CFIFOHH, DnFIFO/ DnFIFOL/ DnFIFOH/ DnFIFOLL/ DnFIFOHH : FIFO Port Register (n = 0, 1)

Base address: USBHS = 0x4011_1000

Offset address: 0x014 (CFIFO/CFIFOL/CFIFOLL)
0x016 (CFIFOH)
0x017 (CFIFOHH)
0x018 (DnFIFO/DnFIFOL/DnFIFOLL)
0x01A (DnFIFOH)
0x01B (DnFIFOHH)

Bit position:	31																													0
Bit field:	FIFOPORT[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FIFOPORT[31:0]*1	Read receive data from the FIFO buffer or write transmit data to the FIFO buffer by accessing these bits.	R/W

Note 1. The valid bits depend on the MBW[1:0] and BIGEND settings in the associated port selection register.

Three FIFO ports are provided:

- CFIFO
- D0FIFO
- D1FIFO

Each FIFO port is configured with:

- A port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR)

Each FIFO port has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port
- Access to the FIFO buffer for DMA or DTC transfers is through the D0FIFO or D1FIFO port
- The D0FIFO and D1FIFO ports can also be accessed by the CPU
- When using functions specific to the FIFO port, such as the DMA or DTC transfer function, you cannot change the pipe number selected in the CURPIPE[3:0] bits of the Port Selection Register
- Registers configuring one FIFO port do not affect other FIFO ports
- The same pipe must not be assigned to two or more FIFO ports
- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU

FIFOPORT bits (FIFOPORT[31:0])

When the FIFOPORT bits is accessed, the USBHS reads the received data from the FIFO buffer or writes the transmission data to the FIFO buffer. The FIFO port register can be accessed only when the FRDY flag in the associated port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

设备控制器模式

在设备控制器模式下，在高速通信期间使用来自USB主机的SetFeature请求设置这些位。
当这些位为0001b至0100b时，USBHS不会进入暂停状态。要在设置测试模式后返回正常USB通信，请发出硬件复位。

29.2.7 CFIFO/ CFIFOL/ CFIFOH/ CFIFOLL/ CFIFOHH, DnFIFO/ DnFIFOL/ DnFIFOH/ DnFIFOLLDnFIFOHH:FIFO端口寄存器(n=0 1)

Base address: USBHS = 0x4011_1000

Offset address: 0x014 (CFIFO/CFIFOL/CFIFOLL)
0x016 (CFIFOH)
0x017 (CFIFOHH)
0x018 (DnFIFO/DnFIFOL/DnFIFOLL)
0x01A (DnFIFOH)
0x01B (DnFIFOHH)

Bit position:	31																													0
Bit field:	FIFOPORT[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FIFOPORT[31:0]*1	通过访问这些位从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。	R/W

注1.有效位取决于相关端口选择寄存器中的MBW[1:0]和BIGEND设置。

提供了三个FIFO端口：

- CFIFO
- D0FIFO
- D1FIFO

每个FIFO端口配置有：

●一个端口寄存器（CFIFO、D0FIFO或D1FIFO），用于处理从FIFO缓冲区读取数据并将数据写入FIFO缓冲区

●端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL），用于选择分配给FIFO端口的管道

●一个端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）

每个FIFO端口具有以下约束：

●通过CFIFO端口访问DCP控制传输的FIFO缓冲区

●通过D0FIFO或D1FIFO端口访问DMA或DTC传输的FIFO缓冲区

●D0FIFO和D1FIFO端口也可以被CPU访问

●当使用特定于FIFO端口的功能时，例如DMA或DTC传输功能，您无法更改端口选择寄存器的CURPIPE[3:0]位中选择的管道编号

●配置一个FIFO端口的寄存器不会影响其他FIFO端口

●不能将同一管道分配给两个或多个FIFO端口

●有两种FIFO缓冲区状态，一种授予CPU访问权限，另一种授予串行接口引擎(SIE)。当SIE有访问权限时，CPU不能访问FIFO缓冲区

FIFOPORT bits (FIFOPORT[31:0])

当访问FIFOPORT位时，USBHS从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。只有当相关端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）中的FRDY标志为1时，才能访问FIFO端口寄存器。

The valid bits in the FIFO port register depend on the MBW[1:0] and BIGEND settings in the port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL). See Table 29.6 to Table 29.8.

Table 29.6 Endian operation in 32-bit access (MBW[1:0] = 10b)

BIGEND	CFIFO, D0FIFO, D1FIFO b31 to b24	CFIFO, D0FIFO, D1FIFO b23 to b16	CFIFO, D0FIFO, D1FIFO b15 to b8	CFIFO, D0FIFO, D1FIFO b7 to b0	Remarks
0	Located at N+3	Located at N+2	Located at N+1	Located at N+0	Transmit data is sent from the address N +0. Receive data is stored from the address N+0.
1	Located at N+0	Located at N+1	Located at N+2	Located at N+3	Transmission data is sent from the address N+3. Receive data is stored from the address N+3.

Table 29.7 Endian operation in 16-bit access (MBW[1:0] = 01b)

BIGEND	CFIFOL, D0FIFOL, D1FIFOL b15 to b8	CFIFOL, D0FIFOL, D1FIFOL b7 to b0	CFIFOH, D0FIFOH, D1FIFOH b15 to b8	CFIFOH, D0FIFOH, D1FIFOH b7 to b0	Remarks
0	Access prohibited*1		Located at N+1	Located at N+0	Transmit data is sent from the address N +0. Receive data is stored from the address N+0.
1	Located at N+0	Located at N+1	Access prohibited*1		Transmit data is sent from the address N +1. Receive data is stored from the address N+1.

Note 1. Writing to or reading from these areas is prohibited.

Table 29.8 Endian operation in 8-bit access (MBW[1:0] = 00b)

BIGEND	CFIFOLL, D1FIFOLL, D0FIFOLL	CFIFOHH, D1FIFOHH, D0FIFOHH
0	Access prohibited*1	Located at N+0
1	Located at N+0	Access prohibited*1

Note 1. Writing to or reading from these locations is prohibited.

29.2.8 CFIFOSEL : CFIFO Port Selection Register

Base address: USBHS = 0x4011_1000

Offset address: 0x020

Bit position:	15	14	13	12	11	9	8	7	6	5	4	3	0
Bit field:	RCNT	REW	—	—	MBW[1:0]	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]	
Value after reset:	0	0	x	x	0	0	x	0	x	x	0	x	0 0 0 0 0

FIFO端口寄存器中的有效位取决于端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）中的MBW[1:0]和BIGEND设置。见表29.6至表29.8。

Table 29.6 32位访问中的字节序操作(MBW[1:0]=10b)

BIGEND	CFIFO, D0FIFO, D1FIFO b31 to b24	CFIFO, D0FIFO, D1FIFO b23 to b16	CFIFO, D0FIFO, D1FIFO b15 to b8	CFIFO, D0FIFO, D1FIFO b7 to b0	Remarks
0	位于N+3	位于N+2	位于N+1	位于N+0	发送数据从地址N+0发送。接收数据从地址N+0开始存储。
1	位于N+0	位于N+1	位于N+2	位于N+3	传输数据从地址N+3发送。接收数据从地址N+3开始存储。

Table 29.7 16位访问中的字节序操作(MBW[1:0]=01b)

BIGEND	CFIFOL, D0FIFOL, D1FIFOL b15 to b8	CFIFOL, D0FIFOL, D1FIFOL b7 to b0	CFIFOH, D0FIFOH, D1FIFOH b15 to b8	CFIFOH, D0FIFOH, D1FIFOH b7 to b0	Remarks
0	禁止访问*1		位于N+1	位于N+0	发送数据从地址N+0发送。接收数据从地址N+0开始存储。
1	位于N+0	位于N+1	禁止访问*1		发送数据从地址N+1发送。接收数据从地址N+1开始存储。

注1.禁止向这些区域写入或读取。

Table 29.8 8位访问中的字节序操作(MBW[1:0]=00b)

BIGEND	CFIFOLL, D1FIFOLL, D0FIFOLL	CFIFOHH, D1FIFOHH, D0FIFOHH
0	禁止访问*1	位于N+0
1	位于N+0	禁止访问*1

注1.禁止向这些位置写入或读取。

29.2.8 CFIFOSEL:CFIFO端口选择寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x020

Bit position:	15	14	13	12	11	9	8	7	6	5	4	3	0
Bit field:	RCNT	REW	—	—	MBW[1:0]	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]	
重置后的值:	0	0	x	x	0	0	x	0	x	x	0	x	0 0 0 0 0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	FIFO Port Access Pipe Specification 0x0: DCP (default control pipe) 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3 0x4: Pipe 4 0x5: Pipe 5 0x6: Pipe 6 0x7: Pipe 7 0x8: Pipe 8 0x9: Pipe 9 Others: Setting prohibited	R/W
4	—	The read value is undefined. The write value should be 0.	R/W
5	ISEL	FIFO Port Access Direction when DCP Is Selected 0: Select reading from the FIFO buffer 1: Select writing to the FIFO buffer	R/W
7:6	—	The read values are undefined. The write value should be 0.	R/W
8	BIGEND	FIFO Port Endian Control 0: Little endian 1: Big endian	R/W
9	—	The read value is undefined. The write value should be 0.	R/W
11:10	MBW[1:0]	CFIFO Port Access Bit Width 0 0: 8-bit width 0 1: 16-bit width 1 0: 32-bit width 1 1: Setting prohibited	R/W
13:12	—	The read values are undefined. The write value should be 0.	R/W
14	REW	Buffer Pointer Rewind 0: Do not rewind buffer pointer (Writing 0 has no effect.) 1: Rewind buffer pointer	W
15	RCNT	Read Count Mode 0: Clear DTLN[11:0] flags in the FIFO port control register to 000h when all receive data is read from CFIFO 1: Decrement DTLN[11:0] flags each time receive data is read from CFIFO	R/W

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number used to read or write data through the CFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, the pipe specification is maintained until the access is complete, even if the software attempts to change the CURPIPE[3:0] setting. Access continues after the current value is written back to the CURPIPE[3:0] bits.

ISEL bit (FIFO Port Access Direction when DCP Is Selected)

After writing a new value to the ISEL bit while the DCP is the selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process. Set the ISEL and CURPIPE[3:0] bits simultaneously.

BIGEND bit (FIFO Port Endian Control)

Use the BIGEND bit to set the byte endian order of the CFIFO port to be the same as that selected in the endian selection register (MDE).

MBW[1:0] bits (CFIFO Port Access Bit Width)

The MBW[1:0] bits specify the bit width for accessing the CFIFO port.

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	FIFO端口访问管道规范 0x0：DCP（默认控制管道）0x 1：管道10x2：管道20x3：管道 30x4：管道40x5：管道50x6： 管道60x7：管道70x8：管道80x 9：管道9 其他：禁止设置	R/W
4	—	读取值未定义。写入值应为0。	R/W
5	ISEL	选择DCP时的FIFO端口访问方向 0：选择从FIFO缓冲区读取1：选择写入 FIFO缓冲区	R/W
7:6	—	读取的值未定义。写入值应为0。	R/W
8	BIGEND	FIFO端口字节序控制 0：小端1：大 端	R/W
9	—	读取值未定义。写入值应为0。	R/W
11:10	MBW[1:0]	CFIFO端口访问位宽 00：8位宽01：16位宽 10：32位宽11：禁止 设置	R/W
13:12	—	读取的值未定义。写入值应为0。	R/W
14	REW	缓冲区指针倒带 0：不回退缓冲区指针（写入0无效。）1：回退缓冲区指 针	W
15	RCNT	读取计数模式 0：当从CFIFO中读取所有接收数据时，将FIFO端口控制寄存器中的DTLN[11:0]标志 清除为000h 1：每次从CFIFO读取接收数据时递减DTLN[11:0]标志	R/W

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过CFIFO端口读取或写入数据的管道号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，管道规范一直保持到访问完成，即使软件尝试更改CURPIPE[3:0]设置。将当前值写回CURPIPE[3:0]位后继续访问。

ISEL位（选择DCP时的FIFO端口访问方向）

在DCP为选定管道时向ISEL位写入新值后，读取该位以检查写入的值是否与读取的值一致，然后再进行下一个过程。同时设置ISEL和CURPIPE[3:0]位。

BIGEND位（FIFO端口字节序控制）

使用BIGEND位将CFIFO端口的字节字节序设置为与在字节序选择寄存器(MDE)中选择的相同。

MBW[1:0]位（CFIFO端口访问位宽度）

MBW[1:0]位指定访问CFIFO端口的位宽。

RA生态工作室

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, set the CURPIPE[3:0] and MBW[1:0] bits simultaneously. The bit width cannot be changed from 8-bit to 16- or 32-bit, or from 16-bit to 32-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16- or 32-bit width is selected.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double-buffering when reading is already in progress, this setting enables reading either FIFO buffer from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the bit to 1, always check that the FRDY flag is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

When the RCNT bit set to 0, the USBHS clears the CFIFOCTR.DTLN[11:0] flags to 0 on finishing reading all of the received data in the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits, or after reading a single plane in double buffer mode.

With this bit set to 1, the USBHS decrements the value in the CFIFOCTR.DTLN[11:0] flags each time it reads data received from the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits.

29.2.9 DnFIFOSEL : DnFIFO Port Selection Register (n = 0, 1)

Base address: USBHS = 0x4011_1000

Offset address: 0x028 + 0x4 × n

Bit position:	15	14	13	12	11	9	8	7	6	5	4	3	0
Bit field:	RCNT	REW	DCLRM	DREQE	MBW[1:0]	—	BIGEND	—	—	—	—	CURPIPE[3:0]	
Value after reset:	0	0	0	0	0	0	x	0	x	x	x	x	0 0 0 0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	FIFO Port Access Pipe Specification 0x0: No pipe specification 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3 0x4: Pipe 4 0x5: Pipe 5 0x6: Pipe 6 0x7: Pipe 7 0x8: Pipe 8 0x9: Pipe 9 Others: Setting prohibited	R/W
7:4	—	The read values are undefined. The write value should be 0.	R/W
8	BIGEND	FIFO Port Endian Control 0: Little endian 1: Big endian	R/W
9	—	The read value is undefined. The write value should be 0.	R/W
11:10	MBW[1:0]	FIFO Port Access Bit Width 0 0: 8-bit width 0 1: 16-bit width 1 0: 32-bit width 1 1: Setting prohibited	R/W

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，读取以MBW为单位设置的访问大小。

当所选管道正在传输时，同时设置CURPIPE[3:0]和MBW[1:0]位。当数据写入FIFO缓冲区时，位宽不能从8位更改为16位或32位，或从16位更改为32位。

即使选择了16位或32位宽度，也可以通过字节访问控制写入奇数个字节。

REW位（缓冲区指针倒带）

REW位指定是否回绕缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在读取已经在进行时的双缓冲中，此设置允许从第一个条目读取任一FIFO缓冲区。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将该位设置为1之前，请始终检查FRDY标志是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

当RCNT位设置为0时，USBHS在完成读取分配给CURPIPE[3:0]位指定的管道的FIFO缓冲区中的所有接收数据后，将CFIFOCTR.DTLN[11:0]标志清除为0，或在双缓冲模式下读取单个平面后。

该位设置为1时，USBHS每次读取从分配给CURPIPE[3:0]位指定的管道的FIFO缓冲区接收的数据时都会递减CFIFOCTR.DTLN[11:0]标志中的值。

29.2.9 DnFIFOSEL:DnFIFO端口选择寄存器(n=0 1)

Base address: USBHS = 0x4011_1000

Offset address: 0x028 + 0x4 × n

Bit position:	15	14	13	12	11	9	8	7	6	5	4	3	0
Bit field:	RCNT	REW	DCLRM	DREQE	MBW[1:0]	—	BIGEND	—	—	—	—	CURPIPE[3:0]	
重置后的值：	0	0	0	0	0	0	x	0	x	x	x	x	0 0 0 0

Bit	Symbol	Function	R/W
3:0	CURPIPE[3:0]	FIFO端口访问管道规范 0x0：无管道规范0x1：管道10x2：管道20x3：管道30x4：管道40x5：管道50x6：管道60x7：管道70x8：管道80x9：管道9 其他：禁止设置	R/W
7:4	—	读取的值未定义。写入值应为0。	R/W
8	BIGEND	FIFO端口字节序控制 0：小端1：大端	R/W
9	—	读取值未定义。写入值应为0。	R/W
11:10	MBW[1:0]	FIFO端口访问位宽 00：8位宽01：16位宽10：32位宽11：禁止设置	R/W

Bit	Symbol	Function	R/W
12	DREQE	DMA/DTC Transfer Request Enable 0: Disable DMA/DTC transfer request 1: Enable DMA/DTC transfer request	R/W
13	DCLRM	Auto FIFO Buffer Clear Mode after Specified Pipe is Read 0: Disable auto buffer clear mode 1: Enable auto buffer clear mode	R/W
14	REW	Buffer Pointer Rewind 0: Do not rewind buffer pointer (writing 0 has no effect) 1: Rewind buffer pointer	W
15	RCNT	Read Count Mode 0: Clear DTLN[11:0] flags in the FIFO port control register to 000h when all receive data is read from DnFIFO (after read of a single plane in double buffer mode) 1: Decrement DTLN[11:0] flags each time receive data is read from DnFIFO	R/W

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number used to read or write data through the DnFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, the pipe specification is maintained until the access is complete, even if the software attempts to change the CURPIPE[3:0] setting. Access continues after the current value is written back to the CURPIPE[3:0] bits.

BIGEND bit (FIFO Port Endian Control)

Use the BIGEND bit to set the byte endian order of the D0FIFO or D1FIFO port to be the same as that selected in the endian selection register (MDE).

MBW[1:0] bits (FIFO Port Access Bit Width)

The MBW[1:0] bits specify the bit width for accessing the DnFIFO port.

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, set the CURPIPE[3:0] and MBW[1:0] bits simultaneously. The bit width cannot be changed from 8-bit to 16- or 32-bit, or from 16-bit to 32-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16- or 32-bit width is selected.

DREQE bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. Only change the settings of DREQE bit when the CURPIPE[3:0] bits are 0x0.

To enable DMA or DTC transfer requests, set this bit to 1 after setting the CURPIPE[3:0] bits to 0x0, and then set the CURPIPE[3:0] bits to the PIPE number for the transfer.

DCLRM bit (Auto FIFO Buffer Clear Mode after Specified Pipe is Read)

The DCLRM bit enables or disables automatic FIFO buffer clearing after data in the selected pipe is read.

When this bit is set to 1, on receiving a zero-length packet while the FIFO buffer assigned to the selected pipe is empty, or when reading of a received short packet is complete while the PIPECFG.BFRE bit is 1, the USBHS sets the BCLR bit in the FIFO port control register to 1.

When using the USBHS with the SOFCFG.BRDYM bit set to 1, set this bit to 0.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.

Bit	Symbol	Function	R/W
12	DREQE	DMADTC传输请求启用 0：禁用DMADTC传输请求1：启用DM ADTC传输请求	R/W
13	DCLRM	读取指定管道后自动FIFO缓冲区清除模式 0：禁用自动缓冲区清除模式1： 启用自动缓冲区清除模式	R/W
14	REW	缓冲区指针倒带 0：不倒回缓冲区指针（写0无效）1：倒回缓冲区指针	W
15	RCNT	读取计数模式 0：当从DnFIFO中读取所有接收数据时（在双缓冲模式下读取单个平面后），将FIFO端口控制寄存器中的DTLN[11:0]标志位清除为000h 1：每次从DnFIFO读取接收数据时，递减DTLN[11:0]标志	R/W

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。
当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过DnFIFO端口读取或写入数据的管道编号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，管道规范一直保持到访问完成，即使软件尝试更改CURPIPE[3:0]设置。将当前值写回CURPIPE[3:0]位后继续访问。

BIGEND位（FIFO端口字节序控制）

使用BIGEND位将D0FIFO或D1FIFO端口的字节字节序设置为与在字节序选择寄存器(MDE)中选择的相同。

MBW[1:0]位（FIFO端口访问位宽）

MBW[1:0]位指定访问DnFIFO端口的位宽。

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，读取以MBW为单位设置的访问大小。

当所选管道正在传输时，同时设置CURPIPE[3:0]和MBW[1:0]位。当数据写入FIFO缓冲区时，位宽不能从8位更改为16位或32位，或从16位更改为32位。

即使选择了16位或32位宽度，也可以通过字节访问控制写入奇数个字节。

DREQE位（DMADTC传输请求使能）

DREQE位启用或禁用DMA或DTC传输请求的发出。仅当CURPIPE[3:0]位为0x0时更改DREQE位的设置。

要启用DMA或DTC传输请求，请在将CURPIPE[3:0]位设置为0x0后将此位设置为1，然后将CURPIPE[3:0]位到用于传输的PIPE编号。

DCLRM位（读取指定管道后自动FIFO缓冲区清除模式）

在读取所选管道中的数据后，DCLRM位启用或禁用自动FIFO缓冲区清除。

当该位设置为1时，在分配给所选管道的FIFO缓冲区为空时接收到零长度数据包，或在PIPECFG.BFRE位为1时完成读取接收到的短数据包时，USBHS设置FIFO端口控制寄存器中的BCLR位为1。

当使用SOFCFG.BRDYM位设置为1的USBHS时，将此位设置为0。

REW位（缓冲区指针倒带）

REW位指定是否回绕缓冲区指针。

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double-buffering when reading is already in progress, this setting enables reading either FIFO buffer from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the bit to 1, always check that the FRDY flag is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

When the RCNT bit set to 0, the USBHS clears the DnFIFOCTR.DTLN[11:0] flags (n = 0, 1) to 0 on finishing reading all of the received data in the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits, or after reading a single plane in double buffer mode.

With this bit set to 1, the USBHS decrements the value in the CFIFOCTR.DTLN[11:0] flags each time it reads data received from the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits. When accessing DnFIFO with the PIPECFG.BFRE bit set to 1, set the RCNT bit to 0.

29.2.10 CFIFOCTR, DnFIFOCTR : FIFO Port Control Register (n = 0, 1)

Base address: USBHS = 0x4011_1000

Offset address: 0x022 (CFIFOCTR)
0x02A + 0x4 × n (DnFIFOCTR)

Bit position:	15	14	13	12	11											0
Bit field:	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Value after reset:	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	DTLN[11:0]	Receive Data Length Flag The meaning of the values differs depending on the RCNT bit setting in the port selection register. For details, see the description of the DTLN[11:0] bits.	R
12	—	The read value is undefined. The write value should be 0.	R/W
13	FRDY	FIFO Port Ready Flag 0: FIFO port access disabled 1: FIFO port access enabled	R
14	BCLR	CPU Buffer Clear 0: No operation (writing 0 has no effect) 1: Clear FIFO buffer on the CPU side	W
15	BVAL	FIFO Buffer Valid Flag Set this bit to 1 when data is completely written to the FIFO buffer on the CPU side for the selected pipe (CURPIPE[3:0] setting). 0: Invalid (writing 0 has no effect) 1: Writing ended	R/W

The CFIFOCTR, D0FIFOCTR, and D1FIFOCTR registers correspond to the CFIFO, D0FIFO, and D1FIFO buffers.

DTLN[11:0] flags (Receive Data Length Flag)

The DTLN[11:0] flags indicate the length of the receive data.

While the FIFO buffer is being read, the DTLN[11:0] bits indicate different values depending on the DnFIFOSEL.RCNT bit (n = 0, 1), as follows:

- RCNT = 0:
  The USBHS sets the DTLN[11:0] flags to indicate the length of the receive data until the CPU or DMA/DTC has read all of the received data in the FIFO buffer (or until it has read a single plane in double buffer mode).
  While the PIPECFG.BFRE bit is 1, the USBHS retains the length of the receive data until the BCLR bit is set to 1, even after all the data is read.
- RCNT = 1:

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在读取已经在进行时的双缓冲中，此设置允许从第一个条目读取任一FIFO缓冲区。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将该位设置为1之前，请始终检查FRDY标志是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

当RCNT位设置为0时，USBHS将DnFIFOCTR.DTLN[11:0]标志(n=0 1)清除为0，完成读取分配给CURPIPE中指定管道的FIFO缓冲区中的所有接收数据[3:0]位，或在双缓冲模式下读取单个平面后。

该位设置为1时，USBHS每次读取从分配给CURPIPE[3:0]位指定的管道的FIFO缓冲区接收的数据时都会递减CFIFOCTR.DTLN[11:0]标志中的值。当PIPECFG.BFRE位设置为1访问DnFIFO时，将RCNT位设置为0。

29.2.10 CFIFOCTR DnFIFOCTR:FIFO端口控制寄存器(n=0 1)

Base address: USBHS = 0x4011_1000

Offset address: 0x022 (CFIFOCTR)
0x02A + 0x4 × n (DnFIFOCTR)

Bit position:	15	14	13	12	11											0
Bit field:	BVAL	BCLR	FRDY	—	DTLN[11:0]											
重置后的值：	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	DTLN[11:0]	接收数据长度标志 这些值的含义因端口选择寄存器中的RCNT位设置而异。有关详细信息，请参见DTLN[11:0]位的说明。	R
12	—	读取值未定义。写入值应为0。	R/W
13	FRDY	FIFO端口就绪标志 0：禁止FIFO端口访问1：使能FIFO端口访问	R
14	BCLR	CPU缓冲区清除 0：无操作（写0无效）1：清除CPU端的FIFO缓冲区	W
15	BVAL	FIFO缓冲区有效标志 当数据完全写入所选管道的CPU端的FIFO缓冲区时，将此位设置为1（CURPIPE[3:0]设置）。 0：无效（写入0无效）1：写入结束	R/W

CFIFOCTR、D0FIFOCTR和D1FIFOCTR寄存器对应于CFIFO、D0FIFO和D1FIFO缓冲区。

DTLN[11:0]标志（接收数据长度标志）

DTLN[11:0]标志指示接收数据的长度。

在读取FIFO缓冲区时，DTLN[11:0]位指示不同的值，具体取决于DnFIFOSEL.RCNT位(n=0 1)，如下所示：

- RCNT = 0:
  USBHS设置DTLN[11:0]标志以指示接收数据的长度，直到CPU或DMADTC已读取FIFO缓冲区中的所有接收数据（或直到它在双缓冲区模式下读取单个平面）.当PIPECFG.BFRE位为1时，USBHS将保留接收数据的长度，直到BCLR位设置为1，即使在读取所有数据之后也是如此。
- RCNT = 1:

The USBHS decrements the value indicated in the DTLN[11:0] flags each time the CPU or DMA/DTC reads the receive data from the FIFO buffer. (The value is decremented by 1 when MBW[1:0] = 00b, by 2 when MBW[1:0] = 01b, and by 4 when MBW[1:0] = 10b.)
The USBHS sets these flags to 0 when all the data is read from the FIFO buffer. In double buffer mode, if data is received in one FIFO buffer plane before all of the data is read from the other plane, the USBHS sets these bits to indicate the length of the receive data in the latter plane when all of the data is read from the former plane.
When the RCNT bit is 1, reading the DTLN[11:0] flags while the FIFO buffer is being read returns the latest value within 150 ns after the FIFO port read cycle.

FRDY flag (FIFO Port Ready Flag)

The FRDY flag indicates whether the FIFO port can be accessed by the CPU or DMA/DTC.

In the following cases, the USBHS sets the FRDY flag to 1 but data cannot be read through the FIFO port because there is no data to be read:

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit is 1

In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer on the CPU for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBHS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBHS to clear both sets of FIFO buffers regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY flag in the FIFO port control register is 1 (set by the USBHS).

BVAL bit (FIFO Buffer Valid Flag)

Set the BVAL bit to 1 when data is completely written to the FIFO buffer on the CPU for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set this bit to 1 in the following cases:

- To transmit a short packet, set this bit to 1 after data is written
- To transmit a zero-length packet, set this bit to 1 before data is written to the FIFO buffer
- Set this bit to 1 after the specified number of data bytes is written for the pipe in continuous transfer mode, where the number is a natural integer multiple of the maximum packet size and less than the buffer size

The USBHS then switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

When the selected pipe is in use for transmission, simultaneously setting the BVAL flag and the BCLR bit to 1 causes the USBHS to clear the data that is already written and enables transmission of a zero-length packet. When data of the maximum packet size is written for the pipe in non-continuous transfer mode, the USBHS sets this bit to 1 and switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBHS). When the selected pipe is receiving, do not set the BVAL flag to 1.

每次CPU或DMADTC从FIFO缓冲区读取接收数据时，USBHS都会递减DTLN[11:0]标志中指示的值。（当MBW[1:0]=00b时该值减1，当MBW[1:0]=01b时减2，当MBW[1:0]=10b时减4。）USBHS将这些标志设置为0当从FIFO缓冲区中读取所有数据时。在双缓冲模式下，如果在一个FIFO缓冲平面中的数据在从另一个平面读取所有数据之前接收到数据，则USBHS设置这些位以指示在读取所有数据时后一个平面中接收数据的长度从前飞机。当RCNT位为1时，在读取FIFO缓冲区时读取DTLN[11:0]标志会在FIFO端口读取周期后150ns内返回最新值。

FRDY标志（FIFO端口就绪标志）

FRDY标志指示CPU或DMADTC是否可以访问FIFO端口。

在以下情况下，USBHS将FRDY标志设置为1，但由于没有数据可读取，因此无法通过FIFO端口读取数据：

●当分配给所选管道的FIFO缓冲区为空时，接收到一个长度为零的数据包

●PIPECFG.BFRE位为1时，接收到一个短数据包并完全读取数据

在这些情况下，将BCLR位设置为1以清除FIFO缓冲区，并启用下一个数据的发送和接收。

BCLR位（CPU缓冲区清除）

将BCLR位设置为1以清除CPU上所选管道的FIFO缓冲区。

当分配给所选管道的FIFO缓冲区设置为双缓冲区模式时，USBHS仅清除
即使两个平面都已启用读取，也有FIFO缓冲区。

当DCP为选定管道时，将BCLR位设置为1允许USBHS清除两组FIFO缓冲区，而不管CPU或SIE是否具有访问权限。要在SIE具有访问权限时清除缓冲区，请将DCPCTR.PID[1:0]位设置为00b（NAK响应），然后再将BCLR位设置为1。

当所选管道不是DCP时，仅在FIFO端口控制寄存器中的Frdy标志为1（由USBH设置）时，仅将1个写入BCLR位。

BVAL位（FIFO缓冲区有效标志）

当数据完全写入CPU上的FIFO缓冲区时，将BVAL位设置为1，用于
CURPIPE[3:0].

当所选管道正在传输时，在以下情况下将此位设置为1：

●发送短数据包，写入数据后将该位设置为1

●要发送零长度数据包，请在数据写入FIFO缓冲区之前将此位设置为1

●在连续传输模式下为管道写入指定数量的数据字节后，将此位设置为1，其中该数字是最大数据包大小的自然整数倍，并且小于缓冲区大小

然后USBHS将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

当所选管道用于传输时，同时将BVAL标志和BCLR位设置为1会导致
USBHS清除已写入的数据并启用零长度数据包的传输。当在非连续传输模式下为管道写入最大数据包大小的数据时，USBHS将该位设置为1，并将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

仅在FRDY位为1（由USBHS设置）时将1写入BVAL标志。当所选管道正在接收时，不要将BVAL标志设置为1。

29.2.11 INTENB0 : Interrupt Enable Register 0

Base address: USBHS = 0x4011_1000

Offset address: 0x030

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	—	The read values are undefined. The write value should be 0.	R/W
8	BRDYE	Buffer Ready Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
9	NRDYE	Buffer Not Ready Response Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
10	BEMPE	Buffer Empty Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
11	CTRE	Control Transfer Stage Transition Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
12	DVSE	Device State Transition Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
13	SOFE	Frame Number Update Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
14	RSME	Resume Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
15	VBSE	VBUS Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W

Note: The RSME, DVSE, and CTRE bits can only be set to 1 in device controller mode. Do not set these bits to 1 in host controller mode.

When a status flag in the INTSTS0 register sets to 1 and the associated interrupt request enable bit setting in the INTENB0 register is 1, the USBHS issues a USBHS interrupt request.

Regardless of the INTENB0 register setting, the status flag in the INTSTS0 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB0 register is switched from 0 to 1 while the associated status flag in the INTSTS0 register is set to 1, a USBHS interrupt is requested.

29.2.12 INTENB1 : Interrupt Enable Register 1

Base address: USBHS = 0x4011_1000

Offset address: 0x032

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	L1RSMENDE	LPMENDE	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE
Value after reset:	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

29.2.11 INTENB0:中断使能寄存器0

Base address: USBHS = 0x4011_1000

Offset address: 0x030

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	—	读取的值未定义。写入值应为0。	R/W
8	BRDYE	缓冲区就绪中断请求使能 0：禁止中断请求1：允许中断请求	R/W
9	NRDYE	缓冲区未就绪响应中断请求使能 0：禁止中断请求1：允许中断请求	R/W
10	BEMPE	缓冲区空中断请求使能 0：禁止中断请求1：允许中断请求	R/W
11	CTRE	控制传输级转换中断请求使能 0：禁止中断请求1：允许中断请求	R/W
12	DVSE	设备状态转换中断请求使能 0：禁止中断请求1：允许中断请求	R/W
13	SOFE	帧号更新中断请求使能 0：禁止中断请求1：允许中断请求	R/W
14	RSME	恢复中断请求使能 0：禁止中断请求1：允许中断请求	R/W
15	VBSE	VBUS中断请求使能 0：禁止中断请求1：允许中断请求	R/W

Note: RSME、DVSE和CTRE位只能在设备控制器模式下设置为1。不要在主机控制器模式下将这些位设置为1。

当INTSTS0寄存器中的状态标志设置为1并且INTENB0寄存器中相关的中断请求使能位设置为1时，USBHS发出USBHS中断请求。

无论INTENB0寄存器设置如何，INTSTS0寄存器中的状态标志都会设置为1，以响应满足相关条件的状态变化。

当INTENB0寄存器中的中断请求使能位从0切换到1时，而相关的状态标志在INTSTS0寄存器设置为1，请求USBHS中断。

29.2.12 INTENB1：中断使能寄存器1

Base address: USBHS = 0x4011_1000

Offset address: 0x032

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	L1RSMENDE	LPMENDE	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE
重置后的值:	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

Bit	Symbol	Function	R/W
0	PDDETINTE	PDDETINT Detection Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
3:1	—	The read values are undefined. The write value should be 0.	R/W
4	SACKE	Setup Transaction Normal Response Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
5	SIGNE	Setup Transaction Error Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
6	EOFERRE	EOF Error Detection Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
7	—	The read values are undefined. The write value should be 0.	R/W
8	LPMENDE	LPM Transaction End Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
9	L1RSMENDE	L1 Resume End Interrupt Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
10	—	The read values are undefined. The write value should be 0.	R/W
11	ATTCHE	Connection Detection Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
12	DTCHE	Disconnection Detection Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
13	—	The read values are undefined. The write value should be 0.	R/W
14	BCHGE	USB Bus Change Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W
15	OVRCRE	OVRCRE Interrupt Request Enable 0: Disable interrupt request 1: Enable interrupt request	R/W

When a status flag in the INTSTS1 register sets to 1 and the associated interrupt request enable bit setting in the INTENB1 register is 1, the USBHS issues a USBHS interrupt request.

Regardless of the INTENB1 register setting, the status flag in the INTSTS1 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB1 register is switched from 0 to 1 while the associated status flag in the INTSTS1 register is set to 1, a USBHS interrupt is requested.

29.2.13 BRDYENB : BRDY Interrupt Enable Register

Base address: USBHS = 0x4011_1000

Offset address: 0x036

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBRDYE[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PDDETINTE	PDDETINT检测中断请求使能 0：禁止中断请求1：允许中断请求	R/W
3:1	—	读取的值未定义。写入值应为0。	R/W
4	SACKE	设置事务正常响应中断请求使能 0：禁止中断请求1：允许中断请求	R/W
5	SIGNE	设置事务错误中断请求启用 0：禁止中断请求1：允许中断请求	R/W
6	EOFERRE	EOF错误检测中断请求使能 0：禁止中断请求1：允许中断请求	R/W
7	—	读取的值未定义。写入值应为0。	R/W
8	LPMENDE	LPM事务结束中断请求使能 0：禁止中断请求1：允许中断请求	R/W
9	L1RSMENDE	L1恢复结束中断使能 0：禁止中断请求1：允许中断请求	R/W
10	—	读取的值未定义。写入值应为0。	R/W
11	ATTCHE	连接检测中断请求使能 0：禁止中断请求1：允许中断请求	R/W
12	DTCHE	断线检测中断请求使能 0：禁止中断请求1：允许中断请求	R/W
13	—	读取的值未定义。写入值应为0。	R/W
14	BCHGE	USB总线更改中断请求启用 0：禁止中断请求1：允许中断请求	R/W
15	OVRCRE	OVRCRE中断请求使能 0：禁止中断请求1：允许中断请求	R/W

当INTSTS1寄存器中的状态标志设置为1并且INTENB1寄存器中相关的中断请求使能位设置为1时，USBHS发出USBHS中断请求。

无论INTENB1寄存器设置如何，INTSTS1寄存器中的状态标志都会设置为1，以响应满足相关条件的状态更改。

当INTENB1寄存器中的中断请求使能位从0切换到1时，而相关的状态标志在INTSTS1寄存器设置为1，请求USBHS中断。

29.2.13 BRDYENB:BRDY中断使能寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x036

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBRDYE[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBRDYE[9:0]	BRDY Interrupt Request Enable for Pipes [9:0]*1 0: Disable interrupt request 1: Enable interrupt request	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.

The BRDYENB register enables or disables the INTSTS0.BRDY bit to be set to 1 when a BRDY interrupt is detected for each pipe.

When a status flag in the BRDYSTS register sets to 1 and the associated PIPEBRDYEn (n = 9 to 0) bit setting in the BRDYENB register is 1, the INTSTS0.BRDY flag sets to 1. In this case, if the BRDYE bit in INTENB0 is 1, the USBHS generates a BRDY interrupt request. While at least one PIPEBRDYEn flag indicates 1, the INTSTS0.BRDY flag sets to 1 when the associated interrupt request enable bit in the BRDYENB register is changed from 0 to 1 by software.

29.2.14 NRDYENB : NRDY Interrupt Enable Register

Base address: USBHS = 0x4011_1000

Offset address: 0x038

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPENRDYE[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPENRDYE[9:0]	NRDY Interrupt Enable for Pipes [9:0]*1 0: Disable interrupt request 1: Enable interrupt request	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.

The NRDYENB register enables or disables the INTSTS0.NRDY bit to be set to 1 when a NRDY interrupt is detected for each pipe.

When a status flag in the NRDYSTS register sets to 1 and the associated PIPENRDYEn (n = 0 to 9) bit setting in the NRDYENB register is 1, the INTSTS0.NRDY flag sets to 1. In this case, if the NRDYE bit in INTENB0 is 1, the USBHS generates a NRDY interrupt request. While at least one PIPEBRDYEn flag indicates 1, the INTSTS0.NRDY flag sets to 1 when the associated interrupt request enable bit in the NRDYENB register is changed from 0 to 1 by software.

29.2.15 BEMPENB : BEMP Interrupt Enable Register

Base address: USBHS = 0x4011_1000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBEMPE[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBEMPE[9:0]	BEMP Interrupt Enable for Pipes [9:0]*1 0: Disable interrupt request 1: Enable interrupt request	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.

Bit	Symbol	Function	R/W
9:0	PIPEBRDYE[9:0]	管道的BRDY中断请求启用[9:0]*1 0：禁止中断请求1：允许中断请求	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.每个位号对应相同的管道号。

当检测到每个管道的BRDY中断时，BRDYENB寄存器启用或禁用INTSTS0.BRDY位以设置为1。

当BRDYSTS寄存器中的状态标志设置为1并且相关的PIPEBRDYEn（n=9到0）位设置BRDYENB寄存器为1，INTSTS0.BRDY标志置1。这种情况下，如果INTENB0中的BRDYE位为1，USBHS产生一个BRDY中断请求。虽然至少有一个PIPEBRDYEn标志指示1，但当BRDYENB寄存器中的相关中断请求使能位由软件从0变为1时，INTSTS0.BRDY标志设置为1。

29.2.14 NRDYENB:NRDY中断使能寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x038

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPENRDYE[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPENRDYE[9:0]	NRDY中断使能管道[9:0]*1 0：禁止中断请求1：允许中断请求	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.每个位号对应相同的管道号。

当检测到每个管道的NRDY中断时，NRDYENB寄存器启用或禁用INTSTS0.NRDY位设置为1。

当NRDYSTS寄存器中的状态标志设置为1并且相关的PIPENRDYEn（n=0到9）位设置在NRDYENB寄存器为1，INTSTS0.NRDY标志设置为1。这种情况下，如果INTENB0中的NRDYE位为1，USBHS产生一个NRDY中断请求。虽然至少有一个PIPEBRDYEn标志指示1，但当NRDYENB寄存器中的相关中断请求使能位由软件从0变为1时，INTSTS0.NRDY标志设置为1。

29.2.15 BEMPENB:BEMP中断使能寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x03A

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBEMPE[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBEMPE[9:0]	管道的BEMP中断启用[9:0]*1 0：禁止中断请求1：允许中断请求	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.每个位号对应相同的管道号。

The BEMPENB register enables or disables the INTSTS0.BEMP bit to be set to 1 when a BEMP interrupt is detected for each pipe.

When a status flag in the BEMPSTS register sets to 1 and the associated PIPEBEMPEn (n = 0 to 9) bit setting in the BEMPENB register is 1, the INTSTS0.BEMP flag sets to 1. In this case, if the BEMPE bit in INTENB0 is 1, the USBHS generates a BEMP interrupt request. While at least one PIPEBEMPEn flag indicates 1, the INTSTS0.BEMP flag sets to 1 when the associated interrupt request enable bit in the BEMPENB register is changed from 0 to 1 by software.

29.2.16 SOFCFG : SOF Output Configuration Register

Base address: USBHS = 0x4011_1000

Offset address: 0x03C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	INTL	EDGESTS	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	0	x	0	0	0	x	x	x	x

Bit	Symbol	Function	R/W
3:0	—	The read values are undefined. The write value should be 0.	R/W
4	EDGESTS	Interrupt Edge Processing Status Flag*1 Indicates 1 during the edge processing of an edge interrupt output signal.	R
5	INTL	Interrupt Output Sense Select*2 0: Edge detection 1: Level detection	R/W
6	BRDYM	PIPEBRDY Interrupt Status Clear Timing*3 0: Clear BRDY flag through software 1: Clear BRDY flag by the USBHS through a data read from the FIFO buffer or data write to the FIFO buffer	R/W
7	—	The read values are undefined. The write value should be 0.	R/W
8	TRNENSEL	Transaction-Enabled Time Select*4 0: Not low-speed communication 1: Low-speed communication	R/W
15:9	—	The read values are undefined. The write value should be 0.	R/W

Note 1. Confirm that the EDGESTS flag is 0 before stopping the clock supply to the USBHS.
Note 2. When the INTL bit is set to 0, to stop the PHY clock (LPSTS.SUSPENDM = 0) after clearing the interrupt status, write 0 to the LPSTS.SUSPENDM bit after confirming that the EDGESTS flag is cleared to 0.
Note 3. When setting the BRDYM bit to 1, set the INTL bit to 1.
Note 4. The setting in the TRNENSEL bit is only valid in host controller mode. Even in host controller mode, the setting of this bit has no effect on the transaction-enabled time during high-speed communication.

EDGESTS flag (Interrupt Edge Processing Status Flag)

The EDGESTS flag indicates 1 during the edge processing of an edge interrupt output signal. Confirm that this flag is 0 before stopping the PHY clock.

BRDYM bit (PIPEBRDY Interrupt Status Clear Timing)

The BRDYM bit specifies how the BRDY interrupt status flags for the pipes are cleared.

TRNENSEL bit (Transaction-Enabled Time Select)

When the USB port is in use for full- or low-speed communications, the TRNENSEL bit specifies the timing with which the USBHS issues tokens in a frame (transaction-enabled time).

Set this bit to 1 when a low-speed device is connected through a hub. The bit is only valid in host controller mode. Set this bit to 0 when the interface is in use as a device controller.

当检测到每个管道的BEMP中断时，BEMPENB寄存器启用或禁用INTSTS0.BEMP位设置为1。

当BEMPSTS寄存器中的状态标志设置为1并且相关的PIPEBEMPEn（n=0到9）位设置在BEMPENB寄存器为1，INTSTS0.BEMP标志置1。这种情况下，如果INTENB0中的BEMPE位为1，USBHS产生一个BEMP中断请求。虽然至少有一个PIPEBEMPEn标志指示1，但当BEMPENB寄存器中的相关中断请求使能位由软件从0变为1时，INTSTS0.BEMP标志设置为1。

29.2.16 SOFCFG:SOF输出配置寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x03C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	INTL	EDGESTS	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	0	x	0	0	0	x	x	x	x

Bit	Symbol	Function	R/W
3:0	—	读取的值未定义。写入值应为0。	R/W
4	EDGESTS	中断边沿处理状态标志*1 在边沿中断输出信号的边沿处理期间表示1。	R
5	INTL	中断输出检测选择*2 0：边缘检测1：电平检测	R/W
6	BRDYM	PIPEBRDY中断状态清除时序*3 0：通过软件清除BRDY标志1：USBHS通过从FIFO缓冲区读取数据或向FIFO缓冲区写入数据清除BRDY标志	R/W
7	—	读取的值未定义。写入值应为0。	R/W
8	TRNENSEL	事务启用时间选择*4 0：非低速通讯1：低速通讯	R/W
15:9	—	读取的值未定义。写入值应为0。	R/W

注1.在停止向USBHS提供时钟之前，请确认EDGESTS标志为0。
注2.当INTL位设置为0时，要在清除中断状态后停止PHY时钟(LPSTS.SUSPENDM=0)，将0写入确认EDGESTS标志清零后的LPSTS.SUSPENDM位。
注3.将BRDYM位设置为1时，将INTL位设置为1。
注4.TRNENSEL位的设置仅在主机控制器模式下有效。即使在主机控制器模式下，该位的设置也不会影响高速通信期间的事务使能时间。

EDGESTS标志（中断边缘处理状态标志）

EDGESTS标志在边沿中断输出信号的边沿处理期间指示为1。在停止PHY时钟之前确认该标志为0。

BRDYM位（PIPEBRDY中断状态清除时序）

BRDYM位指定如何清除管道的BRDY中断状态标志。

TRNENSEL位（事务使能时间选择）

当USB端口用于全速或低速通信时，TRNENSEL位指定USBHS在一个帧中发布令牌（事务启用时间）。

当通过集线器连接低速设备时，将此位设置为1。该位仅在主机控制器模式下有效。当接口用作设备控制器时，将此位设置为0。

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29.2.17 PHYSET : PHY Setting Register

Base address: USBHS = 0x4011_1000

Offset address: 0x03E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HSEB	—	—	—	REPSTART	—	REPSEL[1:0]		—	—	CLKSEL[1:0]		CDPEN	—	PLLRESET	DIRPD
Value after reset:	x	x	x	x	0	x	0	0	x	x	1	1	0	x	1	1

Bit	Symbol	Function	R/W
0	DIRPD	Power-Down Control 0: Do not enter low power mode 1: Enter low power mode	R/W
1	PLLRESET	PLL Reset Control*1 0: Disable PLL reset control for UTMI_PHY 1: Enable PLL reset control for UTMI_PHY	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CDPEN	Charging Downstream Port Enable 0: Disable downstream port charging 1: Enable downstream port charging	R/W
5:4	CLKSEL[1:0]	Input System Clock Frequency 0 0: 12 MHz 0 1: Setting prohibited 1 0: 20 MHz 1 1: 24 MHz	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
9:8	REPSEL[1:0]	Terminating Resistance Adjustment Cycle 0 0: No cycle is set 0 1: Adjust terminating resistance at 16-second intervals 1 0: Adjust terminating resistance at 64-second intervals 1 1: Adjust terminating resistance at 128-second intervals	R/W
10	—	This bit is read as 0. The write value should be 0.	R/W
11	REPSTART	Forcibly Start Terminating Resistance Adjustment 0: Force terminating resistance adjustment to start 1: Do not force terminating resistance adjustment to start	R/W
14:12	—	These bits are read as 0. The write value should be 0.	R/W
15	HSEB	CL-only mode 0: Disable CL-only mode 1: Enable CL-only mode	R/W

Note 1. Because the value of the PLLRESET bit is 1 after a reset, changing the setting after release from the reset state is not required. Do not set the PLLRESET bit to 1 after setting the PLLRESET bit to 0. Operation is not guaranteed.

CLKSEL[1:0] bits (Input System Clock Frequency)

The CLKSEL[1:0] bits select the transfer clock source for the USBHS.

For the transfer clock generated in the USB-PHY internal PLL, these bits set the input clock frequency. To input the clock source from the EXTAL pin, the USB 2.0 clock specification must be strictly followed.

Writing to the CKSEL[1:0] bits is invalid in CL-only mode because the internal PLL is stopped (see the description for HSEB bit (CL-only mode)). For the clock settings, see section 29.3.3. Supplying the Clock.

HSEB bit (CL-only mode)

The HSEB bit selects whether the USBHS operates in CL-only mode. High-speed transfer by the USBHS requires the use of internal high-speed analog circuits including the PLL, clock, and data recovery (CDR) circuit in the USB-PHY block.

CL-only mode limits the transfer to the USB 1.1 specification (full- and low-speed transfer only). Power consumption can be reduced by stopping the internal PLL of the PHY module and other high-speed analog circuits.

29.2.17 PHYSET：PHY设置寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x03E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	HSEB	—	—	—	代表馅饼	—	REPSEL[1:0]		—	—	CLKSEL[1:0]		CDPEN	—	PLLRESET	DIRPD
重置后的值：	x	x	x	x	0	x	0	0	x	x	1	1	0	x	1	1

Bit	Symbol	Function	R/W
0	DIRPD	Power-Down Control 0：不进入低功耗模式1：进入低功耗模式	R/W
1	PLLRESET	PLL复位控制*1 0：禁用UTMI_PHY的PLL复位控制1：启用UTMI_PHY的PLL复位控制	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	CDPEN	充电下行端口使能 0：关闭下行端口充电1：开启下行端口充电	R/W
5:4	CLKSEL[1:0]	输入系统时钟频率 00：12MHz01：禁止 设置10：20MHz11：24MHz	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
9:8	REPSEL[1:0]	终止电阻调整周期 00：不设置周期01：每16秒调整一次终端电阻10：每64秒调整一次终端电阻11：每128秒调整一次终端电阻	R/W
10	—	该位读取为0。写入值应为0。	R/W
11	REPSTART	强制开始终止电阻调整 0：强制启动终端电阻调整1：不强制启动终端电阻调整	R/W
14:12	—	这些位被读取为0。写入值应为0。	R/W
15	HSEB	CL-only mode 0：禁用CL-only模式1：启用CL-only模式	R/W

注1.由于PLLRESET位的值在复位后为1，因此无需在从复位状态释放后更改设置。在将PLLRESET位设置为0后不要将PLLRESET位设置为1。不能保证操作。

CLKSEL[1:0]位（输入系统时钟频率）

CLKSEL[1:0]位选择USBHS的传输时钟源。

对于USB-PHY内部PLL中生成的传输时钟，这些位设置输入时钟频率。要从EXTAL引脚输入时钟源，必须严格遵循USB2.0时钟规范。

在CL-only模式下写入CKSEL[1:0]位无效，因为内部PLL已停止（请参见HSEB位（仅限CL模式））。有关时钟设置，请参阅第29.3.3节。提供时钟。

HSEB bit (CL-only mode)

HSEB位选择USBHS是否工作在CL-only模式。USBHS的高速传输需要使用内部高速模拟电路，包括USB-PHY模块中的PLL、时钟和数据恢复(CDR)电路。

仅CL模式将传输限制为USB1.1规范（仅限全低速传输）。通过停止PHY模块的内部PLL和其他高速模拟电路可以降低功耗。

In CL-only mode, the USBHS requires supply clocks of 48 MHz and 60 MHz, generated in the Clock Generation Circuit. For the clock supply method, see section 8, Clock Generation Circuit.

29.2.18 INTSTS0 : Interrupt Status Register 0

Base address: USBHS = 0x4011_1000

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6			3	2		0
Bit field:	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CTSQ[2:0]	Control Transfer Stage Flag*1 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error	R
3	VALID	USB Request Reception Flag*1 0: Setup packet not received 1: Setup packet received	R/W*3
6:4	DVSQ[2:0]	Device State*1 Indicates the device state. 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x : Suspend state	R
7	VBSTS	VBUS Input Status Flag 0: USBHS_VBUS pin is low 1: USBHS_VBUS pin is high	R
8	BRDY	BRDY Interrupt Status Flag 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R
9	NRDY	NRDY Interrupt Status Flag 0: No NRDY interrupt occurred 1: NRDY interrupt occurred	R
10	BEMP	BEMP Interrupt Status Flag 0: No BEMP interrupt occurred 1: BEMP interrupt occurred	R
11	CTRT	Control Transfer Stage Transition Interrupt Status Flag*2 0: No control transfer stage transition interrupt occurred 1: Control transfer stage transition interrupt occurred	R/W*3
12	DVST	Device State Transition Interrupt Status Flag*2 0: No device state transition interrupt occurred 1: Device state transition interrupt occurred	R/W*3
13	SOFR	Frame Number Refresh Interrupt Status Flag 0: No SOF interrupt occurred 1: SOF interrupt occurred	R/W*3
14	RESM	Resume Interrupt Status Flag*2 *4 0: No resume interrupt occurred 1: Resume interrupt occurred	R/W*3

在CL-only模式下，USBHS需要48MHz和60MHz的电源时钟，由时钟生成电路生成。
关于时钟提供方法，请参见第8节"时钟生成电路"。

29.2.18 INTSTS0：中断状态寄存器0

Base address: USBHS = 0x4011_1000

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6			3	2		0
Bit field:	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CTSQ[2:0]	控制传输阶段标志*1 000：空闲或设置阶段001：控制读取数据阶段010：控制读取状态阶段011：控制写入数据阶段100：控制写入状态阶段101：控制写入（无数据）状态阶段110：控制传输顺序错误	R
3	VALID	USB请求接收标志*1 0：未收到设置包1：收到设置包	R/W*3
6:4	DVSQ[2:0]	设备状态*1 指示设备状态。 000：通电状态001：默认状态010：地址状态011：配置状态1xx：挂起状态	R
7	VBSTS	VBUS输入状态标志 0：USBHS_VBUS引脚为低电平1：USBHS_VBUS引脚为高电平	R
8	BRDY	BRDY中断状态标志 0：未发生BRDY中断1：发生BRDY中断	R
9	NRDY	NRDY中断状态标志 0：未发生NRDY中断1：发生NRDY中断	R
10	BEMP	BEMP中断状态标志 0：未发生BEMP中断1：发生BEMP中断	R
11	CTRT	控制传输阶段转换中断状态标志*2 0：未发生控制转移阶段转换中断1：发生控制转移阶段转换中断	R/W*3
12	DVST	设备状态转换中断状态标志*2 0：未发生设备状态转换中断1：发生设备状态转换中断	R/W*3
13	SOFR	帧号刷新中断状态标志 0：未发生SOF中断1：发生SOF中断	R/W*3
14	RESM	恢复中断状态标志*2*4 0：未发生恢复中断1：发生恢复中断	R/W*3

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Bit	Symbol	Function	R/W
15	VBINT	VBUS Interrupt Status Flag*4 0: No VBUS interrupt occurred on detecting a change in the USBHS_VBUS pin 1: VBUS interrupt occurred on detecting a change in the USBHS_VBUS pin	R/W*3

Note 1. The CTSQ[2:0], VALID, and DVSQ[2:0] flags are only valid in device controller mode.
Note 2. The status of the CTRT, DVST, and RESM flags are changed only in device controller mode. Set the associated interrupt enable bits to 0 (disabled) in host controller mode.
Note 3. To clear the CTRT, DVST, SOFR, RESM, or VBINT flags, write 0 only to the flags to be cleared. Write 1 to the other flags. Do not write 0 to the status flags indicating 0.
Note 4. The USBHS detects a change in the status in the RESM or VBINT flag even while the clock supply is stopped (LPSTS.SUSPENDM = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status by software.

BRDY flag (BRDY Interrupt Status Flag)

The BRDY flag indicates the BRDY interrupt state. For the conditions that cause the flag to be set, see section 29.2.13. BRDYENB : BRDY Interrupt Enable Register.

The USBHS clears the BRDY flag to 0 when 0 is written to the BRDYSTS.PIPEBRDYn (n = 0 to 9) flags for all pipes for which the BRDY interrupt is enabled (BRDYENB.PIPEBRDYEn bits). Writing 0 to the BRDY flag in the software does not clear the flag.

NRDY flag (NRDY Interrupt Status Flag)

The NRDY flag indicates the NRDY interrupt state. For the conditions that cause the flag to be set, see section 29.2.14. NRDYENB : NRDY Interrupt Enable Register.

The USBHS clears the NRDY flag to 0 when 0 is written to the NRDYSTS.PIPENRDYn (n = 0 to 9) flags for all pipes for which the NRDY interrupt is enabled (NRDYENB.PIPENRDYEn bits). Writing 0 to the NRDY flag in the software does not clear the flag.

BEMP flag (BEMP Interrupt Status Flag)

The BEMP indicates the BEMP interrupt state. For the conditions that cause the flag to be set, see section 29.2.15. BEMPENB : BEMP Interrupt Enable Register.

The USBHS clears the BEMP flag to 0 when 0 is written to the BEMPSTS.PIPEBEMPn (n = 0 to 9) flags for all pipes for which the BEMP interrupt is enabled (BEMPENB.PIPEBEMPEn bits). Writing 0 to the BEMP flag in the software does not clear the flag.

CTRT flag (Control Transfer Stage Transition Interrupt Status Flag)

In device controller mode, the USBHS updates the value of the CTSQ[2:0] bits and sets the CTRT flag to 1 on detecting a transition in the control transfer stage. When a control transfer stage transition interrupt occurs, clear the CTRT flag before the USBHS detects the next control transfer stage transition.

Values read from the CTRT flag in host controller mode are invalid.

DVST flag (Device State Transition Interrupt Status Flag)

In device controller mode, the USBHS updates the value of the PL1CTRL1.DVSQ[3:0] bits and sets the DVST flag to 1 on detecting a change in the device state. When a device state transition interrupt occurs, clear the DVST flag before the USBHS detects the next device state transition.

Values read from the DVST flag in host controller mode are invalid.

SOFR flag (Frame Number Refresh Interrupt Status Flag)

In host controller mode, the USBHS sets the SOFR flag to 1 on updating the frame number when the DVSTCTR0.UACT bit is set to 1 by software. An SOFR interrupt is detected every 1 ms.

In device controller mode, the USBHS sets the SOFR flag to 1 on updating the frame number. An SOFR interrupt is detected every 1 ms. The USBHS can detect an SOFR interrupt through the SOF complementation function even when a corrupted SOF packet is received from the USB host. See section 29.3.13. SOF Complementation Function.

Bit	Symbol	Function	R/W
15	VBINT	VBUS中断状态标志*4 0：检测到USBHS_VBUS引脚变化时未发生VBUS中断1：检测到USBHS_VBUS引脚变化时发生VBUS中断	R/W*3

注1.CTSQ[2:0]、VALID和DVSQ[2:0]标志仅在设备控制器模式下有效。
注2.CTRT、DVST和RESM标志的状态仅在设备控制器模式下更改。在主机控制器模式下，将相关的中断使能位设置为0（禁用）。

注3.要清除CTRT、DVST、SOFR、RESM或VBINT标志，只需将0写入要清除的标志。将1写入其他标志。不要将0写入指示0的状态标志。

注4.即使在时钟供应停止(LPSTS.SUSPENDM=0)时，USBHS也会检测到RESM或VBINT标志的状态变化，并在相关中断请求位为1时请求中断。启用时钟供应在通过软件清除状态之前。

BRDY标志（BRDY中断状态标志）

BRDY标志指示BRDY中断状态。有关导致设置标志的条件，请参阅第29.2.13节。
BRDYENB：BRDY中断允许寄存器。

当0写入BRDYSTS.PIPEBRDYn（n=0到9）标志时，USBHS将BRDY标志清除为0，用于所有启用了BRDY中断的管道（BRDYENB.PIPEBRDYEn位）。在软件中将0写入BRDY标志不会清除该标志。

NRDY标志（NRDY中断状态标志）

NRDY标志指示NRDY中断状态。有关导致设置标志的条件，请参阅第29.2.14节。
NRDYENB：NRDY中断允许寄存器。

当0写入所有启用了NRDY中断的管道（NRDYENB.PIPENRDYEn位）的NRDYSTS.PIPENRDYn（n=0到9）标志时，USBHS将NRDY标志清除为0。在软件中将0写入NRDY标志不会清除该标志。

BEMP标志（BEMP中断状态标志）

BEMP指示BEMP中断状态。有关导致设置标志的条件，请参阅第29.2.15节。
BEMPENB：BEMP中断使能寄存器。

当0写入所有启用了BEMP中断的管道（BEMPENB.PIPEBEMPEn位）的BEMPSTS.PIPEBEMPn（n=0到9）标志时，USBHS将BEMP标志清除为0。在软件中将0写入BEMP标志不会清除该标志。

CTRT标志（控制传输阶段转换中断状态标志）

在设备控制器模式下，USBHS更新CTSQ[2:0]位的值并将CTRT标志设置为1检测到控制传输阶段的转换。当控制传输阶段转换中断发生时，在USBHS检测到下一个控制传输阶段转换之前清除CTRT标志。

在主机控制器模式下从CTRT标志读取的值无效。

DVST标志（设备状态转换中断状态标志）

在设备控制器模式下，USBHS更新PL1CTRL1.DVSQ[3:0]位的值并将DVST标志设置为1，以检测设备状态的变化。当设备状态转换中断发生时，在USBHS检测到下一个设备状态转换之前清除DVST标志。

在主机控制器模式下从DVST标志读取的值无效。

SOFR标志（帧号刷新中断状态标志）

在主机控制器模式下，当DVSTCTR0.UACT位被软件设置为1时，USBHS在更新帧号时将SOFR标志设置为1。每1ms检测一次SOFR中断。

在设备控制器模式下，USBHS在更新帧号时将SOFR标志设置为1。每1ms检测一次SOFR中断。即使从USB主机接收到损坏的SOF数据包，USBHS也可以通过SOF补充功能检测SOFR中断。请参阅第29.3.13节。SOF互补函数。

RESM flag (Resume Interrupt Status Flag)

In device controller mode, the USBHS sets the RESM flag to 1 on detecting the falling edge of the signal on the USBHS_DP pin in the Suspend state (PL1CTRL1.DVSQ[3:0] = 01xxb).

Values read from the RESM flag in host controller mode are invalid.

VBINT flag (VBUS Interrupt Status Flag)

The USBHS sets the VBINT flag to 1 on detecting a level change (high to low or low to high) in the USBHS_VBUS pin input value. The USBHS sets the VBSTS flag to indicate the USBHS_VBUS pin input value. When a VBINT interrupt occurs, eliminate transient elements by reading the VBSTS flag at least three times through software processing and check that the values read are the same.

29.2.19 INTSTS1 : Interrupt Status Register 1

Base address: USBHS = 0x4011_1000

Offset address: 0x042

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCR	BCHG	—	DTCH	ATTCH	—	L1RSMEND	LPMEND	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT
Value after reset:	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

Bit	Symbol	Function	R/W
0	PDDETINT	PDDET Detection Interrupt Status Flag*1 0: No PDDET interrupt occurred 1: PDDET interrupt occurred	R/W*2
3:1	—	The read values are undefined. The write value should be 0.	R/W
4	SACK	Setup Transaction Normal Response Interrupt Status Flag 0: No SACK interrupt occurred 1: SACK interrupt occurred	R/W*2
5	SIGN	Setup Transaction Error Interrupt Status Flag 0: No SIGN interrupt occurred 1: SIGN interrupt occurred	R/W*2
6	EOFERR	EOF Error Detection Interrupt Status Flag 0: No EOFERR interrupt occurred 1: EOFERR interrupt occurred	R/W*2
7	—	The read value is undefined. The write value should be 0.	R/W
8	LPMEND	LPM Transaction End Interrupt Status Flag 0: No LPMEND interrupt occurred 1: LPMEND interrupt occurred	R/W*2
9	L1RSMEND	L1 Resume End Interrupt Status Flag 0: No L1RSMEND interrupt occurred 1: L1RSMEND interrupt occurred	R/W*2
10	—	The read value is undefined. The write value should be 0.	R/W
11	ATTCH	USB Connection Detection Interrupt Status Flag 0: No ATTCH interrupt occurred 1: ATTCH interrupt occurred	R/W*2
12	DTCH	USB Disconnection Detection Interrupt Status Flag 0: No DTCH interrupt occurred 1: DTCH interrupt occurred	R/W*2
13	—	The read value is undefined. The write value should be 0.	R/W
14	BCHG	USB Bus Change Interrupt Status Flag*1 0: No BCHG interrupt occurred 1: BCHG interrupt occurred	R/W*2

RESM标志（恢复中断状态标志）

在设备控制器模式下，USBHS在检测到信号的下降沿时将RE SM标志设置为1
USBHS_DP引脚处于挂起状态(PL1CTRL1.DVSQ[3:0]=01xxb)。

在主机控制器模式下从RESM标志读取的值无效。

VBINT标志（VBUS中断状态标志）

USBHS在检测到USBHS_VBUS引脚输入值的电平变化（从高到低或从低到高）时将VBINT标志设置为1。USBHS设置VBSTS标志以指示USBHS_VBUS引脚输入值。当发生VBINT中断时，通过软件处理至少3次读取VBSTS标志来消除瞬态元素，并检查读取的值是否相同。

29.2.19 INTSTS1：中断状态寄存器1

Base address: USBHS = 0x4011_1000

Offset address: 0x042

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	OVRCR	BCHG	—	DTCH	ATTCH	—	L1RSMEND	LPMEND	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT
重置后的值：	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

Bit	Symbol	Function	R/W
0	PDDETINT	PDDET检测中断状态标志*1 0：未发生PDDET中断1：发生PDDET中断	R/W*2
3:1	—	读取的值未定义。写入值应为0。	R/W
4	SACK	设置事务正常响应中断状态标志 0：未发生SACK中断1：发生SACK中断	R/W*2
5	SIGN	设置事务错误中断状态标志 0：未发生SIGN中断1：发生SIGN中断	R/W*2
6	EOFERR	EOF错误检测中断状态标志 0：未发生EOFERR中断1：发生EOFERR中断	R/W*2
7	—	读取值未定义。写入值应为0。	R/W
8	LPMEND	LPM事务结束中断状态标志 0：未发生LPMEND中断1：发生LPMEND中断	R/W*2
9	L1RSMEND	L1恢复结束中断状态标志 0：未发生L1RSMEND中断1：发生L1RSMEND中断	R/W*2
10	—	读取值未定义。写入值应为0。	R/W
11	ATTCH	USB连接检测中断状态标志 0：未发生ATTCH中断1：发生ATTCH中断	R/W*2
12	DTCH	USB断线检测中断状态标志 0：未发生DTCH中断1：发生DTCH中断	R/W*2
13	—	读取值未定义。写入值应为0。	R/W
14	BCHG	USB总线改变中断状态标志*1 0：未发生BCHG中断1：发生BCHG中断	R/W*2

Bit	Symbol	Function	R/W
15	OVRCR	OVRCR Interrupt Status Flag*1 0: No OVRCR interrupt occurred 1: OVRCR interrupt occurred	R/W*2

Note: Only enable the status change interrupts indicated in the flags in INTSTS1 in host controller mode, except for the PDDET detection interrupt.

Note 1. The USBHS detects a change in the status in the PDDETINT, BCHG, or OVRCR flag even while the clock supply is stopped (LPSTS.SUSPENDM = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status by software. No other interrupts can be detected while the clock supply is stopped (LPSTS.SUSPENDM = 0).

Note 2. To clear the flags in INTSTS1, write 0 only to the flags to be cleared. Write 1 to the other bits.

PDDETINT flag (PDDET Detection Interrupt Status Flag)

The USBHS sets the PDDETINT flag to 1 on detecting a level change (high to low or low to high) in the PDDET pin input value. When the PDDETINT interrupt is generated, perform debouncing by reading the PDDETSTS flag at least three times through software processing and checking that the values read are the same.

SACK flag (Setup Transaction Normal Response Interrupt Status Flag)

The SACK flag indicates the status of the setup transaction normal response interrupt in host controller mode.

The USBHS detects the SACK interrupt and sets this bit to 1 when an ACK response is returned from a peripheral device during the setup transactions issued by the USBHS. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

Values read from the SACK flag in device controller mode are invalid.

SIGN flag (Setup Transaction Error Interrupt Status Flag)

The SIGN flag indicates the status of setup transaction error interrupts in host controller mode.

The USBHS detects the SIGN interrupt and sets this bit to 1 when an ACK response is not returned from a peripheral device three consecutive times during the setup transactions issued by the USBHS. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions:

- Timeout is detected by the USBHS when the peripheral device has returned no response
- A corrupted ACK packet is received
- A handshake other than ACK (NAK, NYET, or STALL) is received

Values read from the SIGN flag in device controller mode are invalid.

EOFERR flag (EOF Error Detection Interrupt Status Flag)

The EOFERR flag indicates the status of EOF error detection interrupts in host controller mode.

The USBHS detects the EOFERR interrupt and sets this bit to 1 on detecting that communication did not complete at the EOF2 timing defined in the USB 2.0 specification. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

After detecting the EOFERR interrupt, the USBHS controls the hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt was detected to 0
- Puts the port in which the EOFERR interrupt occurred into the idle state

The software must terminate all pipes in which communications are being carried out and re-enumerate the USB port.

Values read from the EOFERR flag in device controller mode are invalid.

LPMEND flag (LPM Transaction End Interrupt Status Flag)

The PLPMEND flag indicates the status of LPM transaction end interrupts in host controller mode.

Bit	Symbol	Function	R/W
15	OVRCR	OVRCR中断状态标志*1 0：未发生OVRCR中断1：发生OVRCR中断	R/W*2

Note: 仅在主机控制器模式下启用INTSTS1中标志指示的状态更改中断，PDDET检测中断除外。

注1.即使在时钟供应停止(LPSTS.SUSPENDM=0)时，USBHS也会检测到PDDETINT、BCHG或OVRCR标志的状态变化，并在相关中断请求位为1时请求中断。使能通过软件清除状态之前的时钟供应。停止提供时钟(LPSTS.SUSPENDM=0)时无法检测到其他中断。

注2.要清除INTSTS1中的标志，只需将0写入要清除的标志。将1写入其他位。

PDDETINT标志（PDDET检测中断状态标志）

USBHS在检测到PDDET引脚输入值的电平变化（从高到低或从低到高）时将PDDETINT标志设置为1。当产生PDDETINT中断时，通过软件处理至少3次读取PDDETSTS标志并检查读取的值是否相同来执行去抖动。

SACK标志（设置事务正常响应中断状态标志）

SACK标志指示主机控制器模式下设置事务正常响应中断的状态。

在USBHS发出的设置事务期间，当外围设备返回ACK响应时，USBHS检测到SACK中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

在设备控制器模式下从SACK标志读取的值无效。

SIGN标志（设置事务错误中断状态标志）

SIGN标志指示主机控制器模式下设置事务错误中断的状态。

在USBHS发出的设置事务期间，如果外围设备连续3次没有返回ACK响应，则USBHS检测到SIGN中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

当三个连续的设置事务发生以下任何响应条件时，USBHS检测到SIGN中断：

- ●当外围设备没有返回响应时，USBHS检测到超时
- ●收到损坏的ACK数据包
- ●收到ACK（NAK、NYET或STALL）以外的握手

在设备控制器模式下从SIGN标志读取的值无效。

EOFERR标志（EOF错误检测中断状态标志）

EOFERR标志指示主机控制器模式下EOF错误检测中断的状态。

USBHS检测到EOFERR中断并在检测到通信未完成时将该位设置为1
USB2.0规范中定义的EOF2时序。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

检测到EOFERR中断后，USBHS对硬件进行如下控制，而不考虑相关的中断使能位设置：

- ●将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- ●将发生EOFERR中断的端口置于空闲状态

软件必须终止正在执行通信的所有管道并重新枚举USB端口。

在设备控制器模式下从EOFERR标志读取的值无效。

LPMEND标志（LPM事务结束中断状态标志）

PLPMEND标志指示主机控制器模式下LPM事务结束中断的状态。

When the HL1CTRL1.L1REQ bit sets to 1, the USBHS sends an LPM token. When the LPM transaction is ended because a response from the function device or a timeout is detected, the USBHS sets this flag to 1.

Values read from the LPMEND flag in device controller mode are invalid.

L1RSMEND flag (L1 Resume End Interrupt Status Flag)

The L1RSMEND flag indicates the status of L1 resume end interrupts in host controller mode.

When performing resume processing after transitioning to the L1 state because an ACK was received in response to an LPM token, the USBHS sets this flag to 1.

Values read from the L1RSMEND flag in device controller mode are invalid.

ATTCH flag (USB Connection Detection Interrupt Status Flag)

The ATTCH flag indicates the status of USB attach detection interrupts in host controller mode.

The USBHS detects the ATTCH interrupt and sets this bit to 1 on detecting a J- or K-state on the full- or low-speed signal level for 2.5 µs. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS detects the ATTCH interrupt on any of the following conditions:

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs

Values read from the ATTCH flag in device controller mode are invalid.

DTCH flag (USB Disconnection Detection Interrupt Status Flag)

The DTCH flag indicates the status of USB detach detection interrupts in host controller mode.

The USBHS detects the DTCH interrupt and sets this bit to 1 on detecting a USB bus detach event. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS detects bus detach events based on the USB 2.0 specification.

After detecting the DTCH interrupt, the USBHS controls hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt was detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state

The software must terminate all pipes in which communications are being carried out and invoke the wait state for attaching to the USB port (waiting for ATTCH interrupt generation).

Values read from the DTCH flag in device controller mode are invalid.

BCHG flag (USB Bus Change Interrupt Status Flag)

The BCHG flag indicates the status of USB bus change interrupts in host controller mode.

The USBHS detects the BCHG interrupt and sets this bit to 1 when a change in the full-speed signal level occurs on the USB port. This includes any change from J-state, K-state, or SE0 to J-state, K-state, or SE0. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS sets the SYSSTS0.LNST[1:0] flags to indicate the input state of the USB port. When a BCHG interrupt occurs, eliminate transient elements by repeat reading the LNST[1:0] bits by software until the same value is read at least three times.

Changes in the USB bus state can be detected while the PHY clock is stopped.

Values read from the BCHG flag in device controller mode are invalid.

OVRCR flag (OVRCR Interrupt Status Flag)

The OVRCR flag indicates the input status on the USBHS_OVCUR0A pin or changes on the USBHS_OVCUR0B pin. If the INTENB1.OVRCRE bit sets to 1, the USBHS requests the interrupt.

The USBHS sets the SYSSTS0.OVCMON[1:0] flags to indicate the input state of the USBHS_OVCUR0A and USBHS_OVCUR0B pins.

当HL1CTRL1.L1REQ位设置为1时，USBHS发送一个LPM令牌。当LPM事务因检测到来自功能设备的响应或超时而结束时，USBHS将此标志设置为1。

在设备控制器模式下从LPMEND标志读取的值无效。

L1RSMEND标志（L1恢复结束中断状态标志）

L1RSMEND标志指示主机控制器模式下L1恢复结束中断的状态。

在转换到L1状态后执行恢复处理时，因为接收到响应LPM令牌的ACK，USBHS将此标志设置为1。

在设备控制器模式下从L1RSMEND标志读取的值无效。

ATTCH标志（USB连接检测中断状态标志）

ATTCH标志指示主机控制器模式下USB连接检测中断的状态。

USBHS检测到ATTCH中断，并在检测到全速或低速信号电平上的JorK状态持续2.5µs时将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

USBHS在以下任何条件下检测ATTCH中断：

- K-state、SE0或SE1变为J-state，J-state持续2.5µs
- J-state、SE0或SE1变为K-state，K-state持续2.5µs

在设备控制器模式下从ATTCH标志读取的值无效。

DTCH标志（USB断开检测中断状态标志）

DTCH标志指示主机控制器模式下USB分离检测中断的状态。

USBHS检测到DTCH中断并在检测到USB总线分离事件时将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

USBHS根据USB2.0规范检测总线分离事件。

检测到DTCH中断后，USBHS对硬件进行如下控制，而不管相关的中断使能位设置如何：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态

软件必须终止正在执行通信的所有管道并调用等待状态以连接到USB端口（等待ATTCH中断生成）。

在设备控制器模式下从DTCH标志读取的值无效。

BCHG标志（USB总线更改中断状态标志）

BCHG标志指示主机控制器模式下USB总线更改中断的状态。

当全速信号电平发生变化时，USBHS检测到BCHG中断并将该位设置为1。
USB端口。这包括从J-state、K-state或SE0到J-state、K-state或SE0的任何更改。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

USBHS设置SYSSTS0.LNST[1:0]标志以指示USB端口的输入状态。当发生BCHG中断时，通过软件重复读取LNST[1:0]位来消除瞬态元素，直到至少读取3次相同的值。

当PHY时钟停止时，可以检测到USB总线状态的变化。

在设备控制器模式下从BCHG标志读取的值无效。

OVRCR标志（OVRCR中断状态标志）

OVRCR标志指示USBHS_OVCUR0A引脚上的输入状态或USBHS_OVCUR0B引脚上的变化。如果INTENB1.OVRCRE位设置为1，则USBHS请求中断。

USBHS设置SYSSTS0.OVCMON[1:0]标志以指示USBHS_OVCUR0A的输入状态和
USBHS_OVCUR0B pins.

These pins allow overcurrent detection by software in host controller mode. To implement this function, connect the overcurrent signal from the external power supply IC that supplies VBUS to connected USB devices to the OVCUR0A or OVCUR0B pin. On detection of an OVRCR interrupt, eliminate transients by repeatedly reading the OVCMON[1:0] flags through the software until the same value is read at least three times.

29.2.20 BRDYSTS : BRDY Interrupt Status Register

Base address: USBHS = 0x4011_1000

Offset address: 0x046

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBRDY[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBRDY[9:0]	BRDY Interrupt Status Flag for Pipe[9:0]*1 0: No BRDY interrupt occurred 1: BRDY interrupt occurred	R/W*2
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.
Note 2. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated in the PIPEBRDY[9:0] flags, write 0 only to the bits to be cleared. Write 1 to the other bits.
When the SOFCFG.BRDYM bit is set to 0, clear BRDY interrupts before accessing the FIFO.

PIPEBRDY[9:0] flags (BRDY Interrupt Status Flag for Pipe[9:0])

When the BRDY interrupt is detected, the USBHS sets the associated bit in the PIPEBRDY[9:0] flags to 1. For details on BRDY interrupts, see section 29.3.6.1. BRDY interrupt.

29.2.21 NRDYSTS : NRDY Interrupt Status Register

Base address: USBHS = 0x4011_1000

Offset address: 0x048

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPENRDY[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPENRDY[9:0]	NRDY Interrupt Status Flag for Pipe[9:0]*1 0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W*2
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.
Note 2. To clear the status indicated in the PIPENRDY[9:0] flags, write 0 only to the bits to be cleared. Write 1 to the other bits.

PIPENRDY[9:0] flags (NRDY Interrupt Status Flag for Pipe[9:0])

If an internal NRDY interrupt is detected while the PID[1:0] bits in a pipe control register are 01b (BUF response), the USBHS sets the associated bit in the PIPENRDY[9:0] flags to 1. For details on NRDY interrupts, see section 29.3.6.2. NRDY interrupt.

这些引脚允许在主机控制器模式下通过软件进行过流检测。要实现此功能，请将来自为所连接的USB设备提供VBUS的外部电源IC的过流信号连接到OVCUR0A或OVCUR0B引脚。在检测到OVRCR中断时，通过软件重复读取OVCMON[1:0]标志来消除瞬变，直到至少读取相同的值3次。

29.2.20 BRDYSTS:BRDY中断状态寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x046

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBRDY[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBRDY[9:0]	Pipe[9:0]的BRDY中断状态标志*1 0：未发生BRDY中断1：发生BRDY中断	R/W*2
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.每个位号对应相同的管道号。
注2.当SOFCFG.BRDYM位设置为0时，要清除PIPEBRDY[9: 0]标志中指示的状态，仅将0写入要清除的位。将1写入其他位。当SOFCFG.BRDYM位设置为0时，在访问FIFO之前清除BRDY中断。

PIPEBRDY[9: 0]标志（管道[9:0]的BRDY中断状态标志）

当检测到BRDY中断时，USBHS将PIPEBRDY[9: 0]标志中的相关位设置为1。有关详细信息BRDY中断，参见第29.3.6.1节。BRDY中断。

29.2.21 NRDYSTS:NRDY中断状态寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x048

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPENRDY[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPENRDY[9:0]	Pipe[9:0]的NRDY中断状态标志*1 0：未发生NRDY中断1：发生NRDY中断。	R/W*2
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.每个位号对应相同的管道号。
注2.要清除PIPENRDY[9: 0]标志中指示的状态，仅将0写入要清除的位。将1写入其他位。

PIPENRDY[9: 0]标志（管道[9:0]的NRDY中断状态标志）

如果在管道控制寄存器中的PID[1:0]位为01b（BUF响应）时检测到内部NRDY中断，则USBHS将PIPENRDY[9: 0]标志中的相关位设置为1。有关NRDY的详细信息中断，见第29.3.6.2节。
NRDY interrupt.

29.2.22 BEMPSTS : BEMP Interrupt Status Register

Base address: USBHS = 0x4011_1000

Offset address: 0x04A

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBEMP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBEMP[9:0]	BEMP Interrupt Status Flag for Pipe[9:0]*1 0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W*2
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.
Note 2. To clear the status indicated in the PIPEBEMP[9:0] flags, write 0 only to the bits to be cleared. Write 1 to the other bits.

PIPEBEMP[9:0] flags (BEMP Interrupt Status Flag for Pipe[9:0])

If an BEMP interrupt is detected while the PID[1:0] bits in a pipe control register are 01b (BUF response), the USBHS sets the associated bit in the PIPEBEMP[9:0] flags to 1. For details on BEMP interrupts, see section 29.3.6.3. BEMP interrupt.

29.2.23 FRMNUM : Frame Number Register

Base address: USBHS = 0x4011_1000

Offset address: 0x04C

Bit position:	15	14	13	12	11	10										0
Bit field:	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FRNM[10:0]*1	Frame Number Flag	R
13:11	—	These bits are read as 0. The write value should be 0.	R/W
14	CRCE	CRC Error Detection Status Flag 0: No error occurred 1: Error occurred	R/W
15	OVRN	Overrun/Underrun Detection Status Flag 0: No error occurred 1: Error occurred.	R/W

Note 1. The OVRN flag is for debugging. Design the timing so that no overrun or underrun occurs in the system.

FRNM[10:0] flags (Frame Number Flag)

The USBHS sets the FRNM[10:0] flags to indicate the latest frame number, which is updated every 1 ms, when an SOF packet is issued or received.

CRCE flag (CRC Error Detection Status Flag)

The CRCE flag sets to 1 when a CRC error or bit stuffing error occurs during isochronous transfer. On detecting a CRC error, the USBHS generates an internal NRDY interrupt.

To clear the CRCE flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

29.2.22 BEMPSTS:BEMP中断状态寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x04A

Bit position:	15	14	13	12	11	10	9									0
Bit field:	—	—	—	—	—	—	PIPEBEMP[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	PIPEBEMP[9:0]	Pipe[9:0]的BEMP中断状态标志*1 0：未发生BEMP中断1：发生BEMP中断。	R/W*2
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.每个位号对应相同的管道号。
注2.要清除PIPEBEMP[9:0]标志中指示的状态，仅将0写入要清除的位。将1写入其他位。

PIPEBEMP[9:0]标志（管道[9:0]的BEMP中断状态标志）

如果在管道控制寄存器中的PID[1:0]位为01b（BUF响应）时检测到BEMP中断，则USBHS将PIPEBEMP[9:0]标志中的相关位设置为1。有关BEMP中断的详细信息，见第29.3.6.3节。BEMP中断。

29.2.23 FRMNUM:帧号寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x04C

Bit position:	15	14	13	12	11	10										0
Bit field:	OVRN	CRCE	—	—	—	FRNM[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	FRNM[10:0]*1	帧号标志	R
13:11	—	这些位被读取为0。写入值应为0。	R/W
14	CRCE	CRC错误检测状态标志 0：未发生错误1：发生错误	R/W
15	OVRN	溢出欠载检测状态标志 0：未发生错误1：发生错误。	R/W

注1.OVRN标志用于调试。设计时序，使系统不会发生溢出或欠载。

FRNM[10:0]标志（帧号标志）

USBHS设置FRNM[10:0]标志以指示最新的帧号，该帧号每1ms更新一次，当发出或接收SOF数据包时。

CRCE标志（CRC错误检测状态标志）

当同步传输期间发生CRC错误或位填充错误时，CRCE标志设置为1。在检测到CRC错误时，USBHS产生一个内部NRDY中断。

要清除CRCE标志，向其写入0，同时向FRMNUM寄存器中的其他位写入1。

OVRN flag (Overrun/Underrun Detection Status Flag)

The OVRN flag sets to 1 when an overrun or underrun error occurs during isochronous transfer. To clear the flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

In host controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the time to issue an OUT token comes before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the time to issue an IN token comes when no FIFO buffer planes are empty

In device controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the IN token is received before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the OUT token is received when no FIFO buffer planes are empty

29.2.24 UFRMNUM : µFrame Number Register

Base address: USBHS = 0x4011_1000

Offset address: 0x04E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
Bit field:	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]	
Value after reset:	0	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

Bit	Symbol	Function	R/W
2:0	UFRNM[2:0]	Microframe number	R
14:3	—	These bits are read as 0. The write value should be 0.	R/W
15	DVCHG	Device State Change 0: Disable writes to the USBADDR.STSRECOV0[2:0] and USBADDR.USBADDR[6:0] bits 1: Enable writes to the USBADDR.STSRECOV0[2:0] and USBADDR.USBADDR[6:0] bits	R/W

UFRNM[2:0] flags (Microframe number)

The USBHS sets the UFRNM[2:0] flags to indicate the microframe number during high-speed operation. When not in high-speed operation, the USBHS sets these bits to 00b.

Read these bits repeatedly until the same value is read twice.

29.2.25 USBADDR : USB Address Register

Base address: USBHS = 0x4011_1000

Offset address: 0x050

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	STSRECOV0[2:0]			—	USBADDR[6:0]						
Value after reset:	x	x	x	x	x	0	0	0	x	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	USBADDR[6:0]	USB Address Flag In device controller mode, these flags indicate the USB address assigned by the host when the USBHS processed the SET_ADDRESS request successfully.	R
7	—	The read value is undefined. The write value should be 0.	R/W

OVRN标志（溢出欠载检测状态标志）

当同步传输期间发生溢出或欠载错误时，OVRN标志设置为1。要清除该标志，请向其写入0，同时向FRMNUM寄存器中的其他位写入1。

在主机控制器模式下，OVRN标志在以下任何条件下设置为1：

●对于传输同步管道，发出OUT令牌的时间是在所有传输数据写入FIFO缓冲区之前

●对于接收同步管道，在没有FIFO缓冲平面为空时发出IN令牌

在设备控制器模式下，OVRN标志在以下任何条件下设置为1：

●对于传输同步管道，在所有传输数据写入FIFO缓冲区之前接收到IN令牌

●对于接收同步管道，当没有FIFO缓冲平面为空时接收OUT令牌

29.2.24 UFRMNUM:µFrame编号寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x04E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
Bit field:	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]	
重置后的值：	0	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

Bit	Symbol	Function	R/W
2:0	UFRNM[2:0]	Microframe number	R
14:3	—	这些位被读取为0。写入值应为0。	R/W
15	DVCHG	设备状态更改 0：禁止写入USBADDR.STSRECOV0[2:0]和USBADDR.USBADDR[6:0]位 1：允许写入USBADDR.STSRECOV0[2:0]和USBADDR.USBADDR[6:0]位	R/W

UFRNM[2:0] flags (Microframe number)

USBHS设置UFRNM[2:0]标志以指示高速操作期间的微帧数。当不在高速运行时，USBHS将这些位设置为00b。

重复读取这些位，直到读取两次相同的值。

29.2.25 USBADDR:USB地址寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x050

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	STSRECOV0[2:0]			—	USBADDR[6:0]						
重置后的值：	x	x	x	x	x	0	0	0	x	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	USBADDR[6:0]	USB地址标志 在设备控制器模式下，这些标志指示USBHS成功处理SET_ADDRESS请求时主机分配的USB地址。	R
7	—	读取值未定义。写入值应为0。	R/W

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Bit	Symbol	Function	R/W
10:8	STSRECOV0[2:0]	Status Recovery [D]: In deice controller mode [H]: In host controller mode (settings other than 010b, 100b, or 110b are prohibited) 0 0 0: Reserved 0 0 1: [D] Return to the full-speed connection and Default state 0 1 0: [D] Return to the full-speed connection and Address state [H] Return to the low-speed state (bits DVSTCTR0.RHST[2:0] = 001b) 0 1 1: [D] Return to the full-speed connection and Configured state 1 0 0: [D] Return to the suspend connection and Suspend state [H] Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b) 1 0 1: [D] Return to the high-speed connection and Default state 1 1 0: [D] Return to the high-speed connection and Address state [H] Return to the high-speed state (bits DVSTCTR0.RHST[2:0] = 011b) 1 1 1: [D] Return to the high-speed connection and Configured state	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W

USBADDR[6:0] flags (USB Address Flag)

In device controller mode, the USBADDR[6:0] flags indicate the USB address received when the USBHS processed a SetAddress request successfully. The USBHS sets the USBADDR[6:0] bits to 00b on detecting a USB bus reset.

In host controller mode, the USBADDR[6:0] bits are invalid.

STSRECOV0[2:0] bits (Status Recovery)

Use the STSRECOV[3:0] bits to resume the state of the internal sequencer on recovering from USB power shut-off. For details, see section 29.3.17. Release from Deep Software Standby Mode Because of USB Suspend/Resume Interrupts.

Writing to these bits is enabled while the DVCHGR.DVCHG bit is set to 1.

29.2.26 USBREQ : USB Request Type Register

Base address: USBHS = 0x4011_1000

Offset address: 0x054

Bit position:	15							7							0
Bit field:	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	BMREQUESTTYPE[7:0]	USB request bmRequestType value	R/W*1
15:8	BREQUEST[7:0]	USB request bRequest value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

BMREQUESTTYPE[7:0] bits (USB request bmRequestType value)

The BMREQUESTTYPE[7:0] bits hold the bmRequestType value of USB requests.

- In host controller mode:
  Set these bits to the value of the USB request data in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

BREQUEST[7:0] bits (USB request bRequest value)

The BREQUEST[7:0] bits hold the bRequest value of USB requests.

- In host controller mode:

Bit	Symbol	Function	R/W
10:8	STSRECOV0[2:0]	状态恢复[D]：除冰控制器模式[H]：主机控制器模式（禁止010b、100b或110b以外的设置） 000：保留001：[D]返回全速连接和默认状态010：[D]返回全速连接和地址状态 [H]返回低速状态（位DVSTCTR0.RHST[2:0]=001b） 011：[D]返回全速连接和配置状态100：[D]返回挂起连接和挂起状态 [H]返回全速状态（位DVSTTCTR0.RHST[2:0]=010b） 101：[D]返回高速连接和默认状态110：[D]返回高速连接和地址状态 [H]返回高速状态（位DVSTCT0.RHST[2:0]=011b） 111：[D]返回高速连接和配置状态	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W

USBADDR[6:0]标志（USB地址标志）

在设备控制器模式下，USBADDR[6:0]标志指示当USBHS处理一个SetAddress请求成功。USBHS在检测到USB总线复位时将USBADDR[6:0]位设置为00b。

在主机控制器模式下，USBADDR[6:0]位无效。

STSRECOV0[2:0] bits (Status Recovery)

使用STSRECOV[3:0]位在从USB电源关闭恢复时恢复内部定序器的状态。有关详细信息，请参阅第29.3.17节。由于USB挂起恢复中断而从深度软件待机模式中释放。

当DVCHGR.DVCHG位设置为1时，可以写入这些位。

29.2.26 USBREQ:USB请求类型寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x054

Bit position:	15							7							0
Bit field:	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	BMREQUESTTYPE[7:0]	USB请求bmRequestType值	R/W*1
15:8	BREQUEST[7:0]	USB请求bRequest值	R/W*1

注1.在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

BMREQUESTTYPE[7:0]位（USB请求bmRequestType值）

BMREQUESTTYPE[7:0]位保存USB请求的bmRequestType值。

●在主机控制器模式下：
在传输设置事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：
这些位指示接收设置事务中USB请求数据的值。写入位无效。

BREQUEST[7:0]位（USB请求bRequest值）

BREQUEST[7:0]位保存USB请求的bRequest值。

●在主机控制器模式下：

Set these bits to the value of the USB request data in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:
  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

29.2.27 USBVAL : USB Request Value Register

Base address: USBHS = 0x4011_1000

Offset address: 0x056

Bit position:	15															0
Bit field:	WVALUE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WVALUE[15:0]	USB request wValue value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

WVALUE[15:0] bits (USB request wValue value)

The WVALUE[15:0] bits hold the wValue value of USB requests.

- In host controller mode:
  Set these bits to the wValue value for USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wValue value of USB requests in reception setup transactions. Writing to the bits has no effect.

29.2.28 USBINDX : USB Request Index Register

Base address: USBHS = 0x4011_1000

Offset address: 0x058

Bit position:	15															0
Bit field:	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WINDEX[15:0]	USB request wIndex value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

WINDEX[15:0] bits (USB request wIndex value)

- In host controller mode:
  Set these bits to the wIndex value of USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wIndex value of USB requests received in reception setup transactions. Writing to the bits has no effect.

在传输设置事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：
这些位指示接收设置事务中USB请求数据的值。写入位无效。

29.2.27 USBVAL:USB请求值寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x056

Bit position:	15															0
Bit field:	WVALUE[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WVALUE[15:0]	USB请求wValue值	R/W*1

注1.在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写位。

WVALUE[15:0]位（USB请求wValue值）

WVALUE[15:0]位保存USB请求的wValue值。

●在主机控制器模式下：
将这些位设置为传输设置事务中USB请求的wValue值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：
这些位指示接收设置事务中USB请求的wValue值。写入位无效。

29.2.28 USBINDX:USB请求索引寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x058

Bit position:	15															0
Bit field:	WINDEX[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WINDEX[15:0]	USB请求wIndex值	R/W*1

注1.在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写位。

WINDEX[15:0]位（USB请求wIndex值）

●在主机控制器模式下：
将这些位设置为传输设置事务中USB请求的wIndex值。当DCPCTR.SUREQ位为1时，不要更改位的值。

●在设备控制器模式下：
这些位指示在接收设置事务中接收到的USB请求的wIndex值。写入位无效。

29.2.29 USBLENG : USB Request Length Register

Base address: USBHS = 0x4011_1000

Offset address: 0x05A

Bit position:	15															0
Bit field:	WLENTUH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WLENTUH[15:0]	USB request wLength value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

WLENTUH[15:0] bits (USB request wLength value)

The WLENTUH[15:0] bits hold the wLength value of USB requests.

- In host controller mode:
  Set the wLength value of USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wLength value of USB requests in reception setup transactions. Writing to the bits has no effect.

29.2.30 DCPCFG : DCP Configuration Register

Base address: USBHS = 0x4011_1000

Offset address: 0x05C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CNTMD	SHTNAK	—	—	DIR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	DIR	Transfer Direction 0: Data receiving direction 1: Data transmitting direction	R/W
6:5	—	The read values are undefined. The write value should be 0.	R/W
7	SHTNAK	Pipe Blocking on End of Transfer 0: Keep pipe open after transfer ends 1: Disable pipe after transfer ends	R/W
8	CNTMD	Continuous Transfer Mode 0: Non-continuous transfer mode 1: Continuous transfer mode	R/W
15:9	—	The read values are undefined. The write value should be 0.	R/W

Note: Only set the bits in the DCPCFG register while the PID is NAK. Before setting the bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBHS, checking the PBUSY bit through software is not necessary.

DIR bit (Transfer Direction)

In host controller mode, the DIR bit sets the transfer direction of the data stage and status stage for control transfers. In device controller mode, set the DIR bit to 0.

29.2.29 USBLENG:USB请求长度寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x05A

Bit position:	15															0
Bit field:	WLENTUH[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	WLENTUH[15:0]	USB请求wLength值	R/W*1

注1.在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写位。

WLENTUH[15:0]位（USB请求wLength值）

WLENTUH[15:0]位保存USB请求的wLength值。

- 在主机控制器模式下：
  在传输设置事务中设置USB请求的wLength值。不要更改位的值，而DCPCTR.SUREQ位为1。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求的wLength值。写入位无效。

29.2.30 DCPCFG:DCP配置寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x05C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CNTMD	SHTNAK	—	—	DIR	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	DIR	转移方向 0：数据接收方向1：数据发送方向	R/W
6:5	—	读取的值未定义。写入值应为0。	R/W
7	SHTNAK	传输结束时管道阻塞 0：传输结束后保持管道打开1：传输结束后禁用管道	R/W
8	CNTMD	连续传输模式 0：非连续传输模式1：连续传输模式	R/W
15:9	—	读取的值未定义。写入值应为0。	R/W

Note: 仅在PID为NAK时设置DCPCFG寄存器中的位。在设置这些位之前，检查DCPCTR.PBUSY位是否为0，然后将DCP的DCPCTR.PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBHS更改为NAK，则无需通过软件检查PBUSY位。

DIR位（传输方向）

在主机控制器模式下，DIR位设置控制传输的数据阶段和状态阶段的传输方向。在设备控制器模式下，将DIR位设置为0。

SHTNAK bit (Pipe Blocking on End of Transfer)

The SHTNAK bit specifies whether to change PID to NAK on transfer end when the selected pipe is receiving. It is only valid when the selected pipe is receiving.

When the SHTNAK bit is 1, the USBHS changes the DCPCTR.PID[1:0] bits for the DCP to NAK on determining that a transfer has ended. The USBHS determines transfer end on the following condition:

- A short packet, including a zero-length packet, is successfully received

CNTMD bit (Continuous Transfer Mode)

The CNTMD bit indicates whether transfer through the default control pipe is in continuous transfer mode.

29.2.31 DCPMAXP : DCP Maximum Packet Size Register

Base address: USBHS = 0x4011_1000

Offset address: 0x05E

Bit position:	15				11	10	9	8	7	6						0
Bit field:	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	x	x	x	x	x	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	MXPS[6:0]	Maximum Packet Size*1 Maximum data payload specification (maximum packet size) for the DCP	R/W
11:7	—	The read values are undefined. The write value should be 0.	R/W
15:12	DEVSEL[3:0]	Device Select*2 0x0: Address 0x0 0x1: Address 0x1 0x2: Address 0x2 0x3: Address 0x3 0x4: Address 0x4 0x5: Address 0x5	R/W

Note 1. Only set the MXPS[6:0] bits while PID is NAK. Before setting this bit, check that the CSSTS and PBUSY bits are 0, and then change the DCPCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK), and the CFIFOSEL.CURPIPE[3:0] bits to 0000b. If the DCPCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY bits through software is not necessary. After the MXPS[6:0] bits are set and the DCP is set to the CURPIPE[3:0] bits in a port select register, clear the buffer by setting the BCLR bit the port control register to 1.

Note 2. Only set the DEVSEL[3:0] bits while PID is NAK and the DCPCTR.SUREQ bits are 0. Before setting these bits, check that the CSSTS and PBUSY flags are 0, and then change the DCPCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK), and the DCPCTR.SUREQ[3:0] bits to 0. If the DCPCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY bits through software is not necessary.

MXPS[6:0] bits (Maximum Packet Size)

The MXPS[6:0] bits specify the maximum data payload (maximum packet size) for the DCP. The initial value is 0x40 (64 bytes). Set the bits to a USB 2.0-compliant value. Do not write to the FIFO buffer or set PID = BUF while MXPS[6:0] is set to 0.

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target peripheral device for a control transfer. Set up the device address in the associated DEVADDn (n = 0 to A) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register. In device controller mode, set these bits to 0000b.

SHTNAK位（传输结束时的管道阻塞）

SHTNAK位指定当所选管道正在接收时，是否在传输结束时将PID更改为NAK。仅在所选管道正在接收时有效。

当SHTNAK位为1时，USBHS在确定传输已经结束时将DCPCR.PID[1:0]位更改为NAK。USBHS在以下条件下确定传输结束：

●成功接收短包，包括零长度包

CNTMD位（连续传输模式）

CNTMD位指示通过默认控制管道的传输是否处于连续传输模式。

29.2.31 DCPMAXP:DCP最大数据包大小寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x05E

Bit position:	15				11	10	9	8	7	6						0
Bit field:	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
重置后的值:	0	0	0	0	x	x	x	x	x	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	MXPS[6:0]	最大数据包大小*1 DCP的最大数据有效负载规范（最大数据包大小）	R/W
11:7	—	读取的值未定义。写入值应为0。	R/W
15:12	DEVSEL[3:0]	设备选择*2 0x0: Address 0x0 0x1: Address 0x1 0x2: Address 0x2 0x3: Address 0x3 0x4: Address 0x4 0x5: Address 0x5	R/W

注1.仅在PID为NAK时设置MXPS[6:0]位。在设置该位之前，检查CSSTS和PBUSY位是否为0，然后将DCPCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)，以及CFIFOSEL.CURPIPE[3:0]位到0000b。如果DCPCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY位。在设置MXPS[6:0]位并将DCP设置为端口选择寄存器中的CURPIPE[3:0]位后，通过将端口控制寄存器的BCLR位设置为1来清除缓冲区。

注2.仅在PID为NAK且DCPCTR.SUREQ位为0时设置DEVSEL[3:0]位。在设置这些位之前，请检查CSSTS和PBUSY标志为0，然后将DCPCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)，然后DCPCTR.SUREQ[3:0]位为0。如果DCPCTR.PID[1:0]位被USBHS更改为00b(NAK)，请检查CSSTS和不需要通过软件进行PBUSY位。

MXPS[6:0]位（最大数据包大小）

MXPS[6:0]位指定DCP的最大数据有效载荷（最大数据包大小）。初始值为0x40（64字节）。将这些位设置为符合USB2.0的值。当MXPS[6:0]设置为0时，不要写入FIFO缓冲区或设置PID=BUF。

DEVSEL[3:0] bits (Device Select)

在主机控制器模式下，DEVSEL[3:0]位指定目标外围设备的地址以进行控制传输。首先在相关的DEVADDn（n=0到A）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。在设备控制器模式下，将这些位设置为0000b。

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29.2.32 DCPCTR : DCP Control Register

Base address: USBHS = 0x4011_1000

Offset address: 0x060

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	SUREQ	CSCLR	CSSTS	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	PINGE	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	x	x	x	0	0	1	0	0	x	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	Response PID 0 0: NAK response 0 1: BUF response (depends on buffer state) 1 0: STALL response 1 0: STALL response	R/W
2	CCPL	Control Transfer End Enable 0: Disable control transfer completion 1: Enable control transfer completion	R/W
3	—	The read value is undefined. The write value should be 0.	R/W
4	PINGE	PING Token Issue Enable*1 0: Disable PING token 1: Enable normal PING operation	R/W
5	PBUSY	Pipe Busy Flag 0: DCP not used for the USB bus 1: DCP in use for the USB bus	R
6	SQMON	Sequence Toggle Bit Monitor Flag 0: DATA0 1: DATA1	R
7	SQSET	Sequence Toggle Bit Set*1 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1	W
8	SQCLR	Sequence Toggle Bit Clear*1 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0	W
10:9	—	The read values are undefined. The write value should be 0.	R/W
11	SUREQCLR	SUREQ Bit Clear 0: Invalid (writing 0 has no effect) 1: Clear SUREQ to 0	W
12	CSSTS	CSSTS Status Flag 0: Start-split (SSPLIT) transaction, or processing for devices that are not using split transactions, in progress 1: Complete-split (CSPLIT) transaction in progress	R
13	CSCLR	CSSTS Status Flag Clear 0: (writing 0 has no effect) 1: Clear CSSTS to 0	W
14	SUREQ	SETUP Token Transmission 0: Invalid (writing 0 has no effect) 1: Transmit setup packet	R/W
15	BSTS	Buffer Status Flag 0: Buffer access disabled 1: Buffer access enabled	R

Note 1. Only set the SQSET, SQCLR, and PINGE bits while PID is NAK. Before setting these bits, check that the CSSTS and PBUSY bits are 0, and then change the DCPCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the DCPCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY bits through the software is not necessary.

29.2.32 DCPCTR:DCP控制寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x060

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	SUREQ	CSCLR	CSSTS	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	PINGE	—	CCPL	PID[1:0]	
重置后的值:	0	0	0	0	x	x	x	0	0	1	0	0	x	0	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	响应PID 00：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应10：STALL响应	R/W
2	CCPL	控制传输结束使能 0：禁止控制传输完成1：使能控制传输完成	R/W
3	—	读取值未定义。写入值应为0。	R/W
4	PINGE	PING令牌发布启用*1 0：禁用PING令牌1：启用正常PING操作	R/W
5	PBUSY	管道忙标志 0：USB总线不使用DCP1：USB总线使用DCP	R
6	SQMON	序列切换位监控标志 0: DATA0 1: DATA1	R
7	SQSET	序列切换位设置*1 0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1	W
8	SQCLR	序列切换位清除*1 0：无效（写0无效）1：清除下一笔交易的期望值到DATA0	W
10:9	—	读取的值未定义。写入值应为0。	R/W
11	SUREQCLR	SUEQ位清零 0：无效（写0无效）1：清除SUREQ为0	W
12	CSSTS	CSSTS状态标志 0：开始拆分(SSPLIT)事务，或正在处理未使用拆分事务的设备 1：完成拆分（CSPLIT）事务正在进行中	R
13	CSCLR	CSSTS状态标志清除 0：（写0无效）1：清除CSSTS为0	W
14	SUREQ	SETUP令牌传输 0：无效（写0无效）1：发送设置包	R/W
15	BSTS	缓冲区状态标志 0：禁止缓冲区访问1：允许缓冲区访问	R

注1.仅在PID为NAK时设置SQSET、SQCLR和PINGE位。在设置这些位之前，请检查CSSTS和PBUSY位是否为0，然后将DCPCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果DCPCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY位。

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PID[1:0] bits (Response PID)

The PID[1:0] bits control the USB response type during control transfers.

In host controller mode, to change the PID[1:0] setting from NAK to BUF:

- When the transmitting direction is set:
  a. Write all of the transmit data to the FIFO buffer while the DVSTCTR0.UACT bit is 1 and PID is NAK.
  b. Set PID[1:0] bits to 01b (BUF).
  The USBHS then executes the OUT transaction (or PING transaction)
- When the receiving direction is set:
  a. Check that the FIFO buffer is empty (or empty the buffer) while the DVSTCTR0.UACT bit is 1 and PID is NAK.
  b. Set PID[1:0] bits to 01b (BUF).
  The USBHS then executes the IN transaction.

The USBHS changes the PID[1:0] setting as follows:

- When the PID[1:0] bits are set to BUF (01b) by software and the USBHS has received data exceeding MaxPacketSize, the USBHS sets PID[1:0] to STALL (11b)
- When a reception error, such as a CRC error, is detected three times consecutively, the USBHS sets PID[1:0] to NAK (00b)
- On receiving the STALL handshake, the USBHS sets PID[1:0] to STALL (11b)

In device controller mode, the USBHS changes the PID[1:0] setting as follows:

- On receiving a setup packet, the USBHS sets PID[1:0] to NAK (00b). The USBHS then sets the INTSTS0.VALID flag to 1, and the PID[1:0] setting cannot be changed until the software clears the VALID flag to 0.
- When the PID[1:0] bits are set to BUF (01b) by software and the USBHS has received data exceeding MaxPacketSize, the USBHS sets PID[1:0] to STALL (11b)
- On detecting a control transfer sequence error, the USBHS sets PID[1:0] to STALL (1xb)
- On detecting a USB bus reset, the USBHS sets PID[1:0] to NAK

The USBHS does not check the PID[1:0] setting while processing a SET_ADDRESS request.

CCPL bit (Control Transfer End Enable)

In device controller mode, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed. When the bit is set to 1 by software while the associated PID[1:0] bits are set to BUF, the USBHS completes the control transfer status stage.

During control read transfers, the USBHS transmits the ACK handshake in response to the OUT transaction from the USB host. During control write or no-data control transfers, it transmits the zero-length packet in response to the IN transaction from the USB host. On detecting a SET_ADDRESS request, the USBHS operates in auto response mode from the setup stage up to status stage completion regardless of the CCPL bit setting.

The USBHS changes the CCPL bit from 1 to 0 on receiving a new setup packet. The software cannot write 1 to the bit while the INTSTS0.VALID bit is 1. The bit is initialized by a USB bus reset.

In host controller mode, always write 0 to the CCPL bit.

PINGE bit (PING Token Issue Enable)

In host controller mode, when the software sets the PINGE bit to 1, the USBHS issues a PING token for transfer in the transmitting direction, which triggers the transfer to start. If an ACK handshake is detected in the PING transaction, the OUT transaction is executed in the next transaction. If a NAK or NYET handshake is detected in the OUT transaction, the PING transaction is executed in the next transaction.

If the software sets this bit to 0, the USBHS issues no PING token for transfer in the transmitting direction. All transfers in the transmitting direction are executed in the OUT transaction.

PID[1:0] bits (Response PID)

PID[1:0]位在控制传输期间控制USB响应类型。

在主机控制器模式下，要将PID[1:0]设置从NAK更改为BUF：

●设置传输方向时：

a. 当DVSTCTR0.UACT位为1且PID为NAK时，将所有发送数据写入FIFO缓冲区。

湾。将PID[1:0]位设置为01b(BUF)。
然后USBHS执行OUT事务（或PING事务）

●设置接收方向时：

a. 在DVSTCTR0.UACT位为1且PID为NAK时检查FIFO缓冲区是否为空（或清空缓冲区）。

湾。将PID[1:0]位设置为01b(BUF)。
然后USBHS执行IN事务。

USBHS将PID[1:0]设置更改如下：

●当PID[1:0]位被软件设置为BUF(01b)并且USBHS接收到超过MaxPacketSize的数据时，USBHS将PID[1:0]设置为STALL(11b)

●当连续3次检测到接收错误（例如CRC错误）时，USBHS将PID[1:0]设置为NAK(00b)

●在接收到STALL握手时，USBHS将PID[1:0]设置为STALL(11b)

在设备控制器模式下，USBHS将PID[1:0]设置更改如下：

●在接收到一个设置数据包时，USBHS将PID[1:0]设置为NAK(00b)。然后USBHS将INTSTS0.VALID标志设置为1，并且在软件将VALID标志清除为0之前无法更改PID[1:0]设置。

●当PID[1:0]位被软件设置为BUF(01b)并且USBHS接收到超过MaxPacketSize的数据时，USBHS将PID[1:0]设置为STALL(11b)

●在检测到控制传输序列错误时，USBHS将PID[1:0]设置为STALL(1xb)

●在检测到USB总线复位时，USBHS将PID[1:0]设置为NAK

USBHS在处理SET_ADDRESS请求时不检查PID[1:0]设置。

CCPL位（控制传输结束使能）

在设备控制器模式下，将CCPL位设置为1可以完成控制传输的状态阶段。当该位由软件设置为1且相关的PID[1:0]位设置为BUF时，USBHS完成控制传输状态阶段。

在控制读取传输期间，USBHS发送ACK握手以响应来自USB主机的OUT事务。在控制写入或无数据控制传输期间，它传输零长度数据包以响应来自USB主机的IN事务。在检测到SET_ADDRESS请求时，USBHS从设置阶段到状态阶段完成以自动响应模式运行，无论CCPL位设置如何。

USBHS在接收到新的设置数据包时将CCPL位从1更改为0。当INTSTS0.VALID位为1时，软件无法向该位写入1。该位由USB总线复位初始化。

在主机控制器模式下，始终将0写入CCPL位。

PINGE位（PING令牌发布启用）

在主机控制器模式下，当软件将PINGE位设置为1时，USBHS会发出一个PING令牌以进行传输方向的传输，从而触发传输开始。如果在PING事务中检测到ACK握手，则在 下一个事务中执行OUT事务。如果在OUT事务中检测到NAK或NYET握手，则

PING事务在下一个事务中执行。

如果软件将此位设置为0，则USBHS不会发出PING令牌以进行传输方向的传输。发送方向的所有传输都在OUT事务中执行。

PBUSY flag (Pipe Busy Flag)

The PBUSY bit indicates whether DCP is used for the transaction when USBHS changes the PID[1:0] bits from BUF to NAK. The USBHS changes the PBUSY flag from 0 to 1 on start of a USB transaction for the selected pipe. It changes the PBUSY flag from 1 to 0 on completion of one transaction.

After PID is set to NAK by software, the value in the PBUSY flag indicates whether changes to pipe settings can proceed.

For details, see section 29.3.7.1. Pipe control register switching procedures.

SQMON flag (Sequence Toggle Bit Monitor Flag)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

The USBHS toggles the bit on normal completion of the transaction. It does not toggle the bit, however, when a DATAPID mismatch occurs during a transfer in the receiving direction.

In device controller mode, the USBHS sets the SQMON bit to 1 (specifies DATA1 as the expected value) on successful reception of the setup packet.

In device controller mode, the USBHS does not reference this bit during IN or OUT transactions at the status stage, and it does not toggle the bit on normal completion.

SQSET bit (Sequence Toggle Bit Set)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR bit (Sequence Toggle Bit Clear)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer. It is read as 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR bit (SUREQ Bit Clear)

In host controller mode, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The bit is read as 0.

If transfer stops while the SUREQ bit is set to 1 in a setup transaction, set the SUREQCLR bit to 1 through software. This is not necessary at the end of a normal setup transaction, because the USBHS automatically clears the SUREQ bit to 0.

Only control the SUREQ bit through the SUREQCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a bus disconnection was detected.

In device controller mode, always write 0 to the SUREQCLR bit.

CSSTS flag (CSSTS Status Flag)

In host controller mode, the CSSTS flag indicates the complete-split state in split transactions for pipes that are not isochronous. The USBHS sets the CSSTS flag to 1 at the beginning of a complete-split transaction and sets the flag back to 0 when it detects transaction completion.

Values read from the CSSTS flag in device controller mode are invalid.

CSCLR bit (CSSTS Status Flag Clear)

In host controller mode, setting the CSCLR bit to 1 clears the CSSTS bit to 0.

Set this bit to 1 through software when forcing the next transfer to restart from start-split in transfers using split transactions. This is not necessary at the end of a successful complete-split transaction in a normal split transaction, because the USBHS automatically clears the CSSTS flag to 0.

Only control the CSSTS flag through the CSCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a port disconnection was detected. Writing 1 to this bit while the CSSTS flag is 0 has no effect; the flag remains 0.

In device controller mode, always write 0 to this bit.

PBUSY标志（管道忙标志）

当USBHS将PID[1:0]位从BUF更改为
纳克。USBHS在所选管道的USB事务开始时将PBUSY标志从0更改为1。它改变了
PBUSY标志在一个事务完成时从1变为0。

软件将PID设置为NAK后，PBUSY标志中的值指示是否可以继续对管道设置进行更改。

详见29.3.7.1节。管道控制寄存器切换程序。

SQMON标志（序列切换位监控标志）

SQMON位指示DCP传输期间下一个事务的序列切换位的预期值。

USBHS在事务正常完成时切换该位。但是，当在接收方向的传输过程中发生DATAPID不匹配时，它不会切换该位
。

在设备控制器模式下，USBHS在成功接收到设置数据包时将SQMON位设置为1（指定DATA1作为预期值）。

在设备控制器模式下，USBHS在状态阶段的IN或OUT事务期间不参考该位，并且在正常完成时不切换该位。

SQSET位（序列切换位设置）

SQSET位将DATA1指定为DCP传输期间下一个事务的序列切换位的预期值。

不要同时将SQCLR和SQSET位设置为1。

SQCLR位（序列翻转位清除）

SQCLR位将DATA0指定为DCP传输期间下一个事务的序列切换位的预期值。读为0。

不要同时将SQCLR和SQSET位设置为1。

SUREQCLR bit (SUREQ Bit Clear)

在主机控制器模式下，将SUREQCLR位设置为1会将SUREQ位清除为0。该位被读取为0。

如果在设置事务中将SUREQ位设置为1时传输停止，则通过软件将SUREQCLR位设置为1。这在正常设置事务结束
时不是必需的，因为USBHS会自动将SUREQ位清除为0。

当DVSTCTR0.UACT位为0时，仅通过SUREQCLR位控制SUREQ位。当UACT为0时，由于检测到总线断开，
通信停止或没有传输发生。

在设备控制器模式下，始终将0写入SUREQCLR位。

CSSTS标志（CSSTS状态标志）

在主机控制器模式下，CSSTS标志指示非同步管道的拆分事务中的完全拆分状态。USBHS在完全拆分事务开始时
将CSSTS标志设置为1，并在检测到事务完成时将该标志设置回0。

在设备控制器模式下从CSSTS标志读取的值无效。

CSCLR位（CSSTS状态标志清除）

在主机控制器模式下，将CSCLR位设置为1会将CSSTS位清零。

在使用拆分事务的传输中强制下一次传输从start-split重新启动时，通过软件将此位设置为1。
在正常拆分事务中成功完成拆分事务结束时，这不是必需的，因为USBHS会自动将CSSTS标志清除为0。

仅当DVSTCTR0.UACT位为0时，通过CSCLR位控制CSSTS标志。当UACT为0时，由于检测到端口断开，通信停
止或不发生传输。CSSTS标志为0时向该位写入1无效；标志保持为0。

在设备控制器模式下，始终向该位写入0。

SUREQ bit (SETUP Token Transmission)

In host controller mode, setting the SUREQ bit to 1 triggers the USBHS to transmit the setup packet. After completing the setup transaction process, the USBHS generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0. The USBHS also clears the SUREQ bit to 0 when the software sets the SUREQCLR bit to 1.

Before setting the SUREQ bit to 1, set the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the wanted USB request in the setup transaction. Also check that the PID[1:0] bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not change the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is complete (SUREQ bit = 1). Write 1 to the SUREQ bit only when transmitting the setup token. Otherwise, write 0.

In device controller mode, always write 0 to this bit.

BSTS flag (Buffer Status Flag)

The BSTS flag indicates the status of access to the DCP FIFO buffer. The meaning of this flag varies as follows depending on the CFIFOSEL.ISEL setting:

- When ISEL = 0, the bit indicates whether receive data can be read from the buffer
- When ISEL = 1, the bit indicates whether transmit data can be written to the buffer

29.2.33 PIPESEL : Pipe Window Select Register

Base address: USBHS = 0x4011_1000

Offset address: 0x064

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PIPESEL[3:0]	Pipe Window Select 0x0: No pipe selected 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3 0x4: Pipe 4 0x5: Pipe 5 0x6 Pipe 6 0x7: Pipe 7 0x8: Pipe 8 0x9: Pipe 9 Others: Setting prohibited	R/W
15:4	—	The read values are undefined. The write value should be 0.	R/W

Set pipes 1 to 9 using the PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN registers (n = 0 to 9).

After selecting the pipe in the PIPESEL register, pipe functions must be set in the associated PIPECFG, PIPEMAXP, and PIPEPERI registers. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set independently of the pipe selection in this register.

PIPESEL[3:0] bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number associated with the PIPECFG, PIPEMAXP, and PIPEPERI registers used for data writing and reading. Selecting a pipe number in the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI associated with the selected pipe number.

When PIPESEL[3:0] = 0x0, 0 is read from all of the bits in PIPECFG, PIPEMAXP, and PIPEPERI. Writing to these bits has no effect.

SURESQ位（SETUP令牌传输）

在主机控制器模式下，将SUREQ位设置为1会触发USBHS发送设置数据包。完成设置事务处理后，USBHS产生SACK或SIGN中断并将SUREQ位清零。当软件将SUREQCLR位设置为1时，USBHS也将SUREQ位清零。

在将SUREQ位设置为1之前，将DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX和USBLENG在设置事务中适当地传输所需的USB请求。还要检查DCP的PID[1:0]位是否设置为NAK。将SUREQ位设置为1后，在设置事务完成（SUREQ位=1）之前，不要更改DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX或USBLENG。仅在发送设置令牌时向SUREQ位写入1。否则，写0。

在设备控制器模式下，始终向该位写入0。

BSTS标志（缓冲区状态标志）

BSTS标志指示访问DCPFIFO缓冲区的状态。根据CFIFOSEL.ISEL设置，该标志的含义如下：

- ISEL=0时，该位指示是否可以从缓冲区读取接收数据
- ISEL=1时，该位指示发送数据是否可以写入缓冲区

29.2.33 PIPESEL:管道窗口选择寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x064

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Bit	Symbol	Function	R/W
3:0	PIPESEL[3:0]	管道窗口选择 0x0：未选择管道0x1 ：管道10x2：管道20x 3：管道30x4：管道40 x5：管道50x6管道60x 7：管道70x8：管道80 x9：管道9 其他：禁止设置	R/W
15:4	—	读取的值未定义。写入值应为0。	R/W

使用PIPESEL、PIPECFG、PIPEMAXP、PIPEPERI、PIPEnCTR、PIPEnTRE和PIPEnTRN寄存器（n=0到9）设置管道1到9。

在PIPESEL寄存器中选择管道后，必须在相关的PIPECFG、PIPEMAXP和PIPEPERI寄存器。PIPEnCTR、PIPEnTRE和PIPEnTRN可以独立于该寄存器中的管道选择进行设置。

PIPESEL[3:0]位（管道窗口选择）

PIPESEL[3:0]位选择与用于数据写入和读取的PIPECFG、PIPEMAXP和PIPEPERI寄存器相关的管道编号。在PIPESEL[3:0]位中选择一个管道编号允许写入和读取与所选管道编号相关的PIPECFG、PIPEMAXP和PIPEPERI。

当PIPESEL[3:0]=0x0时，从PIPECFG、PIPEMAXP和PIPEPERI中的所有位读取0。写入这些位无效。

29.2.34 PIPECFG : Pipe Configuration Register

Base address: USBHS = 0x4011_1000

Offset address: 0x068

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	x	x	x	0	0	0	0	x	x	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	EPNUM[3:0]	Endpoint Number*1 Specifies the endpoint number for the selected pipe. Setting 0x0 indicates the pipe is not used.	R/W
4	DIR	Transfer Direction*2 *3 0: Receiving direction 1: Transmitting direction	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	SHTNAK	Pipe Disabled at End of Transfer*1 0: Continue pipe operation after transfer ends 1: Disable pipe after transfer ends	R/W
8	CNTMD	Continuous Transfer Mode*2 *3 0: Discontinuous transfer mode 1: Continuous transfer mode	R/W
9	DBLB	Double Buffer Mode*2 *3 0: Single buffer 1: Double buffer	R/W
10	BFRE	BRDY Interrupt Operation Specification*2 *3 0: Generate BRDY interrupt on transmitting or receiving data 1: Generate BRDY interrupt on completion of reading data	R/W
13:11	—	These bits are read as 0. The write value should be 0.	R/W
15:14	TYPE[1:0]	Transfer Type*1 0 0: Pipe not used 0 1: (Pipe 1 to 5) Bulk transfer (Pipe 6 to 9) Setting prohibited 1 0: (Pipe 1 to 5) Setting prohibited (Pipe 6 to 9) Interrupt transfer 1 1: (Pipe 1 to 2) Isochronous transfer (Pipe 3 to 9) Setting prohibited	R/W

Note 1. Only set the TYPE[1:0], SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY flags through the software is not necessary.

Note 2. Only set the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

Note 3. To change the BFRE, DBLB, or DIR bit after completing USB communication on the selected pipe, in addition to the constraints described in note 2, write 1 and 0 to the PIPEnCTR.ACLRM bit continuously through software and clear the FIFO buffer assigned to the pipe.

EPNUM[3:0] bits (Endpoint Number)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe. Setting 0000b indicates the pipe not used.

Set these bits so that the combination of the DIR and EPNUM[3:0] settings is different from those for other pipes. (The EPNUM[3:0] bits can be set to 0000b for all pipes.)

DIR bit (Transfer Direction)

The DIR bit specifies the transfer direction for the selected pipe.

29.2.34 PIPECFG:管道配置寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x068

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	DIR	EPNUM[3:0]			
重置后的值：	0	0	x	x	x	0	0	0	0	x	x	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	EPNUM[3:0]	端点编号*1 指定选定管道的端点编号。设置0x0表示不使用管道。	R/W
4	DIR	传输方向*2*3 0：接收方向1：发送方向	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	SHTNAK	传输结束时管道禁用*1 0：传输结束后继续管道操作1：传输结束后禁用管道	R/W
8	CNTMD	连续传输模式*2*3 0：不连续传输模式1：连续传输模式	R/W
9	DBLB	双缓冲模式*2*3 0：单缓冲区1：双缓冲区	R/W
10	BFRE	BRDY中断操作规范*2*3 0：发送或接收数据时产生BRDY中断1：读取数据完成时产生BRDY中断	R/W
13:11	—	这些位被读取为0。写入值应为0。	R/W
15:14	TYPE[1:0]	传输类型*1 00：管道未使用01：（管道1到5）批量传输 （管6至9）禁止设置 10：（管道1到5）设置禁止（管道6到9）中断传输 11:(管道1到2)同步传输(管道3到9)禁止设置	R/W

注1.PID为NAK时，仅设置TYPE[1:0]、SHTNAK和EPNUM[3:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY标志。

注2.仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置BFRE、DBLB和DIR位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

注3.在选定管道上完成USB通信后更改BFRE、DBLB或DIR位，除了约束
如注2所述，通过软件连续向PIPEnCTR.ACLRM位写入1和0，并清除分配给管道的FIFO缓冲区。

EPNUM[3:0] bits (Endpoint Number)

EPNUM[3:0]位指定所选管道的端点号。设置0000b表示管道未使用。

设置这些位，以便DIR和EPNUM[3:0]设置的组合不同于其他管道的设置。（这所有管道的EPNUM[3:0]位都可以设置为0000b。）

DIR位（传输方向）

DIR位指定所选管道的传输方向。

When the software sets this bit to 0, the USBHS uses the selected pipe for receiving. When the software sets this bit to 1, the USBHS uses the selected pipe for transmitting.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change the PIPEnCTR.PID[1:0] bits to 00b (NAK) at the end of transfer when the selected pipe is set in the receiving direction. The bit is valid for pipes 1 to 5 in the receiving direction.

When the software sets this bit to 1 for a receiving pipe, the USBHS changes the associated PIPEnCTR.PID[1:0] bits to 00b (NAK) on determining the transfer end. The USBHS determines that the transfer has ended on the following conditions:

- Short packet data (including a zero-length packet) was successfully received
- The transaction counter is used and the number of packets specified for the transaction counter were successfully received

CNTMD bit (Continuous Transfer Mode)

The CNTMD bit specifies whether to operate the selected pipe in continuous transfer mode. The bit is valid for pipes 1 to 5 of the bulk transfer type.

Based on this bit setting, the USBHS determines the completion of transmission or reception for the FIFO buffer allocated to the selected pipe as shown in Table 29.9.

Table 29.9 Relationship between the CNTMD setting and methods for determining completion of FIFO buffer transmission or reception

CNTMD bit setting	Methods for determining readable state and transmittable state
0	Condition for FIFO buffer readable state in receiving direction (DIR = 0): ● The USBHS received one packet
	Conditions for FIFO buffer transmittable state in transmitting direction (DIR = 1): When one of the following is satisfied: 1. Software (or DMAC/DTC) wrote data of the maximum packet size to the FIFO buffer 2. Software (or DMAC/DTC) wrote data of the short packet size (including 0 bytes) to the FIFO buffer and set the BVAL flag in the port control register to 1
1	Condition for FIFO buffer readable state in receiving direction (DIR = 0): 1. The byte count of data received in the FIFO buffer allocated to the selected pipe is equal to the allocated byte count ((BUFSIZE + 1) × 64). 2. The USBHS received a short packet, other than a zero-length packet. 3. The USBHS received a zero-length packet when data was already contained in the FIFO buffer allocated to the selected pipe. 4. Software received the number of packets specified for the transaction counter set for the selected pipe.
	Conditions for FIFO buffer transmittable state in transmitting direction (DIR = 1): When one of the following is satisfied. 1. The amount of data written by software (or DMAC/DTC) is equal to the size of the FIFO buffer allocated to the selected pipe. 2. The software (or DMAC/DTC) wrote data of smaller size than that of the FIFO buffer allocated to the selected pipe (including 0 bytes) and set the BVAL flag in the port control register to 1. 3. The software (or DMAC/DTC) wrote data of smaller size than that of one FIFO buffer allocated to the selected pipe (including 0 bytes) and asserted the DENDx_N signal on the last write.

DBLB bit (Double Buffer Mode)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe. The bit is valid for pipes 1 to 5.

When the software sets this bit to 1, the USBHS allocates twice the FIFO buffer size specified in the PIPEBUF.BUFSIZE[5:0] bits for the selected pipe. The FIFO buffer size that the USBHS allocates to the selected pipe is as follows:

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

BFRE bit (BRDY Interrupt Operation Specification)

The BFRE bit specifies the BRDY interrupt generation timing from the USBHS to the CPU for the selected pipe.

When the software sets the BFRE bit to 1 and the selected pipe is in the receiving direction, the USBHS detects the transfer completion and generates the BRDY interrupt on reading the packet.

当软件将此位设置为0时，USBHS使用所选管道进行接收。当软件将该位设置为1时，USBHS使用选定的管道进行传输。

SHTNAK位（传输结束时禁用管道）

SHTNAK位指定当所选管道设置为接收方向时，是否在传输结束时将PIPEnCTR.PID[1:0]位更改为00b(NAK)。该位对接收方向的管道1到5有效。

当软件将该位设置为1用于接收管道时，USBHS在确定传输结束时将相关的PIPEnCTR.PID[1:0]位更改为00b(NAK)。USBHS在以下条件下确定传输已结束：

●成功接收短包数据（包括零长度包）

●使用事务计数器，并且成功接收了为事务计数器指定的数据包数

CNTMD位（连续传输模式）

CNTMD位指定是否在连续传输模式下操作选定的管道。该位对批量传输类型的管道1到5有效。

根据该位设置，USBHS确定分配给所选管道的FIFO缓冲区的发送或接收是否完成，如表29.9所示。

Table 29.9 CNTMD设置与确定FIFO缓冲区发送或接收完成的方法之间的关系

CNTMD位设置	确定可读状态和可传输状态的方法
0	接收方向（DIR=0）FIFO缓冲区可读状态的条件：● USBHS收到一个数据包
	发送方向(DIR=1)的FIFO缓冲区可发送状态的条件： 当满足以下条件之一时：1.软件（或DMACDTC）将最大数据包大小的数据写入FIFO缓冲区2.软件（或DMACDTC）将短数据包大小（包括0字节）的数据写入FIFO缓冲区并将端口控制寄存器中的BVAL标志设置为1
1	接收方向（DIR=0）FIFO缓冲区可读状态的条件：1.分配给所选管道的FIFO缓冲区中接收到的数据字节数等于分配的字节数（（BUFSIZE+1）×64）。2.USBHS收到一个短数据包，而不是零长度数据包。3.当数据已经包含在分配给所选管道的FIFO缓冲区中时，USBHS接收到一个长度为零的数据包。4.软件接收到为选定管道设置的事务计数器指定的数据包数量。
	发送方向(DIR=1)的FIFO缓冲区可发送状态的条件： 满足以下条件之一时。1.软件（或DMACDTC）写入的数据量等于分配给所选管道的FIFO缓冲区的大小。2.软件（或DMACDTC）写入小于分配给所选管道的FIFO缓冲区大小的数据（包括0字节），并将端口控制寄存器中的BVAL标志设置为1。3.软件（或DMACDTC)写入的数据小于分配给所选管道的一个FIFO缓冲区的数据（包括0字节），并在最后一次写入时置位DENDx_N信号。

DBLB位（双缓冲模式）

DBLB位为所选管道使用的FIFO缓冲区选择单缓冲区模式或双缓冲区模式。该位对管道1到5有效。

当软件将该位设置为1时，USBHS分配两倍于所选管道的PIPEBUF.BUFSIZE[5:0]位。USBHS分配给所选管道的FIFO缓冲区大小如下：

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

BFRE位（BRDY中断操作规范）

BFRE位为所选管道指定从USBHS到CPU的BRDY中断生成时序。

当软件将BFRE位设置为1且所选管道处于接收方向时，USBHS检测到传输完成并在读取数据包时产生BRDY中断。

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When a BRDY interrupt is generated with this setting, the software must write 1 to the BCLR bit in the port control register. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.

When the BFRE bit is set to 1 by software and the selected pipe is in the transmitting direction, the USBHS does not generate the BRDY interrupt. For details, see section 29.3.6.1. BRDY interrupt.

TYPE[1:0] bits (Transfer Type)

The TYPE[1:0] bits specify the transfer type for the pipe selected in the PIPESEL.PIPESEL[3:0] bits. Before setting PID to BUF and starting USB communication on the selected pipe, set the TYPE[1:0] bits to a value other than 00b.

29.2.35 PIPEBUF : Pipe Buffer Register

Base address: USBHS = 0x4011_1000

Offset address: 0x06A

Bit position:	15	14					9	8	7							0
Bit field:	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
Value after reset:	x	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	BUFNMB[7:0]	Buffer Number Specifies the FIFO buffer number of the selected pipe (0x04 to 0x87).	R/W
9:8	—	The read values are undefined. The write value should be 0.	R/W
14:10	BUFSIZE[4:0]	Buffer Size 0x00: 64 bytes 0x01: 128 bytes ⋮ 0x1F: 2 KB	R/W
15	—	The read value is undefined. The write value should be 0.	R/W

Note: Only set the bits in the PIPEBUF register while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY flags through the software is not necessary.

BUFNMB[7:0] bits (Buffer Number)

The BUFNMB[7:0] bits specify the first block number of the FIFO buffer to be allocated to the selected pipe.

The USBHS allocates the FIFO buffer blocks to the selected pipe as follows:

Block number: BUFNMB to block number: BUFNMB + (BUFSIZE + 1) × (DBLB + 1) - 1

Set a value within the memory size range for these bits (0 [0x00] to 8640 [0x87] for 8.5 KB), while observing the following conditions:

- 0x00 is for DCP only
- 0x04 is for pipe 6 only, but is available for other pipes when pipe 6 is not used. When pipe 6 is selected, writes to these bits are disabled. The USBHS automatically allocates 0x04 to the BUFNMB bits for pipe 6.
- 0x05 is for pipe 7 only, but is available for other pipes when pipe 7 is not used. When pipe 7 is selected, writes to these bits are disabled. The USBHS automatically allocates 0x05 to the BUFNMB bits for pipe 7.
- 0x06 is for pipe 8 only, but is available for other pipes when pipe 8 is not used. When pipe 8 is selected, writes to these bits are disabled. The USBHS automatically allocates 0x06 to the BUFNMB bits for pipe 8.
- 0x07 is for pipe 9 only, but is available for other pipes when pipe 9 is not used. When pipe 9 is selected, writes to these bits are disabled. The USBHS automatically allocates 0x07 to the BUFNMB bits for pipe 9.

BUFSIZE[4:0] bits (Buffer Size)

The BUFSIZE[4:0] bits specify the FIFO buffer size (number of blocks) to be allocated to the selected pipe. One block is 64 bytes.

当使用该设置产生BRDY中断时，软件必须将1写入端口控制寄存器中的BCLR位。
在将1写入BCLR位之前，分配给所选管道的FIFO缓冲区不会用于接收。

当BFRE位由软件设置为1且所选管道处于发送方向时，USBHS不会产生BRDY中断。详见29.3.6.1节。BRDY中断。

TYPE[1:0] bits (Transfer Type)

TYPE[1:0]位指定在PIPESEL.PIPESEL[3:0]位中选择的管道的传输类型。设置PID之前BUF并在所选管道上启动USB通信，将TYPE[1:0]位设置为00b以外的值。

29.2.35 PIPEBUF:管道缓冲寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x06A

Bit position:	15	14					9	8	7							0
Bit field:	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
重置后的值:	x	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	BUFNMB[7:0]	缓冲区号 指定所选管道的FIFO缓冲区编号（0x04到0x87）。	R/W
9:8	—	读取的值未定义。写入值应为0。	R/W
14:10	BUFSIZE[4:0]	缓冲区大小 0x00: 64 bytes 0x01: 128 bytes ⋮ 0x1F: 2 KB	R/W
15	—	读取值未定义。写入值应为0。	R/W

Note: 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置PIPEBUF寄存器中的位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY标志。

BUFNMB[7:0] bits (Buffer Number)

BUFNMB[7:0]位指定要分配给所选管道的FIFO缓冲区的第一个块号。

USBHS将FIFO缓冲区块分配给所选管道，如下所示：

块号：BUFNMB到块号：BUFNMB+(BUFSIZE+1)×(DBLB+1)1

为这些位设置一个内存大小范围内的值（0[0x00]到8640[0x87]，对于8.5KB），同时遵守以下条件：

●0x00仅用于DCP

●0x04仅适用于管道6，但在不使用管道6时可用于其他管道。选择管道6时，将这些位写入这些位。USBHS自动将0x04分配给管道6的BUFNMB位。

●0x05仅适用于管道7，但在管道7不使用时可用于其他管道。选择管道7时，将这些位写入这些位。USBHS自动将0x05分配给管道7的BUFNMB位。

●0x06仅用于管道8，但在不使用管道8时可用于其他管道。选择管道8时，将这些位写入这些位。USBHS自动将0x06分配给管道8的BUFNMB位。

●0x07仅适用于管道9，但在不使用管道9时可用于其他管道。选择管道9时，将这些位写入这些位。USBHS自动将0x07分配给管道9的BUFNMB位。

BUFSIZE[4:0] bits (Buffer Size)

BUFSIZE[4:0]位指定要分配给所选管道的FIFO缓冲区大小（块数）。一个块是64字节。

When the software sets the DBLB bit to 1, the USBHS allocates twice the FIFO buffer size specified in these bits to the selected pipe. The DBLB = 1 setting is valid for pipes 1 to 5.

The USBHS allocates the FIFO buffer blocks to the selected pipe as follows:

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

Set the value within the following range:

- For pipes 1 to 5, set a value from 0x00 to 0x1F (up to 2 KB)
- For pipes 6 to 9, only set a value of 0x00 (64 bytes)

29.2.36 PIPEMAXP : Pipe Maximum Packet Size Register

Base address: USBHS = 0x4011_1000

Offset address: 0x06C

Bit position:	15			12	11	10									0
Bit field:	DEVSEL[3:0]				—	MXPS[10:0]									
Value after reset:	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	MXPS[10:0]*1 *2	Maximum Packet Size ● Pipes 1 and 2 1 byte (0x001) to 1024 bytes (0x400) ● Pipes 3 to 5 8 bytes (0x008), 16 bytes (0x010), 32 bytes (0x020), 64 bytes (0x040), 512 bytes (0x200) (Bits 2 to 0 not supported.) ● Pipes 6 to 9 1 byte (0x001) to 64 bytes (0x040) (Bits 10 to 7 not supported.)	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
15:12	DEVSEL[3:0]*3	Device Select 0x0: Address 0x0 0x1: Address 0x1 ⋮ 0x9: Address 0x9 0xA: Address 0xA Others: Reserved	R/W

Note 1. The initial value of the MXPS[10:0] bits is 0x00 when no pipe is selected in the PIPESEL.PIPESEL[3:0] bits and 0x40 when a pipe is selected.

Note 2. Only set the MXPS[10:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY flags through the software is not necessary.

Note 3. Only set the DEVSEL[3:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

MXPS[10:0] bits (Maximum Packet Size)

The MXPS[10:0] bits specify the maximum data payload (maximum packet size) for the selected pipe.

Set these bits to the appropriate value for each transfer type based on the USB 2.0 specification. When MXPS[10:0] = 0, do not write to the FIFO buffer or set PID to BUF. These writes have no effect.

To communicate on an isochronous pipe using a split transaction, set the value in the MXPS[10:0] bits to 188 bytes or less.

当软件将DBLB位设置为1时，USBHS将这些位中指定的两倍FIFO缓冲区大小分配给所选管道。DBLB=1设置对管道1到5有效。

USBHS将FIFO缓冲区块分配给所选管道，如下所示：

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

将值设置在以下范围内：

●对于管道1到5，设置一个从0x00到0x1F的值（最大2KB）

●对于管道6到9，仅设置值0x00（64字节）

29.2.36 PIPEMAXP:管道最大数据包大小寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x06C

Bit position:	15			12	11	10									0
Bit field:	DEVSEL[3:0]				—	MXPS[10:0]									
重置后的值:	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	MXPS[10:0]*1 *2	最大数据包大小● 管道1和21字节(0x001)到1024字节(0x400) ● 管道3到58字节(0x008)、16字节(0x010)、32字节(0x020)、64字节(0x040)、512字节(0x200)（不支持位2到0。） ● 管道6到91字节(0x001)到64字节(0x040)（不支持位10到7。）	R/W
11	—	该位读取为0。写入值应为0。	R/W
15:12	DEVSEL[3:0]*3	设备选择 0x0: Address 0x0 0x1: Address 0x1 ⋮ 0x9: Address 0x9 0xA: Address 0xA Others: Reserved	R/W

注1.在PIPESEL.PIPESEL[3:0]位中未选择管道时，MXPS[10:0]位的初始值为0x00，选择管道时为0x40。

注2.仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置MXPS[10:0]位。
在设置这些位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后更改PIPEnCTR.PID[1:0]位从01b(BUF)到00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY标志。

注3.仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置DEVSEL[3:0]位。
在设置这些位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后更改PIPEnCTR.PID[1:0]位从01b(BUF)到00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

MXPS[10:0]位（最大数据包大小）

MXPS[10:0]位指定所选管道的最大数据有效负载（最大数据包大小）。

根据USB2.0规范将这些位设置为每种传输类型的适当值。当MXPS[10:0]=0时，不要写入FIFO缓冲区或将PID设置为BUF。这些写入没有效果。

要使用拆分事务在同步管道上进行通信，请将MXPS[10:0]位中的值设置为188字节或更少。

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target device for USB communication. Set up the device address in the associated DEVADDn (n = 0 to A) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0x2, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0x0.

29.2.37 PIPEPERI : Pipe Cycle Control Register

Base address: USBHS = 0x4011_1000

Offset address: 0x06E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after reset:	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0	0

Bit	Symbol	Function	R/W
2:0	IITV[2:0]*1	Interval Error Detection Interval Specifies the interval error detection timing for the selected pipe as the n-th power of 2 of the frame timing.	R/W
11:3	—	These bits are read as 0. The write value should be 0.	R/W
12	IFIS	Isochronous IN Buffer Flush 0: Do not flush buffer 1: Flush buffer	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set the IITV[2:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

PIPEPERI selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfers, and sets the interval error detection interval for pipes 1 to 9.

IITV[2:0] bits (Interval Error Detection Interval)

To change the IITV[2:0] bits to another value after they are set and USB communication is performed, set the PIPEnCTR.PID[1:0] bits to 00b (NAK) and then set the PIPEnCTR.ACLRM bit to 1 to initialize the interval timer.

The IITV[2:0] bits are not provided for pipes 3 to 5. Write 000b to bit positions of the IITV[2:0] bits associated with pipes 3 to 5.

IFIS bit (Isochronous IN Buffer Flush)

The IFIS bit specifies whether to flush the buffer when the pipe specified in the PIPESEL.PIPESEL[3:0] bits is used for isochronous IN transfers.

In device controller mode when the selected pipe is for isochronous IN transfers, the USBHS automatically clears the FIFO buffer if the USBHS fails to receive the IN token from the USB host within the interval set in the IITV[2:0] bits in terms of frames.

When double buffering is specified (PIPECFG.DBLB = 1), the USBHS only clears the data in the previously used plane.

The USBHS clears the FIFO buffer on receiving the SOF packet immediately after the frame in which the USBHS expected to receive the IN token. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time the SOF packet is expected to be received by using the internal complementation function.

In host controller mode, set the IITV[2:0] bits to 000b.

Set the IITV[2:0] bits to 000b when the selected pipe is not used for isochronous transfers.

DEVSEL[3:0] bits (Device Select)

在主机控制器模式下，DEVSEL[3:0]位指定USB通信的目标设备的地址。首先在相关的DEVADDn（n=0到A）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0x2，首先设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0x0。

29.2.37 PIPEPERI:管道循环控制寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x06E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
重置后的值:	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0	0

Bit	Symbol	Function	R/W
2:0	IITV[2:0]*1	间隔错误检测间隔 将所选管道的间隔错误检测时间指定为帧时间的2的n次方。	R/W
11:3	—	这些位被读取为0。写入值应为0。	R/W
12	IFIS	同步IN缓冲区刷新 0：不刷新缓冲区1： 刷新缓冲区	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W

注1.仅在PID为NAK时设置IITV[2:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY flags为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

PIPEPERI选择在同步IN传输期间发生间隔错误时是否刷新缓冲区，并设置管道1到9的间隔错误检测间隔。

IITV[2:0]位（间隔错误检测间隔）

要在设置IITV[2:0]位并在执行USB通信后将其更改为另一个值，请设置PIPEnCTR.PID[1:0]位为00b(NAK)，然后将PIPEnCTR.ACLRM位设置为1以初始化间隔定时器。

不为管道3到5提供IITV[2:0]位。将000b写入与管道3到5相关联的IITV[2:0]位的位位置。

IFIS位（同步IN缓冲区刷新）

IFIS位指定当PIPESEL.PIPESEL[3:0]位中指定的管道用于同步IN传输时是否刷新缓冲区。

在设备控制器模式下，当所选管道用于同步IN传输时，如果USBHS在IITV[2:0]位设置的时间间隔内未能从USB主机接收到IN令牌，则USBHS自动清除FIFO缓冲区帧。

当指定双缓冲时（PIPECFG.DBLB=1），USBHS仅清除先前使用的平面中的数据。

在USBHS预期接收IN令牌的帧之后，USBHS在接收到SOF数据包后立即清除FIFO缓冲区。即使SOF数据包已损坏，FIFO缓冲区也会在预期接收SOF数据包时使用内部补充功能清除。

在主机控制器模式下，将IITV[2:0]位设置为000b。

当所选管道不用于同步传输时，将IITV[2:0]位设置为000b。

29.2.38 PIPEnCTR : Pipe n Control Register (n = 1 to 9)

Base address: USBHS = 0x4011_1000

Offset address: 0x070 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	INBUFM	CSCLR	CSSTS	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	x	0	0	0	0	0	0	x	x	x	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	Response PID 0 0: NAK response 0 1: BUF response (depends on buffer state) 1 0: STALL response 1 1: STALL response	R/W
4:2	—	The read values are undefined. The write value should be 0.	R/W
5	PBUSY	Pipe Busy Flag 0: Pipe n not in use for the transaction 1: Pipe n in use for the transaction	R
6	SQMON	Sequence Toggle Bit Monitor Flag 0: DATA0 1: DATA1	R
7	SQSET	Sequence Toggle Bit Set*1 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W
8	SQCLR	Sequence Toggle Bit Clear*1 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0	W
9	ACLRM	Auto Buffer Clear Mode*2 0: Disable 1: Enable (initialize all buffers)	R/W
10	ATREPM	Auto Response Mode*1 *3 0: Disable auto response mode 1: Enable auto response mode	R/W
11	—	The read value is undefined. The write value should be 0.	R/W
12	CSSTS	CSSTS Status Flag 0: Start-split (SSPLIT) transaction, or processing for devices that are not using split transactions, in progress. 1: Complete-split (CSPLIT) transaction in progress.	R
13	CSCLR	CSPLIT Status Clear 0: Invalid (writing 0 has no effect) 1: Clear CSSTS to 0	W
14	INBUFM	Transmit Buffer Monitor Flag*3 0: No data to be transmitted is in the FIFO buffer 1: Data to be transmitted is in the FIFO buffer	R
15	BSTS	Buffer Status Flag 0: Buffer access disabled 1: Buffer access enabled	R

Note 1. Only set the ATREPM bit while PID is NAK. Before setting this bit, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

Note 2. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

29.2.38 PIPEnCTR:管道n控制寄存器(n=1到9)

Base address: USBHS = 0x4011_1000

Offset address: 0x070 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	BSTS	INBUFM	CSCLR	CSSTS	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值:	0	0	0	0	x	0	0	0	0	0	0	x	x	x	0	0

Bit	Symbol	Function	R/W
1:0	PID[1:0]	响应PID 00：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应	R/W
4:2	—	读取的值未定义。写入值应为0。	R/W
5	PBUSY	管道忙标志 0：管道n未用于事务1：管道n正在用于事务	R
6	SQMON	序列切换位监控标志 0: DATA0 1: DATA1	R
7	SQSET	序列切换位设置*1 0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1。该位读为0。	R/W
8	SQCLR	序列切换位清除*1 0：无效（写0无效）1：清除下一笔交易的期望值到DATA0	W
9	ACLRM	自动缓冲区清除模式*2 0：禁用1：启用（初始化所有缓冲区）	R/W
10	ATREPM	自动响应模式*1*3 0：禁用自动响应模式1：启用自动响应模式	R/W
11	—	读取值未定义。写入值应为0。	R/W
12	CSSTS	CSSTS状态标志 0：开始拆分(SSPLIT)事务，或正在处理未使用拆分事务的设备。 1：完成拆分（CSPLIT）事务正在进行中。	R
13	CSCLR	CSPLIT状态清除 0：无效（写0无效）1：清除CSSTS为0	W
14	INBUFM	发送缓冲器监视标志*3 0：FIFO缓冲区中没有要发送的数据1：FIFO缓冲区中没有要发送的数据	R
15	BSTS	缓冲区状态标志 0：禁止缓冲区访问1：允许缓冲区访问	R

注1.仅当PID为NAK时设置ATREPM位。在设置该位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

注2.仅在PID为NAK时和在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。在设置该位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

Note 3. The ATREPM bit and the INBUFM flag in the PIPE6CTR to PIPE9CTR registers are reserved. The read value is undefined. The write value must be 0.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction on the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USB transfer. Table 29.10 and Table 29.11 show the basic operations of the USBHS (when there are no errors in the communication packets) based on the PID[1:0] bit setting.

After changing the PID[1:0] setting from BUF to NAK through the software during USB communication on the selected pipe, check that the PBUSY bit is 1 to see if USB transfer on the selected pipe has actually entered the NAK state. If the USBHS changes the PID[1:0] bits to NAK, checking the PBUSY bit through the software is not necessary.

The USBHS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBHS sets PID to NAK on recognizing completion of the transfer when the selected pipe is in the receiving direction and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software
- The USBHS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBHS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBHS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBHS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode

To specify the response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, set 00b (NAK) and then 01b (BUF)

Table 29.10 Operation of the USBHS based on the PIPEnCTR.PID[1:0] setting in host controller mode

PID[1:0] value	Transfer type (TYPE[1:0] value)	Transfer direction (DIR value)	USBHS operation
00b (NAK)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens
01b (BUF)	Bulk or Interrupt	Does not depend on the setting	Issues tokens when the DVSTCTR0.UACT bit is 1 and the FIFO buffer associated with the selected pipe is ready for transmission and reception. Does not issue tokens when the DVSTCTR0.UACT bit is 0 or the FIFO buffer associated with the selected pipe is not ready for transmission or reception.
	Isochronous	Does not depend on the setting	Issues tokens when the DVSTCTR0.UACT bit is 1, regardless of the state of the FIFO buffer associated with the selected pipe. Does not issue tokens when UACT = 0.
10b (STALL) or 11b (STALL)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens.

注3.PIPE6CTR至PIPE9CTR寄存器中的ATREPM位和INBUFM标志被保留。读取值未定义。写入值必须为0。

PID[1:0] bits (Response PID)

PID[1:0]位指定所选管道上下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联的管道进行USB传输。表29.10和表29.11显示了基于PID[1:0]位设置的USBHS的基本操作（通信数据包中没有错误时）。

在选定管道上进行USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以查看选定管道上的USB传输是否真正进入了NAK状态。如果USBHS将PID[1:0]位更改为NAK，则无需通过软件检查PBUSY位。

USBHS在以下情况下更改PIPEnCTR.PID[1:0]设置：

●USBHS设置为NAK，以识别所选管道处于接收方向和PIPECFG.SHTNAK位时，将所选管道设置为1bySoffate

●USBHS在接收到负载超过所选管道最大数据包大小的数据包时将PID设置为STALL(11b)

●USBHS在设备控制器模式下检测到USB总线复位时将PID设置为NAK

●USBHS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK

●USBHS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)

要指定响应类型，请按如下方式设置PID[1:0]位：

●要从NAK(00b)转换到STALL，设置10b

●要从BUF(01b)转换到STALL，设置11b

●要从STALL(11b)转换为NAK，请设置10b，然后设置00b

●要从STALL转换到BUF，请设置00b(NAK)，然后设置01b(BUF)

Table 29.10 USBHS在主机控制器模式下基于PIPEnCTR.PID[1:0]设置的操作

PID[1:0] value	传输类型（TYPE[1:0]值）	传输方向（DIR值）	USBHS operation
00b (NAK)	不依赖于设置	不依赖于设置	不发行代币
01b (BUF)	批量或中断	不依赖于设置	发行令牌时 DVSTCTR0.UACT位为1，与所选管道关联的FIFO缓冲区已准备好进行发送和接收。当DVSTCTR0.UACT位为0或与所选管道关联的FIFO缓冲区未准备好进行发送或接收时，不发出令牌。
	Isochronous	不依赖于设置	发行令牌时 无论与所选管道关联的FIFO缓冲区的状态如何，DVSTCTR0.UACT位为1。不发行代币时 UACT = 0.
10b (STALL) or 11b (STALL)	不依赖于设置	不依赖于设置	不发行代币。

Table 29.11 Operation of the USBHS based on the PIPEnCTR.PID[1:0] setting in device controller mode

PID[1:0] value	Transfer type (TYPE[1:0] value)	Transfer direction (DIR value)	USBHS operation
00b (NAK)	Bulk or Interrupt	Does not depend on the setting	Returns NAK in response to the token from the USB host
	Isochronous	Receiving direction (DIR = 0)	Returns nothing in response to the token from the USB host
		Transmitting direction (DIR = 1)	Transmits a zero-length packet in response to the token from the USB host
01b (BUF)	Bulk	Receiving direction (DIR = 0)	Receives data and returns ACK or NYET in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, returns NAK. Returns ACK in response to the PING token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, returns NAK.
	Interrupt	Receiving direction (DIR = 0)	Receives data and returns ACK response in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, returns NAK.
	Bulk or Interrupt	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the FIFO buffer associated with the selected pipe is ready for transmission. Otherwise, returns NAK.
	Isochronous	Receiving direction (DIR = 0)	Receives data in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, discards the data.
		Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the associated FIFO buffer is ready for transmission. Otherwise, transmits a zero-length packet.
10b (STALL) or 11b (STALL)	Bulk or Interrupt	Does not depend on the setting.	Returns STALL in response to the token from the USB host
	Isochronous	Does not depend on the setting.	Returns nothing in response to the token from the USB host

PBUSY flag (Pipe Busy Flag)

The PBUSY flag indicates whether the selected pipe is being used for the current transaction.

The USBHS changes the PBUSY bit from 0 to 1 on start of the USB transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible. For details, see section 29.3.7.1. Pipe control register switching procedures.

Table 29.11 USBHS在设备控制器模式下基于PIPEnCTR.PID[1:0]设置的操作

PID[1:0] value	传输类型（TYPE[1:0]值）	传输方向（DIR值）	USBHS operation
00b (NAK)	批量或中断	不依赖于设置	返回NAK以响应来自USB主机的令牌
	Isochronous	接收方向(DIR=0)	响应来自USB主机的令牌，不返回任何内容
		发射方向(DIR=1)	传输一个长度为零的数据包以响应来自USB主机的令牌
01b (BUF)	Bulk	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK或NYET以响应来自USB主机的OUT令牌。否则，返回NAK。 如果与所选管道关联的FIFO缓冲区已准备好接收，则返回ACK以响应来自USB主机的PING令牌。否则，返回NAK。
	Interrupt	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK响应以响应来自USB主机的OUT令牌。否则，返回NAK。
	批量或中断	发射方向(DIR=1)	如果与所选管道关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，返回NAK。
	Isochronous	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据以响应来自USB主机的OUT令牌。否则，丢弃数据。
		发射方向(DIR=1)	如果关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，发送一个零长度数据包。
10b (STALL) or 11b (STALL)	批量或中断	不依赖于设置。	返回STALL以响应来自USB主机的令牌
	Isochronous	不依赖于设置。	响应来自USB主机的令牌，不返回任何内容

PBUSY标志（管道忙标志）

PBUSY标志指示所选管道是否正在用于当前事务。

USBHS在所选管道的USB事务开始时将PBUSY位从0更改为1，并更改PBUSY位在一个事务完成时从1变为0。

在PID设置为NAK后，通过软件读取PBUSY位可以检查是否可以更改管道设置。详见29.3.7.1节。管道控制寄存器切换程序。

SQMON flag (Sequence Toggle Bit Monitor Flag)

The SQMON flag indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

When the selected pipe is not the isochronous transfer type, the USBHS toggles the SQMON flag on successful completion of the transaction. However, the USBHS does not toggle the SQMON flag when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through the software causes the USBHS to set DATA1 as the expected value of the sequence toggle bit for the next transaction on the selected pipe.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through the software causes the USBHS to clear the expected value of the sequence toggle bit for the next transaction on the selected pipe to DATA0.

In host controller mode, when this bit is set to 1 for a bulk OUT transfer pipe, the USBHS starts the next transfer for the selected pipe from a PING token.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 29.12 shows the data cleared by writing 1 and 0 continuously to the ACLRM bit and the cases in which this processing is required.

Table 29.12 Data cleared by the USBHS when ACLRM = 1

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe (two FIFO buffers in double buffer mode)	When clearing all data in the FIFO buffer allocated to the selected pipe
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value

ATREPM bit (Auto Response Mode)

The ATREPM bit enables or disables auto response mode for the selected pipe.

This bit can be set to 1 in device controller mode when the selected pipe is the bulk transfer type. When the bit is set to 1, the USBHS responds to the token from the USB host as follows:

- When the selected pipe is set for bulk IN transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 1):
  - When the ATREPM bit = 1 and PID = BUF, the USBHS transmits a zero-length packet in response to the IN token.
  - The USBHS updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USBHS receives ACK from the USB host. In a single transaction, the IN token is received, a zero-length packet is transmitted, and then ACK is received. The USBHS does not generate the BRDY or BEMP interrupt.
- When the selected pipe is set for bulk OUT transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 0):
  When the ATREPM bit = 1 and PID = BUF, the USBHS returns NAK in response to the OUT token or PING token and generates an NRDY interrupt.

For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode. When the selected pipe uses isochronous transfer, always set this bit to 0.

In host controller mode, always set the ATREPM bit to 0.

CSSTS flag (CSSTS Status Flag)

In host controller mode, the CSSTS flag indicates the complete-split status of a split transaction. It is valid for pipes that are not the isochronous transfer type.

The USBHS sets the CSSTS flag to 1 at the beginning of the complete-split transaction, and sets the CSSTS flag to 0 on detecting completion of the complete-split transaction. If a detach event is detected during the transaction, the CSSTS flag might stay set to 1. In this case, clear the CSSTS flag by setting the CSCLR bit to 1.

SQMON标志（序列切换位监控标志）

SQMON标志指示所选管道的下一个事务的序列切换位的预期值。

当所选管道不是同步传输类型时，USBHS在事务成功完成时切换SQMON标志。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBHS不会触发SQMON标志。

SQSET位（序列切换位设置）

通过软件将SQSET位设置为1会导致USBHS将DATA1设置为所选管道上下一个事务的序列切换位的预期值。

SQCLR位（序列翻转位清除）

通过软件将SQCLR位设置为1会导致USBHS将所选管道上下一个事务的序列切换位的预期值清除为DATA0。

在主机控制器模式下，当该位为批量OUT传输管道设置为1时，USBHS从PING令牌开始选定管道的下一次传输。

ACLRM位（自动缓冲区清除模式）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。要完全清除分配给所选管道的FIFO缓冲区中的数据，请向ACLRM位连续写入1和0。

表29.12显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 29.12 当ACLRM=1时USBHS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	FIFO缓冲区中的所有数据分配给所选管道（双缓冲区模式下的两个FIFO缓冲区）	清除分配给所选管道的FIFO缓冲区中的所有数据时
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时

ATREPM位（自动响应模式）

ATREPM位启用或禁用所选管道的自动响应模式。

当所选管道为批量传输类型时，该位可以在设备控制器模式下设置为1。当该位设置为1时，USBHS响应来自USB主机的令牌，如下所示：

●Whentheselectedpipeissetforbulk INtransfers(PIPECFG.TYPE[1:0]=01bandPIPECFG.DIR=1):

当ATREPM位=1且PID=BUF时，USBHS发送一个长度为零的数据包以响应IN令牌。

每次USBHS从USB主机接收到ACK时，USBHS都会更新（允许切换）序列切换位(DATA-PID)。在单个事务中，收到IN令牌，发送零长度数据包，然后收到ACK。USBHS不会产生BRDY或BEMP中断。

●当所选管道设置为批量OUT传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=0）：
当ATREPM位=1且PID=BUF时，USBHS返回NAK以响应OUT令牌或PING令牌并产生NRDY中断。

对于自动响应模式下的USB通信，当FIFO缓冲区为空时，将ATREPM位设置为1。在自动响应模式下的USB通信期间不要写入FIFO缓冲区。当所选管道使用同步传输时，始终将此位设置为0。

在主机控制器模式下，始终将ATREPM位设置为0。

CSSTS标志（CSSTS状态标志）

在主机控制器模式下，CSSTS标志指示拆分事务的完全拆分状态。它对非同步传输类型的管道有效。

USBHS在完成拆分事务开始时将CSSTS标志设置为1，并在检测到完成拆分事务完成时将CSSTS标志设置为0。如果在事务期间检测到分离事件，CSSTS标志可能保持设置为1。在这种情况下，通过将CSCLR位设置为1来清除CSSTS标志。

Values read from the CSSTS flag in device controller mode are invalid.

CSCLR bit (CSPLIT Status Clear)

In host controller mode, if the software sets the CSCLR bit to 1, the USBHS clears the CSSTS flag to 0. In split transactions, set the CSCLR bit to 1 by software to force the next transfer to restart from start-split. Because the USBHS automatically clears the CSSTS flag to 0 at the end of a successful complete-split transaction in a normal split transaction, clearing the flag through software is not required. Only clear the CSSTS flag using the CSCLR bit when the DVSTCTR0.UACT bit is set to 0 or when no transfer was made after a detach detect. If the CSCLR bit is set to 1 while the CSSTS flag is 0, the CSSTS flag remains 0.

In device controller mode, always write 0 to the CSCLR bit.

INBUFM flag (Transmit Buffer Monitor Flag)

The INBUMFM flag indicates the FIFO buffer status for the selected pipe in the transmitting direction.

When the selected pipe is set in the transmitting direction (PIPECFG.DIR = 1), the USBHS sets this bit to 1 when the CPU or DMA/DTC completes writing data to at least one FIFO buffer plane.

The USBHS sets this bit to 0 when the USBHS completes transmission of data from the FIFO buffer plane to which all the data is written. In double buffer mode (PIPECFG.DBLB = 1), the USBHS sets the INBUFM flag to 0 when the USBHS completes transmission of data from the two FIFO buffer planes before the CPU or DMA/DTC completes writing data to one FIFO buffer plane.

The INBUFM flag indicates the same value as the BSTS flag when the selected pipe is in the receiving direction (PIPECFG.DIR = 0).

BSTS flag (Buffer Status Flag)

The BSTS flag indicates the FIFO buffer status for the selected pipe. The meaning of the BSTS flag depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 29.13.

Table 29.13 BSTS flag operation

DIR value	BFRE value	DCLRM value	Meaning of BSTS flag
0	0	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
		1	Setting prohibited
	1	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 when the software sets the BCLR bit in the port control register to 1 after the data read is complete
		1	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
1	0	0	Sets to 1 when transmit data can be written to the FIFO buffer, and clears to 0 on completion of data write
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

29.2.39 PIPEnTRE : Pipe n Transaction Counter Enable Register (n = 1 to 5)

Base address: USBHS = 0x4011_1000

Offset address: 0x090 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	0	0	x	x	x	x	x	x	x	x

在设备控制器模式下从CSSTS标志读取的值无效。

CSCLR位（CSPLIT状态清除）

在主机控制器模式下，如果软件将CSCLR位设置为1，则USBHS将CSSTS标志清除为0。在拆分事务中，通过软件将CSCLR位设置为1，以强制下一次传输从start-split重新开始。由于USBHS在正常拆分事务中成功完成拆分事务结束时会自动将CSSTS标志清零，因此不需要通过软件清除该标志。仅当DVSTCTR0.UACT位设置为0或在分离检测后未进行传输时，才使用CSCLR位清除CSSTS标志。如果CSCLR位设置为1，而

CSSTS标志为0，CSSTS标志保持为0。

在设备控制器模式下，始终将0写入CSCLR位。

INBUFM标志（发送缓冲区监控标志）

INBUMFM标志指示发送方向上所选管道的FIFO缓冲区状态。

当所选管道设置为发送方向(PIPECFG.DIR=1)时，当CPU或DMADTC完成将数据写入至少一个FIFO缓冲区平面时，USBHS将该位设置为1。

当USBHS完成从写入所有数据的FIFO缓冲区平面的数据传输时，USBHS将该位设置为0。在双缓冲模式(PIPECFG.DBLB=1)中，当USBHS在CPU或DMADTC完成将数据写入一个FIFO缓冲平面之前完成从两个FIFO缓冲平面的数据传输时，USBHS将INBUFM标志设置为0。

当所选管道处于接收方向时（PIPECFG.DIR=0），INBUFM标志表示与BSTS标志相同的值。

BSTS标志（缓冲区状态标志）

BSTS标志指示所选管道的FIFO缓冲区状态。BSTS标志的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表29.13所示。

Table 29.13 BSTS标志操作

方向值	BFRE value	DCLRM value	BSTS标志的含义
0	0	0	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
		1	禁止设定
	1	0	接收数据可以从FIFO缓冲区读取时设置为1，当数据读取完成后软件将端口控制寄存器中的BCLR位设置为1时清除为0
		1	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
1	0	0	当发送数据可以写入FIFO缓冲区时设置为1，并在数据写入完成时清除为0
		1	禁止设定
	1	0	禁止设定
		1	禁止设定

29.2.39 PIPEnTRE:管道n事务计数器启用寄存器(n=1到5)

Base address: USBHS = 0x4011_1000

Offset address: 0x090 + 0x4 × (n - 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
重置后的值:	x	x	x	x	x	x	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	—	The read values are undefined. The write value should be 0.	R/W
8	TRCLR	Transaction Counter Clear 0: Invalid (writing 0 has no effect) 1: Clear current counter value	R/W
9	TRENB	Transaction Counter Enable 0: Disable transaction counter 1: Enable transaction counter	R/W
15:10	—	The read values are undefined. The write value should be 0.	R/W

Note: Only change the PIPEnTRE register settings while the PIPEnCTR.CSSTS flag is 0 and the PIPEnCTR.PID[1:0] bits are 00b (NAK response). Only change the PIPEnCTR.PID[1:0] bits of the selected pipe from 01b (BUF response) to 00b (NAK response) after confirming that the value of the PIPEnCTR.PBUSY and PIPEnCTR.CSSTS flags is 0. However, software processing to check the PIPEnCTR.PBUSY flag is not required if the USBHS has changed the PID[1:0] bits to 00b (NAK response).

TRCLR bit (Transaction Counter Clear)

When the TRCLR bit sets to 1, the USBHS clears the count value of the transaction counter associated with the selected pipe and then clears the TRCLR bit to 0.

TRENB bit (Transaction Counter Enable)

The TRENB bit enables or disables the transaction counter.

For receiving pipes, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through the software allows the USBHS to control hardware on having received the number of packets equal to the TRNCNT[15:0] setting as follows:

- When the PIPECFG.SHTNAK bit is 1, the USBHS changes the PID bits to NAK for the associated pipe on having received the number of packets equal to the TRNCNT[15:0] setting
- When the PIPECFG.BFRE bit is 1, the USBHS asserts the BRDY interrupt on having received the number of packets equal to the TRNCNT[15:0] setting and then reading the last received data.

For transmitting pipes, set the TRENB bit to 0.

When the transaction counter is not used, set this bit to 0. When the transaction counter is used, set the TRNCNT[15:0] bits before setting this bit to 1. Set this bit to 1 before receiving the first packet to be counted by the transaction counter.

29.2.40 PIPEnTRN : Pipe n Transaction Counter Register (n = 1 to 5)

Base address: USBHS = 0x4011_1000

Offset address: 0x092 + 0x4 × (n - 1)

Bit position:	15															0
Bit field:	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TRNCNT[15:0]	Transaction Counter*1 • When written to: Specifies the total packets (number of transactions) to be received by pipe n. • When read from: When PIPEnTRE.TRENB is 0, indicates the specified number of transactions. When PIPEnTRE.TRENB is 1, indicates the current transaction count.	R/W

Note 1. Only set the TRNCNT[15:0] bits while PID is NAK and PIPEnTRE.TRENB is 0. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

The PIPEnTRN registers retain their settings during a USB bus reset.

Bit	Symbol	Function	R/W
7:0	—	读取的值未定义。写入值应为0。	R/W
8	TRCLR	交易计数器清除 0：无效（写0无效）1：清除当前计数器值	R/W
9	TRENB	事务计数器启用 0：禁用事务计数器1：启用事务计数器	R/W
15:10	—	读取的值未定义。写入值应为0。	R/W

Note: 仅在PIPEnCTR.CSSTS标志为0且PIPEnCTR.PID[1:0]位为00b（NAK响应）时更改PIPEnTRE寄存器设置。仅在确认PIPEnCTR.PBUSY和PIPEnCTR.CSSTS标志的值为0后，将所选管道的PIPEnCTR.PID[1:0]位从01b（BUF响应）更改为00b（NAK响应）。但是，软件处理如果USBHS已将PID[1:0]位更改为00b（NAK响应），则不需要检查PIPEnCTR.PBUSY标志。

TRCLR位（事务计数器清零）

当TRCLR位设置为1时，USBHS清除与所选管道关联的事务计数器的计数值，然后将TRCLR位清除为0。

TRENB位（事务计数器使能）

TRENB位启用或禁用事务计数器。

对于接收管道，在设置接收管道的总包数后，将TRENB位设置为1
PIPEnTRN.TRNCNT[15:0]位通过软件允许USBHS在接收到等于TRNCNT[15:0]设置的数据包数量时控制硬件，如下所示：

●当PIPECFG.SHTNAK位为1时，USBHS在接收到等于TRNCNT[15:0]设置的数据包数量时将关联管道的PID位更改为NAK

●当PIPECFG.BFRE位为1时，USBHS在接收到等于TRNCNT[15:0]设置的数据包数量并读取最后接收到的数据时触发BRDY中断。

对于传输管道，将TRENB位设置为0。

当不使用事务计数器时，将该位设置为0。当使用事务计数器时，将该位设置为1之前设置TRNCNT[15:0]位。在接收第一个要计数的数据包之前将该位设置为1由交易柜台。

29.2.40 PIPEnTRN:管道n事务计数器寄存器(n=1到5)

Base address: USBHS = 0x4011_1000

Offset address: 0x092 + 0x4 × (n - 1)

Bit position:	15															0
Bit field:	TRNCNT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TRNCNT[15:0]	交易柜台*1 • 写入时： 指定管道n接收的总数据包（事务数）。 • 从以下位置读取时： 当PIPEnTRE.TRENB为0时，表示指定的事务数。 当PIPEnTRE.TRENB为1时，表示当前事务计数。	R/W

注1.仅当PID为NAK且PIPEnTRE.TRENB为0时设置TRNCNT[15:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

PIPEnTRN寄存器在USB总线复位期间保留其设置。

TRNCNT[15:0] bits (Transaction Counter)

The USBHS increments the value of the TRNCNT[15:0] bits by one when all of the following conditions are satisfied on receiving the packet:

- The PIPEnTRE.TRENB bit is 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting

The USBHS clears the value of the TRNCNT[15:0] bits to 0 when any of the following conditions is satisfied.

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting

Both the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The USBHS received a short packet

Both the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The PIPEnTRE.TRCLR bit was set to 1 by software

For transmitting pipes, set the TRNCNT[15:0] bits to 0. When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.

Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is enabled only when the PIPEnTRE.TRENB bit is 0. To set the number of transactions to be transferred, set the TRCLR bit to 1 to clear the current counter value before setting the PIPEnTRE.TRENB bit to 1.

29.2.41 DEVADDn : Device Address n Configuration Register (n = 0 to 9, A)

Base address: USBHS = 0x4011_1000

Offset address: 0x0D0 + 0x2 × n (n = 0 to 9)
0x0E4 (n = A)

Bit position:	15	14			10			7		5	4	3	2	1	0
Bit field:	—	UPPHUB[3:0]				HUBPORT[2:0]			USBSPD[1:0]	—	—	—	—	—	—
Value after reset:	x	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x

Bit	Symbol	Function	R/W
5:0	—	The read values are undefined. The write value should be 0.	R/W
7:6	USBSPD[1:0]	Transfer Speed of Communication Target Device 0 0: Do not use DEVADDm 0 1: Low speed 1 0: Full speed 1 1: High speed	R/W
10:8	HUBPORT[2:0]	Communication Target Connecting Hub Port 0 0 0: Connect directly to the USBHS port Others: Port number of the hub	R/W
14:11	UPPHUB[3:0]	Communication Target Connecting Hub Register 0x0: Connect directly to the USBHS port Others: USB address of the hub. The value as 0xB or more is reserved.	R/W
15	—	The read value is undefined. The write value should be 0.	R/W

TRNCNT[15:0] bits (Transaction Counter)

当接收到数据包时满足以下所有条件时，USBHS将TRNCNT[15:0]位的值加一：

●PIPEnTRE.TRENB位为1
●(TRNCNT[15:0]设定值≠当前计数器值+1)收到数据包
●接收数据包的有效载荷与PIPEMAXP.MXPS[8:0]设置一致

当满足以下任一条件时，USBHS将TRNCNT[15:0]位的值清零。

满足以下所有条件：

●PIPEnTRE.TRENB位=1
●(TRNCNT[15:0]setvalue=currentcountervalue+1)收到数据包
●接收数据包的有效载荷与PIPEMAXP.MXPS[8:0]设置一致

满足以下两个条件：

●PIPEnTRE.TRENB位=1
●USBHS收到一个短数据包

满足以下两个条件：

●PIPEnTRE.TRENB位=1
●PIPEnTRE.TRCLR位由软件设置为1

对于传输管道，将TRNCNT[15:0]位设置为0。当不使用事务计数器时，将TRNCNT[15:0]位设置为0。

仅当PIPEnTRE.TRENB位为0时才使能将要传输的事务数设置到TRNCNT[15:0]位。要设置要传输的事务数，请将TRCLR位设置为1以清除当前计数器将PIPEnTRE.TRENB位设置为1之前的值。

29.2.41 DEVADDn：器件地址n配置寄存器（n=0到9，A）

Base address: USBHS = 0x4011_1000

Offset address: 0x0D0 + 0x2 × n (n = 0 to 9)
0x0E4 (n = A)

Bit position:	15	14			10			7		5	4	3	2	1	0
Bit field:	—	UPPHUB[3:0]				HUBPORT[2:0]			USBSPD[1:0]	—	—	—	—	—	—
重置后的值：	x	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x

Bit	Symbol	Function	R/W
5:0	—	读取的值未定义。写入值应为0。	R/W
7:6	USBSPD[1:0]	通信目标设备的传输速度 00：不使用DEVADDm01： 低速10：全速11：高速	R/W
10:8	HUBPORT[2:0]	通信对象连接集线器端口 000：直接连接到USBHS端口 其他：集线器的端口号	R/W
14:11	UPPHUB[3:0]	通信对象连接集线器寄存器 0x0：直接连接到USBHS端口 其他：集线器的USB地址。保留0xB或更大的值。	R/W
15	—	读取值未定义。写入值应为0。	R/W

The DEVADDn register specifies the transfer speed of the peripheral device that is the communication target for pipes 0 to 9.

In host controller mode, set all DEVADDn bits before starting communication to any pipes. Only change the bits in DEVADDn when no valid pipes are using the bit settings. A valid pipe is defined as one that satisfies both of the following conditions:

- DEVADDm is selected in the DEVSEL[3:0] bits
- The PID[1:0] bits are set to BUF for the selected pipe, or the selected pipe is the DCP with the DCPCTR.SUREQ bit set to 1

In device controller mode, set all bits in this register to 0.

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

The USBSPD[1:0] bits specify the USB transfer speed of the target peripheral device. In host controller mode, the USBHS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.

HUBPORT[2:0] bits (Communication Target Connecting Hub Port)

In host controller mode, the USBHS generates packets based on the HUBPORT[2:0] setting when performing a split transaction.

UPPHUB[3:0] bits (Communication Target Connecting Hub Register)

In host controller mode, the USBHS generates packets based on the UPPHUB[3:0] setting when performing a split transaction.

29.2.42 LPCTRL : Low Power Control Register

Base address: USBHS = 0x4011_1000

Offset address: 0x100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	HWUPM	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	0	0	x	x	x	x	x	x	0

Bit	Symbol	Function	R/W
6:0	—	The read values are undefined. The write value should be 0.	R/W
7	HWUPM	Resume Return Mode Setting 0: Hardware does not recover while CPU clock inactive 1: Hardware recovers while CPU clock inactive	R/W
8	—	This bit is read as 0. The write value should be 0.	R/W
15:9	—	The read values are undefined. The write value should be 0.	R/W

HWUPM bit (Resume Return Mode Setting)

The HWUPM bit specifies whether to enable hardware processing for return from low power mode even while the CPU clock is inactive.

In device controller mode, processing for return from low power mode on detecting Resume is enabled even while the CPU clock is inactive.

This bit specifies whether to detect Resume while the CPU clock is inactive. The PL1CTRL1.L1EXTMD bit controls whether to make a hardware return. To make a hardware return from the LPM L1 low power state while the CPU clock is inactive, set this bit and the PL1CTRL1.L1EXTMD bit to 1.

DEVADDn寄存器指定作为管道0到9的通信目标的外围设备的传输速度。

在主机控制器模式下，在开始与任何管道通信之前设置所有DEVADDn位。仅更改中的位DEVADDn当没有有效管道使用位设置时。有效管道被定义为同时满足以下两个条件的管道：

- DEVADDm在DEVSEL[3:0]位中选择
- 所选管道的PID[1:0]位设置为BUF，或者所选管道是DCPCTR.SUREQ位设置为1的DCP

在设备控制器模式下，将此寄存器中的所有位设置为0。

USBSPD[1:0]位（通信目标设备的传输速度）

USBSPD[1:0]位指定目标外围设备的USB传输速度。在主机控制器模式下，USBHS根据USBSPD[1:0]设置生成数据包。在设备控制器模式下，将这些位设置为00b。

HUBPORT[2:0]位（通信目标连接集线器端口）

在主机控制器模式下，USBHS在执行拆分事务时根据HUBPORT[2:0]设置生成数据包。

UPPHUB[3:0]位（通信目标连接集线器寄存器）

在主机控制器模式下，USBHS在执行拆分事务时根据UPPHUB[3:0]设置生成数据包。

29.2.42 LPCTRL:低功耗控制寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x100

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	HWUPM	—	—	—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	0	0	x	x	x	x	x	x	0

Bit	Symbol	Function	R/W
6:0	—	读取的值未定义。写入值应为0。	R/W
7	HWUPM	恢复返回模式设置 0：CPU时钟不活动时硬件不恢复1：CPU时钟不活动时硬件恢复	R/W
8	—	该位读取为0。写入值应为0。	R/W
15:9	—	读取的值未定义。写入值应为0。	R/W

HWUPM位（恢复返回模式设置）

HWUPM位指定是否启用硬件处理以从低功耗模式返回，即使在CPU时钟不活动时也是如此。

在设备控制器模式下，即使CPU时钟处于非活动状态，也会启用在检测到Resume时从低功耗模式返回的处理。

该位指定是否在CPU时钟不活动时检测Resume。PL1CTRL1.L1EXTMD位控制是否进行硬件返回。要在CPU时钟不活动时使硬件从LPML1低功耗状态返回，设置该位和PL1CTRL1.L1EXTMD位为1。

29.2.43 LPSTS : Low Power Status Register

Base address: USBHS = 0x4011_1000

Offset address: 0x102

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	SUSP ENDM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	0	x	0	x	x	x	0	x	x	x	x	0	x	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	—	The read value is undefined. The write value should be 0.	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
7:4	—	The read values are undefined. The write value should be 0.	R/W
8	—	This bit is read as 0. The write value should be 0.	R/W
11:9	—	The read values are undefined. The write value should be 0.	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	—	The read value is undefined. The write value should be 0.	R/W
14	SUSPENDM	UTMI SuspendM Control 0: UTMI suspension mode 1: UTMI normal mode	R/W
15	—	The read value is undefined. The write value should be 0.	R/W

SUSPENDM bit (UTMI SuspendM Control)

The SUSPENDM bit controls the SuspendM signal to be sent to the PHY designed under the UTMI specification. The initial value is 0 with the UTMI is in suspension mode.

Set this bit to 1 to supply the PHY clock to operate the USB2.0 host or device controller.

In compliance with the UTMI specification, clock output is normally controlled by the SuspendM signal. When the SUSPENDM bit is 0, the clock to LINK is stopped. Because the PHY in this MCU follows the UTMI specification, setting the SUSPENDM bit to 1 is required to supply the PHY clock. For the clock settings, see section 29.3.3. Supplying the Clock.

When the SUSPENDM bit is 0, the USBHS cannot be written to but can be read from. The registers listed in Table 29.14 are writable even when the SUSPENDM bit is 0.

Table 29.14 Registers that can be written to by software when SUSPENDM = 0

Address	Register or bit name
0x4006_0000	SYSCFG register
0x4006_0002	BUSWAIT register
0x4006_0032	INTENB1.PDDETINTE bit
0x4006_0100	LPCTRL register
0x4006_0102	LPSTS register
0x4006_0140	BCCTRL register

The value written to the SYSCFG register while the PHY clock is inactive is updated only after the PHY clock begins oscillating. The PHY clock oscillates in the following cases described in this section.

When SUSPENDM bit is set to 1, the PLLSTA.PLLLOCK flag is set to 1 after the predetermined time has passed. The USB-PHY internal PLL is stopped when the SUSPENDM bit is set to 0.

For details on CL-only mode, see section 29.2.17. PHYSET : PHY Setting Register.

29.2.43 LPSTS：低功耗状态寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x102

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	SUSP ENDM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	x	0	x	0	x	x	x	0	x	x	x	x	0	x	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	—	读取值未定义。写入值应为0。	R/W
3	—	该位读取为0。写入值应为0。	R/W
7:4	—	读取的值未定义。写入值应为0。	R/W
8	—	该位读取为0。写入值应为0。	R/W
11:9	—	读取的值未定义。写入值应为0。	R/W
12	—	该位读取为0。写入值应为0。	R/W
13	—	读取值未定义。写入值应为0。	R/W
14	SUSPENDM	UTMI SuspendM Control 0：UTMI暂停模式1：UTMI 正常模式	R/W
15	—	读取值未定义。写入值应为0。	R/W

SUSPENDM bit (UTMI SuspendM Control)

SUSPENDM位控制要发送到根据UTMI规范设计的PHY的SuspendM信号。初始值为0，UTMI处于暂停模式。

将此位设置为1以提供PHY时钟以操作USB2.0主机或设备控制器。

根据UTMI规范，时钟输出通常由SuspendM信号控制。当。。。的时候
SUSPENDM位为0，LINK时钟停止。由于该MCU中的PHY遵循UTMI规范，因此需要将SUSPENDM位设置为1以提供PHY时钟。有关时钟设置，请参阅第29.3.3节。提供时钟。

当SUSPENDM位为0时，USBHS不能被写入但可以被读取。即使SUSPENDM位为0，表29.14中列出的寄存器也是可写的。

Table 29.14 SUSPENDM=0时软件可写入的寄存器

Address	寄存器或位名称
0x4006_0000	SYSCFG register
0x4006_0002	BUSWAIT register
0x4006_0032	INTENB1.PDDETINTE bit
0x4006_0100	LPCTRL register
0x4006_0102	LPSTS register
0x4006_0140	BCCTRL register

PHY时钟不活动时写入SYSCFG寄存器的值仅在PHY时钟开始振荡后更新。PHY时钟在本节所述的以下情况下振荡。

当SUSPENDM位设置为1时，PLLSTA.PLLLOCK标志在经过预定时间后设置为1。这
当SUSPENDM位设置为0时，USB-PHY内部PLL停止。

有关CL-only模式的详细信息，请参阅第29.2.17节。PHYSET：PHY设置寄存器。

If the PL1CTRL1.L1EXTMD bit is 0, setting or clearing of this bit is controlled by software. If the PL1CTRL1.L1EXTMD bit is 1, transitions to the L1 or L2 state of this bit are controlled by software and recovery from the L1 or L2 state is controlled by hardware.

29.2.44 BCCTRL : Battery Charging Control Register

Base address: USBHS = 0x4011_1000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PDDETSTS	CHGDETSTS	—	—	DCPMODE	VDMSRCE	IDPSINKE	VDPSRCE	IDMSINKE	IDPSRCE
Value after reset:	x	x	x	x	x	x	0	0	x	x	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IDPSRCE	IDPSRC Control*2 0: Disable IDP_SRC circuit 1: Enable IDP_SRC circuit	R/W
1	IDMSINKE	IDMSINK Control*2 0: Disable IDM_SINK circuit 1: Enable IDM_SINK circuit	R/W*1
2	VDPSRCE	VDPSRC Control*2 0: Disable VDP_SRC circuit 1: Enable VDP_SRC circuit	R/W
3	IDPSINKE	IDPSINK Control*2 0: Disable IDP_SINK circuit 1: Enable IDP_SINK circuit	R/W
4	VDMSRCE	VDMSRC Control*2 0: Disable VDM_SRC circuit 1: Enable VDM_SRC circuit	R/W
5	DCPMODE	DCP Mode Control 0: Disable RDCP_DAT resistor 1: Enable RDCP_DAT resistor	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	CHGDETSTS	CHGDET Status Flag 0: The CHGDET pin is at low level 1: The CHGDET pin is at high level	R
9	PDDETSTS	PDDET Status Flag 0: The PDDET pin is at low level 1: The PDDET pin is at high level	R
15:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. All bits in the BCCTRL register can be changed while the UTMI clock is inactive.
Note 2. In device controller mode, set the IDPSRCE, IDMSINKE, VDPSRCE, IDPSINKE, and VDMSRCE bits to 1 after setting the SYSCFG.DRPD bit to 0.

IDPSRCE bit (IDPSRC Control)

In device controller mode, set the IDPSRCE bit to 1 to perform data contact detection.

The Battery Charging Standard provides two ways to handle data contact detection, one through the software and one using hardware to contact the data line. The IDPSRE bit uses the hardware method.

When the IDPSRE bit is set to 1, the USBHS enables the IDP_SRC circuit and, at the same time, controls D- pull-down.

(D- pull-down is controlled with the VUH_DMPULLDOWN signal.)

IDMSINKE bit (IDMSINK Control)

In device controller mode, set the IDMSINKE bit to 1 to perform primary detection.

如果PL1CTRL1.L1EXTMD位为0，则该位的设置或清除由软件控制。如果PL1CTRL1.L1EXTMD位为1，则转换到该位的L1或L2状态由软件控制，从L1或L2状态恢复由硬件控制。

29.2.44 BCCTRL:电池充电控制寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x140

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	PDDETSTS	CHGDETSTS	—	—	DCPMODE	VDMSRCE	IDPSINKE	VDPSRCE	IDMSINKE	IDPSRCE
重置后的值:	x	x	x	x	x	x	0	0	x	x	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IDPSRCE	IDPSRC Control*2 0：禁用IDP_SRC电路1：启用IDP_SRC电路	R/W
1	IDMSINKE	IDMSINK Control*2 0：禁用IDM_SINK电路1：启用IDM_SINK电路	R/W*1
2	VDPSRCE	VDPSRC Control*2 0：禁用VDP_SRC电路1：启用VDP_SRC电路	R/W
3	IDPSINKE	IDPSINK Control*2 0：禁用IDP_SINK电路1：启用IDP_SINK电路	R/W
4	VDMSRCE	VDMSRC Control*2 0：禁用VDM_SRC电路1：启用VDM_SRC电路	R/W
5	DCPMODE	DCP模式控制 0：禁用RDCP_DAT电阻1：启用RDCP_DAT电阻	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
8	CHGDETSTS	CHGDET状态标志 0：CHGDET引脚为低电平1：CHGDET引脚为高电平	R
9	PDDETSTS	PDDET状态标志 0：PDDET引脚为低电平1：PDDET引脚为高电平	R
15:10	—	这些位被读取为0。写入值应为0。	R/W

注1.当UTMI时钟无效时，BCCTRL寄存器中的所有位都可以更改。
注2.在设备控制器模式下，设置IDPSRCE、IDMSINKE、VDPSRCE、IDPSINKE和VDMSRCE位为1后设置SYSCFG.DRPD位为0。

IDPSRCE bit (IDPSRC Control)

在设备控制器模式下，将IDPSRCE位设置为1以执行数据接触检测。

电池充电标准提供了两种处理数据接触检测的方法，一种是通过软件，另一种是通过硬件接触数据线。IDPSRE位使用硬件方法。

当IDPSRE位设置为1时，USBHS使能IDP_SRC电路，同时控制Dpull-down。

（Dpull-down由VUH_DMPULLDOWN信号控制。）

IDMSINKE bit (IDMSINK Control)

在设备控制器模式下，将IDMSINKE位设置为1以执行主要检测。

VDPSRCE bit (VDPSRC Control)

In device controller mode, set the VDPSRCE bit to 1 to perform primary detection.

IDPSINKE bit (IDPSINK Control)

In device controller mode, set the IDPSINKE bit to 1 to perform secondary detection. In host controller mode, set this bit to 1 to enable the portable device detection circuit.

VDMSRCE bit (VDMSRC Control)

In device controller mode, set the VDMSRCE bit to 1 to perform secondary detection. Setting this bit to 1 enables the DCP detection circuit. In host controller mode, set this bit to 1 when a portable device is detected. Setting this bit to 1 allows the device that is performing primary detection to determine the charger detection method.

DCPMODE bit (DCP Mode Control)

Set the DCPMODE bit to 1 to operate as a dedicated charging port (DCP). Setting this bit to 1 disables USB communication.

CHGDETSTS flag (CHGDET Status Flag)

The CHGDETSTS flag indicates the charger port detection state.

PDDETSTS flag (PDDET Status Flag)

The PDDETSTS flag indicates the following states based on the controller mode:

- In host controller mode: PD detection state
- In device controller mode: DCP detection state

29.2.45 PL1CTRL1 : Function L1 Control Register 1

Base address: USBHS = 0x4011_1000

Offset address: 0x144

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	L1EXTMD	—		HIRDTHR[3:0]				DVSQ[3:0]				L1NEGOMD	L1RESPMD[1:0]		L1RESPEN
Value after reset:	x	0	x	x	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	L1RESPEN	L1 Response Enable 0: Do not support LPM 1: Support LPM	R/W
2:1	L1RESPMD[1:0]	L1 Response Mode 0 0: NYET response 0 1: ACK response 1 0: STALL response 1 1: Response based on L1NEGOMD setting	R/W
3	L1NEGOMD	L1 Response Negotiation Control This bit is only valid when the L1RESPMD[1:0] value is 11b. 0: Return ACK when received HIRD is larger than HIRDTHR[3:0]. Otherwise (including when HIRD = HIRDTHR[3:0]), return NYET 1: Return ACK when received HIRD is smaller than HIRDTHR[3:0]. Otherwise (including when HIRD = HIRDTHR[3:0]), return NYET	R/W
7:4	DVSQ[3:0]	DVSQ Extension Flag 0 0 0 0: Powered state 0 0 0 1: Default state 0 0 1 0: Address state 0 0 1 1: Configured state 0 1 x x: Suspend state 1 0 x x: L1 state	R

VDPSRCE bit (VDPSRC Control)

在设备控制器模式下，将VDPSRCE位设置为1以执行主检测。

IDPSINKE bit (IDPSINK Control)

在设备控制器模式下，将IDPSINKE位设置为1以执行辅助检测。在主机控制器模式下，将此位设置为1以启用便携式设备检测电路。

VDMSRCE bit (VDMSRC Control)

在设备控制器模式下，将VDMSRCE位设置为1以执行辅助检测。将此位设置为1启用DCP检测电路。在主机控制器模式下，当检测到便携式设备时，将该位设置为1。将此位设置为1允许执行主检测的设备确定充电器检测方法。

DCPMODE位（DCP模式控制）

将DCPMODE位设置为1可用作专用充电端口(DCP)。将此位设置为1将禁用USB通信。

CHGDETSTS标志（CHGDET状态标志）

CHGDETSTS标志指示充电器端口检测状态。

PDDETSTS标志（PDDET状态标志）

PDDETSTS标志根据控制器模式指示以下状态：

●主控模式下：PD检测状态

●在设备控制器模式下：DCP检测状态

29.2.45 PL1CTRL1:功能L1控制寄存器1

Base address: USBHS = 0x4011_1000

Offset address: 0x144

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	L1EXTMD	—		HIRDTHR[3:0]				DVSQ[3:0]				L1NEGOMD	L1RESPMD[1:0]		L1RESPEN
重置后的值：	x	0	x	x	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	L1RESPEN	L1响应启用 0：不支持LPM1：支持 LPM	R/W
2:1	L1RESPMD[1:0]	L1响应模式 00：NYET响应01：ACK响应10：STALL响应1 1：基于L1NEGOMD设置的响应	R/W
3	L1NEGOMD	L1响应协商控制 该位仅在L1RESPMD[1:0]值为11b时有效。 0：当接收到的HIRD大于HIRDTHR[3:0]时返回ACK。否则（包括当HIRD=HIRDTHR[3:0]时），返回NYET 1：当接收到的HIRD小于HIRDTHR[3:0]时返回ACK。否则（包括当HIRD=HIRDTHR[3:0]时），返回NYET	R/W
7:4	DVSQ[3:0]	DVSQ扩展标志 0000：上电状态0001： 默认状态0010：地址状态 0011：配置状态01xx： 挂起状态10xx：L1状态	R

Bit	Symbol	Function	R/W
11:8	HIRDTHR[3:0]	L1 Response Negotiation Threshold Value HIRD threshold value used when the L1RESPMD[1:0] bits are 11b. The format is the same as the HIRD field in HL1CTRL.	R/W
13:12	—	The read values are undefined. The write value should be 0.	R/W
14	L1EXTMD	PHY Control Mode at L1 Return 0: Do not set LPSTS.SUSPENDM bit through hardware when Host K is received 1: Set LPSTS.SUSPENDM bit through hardware when Host K is received	R/W
15	—	The read value is undefined. The write value should be 0.	R/W

L1RESPEN bit (L1 Response Enable)

If the USBHS receives an LPM token while the L1RESPEN bit is 0, it returns no response. If the USBHS receives an LPM token while this bit is 1, it returns a response based on the L1RESPMD[1:0] setting.

L1RESPMD[1:0] bits (L1 Response Mode)

When the L1RESPEN bit is set to 1, the USBHS returns a response to the LPM token based on the setting in the L1RESPMD[1:0] bits.

L1NEGOMD bit (L1 Response Negotiation Control)

The L1NEGOMD bit specifies the negotiation function for the HIRD value.

HIRDTHR[3:0] bits (L1 Response Negotiation Threshold Value)

The HIRDTHR[3:0] bits specify the HIRD threshold value used for L1NEGOMD. The format of the set value is the same as the HIRD field in HL1CTRL.

L1EXTMD bit (PHY Control Mode at L1 Return)

The L1EXTMD bit specifies the LPSTS.SUSPENDM bit control method when a host K signal is received in the L1 state while the LPSTS.SUSPENDM bit is 0 and the PHY is inactive.

Similar to the Suspend constraints, because the minimum host K period is 50 µs, the PHY might not recover within the host K period specified for software settings on return. The initial value is within software control, so set this bit to 1 during the initialization process when the L1 state is supported.

The LPSTS.SUSPENDM bit is controlled by software on transition to the L1 state regardless of the setting in this bit. It is not cleared by hardware.

When this bit is set to 1, the LPSTS.SUSPENDM bit is also set to 1 on return from L2.

29.2.46 PL1CTRL2 : Function L1 Control Register 2

Base address: USBHS = 0x4011_1000

Offset address: 0x146

Bit position:	15	14	13	12	11					7	6	5	4	3	2	1	0
Bit field:	—	—	—	RWEMON	HIRDMON[3:0]					—	—	—	—	—	—	—	—
Value after reset:	x	x	x	0	0	0	0	0		x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	—	The read values are undefined. The write value should be 0.	R/W
11:8	HIRDMON[3:0]	HIRD Value Monitor When set, indicates that the HIRD field value reflects the lastreceived LPM token.	R
12	RWEMON	RWE Value Monitor When set, indicates that the RWE bit value reflects the lastreceived LPM token.	R
15:13	—	The read values are undefined. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
11:8	HIRDTHR[3:0]	L1响应协商阈值 L1RESPMD[1:0]位为11b时使用的HIRD阈值。格式与HL1CTRL中的HIRD字段相同。	R/W
13:12	—	读取的值未定义。写入值应为0。	R/W
14	L1EXTMD	L1返回的PHY控制模式 0：接收到HostK时不通过硬件设置LPSTS.SUSPENDM位1：接收到HostK时通过硬件设置LPSTS.SUSPENDM位	R/W
15	—	读取值未定义。写入值应为0。	R/W

L1RESPEN位（L1响应使能）

如果USBHS在L1RESPEN位为0时接收到LPM令牌，则它不返回任何响应。如果USBHS在该位为1时接收到LPM令牌，它会根据L1RESPMD[1:0]设置返回响应。

L1RESPMD[1:0]位（L1响应模式）

当L1RESPEN位设置为1时，USBHS根据
L1RESPMD[1:0] bits.

L1NEGOMD位（L1响应协商控制）

L1NEGOMD位指定HIRD值的协商功能。

HIRDTHR[3:0]位（L1响应协商阈值）

HIRDTHR[3:0]位指定用于L1NEGOMD的HIRD阈值。设置值的格式与HL1CTRL中的HIRD字段相同。

L1EXTMD位（L1返回时的PHY控制模式）

L1EXTMD位指定LPSTS.SUSPENDM位在L1状态下接收到主机K信号而LPSTS.SUSPENDM位为0且PHY处于非活动状态时的LPSTS.SUSPENDM位控制方法。

与挂起约束类似，由于最小主机K周期为50µs，因此PHY可能无法在返回时为软件设置指定的主机K周期内恢复。初始值在软件控制范围内，因此在支持L1状态的初始化过程中将此位设置为1。

LPSTS.SUSPENDM位在转换到L1状态时由软件控制，无论该位的设置如何。它不会被硬件清除。

当该位设置为1时，LPSTS.SUSPENDM位在从L2返回时也设置为1。

29.2.46 PL1CTRL2：功能L1控制寄存器2

Base address: USBHS = 0x4011_1000

Offset address: 0x146

Bit position:	15	14	13	12	11					7	6	5	4	3	2	1	0
Bit field:	—	—	—	RWEMON	HIRDMON[3:0]					—	—	—	—	—	—	—	—
重置后的值：	x	x	x	0	0	0	0	0		x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	—	读取的值未定义。写入值应为0。	R/W
11:8	HIRDMON[3:0]	HIRD价值监控器 设置时，指示HIRD字段值反映最后接收的LPM令牌。	R
12	RWEMON	RWE价值监控器 设置时，指示RWE位值反映最后接收的LPM令牌。	R
15:13	—	读取的值未定义。写入值应为0。	R/W

HIRDMON[3:0] bits (HIRD Value Monitor)

Access the HIRDMON[3:0] bits when monitoring the HIRD field value of the received LPM token. The bits reflect the HIRD field value of the last received LPM token.

RWEMON bit (RWE Value Monitor)

Access the RWEMON bit when monitoring the RWE field value of the received LPM token. The bits reflect the RWE field value of the last received LPM token.

29.2.47 HL1CTRL1 : Host L1 Control Register 1

Base address: USBHS = 0x4011_1000

Offset address: 0x148

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	L1STATUS[1:0]	L1REQ
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

Bit	Symbol	Function	R/W
0	L1REQ	L1 Transition Request Set this bit to 1 when requesting a transition to the L1 state. This bit is cleared to 0 by the hardware when the LPM transaction is complete.	R/W
2:1	L1STATUS[1:0]	L1 Request Completion Status Indicates the result of the LPM transaction made by the L1REQ bit: 0 0: ACK received 0 1: NYET received 1 0: STALL received 1 1: Transaction error	R
15:3	—	The read value is undefined. The write value should be 0.	R/W

L1REQ bit (L1 Transition Request)

Set the L1REQ bit to 1 to transition to the L1 state. When the USBHS detects that this bit is 1, it starts the LPM transaction. The USBHS clears this bit to 0 through hardware on completion of the transaction.

L1STATUS[1:0] bits (L1 Request Completion Status)

The L1STATUS[1:0] bits indicate the result of the LPM transaction initiated by the L1REQ bit.

29.2.48 HL1CTRL2 : Host L1 Control Register 2

Base address: USBHS = 0x4011_1000

Offset address: 0x14A

Bit position:	15	14	13	12	11	7	6	5	4	3	0
Bit field:	BESL	—	—	L1RWE	HIRD[3:0]	—	—	—	—	L1ADDR[3:0]	
Value after reset:	0	x	x	0	0	0	0	0	x	x	x	x	0	0	0	0

Bit	Symbol	Function	R/W
3:0	L1ADDR[3:0]	LPM Token DeviceAddress Specify the value to be set in the ADDR field of the LPM token	R/W
7:4	—	The read values are undefined. The write value should be 0.	R/W
11:8	HIRD[3:0]	LPM Token HIRD Specify the value to be set in the HIRD field of the LPM token	R/W
12	L1RWE	LPM Token L1 RemoteWake Enable Specify the value to be set in the RWE field of the LPM token	R/W

HIRDMON[3:0]位（HIRD值监视器）

在监控接收到的LPM令牌的HIRD字段值时访问HIRDMON[3:0]位。这些位反映了最后收到的LPM令牌的HIRD字段值。

RWEMON位（RWE值监视器）

在监控接收到的LPM令牌的RWE字段值时访问RWEMON位。这些位反映了最后收到的LPM令牌的RWE字段值。

29.2.47 HL1CTRL1：主机L1控制寄存器1

Base address: USBHS = 0x4011_1000

Offset address: 0x148

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	L1STATUS[1:0]	L1REQ
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

Bit	Symbol	Function	R/W
0	L1REQ	L1转换请求 当请求转换到L1状态时，将此位设置为1。当LPM事务完成时，该位由硬件清零。	R/W
2:1	L1STATUS[1:0]	L1请求完成状态 指示L1REQ位进行的LPM事务的结果： 00：收到ACK01：收到NYET10：收到STAL L11：交易错误	R
15:3	—	读取值未定义。写入值应为0。	R/W

L1REQ位（L1转换请求）

将L1REQ位设置为1以转换到L1状态。当USBHS检测到该位为1时，它启动LPM事务。USBHS在事务完成时通过硬件将该位清零。

L1STATUS[1:0]位（L1请求完成状态）

L1STATUS[1:0]位指示L1REQ位启动的LPM事务的结果。

29.2.48 HL1CTRL2：主机L1控制寄存器2

Base address: USBHS = 0x4011_1000

Offset address: 0x14A

Bit position:	15	14	13	12	11	7	6	5	4	3	0
Bit field:	BESL	—	—	L1RWE	HIRD[3:0]	—	—	—	—	L1ADDR[3:0]	
重置后的值：	0	x	x	0	0	0	0	0	x	x	x	x	0	0	0	0

Bit	Symbol	Function	R/W
3:0	L1ADDR[3:0]	LPM Token DeviceAddress 指定要在LPM令牌的ADDR字段中设置的值	R/W
7:4	—	读取的值未定义。写入值应为0。	R/W
11:8	HIRD[3:0]	LPM Token HIRD 指定要在LPM令牌的HIRD字段中设置的值	R/W
12	L1RWE	LPM令牌L1远程唤醒启用 指定要在LPM令牌的RWE字段中设置的值	R/W

Bit	Symbol	Function	R/W
14:13	—	The read values are undefined. The write value should be 0.	R/W
15	BESL	BESL & Alternate HIRD Selects the K-State drive period on L1 Resume	R/W

L1ADDR[3:0] bits (LPM Token DeviceAddress)

The L1ADDR[3:0] bits specify the value to be set in the ADDR field of the LPM token that the USBHS transmits when the HL1CTRL1.L1REQ bit is set to 1.

HIRD[3:0] bits (LPM Token HIRD)

The HIRD[3:0] bits specify the value to be set in the HIRD field of the LPM token that the USBHS transmits when the HL1CTRL1.L1REQ bit is set to 1. Table 29.15 shows the relationship between the HIRD settings and the HIRD field values.

Table 29.15 Relationship between the HIRD bit settings and the HIRD field values

HIRD[3:0] setting	When BESL = 0	When BESL = 1
0x0	50 µs (setting prohibited)	75 µs
0x1	125 µs	100 µs
0x2	200 µs	150 µs
0x3	275 µs	250 µs
0x4	350 µs	350 µs
0x5	425 µs	450 µs
0x6	500 µs	950 µs
0x7	575 µs	1950 µs
0x8	650 µs	2950 µs
0x9	725 µs	3950 µs
0xA	800 µs	4950 µs
0xB	875 µs	5950 µs
0xC	950 µs	6950 µs
0xD	1025 µs (setting prohibited)	7950 µs
0xE	1100 µs (setting prohibited)	8950 µs
0xF	1175 µs (setting prohibited)	9950 µs

Note: The set value of the HIRD bit is used for the host K drive period on host resume and for the host K period on remote wakeup.

L1RWE bit (LPM Token L1 RemoteWake Enable)

The L1RWE bit specifies the value to be set in the RWE field of the LPM token that the USBHS transmits when the HL1CTRL1.L1REQ bit is set to 1.

The USBHS does not control detection of the remote wakeup signal in the L1 state with this bit. The remote wakeup signal is controlled by the DVSTCTR0.RWUPE bit, as with Suspend.

BESL bit (BESL & Alternate HIRD)

The BESL bit selects the K-state drive period on L1 Resume. For details, see the description of the HIRD bits.

Bit	Symbol	Function	R/W
14:13	—	读取的值未定义。写入值应为0。	R/W
15	BESL	BESL & Alternate HIRD 在L1Resume上选择K-State驱动周期	R/W

L1ADDR[3:0]位（LPM令牌设备地址）

L1ADDR[3:0]位指定要在LPM令牌的ADDR字段中设置的值，当USBHS发送HL1CTRL1.L1REQ位设置为1。

HIRD[3:0]位（LPM令牌HIRD）

HIRD[3:0]位指定要在USBHS发送的LPM令牌的HIRD字段中设置的值。HL1CTRL1.L1REQ位设置为1。表29.15显示了HIRD设置和HIRD字段值之间的关系。

Table 29.15 HIRD位设置和HIRD字段值之间的关系

HIRD[3:0] setting	When BESL = 0	When BESL = 1
0x0	50 µs (setting prohibited)	75 µs
0x1	125 µs	100 µs
0x2	200 µs	150 µs
0x3	275 µs	250 µs
0x4	350 µs	350 µs
0x5	425 µs	450 µs
0x6	500 µs	950 µs
0x7	575 µs	1950 µs
0x8	650 µs	2950 µs
0x9	725 µs	3950 µs
0xA	800 µs	4950 µs
0xB	875 µs	5950 µs
0xC	950 µs	6950 µs
0xD	1025 µs (setting prohibited)	7950 µs
0xE	1100 µs (setting prohibited)	8950 µs
0xF	1175 µs (setting prohibited)	9950 µs

Note: HIRD位的设置值用于主机恢复时的主机K驱动周期和远程唤醒时的主机K周期。

L1RWE位（LPM令牌L1远程唤醒启用）

L1RWE位指定在USBHS发送的LPM令牌的RWE字段中设置的值。HL1CTRL1.L1REQ位设置为1。

USBHS不通过该位控制L1状态下远程唤醒信号的检测。远程唤醒信号由DVSTCTR0.RWUPE位控制，与挂起一样。

BESL位（BESL和备用HIRD）

BESL位选择L1Resume上的K状态驱动周期。有关详细信息，请参见HIRD位的说明。

29.2.49 DPUSR0R : Deep Software Standby USB Transceiver Control/Pin Monitor Register

Base address: USBHS = 0x4011_1000

Offset address: 0x160

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBSTSHM	—	DOVCBHM	DOVCAHM	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
19:0	—	These bits are read as 0. The write value should be 0.	R
20	DOVCAHM	OVRCURA Input Flag Indicates OVRCURA input signal on the USBHS side	R
21	DOVCBHM	OVRCURB Input Flag Indicates OVRCURB input signal on the USBHS side	R
22	—	This bit is read as 0. The write value should be 0.	R
23	DVBSTSHM	VBUS Input Flag Indicates VBUS input signal on the USBHS side	R
31:24	—	These bits are read as 0. The write value should be 0.	R

29.2.50 DPUSR1R : Deep Software Standby USB Suspend/Resume Interrupt Register

Base address: USBHS = 0x4011_1000

Offset address: 0x164

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBSTSH	—	DOVCBH	DOVCAH	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	DVBSTSHE	—	DOVCBHE	DOVCAHE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	DOVCAHE	OVRCURA Interrupt Enable Clear 0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode	R/W
5	DOVCBHE	OVRCURB Interrupt Enable Clear 0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	DVBSTSHE	VBUS Interrupt Enable/Clear 0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode	R/W

29.2.49 DPUSR0R:DeepSoftwareStandbyUSBTransceiverControlPinMonitor Register

Base address: USBHS = 0x4011_1000

Offset address: 0x160

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBSTSHM	—	DOVCBHM	DOVCAHM	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
19:0	—	这些位被读取为0。写入值应为0。	R
20	DOVCAHM	OVRCURA输入标志 指示USBHS侧的OVRCURA输入信号	R
21	DOVCBHM	OVRCURB输入标志 指示USBHS侧的OVRCURB输入信号	R
22	—	该位读取为0。写入值应为0。	R
23	DVBSTSHM	VBUS输入标志 指示USBHS侧的VBUS输入信号	R
31:24	—	这些位被读取为0。写入值应为0。	R

29.2.50 DPUSR1R:深度软件待机USB暂停恢复中断寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x164

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	DVBSTSH	—	DOVCBH	DOVCAH	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	DVBSTSHE	—	DOVCBHE	DOVCAHE	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	DOVCAHE	OVRCURA中断使能清除 0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复	R/W
5	DOVCBHE	OVRCURB中断使能清除 0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	DVBSTSHE	VBUS Interrupt Enable/Clear 0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复	R/W

Bit	Symbol	Function	R/W
19:8	—	These bits are read as 0. The write value should be 0.	R/W
20	DOVCAH	OVRCURA Interrupt Source Return Status Flag 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode	R
21	DOVCBH	OVRCURB Interrupt Source Return Status Flag 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode	R
22	—	This bit is read as 0. The write value should be 0.	R/W
23	DVBSTSH	VBUS Interrupt Source Return Status Flag 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

29.2.51 DPUSR2R : Deep Software Standby USB Suspend/Resume Interrupt Register

Base address: USBHS = 0x4011_1000

Offset address: 0x168

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	DMINTE	DPINTE	—	—	DMVAL	DPVAL	—	—	DMINT	DPINT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DPINT	Indication of Return from DP Interrupt Source 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode	R
1	DMINT	Indication of Return from DM Interrupt Source 0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode	R
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	DPVAL	DP Input Indicates DP input signal on the USBHS side	R
5	DMVAL	DM Input Indicates DM input signal on the USBHS side	R
7:6	—	These bits are read as 0. The write value should be 0.	R/W
8	DPINTE	DP Interrupt Enable Clear 0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode	R/W
9	DMINTE	DM Interrupt Enable Clear 0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

29.2.52 DPUSRCR : Deep Software Standby USB Suspend/Resume Command Register

Base address: USBHS = 0x4011_1000

Offset address: 0x16A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIXPHYPD	FIXPHY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
19:8	—	这些位被读取为0。写入值应为0。	R/W
20	DOVCAH	OVRCURA中断源返回状态标志 0：系统未从深度软件待机模式恢复1：系统从深度软件待机模式恢复	R
21	DOVCBH	OVRCURB中断源返回状态标志 0：系统未从深度软件待机模式恢复1：系统从深度软件待机模式恢复	R
22	—	该位读取为0。写入值应为0。	R/W
23	DVBSTSH	VBUS中断源返回状态标志 0：系统未从深度软件待机模式恢复1：系统从深度软件待机模式恢复	R
31:24	—	这些位被读取为0。写入值应为0。	R/W

29.2.51 DPUSR2R:深度软件待机USB暂停恢复中断寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x168

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	DMINTE	DPINTE	—	—	DMVAL	DPVAL	—	—	DMINT	DPINT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DPINT	从DP中断源返回的指示 0：系统未从深度软件待机模式恢复1：系统从深度软件待机模式恢复	R
1	DMINT	从DM中断源返回的指示 0：系统未从深度软件待机模式恢复1：系统从深度软件待机模式恢复	R
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	DPVAL	DP Input 指示USBHS侧的DP输入信号	R
5	DMVAL	DM Input 指示USBHS侧的DM输入信号	R
7:6	—	这些位被读取为0。写入值应为0。	R/W
8	DPINTE	DP中断使能清除 0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复	R/W
9	DMINTE	DM中断使能清除 0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W

29.2.52 DPUSRCR:深度软件待机USB挂起恢复命令寄存器

Base address: USBHS = 0x4011_1000

Offset address: 0x16A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIXPHYPD	FIXPHY
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FIXPHY	USB Transceiver Control Fix 0: Normal mode 1: Invoke/recover from Deep Software Standby mode	R/W
1	FIXPHYPD	USB Transceiver Control Fix for PLL 0: Normal mode 1: Invoke/recover from Deep Software Standby mode	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W

29.3 Operation

29.3.1 System Control

This section describes register settings required for initializing the USBHS and controlling power consumption.

29.3.1.1 Setting data to the USBHS registers

Setting the SYSCFG.USBE bit to 1 after starting the PHY clock supply enables and starts USBHS operation. For information on how to supply the PHY clock, see section 29.3.3. Supplying the Clock.

29.3.1.2 Selecting the controller function

The USBHS can operate as a host or device controller.

Use the SYSCFG.DCFM bit to select one of these USBHS functions. The DCFM bit must be changed in the initial settings immediately after a reset or in the D+ pull-up-disabled state (SYSCFG.DPRPU bit = 0) and D+ and D- pulldown- disabled state (SYSCFG.DRPD bit = 0).

29.3.2 Controlling the USB data bus using resistorss

The USBHS provides pull-up and pull-down resistors for the D+ and D- lines. Pull these lines up or down by setting the SYSCFG.DPRPU and DRPD bits.

In device controller mode, confirm that connection to the USB host is made, and then set the SYSCFG.DPRPU bit to 1 and pull up the D+ line (in full-speed communication).

When the SYSCFG.DPRPU bit is set to 0 during communication with a PC, the USBHS disables the pull-up resistor for the USB data line, thereby notifying the USB host of disconnection.

Table 29.16 shows the settings for controlling the resistors for the USB data bus. Control the USB data bus appropriately for your system using the DRPD and DPRPU bit settings.

Table 29.16 Control settings for the USB data bus resistors (excluding OTG operation)

SYSCFG register settings		USB data bus control		
DRPD bit	DPRPU bit	D-Line	D+Line	Function
0	0	Open	Open	When resistors not used
0	1	Open	Pull-Up	When operating as a device controller at full-speed
1	0	Pull-Down	Pull-Down	When operating as a host controller
1	1	—	—	Setting prohibited except during OTG operation

29.3.3 Supplying the Clock

Table 29.17 shows the two input clocks required for the USBHS.

Bit	Symbol	Function	R/W
0	FIXPHY	USB收发器控制修复 0：正常模式1：调用从深度软件待机模式恢复	R/W
1	FIXPHYPD	用于PLL的USB收发器控制修复 0：正常模式1：调用从深度软件待机模式恢复	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W

29.3 Operation

29.3.1 系统控制

本节介绍初始化USBHS和控制功耗所需的寄存器设置。

29.3.1.1 将数据设置到USBHS寄存器

启动PHY时钟电源后将SYSCFG.USBE位设置为1使能并启动USBHS操作。有关如何提供PHY时钟的信息，请参阅第29.3.3节。提供时钟。

29.3.1.2 选择控制器功能

USBHS可以作为主机或设备控制器运行。

使用SYSCFG.DCFM位选择这些USBHS功能之一。DCFM位必须在复位后立即更改为初始设置或在D+上拉禁用状态（SYSCFG.DPRPU位=0）和D+和Dpulldown禁用状态（SYSCFG.DRPD位=0）。

29.3.2 使用电阻控制USB数据总线

USBHS为D+和Dlines提供上拉和下拉电阻。通过设置SYSCFG.DPRPU和DRPD位。

在设备控制器模式下，确认与USB主机的连接已建立，然后将SYSCFG.DPRPU位设置为1并拉高D+线（全速通信）。

当SYSCFG.DPRPU位在与PC通信期间设置为0时，USBHS禁用上拉电阻USB数据线，从而通知USB主机断开。

表29.16显示了用于控制USB数据总线电阻器的设置。使用DRPD和DPRPU位设置为您的系统适当控制USB数据总线。

Table 29.16 USB数据总线电阻的控制设置（不包括OTG操作）

SYSCFG寄存器设置		USB数据总线控制		
DRPD bit	DPRPU bit	D-Line	D+Line	Function
0	0	Open	Open	不使用电阻时
0	1	Open	Pull-Up	作为设备控制器全速运行时
1	0	Pull-Down	Pull-Down	作为主机控制器运行时
1	1	—	—	除OTG操作期间禁止设置

29.3.3 提供时钟

表29.17显示了USBHS所需的两个输入时钟。

Table 29.17 Input clocks

Input clock name	Description
PCLKA	Peripheral module clock A input. There is no constraint on the frequency of the PCLKA input.
PHY clock	PHY clock generated from external input or internal supply ● External input: The clock is generated by the USB-PHY internal PLL based on a 12-MHz, 20-MHz, or 24-MHz clock supplied to the EXTAL pin from outside the MCU. For the external clock specifications, especially the jitter characteristics, strictly follow the specifications of ±50 ppm. ● Internal supply: The clock is generated by supplying 48 MHz and 60 MHz to the USB-PHY module and selecting CL-only mode (PHYSET.HSEB). High-speed operation is not supported with this mode.

Figure 29.2 illustrates the PHY clock settings.

Table 29.17 输入时钟

输入时钟名称	Description
PCLKA	外设模块时钟A输入。 PCLKA输入的频率没有限制。
PHY clock	从外部输入或内部电源产生的PHY时钟● 时钟由USB-PHY内部PLL基于从MCU外部提供给EXTAL引脚的12-MHz、20-MHz或24-MHz时钟生成。 对于外部时钟规范，尤其是抖动特性，严格遵循±50ppm的规范。 ● Internal supply: 通过向USB-PHY模块提供48MHz和60MHz并选择CL-only模式(PHYSET.HSEB)来生成时钟。此模式不支持高速操作。

图29.2说明了PHY时钟设置。

RA生态工作室

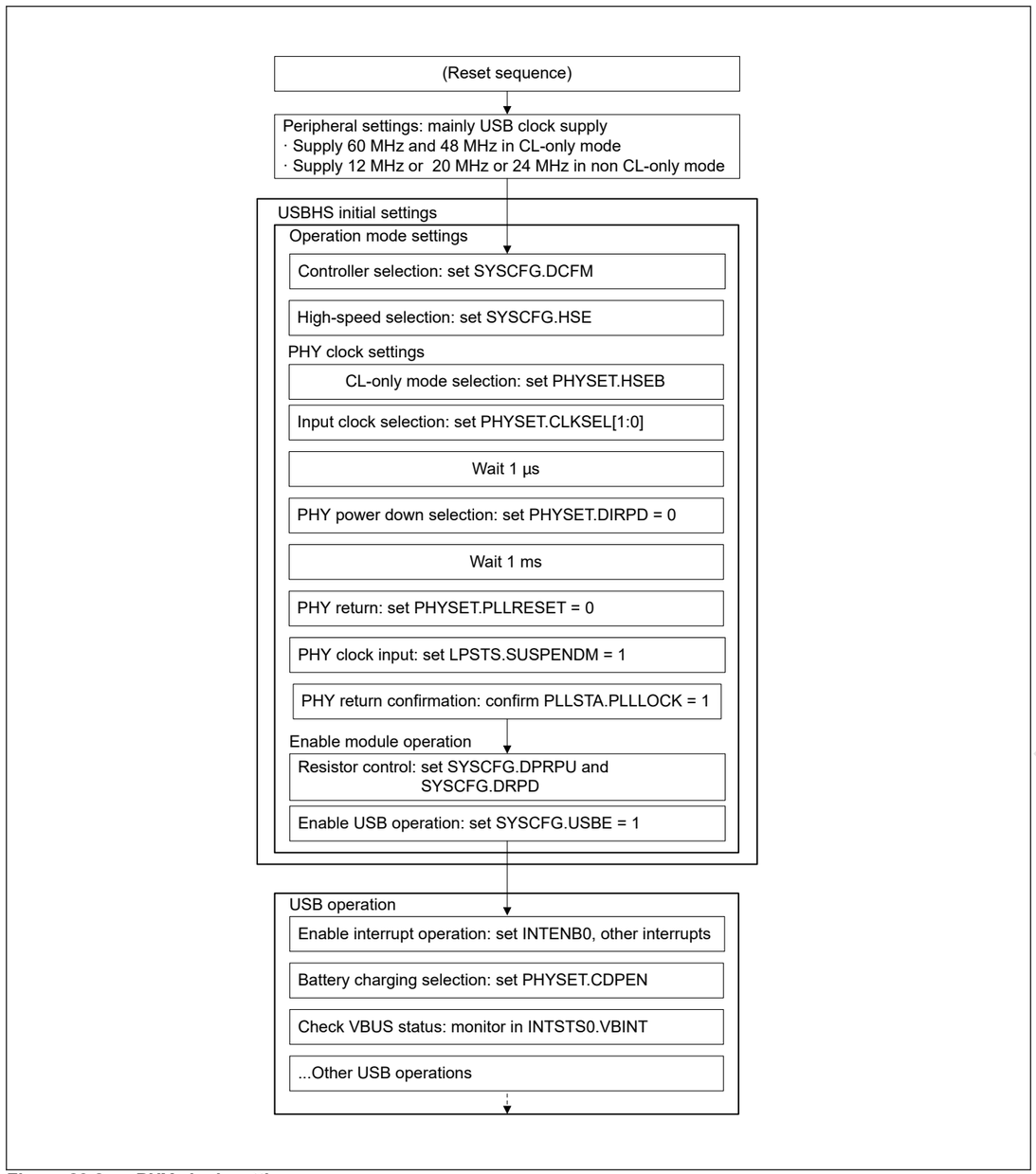

Figure 29.2 PHY clock settings

29.3.4 Constraints on Stopping the Clock

PCLKA and PHY clock can be stopped during disconnection or suspension. However, to stop any of these clocks while the USB is suspended in device controller mode, the stopped clock must be resupplied using the resume interrupt. The PHY clock must be resupplied within 5.5 ms after the resume interrupt is generated.

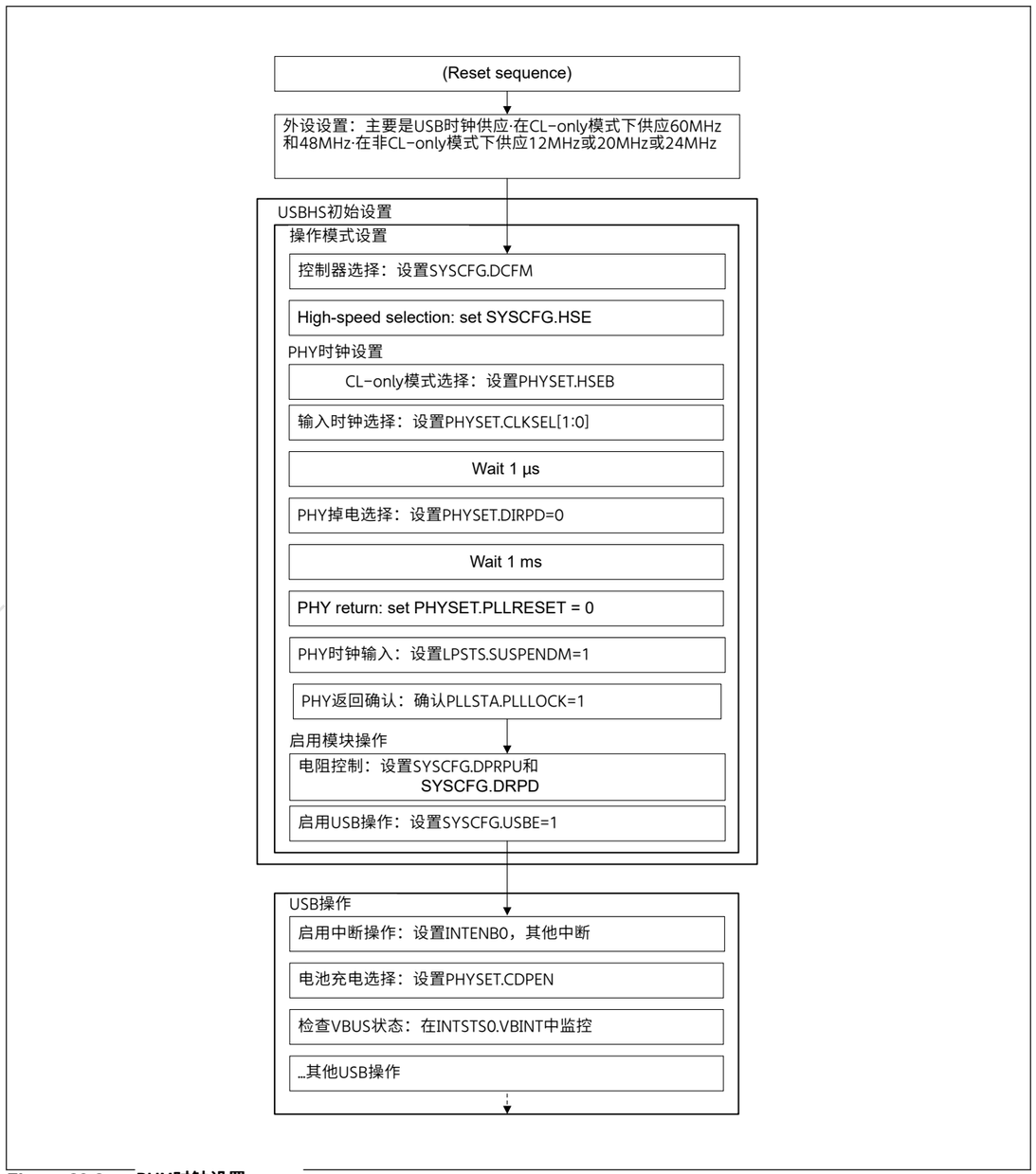

Figure 29.2 PHY时钟设置

29.3.4 停止时钟的限制

PCLKA和PHY时钟可以在断开或挂起期间停止。然而，要停止任何这些时钟，而USB在设备控制器模式下暂停，必须使用恢复中断重新提供停止的时钟。PHY时钟必须在产生恢复中断后的5.5 ms内重新提供。

29.3.5 Interrupts

Table 29.18 lists the interrupt sources in the USBHS. When an interrupt generation condition is satisfied and the interrupt output is enabled using the associated interrupt enable register, the USBHS issues a USBHS interrupt request to the Interrupt Controller Unit (ICU) and a USBHS interrupt is generated.

Table 29.18 Interrupt sources (1 of 2)

Flag to be set to 1	Interrupt name	Interrupt source	Applicable controller function	Status flag
VBINT	VBUS interrupt	• A change in the state of the USB_VBUS input pin is detected (low to high or high to low)	Host or function*1	INTSTS0.VBSTS
RESM	Resume interrupt	• A change in the state of the USB bus is detected in the Suspend state (J-state to K-state or J-state to SE0)	Function	—
SOFR	Frame number update interrupt	In host controller mode: • An SOF packet with a different frame number is transmitted In device controller mode: • When SOFRM is 0: An SOF packet with a different frame number is received • When SOFRM is 1: Failed to receive an SOF packet with the µ frame number 0 because the packet is corrupted.	Host or function	—
DVST	Device state transition interrupt	• A device state transition is detected because of one of the following: – USB bus reset is detected – Suspend state is detected – SET_ADDRESS request is received – SET_CONFIGURATION request is received.	Function	PL1CTRL.DVSQ[3:0]
CTRT	Control transfer stage transition interrupt	• A control transfer stage transition is detected because of one of the following: – Setup stage completed – Control write transfer status stage transition occurred – Control read transfer status stage transition occurred – Control transfer completed – Control transfer sequence error occurred	Function	INTSTS0.CTSQ[2:0]
BEMP	Buffer empty interrupt	• The buffer is empty after all FIFO buffer data is transmitted • A packet larger than the maximum packet size is received	Host or function	BEMPSTS.PIPEBEMP
NRDY	Buffer not ready interrupt	In host controller mode: • A STALL response is received from the peripheral device in response to the issued token • The response from the peripheral device in response to the issued token is not received successfully (no response three times consecutively or packet reception error three times consecutively) • An overrun or underrun error occurred during isochronous transfer In device controller mode: • NAK is returned for an IN or OUT token while the PID[1:0] bits were set to 01b (BUF) • A CRC error or bit stuffing error occurred during data reception in isochronous transfer • An interval error occurred during data reception in isochronous transfer	Host or function	NRDYSTS.PIPENRDY
BRDY	Buffer ready interrupt	• The buffer is ready (read or write state)	Host or function	BRDYSTS.PIPEBRDY
OVRCR	Overcurrent input change interrupt	• USBHS_OVRCR0A pin or USBHS_OVRCR0B pin state change is detected (low to high or high to low)	Host or function	SYSSTS0.OVCMON[1:0]

29.3.5 Interrupts

表29.18列出了USBHS中的中断源。当满足中断产生条件并使用相关的中断使能寄存器使能中断输出时，USBHS向中断控制器单元(ICU)发出USBHS中断请求，并产生USBHS中断。

Table 29.18 中断源(1of2)

标志设置为1	中断名称	中断源	适用控制器功能	状态标志
VBINT	VBUS interrupt	• 检测到USB_VBUS输入引脚的状态变化（从低到高或从高到低）	主机或功能*1	INTSTS0.VBSTS
RESM	恢复中断	• 在USB总线的状态变化被检测到挂起状态（J状态到K状态或J状态到SE0）	Function	—
SOFR	帧号更新中断	在主机控制器模式下： 发送不同帧号的SOF数据包在设备控制器模式下：● 当SOFRM为0时：接收到不同帧号的SOF包 • 当SOFRM为1时：由于包损坏，无法接收到µ帧号为0的SOF包。	主机或功能	—
DVST	设备状态转换中断	• 由于以下原因之一检测到设备状态转换： – 检测到USB总线复位 – 检测到挂起状态 – 收到SET_ADDRESS请求 – 收到SET_CONFIGURATION请求。	Function	PL1CTRL.DVSQ[3:0]
CTRT	控制转移阶段转换中断	• 由于以下原因之一检测到控制转移阶段转换： – 设置阶段完成 – 发生控制写传输状态阶段转换 – 发生控制读取传输状态阶段转换 – 控制转移完成 – 发生控制传输序列错误	Function	INTSTS0.CTSQ[2:0]
BEMP	缓冲区空中断	• 传输完所有FIFO缓冲区数据后缓冲区为空 • 接收到大于最大数据包大小的数据包	主机或功能	BEMPSTS.PIPEBEMP
NRDY	缓冲区未就绪中断	在主机控制器模式下： ● 从外围设备接收到STALL响应以响应颁发的令牌 • 外围设备对下发令牌的响应未成功接收（连续3次无响应或连续3次报文接收错误） ●同步传输期间发生溢出或欠载错误在设备控制器模式下：● NAK返回一个IN或OUT令牌，而PID[1:0]位设置为01b(BUF) • 同步传输中的数据接收过程中发生CRC错误或位填充错误 • 同步传输中的数据接收期间发生间隔错误	主机或功能	NRDYSTS.PIPENRDY
BRDY	缓冲区就绪中断	• 缓冲区就绪（读或写状态）	主机或功能	BRDYSTS.PIPEBRDY
OVRCR	过流输入变化中断	• 检测到USBHS_OVRCR0A引脚或USBHS_OVRCR0B引脚状态变化（低到高或高到低）	主机或功能	SYSSTS0.OVCMON[1:0]

Table 29.18 Interrupt sources (2 of 2)

Flag to be set to 1	Interrupt name	Interrupt source	Applicable controller function	Status flag
BCHG	Bus change interrupt	• USB bus state change is detected	Host	—
DTCH	Device disconnect detection interrupt	• Peripheral device disconnect is detected	Host	—
ATTCH	Device connect detection interrupt	• J-state or K-state is detected on the USB bus for 2.5 µs continuously This interrupt can be used to check whether peripheral devices are connected.	Host	—
EOFERR	EOF error detection interrupt	• An EOF error is detected for a peripheral device	Host	—
SACK	Setup normal interrupt	• A setup transaction normal response (ACK) is received	Host	—
SIGN	Setup error interrupt	• A setup transaction error (no response or ACK packet corruption) is detected three consecutive times	Host	—
PDDETINT	PDDETSTS change detect interrupt	• PDDET pin change is detected	Host or function	BCCTRL.PDDETSTS
LPMEND	LPM transaction end interrupt	• LPM transaction is complete	Host	PL1CTRL.DVSQ[3:0]
L1RSMEND	L1 resume end interrupt	• Resume (from L1 state) processing is complete	Host	PL1CTRL.DVSQ[3:0]

Note 1. Although this interrupt can be generated in host controller mode, it is not usually used in this mode.

29.3.5.1 Selecting the USBHS interrupt detection method

Table 29.19 shows operations for an USBHS interrupt output from the USBHS. In case two or more interrupt sources are generated, the USBHS interrupt output method can be set in the SOFCFG.INTL bit. Set the USBHS interrupt output operation based on your system.

Table 29.19 USBHS interrupt operation

USBHS interrupt output (INTL setting)	When one interrupt source is generated	When two or more interrupt sources are generated
Edge detection (SOFCFG.INTL bit = 0)	Low level output until the source is cleared	When one source is cleared, the USBHS interrupt is negated for 32 clocks at 48 MHz (high pulse output)
Level detection (SOFCFG.INTL bit = 1)	Low level output until the source is cleared	Low level output until all sources are cleared

Table 29.18 中断源（2个中的2个）

标志设置为1	中断名称	中断源	适用控制器功能	状态标志
BCHG	总线变化中断	• 检测到USB总线状态变化	Host	—
DTCH	设备断开检测中断	• 检测到外围设备断开连接	Host	—
ATTCH	设备连接检测中断	• 在USB总线上连续检测到J-state或K-state2.5µs此中断可用于检查外围设备是否连接。	Host	—
EOFERR	EOF错误检测中断	• 检测到外围设备的EOF错误	Host	—
SACK	设置正常中断	• 接收到设置事务正常响应(ACK)	Host	—
SIGN	设置错误中断	• 连续3次检测到设置事务错误（无响应或ACK数据包损坏）	Host	—
PDDETINT	PDDETSTS变化检测中断	• 检测到PDDET引脚变化	主机或功能	BCCTRL.PDDETSTS
LPMEND	LPM事务结束中断	• LPM交易完成	Host	PL1CTRL.DVSQ[3:0]
L1RSMEND	L1恢复结束中断	• 恢复（从L1状态）处理完成	Host	PL1CTRL.DVSQ[3:0]

注1.虽然该中断可以在主机控制器模式下产生，但通常不用于该模式。

29.3.5.1 选择USBHS中断检测方法

表29.19显示了来自USBHS的USBHS中断输出的操作。如果产生两个或更多中断源，USBHS中断输出方法可以在SOFCFG.INTL位中设置。根据您的系统设置USBHS中断输出操作。

Table 29.19 USBHS中断操作

USBHS中断输出（INTL设置）	产生一个中断源时	当产生两个或更多中断源时
边沿检测（SOFCFG.INTL位=0）	低电平输出，直到源清除	当一个源被清除时，USBHS中断在48MHz的32个时钟内被否定（高脉冲输出）
电平检测（SOFCFG.INTL位=1）	低电平输出，直到源清除	低电平输出，直到所有源被清除

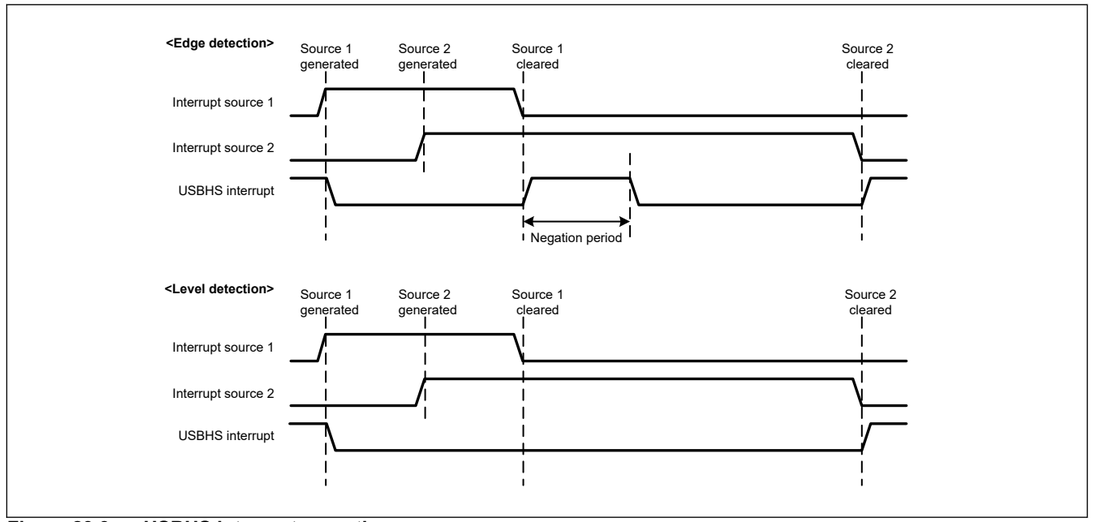

Figure 29.3 USBHS interrupt operation

Figure 29.4 shows an interrupt association chart of the USBHS.

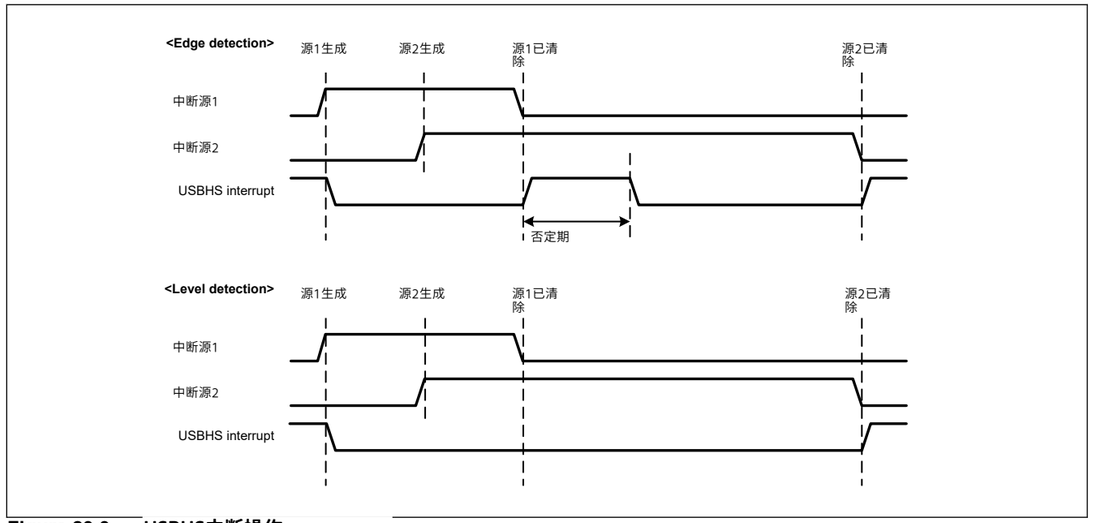

Figure 29.3 USBHS中断操作

图29.4显示了USBHS的中断关联图。

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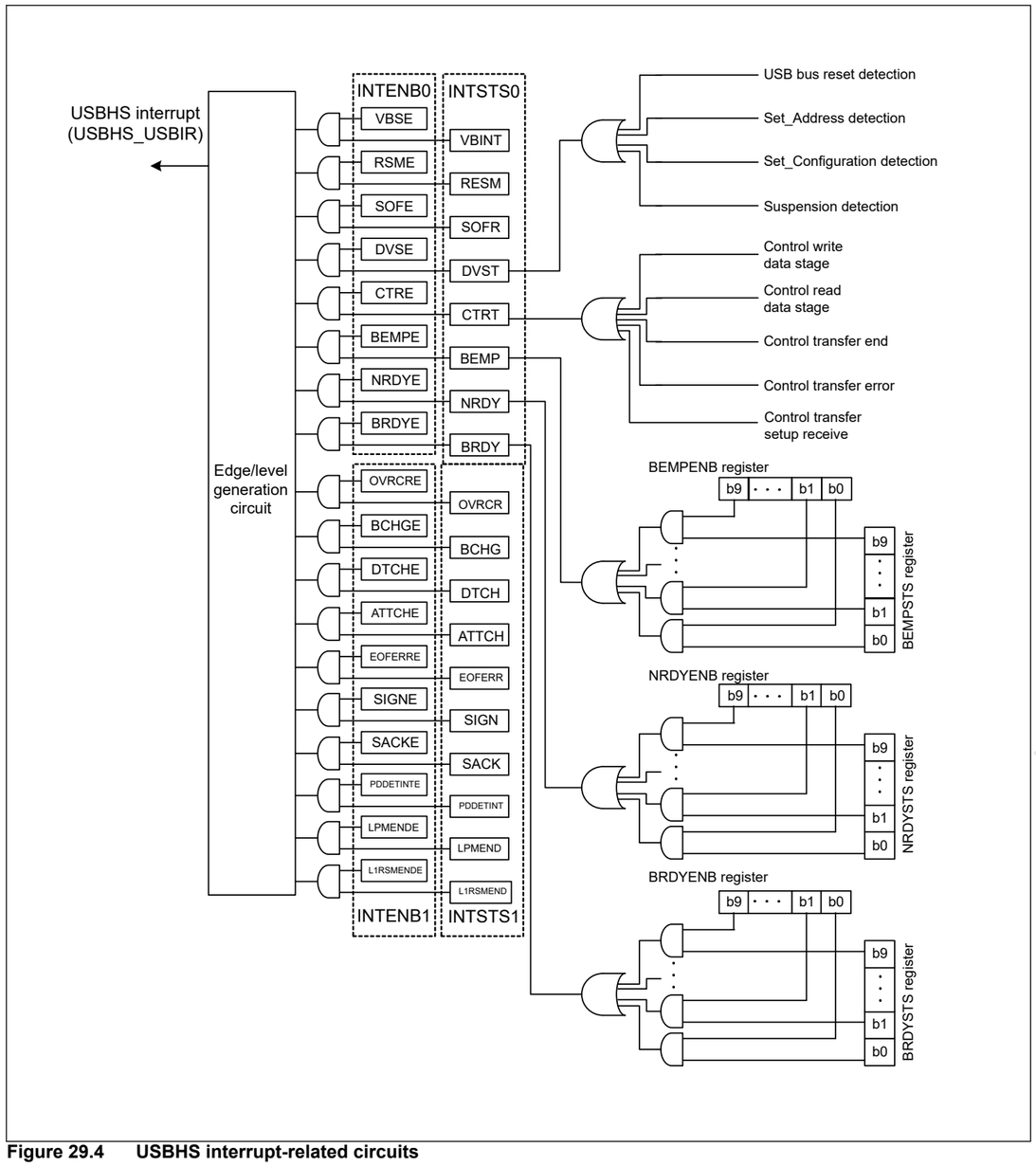

Figure 29.4 USBHS interrupt-related circuits

Table 29.20 shows the interrupts generated by the USBHS.

Table 29.20 USBHS interrupts (1 of 2)

Interrupt name	Interrupt status flag	DTC activation	DMAC activation
USBHS_D0FIFO	DMA transfer request 0	Possible	Possible
USBHS_D1FIFO	DMA transfer request 1	Possible	Possible

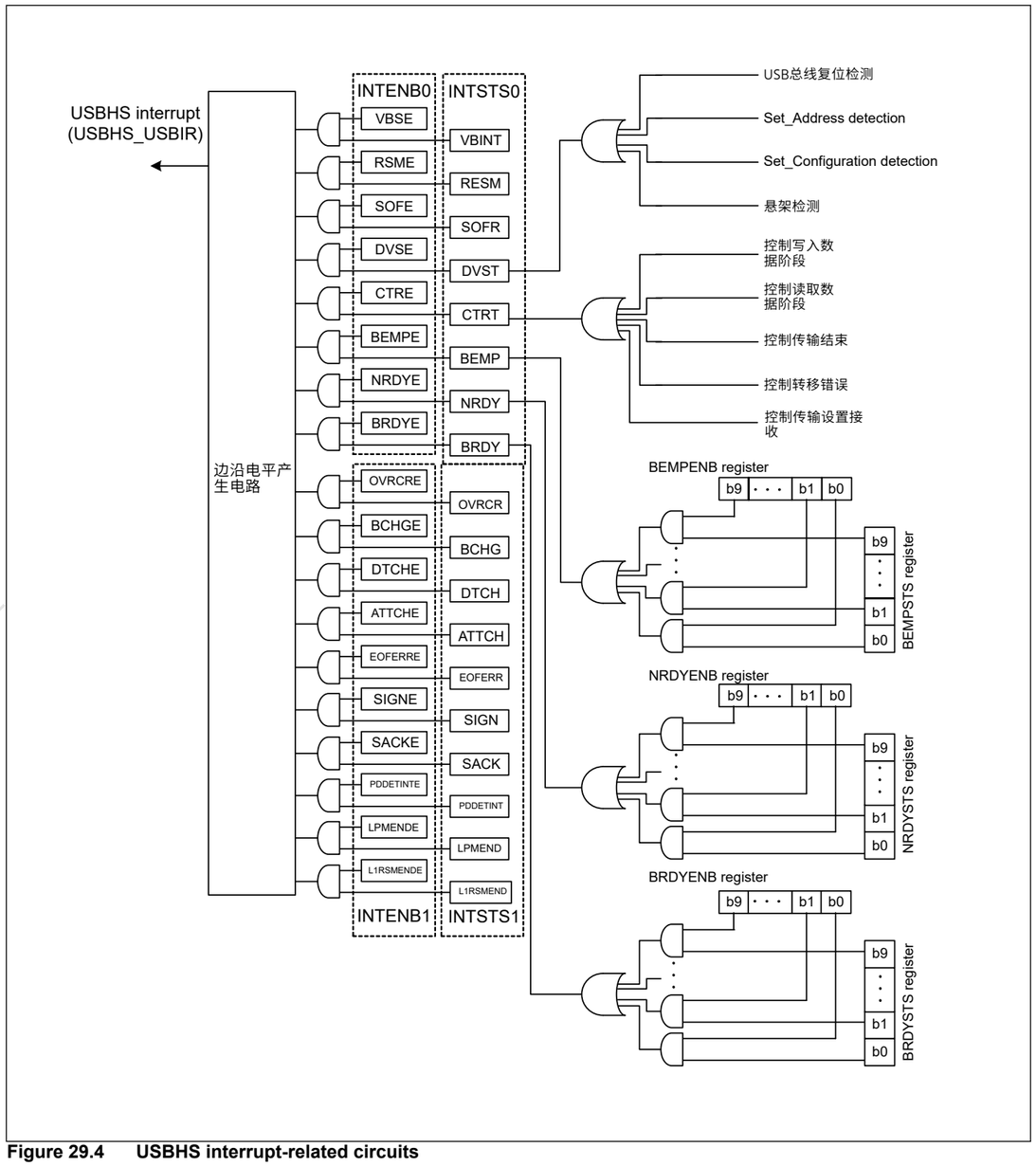

Figure 29.4 USBHS interrupt-related circuits

表29.20显示了USBHS产生的中断。

Table 29.20 USBHS中断(1of2)

中断名称	中断状态标志	DTC activation	DMAC activation
USBHS_D0FIFO	DMA传输请求0	Possible	Possible
USBHS_D1FIFO	DMA传输请求1	Possible	Possible

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Table 29.20 USBHS interrupts (2 of 2)

Interrupt name	Interrupt status flag	DTC activation	DMAC activation
USBHS_USBIR	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent interrupt, bus change interrupt, device disconnect detection interrupt, device connect detection interrupt, EOF error detection interrupt, normal setup operation interrupt, setup error interrupt, PDDETSTS change detection interrupt, LPM transaction end interrupt, and L1 resume end interrupt	Not possible	Not possible

29.3.6 Interrupt Descriptions

29.3.6.1 BRDY interrupt

The BRDY interrupt is generated in both host and device controller modes. This section describes the conditions in which the USBHS sets the associated bit in BRDYSTS to 1. Under these conditions, the USBHS generates a BRDY interrupt if the software sets the bit in BRDYENB associated with the given pipe to 1 and INTENB0.BRDYE bit to 1.

The conditions for generating and clearing the BRDY interrupt depend on the SOFCFG.BRDYM and PIPECFG.BFRE settings for each pipe as follows:

(1) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.

On any of the following conditions, the USBHS generates an internal BRDY interrupt request trigger and sets the BRDYSTS.PIPEBRDY flag associated with the pipe to 1.

For transmitting pipes

- When the DIR bit is changed from 0 to 1 by software
- When writing by the CPU to the FIFO buffer is disabled for a pipe (when the BSTS flag is read as 0) and the USBHS has completed packet transmission. In continuous transfer, a BRDY interrupt is generated on completion of the transmission of data from one FIFO buffer.
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is complete
- When the hardware flushes the buffer of the pipe for isochronous transfers
- When 1 is written to the PIPEnCTR.ACLRM bit, which causes the FIFO buffer to transition from the write-disabled to write-enabled state.

No request trigger is generated for the DCP, that is, during data transmission for control transfers.

For receiving pipes

- When packet reception is successfully complete, enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the given pipe is disabled (when the BSTS flag is read as 0). No request trigger is generated for transactions in which DATA-PID mismatch has occurred. In continuous transmission or reception mode, the request trigger is not generated when the data is of the specified maximum packet size and the buffer has available space. When a short packet is received, the request trigger is generated even if the FIFO buffer has available space. When the transaction counter is used, the request trigger is generated on receiving the specified number of packets. In this case, the request trigger is generated even if the FIFO buffer has available space.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode. No request trigger is generated until completion of reading data from the currently-read FIFO buffer, even if reception by the other FIFO buffer is complete.
  In device controller mode, the BRDY interrupt is not generated in the status stage of control transfers. The PIPEBRDY interrupt status of the selected pipe can be set to 0 by writing 0 to the associated PIPEBRDY flag through the software. In this case, 1s must be written to the associated bits for the other pipes. Clear the BRDY status before accessing the FIFO buffer.

Table 29.20 USBHS中断(2of2)

中断名称	中断状态标志	DTC activation	DMAC activation
USBHS_USBIR	VBUS中断、恢复中断、帧号更新中断、设备状态转换中断、控制传输阶段转换中断、缓冲区空中断、缓冲区未就绪中断、缓冲区就绪中断、过流中断、总线改变中断、设备断开检测中断、设备连接检测中断、EOF错误检测中断、正常设置操作中断、设置错误中断、PDDETSTS更改检测中断、LPM事务结束中断和L1恢复结束中断	不可能	不可能

29.3.6 中断说明

29.3.6.1 BRDY interrupt

在主机和设备控制器模式下都会产生BRDY中断。本节描述USBHS将BRDYSTS中的相关位设置为1的条件。在这些条件下，如果软件将与给定管道相关的BRDYENB中的位设置为1，并且将INTENB0.BRDYE位设置为1，USBHS将生成BRDY中断.

产生和清除BRDY中断的条件取决于每个管道的SOFCFG.BRDYM和PIPECFG.BFRE设置，如下所示：

(1) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=0时

通过这些设置，BRDY中断指示FIFO端口可访问。

在以下任何一种情况下，USBHS产生一个内部BRDY中断请求触发并设置与管道关联的BRDYSTS.PIPEBRDY标志为1。

用于传输管道

●DIR位由软件从0变为1时

●当CPU对FIFO缓冲区的写操作禁止管道时（当BSTS标志读为0时）且USBHS已完成数据包传输。在连续传输中，一个FIFO缓冲区的数据传输完成时会产生一个BRDY中断。

●双缓冲模式下，当一个FIFO缓冲区完成向另一个FIFO缓冲区写入数据时为空时

●直到向当前写入的FIFO缓冲区写入数据完成，才会产生请求触发，即使传输到另一个FIFO缓冲区已完成

●当硬件刷新管道缓冲区以进行同步传输时

●当PIPEnCTR.ACLRM位写入1时，会导致FIFO缓冲区从写禁止状态转变为写使能状态。

没有为DCP生成请求触发，即在控制传输的数据传输期间。

用于接收管道

●当数据包接收成功完成时，允许读取FIFO缓冲区，同时禁止从CPU对给定管道的FIFO缓冲区的读取访问（当BSTS标志被读取为0时）。对于发生DATA-PID不匹配的事务，不会生成请求触发器。在连续发送或接收模式下，当数据达到指定的最大数据包大小且缓冲区有可用空间时，不会生成请求触发。当接收到一个短数据包时，即使FIFO缓冲区有可用空间，也会生成请求触发。当使用事务计数器时，在接收到指定数量的数据包时生成请求触发器。在这种情况下，即使FIFO缓冲区有可用空间，也会生成请求触发。

●当一个FIFO缓冲区在双缓冲区模式下从另一个FIFO缓冲区读取数据完成后使能读取。在从当前读取的FIFO缓冲区读取数据完成之前，不会生成请求触发，即使其他FIFO缓冲区的接收已完成。在设备控制器模式下，在控制传输的状态阶段不会产生BRDY中断。通过软件将0写入相关的PIPEBRDY标志，可以将所选管道的PIPEBRDY中断状态设置为0。在这种情况下，必须将1写入其他管道的相关位。在访问之前清除BRDY状态

FIFO buffer.

(2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1

With these settings, the USBHS generates a BRDY interrupt on completion of reading all data for a single transfer using the receiving pipe, and sets the bit in BRDYSTS associated with the pipe to 1.

On any of the following conditions, the USBHS determines that the last data for a single transfer was received:

- When a short packet including a zero-length packet is received
- When the PIPEnTRN register is used and the number of packets specified in the PIPEnTRN.TRNCNT[15:0] bits are completely received

When the data is completely read after any of these conditions is satisfied, the USBHS determines that all data for a single transfer is completely read.

When a zero-length packet is received while the FIFO buffer is empty, the USBHS determines that all data for a single transfer is completely read when the FRDY flag in the FIFO port control register is 1 and the DTLN[11:0] flags are 0. In this case, to start the next transfer, write 1 to the BCLR bit in the associated port control register through software. With these settings, the USBHS does not detect a BRDY interrupt for the transmitting pipe.

The PIPEBRDY interrupt status of a pipe can be set to 0 by writing 0 to the associated BRDYSTS.PIPEBRDY flag through the software. In this case, 1s must be written to the PIPEBRDY bits for the other pipes.

In this mode, do not change the PIPECFG.BFRE bit setting until all data for a single transfer is processed. When it is necessary to change the PIPECFG.BFRE bit before completion of processing, all FIFO buffers for the pipe must be cleared using the PIPEnCTR.ACLRM bit.

(3) When SOFCFG.BRDYM = 1 and PIPECFG.BFRE = 0

With these settings, the BRDYSTS.PIPEBRDY flag values are linked to the BSTS flag setting for each pipe. In other words, the BRDY interrupt status bits are set to 1 or 0 by the USBHS depending on the FIFO buffer status.

For transmitting pipes

The BRDY interrupt status bits are set to 1 when the FIFO port is ready for write access, and are set to 0 when it is not ready. The BRDY interrupt is not generated for the DCP in the transmitting direction even when it is ready for write access.

For receiving pipes

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for read access, and are set to 0 when all data is read (not ready for read access).

When a zero-length packet is received while the FIFO buffer is empty, the associated bit is set to 1 and the BRDY interrupt is continuously generated until the software writes 1 to BCLR. With this setting, the PIPEBRDY flag cannot be set to 0 by software.

When the SOFCFG.BRDYM bit is set to 1, set the PIPECFG.BFRE bit for all pipes to 0, and the SOFCFG.INTL bit to 1 for level detection.

Figure 29.5 shows the timing of BRDY interrupt generation.

(2) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=1时

使用这些设置，USBHS在完成使用接收管道读取一次传输的所有数据时生成BRDY中断，并将BRDYSTS中与管道相关的位设置为1。

在以下任何一种情况下，USBHS都会确定接收到单次传输的最后一个数据：

- 收到包含零长度包的短包时
- 当使用PIPEnTRN寄存器并且PIPEnTRN.TRNCNT[15:0]位中指定的数据包数量被完全接收时

当满足这些条件中的任何一个后数据被完全读取时，USBHS确定单次传输的所有数据都被完全读取。

当FIFO缓冲区为空时接收到零长度数据包时，当FIFO端口控制寄存器中的FRDY标志为1且DTLN[11:0]标志为0.在这种情况下，要开始下一次传输，通过软件向相关端口控制寄存器中的BCLR位写入1。使用这些设置，USBHS不会检测到传输管道的BRDY中断。

通过软件将0写入相关的BRDYSTS.PIPEBRDY标志可以将管道的PIPEBRDY中断状态设置为0。在这种情况下，必须将1写入其他管道的PIPEBRDY位。

在此模式下，在处理完单次传输的所有数据之前，不要更改PIPECFG.BFRE位设置。当需要在处理完成之前更改PIPECFG.BFRE位时，必须使用PIPEnCTR.ACLRM位清除管道的所有FIFO缓冲区。

(3) 当SOFCFG.BRDYM=1且PIPECFG.BFRE=0时

通过这些设置，BRDYSTS.PIPEBRDY标志值链接到每个管道的BSTS标志设置。换言之，BRDY中断状态位由USBHS设置为1或0，具体取决于FIFO缓冲区状态。

用于传输管道

当FIFO端口准备好进行写访问时，BRDY中断状态位设置为1，当它未准备好时设置为0。发送方向上的DCP不会产生BRDY中断，即使它已准备好进行写访问。

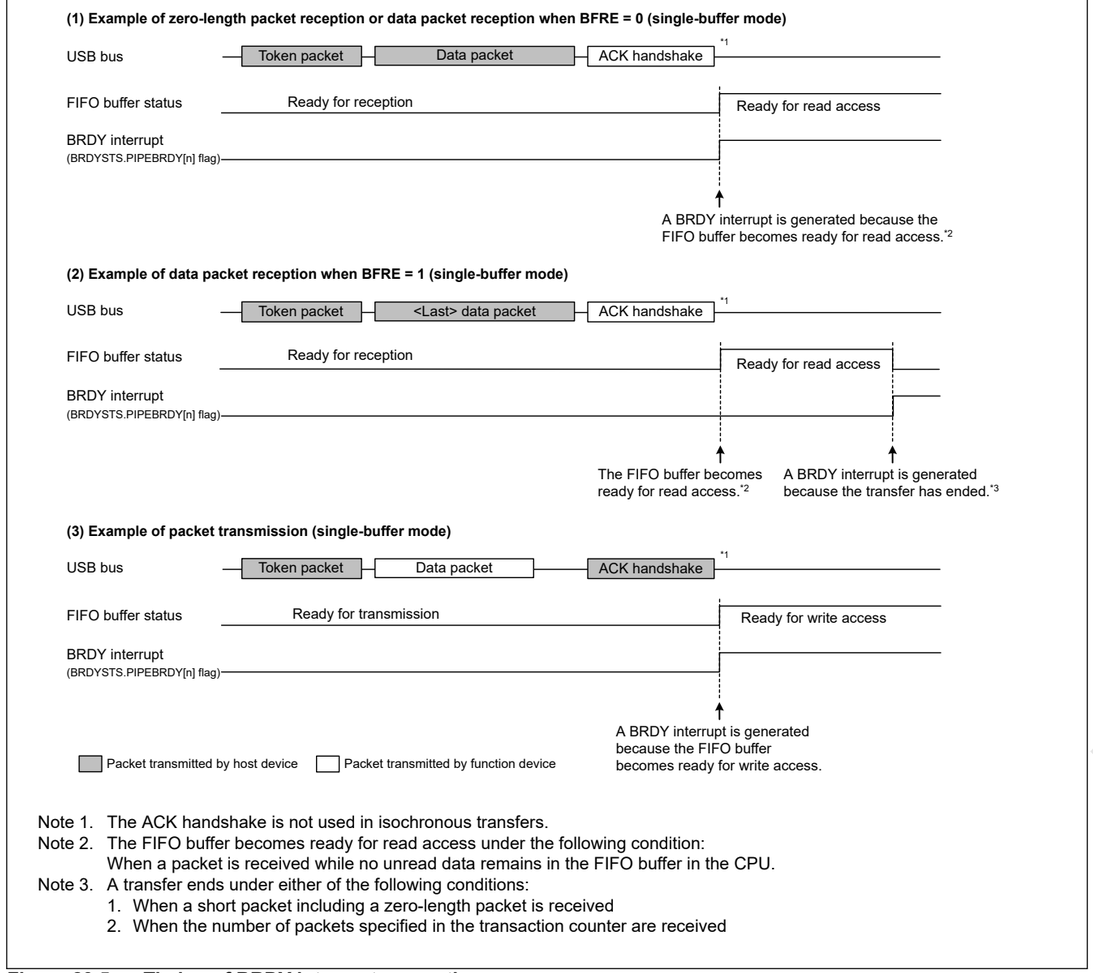
用于接收管道

当FIFO缓冲区准备好进行读取访问时，BRDY中断状态位设置为1，当读取所有数据（未准备好进行读取访问）时设置为0。

当FIFO缓冲区为空时接收到零长度数据包时，相关位设置为1，并且持续产生BRDY中断，直到软件将1写入BCLR。使用此设置，PIPEBRDY标志不能由软件设置为0。

当SOFCFG.BRDYM位设置为1时，将所有管道的PIPECFG.BFRE位设置为0，并将SOFCFG.INTL位设置为1以进行电平检测。

图29.5显示了BRDY中断产生的时序。



Note 1. The ACK handshake is not used in isochronous transfers.
Note 2. The FIFO buffer becomes ready for read access under the following condition:
When a packet is received while no unread data remains in the FIFO buffer in the CPU.
Note 3. A transfer ends under either of the following conditions:
1. When a short packet including a zero-length packet is received
2. When the number of packets specified in the transaction counter are received

Figure 29.5 Timing of BRDY interrupt generation

The condition for clearing the INTSTS0.BRDY flag depends on the SOFCFG.BRDYM bit setting value, as shown in Table 29.21

Table 29.21 Conditions for clearing the BRDY flag

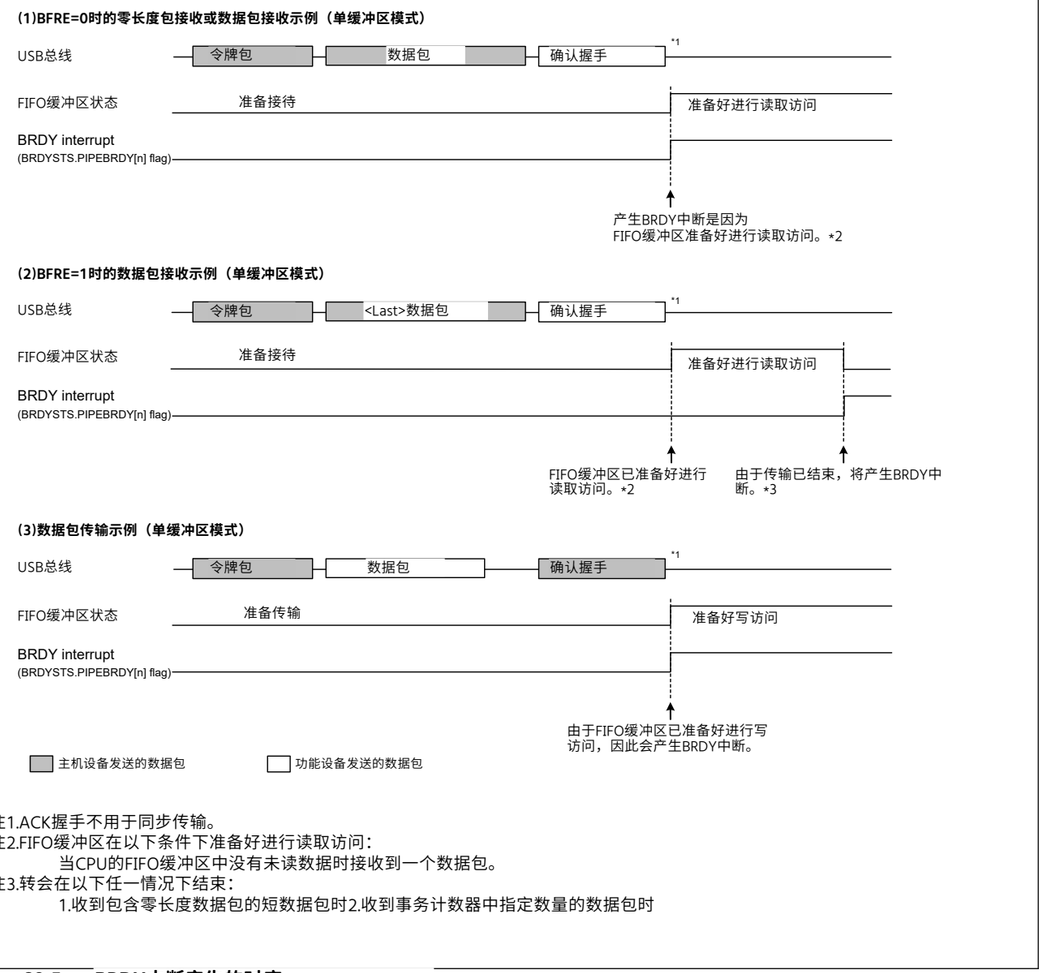
BRDYM bit	Condition for clearing BRDY flag
0	The USBHS clears the BRDY flag to 0 when all bits in BRDYSTS are set to 0 by software
1	The USBHS clears the BRDY flag to 0 when the BSTS flags for all pipes have cleared to 0

29.3.6.2 NRDY interrupt

On generating an internal NRDY interrupt request for the pipe whose PID[1:0] bits are set to 01b (BUF response) by software, the USBHS sets the associated NRDYSTS.PIPENRDY flag to 1. If the associated bit in NRDYENB is set to 1 by software, the USBHS sets the INTSTS0.NRDY flag to 1 and generates a USBHS interrupt.

This section describes the conditions in which the USBHS generates the internal NRDY interrupt request for a given pipe.

The internal NRDY interrupt request is not generated during setup transaction execution in host controller mode. During setup transactions in host controller mode, the SACK or SIGN interrupt is detected.



注1.ACK握手不用于同步传输。
注2.FIFO缓冲区在以下条件下准备好进行读取访问：
当CPU的FIFO缓冲区中没有未读数据时接收到一个数据包。
注3.转会在以下任一情况下结束：
1.收到包含零长度数据包的短数据包时2.收到事务计数器中指定数量的数据包时

Figure 29.5 BRDY中断产生的时序

INTSTS0.BRDY标志清零的条件取决于SOFCFG.BRDYM位设置值，如表29.21所示

Table 29.21 清除BRDY标志的条件

BRDYM位	清除BRDY标志的条件
0	当软件将BRDYSTS中的所有位设置为0时，USBHS将BRDY标志清零
1	当所有管道的BSTS标志清除为0时，USBHS将BRDY标志清除为0

29.3.6.2 NRDY interrupt

在为PID[1:0]位由软件设置为01b（BUF响应）的管道生成内部NRDY中断请求时，USBHS将相关的NRDYSTS.PIPENRDY标志设置为1。如果NRDYENB中的相关位设置为通过软件置1，USBHS将INTSTS0.NRDY标志设置为1并产生USBHS中断。

本节描述USBHS为给定管道生成内部NRDY中断请求的条件。

内部NRDY中断请求在主控制器模式下的设置事务执行期间不会产生。在主机控制器模式下的设置事务期间，检测到SACK或SIGN中断。

The internal NRDY interrupt request is not generated during status stage execution of the control transfer in device controller mode

(1) In host controller mode when no split transactions occur in the connection

For transmitting pipes

On any of the following conditions, the USBHS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBHS transmits a zero-length packet following the OUT token and sets the associated NRDYSTS.PIPENRDY flag and the FRMNUM.OVRN flag to 1.
- During communications other than setup transactions on pipes not used for isochronous transfers, when any combination of the following two conditions occurs three consecutive times:
  - No response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device
  - An error is detected in the packet from the peripheral device. In this case, the USBHS sets the associated PIPENRDY flag to 1 and changes the PID[1:0] setting for the associated pipe to 00b (NAK response)
- During communications other than setup transactions, when the STALL handshake is received from the peripheral device (includes STALL for both OUT and PING). In this case, the USBHS sets the associated PIPENRDY flag to 1 and changes the PID[1:0] setting for the associated pipe to 11b (STALL response).

For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBHS discards the received data for the IN token and sets the associated PIPENRDY flag and the OVRN flag to 1. When a packet error is detected in the received data for the IN token, the USBHS also sets the FRMNUM.CRCE flag to 1.
- For non-isochronous transfer pipes, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device for the IN token issued by the USBHS (when timeout is detected before detection of the DATA packet from the peripheral device)
  - An error is detected in the packet from the peripheral device. In this case, the USBHS sets the associated PIPENRDY flag to 1 and changes the associated PID[1:0] setting for the pipe to 00b (NAK response).
- For isochronous transfer pipes, when no response is returned from the peripheral device for the IN token (when timeout is detected before detection of the DATA packet from the peripheral device) or an error is detected in the packet from the peripheral device. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe to 1. The PID[1:0] setting for the pipe is not changed.
- For isochronous transfer pipes, when a CRC error or a bit stuffing error is detected in the received data packet. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe and the CRCE flag to 1.
- When the STALL handshake is received. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe to 1 and changes the PID[1:0] setting for the associated pipe to STALL.

(2) In host controller mode when split transactions occur in the connection

For transmitting pipes

On any of the following conditions, the USBHS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBHS sets the associated RDYSTS.PIPENRDY flag for the given pipes to 1 on issuing a start-split transaction and sets the FRMNUM.OVRN flag to 1. The USBHS also transmits a zero-length packet following the OUT token.
- For non-isochronous transfer pipes, when any combination of the following two cases occurs three consecutive times:
  - No response is returned from the hub for start-split and complete-split transactions (when timeout is detected before detection of the handshake packet from the hub)

在设备控制器模式下控制传输的状态阶段执行期间不产生内部NRDY中断请求

(1) 在主机控制器模式下，连接中没有发生拆分事务

用于传输管道

在以下任何一种情况下，USBHS都会检测到NRDY中断：

●对于同步传输管道，当FIFO缓冲区中没有要传输的数据时发出OUT令牌的时间到来。在这种情况下，USBHS在OUT令牌之后发送一个长度为零的数据包，并将相关的NRDYSTS.PIPENRDY标志和FRMNUM.OVRN标志设置为1。

●在不用于同步传输的管道上的设置事务以外的通信期间，当以下两种情况的任意组合连续发生3次时：

外围设备没有返回响应（当在检测到来自外围设备的握手包之前检测到超时时

在来自外围设备的数据包中检测到错误。在这种情况下，USBHS将关联的PIPENRDY标志设置为1，并将关联管道的PID[1:0]设置更改为00b（NAK响应）

●在设置事务以外的通信期间，当从外围设备接收到STALL握手时（包括OUT和PING的STALL）。在这种情况下，USBHS将关联的PIPENRDY标志设置为1，并将关联管道的PID[1:0]设置更改为11b（STALL响应）。

用于接收管道

●对于同步传输管道，当发出IN令牌的时间到来但FIFO中没有可用空间时
缓冲。在这种情况下，USBHS丢弃IN令牌的接收数据并将相关的PIPENRDY标志和OVRN标志设置为1。当在IN令牌的接收数据中检测到数据包错误时，USBHS也会设置FRMNUM.CRCE标志为1。

●对于非等时传输管道，当以下两种情况的任意组合连续出现3次时：

USBHS发出的IN令牌没有从外围设备返回响应（当在检测到来自外围设备的DATA包之前检测到超时时）

在来自外围设备的数据包中检测到错误。在这种情况下，USBHS将相关的PIPENRDY标志设置为1，并将管道的相关PID[1:0]设置更改为00b（NAK响应）。

●对于同步传输管道，当外围设备没有返回对IN令牌的响应时（在检测到来自外围设备的DATA数据包之前检测到超时）或在外围设备的数据包中检测到错误。在这种情况下，USBHS将每个管道的相关NRDYSTS.PIPENRDY标志设置为1。管道的PID[1:0]设置不会更改。

●对于同步传输管道，当在接收到的数据包中检测到CRC错误或比特填充错误时。在这种情况下，USBHS为每个管道设置相关的NRDYSTS.PIPENRDY标志，并将CRCE标志设置为1。

●收到STALL握手时。在这种情况下，USBHS将每个管道的相关NRDYSTS.PIPENRDY标志设置为1，并将相关管道的PID[1:0]设置更改为STALL。

(2) 在连接中发生拆分事务时处于主机控制器模式

用于传输管道

在以下任何一种情况下，USBHS都会检测到NRDY中断：

●对于同步传输管道，当FIFO缓冲区中没有要传输的数据时发出OUT令牌的时间到来。在这种情况下，USBHS在发出开始分割事务时将给定管道的相关RDYSTS.PIPENRDY标志设置为1，并将FRMNUM.OVRN标志设置为1。USBHS还在OUT令牌之后传输零长度数据包。

●对于非等时传输管道，当以下两种情况的任意组合连续出现3次时：

集线器没有响应开始拆分和完成拆分事务（在检测到来自集线器的握手包之前检测到超时）

– An error is detected in the packet from the hub. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1 and changes the associated PID[1:0] setting for the pipe to 00b (NAK response).When an NRDY interrupt is detected on complete-split issuance, the USBHS clears the CSSTS flag to 0.

- When a STALL handshake is received for the complete-split transaction. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1, changes the associated PID[1:0] setting for the pipe to 11b (STALL response), and clears the CSSTS flag to 0. An interrupt is not detected during setup transaction.

For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the given pipe and the FRMNUM.OVRN flag to 1 on start-split issuance. The USBHS discards the received data for the IN token.
- During bulk-pipe transfers or transfers other than setup transactions with the DCP, when any combination of the following two cases occurs three consecutive times:
  – No response is returned from the hub for the IN token the USBHS issued on issuance of the start-split or complete-split transactions (when timeout is detected before detection of the data packet from the hub)
  – An error is detected in the packet from the hub. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1 and changes the associated PID[1:0] setting for the pipe to 00b (NAK response). When this condition occurs during complete-split, the USBHS clears the CSSTS flag to 0.
- During a complete-split transaction for isochronous transfer or interrupt transfer pipes, when any combination of the following two cases occurs three consecutive times:
  – No response is returned from the hub for the IN token issued by the USBHS (when a timeout is detected before detection of the DATA packet from the hub)
  – An error is detected in the packet from the hub. On generating this condition for an interrupt transfer pipe, the USBHS sets the associated NRDYSTS.PIPENRDY flag to 1, changes the associated PID[1:0] setting for the pipe to 00b (NAK response), and clears the CSSTS flag to 0. On generating this condition for the pipe for isochronous transfers, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1, CRCE flag to 1, and clears the CSSTS bit to 0. It does not change the PID[1:0] setting.
- During a complete-split transaction, when the STALL handshake is received for a non-isochronous transfer pipe. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1, changes the associated PID[1:0] setting for the pipe to 11b (STALL response), and clears the CSSTS flag to 0.
- During a complete-split transaction, when the NYET handshake is received for an isochronous transfer or interrupt transfer pipe for the microframe number = 4. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe to 1 and the CRCE flag to 1, and clears the CSSTS flag to 0. It does not change the PID[1:0] setting.

(3) In device controller mode

For transmitting pipes

- When an IN token is received while there is no data to be transmitted in the FIFO buffer. In this case, the USBHS generates an NRDY interrupt request on reception of the IN token and sets the NRDYSTS.PIPENRDY flag to 1. For an isochronous transfer pipe in which an interrupt is generated, the USBHS transmits a zero-length packet and sets the FRMNUM.OVRN flag to 1.

For receiving pipes

- When an OUT token is received but there is no space available in the FIFO buffer. For an isochronous transfer pipe in which an interrupt is generated, the USBHS generates an NRDY interrupt request on reception of the OUT token and sets the NRDYSTS.PIPENRDY flag to 1 and the FRMNUM.OVRN flag to 1. For a non-isochronous transfer pipe in which an interrupt is generated, the USBHS generates an NRDY interrupt request when an NAK handshake is transferred after the data following the OUT token is received, and sets the NRDYSTS.PIPENRDY flag to 1. The NRDY interrupt request is not generated during retransmission because of a DATA-PID mismatch. In addition, the NRDY interrupt request is not generated if an error occurs in the DATA packet.
- On receiving a PING token when there is no space available in the FIFO buffer. The USBHS generates an NRDY interrupt request on reception of the PING token, setting the NRDYSTS.PIPENRDY flag to 1.

在来自集线器的数据包中检测到错误。在这种情况下，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，并将管道的相关PID[1:0]设置更改为00b（NAK响应）。当在发出完全拆分时检测到NRDY中断时，USBHS将CSSTS标志清零。

●当为完全拆分事务接收到STALL握手时。在这种情况下，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，将管道的相关PID[1:0]设置更改为11b（STALL响应），并将CSSTS标志清除为0。中断是在设置事务期间未检测到。

用于接收管道

●对于同步传输管道，当发出IN令牌的时间到来但FIFO缓冲区中没有可用空间时。在这种情况下，USBHS将给定管道的相关NRDYSTS.PIPENRDY标志和FRMNUM.OVRN标志设置为1在开始拆分发布时。USBHS丢弃接收到的IN令牌数据。

●在批量管道传输或与DCP的设置事务以外的传输过程中，当以下两种情况的任意组合发生连续3次时：

没有从集线器返回对USBHS在发出start-split或completesplit事务时发出的IN令牌的响应（当在检测到来自集线器的数据包之前检测到超时时）

在来自集线器的数据包中检测到错误。在这种情况下，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，并将管道的相关PID[1:0]设置更改为00b（NAK响应）。如果在完全拆分期间发生这种情况，USBHS会将CSSTS标志清除为0。

●在等时传输或中断传输管道的完全拆分事务中，当以下两种情况的任意组合连续发生3次时：

对于USBHS发出的IN令牌，集线器没有返回响应（当在检测到来自集线器的DATA数据包之前检测到超时时）

在来自集线器的数据包中检测到错误。在为中断传输管道生成此条件时，
USBHS将关联的NRDYSTS.PIPENRDY标志设置为1，将管道的关联PID[1:0]设置更改为00b（NAK响应），并将CSSTS标志清除为0。在为同步传输的管道生成此条件时，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，CRCE标志设置为1，并将CSSTS位清除为0。它不会更改PID[1:0]设置。

●在完全拆分事务期间，当接收到非同步传输管道的STALL握手时。在这种情况下，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，将管道的相关PID[1:0]设置更改为11b（STALL响应），并将CSSTS标志清除为0。

●在完全拆分事务期间，当接收到同步传输或中断的NYET握手时
微帧编号的传输管道=4。在这种情况下，USBHS将每个管道的相关NRDYSTS.PIPENRDY标志设置为1，CRCE标志设置为1，并将CSSTS标志清除为0。它不会更改PID[1:0]设置。

(3) 在设备控制器模式下

用于传输管道

●当接收到一个IN令牌而FIFO缓冲区中没有要传输的数据时。在这种情况下，USBHS
在接收到IN令牌时生成NRDY中断请求并将NRDYSTS.PIPENRDY标志设置为1。对于产生中断的同步传输管道，USBHS发送一个长度为零的数据包并将FRMNUM.OVRN标志设置为1.

用于接收管道

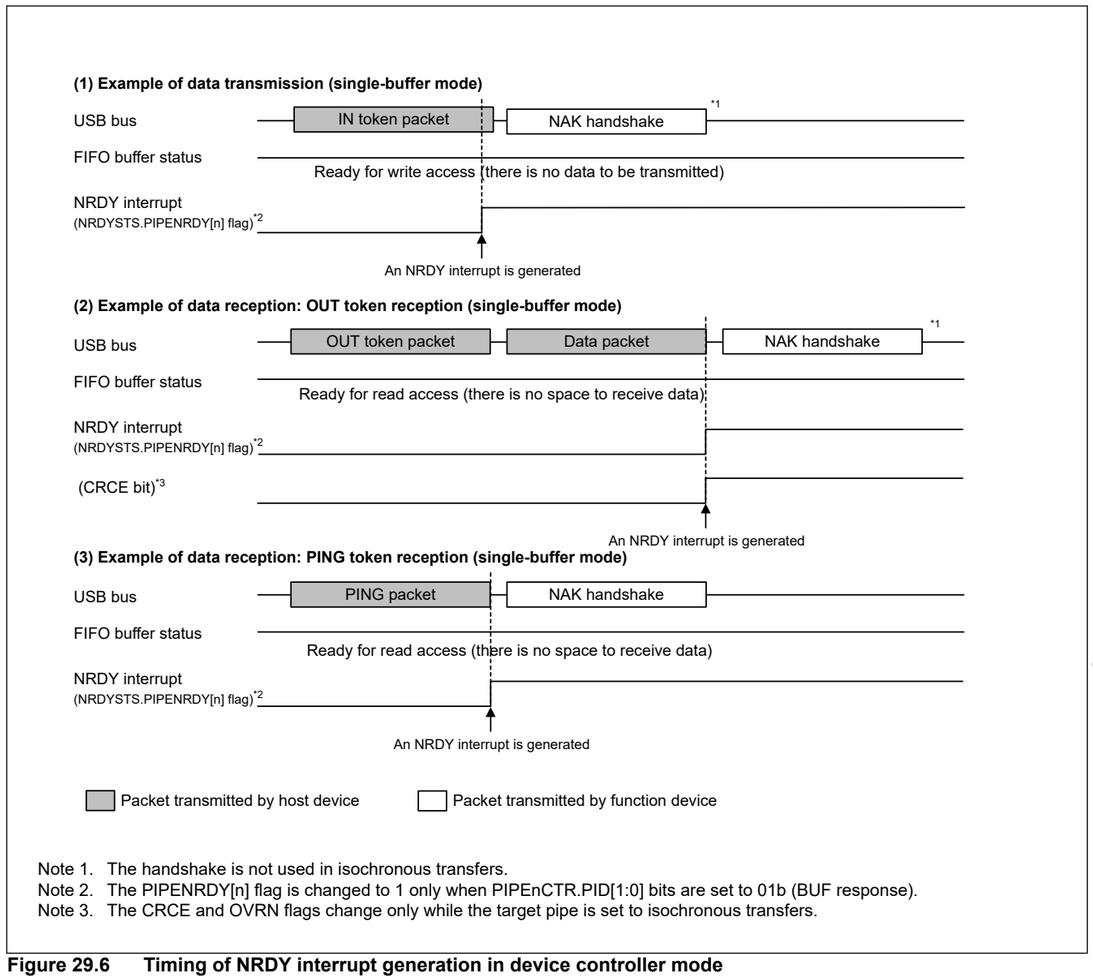
●当接收到OUT令牌但FIFO缓冲区中没有可用空间时。对于产生中断的同步传输管道，USBHS在接收到OUT令牌时产生一个NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1，将FRMNUM.OVRN标志设置为1。对于非同步传输管道在产生中断时，USBHS在接收到OUT令牌之后的数据后传输NAK握手时产生NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1。在重传期间不会产生NRDY中断请求，因为DATA-PID不匹配。除此之外

如果DATA包中发生错误，则不会产生NRDY中断请求。

●在FIFO缓冲区中没有可用空间时接收PING令牌。USBHS在接收到PING令牌时生成一个NRDY中断请求，将NRDYSTS.PIPENRDY标志设置为1。

- For isochronous transfer pipes, when a token is not received successfully within an interval frame. In this case, the USBHS generates an NRDY interrupt request when the SOF is received, and sets the NRDYSTS.PIPENRDY flag to 1.

Figure 29.6 shows the timing of NRDY interrupt generation in device controller mode.



Note 1. The handshake is not used in isochronous transfers.
Note 2. The PIPENRDY[n] flag is changed to 1 only when PIPEnCTR.PID[1:0] bits are set to 01b (BUF response).
Note 3. The CRCE and OVRN flags change only while the target pipe is set to isochronous transfers.

Figure 29.6 Timing of NRDY interrupt generation in device controller mode

29.3.6.3 BEMP interrupt

On detecting a BEMP interrupt for the pipe whose PID[1:0] bits in the pipe control register are set to 01b (BUF response) by software, the USBHS sets the associated BEMPSTS.PIPEBEMP flag to 1. If the associated BEMPENB bit is set to 1 by software, the USBHS sets the INTSTS0.BEMP flag to 1 and generates a USB interrupt. This section describes the conditions in which the USBHS generates an internal BEMP interrupt request.

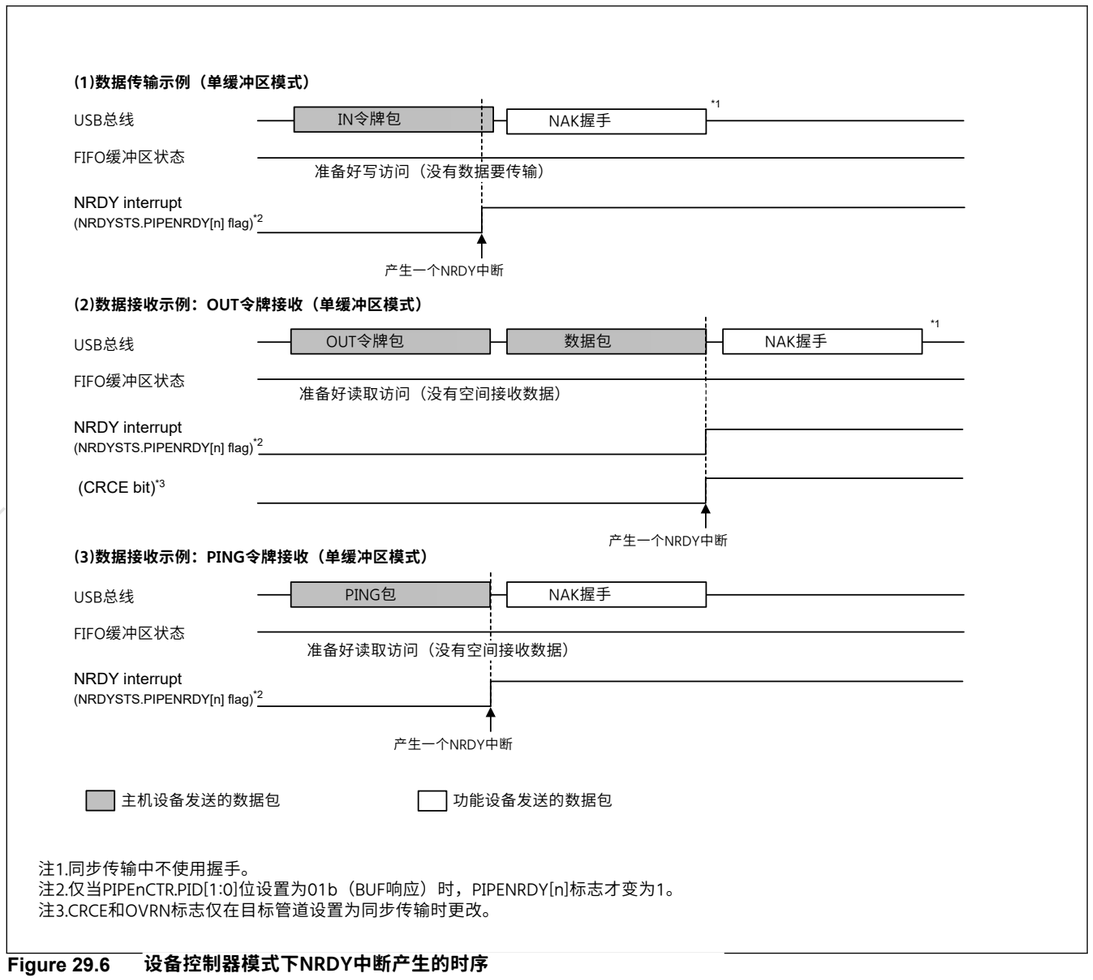
(1) For transmitting pipes

When the FIFO buffer of the associated pipe is empty on completion of transmission, including zero-length packet transmission, and in single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for a non-DCP pipe. The internal BEMP interrupt request is not generated in any of the following conditions:

- When the CPU or DMA/DTC has already started writing data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode
- When the buffer is cleared (emptied) by setting 1 to the PIPEnCTR.ACLRM or the BCLR bit in the port control register

●对于同步传输管道，当在间隔帧内没有成功接收到令牌时。在这种情况下，
USBHS在接收到SOF时产生一个NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1。

图29.6显示了设备控制器模式下NRDY中断产生的时序。



注1.同步传输中不使用握手。
注2.仅当PIPEnCTR.PID[1:0]位设置为01b（BUF响应）时，PIPENRDY[n]标志才变为1。
注3.CRCE和OVRN标志仅在目标管道设置为同步传输时更改。

Figure 29.6 设备控制器模式下NRDY中断产生的时序

29.3.6.3 BEMP interrupt

在检测到管道控制寄存器中的PID[1:0]位被软件设置为01b（BUF响应）的管道的BEMP中断时，USBHS将相关的BEMPSTS.PIPEBEMP标志设置为1。如果相关的BEMPENB位是由软件设置为1，USBHS将INTSTS0.BEMP标志设置为1并产生USB中断。本节介绍USBHS产生内部BEMP中断请求的条件。

(1) 用于传输管道

当相关管道的FIFO缓冲区在传输完成时为空时，包括零长度数据包传输，并且在单缓冲区模式下，内部BEMP中断请求与非DCP管道的BRDY中断同时生成。在以下任何一种情况下都不会产生内部BEMP中断请求：

●当CPU或DMADTC在双缓冲模式下从一个FIFO缓冲区完成数据传输后已经开始向CPU的FIFO缓冲区写入数据时

●当通过将PIPEnCTR.ACLRM或端口控制寄存器中的BCLR位设置为1来清除（清空）缓冲区时

- When an IN transfer (zero-length packet transmission) is performed during the control transfer status stage in device controller mode

(2) For receiving pipes

When a successfully-received data packet size exceeds the specified maximum packet size. In this case, the USBHS generates a BEMP interrupt request, sets the associated BEMPSTS.PIPEBEMP flag to 1, discards the received data, and changes the associated PID[1:0] setting for the pipe to STALL (11b). The USBHS returns no response in host controller mode, and returns STALL response in device controller mode.

The internal BEMP interrupt request is not generated in any of the following conditions:

- When a CRC error or a bit stuffing error is detected in the received data
- When a setup transaction is being performed:
  - Writing 0 to the BEMPSTS.PIPEBEMP flag clears the status
  - Writing 1 to the BEMPSTS.PIPEBEMP flag has no effect

Figure 29.7 shows the timing of BEMP interrupt generation in device controller mode.

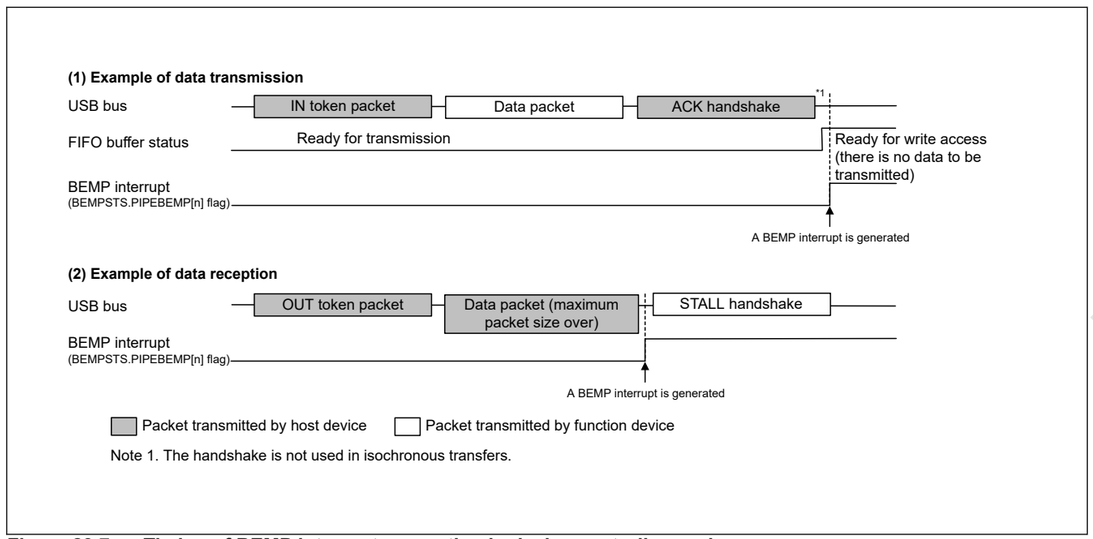


Figure 29.7 Timing of BEMP interrupt generation in device controller mode

29.3.6.4 Device state transition interrupt (device controller mode)

Figure 29.8 shows a diagram of the USBHS device state transitions. The USBHS controls device states and generates device state transition interrupts. However, recovery from the Suspend state (resume signal detection) is detected by means of the resume interrupt. Device state transition interrupts can be enabled or disabled independently in INTENB0. Devices whose states have changed can be checked in the PL1CTRL.DVSQ[3:0] flags.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is detected.

The USBHS controls device states, and device state transition interrupts can be generated, only in device controller mode.

●在设备控制器模式的控制传输状态阶段进行IN传输（零长度包传输）时

(2) 用于接收管道

当成功接收的数据包大小超过指定的最大包大小时。在这种情况下，USBHS生成一个BEMP中断请求，将相关的BEMPSTS.PIPEBEMP标志设置为1，丢弃接收到的数据，并将管道的相关PID[1:0]设置更改为STALL(11b)。USBHS在主机控制器模式下不返回响应，在设备控制器模式下返回STALL响应。

在以下任何一种情况下都不会产生内部BEMP中断请求：

●在接收到的数据中检测到CRC错误或位填充错误时

●执行设置事务时：

将0写入BEMPSTS.PIPEBEMP标志清除状态

向BEMPSTS.PIPEBEMP标志写入1无效

图29.7显示了设备控制器模式下BEMP中断产生的时序。

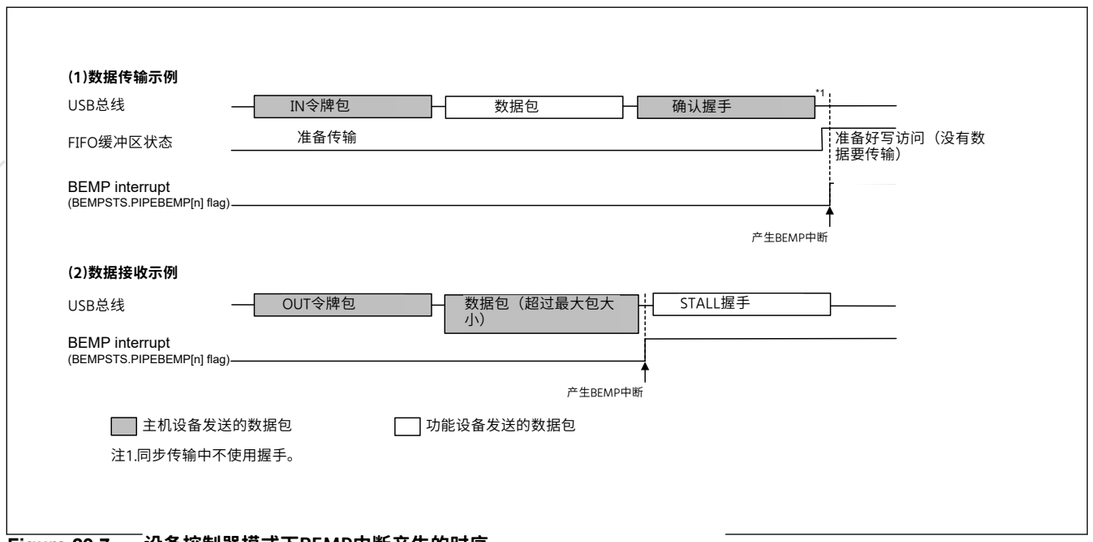


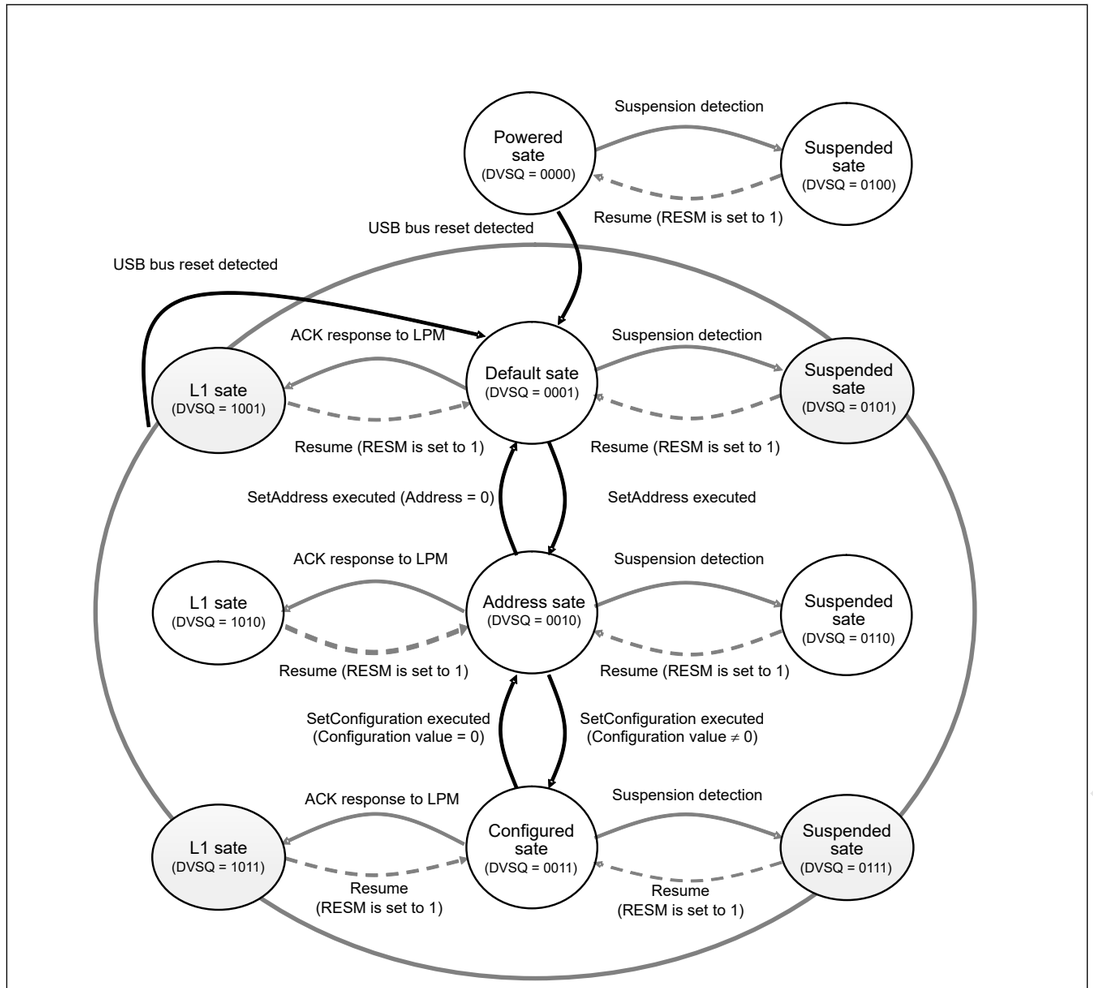
Figure 29.7 设备控制器模式下BEMP中断产生的时序

29.3.6.4 设备状态转换中断（设备控制器模式）

图29.8显示了USBHS设备状态转换的示意图。USBHS控制设备状态并产生设备状态转换中断。但是，从挂起状态的恢复（恢复信号检测）是通过恢复中断来检测的。可以在INTENB0中独立启用或禁用设备状态转换中断。可以在PL1CTRL.DVSQ[3:0]标志中检查状态已更改的设备。

当转换到默认状态时，检测到USB总线复位后会产生设备状态转换中断。

USBHS控制设备状态，并且只能在设备控制器模式下产生设备状态转换中断。



Note 1. For a transition, indicated by a solid line, the DVST bit is set to 1. For a resume, indicated by a dashed line, the RESM bit is set to 1.

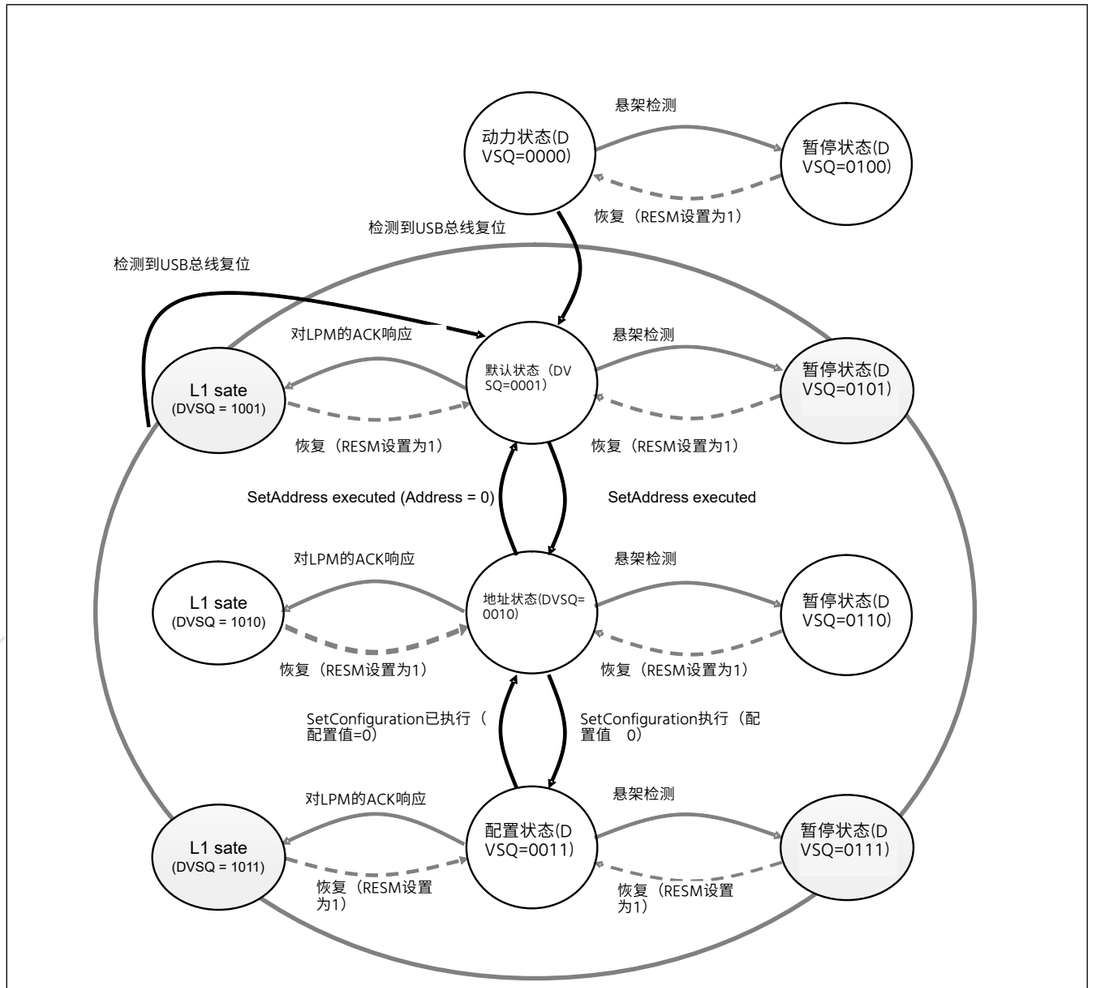
Figure 29.8 Device state transitions

29.3.6.5 Control transfer stage transition interrupt (device controller mode)

Figure 29.9 shows a diagram of the control transfer stage transitions of the USBHS. The USBHS controls the control transfer sequence and generates control transfer stage transition interrupts. Control transfer stage transition interrupts can be enabled or disabled independently in INTENB0. Transfer stages that have transitioned can be checked in the INTSTS0.CTSQ[2:0] bits.

Control transfer stage transition interrupts are generated only in device controller mode. This section describes control transfer sequence errors. When an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).

- Control read transfer errors
  - An OUT token or PING token is received but no data is transferred in response to the IN token at the data stage
  - An IN token is received at the status stage



注1.对于由实线表示的转换，DVST位设置为1。对于由虚线表示的恢复，RESM位设置为1。

Figure 29.8 设备状态转换

29.3.6.5 控制转移阶段转换中断（设备控制器模式）

图29.9显示了USBHS的控制传输阶段转换图。USBHS控制控制传输序列并产生控制传输阶段转换中断。控制转移阶段转换中断可以在INTENB0中独立启用或禁用。可以在INTSTS0.CTSQ[2:0]位中检查已转换的传输阶段。

控制转移阶段转换中断仅在设备控制器模式下产生。本节描述控制传输序列错误。发生错误时，DCPCTR.PID[1:0]位设置为1xb（STALL响应）。

- 控制读取传输错误
  - 接收到OUT令牌或PING令牌，但在数据阶段没有响应IN令牌传输数据
  - 在状态阶段收到一个IN令牌

- A data packet with DATAPID = DATA0 is received at the status stage

- Control write transfer errors
  - An IN token is received but no ACK returned in response to the OUT token in the data stage
  - A data packet with DATAPID = DATA0 is received as the first data packet at the data stage
  - An OUT token or PING token is received in the status stage

- Control write no data transfer errors
  - An OUT token or PING token is received at the status stage

At the control write transfer data stage, if the receive data length exceeds the wLength value of the USB request, it is not recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT flag = 1), the CTSQ[2:0] = 110b value is saved until CTRT flag clears to 0, clearing the interrupt status. While CTSQ[2:0] bits = 110b is being saved, no CTRT interrupt for ending the setup stage is generated, even if a new USB request is received. The USBHS saves the setup stage completion status, and it generates a CTRT interrupt after the interrupt status is cleared by software.

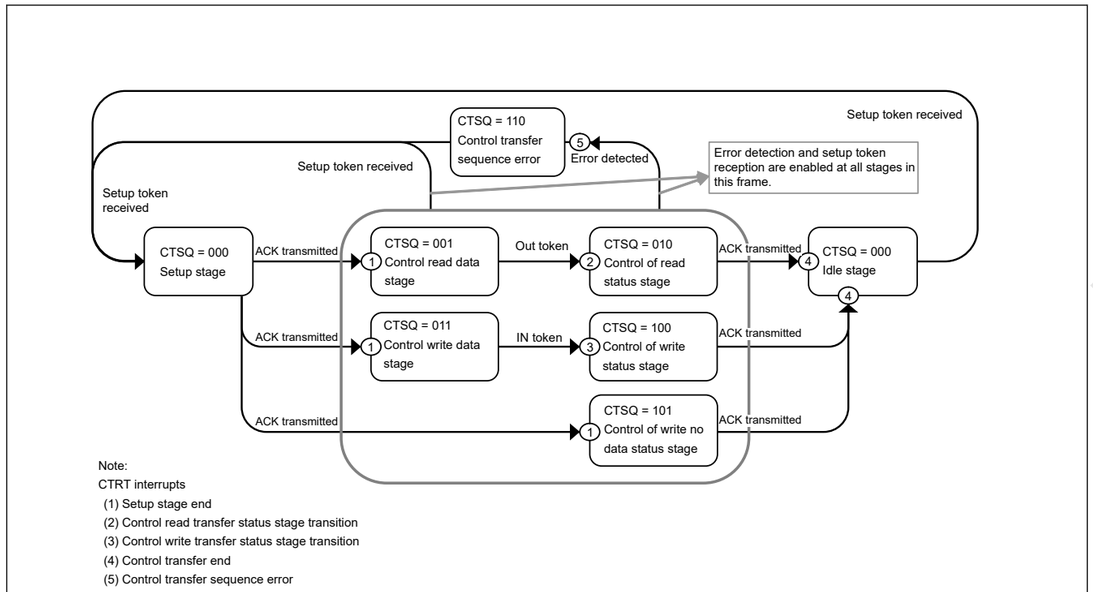


Figure 29.9 Control transfer stage transitions

29.3.6.6 Frame update interrupt

In host controller mode, an interrupt is generated when the frame number is updated.

In device controller mode, an SOFR interrupt is generated when the frame number is updated. The USBHS updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

29.3.6.7 VBUS interrupt

When the USBHS_VBUS pin level changes, a VBUS interrupt is generated. The level of the USBHS_VBUS pin can be checked in the INTSTS0.VBSTS flag. Whether the host controller is connected or disconnected can be confirmed using the

在状态阶段接收到DATAPID=DATA0的数据包

●控制写入传输错误

在数据阶段接收到一个IN令牌但没有返回ACK以响应OUT令牌

DATAPID=DATA0的数据包作为数据阶段的第一个数据包被接收

在状态阶段收到OUT令牌或PING令牌

●控制写入无数据传输错误

在状态阶段收到OUT令牌或PING令牌

在控制写入传输数据阶段，如果接收数据长度超过USB请求的wLength值，则不被识别为控制传输序列错误。在控制读取传输状态阶段，除了零长度数据包之外的数据包被一个ACK响应接收并且传输正常结束。

当CTRT中断响应序列错误（INTSTS0.CTRT标志=1）时，CTSQ[2:0]=110b值被保存，直到CTRT标志清除为0，清除中断状态。在保存CTSQ[2:0]位=110b时，不会产生用于结束设置阶段的CTRT中断，即使收到新的USB请求也是如此。USBHS保存建立阶段完成状态，软件清除中断状态后产生CTRT中断。

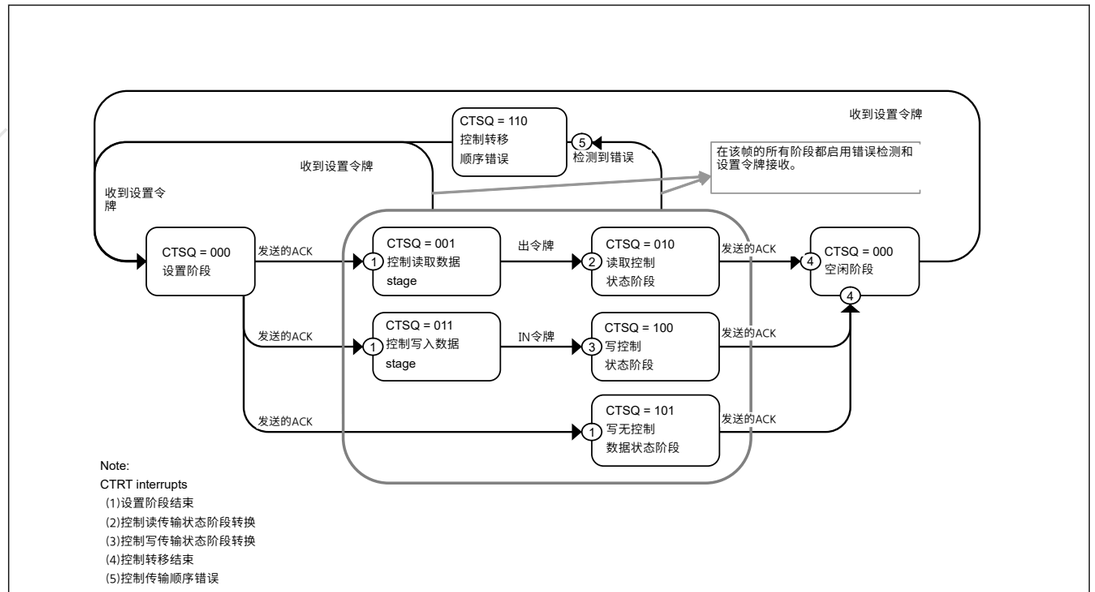


Figure 29.9 控制转移阶段转换

29.3.6.6 帧更新中断

在主机控制器模式下，更新帧号时会产生中断。

在设备控制器模式下，更新帧号时会产生SOFR中断。如果在全速运行期间检测到新的SOF数据包，USBHS会更新帧号并生成SOFR中断。

29.3.6.7 VBUS interrupt

当USBHS_VBUS引脚电平改变时，会产生VBUS中断。USBHS_VBUS引脚的电平可以在INTSTS0.VBSTS标志中检查。上位控制器是否连接或断开可以使用确认

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VBUS interrupt. If the system is activated with the host controller connected, the first VBUS interrupt is not generated, because there is no change in the USBHS_VBUS pin level.

29.3.6.8 Resume interrupt

In device controller mode, a resume interrupt is generated when the device is in the Suspend state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the Suspend state is detected by means of the resume interrupt.

In host controller mode, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

29.3.6.9 OVRCR interrupt

An OVRCR interrupt is generated when the USBHS_OVRCURA or USBHS_OVRCURB pin level has changed. The levels of the USBHS_OVRCURA and USBHS_OVRCURB pins can be checked in the SYSSTS0.OVCMON[1:0] flags. The external power supply IC can check whether overcurrent is detected using the OVRCR interrupt.

For OTG connections, the OVRCR interrupt allows you to check whether a change is detected in the VBUS comparator.

29.3.6.10 BCHG interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether a peripheral device is connected. It can also be used to detect a remote wakeup in host controller mode. The BCHG interrupt is generated in both host and device controller modes.

29.3.6.11 DTCH interrupt

A DTCH interrupt occurs when a USB bus disconnect is detected in host controller mode. The USBHS detects bus disconnects in compliance with the USB 2.0 specification.

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software. The pipes enter the wait state for a bus connection to the port, waiting for an ATTCH interrupt to occur. Regardless of the value set in the associated interrupt enable bit, the USBHS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt is detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state

29.3.6.12 SACK interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet is received from the peripheral device in host controller mode. The SACK interrupt can be used to confirm that the setup transaction is successfully complete.

29.3.6.13 SIGN interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet is not correctly received from the peripheral device three consecutive times in host controller mode. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

29.3.6.14 ATTCH interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 µs in host controller mode. To be more specific, an ATTCH interrupt is detected in any of the following conditions:

- When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 µs
- When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 µs

29.3.6.15 EOFERR interrupt

An EOFERR interrupt occurs when the USBHS detects that communication is not complete at the EOF2 timing defined in the USB 2.0 specification.

VBUS中断。如果系统在连接主机控制器的情况下激活，则不会产生第一个VBUS中断，因为USBHS_VBUS引脚电平没有变化。

29.3.6.8 恢复中断

在设备控制器模式下，当设备处于Suspend状态并且USB总线状态发生变化（从J-state到K-state，或从J-state到SE0）时，会产生一个恢复中断。通过恢复中断检测从挂起状态的恢复。

在主机控制器模式下，不会产生恢复中断。使用BCHG中断来检测USB总线状态的变化。

29.3.6.9 OVRCR interrupt

当USBHS_OVRCURA或USBHS_OVRCURB引脚电平发生变化时，会产生OVRCR中断。USBHS_OVRCURA和USBHS_OVRCURB引脚的电平可以在SYSSTS0.OVCMON[1:0]标志中检查。外部电源IC可以使用OVRCR中断检查是否检测到过电流。

对于OTG连接，OVRCR中断允许您检查是否在VBUS比较器中检测到变化。

29.3.6.10 BCHG interrupt

当USB总线状态改变时会产生BCHG中断。BCHG中断可用于检测是否连接了外围设备。它还可用于检测主机控制器模式下的远程唤醒。BCHG中断在主机和设备控制器模式下产生。

29.3.6.11 DTCH interrupt

当在主机控制器模式下检测到USB总线断开连接时，会发生DTCH中断。USBHS检测符合USB2.0规范的总线断开连接。

在检测到中断时，为相关端口执行通信的所有管道必须由软件终止。管道进入等待状态，等待总线连接到端口，等待ATTCH中断发生。无论相关中断使能位中设置的值如何，USBHS硬件：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态

29.3.6.12 SACK中断

当在主机控制器模式下从外围设备接收到对发送的设置数据包的ACK响应时，将产生SACK中断。SACK中断可用于确认设置事务成功完成。

29.3.6.13 标志中断

在主机控制器模式下，如果连续三次未从外围设备正确接收到已发送的设置数据包的ACK响应，则会产生SIGN中断。SIGN中断可用于检测没有从外围设备发送的ACK响应或ACK数据包的损坏。

29.3.6.14 ATTCH interrupt

在主机控制器模式下，当在USB端口上检测到全速信号电平的J状态或K状态持续2.5µs时，将产生ATTCH中断。更具体地说，在以下任何一种情况下都会检测到ATTCH中断：

- 当K-state、SE0或SE1变为J-state时，J-state持续2.5µs
- J-state、SE0或SE1变为K-state时，K-state持续2.5µs

29.3.6.15 EOFERR interrupt

当USBHS检测到在USB2.0规范中定义的EOF2时序未完成通信时，将发生EOFERR中断。

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software, and the port must be re-enumerated. Regardless of the value set in the associated interrupt enable bit, the USBHS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt is detected to 0
- Puts the port in which the EOFERR interrupt is generated into the idle state

29.3.6.16 PDDETINT interrupt

The USBHS sets the INTSTS1.PDDETINT flag to 1 on detecting a level change (high to low or low to high) in the PDDET pin input value and generates the PDDETINT interrupt. When the PDDETINT interrupt is generated, use software to repeatedly read the BCCTRL.PDDETSTS flag until the same value is read three or more times, and perform debounce processing.

29.3.6.17 LPMEND interrupt

When the LPM transaction ends because a response from the peripheral device or a timeout is detected, the INTSTS1.LPMEND flag sets to 1 and the LPMEND interrupt is generated.

29.3.6.18 L1RSMEND interrupt

When performing resume processing when the USBHS has transitioned to the L1 state because an ACK is received in response to an LPM token, the USBHS sets the INTSTS1.L1RSMEND flag to 1 on completion of the resume processing.

29.3.7 Pipe Control

Table 29.22 lists the pipe settings for the USBHS. USB data transfer is performed through logical pipes that the software associates with endpoints. The USBHS provides 10 pipes for data transfer. Set up the pipes based on your system specifications.

Table 29.22 Pipe settings (1 of 2)

Register name	Bit name	Setting	Notes
DCPCFG PIPECFG	TYPE[1:0]	Transfer type	Pipes 1 to 9: Settable
	BFRE	BRDY interrupt mode	Pipes 1 to 5: Settable
	DBLB	Double buffer select	Pipes 1 to 5: Settable
	CNTMD	Selection of continuous transfer or discontinuous transfer	Pipes 1, 2: Settable only for bulk transfers Pipes 3 to 5: Settable
	DIR	Transfer direction select	IN or OUT settable
	EPNUM[3:0]	Endpoint number	Pipes 1 to 9: Settable Set this number to a value other than 0000 when one or more pipes are used.
	SHTNAK	Selects disabled state for pipe when transfer ends	Pipes 1, 2: Settable only for bulk transfers Pipes 3 to 5: Settable
PIPEBUF	BUFSIZE	FIFO buffer size	DCP: Setting disabled (fixed to 256 bytes) Pipes 1 to 5: Settable up to 2 KB Pipes 6 to 9: Setting disabled (fixed to 64 bytes)
	BUFNMB	FIFO buffer number	DCP: Setting disabled (fixed to 0h-3h area) Pipes 1 to 5: Setting disabled (8h-87h area specifiable) Pipes 6 to 9: Setting disabled (fixed to 4h-7h area)
DCPMAXP PIPEMAXP	DEVSEL[3:0]	Device select	Viewable only in host controller mode
	MXPS	Maximum packet size	Setting compliant with USB specification
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Setting disabled
	IITV[2:0]	Interval counter	Pipes 1, 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Settable only in host controller mode

在检测到中断时，所有为相关端口执行通信的管道必须由软件终止，并且必须重新枚举该端口。无论相关中断使能位中设置的值如何，USBHS硬件：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将产生EOFERR中断的端口置于空闲状态

29.3.6.16 PDDETINT interrupt

USBHS在检测到PDDET引脚输入值的电平变化（从高到低或从低到高）时将INTSTS1.PDDETINT标志设置为1，并产生PDDETINT中断。当PDDETINT中断产生时，用软件反复读取BCCTRL.PDDETSTS标志，直到读取3次以上相同的值，并进行去抖动处理。

29.3.6.17 LPMEND interrupt

当LPM事务由于检测到来自外围设备的响应或超时而结束时，
INTSTS1.LPMEND标志设置为1并产生LPMEND中断。

29.3.6.18 L1RSMEND interrupt

当USBHS由于接收到响应LPM令牌的ACK而转换到L1状态时执行恢复处理时，USBHS在恢复处理完成时将INTSTS1.L1RSMEND标志设置为1。

29.3.7 管道控制

表29.22列出了USBHS的管道设置。USB数据传输是通过软件与端点关联的逻辑管道执行的。USBHS提供了10个用于数据传输的管道。根据您的系统规格设置管道。

Table 29.22 管道设置(1of2)

注册名称	位名称	Setting	Notes
DCPCFG PIPECFG	TYPE[1:0]	传输类型	管道1至9：可设置
	BFRE	BRDY中断模式	管道1至5：可设置
	DBLB	双缓冲选择	管道1至5：可设置
	CNTMD	选择连续转移或不连续转移	管道1、2：仅可设置批量传输 管道3至5：可设置
	DIR	传输方向选择	输入或输出可设置
	EPNUM[3:0]	端点编号	管道1到9：可设置当使用一个或多个管道时，将此数字设置为0000以外的值。
	SHTNAK	传输结束时为管道选择禁用状态	管道1、2：仅可设置批量传输 管道3至5：可设置
PIPEBUF	BUFSIZE	FIFO缓冲区大小	DCP：设置禁用（固定为256字节） 管道1到5：最大可设置2KB 管道6到9：设置禁用（固定为64字节）
	BUFNMB	先进先出缓冲器编号	DCP：设置禁用（固定为0h-3h区域） 管道1至5：禁用设置（可指定8h-87h区域） 管道6至9：禁用设置（固定为4h-7h区域）
DCPMAXP PIPEMAXP	DEVSEL[3:0]	设备选择	仅在主机控制器模式下可见
	MXPS	最大数据包大小	符合USB规格的设置
PIPEPERI	IFIS	缓冲区刷新	管道1、2：仅可设置用于同步传输 管道3至5：设置禁用管道6至9：设置禁用
	IITV[2:0]	间隔计数器	管道1、2：仅可设置用于同步传输管道3至5：设置禁用 管道6到9：仅在主机控制器模式下可设置

Table 29.22 Pipe settings (2 of 2)

Register name	Bit name	Setting	Notes
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit
	INBUFM	IN buffer monitor	Available only for pipes 1 to 5
	SUREQ	Setup request	Settable only for the DCP and controlled in host controller mode
	SUREQCLR	SUREQ clear	Settable only for the DCP and controlled in host controller mode
	CSCLR	CSSTS clear	Controllable only in host controller mode
	CSSTS	Split status check	Viewable only in host controller mode
	ATREPM	Auto response mode	Pipes 1 to 5: Settable only in device controller mode
	ACLRM	Auto buffer clear	Pipes 1 to 9: Settable
	SQCLR	Sequence clear	Clears the data toggle bit
	SQSET	Sequence set	Sets the data toggle bit
	SQMON	Sequence check	Monitors the data toggle bit
	PBUSY	PIPE busy check	—
	PID[1:0]	Response PID	—
PIPEnTRE	TRENB	Transaction count enable	Pipes 1 to 5: Settable
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Settable
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Settable

29.3.7.1 Pipe control register switching procedures

The following bits in the pipe control registers can be changed only when USB communication is prohibited (PID[1:0] bits are 00b (NAK response)). Figure 29.10 shows pipe control register switching procedures when USB communication is enabled (PID[1:0] bits are 00b (BUF response)).

Do not change the following registers and bits when USB communication is enabled (PID[1:0] bits are 01b (BUFresponse)):

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN
- Bits in DEVADDn (n = 0 to A)

To set the CSCLR bits and bits in DEVADDn (n = 0 to A), follow the procedures described in section 29.2. Register Descriptions.

Table 29.22 管道设置(2of2)

注册名称	位名称	Setting	Notes
DCPCTR PIPEnCTR	BSTS	缓冲状态	对于DCP，接收缓冲区状态和发送缓冲区状态通过ISEL位切换
	INBUFM	IN缓冲监视器	仅适用于管道1至5
	SUREQ	设置请求	只能为DCP设置并在主机控制器模式下控制
	SUREQCLR	SUREQ clear	只能为DCP设置并在主机控制器模式下控制
	CSCLR	CSSTS clear	仅在主机控制器模式下可控
	CSSTS	拆分状态检查	仅在主机控制器模式下可见
	ATREPM	自动响应模式	管道1到5：仅在设备控制器模式下可设置
	ACLRM	自动缓冲区清除	管道1至9：可设置
	SQCLR	序列清晰	清除数据切换位
	SQSET	序列集	设置数据切换位
	SQMON	序列检查	监控数据切换位
	PBUSY	管道忙检查	—
	PID[1:0]	响应PID	—
PIPEnTRE	TRENB	事务计数启用	管道1至5：可设置
	TRCLR	当前交易柜台清零	管道1至5：可设置
PIPEnTRN	TRNCNT	交易柜台	管道1至5：可设置

29.3.7.1 管道控制寄存器切换程序

只有当USB通信被禁止时（PID[1:0]位为00b（NAK响应））才能更改管道控制寄存器中的以下位。图29.10显示了启用USB通信时的管道控制寄存器切换过程（PID[1:0]位为00b（BUF响应））。

启用USB通信时，请勿更改以下寄存器和位（PID[1:0]位为01b(BUFresponse)）：

- DCPCFG和DCPMAXP中的位
- DCPCTR中的SQCLR和SQSET位
- PIPECFG、PIPEBUF、PIPEMAXP和PIPEPERI中的位
- PIPEnCTR中的ATREPM、ACLRM、SQCLR和SQSET位
- PIPEnTRE和PIPEnTRN中的位
- DEVADDn中的位（n=0到A）

要设置CSCLR位和DEVADDn中的位（n=0到A），请遵循第29.2节中描述的程序。登记 Descriptions.

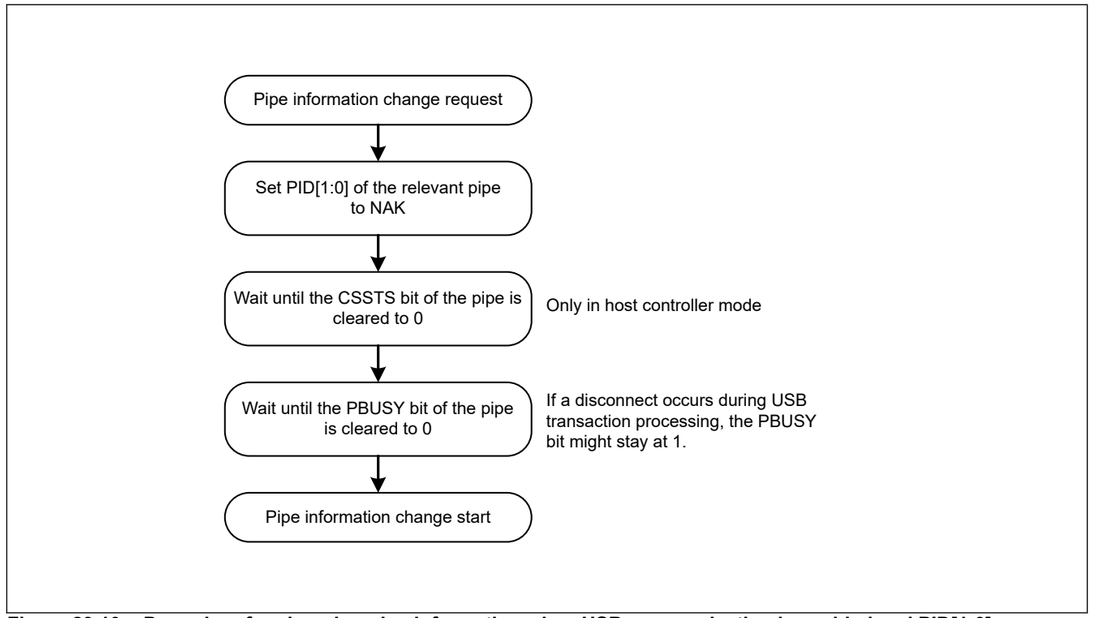

Figure 29.10 Procedure for changing pipe information when USB communication is enabled and PID[1:0] bits are 01b (BUF response)

The following bits in the pipe control registers can be changed only when the selected pipe information is not set in the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Do not set the following registers while the CURPIPE[3:0] bits are set:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- PIPEnCTR and ACLRM bits

To change pipe information, you must set the CURPIPE[3:0] bits to a pipe other than the one to be changed. For the DCP, the buffer must be cleared using the BCLR bit after the pipe information is changed.

29.3.7.2 Transfer types

The PIPECFG.TYPE[1:0] bits specify the following transfer types for each pipe:

- DCP: No setting necessary (fixed at control transfer)
- Pipes 1 and 2: Set to bulk transfer or isochronous transfer
- Pipes 3 to 5: Set to bulk transfer
- Pipes 6 to 9: Set to interrupt transfer

29.3.7.3 Endpoint number

The PIPECFG.EPNUM[3:0] bits are used to set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to 15.

- DCP: No setting is necessary (fixed at endpoint 0)
- Pipes 1 to 9: Select and set the endpoint numbers from 1 to 15 so that the combination of the PIPECFG.DIR and EPNUM[3:0] bits is unique

29.3.7.4 Maximum packet size setting

Specify the maximum packet size for each pipe in the MXPS bits in DCPMAXP and PIPEMAXP. The DCP and pipes 1 to 5 can be set to any of the maximum pipe sizes defined in the USB 2.0 specification. For pipes 6 to 9, the maximum packet

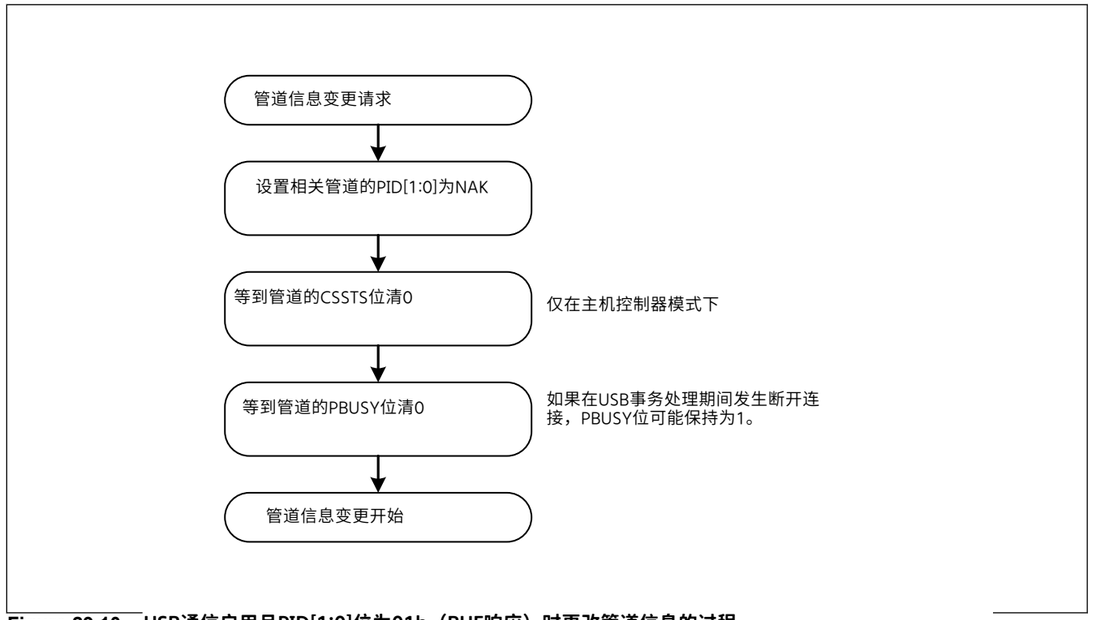

Figure 29.10 USB通信启用且PID[1:0]位为01b（BUF响应）时更改管道信息的过程

管道控制寄存器中的以下位只有在所选管道信息未设置时才能更改CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位。

设置CURPIPE[3:0]位时不要设置以下寄存器：

●DCPCFG和DCPMAXP中的位

●PIPECFG、PIPEBUF、PIPEMAXP和PIPEPERI中的位

●PIPEnCTR和ACLRM位

要更改管道信息，您必须将CURPIPE[3:0]位设置为要更改的管道以外的管道。对于DCP，必须在管道信息更改后使用BCLR位清除缓冲区。

29.3.7.2 传输类型

PIPECFG.TYPE[1:0]位为每个管道指定以下传输类型：

●DCP：无需设置（控制转移时固定）

●管道1和2：设置为批量传输或同步传输

●管道3到5：设置为批量传输

●管道6到9：设置为中断传输

29.3.7.3 端点编号

PIPECFG.EPNUM[3:0]位用于设置每个管道的端点编号。DCP固定在端点0。其他管道可以设置从端点1到15。

●DCP：无需设置（固定在端点0）

●管道1到9：从1到15选择和设置端点编号，以便PIPECFG.DIR和EPNUM[3:0]位的组合是唯一的

29.3.7.4 最大数据包大小设置

在DCPMAXP和PIPEMAXP的MXPS位中指定每个管道的最大数据包大小。DCP和管道1到5可以设置为USB2.0规范中定义的任何最大管道尺寸。对于管道6到9，最大数据包

size is 64 bytes. Set the maximum packet size as follows before starting a transfer (PID[1:0] bits are set to 01b (BUF response)):

- DCP: Set to 64 for high-speed operation
- DCP: Set to 8, 16, 32, or 64 for full-speed operation
- Pipes 1 to 5: Set to 512 for high-speed bulk transfers
- Pipes 1 to 5: Set to 8, 16, 32, or 64 for full-speed bulk transfers
- Pipes 1, 2: Set between 1 and 1024 for high-speed isochronous transfers
- Pipes 1, 2: Set between 1 and 1023 for full-speed isochronous transfers
- Pipes 6 to 9: Set between 1 and 64

High-bandwidth interrupt transfers and isochronous transfers are not supported.

29.3.7.5 Transaction counter for pipes 1 to 5 in the receiving direction

When the specified number of transactions is complete in the data packet receiving direction, the USBHS recognizes that the transfer has ended. Two transaction counters are provided. One is the PIPEnTRN register, which specifies the number of transactions to be executed, and the other is the current counter, which internally counts the number of executed transactions. If the PIPECFG.SHTNAK bit is set to 1, when the current counter value matches the specified number of transactions, the associated PIPEnCTR.PID[1:0] bits are set to 00b (NAK response) and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The data read from PIPEnTRN differs depending on the PIPEnTRE.TRENB setting as follows:

- The TRENB bit = 0: Specified transaction counter value can be read
- The TRENB bit = 1: Current counter value indicating the internally counted number of executed transactions can be read.

The following constraints apply when working with the TRCLR bit:

- If the transactions are being counted and the PIPEnCTR.PID[1:0] bits are set to 01b (BUF response), the current counter cannot be cleared
- If there is any data left in the buffer, the current counter cannot be cleared

29.3.7.6 Response PID

Specify the response PID for each pipe in the PID[1:0] bits in DCPCTR and PIPEnCTR. This section describes the USBHS operation with different response PID settings.

Software response PID settings in host controller mode

Select the response PID to specify the execution of transactions as follows:

- NAK setting: Using pipes is disabled and no transactions are executed
- BUF setting: Transactions are executed based on the FIFO buffer state:
  OUT direction: An OUT token is issued if the FIFO buffer contains transmit data.
  IN direction: An IN token is issued if the FIFO buffer is not full and can receive data.
- STALL setting: Using pipes is disabled and no transactions are executed

Note: Use the SUREQ bit to execute setup transactions for the DCP.

Software response PID settings in device controller mode

Select the response PID to respond as follows to transactions from the host:

- NAK setting: A NAK response is returned to all generated transactions
- BUF setting: A response is returned to transactions based on the FIFO buffer
- STALL setting: A STALL response is returned to all generated transactions

大小为64字节。在开始传输之前设置最大数据包大小如下（PID[1:0]位设置为01b（BUF响应））：

●DCP：设置为64用于高速运行
●DCP：设置为8、16、32或64以实现全速运行
●管道1到5：设置为512用于高速批量传输
●管道1到5：设置为8、16、32或64以实现全速批量传输
●管道1、2：设置在1到1024之间，用于高速同步传输
●管道1、2：设置在1和1023之间，用于全速同步传输
●管道6到9：设置在1到64之间

不支持高带宽中断传输和同步传输。

29.3.7.5 接收方向上管道1到5的事务计数器

当在数据包接收方向完成指定数量的事务时，USBHS识别传输已结束。提供了两个交易柜台。一个是PIPEnTRN寄存器，它指定要执行的事务数，另一个是当前计数器，它在内部对执行的事务数进行计数。如果PIPECFG.SHTNAK位设置为1，则当当前计数器值与指定的事务数匹配时，相关的PIPEnCTR.PID[1:0]位设置为00b（NAK响应）并禁用后续传输。通过PIPEnTRE.TRCLR位初始化事务计数器功能的当前计数器，事务可以从头开始重新计数。从PIPEnTRN读取的数据因PIPEnTRE.TRENB设置而异，如下所示：

●TRENB位=0：可以读取指定的事务计数器值
●TRENB位=1：当前计数器值表示内部计数的已执行事务数可以被读取。

使用TRCLR位时适用以下约束：

●如果正在对事务进行计数且PIPEnCTR.PID[1:0]位设置为01b（BUF响应），则无法清除当前计数器

●如果缓冲区中还有数据，则无法清除当前计数器

29.3.7.6 响应PID

在DCPCTR和PIPEnCTR的PID[1:0]位中指定每个管道的响应PID。本节介绍具有不同响应PID设置的USBHS操作。

主机控制器模式下的软件响应PID设置

选择响应PID来指定事务的执行，如下所示：

●NAK设置：禁用使用管道，不执行任何事务
●BUF设置：根据FIFO缓冲区状态执行事务：
  OUT方向：如果FIFO缓冲区包含发送数据，则发出OUT令牌。
  IN方向：如果FIFO缓冲区未满并且可以接收数据，则发出IN令牌。
●STALL设置：禁止使用管道，不执行任何事务

注意：使用SUREQ位执行DCP的设置事务。

设备控制器模式下的软件响应PID设置

选择响应PID以对来自主机的事务进行如下响应：

●NAK设置：对所有生成的事务返回NAK响应
●BUF设置：根据FIFO缓冲区向事务返回响应
●STALL设置：向所有生成的事务返回STALL响应

Note: For setup transactions, an ACK response is always returned, regardless of the PID[1:0] bits setting, and the USB request is stored in the register.

Hardware response PID settings in host controller mode and Hardware response PID settings in device controller mode describe situations in which the USBHS writes to the PID[1:0] bits because of specific transaction results.

Hardware response PID settings in host controller mode

- NAK setting: The PID[1:0] bits are set to 00b (NAK response) in the following cases, and issuing of tokens is automatically stopped:
  - When a non-isochronous transfer is performed and an NRDY interrupt is generated. For details, see section 29.3.6.2. NRDY interrupt
  - If a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
  - If transaction counting ends when the SHTNAK bit is set to 1 for bulk transfers
- BUF setting: The USBHS does not write this setting
- STALL setting: The PID[1:0] bits are set to STALL in the following cases, and issuing of tokens is automatically stopped:
  - When STALL is received in response to a transmitted token
  - When a received data packet exceeds the maximum packet size

Hardware response PID settings in device controller mode

- NAK setting: The PID[1:0] bits are set to 00b (NAK response) in the following cases, and a NAK response is returned to transactions:
  - When the setup token is received normally (DCP only)
  - If transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
- BUF setting: The USBHS does not write this setting
- STALL setting: The PID[1:0] bits are set to STALL in the following cases, and a STALL response is returned to transactions:
  - When a received data packet exceeds the maximum packet size
  - When a control transfer sequence error is detected

29.3.7.7 Data PID sequence bit

The USBHS automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit toggles on ACK handshake reception. When data is received, the sequence bit toggles on ACK handshake transmission. The SQCLR bit in DCPCTR and the SQSET bit in PIPEnCTR can be used to change the data PID sequence bit.

In device controller mode when control transfers are used, the USBHS automatically sets the sequence bit for stage transitions. DATA1 is returned when the setup stage ends. The sequence bit is not referenced and PID = DATA1 is returned in the status stage. Therefore, no software settings are required. However, in host controller mode when control transfers are used, the sequence bit must be set by software for the stage transitions.

For ClearFeature requests for transmission or reception, the data PID sequence bit must be set by software in both host and device controller modes.

29.3.7.8 Response PID = NAK function

The USBHS provides a function for disabling pipe operation (PID[1:0] bits are set to 00b (NAK response)) when the final data packet of a transaction is received. The USBHS automatically distinguishes this based on reception of a short packet or the transaction counter. Enable this function by setting the PIPECFG.SHTNAK bit to 1.

Note: 对于设置事务，无论PID[1:0]位设置如何，始终返回ACK响应，并且USB请求存储在寄存器中。

主机控制器模式下的硬件响应PID设置和设备控制器模式下的硬件响应PID设置描述了USBHS由于特定事务结果而写入PID[1:0]位的情况。

主机控制器模式下的硬件响应PID设置

●NAK设置：在以下情况下，PID[1:0]位设置为00b（NAK响应），令牌自动停止发行：

当执行非同步传输并产生NRDY中断时。详见29.3.6.2节。NRDY中断

如果在PIPECFG.SHTNAK位设置为1以进行批量传输时接收到短数据包

如果在SHTNAK位设置为1以进行批量传输时事务计数结束

●BUF设置：USBHS不写入此设置

●STALL设置：PID[1:0]位在以下情况下设置为STALL，令牌的发行自动停止：

当接收到STALL以响应传输的令牌时

当接收到的数据包超过最大包大小时

设备控制器模式下的硬件响应PID设置

●NAK设置：在以下情况下，PID[1:0]位设置为00b（NAK响应），并向事务返回NAK响应：

正常接收到设置令牌时（仅DCP）

当PIPECFG.SHTNAK位设置为1以进行批量传输时，如果事务计数结束或收到短数据包

●BUF设置：USBHS不写入此设置

●STALL设置：PID[1:0]位在以下情况下设置为STALL，并向事务返回STALL响应：

当接收到的数据包超过最大包大小时

当检测到控制传输序列错误时

29.3.7.7 数据PID序列位

当数据在控制传输数据阶段、批量传输和中断传输中成功传输时，USBHS会自动切换数据PID中的序列位。下一个要发送的数据PID的序列位可以通过DCPCTR和PIPEnCTR中的SQMON位来确认。发送数据时，序列位在ACK握手接收时切换。当接收到数据时，序列位在ACK握手传输上切换。DCPCTR中的SQCLR位和PIPEnCTR中的SQSET位可用于更改数据PID序列位。

在使用控制传输的设备控制器模式下，USBHS自动设置阶段转换的序列位。DATA1在设置阶段结束时返回。不引用序列位，在状态阶段返回PID=DATA1。因此，不需要任何软件设置。但是，在使用控制传输的主机控制器模式下，必须由软件设置序列位以进行阶段转换。

对于发送或接收的ClearFeature请求，数据PID序列位必须由软件在主机和设备控制器模式下设置。

29.3.7.8 响应PID=NAK功能

USBHS提供了在接收到事务的最终数据包时禁用管道操作（PID[1:0]位设置为00b（NAK响应））的功能。USBHS根据收到的短数据包或事务计数器自动区分这一点。通过将PIPECFG.SHTNAK位设置为1来启用此功能。

When the double buffer mode is being used for the FIFO buffer, using this function enables reception of data packets in transfer units. If pipe operation is disabled, software must enable the pipe again (PID[1:0] bits are set to 01b (BUF response)).

The response PID = NAK function can be used only for bulk transfers.

29.3.7.9 Auto response mode

For bulk transfer pipes (1 to 5), when the PIPEnCTR.ATREPM bit is set to 1, a transition is made to auto response mode.

During an OUT transfer (PIPECFG.DIR = 0), OUT-NAK mode is invoked, and during an IN transfer (DIR = 1), null auto response mode is invoked.

29.3.7.10 OUT-NAK mode

For bulk OUT transfer pipes, NAK is returned in response to an OUT token, and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To transition from normal mode to OUT-NAK mode, specify OUT-NAK mode while pipe operation is disabled (PID[1:0] = 00b for NAK response). Next, enable pipe operation (PID[1:0] = 01b for BUF response), on which OUT-NAK mode becomes valid. If an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is returned to the host.

To transition from OUT-NAK mode to normal mode, cancel OUT-NAK mode while pipe operation is disabled (NAK).

Next enable pipe operation (BUF). In normal mode, reception of OUT data is enabled.

29.3.7.11 Null auto response mode

For bulk IN transfer pipes, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To transition from normal mode to null auto response mode, specify null auto response mode while pipe operation is disabled (PID[1:0] bits are set to 00b (NAK response)). Next, enable pipe operation (PID[1:0] bits are set to 01b (BUF response)), on which null auto response mode becomes valid. Before setting null auto response mode, check that PIPEnCTR.INBUFM = 0, because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, empty the buffer using the PIPEnCTR.ACLRM bit. Do not write data from the FIFO port while a transition to null auto response mode is being made.

To transition from null auto response mode to normal mode, keep pipe operation disabled (PID[1:0] bits are set to 00b (NAK response)) for the period of the zero-length packet transmission (about 10 µs) before canceling the null auto response mode. In normal mode, data can be written from the FIFO port, so packet transmission to the host is enabled by enabling pipe operation (PID[1:0] bits are set to 01b (BUF response)).

29.3.8 FIFO Buffer

The USBHS provides a FIFO buffer for data transfers, and it manages the memory area used for each pipe. The FIFO buffer has two states depending on whether the access right is assigned to the system (CPU side) or the USBHS (SIE side).

29.3.8.1 Buffer status

Table 29.23 and Table 29.24 show the buffer status in the USBHS. The FIFO buffer status can be confirmed using the DCPCTR.BSTS and PIPEnCTR.INBUFM bits. The transfer direction for the FIFO buffer can be specified in the PIPECFG.DIR or CFIFOSEL.ISEL bit (when DCP is selected).

The INBUFM bit is valid for pipes 1 to 5 in the transmitting direction.

When a transmitting pipe uses double buffering, the software can read the BSTS bit to monitor the FIFO buffer status on the CPU side and the INBUFM bit to monitor the FIFO buffer status on the SIE side. When write access to the FIFO port by the CPU or DMA/DTC is slow and the buffer empty status cannot be determined using the BEMP interrupt, the software can use the INBUFM bit to confirm the end of transmission.

Table 29.23 Buffer status indicated in the BSTS flag (1 of 2)

ISEL or DIR	BSTS	FIFO buffer status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.

当FIFO缓冲区使用双缓冲区模式时，使用此功能可以接收以传输为单位的数据包。如果禁用管道操作，软件必须再次启用管道（PID[1:0]位设置为01b（BUF响应））。

响应PID=NAK函数只能用于批量传输。

29.3.7.9 自动响应模式

对于批量传输管道（1到5），当PIPEnCTR.ATREPM位设置为1时，将转换到自动响应模式。

在OUT传输期间(PIPECFG.DIR=0)，将调用OUT-NAK模式，在IN传输期间(DIR=1)，将调用空自动响应模式。

29.3.7.10 OUT-NAK mode

对于批量OUT传输管道，NAK响应OUT令牌返回，并且当PIPEnCTR.ATREPM位设置为1。要从正常模式转换到OUT-NAK模式，请在禁用管道操作时指定OUT-NAK模式（对于NAK响应，PID[1:0]=00b）。接下来，启用管道操作（PID[1:0]=01b用于BUF响应），此时OUT-NAK模式变为有效。如果在禁用管道操作之前立即收到OUT令牌，则正常接收令牌数据，并向主机返回ACK。

要从OUT-NAK模式转换到正常模式，请在禁用管道操作(NAK)时取消OUT-NAK模式。

接下来启用管道操作(BUF)。在正常模式下，可以接收OUT数据。

29.3.7.11 空自动响应模式

对于批量IN传输管道，当PIPEnCTR.ATREPM位设置为1时，将连续传输零长度数据包。

要从正常模式转换为空自动响应模式，请在禁用管道操作时指定空自动响应模式（PID[1:0]位设置为00b（NAK响应））。接下来，启用管道操作（PID[1:0]位设置为01b（BUF响应）），此时空自动响应模式变为有效。在设置空自动响应模式之前，请检查PIPEnCTR.INBUFM=0，因为只有在缓冲区为空时才能设置模式。如果INBUFM位为1，则使用PIPEnCTR.ACLRM位清空缓冲区。在转换到空自动响应模式时，不要从FIFO端口写入数据。

要从空自动响应模式转换到正常模式，请在零长度数据包传输期间（约10μs）保持管道操作禁用（PID[1:0]位设置为00b（NAK响应）），然后再取消空自动响应模式。在正常模式下，数据可以从FIFO端口写入，因此通过启用管道操作（PID[1:0]位设置为01b（BUF响应））来启用到主机的数据包传输。

29.3.8 FIFO Buffer

USBHS为数据传输提供FIFO缓冲区，并管理用于每个管道的内存区域。FIFO缓冲区有两种状态，具体取决于访问权限是分配给系统（CPU端）还是USBHS（SIE端）。

29.3.8.1 缓冲状态

表29.23和表29.24显示了USBHS中的缓冲区状态。FIFO缓冲区状态可以使用确认DCPCTR.BSTS和PIPEnCTR.INBUFM位。FIFO缓冲区的传输方向可以在pipecfg.dir或cfifoselisel位（选择DCP时）。

INBUFM位对传输方向的管道1到5有效。

当传输管道使用双缓冲时，软件可以读取BSTS位来监控CPU侧的FIFO缓冲区状态，以及读取INBUFM位来监控SIE侧的FIFO缓冲区状态。当写访问FIFO端口由CPU或DMADTC较慢且无法使用BEMP中断确定缓冲区空状态，软件可以使用INBUFM位确认传输结束。

Table 29.23 BSTS标志中指示的缓冲区状态（2个中的1个）

ISEL或DIR	BSTS	FIFO缓冲区状态
0 (receiving direction)	0	没有接收到数据，或正在接收数据。 禁止从FIFO端口读取。

Table 29.23 Buffer status indicated in the BSTS flag (2 of 2)

ISEL or DIR	BSTS	FIFO buffer status
0 (receiving direction)	1	There is received data, or a zero-length packet is received. Reading from the FIFO port is allowed. When a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	Transmission is not complete. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	Transmission is complete. CPU write is allowed.

Table 29.24 Buffer status indicated in the INBUFM bit

DIR	INBUFM	FIFO buffer status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	Transmission is complete. There is no data waiting to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

29.3.8.2 FIFO buffer clearing

Table 29.25 shows the methods for clearing the FIFO buffer. The FIFO buffer can be cleared using the BCLR bit in the port control register, DnFIFOSEL.DCLRM, or the PIPEnCTR.ACLRM bit.

Single or double buffering can be selected for pipes 1 to 5 in the PIPECFG.DBLB bit.

Table 29.25 Buffer clearing methods

FIFO buffer clearing mode	Clearing the FIFO buffer on the CPU side	Mode for automatically clearing the FIFO buffer after reading the specified pipe data	Auto buffer clear mode for discarding all received packets
Register used	• CFIFOCTR • DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Bit used	BCLR	DCLRM	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid	1: Mode valid 0: Mode invalid

Auto buffer clear mode function

The USBHS discards all received data packets if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet is received, the ACK response is returned to the host controller. The auto buffer clear mode function can only be set in the FIFO buffer reading direction.

Setting the ACLRM bit to 1 and then to 0 clears the FIFO buffer of the selected pipe regardless of the access direction. An access cycle of at least 100 ns is required for the internal hardware sequence processing between ACLRM = 1 and ACLRM = 0.

29.3.8.3 FIFO port functions

Table 29.26 shows the settings for the FIFO port functions. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, set the BVAL flag in the port control register to end writing. To send a zero-length packet, use the BCLR bit to clear the buffer, and then set the BVAL flag to end writing.

In reading, reception of new packets is automatically enabled when all data is read. Data cannot be read when a zerolength packet is received (DTLN[11:0] = 0), so the buffer must be cleared with the BCLR bit. The length of the receive data can be confirmed in the DTLN[11:0] flags in the port control register.

Table 29.23 BSTS标志中指示的缓冲区状态（2个中的2个）

ISEL或DIR	BSTS	FIFO缓冲区状态
0 (receiving direction)	1	有接收数据，或接收到零长度数据包。 允许从FIFO端口读取。 当接收到零长度数据包时，无法读取，必须清除缓冲区。
1 (transmitting direction)	0	传输未完成。 禁止写入FIFO端口。
1 (transmitting direction)	1	传输完成。 允许CPU写入。

Table 29.24 INBUFM位中指示的缓冲区状态

DIR	INBUFM	FIFO缓冲区状态
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	传输完成。 没有等待传输的数据。
1 (transmitting direction)	1	FIFO端口已将数据写入缓冲区。 有数据要传输。

29.3.8.2 FIFO缓冲区清除

表29.25显示了清除FIFO缓冲区的方法。可以使用端口控制寄存器中的BCLR位、DnFIFOSEL.DCLRM或PIPEnCTR.ACLRM位清除FIFO缓冲区。

可以在PIPECFG.DBLB位中为管道1到5选择单缓冲或双缓冲。

Table 29.25 缓冲区清除方法

FIFO缓冲区清除模式	清除FIFO缓冲区 CPU端	自动清除模式 读取指定管道数据后的FIFO缓冲区	自动缓冲区清除模式，用于丢弃所有接收到的数据包
注册使用	• CFIFOCTR • DnFIFOCTR	DnFIFOSEL	PIPEnCTR
使用的位	BCLR	DCLRM	ACLRM
清算条件	通过写1清除	1：模式有效0 ：模式无效	1：模式有效0 ：模式无效

自动缓冲清除模式功能

如果PIPEnCTR.ACLRM位设置为1，USBHS将丢弃所有接收到的数据包。如果接收到正确的数据包，则向主机控制器返回ACK响应。自动缓冲区清除模式功能只能在FIFO缓冲区读取方向设置。

无论访问方向如何，将ACLRM位设置为1，然后设置为0都会清除所选管道的FIFO缓冲区。ACLRM=1和ACLRM=0之间的内部硬件序列处理需要至少100ns的访问周期。

29.3.8.3 先进先出端口功能

表29.26显示了FIFO端口功能的设置。在写访问中，在达到最大数据包大小之前写入数据会自动启用数据传输。要在达到最大数据包大小之前启用传输，请设置端口控制寄存器中的BVAL标志以结束写入。要发送零长度数据包，请使用BCLR位清除缓冲区，然后设置BVAL标志以结束写入。

在读取中，当所有数据被读取时，自动启用新数据包的接收。接收到零长度数据包时（DTLN[11:0]=0）无法读取数据，因此必须使用BCLR位清除缓冲区。接收数据的长度可以在端口控制寄存器中的DTLN[11:0]标志中确认。

Table 29.26 FIFO port function settings

Register name	Bit name	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	Selects DTLN[11:0] read mode
	REW	FIFO buffer rewind (re-read, rewrite)
	DCLRM	Automatically clears receive data for a specified pipe after the data is read (only for DnFIFO)
	DREQE	Enables DMA/DTC transfers (only for DnFIFO)
	MBW[1:0]	FIFO port access bit width
	BIGEND	Selects FIFO port endian
	ISEL	FIFO port access direction (only for DCP)
	CURPIPE[3:0]	Selects the current pipe
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	Ends writing to the FIFO buffer
	BCLR	Clears the FIFO buffer on the CPU side
	DTLN[11:0]	Checks the length of receive data

FIFO port selection

Table 29.27 shows the pipes that can be selected with the different FIFO ports. The pipe to be accessed must be selected in the CURPIPE[3:0] bits in the port selection register. After a pipe is selected, the software must check whether the written value can be correctly read from the CURPIPE[3:0] bits. (If the previous pipe number is read, it indicates that the USBHS is modifying the pipe.) Next, the software checks that the FRDY flag in the port control register is 1.

In addition, the software must specify the bus width to be accessed in the MBW[1:0] bits in the port selection register.

The FIFO buffer access direction conforms to the PIPECFG.DIR setting. For the DCP only, the ISEL bit in the port selection register determines the direction.

Table 29.27 FIFO port access by pipe

Pipe	Access Method	Port that can be used
DCP	CPU access	CFIFO port register
Pipes 1 to 9	CPU access	CFIFO port register D0FIFO/D1FIFO port register
	DMA/DTC access	D0FIFO/D1FIFO port register

REW bit

It is possible to temporarily stop access to a pipe being accessed, access a different pipe, and then continue processing for the first pipe again. The REW bit in the port selection register is used for this processing.

If a pipe is selected in the CURPIPE[3:0] bits in the port selection register with the REW bit set to 1, the pointer used for reading from and writing to the FIFO buffer is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with the REW bit set to 0, data can be read and written in continuation from the previous selection, without the pointer being reset.

To access the FIFO port, the software must check that the FRDY bit in the port control register is 1 after selecting a pipe.

29.3.8.4 DMA/DTC transfers (D0FIFO and D1FIFO ports)

Overview of DMA/DTC transfer

For pipes 1 to 9, the FIFO port can be accessed using the DMAC/DTC. When buffer access for the pipe targeted for DMA/DTC transfer is enabled, a DMA/DTC transfer request is issued.

Select the unit of transfer to the FIFO port in the DnFIFOSEL.MBW[1:0] bits, and select the pipe targeted for the DMA/DTC transfer in the DnFIFOSEL.CURPIPE[3:0] bits. Do not change the selected pipe during the DMA transfer.

Table 29.26 FIFO端口功能设置

注册名称	位名称	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	选择DTLN[11:0]读取模式
	REW	FIFO缓冲区倒带（重新读取、重写）
	DCLRM	读取数据后自动清除指定管道的接收数据（仅适用于DnFIFO）
	DREQE	启用DMADTC传输（仅适用于DnFIFO）
	MBW[1:0]	FIFO端口访问位宽
	BIGEND	选择FIFO端口字节序
	ISEL	FIFO端口访问方向（仅适用于DCP）
	CURPIPE[3:0]选择当前管道	
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	结束写入FIFO缓冲区
	BCLR	清除CPU端的FIFO缓冲区
	DTLN[11:0]	检查接收数据的长度

先进先出端口选择

表29.27显示了可以使用不同FIFO端口选择的管道。必须在端口选择寄存器的CURPIPE[3:0]位中选择要访问的管道。选择管道后，软件必须检查是否可以从CURPIPE[3:0]位正确读取写入的值。（如果读取到之前的管道号，则表明USBHS正在修改管道。）接下来，软件检查端口控制寄存器中的FRDY标志为1。

此外，软件必须在端口选择寄存器的MBW[1:0]位中指定要访问的总线宽度。

FIFO缓冲区访问方向符合PIPECFG.DIR设置。仅对于DCP，端口选择寄存器中的ISEL位决定方向。

Table 29.27 通过管道访问FIFO端口

Pipe	访问方法	可以使用的端口
DCP	CPU访问	CFIFO端口寄存器
管道1到9	CPU访问	CFIFO端口寄存器 D0FIFOD1FIFO端口寄存器
	DMADTC访问	D0FIFOD1FIFO端口寄存器

REW位

可以暂时停止对正在访问的管道的访问，访问不同的管道，然后再次继续处理第一个管道。端口选择寄存器中的REW位用于此处理。

如果在端口选择寄存器的CURPIPE[3:0]位中选择了一个管道，并且REW位设置为1，则用于读取和写入FIFO缓冲区的指针复位，可以进行读取或写入从第一个字节开始。如果在REW位设置为0的情况下选择了管道，则可以从先前的选择继续读取和写入数据，而无需重置指针。

要访问FIFO端口，软件必须在选择管道后检查端口控制寄存器中的FRDY位是否为1。

29.3.8.4 DMADTC传输（D0FIFO和D1FIFO端口）

DMADTC传输概述

对于管道1到9，可以使用DMACDTC访问FIFO端口。当对目标管道进行缓冲区访问时启用DMADTC传输，发出DMADTC传输请求。

在DnFIFOSEL.MBW[1:0]位中选择传输到FIFO端口的单位，并选择目标管道DnFIFOSEL.CURPIPE[3:0]位中的DMADTC传输。在DMA传输期间不要更改选定的管道。

DnFIFO auto clear mode (D0FIFO and D1FIFO port reading direction)

If 1 is set in the DnFIFOSEL.DCLRM bit, the USBHS automatically clears the FIFO buffer of the selected pipe when reading of data from the FIFO buffer is complete.

Table 29.28 shows the packet reception and FIFO buffer clearing processing by software for each of the different settings. As shown in the table, the buffer clearing conditions depend on the value set in the PIPECFG.BFRE bit. Using the DnFIFOSEL.DCLRM bit eliminates the need for the buffer to be cleared by software in any situation that requires buffer clearing. This enables DMA/DTC transfers without involving software.

The DnFIFO auto clear mode can only be set in the FIFO buffer reading direction.

Table 29.28 Packet reception and FIFO buffer clearing processing by software

	Register setting			
	DCLRM = 0		DCLRM = 1	
Buffer status when packet is received	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	No clearing required	No clearing required	No clearing required	No clearing required
Zero-length packet reception	Clearing required	Clearing required	No clearing required	No clearing required
Normal short packet reception	No clearing required	Clearing required	No clearing required	No clearing required
Transaction count end	No clearing required	Clearing required	No clearing required	No clearing required

29.3.8.5 Allocating the FIFO buffer

Figure 29.11 shows an example of a memory map of the FIFO buffer. The FIFO buffer is an area shared by the USBHS and the control CPU of the application. There are two situations for the FIFO buffer: (1) access rights are given to the application (CPU side), and (2) access rights are given to the USBHS (SIE side).

An independent area is set for the FIFO buffer for each pipe. A memory area is determined by the first block number and the number of blocks (specified in the BUFNMB[7:0] and BUFSIZE[4:0] bits in PIPEBUF), where 64 bytes is regarded as one block. When the continuous transfer mode is selected in the CNTMD bit in PIPECFG, set the BUFSIZE[4:0] bits to an integral multiple of the maximum packet size. When double buffering is selected in the DBLB bit in PIPECFG, twice the memory area specified in the BUFSIZE[4:0] bits in PIPEBUF is allocated to the same pipe.

Three FIFO ports are used to access (read data from and write data to) the FIFO buffer. Specify the number of the pipe to be allocated to the FIFO port in the CURPIPE[3:0] bits in C/DnFIFOSEL.

The FIFO buffer status of each pipe can be checked in the DCPCTR.BSTS, PIPEnCTR, and INBUFM bits. The FIFO port access rights can be checked in the FRDY flag in C/DnFIFOCTR.

DnFIFO自动清除模式（D0FIFO和D1FIFO端口读取方向）

如果DnFIFOSEL.DCLRM位设置为1，USBHS会在从FIFO缓冲区读取数据完成时自动清除所选管道的FIFO缓冲区。

表29.28显示了软件对每个不同设置的数据包接收和FIFO缓冲区清除处理。如表所示，缓冲区清除条件取决于PIPECFG.BFRE位中设置的值。使用

DnFIFOSEL.DCLRM位消除了在需要清除缓冲区的任何情况下通过软件清除缓冲区的需要。这可以在不涉及软件的情况下实现DMADTC传输。

DnFIFO自动清除模式只能设置在FIFO缓冲区读取方向。

Table 29.28 通过软件进行数据包接收和FIFO缓冲区清除处理

	注册设置			
	DCLRM = 0		DCLRM = 1	
收到数据包时的缓冲区状态	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
缓冲区已满	无需清算无需清算无需清算无需清算			
零长度数据包接收	需要清算	需要清算	无需清算无需清算	
正常短包接收	无需清算需要清算		无需清算无需清算	
交易计数结束	无需清算需要清算		无需清算无需清算	

29.3.8.5 分配FIFO缓冲区

图29.11显示了FIFO缓冲区的内存映射示例。FIFO缓冲区是由USBHS和应用程序的控制CPU共享的区域。FIFO缓冲区有两种情况：（1）访问权限给应用程序（CPU端），（2）访问权限给USBHS（SIE端）。

为每个管道的FIFO缓冲区设置一个独立的区域。一个内存区域由第一个块号和块数（在PIPEBUF中的BUFNMB[7:0]和BUFSIZE[4:0]位指定）确定，其中64个字节被视为一个块。在PIPECFG的CNTMD位中选择连续传输模式时，将BUFSIZE[4:0]位设置为最大数据包大小的整数倍。当在PIPECFG的DBLB位中选择双缓冲时，PIPEBUF中的BUFSIZE[4:0]位指定的内存区域的两倍将分配给同一管道。

三个FIFO端口用于访问（读取数据和写入数据）FIFO缓冲区。在CDnFIFOSEL的CURPIPE[3:0]位中指定要分配给FIFO端口的管道编号。

可以在DCPCTR.BSTS、PIPEnCTR和INBUFM位中检查每个管道的FIFO缓冲区状态。可以在CDnFIFOCTR中的FRDY标志中检查FIFO端口访问权限。

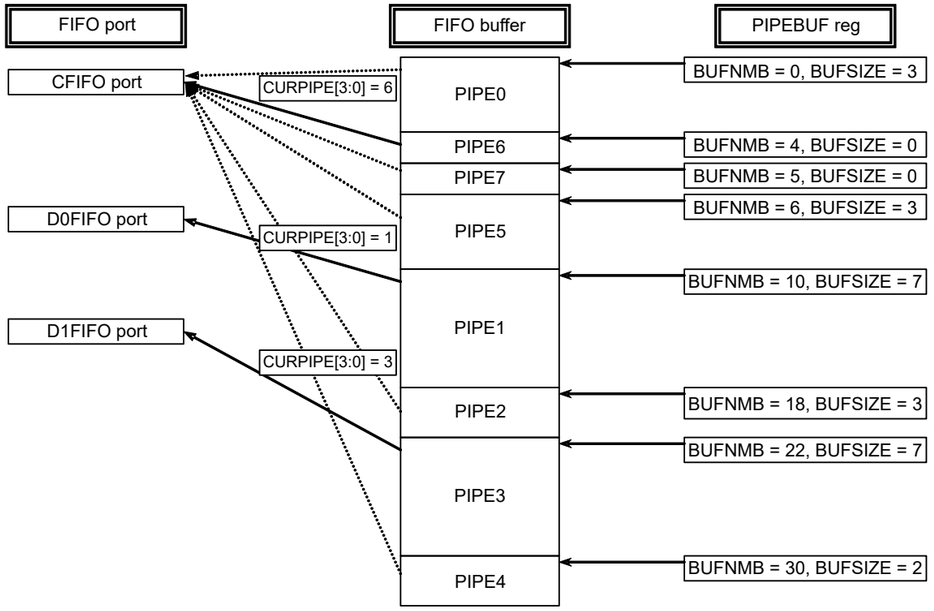

Figure 29.11 Example memory map of the FIFO buffer

29.3.9 Control Transfers Using the DCP

The Default Control Pipe (DCP) is used for data transfers in the control transfer data stage. The FIFO buffer of the DCP is a 64-byte single buffer with a fixed area for both control reads and control writes. The FIFO buffer can be accessed only through the CFIFO port.

29.3.9.1 Control transfers in host controller mode

Setup stage

The USBREQ, USBVAL, USBINDX, and USBLENG registers are used to transmit USB requests for setup transactions. Writing the setup packet data to the register and then writing 1 to the DCPCTR.SUREQ bit transmits the specified data for the setup transaction. On completion of the transaction, the SUREQ bit clears to 0. Do not change these USB request registers while SUREQ = 1.

When an attached function device is detected, the software must issue the first setup transaction for the device using this sequence with the DCPMAXP.DEVSEL[3:0] bits cleared to 0 and the DEVADD0.USBSPD[1:0] bits set appropriately.

When an attached function device is shifted to the Address state, the software must issue setup transactions using this sequence with the assigned USBAddress set in the DEVSEL[3:0] bits and the bits in DEVADDn (n = 0 to A) corresponding to the specified USBAddress set appropriately. For example, when PIPEMAXP.DEVSEL[3:0] = 0010b, make appropriate settings in DEVADD2. When PIPEMAXP.DEVSEL[3:0] = 0101b, make appropriate settings in DEVADD5.

When the setup transaction data is sent, an interrupt request is generated based on the response from the peripheral device (SIGN or SACK bit in INTSTS1). This interrupt request allows the software to check the setup transaction result.

The DATA0 data packet (USB request) for the setup transaction is always transmitted regardless of the status of the DCPCTR.SQMON flag.

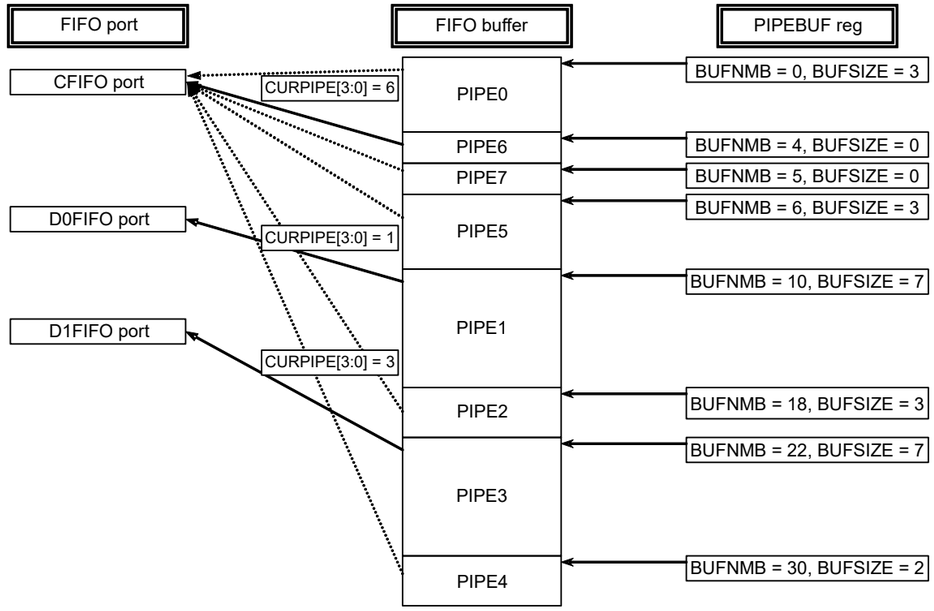

Figure 29.11 FIFO缓冲区的示例内存映射

29.3.9 使用DCP进行控制传输

默认控制管道(DCP)用于控制传输数据阶段的数据传输。DCP的FIFO缓冲区是一个64字节的单缓冲区，具有用于控制读取和控制写入的固定区域。FIFO缓冲区只能通过CFIFO端口访问。

29.3.9.1 主机控制器模式下的控制传输

设置阶段

USBREQ、USBVAL、USBINDX和USBLENG寄存器用于传输设置事务的USB请求。
将设置数据包数据写入寄存器，然后向DCPCTR.SUREQ位写入1，以传输设置事务的指定数据。事务完成后，SUREQ位清除为0。在SUREQ=1时不要更改这些USB请求寄存器。

当检测到连接的功能器件时，软件必须使用此序列为器件发出第一个设置事务，其中DCPMAXP.DEVSEL[3:0]位清零，DEVADD0.USBSPD[1:0]位适当设置。

当连接的功能器件转移到地址状态时，软件必须使用此序列发出设置事务，其中指定的USBAddress设置在DEVSEL[3:0]位和DEVADDn中的位（n=0到A）对应于指定的USBAddress设置得当。例如，当PIPEMAXP.DEVSEL[3:0]=0010b时，在DEVADD2中进行适当的设置。当PIPEMAXP.DEVSEL[3:0]=0101b时，在DEVADD5中进行适当的设置。

发送设置事务数据时，根据外围设备的响应（INTSTS1中的SIGN或SACK位）生成中断请求。该中断请求允许软件检查设置事务结果。

用于设置事务的DATA0数据包（USB请求）始终被传输，无论
DCPCTR.SQMON flag.

Data stage

The data stage is used to transfer data using the DCP FIFO buffer.

Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit. Specify the transfer direction in the DCPCFG.DIR bit.

For the first data packet of the data stage, the data PID must be transferred as DATA1. Set data PID to DATA1 in the DCPCTR.SQSET bit and set the PID[1:0] bits to 01b (BUF response). Completion of data transfer is detected using the BRDY or BEMP interrupt.

Data transfer of multiple packets is enabled in continuous transfer mode. However, when continuous transfer is specified in the receiving direction, the BRDY interrupt is not generated unless the buffer becomes full or a short packet is received (for 256 bytes or less, which is an integral multiple of the maximum packet size). If the transmit data size is an integral multiple of the maximum packet size, control the control write transfer through the software to transmit a zerolength packet last.

Status stage

The status stage is used for zero-length packet data transfers in the reverse direction of the data stage. As in the data stage, data is transfered using the DCP FIFO buffer. Transactions are executed using the same procedure as the data stage.

Data packets in the status stage must be transmitted and received with the data PID set to DATA1 using the DCPCTR.SQSET bit.

When a zero-length packet is received, check the receive-data length in the CFIFOCTR.DTLN[11:0] flags after a BRDY interrupt is generated, and then clear the FIFO buffer using the BCLR bit.

29.3.9.2 Control transfers in device controller mode

Setup stage

The USBHS returns an ACK response to a normal setup packet for the USBHS. The USBHS operates in the setup stage as follows:

On receiving a new setup packet, the USBHS sets the following bits:

- Sets the INTSTS0.VALID flag to 1
- Sets the DCPCTR.PID[1:0] bits to 00b (NAK response)
- Sets the DCPCTR.CCPL bit to 0

When the USBHS receives a data packet following a setup packet, it stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Before performing the response processing for a control transfer, set the VALID flag to 0. When the VALID flag = 1, the PID[1:0] bits cannot be set to 01b (BUF response), and the data stage cannot be terminated.

Using the VALID flag function, the USBHS can suspend a request being processed when it receives a new USB request during a control transfer and return a response to the latest request.

In addition, the USBHS automatically detects the direction bit (bmRequestType bit 8) and the request data length (wLength) in the received USB request. It distinguishes between control read transfers, control write transfers, and nodata control transfers, and it controls stage transitions. For an incorrect sequence, a sequence error occurs in the control transfer stage transition interrupt, and the interrupt is reported to the software. For a diagram of the stage control by the USBHS, see Figure 29.9.

Data stage

The DCP must be used to execute data transfers for received USB requests. Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit.

If the transfer data is larger than the size of the DCP FIFO buffer, execute the data transfer using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

In high-speed control write transfers, a NYET handshake response is returned based on the FIFO buffer status.

数据阶段

数据级用于使用DCPFIFO缓冲区传输数据。

在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。在DCPCFG.DIR位中指定传输方向。

对于数据阶段的第一个数据包，数据PID必须作为DATA1传输。将数据PID设置为DATA1 DCPCTR.SQSET位并将PID[1:0]位设置为01b（BUF响应）。使用检测到数据传输的完成 BRDY或BEMP中断。

在连续传输模式下启用多个数据包的数据传输。但是，当在接收方向指定连续传输时，除非缓冲区变满或接收到短数据包（256字节或更少，这是最大数据包大小的整数倍），否则不会产生BRDY中断。如果传输数据大小是最大数据包大小的整数倍，则通过软件控制控制写入传输，最后传输一个零长度数据包。

状态阶段

状态阶段用于在数据阶段的相反方向上进行零长度分组数据传输。与数据阶段一样，使用DCPFIFO缓冲区传输数据。事务使用与数据阶段相同的过程执行。

状态阶段的数据包必须在数据PID设置为DATA1的情况下使用 DCPCTR.SQSET bit.

当接收到零长度数据包时，在产生BRDY中断后检查CFIFOCTR.DTLN[11:0]标志中的接收数据长度，然后使用BCLR位清除FIFO缓冲区。

29.3.9.2 设备控制器模式下的控制传输

设置阶段

USBHS向USBHS的正常设置数据包返回ACK响应。USBHS在设置阶段运行如下：

在接收到新的设置数据包时，USBHS设置以下位：

●将INTSTS0.VALID标志设置为1

●将DCPCTR.PID[1:0]位设置为00b（NAK响应）

●将DCPCTR.CCPL位设置为0

当USBHS在设置包之后接收到数据包时，它会将USB请求参数存储在USBREQ中， USBVAL, USBINDX, and USBLENG.

在执行控制传输的响应处理之前，将VALID标志设置为0。当VALID标志=1时， PID[1:0]位不能设置为01b（BUF响应），并且不能终止数据阶段。

使用VALID标志功能，USBHS可以在控制传输期间接收到新的USB请求时暂停正在处理的请求，并返回对最新请求的响应。

此外，USBHS会自动检测接收到的USB请求中的方向位（bmRequestTypebit8）和请求数据长度（wLength）。它区分控制读取传输、控制写入传输和无数据控制传输，并控制阶段转换。对于不正确的序列，在控制转移阶段转换中断中发生序列错误，并将中断报告给软件。USBHS的舞台控制图见图29.9。

数据阶段

DCP必须用于执行接收到的USB请求的数据传输。在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。

如果传输数据大于DCPFIFO缓冲区的大小，则使用控制写传输的BRDY中断和控制读传输的BEMP中断执行数据传输。

在高速控制写入传输中，根据FIFO缓冲区状态返回NYET握手响应。

Status stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to 01b (BUF response).Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to 01b (BUF response).

After this setting is made, the USBHS automatically executes the status stage based on the data transfer direction determined at the setup stage. The status stage is executed as follows:

- For control read transfers:
  The USBHS receives a zero-length packet from the USB host and transmits an ACK response
- For control write transfer and no data control transfer:
  The USBHS transmits a zero-length packet and receives an ACK response from the USB host.

Control transfer auto response function

The USBHS automatically responds to a normal SET_ADDRESS request. If the SET_ADDRESS request contains any of the following errors, a response must be returned by software.

- When bmRequestType is not 00h: except control write transfer
- When wIndex is not 00h: request error
- When wLength is not 00h: except no data control transfer
- When wValue is larger than 7Fh: request error
- When PL1CTRL.DVSQ[3:0] flags are 0011b (Configured): control transfer of device state error

A response by the corresponding software is required to all requests other than SET_ADDRESS.

29.3.10 Bulk Transfers (Pipes 1 to 5)

The FIFO buffer usage (setting of single buffer/double buffer or continuous/discontinuous transfer mode) is configurable for bulk transfers. The FIFO buffer size can be set up to 2 KB. The USBHS manages the FIFO buffer state and automatically responds to the PING packet and the NYET handshake.

29.3.10.1 PING packet control in host controller mode

In the OUT direction, a PING packet is automatically transmitted by the USBHS. The USBHS starts communication in the transmitting direction beginning with the PING packet. When it receives an ACK handshake in response to the PING packet, the USBHS transmits an OUT packet. The USBHS returns to the PING transmission state on receiving a NAK or NYET response during an OUT transaction. The procedure is as follows:

Starting OUT data transmission

(1) Transmit PING packet
(2) Receive NAK handshake
(3) Transmit PING packet
(4) Receive ACK handshake
(5) Transmit OUT data packet
(6) Receive ACK handshake
(7) Transmit OUT data packet
⋮
(8) Return to (1) on receiving a NAK/NYET handshake

The USBHS returns to the PING packet transmission state when a hardware reset is issued, the NYET or NAK handshake is received, the sequence toggle bit is cleared (SQCLR), or the buffer clear bit (ACLRM) is set.

29.3.10.2 NYET handshake control in device controller mode

Table 29.29 lists responses to received tokens during bulk and control transfers. The USBHS returns a NYET response when an available area for only one packet is left in the FIFO buffer when the USBHS has received an OUT token during a bulk or control transfer. When the USBHS receives a short packet, however, it returns an ACK response instead of NYET even when this condition occurs.

状态阶段

通过将DCPCTR.CCPL位设置为1而将DCPCTR.PID[1:0]位设置为01b（BUF响应）来终止控制传输。通过在DCPCTR时将DCPCTR.CCPL位设置为1来终止控制传输。PID[1:0]位设置为01b（BUF响应）。

完成此设置后，USBHS根据设置阶段确定的数据传输方向自动执行状态阶段。状态阶段执行如下：

- 对于控制读取传输：
  USBHS接收来自USB主机的零长度数据包并发送ACK响应
- 对于控制写传输和无数据控制传输：
  USBHS发送一个长度为零的数据包并接收来自USB主机的ACK响应。

控制转移自动响应功能

USBHS自动响应正常的SET_ADDRESS请求。如果SET_ADDRESS请求包含以下任何错误，则必须由软件返回响应。

- bmRequestType不为00h时：控制写入传输除外
- wIndex不为00h时：请求错误
- wLength不为00h时：无数据控制传输除外
- wValue大于7Fh时：请求错误
- 当PL1CTRL.DVSQ[3:0]标志为0011b（已配置）时：设备状态错误的控制传输

除SET_ADDRESS之外的所有请求都需要相应软件的响应。

29.3.10 批量传输（管道1到5）

FIFO缓冲区使用（设置单缓冲区双缓冲区或连续不连续传输模式）可配置为批量传输。FIFO缓冲区大小可设置为2 KB。USBHS管理FIFO缓冲区状态并自动响应PING数据包和NYET握手。

29.3.10.1 主机控制器模式下的PING包控制

在OUT方向，USBHS自动发送一个PING数据包。USBHS从PING数据包开始在传输方向上开始通信。当它接收到响应PING数据包的ACK握手时，USBHS发送一个OUT数据包。USBHS在OUT事务期间收到NAK或NYET响应后返回PING传输状态。程序如下：

开始OUT数据传输

(1) 发送PING数据包接收NA
(2) K握手发送PING数据包
(3)
(4) 接收ACK握手发送OUT数
(5) 据包接收ACK握手发送OU
(6) T数据包
(7)
⋮
(8) 收到NAKNYET握手后返回(1)

当发出硬件复位、接收到NYET或NAK握手、清除序列切换位(SQCLR)或设置缓冲区清除位(ACLRM)时，USBHS将返回PING数据包传输状态。

29.3.10.2 设备控制器模式下的NYET握手控制

表29.29列出了在批量和控制传输期间对接收到的令牌的响应。当USBHS在批量或控制传输期间接收到OUT令牌时，如果FIFO缓冲区中只剩下一个数据包的可用区域，则USBHS将返回NYET响应。但是，当USBHS接收到一个短数据包时，即使发生这种情况，它也会返回ACK响应而不是NYET。

Table 29.29 Responses to received tokens

PID[1:0] bit setting	FIFO buffer state	Received token	Response	Note
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY	OUT/PING	ACK	When OUT token is received, data packet is received.*1
	RCV-BRDY	OUT	NYET	Data packet is received*2
	RCV-BRDY	OUT (Short)	ACK	Data packet is received*2
	RCV-BRDY	PING	ACK	*2
	RCV-NRDY	OUT/PING	NAK	—
	TRN-BRDY	IN	DATA0/1	Data packet is transmitted
	TRN-NRDY	IN	NAK	—

Note 1. RCV-BRDY: An available area for two packets is left in the FIFO buffer when an OUT token or a PING token is received.
Note 2. RCV-BRDY: An available area for only one packet is left in the FIFO buffer when an OUT token is received.
RCV-NRDY: No available area is left in the FIFO buffer when a PING token is received.
TRN-BRDY: The FIFO buffer contains transmit data when an IN token is received.
TRN-NRDY: The FIFO buffer contains no transmit data when an IN token is received.

29.3.11 Interrupt Transfers (Pipes 6 to 9)

In device controller mode, the USBHS performs interrupt transfers based on the timing dictated by the host controller. In the interrupt transfer, the USBHS ignores PING packets (no response) and does not transmit the NYET handshake, but returns an ACK, NAK, or STALL response.

In host controller mode, the software can set the timing for issuing tokens using the interval counter. The USBHS does not issue a PING token but issues an OUT token, including for transfers in the OUT direction.

The USBHS does not support high-bandwidth interrupt transfers.

29.3.11.1 Interval counter for interrupt transfers in host controller mode

Specify the transaction interval for interrupt transfers in the PIPEPERI.IITV[2:0] bits. The USBHS issues interrupt transfer tokens based on this interval.

(1) Initializing the counter

The USBHS initializes the interval counter under the following conditions:

- Power-on reset:
  This initializes the IITV[2:0] bits
- FIFO buffer initialization using the PIPEnCTR.ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value. Setting the PIPEnCTR.ACLRM bit to 0 starts counting from the value set in IITV[2:0].

(2) Operation when tokens cannot be transmitted or received even on token generation

No token is generated in the following cases even at token generation time. In these cases, the USBHS tries to execute the transaction in the next interval.

- When the PID[1:0] bits are set to NAK or STALL
- When the FIFO buffer is full at token transmit time in the receiving (IN) direction
- When there is no data to be transmitted in the FIFO buffer at token transmit time in the transmitting (OUT) direction

29.3.12 Isochronous Transfers (Pipes 1 and 2)

The USBHS does not support high-bandwidth isochronous transfers but provides the following functions for isochronous transfers:

Table 29.29 对收到的令牌的响应

PID[1:0]位设置	FIFO缓冲区状态	接收到的令牌	响应	Note
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY	OUT/PING	ACK	当接收到OUT令牌时，接收到数据包。*1
	RCV-BRDY	OUT	NYET	接收数据包*2
	RCV-BRDY	OUT (Short)	ACK	接收数据包*2
	RCV-BRDY	PING	ACK	*2
	RCV-NRDY	OUT/PING	NAK	—
	TRN-BRDY	IN	DATA0/1	传输数据包
	TRN-NRDY	IN	NAK	—

注1.RCV-BRDY：当接收到OUT令牌或PING令牌时，两个数据包的可用区域留在FIFO缓冲区中。
注2.RCV-BRDY：当接收到OUT令牌时，FIFO缓冲区中只剩下一个可用于一个数据包的区域。
RCV-NRDY：接收到PING令牌时，FIFO缓冲区中没有可用区域。
TRN-BRDY：接收到IN令牌时，FIFO缓冲区包含发送数据。
TRN-NRDY：接收到IN令牌时，FIFO缓冲区不包含发送数据。

29.3.11 中断传输（管道6到9）

在设备控制器模式下，USBHS根据主机控制器规定的时序执行中断传输。在中断传输中，USBHS忽略PING数据包（无响应）并且不发送NYET握手，而是返回ACK、NAK或STALL响应。

在主机控制器模式下，软件可以使用间隔计数器设置发布令牌的时间。USBHS不会发出PING令牌，但会发出OUT令牌，包括用于OUT方向的传输。

USBHS不支持高带宽中断传输。

29.3.11.1 主机控制器模式下中断传输的间隔计数器

在PIPEPERI.IITV[2:0]位中指定中断传输的事务间隔。USBHS基于此间隔发出中断传输令牌。

(1) 初始化计数器

USBHS在以下条件下初始化间隔计数器：

- Power-on reset:
  这将初始化IITV[2:0]位

●使用PIPEnCTR.ACLRM位初始化FIFO缓冲区：
这不会初始化IITV[2:0]位，但会初始化计数值。将PIPEnCTR.ACLRM位设置为0从IITV[2:0]中设置的值开始计数。

(2) 即使在生成令牌时也无法发送或接收令牌时的操作

在以下情况下，即使在生成令牌时也不会生成令牌。在这些情况下，USBHS尝试在下一个时间间隔执行事务。

●当PID[1:0]位设置为NAK或STALL时
●接收(IN)方向的令牌发送时FIFO缓冲区已满时
●在发送（OUT）方向的令牌发送时间，FIFO缓冲区中没有要发送的数据时

29.3.12 同步传输（管道1和2）

USBHS不支持高带宽同步传输，但为同步传输提供以下功能：

- Notification of isochronous transfer error
- Interval counter (specified in the PIPEPERI.IITV[2:0] bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (specified in the PIPEPERI.IFIS bit)
- SOF pulse output function

29.3.12.1 Error detection in isochronous transfers

The USBHS provides a function for detecting the errors described in this section, so that when errors occur in isochronous transfers, they can be controlled by software. Table 29.30 and Table 29.31 show the priority order for errors detected by the USBHS and the associated interrupts.

PID errors

- The PID value of the received packet is invalid

CRC errors and bit stuffing errors

- A CRC error is found in a received packet or the bit stuffing is illegal

Maximum packet size exceeded

- The data size of the received packet exceeds the specified maximum packet size

Overrun and underrun errors

In host controller mode:

- The FIFO buffer is full at token transmit time in the IN (receiving) direction
- There is no data to be sent in the FIFO buffer at token transmit time in the OUT (transmitting) direction

In device controller mode:

- There is no data to be sent in the FIFO buffer at token receive time in the IN (transmitting) direction
- The FIFO buffer is full at token receive time in the OUT (receiving) direction

Interval error

In device controller mode, the following cases are treated as an interval error:

- Failure to receive an IN token in the interval frame during an isochronous IN transfer
- Failure to receive an OUT token in the interval frame during an isochronous OUT transfer

Table 29.30 Error detection for token transmission and reception

Detection priority	Error type	Interrupt generated at error detection and status
1	PID error	No interrupts are generated in either host or device controller mode. (Ignored as a corrupted packet.)
2	CRC or bit stuffing error	No interrupts are generated in either host or device controller mode. (Ignored as a corrupted packet.)
3	Overrun or underrun error	An NRDY interrupt is generated to set the OVRN flag to 1 in both host and device controller modes. In device controller mode, a zero-length packet is transmitted in response to an IN token. No data packets are received in response to the OUT token.
4	Interval error	An NRDY interrupt is generated in device controller mode. No interrupt is generated in host controller mode.

Table 29.31 Error detection for data packet reception (1 of 2)

Detection priority	Error type	Interrupt generated at error detection and status
1	PID error	No interrupt is generated. (Ignored as a corrupted packet.)

●同步传输错误通知
●间隔计数器（在PIPEPERI.IITV[2:0]位中指定）
●同步IN传输数据设置控制（IDLY功能）
●同步IN传输缓冲区刷新功能（在PIPEPERI.IFIS位中指定）
●SOF脉冲输出功能

29.3.12.1 同步传输中的错误检测

USBHS提供了检测本节描述的错误的功能，因此当同步传输中出现错误时，可以通过软件进行控制。表29.30和表29.31显示了USBHS检测到的错误和相关中断的优先级顺序。

PID错误

●接收报文的PID值无效

CRC错误和位填充错误

●收到的报文发现CRC错误或比特填充不合法

超出最大数据包大小

●接收包的数据大小超过了指定的最大包大小

溢出和欠载错误

在主机控制器模式下：

●在IN（接收）方向发送令牌时，FIFO缓冲区已满
●在OUT（发送）方向的令牌发送时间，FIFO缓冲区中没有要发送的数据

在设备控制器模式下：

●在IN（发送）方向的令牌接收时间，FIFO缓冲区中没有要发送的数据
●在OUT（接收）方向的令牌接收时间，FIFO缓冲区已满

间隔误差

在设备控制器模式下，以下情况被视为间隔错误：

●等时IN传输期间在间隔帧中接收IN令牌失败
●在等时OUT传输期间未能在间隔帧中接收到OUT令牌

Table 29.30 令牌发送和接收的错误检测

检测优先级	错误类型	错误检测和状态产生的中断
1	PID错误	在主机或设备控制器模式下都不会产生中断。（作为损坏的数据包被忽略。）
2	CRC或位填充错误	在主机或设备控制器模式下都不会产生中断。（作为损坏的数据包被忽略。）
3	溢出或欠载错误	在主机和设备控制器模式下，都会产生一个NRDY中断来将OVRN标志设置为1。在设备控制器模式下，发送一个零长度数据包以响应IN令牌。 没有接收到响应OUT令牌的数据包。
4	间隔误差	在设备控制器模式下会产生一个NRDY中断。在主机控制器模式下不产生中断。

Table 29.31 数据包接收错误检测(1of2)

检测优先级	错误类型	错误检测和状态产生的中断
1	PID错误	不产生中断。（作为损坏的数据包被忽略。）

Table 29.31 Error detection for data packet reception (2 of 2)

Detection priority	Error type	Interrupt generated at error detection and status
2	CRC or bit stuffing error	An NRDY interrupt is generated and the FRMNUM.CRCE bit sets to 1 in both host and device controller modes.
3	Maximum packet size exceeded error	A BEMP interrupt is generated and the PID[1:0] bits set to STALL in both host and device controller modes.

29.3.12.2 DATA PID

The USBHS does not support high-bandwidth transfers. In device controller mode, the USBHS responds as follows to a received PID:

IN direction

- DATA0: Transmitted as data packet PID
- DATA1: Not transmitted
- DATA2: Not transmitted
- mDATA: Not transmitted

OUT direction (full-speed operation)

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Packets ignored
- mDATA: Packets ignored

OUT direction (high-speed operation)

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Received normally as data packet PID
- mDATA: Received normally as data packet PID

29.3.12.3 Interval counter

The isochronous transfer interval can be set in the PIPEPERI.IITV[2:0] bits. In device controller mode, the interval counter enables functions as shown in Table 29.32. In host controller mode, the USBHS generates the token issuance timing, and the interval counter operation is the same as that for interrupt transfers.

Table 29.32 Interval counter functions in device controller mode

Transfer direction	Function	Conditions for detection
IN	Transmit buffer flush	Failure to receive an IN token successfully in the interval frame during an isochronous IN transfer
OUT	Notification of no reception of token	Failure to receive an OUT token successfully in the interval frame during an isochronous OUT transfer

The interval count is performed when an SOF is received or for complemented SOFs, so the isochronism can be maintained even if an SOF is corrupt. The frame interval can be set to 2IITV (μ) frames.

(1) Counter initialization in device controller mode

The USBHS initializes the interval counter under the following conditions:

- Power-on reset:
  This initializes the PIPEPERI.IITV[2:0] bits
- FIFO buffer initialization using the ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value.

Table 29.31 数据包接收错误检测(2of2)

检测优先级	错误类型	错误检测和状态产生的中断
2	CRC或位填充错误	在主机和设备控制器模式下，都会产生一个NRDY中断并且FRMNUM.CRCE位设置为1。
3	超出最大数据包大小错误	在主机和设备控制器模式下，都会产生BEMP中断并且PID[1:0]位设置为STALL。

29.3.12.2 数据PID

USBHS不支持高带宽传输。在设备控制器模式下，USBHS对接收到的PID做出如下响应：

在方向

●DATA0：作为数据包PID发送
●DATA1：未发送
●DATA2：未传输
●mDATA：不传输

OUT方向（全速运行）

●DATA0：作为数据包PID正常接收
●DATA1：作为数据包PID正常接收
●DATA2：忽略的数据包
●mDATA：忽略的数据包

OUT方向（高速运转）

●DATA0：作为数据包PID正常接收
●DATA1：作为数据包PID正常接收
●DATA2：作为数据包PID正常接收
●mDATA：作为数据包PID正常接收

29.3.12.3 间隔计数器

同步传输间隔可以在PIPEPERI.IITV[2:0]位中设置。在设备控制器模式下，间隔计数器启用表29.32中所示的功能。在主机控制器模式下，USBHS产生令牌发布时序，间隔计数器操作与中断传输相同。

Table 29.32 设备控制器模式下的间隔计数器功能

转移方向	Function	检测条件
IN	发送缓冲区刷新	在等时IN传输期间未能在间隔帧中成功接收IN令牌
OUT	未收到令牌的通知	在等时OUT传输期间未能在间隔帧中成功接收OUT令牌

间隔计数是在接收到SOF时执行的，或者是针对补充的SOF执行的，因此即使SOF损坏也可以保持等时性。帧间隔可以设置为2IITV(μ)帧。

(1) 设备控制器模式下的计数器初始化

USBHS在以下条件下初始化间隔计数器：

- Power-on reset:
  这将初始化PIPEPERI.IITV[2:0]位
●使用ACLRM位初始化FIFO缓冲区：
  这不会初始化IITV[2:0]位，但会初始化计数值。

After the interval counter is initialized, the interval count starts under either of the following conditions when a packet is transferred successfully:

- An SOF is received after data is transmitted in response to an IN token, with the PID[1:0] bits set to 01b (BUF response)
- An SOF is received after data is received in response to an OUT token, with PID[1:0] bits set to 01b (BUF response)

The interval counter is not initialized under the following conditions:

- When the PID[1:0] bits are set to NAK or STALL
  This does not stop the interval timer. The USBHS attempts the transaction in the next interval.
- USB bus reset and USB suspension
  This does not initialize the IITV[2:0] bits. When an SOF is received, the interval counter starts counting from the value set before SOF was received.

(2) Interval counting and transfer control in host controller mode

The USBHS controls the interval between token issuance operations based on the PIPEPERI.IITV[2:0] bit settings. Specifically, the USBHS issues a token for a selected pipe once every 2IITV frames.

The USBHS starts counting the token issuance interval at the frame following the frame in which the PID[1:0] bits are set to 01b (BUF response) by software.

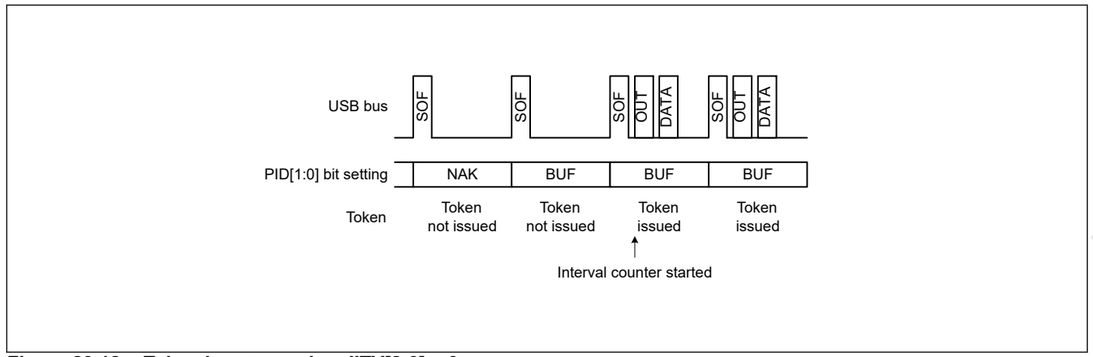

Figure 29.12 Token issuance when IITV[2:0] = 0

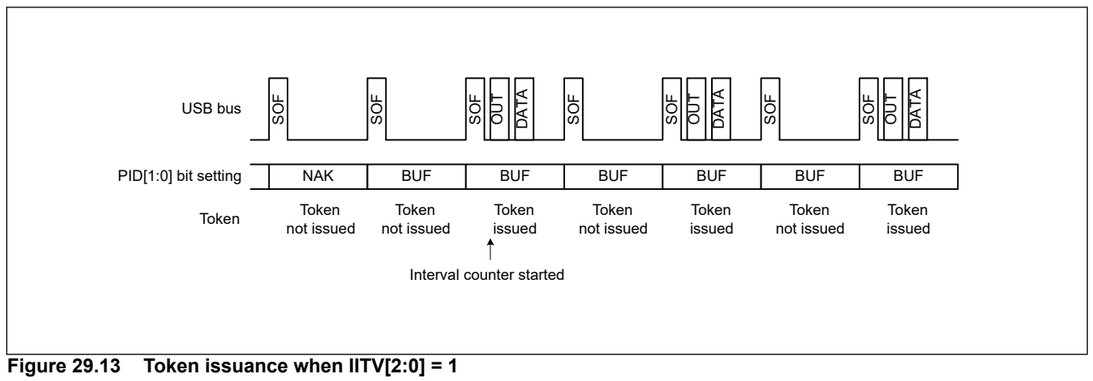

Figure 29.13 Token issuance when IITV[2:0] = 1

When the selected pipe is set for isochronous transfers, the USBHS carries out the following operation in addition to controlling the token issuance interval. The USBHS issues a token even when the NRDY interrupt generation condition is satisfied.

间隔计数器初始化后，当数据包传输成功时，间隔计数在以下任一条件下开始：

●在发送数据以响应IN令牌后收到SOF，PID[1:0]位设置为01b（BUF响应）

●接收到响应OUT令牌的数据后接收SOF，PID[1:0]位设置为01b（BUF响应）

间隔计数器在以下情况下不会初始化：

●当PID[1:0]位设置为NAK或STALL时
这不会停止间隔计时器。USBHS在下一个时间间隔尝试事务。

●USB总线复位和USB挂起
这不会初始化IITV[2:0]位。当接收到SOF时，间隔计数器从接收到SOF之前设置的值开始计数。

(2) 主机控制器模式下的间隔计数和传输控制

USBHS根据PIPEPERI.IITV[2:0]位设置控制令牌发布操作之间的间隔。
具体来说，USBHS每2IITV帧为选定管道发布一次令牌。

USBHS在软件将PID[1:0]位设置为01b（BUF响应）的帧之后的帧开始计算令牌发布间隔。

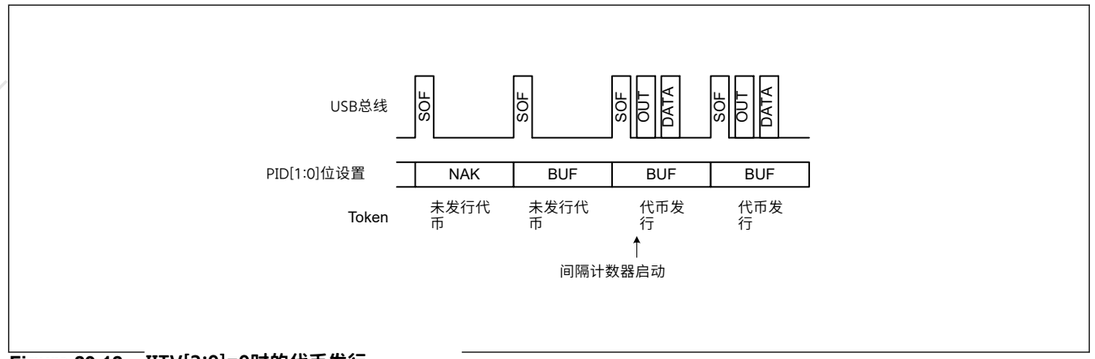

Figure 29.12 IITV[2:0]=0时的代币发行

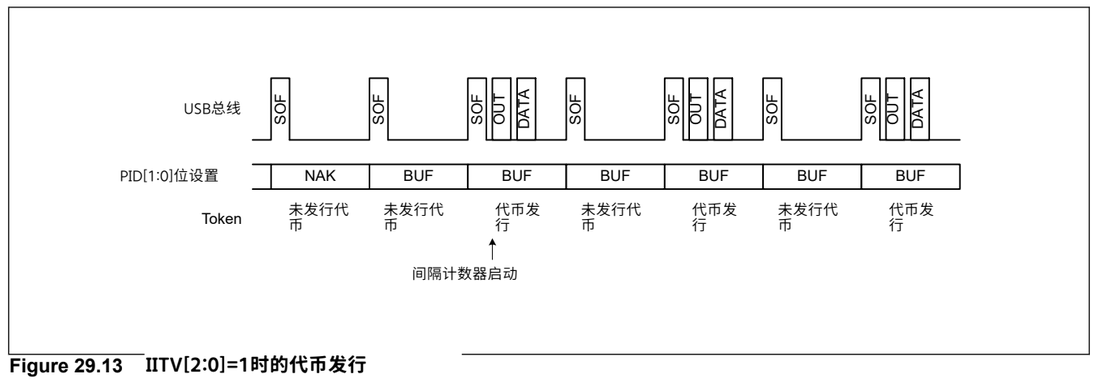

Figure 29.13 IITV[2:0]=1时的代币发行

当所选管道设置为同步传输时，USBHS除了控制令牌发布间隔外，还会执行以下操作。即使满足NRDY中断产生条件，USBHS也会发出一个令牌。

When the selected pipe is for isochronous IN transfers

The USBHS generates an NRDY interrupt when the USBHS issues an IN token but does not receive a packet successfully from a peripheral device (no response or packet error).

When the selected pipe is for isochronous OUT transfers

The USBHS sets the OVRN flag to 1, generating an NRDY interrupt and transmitting a zero-length packet, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer, because the CPU or DMA/DTC is too slow in writing data to the FIFO buffer.

The token issuance interval is reset on any of the following conditions:

- When the MCU is reset
  This initializes the IITV[2:0] bits
- When the PIPEnCTR.ACLRM bit is set to 1 by software

(3) Interval counting and transfer control in device controller mode

When the selected pipe is for isochronous OUT transfers

The USBHS generates an NRDY interrupt when it fails to receive a data packet within the interval set in the PIPEPERI.IITV[2:0] bits.

The USBHS also generates an NRDY interrupt when it fails to receive data because of a CRC error or other errors contained in the data packet or because of the FIFO buffer is full.

The NRDY interrupt is generated on SOF packet reception. Even if the SOF packet is corrupted, internal complementation allows the interrupt to be generated when the SOF packet is received. However, when the IITV[2:0] bits are set to a value other than 0, the USBHS generates an NRDY interrupt on receiving an SOF packet for every interval after interval counting starts.

When the PID[1:0] bits are set to 00b (NAK response) by software after starting the interval timer, the USBHS does not generate an NRDY interrupt on receiving an SOF packet.

The timing for starting interval counting depend on the IITV[2:0] setting as follows:

- When the IITV[2:0] bits = 0:
  The interval counting starts when the PID[1:0] bits of the selected pipe are changed to BUF
- When the IITV[2:0] bits ≠ 0:
  The interval counting starts on completion of successful reception of the first data packet after the PID[1:0] bits for the selected pipe are changed to 01b (BUF response)

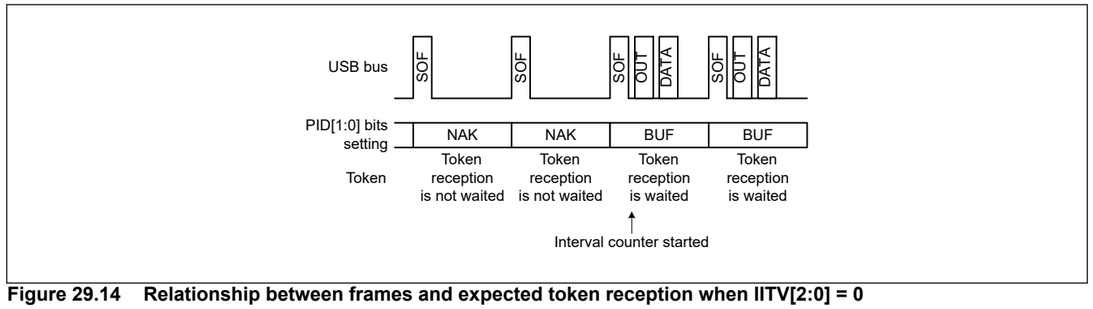

Figure 29.14 Relationship between frames and expected token reception when IITV[2:0] = 0

当所选管道用于同步IN传输时

当USBHS发出IN令牌但未成功接收到来自外围设备的数据包（无响应或数据包错误）时，USBHS生成NRDY中断。

当所选管道用于同步OUT传输时

USBHS将OVRN标志设置为1，产生一个NRDY中断并发送一个长度为零的数据包，当发出OUT令牌的时间到来而FIFO缓冲区中没有要发送的数据时，因为CPU或DMADTC是将数据写入FIFO缓冲区太慢。

令牌发行间隔在以下任何条件下重置：

- ●MCU复位时
  这将初始化IITV[2:0]位
- ●PIPEnCTR.ACLRM位由软件设置为1时

(3) 设备控制器模式下的间隔计数和传输控制

当所选管道用于同步OUT传输时

当USBHS在设置的时间间隔内未能接收到数据包时，会产生一个NRDY中断。
PIPEPERI.IITV[2:0] bits.

当由于数据包中包含的CRC错误或其他错误或由于FIFO缓冲区已满而无法接收数据时，USBHS也会产生NRDY中断。

NRDY中断在SOF数据包接收时产生。即使SOF数据包损坏，内部补码也允许在接收到SOF数据包时产生中断。但是，当IITV[2:0]位设置为0以外的值时，USBHS会在间隔计数开始后的每个间隔接收到SOF数据包时产生NRDY中断。

当PID[1:0]位在启动间隔定时器后由软件设置为00b（NAK响应）时，USBHS在接收到SOF数据包时不会产生NRDY中断。

开始间隔计数的时间取决于IITV[2:0]设置，如下所示：

- ●当IITV[2:0]位=0时：
  当所选管道的PID[1:0]位更改为BUF时，间隔计数开始
- ●当IITV[2:0]位≠0时：
  在所选管道的PID[1:0]位更改为01b（BUF响应）后，第一个数据包的成功接收完成后，间隔计数开始

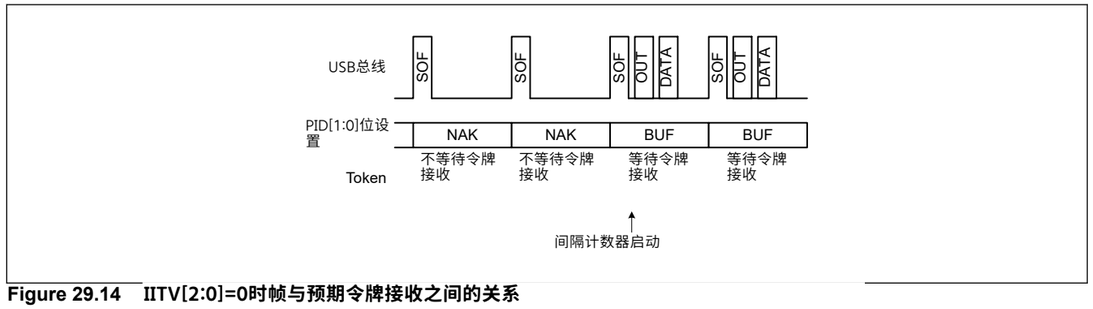

Figure 29.14 IITV[2:0]=0时帧与预期令牌接收之间的关系

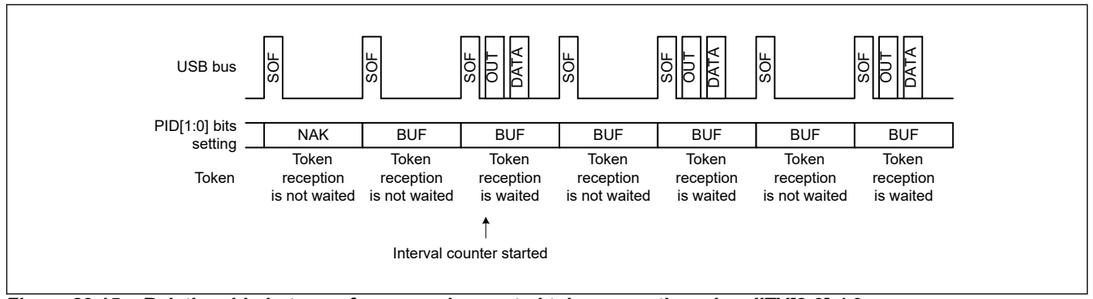

Figure 29.15 Relationship between frames and expected token reception when IITV[2:0] ≠ 0

When the selected pipe is for isochronous IN transfers

The PIPEPERI.IFIS bit must be 1 for this use case. When the IFIS bit is cleared to 0, the USBHS transmits a data packet in response to a received IN token, regardless of the PIPEPERI.IITV[2:0] setting.

When IFIS is 1 and there is data to be transmitted in the FIFO buffer, the USBHS clears the FIFO buffer when it fails to receive an IN token in the frame at the interval set in the IITV[2:0] bits.

The USBHS also clears the FIFO buffer when it fails to receive an IN token successfully because of a bus error, such as a CRC error, contained in the IN token.

The FIFO buffer is cleared on SOF packet reception. Even if the SOF packet is corrupted, the internal complementation allows the FIFO buffer to be cleared when the SOF packet is received.

The timing to start interval counting depends on the IITV[2:0] setting, as with OUT transfers.

The interval is counted on any of the following conditions in device controller mode:

- When a hardware reset is applied to the USBHS (which also sets the IITV[2:0] bits to 000b)
- When the PIPEnCTR.ACLRM bit is set to 1 by software
- When the USBHS detects a USB bus reset

(4) Transmit data setup for isochronous transfers in device controller mode

With isochronous data transmission using the USBHS in device controller mode, after data is written to the FIFO buffer, a data packet can be transmitted in the first frame after the SOF packet is detected. This isochronous transfer transmit data setup function can identify the frame that started transmission.

When the double buffering is used, transmission is only enabled for the buffer in which data writing was completed first, even after the data write to both buffers is complete. Accordingly, even if multiple IN tokens are received, only the one packet of FIFO buffer data is transmitted.

When the FIFO buffer is ready to transmit data when an IN token is received, the data is transferred and a normal response is returned. However, if the FIFO buffer cannot transmit data, a zero-length packet is transmitted and an underrun error occurs.

Figure 29.16 shows an example of transmission using the isochronous transfer transmit data setup function when the IITV[2:0] bits are set to 0 (every frame).

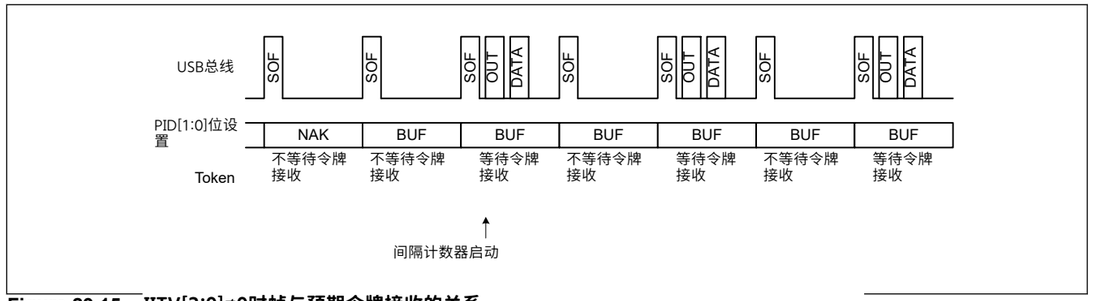

Figure 29.15 IITV[2:0]≠0时帧与预期令牌接收的关系

当所选管道用于同步IN传输时

对于此用例，PIPEPERI.IFIS位必须为1。当IFIS位清0时，USBHS发送数据包以响应接收到的IN令牌，无论PIPEPERI.IITV[2:0]设置如何。

当IFIS为1且FIFO缓冲区中有数据要发送时，USBHS会在其未能按照IITV[2:0]位设置的时间间隔接收帧中的IN令牌时清除FIFO缓冲区。

当USBHS由于总线错误（例如
CRC错误，包含在IN令牌中。

FIFO缓冲区在SOF数据包接收时被清除。即使SOF数据包损坏，内部补码也允许在接收到SOF数据包时清除FIFO缓冲区。

开始间隔计数的时间取决于IITV[2:0]设置，与OUT传输一样。

在设备控制器模式下，根据以下任何条件计算间隔：

●当对USBHS应用硬件复位时（也将IITV[2:0]位设置为000b）

●PIPEnCTR.ACLRM位由软件设置为1时

●当USBHS检测到USB总线复位时

(4) 设备控制器模式下同步传输的传输数据设置

在设备控制器模式下使用USBHS进行等时数据传输，数据写入FIFO缓冲区后，可在检测到SOF包后的第一帧发送数据包。此同步传输传输数据设置功能可以识别开始传输的帧。

当使用双缓冲时，即使在两个缓冲区的数据写入都完成之后，也只对首先完成数据写入的缓冲区启用传输。因此，即使接收到多个IN令牌，也仅发送一包FIFO缓冲器数据。

当接收到IN令牌时，当FIFO缓冲区准备好传输数据时，将传输数据并返回正常响应。但是，如果FIFO缓冲区无法传输数据，则会传输零长度数据包并发生欠载错误。

图29.16显示了使用同步传输传输数据设置功能的传输示例，当
IITV[2:0]位设置为0（每帧）。

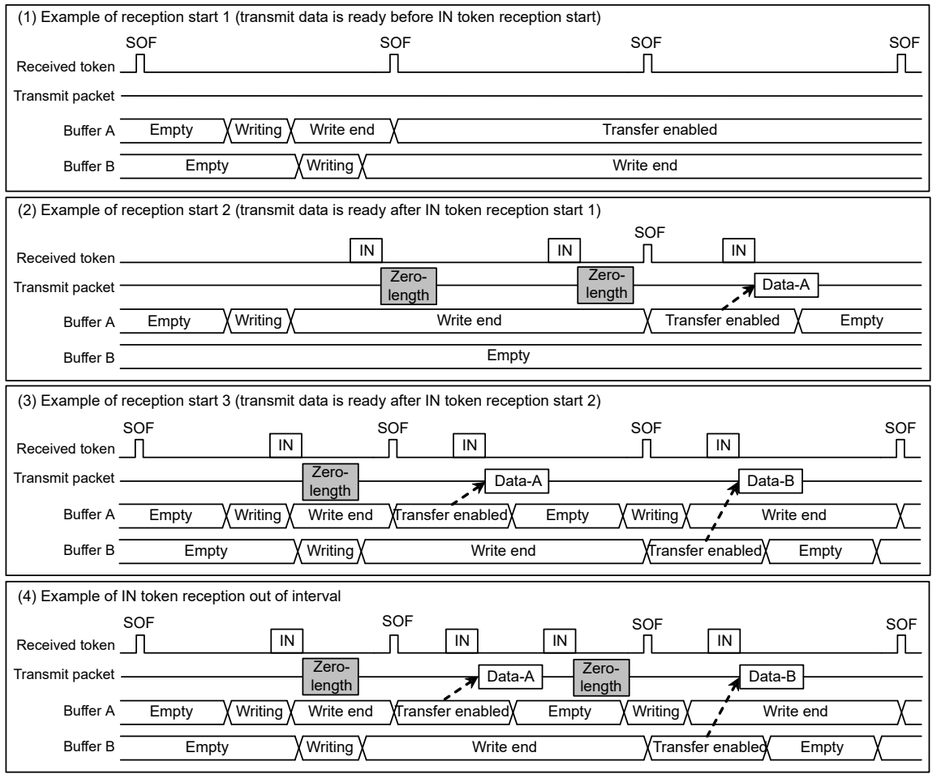

Figure 29.16 Example data setup operation

(5) Isochronous transfer transmit buffer flush in device controller mode

In device controller mode during isochronous data transmission, if the USBHS receives an SOF packet for the next frame without receiving an IN token in the interval frame, it operates as if the IN token is corrupt and clears the buffer that is enabled for transmission, putting that buffer in the writing enabled state.

When double buffering is used and writing to both buffers is complete, the cleared FIFO buffer is assumed to be the one where the data was transmitted in the interval frame, and transmission is enabled for the FIFO buffer that was not cleared on SOF packet reception.

The timing of the buffer flush function depends on the PIPEPERI.IITV[2:0] setting as follows:

- When IITV[2:0] = 0:
  The buffer flush operation starts from the first frame after the pipe is enabled
- When IITV[2:0] ≠ 0:
  The buffer flush operation starts after the first normal transaction

Figure 29.17 shows an example buffer flush. When an unanticipated token is received before the interval frame, the USBHS sends the write data or a zero-length packet as an underrun error, depending on the data setup status.

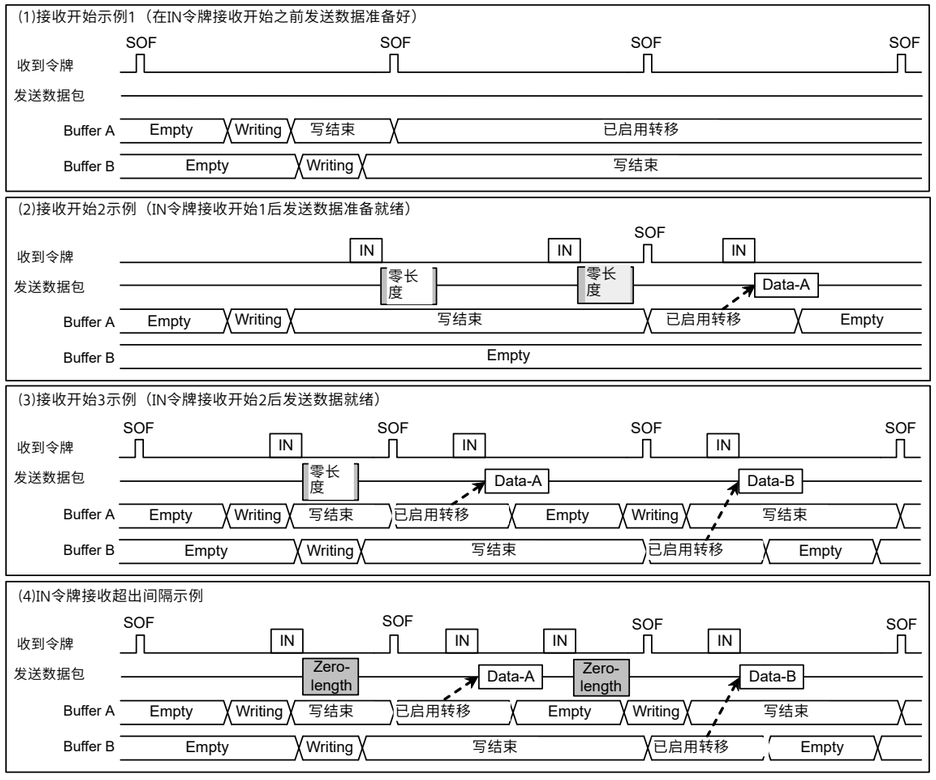

Figure 29.16 示例数据设置操作

(5) 设备控制器模式下的同步传输发送缓冲区刷新

在同步数据传输期间的设备控制器模式下，如果USBHS接收到下一帧的SOF数据包而没有在间隔帧中接收到IN令牌，则它会像IN令牌损坏一样操作并清除启用传输的缓冲区，将该缓冲区处于写入启用状态。

当使用双缓冲并完成对两个缓冲区的写入时，已清除的FIFO缓冲区被假定为在间隔帧中传输数据的缓冲区，并为接收SOF数据包时未清除的FIFO缓冲区启用传输。

缓冲区刷新功能的时间取决于PIPEPERI.IITV[2:0]设置，如下所示：

- When IITV[2:0] = 0:
  缓冲区刷新操作从启用管道后的第一帧开始
- When IITV[2:0] ≠ 0:
  缓冲区刷新操作在第一个正常事务之后开始

图29.17显示了一个示例缓冲区刷新。当在间隔帧之前接收到意外令牌时，USBHS将根据数据设置状态发送写数据或零长度数据包作为欠载错误。

RA生态工作室

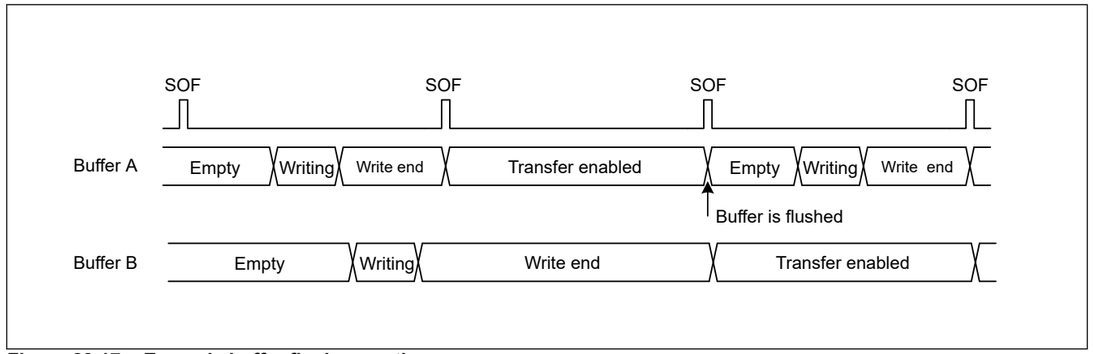

Figure 29.17 Example buffer flush operation

Figure 29.18 shows an example interval error occurrence. There are five types of interval errors, as shown in the figure. An interval error occurs at timing ①, and the buffer flush function is activated.

If an interval error occurs during an IN transfer, the buffer flush function is activated. If it occurs during an OUT transfer, an NRDY interrupt is generated. Use the FRMNUM.OVRN bit to distinguish between this and NRDY interrupts triggered by received packet errors and overrun errors.

For tokens that are shaded in the figure, responses are returned based on the FIFO buffer status.

- IN direction:
  - If the buffer is ready to transfer data, the data is transferred and a normal response is returned
  - If the buffer is not ready to receive data, a zero-length packet is transmitted and an underrun error occurs
- OUT direction:
  - If the buffer is ready to receive data, the data is received and a normal response is returned
  - If the buffer is not ready to receive data, the received data is discarded and an overrun error occurs

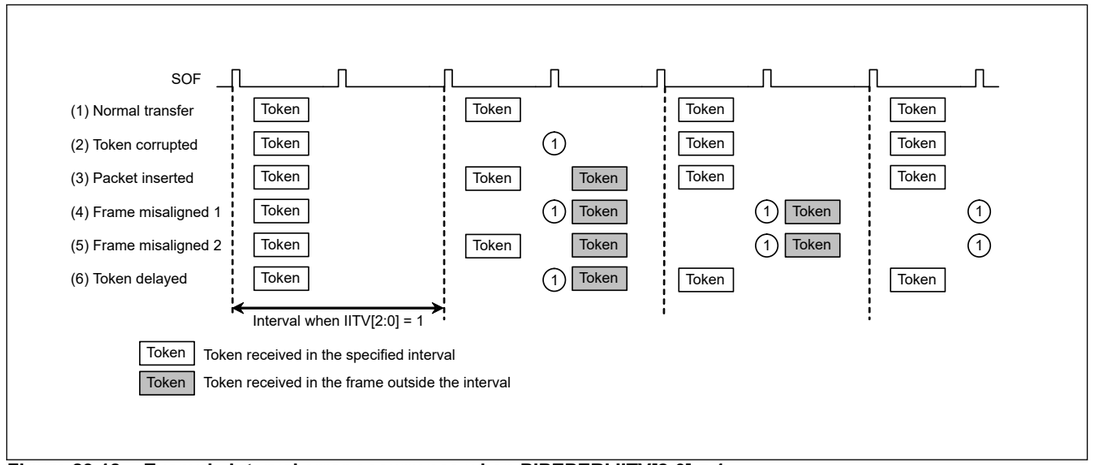

Figure 29.18 Example interval error occurrence when PIPEPERI.IITV[2:0] = 1

29.3.13 SOF Complementation Function

In device controller mode, if packet reception is disabled at intervals of 1 ms in full-speed mode or 125 µs in high-speed mode because the SOF packet is missing or corrupted, the USBHS complements the SOF. SOF complementation begins when the SYSCFG.USBE and LPSTS.SUSPENDM bits are set to 1 and an SOF packet is received. The complementation function is initialized under the following conditions:

- Power-on reset

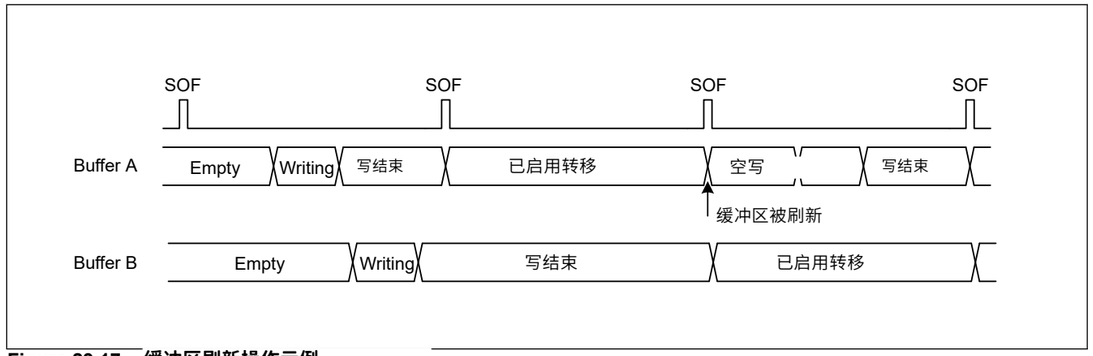

Figure 29.17 缓冲区刷新操作示例

图29.18显示了一个发生间隔错误的示例。如图所示，有五种区间误差。在时间①发生间隔错误，缓冲刷新功能被激活。

如果在IN传输期间发生间隔错误，则会激活缓冲区刷新功能。如果它发生在OUT传输期间，则NRDY中断产生。使用FRMNUM.OVRN位来区分此中断和由接收数据包错误和溢出错误触发的NRDY中断。

对于图中带阴影的令牌，根据FIFO缓冲区状态返回响应。

- IN direction:
  - 如果缓冲区准备好传输数据，则传输数据并返回正常响应
  - 如果缓冲区未准备好传输数据，则传输零长度数据包并发生欠载错误
- OUT direction:
  - 如果缓冲区准备好接收数据，则接收数据并返回正常响应
  - 如果缓冲区没有准备好接收数据，则丢弃接收到的数据并发生溢出错误

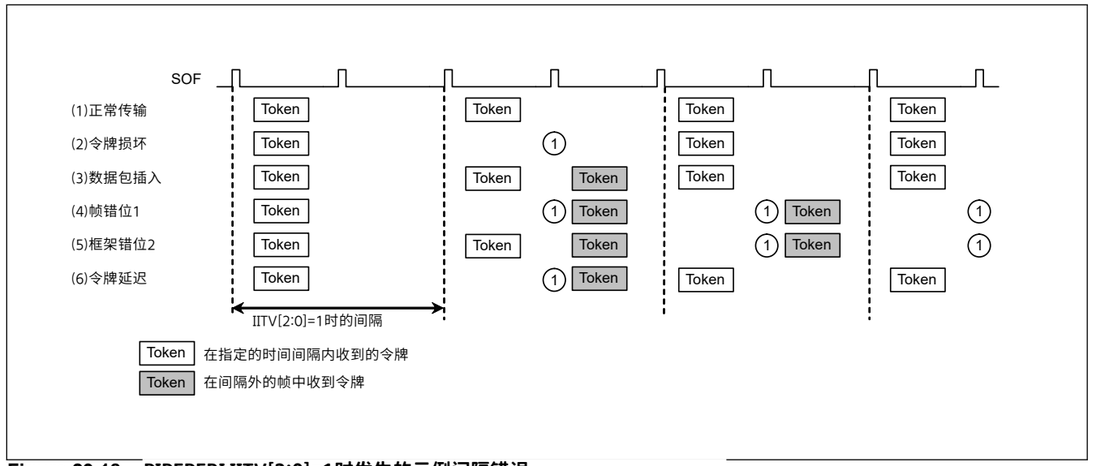

Figure 29.18 PIPEPERI.IITV[2:0]=1时发生的示例间隔错误

29.3.13 SOF互补函数

在设备控制器模式下，如果在全速模式下每隔1ms或在高速模式下每隔125µs禁用数据包接收，因为SOF数据包丢失或损坏，USBHS会补充SOF。当SYSCFG.USBE和LPSTS.SUSPENDM位设置为1并且接收到SOF数据包时，SOF补码开始。补码函数在以下条件下初始化：

- Power-on reset

- USB bus reset
- Suspend state detection

The SOF complementation function operates as follows:

- The frame interval (125 µs or 1 ms) is determined by the reset handshake protocol result
- The complementation function is not activated until an SOF packet is received
- When the first SOF packet is received, complementation is performed by counting 125 µs or 1 ms on the 48-MHz internal clock
- When the second or subsequent SOF packets are received, complementation is performed at the previous reception interval
- Complementation is not performed in the Suspend state or on reception of a USB bus reset. During high-speed operation, complementation continues for 3 ms from the last packet on transition to the Suspend state

The USBHS supports the following functions controlled by SOF packet reception. These functions operate normally with SOF complementation if the SOF packet is missing:

- Updating of the frame number and micro frame number
- SOFR interrupt and micro-SOF lock
- SOF pulse output
- Isochronous transfer interval count

If an SOF packet is missing during full-speed operation, the FFRMNUM.FRNM[10:0] flags are not updated. If a micro-SOF packet is missing during high-speed operation, the URMNUM.UFRNM[2:0] bits are updated.

However, if a micro-SOF packet is missing while the UFRNM[2:0] bits are set to 000b, the FRNM bits are not updated. In this case, even if a subsequent micro-SOF packet with a value other than UFRNM[2:0] bits = 000b is received successfully while UFRNM[2:0] bits are set to the value other than 000b, the FRNM bits are not updated.

29.3.14 Pipe Schedule

29.3.14.1 Conditions for generating transactions

In host controller mode and when the DVSTCTR0.UACT bit is set to 1, the USBHS generates transactions under the conditions as shown in Table 29.33.

Table 29.33 Conditions for generating transactions

Transaction	Conditions for generation				
	DIR	PID[1:0]	IITV0	Buffer state	SUREQ
Setup	—*1	—*1	—*1	—*1	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	—*1	Receive area exists	—*1
	OUT	BUF	—*1	Transmit data exists	—*1
Interrupt transfer	IN	BUF	Valid*2	Receive area exists	—*1
	OUT	BUF	Valid*2	Transmit data exists	—*1
Isochronous transfer	IN	BUF	Valid*2	*3	—*1
	OUT	BUF	Valid*2	*4	—*1

Note 1. An em dash (—) in the table indicates that the condition is unrelated to the generating of tokens.
Note 2. "Valid" indicates that, for interrupt transfers and isochronous transfers, a transaction is generated only in transfer frames that are based on the interval counter.
Note 3. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.
Note 4. This indicates that a transaction is generated regardless of whether there is any data to be transmitted. If there is no data to be transmitted, however, a zero-length packet is transmitted.

●USB总线复位
●暂停状态检测

SOF互补函数的操作如下：

●帧间隔（125μs或1ms）由复位握手协议结果决定
●直到收到SOF报文才激活补码功能
●当接收到第一个SOF数据包时，通过在48-MHz内部时钟上计数125μs或1ms来执行补码
●当接收到第二个或后续的SOF数据包时，按照前一个接收间隔进行补码
●在挂起状态或接收到USB总线复位时不执行补码。在高速运行期间，从最后一个数据包转换到暂停状态时，互补会持续3ms

USBHS支持以下由SOF数据包接收控制的功能。这些功能正常运行
如果SOF数据包丢失，则SOF补充：

●更新帧号和微帧号
●SOFR中断和micro-SOF锁定
●SOF脉冲输出
●同步传输间隔计数

如果在全速操作期间丢失SOF数据包，则FFRMNUM.FRNM[10:0]标志不会更新。如果一个微SOF数据包在高速运行期间丢失，URMNUM.UFRNM[2:0]位被更新。

但是，如果在UFRNM[2:0]位设置为000b时缺少micro-SOF数据包，则不会更新FRNM位。在这种情况下，即使在将UFRNM[2:0]位设置为000b以外的值时成功接收到具有非UFRNM[2:0]位=000b的值的后续micro-SOF数据包，FRNM位仍为未更新。

29.3.14 管道计划

29.3.14.1 产生交易的条件

在主机控制器模式下，当DVSTCTR0.UACT位设置为1时，USBHS在表29.33所示的条件下生成事务。

Table 29.33 产生交易的条件

Transaction	生成条件				
	DIR	PID[1:0]	IITV0	缓冲状态	SUREQ
Setup	—*1	—*1	—*1	—*1	1 setting
控制传输数据阶段、状态阶段、批量传输	IN	BUF	—*1	接收区存在	—*1
	OUT	BUF	—*1	传输数据存在	—*1
中断传输	IN	BUF	Valid*2	接收区存在	—*1
	OUT	BUF	Valid*2	传输数据存在	—*1
Isochronous transfer	IN	BUF	Valid*2	*3	—*1
	OUT	BUF	Valid*2	*4	—*1

注1.表中的破折号(—)表示该条件与令牌的生成无关。
注2."有效"表示，对于中断传输和同步传输，事务仅在基于间隔计数器的传输帧中生成。

注3.这表示无论是否有接收区域，都会生成一个事务。但是，如果没有接收区域，则丢弃接收到的数据。

注4.这表示无论是否有任何数据要传输，都会产生交易。然而，如果没有要传输的数据，则传输零长度数据包。

29.3.14.2 Transfer schedule

This section describes the transfer scheduling within a frame of the USBHS. After the USBHS sends an SOF, the transfer is carried out in the following sequence:

1. Execution of periodic transfers:
   A pipe is searched for in the order of pipe 1 → pipe 2 → pipe 6 → pipe 7 → pipe 8 → pipe 9, and then if there is a pipe for which an isochronous or interrupt transfer transaction can be generated, the transaction is generated.
2. Setup transactions for control transfers:
   The DCP is checked, and if a setup transaction is possible, it is sent.
3. Execution of bulk transfers, control transfer data stages, and control transfer status stages:
   A pipe is searched for in the order of DCP → pipe 1 → pipe 2 → pipe 3 → pipe 4 → pipe 5, and then if there is a pipe for which a transaction for a bulk transfer, a control transfer data stage, or a control transfer status stage can be generated, the transaction is generated.
   When a transaction is generated, processing moves to the next pipe transaction regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, step 3 is repeated.

29.3.14.3 Enabling USB communication

Setting the DVSTCTR0.UACT bit to 1 initiates an SOF transmission, and transaction generation is enabled. Setting the UACT bit to 0 stops SOF transmission, and the Suspend state is invoked. If the UACT setting is changed from 1 to 0, processing stops after the next SOF is sent.

29.3.15 Battery charging detection processing

The USBHS provides control over the data contact detection processing (D+ line contact checking), primary detection processing (charger detection processing), and secondary detection processing (charger determination processing) as defined in the Battery Charging Specification.

This section describes operations required in device and host controller modes.

29.3.15.1 Processing in device controller mode

To operate a function device as a battery charging portable device:

1. Start primary detection processing after detecting contact with the D+ and D- lines. The Battery Charging Specification describes two processing methods for Data Contact Detection. The USBHS supports both methods as follows:
   - Software processing
     After a VBINT interrupt or polling of the VBSTS flag indicates a change in the state of the USBHS_VBUS input pin, software controls a wait from 300 to 900 ms. The BCCTRL.VDPSRCE and IDMSINKE bits are then both set to 1, enabling the VDP_SRC and IMP_SINK circuits, respectively, to start primary detection processing.
   - Hardware processing
     Apply 7 to 13 µA of current to the D+ line to hold the D+ line at the logical high level. This is done to detect the D+ and D- lines going to the logical low level because of pull-down resistors on the host device side when the D+ and D- lines come in contact with those of the host. Monitor the SYSSTS0.LNST[1:0] flags while the BCCTRL.IDPSRCE bit is set to 1, enabling the IDP_SRC circuit, to see when the level on the D+ line changes from high to low. After detecting a low level on the D+ line, clear the BCCTRL.IDPSRCE bit to 0, disabling the IDP_SRC circuit, and set both the BCCTRL.VDPSRCE and IDMSINKE bits to 1, enabling the VDP_SRC and IDM_SINK circuits, respectively, to start primary detection processing. The VDPSRCE and IDMSINKE bits must be set to 1 simultaneously.
2. After the start of primary detection processing followed by a software-controlled wait of 40 ms, check the BCCTRL.CHGDETSTS flag. A value of 1 indicates detection of a charger, and secondary detection processing starts.*1
3. To start secondary detection processing, clear both the BCCTRL.VDPSRCE and IDMSINKE bits to 0, disabling the VDP_SRC and IDM_SINK circuits, respectively. Next, set both the BCCTRL.VDMSRCE and IDPSINKE bits to 1, enabling the VDM_SRC and IDP_SINK circuits, respectively.
4. After the start of secondary detection processing followed by a software-controlled wait of 40 ms, check the BCCTRL.PDDETSTS flag. A value of 1 indicates that secondary detection processing is complete.

29.3.14.2 转移时间表

本节介绍USBHS帧内的传输调度。USBHS发送SOF后，按以下顺序进行传输：

1.定期转账的执行：
按照管道1→管道2→管道6→管道7→管道8→管道9的顺序查找管道，如果有管道可以产生等时或中断传输事务，则产生该事务.

2.为控制转移设置交易：
DCP被检查，如果设置事务是可能的，它被发送。

3、批量传输、控制传输数据阶段、控制传输状态阶段的执行：
按照DCP→管道1→管道2→管道3→管道4→管道5的顺序搜索管道，然后如果有管道需要进行批量传输、控制传输数据阶段或可以生成控制转移状态阶段，生成事务。生成事务时，无论来自外围设备的响应是ACK还是NAK，处理都会转移到下一个管道事务。如果帧内有时间进行传输，则重复步骤3。

29.3.14.3 启用USB通信

将DVSTCR0.UACT位设置为1启动SOF传输，并启用事务生成。设置
UACT位为0停止SOF传输，并调用暂停状态。如果UACT设置从1更改为0，则在发送下一个SOF后处理停止
。

29.3.15 电池充电检测处理

USBHS提供对电池充电规范中定义的数据接触检测处理（D+线路接触检查）、一次检测处理（充电器检测处理）和二次检测处理（充电器确定处理）的控制。

本节介绍设备和主机控制器模式所需的操作。

29.3.15.1 设备控制器模式下的处理

将功能设备作为电池充电便携式设备操作：

1.检测到与D+和Dlines的接触后开始初级检测处理。电池充电规范描述了数据接触检测的两种处理方法。USBHS支持以下两种方法：

●软件处理
在VBINT中断或轮询VBSTS标志指示USBHS_VBUS输入引脚的状态发生变化后，软件控制从300到900ms的等待。然后BCCTRL.VDPSRCE和IDMSINKE位都设置为1，分别使VDP_SRC和IMP_SINK电路开始主要检测处理。

●硬件加工
向D+线施加7到13µA的电流，以将D+线保持在逻辑高电平。这样做是为了检测D+和Dlines进入逻辑低电平，因为当D+和Dlines与主机的那些接触时，由于主机设备侧的下拉电阻器。监控SYSSTS0.LNST[1:0]标志，而

BCCTRL.IDPSRCE位设置为1，启用IDP_SRC电路，以查看D+线上的电平何时从高变为低。检测到D+线上的低电平后，将BCCTRL.IDPSRCE位清除为0，禁用IDP_SRC电路，并将BCCTRL.VDPSRCE和IDMSINKE位都设置为1，启用VDP_SRC和

IDM_SINK电路分别启动初级检测处理。VDPSRCE和IDMSINKE位必须同时设置为1。

2.主要检测处理开始后，软件控制等待40毫秒后，检查
BCCTRL.CHGDETSTS标志。值为1表示检测到充电器，并开始二次检测处理。*1

3.要开始二次检测处理，请将BCCTRL.VDPSRCE和IDMSINKE位都清零，分别禁用VDP_SRC和IDM_SINK电路。接下来，将BCCTRL.VDMSRCE和IDPSINKE位都设置为1，分别启用VDM_SRC和IDP_SINK电路。

4.二次检测处理开始后，软件控制等待40毫秒后，检查BCCTRL.PDDETSTS标志。值为1表示二次检测处理完成。

Note 1. In primary detection processing, detection of a voltage above the range from 0.25 to 0.4 V and below the range from 0.8 to 2.0 V on the D-Line indicates that the other device is a host device that supports battery charging (charging downstream port). The BCCTRL.CHGDETSTS flag in the PHY block only indicates whether the voltage on the D-line is higher than the range from 0.25 to 0.4 V, so add processing as required to read the SYSSTS0.LNST[1:0] flags and confirm that the voltage on the D- line is also below the range from 0.8 to 2.0 V.

Figure 29.19 illustrates this processing flow.

注1.在初级检测处理中，在D-Line上检测到高于0.25至0.4V范围且低于0.8至2.0V范围的电压表示其他设备是支持电池充电的主机设备（充电下游港口）。PHY块中的BCCTRL.CHGDETSTS标志位仅指示Dline上的电压是否高于0.25至0.4V的范围，因此根据需要添加处理以读取SYSSTS0.LNST[1:0]标志并确认电压Dline上的电压也低于0.8至2.0V的范围。

图29.19说明了这个处理流程。

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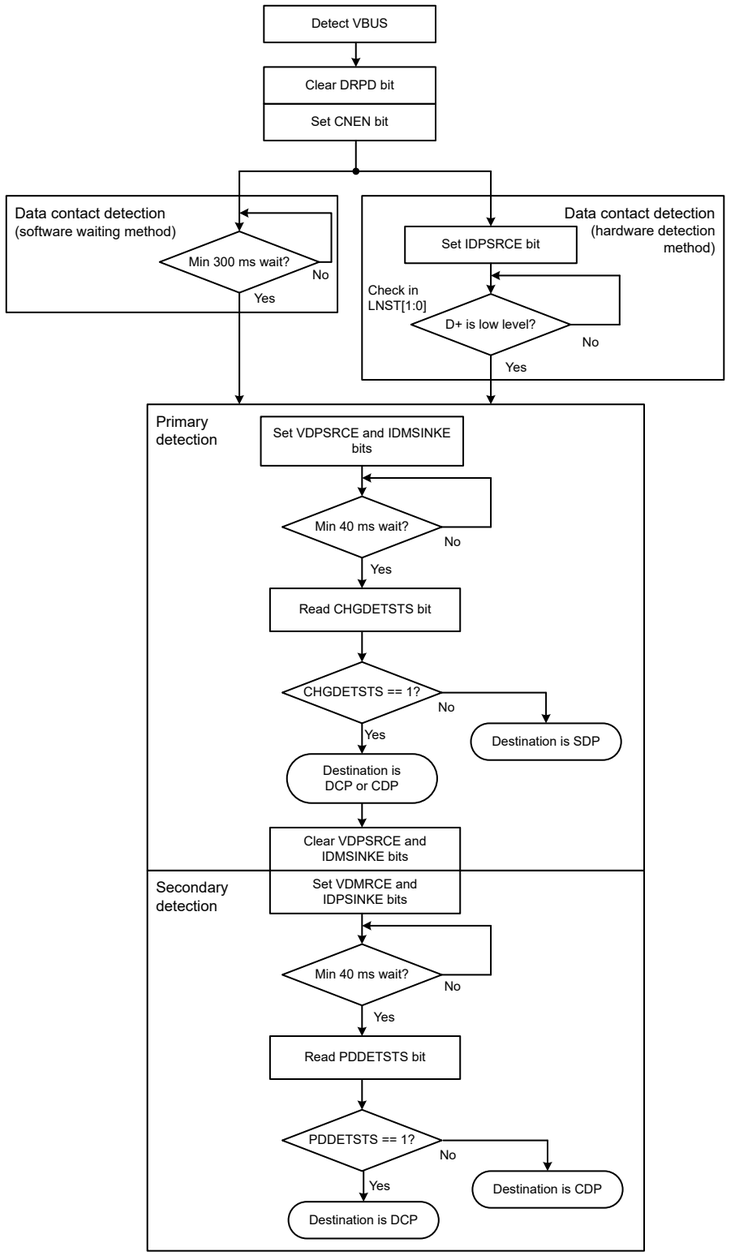

Figure 29.19 Processing flow as portable device

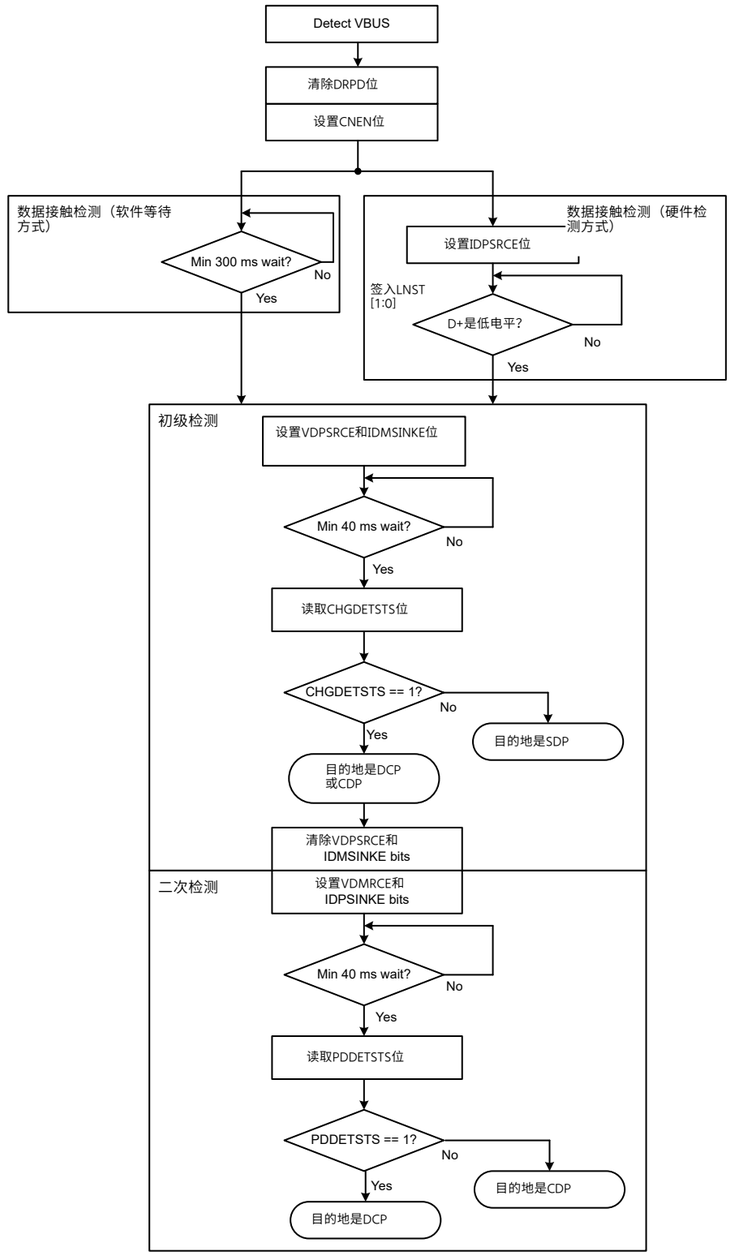

Figure 29.19 作为便携式设备的处理流程

29.3.15.2 Processing in host controller mode

In host controller mode, driving the D- line is required for a portable device to perform primary detection. The USBHS supports the following two primary detection methods:

- When the hardware has a portable device detection function
- When the hardware does not have the function or the function is present but not used

Figure 29.20 and Figure 29.21 show the processing flows for these methods.

(1) When the hardware has a portable device detection function

a. Start driving the USBHS_VBUS input pin.

b. Set the BCCTRL.IDMSINKE bit to 1 to enable the portable device detection circuit.

c. Monitor the portable device detection signal and start driving the D-line when the level of the portable device detection signal is high*1.

d. Stop driving the D-line when the portable device detection signal is at the low level*1.

Note 1. The PDDETINT interrupt indicates a change in the level of the portable device detection signal (EUH_CPDDET), and the current level can be obtained by reading the PDDETSTS flag.

(2) When the hardware does not have a portable device detection function or the function is not used

Software handles the timing of steps a. and b.

a. After a disconnect is detected, start driving the D-line within 200 ms.

b. After a connect is detected, stop driving the D-line within 10 ms.

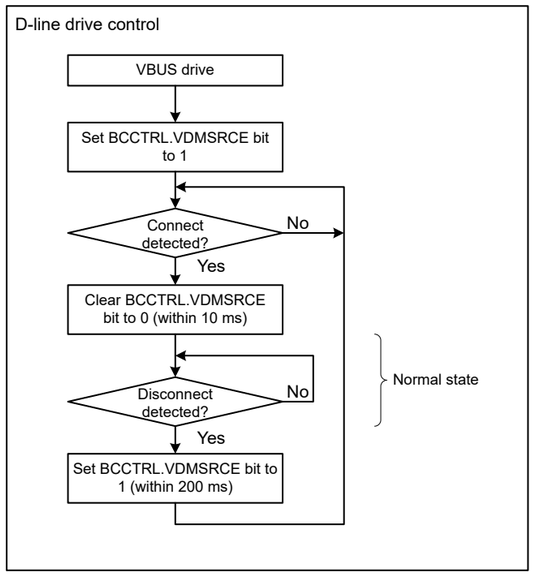

Figure 29.20 Processing flow as charging downstream port without hardware portable device detectionfunction or when function is not used

29.3.15.2 主机控制器模式下的处理

在主机控制器模式下，便携式设备需要驱动Dline才能执行初级检测。USBHS支持以下两种主要检测方法：

●当硬件具有便携设备检测功能时

●当硬件不具备该功能或该功能存在但未使用时

图29.20和图29.21显示了这些方法的处理流程。

(1) 当硬件具有便携设备检测功能时

a. 开始驱动USBHS_VBUS输入引脚。

湾。将BCCTRL.IDMSINKE位设置为1以启用便携式设备检测电路。

c. 监视便携设备检测信号，当便携设备检测信号为高电平时开始驱动D线*1。

d。便携设备检测信号为低电平时停止驱动D线*1。

注1.PDDETINT中断表示便携式设备检测信号（EUH_CPDDET）的电平发生变化，通过读取PDDETSTS标志可以获得当前电平。

(2) 硬件不具备便携设备检测功能或未使用该功能时

软件处理步骤a的时间安排。和b。

a. 检测到断开后，在200毫秒内开始驱动D线。

湾。检测到连接后，在10ms内停止驱动D线。

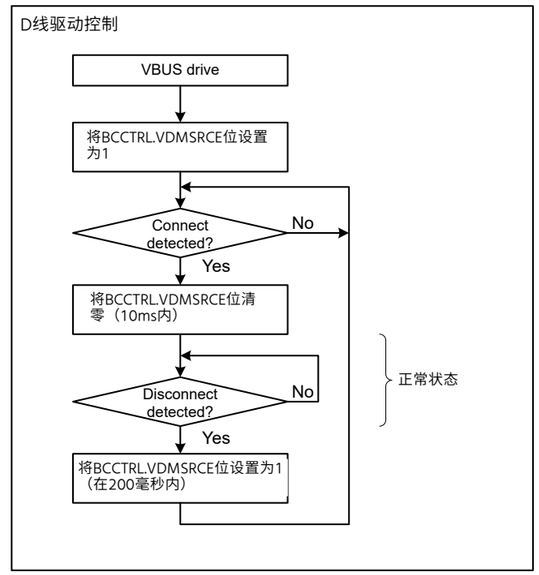

Figure 29.20 没有硬件便携设备检测功能或不使用功能时作为充电下行端口的处理流程

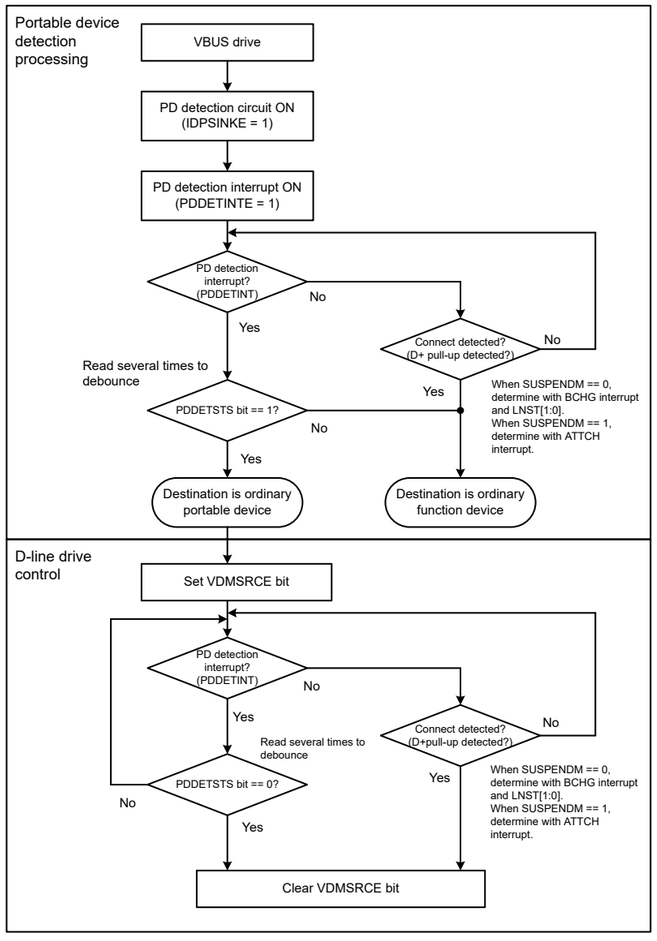

Figure 29.21 Processing flow as charging downstream port with hardware portable device detection function

29.3.16 Link Power Management Processing

The Link Power Management standard defines the existing Suspend state as the L2 state and also defines the L1 state as a state that allows transition and return with lower latency than the L2 state (Suspend). Table 29.34 provides a comparison between the L2 (Suspend) and L1 states.

Table 29.34 Comparison between L2 (Suspend) state and L1 state (1 of 2) (1 of 2)

Parameter	L1 state	L2 (Suspend) state
Transition	LPM transaction	Idle for 3 ms

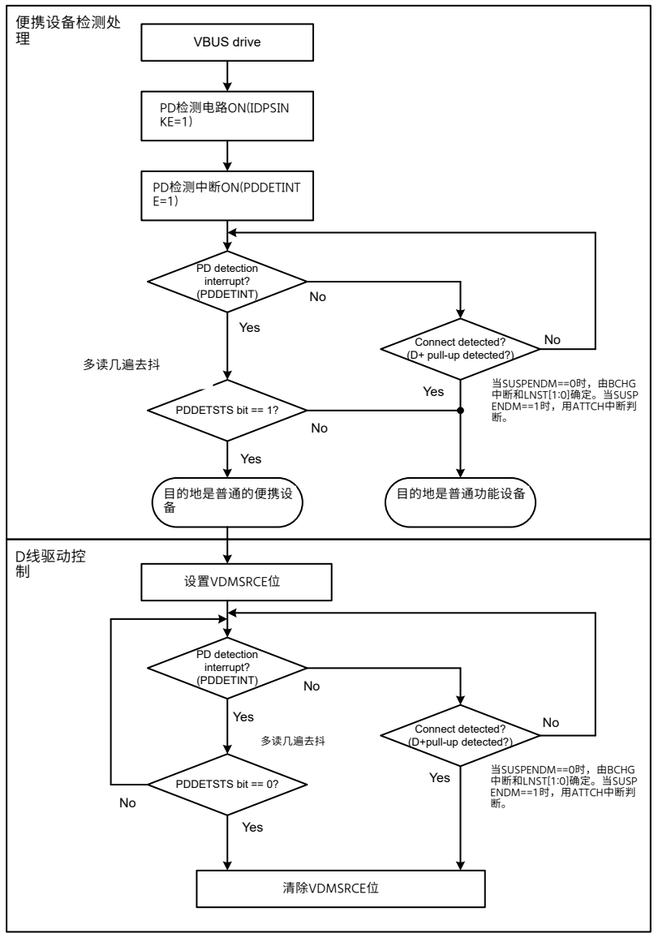

Figure 29.21 具有硬件便携设备检测功能的充电下行端口的处理流程

29.3.16 链路电源管理处理

LinkPowerManagement标准将现有的Suspend状态定义为L2状态，并将L1状态定义为允许转换和返回时延迟低于L2状态(Suspend)的状态。表29.34提供了L2（挂起）和L1状态之间的比较。

Table 29.34 L2（挂起）状态和L1状态之间的比较（1of2）（1of2）

Parameter	L1 state	L2 (Suspend) state
Transition	LPM transaction	空闲3毫秒

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Table 29.34 Comparison between L2 (Suspend) state and L1 state (1 of 2) (2 of 2)

Parameter	L1 state	L2 (Suspend) state
Return caused by host	Host: Minimum drive period (75 µs to 1.175 ms) can be specified by the host. Function: 10-µs K drive	Host: Minimum 20-ms K drive Function: 10-ms K drive
Return caused by function	Device: 50-µs K drive Function: 60- to 990-µs K drive Device: 10-µs K drive	Function: 1- to 15-ms K drive Host: Minimum 20-ms K drive Function: 10-ms K drive
Signaling	Low- and full-speed idle	Low- and full-speed idle

29.3.16.1 Processing in device controller mode

(1) Descriptor contents

In device controller mode, the USBHS must return its descriptor on receiving the GetDescriptor command.

Change the content of the descriptor to be returned depending on whether the transition to and return from the L1 state corresponds to the processing for the LPM transaction. The following table shows the relationship between LPM correspondence and the descriptor.

Table 29.35 Relationship between LPM correspondence and descriptor

Correspondence with LPM	bcdUSB field	USB2.0 extension descriptor		Response to received LPM request	Notes
		Provided/ not provided	Value of LPM bit		
Does not correspond	0200h	Not provided	—	No response	Normal operation when the LPM is not supported
	0201h	Provided	0	STALL	Setting for clear non-correspondence to LPM. In this case, a STALL response must be returned.
Corresponds	0201h	Provided	1	ACK or NYET	Normal operation when the LPM is supported

Declare whether to correspond to the transition to and return from L1 in the LPM bit in the USB 2.0 extension descriptor. To provide the USB2.0 extension descriptor, the bcdUSB field of the device descriptor must be set to a value of 0201h or larger.

When the LPM is not supported, the USB2.0 extension descriptor is not provided and the bcdUSB field value must be 0200h. If an LPM token is received in this case, it must be ignored. It is also possible to set the bcdUSB field value to 0201h and the LPM bit in the USB2.0 extension descriptor to 0 (LPM tokens not supported). In this case, the LPM token cannot be ignored and a STALL response must be returned.

When the LPM token is supported, set the bcdUSB field value to 0201h and set the LPM bit in the USB 2.0 extension descriptor to 1 (LPM tokens supported). This allows acknowledgment when returning a NYET or ACK response to the LPM token.

(2) Processing during LPM token reception

Transition to and return from the L1 state in device controller mode is as follows:

a. When the USBHS receives an LPM token from the host, the L1RESPEN, L1RESPMD[1:0], and L1NEGOMD settings in PL1CTRL1 determine whether a response packet is sent or the token is ignored and, if a response is to be sent, whether it is an ACK, NYET, or STALL packet.

b. If an ACK response to the LPM token is sent and the host does not transmit another LPM token in 8 µs, the USBHS enters the L1 state. The USBHS handles detection of the newly transmitted packet and the transition to the L1 state. The DVST interrupt can be used to detect the transition.

Table 29.34 L2（挂起）状态和L1状态之间的比较(1of2)(2of2)

Parameter	L1 state	L2 (Suspend) state
主机造成的退货	Host: 主机可以指定最小驱动周期（75µs至1.175ms）。功能：10-µsK驱动	Host: 最小20毫秒K驱动器 Function: 10-ms K drive
函数导致的返回	Device: 50-µs K drive Function: 60- to 990-µs K drive Device: 10-µs K drive	Function: 1- to 15-ms K drive Host: 最小20毫秒K驱动器 Function: 10-ms K drive
Signaling	Low- and full-speed idle	Low- and full-speed idle

29.3.16.1 设备控制器模式下的处理

(1) 描述符内容

在设备控制器模式下，USBHS必须在接收到GetDescriptor命令时返回其描述符。

根据L1状态的转换和返回是否对应于LPM事务的处理，更改要返回的描述符的内容。下表显示了LPM对应关系和描述符之间的关系。

Table 29.35 LPM对应与描述符的关系

与LPM的通信	bcdUSB field	USB2.0扩展描述符		收到的回复 LPM request	Notes
		提供未提供	LPM位的值		
不对应	0200h	不提供	—	没有反应	不支持LPM时的正常操作
	0201h	Provided	0	STALL	设置明确不对应 LPM。在这种情况下，必须返回一个STALL响应。
Corresponds	0201h	Provided	1	ACK或NYET	支持LPM时的正常操作

在USB2.0扩展描述符中的LPM位中声明是否对应于L1的转换和返回。要提供USB2.0扩展描述符，设备描述符的bcdUSB字段必须设置为0201h或更大的值。

不支持LPM时，不提供USB2.0扩展描述符，bcdUSB字段值必须为0200h。如果在这种情况下接收到LPM令牌，则必须将其忽略。也可以将bcdUSB字段值设置为0201h，并将USB2.0扩展描述符中的LPM位设置为0（不支持LPM令牌）。在这种情况下，不能忽略LPM令牌并且必须返回STALL响应。

当支持LPM令牌时，将bcdUSB字段值设置为0201h，并将USB2.0扩展描述符中的LPM位设置为1（支持LPM令牌）。这允许在向LPM令牌返回NYET或ACK响应时进行确认。

(2) LPM令牌接收期间的处理

设备控制器模式下L1状态的转换和返回如下：

a. 当USBHS从主机接收到LPM令牌时，PL1CTRL1中的L1RESPEN、L1RESPMD[1:0]和L1NEGOMD设置确定是发送响应包还是忽略令牌，如果要发送响应，是否是ACK、NYET或STALL数据包。

湾。如果发送了对LPM令牌的ACK响应并且主机在8µs内没有发送另一个LPM令牌，则USBHS进入L1状态。USBHS处理新传输数据包的检测和向L1状态的转换。DVST中断可用于检测转换。

c. Two types of processing can return the USBHS from the L1 state:

- When the host drives the D-line in the K-state:
  The function device detects the K-state and starts processing the return from the L1 state in response to an RESM interrupt request
- When the function device outputs a remote wakeup signal:
  If the software on the function device sets the DVSTCTR0.WKUP bit to 1, it sends a remote wakeup signal to the host

The software clears the DVSTCTR0.WKUP bit to 0 on returning from the L2 (Suspend) state, and the USBHS clears the DVSTCTR0.WKUP bit to 0 for return from the L1 state.

(3) HIRD field value negotiation function

The HIRD field value included in the LPM token indicates the host K-drive period on return from the L1 state. The HIRD field value can be adjusted according to the requirements of the target system. For example, a small HIRD field value is better for systems focusing on higher transfer efficiency, while a large HIRD field value is better for systems focusing on low power consumption.

Based on the L1NEGOMD and HIRDTHR[3:0] settings in PL1CTRL1, an ACK response is returned when the received HIRD field value is in the expected range, and otherwise a NYET response is returned, requesting the host to change the HIRD field value.

Note: This HIRD field value negotiation function at the host must also support negotiation processing.

29.3.16.2 Processing in host controller mode

(1) Processing during LPM token transmission

Transition to and return from the L1 state in host controller mode is as follows:

a. When the HL1CTRL.L1REQ bit is set to 1, an LPM token is sent to the function device from the host device.

b. If an ACK response is received from the function device, a transition to the L1 state starts within 10 µs and is complete within 50 µs. If a transaction error is detected, another LPM token is transmitted within 8 µs. Retransmission can proceed up to two times. The USBHS handles all of this processing.

c. Two types of processing can return the USBHS from the L1 state:

- When the host drives the D-line for the K state:
  When the DVSTCTR0.RESUME bit is set to 1, the host device starts driving the D-line for the K-state and starts processing the return
- When the function device generates a remote wakeup signal:
  When the host device detects a remote wakeup signal from the function device, it sets the DVSTCTR0.RESUME bit to 1 and starts driving the D-line for the K-state

Unlike when returning from the Suspend (L2) state, the USBHS clears the DVSTCTR0.RESUME bit to 0. After clearing the RESUME bit, it sets the DVSTCTR0.UACT bit to 1 and issues an L1RSMEND interrupt request.

29.3.17 Release from Deep Software Standby Mode Because of USB Suspend/Resume Interrupts

Deep Software Standby mode can be canceled by a USB suspend/resume interrupt. USB suspend/resume interrupts are detected by the USB resume detecting unit, which controls and monitors the USB I/O pins to detect the interrupts.

Figure 29.22 shows the flow for setting the USBHS when entering Deep Software Standby mode from either host or device controller mode. Figure 29.23 and Figure 29.24 show the flows for setting the USBHS when canceling Deep Software Standby mode from host controller mode. Figure 29.25 shows the flow for setting the USBHS when canceling Deep Software Standby mode from device controller mode.

c. 两种类型的处理可以使USBHS从L1状态返回：

●当主机在K态驱动D线时：
功能设备检测到K状态并开始处理从L1状态返回以响应RESM中断请求

●当功能设备输出远程唤醒信号时：
如果功能设备上的软件将DVSTCTR0.WKUP位设置为1，它会向主机发送远程唤醒信号

软件在从L2（挂起）状态返回时将DVSTCTR0.WKUP位清除为0，并且USBHS清除
DVSTCTR0.WKUP位为0表示从L1状态返回。

(3) HIRD字段值协商功能

LPM令牌中包含的HIRD字段值指示从L1状态返回的主机K-drive周期。HIRD字段值可以根据目标系统的要求进行调整。例如，较小的HIRD字段值更适合专注于更高传输效率的系统，而较大的HIRD字段值更适合专注于低功耗的系统。

根据PL1CTRL1中的L1NEGOMD和HIRDTHR[3:0]设置，当接收到的HIRD字段值在预期范围内时返回ACK响应，否则返回NYET响应，请求主机更改
HIRD字段值。

Note: 主机上的这个HIRD字段值协商功能也必须支持协商处理。

29.3.16.2 主机控制器模式下的处理

(1) LPM令牌传输期间的处理

主机控制器模式下L1状态的转换和返回如下：

a. 当HL1CTRL.L1REQ位设置为1时，LPM令牌从主机设备发送到功能设备。

湾。如果从功能设备接收到ACK响应，则在10µs内开始转换到L1状态，并在50µs内完成。如果检测到事务错误，则会在8µs内发送另一个LPM令牌。重传最多可以进行两次。USBHS处理所有这些处理。

c. 两种类型的处理可以使USBHS从L1状态返回：

●当主机驱动D线为K状态时：
当DVSTCTR0.RESUME位设置为1时，主机设备开始驱动D线为K状态并开始处理返回

●当功能设备产生远程唤醒信号时：
当主机设备检测到来自功能设备的远程唤醒信号时，它会将DVSTCTR0.RESUME位设置为1，并开始驱动D线为K状态

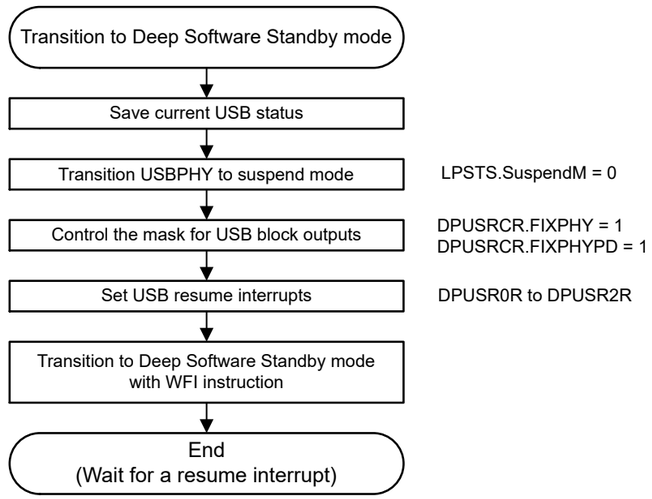
与从挂起(L2)状态返回时不同，USBHS将DVSTCTR0.RESUME位清除为0。清除RESUME位后，将DVSTCTR0.UACT位设置为1并发出L1RSMEND中断请求。

29.3.17 由于USB挂起恢复而从深度软件待机模式中释放 Interrupts

深度软件待机模式可以通过USB挂起恢复中断来取消。USB暂停恢复中断由USB恢复检测单元检测，该单元控制和监视USBIO引脚以检测中断。

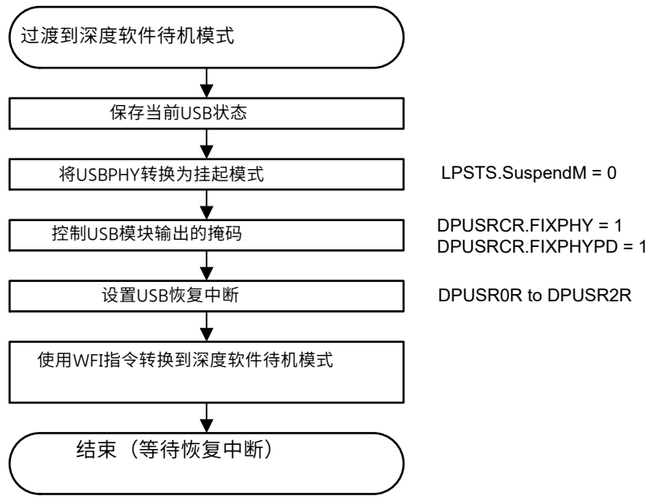
图29.22显示了从主机或设备控制器模式进入深度软件待机模式时设置USBHS的流程。图29.23和图29.24显示了从主机控制器模式取消深度软件待机模式时设置USBHS的流程。图29.25显示取消Deep时设置USBHS的流程

设备控制器模式下的软件待机模式。



Note 1. When connected to an external device, transition to Deep Software Standby mode is enabled only on USB Suspend.
Note 2. Never invoke Deep Software Standby mode in the following cases:
- In an L1 Suspend status with the USB-LPM protocol.
- When remote wakeup is enabled in host controller mode.

Figure 29.22 USBHS setup flow for transition to Deep Software Standby mode as a host or device controller



注1.当连接到外部设备时，只有在USB挂起时才能转换到深度软件待机模式。
注2.在下列情况下切勿调用深度软件待机模式：
- 使用USB-LPM协议处于L1挂起状态。
- 在主机控制器模式下启用远程唤醒时。

Figure 29.22 作为主机或设备控制器转换到深度软件待机模式的USBHS设置流程

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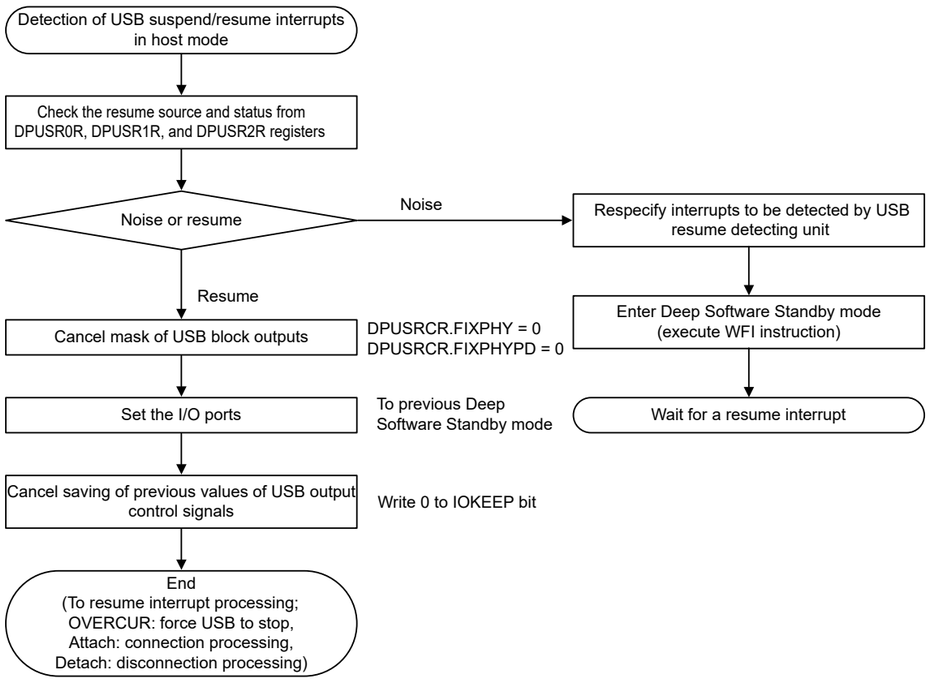


Figure 29.23 USBHS setup flow for canceling Deep Software Standby mode as a host controller (1)

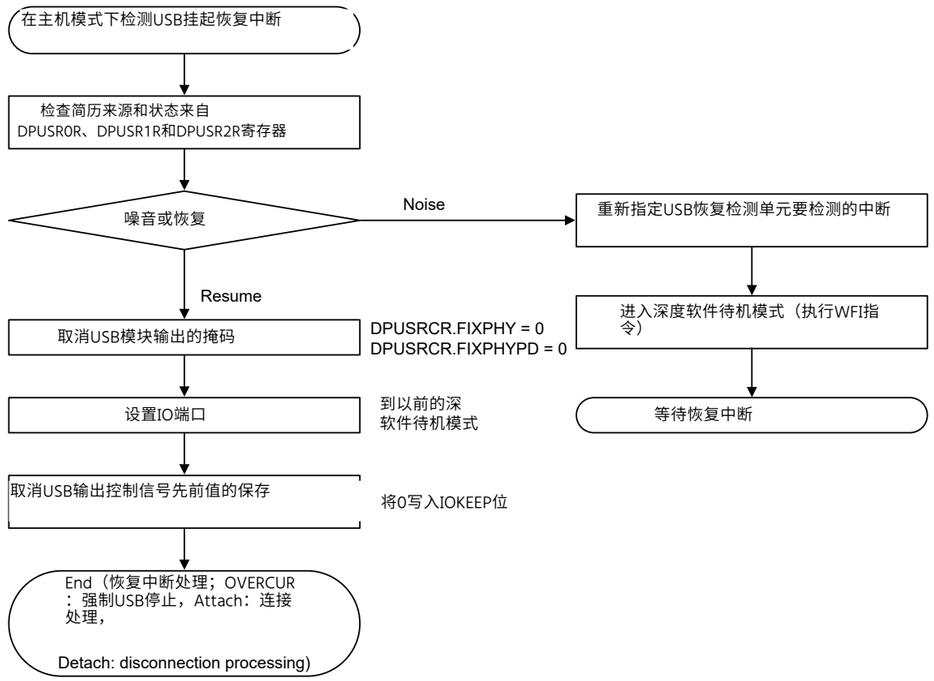


Figure 29.23 用于取消作为主机控制器的深度软件待机模式的USBHS设置流程(1)

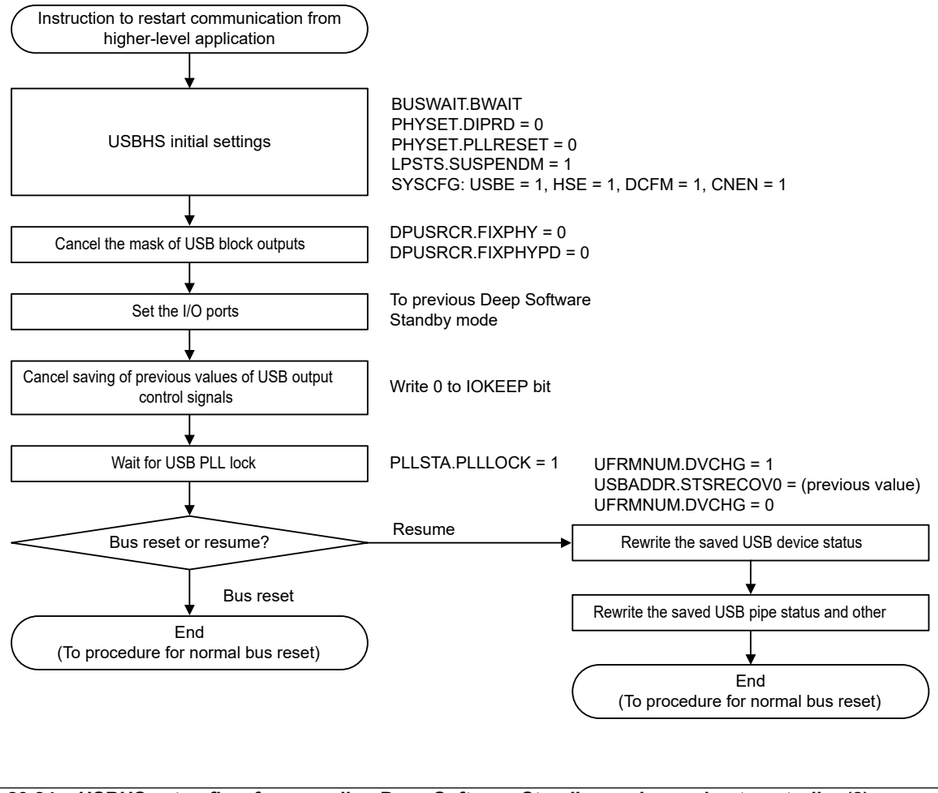


Figure 29.24 USBHS setup flow for canceling Deep Software Standby mode as a host controller (2)

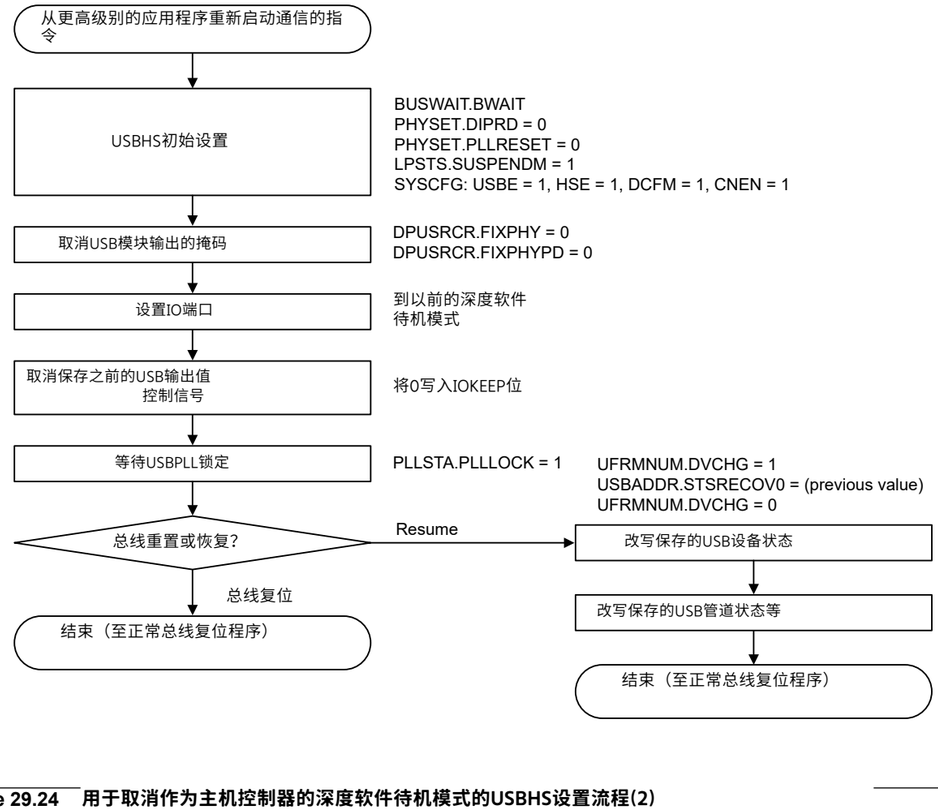
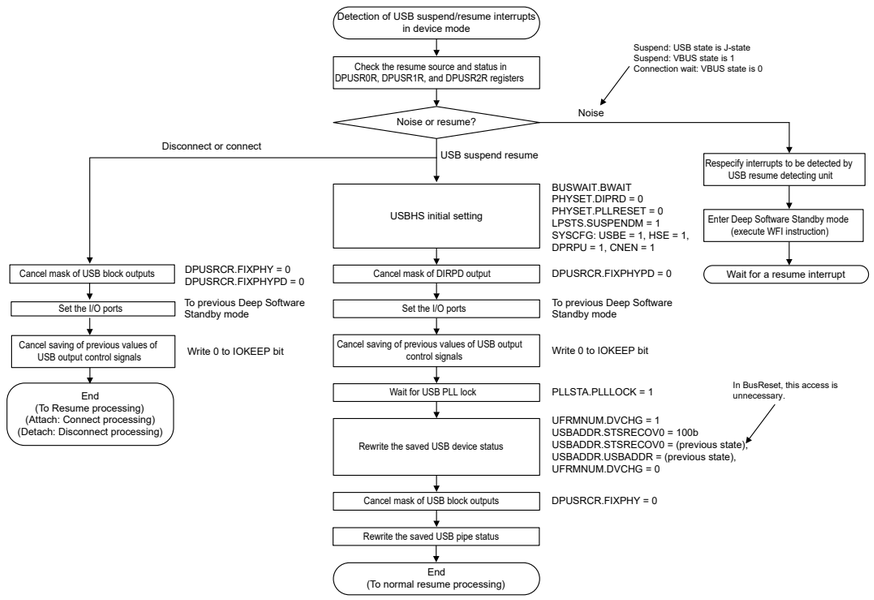
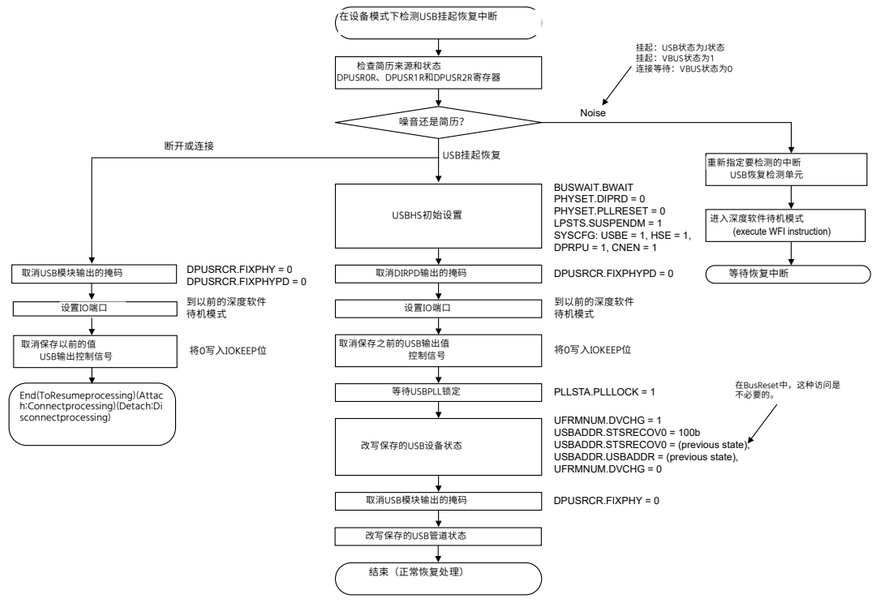


Figure 29.24 用于取消作为主机控制器的深度软件待机模式的USBHS设置流程(2)



Note 1. In BusReset return, the write to the STSRECOV0 bit must be within 2.5 μS of USBHS-PHY PLL oscillation start.

Figure 29.25 USBHS setup flow for transition to Deep Software Standby mode as a host or device controller



注1.在BusReset返回时，写入STSRECOV0位必须在USBHS-PHYPLL振荡开始的2.5μS内。

Figure 29.25 作为主机或设备控制器转换到深度软件待机模式的USBHS设置流程

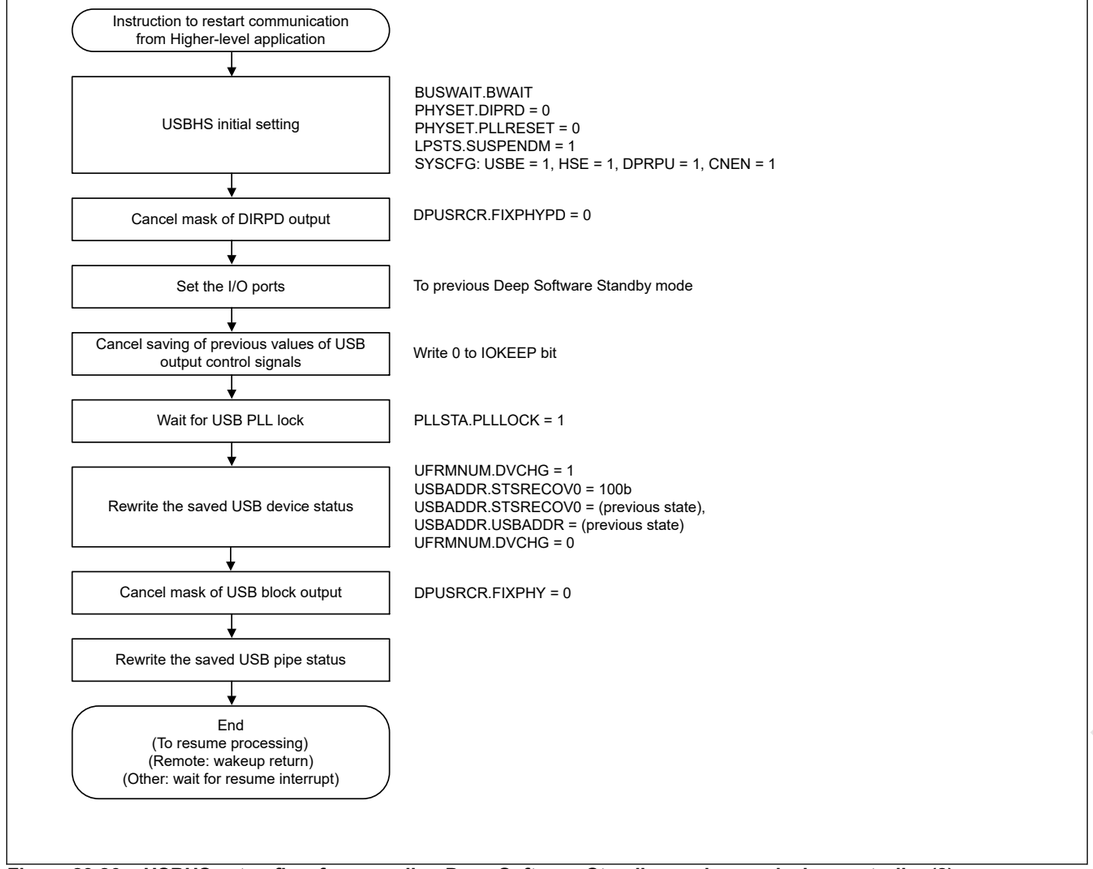


Figure 29.26 USBHS setup flow for canceling Deep Software Standby mode as a device controller (2)

29.3.18 Example External Connection Circuits

Figure 29.27 shows an example OTG connection in a self-powered system. The USBHS controls the pull-up resistor of the D+ line and the pull-down resistor of D+ and D- lines. Select pull-up and pull-down for the lines in the SYSCFG.DPRPU and SYSCFG.DRPD bits. In device controller mode, the pull-up resistor of USB data line is disabled if SYSCFG.DPRPU bit is set to 0 while communicating with the USB host. The USBHS can use this to notify the USB host of a device disconnect.

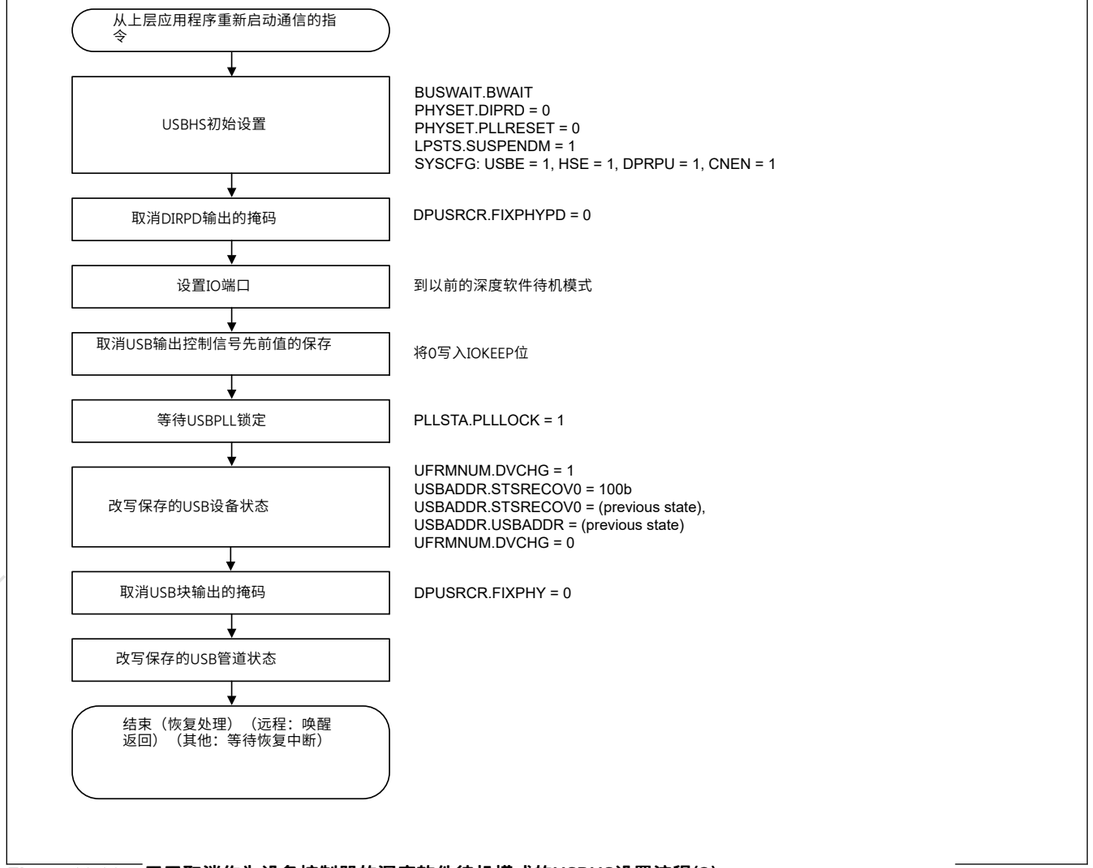


Figure 29.26 用于取消作为设备控制器的深度软件待机模式的USBHS设置流程(2)

29.3.18 外部连接电路示例

图29.27显示了自供电系统中的示例OTG连接。USBHS控制D+线的上拉电阻和D+、D线的下拉电阻。为SYSCFG.DPRPU和SYSCFG.DRPD位中的线路选择上拉和下拉。在设备控制器模式下，如果在与USB主机通信时将SYSCFG.DPRPU位设置为0，则禁用USB数据线的上拉电阻。USBHS可以使用它来通知USB主机设备断开连接。

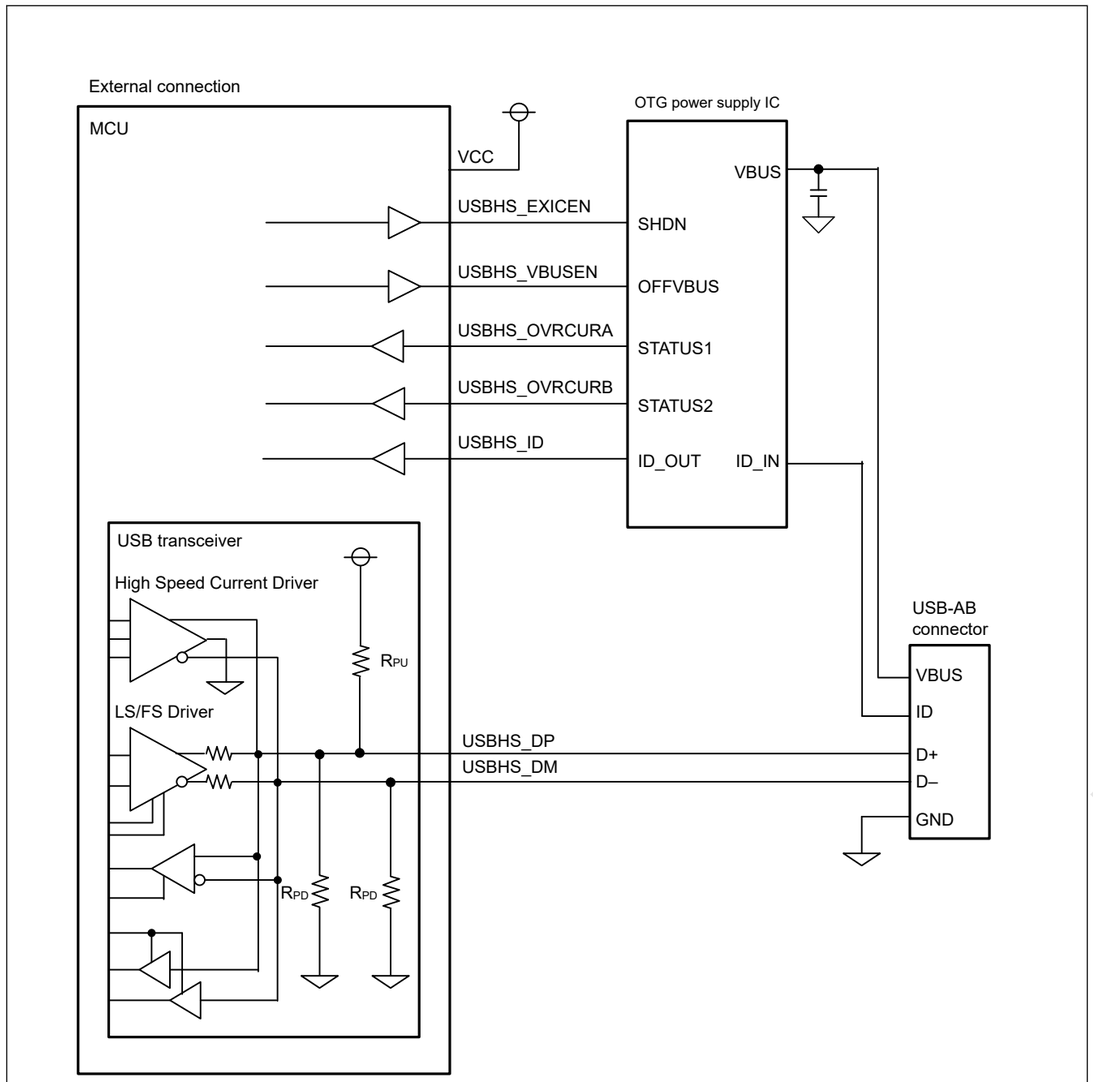


Figure 29.27 Example OTG connection in a self-powered system

Figure 29.28Figure 33.28 shows an example USB device connection in a self-powered system.

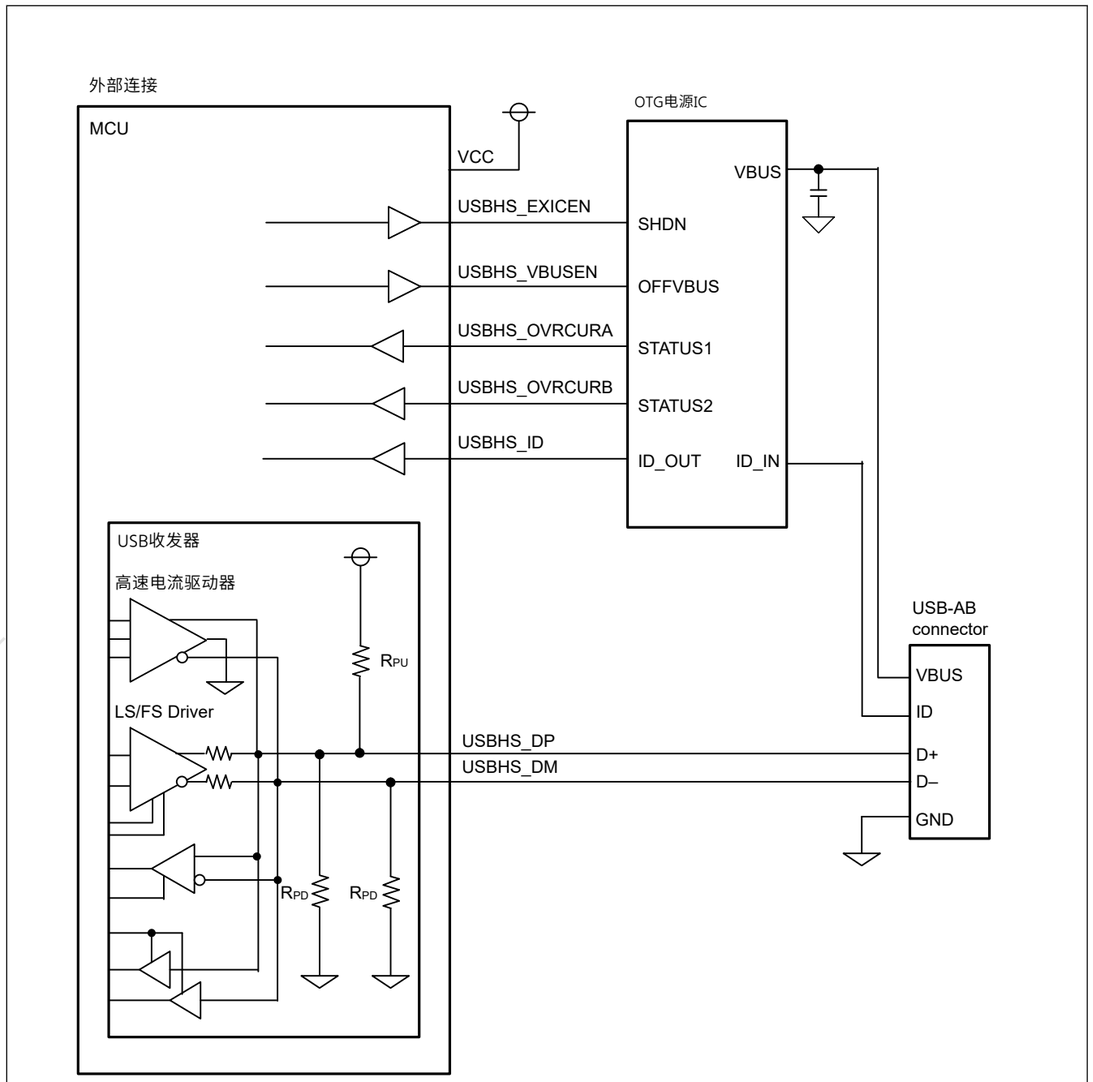
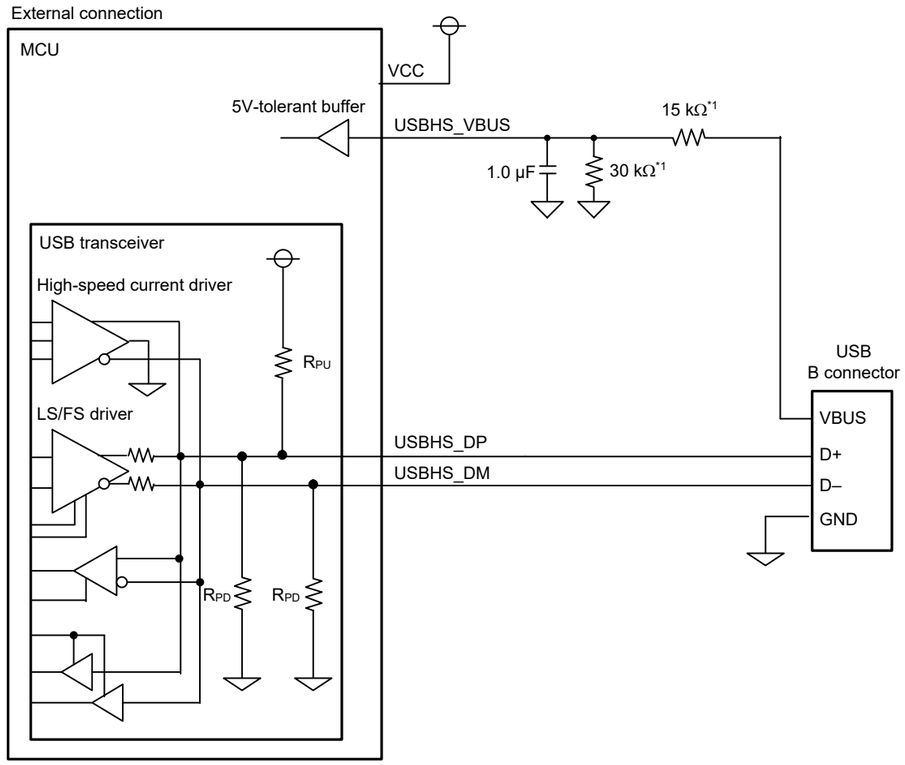


Figure 29.27 自供电系统中的示例OTG连接

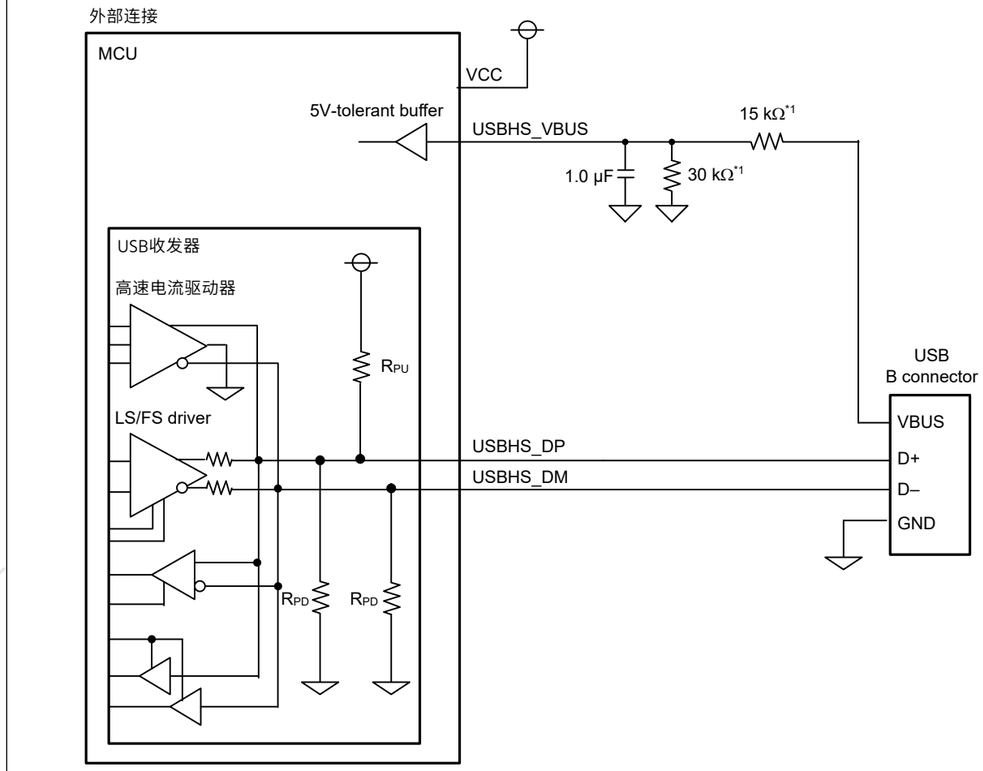
图29.28图33.28显示了自供电系统中的USB设备连接示例。



Note 1. The VBUS (5 V) can be directly connected to the MCU if the VCC power supply of the MCU is not turned off when the USB is connected. If the VCC power supply of the MCU is turned off, the VBUS should be less than 3.6 V.

Figure 29.28 Example device connection in self-powered system

Figure 29.29 shows an example USB device connection in a bus-powered system.



注1.VBUS(5V)可以直接连接到MCU的VCC电源如果没有关闭MCU时当USB已连接。如果关闭MCU的VCC电源，则VBUS应小于3.6V。

Figure 29.28 自供电系统中的示例设备连接

图29.29显示了总线供电系统中的USB设备连接示例。

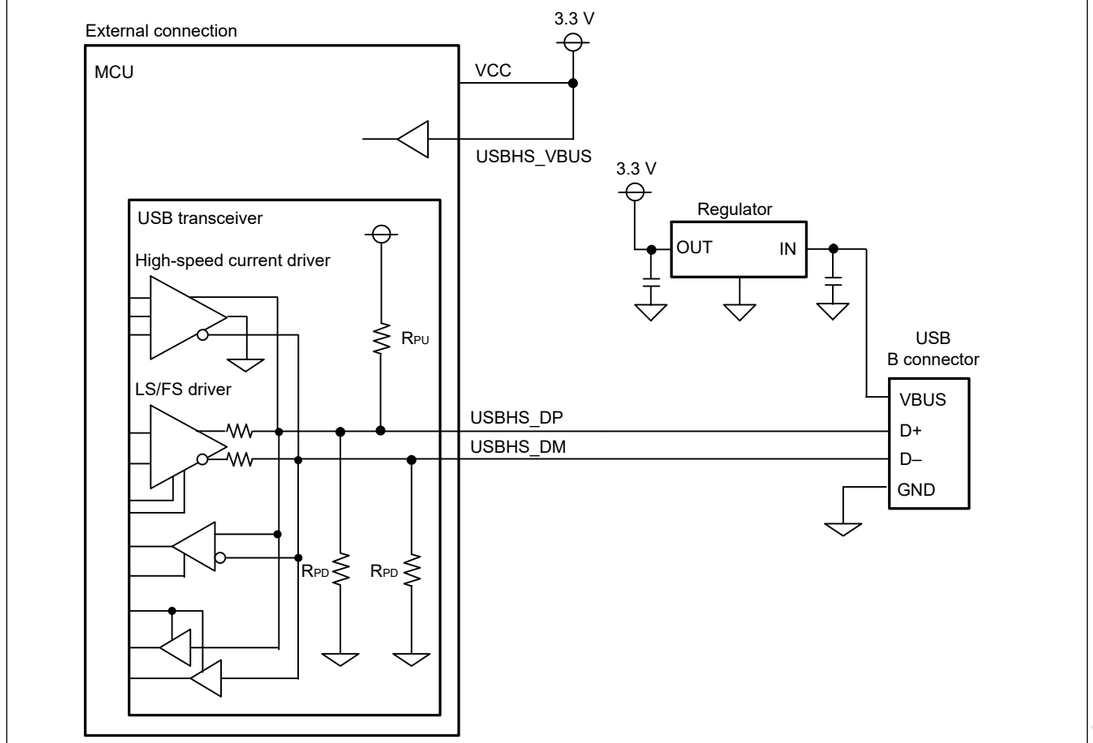


Figure 29.29 Example device connection in a bus-powered system

Figure 29.30 shows an example USB host connection.

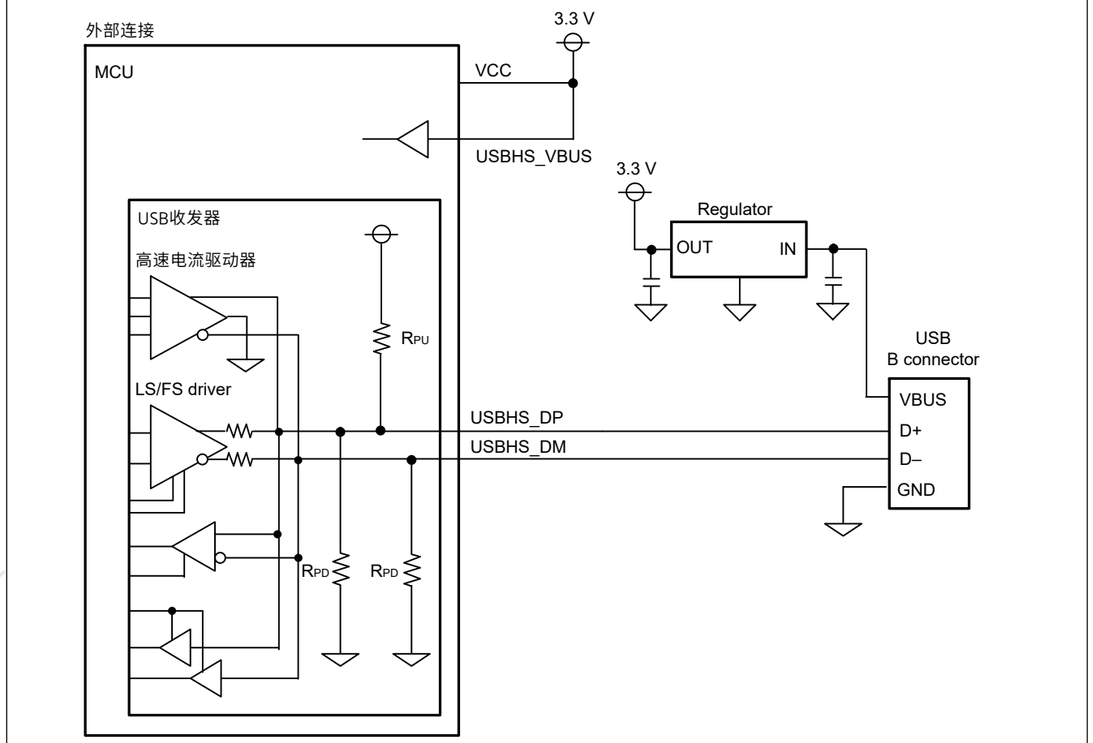


Figure 29.29 总线供电系统中的示例设备连接

图29.30显示了一个示例USB主机连接。

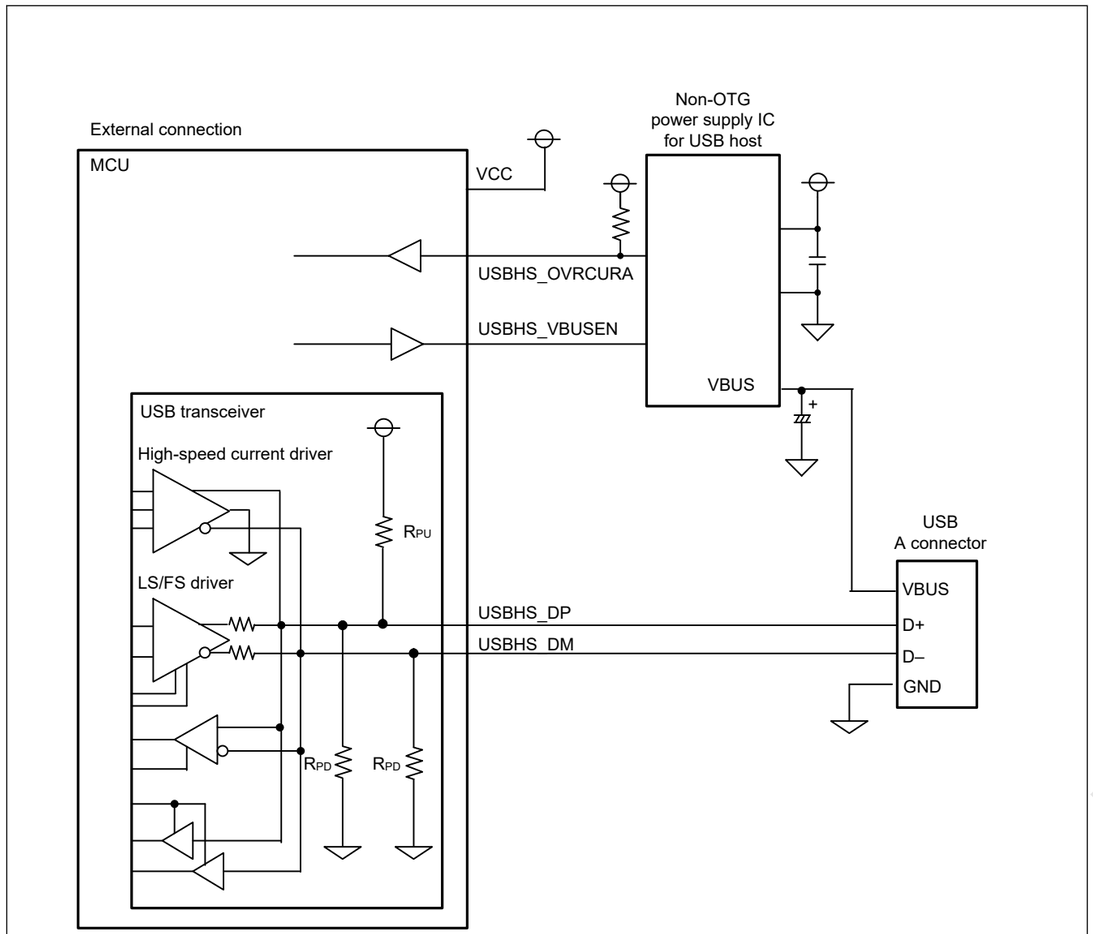


Figure 29.30 Example USB host connection

29.4 Usage Notes

29.4.1 Settings for the Module-Stop Function

USBHS operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The USBHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. After releasing module stop, make settings required to activate the PHY circuit, including the input system clock frequency setting, and then clear the PHYSET.DIRPD bit to 0. For details, see section 10, Low Power Modes .

29.4.2 Setup for Transitioning to Deep Software Standby Mode

Before transitioning to Deep Software Standby mode, clear the DVSTCTR0.VBUSEN bit to 0.

29.4.3 Clearing the Interrupt Status Register on Exiting Software Standby Mode

Because the input buffer is always enabled in Software Standby mode, an unexpected interrupt might occur under the following conditions:

- When the interrupt is enabled in Normal mode

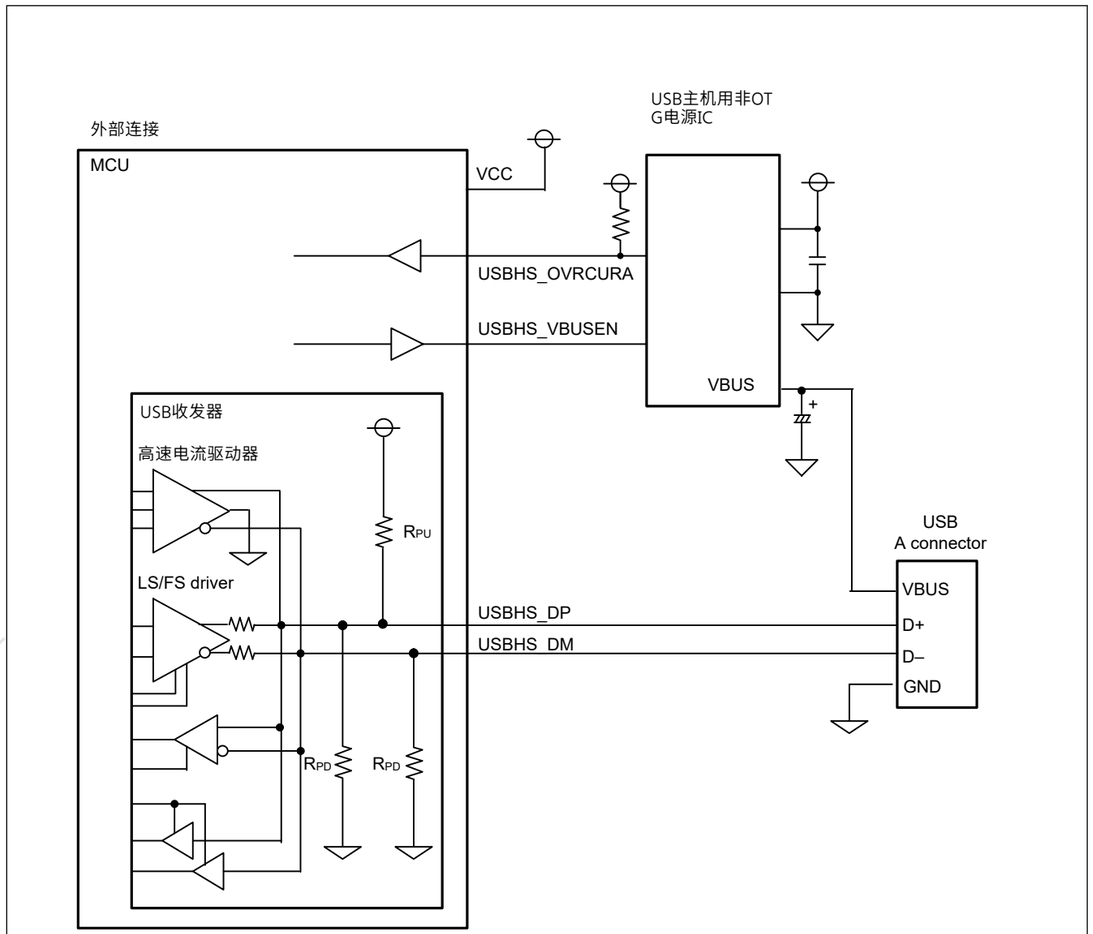


Figure 29.30 示例USB主机连接

29.4 使用说明

29.4.1 模块停止功能的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用USBHS操作。USBHS在复位后最初停止。释放模块停止状态可以访问寄存器。解除模块停止后，进行激活PHY电路所需的设置，包括输入系统时钟频率设置，然后将PHYSET.DIRPD位清为0。详细信息请参见第10节，低功耗模式。

29.4.2 转换到深度软件待机模式的设置

在转换到深度软件待机模式之前，将DVSTCTR0.VBUSEN位清零。

29.4.3 退出软件待机模式时清除中断状态寄存器

由于在软件待机模式下始终启用输入缓冲区，因此在以下情况下可能会发生意外中断：

●在正常模式下使能中断时

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- When the interrupt is disabled in Software Standby mode
- When the input level of the pin that cancels Software Standby is changed in Software Standby mode

These conditions might cause the associated interrupt flag in the Interrupt Status Register to set unexpectedly. After the MCU exits the Software Standby mode, the unexpected interrupt might be sent to the interrupt controller. To avoid this, always clear the INTSTS0 and INTSTS1 registers in the canceling sequence.

29.4.4 Clearing the Interrupt Status Register after Setting Up the Port Function

The input buffer is disabled before the PmnPFS.PSEL and PmnPFS.PMR ports are set up, so the internal signal is fixed high or low. The input buffer is enabled after the port is set so that the external pin state is propagated to the MCU. An unexpected interrupt might occur at this time, causing the VBINT and OVRCR bits in INTSTS0 and INTSTS1, or other interrupt status flags to set to 1. To avoid a malfunction, always clear the INTSTS0 and INTSTS1 registers after setting up the port.

●在软件待机模式下禁用中断时

●在软件待机模式下，取消软件待机的引脚的输入电平发生变化时

这些情况可能会导致中断状态寄存器中的相关中断标志意外设置。MCU退出软件待机模式后，可能会向中断控制器发送意外中断。为避免这种情况，请始终在取消序列中清除INTSTS0和INTSTS1寄存器。

29.4.4 设置端口功能后清除中断状态寄存器

在设置PmnPFS.PSEL和PmnPFS.PMR端口之前，输入缓冲器被禁用，因此内部信号固定为高或低。设置端口后启用输入缓冲器，以便将外部引脚状态传播到MCU。此时可能会发生意外中断，导致INTSTS0和INTSTS1中的VBINT和OVRCR位或其他中断状态标志设置为1。为避免故障，请务必在设置端口后清除INTSTS0和INTSTS1寄存器。

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30. Serial Communications Interface (SCI)

30.1 Overview

The Serial Communications Interface (SCI) × 10 channels have asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface
- Manchester interface
- Extended Serial interface

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3 to 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

In this section, PCLK refers to PCLKA.

Table 30.1 lists the SCI specifications, Figure 30.1 shows a block diagram of SCI, and Table 30.3 lists the I/O pins.

Table 30.1 SCI specifications (1 of 3)

Parameter		Specifications
Number of modules		10 (SCIn (n = 0 to 9))
Serial communication modes		• Asynchronous • Clock synchronous • Simple IIC • Simple SPI • Smart card interface • Manchester interface (SCIn (n = 3, 4)) • Extended Serial interface (SCIn (n = 1, 2))
Transfer speed		Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering
Data transfer		Selectable as LSB-first or MSB-first transfer
Inverter for communication terminals (RXDn, TXDn)		Selectable inverter for each terminals (RXDn, TXDn) (SCIn (n = 0, 3 to 9)
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, receive data ready*, address match*. (* SCIn (n = 0, 3 to 9) support) Completion of generation of a start condition, restart condition, or stop condition. (for simple IIC mode)
Module-stop function		Module-stop state can be set for each channel
Snooze end request		SCI0 address mismatch (SCI0_DCUF)
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO (only SCIn (n = 0, 3 to 9) supports FIFO)
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Adjustment of receive sampling timing	Adjustable receive sampling timing before/after the default timing

30. 串行通信接口(SCI)

30.1 Overview

串行通信接口(SCI)×10通道具有异步和同步串行接口：

●异步接口（UART和异步通信接口适配器(ACIA)）

●8位时钟同步接口

- Simple IIC (master-only)

●简单的SPI

●智能卡接口

●曼彻斯特接口

●扩展串行接口

智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。SCIn(n=0 3to9)具有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。

在本节中，PCLK指的是PCLKA。

表30.1列出了SCI规格，图30.1显示了SCI的框图，表30.3列出了IO引脚。

Table 30.1 SCI规范(1of3)

Parameter		Specifications
模块数量		10 (SCIn (n = 0 to 9))
串行通信模式		• Asynchronous • 时钟同步 • Simple IIC • 简单的SPI • 智能卡接口 • 曼彻斯特接口(SCIn(n=3 4)) • 扩展串行接口(SCIn(n=1 2))
传输速度		可通过片上波特率发生器指定比特率
Full-duplex communications		• 发送器：可使用双缓冲进行连续传输 • 接收器：使用双缓冲可以连续接收
数据传输		可选择LSB优先或MSB优先传输
通信终端用变频器（RXDn、TXDn）		每个端子(RXDn TXDn)的可选逆变器(SCIn(n=0 3to9)
中断源		发送结束、发送数据空、接收数据满、接收错误、接收数据就绪*、地址匹配*。(*SCIn(n=0 3to9)support)完成启动条件、重启条件或停止条件的生成。（对于简单IIC模式）
Module-stop function		每个通道可设置模块停止状态
暂停结束请求		SCI0地址不匹配(SCI0_DCUF)
时钟同步模式	数据长度	8 bits
	接收错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO（仅SCIn(n=0 3to9)支持FIFO)
异步模式	数据长度	7、8或9位
	传输停止位	1或2位
	接收采样时序的调整	默认时序后可调接收采样时序

Table 30.1 SCI specifications (2 of 3)

Parameter		Specifications
	Adjustment of transmit timing	Adjustable edge timing of transmit waveform controlled by the setting value of registers.
	Parity	Even parity, odd parity, or no parity
	Receive error detection	• Parity error • Overrun error • Framing error
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO (SCIn (n = 0, 3 to 9) supports FIFO)
	Address match	Interrupt request/event output can be issued upon detecting a match between received data and the value in the compare match register (SCIn (n = 0, 3 to 9) support)
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued when detecting a mismatch between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by read from SPTR register
	Clock source	Selectable to internal or external clock Transfer rate clock input from the GPT can be used. (SCIn (n = 1, 2)
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled among multiple processors
	Noise cancellation	Digital noise filters included on signal paths from the RXDn pin inputs
Smart card interface mode	Error processing	Error signal can be automatically transmitted upon detecting a parity error during reception
		Data can be automatically retransmitted upon receiving an error signal during transmission
	Data type	Both direct and inverse convention supported
Manchester mode	Communication format	Manchester code with the preface and the Start Bit added
	Data length	7,8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, framing, Manchester errors
	Hardware flow control	CTSn and RTSn pins can be used in controlling transmission
	Clock source	Only internal clock can be used.
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communication function	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters
	Preface setting / detection function	The function outputs the configured the preface pattern and detects it.
	Start Bit setting / detection function	The function outputs the configured the Start Bit pattern and detects it.
	Reception retiming function	Timing correction is performed for each bit of the received signal
Simple IIC mode	Transfer format	IIC bus format (MSB-first only)
	Operating mode	Master (single-master operation only)

Table 30.1 SCI规范(2of3)

Parameter		Specifications
	发射时序的调整	由寄存器的设定值控制的可调整的发送波形边沿时序。
	Parity	偶校验、奇校验或无校验
	接收错误检测	• 奇偶校验错误 • 溢出错误 • 构图错误
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO(SCIn(n=0 3to9)支持FIFO)
	地址匹配	检测到接收数据与比较匹配寄存器中的值匹配时，可以发出中断请求事件输出（支持SCIn（n=0 3to9））
	地址不匹配（仅SCI0）接收数据	当检测到接收到的数据与比较匹配寄存器中的值不匹配时，可以发出贪睡结束请求
	Start-bit detection	可选择低电平或下降沿检测
	断线检测	通过从SPTR寄存器读取可检测到的帧错误中断
	时钟源	可选择内部或外部时钟 可以使用来自GPT的传输速率时钟输入。(SCIn(n=1 2)
	Double-speed mode	波特率发生器双速模式可选
	多处理器通讯功能	在多个处理器之间启用串行通信
	噪音消除	来自RXDn引脚输入的信号路径上包含数字噪声滤波器
智能卡接口方式	错误处理	在接收过程中检测到奇偶校验错误时可以自动发送错误信号
		传输过程中接收到错误信号可自动重传数据
	数据类型	支持直接和反向约定
曼彻斯特模式	通讯格式	添加了前言和起始位的曼彻斯特代码
	数据长度	7 8或9位
	传输停止位	1或2位
	奇偶校验函数	偶校验、奇校验或无校验
	接收错误检测	奇偶校验、超限、成帧、曼彻斯特错误
	硬件流控制	CTSn和RTSn引脚可用于控制传输
	时钟源	只能使用内部时钟。
	Double-speed mode	波特率发生器双速模式可选
	多处理器通讯功能	多个处理器之间的串行通信
	噪音消除	来自RXDn引脚输入的信号路径包含数字噪声滤波器
	前言设定检测功能	该函数输出配置的序言模式并检测它。
	起始位设置检测功能	该函数输出配置的起始位模式并检测它。
	接收重定时功能	对接收信号的每一位进行定时校正
简单IIC模式	传输格式	IIC总线格式（仅MSB优先）
	操作模式	主机（仅限单主机操作）

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Table 30.1 SCI specifications (3 of 3)

Parameter		Specifications
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	SSn input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high.
	Clock settings	Configurable among four clock phase and clock polarity settings
Extended serial mode	Start Frame transmission	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection
	Start Frame reception	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Function for measuring bit rates
	I/O control function	• Selectable polarity for TXDXn and RXDXn signals • Selection of a digital filter for the RXDXn signal • Half-duplex operation employing RXDXn and TXDXn signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDXn • Signals received on RXDXn can be passed though to SCIn (n = 1, 2) when the extended serial mode control section is off.
	Timer function	• Usable as a reloading timer
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output for receive error or error signal detection (SCIn_ERI) (n = 0 to 9)
		Receive data full event output (SCIn_RXI) (n = 0 to 9)
		Transmit data empty event output (SCIn_TXI) (n = 0 to 9)
		Address match event output (SCIn_AM) (n = 0, 3 to 9)
		Transmit end event output (SCIn_TEI) (n = 0 to 9)
TrustZone Fileter		Security attribution can be set for each channels

Table 30.2 Functions of SCI Channel (1 of 2)

Item	SCI0, SCI5 to SCI9	SCI3, SCI4	SCI1, SCI2
Asynchronous mode	Available	Available	Available
Clock synchronous mode	Available	Available	Available
Smart card interface mode	Available	Available	Available
Simple I2C mode	Available	Available	Available
Simple SPI mode	Available	Available	Available
FIFO mode	Available	Available	Not Available
Address match	Available	Available	Not Available

Table 30.1 SCI规范（3个中的3个）

Parameter		Specifications
	传输率	高达400kbps
	噪音消除	来自SCLn和SDAn引脚输入的信号路径包含数字噪声滤波器，并提供可调节的噪声消除间隔
简单SPI模式	数据长度	8 bits
	错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	SSn输入引脚功能	通过将SSn引脚驱动为高电平，可以在输出引脚上调用高阻抗状态。
	时钟设置	可在四个时钟相位和时钟极性设置之间进行配置
扩展串行模式	开始帧传输	• 在指定宽度上输出低电平作为中断字段并在完成时生成中断 • 检测总线冲突并在检测时产生中断
	开始帧接收	• 检测中断字段低宽度并在检测时产生中断 • 比较控制字段0和1并在两者匹配时产生中断 • 可以设置两种比较数据（主要和次要）控制字段1。 • 可以在控制字段1中设置优先级中断位。 • 处理不包含中断字段的起始帧 • 不包含控制字段0的起始帧的处理 • 测量比特率的功能
	IO控制功能	• TXDXn和RXDXn信号的可选极性 • 为RXDXn信号选择数字滤波器 • 采用在同一引脚上复用的RXDXn和TXDXn信号的半双工操作 • 通过RXDXn接收的数据采样的可选时序 • 当扩展串行模式控制部分关闭时，RXDXn上接收的信号可以传递到SCIn(n=1 2)。
	定时器功能	• 可用作重新加载计时器
比特率调制功能		通过校正片上波特率发生器的输出来减少错误
事件链接功能		接收错误或错误信号检测的错误事件输出(SCIn_ERI)(n=0到9)
		接收数据满事件输出(SCIn_RXI)(n=0to9)
		发送数据空事件输出(SCIn_TXI)(n=0to9)
		地址匹配事件输出(SCIn_AM)(n=0 3to9)
		发送结束事件输出(SCIn_TEI)(n=0to9)
TrustZone Fileter		可以为每个通道设置安全属性

Table 30.2 SCI频道的功能(1of2)

Item	SCI0, SCI5 to SCI9	SCI3, SCI4	SCI1, SCI2
异步模式	Available	Available	Available
时钟同步模式	Available	Available	Available
智能卡接口方式	Available	Available	Available
简单I2C模式	Available	Available	Available
简单SPI模式	Available	Available	Available
FIFO mode	Available	Available	无法使用
地址匹配	Available	Available	无法使用

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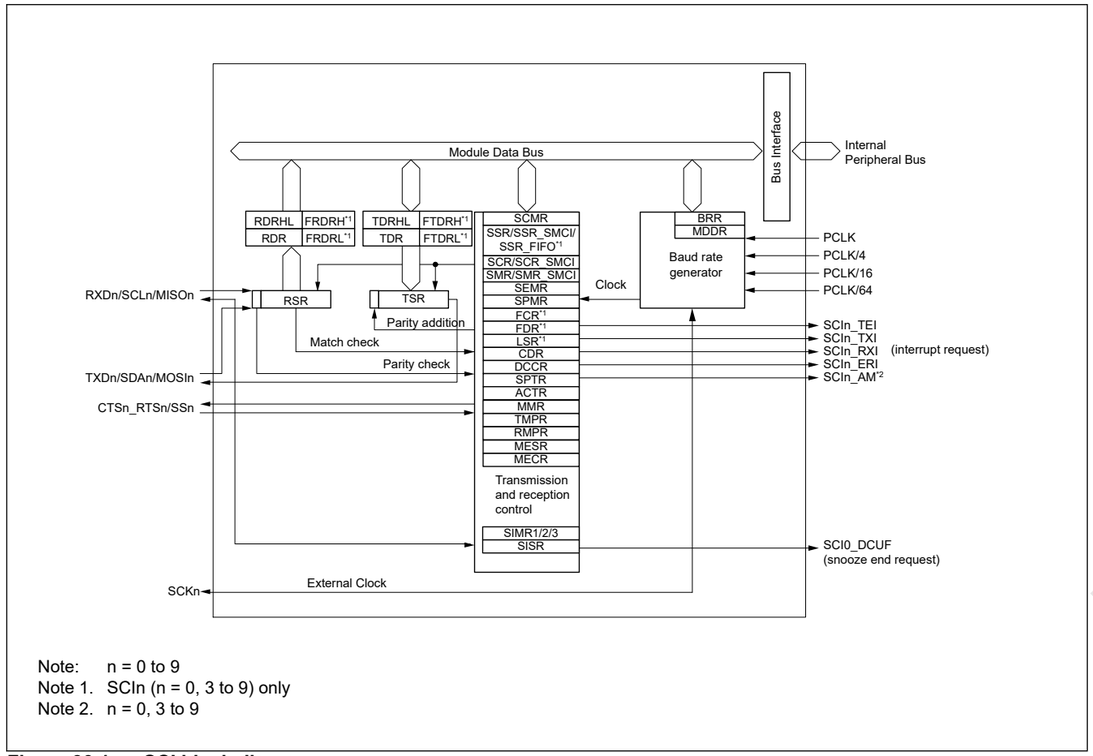
Table 30.2 Functions of SCI Channel (2 of 2)

Item	SCI0, SCI5 to SCI9	SCI3, SCI4	SCI1, SCI2
Manchester mode	Not Available	Available	Not Available
Extended serial mode	Not Available	Not Available	Available
GPT clock input	Not Available	Not Available	Available

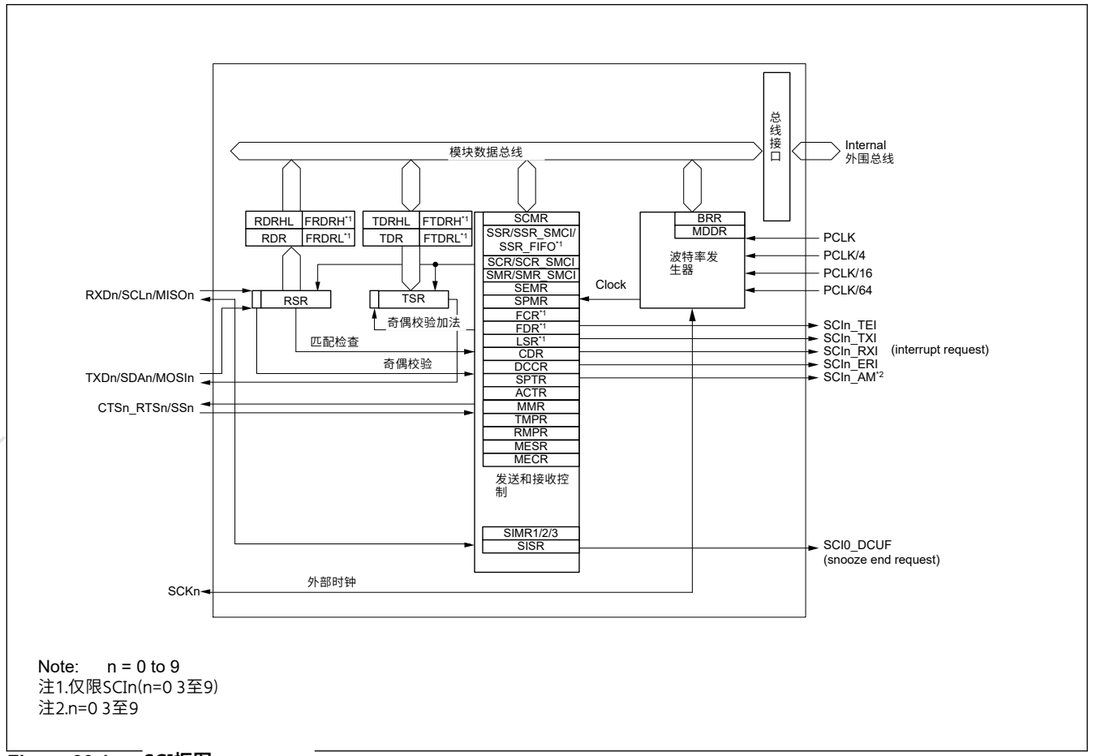


Note: n = 0 to 9
Note 1. SCIn (n = 0, 3 to 9) only
Note 2. n = 0, 3 to 9

Figure 30.1 SCI block diagram

Table 30.2 SCI频道的功能(2of2)

Item	SCI0, SCI5 to SCI9	SCI3, SCI4	SCI1, SCI2
曼彻斯特模式	无法使用	Available	无法使用
扩展串行模式	无法使用	无法使用	Available
GPT时钟输入	无法使用	无法使用	Available



Note: n = 0 to 9
注1.仅限SCIn(n=0 3至9)
注2.n=0 3至9

Figure 30.1 SCI框图

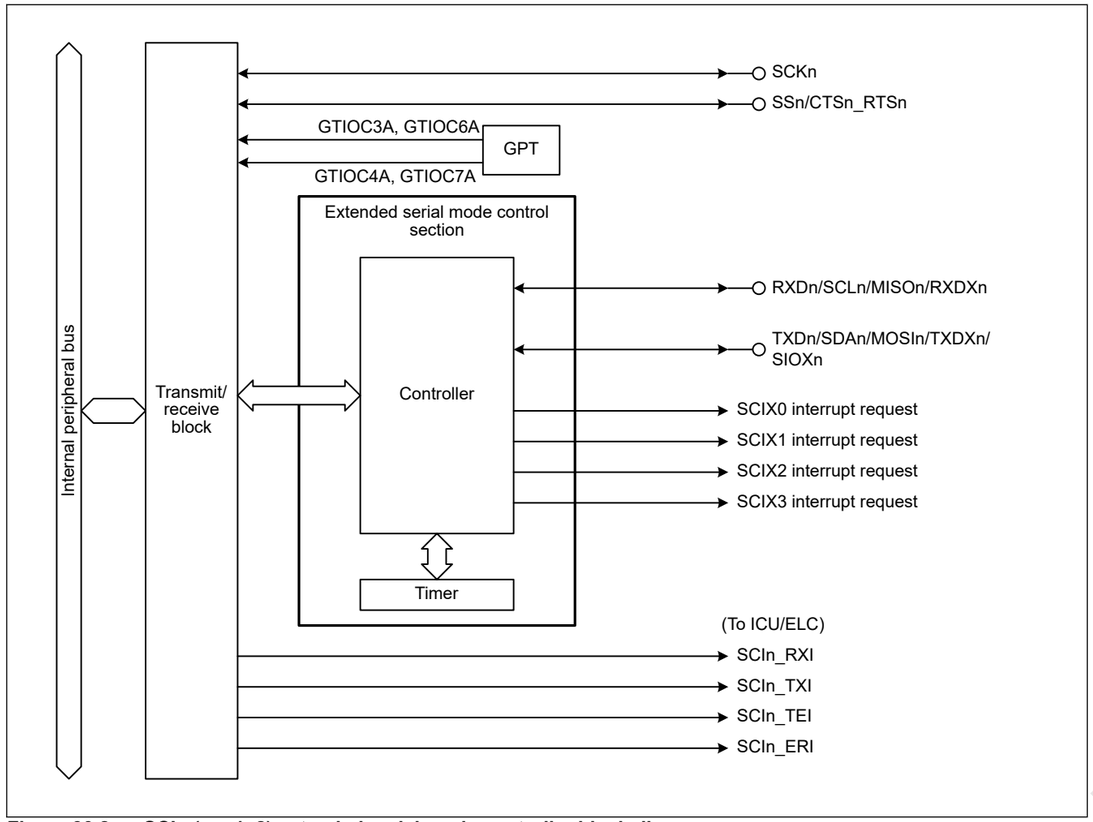


Figure 30.2 SCIn (n = 1, 2) extended serial mode controller block diagram

Table 30.3 SCI I/O pins

Function	Pin name	Input/ Output	Description
SCIn (n = 0 to 9)	RXDn/SCLn/MISOn	Input/ Output	SCIn receive data input SCIn I2C clock input/output SCIn slave transmit data input/output
	TXDn/SDAn/MOSIn	Input/ Output	SCIn transmit data output SCIn I2C data input/output SCIn master transmit data input/output
	SSn/CTSn_RTSn	Input/ Output	SCIn chip select input, active-low SCIn transfer start control input/output, active-low
	CTSn (n = 0, 3 to 9)	Input	SCIn transfer start control input, active-low
	RXDXn (n = 1, 2)	Input/ Output	SCIn receive data input (Extended Serial Mode)
	TXDXn/SIOXn (n = 1, 2)	Input/ Output	SCIn transmit data output (Extended Serial Mode) SCIn transmit data input/output (Extended Serial Mode)
	SCKn	Input/ Output	SCIn clock input/output

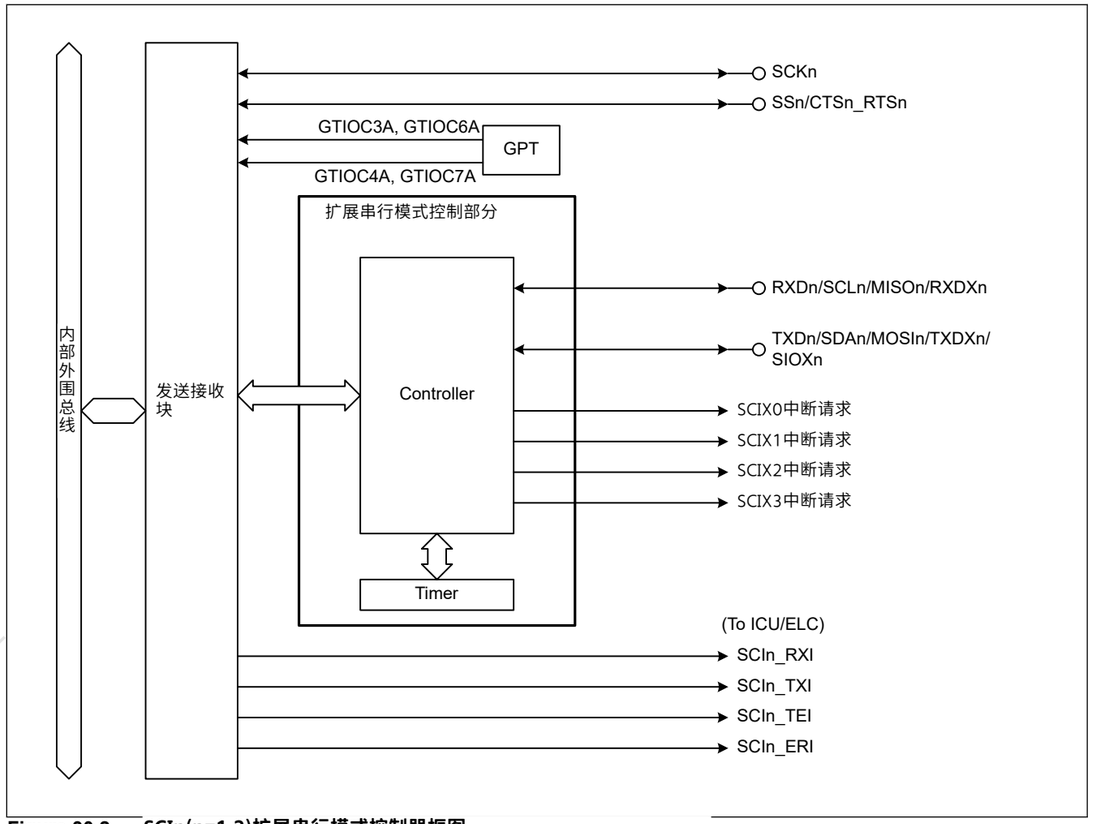


Figure 30.2 SCIn(n=1 2)扩展串行模式控制器框图

Table 30.3 SCIIO引脚

Function	引脚名称	Input/ Output	Description
SCIn (n = 0 to 9)	RXDn/SCLn/MISOn	Input/ Output	SCIn接收数据输入 SCIn I2C clock input/output SCIn从机发送数据输入输出
	TXDn/SDAn/MOSIn	Input/ Output	SCIn发送数据输出SCInI2C 数据输入输出 SCIn主机发送数据输入输出
	SSn/CTSn_RTSn	Input/ Output	SCIn片选输入，低电平有效 SCIn传输开始控制输入输出，低电平有效
	CTSn (n = 0, 3 to 9)	Input	SCIn传输开始控制输入，低电平有效
	RXDXn (n = 1, 2)	Input/ Output	SCIn接收数据输入（扩展串行模式）
	TXDXn/SIOXn (n = 1, 2)	Input/ Output	SCIn发送数据输出（扩展串行模式） SCIn传输数据输入输出（扩展串行模式）
	SCKn	Input/ Output	SCIn clock input/output

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30.2 Register Descriptions

30.2.1 RSR : Receive Shift Register

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, the data is automatically transferred to the RDR, RDRHL, or the receive FIFO register. The RSR register cannot be directly accessed by the CPU.

30.2.2 RDR : Receive Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores received data. When one frame of serial data is received, it is transferred from RSR to RDR, and the RSR register can receive more data. Because RSR and RDR function as a double buffer, continuous received operations can be performed.

Read the RDR only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next frame of data is received before reading the received data from RDR, an overrun error occurs. The CPU cannot write to the RDR.

30.2.3 RDRHL : Receive Data Register for Non-Manchester mode (MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial Receive Data	R
15:9	—	These bits are read as 0.	R

RDRHL is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are the shadow register of RDR, so access to RDRHL affects the RDR register. Access to the RDRHL register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to the RDR/RDRHL registers, allowing the RSR register to receive more data.

The RSR and RDRHL registers form a double-buffered structure to enable continuous reception. RDRHL should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL. The CPU cannot write to the RDRHL register.

30.2 注册说明

30.2.1 RSR:接收移位寄存器

RSR是一个移位寄存器，它接收从RXDn引脚输入的串行数据并将其转换为并行数据。当接收到一帧数据时，数据会自动传输到RDR、RDRHL或接收FIFO寄存器。CPU不能直接访问RSR寄存器。

30.2.2 RDR:接收数据寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

RDR是一个8位寄存器，用于存储接收到的数据。当接收到一帧串行数据时，将其从RSR传输到RDR，而RSR寄存器可以接收更多的数据。由于RSR和RDR用作双缓冲器，因此可以执行连续接收操作。

在接收数据完全中断(SCIn_RXI)发生后，仅读取一次RDR。

Note: 如果在从RDR读取接收到的数据之前接收到下一帧数据，则会发生溢出错误。CPU无法写入RDR。

30.2.3 RDRHL:非曼彻斯特模式的接收数据寄存器(MMR.MANEN=0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	串行接收数据	R
15:9	—	这些位读为0。	R

RDRHL是一个16位寄存器，用于存储接收到的数据。选择异步模式和9位数据长度时，请使用此寄存器。

RDRHL的低8位是RDR的影子寄存器，因此访问RDRHL会影响RDR寄存器。访问
如果选择7位或8位数据长度，则禁止RDRHL寄存器。

接收到一帧数据后，将接收到的数据从RSR寄存器传送到RDRRDRHL寄存器，使RSR寄存器可以接收更多数据。

RSR和RDRHL寄存器形成一个双缓冲结构以实现连续接收。只有在发出接收数据完全中断(SCIn_RXI)请求时才应读取RDRHL。在从RDRHL读取接收到的数据之前接收到下一帧数据时，会发生溢出错误。CPU无法写入RDRHL寄存器。

30.2.4 RDRHL_MAN : Receive Data Register for Manchester mode (MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RSYNC	—	—	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial receive data It can read serial receive data	R
9	MPB	Multi-processor bit It can read multi-processor bit corresponded to serial receive data (RDATA[8:0]) 0: Data transmission cycles 1: ID transmission cycles	R
11:10	—	These bits are read as 0. The write value should be 0.	R
12	RSYNC	Receive SYNC data bit It is valid when MMR.SBSEL = 1 in Manchester mode, 0 is read otherwise. 0: The received the Start Bit is DATA SYNC 1: The received the Start Bit is COMMAND SYNC	R
15:13	—	These bits are read as 0. The write value should be 0.	R

RDRHL_MAN is a 16-bit register that stores received data. Use this register when asynchronous mode and 9-bit data length are selected. The lower 8 bits of RDRHL_MAN are the shadow register of RDR, so access to RDRHL_MAN affects the RDR register. Access to the RDRHL_MAN register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to the RDR/RDRHL_MAN registers, allowing the RSR register to receive more data.

The RSR and RDRHL_MAN registers form a double-buffered structure to enable continuous reception.

RDRHL_MAN should be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from RDRHL_MAN.

The CPU cannot write to the RDRHL_MAN register.

RDAT[8:0] bit (Serial receive data)

It can read serial receive data.

MPB bit (Multi-processor bit)

Holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

RSYNC bit (Receive SYNC data bit)

When Manchester mode and MMR.SBSEL = "1", this bit indicates the type of SYNC of the received the Start Bit. For other settings, it is fixed to 0.

30.2.5 FRDRHL/FRDRH/FRDRL : Receive FIFO Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x10 (FRDRHL/FRDRH)
0x11 (FRDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

30.2.4 RDRHL_MAN：曼彻斯特模式的接收数据寄存器（MMR.MANEN=1）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	RSYNC	—	—	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	串口接收数据 可读取串口接收数据	R
9	MPB	Multi-processor bit 它可以读取对应于串行接收数据的多处理器位（RDATA[8:0]） 0：数据传输周期1：ID传输周期	R
11:10	—	这些位被读取为0。写入值应为0。	R
12	RSYNC	接收同步数据位 曼彻斯特模式下MMR.SBSEL=1时有效，否则读取0。 0：接收的起始位为DATASYNC1：接收的起始位为COMMANDSYNC	R
15:13	—	这些位被读取为0。写入值应为0。	R

RDRHL_MAN是一个16位寄存器，用于存储接收到的数据。选择异步模式和9位数据长度时，请使用此寄存器。RDRHL_MAN的低8位是RDR的影子寄存器，因此访问RDRHL_MAN会影响RDR寄存器。如果选择7位或8位数据长度，则禁止访问RDRHL_MAN寄存器。

接收到一帧数据后，将接收到的数据从RSR寄存器传送到RDRRDRHL_MAN寄存器，从而允许RSR寄存器接收更多数据。

RSR和RDRHL_MAN寄存器形成一个双缓冲结构以实现连续接收。

只有在发出接收数据完全中断(SCIn_RXI)请求时，才应读取RDRHL_MAN。在从RDRHL_MAN读取接收到的数据之前接收到下一帧数据时，会发生溢出错误。

CPU无法写入RDRHL_MAN寄存器。

RDAT[8:0]位（串行接收数据）

它可以读取串行接收数据。

MPB bit (Multi-processor bit)

保存接收帧中多处理器位的值。当SCR.RE位为0时，该位不变。

RSYNC位（接收SYNC数据位）

当曼彻斯特模式和MMR.SBSEL="1"时，该位指示接收到的StartBit的SYNC类型。对于其他设置，它固定为0。

30.2.5 FRDRHLFRDRHFRDRL:接收FIFO数据寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x10 (FRDRHL/FRDRH)
0x11 (FRDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	Serial receive data Stores the serial receive data. Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected.	R
9	MPB	Multi-Processor Bit Flag Stores the value of the multi-processor bit in the serial receive data, RDAT[8:0]. Valid only in asynchronous mode with SMR.MP = 1, and with FIFO selected. 0: Data transmission cycle 1: ID transmission cycle	R
10	DR	Receive Data Ready Flag This flag is the same as SSR_FIFO.DR. 0: Receiving is in progress, or no received data remains in the FRDRH and FRDRL registers after successfully completed reception 1: Next receive data is not received for a period after successfully completed reception	R*1
11	PER	Parity Error Flag 0: No parity error occurred in the first data of FRDRH and FRDRL 1: Parity error occurred in the first data of FRDRH and FRDRL	R
12	FER	Framing Error Flag 0: No framing error occurred in the first data of FRDRH and FRDRL 1: Framing error occurred in the first data of FRDRH and FRDRL	R
13	ORER	Overrun Error Flag This flag is the same as SSR_FIFO.ORER. 0: No overrun error occurred 1: Overrun error occurred	R*1
14	RDF	Receive FIFO Data Full Flag This flag is the same as SSR_FIFO.RDF. 0: The amount of receive data written in FRDRH and FRDRL is less than the specified receive triggering number 1: The amount of receive data written in FRDRH and FRDRL is equal to or greater than the specified receive triggering number	R*1
15	—	This bit is read as 0.	R

Note 1. If this flag is read, it indicates the same value as that read from the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of the 8-bit FRDRH and FRDRL registers. FRDRH is assigned to the FRDRHL[15:8] bits, and allocated to the same address as FRDRHL. FRDRL is assigned to the FRDRHL[7:0] bits, and allocated to (the address of FRDRHL + 1) address.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information readable by software. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

The SCI completes reception of one frame of serial data by transferring the received data from the Receive Shift Register (RSR) into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full, subsequent serial receive data is lost. The CPU can read from the FRDRH and FRDRL registers but cannot write to them.

Reading 1 from the RDF, ORER, or DR flags of the FRDRH register is the same as reading from those bits in the SSR_FIFO register. When writing 0 to clear a flag in the SSR_FIFO register after reading the FRDRH register, write 0 only to the flag that is to be cleared and write 1 to the other flags.

When reading both the FRDRH and FRDRL registers, read in order from FRDRH to FRDRL. The FRDRHL register can be accessed in 16-bit units.

Bit	Symbol	Function	R/W
8:0	RDAT[8:0]	串口接收数据 存储串行接收数据。仅在异步模式下有效，包括多处理器模式和时钟同步模式，并且选择了FIFO。	R
9	MPB	多处理器位标志 将多处理器位的值存储在串行接收数据RDAT[8:0]中。仅在SMR.MP=1且选择了FIFO的异步模式下有效。 0：数据发送周期1：ID发送周期	R
10	DR	接收数据就绪标志 该标志与SSR_FIFO.DR相同。 0：接收中，或成功完成接收后，FRRDH和FRDRL寄存器中没有接收到的数据 1：接收成功后一段时间内没有接收到下一个接收数据	R*1
11	PER	奇偶校验错误标志 0：FRRDH和FRDRL的第一个数据没有发生奇偶校验错误1：FRRDH和FRDRL的第一个数据发生奇偶校验错误	R
12	FER	成帧错误标志 0：FRRDH和FRDRL的第一个数据没有发生帧错误1：FRRDH和FRDRL的第一个数据发生了帧错误	R
13	ORER	溢出错误标志 该标志与SSR_FIFO.ORER相同。 0：未发生溢出错误1：发生溢出错误	R*1
14	RDF	接收FIFO数据满标志 该标志与SSR_FIFO.RDF相同。 0：FRRDH和FRRDL写入的接收数据量小于指定的接收触发数 1：写入FRRDH和FRRDL的接收数据量等于或大于指定的接收触发数	R*1
15	—	该位读为0。	R

注1.如果读取该标志，则表示与从SSR_FIFO寄存器读取的值相同。将0写入SSR_FIFO寄存器以清除标志。

FRDRHL是一个16位寄存器，由8位FRDRH和FRDRL寄存器组成。FRDRH被分配到FRDRHL[15:8]位，并分配到与FRDRHL相同的地址。FRDRL分配给FRDRHL[7:0]位，并分配给（FRDRHL+1的地址）地址。

FRDRH和FRDRL构成一个16级FIFO寄存器，用于存储串行接收数据和软件可读的相关状态信息。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

SCI通过将接收到的数据从接收移位寄存器（RSR）传送到FRDRH和FRDRL中进行存储，从而完成一帧串行数据的接收。执行连续接收，直到存储16个阶段。如果在FRDRH和FRDRL中没有接收到数据时读取数据，则该值未定义。当FRDRH和FRDRL已满时，后续的串行接收数据会丢失。CPU可以读取FRDRH和FRDRL寄存器，但不能写入它们。

从FRDRH寄存器的RDF、ORER或DR标志读取1与从SSR_FIFO寄存器。在读取FRDRH寄存器后写入0以清除SSR_FIFO寄存器中的标志时，仅将0写入要清除的标志，将1写入其他标志。

读取FRDRH和FRDRL寄存器时，按从FRDRH到FRDRL的顺序读取。FRDRHL寄存器可以以16位为单位进行访问。

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30.2.6 TDR : Transmit Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	Serial Transmit Data	R/W

TDR is an 8-bit register that stores transmit data.

When the SCI detects that the TSR register is empty, it transfers the transmit data written in the TDR register to the TSR register and starts transmission.

The double-buffered structure of the TDR and TSR registers enables continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to the TSR register to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

30.2.7 TDRHL : Transmit Data Register for Non-Manchester mode (MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial Transmit Data	R/W
15:9	—	This bit is read as 1. The write value should be 1.	R/W

TDRHL is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are the shadow register of TDR, so access to TDRHL affects the TDR register. Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL registers is transferred to TSR and transmission starts.

The TSR and TDRHL registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation continues by transferring the data to the TSR register.

The CPU can read and write to the TDRHL register. Bits [15:9] in TDRHL are fixed to 1. These bits are read as 1. The write value should be 1.

Write transmit data to theTDRHL register only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

30.2.6 TDR：发送数据寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	串行传输数据	R/W

TDR是一个8位寄存器，用于存储发送数据。

当SCI检测到TSR寄存器为空时，将写入TDR寄存器的发送数据传送到TSR寄存器并开始发送。

TDR和TSR寄存器的双缓冲结构可实现连续串行传输。如果在发送一帧数据时，下一个发送数据已经写入TDR，则SCI将写入的数据传输到TSR寄存器继续发送。

CPU可以随时读取或写入TDR。每次发送数据空中断(SCIn_TXI)后，仅将发送数据写入TDR一次。

30.2.7 TDRHL：非曼彻斯特模式的发送数据寄存器（MMR.MANEN=0）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TDAT[8:0]								
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	串行传输数据	R/W
15:9	—	该位读取为1。写入值应为1。	R/W

TDRHL是一个16位寄存器，用于存储发送数据。选择异步模式和9位数据长度时，请使用此寄存器。

TDRHL的低8位是TDR的影子寄存器，因此访问TDRHL会影响TDR寄存器。访问
如果选择7位或8位数据长度，则禁止TDRHL寄存器。

当在TSR寄存器中检测到空空间时，存储在TDRHL寄存器中的发送数据被传送到TSR并开始发送。

TSR和TDRHL寄存器具有双缓冲结构以支持连续传输。当发送完一帧数据后，下一个要发送的数据存储在TDRHL中时，通过将数据传输到TSR寄存器来继续发送操作。

CPU可以读取和写入TDRHL寄存器。TDRHL中的位[15:9]固定为1。这些位被读取为1。写入值应为1。

当发送数据空中断(SCIn_TXI)请求发出时，仅将发送数据写入TDRHL寄存器一次。

30.2.8 TDRHL_MAN : Transmit Data Register for Manchester mode (MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n(n = 3, 4)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSYNC	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial transmit data It can set serial transmit data	R/W
9	MPBT	Multi-processor transfer bit flag Value of the multi-processor bit in the transmission frame 0: Data transmission cycles 1: ID transmission cycles	R/W
11:10	—	The write value should be 1.	R
12	TSYNC	Transmit SYNC data bit It is valid when MMR.SBSEL = 1 and MMR.SYNSEL = 1 in Manchester mode. 0: The Start Bit is transmitted as DATA SYNC. 1: The Start Bit is transmitted as COMMAND SYNC.	R/W
15:13	—	The write value should be 1.	R

TDRHL_MAN is a 16-bit register that stores transmit data. Use this register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL_MAN are the shadow register of TDR, so access to TDRHL_MAN affects the TDR register. Access to the TDRHL_MAN register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL_MAN registers is transferred to TSR and transmission starts.

The TSR and TDRHL_MAN registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL_MAN after one frame of data is transmitted, the transmitting operation continues by transferring the data to the TSR register.

Write transmit data to theTDRHL_MAN register only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

TDAT[8:0] bit (Serial transmit data)

This register sets serial transmission data.

MPBT bit (Multi-processor transfer bit flag)

Selects the multi processor bit of transmit frame.

TSYNC bit (Transmit SYNC data bit)

When Manchester mode and MMR.SBSEL = "1" and MMR.SYNSEL = "1",the type of SYNC selected according to this bit becames the Start Bit of the transmission frame.

30.2.8 TDRHL_MAN：曼彻斯特模式的发送数据寄存器（MMR.MANEN=1）

Base address: SCIn = 0x4011_8000 + 0x0100 × n(n = 3, 4)

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TSYNC	—	—	MPBT	TDAT[8:0]								
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	串行传输数据 可设置串口发送数据	R/W
9	MPBT	多处理器传输位标志 传输帧中多处理器位的值 0：数据传输周期1：ID传输周期	R/W
11:10	—	写入值应为1。	R
12	TSYNC	发送SYNC数据位 在曼彻斯特模式下，当MMR.SBSEL=1和MMR.SYNSEL=1时有效。 0：起始位作为DATASYNC发送。1：起始位作为COMMANDSYNC发送。	R/W
15:13	—	写入值应为1。	R

TDRHL_MAN是一个16位寄存器，用于存储发送数据。选择异步模式和9位数据长度时，请使用此寄存器。

TDRHL_MAN的低8位是TDR的影子寄存器，因此访问TDRHL_MAN会影响TDR寄存器。
如果选择7位或8位数据长度，则禁止访问TDRHL_MAN寄存器。

当在TSR寄存器中检测到空空间时，存储在TDRHL_MAN寄存器中的发送数据被传输到TSR和传输开始。

TSR和TDRHL_MAN寄存器具有双缓冲结构以支持连续传输。当下一个要发送的数据在发送一帧数据后存储在TDRHL_MAN中时，通过将数据传输到TSR寄存器来继续发送操作。

当发出发送数据空中断(SCIn_TXI)请求时，仅将发送数据写入TDRHL_MAN寄存器一次。

TDAT[8:0]位（串行发送数据）

该寄存器设置串行传输数据。

MPBT位（多处理器传输位标志）

选择发送帧的多处理器位。

TSYNC位（发送SYNC数据位）

当曼彻斯特模式和MMR.SBSEL="1"且MMR.SYNSEL="1"时，根据该位选择的SYNC类型成为传输帧的起始位。

30.2.9 FTDRHL/FTDRH/FTDRL : Transmit FIFO Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x0E (FTDRHL/FTDRH)
0x0F (FTDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MPBT	TDAT[8:0]								
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	Serial transmit data Specifies the serial transmit data. Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected.	W
9	MPBT	Multi-Processor Transfer Bit Flag Specifies the multi-processor bit in the transmission frame. Valid only in asynchronous mode and SMR.MP = 1, and with FIFO selected.Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected. 0: Data transmission cycle 1: ID transmission cycle	W
15:10	—	The write value should be 1.	W

FTDRHL is a 16-bit register that consists of the 8-bit FTDRH and FTDRL registers. FTDRH is assigned to the FTDRHL[15:8] bits, and allocated to the same address as FTDRHL. FTDRL is assigned to the FTDRHL[7:0] bits, and allocated to (the address of FTDRHL + 1) address.

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and a multi-processor transfer bit. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

When the SCI detects that the Transmit Shift Register (TSR) is empty, it transfers data written in the FTDRH and FTDRL registers to the TSR register and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDRHL is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to the FTDRH and FTDRL registers but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in order from FTDRH to FTDRL.

TDAT[8:0] bits (Serial transmit data)

The TDAT[8:0] bits set the serial transmission data. This is valid only when FIFO is selected in asynchronous mode (including multiprocessor) or clock synchronous mode.

MPBT flag (Multi-Processor Transfer Bit Flag)

The MPBT flag specifies the value of the multi-processor bit of the transmit frame. When FCR.FM = 1, SSR.MPBT is invalid.

30.2.10 TSR : Transmit Shift Register

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to TSR, then sends the data to the TXDn pin. The CPU cannot directly access the TSR.

30.2.9 FTDRHLFTDRHFTDRL:发送FIFO数据寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x0E (FTDRHL/FTDRH)
0x0F (FTDRL)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	MPBT	TDAT[8:0]								
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
8:0	TDAT[8:0]	串行传输数据 指定串行传输数据。 仅在异步模式下有效，包括多处理器模式和时钟同步模式，并且选择了FIFO。	W
9	MPBT	多处理器传输位标志 指定传输帧中的多处理器位。仅在异步模式和SMR.MP=1且选择FIFO时有效。仅在异步模式下有效，包括多处理器模式和时钟同步模式，并选择FIFO。 0：数据发送周期1：ID发送周期	W
15:10	—	写入值应为1。	W

FTDRHL是一个16位寄存器，由8位FTDRH和FTDRL寄存器组成。FTDRH分配给FTDRHL[15:8]位，并分配到与FTDRHL相同的地址。FTDRL分配给FTDRHL[7:0]位，并分配给（FTDRHL的地址+1）地址。

FTDRH和FTDRL构成一个16级FIFO寄存器，用于存储串行传输的数据和一个多处理器传输位。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

当SCI检测到传输移位寄存器(TSR)为空时，它将写入FTDRH和FTDRL寄存器的数据传输到TSR寄存器并开始串行传输。执行连续串行传输，直到在FTDRH和FTDRL中没有剩余传输数据。当FTDRHL充满传输数据时，不能再写入数据。如果尝试写入新数据，则忽略该数据。CPU可以写入FTDRH和FTDRL寄存器，但不能读取它们。

当同时写入FTDRH和FTDRL寄存器时，按照从FTDRH到FTDRL的顺序写入。

TDAT[8:0]位（串行发送数据）

TDAT[8:0]位设置串行传输数据。这仅在异步模式（包括多处理器）或时钟同步模式下选择FIFO时有效。

MPBT标志（多处理器传输位标志）

MPBT标志指定发送帧的多处理器位的值。FCR.FM=1时，SSR.MPBT无效。

30.2.10 TSR：发送移位寄存器

TSR是传送串行数据的移位寄存器。为了进行串行数据传输，SCI首先自动将发送数据从TDR、TDRHL或发送FIFO传输到TSR，然后将数据发送到TXDn引脚。CPU不能直接访问TSR。

30.2.11 SMR : Serial Mode Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	Clock Select 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*4
2	MP	Multi-Processor Mode Valid only in asynchronous mode. 0: Disable multi-processor communications function 1: Enable multi-processor communications function	R/W*4
3	STOP	Stop Bit Length Valid only in asynchronous mode. 0: 1 stop bit 1: 2 stop bits	R/W*4
4	PM	Parity Mode Valid only when the PE bit is 1. 0: Even parity 1: Odd parity	R/W*4
5	PE	Parity Enable Valid only in asynchronous mode. 0: When transmitting: Do not add parity bit When receiving: Do not check parity bit 1: When transmitting: Add parity bit When receiving: Check parity bit	R/W*4
6	CHR	Character Length Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SCMR.CHR1 bit. 0: SCMR.CHR1 = 0: Transmit/receive in 9-bit data length SCMR.CHR1 = 1: Transmit/receive in 8-bit data length (initial value) 1: SCMR.CHR1 = 0: Transmit/receive in 9-bit data length SCMR.CHR1 = 1: Transmit/receive in 7-bit data length*3	R/W*4
7	CM	Communication Mode 0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode	R/W*4

Note 1. n is the decimal notation of the value of n in the BRR register. See section 30.2.20. BRR : Bit Rate Register.
Note 2. In any mode other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB (bit [7]) in the TDR register is not transmitted in transmit mode.
Note 4. Writable only when SCR.TE = 0 and SCR.RE = 0 (both serial transmission and reception are disabled).

The SMR register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 30.2.20. BRR : Bit Rate Register.

30.2.11 SMR：非智能卡接口模式的串行模式寄存器（SCMR.SMIF=0）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	时钟选择 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*4
2	MP	Multi-Processor Mode 仅在异步模式下有效。 0：禁用多机通讯功能1：启用多机通讯功能	R/W*4
3	STOP	停止位长度 仅在异步模式下有效。 0：1个停止位1 ：2个停止位	R/W*4
4	PM	奇偶校验模式 仅在PE位为1时有效。 0：偶校验1： 奇校验	R/W*4
5	PE	奇偶校验使能 仅在异步模式下有效。 0：发送时：不加校验位接收时：不校验校 验位 1：发送时：添加校验位接收时：校 验校验位	R/W*4
6	CHR	字符长度 仅在异步模式下有效。*2 结合SCMR.CHR1位选择发送接收字符长度。 0：SCMR.CHR1=0：发送接收9位数据长度 SCMR.CHR1=1：发送接收8位数据长度（初始值） 1：SCMR.CHR1=0：发送接收9位数据长度SCMR.CHR1=1： 发送接收7位数据长度*3	R/W*4
7	CM	通讯方式 0：异步模式或简单IIC模式1：时钟同步模式或简 单SPI模式	R/W*4

注1.n是BRR寄存器中n值的十进制表示法。请参阅第30.2.20节。BRR：比特率寄存器。
注2.在异步模式以外的任何模式下，该位设置无效，使用8位的固定数据长度。
注3.LSB-first是固定的，并且TDR寄存器中的MSB（位[7]）在发送模式下不发送。
注4.仅当SCR.TE=0且SCR.RE=0时可写（串行发送和接收均禁用）。

SMR寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0] bits (Clock Select)

CKS[1:0]位选择片内波特率发生器的时钟源。关于这些位的设置与波特率的关系，请参见第30.2.20节。BRR：比特率寄存器。

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MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The PE and PM bit settings are invalid in multi-processor mode.

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception. The PM bit setting is invalid in multiprocessor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception. Regardless of the PE bit setting, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the SCMR.CHR1 bit. In modes other than asynchronous, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode

30.2.12 SMR_SMCI : Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	Clock Select 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*2
3:2	BCP[1:0]	Base Clock Pulse Selects the number of base clock cycles in combination with the SCMR.BCP2 bit. Table 30.4 lists the combinations of the SCMR.BCP2 and SMR.BCP[1:0] bits.	R/W*2
4	PM	Parity Mode Valid only when the PE bit is 1. 0: Even parity 1: Odd parity	R/W*2
5	PE	Parity Enable When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2

MP bit (Multi-Processor Mode)

MP位禁用或启用多处理器通信功能。PE和PM位设置在多处理器模式下无效。

停止位（停止位长度）

STOP位选择传输中的停止位长度。

在接收中，无论该位设置如何，都只检查第一个停止位。如果第二个停止位为0，则将其视为下一个发送帧的起始位。

PM bit (Parity Mode)

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。PM位设置在多处理器模式下无效。

PE位（奇偶校验使能）

当PE位设置为1时，发送数据时添加奇偶校验位，接收时检查奇偶校验位。无论PE位设置如何，在多处理器格式中都不会添加或检查奇偶校验位。

CHR bit (Character Length)

CHR位与SCMR.CHR1位一起选择发送和接收的数据长度。在非异步模式下，使用8位的固定数据长度。

CM bit (Communication Mode)

CM位选择通信模式：

●异步模式或简单IIC模式

●时钟同步模式或简单SPI模式

30.2.12 SMR_SMCI：智能卡接口模式的串行模式寄存器(SCMR.SMIF=1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKS[1:0]	时钟选择 0 0: PCLK clock (n = 0)*1 0 1: PCLK/4 clock (n = 1)*1 1 0: PCLK/16 clock (n = 2)*1 1 1: PCLK/64 clock (n = 3)*1	R/W*2
3:2	BCP[1:0]	基本时钟脉冲 结合SCMR.BCP2位选择基本时钟周期数。表30.4列出了SCMR.BCP2和SMR.BCP[1:0]位的组合。	R/W*2
4	PM	奇偶校验模式 仅在PE位为1时有效。 0：偶校验1： 奇校验	R/W*2
5	PE	奇偶校验使能 当该位设置为1时，发送数据时添加一个奇偶校验位，并检查接收数据的奇偶校验。在智能卡接口模式下将此位设置为1。	R/W*2

Bit	Symbol	Function	R/W
6	BLK	Block Transfer Mode 0: Normal mode operation 1: Block transfer mode operation	R/W*2
7	GM	GSM Mode 0: Normal mode operation 1: GSM mode operation	R/W*2

Note 1. n is the decimal notation of the value of n in the BRR register. See section 30.2.20. BRR : Bit Rate Register.
Note 2. Writable only when SCR_SMCI.TE = 0 and SCR_SMCI.RE = 0 (both serial transmission and reception are disabled).

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 30.2.20. BRR : Bit Rate Register.

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set these bits in combination with the SCMR.BCP2 bit.

For details, see section 30.7.4. Receive Data Sampling Timing and Reception Margin.

Table 30.4 Combinations of SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period*1
0	00b	93 clock cycles (S = 93)
0	01b	128 clock cycles (S = 128)
0	10b	186 clock cycles (S = 186)
0	11b	512 clock cycles (S = 512)
1	00b	32 clock cycles (S = 32) (initial value)
1	01b	64 clock cycles (S = 64)
1	10b	372 clock cycles (S = 372)
1	11b	256 clock cycles (S = 256)

Note 1. S is the value of S in BRR (see section 30.2.20. BRR : Bit Rate Register).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd). For details on the usage of this bit in smart card interface mode, see section 30.7.2. Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1. The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK bit (Block Transfer Mode)

Setting the BLK bit to 1 enables block transfer mode operation. For details, see section 30.7.3. Block Transfer Mode.

GM bit (GSM Mode)

Setting the GM bit to 1 enables GSM mode operation. In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETUs (elementary time unit = 1-bit transfer time) from the start bit, and clock output control is added. For details, see section 30.7.6. Serial Data Transmission (Except in Block Transfer Mode) and section 30.7.8. Clock Output Control.

Bit	Symbol	Function	R/W
6	BLK	块传输模式 0：正常模式操作1：块传输模式操作	R/W*2
7	GM	GSM Mode 0：正常模式操作1：GSM模式操作	R/W*2

注1.n是BRR寄存器中n值的十进制表示法。请参阅第30.2.20节。BRR：比特率寄存器。
注2.仅当SCR_SMCI.TE=0且SCR_SMCI.RE=0时可写（串行发送和接收均禁用）。

SMR_SMCI寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0] bits (Clock Select)

CKS[1:0]位选择片内波特率发生器的时钟源。关于这些位的设置与波特率的关系，请参见第30.2.20节。BRR：比特率寄存器。

BCP[1:0]位（基本时钟脉冲）

BCP[1:0]位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将这些位与SCMR.BCP2位一起设置。

有关详细信息，请参阅第30.7.4节。接收数据采样时序和接收余量。

Table 30.4 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数*1
0	00b	93个时钟周期(S=93)
0	01b	128个时钟周期(S=128)
0	10b	186个时钟周期(S=186)
0	11b	512个时钟周期(S=512)
1	00b	32个时钟周期(S=32)（初始值）
1	01b	64个时钟周期(S=64)
1	10b	372个时钟周期(S=372)
1	11b	256个时钟周期(S=256)

注1.S是BRR中S的值（参见第30.2.20节。BRR：比特率寄存器）。

PM bit (Parity Mode)

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。关于该位在智能卡接口模式下的使用详情，请参见第30.7.2节。数据格式（块传输模式除外）。

PE位（奇偶校验使能）

将PE位设置为1。发送数据前添加奇偶校验位，接收时校验奇偶校验位。

BLK位（块传输模式）

将BLK位设置为1可启用块传输模式操作。有关详细信息，请参见第30.7.3节。块传输模式。

GM bit (GSM Mode)

将GM位设置为1启用GSM模式操作。在GSM模式下，SSR_SMCI.TEND标志设置时序从起始位前移到11.0ETU（基本时间单位=1位传输时间），并添加了时钟输出控制。详见30.7.6节。串行数据传输（块传输模式除外）和第30.7.8节。时钟输出控制。

30.2.13 SCR : Serial Control Register for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	Clock Enable 0 0: In asynchronous mode, the SCKn pin is available for use as an I/O port based on the I/O port settings. In clock synchronous mode, the SCKn pin functions as the clock output pin. 0 1: In asynchronous mode, a clock with the same frequency as the bit rate is output from the SCKn pin. In clock synchronous mode, the SCKn pin functions as the clock output pin. Others: In asynchronous mode, input a clock with a frequency 16 times the bit rate from the SCKn pin when the SEMR.ABCS bit is 0. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. The SCKn pin is available for use as an I/O port based on the I/O port settings when the GPT clock*4 is used. In clock synchronous mode, the SCKn pin functions as the clock input pin.	R/W*1
2	TEIE	Transmit End Interrupt Enable 0: Disable SCIn_TEI interrupt requests 1: Enable SCIn_TEI interrupt requests	R/W
3	MPIE	Multi-Processor Interrupt Enable Valid in asynchronous mode when SMR.MP = 1. 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 and the status flags SYER, PFER, and SBER in MESR are disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and normal reception is resumed.	R/W*3
4	RE	Receive Enable 0: Disable serial reception 1: Enable serial reception	R/W*2
5	TE	Transmit Enable 0: Disable serial transmission 1: Enable serial transmission	R/W*2
6	RIE	Receive Interrupt Enable 0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests	R/W
7	TIE	Transmit Interrupt Enable 0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests	R/W

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0, when the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. When the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.
Note 3. When writing a new value to a bit other than the MPIE bit of this register in multi-processor mode (SMR.MP bit = 1), write 0 to the MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by a read-modify-write operation when using a bit manipulation instruction.
Note 4. GPT clock is selectable for SCI1 and SCI2.

The SCR register controls operation and clock source selection for transmission and reception.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and the SCKn pin function.

30.2.13 SCR：非智能卡接口模式的串行控制寄存器（SCMR.SMIF=0）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	时钟使能 00：在异步模式下，SCKn引脚可根据IO端口设置用作IO端口。在时钟同步模式下，SCKn引脚用作时钟输出引脚。 01：在异步模式下，从SCKn引脚输出与比特率相同频率的时钟。在时钟同步模式下，SCKn引脚用作时钟输出引脚。 其他：异步模式下，SEMR.ABCS位为0时，从SCKn管脚输入16倍比特率的时钟。SEMR.ABCS位为1时，输入8倍比特率的时钟信号.当使用GPT时钟*4时，SCKn引脚可根据IO端口设置用作IO端口。在时钟同步模式下，SCKn引脚用作时钟输入引脚。	R/W*1
2	TEIE	发送结束中断使能 0：禁用SCIn_TEI中断请求1：启用SCIn_TEI中断请求	R/W
3	MPIE	多处理器中断使能 当SMR.MP=1时在异步模式下有效。 0：正常接收1：接收多处理器位设置为0的数据时，不读取数据，将SSR中的状态标志RDRF、ORER和FER设置为1，并将状态标志SYER、PFER和MESR中的SBER被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动设置为0，并恢复正常接收。	R/W*3
4	RE	接收启用 0：禁用串口接收1：启用串口接收	R/W*2
5	TE	发送启用 0：禁用串口传输1：启用串口传输	R/W*2
6	RIE	接收中断使能 0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI和SCIn_ERI中断请求	R/W
7	TIE	发送中断使能 0：禁用SCIn_TXI中断请求1：启用SCIn_TXI中断请求	R/W

注1.仅当TE=0且RE=0时可写。
注2.只有当TE=0且RE=0时，当SMR.CM位为1时，才能写入1。将TE或RE设置为1后，TE和RE只能写入0。当SMR.CM位为0且SIMR1.IICM位为0时，在任何情况下都可以写入。
注3.在多处理器模式下（SMR.MP位=1）向该寄存器的MPIE位以外的位写入新值时，将0写入MPIE位使用存储指令以避免在使用位操作指令时通过读–修改–写操作意外将MPIE位设置为1。
注4.GPT时钟可选择用于SCI1和SCI2。

SCR寄存器控制发送和接收的操作和时钟源选择。

CKE[1:0] bits (Clock Enable)

CKE[1:0]位选择时钟源和SCKn引脚功能。

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TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables SCIn_TEI interrupt requests. Set TEIE to 0 to disable an SCIn_TEI interrupt request.

In simple IIC mode, SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags RDRF, ORER, FER, RDF, and DR in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically set to 0, and normal reception resumes. For details, see section 30.4. Multi-Processor Communication Function.

When the MPB bit in the SSR register is 0, the receive data is not transferred from the RSR register to the RDR register, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the MPB bit is set to 1, the MPIE bit is automatically set to 0, SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and setting of the ORER and FER flags to 1 is enabled.

Set MPIE to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Set the reception format in the SMR register before setting the RE bit to 1.

In non-FIFO operation, when reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER flags in the SSR register are not affected, and the previous values are retained.

When FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When the TE bit is set to 1, serial transmission is started by writing transmit data to the TDR register. Set the transmission format in the SMR register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

Note: To switch the TIE bit value from 0 to 1 in FIFO mode, set the TIE and TE bits to 1 simultaneously or set the TIE bit to 1 when TE = 1. When TE = 0 in FIFO mode, setting the TIE bit to 1 is prohibited.

TEIE位（发送结束中断允许）

TEIE位启用或禁用SCIn_TEI中断请求。将TEIE设置为0以禁用SCIn_TEI中断请求。

在简单IIC模式下，SCIn_TEI在完成发出启动、重新启动或停止条件(STIn)时分配给中断。
在这种情况下，TEIE位可用于启用或禁用STI。

MPIE位（多处理器中断允许）

当MPIE位设置为1并且接收到多处理器位设置为0的数据时，不读取数据并且将SSRSSR_FIFO中的状态标志RDRF、ORER、FER、RDF和DR设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动设置为0，并恢复正常接收。有关详细信息，请参阅第30.4节。多处理器通信功能。

当SSR寄存器的MPB位为0时，接收数据不会从RSR寄存器传送到RDR寄存器，不会检测到接收错误，并且将标志ORER和FER设置为1被禁止。

当MPB位设置为1时，MPIE位自动设置为0，允许SCIn_RXI和SCIn_ERI中断请求（如果SCR中的RIE位设置为1），并且允许设置ORER和FER标志为1.

如果不使用多处理器通信功能，则将MPIE设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。当RE位设置为1时，串行接收通过检测异步模式下的起始位或时钟同步模式下的同步时钟输入来启动。在将RE位设置为1之前，在SMR寄存器中设置接收格式。

在非FIFO操作中，当通过将RE位设置为0来停止接收时，RDRF、ORER、FER和PER标志
SSR寄存器不受影响，保留之前的值。

WhenFIFOoperationisselectedandreceptionishaltedbysettingtheREbitto0 theRDF ORER FER PER andDRflagsin SSR_FIFOarenotaffectedandthepreviousvaluesareretained.

TE位（发送使能）

TE位启用或禁用串行传输。

当TE位设置为1时，通过将发送数据写入TDR寄存器开始串行发送。在将TE位设置为1之前，在SMR寄存器中设置传输格式。

RIE位（接收中断允许）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

SCIn_ERI中断请求可以通过从SSRSSR_FIFO中的ORER、FER或PER标志读取1然后将该标志设置为0或通过将RIE位设置为0来取消。

TIE位（发送中断允许）

TIE位启用或禁用SCIn_TXI中断请求。通过将TIE位设置为0来禁用SCIn_TXI中断请求。

Note: 要在FIFO模式下将TIE位值从0切换为1，请将TIE和TE位同时设置为1，或者在TE=1时将TIE位设置为1。在FIFO模式下，当TE=0时，将TIE位设置为1是禁止。

30.2.14 SCR_SMCI : Serial Control Register for Smart Card Interface Mode (SCMR.SMIF = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	Clock Enable 0 0: When SMR_SMCI.GM = 0: Disable output The SCKn pin is available for use as an I/O port if set up in the I/O port settings When SMR_SMCI.GM = 1: Fix output low 0 1: When SMR_SMCI.GM = 0: Output clock When SMR_SMCI.GM = 1: Output clock 1 0: When SMR_SMCI.GM = 0: Setting prohibited When SMR_SMCI.GM = 1: Fix output high 1 1: When SMR_SMCI.GM = 0: Setting prohibited When SMR_SMCI.GM = 1: Output clock	R/W*1
2	TEIE	Transmit End Interrupt Enable Set this bit to 0 in smart card interface mode	R/W
3	MPIE	Multi-Processor Interrupt Enable Set this bit to 0 in smart card interface mode	R/W
4	RE	Receive Enable 0: Disable serial reception 1: Enable serial reception	R/W*2
5	TE	Transmit Enable 0: Disable serial transmission 1: Enable serial transmission	R/W*2
6	RIE	Receive Interrupt Enable 0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests	R/W
7	TIE	Transmit Interrupt Enable 0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests	R/W

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written to TE and RE.

The SCR_SMCI register sets transmission and reception control, interrupt control, and clock source selection for transmission and reception.

For details on interrupt requests, see section 30.12. Interrupt Sources.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin. In GSM mode, clock output can be dynamically switched. For details, see section 30.7.8. Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

Set the TEIE bit to 0 in smart card interface mode.

MPIE bit (Multi-Processor Interrupt Enable)

Set the MPIE bit to 0 in smart card interface mode.

30.2.14 SCR_SMCI：智能卡接口模式的串行控制寄存器(SCMR.SMIF=1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CKE[1:0]	时钟使能 00：当SMR_SMCI.GM=0时：禁用输出 如果在IO端口设置中设置SCKn引脚可用作IO端口 当SMR_SMCI.GM=1时：固定输出低 01：当SMR_SMCI.GM=0：输出时钟当SMR_S MCI.GM=1：输出时钟 10：当SMR_SMCI.GM=0时：禁止设置当SMR_SMC I.GM=1时：固定输出高 11：当SMR_SMCI.GM=0时：禁止设置当SMR_SMC I.GM=1时：输出时钟	R/W*1
2	TEIE	发送结束中断使能 在智能卡接口模式下将此位设置为0	R/W
3	MPIE	多处理器中断使能 在智能卡接口模式下将此位设置为0	R/W
4	RE	接收启用 0：禁用串口接收1：启用 串口接收	R/W*2
5	TE	发送启用 0：禁用串口传输1：启用串口 传输	R/W*2
6	RIE	接收中断使能 0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI 和SCIn_ERI中断请求	R/W
7	TIE	发送中断使能 0：禁用SCIn_TXI中断请求1：启用SCIn _TXI中断请求	R/W

注1.仅当TE=0且RE=0时可写。
注2.只有TE=0且RE=0时才能写入1。将TE或RE设置为1后，TE和RE只能写入0。

SCR_SMCI寄存器设置发送和接收的发送和接收控制、中断控制以及发送和接收的时钟源选择。

有关中断请求的详细信息，请参阅第30.12节。中断源。

CKE[1:0] bits (Clock Enable)

CKE[1:0]位控制SCKn引脚的时钟输出。在GSM模式下，时钟输出可以动态切换。
有关详细信息，请参阅第30.7.8节。时钟输出控制。

TEIE位（发送结束中断允许）

在智能卡接口模式下将TEIE位设置为0。

MPIE位（多处理器中断允许）

在智能卡接口模式下将MPIE位设置为0。

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit. Set the reception format in the SMR_SMCI register before setting the RE bit to 1.

If reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission. When the TE bit is set to 1, serial transmission is started by writing transmit data to TDR. Set the transmission format in the SMR_SMCI register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in the SSR_SMCI register, and then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0.

30.2.15 SSR : Serial Status Register for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0, FCR.FM = 0, and MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	Multi-Processor Bit Transfer Sets the value of the multi-processor bit in the transmission frame. 0: Data transmission cycle 1: ID transmission cycle	R/W
1	MPB	Multi-Processor Value of the multi-processor bit in the reception frame. 0: Data transmission cycle 1: ID transmission cycle	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/(W)*1
4	FER	Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/(W)*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/(W)*1

RE位（接收使能）

RE位启用或禁用串行接收。当RE位设置为1时，串行接收通过检测起始位开始。
在将RE位设置为1之前，在SMR_SMCI寄存器中设置接收格式。

如果通过将RE位设置为0来停止接收，则SSR_SMCI中的ORER、FER和PER标志不受影响，并且保留以前的值。

TE位（发送使能）

TE位启用或禁用串行传输。当TE位设置为1时，通过将发送数据写入TDR开始串行发送。在将TE位设置为1之前，在SMR_SMCI寄存器中设置传输格式。

RIE位（接收中断允许）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

通过从SSR_SMCI寄存器中的ORER、FER或PER标志读取1，然后将该标志设置为0，或将RIE位设置为0，可以取消SCIn_ERI中断请求。

TIE位（发送中断允许）

TIE位启用或禁用SCIn_TXI中断请求。通过将TIE位设置为0来禁用SCIn_TXI中断请求。

30.2.15 SSR：非智能卡接口和非FIFO模式的串行状态寄存器（SCMR.SMIF=0、FCR.FM=0和MMR.MANEN=0）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	多处理器位传输 设置传输帧中多处理器位的值。 0：数据发送周期1：ID发送周期	R/W
1	MPB	Multi-Processor 接收帧中多处理器位的值。 0：数据发送周期1：ID发送周期	R
2	TEND	发送结束标志 0：字符传输中1：字符传输完成	R
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1 ：发生奇偶校验错误	R/(W)*1
4	FER	成帧错误标志 0：未发生帧错误1：发生帧错误	R/(W)*1
5	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/(W)*1

Bit	Symbol	Function	R/W
6	RDRF	Receive Data Full Flag 0: No received data in RDR register 1: Received data in RDR register	R/(W)*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data in TDR register 1: No transmit data in TDR register	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides SCI status flags and transmission and reception multi-processor bits.

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit sets the value of the multi-processor bit in the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and the FCR.FM bit is set to 0 (non-FIFO selected). When the SCR.TE bit is set to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated on transmission of the tail-end bit of a character being transmitted.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR.TE bit is 1

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  Although receive data is transferred to the RDR register when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read the PER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  In 2-stop-bit mode, only the first stop bit is checked. The second stop bit is not checked. Although receive data is transferred to the RDR register when the framing error occurs, no SCIn_RXI interrupt request occurs. When the FER flag is to 1, the subsequent receive data is not transferred to the RDR register.

Bit	Symbol	Function	R/W
6	RDRF	接收数据满标志 0：RDR寄存器中没有接收到数据1： RDR寄存器中接收到数据	R/(W)*1
7	TDRE	传输数据空标志 0：在TDR寄存器中发送数据1：在T DR寄存器中不发送数据	R/(W)*1

注1.读1后只能写0清除标志。

SSR寄存器提供SCI状态标志和发送和接收多处理器位。

MPBT bit (Multi-Processor Bit Transfer)

MPBT位设置发送帧中多处理器位的值。

MPB bit (Multi-Processor)

MPB位保存接收帧中多处理器位的值。当SCR.RE位为0时，该位不变。

TEND标志（发送结束标志）

TEND标志表示传输完成。

[Setting conditions]

●当SCR.TE位设置为0（禁用串行传输）且FCR.FM位设置为0（选择非FIFO）时。当SCR.TE位设置为1时，TEND标志不受影响并保持值1。

●TDR寄存器未在发送字符的尾端位时更新时。

[Clearing conditions]

●当SCR.TE位为1时将发送数据写入TDR寄存器

●当SCR.TE位为1时，读取TDRE=1后向TDRE写入0

PER标志（奇偶校验错误标志）

PER标志表示在异步模式接收过程中发生奇偶校验错误，接收异常结束。

[Setting condition]

●当地址匹配功能被禁用（DCCR.DCME=0）时，在异步模式接收期间检测到奇偶校验错误。

尽管发生奇偶校验错误时接收数据被传送到RDR寄存器，但不会发生SCIn_RXI中断请求。当PER标志设置为1时，后续接收数据不会传送到RDR寄存器。

[Clearing condition]

●读取PER=1后向PER写入0时。将0写入PER标志后，读取PER标志以检查它是否实际设置为0。

当SCR.RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

FER标志（帧错误标志）

FER标志表示在异步模式下接收过程中发生了帧错误，并且接收异常结束。

[Setting condition]

●当地址匹配功能被禁用（DCCR.DCME=0）时，在异步模式接收期间采样0作为停止位时。

在2停止位模式下，仅检查第一个停止位。不检查第二个停止位。虽然发生帧错误时接收数据被传输到RDR寄存器，但不会发生SCIn_RXI中断请求。当FER标志为1时，后续接收数据不传送到RDR寄存器。

[Clearing condition]

- When 0 is written to FER after reading FER = 1. After writing 0 to the FER flag, read the FER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error and a framing error is read from the RDR register.

  The data received before an overrun error occurred is saved in the RDR register, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read the ORER flag to check that it is actually set to 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after reading RDRF = 1
- When data is forwarded from the RDR register

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When 0 is written to TDRE after reading TDRE = 1
- When the SCR.TE bit is 1 and data is written to the TDR register

30.2.16 SSR_FIFO : Serial Status Register for Non-Smart Card Interface and FIFO Mode (SCMR.SMIF = 0, FCR.FM = 1, and MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

[Clearing condition]

●当读取FER=1后向FER写入0时。将0写入FER标志后，读取FER标志以检查它是否实际设置为0。

当SCR.RE位设置为0（禁用串行接收）时，FER标志不受影响并保留其先前的值。

ORER标志（溢出错误标志）

ORER标志表示接收期间发生溢出错误，接收异常结束。

[Setting condition]

●在接收没有奇偶校验错误和帧错误的数据之前接收下一个数据时，从RDR寄存器中读取。

溢出错误发生前接收到的数据保存在RDR寄存器中，但错误发生后接收到的数据丢失。
当ORER标志设置为1时，接收数据不转发到RDR寄存器。在时钟同步模式下，串行发送和接收停止。

[Clearing condition]

●读取ORER=1后向ORER写入0时。向ORER标志写入0后，读取ORER标志以检查它是否实际设置为0。

当SCR.RE位设置为0（禁用串行接收）时，ORER标志不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

●接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

●读取RDRF=1后向RDRF写入0时

●从RDR寄存器转发数据时

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

●当SCR.TE位为0时

●当数据从TDR寄存器传送到TSR寄存器时

[Clearing conditions]

●读取TDRE=1后写入0时

●当SCR.TE位为1且数据写入TDR寄存器时

30.2.16 SSR_FIFO：非智能卡接口和FIFO模式的串行状态寄存器（SCMR.SMIF=0、FCR.FM=1和MMR.MANEN=0）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDFE	RDF	ORER	FER	PER	TEND	—	DR
重置后的值：	1	0	0	0	0	0	x	0

Bit	Symbol	Function	R/W
0	DR	Receive Data Ready Flag 0: Receiving is in progress, or no received data remains in FRDRHL after successfully completed reception (receive FIFO empty) 1: Next receive data is not received for a period after normal receiving is complete, when the amount of data stored in the FIFO is equal to or less than the receive triggering number	R/W*1
1	—	The read value is undefined. The write value should be 1.	R/W
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R/W*1
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	FER	Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/W*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
6	RDF	Receive FIFO Data Full Flag 0: The amount of receive data written in FRDRHL is less than the specified receive triggering number 1: The amount of receive data written in FRDRHL is equal to or greater than the specified receive triggering number	R/W*1
7	TDFE	Transmit FIFO Data Empty Flag 0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number	R/W*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_FIFO register provides the SCI with FIFO mode status flags.

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number, and that no next data is received after 15 ETUs (elementary time units) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, when FIFO operation is selected.

In clock synchronous mode, the DR flag is not set to 1.

[Setting condition]

- When FRDRHL contains less data than the specified receive triggering number, and no next data is received after 15 ETUs*1 from the last stop bit, and the SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR, after all received data is read
- When the FCR.FM bit is changed from 0 to 1

Note 1. This is equivalent to 1.5 frames in the 8-bit format with one stop bit.
The DR flag is only set to 1 when FIFO is selected in asynchronous mode, including multi-processor mode. It is not set to 1 in other operation modes.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, so the transmission is halted.

[Setting condition]

Bit	Symbol	Function	R/W
0	DR	接收数据就绪标志 0：接收中，或者接收成功后FRDRHL中没有接收到的数据（接收FIFO为空） 1：正常接收完成后一段时间内没有接收到下一个接收数据，此时FIFO中存储的数据量等于或小于接收触发数	R/W*1
1	—	读取值未定义。写入值应为1。	R/W
2	TEND	发送结束标志 0：字符传输中1：字符传输完成	R/W*1
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/W*1
4	FER	成帧错误标志 0：未发生帧错误1：发生帧错误	R/W*1
5	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/W*1
6	RDF	接收FIFO数据满标志 0：写入FRDRHL的接收数据量小于指定的接收触发数 1：写入FRDRHL的接收数据量等于或大于指定的接收触发数	R/W*1
7	TDFE	发送FIFO数据空标志 0：写入FTDRHL的发送数据量超过指定的发送触发数 1：写入FTDRHL的发送数据量等于或小于指定的发送触发数	R/W*1

注1.只能写入0，读取1后清除标志。

SSR_FIFO寄存器为SCI提供FIFO模式状态标志。

DR标志（接收数据就绪标志）

DR标志表示存储在接收FIFO数据寄存器(FRDRHL)中的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU（基本时间单位）后没有接收到下一个数据.此标志仅在选择FIFO操作时在异步模式下有效，包括多处理器模式。

在时钟同步模式下，DR标志不设置为1。

[Setting condition]

●当FRDRHL包含的数据少于指定的接收触发数，并且从最后一个停止位开始15个ETU*1后没有接收到下一个数据，并且SSR_FIFO.FER和SSR_FIFO.PER标志为0。

[Clearing conditions]

●从DR读取1时，在读取所有接收到的数据后

●当FCR.FM位由0变为1时

注1.这相当于8位格式的1.5帧，带有一位停止位。
只有在异步模式（包括多处理器模式）下选择FIFO时，DR标志才设置为1。在其他操作模式下不设置为1。

TEND标志（发送结束标志）

TEND标志表明FTDRHL在发送串行字符的最后一位时不包含有效数据，因此暂停发送。

[Setting condition]

- When FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written to FTDRHL*1 while the SCR.TE bit is 1
- When 0 is written to TEND after 1 is read from TEND, when the SCR.TE bit is 1
- When the FCR.FM bit is changed from 0 to 1

Note 1. Do not use the TEND bit as a transmit end flag when the DTC writes data to FTDRHL in response to an SCIn_TXI interrupt request.

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When data is received and a parity error is detected, when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to PER after reading PER = 1.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a parity error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When 0 is sampled as the stop bit during reception when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to FER after reading FER = 1.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a framing error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that the receive operation stopped abnormally because an overrun error occurred.

[Setting condition]

- When the next serial reception completes while the receive FIFO is full with 16-byte receive data.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that receive data was transferred to the FRDRHL register, and the amount of data in FRDRHL is equal to or exceeds the specified receive triggering number. When RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- When the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL,*1 and the FIFO is not empty.

●当FTDRHL不包含发送数据时，发送1字节串行字符的最后一位。

[Clearing conditions]

●当SCR.TE位为1时将发送数据写入FTDRHL*1

●从TEND读取1后，向TEND写入0时，SCR.TE位为1时

●当FCR.FM位由0变为1时

注1.当DTC将数据写入FTDRHL以响应SCIn_TXI中断请求时，请勿使用TEND位作为发送结束标志。

PER标志（奇偶校验错误标志）

PER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在奇偶校验错误。

[Setting condition]

●当接收到数据并检测到奇偶校验错误时，当地址匹配功能被禁用时（DCCR.DCME=0）。

[Clearing condition]

●读取PER=1后向PER写入0时。

接收操作是连续的，接收数据存储在FRDRHL寄存器中，即使在接收过程中发生奇偶校验错误。

当SCR.RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

FER标志（帧错误标志）

FER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在帧错误。

[Setting condition]

●当地址匹配功能被禁用（DCCR.DCME=0）时，在接收期间采样0作为停止位时。

[Clearing condition]

●读取FER=1后向FER写入0时。

接收操作是连续的，接收数据存储在FRDRHL寄存器中，即使在接收过程中发生帧错误。

当SCR.RE位设置为0（禁用串行接收）时，FER标志不受影响并保留其先前的值。

ORER标志（溢出错误标志）

ORER标志指示接收操作由于发生溢出错误而异常停止。

[Setting condition]

●当接收FIFO已满16字节接收数据时，下一次串行接收完成时。

[Clearing condition]

●读取ORER=1后向ORER写入0时。

当SCR.RE位设置为0（禁用串行接收）时，ORER标志不受影响并保留其先前的值。

RDF标志（接收FIFO数据满标志）

RDF标志表示接收数据已传送到FRDRHL寄存器，并且FRDRHL中的数据量等于或超过指定的接收触发数。当RTRG设置为0时，即使接收FIFO中的数据量等于0，RDF标志也不会设置。

[Setting condition]

●当FRDRHL中存储了等于或大于指定接收触发数的接收数据量时，*1且FIFO不为空。

[Clearing conditions]

- When 0 is written to RDF after reading RDF = 1
- When FRDRHL is read by the DTC, but only when the block transfer is the last transmission
- When the setting and clearing conditions occur at the same time, the RDF bit is set to 0. After that, when the amount of data stored in the FRDRHL register is the same as or greater than the RTRG value, RDF is set to 1 after 1 PCLK.

Note 1. Because FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that data is transferred from the FTDRHL register into the TSR register, the amount of data in FTDRHL is below the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- When the TE bit in SCR is 0
- When the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number*1

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DTC is activated
- When 0 is written to the TDFE flag after reading TDFE = 1.*2
  The setting conditions are given priority when TE = 0. When the setting condition and clearing condition occur at the same time, the TDFE flag is set to 0. After that, when the amount of data stored in the FTDRHL register is equal to or less than the TTRG value, TDFE is set to 1 after 1 PCLK.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, when the TDFE flag is 1, the maximum amount of data that can be written to the FTDRHL register is 16 minus FDR.T[4:0] bytes. If more data is written, data is discarded.
Note 2. Do not clear the TDFE flag during block transfer processing by the DTC.

30.2.17 SSR_SMCI : Serial Status Register for Smart Card Interface Mode (SCMR.SMIF = 1, and MMR.MANEN = 0)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	Multi-Processor Bit Transfer Set this bit to 0 in smart card interface mode	R/W
1	MPB	Multi-Processor Set this bit to 0 in smart card interface mode	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer is complete	R
3	PER	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	ERS	Error Signal Status Flag 0: No low error signal response 1: Low error signal response occurred	R/W*1

[Clearing conditions]

●读取RDF=1后向RDF写入0时

●当DTC读取FRDRHL时，但仅当块传输是最后一次传输时

●当设置和清除条件同时发生时，RDF位被设置为0。之后，当FRDRHL寄存器中存储的数据量等于或大于RTRG值时，RDF被设置为1在1个PCLK之后。

注1.因为FRDRHL是16级FIFO寄存器，所以当RDF为1时可以读取的最大数据量等于指定的接收触发数。如果在读取FRDRHL中的所有数据后尝试读取，则数据未定义。

TDFE标志（发送FIFO数据空标志）

TDFE标志表示数据从FTDRHL寄存器传送到TSR寄存器，在
FTDRHL低于指定的发送触发数，并且允许将发送数据写入FTDRHL。

[Setting conditions]

●当SCR的TE位为0时

●当写入FTDRHL的发送数据量等于或小于指定的发送触发数时*1

[Clearing conditions]

●当DTC激活时，在最后一次传输上执行写入FTDRHL时

●读取TDFE=1后向TDFE标志写入0时。*2
  当TE=0时，设置条件优先。当设置条件和清除条件同时发生时，TDFE标志设置为0。之后，当FTDRHL寄存器中存储的数据量等于或小于比TTRG值，TDFE在1个PCLK后设置为1。

注1.由于FTDRHL寄存器为16级FIFO寄存器，因此当TDFE标志为1时，可写入FTDRHL寄存器的最大数据量为16减去FDR.T[4:0]字节。如果写入更多数据，则丢弃数据。
注2.在DTC的块传输处理过程中，不要清除TDFE标志。

30.2.17 SSR_SMCI：智能卡接口模式的串行状态寄存器（SCMR.SMIF=1，MMR.MANEN=0）

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MPBT	多处理器位传输 在智能卡接口模式下将此位设置为0	R/W
1	MPB	Multi-Processor 在智能卡接口模式下将此位设置为0	R
2	TEND	发送结束标志 0：字符传输中1：字符传输完成	R
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1 ：发生奇偶校验错误	R/W*1
4	ERS	错误信号状态标志 0：无低位错误信号响应1：发生低位错误信号响应	R/W*1

Bit	Symbol	Function	R/W
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
6	RDRF	Receive Data Full Flag 0: No received data in RDR register 1: Received data in RDR register	R/W*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data in TDR register 1: No transmit data in TDR register	R/W*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_SMCI register provides the SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

When there is no error signal from the receiving side, the TEND flag is set to 1 when more data for transfer is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 (serial transmission is disabled).
  When the SCR_SMCI.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period elapses after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by the following register settings:
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETUs after the start of transmission
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETUs after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETUs after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETUs after the start of transmission

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to TDRE after reading TDRE = 1 while the SCR_SMCI.TE bit is 1

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception. Although receive data is transferred to RDR when a parity error occurs, no SCIn_RXI interrupt request occurs. After the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1. After writing 0 to the PER flag, read the flag to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

Bit	Symbol	Function	R/W
5	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/W*1
6	RDRF	接收数据满标志 0：RDR寄存器中没有接收到数据1：RDR寄存器中接收到数据	R/W*1
7	TDRE	传输数据空标志 0：在TDR寄存器中发送数据1：在TDR寄存器中不发送数据	R/W*1

注1.只能写入0，读取1后清除标志。

SSR_SMCI寄存器为SCI提供智能卡接口模式状态标志。

TEND标志（发送结束标志）

当接收端没有错误信号时，当更多数据准备好传输到TDR寄存器时，TEND标志设置为1。

[Setting conditions]

- 当SCR_SMCI.TE位=0时（禁用串行传输）。
  当SCR_SMCI.TE位从0变为1时，TEND标志不受影响并保持值1。
- 在最后一次发送1个字节后经过指定时间后，ERS标志为0，并且不更新TDR寄存器。

  设置时序由以下寄存器设置确定：
  - 当SMR_SMCI.GM=0且SMR_SMCI.BLK=0时，传输开始后12.5ETU
  - 当SMR_SMCI.GM=0和SMR_SMCI.BLK=1时，传输开始后11.5ETU
  - 当SMR_SMCI.GM=1和SMR_SMCI.BLK=0时，传输开始后11.0ETU
  - 当SMR_SMCI.GM=1且SMR_SMCI.BLK=1时，传输开始后11.0ETU

[Clearing conditions]

- 当SCR_SMCI.TE位为1时将发送数据写入TDR寄存器
- 当SCR_SMCI.TE位为1时，读取TDRE=1后向TDRE写入0

PER标志（奇偶校验错误标志）

PER标志表示在异步模式接收过程中发生奇偶校验错误，接收异常结束。

[Setting condition]

- 在接收过程中检测到奇偶校验错误时。尽管发生奇偶校验错误时将接收数据传输到RDR，但不会发生SCIn_RXI中断请求。PER标志设置为1后，后续接收数据不会传输到RDR。

[Clearing condition]

- 读取PER=1后向PER写入0时。将0写入PER标志后，读取该标志以检查它是否实际设置为0。

当SCR_SMCI中的RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

ERS标志（错误信号状态标志）

[Setting condition]

- 采样低误差信号时。

[Clearing condition]

- When 0 is written to ERS after reading ERS = 1.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error is read from the RDR register. The data received before an overrun error occurred is saved in the RDR, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1. After writing 0 to the ORER flag, read the flag to check that it is actually set to 0.

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to RDRF after reading RDRF = 1
- When data is forwarded from the RDR register

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When 0 is written to TDRE after reading TDRE = 1
- When the SCR_SMCI.TE bit is 1 and data is written to the TDR register

30.2.18 SSR_MANC : Serial Status Register for Manchester Mode (SCMR.SMIF = 0, and MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MER
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MER	Manchester Error Flag Valid for Manchester mode only 0: No Manchester error occurred 1: Manchester error has occurred	R/(W)*1

●读取ERS =1后向ERS 写入0时。

ORER标志（溢出错误标志）

ORER标志表示接收期间发生溢出错误，接收异常结束。

[Setting condition]

●在从RDR寄存器读取没有奇偶校验错误的接收数据之前接收到下一个数据时。发生溢出错误前接收的数据保存在RDR中，但错误发生后接收的数据会丢失。当ORER标志设置为1时，接收数据不转发到RDR寄存器。

[Clearing condition]

●读取ORER=1后向ORER写入0时。向ORER标志写入0后，读取该标志以检查它是否实际设置为0。

当SCR_SMCI中的RE位设置为0时，ORER标志不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

●接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

●读取RDRF=1后向RDRF写入0时

●从RDR寄存器转发数据时

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

●当SCR_SMCI.TE位为0时

●当数据从TDR寄存器传送到TSR寄存器时

[Clearing conditions]

●读取TDRE=1后写入0时

●当SCR_SMCI.TE位为1且数据写入TDR寄存器时

30.2.18 SSR_MANC：曼彻斯特模式的串行状态寄存器（SCMR.SMIF=0，并且MMR.MANEN = 1)

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MER
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	Function	R/W
0	MER	曼彻斯特错误标志 仅适用于曼彻斯特模式 0：未发生曼彻斯特错误1：发生曼彻斯特错误	R/(W)*1

Bit	Symbol	Function	R/W
1	MPB	Multi-Processor Value of the multi-processor bit in the reception frame 0: Data transmission cycles 1: ID transmission cycles	R
2	TEND	Transmit End Flag 0: A character is being transmitted 1: Character transfer has been completed.	R
3	PER	Parity Error Flag 0: No parity error occurred 1: A parity error has occurred	R/(W)*1
4	FER	Framing Error Flag 0: No framing error occurred 1: A framing error has occurred	R/(W)*1
5	ORER	Overrun Error Flag 0: No overrun error occurred 1: An overrun error has occurred	R/(W)*1
6	RDRF	Receive Data Full Flag 0: No received data is in RDR register 1: Received data is in RDR register	R/(W)*1
7	TDRE	Transmit Data Empty Flag 0: Transmit data is in TDR register 1: No transmit data is in TDR register	R/(W)*1

Note 1. Only 0 can be written to this bit, to clear the flag after confirmed(read) the flag is set to 1.

SSR is constructed in the status flag of SCI and reception multi processor bits.

MER flag (Manchester Error Flag)

When data is received in Manchester mode, Manchester error is detected and it is displayed.

[Setting conditions]

- When receiving in Manchester mode and detecting Manchester code error in data area of received frame.
  Received data when an error occurs is transferred to the RDR register, but the RXI interrupt request is not generatedand the ERI interrupt request is generated.
  When the Manchester error flag is set to “1”, subsequent receive data is not transferred to the RDR register.
  For details on Manchester error, see section 30.5.11. Errors in Manchester Mode.

[Clearing conditions]

- When 0 is written to MER after reading MER = 1 (after writing 0 to it, read the MER bit to check that it has actually been set to 0.)
  Even when the RE bit in SCR is set to 0 (serial reception is disabled), the MER flag is not affected and retains its previous value.

MPB flag (Multi-Processor)

Holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

Indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and FCR.FM bit is set to 0 (non-FIFO selected).
  When the SCR.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated at the time of transmission of the tail-end bit of a character being transmitted

[Clearing conditions]

- When transmit data are written to the TDR register while the SCR.TE bit is 1.

Bit	Symbol	Function	R/W
1	MPB	Multi-Processor 接收帧中多处理器位的值 0：数据传输周期1：ID传输周期	R
2	TEND	发送结束标志 0：正在传输字符1：已完成字符传输。	R
3	PER	奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/(W)*1
4	FER	成帧错误标志 0：未发生帧错误1：发生帧错误	R/(W)*1
5	ORER	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/(W)*1
6	RDRF	接收数据满标志 0：RDR寄存器中没有接收到的数据1：RDR寄存器中接收到的数据	R/(W)*1
7	TDRE	传输数据空标志 0：发送数据在TDR寄存器1：没有发送数据在TDR寄存器	R/(W)*1

注1.该位只能写入0，确认（读取）后清除标志，标志设置为1。

SSR由SCI的状态标志和接收多处理器位构成。

MER标志（曼彻斯特错误标志）

在曼彻斯特模式下接收数据时，检测到曼彻斯特错误并显示出来。

[Setting conditions]

●曼彻斯特模式接收时，检测接收帧数据区的曼彻斯特码错误。
发生错误时接收到的数据被传送到RDR寄存器，但不产生RXI中断请求，产生ERI中断请求。当曼彻斯特错误标志设置为“1”时，后续接收数据不会传输到RDR寄存器。

有关曼彻斯特错误的详细信息，请参阅第30.5.11节。曼彻斯特模式中的错误。

[Clearing conditions]

●读MER=1后向MER写入0时（向其写入0后，读取MER位以检查它是否已实际设置为0。）即使SCR中的RE位设置为0（串行接收是禁用），MER标志不受影响并保留其先前的值。

MPB flag (Multi-Processor)

保存接收帧中多处理器位的值。当SCR.RE位为0时，该位不变。

TEND标志（发送结束标志）

表示传输完成。

[Setting conditions]

●当SCR.TE位设置为0（禁用串行传输）且FCR.FM位设置为0（选择非FIFO）时。当SCR.TE位从0变为1时，TEND标志不受影响并保持值1。

●发送字符尾端位时，TDR寄存器未更新时

[Clearing conditions]

●当SCR.TE位为1时将发送数据写入TDR寄存器。

- When 0 is written to TDRE after reading TDRE = 1 while the SCR.TE bit is 1.

PER flag (Parity Error Flag)

Indicates that a parity error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When a parity error is detected during reception in Asynchronous Mode and the state of Address Match function invalidity (DCCR.DCME = 0).
  Although receive data when the parity error occurs is transferred to RDR, no RXI interrupt request occurs. Note that when the PER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to PER after reading PER = 1 (after writing 0 to it, read the PER bit to check that it has actually been set to 0.)

Even when the RE bit in SCR is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

Indicates that a framing error has occurred during reception in asynchronous mode and the reception ends abnormally.

[Setting condition]

- When “0” is sampled as the stop bit during reception in Asynchronous Mode and the state of Address Match function invalidity (DCCR.DCME = 0).
  In 2-stop-bit mode, only the first stop bit is checked whether it is 1 but the second stop bit is not checked. Note that although receive data when the framing error occurs is transferred to RDR, no RXI interrupt request occurs. In addition, when the FER flag is being set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to FER after reading FER = 1 (after writing 0 to it, read the FER bit to check that it has actually been set to 0.)
  .

Even when the RE bit in SCR is set to 0, the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

Indicates that an overrun error has occurred during reception and the reception ends abnormally.

[Setting condition]

- When the next data is received before receive data is read from RDR which don’t have any valid reception error.
  In RDR, receive data prior to an overrun error occurrence is retained, but data received after the overrun error occurrence is lost. When the ORER flag is set to 1, reception data isn’t forwarded to RDR register. Note that, in clock synchronous mode, serial transmission and reception will be stop.

[Clearing condition]

- When 0 is written to ORER after reading ORER = 1 (after writing 0 to it, read the ORER bit to check that it has actually been set to 0.)

Even when the RE bit in SCR is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

Indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register

[Clearing conditions]

- When it’s written to “0" after the state of “1" is read

●当SCR.TE位为1时，读取TDRE=1后向TDRE写入0。

PER标志（奇偶校验错误标志）

表示异步接收时发生奇偶校验错误，接收异常结束。

[Setting condition]

●在异步模式接收过程中检测到奇偶校验错误并且地址匹配功能无效状态（DCCR.DCME=0）。虽然发生奇偶校验错误时的接收数据被传输到RDR，但没有发生RXI中断请求。请注意，当PER标志设置为1时，后续接收数据不会传输到RDR。

[Clearing condition]

●读取PER=1后向PER写入0时（写入0后，读取PER位以检查其是否已实际设置为0。）

即使SCR中的RE位设置为0（禁用串行接收），PER标志也不受影响并保持其先前的值。

FER标志（帧错误标志）

表示异步模式接收时出现帧错误，接收异常结束。

[Setting condition]

●当在异步模式接收期间采样“0”作为停止位和地址匹配功能无效状态（DCCR.DCME=0）。在2-stop-bit模式下，只检查第一个停止位是否为1，不检查第二个停止位。请注意，虽然发生帧错误时的接收数据被传输到RDR，但不会发生RXI中断请求。此外，当FER标志设置为1时，后续接收数据不会传输到RDR。

[Clearing condition]

●读取FER=1后向FER写入0时（写入0后，读取FER位以检查其是否已实际设置为0。）

.

即使SCR中的RE位设置为0，FER标志也不受影响并保持其先前的值。

ORER标志（溢出错误标志）

表示接收过程中发生溢出错误，接收异常结束。

[Setting condition]

●在接收数据从没有任何有效接收错误的RDR读取之前接收到下一个数据时。在RDR中，保留发生溢出错误之前的接收数据，但发生溢出错误之后接收的数据会丢失。当ORER标志设置为1时，接收数据不转发到RDR寄存器。请注意，在时钟同步模式下，串行发送和接收将停止。

[Clearing condition]

●读ORER=1后向ORER写入0时（写入0后，读取ORER位以检查其是否已实际设置为0。）

即使SCR中的RE位设置为0，ORER标志也不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

指示RDR寄存器中存在接收数据。

[Setting condition]

●接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器

[Clearing conditions]

●读取“1”状态后写入“0”时

- When it’s read the data from the RDR register

TDRE flag (Transmit Data Empty Flag)

Indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is “0"
- When data is transmitted from the TDR register to the TSR register

[Clearing conditions]

- When it’s written to “0" after the state of “1" is read
- When the SCR.TE bit is 1, it’s written to the TDR register

Note: RDRF and TDRE should not be cleared by SSR register access unless communication is interrupted.

30.2.19 SCMR : Smart Card Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	SMIF	Smart Card Interface Mode Select 0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode	R/W*1
1	—	This bit is read as 1. The write value should be 1.	R/W
2	SINV	Transmitted/Received Data Invert Set the SINV bit to 0 for operation in simple IIC mode. The level of communication terminals (RXD, TXD) are controlled by combination of this bit and SPTR.TINV/RINV. For details, see Figure 30.5. The SINV bit can be used in the following modes: ● Smart card interface mode ● Asynchronous mode (including multi-processor mode) ● Clock synchronous mode ● Simple SPI mode 0: TDR contents are transmitted as they are. Received data is stored as received in the RDR register. 1: TDR register contents are inverted before transmission. Receive data is stored in inverted form in the RDR register.	R/W*1
3	SDIR	Transmitted/Received Data Transfer Direction Set the SDIR bit to 1 for operation in simple IIC mode. The SDIR bit can be used in the following modes: ● Smart card interface mode ● Asynchronous mode (including multi-processor mode) ● Clock synchronous mode ● Simple SPI mode 0: Transfer LSB-first 1: Transfer MSB-first	R/W*1

●从RDR寄存器读取数据时

TDRE标志（传输数据空标志）

指示TDR寄存器中存在发送数据。

[Setting conditions]

●SCR.TE位为“0”时

●当数据从TDR寄存器传送到TSR寄存器时

[Clearing conditions]

●读取“1”状态后写入“0”时

●SCR.TE位为1时，写入TDR寄存器

Note: RDRF和TDRE不应被SSR寄存器访问清除，除非通信中断。

30.2.19 SCMR:智能卡模式寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
重置后的值:	1	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	SMIF	智能卡接口模式选择 0：非智能卡接口模式 （异步模式、时钟同步模式、简单SPI模式或简单IIC模式） 1：智能卡接口方式	R/W*1
1	—	该位读取为1。写入值应为1。	R/W
2	SINV	发送接收数据反转 将SINV位设置为0，以便在简单IIC模式下运行。 通信终端（RXD、TXD）的电平由该位和SPTR.TINVRINV组合控制。详见图30.5。SINV位可用于以下模式：● 智能卡接口方式 ● 异步模式（包括多处理器模式） ● 时钟同步模式 ● 简单SPI模式 0：TDR内容按原样发送。接收到的数据按接收到的方式存储在RDR寄存器中。 1：TDR寄存器内容在发送前反转。接收数据以反转形式存储在RDR寄存器中。	R/W*1
3	SDIR	发送接收数据传输方向 将SDIR位设置为1以在简单IIC模式下运行。 SDIR位可用于以下模式：● 智能卡接口方式 ● 异步模式（包括多处理器模式） ● 时钟同步模式 ● 简单SPI模式 0: Transfer LSB-first 1: Transfer MSB-first	R/W*1

Bit	Symbol	Function	R/W
4	CHR1	Character Length 1 Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SMR.CHR bit. 0: SMR.CHR = 0: Transmit/receive in 9-bit data length SMR.CHR = 1: Transmit/receive in 9-bit data length 1: SMR.CHR = 0: Transmit/receive in 8-bit data length (initial value) SMR.CHR = 1: Transmit/receive in 7-bit data length*3	R/W*1
6:5	—	These bits are read as 1. The write value should be 1.	R/W
7	BCP2	Base Clock Pulse 2 Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 30.5 lists the combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first must be selected and the value of the MSB (bit [7]) in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects smart card interface mode. Setting it to 0 selects all other modes:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode
- Simple IIC mode

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit and receive data logic level. It does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit and receive data in combination with the CHR bit in the SMR register. A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

Table 30.5 Combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00b	93 clock cycles (S = 93)*1
0	01b	128 clock cycles (S = 128)*1
0	10b	186 clock cycles (S = 186)*1
0	11b	512 clock cycles (S = 512)*1
1	00b	32 clock cycles (S = 32) (Initial Value)*1
1	01b	64 clock cycles (S = 64)*1
1	10b	372 clock cycles (S = 372)*1
1	11b	256 clock cycles (S = 256)*1

Note 1. S is the value of S in section 30.2.20. BRR : Bit Rate Register.

Bit	Symbol	Function	R/W
4	CHR1	字符长度1 仅在异步模式下有效。*2 结合SMR.CHR位选择发送接收字符长度。 0：SMR.CHR=0：发送接收9位数据长度SMR.CHR=1： 发送接收9位数据长度 1：SMR.CHR=0：发送接收以8位数据长度（初始值）SMR.CHR=1： 发送接收以7位数据长度*3	R/W*1
6:5	—	这些位被读取为1。写入值应为1。	R/W
7	BCP2	基本时钟脉冲2 结合SMR_SMCI.BCP[1:0]位选择基本时钟周期数。 表30.5列出了SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合。	R/W*1

注1.仅当SCRSCR_SMCI中的TE和RE位为0时可写（串行发送和接收均禁用）。
注2.设置无效，异步模式以外的模式使用固定的8位数据长度。
注3.必须选择LSB-first并且不能传输TDR中MSB（位[7]）的值。

SCMR寄存器选择智能卡接口和通信格式。

SMIF位（智能卡接口模式选择）

将SMIF位设置为1选择智能卡接口模式。将其设置为0会选择所有其他模式：

- ●异步模式，包括多处理器模式
- ●时钟同步模式
- ●简单SPI模式
- ●简单IIC模式

SINV位（发送接收数据反转）

SINV位反转发送和接收数据逻辑电平。它不影响奇偶校验位的逻辑电平。要反转奇偶校验位，请反转SMR或SMR_SMCI中的PM位。

CHR1位（字符长度1）

CHR1位结合SMR寄存器中的CHR位选择发送和接收数据的数据长度。在异步模式以外的模式中使用8位的固定数据长度。

BCP2位（基本时钟脉冲2）

BCP2位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将该位与SMR_SMCI.BCP[1:0]位一起设置。

Table 30.5 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
0	00b	93个时钟周期(S=93)*1
0	01b	128个时钟周期(S=128)*1
0	10b	186个时钟周期(S=186)*1
0	11b	512个时钟周期(S=512)*1
1	00b	32个时钟周期(S=32)(初始值)*1
1	01b	64个时钟周期(S=64)*1
1	10b	372个时钟周期(S=372)*1
1	11b	256个时钟周期(S=256)*1

注1.S为30.2.20节中S的值。BRR：比特率寄存器。

30.2.20 BRR : Bit Rate Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each channel. Table 30.6 shows the relationship between the setting (N) in the BRR and the bit rate (B) for normal asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

The initial value of the BRR register is 0xFF. The BRR register can be read by the CPU, but it can be written to only when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 30.6 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS bit	ABCS E bit		
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B: Bit rate (bps)
N: BRR setting for on-chip baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 30.8 and Table 30.9.
Note 1. Adjust the bit rate so that the widths of high and low level of the SCLn output in simple IIC mode satisfy the I^2C bus standard.

Table 30.7 Calculating widths of SCLn high and low levels

Mode	SCLn	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

30.2.20 BRR:比特率寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

BRR是一个8位寄存器，用于调整比特率。

由于每个SCI通道都有独立的波特率发生器控制，因此可以为每个通道设置不同的比特率。表30.6显示了BRR中的设置(N)与正常异步模式、多处理器传输、时钟同步模式、智能卡接口模式、简单SPI模式和简单IIC模式的比特率(B)之间的关系。

BRR寄存器的初始值为0xFF。BRR寄存器可以被CPU读取，但只有当SCRSCR_SMCI中的TE和RE位为0时才能写入。

Table 30.6 BRR中的N设置与比特率B的关系

Mode	SEMR settings			BRR setting	Error
	BGDM bit	ABCS 位	ABCS E位		
异步、多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\right\} \times 100$
时钟同步，简单的SPI				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	—
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\right\} \times 100$
Simple IIC*1				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	—

Note: B：比特率（bps）
N：片内波特率发生器的BRR设置（0≤N≤255）
PCLK：工作频率(MHz)n和S：由表30.8和表30.9中列出的SMRSMR_SMCI和SCMR寄存器设置决定。

注1.调整比特率，使简单IIC模式下SCLn输出的高低电平宽度满足I2C总线标准。

Table 30.7 计算SCLn高低电平的宽度

Mode	SCLn	公式（以秒为单位的结果）
IIC	高电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLK \times 10^6}$
	低电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLK \times 10^6}$

Table 30.8 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bits setting		
CKS[1:0] bits	Clock source	n
00b	PCLK clock	0
01b	PCLK/4 clock	1
10b	PCLK/16 clock	2
11b	PCLK/64 clock	3

Table 30.9 Base clock settings in smart card interface mode

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bits setting		
BCP2 bit	BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	00b	93 clock cycles	93
0	01b	128 clock cycles	128
0	10b	186 clock cycles	186
0	11b	512 clock cycles	512
1	00b	32 clock cycles	32
1	01b	64 clock cycles	64
1	10b	372 clock cycles	372
1	11b	256 clock cycles	256

Table 30.10 and Table 30.11 list examples of BRR (N) settings in normal asynchronous mode. Table 30.12 lists the maximum bit rate settable for each operating frequency. Table 30.16 lists examples of BRR (N) settings in smart card interface mode.

In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 30.7.4. Receive Data Sampling Timing and Reception Margin. Table 30.13 and Table 30.15 list the maximum bit rates with external clock input.

When either the Asynchronous Mode Base Clock Select bit (ABCS) or the Baud Rate Generator Double-speed Mode Select bit (BGDM) in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice the value listed in Table 30.17. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 30.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (1 of 2)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

Table 30.8 时钟源设置

SMR或SMR_SMCI.CKS[1:0]位设置		
CKS[1:0] bits	时钟源	n
00b	PCLK clock	0
01b	PCLK/4 clock	1
10b	PCLK/16 clock	2
11b	PCLK/64 clock	3

Table 30.9 智能卡接口模式下的基本时钟设置

SCMR.BCP2位设置	SMR_SMCI.BCP[1:0]位设置		
BCP2 bit	BCP[1:0] bits	1位周期的基本时钟周期	S
0	00b	93个时钟周期	93
0	01b	128个时钟周期	128
0	10b	186个时钟周期	186
0	11b	512个时钟周期	512
1	00b	32个时钟周期	32
1	01b	64个时钟周期	64
1	10b	372个时钟周期	372
1	11b	256个时钟周期	256

表30.10和表30.11列出了正常异步模式下的BRR(N)设置示例。表30.12列出了每个工作频率可设置的最大比特率。表30.16列出了智能卡接口模式下的BRR(N)设置示例。

在智能卡接口模式下，可以选择1位数据传输时间内的基本时钟周期数S。有关详细信息，请参阅第30.7.4节。接收数据采样时序和接收余量。表30.13和表30.15列出了外部时钟输入的最大比特率。

当串行扩展模式寄存器(SEMR)中的异步模式基本时钟选择位(ABCS)或波特率发生器双速模式选择位(BGDM)在异步模式下设置为1时，比特率变为该值的两倍列于表30.17中。当这两个寄存器都设置为1时，比特率变为所列值的四倍。

Table 30.10 异步模式下不同比特率的BRR设置示例(1)(1of2)

比特率(bps)	工作频率PCLK(MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03	2	217	0.08
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34	0	19	0.00
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	–2.34	0	9	0.00

Table 30.10 Examples of BRR settings for different bit rates in asynchronous mode (1) (2 of 2)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	–0.93	0	51	0.16	0	55	0.00	0	58	–0.69	0	63	0.00
19200	0	22	–0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	–1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	–2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate increases four times.

Table 30.11 Examples of BRR settings for different bit rates in asynchronous mode (2) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	–0.25	3	110	–0.02	3	132	0.13	3	145	0.33	3	177	–0.25
150	3	64	0.16	3	80	0.47	3	97	–0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	–0.15	2	194	0.16	2	214	–0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	–0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	–0.15	1	194	0.16	1	214	–0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	–0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	–0.15	0	194	0.16	0	214	–0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	–0.35	0	106	0.39	0	129	0.16
19200	0	32	–1.36	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	–0.54	0	32	–1.36

Table 30.11 Examples of BRR settings for different bit rates in asynchronous mode (2) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50			60			100		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	–0.02	—	—	—	3	255	—
150	3	162	–0.15	3	194	0.16	3	255	—
300	3	80	0.47	3	97	–0.35	3	162	–0.15
600	2	162	–0.15	3	48	–0.35	3	80	0.47
1200	2	80	0.47	2	97	–0.35	2	162	–0.15
2400	1	162	–0.15	2	48	–0.35	2	80	0.47

Table 30.10 异步模式下不同比特率的BRR设置示例(1)(2of2)

比特率(bps)	工作频率PCLK(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	–0.17	3	70	0.03	3	75	0.48	3	79	–0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	–0.93	0	51	0.16	0	55	0.00	0	58	–0.69	0	63	0.00
19200	0	22	–0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	–1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	–2.34	0	15	0.00

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。
当ABCS和BGDM都设置为1时，比特率增加四倍。

Table 30.11 异步模式下不同比特率的BRR设置示例(2)(1of3)

比特率(bps)工作频率PCLK(MHz)															
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	–0.25	3	110	–0.02	3	132	0.13	3	145	0.33	3	177	–0.25
150	3	64	0.16	3	80	0.47	3	97	–0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	–0.15	2	194	0.16	2	214	–0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	–0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	–0.15	1	194	0.16	1	214	–0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	–0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	–0.15	0	194	0.16	0	214	–0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	–0.35	0	106	0.39	0	129	0.16
19200	0	32	–1.36	0	40	–0.76	0	48	–0.35	0	53	–0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	–0.54	0	32	–1.36

Table 30.11 异步模式下不同比特率的BRR设置示例(2)(2of3)

比特率(bps)	工作频率PCLK(MHz)								
	50			60			100		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	–0.02	—	—	—	3	255	—
150	3	162	–0.15	3	194	0.16	3	255	—
300	3	80	0.47	3	97	–0.35	3	162	–0.15
600	2	162	–0.15	3	48	–0.35	3	80	0.47
1200	2	80	0.47	2	97	–0.35	2	162	–0.15
2400	1	162	–0.15	2	48	–0.35	2	80	0.47

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Table 30.11 Examples of BRR settings for different bit rates in asynchronous mode (2) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50			60			100		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
4800	1	80	0.47	1	97	–0.35	1	162	–0.15
9600	0	162	–0.15	1	48	–0.35	1	80	0.47
19200	0	80	0.47	0	97	–0.35	0	162	–0.15
31250	0	49	0.00	0	59	0.00	1	24	0.00
38400	0	40	–0.76	0	48	–0.35	0	80	0.47

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS = 1 and BGDM = 1, the bit rate quadruples.

Table 30.12 Maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLK (MHz)	SEMR settings					Maximumbit rate (bps)	PCLK (MHz)	SEMR settings					Maximumbit rate (bps)
	BGDMbit	ABCS bit	ABCSE bit	n	N			BGDMbit	ABCS bit	ABCSEbit	n	N	
8	0	0	0	0	0	250,000	16	0	0	0	0	0	500,000
		1	0	0	0	500,000			1	0	0	0	1,000,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,000,000			1	0	0	0	2,000,000
	Don’tcare	Don’tcare	1	0	0	1,333,333		Don’tcare	Don’tcare	1	0	0	2,666,666
9.8304	0	0	0	0	0	307,200	17.2032	0	0	0	0	0	537,600
		1	0	0	0	614,400			1	0	0	0	1,075,200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,228,800			1	0	0	0	2,150,400
	Don’tcare	Don’tcare	1	0	0	1,638,400		Don’tcare	Don’tcare	1	0	0	2,867,200
10	0	0	0	0	0	312,500	18	0	0	0	0	0	562,500
		1	0	0	0	625,000			1	0	0	0	1,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,250,000			1	0	0	0	2,250,000
	Don’tcare	Don’tcare	1	0	0	1,666,666		Don’tcare	Don’tcare	1	0	0	3,000,000
12	0	0	0	0	0	375,000	19.6608	0	0	0	0	0	614,400
		1	0	0	0	750,000			1	0	0	0	1,228,800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,500,000			1	0	0	0	2,457,600
	Don’tcare	Don’tcare	1	0	0	2,000,000		Don’tcare	Don’tcare	1	0	0	3,276,800
12.288	0	0	0	0	0	384,000	20	0	0	0	0	0	625,000
		1	0	0	0	768,000			1	0	0	0	1,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,536,000			1	0	0	0	2,500,000
	Don’tcare	Don’tcare	1	0	0	2,048,000		Don’tcare	Don’tcare	1	0	0	3,333,333

Table 30.11 异步模式下不同比特率的BRR设置示例(2)(3of3)

比特率(bps)	工作频率PCLK(MHz)								
	50			60			100		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
4800	1	80	0.47	1	97	–0.35	1	162	–0.15
9600	0	162	–0.15	1	48	–0.35	1	80	0.47
19200	0	80	0.47	0	97	–0.35	0	162	–0.15
31250	0	49	0.00	0	59	0.00	1	24	0.00
38400	0	40	–0.76	0	48	–0.35	0	80	0.47

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。
当ABCS=1和BGDM=1时，比特率翻四倍。

Table 30.12 异步模式下每个工作频率的最大比特率（1of2）

PCLK (MHz)	SEMR settings					Maximumbit rate (bps)	PCLK (MHz)	SEMR settings					Maximumbit rate (bps)
	BGDMbit	ABCS位	ABCSE位	n	N			BGDMbit	ABCS位	ABCSEbit	n	N	
8	0	0	0	0	0	250,000	16	0	0	0	0	0	500,000
		1	0	0	0	500,000			1	0	0	0	1,000,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,000,000			1	0	0	0	2,000,000
	Don’tcare	Don’tcare	1	0	0	1,333,333		Don’tcare	Don’tcare	1	0	0	2,666,666
9.8304	0	0	0	0	0	307,200	17.2032	0	0	0	0	0	537,600
		1	0	0	0	614,400			1	0	0	0	1,075,200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,228,800			1	0	0	0	2,150,400
	Don’tcare	Don’tcare	1	0	0	1,638,400		Don’tcare	Don’tcare	1	0	0	2,867,200
10	0	0	0	0	0	312,500	18	0	0	0	0	0	562,500
		1	0	0	0	625,000			1	0	0	0	1,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,250,000			1	0	0	0	2,250,000
	Don’tcare	Don’tcare	1	0	0	1,666,666		Don’tcare	Don’tcare	1	0	0	3,000,000
12	0	0	0	0	0	375,000	19.6608	0	0	0	0	0	614,400
		1	0	0	0	750,000			1	0	0	0	1,228,800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,500,000			1	0	0	0	2,457,600
	Don’tcare	Don’tcare	1	0	0	2,000,000		Don’tcare	Don’tcare	1	0	0	3,276,800
12.288	0	0	0	0	0	384,000	20	0	0	0	0	0	625,000
		1	0	0	0	768,000			1	0	0	0	1,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,536,000			1	0	0	0	2,500,000
	Don’tcare	Don’tcare	1	0	0	2,048,000		Don’tcare	Don’tcare	1	0	0	3,333,333

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Table 30.12 Maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLK (MHz)	SEMR settings					Maximumbit rate (bps)	PCLK (MHz)	SEMR settings					Maximumbit rate (bps)
	BGDMbit	ABCS bit	ABCSE bit	n	N			BGDMbit	ABCS bit	ABCSEbit	n	N	
14	0	0	0	0	0	437,500	25	0	0	0	0	0	781,250
		1	0	0	0	875,000			1	0	0	0	1,562,500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,750,000			1	0	0	0	3,125,000
	Don’tcare	Don’tcare	1	0	0	2,333,333		Don’tcare	Don’are	1	0	0	4,166,666
30	0	0	0	0	0	937,500	50	0	0	0	0	0	1,562,500
		1	0	0	0	1,875,000			1	0	0	0	3,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3,750,000			1	0	0	0	6,250,000
	Don’tcare	Don’tcare	1	0	0	5,000,000		Don’tcare	Don’tcare	1	0	0	8,333,333
33	0	0	0	0	0	1,031,250	60	0	0	0	0	0	1,875,000
		1	0	0	0	2,062,500			1	0	0	0	3,750,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4,125,000			1	0	0	0	7,500,000
	Don’tcare	Don’tcare	1	0	0	5,500,000		Don’tcare	Don’tcare	1	0	0	10,000,000
40	0	0	0	0	0	1,250,000	100	0	0	0	0	0	3,125,000
		1	0	0	0	2,500,000			1	0	0	0	6,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5,000,000			1	0	0	0	12,500,000
	Don’tcare	Don’tcare	1	0	0	6,666,666		Don’tcare	Don’tcare	1	0	0	16,666,666

Table 30.13 Maximum bit rate with external clock input in asynchronous mode (1 of 2)

Maximum bit rate (bps)			
PCLK(MHz)	External inputclock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125,000	250,000
9.8304	2.4576	153,600	307,200
10	2.5000	156,250	312,500
12	3.0000	187,500	375,000
12.288	3.0720	192,000	384,000
14	3.5000	218,750	437,500
16	4.0000	250,000	500,000
17.2032	4.3008	268,800	537,600
18	4.5000	281,250	562,500
19.6608	4.9152	307,200	614,400
20	5.0000	312,500	625,000
25	6.2500	390,625	781,250
30	7.5000	468,750	937,500
33	8.2500	515,625	1,031,250
40	10.0000	625,000	1,250,000
50	12.5000	781,250	1,562,500

Table 30.12 异步模式下每个工作频率的最大比特率（2之2）

PCLK (MHz)	SEMR settings					Maximumbit rate (bps)	PCLK (MHz)	SEMR settings					Maximumbit rate (bps)
	BGDMbitABCS位ABCSE位			n	N			BGDMbitABCS位ABCSEbitnN					
14	0	0	0	0	0	437,500	25	0	0	0	0	0	781,250
		1	0	0	0	875,000			1	0	0	0	1,562,500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1,750,000			1	0	0	0	3,125,000
	Don’tcare	Don’tcare	1	0	0	2,333,333		Don’tcare	Don’are	1	0	0	4,166,666
30	0	0	0	0	0	937,500	50	0	0	0	0	0	1,562,500
		1	0	0	0	1,875,000			1	0	0	0	3,125,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3,750,000			1	0	0	0	6,250,000
	Don’tcare	Don’tcare	1	0	0	5,000,000		Don’tcare	Don’tcare	1	0	0	8,333,333
33	0	0	0	0	0	1,031,250	60	0	0	0	0	0	1,875,000
		1	0	0	0	2,062,500			1	0	0	0	3,750,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4,125,000			1	0	0	0	7,500,000
	Don’tcare	Don’tcare	1	0	0	5,500,000		Don’tcare	Don’tcare	1	0	0	10,000,000
40	0	0	0	0	0	1,250,000	100	0	0	0	0	0	3,125,000
		1	0	0	0	2,500,000			1	0	0	0	6,250,000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5,000,000			1	0	0	0	12,500,000
	Don’tcare	Don’tcare	1	0	0	6,666,666		Don’tcare	Don’tcare	1	0	0	16,666,666

Table 30.13 异步模式下外部时钟输入的最大比特率（1of2）

最大比特率(bps)			
PCLK(MHz)	External inputclock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125,000	250,000
9.8304	2.4576	153,600	307,200
10	2.5000	156,250	312,500
12	3.0000	187,500	375,000
12.288	3.0720	192,000	384,000
14	3.5000	218,750	437,500
16	4.0000	250,000	500,000
17.2032	4.3008	268,800	537,600
18	4.5000	281,250	562,500
19.6608	4.9152	307,200	614,400
20	5.0000	312,500	625,000
25	6.2500	390,625	781,250
30	7.5000	468,750	937,500
33	8.2500	515,625	1,031,250
40	10.0000	625,000	1,250,000
50	12.5000	781,250	1,562,500

Table 30.13 Maximum bit rate with external clock input in asynchronous mode (2 of 2)

Maximum bit rate (bps)			
PCLK(MHz)	External inputclock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
60	15.0000	937,500	1,875,000
100	25.000	1,562,500	3,125,000

Table 30.14 BRR settings for different bit rates in clock synchronous and simple SPI modes

Bit rate (bps)	Operating frequency PCLK (MHz)																					
	8		10		16		20		25		30		33		40		50		60		100	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																						
250	3	124	—	—	3	249																
500	2	249	—	—	3	124	—	—			3	233										
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	155
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	77
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	38
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	1	249
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	124
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	0	249
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	24
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	0	49
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	24
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	9
5 M							0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	4
7.5 M											0	0*1							0	1		
10 M															0	0*1						
15 M																			0	0*1		

Note: Space: Setting prohibited.
—: Can be set, but an error occurs.

Note 1. Continuous transmission or reception is not possible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting to transmit or receive the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. Therefore, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate. When the FIFO is selected, this setting (BRR = 00h and SMR.CKS[1:0] = 00b) is not available.

Table 30.15 Maximum bit rate with external clock input in clock synchronous and simple SPI modes (1 of 2)

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333

Table 30.13 异步模式下外部时钟输入的最大比特率（2之2）

最大比特率(bps)			
PCLK(MHz)	External inputclock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
60	15.0000	937,500	1,875,000
100	25.000	1,562,500	3,125,000

Table 30.14 时钟同步和简单SPI模式下不同比特率的BRR设置

比特率(bps)	工作频率PCLK(MHz)																					
	8		10		16		20		25		30		33		40		50		60		100	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																						
250	3	124	—	—	3	249																
500	2	249	—	—	3	124	—	—			3	233										
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	155
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	77
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	38
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	1	249
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	124
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	0	249
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	24
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	0	49
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	24
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	9
5 M							0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	4
7.5 M											0	0*1							0	1		
10 M															0	0*1						
15 M																			0	0*1		

Note: 空格：禁止设置。—：可以设置，
但发生错误。

注1.不能连续发送或接收。在发送或接收一帧数据后，在开始发送或接收下一帧数据之前会经过1位周期。同步时钟的输出停止1位周期。因此，传输一帧（8位）数据需要9位的时间，平均传输速率为89倍的位速率。

选择FIFO时，此设置（BRR=00h且SMR.CKS[1:0]=00b）不可用。

Table 30.15 时钟同步和简单SPI模式下外部时钟输入的最大比特率（1of2）

PCLK (MHz)	外部输入时钟(MHz)	最大比特率(Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333

Table 30.15 Maximum bit rate with external clock input in clock synchronous and simple SPI modes (2 of 2)

PCLK (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
100	16.6667	16.6666667

Table 30.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (1 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	7.1424			10.00			10.7136			13.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	30	0	1	25	0	1	8.99

Table 30.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (2 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	14.2848			16.00			18.00			20.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	15.99	0	2	6.66

Table 30.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (3 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	25.00			30.00			33.00			40.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	12.49	0	3	5.01	0	4	7.59	0	5	–6.66

Table 30.16 BRR settings for different bit rates in smart card interface mode, n = 0, S = 372 (4 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50.00			60.00			100.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	13	0.01

Table 30.17 Maximum bit rate for each operating frequency in smart card interface mode (S = 32) (1 of 2)

PCLK (MHz)	Maximum bit rate (bps)	n	N
10.00	156,250	0	0
10.7136	167,400	0	0
13.00	203,125	0	0
16.00	250,000	0	0
18.00	281,250	0	0
20.00	312,500	0	0

Table 30.15 时钟同步和简单SPI模式下外部时钟输入的最大比特率(2of2)

PCLK (MHz)	外部输入时钟(MHz)	最大比特率(Mbps)
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
100	16.6667	16.6666667

Table 30.16 智能卡接口模式下不同比特率的BRR设置，n=0 S=372(1of4)

比特率(bps)	工作频率PCLK(MHz)											
	7.1424			10.00			10.7136			13.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	30	0	1	25	0	1	8.99

Table 30.16 智能卡接口模式下不同比特率的BRR设置，n=0，S=372(2of4)

比特率(bps)	工作频率PCLK(MHz)											
	14.2848			16.00			18.00			20.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	15.99	0	2	6.66

Table 30.16 智能卡接口模式下不同比特率的BRR设置，n=0 S=372(3of4)

比特率(bps)	工作频率PCLK(MHz)											
	25.00			30.00			33.00			40.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	12.49	0	3	5.01	0	4	7.59	0	5	–6.66

Table 30.16 智能卡接口模式下不同比特率的BRR设置，n=0 S=372(4of4)

比特率(bps)	工作频率PCLK(MHz)								
	50.00			60.00			100.00		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	13	0.01

Table 30.17 智能卡接口模式下每个工作频率的最大比特率(S=32)(1of2)

PCLK (MHz)	最大比特率(bps)	n	N
10.00	156,250	0	0
10.7136	167,400	0	0
13.00	203,125	0	0
16.00	250,000	0	0
18.00	281,250	0	0
20.00	312,500	0	0

Table 30.17 Maximum bit rate for each operating frequency in smart card interface mode (S = 32) (2 of 2)

PCLK (MHz)	Maximum bit rate (bps)	n	N
25.00	390,625	0	0
30.00	468,750	0	0
33.00	515,625	0	0
40.00	625,000	0	0
50.00	781,250	0	0
60.00	937,500	0	0
100.00	1,562,500	0	0

Table 30.18 BRR settings for different bit rates in simple IIC mode (1 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	31	–2.3	1	12	–3.8	1	15	–2.3	1	19	–2.3
25 k	0	9	0.0	0	12	–3.8	1	4	0.0	1	6	–10.7	1	7	–2.3
50 k	0	4	0.0	0	6	–10.7	1	2	–16.7	1	3	–21.9	1	3	–2.3
100 k	0	2	–16.7	0	3	–21.9	0	4	0.0	0	6	–10.7	1	1	–2.3
250 k	0	0	0.0	0	1	–37.5	0	1	0.0	0	2	–16.7	0	3	–21.9
350 k										0	1	–10.7	0	2	–25.6
400 k										0	1	–21.9	0	1	–2.3

Table 30.18 BRR settings for different bit rates in simple IIC mode (2 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	30			33			40			50			60		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	23	–2.3	1	25	–0.8	0	124	0.00	2	9	–2.3	1	46	–0.27
25 k	1	9	–6.3	1	10	–6.3	0	40	0.00	2	3	–2.3	0	74	0.00
50 k	1	4	–6.3	1	5	–14.1	0	24	0.00	2	1	–2.3	0	37	–1.32
100 k	1	2	–21.9	1	2	–14.1	0	12	–3.85	1	3	–2.3	0	18	–1.32
250 k	0	3	–6.3	0	4	–17.5	0	4	0.00	0	6	–10.7	0	7	–6.25
350 k	0	2	–10.7	0	2	–1.8	0	3	–10.71	0	4	–10.7	0	4	7.14
400 k	0	1	17.2	0	2	–14.1	0	2	4.17	0	3	–2.34	0	4	–6.25

Table 30.18 BRR settings for different bit rates in simple IIC mode (3 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)		
	100		
	n	N	Error (%)
10 k	1	77	0.16
25 k	0	124	0.00
50 k	0	62	–0.79
100 k	0	30	0.81
250 k	0	12	–3.85

Table 30.17 智能卡接口模式下每个工作频率的最大比特率(S=32)(2of2)

PCLK (MHz)	最大比特率(bps)	n	N
25.00	390,625	0	0
30.00	468,750	0	0
33.00	515,625	0	0
40.00	625,000	0	0
50.00	781,250	0	0
60.00	937,500	0	0
100.00	1,562,500	0	0

Table 30.18 简单IIC模式下不同比特率的BRR设置 （1of4）

比特率(bps)	工作频率PCLK(MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	31	–2.3	1	12	–3.8	1	15	–2.3	1	19	–2.3
25 k	0	9	0.0	0	12	–3.8	1	4	0.0	1	6	–10.7	1	7	–2.3
50 k	0	4	0.0	0	6	–10.7	1	2	–16.7	1	3	–21.9	1	3	–2.3
100 k	0	2	–16.7	0	3	–21.9	0	4	0.0	0	6	–10.7	1	1	–2.3
250 k	0	0	0.0	0	1	–37.5	0	1	0.0	0	2	–16.7	0	3	–21.9
350 k										0	1	–10.7	0	2	–25.6
400 k										0	1	–21.9	0	1	–2.3

Table 30.18 简单IIC模式下不同比特率的BRR设置(2of4)

比特率(bps)工作频率PCLK(MHz)															
	30			33			40			50			60		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	23	–2.3	1	25	–0.8	0	124	0.00	2	9	–2.3	1	46	–0.27
25 k	1	9	–6.3	1	10	–6.3	0	40	0.00	2	3	–2.3	0	74	0.00
50 k	1	4	–6.3	1	5	–14.1	0	24	0.00	2	1	–2.3	0	37	–1.32
100 k	1	2	–21.9	1	2	–14.1	0	12	–3.85	1	3	–2.3	0	18	–1.32
250 k	0	3	–6.3	0	4	–17.5	0	4	0.00	0	6	–10.7	0	7	–6.25
350 k	0	2	–10.7	0	2	–1.8	0	3	–10.71	0	4	–10.7	0	4	7.14
400 k	0	1	17.2	0	2	–14.1	0	2	4.17	0	3	–2.34	0	4	–6.25

Table 30.18 简单的不同比特率的BRR设置
IIC模式（4个中的3个）

比特率(bps)	工作频率PCLK(MHz)		
	100		
	n	N	Error (%)
10 k	1	77	0.16
25 k	0	124	0.00
50 k	0	62	–0.79
100 k	0	30	0.81
250 k	0	12	–3.85

Table 30.18 BRR settings for different bit rates in simple IIC mode (4 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)		
	100		
	n	N	Error (%)
350 k	0	8	–0.79
400 k	0	8	–13.19

Table 30.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (1 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	8			10			16			20		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	0	24	43.75/50.00	0	31	44.80/51.20	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	6	19.60/22.40
50 k	0	4	8.75/10.00	0	6	9.80/11.20	1	2	10.50/12.00	1	3	11.20/12.80
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	1	2.80/3.20	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

Table 30.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (2 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)											
	25			30			33			40		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	1	19	44.80/51.20	1	23	44.80/51.20	1	25	44.12/50.42	1	32	46.20/52.80
25 k	1	7	17.92/20.48	1	9	18.66/21.33	1	10	18.66/21.33	1	12	18.20/20.80
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	5	10.18/11.63	1	6	9.80/11.20
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.81	0	13	4.90/5.60
250 k	0	3	2.24/2.56	0	3	1.86/2.13	0	4	2.12/2.42	0	4	1.75/2.00
350 k	0	2	1.68/1.92	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28	0	1	0.93/1.07	0	2	1.27 /1.45	0	2	1.05/1.20

Table 30.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (3 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50			60			100		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
10 k	2	9	44.80/51.20	1	46	44.80/51.20	0	0	43.68/49.92

Table 30.18 简单的不同比特率的BRR设置
IIC模式（4个中的4个）

比特率(bps)	工作频率PCLK(MHz)		
	100		
	n	N	Error (%)
350 k	0	8	–0.79
400 k	0	8	–13.19

Table 30.19 简单IIC模式下多个比特率下SCL高电平和低电平的最小宽度（4个中的1个）

比特率(bps)	工作频率PCLK(MHz)											
	8			10			16			20		
	n	N	分钟。SCL高低电平的宽度(µs)	n	N	分钟。SCL高低电平的宽度(µs)	n	N	分钟。SCL高低电平的宽度(µs)	n	N	分钟。SCL高低电平的宽度(µs)
10 k	0	24	43.75/50.00	0	31	44.80/51.20	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	6	19.60/22.40
50 k	0	4	8.75/10.00	0	6	9.80/11.20	1	2	10.50/12.00	1	3	11.20/12.80
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.37/5.00	0	6	4.90/5.60
250 k	0	0	1.75/2.00	0	1	2.80/3.20	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

Table 30.19 简单IIC模式下多个比特率下SCL高电平和低电平的最小宽度（4个中的2个）

比特率(bps)工作频率PCLK(MHz)												
	25			30			33			40		
	n	N	分钟。SCL高低电平的宽度(µs)	n	N	分钟。SCL高低电平的宽度(µs)	n	N	分钟。SCL高低电平的宽度(µs)	n	N	分钟。SCL高低电平的宽度(µs)
10 k	1	19	44.80/51.20	1	23	44.80/51.20	1	25	44.12/50.42	1	32	46.20/52.80
25 k	1	7	17.92/20.48	1	9	18.66/21.33	1	10	18.66/21.33	1	12	18.20/20.80
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	5	10.18/11.63	1	6	9.80/11.20
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.81	0	13	4.90/5.60
250 k	0	3	2.24/2.56	0	3	1.86/2.13	0	4	2.12/2.42	0	4	1.75/2.00
350 k	0	2	1.68/1.92	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28	0	1	0.93/1.07	0	2	1.27 /1.45	0	2	1.05/1.20

Table 30.19 简单IIC模式下多个比特率下SCL高电平和低电平的最小宽度（3of4）

比特率(bps)工作频率PCLK(MHz)									
	50			60			100		
	nN最小值。SCL高低电平的宽度(µs)			n	N	分钟。SCL高低电平的宽度(µs)	nN最小值。SCL高低电平的宽度(µs)		
10 k	2	9	44.80/51.20	1	46	44.80/51.20	0	0	43.68/49.92

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Table 30.19 Minimum widths at SCL high and low levels at multiple bit rates in simple IIC mode (4 of 4)

Bit rate (bps)	Operating frequency PCLK (MHz)								
	50			60			100		
	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)	n	N	Min. widths at SCL high/low levels (µs)
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	0	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	0	8.82/10.08
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	0	4.34/4.96
250 k	0	6	1.96/2.24	0	7	1.87/2.13	0	0	1.82/2.08
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	0	1.26/1.44
400 k	0	3	1.12/1.28	0	4	1.17/1.33	0	0	1.26/1.44

30.2.21 MDDR : Modulation Duty Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

MDDR corrects the bit rate adjusted by the BRR register.

When the BRME bit in SEMR is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected using the settings in MDDR (M/256). Table 30.20 shows the relationship between the MDDR setting (M) and the bit rate (B).

The initial value of MDDR is 0xFF. Bit [7] in this register is fixed to 1.

The CPU can read the MDDR register, but this register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 30.19 简单IIC模式下多个比特率的SCL高电平和低电平的最小宽度（4个中的4个）

比特率(bps)工作频率PCLK(MHz)									
	50			60			100		
	nN最小值。SCL高低电平的宽度(µs)			n	N	分钟。SCL高低电平的宽度(µs)	nN最小值。SCL高低电平的宽度(µs)		
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	0	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	0	8.82/10.08
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	0	4.34/4.96
250 k	0	6	1.96/2.24	0	7	1.87/2.13	0	0	1.82/2.08
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	0	1.26/1.44
400 k	0	3	1.12/1.28	0	4	1.17/1.33	0	0	1.26/1.44

30.2.21 MDDR：调制占空比寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

MDDR校正由BRR寄存器调整的比特率。

当SEMR中的BRME位设置为1时，片上波特率发生器生成的比特率使用MDDR(M256)中的设置进行均匀校正。表30.20显示了MDDR设置(M)和比特率(B)之间的关系。

MDDR的初始值为0xFF。该寄存器中的位[7]固定为1。

CPU可以读取MDDR寄存器，但该寄存器只有在SCRSCR_SMCI中的TE和RE位为0时才可写。

Table 30.20 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 256)
N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLK: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 30.8 and Table 30.9 in section 30.2.20. BRR : Bit Rate Register.

Mode	SEMR settings BGDM bit	ABCS bit	ABCSE bit	BRR setting	Error
Asynchronous multiprocessor transfer	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	×	×	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Clock synchronous, simple SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	—
Smart card interface				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	—

Note 1. Do not use this function in clock synchronous mode or in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths at high and low level of the SCLn output in simple IIC mode satisfy the IIC standard.

Table 30.21 and Table 30.22 list examples of N settings in BRR and M settings in MDDR in normal asynchronous mode.

Table 30.21 Examples of the BRR and MDDR settings for different bit rates in asynchronous mode (1) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Table 30.20 使用比特率调制功能时MDDR设置(M)和比特率(B)的关系

B：比特率（bps）
M: MDDR setting (128 ≤ MDDR ≤ 256)
N：波特率发生器的BRR设置（0≤N≤255）
PCLK：工作频率(MHz)n和S：由SMRSMR_SMCI和SCMR寄存器设置确定，如第30.2.20节中的表30.8和表30.9中所列。BRR：比特率寄存器。

Mode	SEMR settings BGDM bit	ABCS位	ABCSE bit	BRR setting	Error
异步多处理器传输	0	0	0	$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	1	0	0	$N = \frac{PCLK \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLK \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
	×	×	1	$N = \frac{PCLK \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
时钟同步，简单SPI*1				$N = \frac{PCLK \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	—
智能卡接口				$N = \frac{PCLK \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error(\%) = \left\{\frac{PCLK \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\right\} \times 100$
Simple IIC*2				$N = \frac{PCLK \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	—

注1.不要在时钟同步模式或简单SPI模式的最高速度设置中使用此功能（SMR.CKS[1:0]=00b，SCR.CKE[1] = 0, and BRR = 0).
注2.调整比特率，使简单IIC模式下SCLn输出的高低电平宽度满足IIC标准。

表30.21和表30.22列出了正常异步模式下BRR中的N设置和MDDR中的M设置的示例。

Table 30.21 异步模式下不同比特率的BRR和MDDR设置示例(1)(1of3)

比特率(bps)	工作频率PCLK(MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Table 30.21 Examples of the BRR and MDDR settings for different bit rates in asynchronous mode (1) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

Table 30.21 Examples of the BRR and MDDR settings for different bit rates in asynchronous mode (1) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

Table 30.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (1 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	19.6608					20					25				
	n	N	M	BG DM bit	Error (%)	n	N	M	BG DM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

Table 30.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (2 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Table 30.21 异步模式下不同比特率的BRR和MDDR设置示例(1)(2of3)

比特率(bps)	工作频率PCLK(MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

Table 30.21 异步模式下不同比特率的BRR和MDDR设置示例(1)(3of3)

比特率(bps)	工作频率PCLK(MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

注1.在本例中，SEMR寄存器中的ABCS和ABCSE位为0。SEMR.BRME=0(M=256)禁用比特率调制功能。

Table 30.22 异步模式下不同比特率的BRR和MDDR设置示例(2)(1of3)

比特率(bps)	工作频率PCLK(MHz)														
	19.6608					20					25				
	n	N	M	BG DM bit	Error (%)	n	N	M	BG DM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

Table 30.22 异步模式下不同比特率的BRR和MDDR设置示例(2)(2of3)

比特率(bps)	工作频率PCLK(MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Table 30.22 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2) (3 of 3)

Bit rate (bps)	Operating frequency PCLK (MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.01
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0.
SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

30.2.22 SEMR : Serial Extended Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	PADIS	ACS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACS0	Asynchronous Mode Clock Source Select Valid only in asynchronous mode 0: External clock input 1: Logical AND of compare matches output from the internal GPT. These bit for the other SCI channels than SCIn (n = 1, 2) are reserved.	R/W*1
1	PADIS	Preamble function Disable Valid only in asynchronous mode 0: Preamble output function is enabled 1: Preamble output function is disabled These bits for the other SCI channels than SCIn (n = 0, 3 to 9) are reserved.	R/W
2	BRME	Bit Rate Modulation Enable 0: Disable bit rate modulation function 1: Enable bit rate modulation function	R/W*1
3	ABCSE	Asynchronous Mode Extended Base Clock Select 1 Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Clock cycles for 1-bit period determined by combination of the BGDM and ABCS bits in the SEMR register 1: Baud rate is 6 base clock cycles for 1-bit period These bits for the other SCI channels than SCIn (n = 0, 3 to 9) are reserved.	R/W*1
4	ABCS	Asynchronous Mode Base Clock Select Valid only in asynchronous mode. 0: Select 16 base clock cycles for 1-bit period 1: Select 8 base clock cycles for 1-bit period	R/W*1
5	NFEN	Digital Noise Filter Function Enable The NFEN bit must be 0 in all other modes. 0: In asynchronous mode: Disable noise cancellation function for RXDn input signal In simple I2C mode: Disable noise cancellation function for SCLn and SDAn input signals 1: In asynchronous mode: Enable noise cancellation function for RXDn input signal In simple I2C mode: Enable noise cancellation function for SCLn and SDAn input signals	R/W*1

Table 30.22 异步模式下不同比特率的BRR和MDDR设置示例(2)(3of3)

比特率(bps)	工作频率PCLK(MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.01
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

注1.在本例中，SEMR寄存器中的ABCS和ABCSE位为0。
SEMR.BRME=0(M=256)禁用比特率调制功能。

30.2.22 SEMR:串行扩展模式寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	PADIS	ACS0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ACS0	异步模式时钟源选择 仅在异步模式下有效 0：外部时钟输入1：比较的逻辑与匹配来自内部GPT的输出。 这些位用于除SCIn(n=1 2)之外的其他SCI通道。	R/W*1
1	PADIS	前导功能禁用 仅在异步模式下有效 0：前导输出功能有效1：前导输出功能 无效 这些位用于除SCIn（n=0、3到9）以外的其他SCI通道。	R/W
2	BRME	比特率调制启用 0：禁用码率调制功能1：启用码率调制 功能	R/W*1
3	ABCSE	异步模式扩展基本时钟选择1 仅在SCR.CKE[1]=0的异步模式下有效。 0：1位周期的时钟周期由SEMR寄存器中的BGDM和ABCS位组合确定 1：波特率为1位周期的6个基本时钟周期 这些位用于除SCIn（n=0、3到9）以外的其他SCI通道。	R/W*1
4	ABCS	异步模式基本时钟选择 仅在异步模式下有效。 0：为1位周期选择16个基本时钟周期1：为1位 周期选择8个基本时钟周期	R/W*1
5	NFEN	数字噪声滤波器功能启用 在所有其他模式下，NFEN位必须为0。 0：异步模式：禁用RXDn输入信号的噪声消除功能简单I2C模式：禁用SCLn和SDAn输入信号的噪声消除功能 1：异步模式下：使能RXDn输入信号的噪声消除功能在简单I2C模式下：使能SCLn和SDAn输入信号的噪声消除功能	R/W*1

Bit	Symbol	Function	R/W
6	BGDM	Baud Rate Generator Double-Speed Mode Select Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Output clock from baud rate generator with normal frequency 1: Output clock from baud rate generator with doubled frequency	R/W*1
7	RXDESEL	Asynchronous Start Bit Edge Detection Select Valid only in asynchronous mode. 0: Detect low level on RXDn pin as start bit 1: Detect falling edge of RXDn pin as start bit	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).

The SEMR register selects the clock source for the 1-bit period in asynchronous mode.

ACS0 bit (Asynchronous Mode Clock Source Select)

Selects the clock source in the asynchronous mode.

The ACS0 bit is valid in asynchronous mode (SMR.CM bit = 0) and when an external clock input is selected (SCR.CKE[1:0] bits = 10b or 11b). This bit is used to select an external clock input or the logical AND of compare matches output from the internal GPT.

Set the ACS0 bit to 0 in other than asynchronous mode.

For SCI1 and SCI2, the GTIOCnA output (n = 3, 4, 6, 7) of GPT can be set as the serial transfer base clock. Refer to Table 30.23 for details.

These bits for the other SCI channels than SCI1 and SCI2 are reserved. The write values to these bits for other than SCI1 and SCI2 should be 0.

Table 30.23 Correspondence between SCI Channels and Compare Match Outputs

SCI	GPT	Compare Match Output
SCI1	GPT3	GTIOC3A
	GPT4	GTIOC4A
SCI2	GPT6	GTIOC6A
	GPT7	GTIOC7A

Figure 30.3, Figure 30.4 show a setting example of when GTIOC3A and GTIOC4A are selected for output.

This figure shows an example when GPT clock is input to SCI1.

When generating 187.5 kbps of GPT average transfer rate for PCLKD = 32 MHz:

1. Generate a frequency of 4 MHz using GTIOC3A as the base clock.
2. Generate 3/4 clock enable of base clock to set an average transfer rate of 3 MHz/16 = 187.5 kbps using GTIOC4A.

Setting examples of GPT and SCI

- GPT3.GTSSR = 0x80000000, GPT4.GTSSR = 0x80000000 (Enable software counter start)
- GPT3.GTPR = 0x00000007, GPT4.GTPR = 0x0000001F (Maximum count value of GTCNT)
- GPT3.GTCCRA = 0x00000003, GPT4.GTCCRA = 0x00000007 (Compare match value)
- GPT3.GTCR = 0x00000000, GPT4.GTCR = 0x00000000 (Saw-wave PWM mode, timer prescaler is PCLKD/1)
- GPT3.GTIOR = 0x00000306, GPT4.GTIOR = 0x00000306

(Initial output low, output high at GTCCRA compare match, output low at cycle end)

- SCR.SCK[1:0] = 10b (External clock input or GPT clock input is selected)
- SEMR = 0x01 (TMR clock input is selected with 16 base clock cycles for 1-bit period)
- GPT3.GTSTR = 0x00000018 (Software start GTCNT counter)

Bit	Symbol	Function	R/W
6	BGDM	波特率发生器双速模式选择 仅在SCR.CKE[1]=0的异步模式下有效。 0：波特率发生器输出时钟，正常频率1：波特率发生器输出时钟，频率加倍	R/W*1
7	RXDESEL	异步起始位边沿检测选择 仅在异步模式下有效。 0：检测RXDn引脚的低电平作为起始位1：检测RXDn引脚的下降沿作为起始位	R/W*1

注1.仅当SCRSCR_SMCI中的TE和RE位为0时可写（串行发送和接收均禁用）。

SEMR寄存器选择异步模式下1位周期的时钟源。

ACS0位（异步模式时钟源选择）

选择异步模式下的时钟源。

ACS0位在异步模式（SMR.CM位=0）和选择外部时钟输入时（SCR.CKE[1:0]位=10b或11b）有效。该位用于选择外部时钟输入或内部GPT的比较匹配输出的逻辑与。

在非异步模式下将ACS0位设置为0。

对于SCI1和SCI2，GPT的GTIOCnA输出(n=3 4 6 7)可以设置为串行传输基准时钟。详见表30.23。

这些位用于除SCI1和SCI2之外的其他SCI通道。SCI1和SCI2以外的这些位的写入值应为0。

Table 30.23 SCI通道和比较匹配输出之间的对应关系

SCI	GPT	比较匹配输出
SCI1	GPT3	GTIOC3A
	GPT4	GTIOC4A
SCI2	GPT6	GTIOC6A
	GPT7	GTIOC7A

图30.3、图30.4显示了选择GTIOC3A和GTIOC4A输出时的设置示例。

此图显示了GPT时钟输入到SCI1时的示例。

当为PCLKD=32MHz生成187.5kbps的GPT平均传输速率时：

1.使用GTIOC3A作为基本时钟生成4MHz的频率。

2.使用GTIOC4A生成基本时钟的34时钟使能，以设置3MHz16=187.5kbps的平均传输速率。

GPT和SCI的树立榜样

●GPT3.GTSSR=0x80000000，GPT4.GTSSR=0x80000000（启用软件计数器启动）

●GPT3.GTPR=0x00000007 GPT4.GTPR=0x0000001F（GTCNT的最大计数值）

- GPT3.GTCCRA = 0x00000003, GPT4.GTCCRA = 0x00000007 (Compare match value)

●GPT3.GTCR=0x00000000 GPT4.GTCR=0x00000000（锯波PWM模式，定时器预分频器为PCLKD1）

- GPT3.GTIOR = 0x00000306, GPT4.GTIOR = 0x00000306

（初始输出低，GTCCRA比较匹配时输出高，循环结束时输出低）

●SCR.SCK[1:0]=10b（选择外部时钟输入或GPT时钟输入）

●SEMR=0x01（TMR时钟输入选择16个基本时钟周期用于1位周期）

- GPT3.GTSTR = 0x00000018 (Software start GTCNT counter)

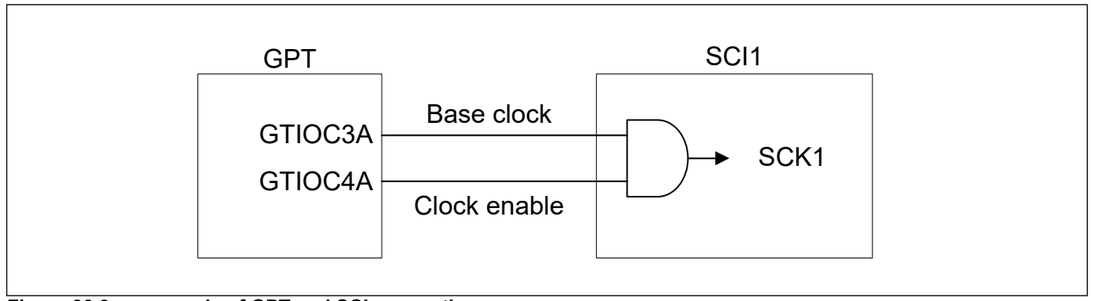

Figure 30.3 example of GPT and SCI connection

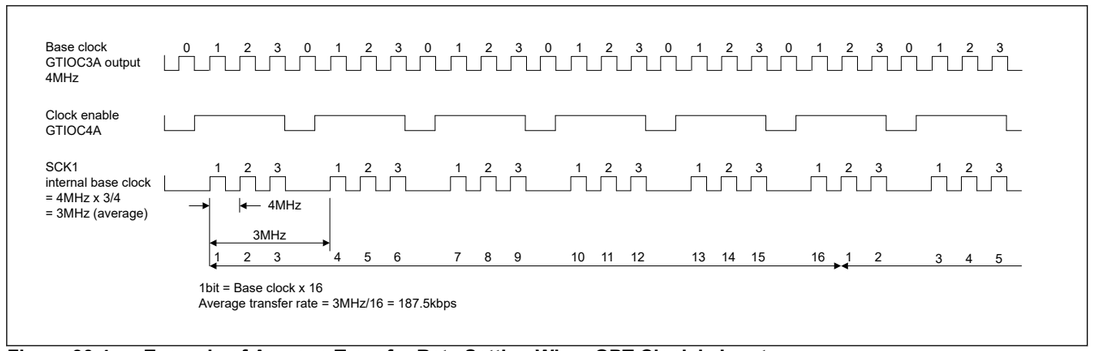

Figure 30.4 Example of Average Transfer Rate Setting When GPT Clock is Input

PADIS bit (Preamble function Disable)

In asynchronous mode, select enable / disable of preamble function. In Manchester mode, preamble is not output regardless of this bit setting

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables or disables the bit rate modulation function. The bit rate generated by the on-chip baud rate generator is evenly corrected when this function is enabled. Set to 0 in Manchester mode.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The ABCSE bit sets the pulse number for the base clock in a 1-bit period to 6, and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use this bit and set SMR.CKS[1:0] = 00b and BRR = 0.

Set it to "0" in modes other than asynchronous mode. Even in asynchronous mode, set it to "0" when using external clock.

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the number of clock cycles for a 1-bit period.

Set it to "0" in modes other than asynchronous mode and Manchester mode.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the digital noise filter function is enabled:

- Noise cancellation is applied to the RXDn input signal in asynchronous mode
- Noise cancellation is applied to the SDAn and SCLn input signals in simple I^2C mode

In all other modes, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as received.

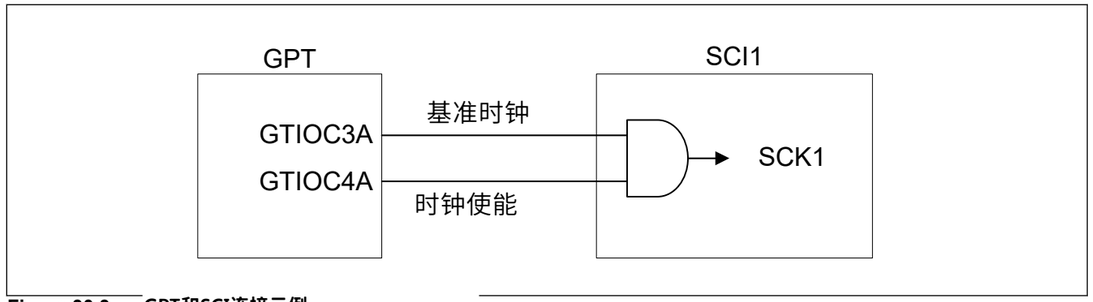

Figure 30.3 GPT和SCI连接示例

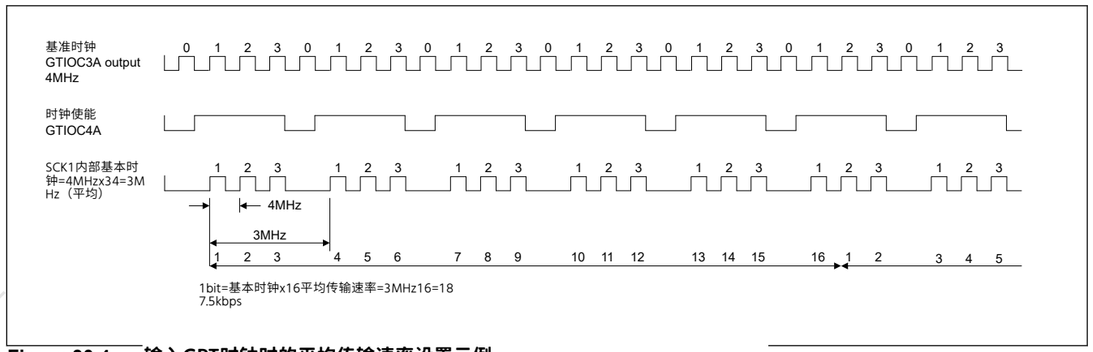

Figure 30.4 输入GPT时钟时的平均传输速率设置示例

PADIS位（前导功能禁用）

在异步模式下，选择enabledisableofpreamble功能。在曼彻斯特模式下，无论该位设置如何，都不会输出前导码

BRME位（比特率调制启用）

BRME位启用或禁用比特率调制功能。该功能使能时，片内波特率发生器产生的比特率得到均匀校正。在曼彻斯特模式下设置为0。

ABCSE位（异步模式扩展基本时钟选择1）

ABCSE位将基本时钟在1位周期内的脉冲数设置为6，并从波特率发生器输出双频时钟。当比特率设置为6并同时分频总线时钟频率时，使用该位并设置SMR.CKS[1:0]=00b和BRR=0。

在异步模式以外的模式下将其设置为“0”。即使在异步模式下，使用外部时钟时也将其设置为“0”。

ABCS位（异步模式基本时钟选择）

ABCS位选择1位周期的时钟周期数。

在异步模式和曼彻斯特模式以外的模式下将其设置为“0”。

NFEN位（数字噪声滤波器功能使能）

NFEN位启用或禁用数字噪声滤波器功能。

启用数字噪声滤波器功能时：

●在异步模式下对RXDn输入信号应用噪声消除

●在简单I2C模式下，对SDAn和SCLn输入信号应用噪声消除

在所有其他模式下，将NFEN位设置为0以禁用数字噪声滤波器功能。禁用该功能时，输入信号按接收到的方式传输。

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects whether or not to double the base clock frequency output from the baud rate generator.

The BGDM bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0) or Manchester mode (MMR.MANEN = 1). When external clock is selected (SCR.CKE[1] = 1), set it to 0. The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode or Manchester mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDESEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data reception operation depends on the setting of this bit. Set this bit to 1 when reception must be stopped while a break occurs or when reception must be started without keeping the RXDn pin input at the high level for the period of one data frame or longer after completion of the break.

Set this bit to 0 in modes other than asynchronous mode.

30.2.23 SNFR : Noise Filter Setting Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	NFCS[2:0]	Noise Filter Clock Select In asynchronous mode, selects the standard setting for the base clock. In simple I2C mode, selects the standard settings for the clock source of the on-chip baud rate generator selected in the SMR.CKS[1:0] bits. 0 0 0: In asynchronous mode: Use clock signal divided by 1 with noise filter In simple I2C mode: Setting prohibited 0 0 1: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 1 with noise filter 0 1 0: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 2 with noise filter 0 1 1: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 4 with noise filter 1 0 0: In asynchronous mode: Setting prohibited In simple I2C mode: Use clock signal divided by 8 with noise filter Others: Setting prohibited	R/W*1
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple I2C mode, when 32 clocks are selected as one bit period in the basic clock selection bits of the SEMR register, set the NFCS [2: 0] bits in the range from 001b to 100b. When any other value is selected for the basic clock selection bit, set the NFCS bit to 001b.

BGDM位（波特率发生器双速模式选择）

BGDM位选择是否将波特率发生器输出的基本时钟频率加倍。

在异步模式(SMR.CM=0)或曼彻斯特模式(MMR.MANEN=1)选择片内波特率发生器作为时钟源(SCR.CKE[1]=0)时，BGDM位有效。选择外时钟（SCR.CKE[1]=1）时，将其设置为0。基本时钟是由BaudRateGenerator的时钟输出生成的。当BGDM位设置为1时，基本时钟周期减半，比特率加倍。

在异步模式或曼彻斯特模式以外的模式下将此位设置为0。

RXDESEL位（异步起始位边沿检测选择）

RXDESEL位选择异步模式下接收起始位的检测方法。发生中断时，数据接收操作取决于该位的设置。如果在发生中断时必须停止接收，或者在中断完成后，RXDn引脚输入在一个数据帧或更长时间内不保持高电平而必须开始接收时，将该位设置为1。

在异步模式以外的模式下将此位设置为0。

30.2.23 SNFR：噪声滤波器设置寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	NFCS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	NFCS[2:0]	噪声滤波器时钟选择 在异步模式下，选择基本时钟的标准设置。 在简单I2C模式下，选择SMR.CKS[1:0]位中选择的片内波特率发生器时钟源的标准设置。 000：在异步模式下：使用时钟信号除以1和噪声滤波器在简单I2C模式下： 禁止设置 001：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以1和噪声滤波器 010：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以2和噪声滤波器 011：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以4和噪声滤波器 100：异步模式下：禁止设置 在简单I2C模式下：使用时钟信号除以8和噪声滤波器 其他：禁止设置	R/W*1
7:3	—	这些位被读取为0。写入值应为0。	R/W

注1.只有当SCRSCR_SMCI中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SNFR寄存器设置数字噪声滤波器时钟。

NFCS[2:0]位（噪声滤波器时钟选择）

NFCS[2:0]位选择数字噪声滤波器的采样时钟。要在异步模式下使用噪声滤波器，请将这些位设置为000b。在简单I2C模式下，当在SEMR寄存器的基本时钟选择位中选择32个时钟作为一个位周期时，将NFCS[2:0]位设置在001b到100b的范围内。当基本时钟选择位选择任何其他值时，将NFCS位设置为001b。

30.2.24 SIMR1 : IIC Mode Register 1

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICM	Simple IIC Mode Select 0: SCMR.SMIF = 0: Asynchronous mode (including multi-processor mode), clock synchronous mode, or simple SPI mode SCMR.SMIF = 1: Smart card interface mode 1: SCMR.SMIF = 0: Simple IIC mode SCMR.SMIF = 1: Setting prohibited	R/W*1
2:1	—	These bits are read as 0. The write value should be 0.	R/W
7:3	IICDL[4:0]	SDAn Delay Output Select SDAn signal output delay in cycles of the clock signal from the on-chip baud rate generator. 0x00: No output delay Others: (IICDL - 1) to (IICDL) cycles	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).

SIMR1 selects simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SCMR.SMIF bit, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDAn Delay Output Select)

The IICDL[4:0] bits specify an output delay on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLK by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set 00000b to IICDL[4:0] bits unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

Table 30.24 Settable value of IICDL[4: 0] bits in each communication mode

Communication mode	ABCS	Settable value of IICDL[4:0] bits
Other than simple IIC mode	Don't care	00000b
Simple IIC mode	0	00001b to 11111b
	1	00001b to 00100b

30.2.25 SIMR2 : IIC Mode Register 2

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

30.2.24 SIMR1：IIC模式寄存器1

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICDL[4:0]					—	—	IICM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICM	简单IIC模式选择 0：SCMR.SMIF=0：异步模式（包括多处理器模式）、时钟同步模式或简单SPI模式 SCMR.SMIF=1：智能卡接口模式 1：SCMR.SMIF=0：简单IIC模式SCMR.S MIF=1：禁止设置	R/W*1
2:1	—	这些位被读取为0。写入值应为0。	R/W
7:3	IICDL[4:0]	SDAn延迟输出选择 SDAn信号输出延迟来自片内波特率发生器的时钟信号周期。 0x00：无输出延迟 其他：（IICDL1）至（IICDL）周期	R/W*1

注1.只有当SCR寄存器中的RE和TE位为0（串行发送和接收都被禁止）时，才能写入这些位。

SIMR1选择简单IIC模式和SDAn输出的延迟级数。

IICM位（简单IIC模式选择）

IICM位与SCMR.SMIF位一起选择工作模式。

IICDL[4:0]位（SDAn延迟输出选择）

IICDL[4:0]位指定SDAn引脚上相对于SCLn引脚输出下降沿的输出延迟。

可用的延迟设置范围从无延迟到31个周期，以来自片上波特率发生器的时钟信号为基准。通过在SMR.CKS[1:0]中设置的除数对PCLK进行分频获得的信号作为来自片上波特率发生器的时钟信号提供。除非在简单IIC模式下操作，否则将00000b设置为IICDL[4:0]位。在简单IIC模式下，将位设置为00001b到11111b范围内的值。

Table 30.24 每种通信模式下IICDL[4:0]位的可设置值

通讯方式	ABCS	IICDL[4:0]位的可设置值
除了简单的IIC模式	不在乎	00000b
简单IIC模式	0	00001b to 11111b
	1	00001b to 00100b

30.2.25 SIMR2：IIC模式寄存器2

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	IICACKT	—	—	—	IICCSC	IICINTM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICINTM	IIC Interrupt Mode Select 0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts	R/W*1
1	IICCSC	Clock Synchronization 0: Do not synchronize with clock signal 1: Synchronize with clock signal	R/W*1
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	IICACKT	ACK Transmission Data 0: ACK transmission 1: NACK transmission and ACK/NACK reception	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (serial reception and transmission disabled).

SIMR2 selects how reception and transmission are controlled in simple IIC mode.

IICINTM bit (IIC Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SCLn clock signal is to be synchronized when the SCLn pin is driven low because a wait was inserted by another other device.

The SCLn clock signal is not synchronized if the IICCSC bit is 0. The SCLn clock signal is generated according to the rate selected in the BRR register regardless of the level being input on the SCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set the IICACKT bit to 1 when ACK and NACK bits are received.

30.2.26 SIMR3 : IIC Mode Register 3

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICSTAREQ	Start Condition Generation 0: Do not generate start condition 1: Generate start condition*1 *3 *5 *6	R/W
1	IICRSTAREQ	Restart Condition Generation 0: Do not generate restart condition 1: Generate restart condition*2 *3 *5 *6	R/W
2	IICSTPREQ	Stop Condition Generation 0: Do not generate stop condition 1: Generate stop condition*2 *3 *5 *6	R/W

Bit	Symbol	Function	R/W
0	IICINTM	IIC中断模式选择 0：使用ACKNACK中断1：使用接收和发送中断	R/W*1
1	IICCSC	时钟同步 0：不与时钟信号同步1：与时钟信号同步	R/W*1
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	IICACKT	ACK传输数据 0：ACK发送1：NACK发送和ACKNACK接收	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

注1.只有当SCR寄存器中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SIMR2选择在简单IIC模式下如何控制接收和发送。

IICINTM位（IIC中断模式选择）

IICINTM位选择简单IIC模式下的中断请求源。

IICCSC bit (Clock Synchronization)

如果在SCLn引脚被驱动为低电平时内部生成的SCLn时钟信号要同步，则将IICCSC位设置为1，因为另一个其他设备插入了等待。

如果IICCSC位为0，则SCLn时钟信号不同步。SCLn时钟信号根据BRR寄存器中选择的速率生成，与SCLn引脚上输入的电平无关。

除调试期间外，将IICCSC位设置为1。

IICACKT位（ACK传输数据）

传输的数据包含ACK位。当收到ACK和NACK位时，将IICACKT位设置为1。

30.2.26 SIMR3：IIC模式寄存器3

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	IICSTAREQ	开始条件生成 0：不产生启动条件1：产生启动条件*1*3*5*6	R/W
1	IICRSTAREQ	重启条件生成 0：不产生重启条件1：产生重启条件*2*3*5*6	R/W
2	IICSTPREQ	停止条件生成 0：不产生停止条件1：产生停止条件*2*3*5*6	R/W

Bit	Symbol	Function	R/W
3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag 0: No requests are being made for generating conditions, or a condition is being generated 1: Generation of start, restart, or stop condition is complete. When 0 is written to IICSTIF, it is set to 0*4	R/W*4
5:4	IICSDAS[1:0]	SDAn Output Select 0 0: Output serial data 0 1: Generate start, restart, or stop condition 1 0: Output low on SDAn pin 1 1: Drive SDAn pin to high-impedance state	R/W
7:6	IICSCLS[1:0]	SCLn Output Select 0 0: Output serial clock 0 1: Generate start, restart, or stop condition 1 0: Output low on SCLn pin 1 1: Drive SCLn pin to high-impedance state	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that the bus is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that the bus is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

The SIMR3 register is used to control the start, restart, and stop conditions in the simple I^2C mode, and to hold the SSDAn and SSCLn pins at fixed levels.

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of start condition generation.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICRSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of restart condition generation.

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTPREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of stop condition generation.

Bit	Symbol	Function	R/W
3	IICSTIF	发出启动、重启或停止条件完成标志 0：没有请求生成条件，或者正在生成条件 1：启动、重启或停止条件的生成完成。0写入IICSTIF时，设置为0*4	R/W*4
5:4	IICSDAS[1:0]	SDAn输出选择 00：输出串行数据01：产生启动、重启或停止条件10：SDAn引脚输出低电平11：驱动SDAn引脚为高阻状态	R/W
7:6	IICSCLS[1:0]	SCLn输出选择 00：输出串行时钟01：产生启动、重启或停止条件10：SCLn引脚输出低电平11：驱动SCLn引脚为高阻状态	R/W

注1.仅在检查总线状态并确认总线空闲后才生成启动条件。
注2.检查总线状态并确认总线繁忙后，生成重新启动或停止条件。
注3.在给定时间，不要将IICSTAREQ、IICRSTAREQ和IICSTPREQ位中的一个以上设置为1。
注4.只写0。当写1时，该值被忽略。
注5.在IICSTIF标志的值为0后执行条件生成。
注6.当该位为1时，请勿向该位写入0。当该位为1时，通过向该位写入0来暂停条件的产生。

SIMR3寄存器用于控制简单I2C模式下的启动、重启和停止条件，并将SSDAn和SSCLn引脚保持在固定电平。

IICSTAREQ位（开始条件生成）

当要产生一个开始条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICSTAREQ位为1。

[Setting condition]

●向该位写入1。

[Clearing condition]

●完成启动条件生成。

IICRSTAREQ位（重启条件生成）

当要产生重启条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICRSTAREQ位为1。

[Setting condition]

●向该位写入1。

[Clearing condition]

●完成重启条件生成。

IICSTPREQ位（停止条件生成）

当要产生停止条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICSTPREQ位为1。

[Setting condition]

●向该位写入1。

[Clearing condition]

●停止条件生成完成时。

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the condition generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- On completion of a start, restart, or stop condition generation.

  If the setting condition conflicts with any of the clearing conditions for the flag, the clearing condition takes precedence.

[Clearing conditions]

- On writing 0 to the bit. After writing 0 to the IICSTIF bit, read the bit to check that it is actually set to 0.
- On writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode.
- On writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDAn Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin. Set IICSDAS[1:0] and IICSCLS[1:0]to the same value during normal operations.

IICSCLS[1:0] bits (SCLn Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin. Set IICSDAS[1:0] and IICSCLS[1:0] to the same value during normal operations.

30.2.27 SISR : IIC Status Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK Reception Data Flag 0: ACK received 1: NACK received	R
1	—	This bit is read as 0.	R
2	—	The read value is undefined.	R
3	—	This bit is read as 0.	R
5:4	—	The read value is undefined.	R
7:6	—	These bits are read as 0.	R

SISR monitors the state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. The IICACKR flag is updated on the rising edge of the SCLn clock for the received ACK/NACK bit.

IICSTIF标志（发出启动、重启或停止条件完成标志）

生成条件后，IICSTIF标志指示条件生成完成。使用时
IICSTAREQ、IICRSTAREQ或IICSTPREQ位会导致条件生成，请在将IICSTIF标志设置为0后执行此操作。

当IICSTIF标志为1且通过设置SCR.TEIE位使能中断请求时，输出STI请求。

[Setting condition]

●完成启动、重新启动或停止条件生成时。

如果设置条件与标志的任何清除条件冲突，则清除条件优先。

[Clearing conditions]

●向该位写入0。将0写入IICSTIF位后，读取该位以检查它是否实际设置为0。
●在非简单IIC模式下向SIMR1.IICM位写入0。
●将0写入SCR.TE位。

IICSDAS[1:0]位（SDAn输出选择）

IICSDAS[1:0]位控制SDAn引脚的输出。在正常操作期间将IICSDAS[1:0]和IICSCLS[1:0]设置为相同的值。

IICSCLS[1:0]位（SCLn输出选择）

IICSCLS[1:0]位控制SCLn引脚的输出。在正常操作期间将IICSDAS[1:0]和IICSCLS[1:0]设置为相同的值。

30.2.27 SISR:IIC状态寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	IICACKR
重置后的值：	0	0	x	x	0	x	0	0

Bit	Symbol	Function	R/W
0	IICACKR	ACK接收数据标志 0：收到ACK1：收到NACK	R
1	—	该位读为0。	R
2	—	读取值未定义。	R
3	—	该位读为0。	R
5:4	—	读取值未定义。	R
7:6	—	这些位读为0。	R

SISR在简单IIC模式下监控状态。

IICACKR标志（ACK接收数据标志）

接收到的ACK和NACK位可以从IICACKR标志中读取。IICACKR标志在上升沿更新
接收到的ACKNACK位的SCLn时钟。

30.2.28 SPMR : SPI Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKPH	CKPOL	—	MFF	CSTPEN	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSE	SSn Pin Function Enable 0: Disable SSn pin function 1: Enable SSn pin function	R/W*1
1	CTSE	CTS Enable 0: Disable CTS function (enable RTS output function) 1: Enable CTS function	R/W*1
2	MSS	Master Slave Select 0: Transmit through TXDn pin and receive through RXDn pin (master mode) 1: Receive through TXDn pin and transmit through RXDn pin (slave mode)	R/W*1
3	CSTPEN	CTS external pin Enable 0: Alternate setting to use CTS and RTS functions as either one terminal 1: Dedicated setting for separately using CTS and RTS functions with 2 terminals These bits for the other SCI channels than SCIn (n = 0, 3 to 9) are reserved.	R/W
4	MFF	Mode Fault Flag 0: No mode fault error 1: Mode fault error	R/W*2
5	—	This bit is read as 0. The write value should be 0.	R/W
6	CKPOL	Clock Polarity Select 0: Do not invert clock polarity 1: Invert clock polarity	R/W*1
7	CKPH	Clock Phase Select 0: Do not delay clock 1: Delay clock	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).
Note 2. Only 0 can be written to this bit, to clear the flag.

SPMR selects the extension settings in asynchronous and clock synchronous modes.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 to use the SSn pin to control transmission and reception in simple SPI mode. Set this bit to 0 in all other modes. In simple SPI mode, when master mode is selected (SCR.CKE[1:0] = 00b and SPMR.MSS = 0) and there is a single master, the SSn pin on the master side is not required to control reception and transmission. In such a case, set the SSE bit to 0. Do not set both the SSE and CTSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 if the SSn pin is to be used for inputting the CTS control signal to control transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

MSS bit (Master Slave Select)

The MSS bit selects master or slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when this bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin.

30.2.28 SPMR:SPI模式寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)
SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CKPH	CKPOL	—	MFF	CSTPEN	MSS	CTSE	SSE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSE	SSn引脚功能使能 0：禁用SSn引脚功能1：启用SSn引脚功能	R/W*1
1	CTSE	CTS Enable 0：关闭CTS功能（开启RTS输出功能）1：开启CTS功能	R/W*1
2	MSS	主从选择 0：通过TXDn引脚发送并通过RXDn引脚接收（主模式）1：通过TXDn引脚接收并通过RXDn引脚发送（从模式）	R/W*1
3	CSTPEN	CTS外部引脚使能 0：将CTS和RTS功能用作一个端子的交替设置1：单独使用2个端子的CTS和RTS功能的专用设置这些位保留用于除SCIn之外的其他SCI通道（n=0、3至9）。	R/W
4	MFF	模式故障标志 0：无模式故障错误1 ：模式故障错误	R/W*2
5	—	该位读取为0。写入值应为0。	R/W
6	CKPOL	时钟极性选择 0：不反转时钟极性1：反转时钟极性	R/W*1
7	CKPH	时钟相位选择 0：不延迟时钟1：延迟时钟	R/W*1

注1.只有当SCR寄存器中的RE和TE位为0（串行发送和接收都被禁止）时，才能写入这些位。

注2.该位只能写入0，以清除标志。

SPMR在异步和时钟同步模式下选择扩展设置。

SSE位（SSn引脚功能使能）

将SSE位设置为1以使用SSn引脚控制简单SPI模式下的发送和接收。在所有其他模式下将此位设置为0。在简单的SPI模式下，选择主模式（SCR.CKE[1：0]=00B和SPMR.MSS=0），并且有一个主人，主侧不需要SSNPIN来控制接收和传输.在这种情况下，请将SSE位设置为0。不要将SSE和CTSE位都设置为1。如果进行此设置，则操作与将这些位设置为0时的操作相同。

CTSE bit (CTS Enable)

如果SSn引脚用于输入CTS控制信号以控制发送和接收，请将CTSE位设置为1。该位设置为0时输出RTS信号。在智能卡接口模式、简单SPI模式和简单模式下设置该位为0
IIC模式。不要将CTSE和SSE位都设置为1。如果进行此设置，则操作与将这些位设置为0时的操作相同。

MSS位（主从选择）

MSS位选择简单SPI模式下的主机或从机操作。当该位设置为1时，TXDn和RXDn引脚的功能相反，因此数据通过TXDn引脚接收并通过RXDn引脚发送。

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Set this bit to 0 in modes other than simple SPI mode.

CSTPEN bit (CTS external pin Enable)

Select the terminals usage method when using the CTS and RTS functions.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading this flag.

[Setting condition]

- When input on the SSn pin is low during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- On writing 0 to the bit after it is read as 1.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 30.99 for details. Set the CKPOL bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 30.99 for details. Set the CKPH bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

30.2.29 FCR : FIFO Control Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FM	FIFO Mode Select Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. 0: Non-FIFO mode. Selects TDR/RDR or TDRHL/RDRHL for communication. 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1
1	RFRST	Receive FIFO Data Register Reset Valid only when FCR.FM = 1. 0: Do not reset FRDRHL 1: Reset FRDRHL	R/W
2	TFRST	Transmit FIFO Data Register Reset Valid only when FCR.FM = 1. 0: Do not reset FTDRHL 1: Reset FTDRHL	R/W
3	DRES	Receive Data Ready Error Select Selects the interrupt requested when detecting receive data ready. 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI)	R/W
7:4	TTRG[3:0]	Transmit FIFO Data Trigger Number Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. The trigger number is specified in the TTRG[3:0] bits.	R/W

在简单SPI模式以外的模式下将此位设置为0。

CSTPEN位（CTS外部引脚使能）

使用CTS和RTS功能时选择终端使用方法。

MFF标志（模式故障标志）

MFF标志指示模式故障错误。在多主机配置中，通过读取该标志确定模式故障错误发生。

[Setting condition]

●在简单SPI模式（SSE位=1和MSS位=0）的主机操作期间，SSn引脚上的输入为低电平。

[Clearing condition]

●读为1后向该位写入0。

CKPOL位（时钟极性选择）

CKPOL位选择通过SCKn引脚输出的时钟信号的极性。详见图30.99。设置在除简单SPI模式和时钟同步模式之外的所有模式中，CKPOL位为0。

CKPH位（时钟相位选择）

CKPH位选择通过SCKn引脚输出的时钟信号的相位。详见图30.99。设置CKPH位在除简单SPI模式和时钟同步模式之外的所有模式下为0。

30.2.29 FCR：先进先出控制寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
重置后的值：	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FM	先进先出模式选择 仅在异步模式下有效，包括多处理器模式或时钟同步模式。 0: Non-FIFO mode. 选择TDRRDR或TDRHLRDRHL进行通信。 1: FIFO mode. 选择FTDRHLFRDRHL进行通信。	R/W*1
1	RFRST	接收FIFO数据寄存器复位 仅当FCR.FM=1时有效。 0：不复位FRDRHL1：复位FRDRHL	R/W
2	TFRST	发送FIFO数据寄存器复位 仅当FCR.FM=1时有效。 0：不复位FTDRHL1：复位FTDRHL	R/W
3	DRES	接收数据就绪错误选择 当检测到接收数据就绪时选择请求的中断。 0：接收数据满中断（SCIn_RXI）1：接收错误中断（SCIn_ERI）	R/W
7:4	TTRG[3:0]	发送FIFO数据触发数 仅在异步模式下有效，包括多处理器模式或时钟同步模式。触发编号在TTRG[3:0]位中指定。	R/W

Bit	Symbol	Function	R/W
11:8	RTRG[3:0]	Receive FIFO Data Trigger Number Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode. The trigger number is specified in the RTRG[3:0] bits.	R/W
15:12	RSTRG[3:0]	RTS Output Active Trigger Number Select Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0. The trigger number is specified in the RSTRG[3:0] bits.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

FCR selects FIFO mode, resets FTDRHL and FRDRHL, selects the FIFO data trigger number for transmission or reception, and selects the RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR, or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

When the RFRST bit is set to 1, the FRDRHL register is reset and the received data count resets to 0. When 1 is written to the RFRST bit, it clears to 0 after 1 PCLK.

TFRST bit (Transmit FIFO Data Register Reset)

When the TFRST bit is set to 1, the FTDRHL register is reset and the transmit data count resets to 0. When 1 is written to the TFRST bit, it clears to 0 after 1 PCLK.

DRES bit (Receive Data Ready Error Select)

When detecting a receive data ready error, the selection can be made from an SCIn_RXI interrupt request or an SCIn_ERI interrupt request. When starting DTC or DMAC and reading from the FRDRH and FRDRL registers, set the DRES bit to 1.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in FTDRHL is equal to or less than the transmit triggering number specified in the TTRG[3:0] bits, and software can write data to FTDRHL. If SCR.TIE = 1, an SCIn_TXI interrupt request occurs.

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in FRDRHL is equal to or greater than the receive triggering number specified in the RTRG[3:0] bits, and software can read data from FRDRHL. If SCR.RIE = 1, an SCIn_RXI interrupt request occurs.

When RTRG[3:0] is 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0, and an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in FRDRHL is equal to or greater than the receive triggering number specified in the RSTRG[3:0] bits, the RTS signal goes high.

When RSTRG[3:0] is 0, the RTS signal does not go high even when the amount of data in FRDRHL is equal to 0.

30.2.30 FDR : FIFO Data Count Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:8	RTRG[3:0]	接收FIFO数据触发数 仅在异步模式下有效，包括多处理器模式或时钟同步模式。触发编号在RTRG[3:0]位中指定。	R/W
15:12	RSTRG[3:0]	RTS输出有源触发数选择 仅在异步模式下有效，包括多处理器模式或时钟同步模式，当FCR.FM=1、SPMR.CTSE=0和SPMR.SSE=0时。触发数在RSTRG[3:0]中指定位。	R/W

注1.仅当TE=0且RE=0时可写。

FCR选择FIFO模式，复位FTDRHL和FRDRHL，选择发送或接收的FIFO数据触发数，选择RTS输出激活触发数。

FM位（FIFO模式选择）

当FM位设置为1时，选择FTDRHL和FRDRHL进行通信。当FM位设置为0时，TDR和选择RDR或TDRHL和RDRHL进行通信。

RFRST位（接收FIFO数据寄存器复位）

当RFRST位设置为1时，FRDRHL寄存器复位，接收数据计数复位为0。当向RFRST位写入1时，它在1个PCLK后清除为0。

TFRST位（发送FIFO数据寄存器复位）

当TFRST位设置为1时，FTDRHL寄存器复位并且发送数据计数复位为0。当1写入TFRST位时，它在1个PCLK后清除为0。

DRES位（接收数据就绪错误选择）

当检测到接收数据就绪错误时，可以从SCIn_RXI中断请求或SCIn_ERI中断请求中进行选择。启动DTC或DMAC并读取FRDRH和FRDRL寄存器时，将DRES位设置为1。

TTRG[3:0]位（发送FIFO数据触发编号）

当FTDRHL中的发送数据量等于或小于TTRG[3:0]位中指定的发送触发数时，TDFE标志设置为1，并且软件可以将数据写入FTDRHL。如果SCR.TIE=1，则发生SCIn_TXI中断请求。

RTRG[3:0]位（接收FIFO数据触发编号）

当FRDRHL中的接收数据量等于或大于RTRG[3:0]位中指定的接收触发数时，RDF标志设置为1，并且软件可以从FRDRHL中读取数据。如果SCR.RIE=1，则发生SCIn_RXI中断请求。

当RTRG[3:0]为0时，即使接收FIFO中的数据量等于0，RDF标志也不置位，并且SCIn_RXI中断不发生。

RSTRG[3:0]位（RTS输出有效触发数选择）

当FRDRHL中存储的接收数据量等于或大于RSTRG[3:0]位中指定的接收触发数时，RTS信号变为高电平。

当RSTRG[3:0]为0时，即使FRDRHL中的数据量等于0，RTS信号也不会变高。

30.2.30 FDR:FIFO数据计数寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	T[4:0]					—	—	—	R[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	R[4:0]	Receive FIFO Data Count Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of receive data stored in FRDRHL.	R
7:5	—	These bits are read as 0.	R
12:8	T[4:0]	Transmit FIFO Data Count Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of non-transmitted data stored in FTDRHL.	R
15:13	—	These bits are read as 0.	R

The FDR register indicates the amount of data stored in FRDRHL and FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. 0x00 means no receive data, and 0x10 means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. 0x00 means no transmit data, and 0x10 means that all (maximum amount) of the data to be transmitted is stored in FTDRHL.

30.2.31 LSR : Line Status Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ORER	Overrun Error Flag Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, and when FIFO is selected. 0: No overrun error occurred 1: Overrun error occurred	R*1
1	—	This bit is read as 0.	R
6:2	FNUM[4:0]	Framing Error Count Indicates the amount of data with a framing error in the receive data stored in FRDRHL.	R
7	—	This bit is read as 0.	R
12:8	PNUM[4:0]	Parity Error Count Indicates the amount of data with a parity error in the receive data stored in FRDRHL.	R
15:13	—	These bits are read as 0.	R

Note 1. Write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the receive error status.

ORER flag (Overrun Error Flag)

The ORER flag reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The FNUM[4:0] value indicates the amount of data with a framing error stored in the FRDRHL register.

Bit	Symbol	Function	R/W
4:0	R[4:0]	ReceiveFIFODataCount仅在异步模式下有效，包括多处理器模式，或时钟同步模式，当FCR.FM=1时。表示FRDRHL中存储的接收数据量。	R
7:5	—	这些位读为0。	R
12:8	T[4:0]	TransmitFIFODataCount仅在异步模式下有效，包括多处理器模式或时钟同步模式，当FCR.FM=1时。表示存储在FTDRHL中的未发送数据量。	R
15:13	—	这些位读为0。	R

FDR寄存器指示存储在FRDRHL和FTDRHL中的数据量。

R[4:0]位（接收FIFO数据计数）

R[4:0]位指示存储在FRDRHL中的接收数据量。0x00表示没有接收数据，0x10表示最大接收数据存储在FRDRHL中。

T[4:0]位（发送FIFO数据计数）

T[4:0]位指示存储在FTDRHL中的未传输数据量。0x00表示没有传输数据，0x10表示所有（最大量）要传输的数据都存储在FTDRHL中。

30.2.31 LSR：线路状态寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ORER	溢出错误标志 仅在异步模式下有效，包括多处理器模式或时钟同步模式，以及选择FIFO时。 0：未发生溢出错误1：发生溢出错误	R*1
1	—	该位读为0。	R
6:2	FNUM[4:0]	帧错误计数 表示FRDRHL中存储的接收数据中存在帧错误的数据量。	R
7	—	该位读为0。	R
12:8	PNUM[4:0]	奇偶错误计数 表示FRDRHL中存储的接收数据中有奇偶校验错误的数据量。	R
15:13	—	这些位读为0。	R

注1.将0写入SSR_FIFO.ORER以清除标志。

LSR寄存器指示接收错误状态。

ORER标志（溢出错误标志）

ORER标志反映了SSR_FIFO.ORER中的值。

FNUM[4:0]位（帧错误计数）

FNUM[4:0]值表示存储在FRDRHL寄存器中的具有帧错误的数据量。

PNUM[4:0] bits (Parity Error Count)

The PNUM[4:0] value indicates the amount of data with a parity error stored in the FRDRHL register.

30.2.32 CDR : Compare Match Data Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	Compare Match Data Holds compare data pattern for address match wakeup function.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the compare data for the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function, when the address match function is enabled (DCCR.DCME = 1).

Three bit lengths are available:

- CMPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length

30.2.33 DCCR : Data Compare Match Control Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCMF	Data Compare Match Flag 0: Not matched 1: Matched	R/(W)*1
2:1	—	These bits are read as 0. The write value should be 0.	R/W
3	DPER	Data Compare Match Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/(W)*1
4	DFER	Data Compare Match Framing Error Flag 0: No framing error occurred 1: Framing error occurred	R/(W)*1
5	—	This bit is read as 0. The write value should be 0.	R/W

PNUM[4:0]位（奇偶校验错误计数）

PNUM[4:0]值表示存储在FRDRHL寄存器中的具有奇偶校验错误的数据量。

30.2.32 CDR:比较匹配数据寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPD[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CMPD[8:0]	比较匹配数据 保存地址匹配唤醒功能的比较数据模式。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

CDR寄存器设置地址匹配功能的比较数据。

CMPD[8:0]位（比较匹配数据）

当地址匹配功能启用时（DCCR.DCME=1），CMPD[8:0]位设置要比较的数据以接收地址匹配功能的数据。

提供三种位长：

●CMPD[6:0]，7位长度

●CMPD[7:0]8位长度

●CMPD[8:0]，9位长度

30.2.33 DCCR:数据比较匹配控制寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
重置后的值：	0	1	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCMF	数据比较匹配标志 0：不匹配1：匹配	R/(W)*1
2:1	—	这些位被读取为0。写入值应为0。	R/W
3	DPER	数据比较匹配奇偶校验错误标志 0：未发生奇偶校验错误1：发生奇偶校验错误	R/(W)*1
4	DFER	数据比较匹配帧错误标志 0：未发生帧错误1：发生帧错误	R/(W)*1
5	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
6	IDSEL	ID Frame Select Valid only in asynchronous mode, including multi-processor mode. 0: Always compare data regardless of the MPB bit value 1: Only compare data when MPB bit = 1 (ID frame)	R/W
7	DCME	Data Compare Match Enable Valid only in asynchronous mode, including multi-processor mode. 0: Disable address match function 1: Enable address match function	R/W

Note 1. Only 0 can be written, to clear the flag after reading 1.

The DCCR register controls the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detected a receive data match with the comparison data (CDR.CMPD).

[Setting condition]

- On match of the comparison data (CDR.CMPD) with the receive data when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the SCR.RE bit to 0 does not affect the DCMF flag, which retains its previous value.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred on address match detection (receive data match detection).

[Setting condition]

- When a parity error is detected in a frame in which an address match is detected.

[Clearing conditions]

- When 0 is written after 1 is read from DPER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DPER flag is not affected and retains its previous value.

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurred on address match detection (receive data match detection).

[Setting conditions]

- When a stop bit of a frame in which an address match is detected is 0.

  When in 2-stop-bit mode, only the first bit of the stop bits is checked for a value of 1 (the second stop bit is not checked).

[Clearing conditions]

- When 0 is written after 1 is read from DFER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DFER flag is not affected and retains its previous value.

IDSEL bit (ID Frame Select)

The IDSEL bit selects whether to compare data regardless of the MPB bit value or to compare data only when MPB = 1 (ID frame), when the address match function is enabled.

DCME bit (Data Compare Match Enable)

The DCME bit enables or disables the address match function (data compare match function).

If the SCI detects a match to the comparison data (CDR.CMPD) with the receive data, the DCME bit clears automatically, after which SCI operation mode is in normal receive mode. See section 30.3.6. Address Match (Receive Data Match Detection) Function.

Bit	Symbol	Function	R/W
6	IDSEL	ID帧选择 仅在异步模式下有效，包括多处理器模式。 0：无论MPB位值如何，始终比较数据1：仅当MPB位=1时比较数据（ID帧）	R/W
7	DCME	数据比较匹配启用 仅在异步模式下有效，包括多处理器模式。 0：禁用地址匹配功能1：启用地址匹配功能	R/W

注1.只能写入0，读取1后清除标志。

DCCR寄存器控制地址匹配功能。

DCMF标志（数据比较匹配标志）

DCMF标志表示SCI检测到接收数据与比较数据(CDR.CMPD)匹配。

[Setting condition]

●当DCCR.DCME=1时，比较数据(CDR.CMPD)与接收数据匹配。

[Clearing condition]

●从DCMF读取1后写入0时。

将SCR.RE位清除为0不会影响DCMF标志，它保留其先前的值。

DPER标志（数据比较匹配奇偶校验错误标志）

DPER标志表示在地址匹配检测（接收数据匹配检测）时发生奇偶校验错误。

[Setting condition]

●在检测到地址匹配的帧中检测到奇偶校验错误时。

[Clearing conditions]

●从DPER读取1后写入0时。

当SCR.RE位设置为0（禁用串行接收）时，DPER标志不受影响并保留其先前的值。

DFER标志（数据比较匹配帧错误标志）

DFER标志表示在地址匹配检测（接收数据匹配检测）时发生了帧错误。

[Setting conditions]

●当检测到地址匹配的帧的停止位为0时。

在2停止位模式下，仅检查停止位的第一位是否为1（不检查第二个停止位）。

[Clearing conditions]

●从DFER读取1后写入0时。

当SCR.RE位设置为0（禁用串行接收）时，DFER标志不受影响并保留其先前的值。

IDSEL位（ID帧选择）

IDSEL位选择无论MPB位值如何比较数据，还是仅在MPB=1（ID帧）时比较数据，当地址匹配功能启用时。

DCME位（数据比较匹配使能）

DCME位启用或禁用地址匹配功能（数据比较匹配功能）。

如果SCI检测到比较数据（CDR.CMPD）与接收数据匹配，则DCME位自动清零，此后SCI操作模式进入正常接收模式。请参见第30.3.6节。地址匹配（接收数据匹配检测）功能。

The write value must be 0 for all modes other than asynchronous mode.

30.2.34 SPTR : Serial Port Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ATEN	ASEN	TINV	RINV	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	RXDMON	Serial Input Data Monitor Indicates the state of the RXDn pin. 0: When RINV is 0, RXDn terminal is the low level. When RINV is 1, RXDn terminal is the High level. 1: When RINV is 0, RXDn terminal is the High level. When RINV is 1, RXDn terminal is the Low level.	R
1	SPB2DT	Serial Port Break Data Select Selects the output level of the TXDn pin when SCR.TE = 0. 0: When TINV is 0, Low level is output in TXDn terminal. When TINV is 1, High level is output in TXDn terminal. 1: When TINV is 1'b0, High level is output in TXDn terminal. When TINV is 1'b1, Low level is output in TXDn terminal.	R/W
2	SPB2IO	Serial Port Break I/O*1 Selects whether the value of SPB2DT is output to TXDn pin. 0: Do not output value of SPB2DT bit on TXDn pin 1: Output value of SPB2DT bit on TXDn pin	R/W
3	—	These bits are read as 0. The write value should be 0.	R/W
4	RINV	RXD invert bit 0: Received data from RXDn is not inverted and input.*2 1: Received data from RXDn is inverted and input.	R/W*3
5	TINV	TXD invert bit 0: Transmit data is not inverted and output to TXDn.*2 1: Transmit data is inverted and output to TXDn.	R/W*3
6	ASEN	Adjust receive sampling timing enable (This bit enables in asynchronous mode using internal clock) This function can adjust the receive sampling timing. In asynchronous mode using internal clock, see section 30.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in detail. 0: Adjust sampling timing disable. 1: Adjust sampling timing enable.	R/W*3
7	ATEN	Adjust transmit timing enable (This bit enables in asynchronous mode using internal clock) This function can adjust the transmit edge of TXDn waveform. See section 30.3.11. The function of adjust transmit timing (Asynchronous Mode) in detail. 0: Adjust transmit timing disable. 1: Adjust transmit timing enable.	R/W*3

Note 1. Please use this bit in asynchronous mode and manchester mode. Movement by other mode isn't guaranteed.
Note 2. RINV/TINV should be set to 0 in smart card interface mode and simple I2C mode.
Note 3. Change the value of these bits only at SCR.TE = SCR.RE = 0.

The SPTR register provides confirmation of the serial reception pin (RXDn pin) status and sets the transmission and receive pin status.

And SPTR register has enable bits for adjust functions of receive sampling timing and transmit timing.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO, and SPTR.SPB2DT settings, as shown in Table 30.25.

对于异步模式以外的所有模式，写入值必须为0。

30.2.34 SPTR:串行端口寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ATEN	ASEN	TINV	RINV	—	SPB2IO	SPB2DT	RXDMON
重置后的值:	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
0	RXDMON	串行输入数据监视器 指示RXDn引脚的状态。 0：当RINV为0时，RXDn端为低电平。当RINV为1时，RXDn端为高电平。 1：当RINV为0时，RXDn端为高电平。当RINV为1时，RXDn端为低电平。	R
1	SPB2DT	串行端口中断数据选择 选择SCR.TE=0时TXDn引脚的输出电平。 0：当TINV为0时，TXDn端输出低电平。当TINV为1时，TXDn端输出高电平。 1：当TINV为1'b0时，TXDn端输出高电平。当TINV为1'b1时，TXDn端输出低电平。	R/W
2	SPB2IO	串口中断IO*1 选择是否将SPB2DT的值输出到TXDn引脚。 0：不输出TXDn引脚上SPB2DT位的值1：输出TXDn引脚上SPB2DT位的值	R/W
3	—	这些位被读取为0。写入值应为0。	R/W
4	RINV	RXD反转位 0：从RXDn接收的数据不反相输入。*2 1：从RXDn接收到的数据被反转并输入。	R/W*3
5	TINV	TXD反转位 0：发送数据不反相并输出到TXDn。*2 1：发送数据反转并输出到TXDn。	R/W*3
6	ASEN	调整接收采样时序使能（该位在使用内部时钟的异步模式下使能）该功能可以调整接收采样时序。 在使用内部时钟的异步模式下，请参阅第30.3.10节。详细调整接收采样时间（异步模式）的功能。 0：调整采样时序禁用。1：调整采样时序使能。	R/W*3
7	ATEN	调整发送时序使能（该位在使用内部时钟的异步模式下使能）该功能可以调整TXDn波形的发送边沿。请参阅第30.3.11节。详细调整发送时间（异步模式）的功能。 0：调整发送时序禁用。1：调整发送时序使能。	R/W*3

注1.请在异步模式和曼彻斯特模式下使用该位。不能保证通过其他模式移动。
注2.RINVTINV在智能卡接口模式和简单I2C模式下应设置为0。
注3.仅在SCR.TE=SCR.RE=0时更改这些位的值。

SPTR寄存器提供串行接收引脚（RXDn引脚）状态的确认，并设置发送和接收引脚状态。

SPTR寄存器具有调整接收采样时序和发送时序功能的使能位。

TXDn引脚状态由SCR.TE、SPTR.SPB2IO和SPTR.SPB2DT设置的组合决定，如表30.25所示。

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The data of RDR is controlled by RINV and SCMR.SINV. And the data from TXDn terminal is controlled by TINV and SCMR.SINV. The control by RINV/TINV are done to communication terminals(RXDn/TXDn), so they can control not only data-bits but also other bits (start bit, stop bit, parity bit). Please refer to Figure 30.5 in detail.

Table 30.25 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	—	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	—	—	Serial transmit data is output

Note: —: Do not care.
Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

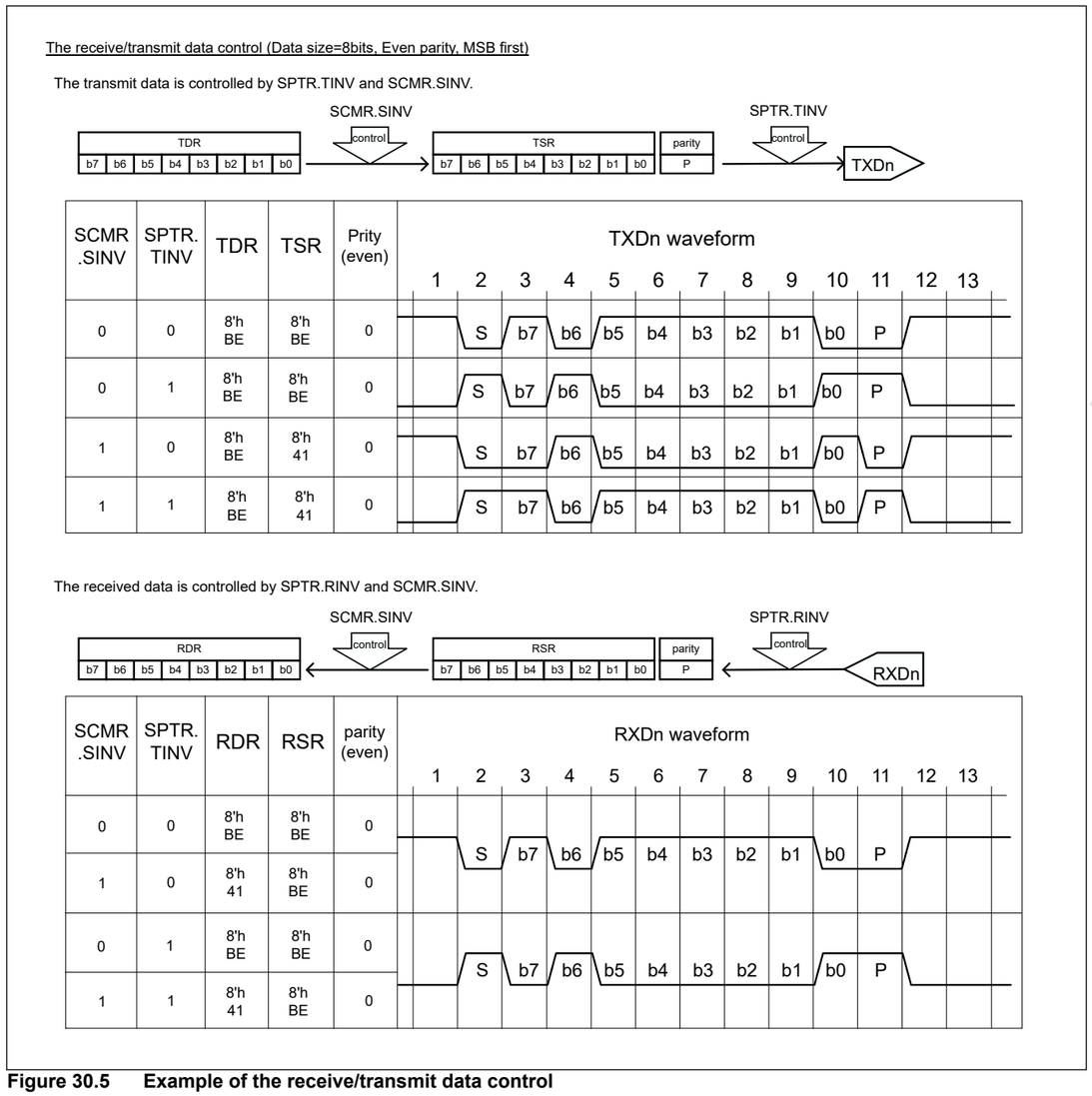

Figure 30.5 Example of the receive/transmit data control

RDR的数据由RINV和SCMR.SINV控制。来自TXDn终端的数据由TINV和SCMR.SINV。RINVTINV的控制是对通信终端（RXDnTXDn）进行的，因此它们不仅可以控制数据位，还可以控制其他位（起始位、停止位、奇偶校验位）。详细请参考图30.5。

Table 30.25 TXDn引脚状态

SCR.TE的价值	SPTR.SPB2IO的值	SPTR.SPB2DT的值	TXDn引脚状态
0	0	—	Hi-Z (initial value)
0	1	0	低电平输出
0	1	1	高电平输出
1	—	—	串行传输数据输出

Note: -：不管。
Note: 仅在异步模式下使用SPTR寄存器。不保证在任何其他模式下使用该寄存器。

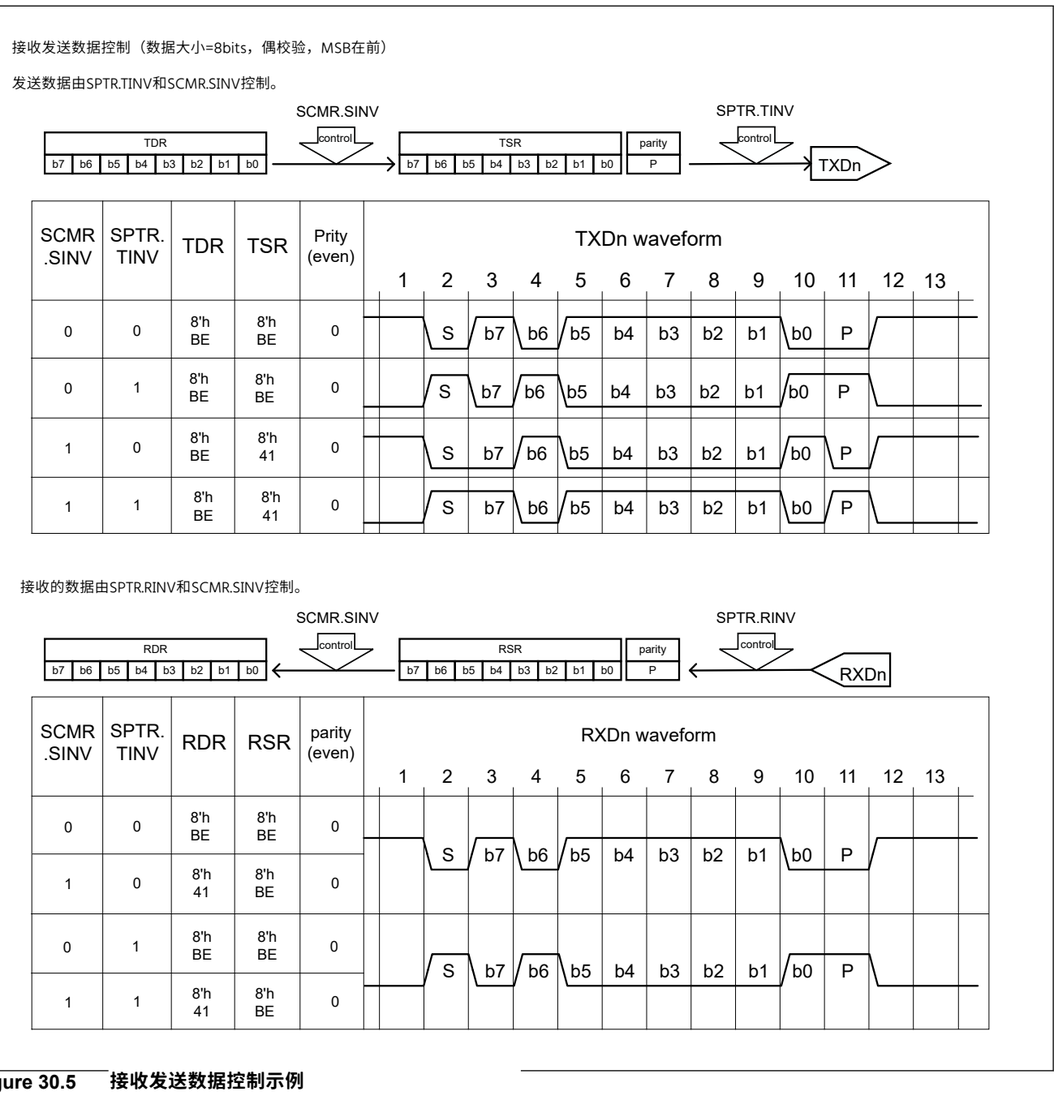

Figure 30.5 接收发送数据控制示例

30.2.35 ACTR : Adjustment Communication Timing Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AET	ATT[2:0]			AJD	AST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	AST	Adjustment value for receive Sampling Timing The sampling timing of RXD terminal is adjusted from the middle of bit by the following formula. Adjustment sampling timing = base clock * the setting value of AST[2:0]. This bit is effective only at SPTR.ASEN = 1. This setting timing is limited by setting the base clock cycles. Refer to section 30.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in detail.	R/W*1
3	AJD	Adjustment Direction for receive sampling timing Adjustment direction for RXD receive sampling timing is determined by this bit. 0: The sampling timing is adjusted backward to the middle of bit. 1: The sampling timing is adjusted forward to the middle of bit. This bit is effective only at SPTR.ASEN = 1. Refer to section 30.3.10. The function of adjust receive sampling timing (Asynchronous Mode) in detail.	R/W*1
6:4	ATT	Adjustment value for Transmit timing The selected edge timing of TXD is adjusted by the following formula. Adjustment edge timing = base clock * the setting value of ATT[2:0]. This bit is effective only at SPTR.ATEN = 1. This setting timing is limited by setting the base clock cycles. Refer to section 30.3.11. The function of adjust transmit timing (Asynchronous Mode) in detail.	R/W*2
7	AET	Adjustment edge for transmit timing The adjustable edge is set by this bit. When SPTR.TINV is 0, 0: Adjust the rising edge timing. 1: Adjust the falling edge timing. When SPTR.TINV is 1, 0: Adjust the falling edge timing. 1: Adjust the rising edge timing. This bit is effective only at SPTR.ATEN = 1. Refer to section 30.3.11. The function of adjust transmit timing (Asynchronous Mode) in detail.	R/W*2

Note 1. Write this bit only when SPTR.ASEN = 0.
Note 2. Write this bit only when SPTR.ATEN = 0.

This register controls adjustment of receive sampling timing and transmit timing. This register is effective only when asynchronous mode using internal clock.

Refer to section 30.3.10. The function of adjust receive sampling timing (Asynchronous Mode) about adjustment receive sampling timing by this register.

Refer to section 30.3.11. The function of adjust transmit timing (Asynchronous Mode) about adjustment transmit timing by this register.

Note: Sentences and a timing chart of the IP operation explanation (except section 30.1. Overview, section 30.2. Register Descriptions, section 30.3.10. The function of adjust receive sampling timing (Asynchronous Mode) and section 30.3.11. The function of adjust transmit timing (Asynchronous Mode)) are mentioned by the condition that the function added in SCIM-7 is off (SPTR.ASEN = 0, SPTR.ATEN = 0).

30.2.35 ACTR:调整通信时序寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 0, 3 to 9)

Offset address: 0x1D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AET	ATT[2:0]			AJD	AST[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	AST	接收采样时序的调整值 RXD端的采样时序由下式从位中间开始调整。调整采样时序=基准时钟*AST[2:0]的设置值。 该位仅在SPTR.ASEN=1时有效。此设置时序受设置基本时钟周期的限制。请参阅第30.3.10节。详细调整接收采样时间（异步模式）的功能。	R/W*1
3	AJD	接收采样时序调整方向 RXD接收采样时序的调整方向由该位决定。 0：采样定时向后调整到位中间。1：采样定时向前调整到位中间。 该位仅在SPTR.ASEN=1时有效。请参阅第30.3.10节。详细调整接收采样时间（异步模式）的功能。	R/W*1
6:4	ATT	发送时间的调整值 TXD的选定边沿时序通过以下公式进行调整。 调整边沿时序=基准时钟*ATT[2:0]的设置值。 该位仅在SPTR.ATEN=1时有效。此设置时序受设置基本时钟周期的限制。请参阅第30.3.11节。详细调整发送时间（异步模式）的功能。	R/W*2
7	AET	发送定时的调整边沿 可调边沿由该位设置。 当SPTR.TINV为0时， 0：调整上升沿时序。1：调整下降沿时序。 当SPTR.TINV为1时， 0：调整下降沿时序。1：调整上升沿时序。 该位仅在SPTR.ATEN=1时有效。请参阅第30.3.11节。详细调整发送时间（异步模式）的功能。	R/W*2

注1.仅当SPTR.ASEN=0时写入该位。注2.仅当SPTR.ATEN=0时写入该位。

该寄存器控制接收采样时序和发送时序的调整。该寄存器仅在异步模式使用内部时钟时有效。

请参阅第30.3.10节。通过该寄存器调整接收采样时序的调整接收采样时序（异步模式）功能。

请参阅第30.3.11节。通过该寄存器调整发送时序的调整发送时序（异步模式）功能。

Note: IP操作说明的语句和时序图（30.1节概述、30.2节注册除外）
说明，第30.3.10节。调整接收采样时间（异步模式）的功能和第30.3.11节。调整发送时间（异步模式）的功能是在SCIM-7中添加的功能关闭（SPTR.ASEN=0，SPTR.ATEN=0）的条件下提到的。

RA生态工作室

30.2.36 MMR : Manchester Mode Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MANEN	SBSEL	SYNSEL	SYNVAL	—	ERTEN	TMPOL	RMPOL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMPOL	Polarity of Received Manchester Code Sets the polarity of the received Manchester code 0: Logic 0 is coded as a zero-to-one transition in Manchester code Logic 1 is coded as a one-to-zero transition in Manchester code 1: Logic 0 is coded as a one-to-zero transition in Manchester code Logic 1 is coded as a zero-to-one transition in Manchester code	R/W*1
1	TMPOL	Polarity of Transmit Manchester Code Sets the polarity of the transmit Manchester code 0: Logic 0 is coded as a zero-to-one transition in Manchester code Logic 1 is coded as a one-to-zero transition in Manchester code 1: Logic 0 is coded as a one-to-zero transition in Manchester code Logic 1 is coded as a zero-to-one transition in Manchester code	R/W*1
2	ERTEN	Manchester Edge Retiming Enable Sets the receive retiming function 0: Disables the receive retiming function 1: Enables the receive retiming function	R/W*1
3	—	This bit is read as 0. The write value should be 0.	R
4	SYNVAL	SYNC value Setting Sets the SYNC type of the start bit(s) in the Manchester code When the start bit area consists of one bit.(SBSEL = "0") ● when transmitting 0: The start bit is added as a zero-to-one transition. 1: The start bit is added as a one-to-zero transition. ● when receiving 0: Only when the start bit is a zero-to-one transition, the data is received. The other cases are judged as an error. 1: Only when the start bit is a one-to-zero transition, the data is received. The other cases are judged as an error. When the start bit area consists of three bits.(SBSEL = "1") ● when transmitting 0: The start bits are added as a zero-to-one transition. (DATA SYNC) 1: The start bits are coded as a one-to-zero transition. (COMMAND SYNC) ● when receiving When the start bit area consists of three bits, data is received regardless of the value of this bit.	R/W*1
5	SYNSEL	SYNC Select 0: The start bit pattern is set with the SYNVAL bit 1: The start bit pattern is set with the TSYNC bit.	R/W*1
6	SBSEL	Start Bit Select 0: The start bit area consists of one bit. 1: The start bit area consists of three bits (COMMAND SYNC or DATA SYNC)	R/W*1
7	MANEN	Manchester Mode Enable Sets the Manchester mode 0: Disables the Manchester mode 1: Enables the Manchester mode	R/W*1

Note: Bits 6 to 0 in this register are valid only when the Manchester mode is enabled.(MANEN = "1") in bit 7.
Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

This register is used to enable or disable the Manchester mode, set the start bit area, and set the logic polarity.

30.2.36 MMR:曼彻斯特模式寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MANEN	SBSEL	SYNSEL	SYNVAL	—	ERTEN	TMPOL	RMPOL
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMPOL	接收到的曼彻斯特码的极性 设置接收到的曼彻斯特码的极性 0：逻辑0编码为曼彻斯特码中的零到一转换逻辑1编码为曼彻斯特码中的一到零转换 1：逻辑0被编码为曼彻斯特码中的1到零转换逻辑1被编码为曼彻斯特码中的0到1转换	R/W*1
1	TMPOL	发送曼彻斯特码的极性 设置发送曼彻斯特码的极性 0：逻辑0编码为曼彻斯特码中的零到一转换逻辑1编码为曼彻斯特码中的一到零转换 1：逻辑0被编码为曼彻斯特码中的1到零转换逻辑1被编码为曼彻斯特码中的0到1转换	R/W*1
2	ERTEN	曼彻斯特边缘重定时启用 设置接收重定时功能 0：关闭接收重定时功能1：打开接收重定时功能	R/W*1
3	—	该位读取为0。写入值应为0。	R
4	SYNVAL	SYNC值设置 设置曼彻斯特代码中起始位的SYNC类型 起始位区域为1位时。(SBSEL="0")● 传输时 0：添加起始位作为从零到一的转换。1：添加起始位作为1到零的转换。 ● 接收时 0：仅当起始位为0到1转换时，才接收数据。其他情况判断为错误。 1：仅当起始位为1到零跳变时，才接收数据。其他情况判断为错误。 当起始位区域由三位组成时。(SBSEL="1")● 传输时 0：添加起始位作为零到一的转换。(DATASYNC)1：起始位被编码为一个从一到零的转换。（命令同步） ●接收时当起始位区域由三位组成时，无论该位的值如何，都将接收数据。	R/W*1
5	SYNSEL	同步选择 0：使用SYNVAL位设置起始位模式1：使用TSYNC位设置起始位模式。	R/W*1
6	SBSEL	起始位选择 0：起始位区域由一位组成。1：起始位区域由三位组成（COMMANDSYNC或DATASYNC）	R/W*1
7	MANEN	ManchesterModeEnable设置曼彻斯特模式 0：禁用曼彻斯特模式1：启用曼彻斯特模式	R/W*1

Note: 该寄存器中的位6到0仅在启用曼彻斯特模式时有效。（MANEN="1"）在位7中。
注1.只有当SCR中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

该寄存器用于启用或禁用曼彻斯特模式、设置起始位区域和设置逻辑极性。

RMPOL bit (Polarity of Received Manchester Code)

This bit sets the polarity of the received Manchester code. For details, see section 30.5.7. Serial Data Reception in Manchester Mode.

TMPOL bit (Polarity of Transmit Manchester Code)

This bit sets the polarity of the transmit Manchester code. For details, see section 30.5.6. Serial data transmission in Manchester mode.

ERTEN bit (Manchester Edge Retiming Enable)

This bit sets the receive retiming function in Manchester mode.

For information on the receive retiming function, see section 30.5.9. Receive Retiming.

SYNVAL bit (SYNC value Setting)

This bit is valid when the SYNSEL bit of this register is set to “0”.

The SYNC type can be set by combining this bit and the SBSEL bit.

For the start bit area determined by the combination of this bit and the SBSEL bit, see Figure 30.52 and Figure 30.53.

SYNSEL bit (SYNC Select)

This bit is valid when the SBSEL bit of this register is set to “1”. This bit determines the destination to be referred to for setting the SYNC type of the start bit area added to Manchester frames.

When this bit is set to “0”, the SYNVAL bit of this register is referred to.

When this bit is set to “1”, the TSYNC bit in the TDRH register is referred to.

For detail, see the bit table in section 30.2.36. MMR : Manchester Mode Register.

SBSEL bit (Start Bit Select)

This bit sets the start bit area in Manchester frames.

When this bit is set to 1, the start bit area added to each frame consists of three bits, and the SYNSEL and SYNVAL bits in this register are valid.

When this bit is set to 0, the start bit area added to each frame consists of one bit.

MANEN bit (Manchester Mode Enable)

This bit sets the Manchester mode.

When this bit is set to 0, the Manchester mode is disabled.

When this bit is set to 1, the Manchester mode is enabled.

30.2.37 TMPR : Transmit Manchester Preface Setting Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	TPPAT[1:0]		TPLEN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TPLEN	Transmit preface length Set the preface length of the transmit data in Manchester mode 0x0: Disables the transmit preface generation Others: Transmit preface length (bit length)	R/W*1

RMPOL位（接收曼彻斯特码的极性）

该位设置接收到的曼彻斯特码的极性。有关详细信息，请参阅第30.5.7节。串行数据接收
曼彻斯特模式。

TMPOL位（发送曼彻斯特码的极性）

该位设置发送曼彻斯特码的极性。详见30.5.6节。串行数据传输
曼彻斯特模式。

ERTEN位（曼彻斯特边沿重定时使能）

该位设置曼彻斯特模式下的接收重定时功能。

有关接收重定时功能的信息，请参见第30.5.9节。接收重定时。

SYNVAL位（SYNC值设置）

当该寄存器的SYNSEL位设置为“0”时，该位有效。

SYNC类型可以通过组合该位和SBSEL位来设置。

由该位和SBSEL位组合决定的起始位区域见图30.52和图30.53。

SYNSEL bit (SYNC Select)

当该寄存器的SBSEL位设置为“1”时，该位有效。该位确定要参考的目标，以设置添加到曼彻斯特帧的起始位区域的SYNC类型。

当该位设置为“0”时，参考该寄存器的SYNVAL位。

当该位设置为“1”时，参考TDRH寄存器中的TSYNC位。

详情请参见30.2.36节中的位表。MMR：曼彻斯特模式寄存器。

SBSEL bit (Start Bit Select)

该位设置曼彻斯特帧中的起始位区域。

当该位设置为1时，添加到每帧的起始位区域由3位组成，该寄存器中的SYNSEL和SYNVAL位有效。

当该位设置为0时，添加到每一帧的起始位区域由一位组成。

MANEN位（曼彻斯特模式使能）

该位设置曼彻斯特模式。

当该位设置为0时，曼彻斯特模式被禁用。

当该位设置为1时，启用曼彻斯特模式。

30.2.37 TMPR：发送曼彻斯特前言设置寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	TPPAT[1:0]		TPLEN[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TPLEN	传输前言长度 设置曼彻斯特模式下发送数据的前言长度 0x0：禁用发送前言生成 其他：传输前言长度（位长）	R/W*1

Bit	Symbol	Function	R/W
5:4	TPPAT	Transmit preface pattern Set the preface pattern of the transmit data 0 0: ALL ZERO 0 1: ZERO ONE 1 0: ONE ZERO 1 1: ALL ONE	R/W*1
7:6	—	The read value is undefined. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).
Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

This register is used to set the preface length and preface pattern of the transmit data in Manchester mode.

TPLEN bit (Transmit preface length)

These bits set the preface bit length of the transmit data in Manchester mode.

The settable range is 0h to Fh (0d to 15d). 0h disables the transmit preface, which is not added.

TPPAT bit (Transmit preface pattern)

These bits set one of the four preface patterns in Manchester mode.

When these bits are set to 00b, the preface area is set to all zeros.

When these bits are set to 01b, the preface area is set to the zero-one-zero-one pattern.

When these bits are set to 10b, the preface area is set to the one-zero-one-zero pattern.

When these bits are set to 11b, the preface area is set to all ones.

Note: For the transmit and receive data when the TPPAT bits are set, see Figure 30.51.

30.2.38 RMPR : Receive Manchester Preface Setting Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x23

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	RPPAT[1:0]		RPLEN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	RPLEN	Receive Preface Length Set the preface length in received frames when Manchester mode is enabled 0: Disables the receive preface generation Others: Receive preface length (bit length)	R/W*1
5:4	RPPAT	Receive Preface Pattern Set the preface pattern of received frames 0 0: ALL ZERO 0 1: ZERO ONE 1 0: ONE ZERO 1 1: ALL ONE	R/W*1
7:6	—	These bits are read as 0. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).
Note 1. Writing to these bits is only possible when the RE and TE bits in SCR are 0 (both serial transmission and reception are disabled).

This register is used to set the preface length and preface pattern of the received frames in Manchester mode.

RPLEN bit (Receive Preface Length)

These bits set the preface bit length of the received frames in Manchester mode.

Bit	Symbol	Function	R/W
5:4	TPPAT	传输前言模式 设置发送数据的前言模式 00：全零01：零 一10：一个零11 ：全一	R/W*1
7:6	—	读取值未定义。写入值应为0。	R

Note: 该寄存器仅在启用曼彻斯特模式（MMR.MANEN=1）时有效。
注1.只有当SCR中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

该寄存器用于设置曼彻斯特模式下发送数据的前言长度和前言样式。

TPLEN位（发送前言长度）

这些位设置曼彻斯特模式下发送数据的前言位长度。

可设置范围为0h到Fh（0d到15d）。0h禁用未添加的发送前言。

TPPAT位（发送前言模式）

这些位设置曼彻斯特模式中的四个前言模式之一。

当这些位设置为00b时，前言区域设置为全零。

当这些位设置为01b时，前言区域设置为零一零一模式。

当这些位设置为10b时，前言区域设置为一零一零模式。

当这些位设置为11b时，前言区域设置为全1。

Note: 对于设置TPPAT位时的发送和接收数据，请参见图30.51。

30.2.38 RMPR:接收曼彻斯特前言设置寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x23

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	RPPAT[1:0]		RPLEN[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	RPLEN	接收序言长度 启用曼彻斯特模式时设置接收帧中的前言长度 0：禁用接收前言生成 其他：接收前言长度（位长）	R/W*1
5:4	RPPAT	接收前言模式 设置接收帧的前言模式 00：全零01：零 一10：一个零11 ：全一	R/W*1
7:6	—	这些位被读取为0。写入值应为0。	R

Note: 该寄存器仅在启用曼彻斯特模式（MMR.MANEN=1）时有效。
注1.只有当SCR中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

该寄存器用于设置曼彻斯特模式下接收帧的序言长度和序言模式。

RPLEN位（接收前言长度）

这些位设置曼彻斯特模式下接收帧的前言位长度。

The settable range is 0h to Fh (0d to 15d). 0h disables the receive preface, which is not added. When 1h to Fh is set, the set value is handled as the receive preface bit length.

RPPAT bit (Receive Preface Pattern)

These bits set one of the four preface patterns in Manchester mode.

When these bits are set to 00b, the preface area is handled as all zeros.

When these bits are set to 01b, the preface area is handled as the zero-one-zero-one pattern.

When these bits are set to 10b, the preface area is handled as the one-zero-one-zero pattern.

When these bits are set to 11b, the preface area is handled as all ones.

Note: For the transmit and receive data when the RPPAT bits are set, see Figure 30.51.

30.2.39 MESR : Manchester Extended Error Status Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SBER	SYER	PFER
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFER	Preface Error flag This bit is set when a preface error (pattern mismatch) is detected 0: No preface error detected 1: Preface error detected	R/(W)*1
1	SYER	SYNC Error flag This bit is set when no edge is detected in the adjustable range during receive retiming 0: No receive SYNC error detected 1: Receive SYNC error detected	R/(W)*1
2	SBER	Start Bit Error flag This bit is set when a pattern mismatch in the start bit area is detected 0: No start bit error detected 1: Start bit error detected	R/(W)*1
7:3	—	These bits are read as 0. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).
Note 1. Only 0 can be written to this bit, to clear the flag. To clear the flag, confirm that the flag is 1 before setting it to 0.

This register indicates an error status when receiving frames in Manchester mode.

A preface error, receive SYNC error or start bit error was detected.

PFER bit (Preface Error flag)

This bit indicates that a preface error was detected when receiving frames in Manchester mode.

[Setting condition]

- When detecting a preface error when receiving frames in Manchester mode
  The following operations are performed when a preface error occurs.
  When MECR.PFEREN = 1
  The received data is not transferred to the RDR register and no RXI interrupt request occurs. Instead, an ERI interrupt request occurs. Note that when the PFER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  When MECR.PFEREN = 0
  The received data is transferred to the RDR register and an RXI interrupt request occurs. An ERI interrupt request is not generated. The subsequent receive operations are not affected even with the PFER flag being set to 1.

可设置范围为0h到Fh（0d到15d）。0h禁用接收前言，没有添加。当设置1h至Fh时，设置值作为接收前言位长度处理。

RPPAT位（接收前言模式）

这些位设置曼彻斯特模式中的四个前言模式之一。

当这些位设置为00b时，前言区域被处理为全零。

当这些位设置为01b时，前言区域作为零一零一模式处理。

当这些位设置为10b时，前言区域作为一零一零模式处理。

当这些位被设置为11b时，前言区域被当作全1处理。

Note: 对于设置RPPAT位时的发送和接收数据，请参见图30.51。

30.2.39 MESR：曼彻斯特扩展错误状态寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SBER	SYER	PFER
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFER	前言错误标志 当检测到前言错误（模式不匹配）时设置该位 0：未检测到前言错误1：检测到前言错误	R/(W)*1
1	SYER	同步错误标志 当接收重定时期间在可调范围内未检测到边沿时，该位置位 0：未检测到接收同步错误1：检测到接收同步错误	R/(W)*1
2	SBER	起始位错误标志 当检测到起始位区域中的模式不匹配时，设置该位 0：未检测到起始位错误1：检测到起始位错误	R/(W)*1
7:3	—	这些位被读取为0。写入值应为0。	R

Note: 该寄存器仅在启用曼彻斯特模式（MMR.MANEN=1）时有效。
注1.该位只能写入0，以清除标志。要清除标志，请先确认标志为1，然后再将其设置为0。

该寄存器指示在曼彻斯特模式下接收帧时的错误状态。

检测到前言错误、接收同步错误或起始位错误。

PFER位（前言错误标志）

该位表示在曼彻斯特模式下接收帧时检测到前言错误。

[Setting condition]

●曼彻斯特模式接收帧时检测到前言错误出现前言错误时执行以下操作

◦

When MECR.PFEREN = 1
接收到的数据不会传输到RDR寄存器，也不会发生RXI中断请求。相反，会发生ERI中断请求。请注意，当PFER标志设置为1时，随后接收到的数据不会传输到RDR寄存器。

When MECR.PFEREN = 0
接收到的数据被传送到RDR寄存器并产生一个RXI中断请求。不产生ERI中断请求。即使PFER标志设置为1，后续接收操作也不受影响。

[Clearing condition]

- When 0 is written to the bit after it was read as 1

Even if the SCR.RE bit is cleared, the PFER flag is not affected, and the previous state is retained.

SYER bit (SYNC Error flag)

This bit indicates that a receive SYNC error was detected when receiving frames in Manchester mode with

MMR.ERTEN = 1 (Manchester edge retiming enabled).

[Setting condition]

- When detecting a receive SYNC error when receiving frames in Manchester mode
  The following operations are performed when a receive SYNC error occurs.
  When MECR.SYEREN = 1
  Although the received data is transferred to the RDR register, no RXI interrupt request occurs. Instead, an ERI interrupt request occurs. Note that when the SYER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  When MECR.SYEREN = 0
  The received data is transferred to the RDR register and an RXI interrupt request occurs. An ERI interrupt request is not generated. The subsequent receive operations are not affected even with the SYER flag being set to 1.

[Clearing condition]

- When 0 is written to the bit after it was read as 1

Even if the SCR.RE bit is cleared, the SYER flag is not affected, and the previous state is retained.

SBER bit (Start Bit Error flag)

This bit indicates that a start bit error was detected when receiving frames in Manchester mode.

[Setting condition]

- When detecting a start bit error when receiving frames in Manchester mode
  The following operations are performed when a start bit error occurs.
  When MECR.SBEREN = 1
  The received data is not transferred to the RDR register and no RXI interrupt request occurs. Instead, an ERI interrupt request occurs. Note that when the SBER flag is being set to 1, the subsequently received data is not transferred to the RDR register.
  When MECR.SBEREN = 0
  The received data is transferred to the RDR register and an RXI interrupt request occurs. An ERI interrupt request is not generated. The subsequent receive operations are not affected even with the SBER flag being set to 1.

[Clearing condition]

- When 0 is written to the bit after it was read as 1

Even if the SCR.RE bit is cleared, the SBER flag is not affected, and the previous state is retained.

30.2.40 MECR : Manchester Extended Error Control Register

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x25

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SBEREN	SYEREN	PFEREN
Value after reset:	0	0	0	0	0	0	0	0

[Clearing condition]

●读为1后写入0时

即使SCR.RE位被清除，PFER标志也不受影响，并且保持之前的状态。

SYER位（SYNC错误标志）

该位表示在曼彻斯特模式下接收帧时检测到接收同步错误

MMR.ERTEN=1（启用曼彻斯特边沿重定时）。

[Setting condition]

●在曼彻斯特模式下接收帧时检测到接收SYNC错误发生接收SYNC错误时执行
以下操作。

When MECR.SYEREN = 1
虽然接收到的数据被传送到RDR寄存器，但没有发生RXI中断请求。相反，会发生ERI中断请求。请注意，当SYER标志设置为1时，随后接收到的数据不会传输到RDR寄存器。

When MECR.SYEREN = 0
接收到的数据被传送到RDR寄存器并产生一个RXI中断请求。不产生ERI中断请求。即使SYER标志设置为1，后续的接收操作也不受影响。

[Clearing condition]

●读为1后写入0时

即使清除SCR.RE位，SYER标志也不受影响，并且保持之前的状态。

SBER位（起始位错误标志）

该位表示在曼彻斯特模式下接收帧时检测到起始位错误。

[Setting condition]

●在曼彻斯特模式下接收帧时检测到起始位错误发生起始位错误时执行
以下操作。

When MECR.SBEREN = 1
接收到的数据不会传输到RDR寄存器，也不会发生RXI中断请求。相反，会发生ERI中断请求。请注意，当SBER标志设置为1时，随后接收到的数据不会传输到RDR寄存器。

When MECR.SBEREN = 0
接收到的数据被传送到RDR寄存器并产生一个RXI中断请求。不产生ERI中断请求。即使SBER标志设置为1，后续接收操作也不受影响。

[Clearing condition]

●读为1后写入0时

即使SCR.RE位被清除，SBER标志也不受影响，并且保持之前的状态。

30.2.40 MECR：曼彻斯特扩展错误控制寄存器

Base address: SCIn = 0x4011_8000 + 0x0100 × n (n = 3, 4)

Offset address: 0x25

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SBEREN	SYEREN	PFEREN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PFEREN	Preface Error Enable Specifies whether to handle a preface error as an interrupt source 0: Does not handle a preface error as an interrupt source 1: Handles a preface error as an interrupt source	R/W
1	SYEREN	Receive SYNC Error Enable Specifies whether to handle a receive SYNC error as an interrupt source 0: Does not handle a receive SYNC error as an interrupt source 1: Handles a receive SYNC error as an interrupt source	R/W
2	SBEREN	Start Bit Error Enable Specifies whether to handle a start bit error as an interrupt source 0: Does not handle a start bit error as an interrupt source 1: Handles a start bit error as an interrupt source	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R

Note: This register is valid only when the Manchester mode is enabled (MMR.MANEN = 1).

This register is used to specify whether to handle a preface error, receive SYNC error, or a start bit error as an interrupt source in Manchester mode. If those errors are handled as interrupt sources, interrupt requests and event requests are generated at the occurrence of each error, and the next reception is not performed until the corresponding error flag is cleared.

Please set this register when MMR.MANEN = ”0”. And do not change this register during communication.

PFEREN bit (Preface Error Enable)

This bit specifies whether to handle a preface error as an interrupt source.

When it is set to 0, a preface error is not handled as an interrupt source. When it is set to 1, a preface error is handled as an interrupt source.

SYEREN bit (Receive SYNC Error Enable)

This bit specifies whether to handle a receive SYNC error as an interrupt source.

When it is set to 0, a receive SYNC error is not handled as an interrupt source. When it is set to 1, a receive SYNC error is handled as an interrupt source.

SBEREN bit (Start Bit Error Enable)

This bit specifies whether to handle a start bit error as an interrupt source.

When it is set to 0, a start bit error is not handled as an interrupt source. When it is set to 1, a start bit error is handled as an interrupt source.

30.2.41 ESMER : Extended Serial Module Enable Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESME	Extended Serial Mode Enable 0: The extended serial mode is disabled. 1: The extended serial mode is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

ESME bit (Extended Serial Mode Enable)

When the ESME bit is 1, the facilities of the extended serial mode control section are enabled.

Bit	Symbol	Function	R/W
0	PFEREN	前言错误启用 指定是否将序言错误作为中断源处理 0：不将序言错误作为中断源处理1：将序言错误作为中断源处理	R/W
1	SYEREN	接收同步错误启用 指定是否将接收SYNC错误作为中断源处理 0：不将接收同步错误作为中断源处理1：将接收同步错误作为中断源处理	R/W
2	SBEREN	启动位错误启用 指定是否将起始位错误作为中断源处理 0：不将起始位错误作为中断源处理1：将起始位错误作为中断源处理	R/W
7:3	—	这些位被读取为0。写入值应为0。	R

Note: 该寄存器仅在启用曼彻斯特模式（MMR.MANEN=1）时有效。

该寄存器用于指定在曼彻斯特模式下是否处理序言错误、接收同步错误或起始位错误作为中断源。如果将这些错误作为中断源处理，则在每个错误发生时都会产生中断请求和事件请求，并且在相应的错误标志被清除之前不会执行下一次接收。

请在MMR.MANEN=“0”时设置该寄存器。并且不要在通信过程中更改该寄存器。

PFEREN位（前言错误使能）

该位指定是否将序言错误作为中断源处理。

当它设置为0时，前言错误不作为中断源处理。当它设置为1时，前言错误作为中断源处理。

SYEREN位（接收同步错误使能）

该位指定是否将接收同步错误作为中断源处理。

当它设置为0时，接收SYNC错误不作为中断源处理。当它设置为1时，接收SYNC错误作为中断源处理。

SBEREN位（启动位错误启用）

该位指定是否将起始位错误作为中断源处理。

当它设置为0时，起始位错误不作为中断源处理。当它设置为1时，起始位错误作为中断源处理。

30.2.41 ESMER:扩展串行模块使能寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESME
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESME	扩展串行模式启用 0：禁用扩展串行模式。1：使能扩展串行模式。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

ESME位（扩展串行模式启用）

当ESME位为1时，启用扩展串行模式控制部分的功能。

When the ESME bit is 0, the extended serial mode control section is initialized.

Table 30.26 Settings of the ESME Bit and Timer Operation Mode

ESME Bit	Timer Mode	Break Field Low Width Determination Mode	Break Field Low Width Output Mode
0	Available*1	Not available	Not available
1	Available	Available	Available

Note 1. Operation is only possible with PCLK selected.

30.2.42 CR0 : Control Register 0

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x21

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	BRME	RXDSF	SFSF	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	SFSF	Start Frame Status Flag 0: Start Frame detection function is disabled. 1: Start Frame detection function is enabled.	R
2	RXDSF	RXDXn Input Status Flag 0: RXDXn input is enabled. 1: RXDXn input is disabled.	R
3	BRME	Bit Rate Measurement Enable 0: Measurement of bit rate is disabled. 1: Measurement of bit rate is enabled.	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

30.2.43 CR1 : Control Register 1

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PIBS[2:0]			PIBE	CF1DS[1:0]		CF0RE	BFE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFE	Break Field Enable 0: Break Field detection is disabled. 1: Break Field detection is enabled.	R/W
1	CF0RE	Control Field 0 Reception Enable 0: Reception of Control Field 0 is disabled. 1: Reception of Control Field 0 is enabled.	R/W
3:2	CF1DS[1:0]	Control Field 1 Data Register Select 0 0: Selects comparison with the value in PCF1DR. 0 1: Selects comparison with the value in SCF1DR. 1 0: Selects comparison with the values in PCF1DR and SCF1DR. 1 1: Setting prohibited.	R/W

当ESME位为0时，扩展串行模式控制部分被初始化。

Table 30.26 ESME位和定时器操作模式的设置

ESME钻头	定时器模式	断场低宽度测定模式	断场低宽度输出模式
0	Available*1	无法使用	无法使用
1	Available	Available	Available

注1.只有在选择PCLK时才能进行操作。

30.2.42 CR0：控制寄存器0

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x21

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	BRME	RXDSF	SFSF	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	SFSF	开始帧状态标志 0：禁止启动帧检测功能。1：启动帧检测功能使能。	R
2	RXDSF	RXDXn输入状态标志 0：RXDXn输入使能。1：RXDXn输入禁用。	R
3	BRME	比特率测量启用 0：禁止比特率测量。1：启用比特率测量。	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

30.2.43 CR1：控制寄存器1

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x22

Bit position:	7	6	5	4	3	2	1	0
Bit field:	PIBS[2:0]			PIBE	CF1DS[1:0]		CF0RE	BFE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFE	中断字段启用 0：中断场检测被禁用。1：使能断场检测。	R/W
1	CF0RE	控制字段0接收启用 0：禁止接收控制字段0。1：启用控制字段0的接收。	R/W
3:2	CF1DS[1:0]	控制字段1数据寄存器选择 00：选择与PCF1DR中的值进行比较。01：选择与SCF1DR中的值进行比较。10：选择与PCF1DR和SCF1DR中的值进行比较。11：禁止设置。	R/W

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Bit	Symbol	Function	R/W
4	PIBE	Priority Interrupt Bit Enable 0: The priority interrupt bit is disabled. 1: The priority interrupt bit is enabled.	R/W
7:5	PIBS[2:0]	Priority Interrupt Bit Select 0 0 0: 0th bit of Control Field 1 0 0 1: 1st bit of Control Field 1 0 1 0: 2nd bit of Control Field 1 0 1 1: 3rd bit of Control Field 1 1 0 0: 4th bit of Control Field 1 1 0 1: 5th bit of Control Field 1 1 1 0: 6th bit of Control Field 1 1 1 1: 7th bit of Control Field 1	R/W

30.2.44 CR2 : Control Register 2

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x23

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RTS[1:0]		BCCS[1:0]		—	DFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DFCS[2:0]	RXDXn Signal Digital Filter Clock Select 0 0 0: Filter is disabled. 0 0 1: Filter clock is SCI base clock*1 *2 0 1 0: Filter clock is PCLK/8 0 1 1: Filter clock is PCLK/16 1 0 0: Filter clock is PCLK/32 1 0 1: Filter clock is PCLK/64 1 1 0: Filter clock is PCLK/128 1 1 1: Setting prohibited	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	BCCS[1:0]	Bus Collision Detection Clock Select • When SEMR.BGDM = 0 or SEMR.BGDM = 1 and SMR.CKS[1:0] = a value other than 00b 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited • When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Setting prohibited 1 1: Setting prohibited	R/W
7:6	RTS[1:0]	RXDXn Reception Sampling Timing Select • When SCIn.SEMR.ABCS = 0 0 0: Rising edge of the 8th cycle of SCI base clock 0 1: Rising edge of the 10th cycle of SCI base clock 1 0: Rising edge of the 12th cycle of SCI base clock 1 1: Rising edge of the 14th cycle of SCI base clock • When SCIn.SEMR.ABCS = 1 0 0: Rising edge of the 4th cycle of SCI base clock 0 1: Rising edge of the 5th cycle of SCI base clock 1 0: Rising edge of the 6th cycle of SCI base clock 1 1: Rising edge of the 7th cycle of SCI base clock	R/W

Note: The period of the SCI base clock is 1/16 of a single bit period when the SCIn.SEMR.ABCS is 0, and 1/8 of a single bit period when the SCIn.SEMR.ABCS is 1.

Note 1. To use the SCI base clock, set the SCIn.SCR.TE bit to 1.

Bit	Symbol	Function	R/W
4	PIBE	优先中断位使能 0：禁止优先中断位。1：优先中断位使能。	R/W
7:5	PIBS[2:0]	优先中断位选择 000：控制字段1的第0位001：控制字段1的第1位010：控制字段1的第2位011：控制字段1的第3位100：控制字段1的第4位101：控制字段1的第5位110：控制字段1的第6位111：控制字段1的第7位	R/W

30.2.44 CR2：控制寄存器2

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x23

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RTS[1:0]		BCCS[1:0]		—	DFCS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	DFCS[2:0]	RXDXn信号数字滤波器时钟选择 000：过滤器被禁用。001：滤波器时钟为SCI基本时钟*1*2 010：滤波器时钟为PCLK8011：滤波器时钟为PCLK16100：滤波器时钟为PCLK32101：滤波器时钟为PCLK64110：滤波器时钟为PCLK128111：设置禁止	R/W
3	—	该位读取为0。写入值应为0。	R/W
5:4	BCCS[1:0]	总线冲突检测时钟选择● 当SEMR.BGDM=0或SEMR.BGDM=1且SMR.CKS[1:0]=00b以外的值时 00：SCI基准时钟01：SCI基准时钟频率除以210：SCI基准时钟频率除以411：禁止设置 • 当SEMR.BGDM=1且SMR.CKS[1:0]=00b00：SCI基本时钟频率除以201：SCI基本时钟频率除以410：禁止设置11：禁止设置	R/W
7:6	RTS[1:0]	RXDXn接收采样时序选择● 00：SCI基准时钟第8周期上升沿01：SCI基准时钟第10周期上升沿10：SCI基准时钟第12周期上升沿11：SCI第14周期上升沿基准时钟 • 当SCIn.SEMR.ABCS=100：SCI基准时钟第4周期上升沿01：SCI基准时钟1第5周期上升沿0：SCI基准时钟1第6周期上升沿1：SCI基本时钟第7个周期的上升沿	R/W

Note: 当SCIn.SEMR.ABCS为0时，SCI基本时钟的周期为单位周期的116，而当SCIn.SEMR.ABCS为1时，SCI基准时钟的周期为单位周期的18。

注1.要使用SCI基本时钟，请将SCIn.SCR.TE位设置为1。

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Note 2. The SCI base clock divided by 2 is the filter clock when the SEMR.BGDM bit is 1 and the SMR.CKS[1:0] bits are 00b.

30.2.45 CR3 : Control Register 3

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SDST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SDST	Start Frame Detection Start 0: Detection of Start Frame is not performed. 1: Detection of Start Frame is performed.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

SDST bit (Start Frame Detection Start)

Detection of a Start Frame begins when this bit is set to 1. The bit is read as 0.

30.2.46 PCR : Port Control Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x25

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SHARPS	—	—	RXDXPS	TXDXPS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXDXPS	TXDXn Signal Polarity Select 0: The polarity of TXDXn signal is not inverted for output. 1: The polarity of TXDXn signal is inverted for output.	R/W
1	RXDXPS	RXDXn Signal Polarity Select 0: The polarity of RXDXn signal is not inverted for input. 1: The polarity of RXDXn signal is inverted for input.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SHARPS	TXDXn/RXDXn Pin Multiplexing Select 0: The TXDXn and RXDXn pins are independent. 1: The TXDXn and RXDXn signals are multiplexed on the same pin.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

SHARPS bit (TXDXn/RXDXn Pin Multiplexing Select)

When this bit is set to 1, the TXDXn and RXDXn signals are multiplexed on the same pin so that half-duplex communications become possible.

注2.当SEMR.BGDM位为1且SMR.CKS[1:0]位为00b时，SCI基本时钟除以2为滤波器时钟。

30.2.45 CR3：控制寄存器3

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x24

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SDST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SDST	开始帧检测开始 0：不检测起始帧。1：执行起始帧检测。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

SDST位（开始帧检测开始）

当该位设置为1时开始检测起始帧。该位被读取为0。

30.2.46 PCR：端口控制寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x25

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SHARPS	—	—	RXDXPS	TXDXPS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXDXPS	TXDXn信号极性选择 0：TXDXn信号的极性不反相输出。1：TXDXn信号极性反转输出。	R/W
1	RXDXPS	RXDXn信号极性选择 0：RXDXn信号极性不反相输入。1：RXDXn信号极性反相输入。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	SHARPS	TXDXnRXDXn引脚复用选择 0：TXDXn和RXDXn引脚独立。1：TXDXn和RXDXn信号在同一个引脚上复用。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

SHARPS位（TXDXnRXDXn引脚复用选择）

当该位设置为1时，TXDXn和RXDXn信号在同一引脚上复用，从而可以进行半双工通信。

30.2.47 ICR : Interrupt Control Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x26

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	AEDIE	BCDIE	PIBDIE	CF1MIE	CF0MIE	BFDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFDIE	Break Field Low Width Detected Interrupt Enable 0: Interrupts on detection of the low width for a Break Field are disabled. 1: Interrupts on detection of the low width for a Break Field are enabled.	R/W
1	CF0MIE	Control Field 0 Match Detected Interrupt Enable 0: Interrupts on detection of a match with Control Field 0 are disabled. 1: Interrupts on detection of a match with Control Field 0 are enabled.	R/W
2	CF1MIE	Control Field 1 Match Detected Interrupt Enable 0: Interrupts on detection of a match with Control Field 1 are disabled. 1: Interrupts on detection of a match with Control Field 1 are enabled.	R/W
3	PIBDIE	Priority Interrupt Bit Detected Interrupt Enable 0: Interrupts on detection of the priority interrupt bit are disabled. 1: Interrupts on detection of the priority interrupt bit are enabled.	R/W
4	BCDIE	Bus Collision Detected Interrupt Enable 0: Interrupts on detection of a bus collision are disabled. 1: Interrupts on detection of a bus collision are enabled.	R/W
5	AEDIE	Valid Edge Detected Interrupt Enable 0: Interrupts on detection of a valid edge are disabled. 1: Interrupts on detection of a valid edge are enabled.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

30.2.48 STR : Status Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x27

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	AEDF	BCDF	PIBDF	CF1MF	CF0MF	BFDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFDF	Break Field Low Width Detection Flag [Setting conditions] ● Detection of the low width for a Break Field ● Completion of the output of the low width for a Break Field ● Underflow of the timer [Clearing condition] ● Writing 1 to the BFDCL bit in STCR	R
1	CF0MF	Control Field 0 Match Flag [Setting conditions] ● A match between the value received in Control Field 0 and the set value. [Clearing condition] ● Writing 1 to the CF0MCL bit in STCR	R

30.2.47 ICR：中断控制寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x26

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	AEDIE	BCDIE	PIBDIE	CF1MIE	CF0MIE	BFDIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFDIE	中断字段低宽度检测到中断使能 0：禁止检测到中断字段的低宽度时的中断。1：允许检测到中断字段的低宽度时的中断。	R/W
1	CF0MIE	控制字段0匹配检测到中断使能 0：检测到与控制字段0匹配时的中断被禁用。1：检测到与控制字段0匹配时的中断使能。	R/W
2	CF1MIE	控制字段1匹配检测到中断使能 0：检测到与控制字段1匹配时的中断被禁用。1：检测到与控制字段1匹配时的中断使能。	R/W
3	PIBDIE	优先中断位检测到中断使能 0：禁止检测到优先中断位时的中断。1：检测到优先中断位时的中断使能。	R/W
4	BCDIE	总线冲突检测中断使能 0：禁止检测到总线冲突时的中断。1：使能检测到总线冲突时的中断。	R/W
5	AEDIE	有效边沿检测中断使能 0：禁止检测到有效边沿时的中断。1：使能检测到有效边沿时的中断。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

30.2.48 STR:状态寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x27

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	AEDF	BCDF	PIBDF	CF1MF	CF0MF	BFDF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFDF	中断字段低宽度检测标志[设置条件]● 检测中断字段的低宽度 ● 完成中断字段的低宽度输出 ●定时器下溢[清除条件]● 将1写入STCR中的BFDCL位	R
1	CF0MF	控制字段0匹配标志[设置条件]● 控制字段0中接收的值与设定值之间的匹配。[结算条件]● 将1写入STCR中的CF0MCL位	R

Bit	Symbol	Function	R/W
2	CF1MF	Control Field 1 Match Flag [Setting conditions] ● A match between the data received in Control Field 1 and the set values. [Clearing condition] ● Writing 1 to the CF1MCL bit in STCR	R
3	PIBDF	Priority Interrupt Bit Detection Flag [Setting conditions] ● Detection of the priority interrupt bit [Clearing condition] ● Writing 1 to the PIBDCL bit in STCR	R
4	BCDF	Bus Collision Detected Flag [Setting conditions] ● Detection of the bus collision [Clearing condition] ● Writing 1 to the BCDCL bit in STCR	R
5	AEDF	Valid Edge Detection Flag [Setting conditions] ● Detection of a valid edge [Clearing condition] ● Writing 1 to the AEDCL bit in STCR	R
7:6	—	These bits are read as 0. The write value should be 0.	R

30.2.49 STCR : Status Clear Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	AEDCL	BCDCL	PIBDCL	CF1MCL	CF0MCL	BFDCL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFDCL	BFDF Clear Setting this bit to 1 clears the STR.BFDF flag. This bit is read as 0.	R/W
1	CF0MCL	CF0MF Clear Setting this bit to 1 clears the STR.CF0MF flag. This bit is read as 0.	R/W
2	CF1MCL	CF1MF Clear Setting this bit to 1 clears the STR.CF1MF flag. This bit is read as 0.	R/W
3	PIBDCL	PIBDF Clear Setting this bit to 1 clears the STR.PIBDF flag. This bit is read as 0.	R/W
4	BCDCL	BCDF Clear Setting this bit to 1 clears the STR.BCDF flag. This bit is read as 0.	R/W
5	AEDCL	AEDF Clear Setting this bit to 1 clears the STR.AEDF flag. This bit is read as 0.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

30.2.50 CF0DR : Control Field 0 Data Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x29

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2	CF1MF	控制字段1匹配标志[设置条件]● 控制字段1中接收的数据与设定值之间的匹配。[结算条件]● 将1写入STCR中的CF1MCL位	R
3	PIBDF	优先中断位检测标志[设置条件]● 检测优先中断位[清除条件]● 将1写入STCR中的PIBDCL位	R
4	BCDF	BusCollisionDetectedFlag[设定条件]● 总线碰撞检测[清除条件]● 将1写入STCR中的BCDCL位	R
5	AEDF	有效边缘检测标志[设置条件]● 检测有效边沿[清除条件]● 将1写入STCR的AEDCL位	R
7:6	—	这些位被读取为0。写入值应为0。	R

30.2.49 STCR:状态清除寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	AEDCL	BCDCL	PIBDCL	CF1MCL	CF0MCL	BFDCL
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BFDCL	BFDF Clear 将此位设置为1会清除STR.BFDF标志。该位读为0。	R/W
1	CF0MCL	CF0MF Clear 将此位设置为1会清除STR.CF0MF标志。该位读为0。	R/W
2	CF1MCL	CF1MF Clear 将此位设置为1会清除STR.CF1MF标志。该位读为0。	R/W
3	PIBDCL	PIBDF Clear 将此位设置为1会清除STR.PIBDF标志。该位读为0。	R/W
4	BCDCL	BCDF Clear 将此位设置为1会清除STR.BCDF标志。该位读为0。	R/W
5	AEDCL	AEDF Clear 将此位设置为1会清除STR.AEDF标志。该位读为0。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

30.2.50 CF0DR：控制字段0数据寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x29

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

The CF0DR register is an 8-bit readable and writable register that holds a value for comparison with Control Field 0.

30.2.51 CF0CR : Control Field 0 Compare Enable Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CF0CE7	CF0CE6	CF0CE5	CF0CE4	CF0CE3	CF0CE2	CF0CE1	CF0CE0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CF0CE0	Control Field 0 Bit 0 Compare Enable 0: Comparison with bit 0 of Control Field 0 is disabled. 1: Comparison with bit 0 of Control Field 0 is enabled.	R/W
1	CF0CE1	Control Field 1 Bit 0 Compare Enable 0: Comparison with bit 1 of Control Field 0 is disabled. 1: Comparison with bit 1 of Control Field 0 is enabled.	R/W
2	CF0CE2	Control Field 2 Bit 0 Compare Enable 0: Comparison with bit 2 of Control Field 0 is disabled. 1: Comparison with bit 2 of Control Field 0 is enabled.	R/W
3	CF0CE3	Control Field 3 Bit 0 Compare Enable 0: Comparison with bit 3 of Control Field 0 is disabled. 1: Comparison with bit 3 of Control Field 0 is enabled.	R/W
4	CF0CE4	Control Field 4 Bit 0 Compare Enable 0: Comparison with bit 4 of Control Field 0 is disabled. 1: Comparison with bit 4 of Control Field 0 is enabled.	R/W
5	CF0CE5	Control Field 5 Bit 0 Compare Enable 0: Comparison with bit 5 of Control Field 0 is disabled. 1: Comparison with bit 5 of Control Field 0 is enabled.	R/W
6	CF0CE6	Control Field 6 Bit 0 Compare Enable 0: Comparison with bit 6 of Control Field 0 is disabled. 1: Comparison with bit 6 of Control Field 0 is enabled.	R/W
7	CF0CE7	Control Field 7 Bit 0 Compare Enable 0: Comparison with bit 7 of Control Field 0 is disabled. 1: Comparison with bit 7 of Control Field 0 is enabled.	R/W

30.2.52 CF0RR : Control Field 0 Receive Data Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2B

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

CF0RR is a readable register that holds the value received in Control Field 0.

CF0DR寄存器是一个8位可读写寄存器，它保存一个用于与控制字段0进行比较的值。

30.2.51 CF0CR：控制字段0比较使能寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CF0CE7	CF0CE6	CF0CE5	CF0CE4	CF0CE3	CF0CE2	CF0CE1	CF0CE0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CF0CE0	控制字段0位0比较使能 0：禁止与控制字段0的位0进行比较。1：启用与控制字段0的位0的比较。	R/W
1	CF0CE1	控制字段1位0比较使能 0：禁止与控制字段0的位1进行比较。1：启用与控制字段0的位1的比较。	R/W
2	CF0CE2	控制字段2位0比较使能 0：禁止与控制字段0的位2进行比较。1：启用与控制字段0的位2的比较。	R/W
3	CF0CE3	控制字段3位0比较使能 0：禁止与控制字段0的位3比较。1：启用与控制字段0的位3的比较。	R/W
4	CF0CE4	控制字段4位0比较使能 0：禁止与控制字段0的位4进行比较。1：启用与控制字段0的位4的比较。	R/W
5	CF0CE5	控制字段5位0比较使能 0：禁止与控制字段0的位5进行比较。1：启用与控制字段0的位5的比较。	R/W
6	CF0CE6	控制字段6位0比较使能 0：禁止与控制字段0的位6进行比较。1：启用与控制字段0的位6的比较。	R/W
7	CF0CE7	控制字段7位0比较使能 0：禁止与控制字段0的位7进行比较。1：启用与控制字段0的第7位比较。	R/W

30.2.52 CF0RR:控制字段0接收数据寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2B

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	0	0	0	0	0	0	0	0

CF0RR是一个可读寄存器，它保存在控制字段0中接收到的值。

30.2.53 PCF1DR : Primary Control Field 1 Data Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

PCF1DR is an 8-bit readable and writable register that holds the 8-bit primary value for comparison with Control Field 1.

30.2.54 SCF1DR : Secondary Control Field 1 Data Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2D

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

SCF1DR is an 8-bit readable and writable register that holds the 8-bit secondary value for comparison with Control Field 1.

30.2.55 CF1CR : Control Field 1 Compare Enable Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CF1CE7	CF1CE6	CF1CE5	CF1CE4	CF1CE3	CF1CE2	CF1CE1	CF1CE0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CF1CE0	Control Field 1 Bit 0 Compare Enable 0: Comparison with bit 0 of Control Field 1 is disabled. 1: Comparison with bit 0 of Control Field 1 is enabled.	R/W
1	CF1CE1	Control Field 1 Bit 1 Compare Enable 0: Comparison with bit 1 of Control Field 1 is disabled. 1: Comparison with bit 1 of Control Field 1 is enabled.	R/W
2	CF1CE2	Control Field 1 Bit 2 Compare Enable 0: Comparison with bit 2 of Control Field 1 is disabled. 1: Comparison with bit 2 of Control Field 1 is enabled.	R/W
3	CF1CE3	Control Field 1 Bit 3 Compare Enable 0: Comparison with bit 3 of Control Field 1 is disabled. 1: Comparison with bit 3 of Control Field 1 is enabled.	R/W
4	CF1CE4	Control Field 1 Bit 4 Compare Enable 0: Comparison with bit 4 of Control Field 1 is disabled. 1: Comparison with bit 4 of Control Field 1 is enabled.	R/W
5	CF1CE5	Control Field 1 Bit 5 Compare Enable 0: Comparison with bit 5 of Control Field 1 is disabled. 1: Comparison with bit 5 of Control Field 1 is enabled.	R/W
6	CF1CE6	Control Field 1 Bit 6 Compare Enable 0: Comparison with bit 6 of Control Field 1 is disabled. 1: Comparison with bit 6 of Control Field 1 is enabled.	R/W

30.2.53 PCF1DR：主控制字段1数据寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2C

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	0	0	0	0	0	0	0	0

PCF1DR是一个8位可读写寄存器，它保存8位主值，用于与控制字段1进行比较。

30.2.54 SCF1DR：辅助控制字段1数据寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2D

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	0	0	0	0	0	0	0	0

SCF1DR是一个8位可读写寄存器，保存8位辅助值，用于与控制字段1进行比较。

30.2.55 CF1CR：控制字段1比较使能寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CF1CE7	CF1CE6	CF1CE5	CF1CE4	CF1CE3	CF1CE2	CF1CE1	CF1CE0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CF1CE0	控制字段1位0比较使能 0：禁止与控制字段1的位0进行比较。1：启用与控制字段1的位0的比较。	R/W
1	CF1CE1	控制字段1位1比较使能 0：禁止与控制字段1的位1比较。1：启用与控制字段1的位1的比较。	R/W
2	CF1CE2	控制字段1位2比较使能 0：禁止与控制字段1的位2进行比较。1：启用与控制字段1的位2的比较。	R/W
3	CF1CE3	控制字段1位3比较使能 0：禁止与控制字段1的位3比较。1：启用与控制字段1的位3的比较。	R/W
4	CF1CE4	控制字段1位4比较使能 0：禁止与控制字段1的位4比较。1：启用与控制字段1的位4的比较。	R/W
5	CF1CE5	控制字段1位5比较使能 0：禁止与控制字段1的位5进行比较。1：启用与控制字段1的位5的比较。	R/W
6	CF1CE6	控制字段1位6比较使能 0：禁止与控制字段1的位6进行比较。1：启用与控制字段1的位6的比较。	R/W

Bit	Symbol	Function	R/W
7	CF1CE7	Control Field 1 Bit 7 Compare Enable 0: Comparison with bit 7 of Control Field 1 is disabled. 1: Comparison with bit 7 of Control Field 1 is enabled.	R/W

30.2.56 CF1RR : Control Field 1 Receive Data Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2F

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

CF1RR is a readable register that holds the value received in Control Field 1.

30.2.57 TCR : Timer Control Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x30

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCST	Timer Count Start 0: Stops the timer counting 1: Starts the timer counting	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

30.2.58 TMR : Timer Mode Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x31

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCSS[2:0]			TWRC	—	TOMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TOMS[1:0]	Timer Operating Mode Select*1 0 0: Timer mode 0 1: Break Field low width determination mode 1 0: Break Field low width output mode 1 1: Setting prohibited	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	TWRC	Counter Write Control 0: Data is written to the reload register and counter 1: Data is written to the reload register only	R/W

Bit	Symbol	Function	R/W
7	CF1CE7	控制字段1位7比较使能 0：禁止与控制字段1的位7进行比较。1：启用与控制字段1的第7位比较。	R/W

30.2.56 CF1RR:控制字段1接收数据寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x2F

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

CF1RR是一个可读寄存器，它保存在控制字段1中接收到的值。

30.2.57 TCR：定时器控制寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x30

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TCST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TCST	定时器计数开始 0：停止定时器计数1：开始定时器计数	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

30.2.58 TMR:定时器模式寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x31

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	TCSS[2:0]			TWRC	—	TOMS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	TOMS[1:0]	定时器工作模式选择*1 00：定时器模式01：BreakField低宽度确定模式 10：BreakField低宽度输出模式11：禁止设置	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	TWRC	计数器写控制 0：数据写入重载寄存器和计数器1：数据仅写入重载寄存器	R/W

Bit	Symbol	Function	R/W
6:4	TCSS[2:0]	Timer Count Clock Source Select*1 0 0 0: PCLK 0 0 1: PCLK/2 0 1 0: PCLK/4 0 1 1: PCLK/8 1 0 0: PCLK/16 1 0 1: PCLK/32 1 1 0: PCLK/64 1 1 1: PCLK/128	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Rewrite the TOMS[1:0] and TCSS[2:0] bits only when the timer is stopped (TCST = 0).

TWRC bit (Counter Write Control)

This bit determines whether a value written to TPRE or TCNT is written to the reload register only or is written to both the reload register and the counter.

30.2.59 TPRE : Timer Prescaler Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x32

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

TPRE consists of an 8-bit reload register, a read buffer, and a counter, each of which has FFh as its initial value. The counter counts down in synchronization with the counter clock selected by the TMR.TCSS[2:0] bits, and is reloaded with the value in the reload register when it underflows. Underflows of this register provide the clock source to drive counting by the TCNT register. The reload register and read buffer are allocated to the same address. Data is written to the reload register in writing, and the counter value that has been transferred to the read buffer is returned in reading.

It takes one PCLK cycle to load a value from the reload register to the counter.

30.2.60 TCNT : Timer Count Register

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x33

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

TCNT consists of an 8-bit reload register, a read buffer, and a counter, each of which has FFh as its initial value. This down-counter counts underflows of the TPRE register until the TCNT register underflows, and is then reloaded with the value from the reload register. The reload register and read buffer are allocated to the same address. Data is written to the reload register in writing, and the counter value that has been transferred to the read buffer is returned in reading.

It takes one PCLK cycle to load a value from the reload register to the counter.

30.3 Operation in Asynchronous Mode

Figure 30.6 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit or receive data, a parity bit, and stop bits (high level). In asynchronous serial communications, the communications line is usually held in the mark state (high level).

Bit	Symbol	Function	R/W
6:4	TCSS[2:0]	定时器计数时钟源选择*1 0 0 0: PCLK 0 0 1: PCLK/2 0 1 0: PCLK/4 0 1 1: PCLK/8 1 0 0: PCLK/16 1 0 1: PCLK/32 1 1 0: PCLK/64 1 1 1: PCLK/128	R/W
7	—	该位读取为0。写入值应为0。	R/W

注1.仅当定时器停止(TCST=0)时才重写TOMS[1:0]和TCSS[2:0]位。

TWRC位（计数器写控制）

该位确定写入TPRE或TCNT的值是仅写入重载寄存器还是同时写入重载寄存器和计数器。

30.2.59 TPRE：定时器预分频寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x32

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

TPRE由一个8位重载寄存器、一个读缓冲区和一个计数器组成，每个计数器的初始值都为FFh。计数器与TMR.TCSS[2:0]位选择的计数器时钟同步递减计数，并在下溢时重新加载重载寄存器中的值。该寄存器的下溢提供时钟源来驱动TCNT寄存器的计数。重载寄存器和读缓冲区被分配到同一个地址。写入时数据被写入重载寄存器，读取时返回已传送到读缓冲区的计数器值。

将一个值从重载寄存器加载到计数器需要一个PCLK周期。

30.2.60 TCNT：定时器计数寄存器

Base address: SCIm = 0x4011_8000 + 0x0100 × m (m = 1, 2)

Offset address: 0x33

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

TCNT由一个8位重载寄存器、一个读缓冲区和一个计数器组成，每个计数器的初始值都为FFh。该递减计数器对TPRE寄存器的下溢进行计数，直到TCNT寄存器下溢，然后用重新加载寄存器中的值重新加载。重载寄存器和读缓冲区被分配到同一个地址。写入时数据被写入重载寄存器，读取时返回已传送到读缓冲区的计数器值。

将一个值从重载寄存器加载到计数器需要一个PCLK周期。

30.3 异步模式下的操作

图30.6显示了异步串行通信的一般格式。一帧由起始位（低电平）、发送或接收数据、奇偶校验位和停止位（高电平）组成。在异步串行通信中，通信线路通常保持在标记状态（高电平）。

The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

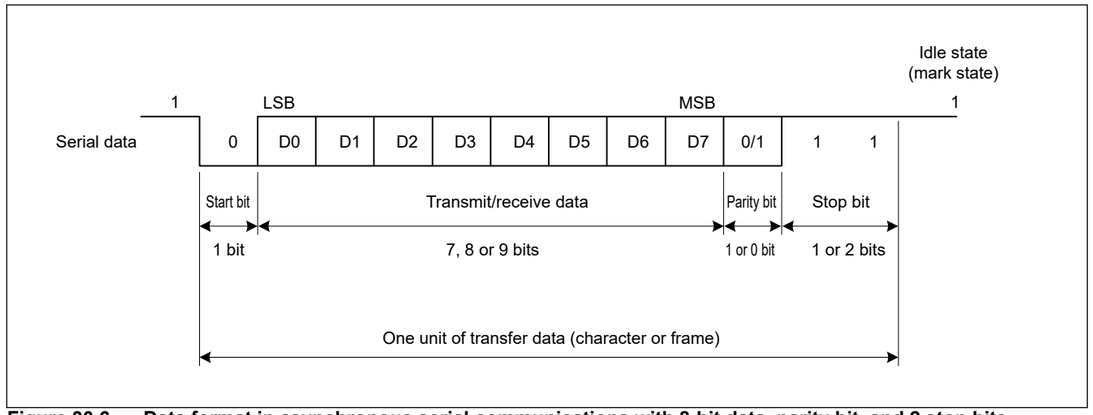

Figure 30.6 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

30.3.1 Serial Data Transfer Format

Table 30.27 lists the serial data transfer formats that can be used in asynchronous mode. Any of 18 transfer formats can be selected with the SMR and SCMR settings. For details on the multi-processor function, see section 30.4. Multi-Processor Communication Function.

Table 30.27 Serial transfer formats in asynchronous mode (1 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP

SCI监控通信线路。当SCI检测到低电平时，将其视为起始位并开始串行通信。

在SCI内部，发射器和接收器是独立的单元，可实现全双工通信。发送器和接收器除了FIFO模式外，都具有双缓冲结构，从而可以在发送或接收过程中读取或写入数据，从而实现数据的连续发送和接收。

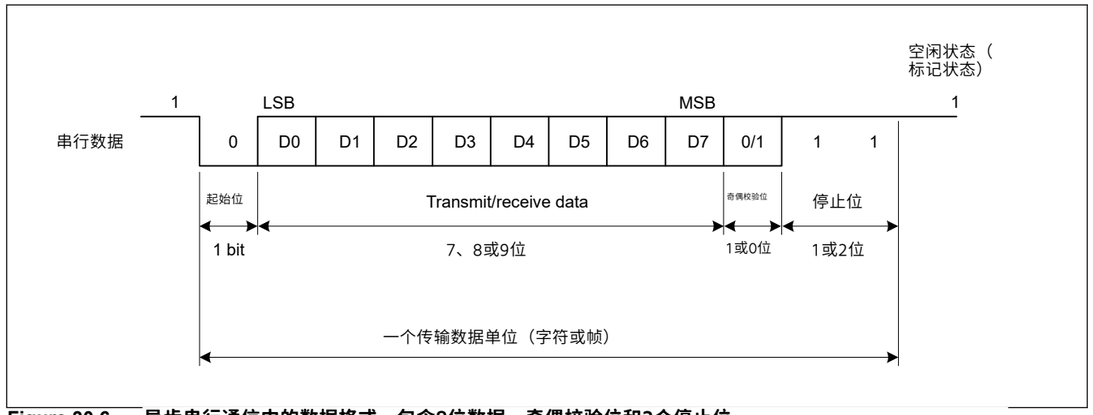

Figure 30.6 异步串行通信中的数据格式，包含8位数据、奇偶校验位和2个停止位

30.3.1 串行数据传输格式

表30.27列出了可以在异步模式下使用的串行数据传输格式。可以使用SMR和SCMR设置选择18种传输格式中的任何一种。有关多处理器功能的详细信息，请参阅第30.4节。多处理器通信功能。

Table 30.27 异步模式下的串行传输格式（1of2）

SCMR setting	SMR setting				串行传输格式和帧长
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	ST 9-bit data SP
0	0	0	0	1	ST 9-bit data SP SP
0	0	1	0	0	ST 9-bit data P SP
0	0	1	0	1	ST 9-bit data P SP SP
1	0	0	0	0	ST 8-bit data SP
1	0	0	0	1	ST 8-bit data SP SP
1	0	1	0	0	ST 8-bit data P SP
1	0	1	0	1	ST 8-bit data P SP SP
1	1	0	0	0	ST 7-bit data SP

Table 30.27 Serial transfer formats in asynchronous mode (2 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: Start bit
SP: Stop bit
P: Parity bit
MPB: Multi-processor bit

30.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs internal synchronization.*2

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit (when sampling timing does not adjust (SPTR.ASEN = 0)), as shown in Figure 30.7 The reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

Note: M: Reception margin
N: Ratio of bit rate to clock
(N = 16 when SEMR.ABCSE = 0 and SEMR.ABCS = 0,
N = 8 when SEMR.ABCS = 1,
N = 6 when SEMR.ABCSE = 1)
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined using the following formula:
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

This represents the computed value. Renesas recommends a margin of 20% to 30% in system design.

Table 30.27 异步模式下的串行传输格式(2of2)

SCMR setting	SMR setting				串行传输格式和帧长
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
1	1	0	0	1	ST 7-bit data SP SP
1	1	1	0	0	ST 7-bit data P SP
1	1	1	0	1	ST 7-bit data P SP SP
0	0	—	1	0	ST 9-bit data MPB SP
0	0	—	1	1	ST 9-bit data MPB SP SP
1	0	—	1	0	ST 8-bit data MPB SP
1	0	—	1	1	ST 8-bit data MPB SP SP
1	1	—	1	0	ST 7-bit data MPB SP
1	1	—	1	1	ST 7-bit data MPB SP SP

ST: 起始位停
SP: 止位奇偶
P: 校验位
MPB: Multi-processor bit

30.3.2 异步模式下接收数据采样时序和接收余量

在异步模式下，SCI在频率为16倍*1比特率的基本时钟上运行。

在接收时，SCI使用基本时钟对起始位的下降沿进行采样，并执行内部同步。*2

由于接收数据在基本时钟的第8个脉冲*1的上升沿进行采样，因此数据在每个位的中间锁存（当采样时序不调整时(SPTR.ASEN=0)），如图30.7所示异步模式下的接收余量由以下公式（1）确定：

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%] \quad \ldots \quad \text{Formula (1)}$$

Note: M：接收余量
N：比特率与时钟的比率
（当SEMR.ABCSE=0和SEMR.ABCS=0时，N=16，
N = 8 when SEMR.ABCS = 1,
N = 6 when SEMR.ABCSE = 1)
D:时钟占空比(D=0.5to1.0)
L：帧长（L=9到13）
F：时钟频率偏差的绝对值

假设公式（1）中的F=0和D=0.5的值，接收裕量使用以下公式确定：
$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\ \%$

这表示计算值。瑞萨建议在系统设计中留出20%到30%的余量。

Note 1. In this example, the SEMR.ABCS bit is 0 and the SEMR.ABCSE is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.

When the ABCSE bit is 1, a sextuple frequency of a bit rate is used as a base clock, and receive data is sampled on the rising edge of the 3rd pulse of the base clock.

Note 2. The determination condition of the start bit is as follows.

The function of adjust sampling timing is OFF (ASEN = 0):

The determination condition of a start bit is that Low beyond half bit length continues. It is same as the sampling timing. In Figure 30.7, Low period should be kept over 8-cycles to detect a start bit. If Low period does not keep over 8-cycles, the IP judges this as a noise. So, the IP does not start reception and wait start bit.

The function of adjust samplint timing is ON (ASEN = 1):

The determination condition of a start bit is that Low keeps up until the sampling timing. Adjusting the sampling timing forward (AJD = 1) increases the possibility of erroneously determin-ing a noise as the start bit.

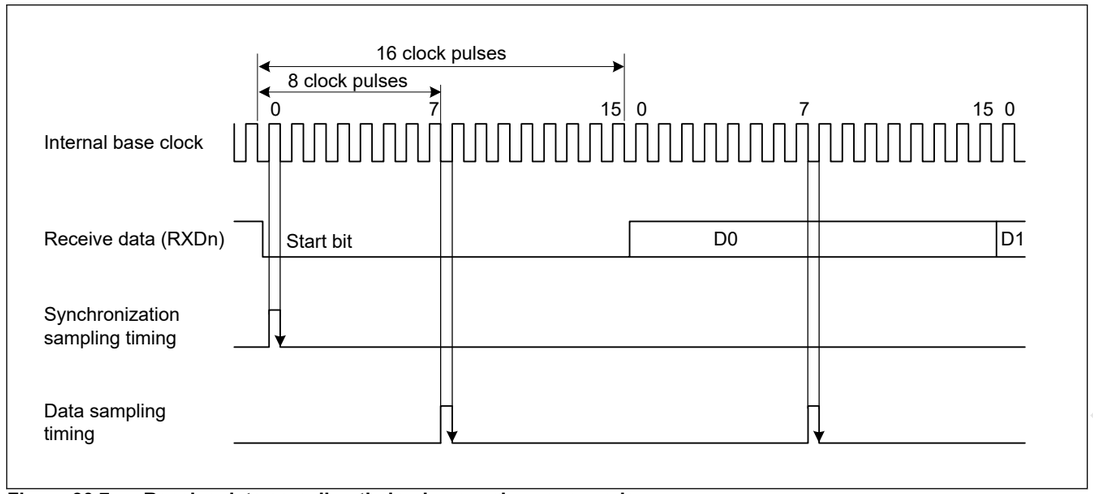

Figure 30.7 Receive data sampling timing in asynchronous mode

30.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the transfer clock of the SCI, based on the SMR.CM and SCR.CKE[1:0] settings.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when SEMR.ABCS = 0) or 8 times the bit rate (when SEMR.ABCS = 1).

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is configured so that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 30.8.

When clock output is enabled, the clock is output after setting the SCR.TE or SCR.RE bit to 1.

注1.本例中，SEMR.ABCS位为0，SEMR.ABCSE位为0。当ABCS位为1，ABCSE位为0时，使用8倍比特率的频率作为基准时钟，并在基本时钟的第4个脉冲的上升沿对接收数据进行采样。

当ABCSE位为1时，以比特率的六倍频为基准时钟，在基准时钟的第3个脉冲的上升沿对接收数据进行采样。

注2.起始位的判断条件如下。

调整采样定时功能关闭（ASEN=0）：

起始位的确定条件是超过半位长度的Low继续。与采样时间相同。在图30.7中，低电平周期应保持超过8个周期以检测起始位。如果Low周期未保持超过8个周期，则IP将其判断为噪声。因此，IP不开始接收并等待开始位。

调整采样定时功能开启（ASEN=1）：

起始位的确定条件是Low一直保持到采样定时。向前调整采样时序(AJD=1)会增加错误地将噪声确定为起始位的可能性。

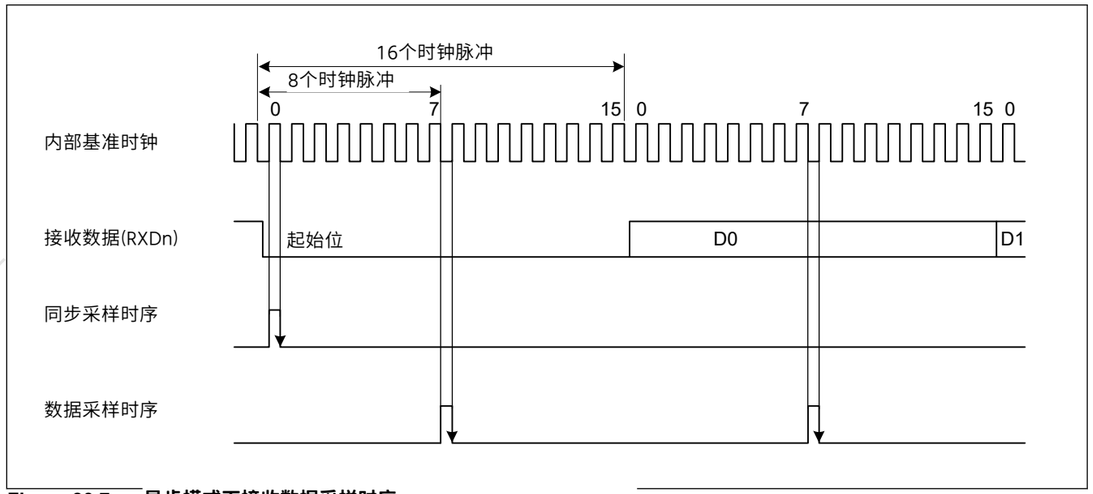

Figure 30.7 异步模式下接收数据采样时序

30.3.3 Clock

根据SMR.CM和SCR.CKE[1:0]设置，可以选择片内波特率发生器产生的内部时钟或输入到SCKn引脚的外部时钟作为SCI的传输时钟。

当外部时钟输入到SCKn引脚时，时钟频率必须为比特率的16倍（SEMR.ABCS=0时）或比特率的8倍（SEMR.ABCS=1时）。

当SCI使用其内部时钟时，时钟可以从SCKn引脚输出。在这种情况下，时钟输出的频率等于比特率，并配置相位，使时钟的上升沿在传输数据的中间，如图30.8所示。

时钟输出使能时，将SCR.TE或SCR.RE位设置为1后输出时钟。

RA生态工作室

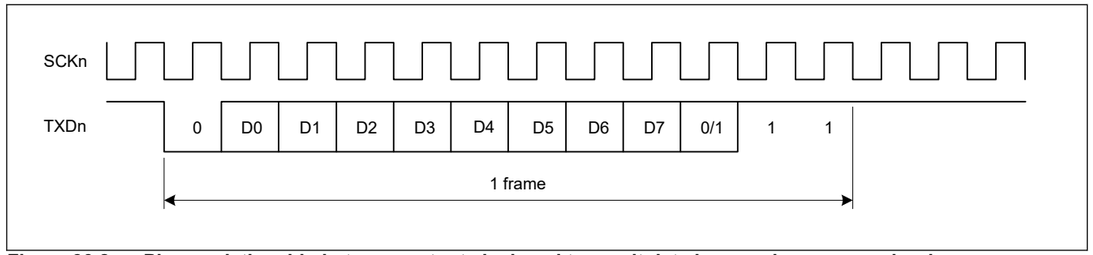

Figure 30.8 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, and STOP = 1

30.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the SEMR.ABCS bit is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0. When the SEMR.BGDM bit is set to 1, the cycle of the base clock is half and the bit rate is double that of when BGDM is set to 0. When the SCR.CKE[1] bit is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate at a bit rate four times that when the ABCS and BGDM bits are set to 0.

When the SEMR.ABCSE bit is set to 1, the number of base clock pulses is 6 during a period of 1 bit, and the SCI operates at a bit rate 16/3 times that when SEMR.ABCS = 0, SEMR.BGDM = 0, and SEMR.ABCSE = 0.

As shown by Formula (1) in section 30.3.2. Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the SEMR.ABCS or SEMR.ABCSE bit is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

30.3.5 CTS and RTS Functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. For the functions of CTS and RTS, you can select the alternate setting that uses either function with one terminal and the dedicated setting that uses each function independently with two terminals. This setting is done with the SPMR.CTSPEN bit.

When the CTS function is enabled, placing a low level on the CTSn_RTSn pin causes transmission to start.

Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function, which uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for output of the low and high levels are shown in this section.

[Conditions for low level output]

Satisfaction of all conditions are listed in this section.

Non-FIFO selected

- The value of the SCR.RE bit is 1
- Reception is not in progress
- There is no received data yet to be read
- The ORER, FER, and PER flags in the SSR register are all 0

FIFO selected

- The value of the SCR.RE bit is 1
- The amount of receive data written in FRDRHL is equal to or less than the setting value of FCRH.RSTRG[3:0]
- The ORER flag in the SSR_FIFO register (ORER in FRDRH) is 0

[Condition for high level output]

- The conditions for low-level output are not satisfied

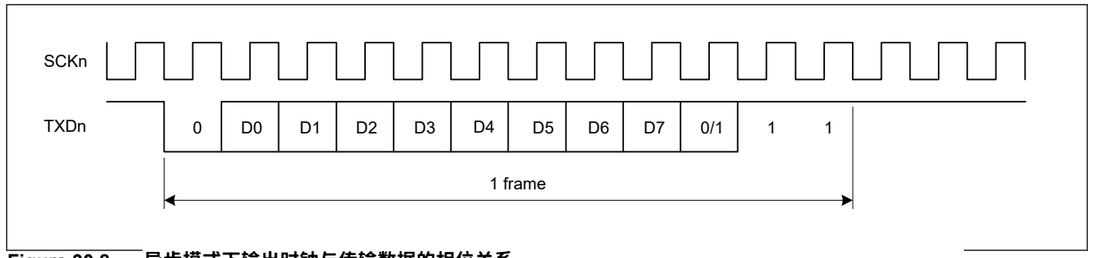

Figure 30.8 异步模式下输出时钟与传输数据的相位关系 SMR.CHR=0，PE=1，MP=0，STOP=1

30.3.4 双倍速操作和6倍比特率的频率

当SEMR.ABCS位设置为1并选择1位周期的8个基本时钟脉冲时，SCI以ABCS设置为0时的两倍比特率运行。当SEMR.BGDM位为设置为1，基本时钟的周期是BGDM设置为0时的一半，比特率是两倍。当SCR.CKE[1]位设置为0并且选择片内波特率发生器时，将ABCS和BGDM位设置为1允许SCI以四倍于ABCS和BGDM位设置为0时的比特率运行。

当SEMR.ABCSE位设置为1时，1位周期内的基本时钟脉冲数为6，SCI以16的比特率运行，是SEMR.ABCS=0时SEMR.BGDM=0时的3倍 和SEMR.ABCSE=0。

如30.3.2节中的公式（1）所示。异步模式下接收数据采样时序和接收裕度，当SEMR.ABCS或SEMR.ABCSE位设置为1时接收裕度减小。因此，如果将ABCS或ABCSE设置为0即可获得目标码率，则为建议您使用SCI，ABCS和ABCSE设置为0。

30.3.5 CTS和RTS函数

CTS功能在传输控制中使用CTSn_RTSn引脚上的输入。将SPMR.CTSE位设置为1可启用CTS功能。对于CTS和RTS的功能，您可以选择在一个端子上使用任一功能的交替设置和在两个端子上独立使用每个功能的专用设置。该设置通过SPMR.CTSPEN位完成。

当CTS功能使能时，将CTSn_RTSn引脚置于低电平会导致传输开始。

在传输过程中将CTSn_RTSn引脚驱动为高电平不会影响当前帧的传输。

在使用CTSn_RTSn引脚输出的RTS功能中，当可以接收时输出低电平。
本节显示了低电平和高电平的输出条件。

【低电平输出的条件】

本节列出了所有条件的满足情况。

Non-FIFO selected

●SCR.RE位的值为1

●接收未进行

●没有接收到的数据尚未读取

●SSR寄存器中的ORER、FER、PER标志位均为0

FIFO selected

●SCR.RE位的值为1

●写入FRDRHL的接收数据量等于或小于FCRH.RSTRG[3:0]的设定值

●SSR_FIFO寄存器中的ORER标志（FRRDH中的ORER）为0

【高电平输出条件】

●不满足低电平输出条件

30.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the DCCR.DCME bit is set to 1, when one frame of data is received, the SCI compares that received data with the data set in CDR.CMPD. If the SCI detects a match to the comparison data (CDR.CMPD*1) with the received data, the SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP bit = 1), if the DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match and receive data where the MPB bit is 0 is always treated as a non-match.

If the DCCR.IDSEL bit is set to 0, SCI performs address match detection regardless of the MPB bit value of the received data.

Until SCI detects a match to the comparison data (CDR.CMPD*1) with receive data, received data is skipped (discarded), and the SCI cannot detect a parity error or framing error.

When SCI detects a match, the DCCR.DCME bit is automatically cleared, and the DCCR.DCMF flag is set to 1. If the DCCR.IDSEL bit is set to 1, the SCR.MPIE bit is automatically cleared. If DCCR.IDSEL is set to 0, the value of the SCR.MPIE bit is retained. If the SCR.RIE bit is set to 1, the SCI issues an SCIn_RXI interrupt request.

If the SCI detects a framing error in the receive data for which a match is detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag is set to 1. The compared receive data is not stored in the RDR register, and SSR.RDRF remains 0. When FCR.FM = 1, the RDR register indicates the FRDRHL register, and the SSR.RDRF flag indicates the SSR_FIFO.RDF flag.

After the SCI detects a match, and DCCR.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the DCCR.DFER or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

Examples of the address match function are shown in Figure 30.9 and Figure 30.10.

Note 1. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, and CMPD[8:0] with 9-bit length.

30.3.6 地址匹配（接收数据匹配检测）功能

地址匹配功能只能在异步模式下使用。

如果DCCR.DCME位设置为1，当接收到一帧数据时，SCI会将接收到的数据与CDR.CMPD中设置的数据进行比较。如果SCI检测到比较数据(CDR.CMPD*1)与接收到的数据匹配，则SCI可以发出SCIn_RXI中断请求。

如果SMR.MP位设置为0，则仅对接收格式的有效数据进行比较。在多处理器模式下（SMR.MP位=1），如果DCCR.IDSEL位设置为1，则接收MPB位为1的数据进行地址匹配比较，接收MPB位为0的数据始终被视为不匹配。

如果DCCR.IDSEL位设置为0，SCI执行地址匹配检测，而不管接收数据的MPB位值如何。

在SCI检测到与接收数据的比较数据(CDR.CMPD*1)匹配之前，会跳过（丢弃）接收到的数据，并且SCI无法检测奇偶校验错误或帧错误。

当SCI检测到匹配时，自动清除DCCR.DCME位，并将DCCR.DCMF标志设置为1。如果DCCR.IDSEL位设置为1，SCR.MPIE位自动清零。如果DCCR.IDSEL设置为0，则SCR.MPIE位被保留。如果SCR.RIE位设置为1，则SCI发出SCIn_RXI中断请求。

如果SCI在检测到匹配的接收数据中检测到帧错误，则DCCR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER标志设置为1。比较后的接收数据不存入RDR寄存器，SSR.RDRF保持为0。当FCR.FM=1时，RDR寄存器指示FRDRHL寄存器，而

SSR.RDRF标志表示SSR_FIFO.RDF标志。

SCI检测到匹配后，DCCR.DCME自动清零，SCI根据当前寄存器设置连续接收下一个数据。

当设置DCCR.DFER或DCCR.DPER标志时，不执行地址匹配。在启用地址匹配功能之前，将DCCR.DFER和DCCR.DPER标志设置为0。

地址匹配函数的例子如图30.9和图30.10所示。

注1.此比较目标可以选择3种长度中的一种：7位长度的CMPD[6:0]、8位长度的CMPD[7:0]和9位长度的CMPD[8:0].

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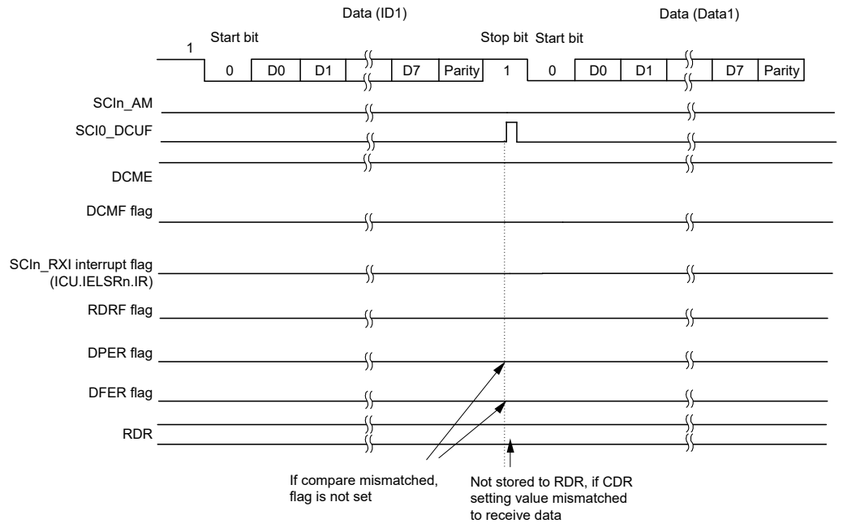
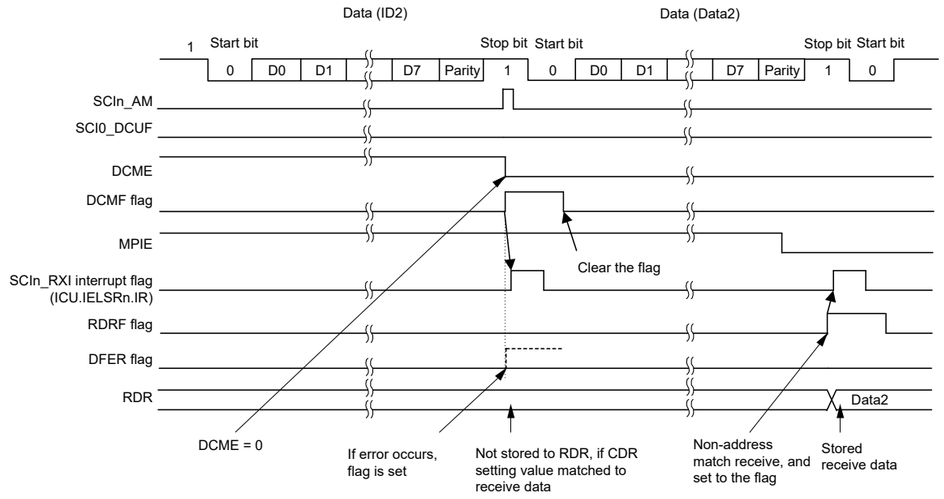
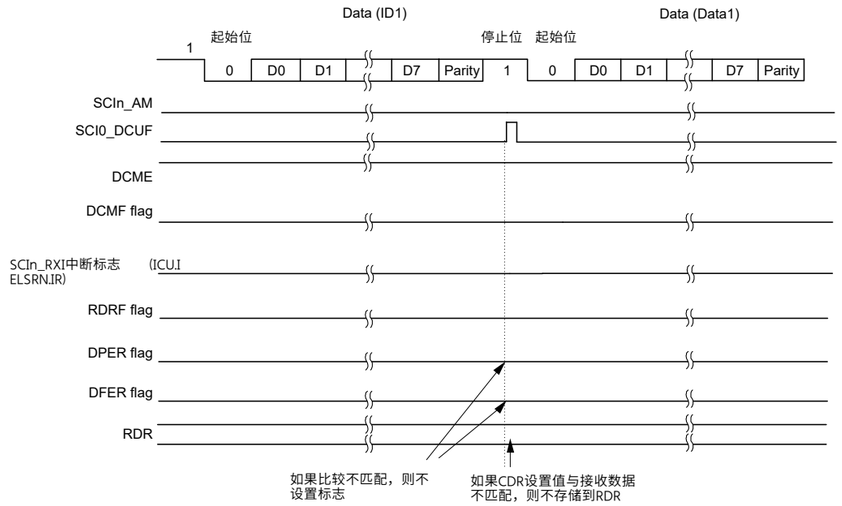


(a) Example of compare mismatched between receive data and CDR (8-bit length/parity/non multi-processor mode)

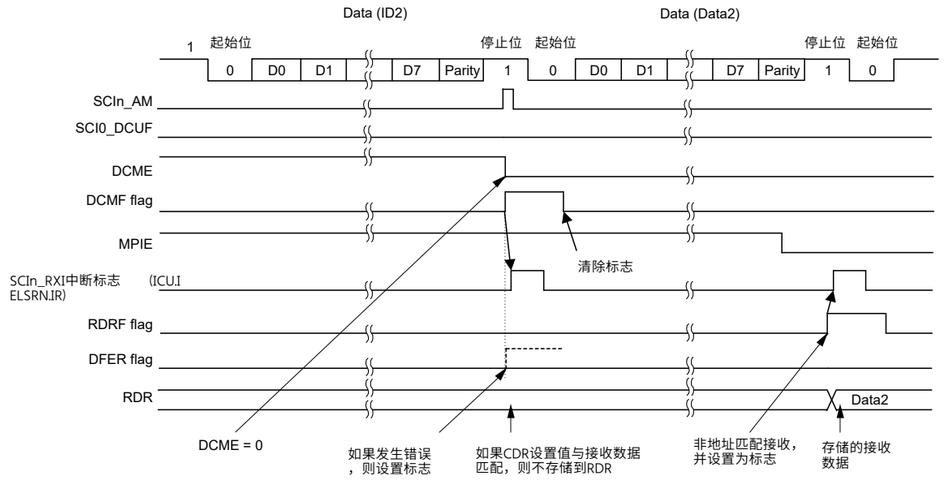


(b) Example of compare matched between receive data and CDR (8-bit length/parity/non multi-processor mode)

Figure 30.9 Example of address match (1) normal mode

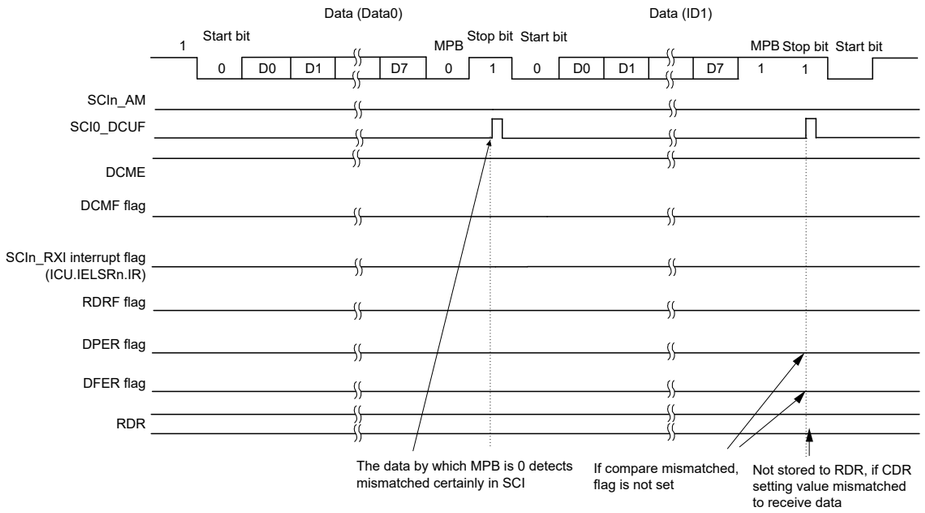


(a)接收数据和CDR比较不匹配的示例（8位长度奇偶校验非多处理器模式）

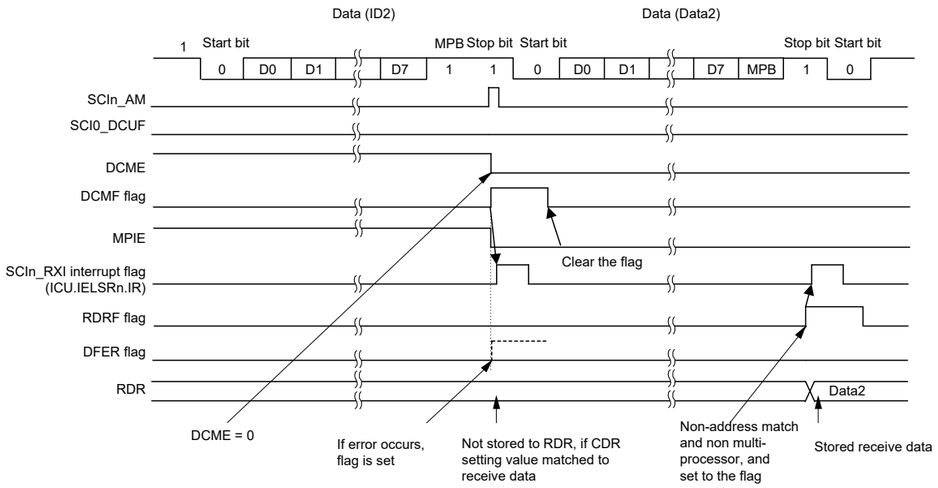


(b)接收数据与CDR比较匹配示例（8位长度奇偶校验非多处理器模式）

Figure 30.9 地址匹配示例（一）普通模式



(a) Example of compare mismatched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)



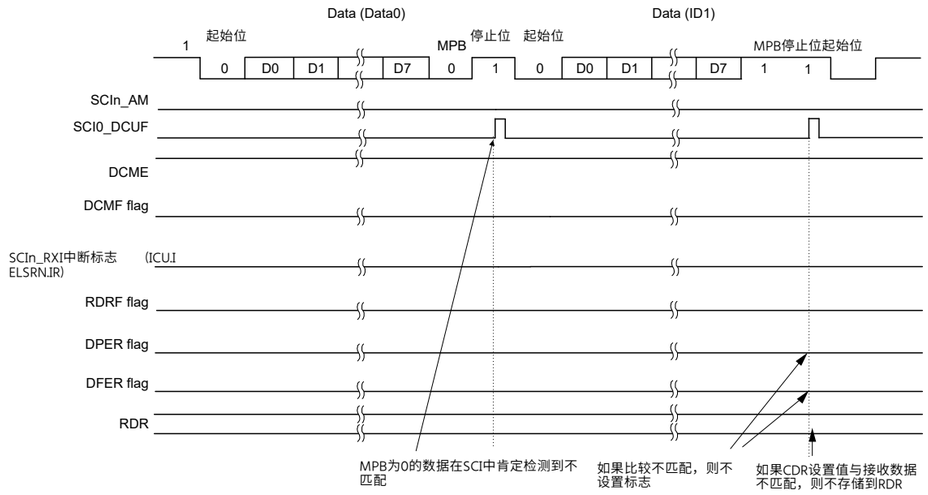
(b) Example of compare matched between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

Figure 30.10 Example of address match (2) multi-processor mode

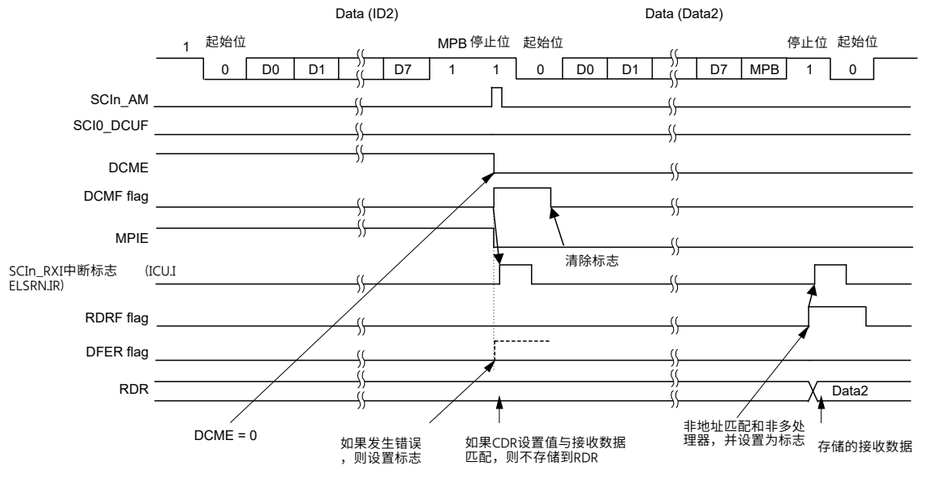
30.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the SCR register, then continue through the SCI initialization procedure (select non-FIFO or FIFO) shown in Table 30.28 and Table 30.29. Whenever the operating mode or transfer format is to be changed, the SCR register must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.



(a)接收数据和CDR比较不匹配的示例（8位长度IDSEL=1多处理器模式）



(b)接收数据和CDR比较匹配的示例（8位长度IDSEL=1多处理器模式）

Figure 30.10 地址匹配示例（二）多处理器模式

30.3.7 异步模式下的SCI初始化

在发送和接收数据之前，首先将初始值0x00写入SCR寄存器，然后继续执行SCI初始化程序（选择非FIFO或FIFO）如表30.28和表30.29所示。每当要更改操作模式或传输格式时，必须在更改之前初始化SCR寄存器。

在异步模式下使用外部时钟时，请确保在初始化期间提供时钟信号。

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Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO nor RDR and RDRHL. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

Table 30.28 Example flow of SCI initialization in asynchronous mode with non-FIFO selected

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM bit to 0	Set the FCR.FM bit to 0.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR. When the clock output is selected in asynchronous mode, the clock is output immediately after SCR settings are made.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR and ACTR	Set the communication terminals status in SPTR and adjustable sampling values in ACTR.
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
11	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn to be used.
12	Initialization completion	

Table 30.29 Example flow of SCI initialization in asynchronous mode with FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM, TFRST, and RFRST bits to 1. Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.	Set the FCR.FM, TFRST, and RFRST bits to 1 (FIFO mode enabled, transmit/receive FIFOs empty). Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR. When the clock output is selected in asynchronous mode, the clock is output immediately after SCR settings are made.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits to 0. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR and ACTR	Set the communication terminals status in SPTR and adjustable sampling values in ACTR.

Note: 将SCR.RE位设置为0既不会初始化SSRSSR_FIFO中的ORER、FER、RDRF、RDF、PER和DR标志，也不会初始化RDR和RDRHL。当TE位设置为0时，所选FIFO缓冲区的TEND标志未初始化。

Note: 在非FIFO模式下，当SCR.TIE位为1时，将SCR.TE位的值从1切换为0或从0切换为1会导致产生SCIn_TXI中断请求。

Table 30.28 选择非FIFO的异步模式下SCI初始化示例流程

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	将FCR.FM位设置为0	将FCR.FM位设置为0。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。 在异步模式下选择时钟输出时，时钟输出后立即进行SCR设置。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位为0。	将SIMR1.IICM位设置为0。 将SPMR.CKPH和CKPOL位设置为0。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在SPTR和ACTR中设置一个值	在SPTR中设置通讯端子状态，在ACTR中设置可调采样值。
8	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
9	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果SEMR中的BRME位设置为0或使用外部时钟。
10	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
11	将SCR.TE或RE位设置为1，并设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn。
12	初始化完成	

Table 30.29 选择FIFO的异步模式下SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	设置FCR.FM、TFRST和RFRST位为1。 设置FCR.TTRG[3:0]，RTRG[3:0]和RSTRG[3:0]位。	将FCR.FM、TFRST和RFRST位设置为1（启用FIFO模式，发送接收FIFO为空）。设置FCR.TTRG[3:0]、RTRG[3:0]和RSTRG[3:0]位。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。 在异步模式下选择时钟输出时，时钟输出后立即进行SCR设置。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位为0。	将SIMR1.IICM位设置为0。 将SPMR.CKPH和CKPOL位设置为0。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在SPTR和ACTR中设置一个值	在SPTR中设置通讯端子状态，在ACTR中设置可调采样值。

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Table 30.29 Example flow of SCI initialization in asynchronous mode with FIFO selected (2 of 2)

No.	Step Name	Description
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the FCR.TFRST and RFRST bits to 0	Set the FCR.TFRST and RFRST bits to 0.
11	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
12	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn to be used.
13	Initialization completion	

30.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 30.11, Figure 30.12, and Figure 30.13 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the SCR.TE bit is set to 1, the high level is output to TXDn for one frame. However, when SEMR.PADIS is set to "1", this preamble will not be output. An example of operation when preamble is not output is shown in Figure 30.14.

1. The SCI transfers data from the TDR[*1] register to the TSR register when data is written to TDR[*1] in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the TDR[*1] register to the TSR register. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to the TDR[*1] register in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR[*1] register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. The SCI checks for update of the TDR register on output of the stop bit.
5. When the TDR register is updated, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from the TDR[*1] register to the TSR register and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If the TDR register is not updated, the SSR.TEND flag is set to 1, the stop bit is sent, and the mark state is entered, in which 1 is output. If the SCR.TEIE bit is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. The TDRHL register when 9-bit data length is selected.

Figure 30.11, Figure 30.12, and Figure 30.13 show examples of serial transmission in asynchronous mode.

Table 30.29 选择FIFO的异步模式下SCI初始化示例流程（2个中的2个）

No.	步骤名称	Description
8	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
9	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果 SEMR中的BRME位设置为0或使用外部时钟。
10	设置FCR.TFRST和 RFRST位为0	将FCR.TFRST和RFRST位设置为0。
11	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
12	将SCR.TE或RE位设置为1，并 设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn。
13	初始化完成	

30.3.8 异步模式下的串行数据传输

(1)选择非FIFO图30.11、图30.12和图30.13显示了异步模式下串行传输的示例。

在串行传输中，SCI的操作如本节所述。当SCR.TE位设置为1时，高电平输出到TXDn一帧。但是，当SEMR.PADIS设置为“1”时，不会输出此前导码。图30.14显示了不输出前导码时的操作示例。

1.当在SCIn_TXI中断处理程序中将数据写入TDR*1时，SCI将数据从TDR*1寄存器传输到TSR寄存器。当一条指令同时将SCR.TE和SCR.TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。

2.在SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平导致数据从TDR*1寄存器传输到TSR寄存器后，传输开始。如果SCR.TIE位为1，则产生SCIn_TXI中断请求。通过在当前发送数据的发送完成之前将下一个发送数据写入SCIn_TXI中断处理程序中的TDR*1寄存器，可以进行连续发送。使用SCIn_TEI中断请求时，在写入最后一个要发送的数据后，将SCR.TIE位设置为0（禁止SCIn_TXI中断请求）并将SCR.TEIE位设置为1（启用SCIn_TEI中断请求）从SCIn_TXI请求的处理例程到TDR*1寄存器。

3.数据按以下顺序从TXDn引脚发送：

- ●起始位
- ●传输数据
- ●奇偶校验位或多处理器位（可根据格式省略）
- ●停止位

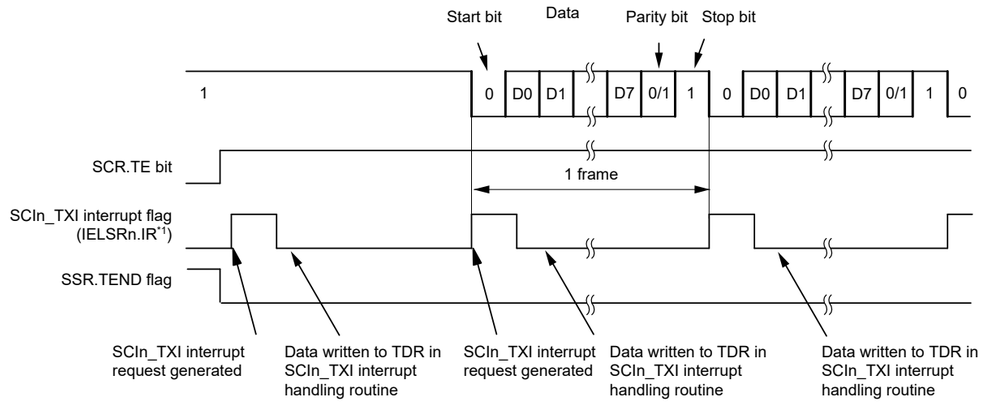
4.SCI在停止位输出时检查TDR寄存器的更新。

5.当TDR寄存器更新时，将SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平输入会导致下一个发送数据从TDR*1寄存器传输到TSR寄存器，并且传输停止位，然后开始下一帧的串行传输。

6、如果TDR寄存器没有更新，则将SSR.TEND标志置1，发送停止位，进入标记状态，其中输出1。如果SCR.TEIE位为1，则SSR.TEND标志设置为1，并产生SCIn_TEI中断请求。

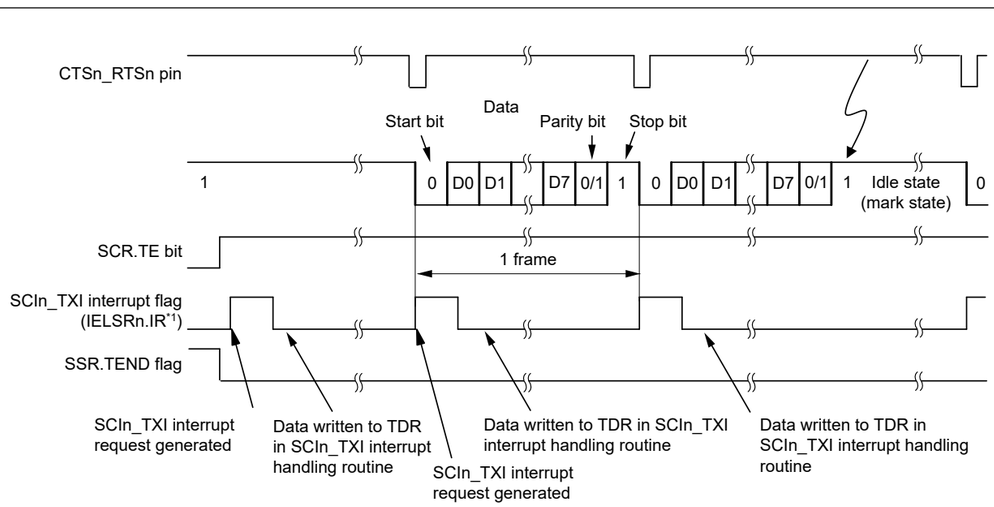
注1.选择9位数据长度时的TDRHL寄存器。

图30.11、图30.12和图30.13显示了异步模式下的串行传输示例。



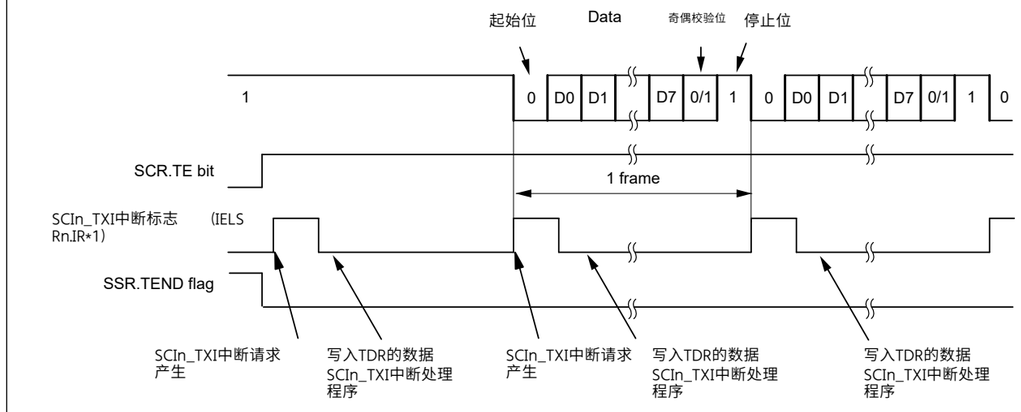
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.11 Example operation for serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission



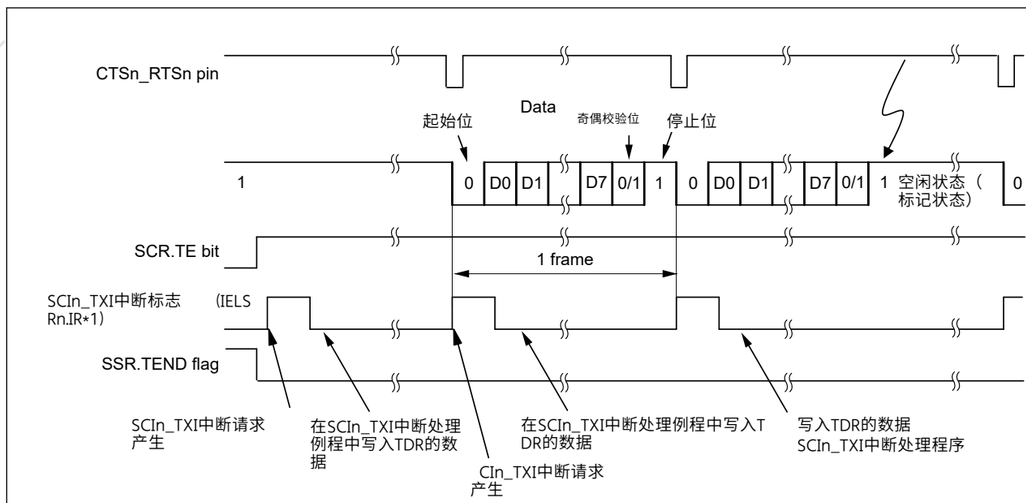
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.12 Example operation for serial transmission in asynchronous mode (2) with 8-bit data, parity bit, one stop bit, CTS function used, and at the beginning of transmission



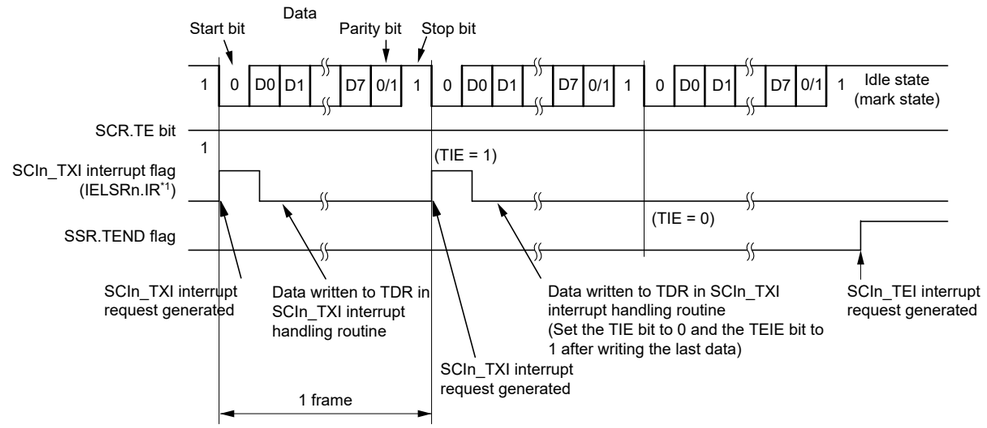
注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.11 异步模式下串行传输的示例操作(1)使用8位数据、奇偶校验位、1个停止位、未使用CTS功能以及传输开始时



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.12 异步模式下串行传输的示例操作(2)使用8位数据、奇偶校验位、一个停止位、使用CTS功能以及在传输开始时



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.13 Example operation for serial transmission in asynchronous mode (3) with 8-bit data, parity bit, one stop bit, CTS function not used, and from the middle of transmission until transmission completion

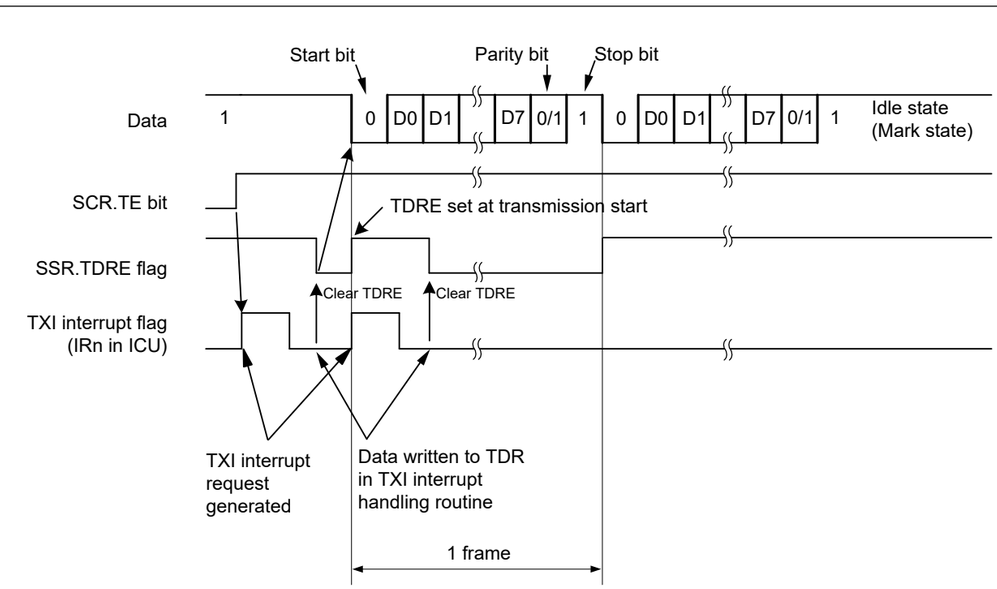
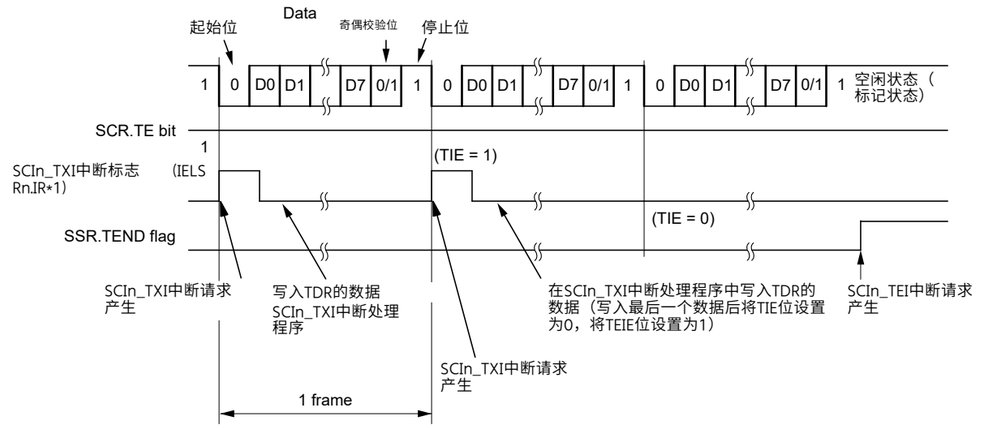


Figure 30.14 Example of Operation for Serial Transmission in Asynchronous Mode (4)(with 8-Bit Data, Parity, 1 Stop Bit, CTS Function Not Used, from the Middle of Transmission until Transmission Completion, stop preamble)



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.13 异步模式下串行传输的示例操作(3)使用8位数据、奇偶校验位、一个停止位、未使用CTS功能，以及从传输中间到传输完成

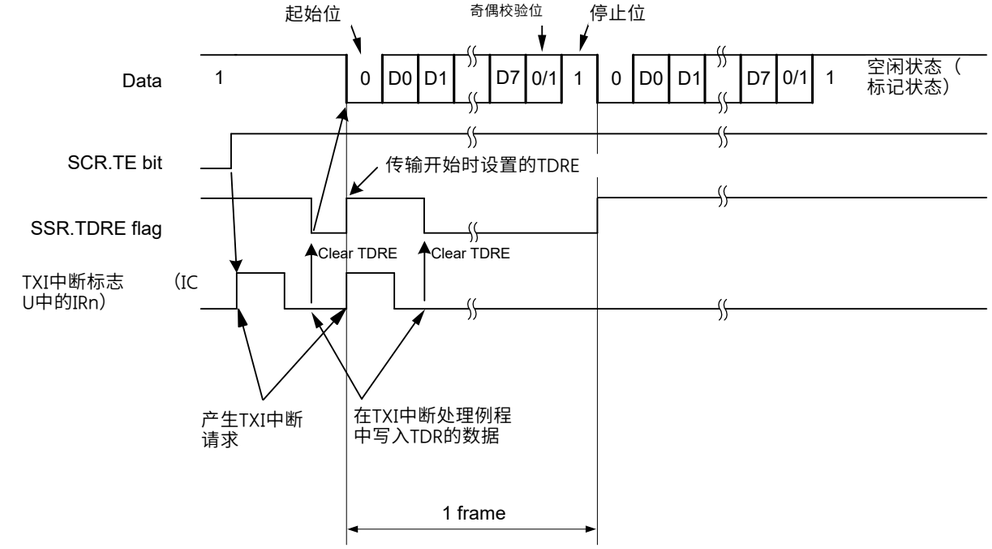
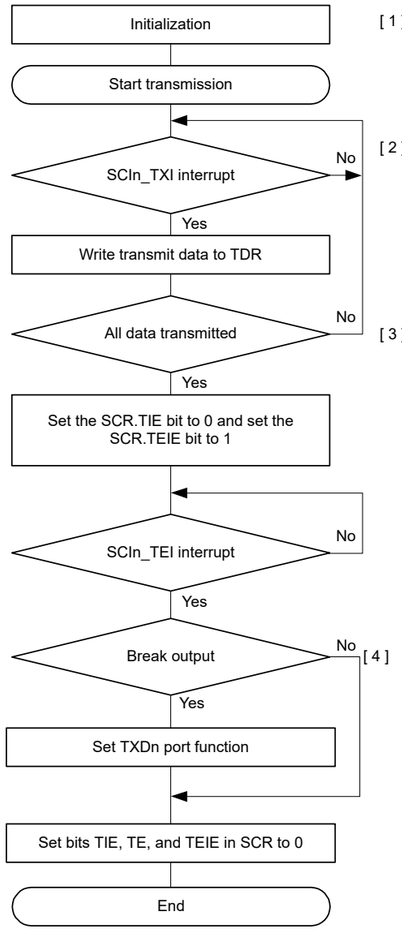


Figure 30.14 异步模式下串行传输的操作示例(4)（使用8位数据，奇偶校验，1个停止位，未使用CTS功能，从传输中间到传输完成，停止序言）



[1] SCI Initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to TDR by an SCIn_TXI interrupt request. When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated. Write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR once using an SCIn_TXI interrupt request. Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

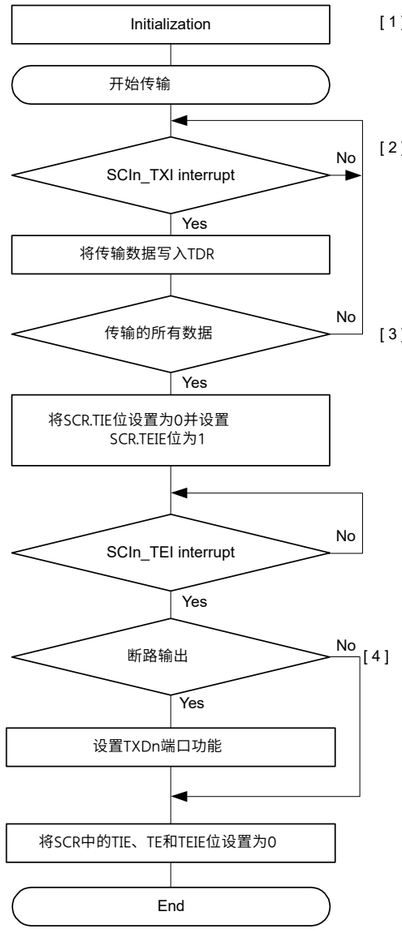
[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 30.15 Example flow of serial transmission in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 30.16 shows an example of a data format that is written to FTDRH and FTDRL register in asynchronous mode.

Data corresponding to the data length is set to FTDRH and FTDRL. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI Initialization:
设置数据传输。
SCR.TE位设置为1后，每帧输出1，并启用传输。

[2]通过SCIn_TXI中断请求将数据写入TDR。当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。在SCIn_TXI中断处理程序中将发送数据写入TDR一次。

[3]串行传输继续程序：
继续串行传输写入传输数据到
TDR一次使用SCIn_TXI中断请求。
也可以通过激活DMAC或DTC将传输数据写入TDR。当SCIn_TEI中断请求正在使用时，设置

在将要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

[4]串行传输结束时中断输出：
要在串行传输中输出中断，在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，设置
SCR.TE位为0。

Figure 30.15 选择非FIFO的异步模式下串行传输示例流程

(2) FIFO selected

图30.16显示了在异步模式下写入FTDRH和FTDRL寄存器的数据格式示例。

对应于数据长度的数据被设置为FTDRH和FTDRL。为未使用的位写入0。从FTDRH按顺序写到FTDRL.

RA生态工作室

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

Note: —: Invalid. The write value should be 0.

Figure 30.16 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level is output to TXDn for one frame (preamble).

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the FTDRL*1 register to the TSR register. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, SSR_FIFO.TDFE is set to 1. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the FTDRL*1*2 register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit
4. On output of the stop bit, the SCI checks whether non-transmitted data remains in the FTDRL*3 register.
5. When data is set to FTDRL*3, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the SCR.TEIE bit is 1, the SSR_FIFO.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data not to FTDRL but to the FTDRH and FTDRL registers.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FTDRL register and not the FTDRH register when 9-bit data length is selected.

Figure 30.17 shows an example flow of serial transmission in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	—	—	8位传输数据							
9 bits	0	Don't care	—	—	—	—	—	—	—	9位传输数据								

Note: —：无效的。写入值应为0。

Figure 30.16 选择FIFO写入FTDRH和FTDRL的数据格式

在串行传输中，SCI的操作如本节所述。当TE位设置为1时，高电平输出到TXDn一帧（前导码）。

1.当数据写入FTDRL*1时，SCI将数据从FTDRL*1寄存器传输到TSR寄存器

SCIn_TXI中断处理程序。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。当一条指令同时将SCR.TE和SCR.TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。

2.在SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平导致数据从FTDRL*1寄存器传输到TSR寄存器后，传输开始。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO.TDFE设置为1。如果SCR.TIE位为1，则产生SCIn_TXI中断请求。在当前发送数据的发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入FTDRL*1，可以进行连续发送。当使用SCIn_TEI中断请求时，将SCR.TIE位设置为0（禁止SCIn_TXI中断请求）并且

将要发送的最后一个数据写入到SCR.TEIE位为1（启用SCIn_TEI中断请求）FTDRL*1*2寄存器来自SCIn_TXI请求的处理例程。

3.数据按以下顺序从TXDn引脚发送：

- ●起始位
- ●传输数据
- ●奇偶校验位或多处理器位（可根据格式省略）
- ●停止位

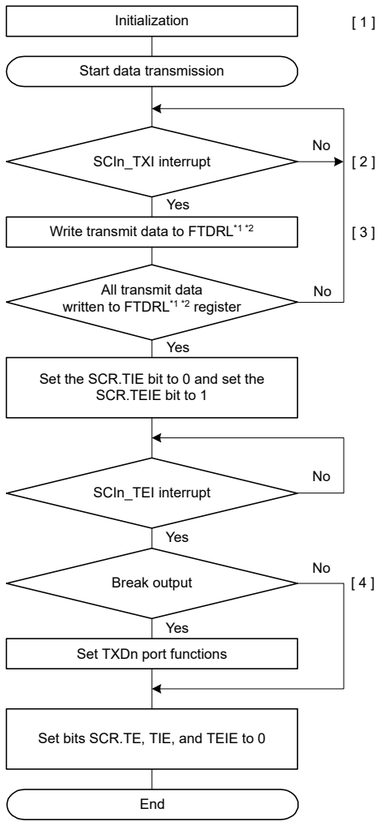
4.在停止位输出时，SCI检查未发送的数据是否保留在FTDRL*3寄存器中。

5.当数据设置为FTDRL*3时，将SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平输入会导致下一个传输数据从FTDRL*1传输到TSR并传输停止位，之后开始下一帧的串行传输。

6.如果FTDRL*3中没有设置数据，则将SSR_FIFO中的TEND标志设置为1，发送停止位，并进入输出1的标记状态。如果SCR.TEIE位为1，则SSR_FIFO.TEND标志设置为1，并产生SCIn_TEI中断请求。

注1.不要将数据写入FTDRL，而是写入FTDRH和FTDRL寄存器。
注2.选择9位数据长度时，按从FTDRH到FTDRL的顺序写入数据。
注意3.SCI仅检查对FTDRL寄存器的更新，而不是选择9位数据长度时的FTDRH寄存器。

图30.17显示了选择FIFO的异步模式下串行传输的示例流程。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRL to TSR, when the quantity of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1 *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and clear the SSR_FIFO.TDFE flag to 0. The number of transmission data it is possible to write in is 16 - (the number of stored transmit FIFO data). Transmit data can also be written to FTDRL by activating the DTC or DMAC. When writing the data to FTDRL by DTC or DMAC, the TDFE flag is cleared automatically, so do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note 1. When data length is 9 bits, this refers to FTDRH and FTDRL registers.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 30.17 Example flow of serial transmission in asynchronous mode with FIFO selected

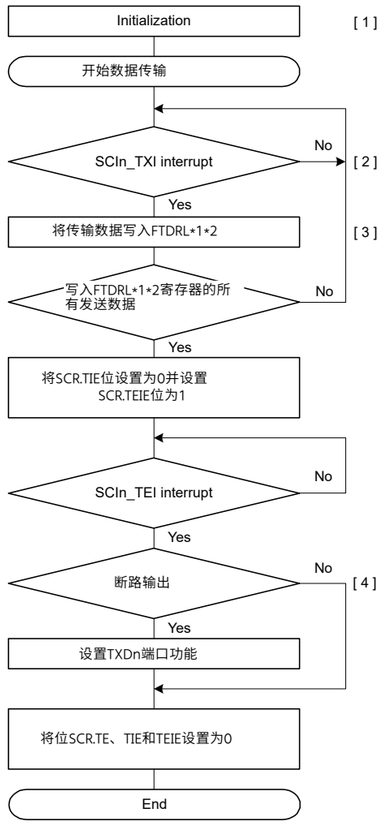
30.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

Figure 30.18 and Figure 30.19 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and when it detects a start bit, the SCI performs internal synchronization, stores receive data in RSR.
3. If the multi-processor communication function is enabled (SMR.MP = 1), see section 30.4.2. Multi-Processor Serial Data Reception. If the address match function (data compare match function) is enabled (DCCR.DCME = 1), the SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and comparison data (CDR.CMPD*1).
4. If the SCI detects an address match, the DCCR.DCME bit is automatically cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt*2 request is generated. To enable the generation of an SCIn_RXI interrupt request, set the SCR.RIE bit to 1. The compared receive data are not stored in the RDR register*3. The SSR.RDRF flag remains 0.



[1] SCI initialization:
设置数据传输。
SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] 通过SCIn_TXI中断请求将数据写入FTDRL*1：
当发送数据从FTDRL传输到TSR时，当写入FTDRL的发送数据量等于或小于指定的发送触发数时，将产生发送数据FIFO空中断（SCIn_TXI）请求。在SCIn_TXI中断处理例程中将发送数据写入FTDRL*1*2一次。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将所有传输数据写入FTDRL，并将SSR_FIFO.TDFE标志清零。可以写入的传输数据数为16（存储的传输FIFO数据数）。也可以通过激活DTC或DMAC将传输数据写入FTDRL。通过DTC或DMAC将数据写入FTDRL时，TDFE标志会自动清除，因此不要写入

TDFE flag.
使用SCIn_TEI中断请求时，将要发送的最后一个数据写入FTDRL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

注1.当数据长度为9位时，指的是FTDRH和FTDRL寄存器。
注2.当数据长度为9位时，按照FTDRH到FTDRL的顺序写入。

Figure 30.17 选择FIFO的异步模式下串行传输示例流程

30.3.9 异步模式下的串行数据接收

(1) Non-FIFO selected

图30.18和图30.19显示了异步模式下串行数据接收操作的示例。

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。

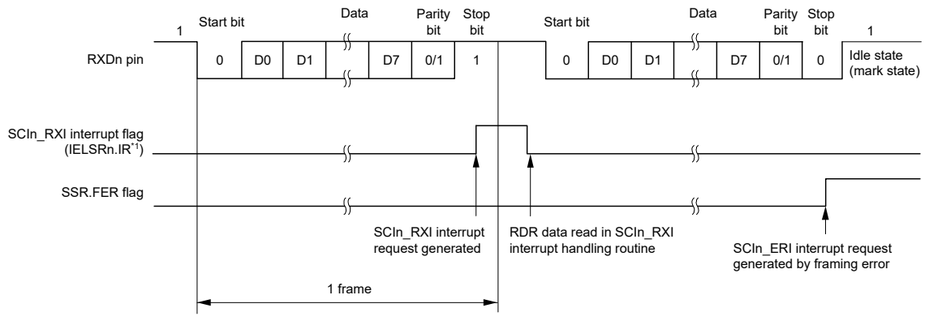
2.SCI监控通信线路，当检测到起始位时，SCI执行内部同步，将接收数据存储在RSR中。

3.如果启用多处理器通信功能（SMR.MP=1），请参见第30.4.2节。多处理器串行数据接收。如果地址匹配功能（数据比较匹配功能）被启用（DCCR.DCME=1），SCI无法检测奇偶校验或帧错误，因为接收数据被跳过（丢弃），直到SCI检测到接收数据和比较之间的匹配数据（CDR.CMPD*1）。

4.如果SCI检测到地址匹配，DCCR.DCME位自动清零，DCCR.DCMF标志变为1，并产生SCIn_AM中断*2请求。要启用SCIn_RXI中断请求的生成，请将SCR.RIE位设置为1。比较的接收数据不存储在RDR寄存器*3中。SSR.RDRF标志保持为0。

5. If the SCI detects a framing error in the receive data for which an address match is detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag becomes 1. To enable the generation of an SCIn_ERI interrupt request, set the SCR.RIE bit to 1.
6. If a framing or a parity error is detected (the DCCR.DFER flag or DCCR.DPER flag is 1) in the SCIn_AM interrupt handling routine, set the DCCR.DFER and DCCR.DPER flags to 0 and set the DCCR.DCME bit to 1 to enable the address match function again. If neither a framing nor a parity error has been detected (the DCCR.DFER and DCCR.DPER flags are both 0), set the DCCR.DCMF flag to 0. See Figure 30.9.
7. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR*3 register.
8. If a parity error is detected, the SSR.PER flag is set to 1 and receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
9. If a framing error is detected, the SSR.FER flag is set to 1 and receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
10. When reception finishes successfully, receive data is transferred to the RDR*3 register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data is complete. Reading the received data that was transferred to the RDR register causes the CTSn_RTSn pin to output low.

Note 1. This scope of comparison is selectable as one of three lengths: CMPD[6:0] is for 7-bit length, CMPD[7:0] is for 8-bit length, and CMPD[8:0] is for 9-bit length.
Note 2. As no interrupt enable bit is assigned to the SCIn_AM interrupt, an interrupt request is generated by setting the DCCR.DCMF to 1.
Note 3. Only read data in the RDRHL register when 9-bit data length is selected.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.18 Example of SCI operation for serial reception in asynchronous mode (1) when the RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit

5.如果SCI在检测到地址匹配的接收数据中检测到帧错误，则DCCR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER标志变为1.要启用SCIn_ERI中断请求的生成，请将SCR.RIE位设置为1。

6.如果在SCIn_AM中断处理例程中检测到成帧或奇偶校验错误（DCCR.DFER标志或DCCR.DPER标志为1），则将DCCR.DFER和DCCR.DPER标志设置为0，并设置DCCR.DCME位为1以再次启用地址匹配功能。如果未检测到成帧错误或奇偶校验错误（DCCR.DFER和DCCR.DPER标志均为0），则将DCCR.DCMF标志设置为0。参见图30.9。

7.如果发生溢出错误，则SSR.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR*3寄存器。

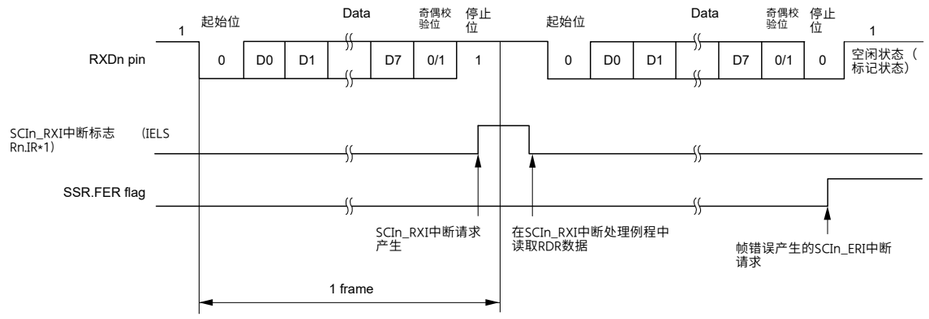
8.如果检测到奇偶校验错误，则将SSR.PER标志设置为1，并将接收数据传输到RDR*3寄存器。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。

9.如果检测到帧错误，则将SSR.FER标志设置为1，并将接收数据传输到RDR*3寄存器。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。

10.接收成功后，接收数据被传送到RDR*3寄存器。如果SCR.RIE位为1，则
SCIn_RXI中断请求产生。通过读取传输到的接收数据启用连续接收
在接收下一个接收数据完成之前，SCIn_RXI中断处理程序中的RDR寄存器。
读取传输到RDR寄存器的接收数据会导致CTSn_RTSn引脚输出低电平。

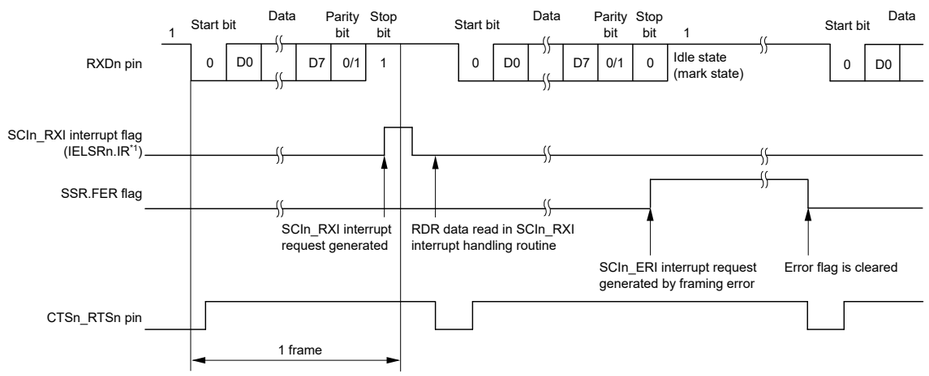
注1.此比较范围可选择以下三种长度之一：CMPD[6:0]用于7位长度，CMPD[7:0]用于8位长度，CMPD[8:0]用于9位长度。

注2.由于没有为SCIn_AM中断分配中断使能位，因此通过设置
DCCR.DCMF to 1.
注3.选择9位数据长度时，仅读取RDRHL寄存器中的数据。



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.18 异步模式下串行接收的SCI操作示例(1)不使用RTS功能时，具有8位数据、奇偶校验位和1个停止位



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.19 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

Table 30.30 lists the states of the flags in the SSR register and receive data handling when a receive error is detected.

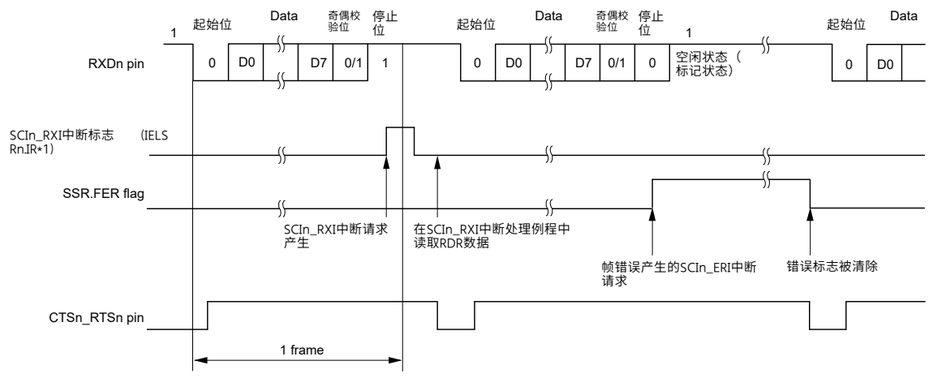
If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER bits to 0 before resuming reception. In addition, be sure to read the RDR or RDRHL register during overrun error processing. When a reception is forced to terminate by setting the SCR.RE bit to 0 during operation, read the RDR or RDRHL register because received data that is not yet read might be left in the RDR or RDRHL.

Figure 30.20 and Figure 30.21 show example flows of serial data reception.

Table 30.30 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register			Receive data	Receive error type
ORER	FER	PER		
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR*1	Framing error
0	0	1	Transferred to RDR*1	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR*1	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.19 使用RTS功能，8位数据、奇偶校验位和1个停止位时，异步模式下串行接收的SCI操作示例(2)

表30.30列出了SSR寄存器中标志的状态以及检测到接收错误时的接收数据处理。

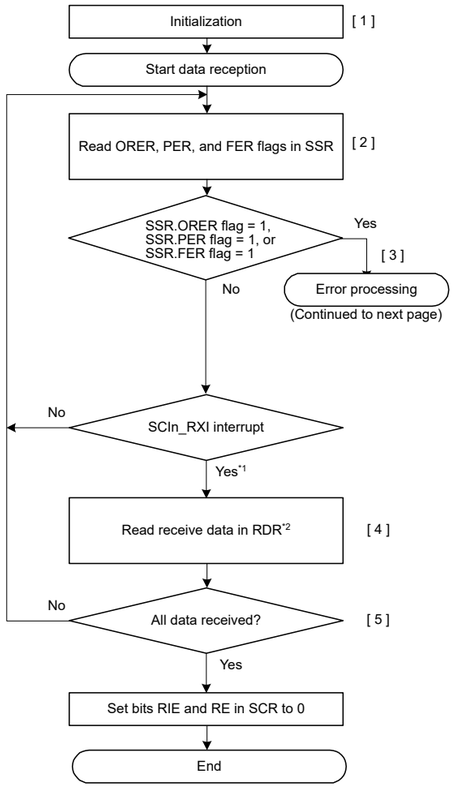
如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。
当接收错误标志为1时，无法恢复数据接收。因此，在恢复接收之前，请将ORER、FER和PER位设置为0。此外，请务必在溢出错误处理期间读取RDR或RDRHL寄存器。如果在操作期间通过将SCR.RE位设置为0来强制终止接收，请读取RDR或RDRHL寄存器，因为尚未读取的已接收数据可能留在RDR或RDRHL中。

图30.20和图30.21显示了串行数据接收的示例流程。

Table 30.30 SSR状态寄存器中的标志和接收数据处理

SSR状态寄存器中的标志			接收数据	接收错误类型
ORER	FER	PER		
1	0	0	Lost	溢出错误
0	1	0	转移到RDR*1	构图错误
0	0	1	转移到RDR*1	奇偶校验错误
1	1	0	Lost	溢出错误+成帧错误
1	0	1	Lost	溢出错误+奇偶校验错误
0	1	1	转移到RDR*1	成帧错误+奇偶校验错误
1	1	1	Lost	溢出错误+帧错误+奇偶校验错误

注1.选择9位数据长度时，仅读取RDRHL寄存器中的数据。



[1] SCI initialization:
Set data reception.

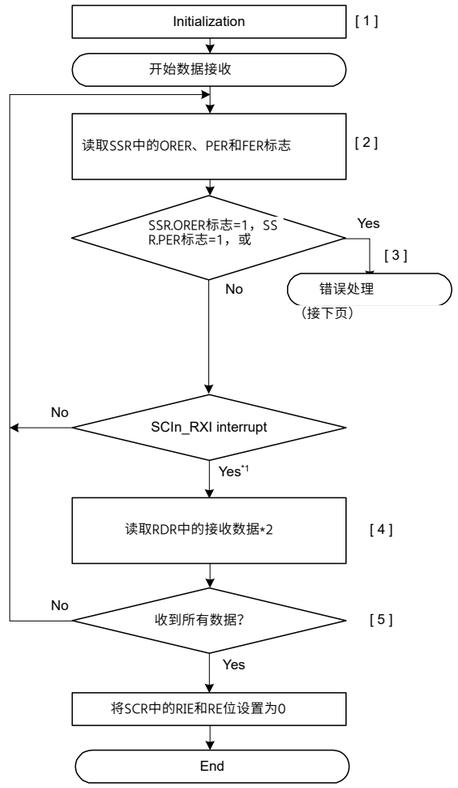
[2][3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. The error type is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, be sure to set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. For a framing error, a break can be detected by reading the value of the input port associated with the RXDn pin.

[4] Read the receive data in RDR once inthe SCIn_RXI interrupt handling routine.

[5] To continue serial reception, before the stop bit of the current frame is received, read data from RDR in the SCIn_RXI interrupt processing routine. The RDR data can also be read by activating the DMAC or DTC.

Note 1. Do not set RE to 0 before reading RDR.
Note 2. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 30.20 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (1)



[1]SCI初始化：设置数据
接收。

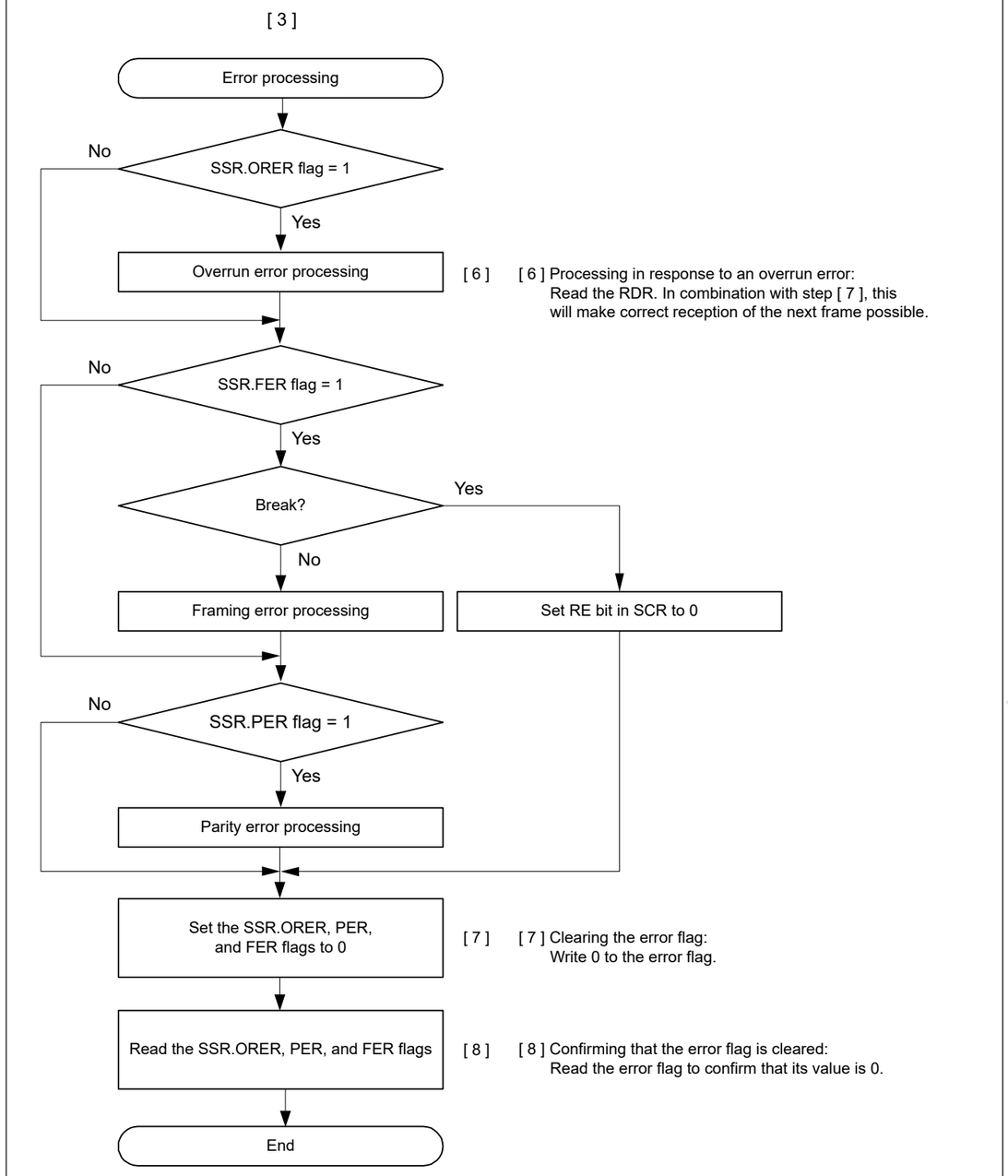
[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中
断。
错误类型通过读取SSR中的ORER、PER和FER标志来识别。执行适当的错误处理后，请务必将ORER、PER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。对于 帧错误，可以通过读取值来检测中断与RXDn引脚相关的输入端口。

[4]在SCIn_RXI中断处理程序中读取一次RDR中的接收数据。

[5]要继续串行接收，在接收到当前帧的停止位之前，在SCIn_RXI中断处理程序中从RDR中读取数据。RDR数据也可以通过激活DMAC或DTC来读取。

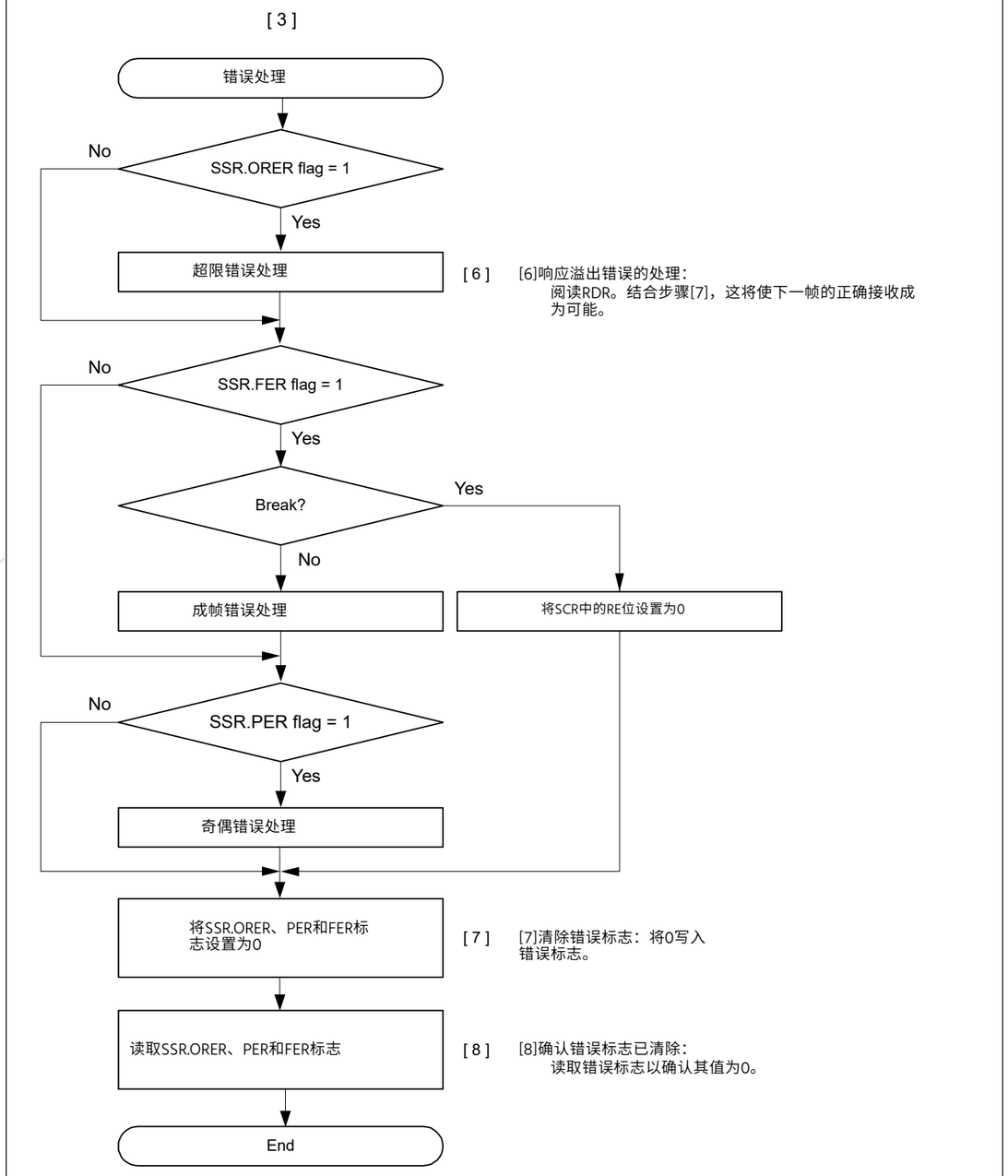
注1.在读取RDR之前不要将RE设置为0。
Note2.TheRDRregisterbecomestheRDRHLregisterwhen9−bitdatalengthisselected.

Figure 30.20 异步模式下串行接收的示例流程，选择了非FIFO和地址匹配已禁用(1)



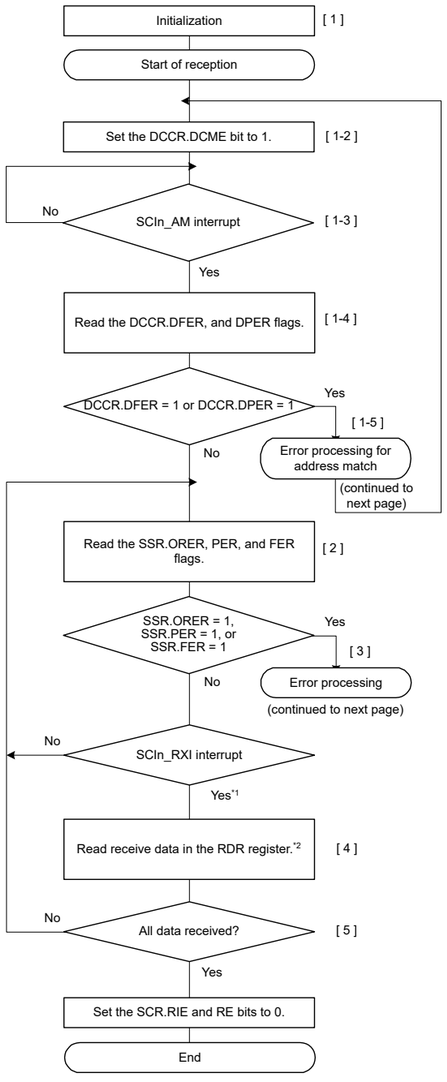
Note: The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 30.21 Example flow of serial reception in asynchronous mode with non-FIFO selected and Address Matching Disabled (2)



Note: 选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 30.21 异步模式下串行接收的示例流程，选择了非FIFO和地址匹配已禁用(2)



[1] SCI initialization:
Set data reception.

[1-2] Address match cycle:
Set the DCCR.DCME bit to 1 to enable address matching.

[1-3] Comparing receive data and data for comparison (CDR.CMPD):
Compare receive data and data for comparison (CDR.CMPD).
The SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and data for comparison.
If the SCI detects an address match, the DCCR.DCME bit is cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt request is issued.

[1-4] [1-5] Reception error processing:
An error is identified by reading the DFER or DPER flag in DCCR in the SCIn_AM interrupt handling routine.
After appropriate handling of the error, set both the DFER and DPER flags to 0.
If either of these flags is set to 1, address matching cannot be resumed.

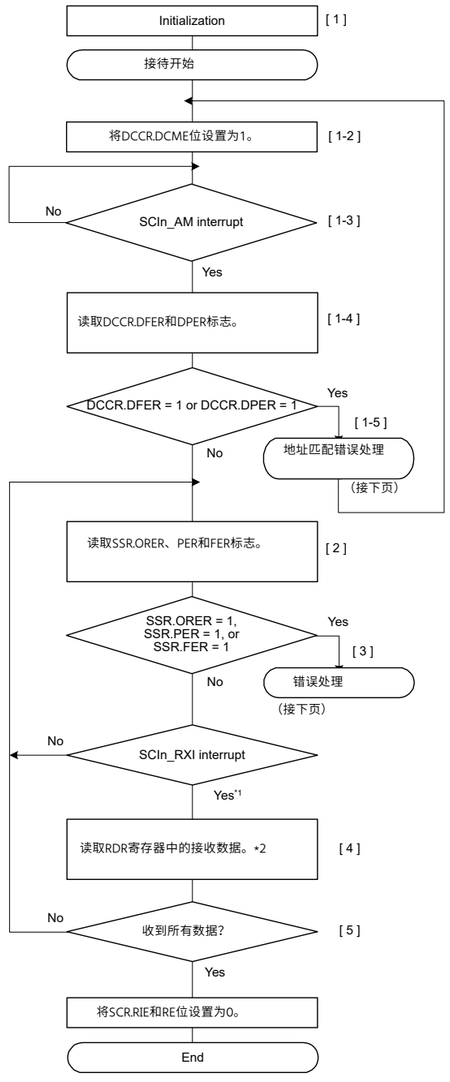
[2] [3] Reception error processing and break detection:
When a reception error occurs, the SCIn_ERI interrupt is generated.
The error is identified by reading the ORER, PER, and FER flags in the SSR.
After appropriate handling of the error, set all of the ORER, PER, and FER flags to 0. If any of these flags is set to 1, reception cannot be resumed.
If a framing error occurs, a break can be detected by reading the value of the input port bit corresponding to the RXDn pin.

[4] Read the receive data in the RDR register from within the SCIn_RXI interrupt handling routine.

[5] Procedure for continuing serial reception:
To continue serial reception, read the value of the RDR register in the SCIn_RXI interrupt handling routine before the stop bit is received.
The value of the RDR register can also be read by activating the DMAC or DTC.

Note 1. Be sure to set the RE bit to 0 before reading the RDR register.
Note 2. The RDRHL register is used instead of the RDR register when the 9-bit data length is selected.

Figure 30.22 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (1)



[1]SCI初始化：设置数据接收。

[1-2]地址匹配周期：将DCCR.DCME位设置为1以启用地址匹配。

[1-3]比较接收数据和比较数据（CDR.CMPD）：比较接收数据和比较数据（CDR.CMPD）。
SCI无法检测奇偶校验或成帧错误，因为接收数据被跳过（丢弃），直到SCI检测到接收数据和用于比较的数据之间的匹配。如果SCI检测到地址匹配，则DCCR.DCME位被清零，

DCCR.DCMF标志变为1，并发出SCIn_AM中断请求。

[1-4][1-5]接收错误处理：通过读取DCCR中的DFER或DPER标志来识别错误

SCIn_AM中断处理例程。
正确处理错误后，将DFER和DPER标志都设置为0。如果这些标志中的任何一个设置为1，则无法恢复地址匹配。

[2][3]接收错误处理和中断检测：当发生接收错误时，会产生SCIn_ERI中断。
通过读取SSR中的ORER、PER和FER标志来识别错误。
正确处理错误后，将所有ORER、PER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。如果发生帧错误，可以通过读取对应于RXDn引脚的输入端口位的值来检测中断。

[4]从SCIn_RXI中断处理程序中读取RDR寄存器中的接收数据。

[5]继续串行接收的过程：要继续串行接收，在接收到停止位之前，在SCIn_RXI中断处理程序中读取RDR寄存器的值。RDR寄存器的值也可以通过激活DMAC或DTC来读取。

注1.务必在读取RDR寄存器之前将RE位设置为0。
注意2。选择9位数据长度时，使用RDRHL寄存器代替RDR寄存器。

Figure 30.22 异步模式下串行接收的示例流程图（未选择FIFO和地址Matching Enabled) (1)

RA生态工作室

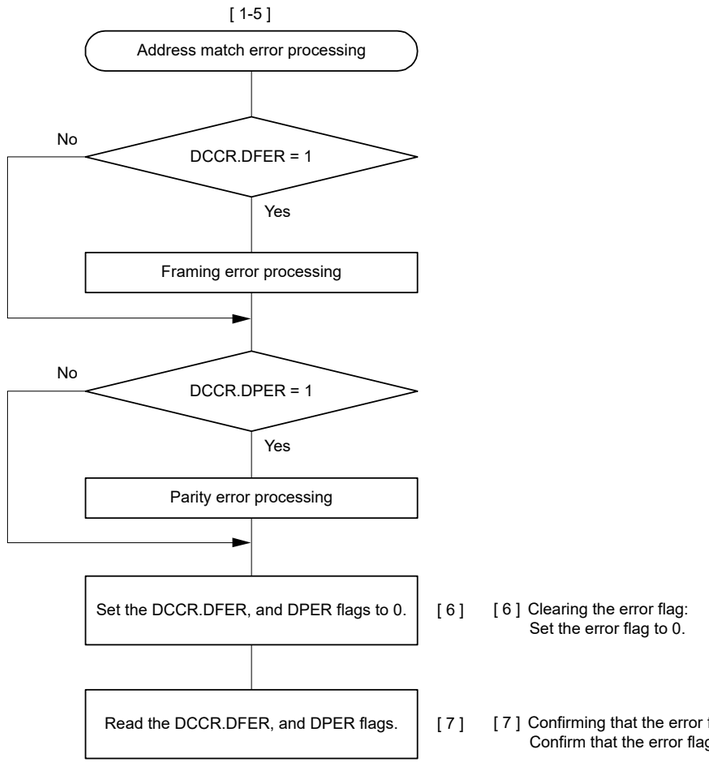


Figure 30.23 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (2)

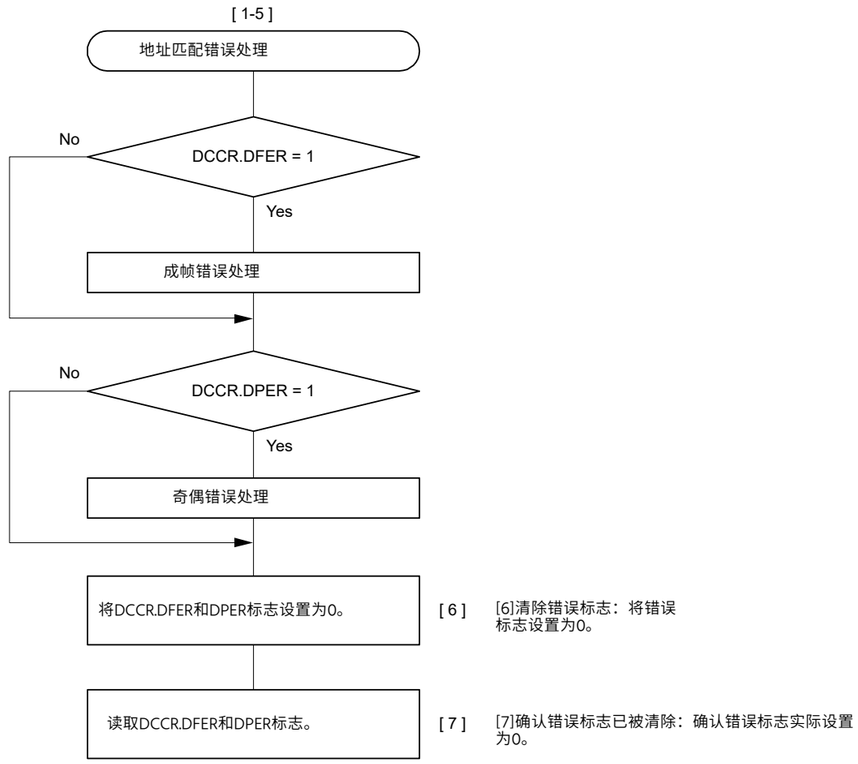


Figure 30.23 异步模式下串行接收的示例流程图（未选择FIFO和地址Matching Enabled) (2)

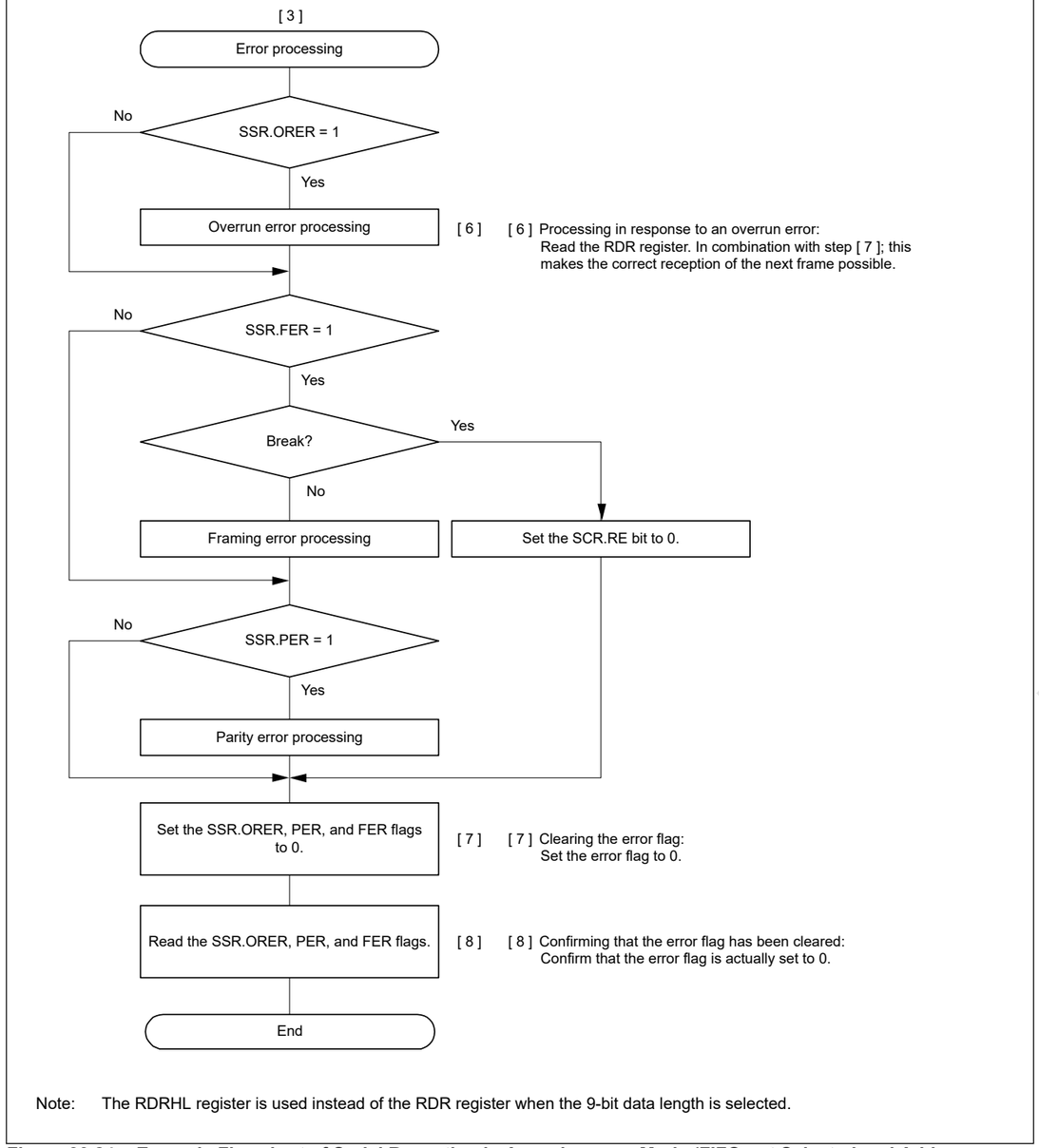


Figure 30.24 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO not Selected and Address Matching Enabled) (3)

(2) FIFO selected

Figure 30.25 shows an example of a data format that is written to FRDRH register and FRDRL register in asynchronous mode.

In asynchronous mode, 0 is written to the MPB bit in the FRDRH register. Data that corresponds to the data length is written to FRDRH and FRDRL. Unused bits are written as 0. Read in order from FRDRH to FRDRL. If software reads FRDRL, the

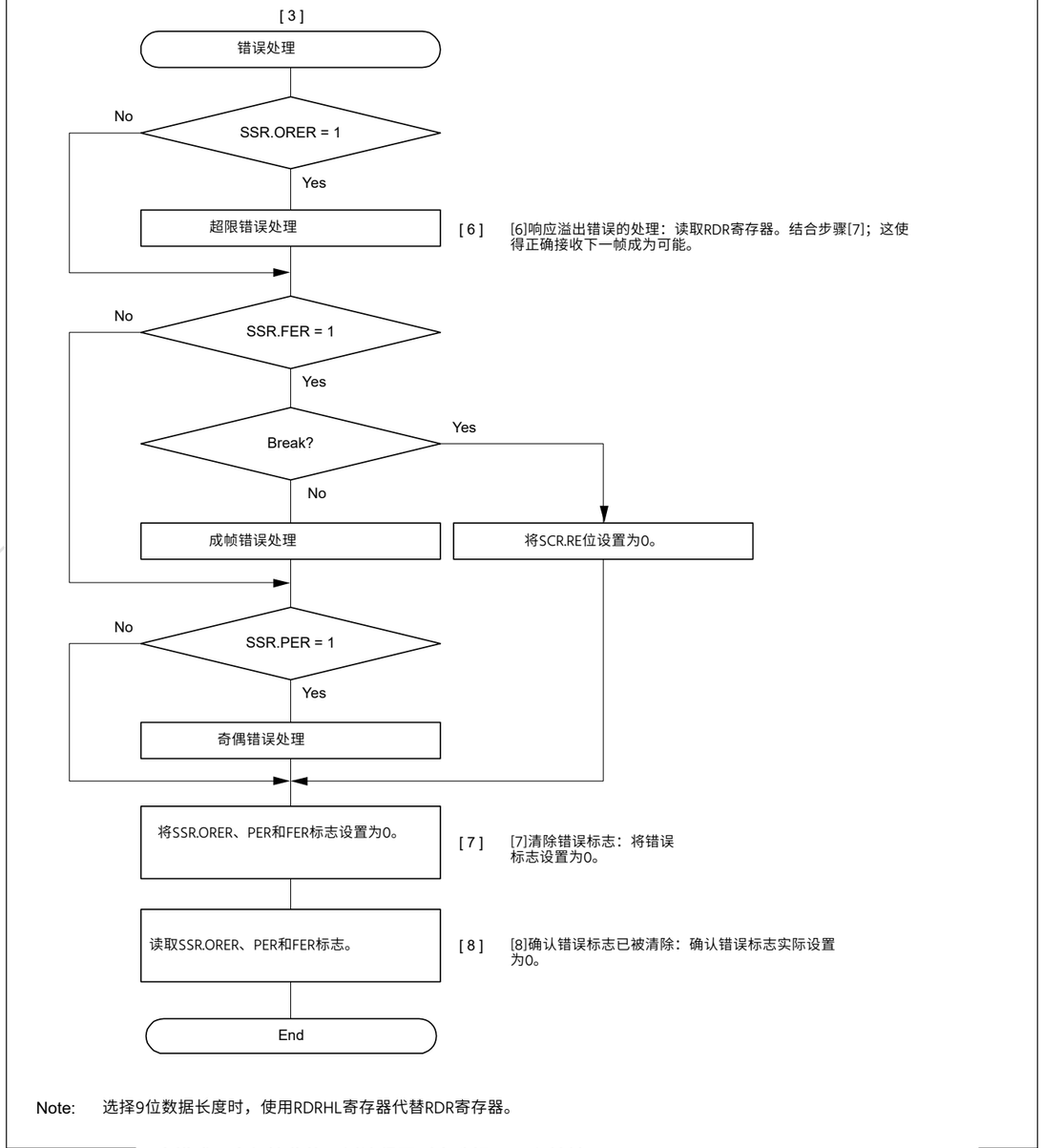


Figure 30.24 异步模式下串行接收的示例流程图（未选择FIFO和地址 Matching Enabled) (3)

(2) FIFO selected

图30.25显示了在异步模式下写入FRDRH寄存器和FRDRL寄存器的数据格式示例。

在异步模式下，将0写入FRDRH寄存器的MPB位。对应于数据长度的数据被写入FRDRH和FRDRL。未使用的位写为0。按从FRDRH到FRDRL的顺序读取。如果软件读取FRDRL，则

SCI updates FER, PER, and receive data (RDAT[8:0]) in the FRDRL register with the next data. The flags RDF, ORER, and DR in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

Note: 0 is always read for MPB bit (FRDRH[1])
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRH[7] bit is read as an indefinite value

Figure 30.25 Data format stored in FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and, when it detects a start bit, the SCI performs internal synchronization, stores receive data in the RSR register.
3. If the multi-processor communications function is enabled (SMR.MP = 1), see section 30.4.2. Multi-Processor Serial Data Reception. If the address match function (data compare match function) is enabled (DCCR.DCME = 1), the SCI cannot detect a parity or framing error as receive data are skipped (discarded) until the SCI detects a match between the receive data and the data for comparison (CDR.CMPD*1).
4. If the SCI detects an address match, the DCCR.DCME bit is automatically cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt*2 request is generated. To enable the generation of an SCIn_RXI interrupt request, set the SCR.RIE bit to 1. The compared receive data are not stored in the RDR register*3. The SSR.RDRF flag remains 0.
5. If the SCI detects a framing error in the receive data for which an address match was detected, the DCCR.DFER flag is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER flag becomes 1. To enable the generation of an SCIn_ERI interrupt request, set the SCR.RIE bit to 1.
6. If a framing or a parity error is detected (the DCCR.DFER flag or DCCR.DPER flag is 1) in the SCIn_AM interrupt handling routine, set the DCCR.DFER and DCCR.DPER flags to 0 and set the DCCR.DCME bit to 1 to enable the address match function again. If neither a framing nor a parity error has been detected (the DCCR.DFER and DCCR.DPER flags are 0), set the DCCR.DCMF flag to 0. See Figure 30.9.
7. If an overrun error occurs during normal communications, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the FRDRL*3 register.
8. If a parity error is detected, the PER flag and receive data are transferred to the FRDRL*3 register. If the SCR.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
9. If a framing error is detected, the FER flag and receive data are transferred to the FRDRL*3 register. If the SCR.RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
10. After a framing error is detected and when SCI detects that the continuous receive data is zero for one frame, reception stops.
11. When the amount of data stored in the FRDRL register falls below the specified receive triggering number, and the next data is not received after 15 ETUs from the last stop bit in asynchronous mode, the SSR_FIFO.DR flag is set to 1. When the SCR.RIE bit is 1 and the FCR.DRES bit is 0, the SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.

SCI使用下一个数据更新FRDRL寄存器中的FER、PER和接收数据(RDAT[8:0])。标志RDF、ORER和FRDRH寄存器中的DR始终反映SSR_FIFO寄存器中的相关标志。

数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8位接收数据							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9位接收数据								

Note: MPB位(FRDRH[1])始终读取0当数据长度为7位时，FRRDH[0]和FRDRL[7]始终读取0
当数据长度为8位时，FRRDH[0]总是读取0
FRDRH[7]位被读取为不定值

Figure 30.25 存储在FRDRH和FRDRL中的数据格式，选择了FIFO

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。

2.SCI监视通信线路，当它检测到一个起始位时，SCI执行内部同步，将接收数据存储在RSR寄存器中。

3.如果启用了多处理器通信功能（SMR.MP=1），请参见第30.4.2节。多处理器串行数据接收。如果地址匹配功能（数据比较匹配功能）被启用（DCCR.DCME=1），SCI无法检测奇偶校验或帧错误，因为接收数据被跳过（丢弃），直到SCI检测到接收数据与用于比较的数据（CDR.CMPD*1）。

4.如果SCI检测到地址匹配，DCCR.DCME位自动清零，DCCR.DCMF标志变为1，并产生SCIn_AM中断*2请求。要启用SCIn_RXI中断请求的生成，请将SCR.RIE位设置为1。比较的接收数据不存储在RDR寄存器*3中。SSR.RDRF标志保持为0。

5.如果SCI在检测到地址匹配的接收数据中检测到帧错误，则DCCR.DFER标志设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER标志变为1.要启用SCIn_ERI中断请求的生成，请将SCR.RIE位设置为1。

6.如果在SCIn_AM中断处理例程中检测到成帧或奇偶校验错误（DCCR.DFER标志或DCCR.DPER标志为1），则将DCCR.DFER和DCCR.DPER标志设置为0，并设置DCCR.DCME位为1以再次启用地址匹配功能。如果既没有检测到成帧错误也没有检测到奇偶校验错误（DCCR.DFER和DCCR.DPER标志为0），将DCCR.DCMF标志设置为0。参见图30.9。

7.如果在正常通信过程中发生溢出错误，则SSR_FIFO.ORER标志设置为1。如果SCR中的SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到FRDRL*3寄存器。

8.如果检测到奇偶校验错误，则将PER标志和接收数据传送到FRDRL*3寄存器。如果SCR.RIE位设置为1，则会产生SCIn_ERI中断请求。

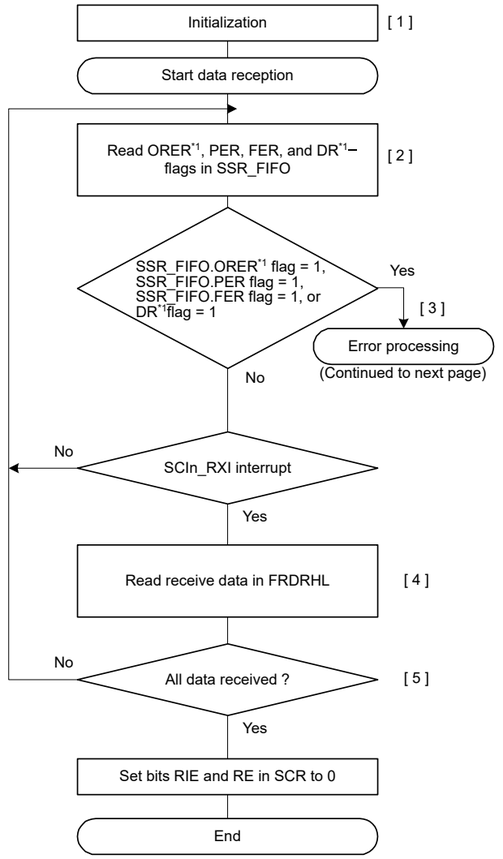
9.如果检测到帧错误，则将FER标志和接收数据传送到FRDRL*3寄存器。如果SCR.RIE位设置为1，则会产生SCIn_ERI中断请求。

10、检测到帧错误后，当SCI检测到连续接收数据一帧为零时，停止接收。

11.当FRDRL寄存器中存储的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU后没有接收到下一个数据时，SSR_FIFO.DR标志设置为1。SCR.RIE位为1，FCR.DRES位为0，SCI产生一个SCIn_RXI中断请求。当FCR.DRES位为1时，SCI产生一个SCIn_ERI中断请求。

12. When reception finishes successfully, receive data is transferred to the FRDRL*3 register. The RDF bit is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the FRDRL*4 register in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*5 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. One of three lengths is selected for the target for comparison: CMPD[6:0] is for 7-bit length, CMPD[7:0] is for 8-bit length, and CMPD[8:0] is for 9-bit length.
Note 2. As no interrupt enable bit is assigned to the SCIn_AM interrupt, an interrupt request is generated by setting the DCCR.DCMF to 1.
Note 3. Only read data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 4. Read data in order from FRDRH and FRDRL when 9-bit data length is selected.
Note 5. The SCI only checks for update to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.



[1] SCI initialization:
Set data reception.

[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON flag. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if ORER*1 flag is set to 1. The reception operation is continuous, even if the FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The receive data stored in the FRDRHL register is read until the number of stored data is below the FCR.RTRG value. Confirm the number of the reception data in the FIFO by reading FDR.R.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF flag and DR flag to 0.
The FRDRHL data can also be read by activating the DMA or DTC. The RDF flag is cleared automatically in this case, so do not write to the RDF flag.

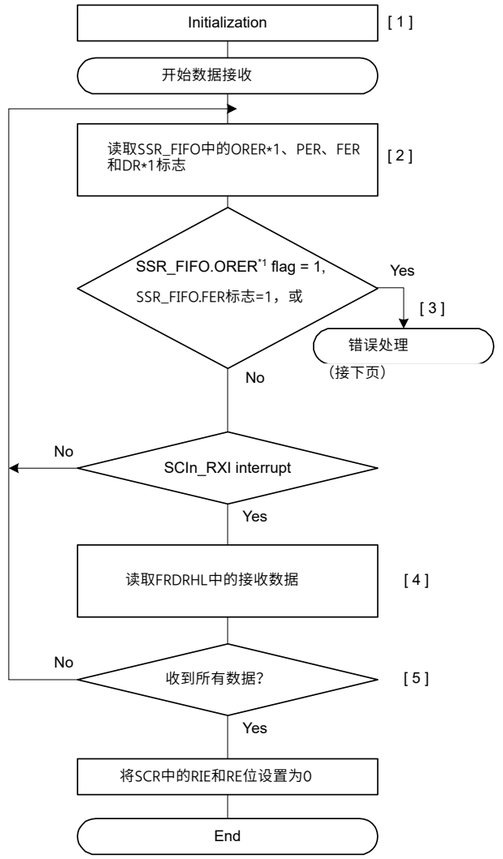
Note 1. Can be read in the FRDRHL.ORER and DR flags.

Figure 30.26 Example flow of serial reception in asynchronous mode with FIFO selected and Address Matching Enabled (1)

12.接收成功后，接收数据被传送到FRRDL*3寄存器。当写入FRDRHL的接收数据量等于或大于指定的接收触发数时，RDF位设置为1。如果SCR中的SCR.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理程序中读取传输到FRDRL*4寄存器的接收数据来启用连续接收。如果传送到FRDRL*5的接收数据小于RTS触发数，CTSn_RTSn引脚输出低电平。

注1.选择三个长度之一作为目标进行比较：CMPD[6:0]为7位长度，CMPD[7:0]为8位长度，CMPD[8:0]为9位长度。

注2.由于没有为SCIn_AM中断分配中断使能位，因此通过设置
DCCR.DCMF to 1.
注3.选择9位数据长度时，仅读取FRDRH和FRDRL寄存器中的数据。
注4.选择9位数据长度时，按FRDRH和FRDRL的顺序读取数据。
Note5.TheSCIonlychecksforupdatetotheFRDRLregisterandnottotheFRDRHregisterwhen9-bitdatalengthisselected.



[1]SCI初始化：设置数据接收。

[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。可以通过读取SPTR.RXDMON标志来检测中断。通过读取SSR_FIFO中的ORER*1、PER、DR*1和FER标志来识别错误。执行适当的错误处理后，请务必将ORER*1标志设置为0。如果ORER*1标志设置为1，则无法恢复接收。接收操作是连续的，即使FER=1或PER=1或DR*1=1。

[4]在SCIn_RXI中断处理程序中读取FRDRHL中的接收数据。读取存储在FRDRHL寄存器中的接收数据，直到存储的数据数量低于FCR.RTRG值。通过读取FDR.R来确认FIFO中接收数据的数量。

[5]串行接收继续程序：
要继续串行接收，在发生溢出错误之前，在SCIn_RXI中断处理程序中从FRDRHL读取数据并将RDF标志和DR标志清除为0。也可以通过激活DMA或DTC来读取FRDRHL数据。在这种情况下，RDF标志会自动清除，因此不要写入RDF标志。

注1.可以在FRDRHL.ORER和DR标志中读取。

Figure 30.26 选择FIFO和地址的异步模式下串行接收示例流程匹配启用(1)

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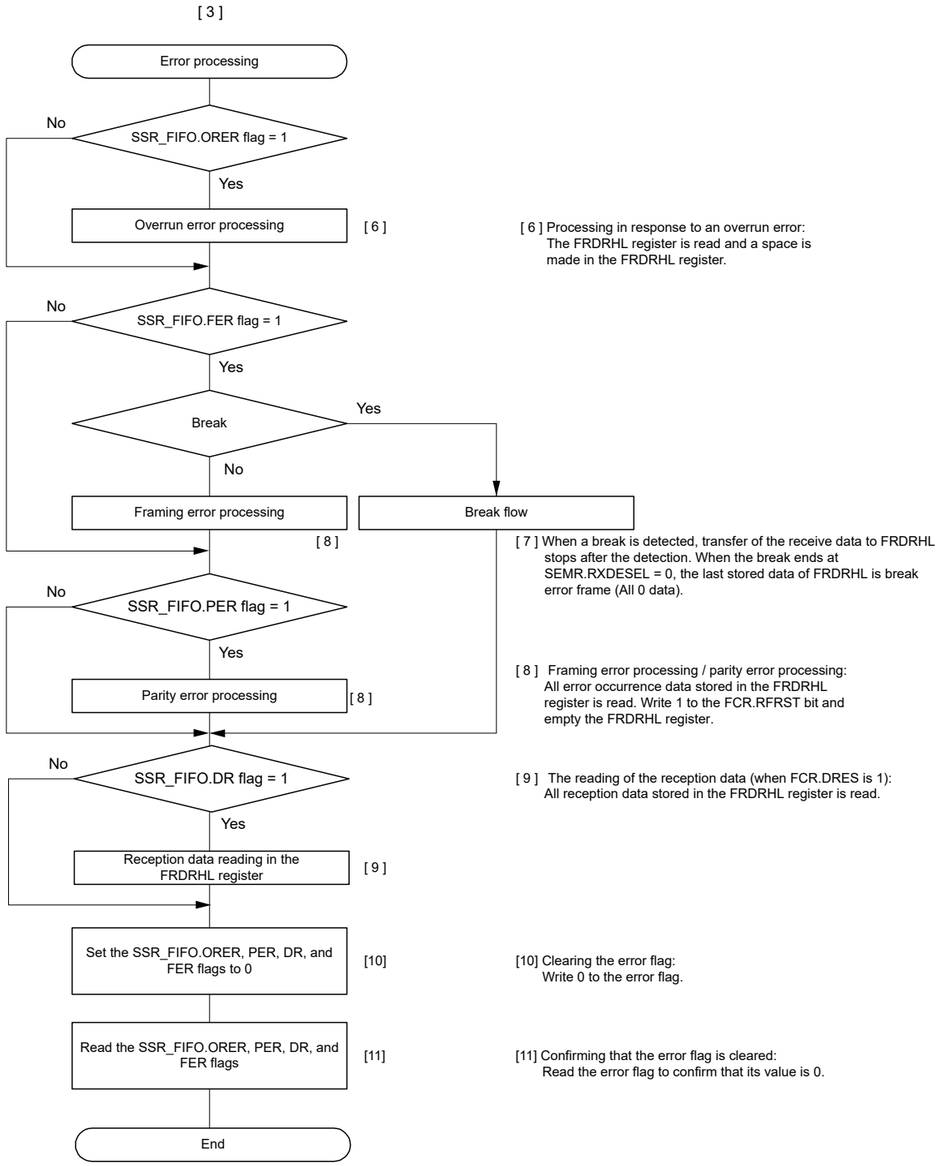


[6] Processing in response to an overrun error:
The FRDRHL register is read and a space is made in the FRDRHL register.

[7] When a break is detected, transfer of the receive data to FRDRHL stops after the detection. When the break ends at SEMR.RXDESEL = 0, the last stored data of FRDRHL is break error frame (All 0 data).

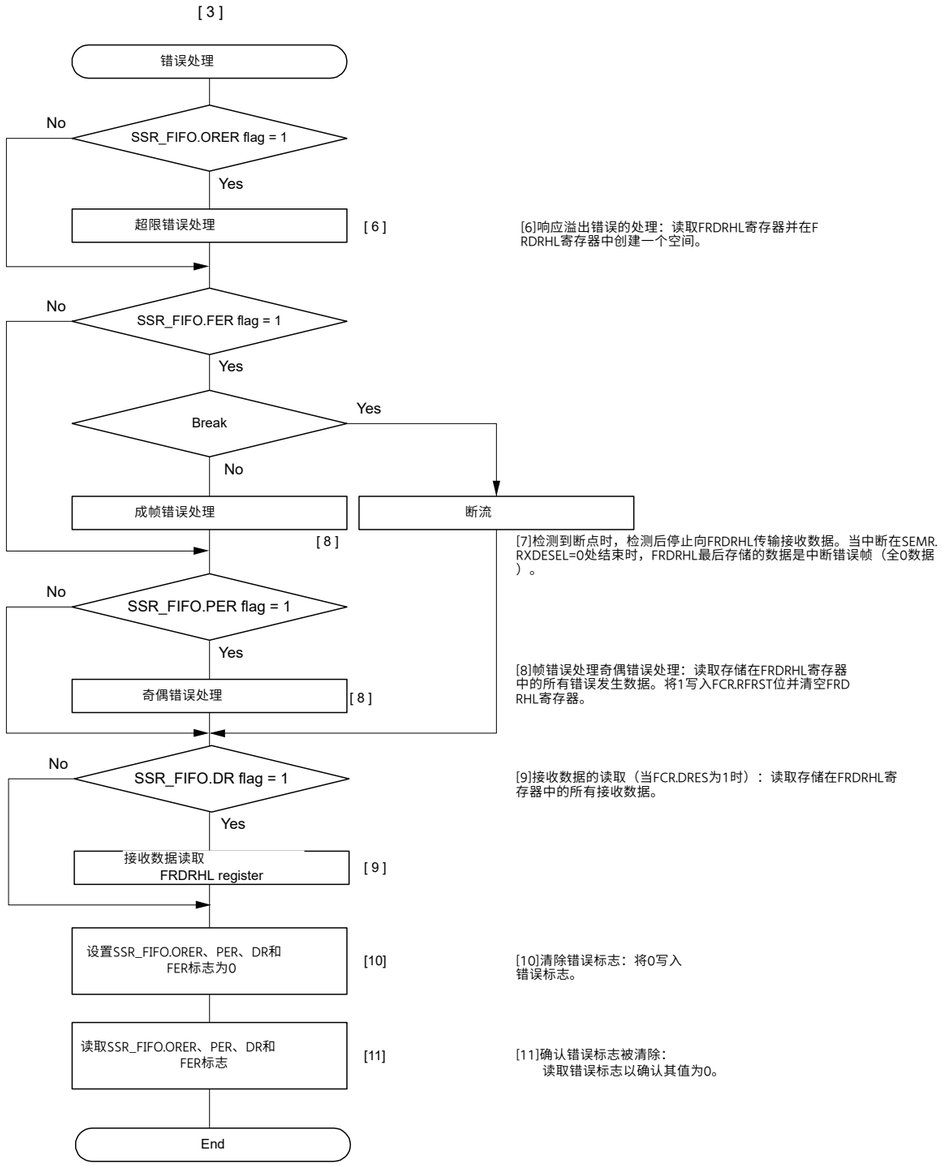
[8] Framing error processing / parity error processing:
All error occurrence data stored in the FRDRHL register is read. Write 1 to the FCR.RFRST bit and empty the FRDRHL register.

[9] The reading of the reception data (when FCR.DRES is 1):
All reception data stored in the FRDRHL register is read.

[10] Clearing the error flag:
Write 0 to the error flag.

[11] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 30.27 Example flow of serial reception in asynchronous mode with FIFO selected Address Matching Disabled (2)



[6]响应溢出错误的处理：读取FRDRHL寄存器并在FRDRHL寄存器中创建一个空间。

[7]检测到断点时，检测后停止向FRDRHL传输接收数据。当中断在SEMR.RXDESEL=0处结束时，FRDRHL最后存储的数据是中断错误帧（全0数据）。

[8]帧错误处理奇偶错误处理：读取存储在FRDRHL寄存器中的所有错误发生数据。将1写入FCR.RFRST位并清空FRDRHL寄存器。

[9]接收数据的读取（当FCR.DRES为1时）：读取存储在FRDRHL寄存器中的所有接收数据。

[10]清除错误标志：将0写入错误标志。

[11]确认错误标志被清除：
读取错误标志以确认其值为0。

Figure 30.27 使用FIFO选择地址匹配的异步模式串行接收示例流程 Disabled (2)

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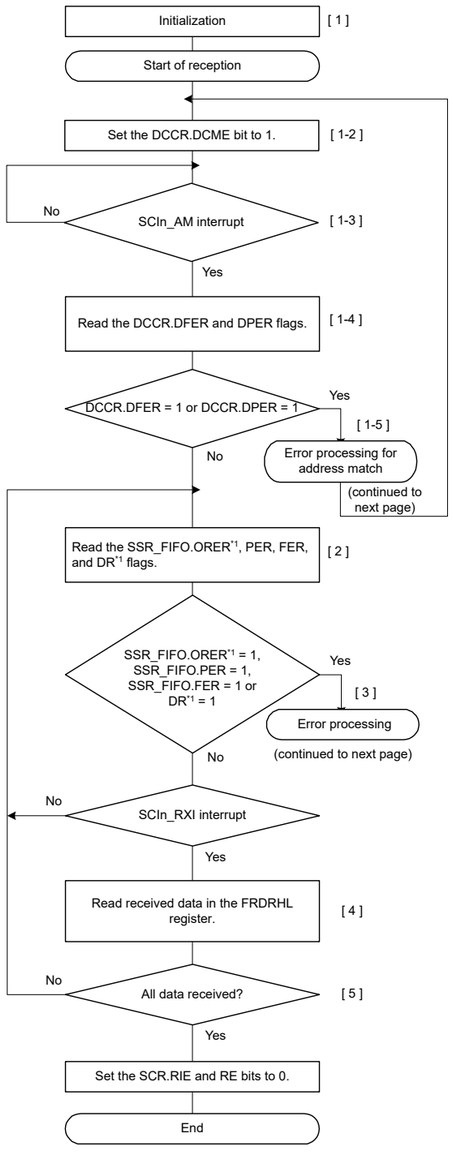


[1] SCI initialization:
Set data reception.

[1-2] Address match cycle:
Set the DCCR.DCME bit to 1 to enable address matching.

[1-3] Comparing received data and data for comparison (CDR.CMPD):
Compare receive data and comparison data.
The SCI cannot detect a parity or framing error as received data are skipped (discarded) until the SCI detects a match between the received data and data for comparison.
If the SCI detects an address match, the DCCR.DCME bit is cleared, the DCCR.DCMF flag becomes 1, and an SCIn_AM interrupt request is issued.

[1-4] [1-5] Reception error processing:
An error is identified by reading the DFER or DPER flag in DCCR from within the SCIn_AM interrupt handling routine.
After appropriate handling of the error, set both the DFER and DPER flags to 0.
If either of these flags is set to 1, address matching cannot be resumed.

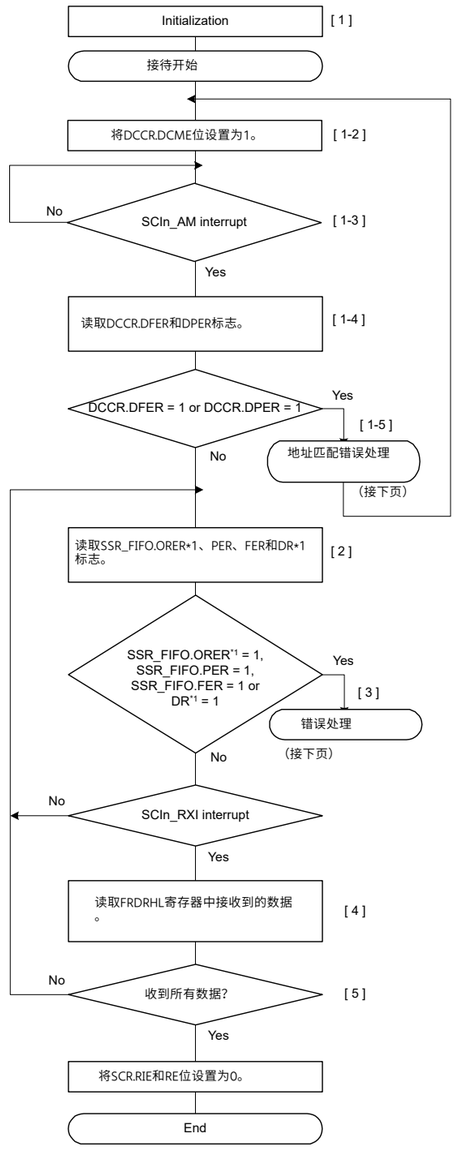
[2] [3] Reception error processing and break detection:
When a reception error occurs, an SCIn_ERI interrupt is generated.
A break is identified by reading SPTR.RXDMON.
The error is identified by reading each among the SSR_FIFO.ORER*1, PER, FER, and DR*1 flags.
After appropriate handling of the error, set the ORER*1 flag to 0.
If the ORER*1 flag remains 1, reception cannot be resumed.
The reception operation is continuous, even if the FER = 1, PER = 1 or DR*1 = 1.

[4] Reading the received data in the FRDRHL register from within the SCIn_RXI interrupt handling routine:
The received data stored in the FRDRHL register are read until the amount of stored data is less than the value of the FCR.RTRG[3:0] bits.
Confirm the number of received data in the FIFO with the value of the FDR.R[4:0] bits.

[5] Serial reception continuation procedure:
To continue with serial reception, read data from the FRDRHL register from within the SCIn_RXI interrupt handling routine before an overrun error occurs, and set the RDF and DR flags to 0. The data in the FRDRHL register can also be read by activating the DMAC or DTC. In this case, do not write to the RDF flag because the flag is automatically cleared.

Note 1. The FRDRHL.ORER and DR flags can also be read.

Figure 30.28 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (1)



[1]SCI初始化：设置数据接收。

[1-2]地址匹配周期：将DCCR.DCME位设置为1以启用地址匹配。

[1-3]比较接收数据和比较数据（CDR.CMPD）：比较接收数据和比较数据。
SCI无法检测奇偶校验或成帧错误，因为接收到的数据被跳过（丢弃），直到SCI检测到接收到的数据与用于比较的数据之间的匹配。如果SCI检测到地址匹配，则DCCR.DCME位被清零，

DCCR.DCMF标志变为1，并发出SCIn_AM中断请求。

[1-4][1-5]接收错误处理：通过从SCIn_AM中断处理例程中读取DCCR中的DFER或DPER标志来识别错误。正确处理错误后，将DFER和DPER标志都设置为0。如果这些标志中的任何一个设置为1，则无法恢复地址匹配。

[2][3]接收错误处理和中断检测：当发生接收错误时，会产生SCIn_ERI中断。
通过读取SPTR.RXDMON来识别中断。
通过读取SSR_FIFO.ORER*1、PER、FER和DR*1标志。
正确处理错误后，将ORER*1标志设置为0。
如果ORER*1标志保持为1，则无法恢复接收。
接收操作是连续的，即使FER=1、PER=1或DR*1 = 1.

[4]从SCIn_RXI中断处理程序中读取FRDRHL寄存器中的接收数据：读取存储在FRDRHL寄存器中的接收数据，直到存储的数据量小于FCR.RTRG[3:0]的值位。确认FIFO中接收到的数据数量与FDR.R[4:0] bits.

[5]串行接收继续过程：要继续串行接收，在溢出错误发生之前从SCIn_RXI中断处理程序中读取FRDRHL寄存器中的数据，并将RDF和DR标志设置为0。FRDRHL寄存器中的数据可以也可以通过激活DMAC或DTC来读取。在这种情况下，不要写入RDF标志，因为该标志会自动清除。

注1.也可以读取FRDRHL.ORER和DR标志。

Figure 30.28 异步模式下串行接收的示例流程图（FIFO选择和地址Matching Enabled) (1)

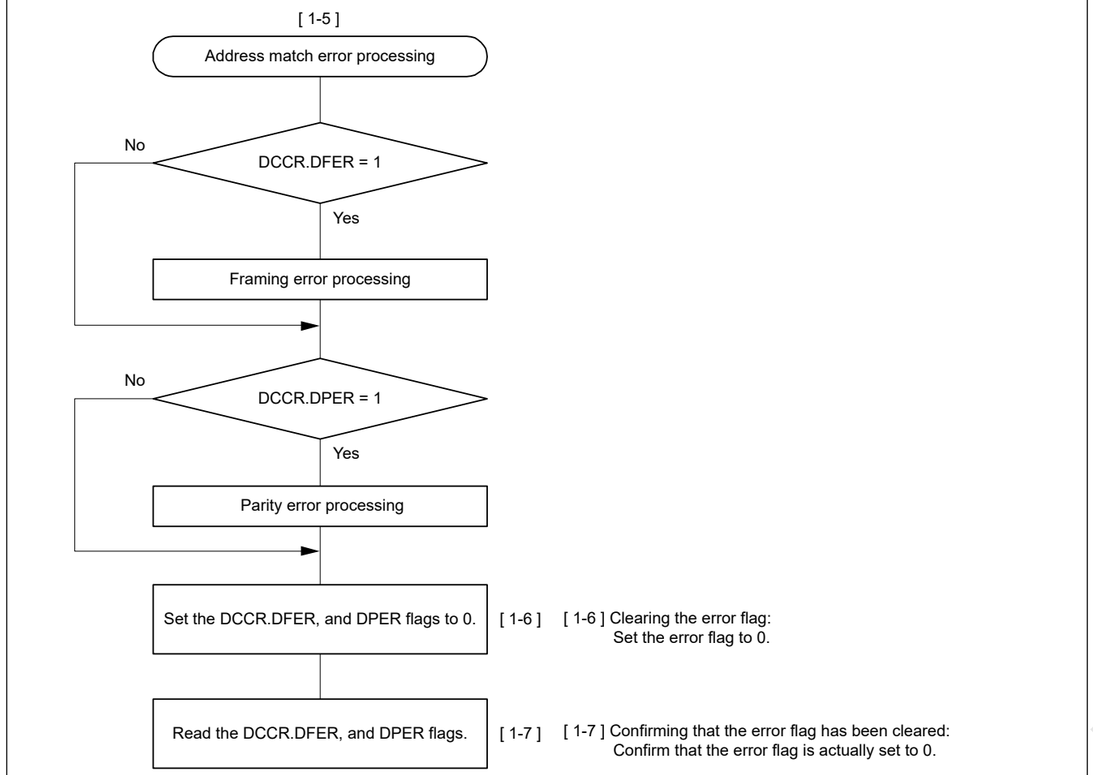


Figure 30.29 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (2)

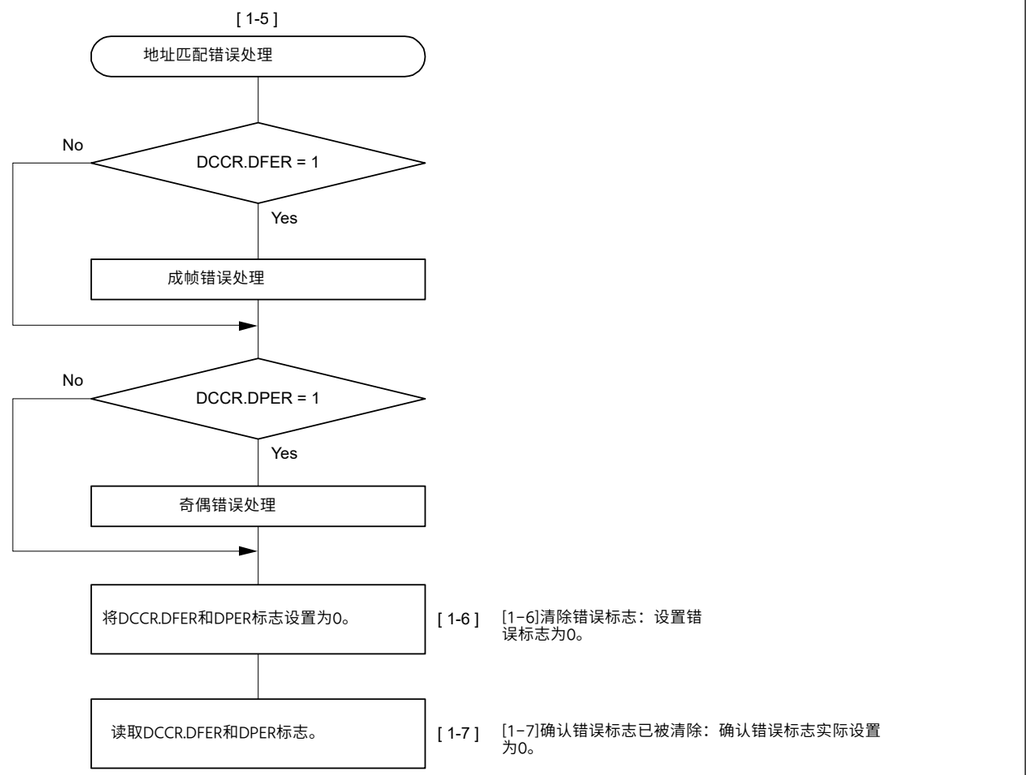
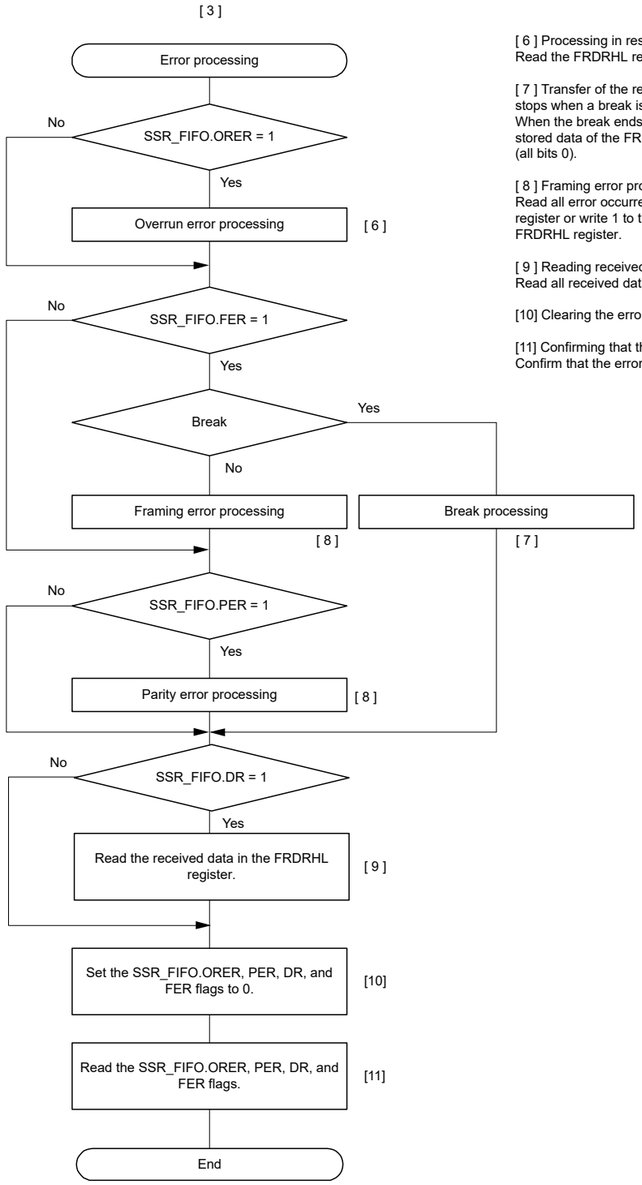


Figure 30.29 异步模式下串行接收的示例流程图（FIFO选择和地址 Matching Enabled) (2)



[6] Processing in response to an overrun error:
Read the FRDRHL register to empty it.

[7] Transfer of the received data to the FRDRHL register stops when a break is detected.
When the break ends at SEMR.RXDESEL = 0, the last stored data of the FRDRHL register is a break error frame (all bits 0).

[8] Framing error processing/parity error processing:
Read all error occurrence data stored in the FRDRHL register or write 1 to the FCR.RFRST bit to empty the FRDRHL register.

[9] Reading received data when FCR.DRES is 1:
Read all received data stored in the FRDRHL register.

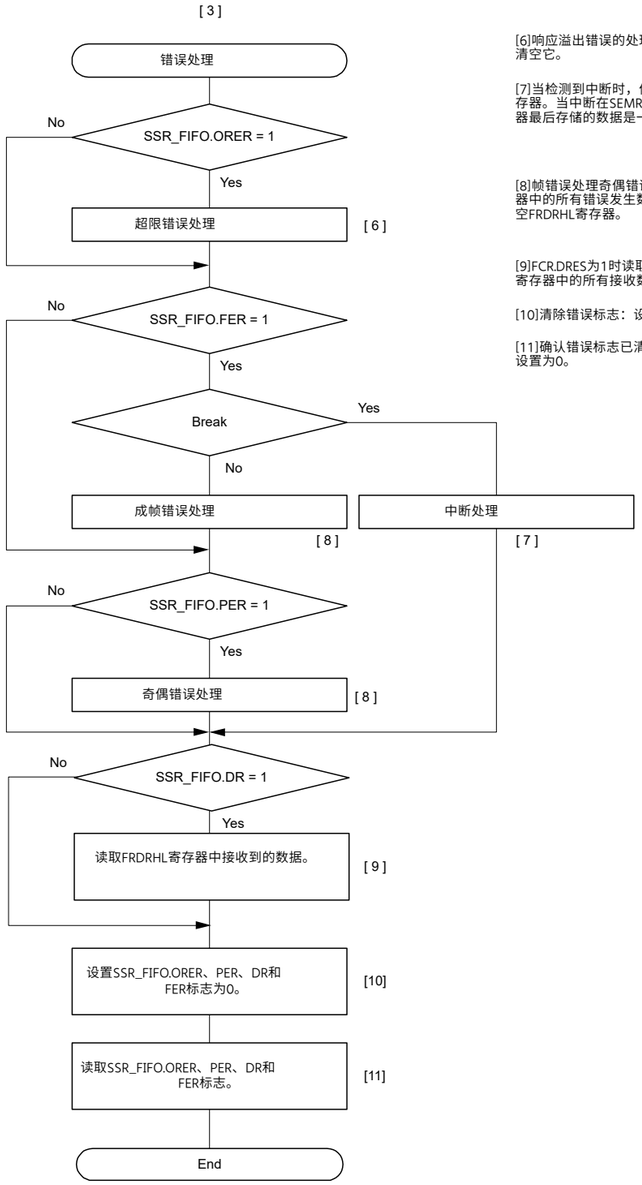
[10] Clearing the error flag: Set the error flag to 0.

[11] Confirming that the error flag is cleared:
Confirm that the error flag is actually set to 0.

Figure 30.30 Example Flowchart of Serial Reception in Asynchronous Mode (FIFO Selected and Address Matching Enabled) (3)

30.3.10 The function of adjust receive sampling timing (Asynchronous Mode)

When there is the difference between the rising transfer time and the falling transfer time through a photo coupler, the receive sampling timing at middle of bit affects the reception margin. In this case, the receive sampling timing is able to adjust from the middle of bit to the optimum timing by using this function.



[6]响应溢出错误的处理：读取FRDRHL寄存器以清空它。

[7]当检测到中断时，停止将接收到的数据传输到FRDRHL寄存器。当中断在SEMR.RXDESEL=0处结束时，FRDRHL寄存器最后存储的数据是一个中断错误帧（所有位为0）。

[8]帧错误处理奇偶错误处理：读取存储在FRDRHL寄存器中的所有错误发生数据或将1写入FCR.RFRST位以清空FRDRHL寄存器。

[9]FCR.DRES为1时读取接收数据：读取存储在FRDRHL寄存器中的所有接收数据。

[10]清除错误标志：设置错误标志为0。

[11]确认错误标志已清除：确认错误标志实际设置为0。

Figure 30.30 异步模式下串行接收的示例流程图（FIFO选择和地址Matching Enabled) (3)

30.3.10 调整接收采样定时功能（异步模式）

当通过光电耦合器的上升传输时间和下降传输时间之间存在差异时，位中间的接收采样时间会影响接收裕度。在这种情况下，接收采样时序可以通过使用该功能从比特中间调整到最佳时序。

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The receive sampling timing is adjusted from the middle of bit by following formula. And the adjustable direction is set by ACTR.AJD. You can select forward or backward from the middle of bit. When adjusting backward (ACTR.AJD = 0), substitute AJD = +1 and substitute AJD = -1 when adjusting forward (ACTR.AJD = 1).

Adjusted sampling timing = the middle of bit + AJD * (base clock * the setting calue of ACTR.AST[2:0])

The setting timing is limited by base clock cycles per 1 bit. Please refer to Table 30.31 in detail.

A reception movement image figure of the communication through a photo coupler with this function is shown in Figure 30.31, Figure 30.32 and Figure 30.33, the movement explanation of this function is shown in Figure 30.34.

Please don't use this function when there is no difference between the rising transfer time and the falling transfer time, because there is a possibility of deteriorating the reception margin.

Table 30.31 The acceptable value of ACTR register (asynchronous mode using internal clock)

SEMR.ABCSE	SEMR.ABCS	The number of base clock cycles/1bit	The acceptable value of ACTR	
			ACTR.AJD	ACTR.AST
1	x	6	0	000b – 010b*1
			1	
0	1	8	0	000b – 011b*1
			1	
0	0	16	0	000b – 111b
			1	

Note: x : Don't care
Note 1. When the value of ACTR.AST is over the acceptable value, sampling is done at default timing. (Adjustment of sampling is not done.)

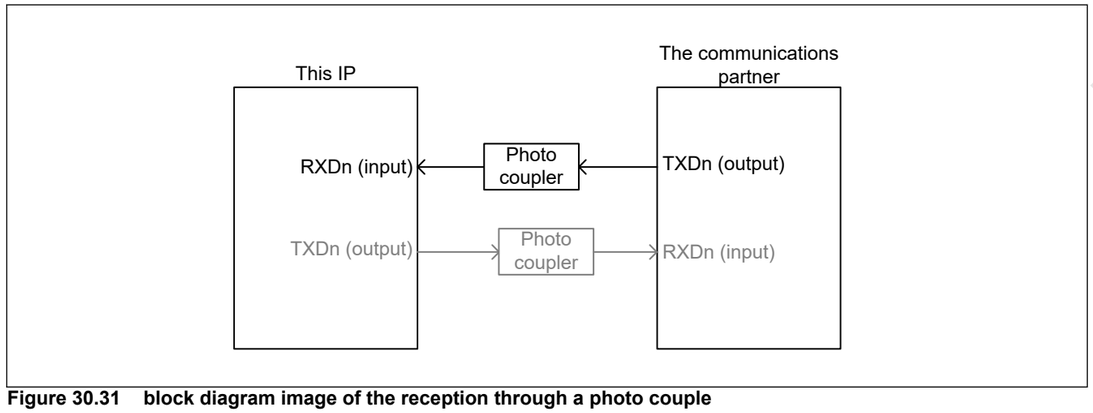


Figure 30.31 block diagram image of the reception through a photo couple

接收采样定时通过以下公式从位中间调整。可调方向由ACTR.AJD。您可以从位的中间选择向前或向后。向后调整时(ACTR.AJD=0)，代入AJD=+1，向前调整时代入AJD=−1(ACTR.AJD=1)。

调整后的采样时间=位中间值+AJD*(基准时钟*ACTR.AST[2:0]的设置值)

设置时序受限于每1位的基本时钟周期。详见表30.31。

图30.31、图30.32、图30.33为具有该功能的光耦通信的接收动作图，该功能的动作说明如图30.34所示。

请不要在上升传输时间和下降传输时间没有差异时使用此功能，因为有可能恶化接收余量。

Table 30.31 ACTR寄存器的可接受值（使用内部时钟的异步模式）

SEMR.ABCSE	SEMR.ABCS	基本时钟周期数1bit	ACTR的可接受值	
			ACTR.AJD	ACTR.AST
1	x	6	0	000b – 010b*1
			1	
0	1	8	0	000b – 011b*1
			1	
0	0	16	0	000b – 111b
			1	

Note: x : Don't care
注1.当ACTR.AST的值超过可接受的值时，将在默认时间进行采样。（未进行采样调整。）

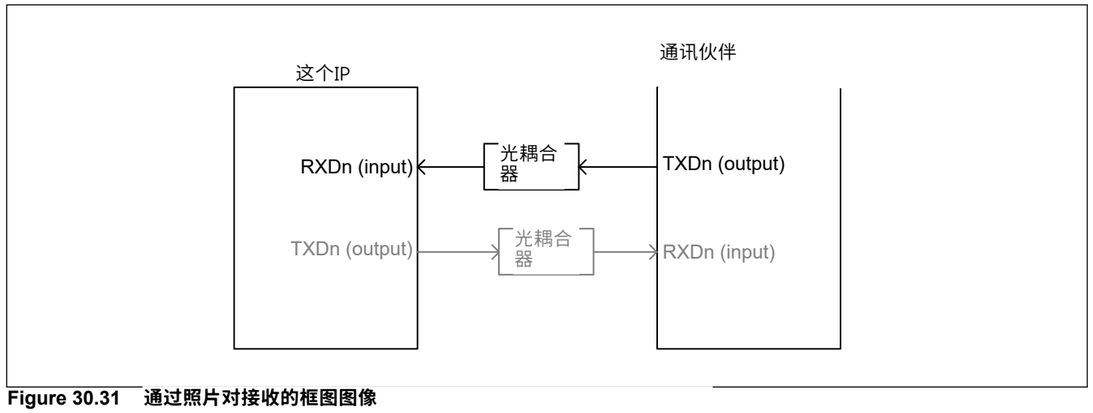
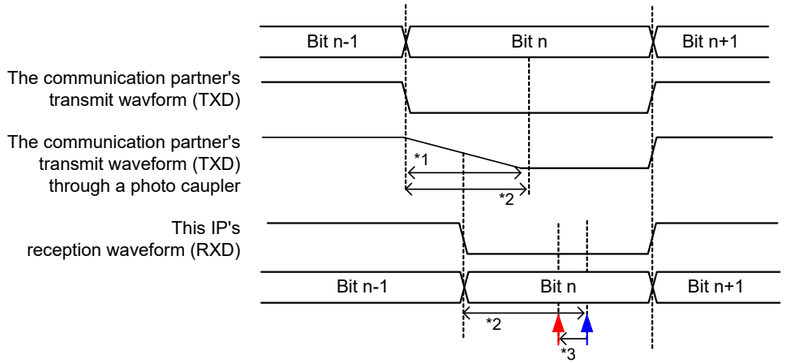


Figure 30.31 通过照片对接收的框图图像

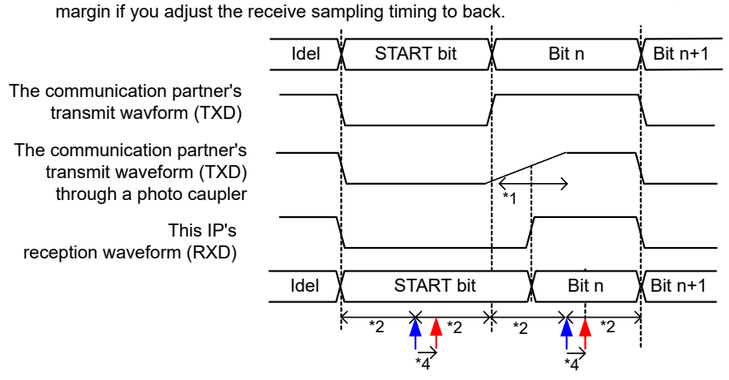
(a) In the case of the falling transfer time >> rising transfer time

The falling edge of reception waveform is made dull like following chart.
In this case, you can sampling at the middle of bit if you adjust the receive sampling timing to forward (AJD=1'b1).



(b) In the case of the falling transfer time << rising transfer time

The rising edge of reception waveform is made dull like following chart.
So, the reception margin of communications partner will be bad. In this case, you can improve the reception margin if you adjust the receive sampling timing to back.



The receive sampling timing when unadjusted (middle of bit)

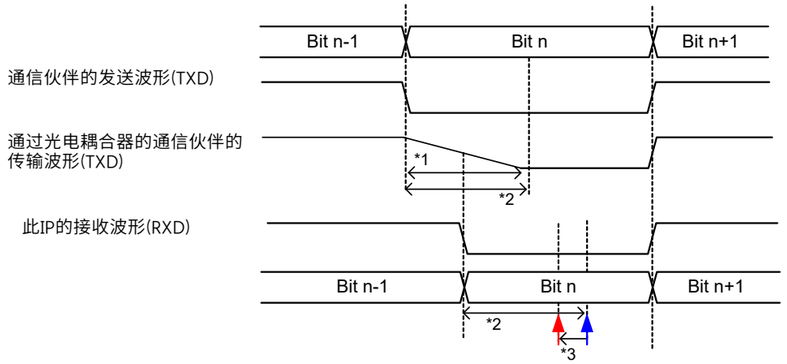
The adjusted receive sampling timing

Note: This waveform shows the operation image of adjustment receive sampling timing.
Note 1. The dull period by a photo coupler
Note 2. Bit center timing at set communication rate
Note 3. When ACTR.AJD is 1, the receive sampling timing is shifted to forward by the setting value of ACTR.AST[2:0].
Note 4. When ACTR.AJD is 0, the Receive sampling timing is shifted to backward by the setting value of ACTR.AST[2:0].

Figure 30.32 The reception movement image figure of the communication through a photo coupler

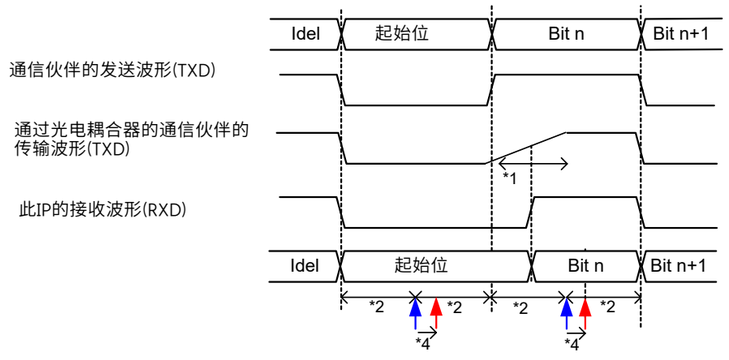
(a)在下降传输时间>>上升传输时间的情况下

接收波形的下降沿变钝，如下图所示。
在这种情况下，如果将接收采样时序调整为正向（AJD=1'b1），则可以在位中间采样。



(b)在下降传输时间<<上升传输时间的情况下

接收波形的上升沿变钝，如下图所示。
因此，通信伙伴的接收幅度会很差。在这种情况下，如果您将接收采样定时向后调整，您可以提高接收裕度。



未调整时的接收采样时序（位中间）

调整后的接收采样时序

Note: 该波形显示了调整接收采样定时的操作图像。
注1.光电耦合器的无光泽期
注2.设定通信速率下的位中心时序
注3.当ACTR.AJD为1时，接收采样定时向前移动ACTR.AST[2:0]的设置值。
注4.当ACTR.AJD为0时，接收采样时序向后移动ACTR.AST[2:0]的设置值。

Figure 30.32 通过光电耦合器进行通信的接收运动图像图

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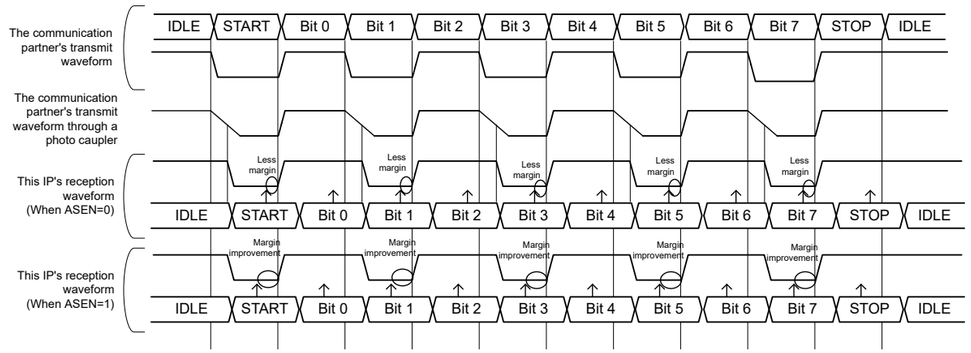
In the case of the falling transfer time >> the rising transfer time by a photo caupler.



In the case of the falling transfer time << the rising transfer time by a photo caupler.

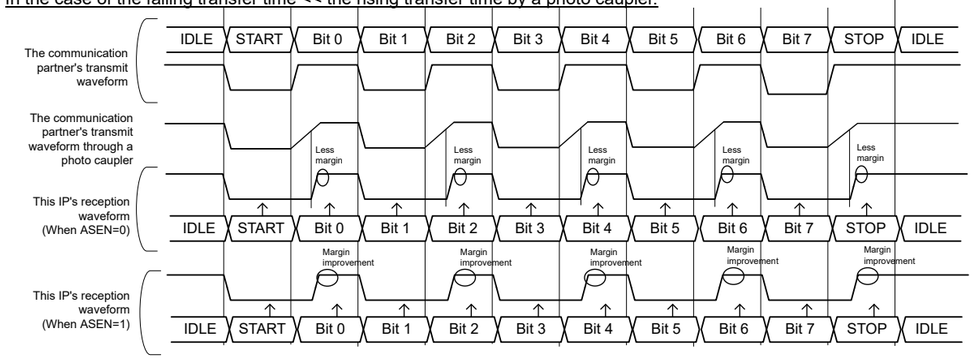
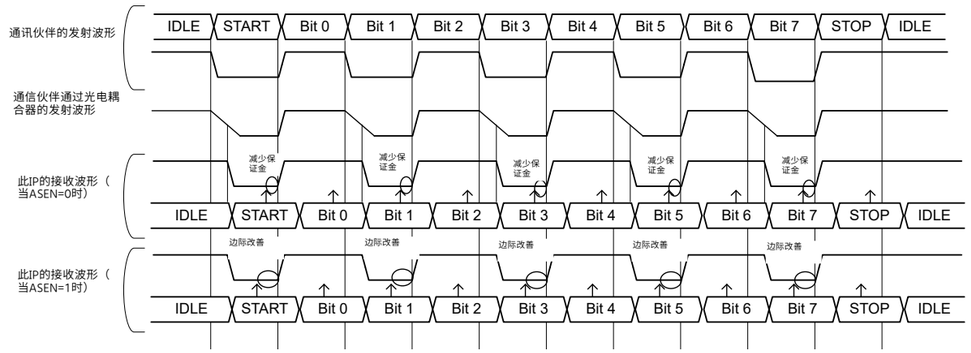


Figure 30.33 Improvement of reception margin when receive sampling timing adjustment function Image

在下降传输时间的情况下>>通过光电卡勒的上升传输时间。



在下降传输时间<<光电耦合器的上升传输时间的情况下。

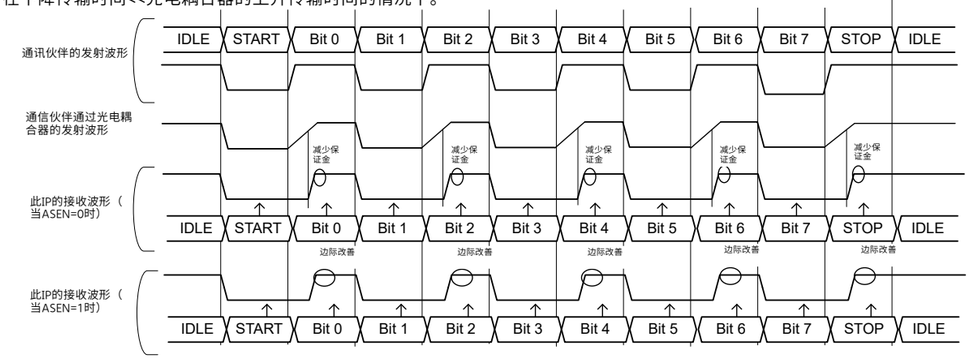


Figure 30.33 接收采样定时调整功能时的接收余量改善Image

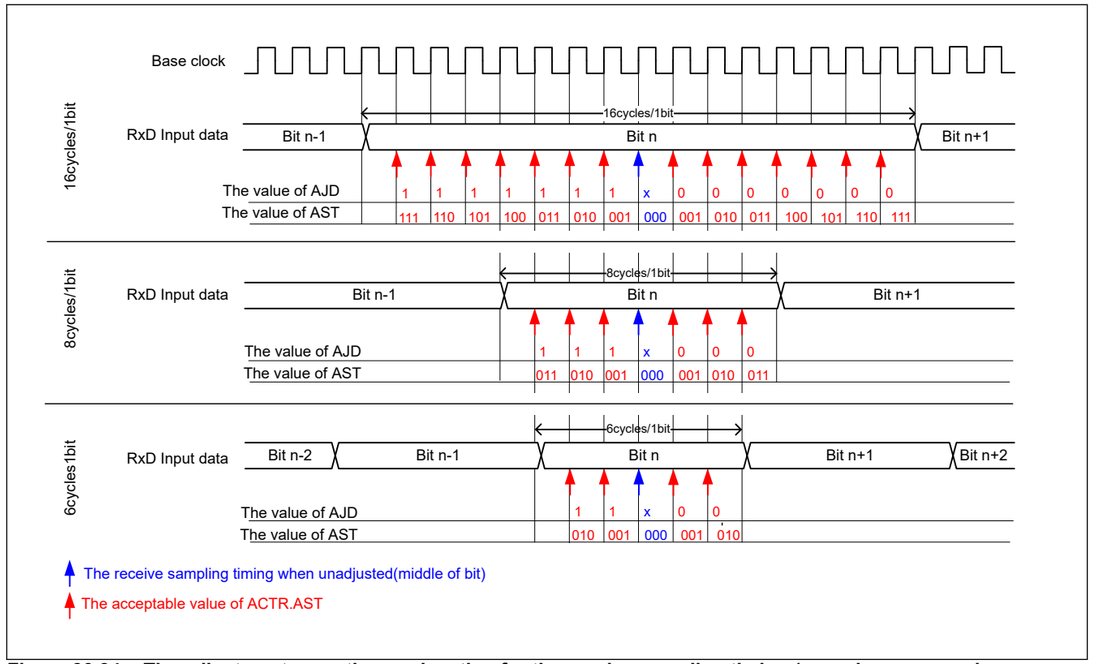


Figure 30.34 The adjustment operation explanation for the receive sampling timing (asynchronous mode using internal clock)

30.3.11 The function of adjust transmit timing (Asynchronous Mode)

In communication via a photo coupler or the like, when either the rising or falling transition time of the TXD output signal is long, then a communication partner receive dulled waveform. In this case, the reception margin may be affected.

In these cases, make a communication partner to be sampling at middle of bit using the function of adjust transmit timing.

When SPTR.ATEN is 1, this function can adjust the edge timing at the timing calculated by the following formula for the edge set with ACTR.AET.

The adjustment edge timing = the base clock * ACTR.ATT[2:0]

In addition, the upper limit of the adjustment edge timing is limited by setting the base clock cycles. Refer to Table 30.32 in details.

A transmission movement image figure of the communication through a photo coupler with this function is shown in Figure 30.35, Figure 30.36 and Figure 30.37, the movement explanation of this function is shown in Figure 30.38 and Figure 30.39.

Please don't use this function when there is not the difference between the rising transfer time and the falling transfer time, there is a possibility of deteriorating the reception margin of a communication partner.

Table 30.32 The acceptable value of ACTR.AET and ACTR.ATT (asynchronous mode using internal clock) (1 of 2)

ABCSE	ABCS	The number of base clock cycles/1bit	The acceptable value of ACTR	
			AET	ATT[2:0]
1	x	6	0	000b – 101b
			1	
0	1	8	0	000b – 111b
			1	

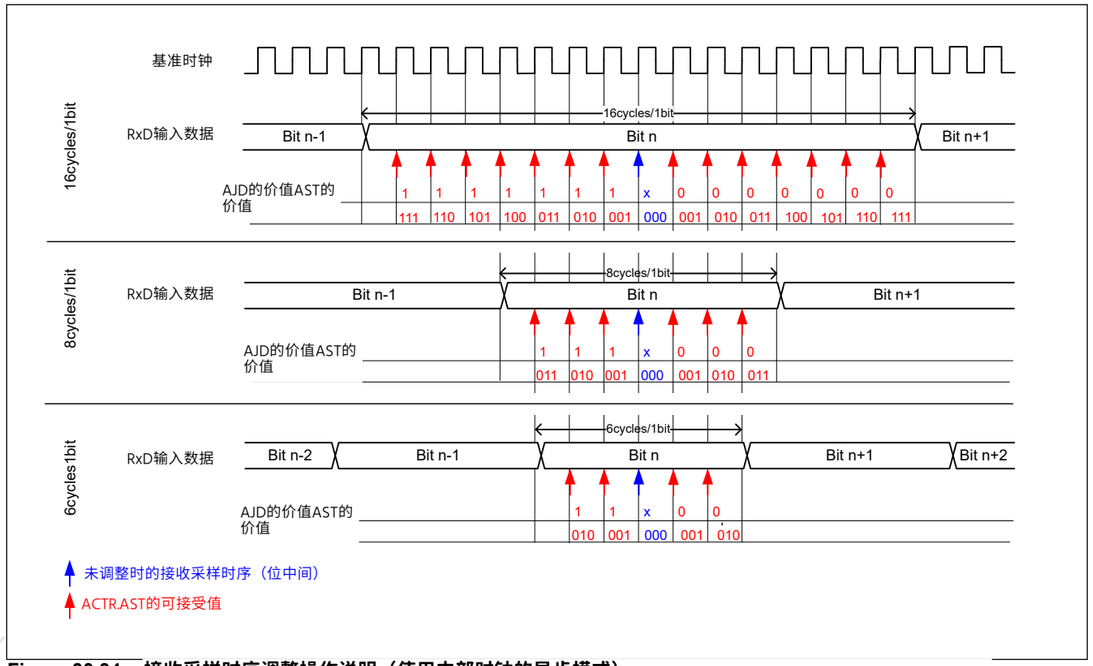


Figure 30.34 接收采样时序调整操作说明（使用内部时钟的异步模式）

30.3.11 调整发送时间的功能（异步模式）

在经由光电耦合器等的通信中，当TXD输出信号的上升或下降过渡时间较长时，通信伙伴接收到钝化的波形。在这种情况下，接收裕量可能会受到影响。

在这些情况下，使用调整发送时间的功能使通信伙伴在位中间进行采样。

当SPTR.ATEN为1时，该功能可以在ACTR.AET设置的边沿通过以下公式计算的时序调整边沿时序。

调整边沿时序=基准时钟*ACTR.ATT[2:0]

另外，调整边沿时序的上限是通过设置基本时钟周期来限制的。详见表30.32。

图30.35、图30.36、图30.37为具有该功能的光耦通信的传输动作图，该功能的动作说明如图30.38和图30.39所示。

请不要在上升传输时间和下降传输时间之间没有差异时使用此功能，这可能会降低通信伙伴的接收裕度。

Table 30.32 ACTR.AET和ACTR.ATT的可接受值（使用内部时钟的异步模式）（1of2）

ABCSE	ABCS	基本时钟周期数1bit	ACTR的可接受值	
			AET	ATT[2:0]
1	x	6	0	000b – 101b
			1	
0	1	8	0	000b – 111b
			1	

Table 30.32 The acceptable value of ACTR.AET and ACTR.ATT (asynchronous mode using internal clock) (2 of 2)

ABCSE	ABCS	The number of base clock cycles/1bit	The acceptable value of ACTR	
			AET	ATT[2:0]
0	0	16	0	000b – 111b
			1	

Note: x : Don't care
Note: When the value of ACTR.AET/ATT is out of the acceptable value, this SCI module doesn't adjust transmit timing.

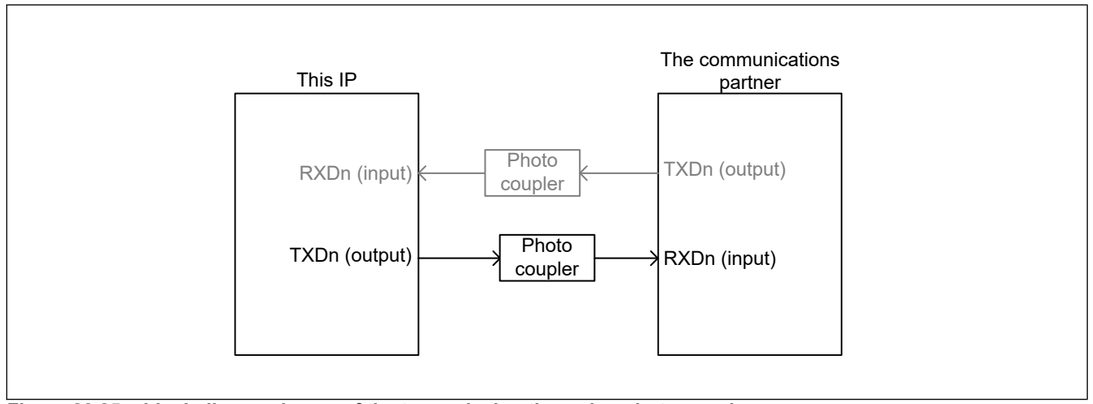


Figure 30.35 block diagram image of the transmission through a photo coupler

Table 30.32 ACTR.AET和ACTR.ATT的可接受值（使用内部时钟的异步模式）(2of2)

ABCSE	ABCS	基本时钟周期数1bit	ACTR的可接受值	
			AET	ATT[2:0]
0	0	16	0	000b – 111b
			1	

Note: x : Don't care
Note: 当ACTR.AETATT的值超出可接受的值时，该SCI模块不调整发送时序。

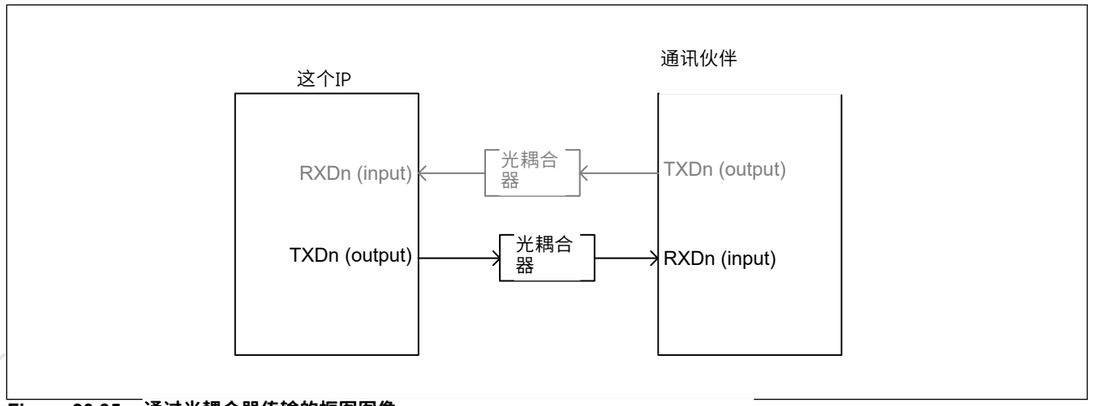


Figure 30.35 通过光耦合器传输的框图图像

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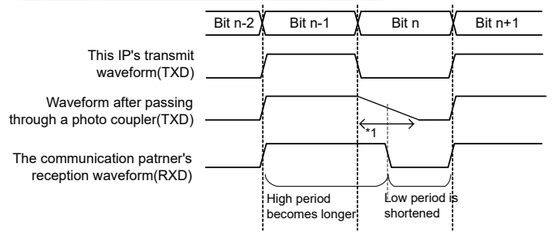
(a) In the case of the falling transfer time >> rising transfer time

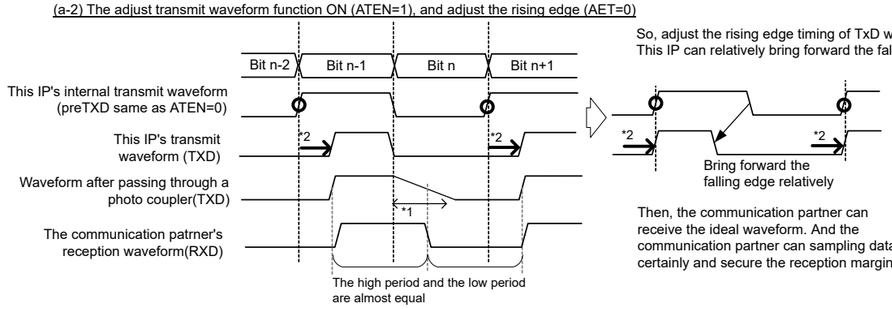
(a-1) The adjust transmit waveform function OFF (ATEN=0)



The falling edge of Transmission waveform is made dull like the figure on the left.
For the reception waveform of the communication partner, High of Bit n-1 becomes longer and Bit n Low becomes shorter.

As this kind of communication waveform collapses, there is a concern that Low value can not be sampled depending on the sampling timing of the communication partner.

(a-2) The adjust transmit waveform function ON (ATEN=1), and adjust the rising edge (AET=0)

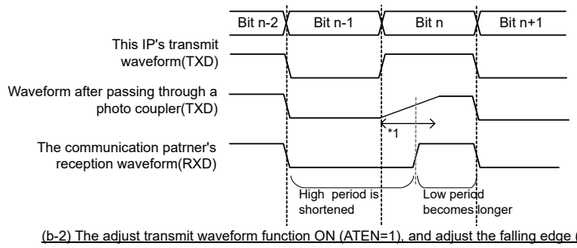


So, adjust the rising edge timing of TxD waveform.
This IP can relatively bring forward the falling edge.

Then, the communication partner can receive the ideal waveform. And the communication partner can sampling data certainly and secure the reception margin.

(b) In the case of the falling transfer time << rising transfer time

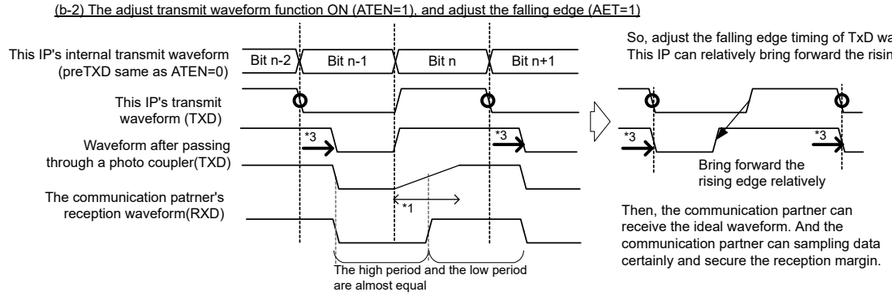
(b-1) The adjust transmit waveform function OFF (ATEN=0)



The rising edge of transmission waveform is made dull like the figure on the left.
For the reception waveform of the communication partner, Low of Bit n becomes longer and Bit n-1 High becomes shorter.

As this kind of communication waveform collapses, there is a concern that High value can not be sampled depending on the sampling timing of the communication partner.

(b-2) The adjust transmit waveform function ON (ATEN=1), and adjust the falling edge (AET=1)



So, adjust the falling edge timing of TxD waveform.
This IP can relatively bring forward the rising edge.

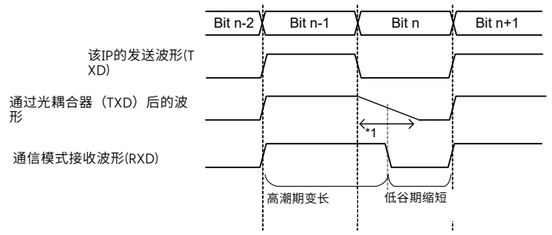
Then, the communication partner can receive the ideal waveform. And the communication partner can sampling data certainly and secure the reception margin.

Note: This waveform shows the operation image of adjustment transmit waveform.
Note 1. The dull period by a photo caupler
Note 2. When ACTR.AET is 0, the rising edge of transmit waveform timing is shifted to back by the setting value of ACTR.ATT[2:0]. This IP transmit waveform bringing forward the falling edge relatively.
Note 3. When ACTR.AET is 1, the falling edge of transmit waveform timing is shifted to back by the setting value of ACTR.ATT[2:0]. This IP transmit waveform bringing forward the rising edge relatively.

Figure 30.36 The transmission movement image figure of the communication through a photo coupler

(a)在下降传输时间>>上升传输时间的情况下

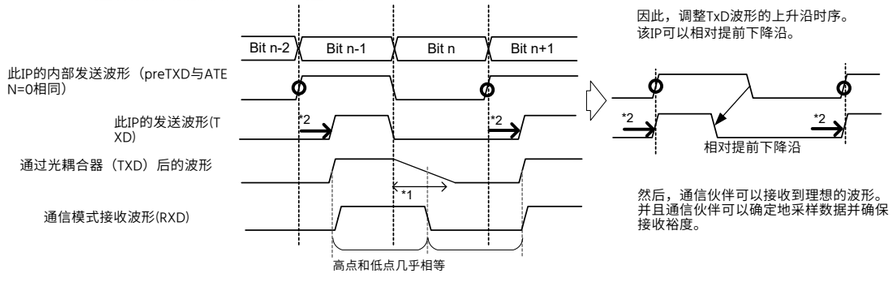
(a-1)调整发射波形功能关闭(ATEN=0)



传输波形的下降沿变暗，如左图。对于通信对方的接收波形，Bitn-1的High变长，BitnLow变短。

由于这种通信波形崩溃，根据通信对方的采样时间，有可能无法采样Low值。

(a-2)调整发射波形功能开启(ATEN=1)，调整上升沿(AET=0)

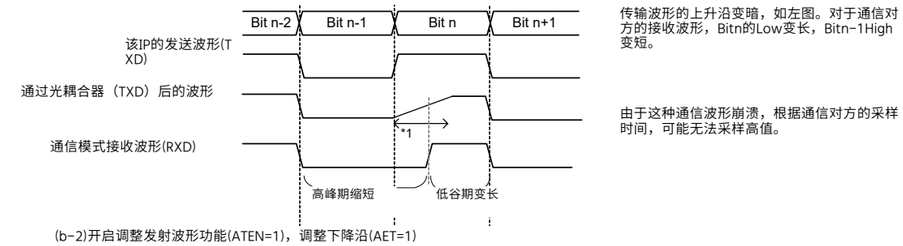


因此，调整TxD波形的上升沿时序。
该IP可以相对提前下降沿。

然后，通信伙伴可以接收到理想的波形。并且通信伙伴可以确定地采样数据并确保接收裕度。

(b)在下降传输时间<<上升传输时间的情况下

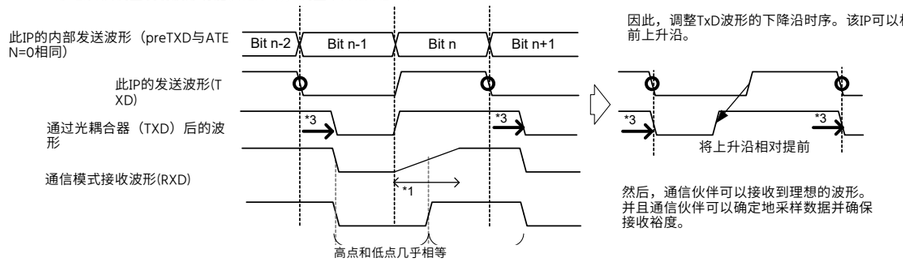
(b-1)调整发射波形功能关闭(ATEN=0)



传输波形的上升沿变暗，如左图。对于通信对方的接收波形，Bitn的Low变长，Bitn-1High变短。

由于这种通信波形崩溃，根据通信对方的采样时间，可能无法采样高值。

(b-2)开启调整发射波形功能(ATEN=1)，调整下降沿(AET=1)



因此，调整TxD波形的下降沿时序。该IP可以相对提前上升沿。

然后，通信伙伴可以接收到理想的波形。并且通信伙伴可以确定地采样数据并确保接收裕度。

Note: 该波形显示调整发射波形的操作图像。
Note1.摄影机的沉闷时期
注2.当ACTR.AET为0时，发送波形时序的上升沿后移设置值ACTR.ATT[2:0]。该IP传输波形相对提前了下降沿。
注3.当ACTR.AET为1时，发送波形时序的下降沿后移设置值ACTR.ATT[2:0]。该IP传输波形相对提前了上升沿。

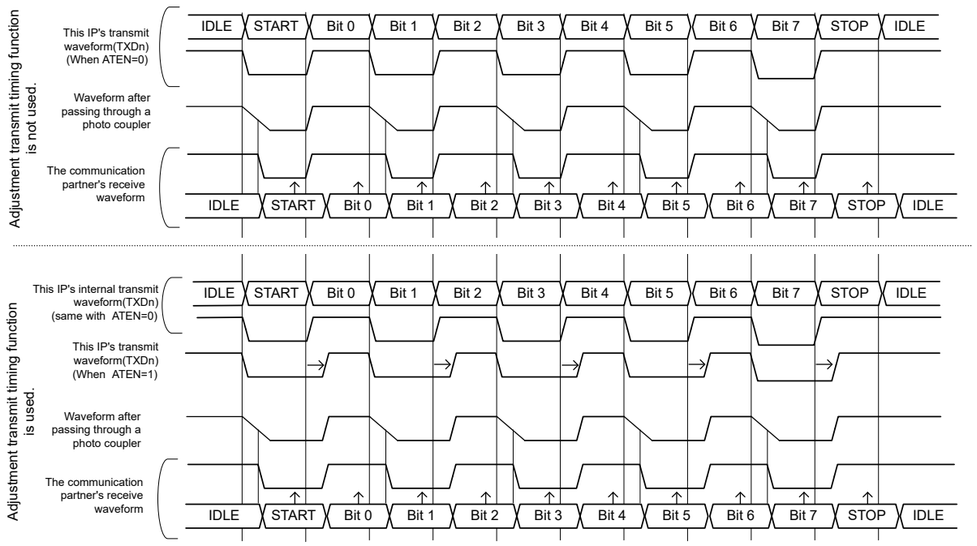
Figure 30.36 通过光电耦合器进行通信的传输运动图像图形

The explanation of transmit waveforms of the communication through a photo coupler using adjust transmit timing function

When using the transmission timing adjustment function, adjust the edge timing of the transmission waveform and correct the reception waveform of the communication partner

The following example is 8 bit long data.

(a) In the case of the falling edge transfer time >> the rising transfer time



(b) In the case of the falling edge transfer time << the rising transfer time

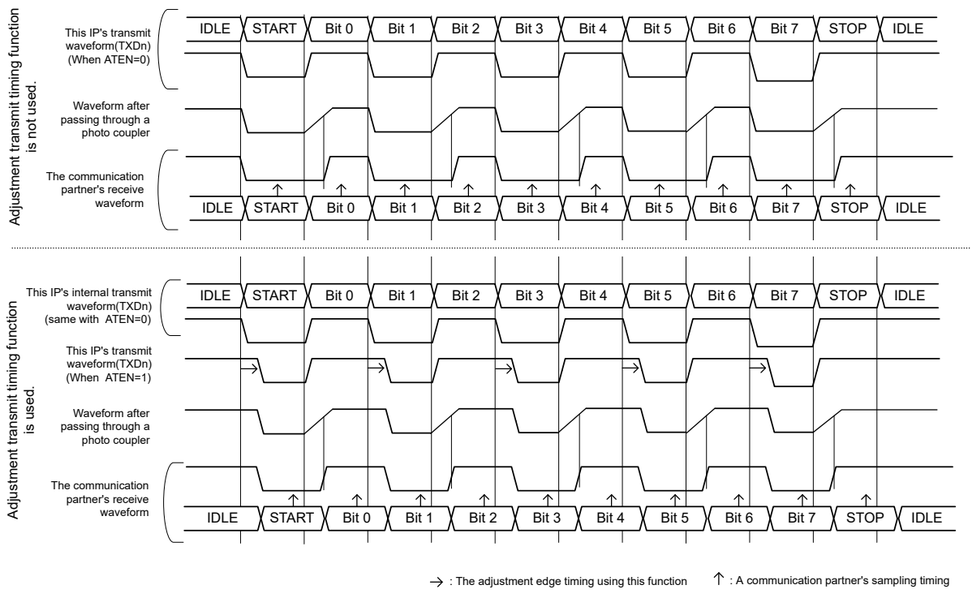
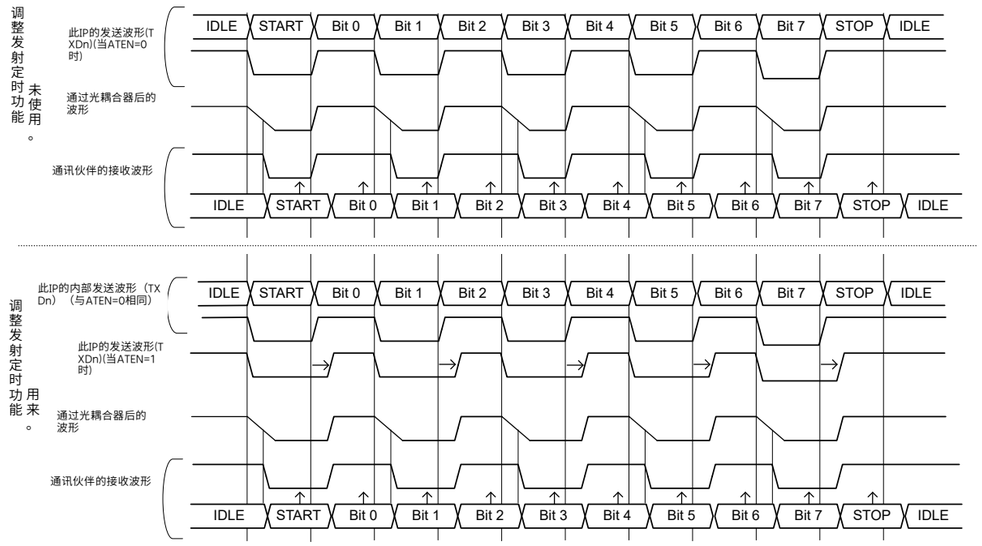


Figure 30.37 The explanation for the transmit waveform through a photo coupler

使用调整发射定时功能通过光电耦合器进行通信的发射波形说明

使用发送定时调整功能时，调整发送波形的边沿定时，修正通信对方的接收波形。下例为8位长的数据。

(a)在下降沿传输时间>>上升沿传输时间的情况下



(b)在下降沿传输时间<<上升沿传输时间的情况下

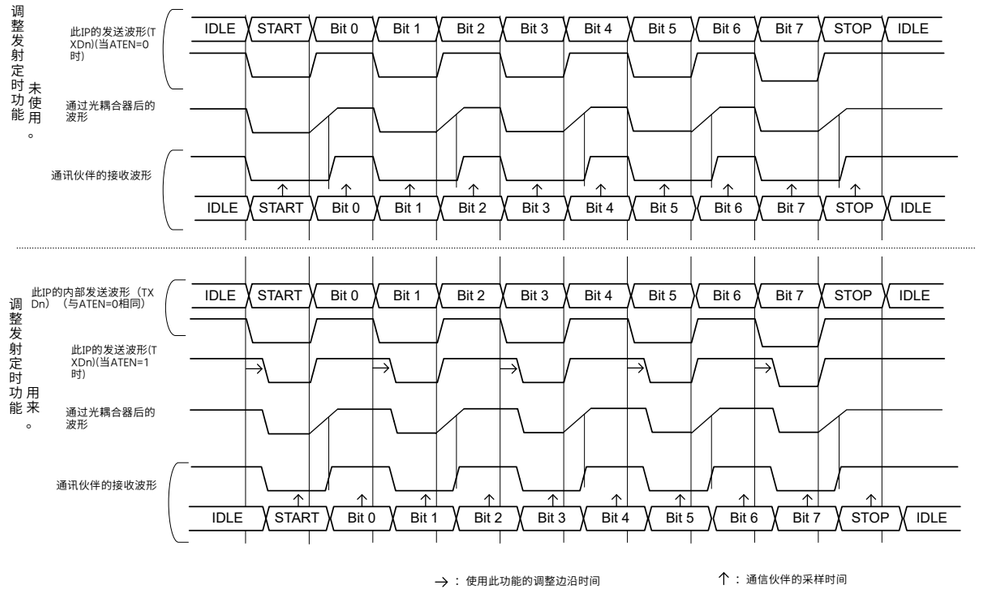


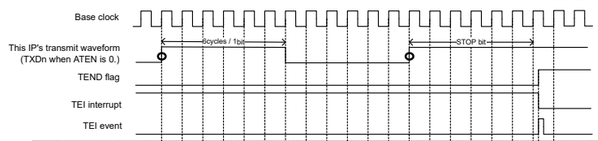
Figure 30.37 通过光电耦合器的发射波形的解释

The operation explanation of adjustment the transmit timing

(a) In the case of the falling transfer time >> rising transfer time

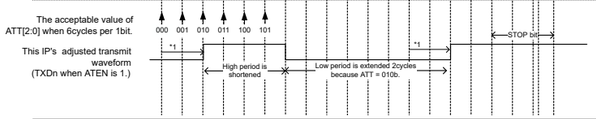
In this case, the high period of a communication partner's reception waveform is made long, and the low period is made short.
Therefore, this IP transmits the waveform with the edge relatively brought forward by adjusting the falling edge timing.
Then adjust value(ATT[2:0]) should be set to make equal the low-period/1bit and high-period/1bit for a communication partner.

This function's operation is explained as an example of 6cycles/1bit.



(a-1) The function of adjust transmit timing OFF (ATEN = 0), AET = x, ATT[2:0] = xxxb

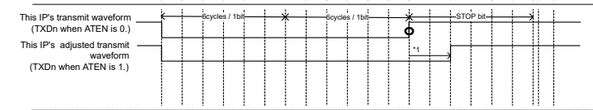
TEND flag is set when stop-bit transmission end.
TEI interrupt and event are output at the same time, too.
Even when ATEN is 1, their timing does not change.



(a-2)The function of adjust transmit timing ON (ATEN = 1), AET = 0, ATT[2:0] = 010b

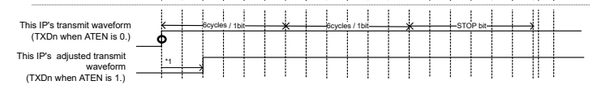
The acceptable value of ATT[2:0] are 000b – 101b when 6cycles per 1bit.

When AET = 0, the rising edge ○ of TxD waveform is adjusted.



(a-3) When the same value continues in the transmission data (0->0)

This function adjust the edge timing of transmit waveform.
So, transmit timing adjustment is not done when the same value continues in the transmission data.
The figure on the left shows the example of ATEN = 1, AET = 0 and ATT[2:0] = 010b.



(a-4)When the same value continues in the transmission data (1->1)

This function adjust the edge timing of transmit waveform.
So, transmit timing adjustment is not done when the same value continues in the transmission data.
The figure on the left shows the example of ATEN = 1, AET = 0 and ATT[2:0] = 010b.

Note 1. Thee rising edge of transmit timing is shifted to back by the setting value of ACTR.ATT[2:0].

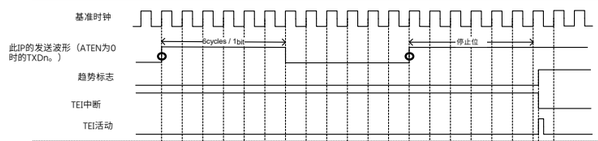
Figure 30.38 The adjustment operation explanation for the transmit timing when AET is 0

调整发送时间的操作说明

(a)在下降传送时间>>上升传送时间的情况下在这种情况下，通信对方的接收波形的高电平周期变长，而低电平周期变短。因此，该IP通过调整下降沿时序来传输边缘相对提前的波形。

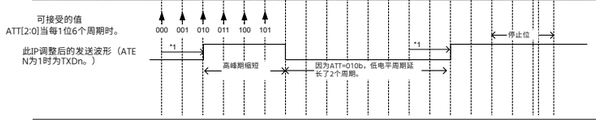
然后调整值（ATT[2:0]）应设置为使通信伙伴的低周期1bit和高周期1bit相等。

该功能的操作以6cycles1bit为例进行说明。



(a-1)调整发送时序的功能OFF(ATEN=0) AET=x ATT[2:0]=xxxb

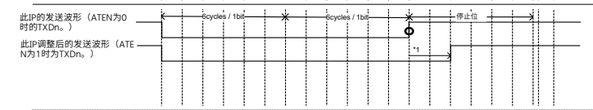
当停止位传输结束时设置TEND标志。
TEI中断和事件也同时输出。
即使ATEN为1，它们的时序也不会改变。



(a-2)调整发送时序的功能ON(ATEN=1) AET=0 ATT[2:0]=010b

ATT[2:0]的可接受值为000b 101b，当每1bit有6个周期时。

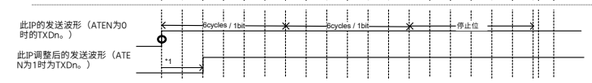
当AET=0时，调整TxD波形的上升沿。



(a-3)发送数据中持续相同值时(0->0)
此功能调整发送波形的边沿时序。

因此，当传输数据中继续相同的值时，不进行传输定时调整。左图显示了ATEN=1、AET=0和

ATT[2:0] = 010b.



(a-4)发送数据中持续相同的值时(1->1)
此功能调整发送波形的边沿时序。

因此，当传输数据中继续相同的值时，不进行传输定时调整。左图显示了ATEN=1、AET=0和

ATT[2:0] = 010b.

注1.发送时序的上升沿由ACTR.ATT[2:0]的设置值向后移动。

Figure 30.38 AET为0时发射时序调整操作说明

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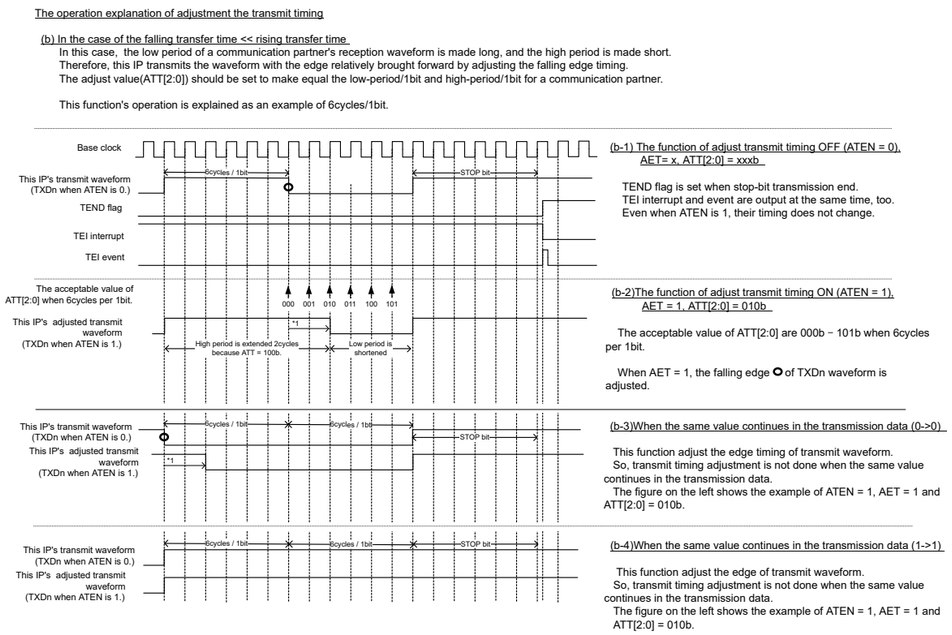


Note 1. The falling edge of transmit timing is shifted to back by the setting value of ACTR.ATT[2:0].

Figure 30.39 The adjustment operation explanation for the transmit timing when AET is 1

30.4 Multi-Processor Communication Function

The multi-processor communication function enables the SCI to transmit and receive data between multiple processors by sharing an asynchronous serial communication line that has an added multi-processor bit. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

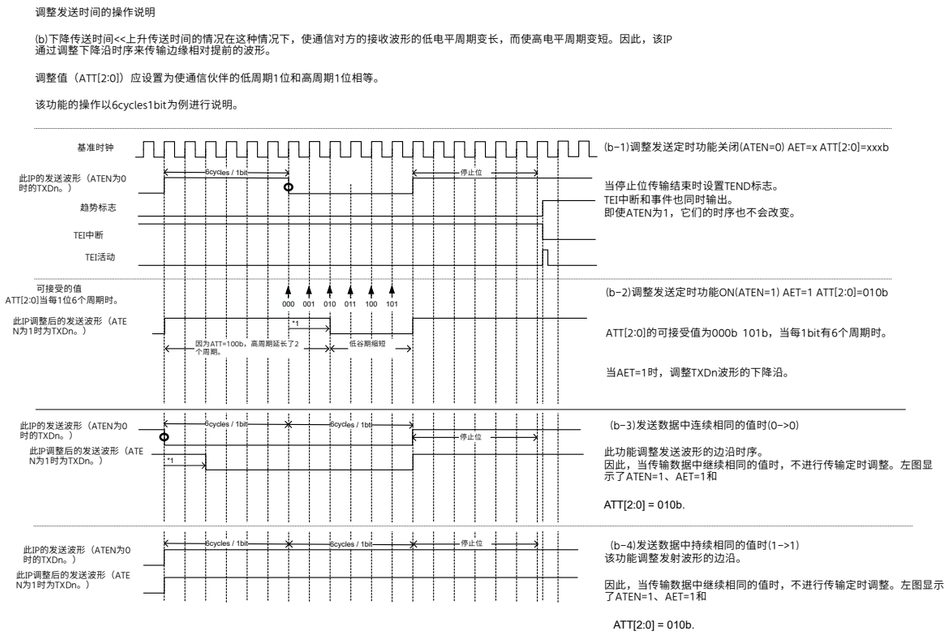
- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle

Figure 30.40 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0 is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives data in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the SCR.MPIE bit. When the MPIE bit is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the RDR register (the RDRHL register when 9-bit data length is selected)
- Detection of a receive error



注1.发送时序的下降沿由ACTR.ATT[2:0]的设置值向后移动。

Figure 30.39 AET为1时发射时序调整操作说明

30.4 多处理器通信功能

多处理器通信功能使SCI能够通过共享一条增加了多处理器位的异步串行通信线路在多个处理器之间发送和接收数据。在多处理器通信中，为每个接收站分配一个唯一的ID代码。串行通信周期由指定接收站的ID传输周期和向指定接收站传输数据的数据传输周期组成。

多处理器位用于区分ID传输周期和数据传输周期：

●当多处理器位设置为1时，传输周期为ID传输周期

●当多处理器位设置为0时，传输周期为数据传输周期

图30.40显示了使用多处理器格式的处理器之间的通信示例。首先，发送站发送将设置为1的多处理器位添加到接收站的ID码的通信数据。接着，发送站发送在发送数据中附加了多处理器比特为0的通信数据。接收站接收到多处理器位设置为1的通信数据后，将接收到的ID与接收站自身的ID进行比较。如果两者匹配，则接收站接收随后发送的通信数据。如果接收到的ID与接收站的ID不匹配，则接收站跳过通信数据，直到接收到多处理器位设置为1的数据。

(1) Non-FIFO selected

为了支持这个功能，SCI提供了SCR.MPIE位。当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

●将接收数据从RSR寄存器传送到RDR寄存器（选择9位数据长度时的RDRHL寄存器）

●接收错误检测

- Setting of the respective RDRF, ORER, and FER status flags in the SSR register

When the SCI receives a character in which the multi-processor bit is set to 1, the SSR.MPBT bit is set to 1 and the SCR.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in normal asynchronous mode.

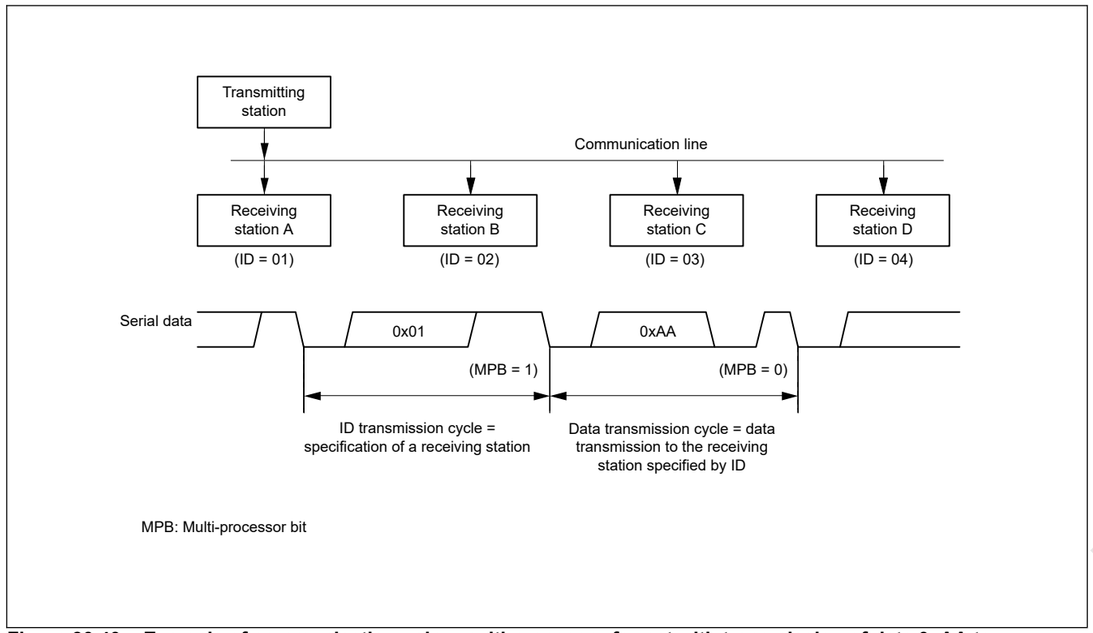


Figure 30.40 Example of communication using multi-processor format with transmission of data 0xAA to receiving station A

(2) FIFO selected

For data transmission, software must write data to FTDRHL.MPBT that corresponds to transmit data in FTDRHL.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to FTDRHL.MPB and receive data is written to FRDRL.

When the MPIE bit is set to 1, the following operations are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the FRDRHL register
- Detection of a receive error
- Break
- Setting of the respective RDF, ORER, and FER status flags in the SSR_FIFO register

When the SCI receives an 8-bit character in which the multi-processor bit is set to 1, the FTDRHL.MPB bit is set to 1 and receive data is written to FRDRHL.RDAT. The SCR.MPIE bit is automatically cleared, returning the SCI to normal reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in normal asynchronous mode with FIFO selected.

30.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

●在SSR寄存器中设置相应的RDRF、ORER和FER状态标志

当SCI接收到多处理器位设置为1的字符时，SSR.MPBT位设置为1，并且SCR.MPIE位自动清零，使SCI恢复正常接收操作。如果SCR.RIE位设置为1，则SCIn_RXI中断产生。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与正常异步模式下的操作没有区别。用于多处理器通信的时钟与正常异步模式下使用的时钟相同。

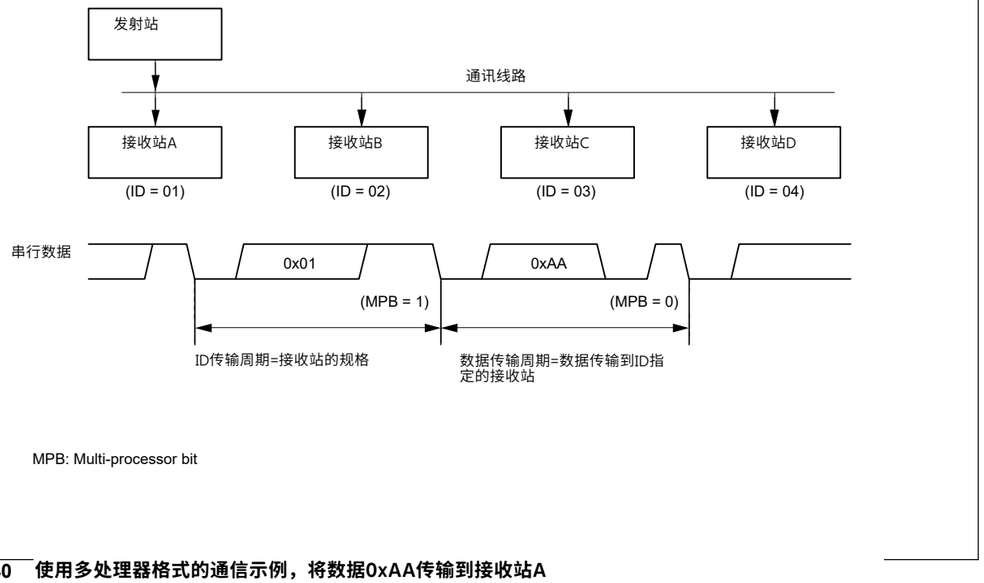


Figure 30.40 使用多处理器格式的通信示例，将数据0xAA传输到接收站A

(2) FIFO selected

对于数据传输，软件必须将数据写入与FTDRHL.TDAT中的传输数据相对应的FTDRHL.MPBT。对于数据接收，作为接收数据一部分的多处理器位被写入FTDRHL.MPB，接收数据被写入FRDRL。

当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

●将接收数据从RSR寄存器传送到FRDRHL寄存器

●接收错误检测

- Break

●在SSR_FIFO寄存器中设置相应的RDF、ORER和FER状态标志

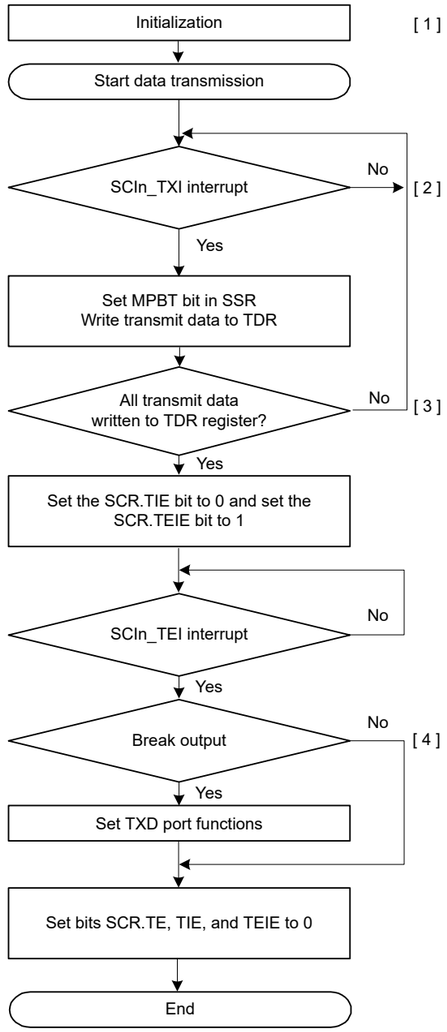
当SCI接收到多处理器位设置为1的8位字符时，FTDRHL.MPB位设置为1，接收数据写入FRDRHL.RDAT。SCR.MPIE位自动清零，使SCI恢复正常接收操作。如果SCR.RIE位设置为1，则会产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与选择FIFO的正常异步模式下的操作没有区别。

30.4.1 多处理器串行数据传输

(1) Non-FIFO selected

Figure 30.41 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the SSR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode. Write the values in the order of the FTDRH register then the FTDRL register.



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Set the MPBT bit in SSR to 0 or 1, and write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request.
Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR.

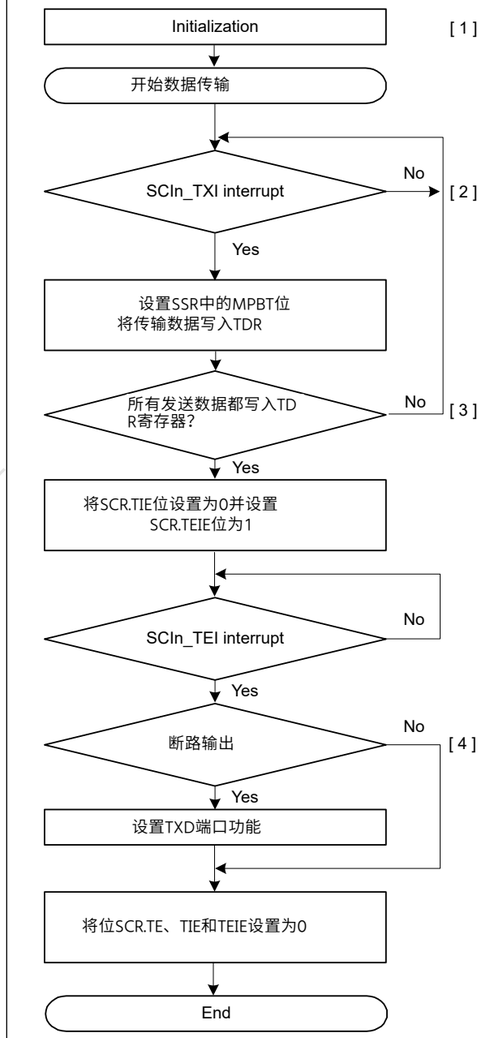
[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 30.41 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 30.42 shows an example of data format that is written to FTDRH and FTDRL in multi-processor mode. The FTDRH.MPBT bit is set to 1. Data is set to FTDRH and FTDRL with the correct data length. Write 0 for unused bits. Write in order from FTDRH to FTDRL.

图30.41显示了一个多处理器数据传输的示例流程。在ID传输周期，ID必须在SSR.MPBT位设置为1的情况下传输。在数据传输周期，数据必须在MPBT位设置为0的情况下传输。其余操作与操作相同在异步模式下。按照FTDRH寄存器然后FTDRL寄存器的顺序写入值。



[1] SCI initialization:
设置数据传输。SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] SCIn_TXI interrupt request:
当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。将SSR中的MPBT位设置为0或1，并将发送数据写入

TDR在SCIn_TXI中断处理例程中执行一次。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据写入TDR一次。发送数据也可以通过激活写入到TDR

DMAC or DTC.
当SCIn_TEI中断请求正在使用时，设置
在要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，请在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Figure 30.41 选择非FIFO的多处理器串行传输示例流程

(2) FIFO selected

图30.42显示了在多处理器模式下写入FTDRH和FTDRL的数据格式示例。这
FTDRH.MPBT位设置为1。数据设置为具有正确数据长度的FTDRH和FTDRL。为未使用的位写入0。从FTDRH到FTDRL的顺序写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

Note: —: Invalid. The write value should be 0.

Figure 30.42 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

Figure 30.43 shows an example flow of multi-processor serial transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the FTDRH.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8位传输数据							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9位传输数据								

Note: –：无效的。写入值应为0。

Figure 30.42 在选择FIFO的多处理器模式下写入FTDRH和FTDRL的数据格式

图30.43显示了选择FIFO的多处理器串行传输示例流程。在ID传输周期中，必须在FTDRH.MPBT位设置为1的情况下传输ID。在数据传输周期中，必须在MPBT位设置为0的情况下传输数据。其余操作与操作相同在异步模式下选择FIFO。

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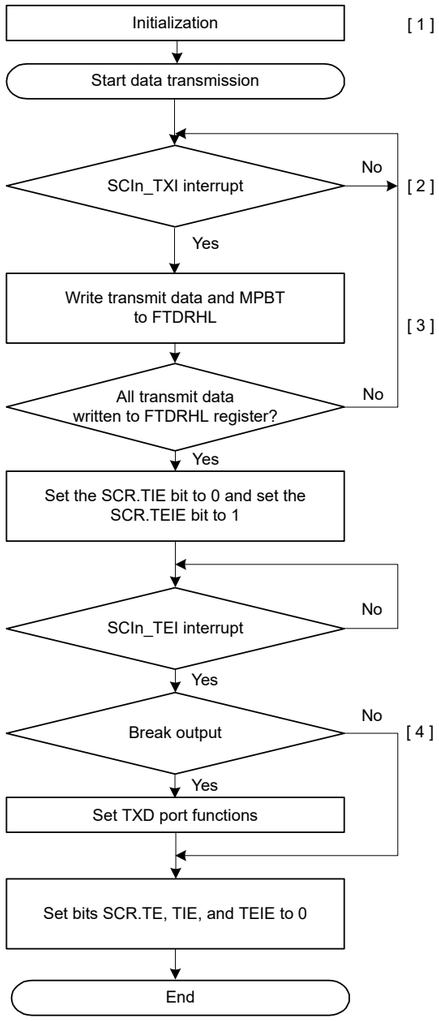


[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRHL by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRHL to TSR, when the quantity of receive data written in FTDRHL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data and MPBT to FTDRHL once using an SCIn_TXI interrupt request.
Transmit data can also be written to FTDRHL by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRHL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXD pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

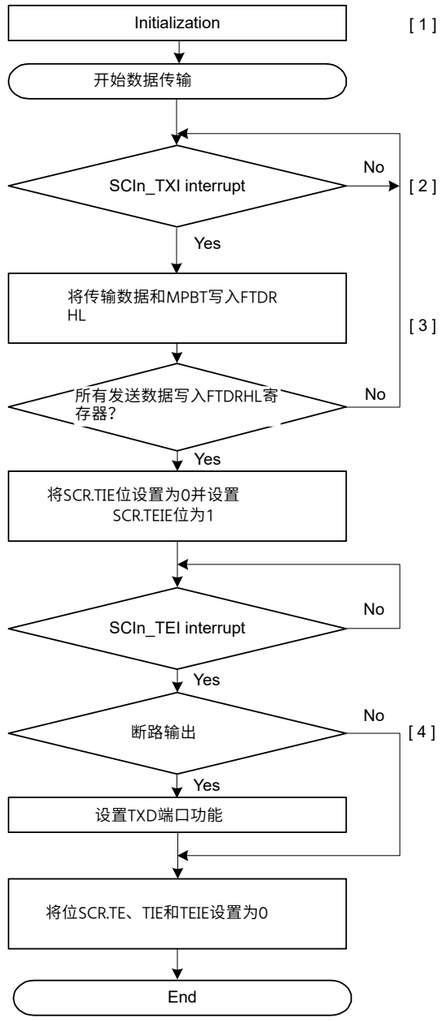
Figure 30.43 Example flow of serial transmission in multi-processor mode with FIFO selected

30.4.2 Multi-Processor Serial Data Reception

(1) Non-FIFO selected

Figure 30.45 and Figure 30.46 are example flows of multi-processor serial reception. When the SCR.MPIE bit is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to the RDR register (the RDRHL register when 9-bit data length is selected), and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as operations in asynchronous mode. Read the order from FRDRH to FRDRL.

Figure 30.44 shows an example operation for data reception.



[1] SCI initialization:
设置数据传输。SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] [2]通过SCIn_TXI中断请求向FTDRHL发送数据写入：当发送数据从FTDRHL传输到TSR时，当写入FTDRHL的接收数据量等于或小于指定的发送触发数时，发送数据FIFO为空产生中断（SCIn_TXI）请求。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据和MPBT写入一次FTDRHL。也可以通过激活DMAC或DTC将传输数据写入FTDRHL。

使用SCIn_TEI中断请求时，将要发送的最后一个数据写入FTDRHL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXD引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Figure 30.43 选择FIFO的多处理器模式下的串行传输示例流程

30.4.2 多处理器串行数据接收

(1) Non-FIFO selected

图30.45和图30.46是多处理器串行接收的示例流程。当SCR.MPIE位设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据被传输到

RDR寄存器（选择9位数据长度时的RDRHL寄存器），并产生SCIn_RXI中断请求。其余操作与异步模式下的操作相同。读取从FRDRH到FRDRL的订单。

图30.44显示了数据接收的示例操作。

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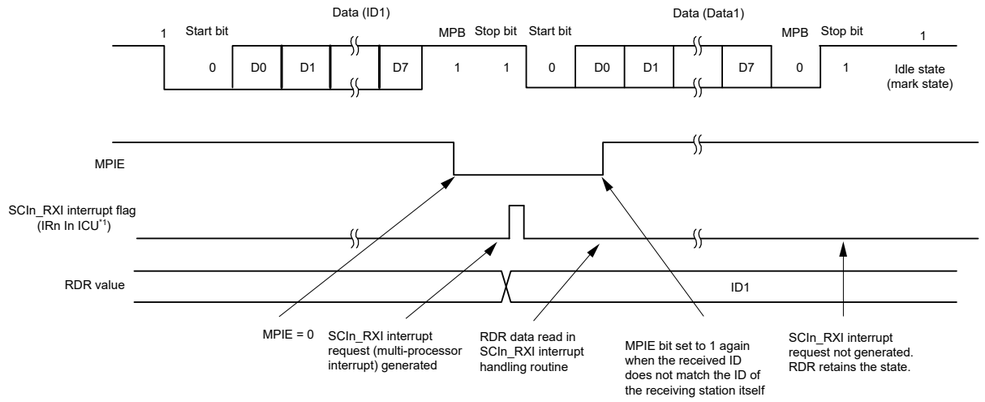
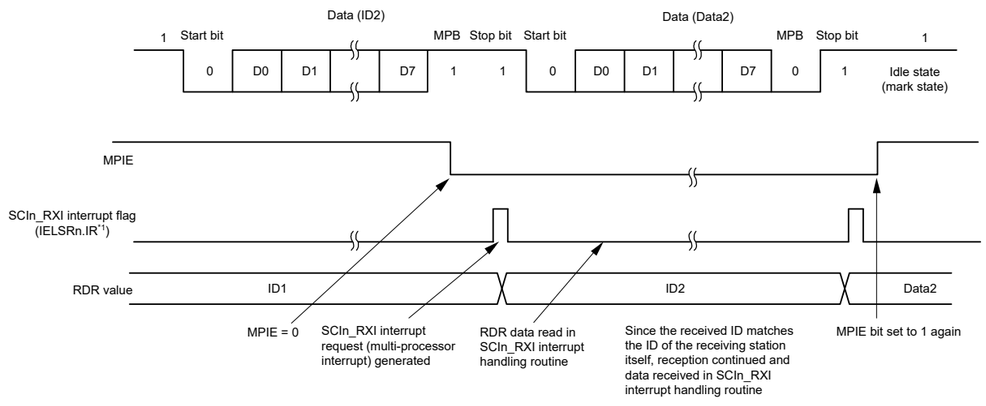


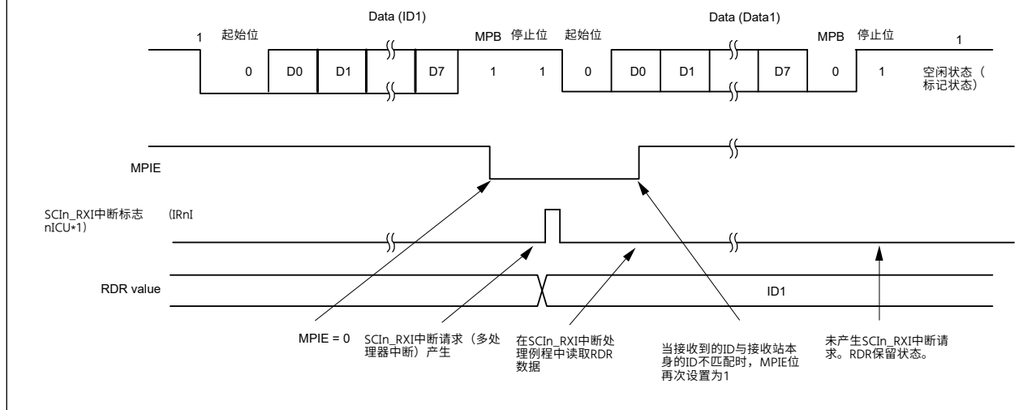
(a) When the received ID does not match the ID of the receiving station itself



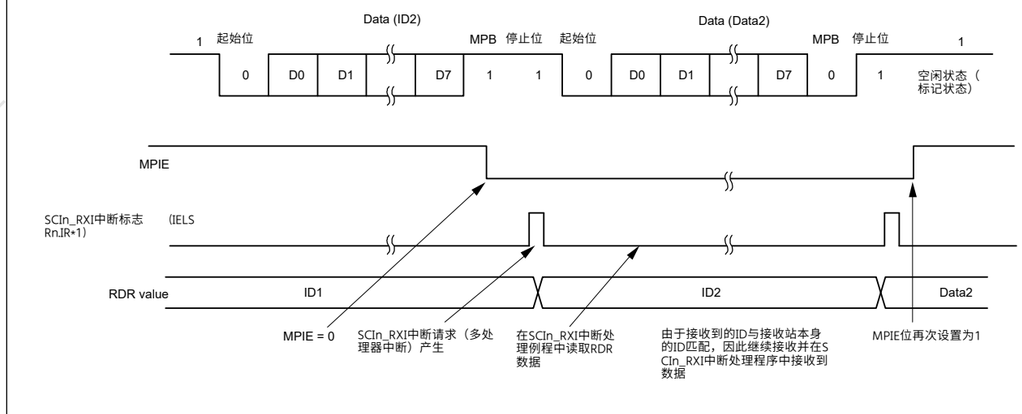
(b) When the received ID matches the ID of the receiving station itself

Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.44 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



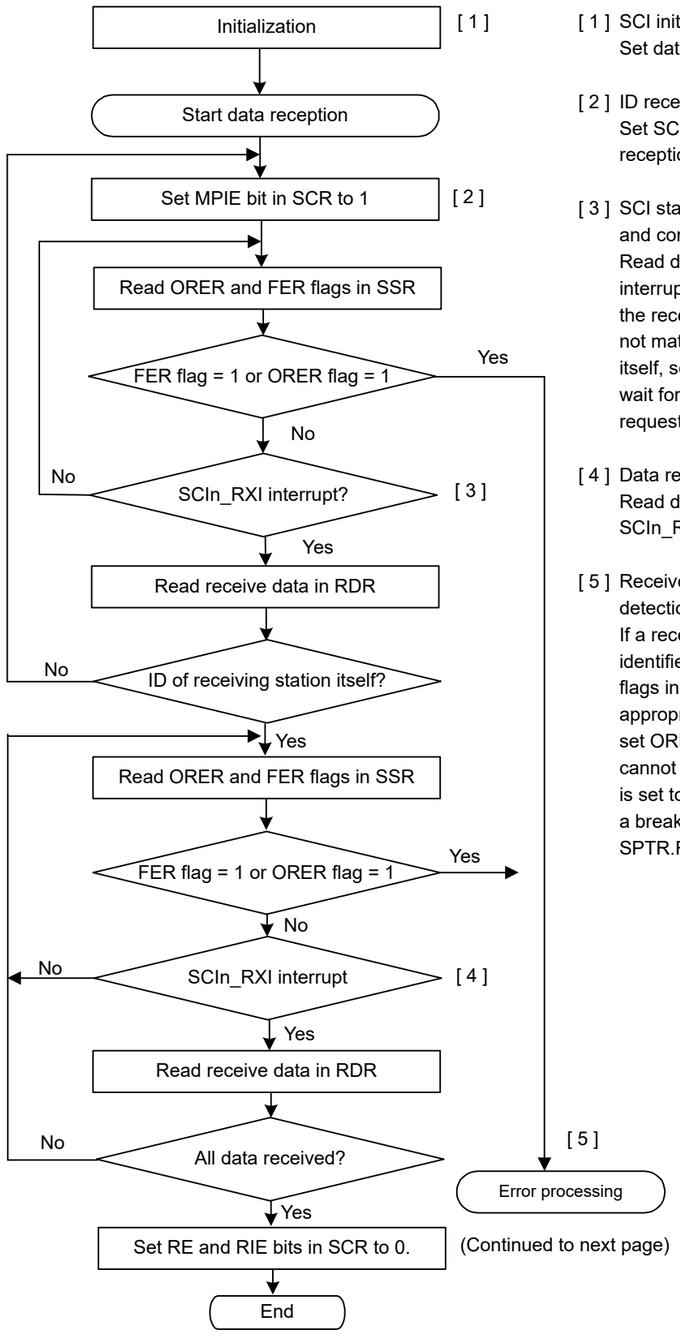
(a)当接收到的ID与接收站本身的ID不匹配时



(b)当接收到的ID与接收站本身的ID匹配时

注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.44 使用8位数据、多处理器位和1个停止位的SCI接收示例



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set SCR.MPIE bit to 1 and wait for ID reception.

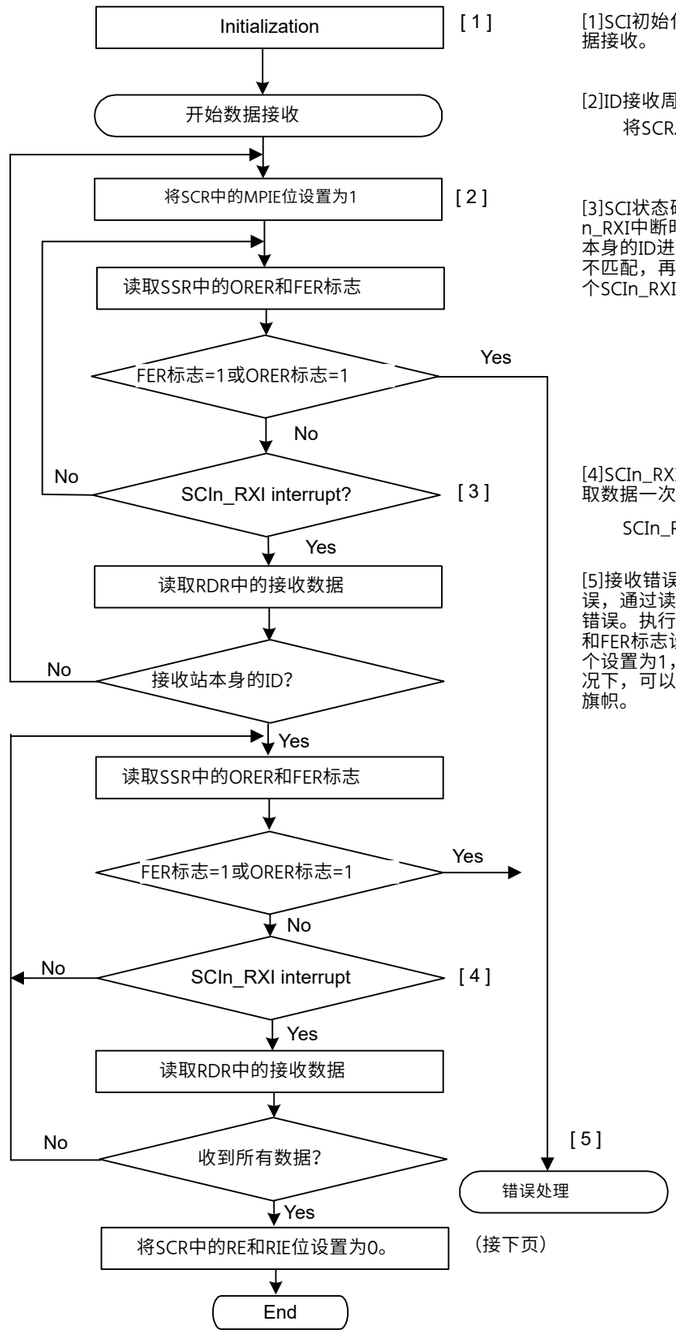
[3] SCI status confirmatIon and reception and comparison of ID:
Read data in RDR*1 at the first SCIn_RXI interrupt and compare it with the ID of the receiving statIon itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR*1 once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in SSR. After performing the appropriate error processing, be sure to set ORER and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading SPTR.RXDMON flag.

Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 30.45 Example flow of multi-processor serial reception with non-FIFO selected (1)



[1]SCI初始化：设置数据接收。

[2]ID接收周期：
将SCR.MPIE位设置为1并等待ID接收。

[3]SCI状态确认及ID接收与比较：在第一次SCIn_RXI中断时读取RDR*1中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，再次将MPIE位设置为1，并等待另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断时的数据接收：在RDR*1中读取数据一次
SCIn_RXI中断程序。

[5]接收错误处理和中断检测：如果发生接收错误，通过读取SSR中的ORER和FER标志来识别错误。执行适当的错误处理后，请务必将ORER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。在帧错误的情况下，可以通过读取SPTR.RXDMON来检测中断旗帜。

注意1.选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 30.45 选择非FIFO的多处理器串行接收示例流程(1)

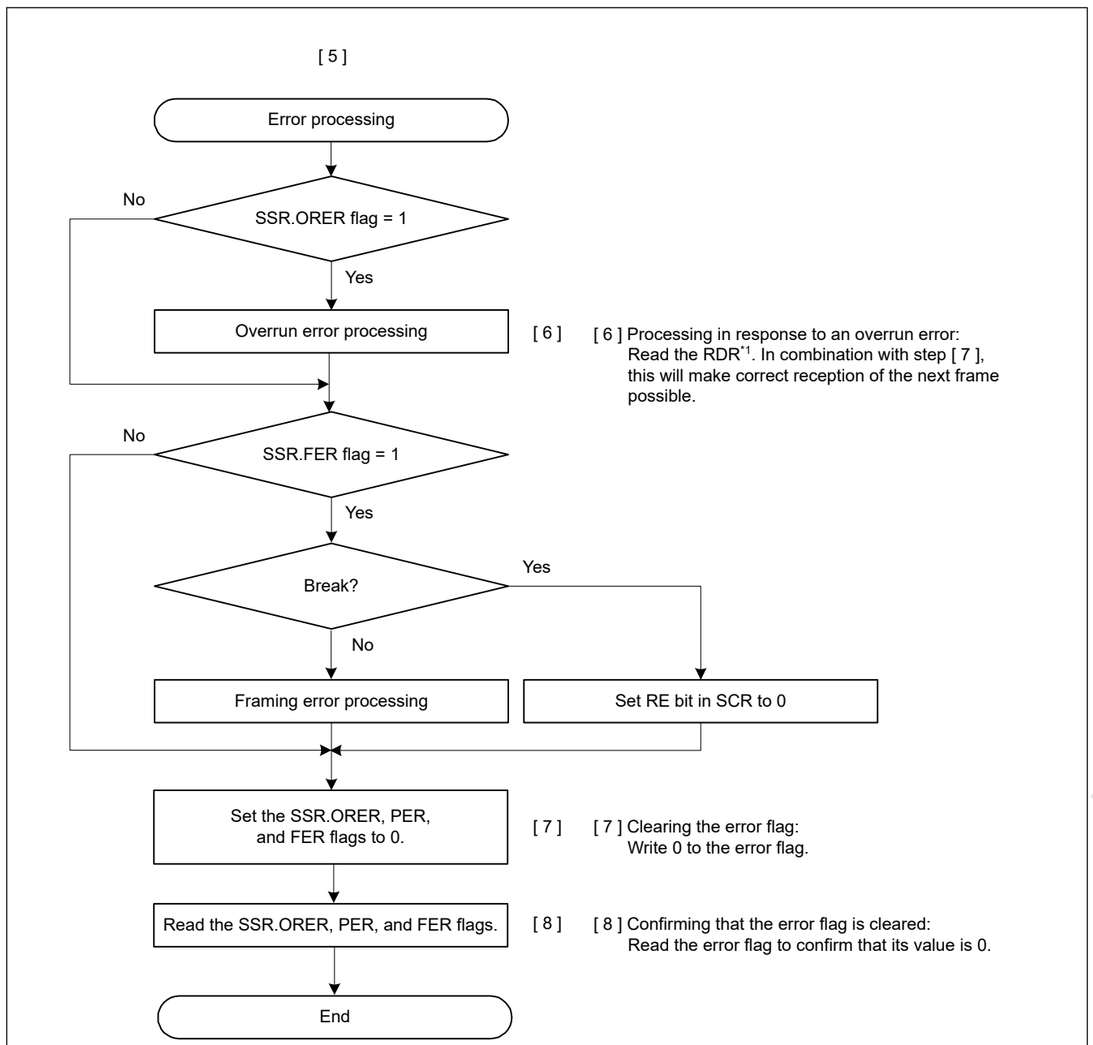


Figure 30.46 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 30.47 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the FRDRH.MPB bit. A value of 0 is written to the FRDRH.PER flag. Data is written to FRDRH and FRDRL with the correct data length. Unused bits are written with 0. Read in order from FRDRH to FRDRL. When software reads the FRDRL register, the SCI updates FER, MPB, and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER and DR flags in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

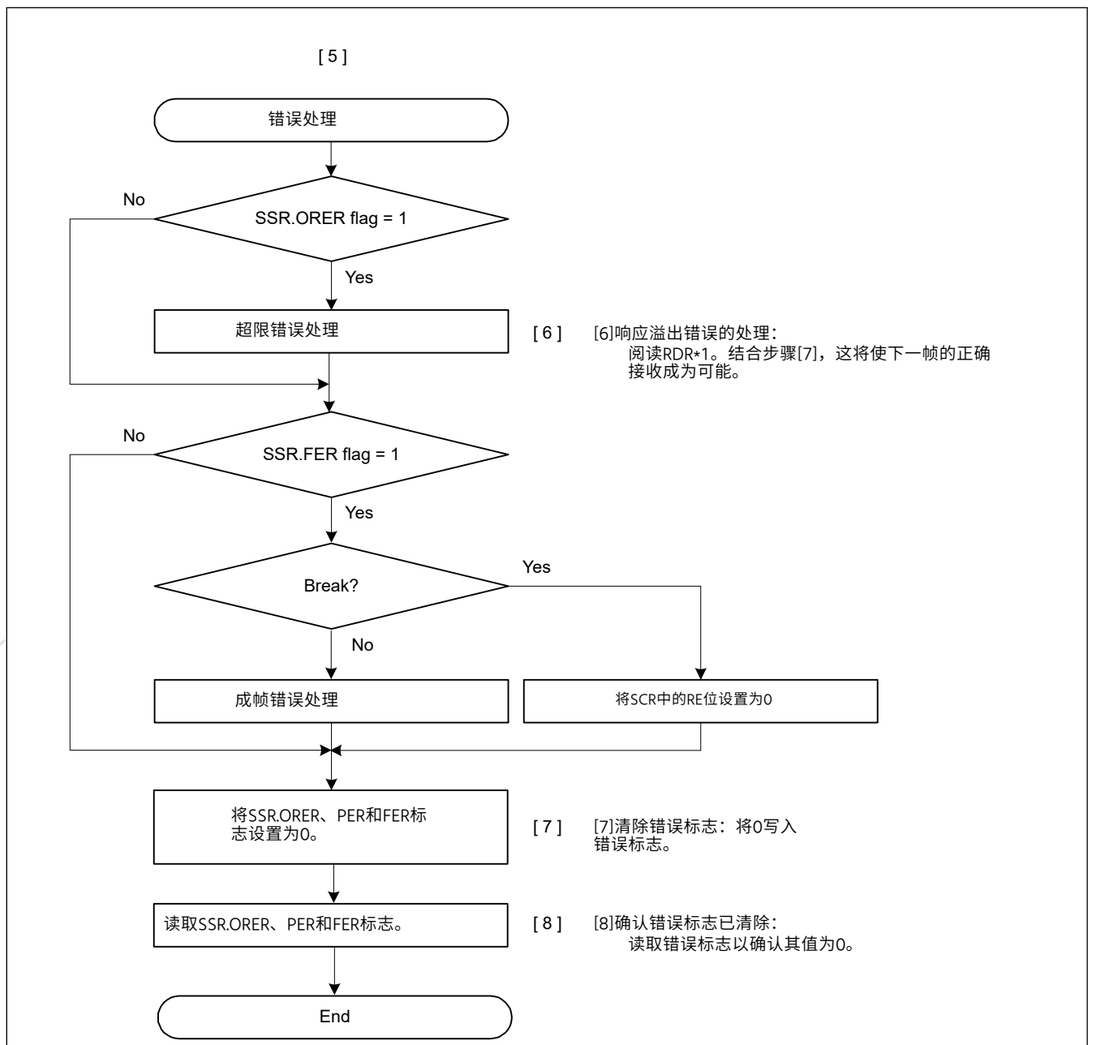


Figure 30.46 选择非FIFO的多处理器串行接收示例流程(2)

(2) FIFO selected

图30.47显示了在多处理器模式下写入FRDRH和FRDRL的数据格式示例。

在多处理器模式下，作为接收数据一部分的MPB值被写入FRDRH.MPB位。值0写入FRDRH.PER标志。数据以正确的数据长度写入FRDRH和FRDRL。未使用的位写入0。按从FRDRH到FRDRL的顺序读取。当软件读取FRDRL寄存器时，SCI用下一个数据更新FER、MPB和FRDRL中的接收数据（RDAT[8:0]）。FRDRH寄存器中的RDF、ORER和DR标志始终反映SSR_FIFO寄存器中的相关标志。

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRHL[15] bit is read as an indefinite value

Figure 30.47 Data format stored in FRDRH and FRDRL in multi-processor mode with FIFO selected

Figure 30.48 shows an example flow of multi-processor data reception with FIFO selected. When the SCR.MPIE is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and associated errors are transferred to the FRDRHL register. The SCR.MPIE bit is automatically cleared and normal reception continues.

If a framing error occurs and the SSR_FIFO.FER flag is set to 1, the SCI continues data reception. The rest of the operations are the same as operations in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8位接收数据							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9位接收数据								

Note: 当数据长度为7位时，FRRDH[0]和FRDRL[7]总是读取0
当数据长度为8位时，FRRDH[0]总是读取0
FRDRHL[15]位被读取为不定值

Figure 30.47 选择FIFO的多处理器模式下存储在FRDRH和FRDRL中的数据格式

图30.48显示了选择FIFO的多处理器数据接收示例流程。当SCR.MPIE设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据、MPB和相关错误被传送到FRDRHL寄存器。SCR.MPIE位自动清零并继续正常接收。

如果发生帧错误并且SSR_FIFO.FER标志设置为1，则SCI继续数据接收。其余操作与选择FIFO的异步模式中的操作相同。

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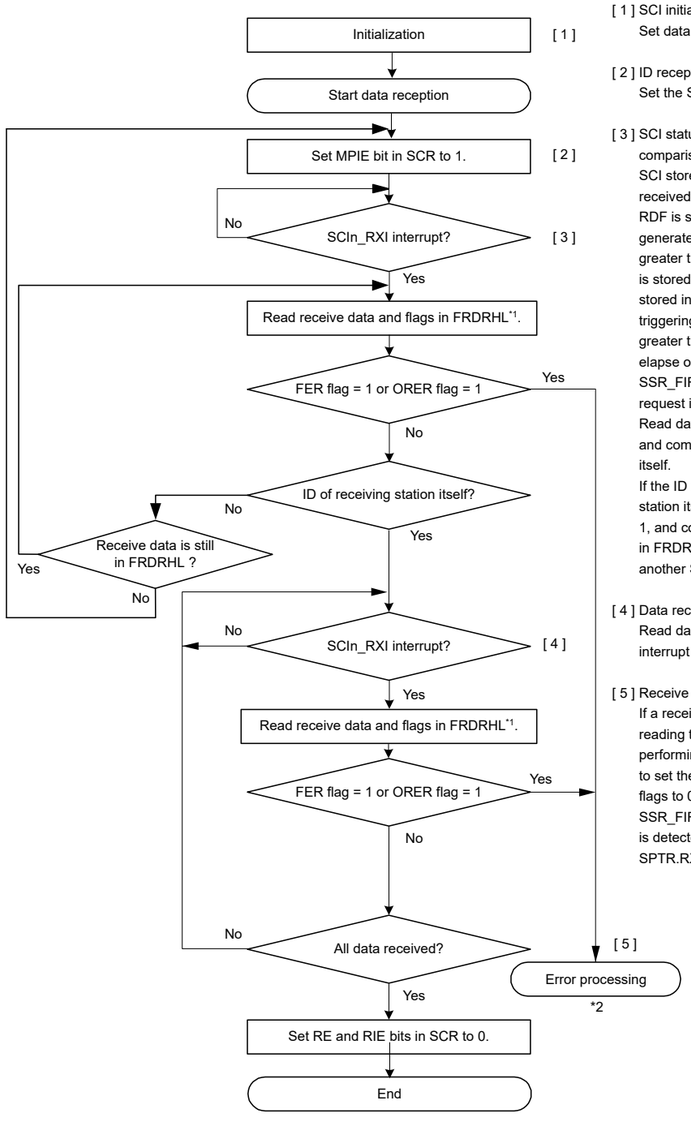


[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set the SCR.MPIE bit to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
SCI stores first data (MPB = 1) and subsequent received data in FRDRHL.
RDF is set to 1 and an SCIn_RXI interrupt request is generated when a quantity of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL. When the quantity of data stored in FRDRHL falls the specified receive triggering number and received data is equal to or greater than 1, and no next data is received after the elapse of 15 ETUs from the last stop bit, SSR_FIFO.DR is set to 1. An SCIn_RXI interrupt request is generated when FCR.DRES bit is 0.
Read data in FRDRHL at the first SCIn_RXI interrupt, and compare it with the ID of the receiving station itself.
If the ID does not match the ID of the receiving station itself, the SCI reads until the data with MPB = 1, and compares next ID. If it is no data with MPB = 1 in FRDRHL, set the MPIE bit to 1 again and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in FRDRHL once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the SSR_FIFO.ORER and SSR_FIFO.FER flags to 0. Reception cannot be resumed if the SSR_FIFO.ORER flag is set to 1. When framing error is detected, a break can be detected by reading the SPTR.RXDMON flag.

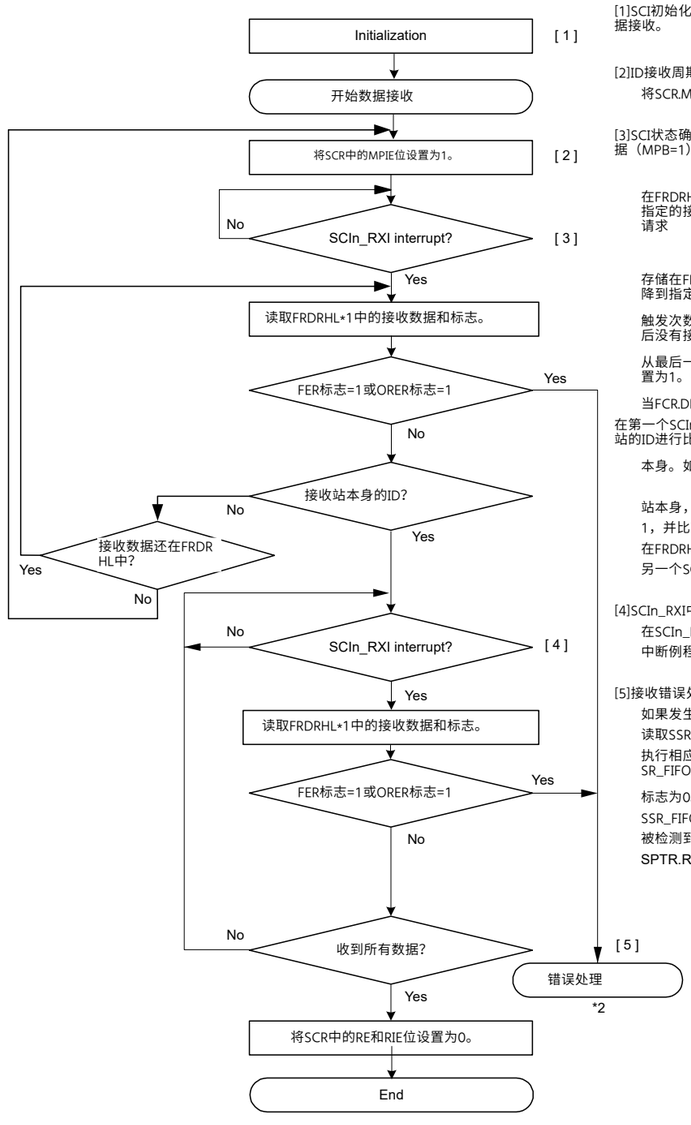
Note 1. If FRDRH and FRDRL are used instead of FRDRHL, read in order from FRDRH to FRDRL.
Note 2. Same as Figure 30.46

Figure 30.48 Example flow of serial reception in multi-processor mode with FIFO selected

30.5 Operation in Manchester mode

In Manchester mode, the transmit or receive serial data is coded in Manchester encoding.

Figure 30.49 shows the conceptual image of Manchester encoding.



[1]SCI初始化：设置数据接收。

[2]ID接收周期：
将SCR.MPIE位设置为1并等待ID接收。

[3]SCI状态确认和ID的接收与比较：SCI存储第一个数据（MPB=1）和后续
在FRDRHL中接收到的数据。当接收数据量等于或大于指定的接收触发次数时，RDF置1并产生SCIn_RXI中断请求
存储在FRDRHL中。当FRDRHL中存储的数据量下降到指定的接收
触发次数和接收到的数据等于或大于1，并且在触发后没有接收到下一个数据
从最后一个停止位经过15个ETU，SSR_FIFO.DR设置为1。SCIn_RXI中断
当FCR.DRES位为0时产生请求。
在第一个SCIn_RXI中断时读取FRDRHL中的数据，并与接收站的ID进行比较
本身。如果ID与接收方的ID不匹配
站本身，SCI读取直到数据与MPB=1，并比较下一个ID。如果没有MPB=1的数据
在FRDRHL中，再次将MPIE位设置为1并等待
另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断处的数据接收：
在SCIn_RXI中读取一次FRDRHL中的数据
中断例程。

[5]接收错误处理和断线检测：
如果发生接收错误，则通过以下方式标识错误
读取SSR_FIFO中的ORER和FER标志。后
执行相应的错误处理，请务必设置SSR_FIFO.ORER和SSR_FIFO.FER
标志为0。接收不能恢复，如果
SSR_FIFO.ORER标志设置为1。当成帧错误时
被检测到，一个休息可以通过读取检测到
SPTR.RXDMON flag.

注1.如果使用FRDRH和FRDRL代替FRDRHL，请按从FRDRH到FRDRL的顺序读取。
注2.同图30.46

Figure 30.48 选择FIFO的多处理器模式下的串行接收示例流程

30.5 曼彻斯特模式下的操作

在曼彻斯特模式下，发送或接收串行数据以曼彻斯特编码进行编码。

图30.49显示了曼彻斯特编码的概念图。

RA生态工作室

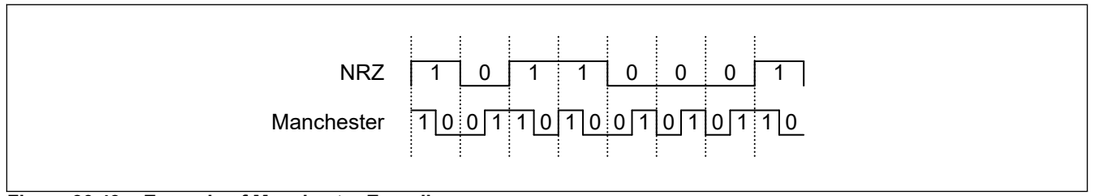


Figure 30.49 Example of Manchester Encoding

In Manchester mode, a preface and a start bit area are added to the transmit data in the register to configure a transmit frame. For transmission, data is encoded in Manchester encoding. When data is received, frames having the same format as transmitted frames are detected and Manchester decoding is performed.

For details on the frame format, see section 30.5.1. Frame Format.

30.5.1 Frame Format

Figure 30.50 shows the frame format in Manchester mode.

In the upper half of the figure, relevant setting registers are shown.

The preface area and the data area are encoded in Manchester encoding.

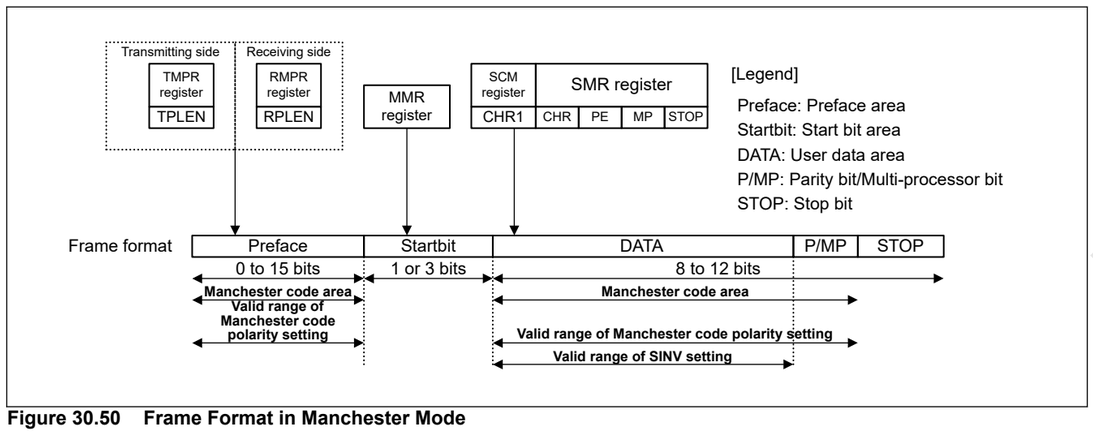


Figure 30.50 Frame Format in Manchester Mode

(1) Preface area

This is a fixed pattern area located at the beginning of each frame.

Different registers are used to set the preface area for transmission and reception. The preface length is determined by setting TMPR.TPLEN[3:0] for transmission. It is determined by setting RMPR.RPLEN[3:0] for reception.

If it is set to 0, the transmit preface is disabled and is not added.

If it is set to 1d to 15d, a preface whose length is determined by this setting is added.

(For example, if it is set to 1d, a 1-bit preface is added. If it is set to 15d, a 15-bit preface is added.)

The preface pattern is set with TMPR.TPPAT[1:0] for transmission and RMPR.RPPAT[1:0] for reception, and is selected from four types of patterns.

Figure 30.51 shows how the preface pattern is set. The preface area and the start bit area are added for each communication frame.

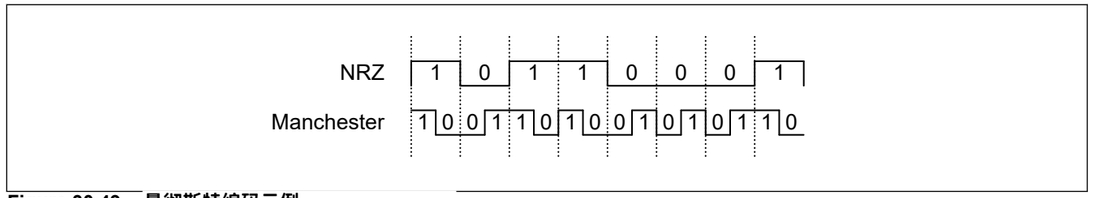


Figure 30.49 曼彻斯特编码示例

在曼彻斯特模式下，前言和起始位区域被添加到寄存器中的发送数据以配置发送帧。对于传输，数据以曼彻斯特编码进行编码。当接收到数据时，检测与传输帧格式相同的帧并执行曼彻斯特解码。

有关帧格式的详细信息，请参见第30.5.1节。帧格式。

30.5.1 帧格式

图30.50显示了曼彻斯特模式下的帧格式。

在图的上半部分，显示了相关的设置寄存器。

前言区和数据区采用曼彻斯特编码。

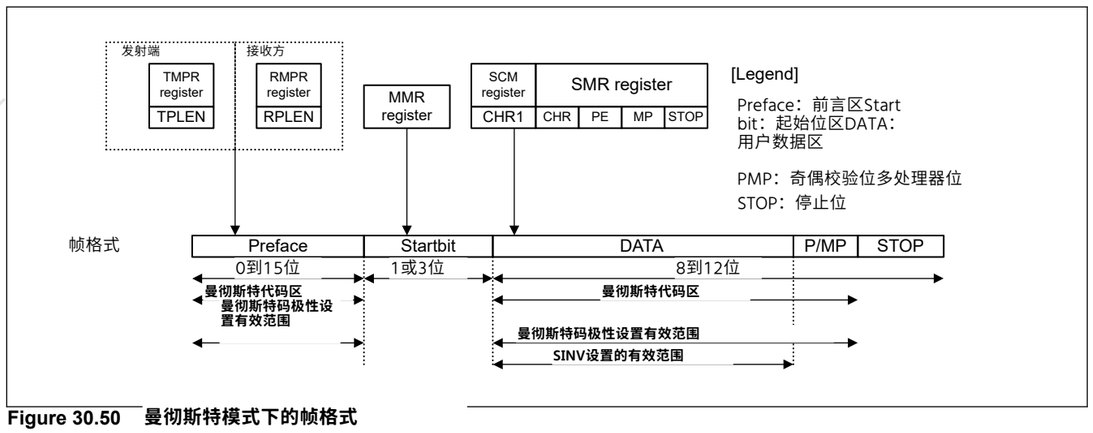


Figure 30.50 曼彻斯特模式下的帧格式

(1) 前言区

这是位于每帧开始处的固定模式区域。

不同的寄存器用于设置发送和接收的前言区域。前言长度通过设置TMPR.TPLEN[3:0]来决定传输。通过设置RMPR.RPLEN[3:0]来确定接收。

如果设置为0，则发送前言被禁用且不添加。

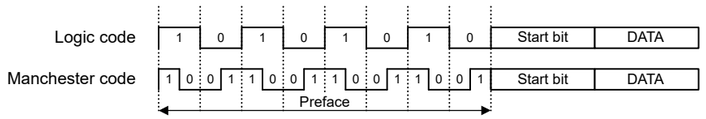
如果设置为1d到15d，则添加一个长度由该设置确定的前言。

（例如，如果设置为1d，则添加1位前言。如果设置为15d，则添加15位前言。）

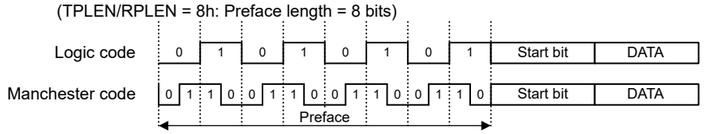
前言模式设置为发送用TMPR.TPPAT[1:0]，接收用RMPR.RPPAT[1:0]，从四种模式中选择。

图30.51显示了如何设置前言模式。为每个通信帧添加前言区和起始位区。

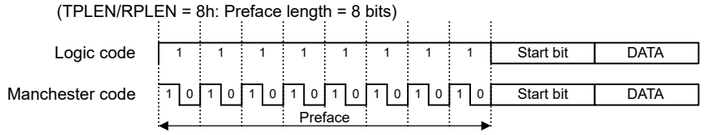
■ TMPR/RMPR = 10: One-zero pattern
(TPLEN/RPLEN = 8h: Preface length = 8 bits)



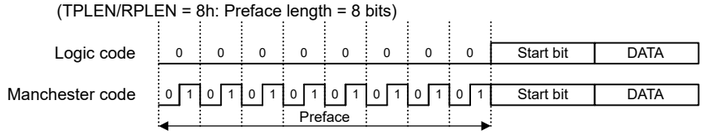
■ TMPR/RMPR = 01: Zero-one pattern
(TPLEN/RPLEN = 8h: Preface length = 8 bits)



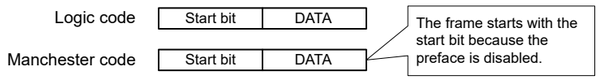
■ TMPR/RMPR = 11: All ones
(TPLEN/RPLEN = 8h: Preface length = 8 bits)



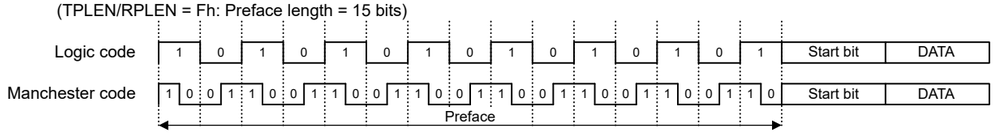
■ TMPR/RMPR = 00: All zeros
(TPLEN/RPLEN = 8h: Preface length = 8 bits)



■ TMPR/RMPR = 01: One-zero pattern
(TPLEN/RPLEN = 0h: Preface disabled)



■ TMPR/RMPR = 10: One-zero pattern
(TPLEN/RPLEN = Fh: Preface length = 15 bits)



■ TMPR/RMPR = 10: One-zero pattern
(TPLEN/RPLEN = 4h: Preface length = 4 bits)

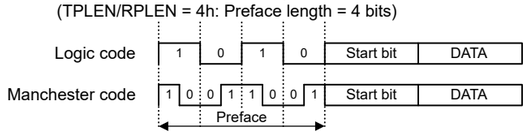


Figure 30.51 Preface Pattern Setting Example

(2) Start bit area

This is an area indicating the start of valid data in a frame. It is added after the preface area.

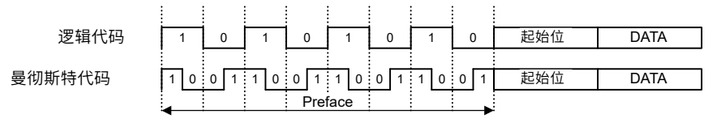
The start bit length is determined by MMR.SBSEL setting. When MMR.SBSEL = “0”, the start bit length is 1 bit.

When MMR.SBSEL = “1”, the start bit length is 3 bits.

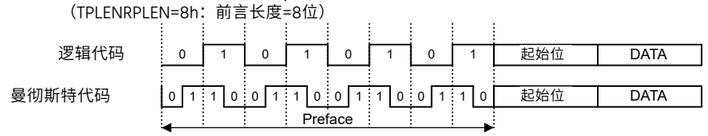
When MMR.SBSEL = “1”, the SYNC type can be selected from command SYNC and data SYNC.

Command SYNC means the three start bits are added as a one-to-zero transition.

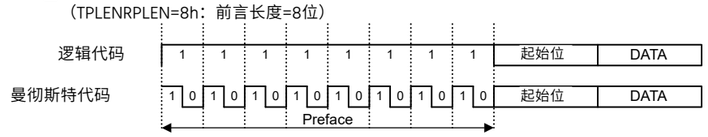
■ TMPR/RMPR = 10: One-zero pattern
（TPLENRPLEN=8h：前言长度=8位）



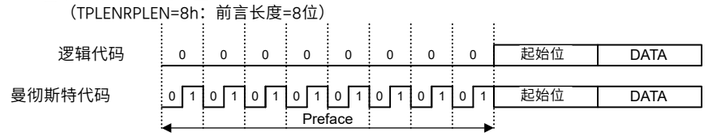
■ TMPR/RMPR = 01: Zero-one pattern
（TPLENRPLEN=8h：前言长度=8位）



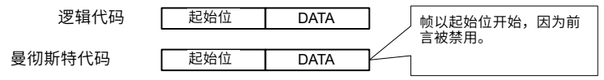
■ TMPRRMPR=11：全为
（TPLENRPLEN=8h：前言长度=8位）



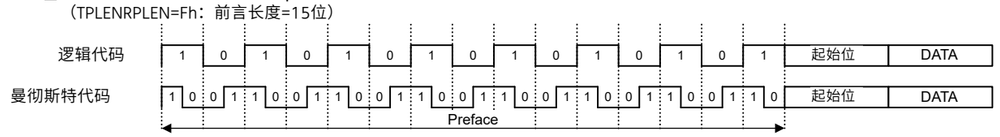
■ TMPRRMPR=00：全零
（TPLENRPLEN=8h：前言长度=8位）



■ TMPR/RMPR = 01: One-zero pattern
(TPLEN/RPLEN = 0h: Preface disabled)



■ TMPR/RMPR = 10: One-zero pattern
（TPLENRPLEN=Fh：前言长度=15位）



■ TMPR/RMPR = 10: One-zero pattern
（TPLENRPLEN=4h：前言长度=4位）

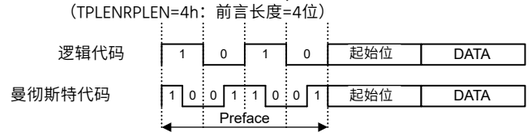


Figure 30.51 前言模式设置示例

(2) 起始位区

这是指示帧中有效数据开始的区域。它添加在前言区域之后。

起始位长度由MMR.SBSEL设置决定。当MMR.SBSEL=“0”时，起始位长度为1位。

当MMR.SBSEL=“1”时，起始位长度为3位。

当MMR.SBSEL=“1”时，SYNC类型可以从命令SYNC和数据SYNC中选择。

命令SYNC意味着三个起始位被添加为一个从1到零的转换。

Data SYNC means the three start bits are added as a zero-to-one transition.

The SYNC type is determined by the MMR.SYNSEL, MMR.SYNVAL and TDRH.TSYNC settings.

(When receiving, the received result is applied to RDRH.RSYNC.)

When MMR.SBSEL = “0”, the start bit is added as a zero-to-one or one-to-zero transition.

The selection is determined by the MMR.SYNVAL setting.

The MMR.SYNSEL bit specifies the destination to be referred to when setting for transmission.

When the MMR.SYNSEL bit is set to 1, the MMR.SYNVAL setting is referred to. When the MMR.SYNSEL bit is set to 0, the TDRH.TSYNC setting is referred to.

Figure 30.52 shows the state of the start bit area according to the settings in the MMR.SYNSEL, MMR.SYNVAL and TDRH.TSYNC registers in the case of transmission. Figure 30.53 shows that in the case of reception.

The start bit(s) is not affected by the MMR.TMPOL or MMR.RMPOL setting.

*d.c.=don't care, Preface=preface area, START=start bit area, Data=user data area, P=parity bit, MP=multi-processor bit, STOP=stop bit

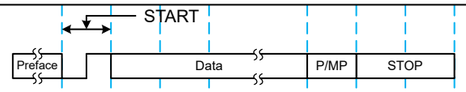
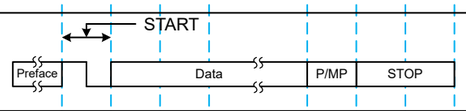
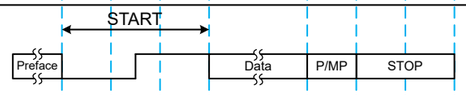
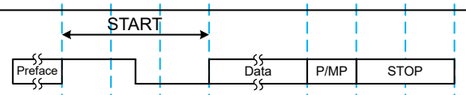
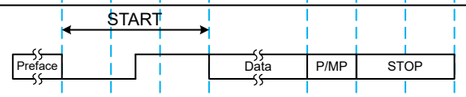
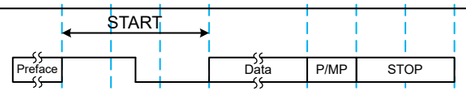
Register setting				Output signal	Output start bit
MMR			TDRHL	Output TXDn waveform	
SBSEL	SYNSEL	SYNVAL	TSYNC		
0	d.c.	0	d.c.		1bit 0 to 1 transition
0	d.c.	1	d.c.		1bit 1->0transition
1	0	0	d.c.		3bit 0to1 transition (DATA SYNC)
1	0	1	d.c.		3bit 1to0 transition (COMMAND SYNC)
1	1	d.c.	0		3bit 0to1 transition (DATA SYNC)
1	1	d.c.	1		3bit 1to0 transition (COMMAND SYNC)

Figure 30.52 Settings Related to and Format of the Start Bit Area at Transmission

数据同步意味着三个起始位被添加为一个零到一的转换。

SYNC类型由MMR.SYNSEL、MMR.SYNVAL和TDRH.TSYNC设置确定。

（接收时，将接收到的结果应用到RDRH.RSYNC。）

当MMR.SBSEL=“0”时，添加起始位作为零到一或一到零的转换。

选择由MMR.SYNVAL设置决定。

MMR.SYNSEL位指定发送设置时要参考的目标。

当MMR.SYNSEL位设置为1时，参考MMR.SYNVAL设置。当MMR.SYNSEL位设置为0时，参考TDRH.TSYNC设置。

图30.52显示了根据MMR.SYNSEL、MMR.SYNVAL和TDRH.TSYNC寄存器在传输的情况下。图30.53显示了接收的情况。

起始位不受MMR.TMPOL或MMR.RMPOL设置的影响。

*d.c.=don'tcare Preface=prefacearea START=startbitarea Data=userdataarea P=parity bit MP=multi-processorbit STOP=stopbit

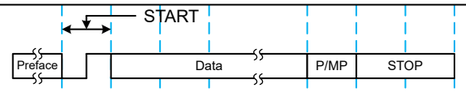
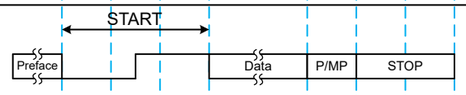
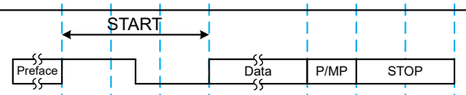
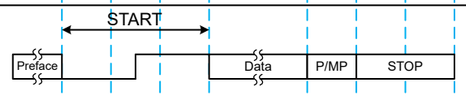
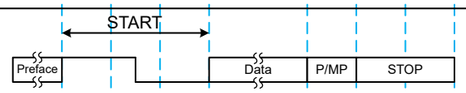
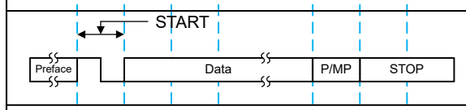
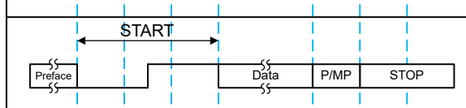
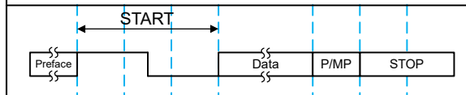
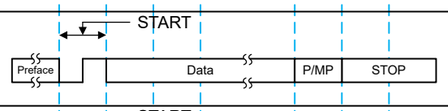
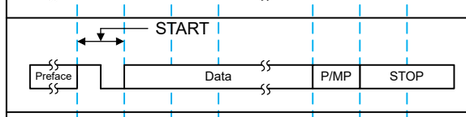
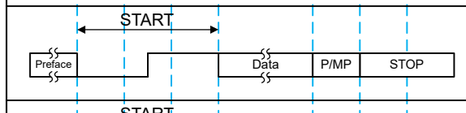
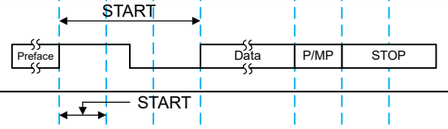
注册设置				输出信号	输出起始位
MMR			TDRHL	输出TXDn波形	
SBSEL	SYNSEL	SYNVAL	TSYNC		
0	d.c.	0	d.c.		1bit0到1转换
0	d.c.	1	d.c.		1bit 1->0transition
1	0	0	d.c.		3bit 0to1 transition (DATA SYNC)
1	0	1	d.c.		3bit 1to0 transition (COMMAND SYNC)
1	1	d.c.	0		3bit 0to1 transition (DATA SYNC)
1	1	d.c.	1		3bit 1to0 transition (COMMAND SYNC)

Figure 30.52 发送时起始位区域的相关设置和格式

When the start bit area is 3 bits long, SYNVAL is not referenced.

d.c. = don't care, Preface = Preface area, START = Start bit area, Data = Data area
P = Parity bit, MP = Multi-processor bit, STOP = Stop bit

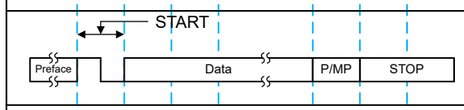
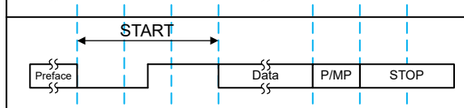
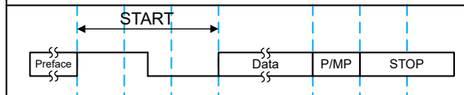
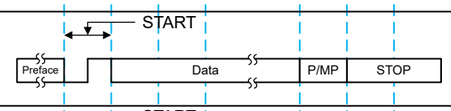
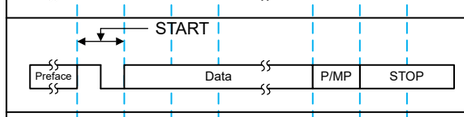
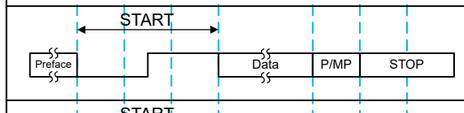
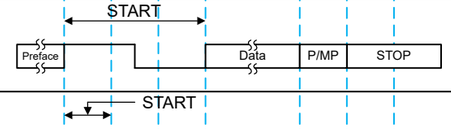
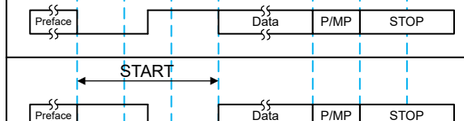
Register setting				Input signal	Start bit detection result*1	Register indication
MMR			TDRH	RXDn input waveform		RDRH.RSYNC
SBSEL	SYNSEL	SYNVAL	TSYNC			
0	d.c.	0	d.c.		Normal start bit (1 bit: 0-to-1 transition)	0
					Start bit error	0
					Start bit error	0
					Start bit error	0
0	d.c.	1	d.c.		Start bit error	0
					Normal start bit (1 bit: 1-to-0 transition)	0
					Start bit error	0
					Start bit error	0
1	d.c.	d.c.	d.c.		Start bit error	0
					Start bit error	0
					Data SYNC	0
					Command SYNC	1

Note 1. Data other than the start bit is assumed to be normal.

Figure 30.53 Settings Related to and Judgment of the Start Bit Area at Reception

当起始位区域为3位长时，不引用SYNVAL。

直流电=don'tcare Preface=Prefacearea START=Startbitarea Data=DataareaP=Paritybit
MP=Multi-processorbit STOP=Stopbit

注册设置				输入信号	起始位检测结果*1	登记指示
MMR			TDRH	RXDn输入波形		RDRH.RSYNC
SBSEL	SYNSEL	SYNVAL	TSYNC			
0	d.c.	0	d.c.		正常起始位（1位：0到1转换）	0
					起始位错误	0
					起始位错误	0
					起始位错误	0
0	d.c.	1	d.c.		起始位错误	0
					正常起始位（1位：1到0转换）	0
					起始位错误	0
					起始位错误	0
1	d.c.	d.c.	d.c.		起始位错误	0
					起始位错误	0
					数据同步	0
					Command SYNC	1

注1.假设起始位以外的数据正常。

Figure 30.53 接收时起始位区域的相关设置和判断

RA生态工作室

(3) DATA

Since the format of the data area is the same as that of the asynchronous mode, see section 30.3.1. Serial Data Transfer Format.

As shown in Figure 30.49, Frame Format in Manchester Mode, the stop bit is not included in the Manchester encoding range.

30.5.2 Clock

As the transfer clock in Manchester mode, the clock generated by the on-chip baud rate generator is used by setting the SMR.CKS[1:0] bit.

Also it is possible to set the oversampling (transfer rate of one-bit period) by SEMR.ABCS bit.

When the SMER.ABCS bit is set to 0, oversampling x16 is selected with the one-bit period being 16 cycles of the base clock. When the SMER.ABCS bit is set to 1, oversampling x8 is selected with the one-bit period being 8 cycles of the base clock.

30.5.3 Initialization of the SCI in Manchester Mode

Before transferring data, write the initial value (00h) to the SCR register and initialize the SCI following the example of flowchart shown in Figure 30.54.

Whenever the operating mode or transfer format is changed, the SCR register must be initialized before the change is made.

Note that setting the SCR.RE bit to 0 initializes none of: the ORER, FER, PER, MER, RDRF, and RDF flags in the SSR register, the SYER, PFER and SBER flags in the MESR register, and the RDR, RDRH, and RDRL registers.

Note also that switching the value of SCR.TE from 0 to 1 when SCR.TIE is 1 generates a TXI interrupt request.

(3) DATA

由于数据区的格式与异步模式相同，见30.3.1节。串行数据传输
Format.

如图30.49，曼彻斯特模式下的帧格式，停止位不包含在曼彻斯特编码范围内。

30.5.2 Clock

作为曼彻斯特模式下的传输时钟，片内波特率发生器产生的时钟用于设置
SMR.CKS[1:0] bit.

也可以通过SEMR.ABCS位设置过采样（一位周期的传输率）。

当SMER.ABCS位设置为0时，选择过采样x16，一位周期为基本时钟的16个周期。当SMER.ABCS位设置为1时，选择过采样x8，一位周期为基本时钟的8个周期。

30.5.3 曼彻斯特模式下SCI的初始化

在传输数据之前，将初始值（00h）写入SCR寄存器并按照图30.54所示的流程图示例初始化SCI。

每当改变操作模式或传输格式时，必须在改变之前初始化SCR寄存器。

请注意，将SCR.RE位设置为0不会初始化以下各项：SSR寄存器中的ORER、FER、PER、MER、RDRF和RDF标志，MESR寄存器中的SYER、PFER和SBER标志，以及RDR、RDRH 和RDRL寄存器。

另请注意，当SCR.TIE为1时，将SCR.TE的值从0切换到1会产生TXI中断请求。

RA生态工作室

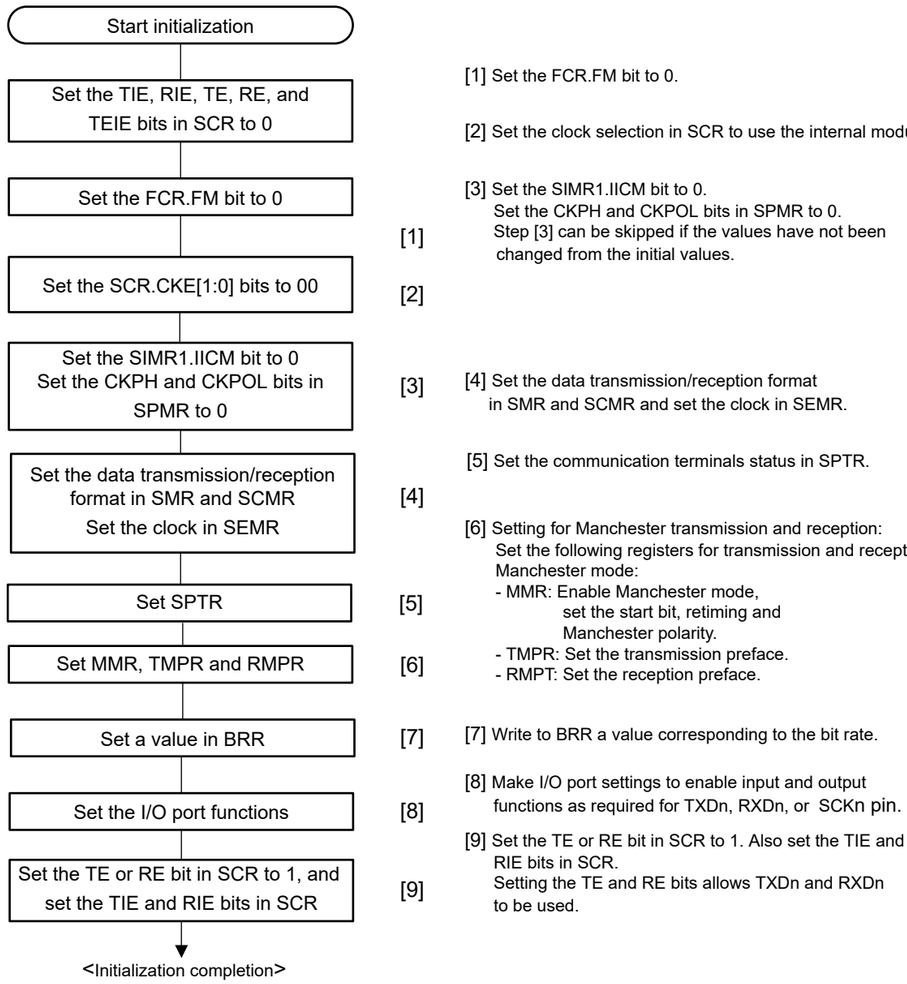


Figure 30.54 SCI Initialization Flow in Manchester Mode

30.5.4 Double-speed operation

When the ABCS bit in SEMR is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0.

When the BGDM bit in SEMR is set to 1, the cycle of the base clock is reduced to half and the SCI operates on the bit rate twice that of when ABCS is set to 0.

When the ABCS and the BGDM bits in SEMR are set to 1, the SCI operates on the bit rate four times that of when the ABCS and the BGDM bits in SEMR are set to 0.

30.5.5 CTS and RTS functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the CTSE bit in SPMR to 1 enables the CTS function. The CTSn_RTSn pin can be set as a multiplexed pin which allows one pin to be used for either function, or as dedicated pins with each pin for a single function. Use the CTSPEN bit in SPMR for this setting.

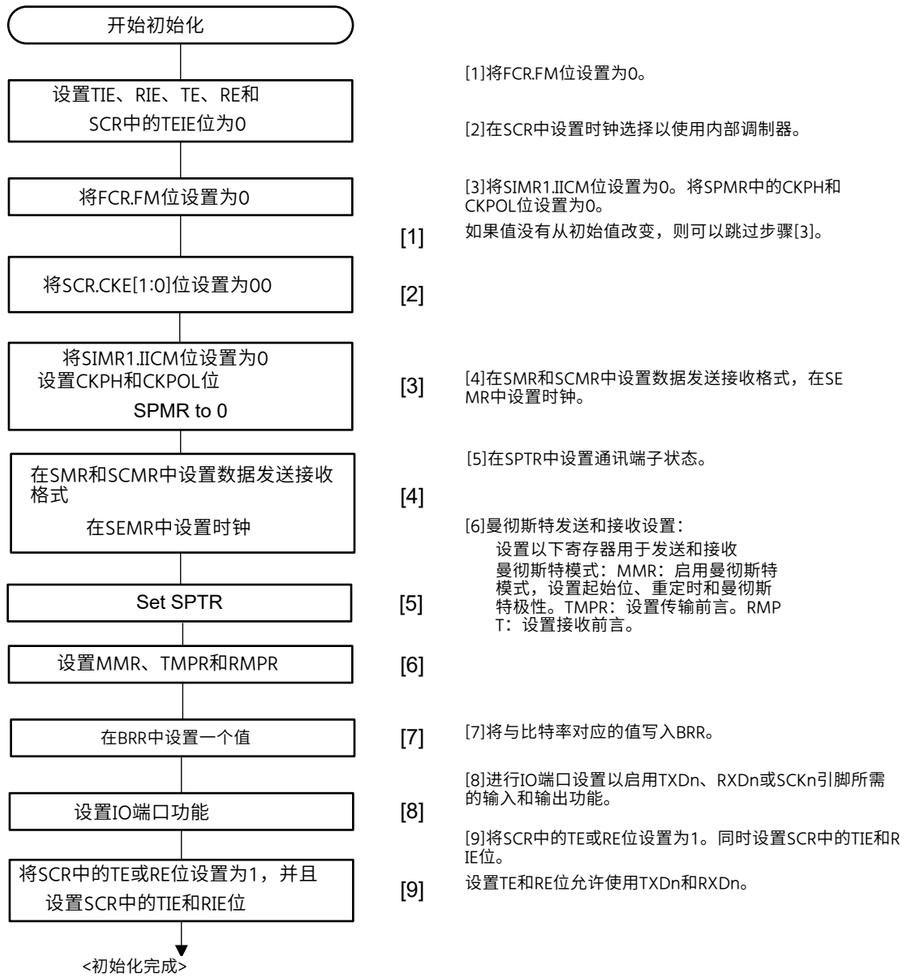


Figure 30.54 曼彻斯特模式下的SCI初始化流程

30.5.4 Double-speed operation

当SEMR中的ABCS位设置为1并选择1位周期的8个基本时钟脉冲时，SCI以ABCS设置为0时的两倍比特率运行。

当SEMR中的BGDM位设置为1时，基本时钟的周期减少到一半，SCI的比特率是ABCS设置为0时的两倍。

当SEMR中的ABCS和BGDM位设置为1时，SCI以四倍的比特率运行。
SEMR中的ABCS和BGDM位设置为0。

30.5.5 CTS和RTS功能

CTS功能在传输控制中使用CTSn_RTSn引脚上的输入。将SPMR中的CTSE位设置为1使能CTS功能。CTSn_RTSn管脚可以设置为多路复用管脚，允许一个管脚用于任一功能，或作为专用管脚，每个管脚用于单一功能。使用SPMR中的CTSPEN位进行此设置。

When the CTS function is enabled, reception starts only when the CTSn_RTSn pin is at the low level.

Applying a high level to the CTSn_RTSn pin after transmission starts does not affect transmission of the current frame, which continues.

The RTS function uses output on the CTSn_RTSn pin to request transmission. When the SCI is ready to receive, it outputs a low level to the CTSn_RTSn pin, Conditions for output of the low level and high level are as follows:

[Conditions for low-level output]

When all conditions listed below are satisfied:

- The value of the RE bit in SCR is 1.
- The SCI is ready to receive.
- There is no received data yet to be read.
- All of the following flags are set to 0: SSR.ORER, FER, PER and MER flags, and MESR.SYER (when SYEREN = 1), PFER (when PFEREN = 1) and SBER flags (when SBEREN = 1).

[Conditions for high-level output]

- When the conditions for low output are not satisfied

30.5.6 Serial data transmission in Manchester mode

The SCI encodes data in Manchester encoding and sends the resultant data in Manchester mode.

When the polarity setting (MR.TMPOL) set to 0, logic 0 is coded as a zero-to-one transition in Manchester code and logic 1 is coded as a one-to-zero transition in Manchester code.

When the polarity setting (MR.TMPOL) set to 1, logic 0 is coded as a one-to-zero transition in Manchester code and logic 1 is coded as a zero-to-one transition in Manchester code.

For this reason, a level transition occurs with the Manchester encoded data in the middle of individual logic data. (See Figure 30.49).

The transmitter constructs transmit frames in a specific format by adding a preface area to data and setting the start bit(s) according to the polarity setting and sends resultant serial data.

For details on the frame format, see section 30.5.1. Frame Format.

Figure 30.55 shows the flowchart in transmission. Figure 30.56, Figure 30.57, and Figure 30.58 show examples of the operation for serial transmission in Manchester mode.

当CTS功能使能时，只有在CTSn_RTSn引脚为低电平时才开始接收。

传输开始后将高电平应用到CTSn_RTSn引脚不会影响当前帧的传输，当前帧会继续传输。

RTS功能使用CTSn_RTSn引脚上的输出来请求传输。当SCI准备好接收时，向CTSn_RTSn管脚输出一个低电平，输出低电平和高电平的条件如下：

[Conditions for low-level output]

当满足下列所有条件时：

●SCR中RE位的值为1。

●SCI已准备好接收。

●没有接收到的数据尚未读取。

●以下所有标志都设置为0：SSR.ORER、FER、PER和MER标志，以及MESR.SYER（当SYEREN=1时）、PFER（当PFEREN=1时）和SBER标志（当SBEREN=1时）。

[Conditions for high-level output]

●不满足低输出条件时

30.5.6 曼彻斯特模式下的串行数据传输

SCI以曼彻斯特编码对数据进行编码，并以曼彻斯特模式发送结果数据。

当极性设置(MR.TMPOL)设置为0时，逻辑0被编码为曼彻斯特代码中的零到一转换，逻辑1被编码为曼彻斯特代码中的一到零转换。

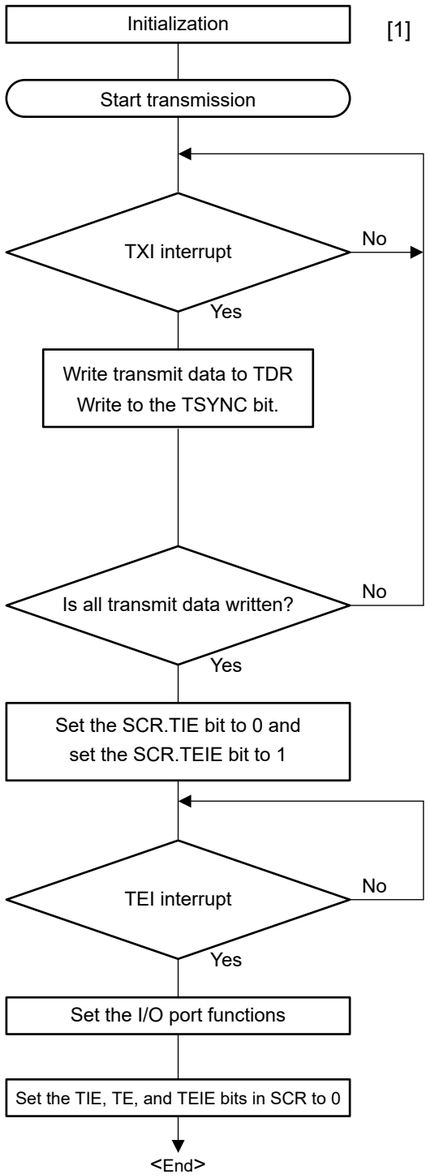
当极性设置(MR.TMPOL)设置为1时，逻辑0被编码为曼彻斯特代码中的一对零转换，逻辑1被编码为曼彻斯特代码中的零到一转换。

出于这个原因，在各个逻辑数据中间的曼彻斯特编码数据会发生电平转换。（看Figure 30.49).

发送器通过向数据添加前言区域并根据极性设置设置起始位来构建特定格式的发送帧，并发送结果串行数据。

有关帧格式的详细信息，请参见第30.5.1节。帧格式。

图30.55显示了传输中的流程图。图30.56、图30.57和图30.58显示了曼彻斯特模式下串行传输的操作示例。



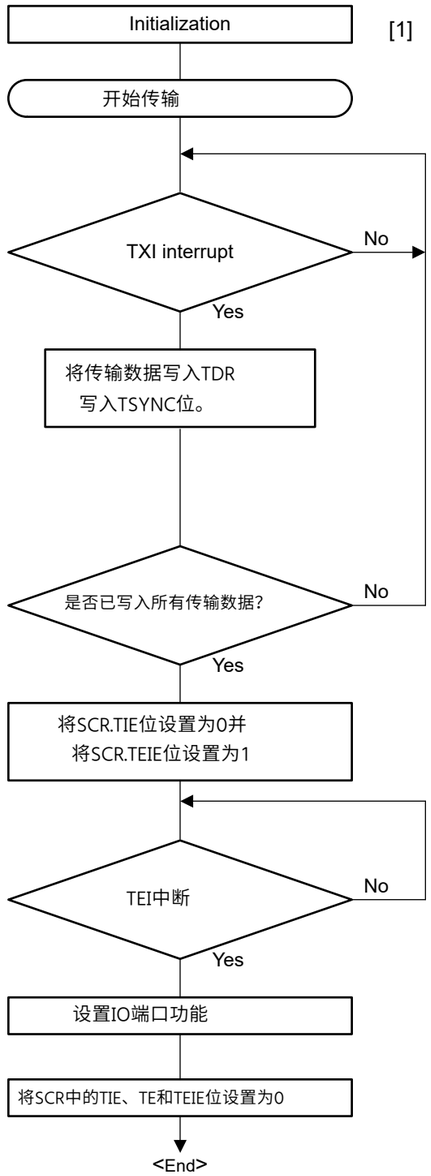
[1] SCI Initialization:
Set data transmission.
Setting the SCR.TE bit to 1 enables transmission.

[2] TXI interrupt:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (TXI) request is generated.

[3] TDR setting:
Write the transmit data to TDR.
When TSYNC is used, also set TDRHL.TYSNC.

[4] Serial transmission continuation procedure:
To continue serial transmission, write the transmit data to TDR once by using an TXI interrupt.
The transmit data can also be written to TDR by activating the DMAC or DTC in the TXI interrupt request.
When TEI interrupt requests are used, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

Figure 30.55 Example of Serial Transmittion Flowchart in Manchester Mode



[1] SCI Initialization:
设置数据传输。将SCR.TE位
设置为1可启用传输。

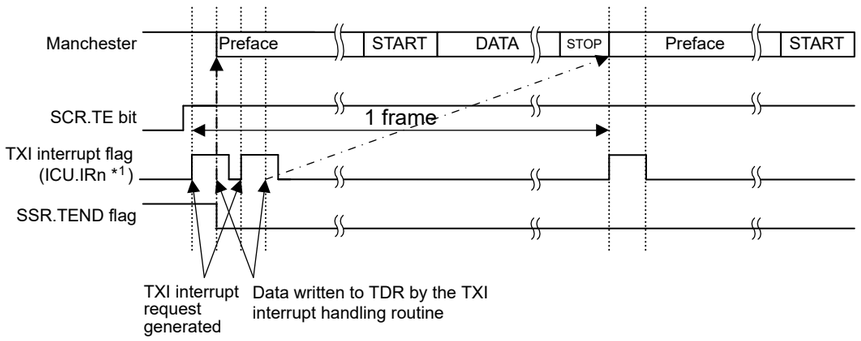
[2]TXI中断：当发送数据从TDR传输到TSR时，会产生发送数据空中断(TXI)请求。

[3] TDR setting:
将发送数据写入TDR。
使用TSYNC时，还要设置TDRHL.TYSNC。

[4] 串行传输继续过程：要继续串行传输，使用TXI中断将传输数据写入TDR一次。也可以通过激活TXI中断请求中的DMAC或DTC将发送数据写入TDR。
当使用TEI中断请求时，设置

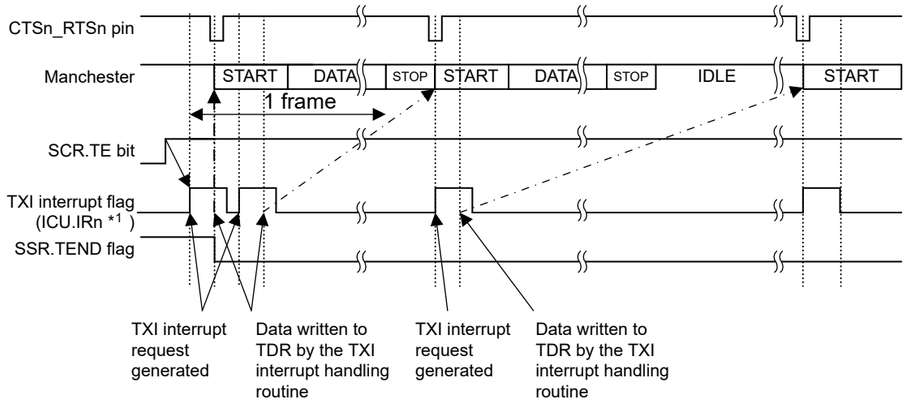
在将要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

Figure 30.55 曼彻斯特模式下的串行传输流程图示例



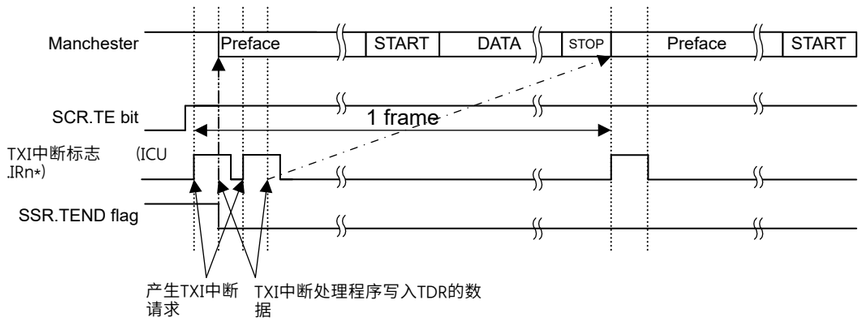
Note 1. For corresponding interrupt numbers, see section 13, Interrupt Controller Unit (ICU)

Figure 30.56 Example of Start-of-Transmission Operation for Serial Transmission in Manchester mode (with Preface but Without the CTS Function)



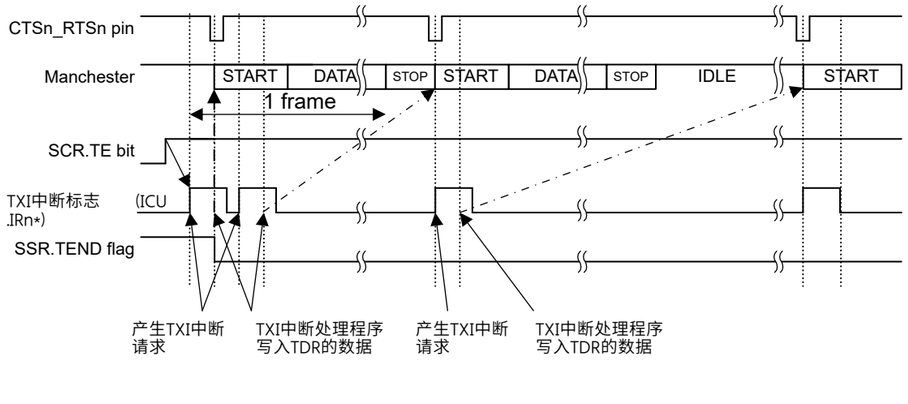
Note 1. For corresponding interrupt numbers, see section 13, Interrupt Controller Unit (ICU)

Figure 30.57 Example of Start-of-Transmission Operation for Serial Transmission in Manchester Mode (Without Preface but with the CTS Function)



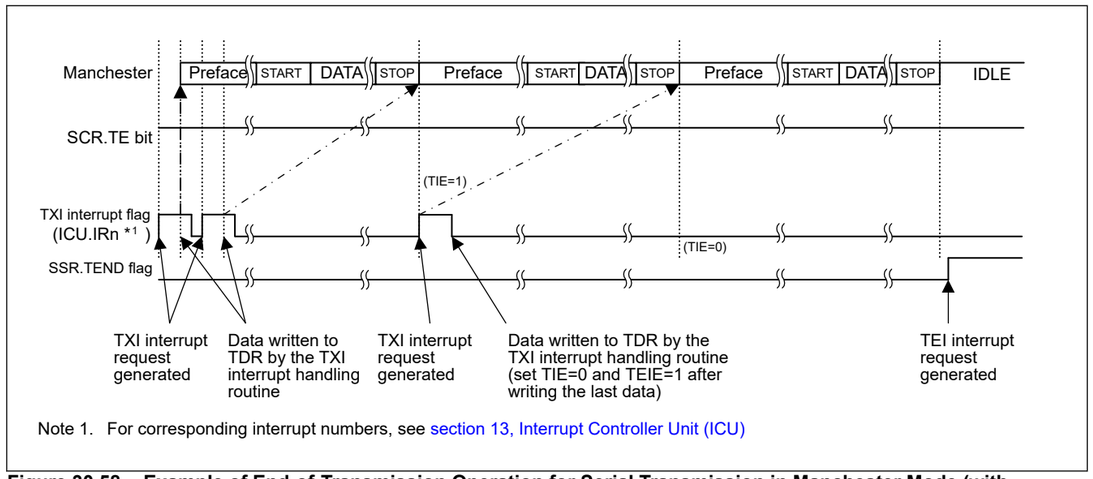
注1.有关相应的中断号，请参阅第13节，中断控制器单元(ICU)

Figure 30.56 曼彻斯特模式下串行传输的传输开始操作示例（使用前言但没有CTS功能）



注1.有关相应的中断号，请参阅第13节，中断控制器单元(ICU)

Figure 30.57 曼彻斯特模式下串行传输的传输开始操作示例（无序但具有CTS功能）



Note 1. For corresponding interrupt numbers, see section 13, Interrupt Controller Unit (ICU)

Figure 30.58 Example of End-of-Transmission Operation for Serial Transmission in Manchester Mode (with Preface but Without the CTS Function)

30.5.7 Serial Data Reception in Manchester Mode

In Manchester mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate. Reception starts by sampling the falling edges of received data at the base clock. As shown in Figure 30.59, reception starts at a falling edge of the received data and it continues if the received data keeps low for the duration of 1/4 bit. If the received data goes high within the duration of 1/4 bit, the SCI judges it as an error and waits for a falling edge again.

If a high level is expected in the first half of a bit in the received data, the SCI judges a low level that continues for one base clock cycle as an error and ignores the change to the low level.

Note 1. This is the case when SEMR.ABCS = 0. When SEMR.ABCS = 1, the SCI operates on a base clock with a frequency of 8 times the bit rate.

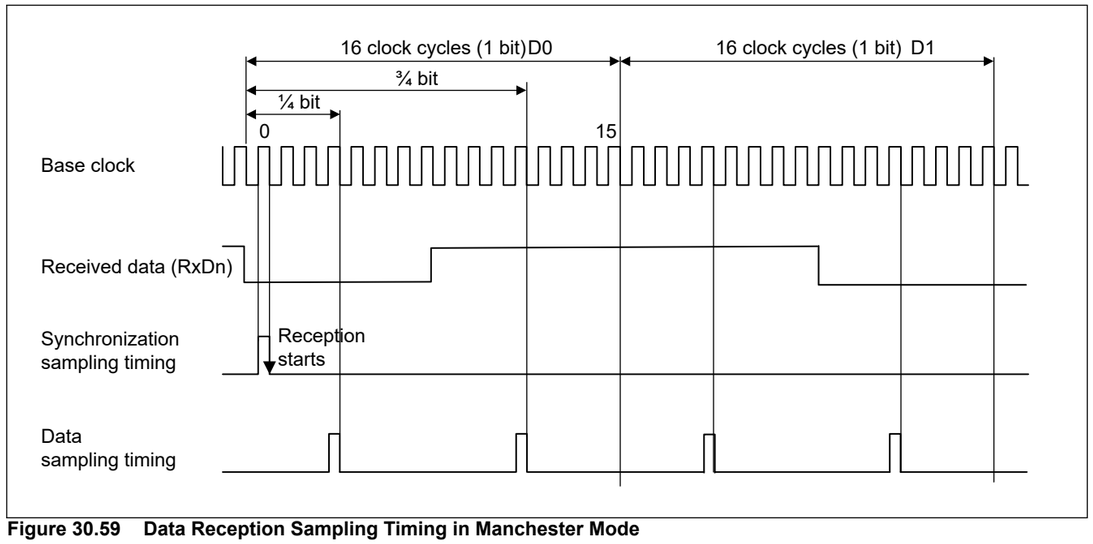
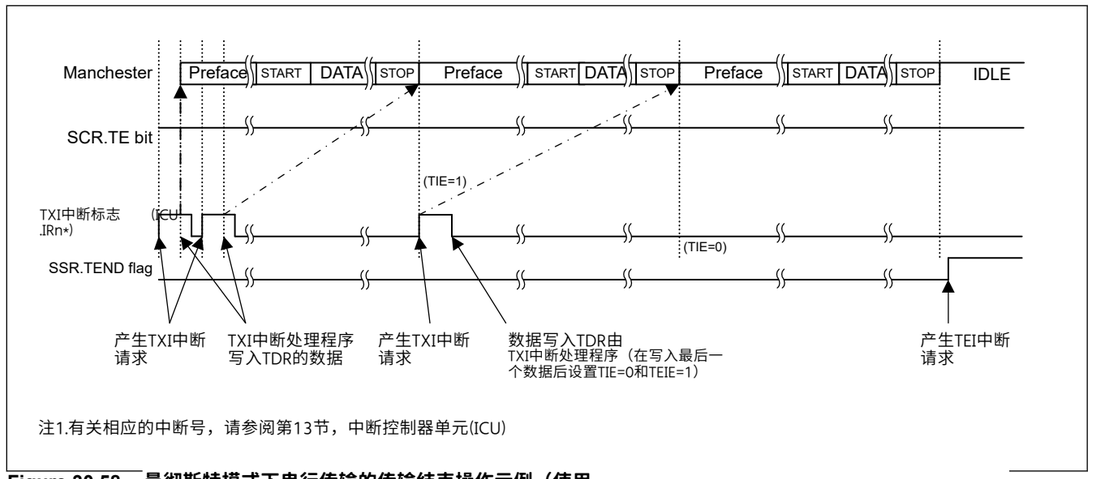


Figure 30.59 Data Reception Sampling Timing in Manchester Mode

In Manchester mode, data reception starts with detection of a preface and start bit area.

The SCI checks the input from the RXDn pin to see whether a preface is added based on the value of RMPR.RPLEN.

If the preface is disabled (RMPR.RPLEN = 0), it moves on to the detection of a start bit area without detecting a preface.



注1.有关相应的中断号，请参阅第13节，中断控制器单元(ICU)

Figure 30.58 曼彻斯特模式下串行传输的传输结束操作示例（使用前言但没有CTS功能）

30.5.7 曼彻斯特模式下的串行数据接收

在曼彻斯特模式下，SCI在频率为16倍*1比特率的基本时钟上运行。接收开始于在基本时钟处对接收到的数据的下降沿进行采样。如图30.59所示，接收在接收数据的下降沿开始，如果接收数据保持低电平持续14位，则继续接收。如果接收到的数据在14bit的时间内变高，则SCI判断为错误，再次等待下降沿。

如果在接收数据的前半个比特中预期为高电平，则SCI将持续一个基本时钟周期的低电平判断为错误，并忽略向低电平的变化。

注1.这是SEMR.ABCS=0时的情况。当SEMR.ABCS=1时，SCI在频率为比特率8倍的基本时钟上运行。

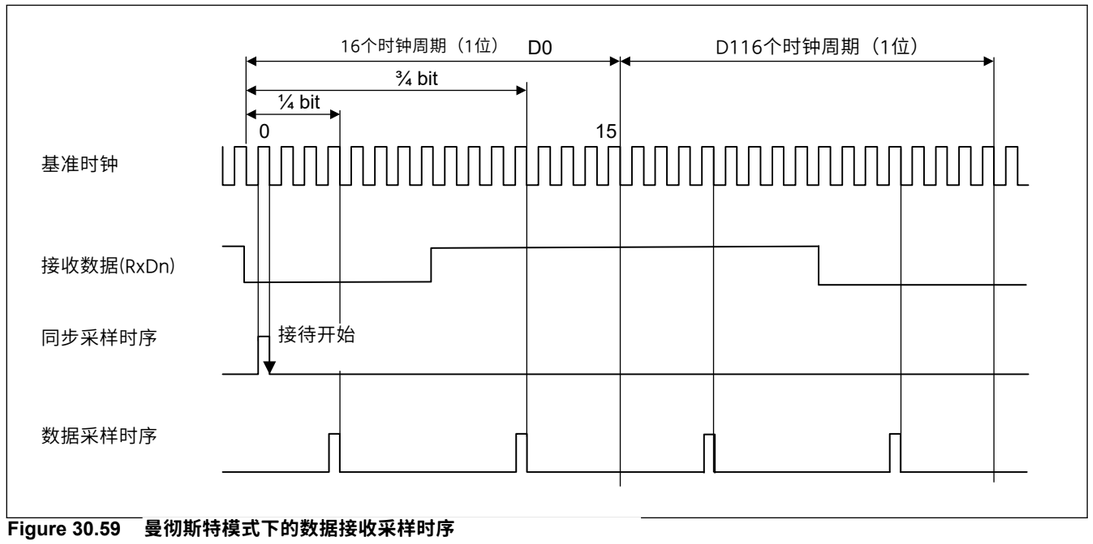


Figure 30.59 曼彻斯特模式下的数据接收采样时序

在曼彻斯特模式下，数据接收从检测前言和起始位区域开始。

SCI检查来自RXDn引脚的输入，以查看是否根据RMPR.RPLEN的值添加了前言。

如果前言被禁用（RMPR.RPLEN=0），它会继续检测起始位区域而不检测前言。

When a preface is enabled, it identifies a preface pattern setting according to the set value in RMPR.RPPAT, and compares it with the RXDn input for a pattern match to detect a preface pattern.

Upon detection of a preface pattern match, it judges it as a normal preface and moves on to the detection of a start bit area.

If detecting a preface pattern mismatch or a Manchester code error in the preface area, it judges it as a preface error and asserts a preface error (PFER).

For start bit detection, the SCI selects an expected value based on the register settings (MMR.SBSEL and SYNVAL), compares it with the RXDn input for a pattern match to detect a start bit area. Upon detection of a start bit pattern match, it judges it as a normal start bit area and moves on to the data processing.

Only when a preface and a start bit area are detected normally, it moves on to the next phase of data reception.

Upon detection of a start bit pattern mismatch, it asserts a start bit error flag (SBER).

In data processing, the SCI shifts the data by the expected received data length based on the register settings (SCMR.CHR1 and SMR.CHR) through the RSR register. If two sampling points in a bit of the received data are identical, the SCI judges this as a Manchester code error.

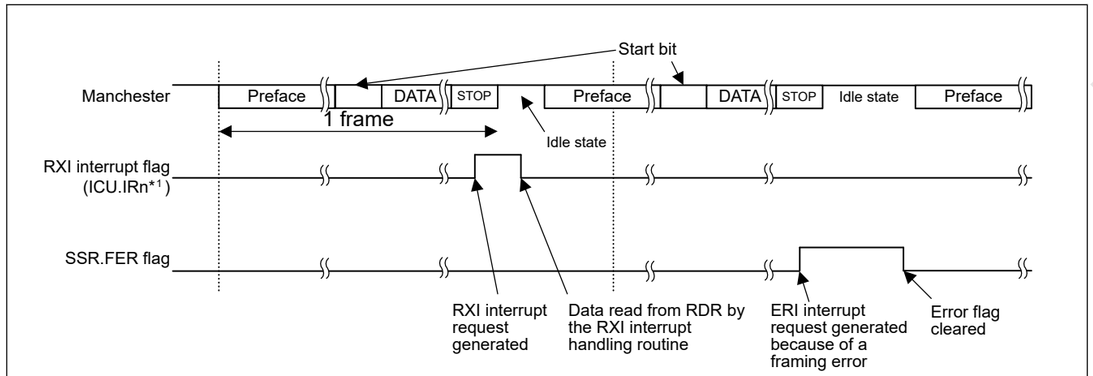
For details, see para. (4) in section 30.5.11. Errors in Manchester Mode.

When the parity function is disabled (SMR.PE = 0), the SCI moves on to the next phase of stop bit detection. When the parity function is enabled (SMR.PE = 1), the SCI performs parity checking. If detecting a parity error, it asserts a parity error flag (PER), and then moves on to stop bit detection.

In stop bit detection, the SCI checks the following in the stop bit area of the received frame:

It has two sampling points in a bit. If both points are at the high level, the bit is recognized as a normal stop bit and the data is stored in the RDR register. At least one low-level point is judged as an abnormal stop bit, causing a framing error flag (FER) to be set. Even when an error is detected, the received data is stored in the RDR register as abnormal data.

Figure 30.60 shows an example of the operation for serial data reception in Manchester mode.



Note 1. For corresponding interrupt numbers, see section 13, Interrupt Controller Unit (ICU).

Figure 30.60 Example of Operation for Serial Data Reception in Manchester mode (with a Preface)

For the state of each status flag in the SSR register and RXDn input processing when a receive error is detected, see section 30.5.11. Errors in Manchester Mode.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated.

Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, PER, MER, SYER*1, PFER*1, and SBER*1 flags to 0 before resuming reception. Also, be sure to read the RDR (or RDRL) register during overrun error processing. When a reception is forcibly terminated by setting the SCR.RE bit to 0 during operation, read the RDR (or the RDRL) register because received data which has not yet been read may be left in the RDR (or the RDRL) register.

Figure 30.61 and Figure 30.62 show examples of serial data reception flowchart in Manchester mode.

Note 1. Effective when the corresponding bit is enabled.

启用前言时，它根据RMPR.RPPAT中的设置值识别前言模式设置，并将其与模式匹配的RXDn输入进行比较，以检测前言模式。

在检测到前言模式匹配时，将其判断为正常前言并继续检测起始位区域。

如果在前言区域检测到前言模式不匹配或曼彻斯特码错误，则将其判断为前言错误并断言前言错误（PFER）。

对于起始位检测，SCI根据寄存器设置（MMR.SBSEL和SYNVAL）选择预期值，将其与模式匹配的RXDn输入进行比较，以检测起始位区域。在检测到起始位模式匹配时，将其判断为正常起始位区域并继续进行数据处理。

只有在正常检测到前言和起始位区域时，才进入下一个数据接收阶段。

在检测到起始位模式不匹配时，它会断言起始位错误标志(SBER)。

在数据处理中，SCI根据寄存器设置（SCMR.CHR1和SMR.CHR）通过RSR寄存器将数据移位预期的接收数据长度。如果接收到的数据位中的两个采样点相同，则SCI判断为曼彻斯特码错误。

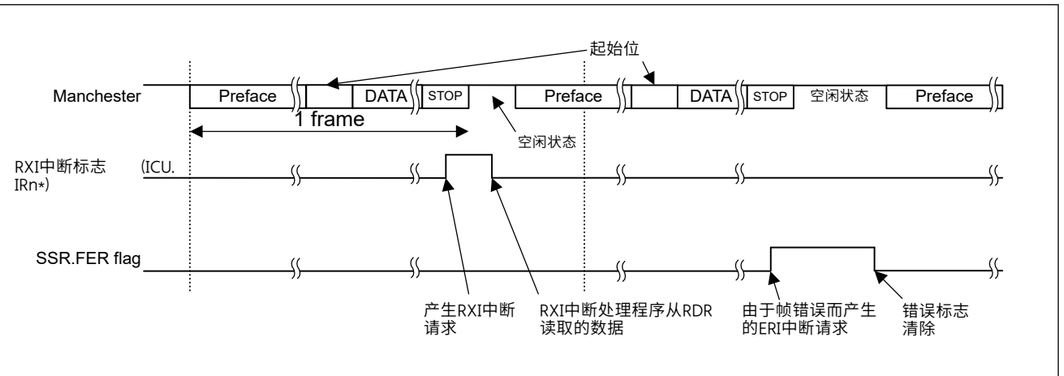
有关详细信息，请参阅段落。(4)在第30.5.11节中。曼彻斯特模式中的错误。

当奇偶校验功能被禁用（SMR.PE=0）时，SCI进入下一个停止位检测阶段。当启用奇偶校验功能时（SMR.PE=1），SCI执行奇偶校验。如果检测到奇偶校验错误，它会置位奇偶校验错误标志(PER)，然后继续进行停止位检测。

在停止位检测中，SCI在接收帧的停止位区域中检查以下内容：

它有两个采样点。如果两个点都处于高电平，则该位被识别为正常停止位，数据存储在RDR寄存器中。至少有一个低电平点被判断为异常停止位，导致设置帧错误标志（FER）。即使检测到错误，接收到的数据也会作为异常数据存储在RDR寄存器中。

图30.60显示了曼彻斯特模式下串行数据接收操作的示例。



注1.有关相应的中断号，请参阅第13节，中断控制器单元(ICU)。

Figure 30.60 曼彻斯特模式下串行数据接收操作示例（附前言）

关于SSR寄存器中各状态标志的状态以及检测到接收错误时的RXDn输入处理，请参阅30.5.11节。曼彻斯特模式中的错误。

如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。

当接收错误标志为1时，无法恢复数据接收。因此，在恢复接收之前将ORER、FER、PER、MER、SYER*1、PFER*1和SBER*1标志设置为0。此外，请务必在溢出错误处理期间读取RDR（或RDRL）寄存器。如果在操作期间通过将SCR.RE位设置为0来强制终止接收，请读取RDR（或RDRL）寄存器，因为尚未读取的接收数据可能留在RDR（或RDRL）寄存器中。

图30.61和图30.62显示了曼彻斯特模式下的串行数据接收流程图示例。

注1.当相应位使能时有效。

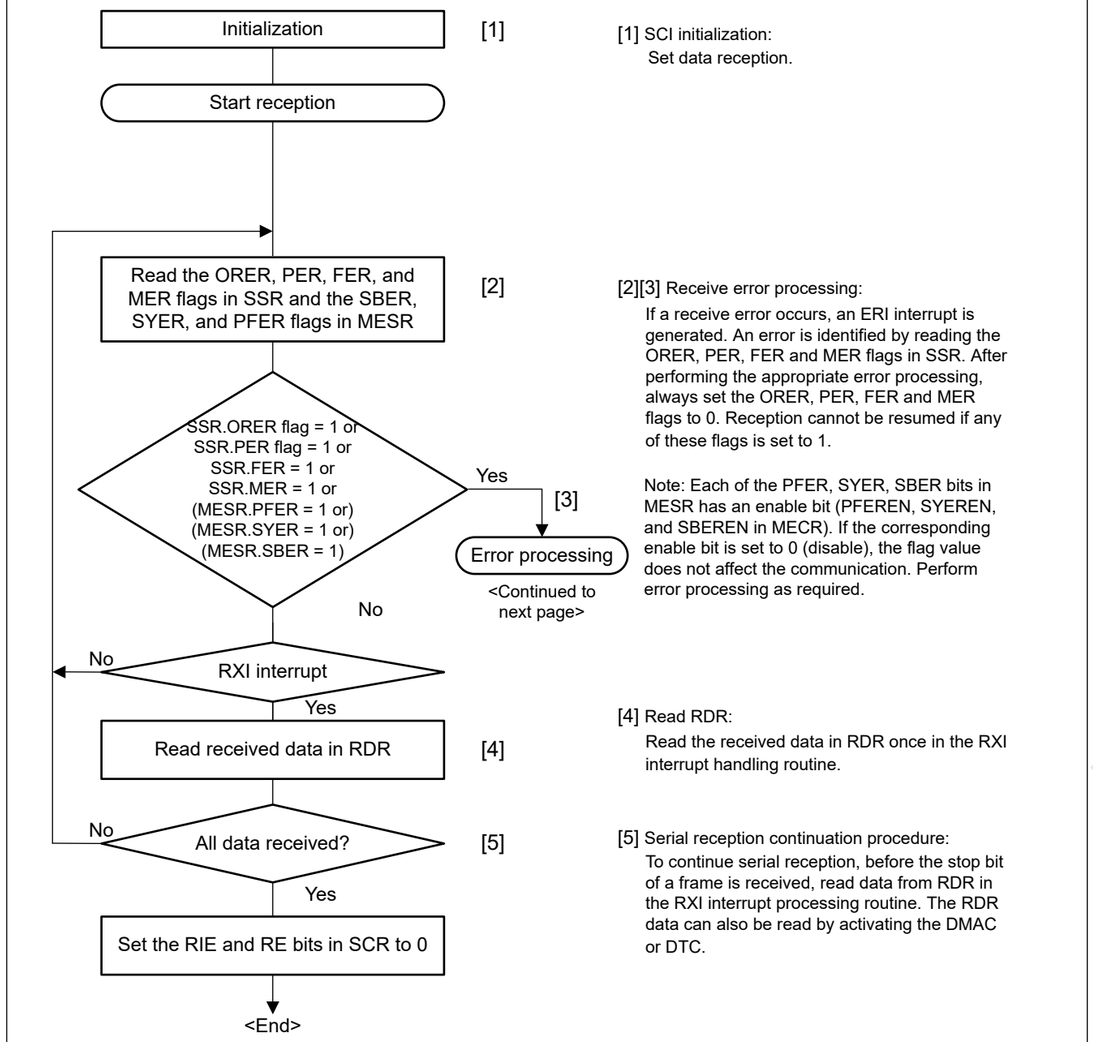


Figure 30.61 Example of Serial Data Reception Flowchart in Manchester Mode (Normal Reception)

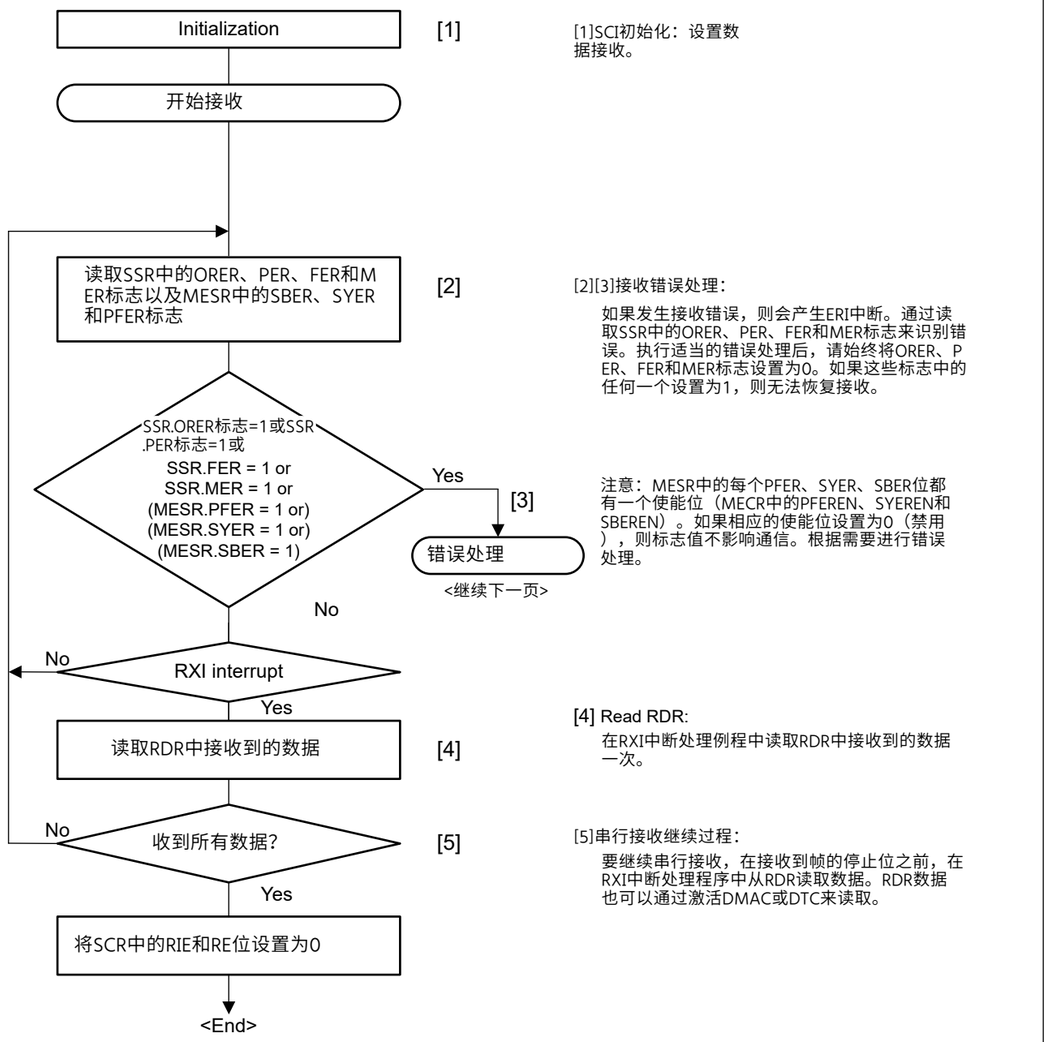


Figure 30.61 曼彻斯特模式下的串行数据接收流程图示例（正常接收）

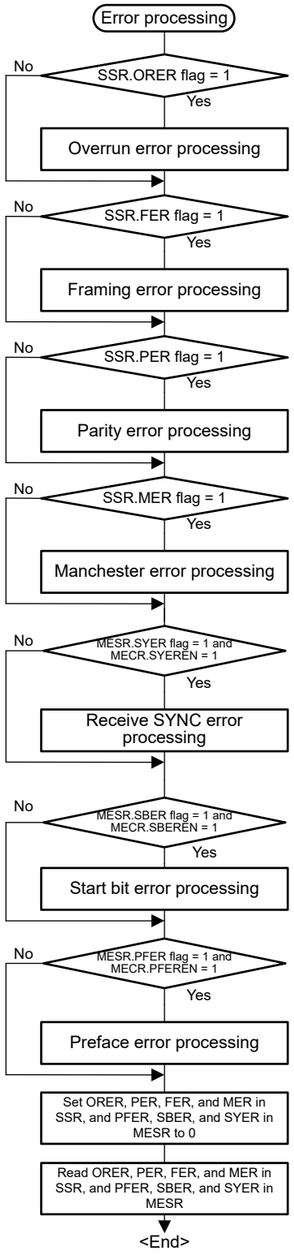


Figure 30.62 Example of Serial Reception Flowchart in Manchester Mode (Error Processing)

30.5.8 Operation When Multi-Processor Bit Is Used

See section 30.4. Multi-Processor Communication Function (1) for the operation in Manchester mode when using multi-processor mode because the operation is the same.

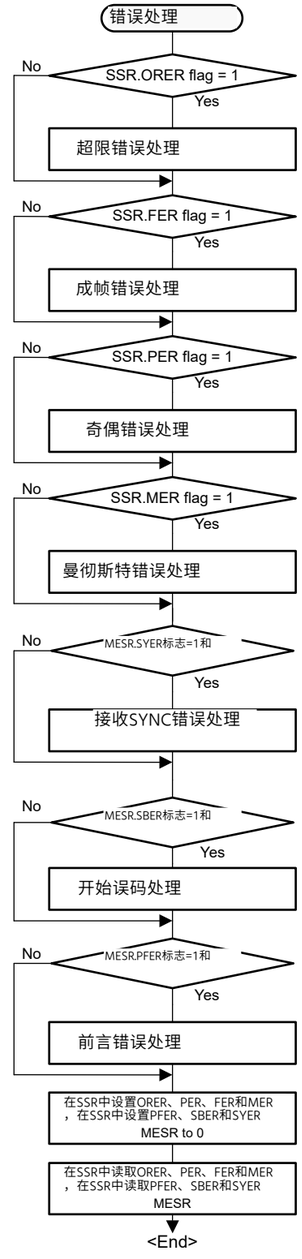


Figure 30.62 曼彻斯特模式下的串行接收流程图示例（错误处理）

30.5.8 使用多处理器位时的操作

请参阅第30.4节。多处理器通信功能(1)曼彻斯特模式下的操作在使用多处理器模式时因为操作是一样的。

A preface and a start bit area are added to the frame format in Manchester mode. See Figure 30.62 for error processing in Manchester mode for the reception flowchart (Figure 30.46). Refer to Table 30.35 for the operation status when detecting various errors.

30.5.9 Receive Retiming

This function corrects the timing for each central edge of the bit, taking advantage of the fact that each bit has an edge in the center in Manchester code.

The receive retiming function can be turned on or off by setting the ERTEN bit in the MMR register.

When the receive retiming function is turned off (MMR.ERTEN = 0), retiming is not performed, causing misalignment between the internal clock and the RXDn input to be accumulated and the receive margin to be reduced.

When the receive retiming function is turned on (MMR.ERTEN = 1), retiming is performed for the preface area, the start bit area*1, and the data area (excluding the stop bit).

Note 1. Retiming is not performed for the start bit area if the preface length is 0 and the start bit length is 3.

As an example, the receive retiming when oversampling x16 is selected is shown below.

When detecting an RXDn input edge two to four cycles before the expected receive cycle, the receive processing is shortened by one sampling CLK cycle.

When detecting a RXDn input edge two to three cycles after the expected receive cycle, the receive processing is extended by one sampling CLK cycle.

(Even if the clock is misaligned with the data by more than two cycles, one cycle is corrected for each bit.)

Figure 30.63 shows the conceptual image of receive retiming range.

When detecting an edge in the tolerance area in the figure, data is received as is without making correction.

When detecting an edge in the SyncJump area in the figure, data is corrected for reception.

When detecting an edge in the SyncError area in the figure, data is received as abnormal data with no correction made.

For a Manchester code error (data matches at the 1/4-phase and 3/4-phase sampling points), the SCI reports a code error.

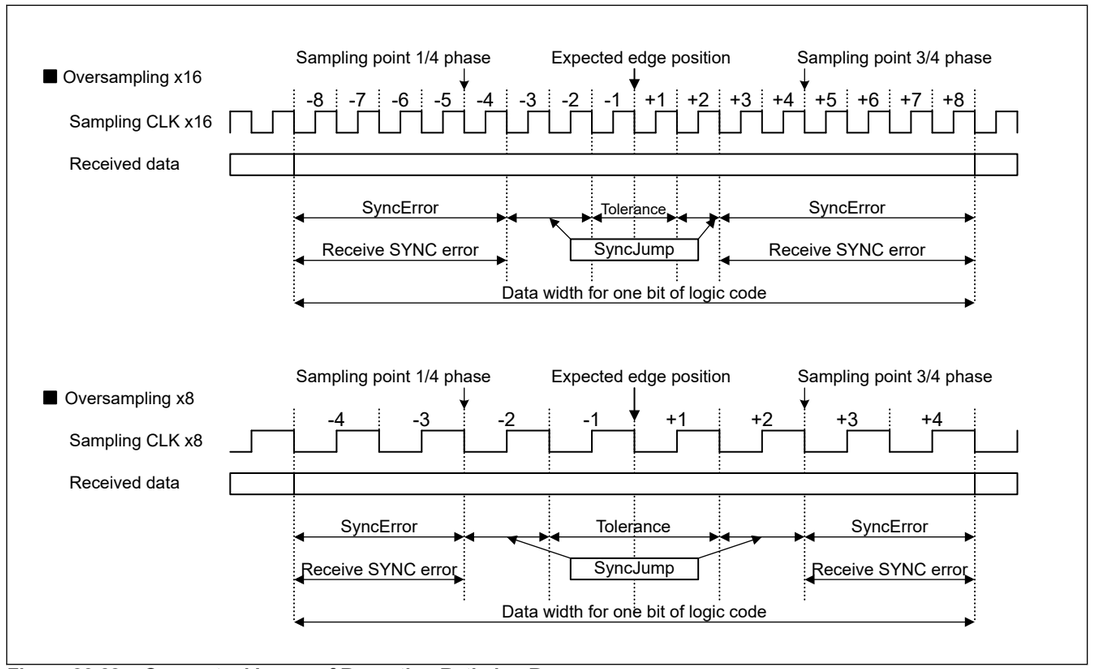


Figure 30.63 Conceptual Image of Reception Retiming Range

曼彻斯特模式的帧格式中添加了前言和起始位区域。接收流程图（图30.46）在曼彻斯特模式下的错误处理见图30.62。检测各种错误时的动作状态见表30.35。

30.5.9 接收重定时

该函数利用曼彻斯特码中每个位在中心的边缘这一事实，校正位的每个中心边沿的时序。

通过设置MMR寄存器中的ERTEN位可以打开或关闭接收重定时功能。

当接收重定时功能关闭时（MMR.ERTEN=0），不执行重定时，导致内部时钟和RXDn输入之间的错位累积，接收裕量减小。

当接收重定时功能打开时（MMR.ERTEN=1），对前言区、起始位区*1和数据区（不包括停止位）执行重定时。

注1.如果序言长度为0且起始位长度为3，则不对起始位区域执行重定时。

例如，选择过采样x16时的接收重定时如下所示。

当在预期接收周期前2到4个周期检测到RXDn输入边沿时，接收处理将缩短1个采样CLK周期。

当在预期接收周期后两到三个周期检测到RXDn输入边沿时，接收处理将延长一个采样CLK周期。

（即使时钟与数据的偏差超过两个周期，也会为每一位校正一个周期。）

图30.63显示了接收重定时范围的概念图。

在图中的公差范围内检测边缘时，直接接收数据而不进行校正。

当在图中的SyncJump区域检测到边缘时，数据被校正以进行接收。

当在图中的SyncError区域检测到边缘时，数据作为异常数据接收，没有进行校正。

对于曼彻斯特编码错误（数据在1个4相和3个4相采样点匹配），SCI报告编码错误。

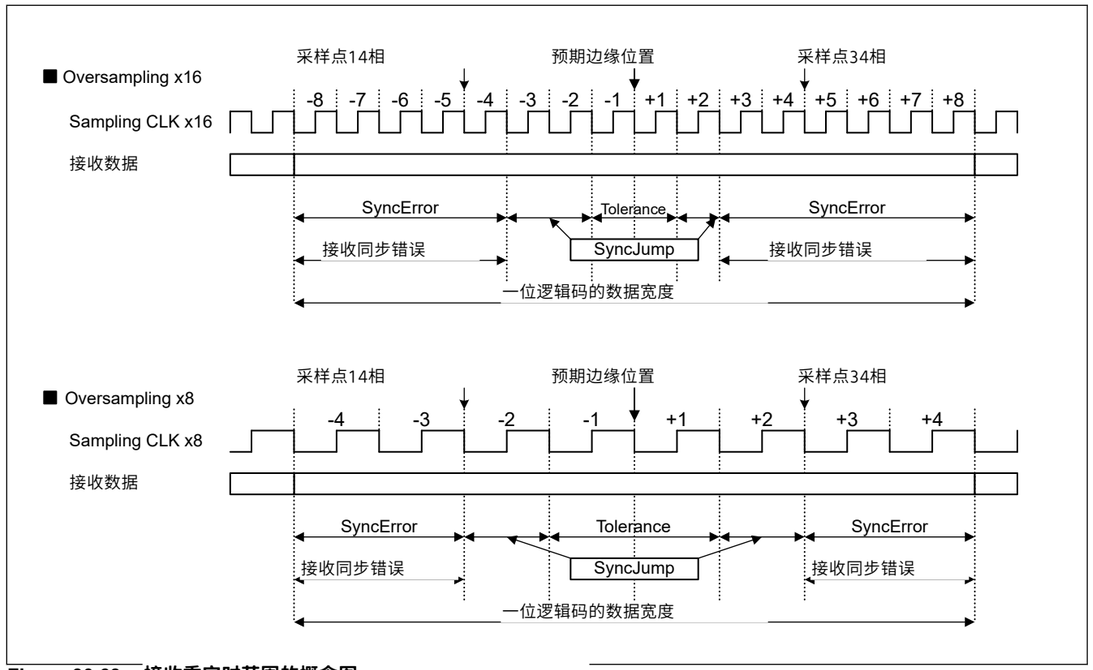


Figure 30.63 接收重定时范围的概念图

30.5.10 Polarity Setting for Manchester Code

The polarity of the Manchester code can be set with the Manchester Mode Register (MMR).

It can be set separately for transmission and reception. Use the MMR.TMPOL bit to set the polarity for transmission and the MMR.RMPOL bit to set the polarity for reception.

The Manchester code polarity setting is valid for the preface area, the data area, and the parity or multi-processor area.

When the initial settings (TMPOL/RMPOL = 0) are used for the polarity of Manchester code, logic 0 is encoded as a zero-to-one transition in Manchester code and logic 1 is encoded as a one-to-zero transition in Manchester code. If the settings are changed to TMPOL/RMPOL = 1, logic 0 is encoded as a one-to-zero transition in Manchester code and logic 1 is encoded as a zero-to-one transition in Manchester code. Figure 30.64 shows the conceptual image of the settings and operation.

Separately from the function above, the transmitted and received data in the data area can be inverted by the transmitted/received data inversion function (SCMR.SINV). Since the polarity of Manchester code (MMR.TMPOL/RMPOL) can be set separately from the transmitted/received data invert function (SCMR.SINV), if both are set to inversion (MMR.TMPOL/RMPOL = 1 and SCMR.SINV = 1), the transmitted and received data are set to initial state (inversion + inversion = normal).

The polarity of the start bit area can be set by a register different from the ones mentioned above.

Since a different register is used, the polarity of the start bit area is not affected by the polarity setting for Manchester code mentioned above.

For details on the setting for the start bit area, see para. (2) in section 30.5.1. Frame Format.

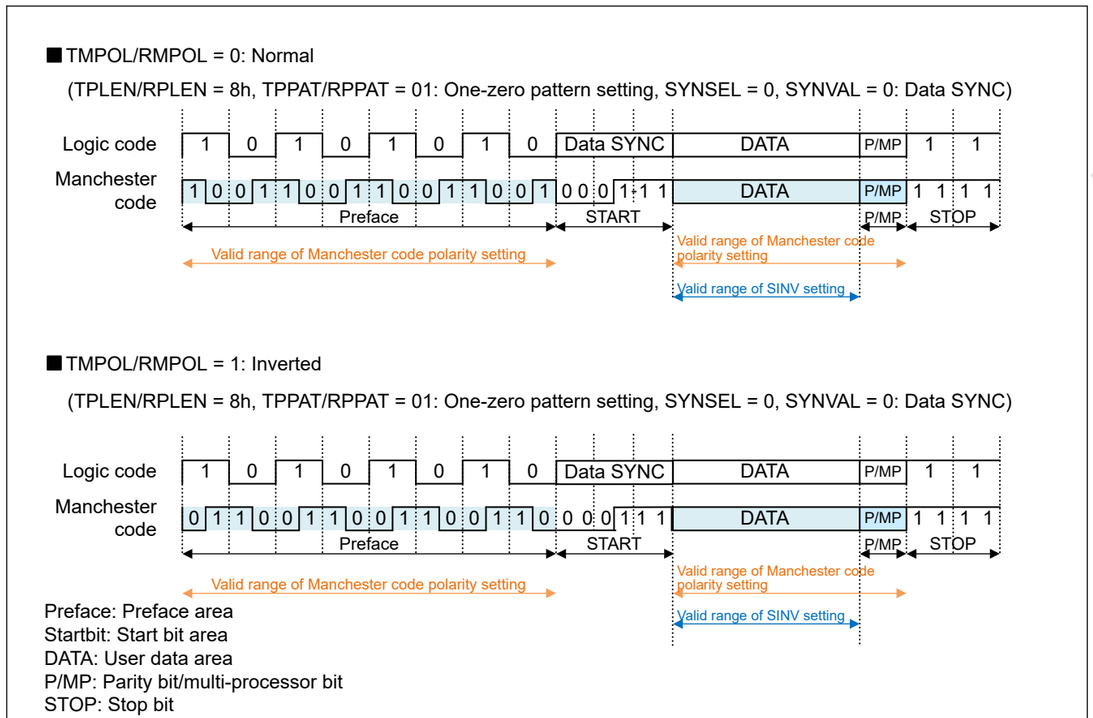


Figure 30.64 Valid Range of the Manchester Code Polarity Setting

30.5.11 Errors in Manchester Mode

There are the following errors in Manchester mode:

30.5.10 曼彻斯特码的极性设置

曼彻斯特码的极性可以通过曼彻斯特模式寄存器(MMR)设置。

可以分别设置发送和接收。使用MMR.TMPOL位设置传输的极性和
MMR.RMPOL位设置接收极性。

曼彻斯特码极性设置对前言区、数据区、奇偶校验或多处理器区有效。

当初始设置(TMPOLRMPOL=0)用于曼彻斯特代码的极性时，逻辑0被编码为曼彻斯特代码中的零到一转换，逻辑1被编码为曼彻斯特代码中的一对零转换。如果设置更改为TMPOLRMPOL=1，则逻辑0被编码为曼彻斯特代码中的一对零转换，逻辑1被编码为曼彻斯特代码中的零到一转换。图30.64显示了设置和操作的概念图。

与上述功能不同，数据区中的发送和接收数据可以通过发送接收数据反转功能(SCMR.SINV)反转。由于曼彻斯特码的极性(MMR.TMPOLRMPOL)可以与发送的接收数据反转功能(SCMR.SINV)分开 设置，如果两者都设置为反转(MMR.TMPOLRMPOL=1和SCMR.SINV=1)，发送和接收的数据设置为初始状态（反转+反转=正常）。

起始位区域的极性可以通过与上述不同的寄存器来设置。

由于使用了不同的寄存器，因此起始位区域的极性不受上述曼彻斯特码极性设置的影响。

有关起始位区域设置的详细信息，请参见第1段。(2)在第30.5.1节中。帧格式。

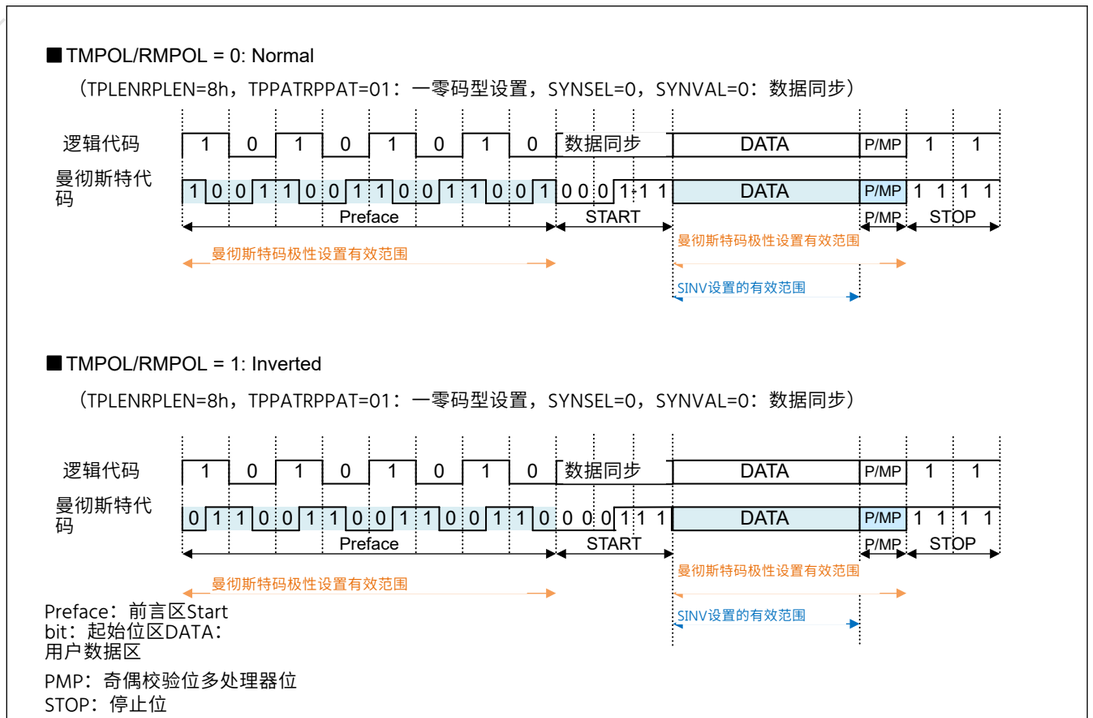


Figure 30.64 曼彻斯特码极性设置的有效范围

30.5.11 曼彻斯特模式中的错误

曼彻斯特模式有以下错误：

1. Parity error
2. Over run error
3. Framing error
4. Manchester error
5. Preface error
6. Start Bit error
7. Receive SYNC error

For errors (1) to (3), see section 30.3.9. Serial Data Reception in Asynchronous Mode (1) because they are the same as in asynchronous mode.

Each errors are judged in each area, but they are reflected on flags and operations at the timing of 3/4-bit sampling of the STOP bit area. If a preface error or start bit error is detected, subsequent data will not be received. Therefore, no other error detection is performed, and the error flag holds the previous information.

Table 30.33 lists the states of the serial status register when detecting errors and judgment about whether to store data in the RDR.

Table 30.34 lists the errors that can be detected in each area of a Manchester frame.

If a Preface error or Start bit error is detected, subsequent data will not be received. Therefore, no other error detection is performed, and the error flag holds the result of the previous frame reception. Also, if an error is detected in the previous frame, data will not be received, but errors in the pre-face area and start bit area will update that flag. Table 30.35 shows the flags and actions in this case.

(4) Manchester error

A Manchester error is generated when a Manchester code error is detected.

In Manchester code, there must be an edge (transition) in the center of the bit.

In the data area of a received frame (including the parity/multi-processor bit), the values of the 1/4-bit and 3/4-bit sampling points are checked in each received 1-bit data, and a Manchester code error is determined if these two values match.

If a Manchester code error is detected, the Manchester error flag (SSR.MER) is asserted.

If a Manchester error occurs, it is handled as an interrupt source and event source. If a Manchester error is detected, the next reception is not performed until the corresponding error flag is cleared.

(5) Preface error

A preface error is generated when the preface pattern does not match or a Manchester code error is detected in the preface area. If a preface error is detected, the preface error flag (SSR.PFER) is asserted.

It is possible to set whether to use this error flag as an interrupt source with the setting of the MECR register.

When MECR.PFEREN = 1, a preface error is handled as an interrupt source or event source. If a preface error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MECR.PFEREN = 0, a preface error is not handled as an interrupt source or event source, and the next reception is not halted. However, a preface error is notified to MESR.PFER.

(6) Start bit error

A start bit error is generated when a mismatch is detected between the start bit area in the received frame and the preset start bit pattern. Upon detection of a start bit error, a start bit error flag (MESR.SBER) is asserted.

It is possible to set whether to use the start bit error as an interrupt source with the setting of the MECR register.

When MECR.SBEREN = 1, a start bit error is handled as an interrupt source or event source. If a start bit error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MECR.SBEREN = 0, a start bit error is not handled as an interrupt source or event source, and the next reception is not halted. However, a start bit error is notified to MESR.SBER.

(7) Receive SYNC error

When the receive retiming function described in section 30.5.9. Receive Retiming is enabled, the receive retiming operation is performed.

1.奇偶校验错误

2.溢出错误

3.构图错误

4.曼彻斯特错误

5.前言错误

6.起始位错误

7.收到SYNC错误

对于错误(1)至(3)，请参阅第30.3.9节。异步模式下的串行数据接收(1)因为它们与异步模式下相同。

在每个区域中判断每个错误，但它们反映在标志和操作上，在3个4位采样的时间
停止位区域。如果检测到前言错误或起始位错误，则不会接收后续数据。因此，不进行其他错误检测，错误标志保存先前的信息。

表30.33列出了串口状态寄存器在检测错误和判断是否存储数据时的状态
RDR.

表30.34列出了在曼彻斯特帧的每个区域中可以检测到的错误。

如果检测到Preface错误或Startbit错误，则不会接收后续数据。因此，不进行其他错误检测，错误标志保存前一帧接收的结果。此外，如果在前一帧中检测到错误，则不会接收数据，但前脸区域和起始位区域中的错误将更新该标志。表30.35显示了这种情况下的标志和操作。

(4)曼彻斯特错误

当检测到曼彻斯特码错误时，就会产生曼彻斯特错误。

在曼彻斯特码中，位的中心必须有一个边（转换）。

在接收帧的数据区（包括奇偶校验多处理器位），在每个接收的1位数据中检查1个4位和3个4位采样点的值，确定曼彻斯特码错误如果这两个值匹配。

如果检测到曼彻斯特代码错误，则曼彻斯特错误标志(SSR.MER)被置位。

如果发生曼彻斯特错误，则将其作为中断源和事件源进行处理。如果检测到曼彻斯特错误，则在清除相应错误标志之前不会执行下一次接收。

(5)前言错误

当前言模式不匹配或在前言区检测到曼彻斯特码错误时，会产生前言错误。如果检测到前言错误，则断言前言错误标志(SSR.PFER)。

可以通过MECR寄存器的设置来设置是否使用该错误标志作为中断源。

当MECR.PFEREN=1时，前言错误作为中断源或事件源处理。如果检测到前言错误，则在相应的错误标志被清除之前不会执行下一次接收。

当MECR.PFEREN=0时，前言错误不会作为中断源或事件源处理，并且不会停止下一次接收。但是，前言错误会通知给MESR.PFER。

(6)起始位错误

当检测到接收帧中的起始位区域与预设的起始位模式不匹配时，会产生起始位错误。在检测到起始位错误时，将置位起始位错误标志(MESR.SBER)。

可以通过MECR寄存器的设置来设置是否使用起始位错误作为中断源。

当MECR.SBEREN=1时，起始位错误作为中断源或事件源处理。如果检测到起始位错误，则在清除相应错误标志之前不会执行下一次接收。

当MECR.SBEREN=0时，不将起始位错误作为中断源或事件源处理，并且不会停止下一次接收。但是，将向MESR.SBER通知起始位错误。

(7)接收同步错误

当接收重定时功能在第30.5.9节中描述。启用接收重定时，执行接收重定时操作。

If no edges are detected within the receive retiming range (SyncError area in Figure 30.63) when receive timing operation is being performed, a receive SYNC error is generated. Upon detection of a receive SYNC error, a receive SYNC error flag (MESR.SYER) is asserted. In areas not subject to retiming, receive SYNC errors are not detected.

The preface area*1, the start bit area*1,*2, and the data area (excluding the stop bit) for which receive retiming operation is performed are checked.

It is possible to set whether to use the receive SYNC error as an interrupt source with the setting of the MECR register.

When MECR.SYEREN = 1, a receive SYNC error is handled as an interrupt source or event source. If a receive SYNC error is detected, the next reception is not performed until the corresponding error flag is cleared.

When MECR.SYEREN = 0, a receive SYNC error is not handled as an interrupt source or event source, and the next reception is not halted. However, a receive SYNC error is notified to MESR.SYER.

Note 1. In the case of a frame that starts with a pattern that expects the first half of the bit to be High, it is excluded from retiming.
Note 2. In the start bit area, when there is no preface length and 3 bit start bit is set, it is not subject to retiming.
Also, the 1st bit and the 2nd bit in the start bit area when 3 bit start bit is set are not subject to retiming.

Table 30.33 Flags in the SSR Register and Receive Data Handling in Manchester Mode

Flag in the SSR register				Flag in the MERS register			received data	Received error status (ERI interrupt / event generation)
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	0	0	0	0	0	0	transfer to RDR	No error
0	1	0	0	0	0	0	transfer to RDR	Framin error
0	0	1	0	0	0	0	transfer to RDR	Parity error
0	1	1	0	0	0	0	transfer to RDR	Framing error + Parity error
0	0	0	1	0	0	0	transfer to RDR	Manchester error
0	1	0	1	0	0	0	transfer to RDR	Framing error + Manchester error
0	0	1	1	0	0	0	transfer to RDR	Parity error + Manchester error
0	1	1	1	0	0	0	transfer to RDR	Framing error + Parity error + Manchester error
1	0	0	0	0	0	0	Lost	Overrun error
1	1	0	0	0	0	0	Lost	Overrun error + Framing error
1	0	1	0	0	0	0	Lost	Overrun error + Parity error
1	1	1	0	0	0	0	Lost	Overrun error + Framing error + Parity error
1	0	0	1	0	0	0	Lost	Overrun error + Manchester error
1	1	0	1	0	0	0	Lost	Overrun error + Framing error + Manchester error
1	0	1	1	0	0	0	Lost	Overrun error + Parity error + Manchester error
1	1	1	1	0	0	0	Lost	Overrun error + Framing error + Parity error + Manchester error
0	Combination of above			0	0	0	transfer to RDR	Errors above + Receive SYNC error*2
1				0	0	0	Lost	Errors above + Receive SYNC error*2
hold	hold	hold	hold	0	1	0	Lost	Preface error*3
hold	hold	hold	hold	1	0	0	Lost	Start bit error*3
hold	hold	hold	hold	0	1	1	Lost	Preface error*3 + Receive SYNC error*2
hold	hold	hold	hold	1	0	1	Lost	Start bit error*3 + Receive SYNC error*2

Note 1. Start bit error and Preface error never become 1 at the same time.
Note 2. When MECR.SYEREN = 1, SCIn_ERI interrupt / event is generated by SYER factor.
Note 3. If MECR.PFEREN = 1 or MECR.SBEREN = 1, an SCIn_ERI interrupt / event is generated when the corresponding flag is set.

如果在执行接收定时操作时在接收重定时范围内（图30.63中的SyncError区域）没有检测到边沿，则会产生接收SYNC错误。在检测到接收同步错误时，接收同步错误标志(MESR.SYER)被置位。在不受重定时限制的区域中，不会检测到接收同步错误。

检查执行接收重定时操作的前言区域*1、起始位区域*1、*2和数据区域（不包括停止位）。

可以通过MECR寄存器的设置来设置是否使用接收SYNC错误作为中断源。

当MECR.SYEREN=1时，接收SYNC错误将作为中断源或事件源处理。如果检测到接收SYNC错误，则在清除相应错误标志之前不会执行下一次接收。

当MECR.SYEREN=0时，接收SYNC错误不会作为中断源或事件源处理，并且不会停止下一次接收。但是，接收同步错误会通知给MESR.SYER。

注1.对于以预期位的前半部分为高的模式开始的帧，它被排除在重定时之外。

注2.在起始位区域中，当没有序言长度且设置了3位起始位时，不进行重定时。
此外，当设置3位起始位时，起始位区域中的第1位和第2位不受重定时的影响。

Table 30.33 SSR寄存器中的标志和曼彻斯特模式下的接收数据处理

SSR寄存器中的标志				MERS寄存器中的标志			接收数据	接收错误状态（ERI中断事件产生）
ORER	FER	PER	MER	SBER*1	PFER*1	SYER		
0	0	0	0	0	0	0	转移到RDR	没有错误
0	1	0	0	0	0	0	转移到RDR	Framin error
0	0	1	0	0	0	0	转移到RDR	奇偶校验错误
0	1	1	0	0	0	0	转移到RDR	成帧错误+奇偶校验错误
0	0	0	1	0	0	0	转移到RDR	曼彻斯特错误
0	1	0	1	0	0	0	转移到RDR	帧错误+曼彻斯特错误
0	0	1	1	0	0	0	转移到RDR	奇偶校验错误+曼彻斯特错误
0	1	1	1	0	0	0	转移到RDR	成帧错误+奇偶校验错误+曼彻斯特错误
1	0	0	0	0	0	0	Lost	溢出错误
1	1	0	0	0	0	0	Lost	溢出错误+成帧错误
1	0	1	0	0	0	0	Lost	溢出错误+奇偶校验错误
1	1	1	0	0	0	0	Lost	溢出错误+帧错误+奇偶校验错误
1	0	0	1	0	0	0	Lost	超限错误+曼彻斯特错误
1	1	0	1	0	0	0	Lost	溢出错误+帧错误+曼彻斯特错误
1	0	1	1	0	0	0	Lost	溢出错误+奇偶校验错误+曼彻斯特错误
1	1	1	1	0	0	0	Lost	溢出错误+成帧错误+奇偶校验错误+曼彻斯特错误
0	以上结合			0	0	0	转移到RDR	上述错误+接收同步错误*2
1				0	0	0	Lost	上述错误+接收同步错误*2
hold	hold	hold	hold	0	1	0	Lost	前言错误*3
hold	hold	hold	hold	1	0	0	Lost	起始位错误*3
hold	hold	hold	hold	0	1	1	Lost	前言错误*3+接收同步错误*2
hold	hold	hold	hold	1	0	1	Lost	起始位错误*3+接收同步错误*2

注1.起始位错误和前言错误永远不会同时变为1。
注2.当MECR.SYEREN=1时，由SYER因素产生SCIn_ERI中断事件。
注3.如果MECR.PFEREN=1或MECR.SBEREN=1，则在设置相应标志时产生SCIn_ERI中断事件。

Table 30.34 Errors Detectable in Each Area

	Preface error (PFER)	Start Bit error (SBER)	Manchester error (MER)	Receive SYNC error (SYER)	Parity error (PER)	Framing error (FER)
Preface area	✓	—	—*1	✓*2	—	—
Start Bit area	—	✓	—	✓*2	—	—
Data area	—	—	✓	✓	—	—
Parity area	—	—	✓	✓	✓	—
Multi-processor area	—	—	✓	✓	—	—
Stop Bit area	—	—	—	—	—	✓

Note: ✓: Detected, —: Not detected
Note 1. When an Manchester code error occurs in the preface area, it is defined as a preface error.
Note 2. It may not be subject to Receive SYNC error detection. For details see the text section 30.5.11. Errors in Manchester Mode (7)

Table 30.35 Operation status due to presence / absence of error in previous frame and operation status list in multiprocessor mode (1 of 2)

Previous frame	Each area of the Frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
No Error	PFER No SYER*1	No Error	Don't Care	Don't Care	Don't Care	0	Don't Care	Don't Care	Lost	set PFER*1	not output	not output
						1					output	output
	No Error	SBER No SYER*1	Don't Care	Don't Care	Don't Care	Don't Care	0	Don't Care	Lost	set SBER*1	not output	not output
							1				output	output
	SYER No PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	SYER No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	No Error	SYER		No Error	Don't Care	Don't Care	0	transfer to RDR	set SYER	not output	not output
								1	Lost		output	output
	No Error	No Error	MER		No Error	Don't Care	Don't Care	Don't Care	transfer to RDR	set MER	output	output
	No Error	No Error	Don't Care	PER	No Error	Don't Care	Don't Care	Don't Care	transfer to RDR	set PER	output	output
	No Error	No Error	Don't Care	Don't Care	FER	Don't Care	Don't Care	Don't Care	transfer to RDR	set FER	output	output
	There is some error ORER					Don't Care	Don't Care	Don't Care	Lost	set some flags*2	output	output
	No Error	No Error	No Error	No Error	No Error ORER	Don't Care	Don't Care	Don't Care	Lost	set ORER	output	output

Table 30.34 每个区域可检测到的错误

	前言错误(PFER)	起始位错误(SBER)	曼彻斯特错误(MER)	接收同步错误(SYER)	奇偶校验错误(PER)	成帧错误(FER)
前言区	✓	—	—*1	✓*2	—	—
起始位区域	—	✓	—	✓*2	—	—
数据区	—	—	✓	✓	—	—
平价区	—	—	✓	✓	✓	—
Multi-processor area	—	—	✓	✓	—	—
停止位区域	—	—	—	—	—	✓

Note: ：检测到，—：未检测到
注1.当序言区出现曼彻斯特码错误时，定义为序言错误。
注2.它可能不受ReceiveSYNC错误检测的影响。有关详细信息，请参阅文本部分30.5.11。曼彻斯特模式中的错误(7)

Table 30.35 由于前一帧中不存在错误而导致的操作状态和多处理器模式下的操作状态列表（1of2）

Previous frame	框架的每个区域					PFERE N	SBERE N	SYERE N	接收数据	错误标志	Interrupt request	事件信号
	preface	起始位	data	parity	stop							
没有错误	PFER No SYER*1	没有错误	不在乎	不在乎	不在乎	0	不在乎	不在乎	Lost	set PFER*1	不输出	不输出
						1					output	output
	没有错误	SBER No SYER*1	不在乎	不在乎	不在乎	不在乎	0	不在乎	Lost	set SBER*1	不输出	不输出
							1				output	output
	SYER No PFER	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	0	转移到RDR	set SYER	不输出	不输出
								1	Lost		output	output
	没有错误	SYER No SBER	不在乎	不在乎	不在乎	不在乎	不在乎	0	转移到RDR	set SYER	不输出	不输出
								1	Lost		output	output
	没有错误	没有错误	SYER		没有错误	不在乎	不在乎	0	转移到RDR	set SYER	不输出	不输出
								1	Lost		output	output
	没有错误	没有错误	MER		没有错误	不在乎	不在乎	不在乎	转移到RDR	设置MER	output	output
	没有错误	没有错误	不在乎	PER	没有错误	不在乎	不在乎	不在乎	转移到RDR	设置PER	output	output
	没有错误	没有错误	不在乎	不在乎	FER	不在乎	不在乎	不在乎	转移到RDR	设置FER	output	output
	有一些错误 ORER					不在乎	不在乎	不在乎	Lost	设置一些标志*2	output	output
	没有错误	没有错误	没有错误	没有错误	没有错误 ORER	不在乎	不在乎	不在乎	Lost	set ORER	output	output

Table 30.35 Operation status due to presence / absence of error in previous frame and operation status list in multiprocessor mode (2 of 2)

Previous frame	Each area of the Frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
some error*3 *6	PFER No SYER*1	No Error	Don't Care	Don't Care	Don't Care	0	Don't Care	Don't Care	Lost	set PFER*1	output*4	not output*5
						1						
	No Error	SBER No SYER*1	Don't Care	Don't Care	Don't Care	Don't Care	0	Don't Care		set SBER*1		
							1					
	SYER No PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0		set SYER		
								1				
	No Error	SYER No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0		set SYER		
								1				
	No Error	No Error	SYER		No Error	Don't Care	Don't Care	0		don't set any flags		
								1				
	No Error	No Error	MER		No Error	Don't Care	Don't Care	Don't Care				
	No Error	No Error	Don't Care	PER	No Error	Don't Care	Don't Care	Don't Care				
	No Error	No Error	Don't Care	Don't Care	FER	Don't Care	Don't Care	Don't Care				
	There is some error ORER					Don't Care	Don't Care	Don't Care				
	No Error	No Error	No Error	No Error	No Error ORER	Don't Care	Don't Care	Don't Care				

Note 1. If SYER is detected, the SYER flag is also set. Other operations are as shown in this table.
Note 2. Other detected error flags including ORER are also set.
Note 3. If all the error flags are cleared before the STOP bit is judged, the operation will be the same as the case where there is no error in the previous frame of this table.
Note 4. Since the SCIn_ERI interrupt request is level output, it remains active due to errors in the previous frame regardless of the presence or absence of error in the relevant frame.
Note 5. Since the error cause is continuously detected, the SCIn_ERI event is not newly output regardless of the presence or absence of errors in the relevant frame.
Note 6. For PFER, SBER, and SYER, when each enable bit is set to disable, it is treated as no error.

Table 30.36 Operation when MPIE = "1" in multi-processor mode (MPIE = "0")

MPB*1	Each area of the frame					PFERE N	SBERE N	SYERE N	received data	Error flag	Interrupt request	Event signal
	preface	start bit	data	parity	stop							
1	No Error	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	transfer to RDR	set some flags	output*2	output*2
	No PFER	No SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	0				
	SYER*3	SYER*3						1	Lost	don't set any flags	not output	not output
	PFER	No Error	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care				
	No Error	SBER	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care					

Note 1. If the received MPB bit us "0", it is not received the frame, and the operation is the same as lost of the reception data of this table.

Table 30.35 由于前一帧中不存在错误而导致的操作状态和多处理器模式下的操作状态列表（2of2）

Previous frame	框架的每个区域					PFERE N	SBERE N	SYERE N	接收数据	错误标志	Interrupt request	事件信号
	preface	起始位	data	parity	stop							
一些错误*3*6	PFER No SYER*1	没有错误	不在乎	不在乎	不在乎	0	不在乎	不在乎	Lost	set PFER*1	output*4	不输出*5
						1						
	没有错误	SBER No SYER*1	不在乎	不在乎	不在乎	不在乎	0	不在乎		set SBER*1		
							1					
	SYER No PFER	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	0		set SYER		
								1				
	没有错误	SYER No SBER	不在乎	不在乎	不在乎	不在乎	不在乎	0		set SYER		
								1				
	没有错误	没有错误	SYER		没有错误	不在乎	不在乎	0		不要设置任何标志		
								1				
	没有错误	没有错误	MER		没有错误	不在乎	不在乎	不在乎				
	没有错误	没有错误	不在乎	PER	没有错误	不在乎	不在乎	不在乎				
	没有错误	没有错误	不在乎	不在乎	FER	不在乎	不在乎	不在乎				
	有一些错误 ORER					不在乎	不在乎	不在乎				
	没有错误	没有错误	没有错误	没有错误	没有错误 ORER	不在乎	不在乎	不在乎				

注1.如果SYER被检测到，SYER标志也被设置。其他操作如本表所示。
注2.还设置了其他检测到的错误标志，包括ORER。
注3.如果在判断STOP位之前清除所有错误标志，则操作将与该表的前一帧没有错误的情况相同。

注4.由于SCIn_ERI中断请求是电平输出，因此无论相关帧中是否存在错误，它都会由于前一帧中的错误而保持活动状态。

注5.由于不断检测错误原因，因此无论相关帧中是否存在错误，都不会重新输出SCIn_ERI事件。

注6.对于PFER、SBER和SYER，当每个使能位设置为禁用时，它被视为无错误。

Table 30.36 多处理器模式下MPIE="1"时的操作(MPIE="0")

MPB*1	框架的每个区域					PFERE N	SBERE N	SYERE N	接收数据	错误标志	Interrupt request	事件信号
	preface	起始位	data	parity	stop							
1	没有错误	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	不在乎	转移到RDR	设置一些标志	output*2	output*2
	No PFER	No SBER	不在乎	不在乎	不在乎	不在乎	不在乎	0				
	SYER*3	SYER*3						1	Lost	不要设置任何标志	不输出	不输出
	PFER	没有错误	不在乎	不在乎	不在乎	不在乎	不在乎	不在乎				
	没有错误	SBER	不在乎	不在乎	不在乎	不在乎	不在乎					

注1.如果接收到的MPB位为“0”，则不接收帧，操作同本表接收数据丢失。

Note 2. If no error is detected, SCIn_RXI interrupt request or event is output, and if it is detected, SCIn_ERI interrupt request or event is output.
Note 3. When SYER is detected in the preface area or the start bit area, the behavior of handling as an error depending on the SYEREN bit changes.

30.6 Operation in Clock Synchronous Mode

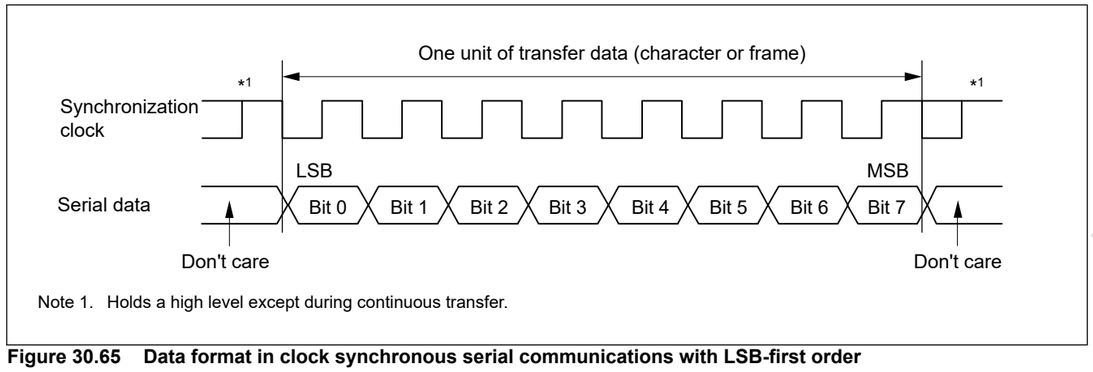
Figure 30.65 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. For single-character data transfer, data consists of 8-bit. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next falling edge. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit as output state. When the SPMR.CKPH bit is 1 in slave mode, the transmission line holds the first bit output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a shared clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to perform continuous transfer in the fastest bit rate setting (BRR[7:0] = 0x00 and SMR.CKS[1:0] = 00b). Therefore, when the FIFO is selected, this setting (BRR[7:0] = 0x00 and SMR.CKS[1:0] = 00b) is not available.



Note 1. Holds a high level except during continuous transfer.

Figure 30.65 Data format in clock synchronous serial communications with LSB-first order

30.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected based on the SCR.CKE[1:0] setting.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed, the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts when the SCR.RE bit set to 1. The synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

When only data reception is performed and the CTS function is enabled, the clock output does not start when the SCR.RE bit set to 1 and the CTSn_RTSn pin input is high. The synchronization clock output starts when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is low. Following that, when the CTSn_RTSn pin input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn pin input continues to be low, the synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

Note 1. The signal is held high while (SPMR.CKPH = 0 and SPMR.CKPOL = 1) or (SPMR.CKPH = 1 and SPMR.CKPOL = 1). It is held low while (SPMR.CKPH = 0 and SPMR.CKPOL = 1) or (SPMR.CKPH = 1 and SPMR.CKPOL = 0).

注2.如果没有检测到错误，则输出SCIn_RXI中断请求或事件，如果检测到，则输出SCIn_ERI中断请求或事件。

注3.在序言区域或起始位区域中检测到SYER时，根据SYEREN位作为错误处理的行为会发生变化。

30.6 时钟同步模式下的操作

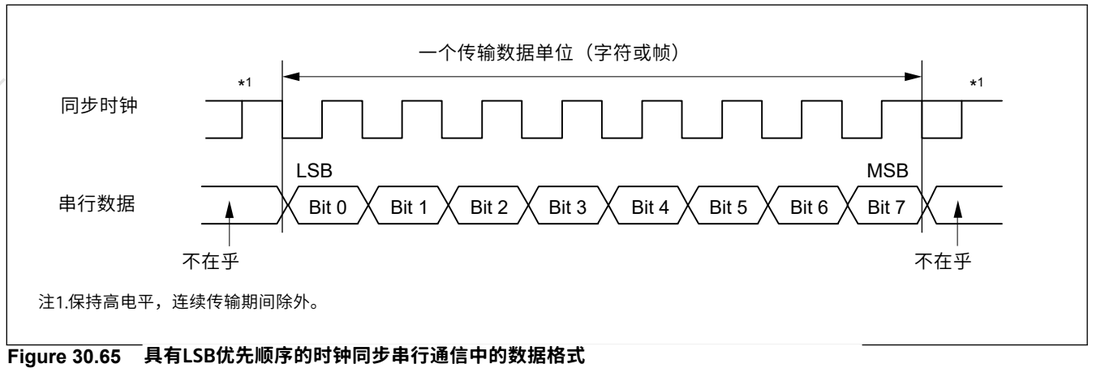
图30.65显示了时钟同步串行数据通信的数据格式。

在时钟同步模式下，数据的发送或接收与时钟脉冲同步。对于单字符数据传输，数据由8位组成。在时钟同步模式下，不能添加奇偶校验位。

在数据传输中，SCI从同步时钟的一个下降沿到下一个下降沿输出数据。在数据接收中，SCI与同步时钟的上升沿同步接收数据。8位数据输出后，传输线保持最后一位作为输出状态。当SPMR.CKPH位在从机模式下为1时，传输线保持第一位输出状态。

在SCI中，发送器和接收器是独立的单元，通过使用共享时钟实现全双工通信。发送端和接收端都具有双缓冲结构，可以在发送时写入下一个发送数据，或者在接收时读取前一个接收数据，实现数据的连续传输。

但是，不可能以最快的比特率设置（BRR[7:0]=0x00和SMR.CKS[1:0]=00b)。Therefore whentheFIFOisselected thissetting(BRR[7:0]=0x00andSMR.CKS[1:0]=00b)isnotavailable.



注1.保持高电平，连续传输期间除外。

Figure 30.65 具有LSB优先顺序的时钟同步串行通信中的数据格式

30.6.1 Clock

可以根据SCR.CKE[1:0]设置选择由片内波特率发生器生成的内部时钟或SCKn引脚上的外部同步时钟输入。

当SCI在内部时钟上运行时，同步时钟从SCKn引脚输出。在一个字符的传输中输出八个同步时钟脉冲。当不执行传输时，时钟保持高电平。但是，当CTS功能禁用时仅执行数据接收时，同步时钟输出会在SCR.RE位设置为1时开始。同步时钟在变为高电平时停止*1并且发生溢出错误或SCR.RE位设置为0。

仅执行数据接收且启用CTS功能时，当SCR.RE位设置为1且CTSn_RTSn引脚输入为高电平时，时钟输出不会启动。当SCR.RE位设置为1且CTSn_RTSn引脚输入为低电平时，同步时钟输出开始。之后，当CTSn_RTSn引脚输入在帧接收完成时为高电平时，同步时钟输出在其变为高电平时停止。如果CTSn_RTSn引脚输入持续为低电平，则同步时钟在变为高电平时停止*1并发生溢出错误或SCR.RE位设置为0。

注1.当(SPMR.CKPH=0且SPMR.CKPOL=1)或(SPMR.CKPH=1且SPMR.CKPOL=1)时，信号保持高电平。它在(SPMR.CKPH=0和SPMR.CKPOL=1)或(SPMR.CKPH=1和SPMR.CKPOL=0)时保持低电平。

30.6.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication is enabled. Conditions for output of the CTSn_RTSn low and high are shown as follows:

[Conditions for low output]

Satisfaction of all the following conditions:

Non-FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- Neither transmission nor reception is in progress
- There is no received data available to be read when the SCR.RE bit is 1
- Transmit data is written when the SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR.ORER flag is 0

FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- Neither transmission nor reception is in progress
- The amount of receive data written in FRDRHL is less than the setting value of FCRH.RSTRG[3:0] when SCR.RE = 1
- Data that has not been transmitted is available in FTDRHL when SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR_FIFO.ORER flag is 0

[Condition for high output]

- The conditions for low output are not satisfied

30.6.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 0x00 to the SCR register, then continue through the SCI initialization procedure given in the sections describing non-FIFO and FIFO selection in section 30.6.2. CTS and RTS Functions. Anytime the operating mode or transfer format is to be changed, the SCR register must be initialized before the change can be made.

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, and PER flags in SSR/SSR_FIFO nor the RDR register. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: In non-FIFO mode, switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the SCR.TIE bit is 1 generates an SCIn_TXI interrupt request.

Table 30.37 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM bit to 0	Set the FCR.FM bit to 0.

30.6.2 CTS和RTS函数

在CTS功能中，当时钟源为内部时钟时，CTSn_RTSn引脚输入控制数据接收或发送的开始。将SPMR.CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚设置为低电平会导致数据接收或发送开始。

在数据发送或接收过程中将CTSn_RTSn引脚设置为高电平不会影响当前帧的发送或接收。

在RTS功能中，当时钟源为外部同步时钟时，CTSn_RTSn引脚输出用于请求开始数据接收或发送。当串行通信启用时，CTSn_RTSn输出变为低电平。CTSn_RTSn低电平和高电平的输出条件如下所示：

[低输出的条件]

满足以下所有条件：

满足以下所有条件时选择非FIFO

- ●SCR.RE位或SCR.TE位的值为1
- ●发送和接收都没有进行
- ●当SCR.RE位为1时，没有可读取的接收数据
- ●当SCR.TE位为1且SCR.CKE[1]位为0时写入发送数据
- ●当SCR.TE位为1且SCR.CKE[1]位为1时，TSR寄存器中的数据可用于传输
- ●SSR.ORER标志为0

满足以下所有条件时选择FIFO

- ●SCR.RE位或SCR.TE位的值为1
- ●发送和接收都没有进行
- ●SCR.RE=1时，FRDRHL写入的接收数据量小于FCRH.RSTRG[3:0]的设定值
- ●当SCR.TE位为1且SCR.CKE[1]位为0时，FTDRHL中未发送的数据可用
- ●当SCR.TE位为1且SCR.CKE[1]位为1时，TSR寄存器中的数据可用于传输
- ●SSR_FIFO.ORER标志为0

【高输出条件】

- ●不满足低输出条件

30.6.3 时钟同步模式下的SCI初始化

在发送和接收数据之前，首先将初始值0x00写入SCR寄存器，然后继续执行第30.6.2节中描述非FIFO和FIFO选择的部分中给出的SCI初始化过程。CTS和RTS功能。每当要更改操作模式或传输格式时，必须先初始化SCR寄存器，然后才能进行更改。

Note: 将SCR.RE位设置为0既不会初始化SSRSSR_FIFO中的ORER、FER和PER标志，也不会初始化RDR寄存器。当TE位设置为0时，所选FIFO缓冲区的TEND标志未初始化。

Note: 在非FIFO模式下，当SCR.TIE位为1时，将SCR.TE位的值从1切换为0或从0切换为1会产生SCIn_TXI中断请求。

Table 30.37 在时钟同步模式下选择非FIFO的SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE位设置为0	
3	将FCR.FM位设置为0	将FCR.FM位设置为0。

Table 30.37 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected (2 of 2)

No.	Step Name	Description
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR	Set the communication terminals status in SPTR.
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
11	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
12	Initialization completion	

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously

Table 30.38 Example flow of SCI initialization in clock synchronous mode with FIFO selected

No.	Step Name	Description
1	Start initialization	
2	Set the SCR.TIE, RIE, TE, RE, and TEIE bits to 0	
3	Set the FCR.FM, TFRST, and RFRST bits to 1. Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.	Set the FCR.FM, TFRST, and RFRST bits to 1 (FIFO mode enabled, transmit/receive FIFOs empty). Set the FCR.TTRG[3:0], RTRG[3:0], and RSTRG[3:0] bits.
4	Set the SCR.CKE[1:0] bits	Set the clock selection in SCR.
5	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits.	Set the SIMR1.IICM bit to 0. Set the SPMR.CKPH and CKPOL bits. Step 5 can be skipped if the values have not been changed from the initial values.
6	Set the data transmission/ reception format in SMR, SCMR, and SEMR	Set data transmission/reception format in SMR, SCMR, and SEMR.
7	Set a value in SPTR	Set the communication terminals status in SPTR.
8	Set a value in BRR	Write a value corresponding to the bit rate to BRR. This step is not necessary if an external clock is used.
9	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not necessary if the BRME bit in SEMR is set to 0 or an external clock is used.
10	Set the FCR.TFRST and RFRST bits to 0	Set the FCR.TFRST and RFRST bits to 0.
11	Set the I/O port functions	Make I/O port settings to enable input and output functions as required for TXDn, RXDn, and SCKn pins.
12	Set the SCR.TE or RE bit to 1, and set the SCR.TIE and RIE bits	Set the SCR.TE or RE bit to 1. Also set the SCR.TIE and RIE bits. Setting the TE and RE bits allows TXDn and RXDn pins to be used.
13	Initialization completion	

Note: In simultaneous transmit and receive operations, the TE and RE bits in SCR must both be set to 0 or set to 1 simultaneously.

Table 30.37 在时钟同步模式下选择非FIFO的SCI初始化示例流程（2个中的2个）

No.	步骤名称	Description
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和 CKPOL bits.	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中 设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在SPTR中设置一个值	在SPTR中设置通讯终端状态。
8	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
9	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果 SEMR中的BRME位设置为0或使用外部时钟。
10	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
11	将SCR.TE或RE位设置为1，并 设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn引脚。
12	初始化完成	

Note: 在同时发送和接收操作中，SCR中的TE和RE位必须都设置为0或同时设置为1

Table 30.38 选择FIFO的时钟同步模式下的SCI初始化示例流程

No.	步骤名称	Description
1	开始初始化	
2	将SCR.TIE、RIE、TE、RE和TEIE 位设置为0	
3	设置FCR.FM、TFRST和 RFRST位为1。 设置FCR.TTRG[3:0]， RTRG[3:0]和RSTRG[3:0]位。	将FCR.FM、TFRST和RFRST位设置为1（启用FIFO模式，发送接收FIFO为空）。设置FCR.TTRG[3:0]、RTRG[3:0]和RSTRG[3:0]位。
4	设置SCR.CKE[1:0]位	在SCR中设置时钟选择。
5	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和 CKPOL bits.	将SIMR1.IICM位设置为0。 设置SPMR.CKPH和CKPOL位。 如果这些值没有从初始值改变，则可以跳过第5步。
6	在SMR、SCMR和SEMR中 设置数据发送接收格式	在SMR、SCMR、SEMR中设置数据发送接收格式。
7	在SPTR中设置一个值	在SPTR中设置通讯终端状态。
8	在BRR中设置一个值	将与比特率对应的值写入BRR。 如果使用外部时钟，则不需要此步骤。
9	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。这一步是没有必要的，如果 SEMR中的BRME位设置为0或使用外部时钟。
10	设置FCR.TFRST和 RFRST位为0	将FCR.TFRST和RFRST位设置为0。
11	设置IO端口功能	进行IO端口设置以启用TXDn、RXDn和所需的输入和输出功能 SCKn pins.
12	将SCR.TE或RE位设置为1，并 设置SCR.TIE和RIE位	将SCR.TE或RE位设置为1。同时设置SCR.TIE和RIE位。 设置TE和RE位允许使用TXDn和RXDn引脚。
13	初始化完成	

Note: 在同时发送和接收操作中，SCR中的TE和RE位必须都设置为0或同时设置为1。

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30.6.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 30.66, Figure 30.67, and Figure 30.68 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit is set to 1 but only after the TIE bit in the SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks for update to the TDR register on output of the last bit.
5. When the TDR register is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the SSR.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 30.66, Figure 30.67, and Figure 30.68 show examples of serial data transmission.

Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Always set the receive error flags to 0 before starting transmission.

Note: Setting the SCR.RE bit to 0 does not clear the receive error flags.

30.6.4 时钟同步模式下的串行数据传输

(1) Non-FIFO selected

图30.66、图30.67和图30.68显示了时钟同步模式下的串行传输示例。

在串行数据传输中，SCI操作如下：

1.当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR寄存器传输到TSR寄存器。发送开始时的SCIn_TXI中断请求在TE位设置为1且仅在SCR中的TIE位也设置为1或当这两个位通过一条指令同时设置为1时产生。

2.将数据从TDR传输到TSR后，SCI开始传输。当SCR.TIE位设置为1时，会产生SCIn_TXI中断请求。在当前发送数据发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入TDR来启用连续发送。使用SCIn_TEI中断请求时，在SCIn_TXI请求的处理例程中将要发送的最后一个数据写入TDR寄存器后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

3.指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当SPMR.CTSE位为1时，时钟信号的输出被暂停，直到输入CTS信号为低电平。

4.SCI在最后一位输出时检查对TDR寄存器的更新。

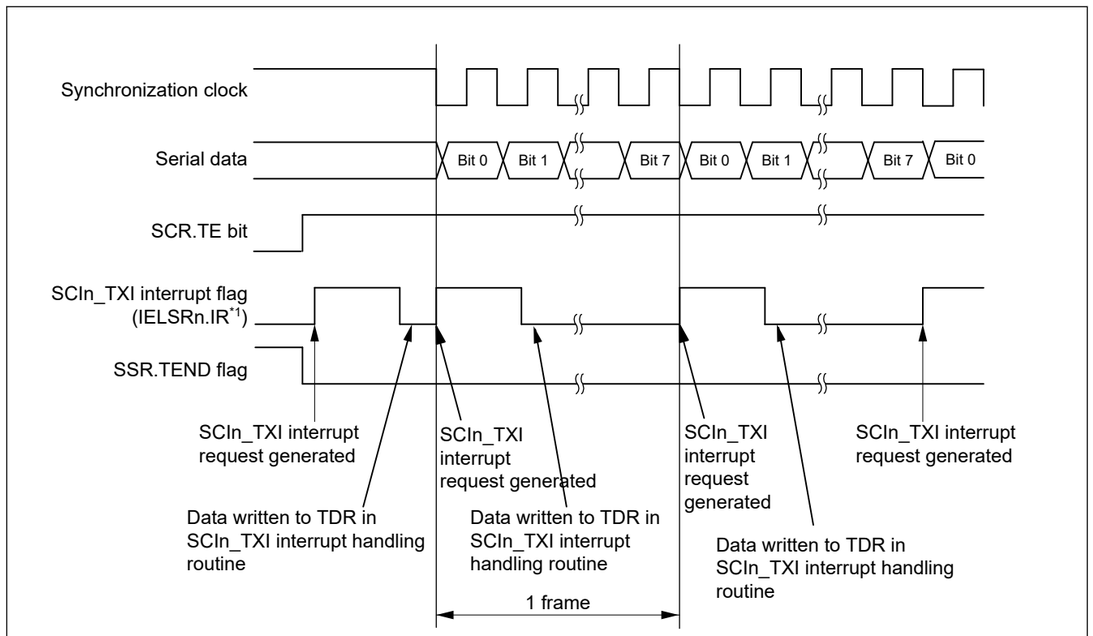
5.TDR寄存器更新后，下一个发送数据从TDR传送到TSR，开始下一帧的串行发送。

6.如果TDR未更新，则SSR.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR.TEIE位为1，则产生SCIn_TEI中断请求并且SCKn引脚保持高电平。

图30.66、图30.67和图30.68显示了串行数据传输的示例。

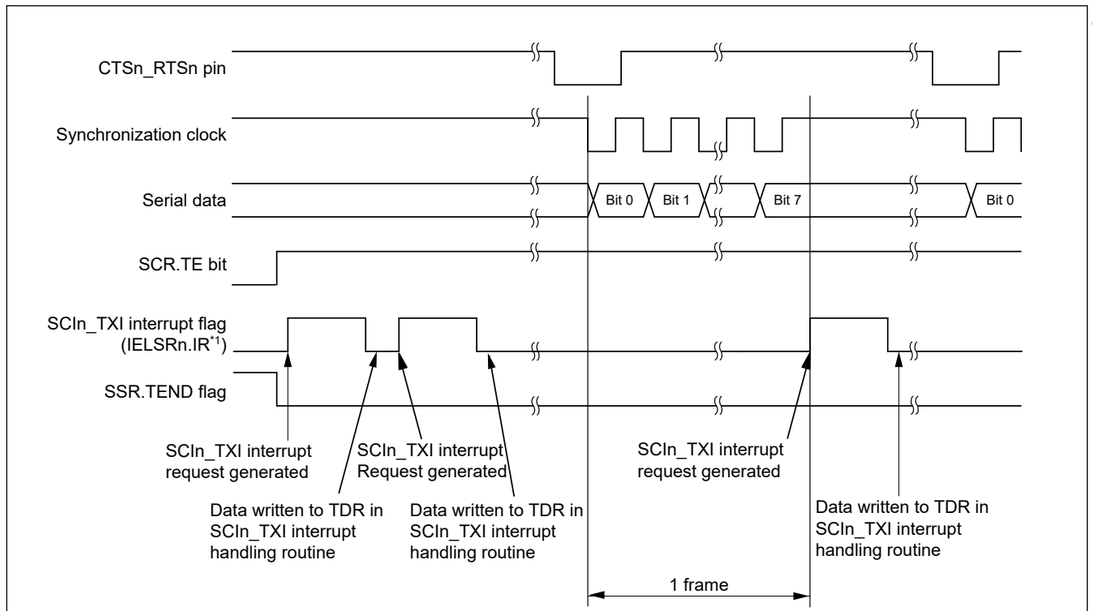
当接收错误标志（SSR中的ORER、FER或PER）设置为1时，发送不会开始。在开始发送之前，请务必将接收错误标志设置为0。

Note: 将SCR.RE位设置为0不会清除接收错误标志。



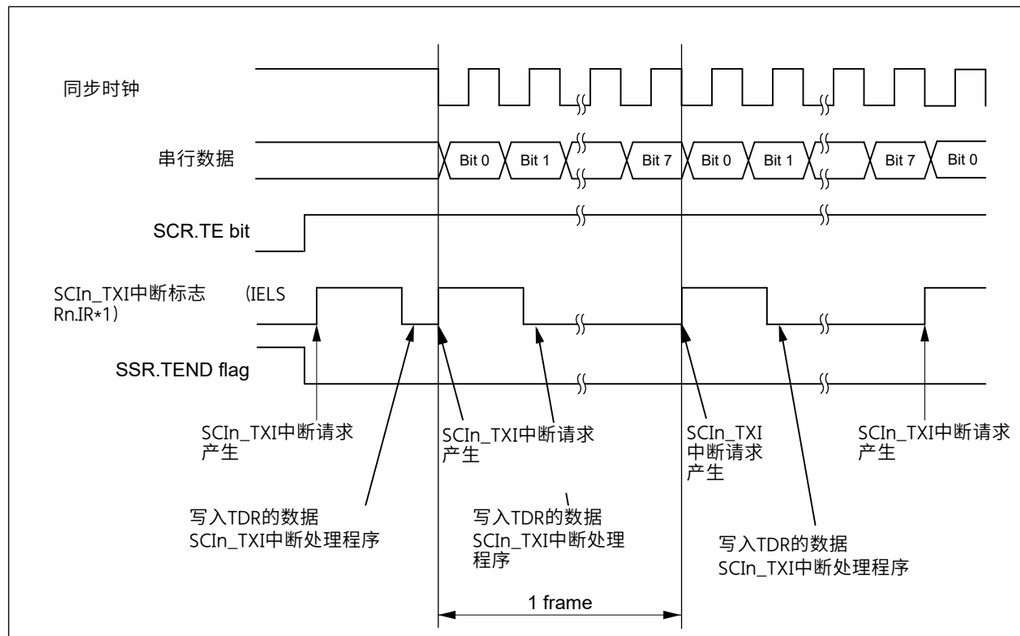
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.66 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission



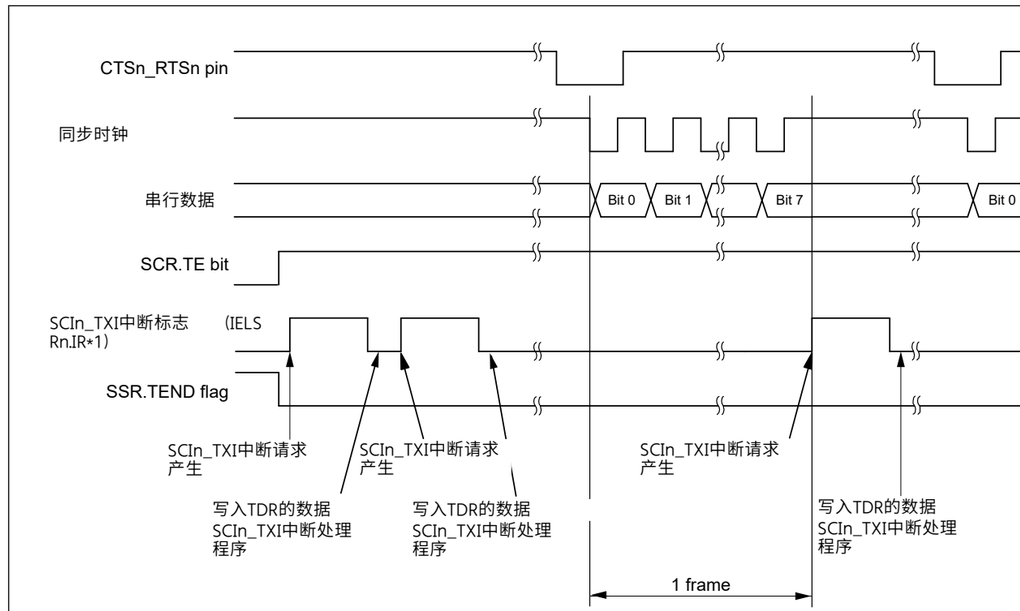
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.67 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



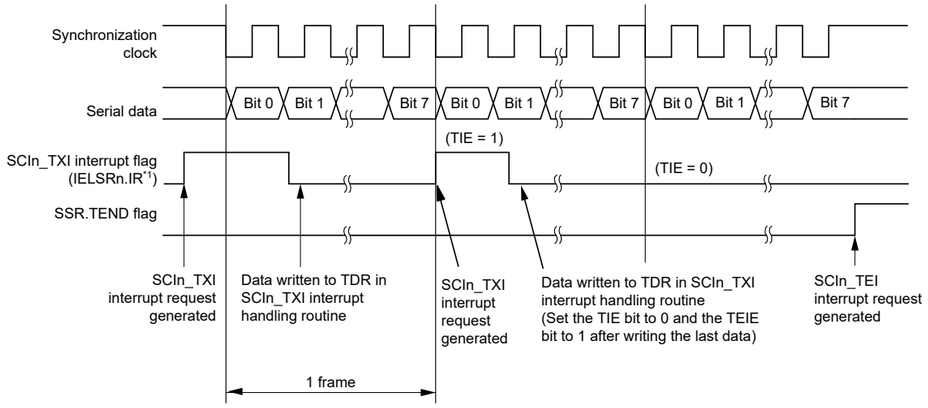
注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.66 传输开始时未使用CTS功能时时钟同步模式下的串行数据传输示例



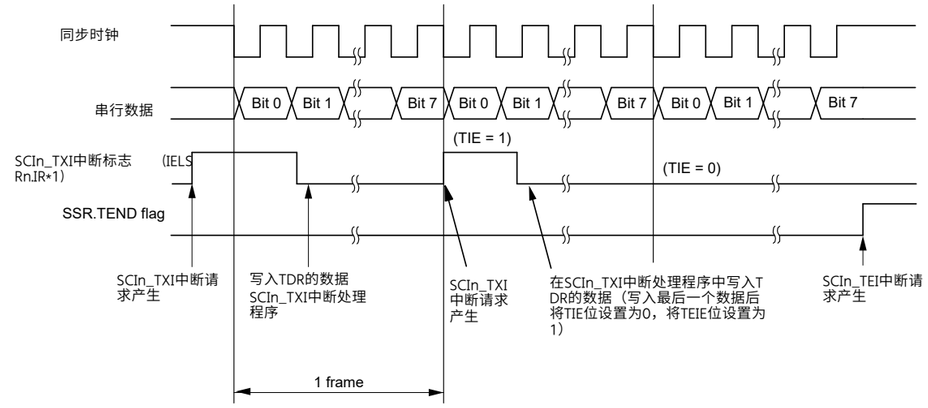
注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.67 传输开始时使用CTS功能时时钟同步模式下的串行数据传输示例



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.68 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.68 从传输中间到传输完成的时钟同步模式下的串行数据传输示例

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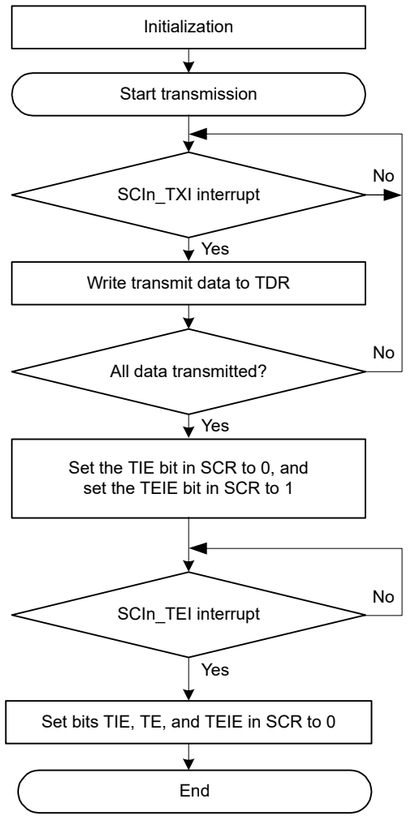


[1] [1]SCI initialization:
Set data transmission.

[2] [2]Writing transmit data write to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] [3]Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR upon accepting a transmit data empty interrupt (SCIn_TXI) request. Transmit data can also be written to TDR by activating the DMAC or DTC by theSCIn_TXI interrup trequest.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to theTDR

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCKn pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

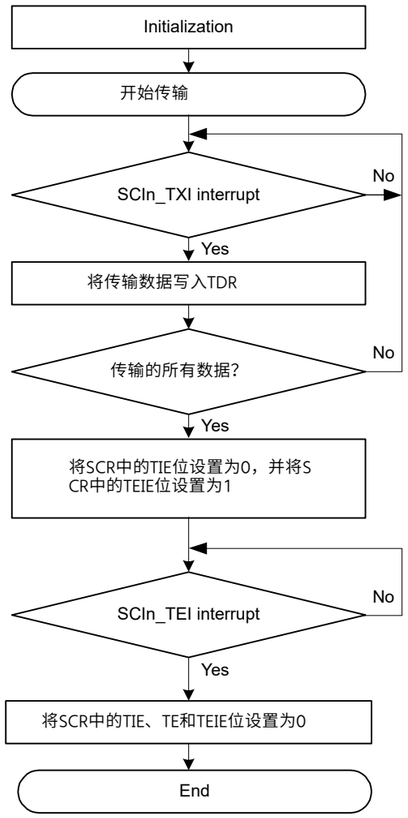
Figure 30.69 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 30.70 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the FTDRL[*1] register to the TSR register when data is written to FTDRL[*1] in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE bit is set to 1 but only after the SCR.TIE bit is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the SSR_FIFO.TDFE is set to 1. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine before transmission of the current transmit data has finished. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL from the handling routine for SCIn_TXI requests.
3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks whether non-transmitted data remains in FTDRL on output of the stop bit.



[1] [1]SCI初始化：设置数据传输。

[2] [2]通过SCIn_TXI中断请求将发送数据写入TDR：当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。传输数据从SCIn_TXI请求的处理例程中写入一次TDR。

[3] [3]串行传输继续程序：要继续串行传输，在接受传输数据空中断（SCIn_TXI）请求后将传输数据写入TDR。发送数据也可以通过SCIn_TXI中断请求激活DMAC或DTC写入TDR。当SCIn_TEI中断请求正在使用时，设置

将要传输的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1

Note: 当使用外部时钟时（SCR.CKE[1:0]位的值为10b或11b），SCKn引脚上最后一位的上升沿将SSR.TEND标志设置为1。设置SCR.TE位在这之后立即变为0可能会导致接收端接收数据保持时间不足。

Figure 30.69 选择非FIFO的时钟同步模式下的串行传输示例流程

(2)选择FIFO图30.70显示了在时钟同步模式下选择FIFO的串行传输示例。

在串行数据传输中，SCI操作如下：

1.当数据写入FTDRL*1时，SCI将数据从FTDRL*1寄存器传输到TSR寄存器
SCIn_TXI中断处理程序。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。发送开始时的SCIn_TXI中断请求在SCR.TE位设置为1时产生，但仅在SCR.TIE位也设置为1或当这两个位通过一条指令同时设置为1时产生。

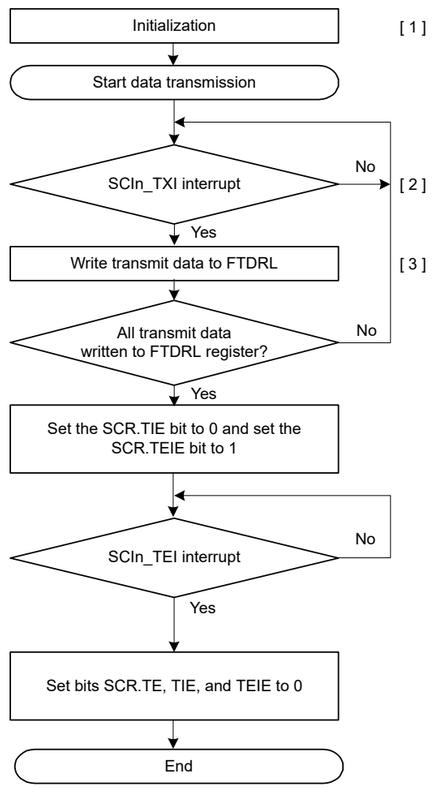
2.将数据从FTDRL传输到TSR后，SCI开始传输。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO.TDFE设置为1。当
SCR.TIE位设置为1，产生SCIn_TXI中断请求。在当前发送数据的发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入FTDRL来启用连续发送。当使用SCIn_TEI中断请求时，在SCIn_TXI请求的处理例程中将要发送的最后一个数据写入FTDRL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

3.指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当SPMR.CTSE位为1时，时钟信号的输出被暂停，直到输入CTS信号为低电平。

4.SCI在停止位输出时检查未传输的数据是否保留在FTDRL中。

5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, the SSR_FIFO.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In clock synchronous mode, FTDRH is not used.



[1]SCI initialization:
Set data transmission.
After the TE bit in SCR is set to 1, 1 is output for a frame, and transmission is enabled.

[2]Transmit data write to FTDRL by an SCIn_TXI interrupt request:
For transmission data from FTDRL to TSR, when the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL once in the SCIn_TXI interrupt handling routine.

[3]Serial transmission continuation procedure:
To continue serial transmission, write the next transmit data to FTDRL in this SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0 before transmission of the current transmit data finishes.
Transmit data can also be written to FTDRL by activating the DMAC or DTC. The TDFE flag is cleared automatically in this case. Do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCKn pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

Figure 30.70 Example flow of serial transmission in clock synchronous mode with FIFO selected

30.6.5 Serial Data Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 30.71 and Figure 30.72 show examples of SCI operation for serial reception in clock synchronous mode.

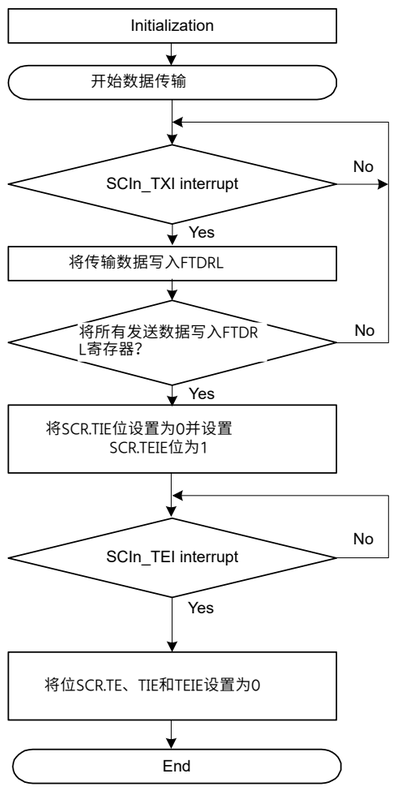
In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.

5.当FTDRL更新时，下一个传输数据从FTDRL传输到TSR并开始下一帧的串行传输。

6.如果FTDRL未更新，则SSR_FIFO.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR.TEIE位为1，则产生SCIn_TEI中断请求并且SCKn引脚保持高电平。

注1.在时钟同步模式下，不使用FTDRH。



[1]SCI初始化：设置数据传输。
SCR中的TE位设置为1后，每帧输出1，使能传输。

[2]通过SCIn_TXI中断请求向FTDRL发送数据写入：对于从FTDRL到TSR的发送数据，当写入FTDRL的发送数据量等于或小于指定的发送触发数时，发送数据FIFO空中断（SCIn_TXI)请求被生成。在SCIn_TXI中断处理例程中将发送数据写入FTDRL一次。

[3]串行传输继续程序：要继续串行传输，在这个SCIn_TXI中断处理程序中将下一个传输数据写入FTDRL并清除

在当前传输数据传输完成之前，SSR_FIFO.TDFE标志为0。发送数据也可以通过激活

DMAC或DTC。在这种情况下，TDFE标志会自动清除。
不要写入TDFE标志。
当SCIn_TEI中断请求正在使用时，设置
在将要传输的最后一个数据写入FTDRL后，SCR.TIE位为0，SCR.TEIE位为1。

Note: 当使用外部时钟时（SCR.CKE[1:0]位的值为10b或11b），SCKn引脚上最后一位的上升沿将SSR_FIFO.TEND标志设置为1。设置SCR.TE位在这之后立即变为0可能会导致接收端接收数据保持时间不足。

Figure 30.70 选择FIFO的时钟同步模式下的串行传输示例流程

30.6.5 时钟同步模式下的串行数据接收

(1) Non-FIFO selected

图30.71和图30.72显示了时钟同步模式下串行接收的SCI操作示例。

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚变为低电平。

2.SCI执行内部初始化，并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。

3.如果发生溢出错误，则SSR.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR寄存器。

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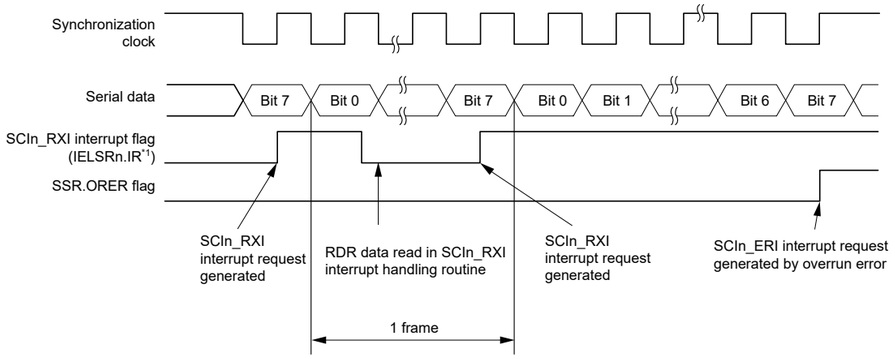
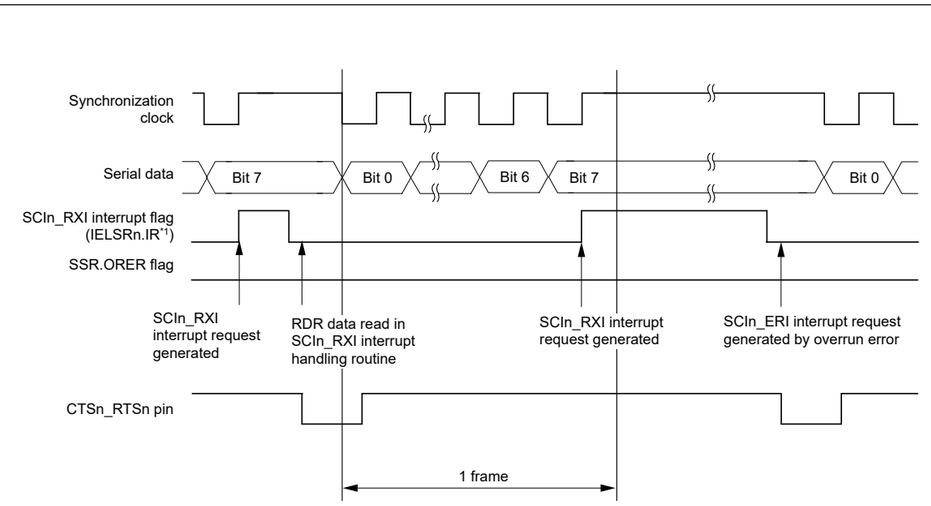
4. When reception completes successfully, receive data is transferred to the RDR register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the received data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.71 Example operation for serial reception in clock synchronous mode (1) when the RTS function is not used

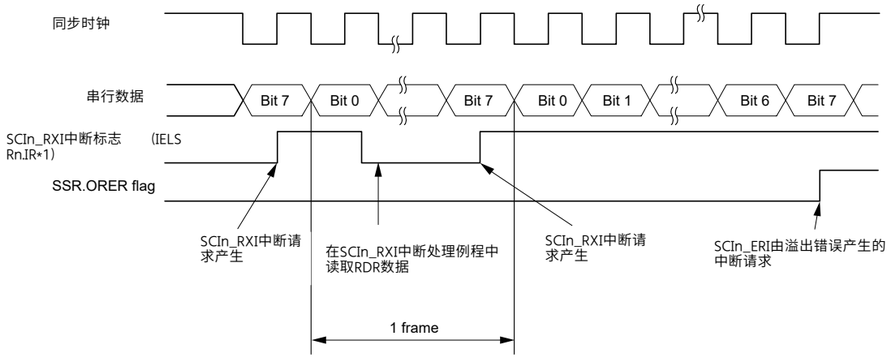


Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.72 Example operation for serial reception in clock synchronous mode (2) when RTS function is used

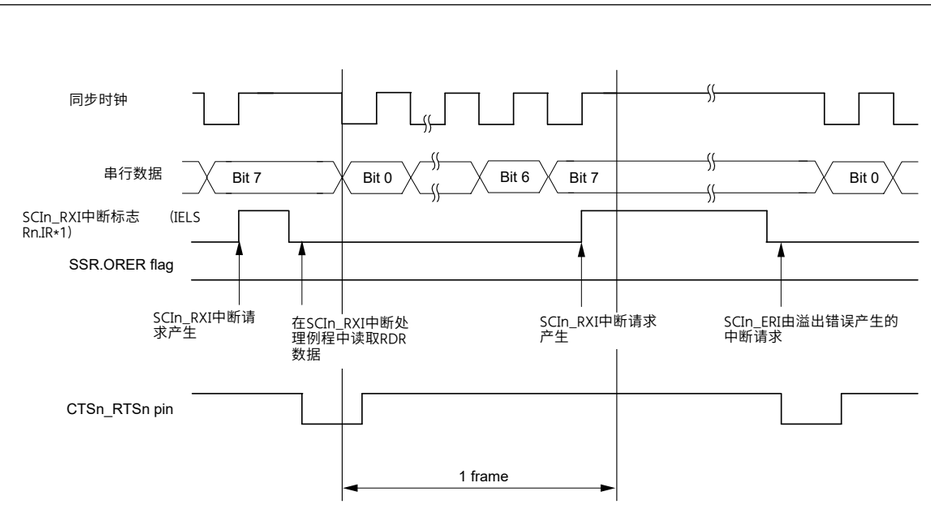
Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER flags in the SSR register to 0 before resuming data reception. Additionally, always read the RDR register during overrun error processing. When a data reception is forced to terminate by a 0 write to the SCR.RE bit during operation, read the RDR register because received data that is not yet read might be left in the RDR register.

4.当接收成功完成时，接收数据被传送到RDR寄存器。如果SCR.RIE位为1，则SCIn_RXI中断请求产生。连续接收是通过读取接收到的数据传输到在接收下一个接收数据完成之前，SCIn_RXI中断处理程序中的RDR寄存器。读取传输到RDR的接收数据会导致CTSn_RTSn引脚输出低电平。



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.71 不使用RTS功能时时钟同步模式下串行接收的示例操作(1)



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.72 使用RTS功能时时钟同步模式下串行接收的示例操作(2)

接收错误标志为1时无法恢复数据传输。因此，在恢复数据接收之前，将SSR寄存器中的ORER、FER和PER标志清除为0。此外，在溢出错误处理期间始终读取RDR寄存器。如果在操作期间通过向SCR.RE位写入0来强制终止数据接收，请读取RDR寄存器，因为尚未读取的已接收数据可能会留在RDR寄存器中。

Figure 30.73 shows an example flow of serial data reception.

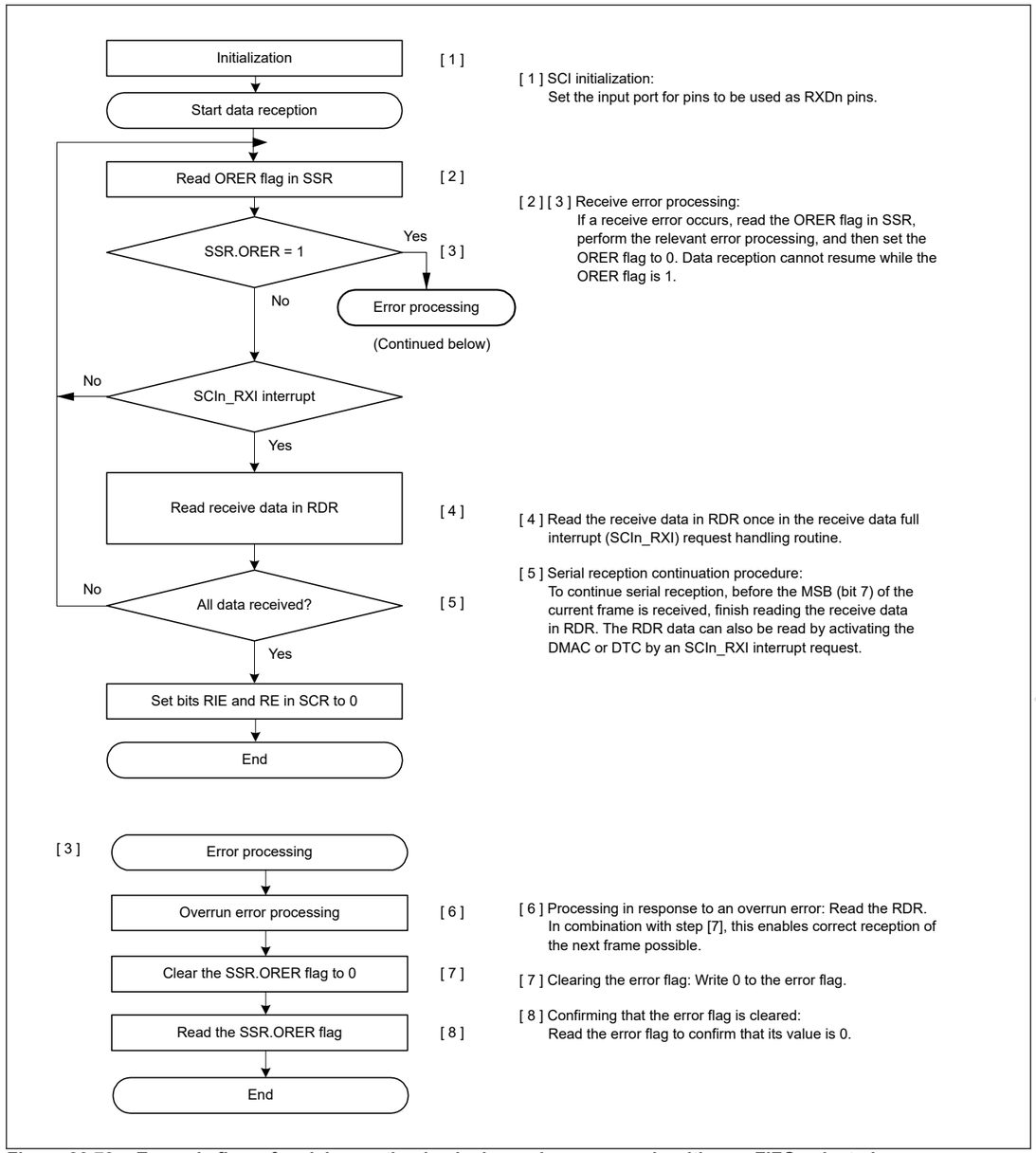


Figure 30.73 Example flow of serial reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 30.74 shows an example of serial reception in clock synchronous mode with FIFO selected.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.

图30.73显示了串行数据接收的示例流程。

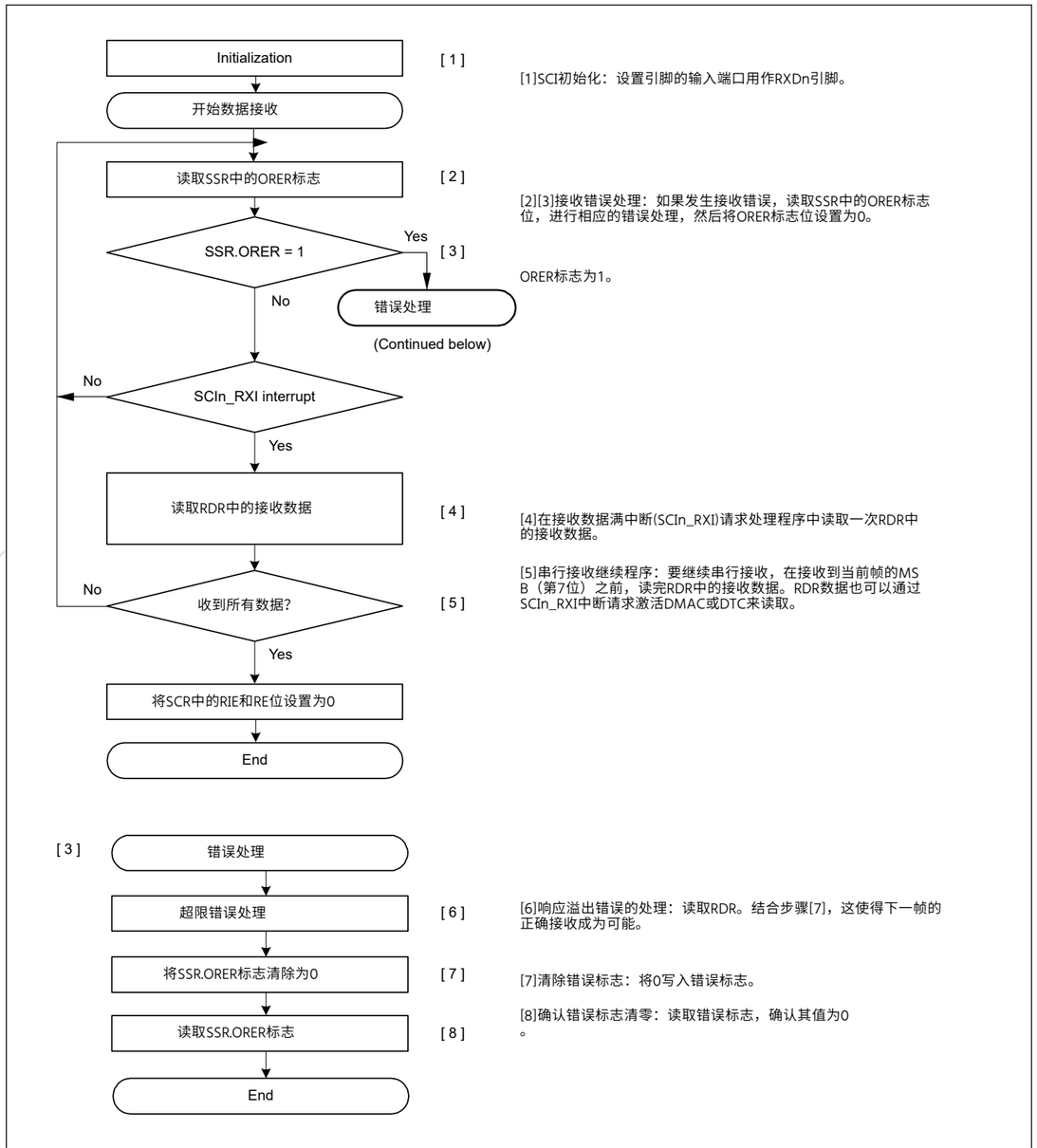


Figure 30.73 选择非FIFO的时钟同步模式下的串行接收示例流程

(2)选择FIFO图30.74显示了在时钟同步模式下选择FIFO的串行接收示例。

在串行数据接收中，SCI操作如下：

1.当SCR.RE位的值变为1时，CTSn_RTSn引脚变为低电平。

2.SCI执行内部初始化，并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。

3. If an overrun error occurs, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Received data is not transferred to the FRDRL[*1] register.
4. When data reception completes successfully, the receive data is transferred to the FRDRL[*1] register. The RDF flag is set to 1 when the amount of the receive data stored in FRDRL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL[*2] in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the RTS trigger number, the CTSn_RTSn pin goes low.

Note 1. In clock synchronous mode, FRDRH is not used.
Note 2. Read data in order from FRDRH to FRDRL when RDF and ORER are read with receive data.

3.如果发生溢出错误，则SSR_FIFO.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收到的数据不传送到FRDRL*1寄存器。

4.当数据接收成功完成时，接收数据被传送到FRDRL*1寄存器。当存储在FRDRL中的接收数据量等于或大于指定的接收触发数时，RDF标志设置为1。如果SCR.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理程序中读取传输到FRDRL*2的接收数据来启用连续数据接收。如果传输到FRDRL的接收数据量小于RTS触发数，则CTSn_RTSn引脚变为低电平。

注1.在时钟同步模式下，不使用FRDRH。
注2.RDF和ORER与接收数据一起读取时，按FRDRH到FRDRL的顺序读取数据。

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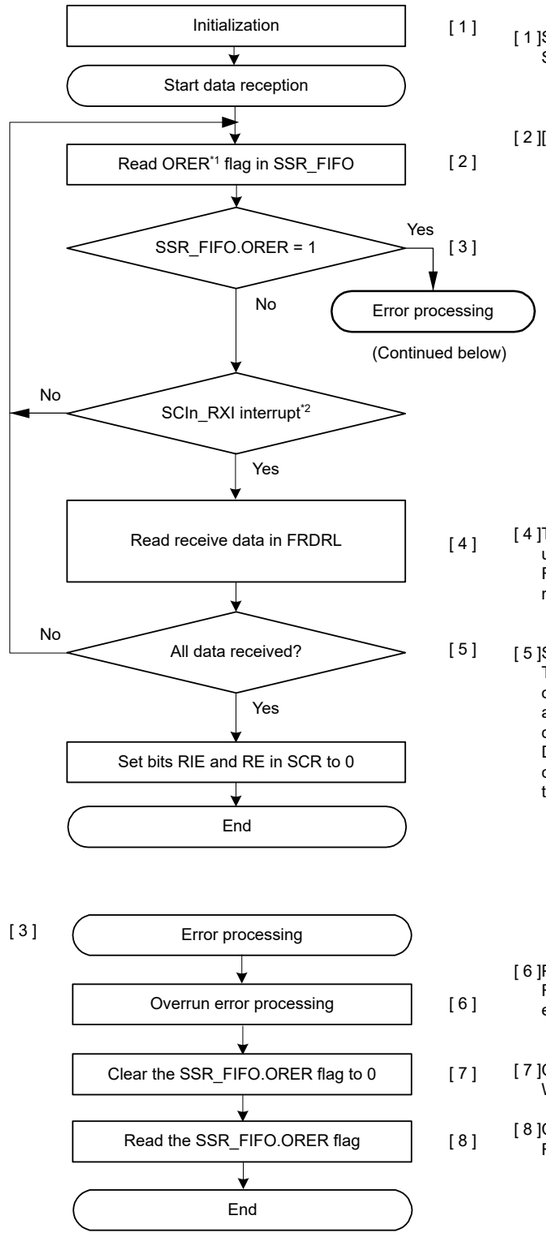


[1]SCI initialization:
Set the input port for pins to be used as RXDn pins.

[2][3]Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the SSR_FIFO.ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4]The receive data stored in FRDRL register is read until the amount of stored data is less than the FCR.RTRG[3:0] value. Software can check readable data in FDR.R[4:0].

[5]Serial reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0.The FRDRL data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.

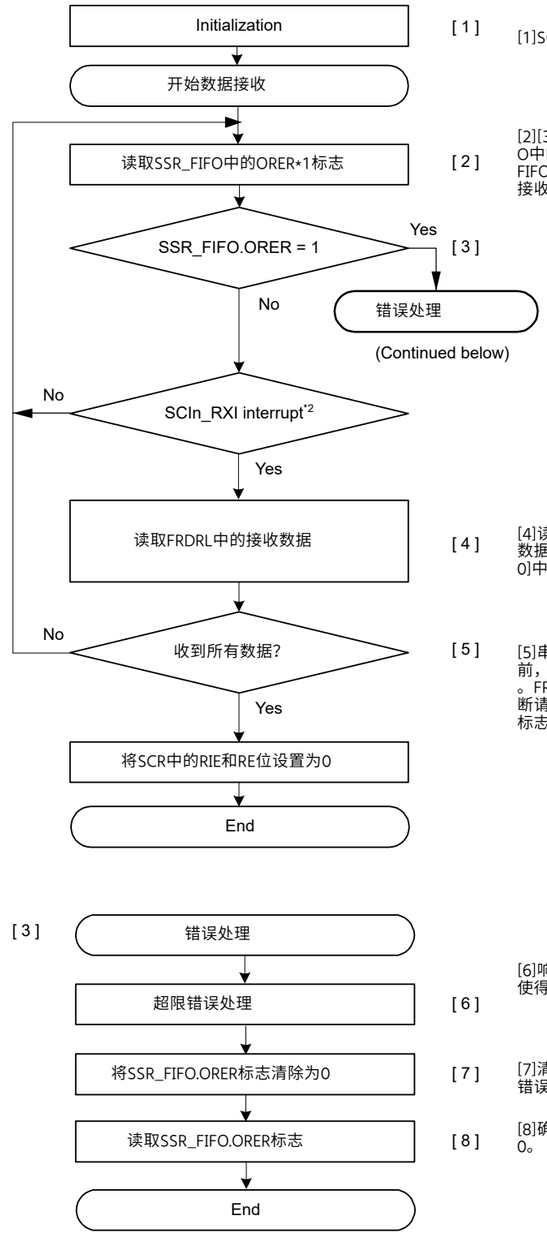
[6]Processing in response to an overrun error:
Read the FRDRL. In combination with step [7], this enables correct reception of the next frame possible.

[7]Clearing the error flag:
Write 0 to the error flag.

[8]Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. It can also be read from FRDRH.ORER. However, to clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data and is an integer times the FIFO triggering number.

Figure 30.74 Example flow of serial reception in clock synchronous mode with FIFO selected



[1]SCI初始化：设置引脚的输入端口用作RXDn引脚。

[2][3]接收错误处理：如果发生接收错误，读取SSR_FIFO中的ORER标志位，进行相应的错误处理，然后将SSR_FIFO.ORER标志位设置为0。当ORER标志位为1时，数据接收不能恢复。

[4]读取存储在FRRDL寄存器中的接收数据，直到存储的数据量小于FCR.RTRG[3:0]的值。软件可以检查FDR.R[4:0]中的可读数据。

[5]串行接收继续程序：要继续串行接收，在发生溢出错误之前，完成FRRDL中的接收数据读取并将SSR_FIFO.RDF标志清0。FRRDL数据也可以通过激活DMAC或DTC来读取SCIn_RXI中断请求。在这种情况下，RDF标志会自动清除。不要写入RDF标志。

[6]响应溢出错误的处理：读取FRRDL。结合步骤[7]，这使得下一帧的正确接收成为可能。

[7]清除错误标志：将0写入错误标志。

[8]确认错误标志清零：读取错误标志，确认其值为0。

注1.也可以从FRDRH.ORER中读取。但是，要清除ORER标志，请将0写入SSR_FIFO寄存器中的相关位。

注2.应该是全部接收数据，是FIFO触发数的整数倍。

Figure 30.74 选择FIFO的时钟同步模式下的串行接收示例流程

30.6.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 30.75 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the SSR.TEND flag is set to 1.
2. Initialize the SCR register, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the RIE and RE bits to 0, and then check that the receive error flag ORER in the SSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

30.6.6 时钟同步的同时串行数据发送和接收 Mode

(1) Non-FIFO selected

图30.75显示了时钟同步模式下同时串行发送和接收操作的示例流程。
初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

1.通过验证SSR.TEND标志是否设置为1来检查SCI是否完成数据传输。

2.初始化SCR寄存器，然后通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1.检查SCI是否完成数据接收。

2.将RIE和RE位设置为0，然后检查SSR寄存器中的接收错误标志ORER是否为0。

3.通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

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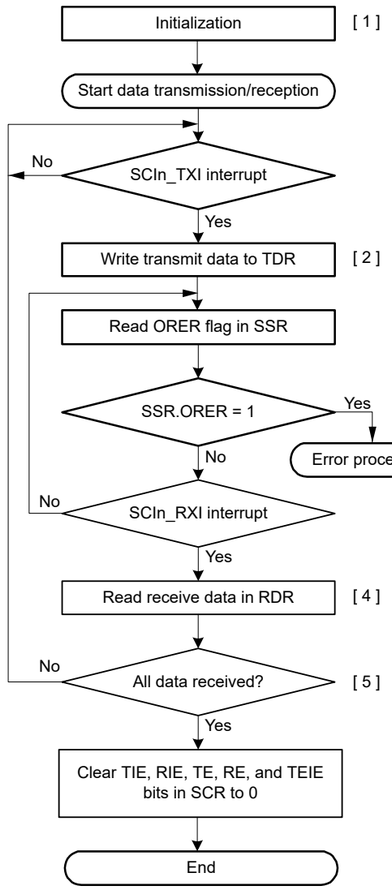


[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the SCIn_TXI interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in RDR once in the SCIn_RXI interrupt request handling routine.

[5] Serial transmission/reception continuation procedure:
To continue serial transmission and reception, before the MSB bit 7 of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB bit 7 of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data can also be written to TDR by activating the DMAC or DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DMAC or DTC by a receive data full interrupt (SCIn_RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 30.75 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 30.76 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

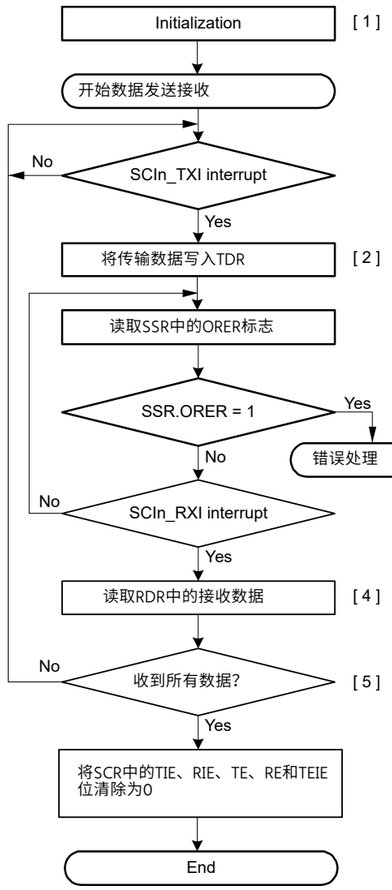
After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the SSR_FIFO.TEND flag is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.



[1]SCI初始化：TXDn管脚可以作为发送数据的输出管脚，RXDn管脚同时可以作为接收数据的输入管脚。

[2]发送数据写入：在SCIn_TXI中断请求处理程序中将发送数据写入TDR一次。

[3]接收错误处理：如果发生接收错误，读取SSR中的ORER标志，进行相关的错误处理，然后将ORER标志设置为0。当ORER标志为1时，数据接收不能恢复。

[4]读取接收数据：在RDR中读取一次接收数据

SCIn_RXI中断请求处理程序。

[5]串口发送接收继续流程：要继续串口发送和接收，在接收到当前帧的MSB位7之前，通过SCIn_RXI中断读完RDR中的接收数据。此外，在当前帧的MSB位7发送之前，通过SCIn_TXI中断将数据写入TDR。发送数据也可以通过发送数据空中断(SCIn_TXI)请求激活DMAC或DTC写入TDR。同样，也可以通过接收数据完全中断(SCIn_RXI)请求激活DMAC或DTC来读取RDR数据。

Note: 从发送或接收操作切换到同时发送和接收操作时，首先设置TIE、RIE、SCR中的TE、RE和TEIE位为0，然后将TIE、RIE、TE和RE位同时设置为1。

Figure 30.75 选择非FIFO的时钟同步模式下同时串行发送和接收的示例流程

(2) FIFO selected

图30.76显示了在时钟同步模式下同时串行发送和接收操作的示例流程，其中
FIFO selected.

初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

1.通过验证SSR_FIFO.TEND标志设置为1来检查SCI是否完成传输。

2.初始化SCR寄存器，然后通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1.检查SCI是否完成接收。

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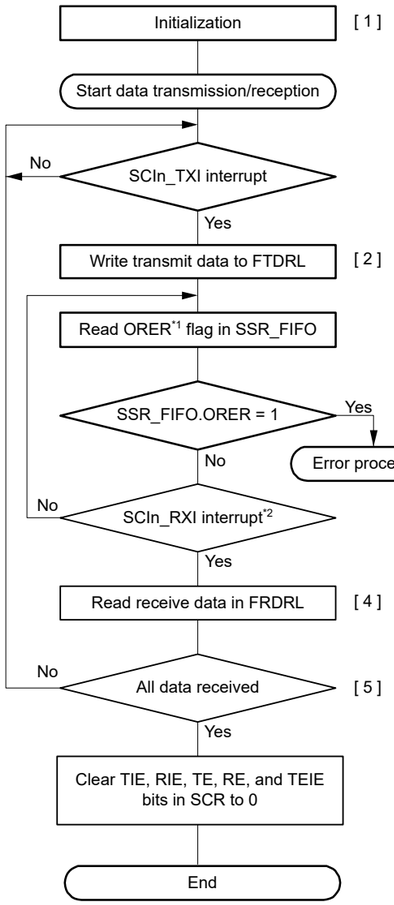
2. Set the RIE and RE bits to 0.
3. Check that the receive error flags ORER in the SSR_FIFO register are 0, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI interrupt request handling routine. The number of transmission data that can be written is 16 bits, which is the number of stored transmit data in the FIFO.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, performthe relevant error processing, and then set the ORER flag to 0. Data reception cannot resume while the ORER flag is 1.

[4] Reading receive data:
The reception data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

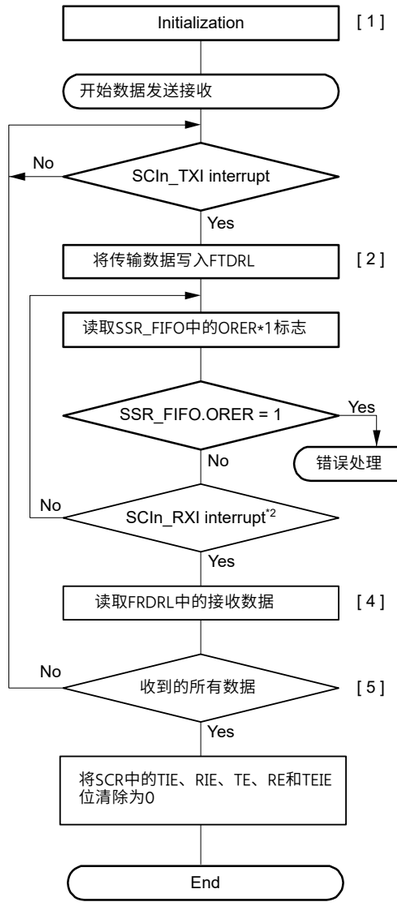
[5] Serial transmission/reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data is finished, write the next transmit data to FTDRL in the SCIn_TXI interrupthandling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DMAC or DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DMAC or DTC by a receive FIFO data full interrupt (SCIn_RXI) request.
The RDF and TDFE flags are cleared automatically in this case. Do not write to the RDF and TDFE flags.

Note 1. It can also be read from FRDRH.ORER. To clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data with amount an integer times FIFO triggering number.

Figure 30.76 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

2.将RIE和RE位设置为0。

3.检查SSR_FIFO寄存器中的接收错误标志ORER是否为0，然后通过一条指令将SCR寄存器中的TIE、RIE、TE和RE位同时设置为1。



[1] SCI initialization:
TXDn引脚可用作传输数据的输出引脚，RXDn引脚可用作

同时接收数据的输入引脚。

[2] 发送数据写入：
在SCIn_TXI中断请求处理例程中将发送数据写入FTDRL。可写入的发送数据个数为16位，即FIFO中存储的发送数据个数。

[3] 接收错误处理：
如果发生接收错误，则读取SSR_FIFO中的ORER标志位，进行相关的错误处理，然后将ORER标志位设置为0。当ORER标志位为1时，无法恢复数据接收。

[4] 读取接收数据：
读取存储在FRDRL寄存器中的接收数据，直到存储的数据数量小于FCR.RTRG值。软件可以检查FDR.R[4:0]中的可读数据。

[5]串口发送接收继续流程：要继续串口接收，在发生溢出错误之前，完成FRRDL中的接收数据读取并将SSR_FIFO.RDF标志清0。要继续串口发送，在当前发送数据的发送完成之前，在SCIn_TXI中断处理程序中将下一个发送数据写入FTDRL，并将SSR_FIFO.TDFE标志清零。发送数据也可以通过发送FIFO数据空中断(SCIn_TXI)请求激活DMAC或DTC写入FTDRL。同样，也可以通过接收FIFO数据满中断(SCIn_RXI)请求激活DMAC或DTC来读取FRDRL数据。在这种情况下，RDF和TDFE标志会自动清除。不要写入RDF和TDFE标志。

注1.也可以从FRDRH.ORER中读取。要清除ORER标志，请将0写入SSR_FIFO寄存器中的相关位。
注2.应该是所有接收数据的数量为FIFO触发数的整数倍。

Figure 30.76 选择FIFO的时钟同步模式下同时串行发送和接收的示例流程

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30.7 Operation in Smart Card Interface Mode

The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

Smart card interface mode can be selected using the appropriate register.

30.7.1 Example Connection

Figure 30.77 shows an example connection between a smart card (IC card) and the MCU. As shown in Figure 30.77, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

Setting the SCR_SMCI.TE and SCR_SMCI.RE bits to 1 with an IC card disconnected enables closed-loop transmission or reception, allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

An output port of the MCU can be used to output a reset signal.

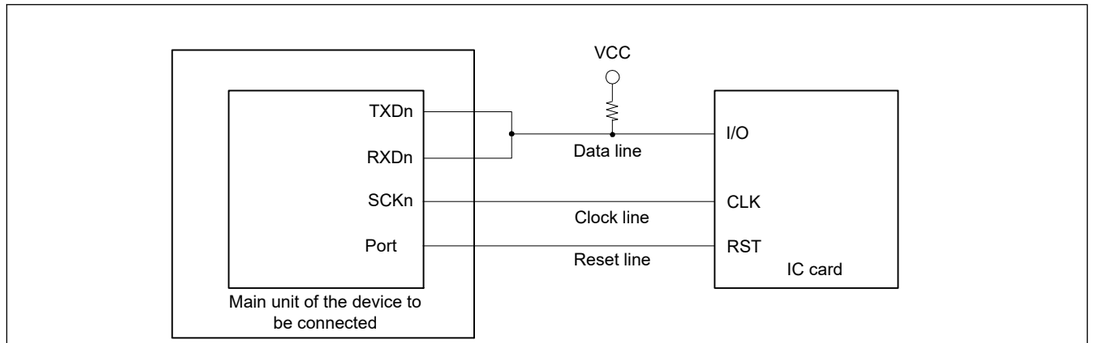

Figure 30.77 Example connection with a smart card (IC card)

30.7.2 Data Format (Except in Block Transfer Mode)

Figure 30.78 shows the data transfer formats in smart card interface mode:

- One frame consists of 8-bit data and a parity bit in asynchronous mode.
- During transmission, at least 2 ETUs (elementary time unit – the time required for transferring 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame.
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit.
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

30.7 智能卡接口模式下的操作

SCI支持符合ISOIEC7816-3（识别卡标准）的智能卡（IC卡）接口，作为SCI的扩展功能。

可以使用适当的寄存器选择智能卡接口模式。

30.7.1 示例连接

图30.77显示了智能卡（IC卡）和MCU之间的示例连接。如图30.77所示，由于MCU使用单条传输线与IC卡通信，因此将TXDn和RXDn引脚互连，并使用电阻将数据传输线上拉到VCC。

在断开IC卡的情况下将SCR_SMCI.TE和SCR_SMCI.RE位设置为1可启用闭环发送或接收，从而实现自诊断。要将SCI产生的时钟脉冲提供给IC卡，请将SCKn引脚输出输入到IC卡的CLK引脚。

MCU的输出端口可用于输出复位信号。

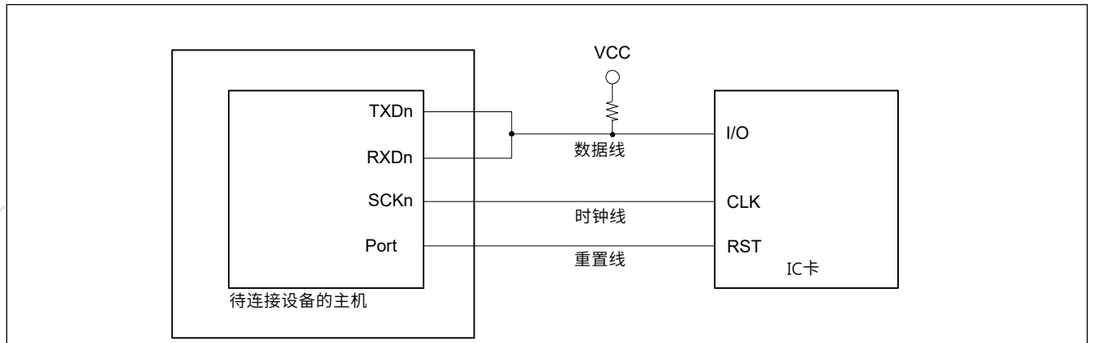

Figure 30.77 与智能卡（IC卡）的连接示例

30.7.2 数据格式（块传输模式除外）

图30.78显示了智能卡接口模式下的数据传输格式：

- 一帧由8位数据和一个异步模式的奇偶校验位组成。
- 在传输过程中，至少设置2个ETU（基本时间单位——传输1位所需的时间）作为从奇偶校验位结束到下一帧开始的保护时间。
- 如果在接收过程中检测到奇偶校验错误，则在从起始位经过10.5ETU后输出1ETU的低错误信号。
- 如果在传输过程中对错误信号进行采样，相同的数据会在至少2个ETU后自动重传。

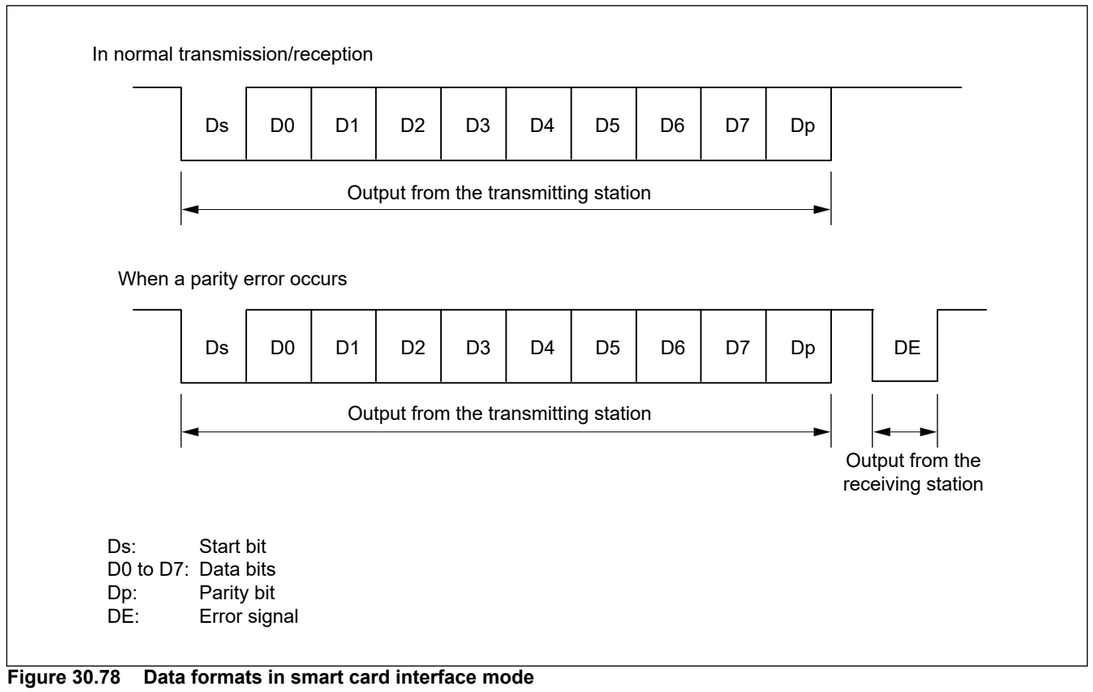

Figure 30.78 Data formats in smart card interface mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 indicate the Z and A states, respectively, and data is transferred with LSB-first for the start character, as shown in Figure 30.79. Therefore, data in the start character in the figure is 0x3B.

When using the direct convention type, write 0 to both the SCMR.SDIR and SCMR.SINV bits. Write 0 to the SMR_SMCI.PM bit to use even parity, which is prescribed by the smart card standard.

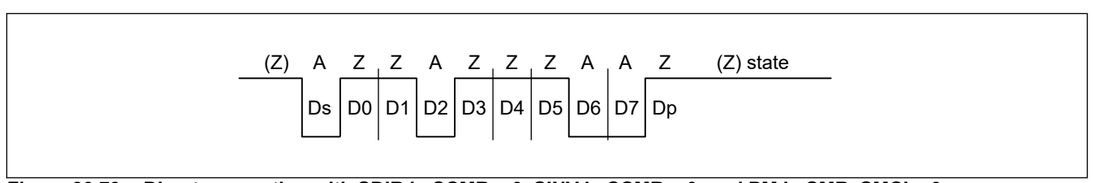

Figure 30.79 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 indicate the A and Z states, respectively, and data is transferred with MSB-first for the start character, as shown in Figure 30.80. Therefore, data in the start character in the figure is 0x3F.

When using the inverse convention type, write 1 to both the SCMR.SDIR and SCMR.SINV bits. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to the Z state. Because the SINV bit of the MCU only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

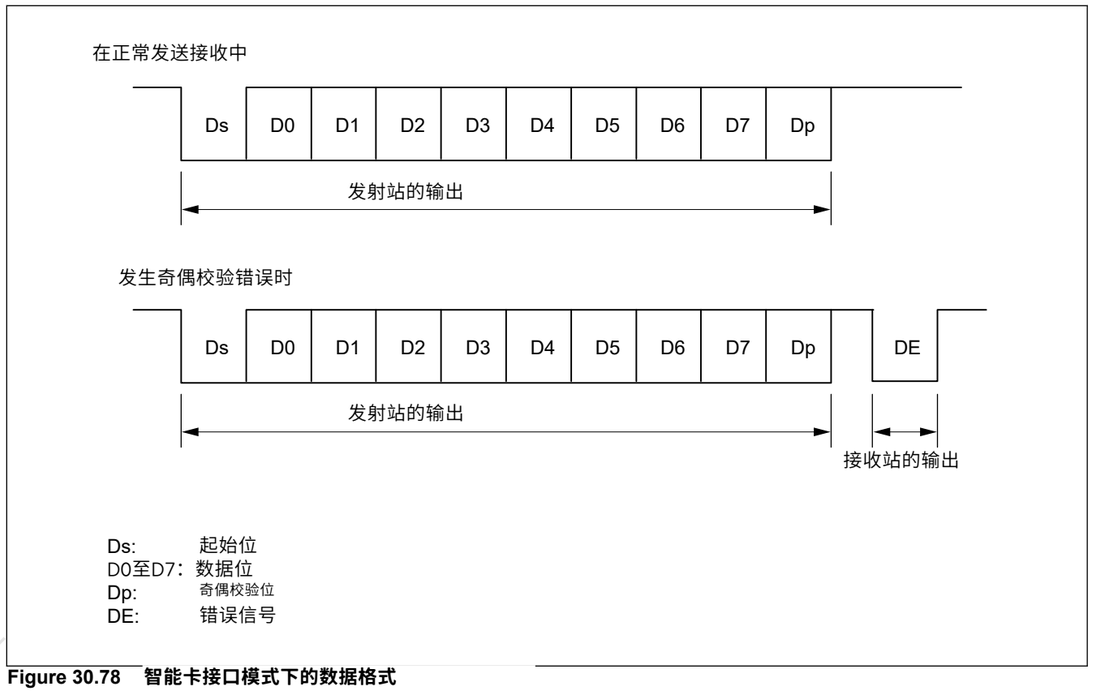

Figure 30.78 智能卡接口模式下的数据格式

与直接约定型和逆约定型IC卡进行通信时，请按照本节的步骤进行。

(1) 直接约定型

对于直接约定类型，逻辑电平1和0分别表示Z和A状态，数据通过LSB-first为起始字符，如图30.79所示。因此，图中起始字符中的数据为0x3B。

使用直接约定类型时，将0写入SCMR.SDIR和SCMR.SINV位。将0写入SMR_SMCI.PM位使用智能卡标准规定的偶校验。

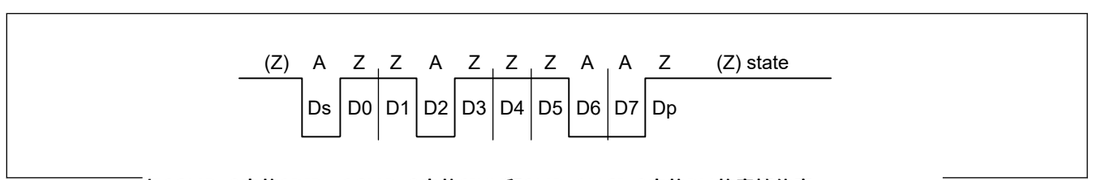

Figure 30.79 与SCMR=0中的SDIR、SCMR=0中的SINV和SMR_SMCI=0中的PM的直接约定

(2) 逆约定型

对于逆约定类型，逻辑电平1和0分别表示A和Z状态，数据通过MSB-first为起始字符，如图30.80所示。因此，图中起始字符中的数据为0x3F。

使用逆约定类型时，将1写入SCMR.SDIR和SCMR.SINV位。奇偶校验位为逻辑电平0，产生偶校验，这是智能卡标准规定的，对应于Z状态。由于MCU的SINV位仅将数据位D7反转为D0，因此向SMR_SMCI中的PM位写入1以反转发送和接收的奇偶校验位。

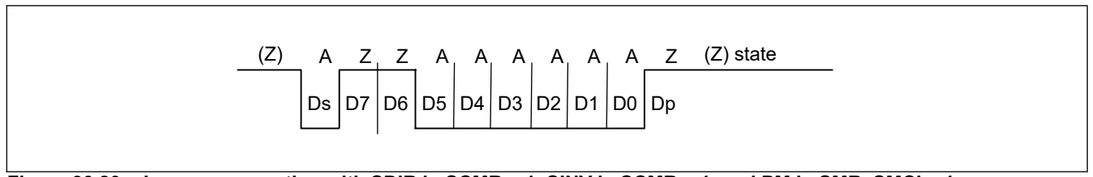

Figure 30.80 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

30.7.3 Block Transfer Mode

Block transfer mode differs from normal smart card interface mode as follows:

- Even if a parity error is detected during reception, no error signal is output. Because the PER flag in SSR_SMCI is set by error detection, clear the PER flag before receiving the parity bit of the next frame.
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in normal smart card interface mode, but the flag is read as 0 because no error signal is transferred

30.7.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate set up in the SCMR.BCP2 and the SMR_SMCI.BCP[1:0] bits. The frequency is always 16 times the bit rate in normal asynchronous mode.

For data reception, the falling edge of the start bit is sampled with the base clock to perform internal synchronization.

Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 30.81. The reception margin is determined by the following formula:

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock ($N = 32, 64, 372, 256$)

D: Duty cycle of clock ($D = 0$ to 1.0)

L: Frame length ($L = 10$)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined using the following formula:

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$$

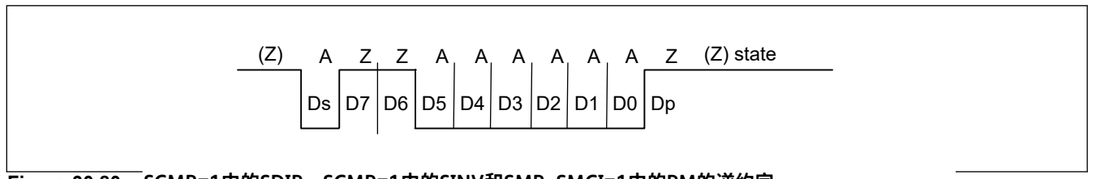

Figure 30.80 SCMR=1中的SDIR、SCMR=1中的SINV和SMR_SMCI=1中的PM的逆约定

30.7.3 块传输模式

块传输模式与普通智能卡接口模式的区别如下：

●即使在接收过程中检测到奇偶校验错误，也不会输出错误信号。因为SSR_SMCI中的PER标志是由错误检测设置的，所以在接收下一帧的奇偶校验位之前清除PER标志。

●在传输过程中，从奇偶校验位结束到下一帧开始至少设置1个ETU作为保护时间

●由于没有重传相同的数据，所以在传输开始后，SSR_SMCI中的TEND标志设置为11.5ETU

●在块传输模式下，SSR_SMCI中的ERS 标志指示错误信号状态，与普通智能卡接口模式一样，但该标志被读取为0，因为没有传输错误信号

30.7.4 接收数据采样时序和接收裕量

只有片内波特率发生器产生的内部时钟可以用作智能卡接口模式下的传输时钟。

在这种模式下，SCI可以在频率为SCMR.BCP2和SMR_SMCI.BCP[1:0]位。在正常异步模式下，频率始终是比特率的16倍。

对于数据接收，起始位的下降沿用基准时钟进行采样，以进行内部同步。

接收数据在基本时钟的第16、32、186、128、46、64、93和256个上升沿进行采样，以便在每个位的中间锁存，如图30.81所示。接收余量由以下公式确定：

$$M = \left|\left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\right| \times 100\ [\%]$$

M：接收余量（%）

N：比特率与时钟的比率（N=32、64、372、256）

D：时钟的占空比（D=0到1.0）

L：帧长（L=10）

F：时钟频率偏差的绝对值

假设指定公式中的F=0、D=0.5和N=372的值，则使用以下公式确定接收余量：

$$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\ \%$$

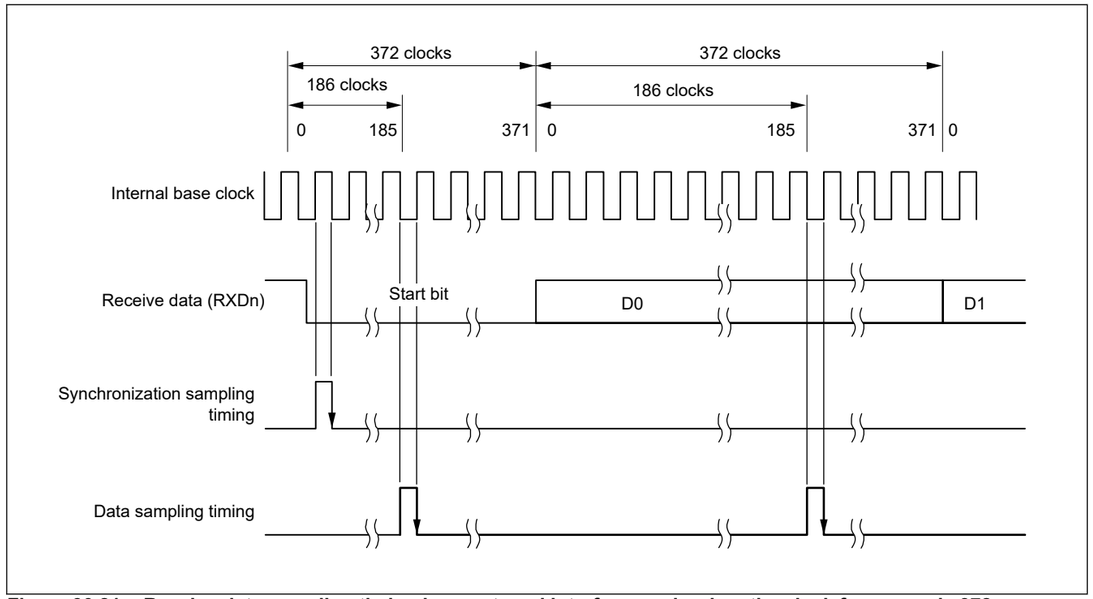

Figure 30.81 Receive data sampling timing in smart card interface mode when the clock frequency is 372 times the bit rate

30.7.5 SCI Initialization (Smart Card Interface Mode)

Before transmitting and receiving data, write the initial value 0x00 in the SCR_SMCI register and initialize the SCI following the example flow shown in Table 30.39.

Always set the initial value in the TIE, RIE, TE, RE, TEIE bits in the SCR_SMCI register before switching from transmission to reception mode or from reception to transmission mode. When SCR_SMCI.RE is set to 0, the RDR register is not initialized.

To change from reception mode to transmission mode, first check that reception has completed, then initialize the SCI. At the end of initialization, set SCR_SMCI.TE = 1 and SCR_SMCI.RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in SSR_SMCI.

To change transmission mode to reception mode, first check that transmission has completed, then initialize the SCI. At the end of initialization, set SCR_SMCI.TE = 0 and SCR_SMCI.RE = 1. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

Table 30.39 Example flow of SCI initialization in smart card interface mode (1 of 2)

No.	Step Name	Description
1	Start initialization	
2	Set SCR_SMCI.TIE, RIE, TE, RE, TEIE, and CKE[1:0] to 0	Stop the communication and initialize SKE[1:0].
3	Set SIMR1.IICM bit to 0. Set SCMR.SMIF to 1.	Set to smart card interface mode.
4	Set SSR_SMCI.ORER, ERS, PER to 0	Write to SSR_SMCI after reading SSR_SMCI.
5	Set SPMR.CKPH, CKPOL	Set the transmission or reception format in SPMR.
6	Set SMR_SMCI.GM, BLK, PM, BCP[1:0], CKS[1:0], and set SMR_SMCI.PE to 1	Set the operation mode and the transmission or reception format in SMR_SMCI.
7	Set SCMR.BCP2, SDIR, SINV	Set the transmission or reception format in SCMR.
8	Set SPTR to the initial value.	Set the Initial value to SPTR.

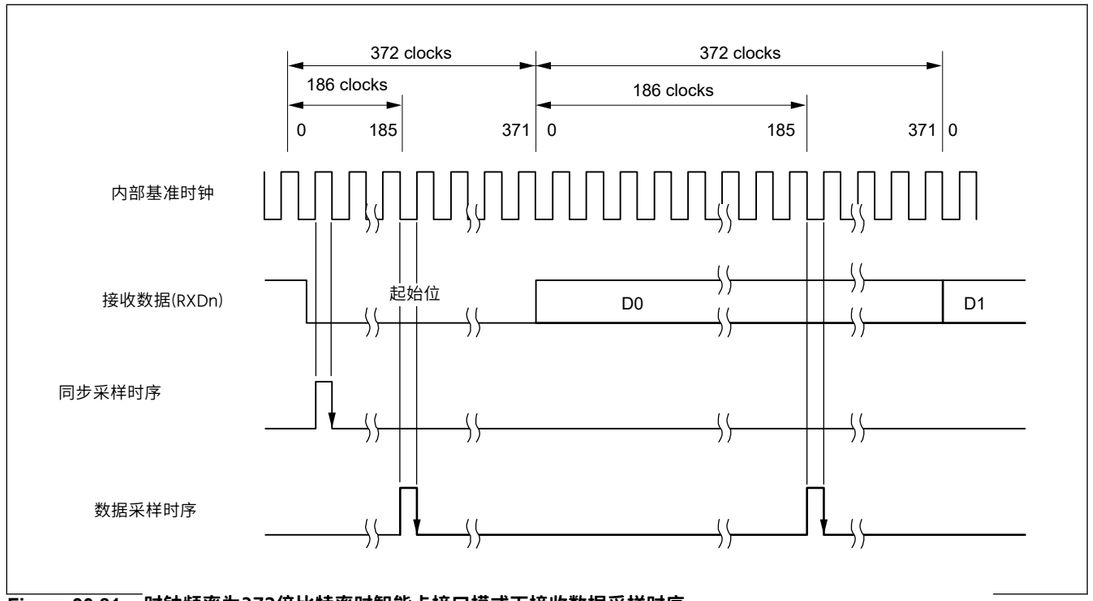

Figure 30.81 时钟频率为372倍比特率时智能卡接口模式下接收数据采样时序

30.7.5 SCI初始化（智能卡接口模式）

在发送和接收数据之前，将初始值0x00写入SCR_SMCI寄存器并按照表30.39所示的示例流程初始化SCI。

在从发送模式切换到接收模式或从接收模式切换到发送模式之前，请务必在SCR_SMCI寄存器中的TIE、RIE、TE、RE、TEIE位中设置初始值。当SCR_SMCI.RE设置为0时，RDR寄存器未初始化。

要从接收模式更改为发送模式，首先检查接收是否完成，然后初始化SCI。在初始化结束时，设置SCR_SMCI.TE=1和SCR_SMCI.RE=0。可以通过读取SSR_SMCI中的SCIn_RXI请求、ORER或PER标志来验证接收完成。

要将传输模式更改为接收模式，首先检查传输是否完成，然后初始化SCI。在初始化结束时，设置SCR_SMCI.TE=0和SCR_SMCI.RE=1。可以通过读取SSR_SMCI中的TEND标志来验证传输完成。

Table 30.39 智能卡接口模式下SCI初始化示例流程（1of2）

No.	步骤名称	Description
1	开始初始化	
2	将SCR_SMCI.TIE、RIE、TE、RE、TEIE和CKE[1:0]设置为0	停止通信并初始化SKE[1:0]。
3	将SIMR1.IICM位设置为0。 将SCMR.SMIF设置为1。	设置为智能卡接口模式。
4	设置SSR_SMCI.ORER、ERS、每到0	读取SSR_SMCI后写入SSR_SMCI。
5	Set SPMR.CKPH, CKPOL	在SPMR中设置发送或接收格式。
6	Set SMR_SMCI.GM, BLK, PM, BCP[1:0]、CKS[1:0]，并设置 SMR_SMCI.PE to 1	在SMR_SMCI中设置操作模式和发送或接收格式。
7	Set SCMR.BCP2, SDIR, SINV	在SCMR中设置发送或接收格式。
8	将SPTR设置为初始值。	将初始值设置为SPTR。

Table 30.39 Example flow of SCI initialization in smart card interface mode (2 of 2)

No.	Step Name	Description
9	Set SEMR.BRME and SEMR.RXDESEL to 0	Set SEMR.BRME and SEMR.RXDESEL to 0.
10	Set a value in BRR	Write the value for the bit rate in BRR.
11	Set the I/O port functions	Set the I/O port functions for TXDn, RXDn, and SCKn.
12	Set a value in SCR_SMCI.CKE[1:0]	Set the SCR_SMCI.CKE[1:0]. Even though the function depends on SMR_SMCI.GM, when the CKE[0] bit is set to 1, the clock is output from the SCKn pin.
13	Set SCR_SMCI.TE or RE to 1, and set SCR_SMCI.TIE, RIE	Set the TE or RE bit in SCR_SMCI to 1, then set the TIE and RIE bits in SCR_SMCI. Do not simultaneously set the TE and RE bits to 1 if self-diagnosis is not used.
14	Initialization completed	

30.7.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be re-transmitted in smart card mode. Figure 30.82 shows the data re-transfer operation during transmission.

1. When an error signal from the receiver end is sampled after 1-frame data is transmitted, the SSR_SMCI.ERS flag is set to 1. If the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
2. For a frame in which an error signal is received, the SSR_SMCI.TEND flag is not set. Data is re-transferred from TDR to TSR, allowing automatic data retransmission.
3. If no error signal is returned from the receiver, the ERS flag is not set to 1.
4. In this case, the SCI determines that transmission of 1-frame data, including the re-transfer, is complete, and the TEND flag is set. If the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 30.84 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DTC or DMAC.

When the SSR_SMCI.TEND flag is set to 1 in transmission and when the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated.

The DTC or DMAC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 before enabling an SCIn_ERI interrupt request to be generated if an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings.

For DTC or DMAC settings, see section 17, Data Transfer Controller (DTC), section 16, DMA Controller (DMAC).

Table 30.39 智能卡接口模式下SCI初始化流程示例（2之2）

No.	步骤名称	Description
9	将SEMR.BRME和SEMR.RXDESEL设置为0	将SEMR.BRME和SEMR.RXDESEL设置为0。
10	在BRR中设置一个值	在BRR中写入比特率的值。
11	设置IO端口功能	设置TXDn、RXDn和SCKn的IO端口功能。
12	在中设置一个值 SCR_SMCI.CKE[1:0]	设置SCR_SMCI.CKE[1:0]。即使函数依赖于SMR_SMCI.GM，当CKE[0]位设置为1，时钟从SCKn引脚输出。
13	将SCR_SMCI.TE或RE设置为1，并设置SCR_SMCI.TIE、RIE	将SCR_SMCI中的TE或RE位设置为1，然后设置SCR_SMCI中的TIE和RIE位。如果不使用自诊断，请勿同时将TE和RE位设置为1。
14	初始化完成	

30.7.6 串行数据传输（块传输模式除外）

智能卡接口模式下的串行数据传输（块传输模式除外）与非智能卡接口模式下的串行数据传输不同之处在于，在智能卡模式下对错误信号进行采样，数据可以重新传输。图30.82显示了传输过程中的数据重传操作。

1.发送1帧数据后，在接收端采样到错误信号时，SSR_SMCI.ERS标志置1。如果SCR_SMCI.RIE位为1，则产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将ERS 标志清零。

2.对于接收到错误信号的帧，不设置SSR_SMCI.TEND标志。数据从TDR重新传输到TSR，允许自动数据重新传输。

3.如果接收器没有返回错误信号，则ERS 标志不设置为1。

4.在这种情况下，SCI确定1帧数据的传输（包括重新传输）已完成，并设置TEND标志。如果SCR_SMCI.TIE位为1，则产生SCIn_TXI中断请求。将传输数据写入TDR以开始传输下一个数据。

图30.84显示了串行传输的示例流程。所有处理步骤都使用一个自动执行SCIn_TXI中断请求以激活DTC或DMAC。

当发送中SSR_SMCI.TEND标志设置为1且SCR_SMCI.TIE位为1时，将产生SCIn_TXI中断请求。

如果先前将SCIn_TXI中断请求指定为DTC或DMAC激活源，则DTC或DMAC由SCIn_TXI中断请求激活，从而允许传输发送数据。当DTC或DMAC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在此重传期间，TEND标志保持为0，并且DTC或DMAC未激活。因此，SCI和DTC或DMAC会自动传输指定的字节数，包括发生错误时的重传。因为ERS 标志不会自动清零，所以如果发生错误，在使能SCIn_ERI中断请求之前将RIE位设置为1，并将ERS 标志清零。

使用DTC或DMAC发送或接收数据时，请务必在进行SCI设置之前启用DTC或DMAC。

对于DTC或DMAC设置，请参阅第17节，数据传输控制器(DTC)，第16节，DMA控制器(DMAC)。

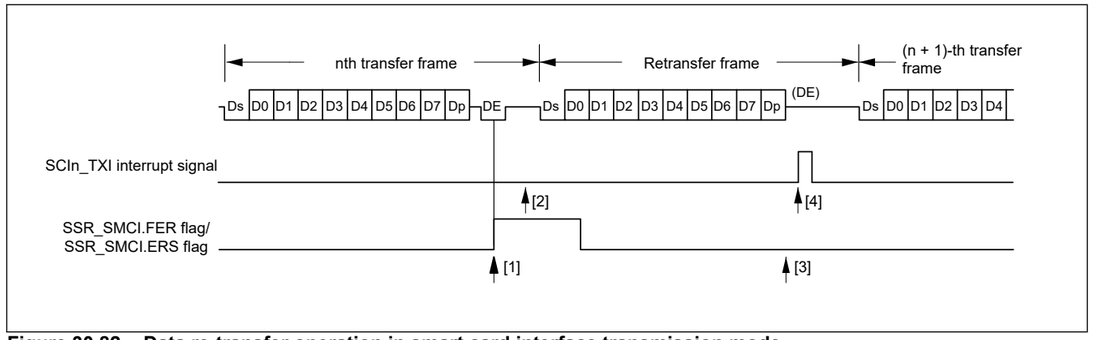

Figure 30.82 Data re-transfer operation in smart card interface transmission mode

The SSR_SMCI.TEND flag is set at different timings depending on the SMR_SMCI.GM bit setting. Figure 30.83 shows the TEND flag generation timing.

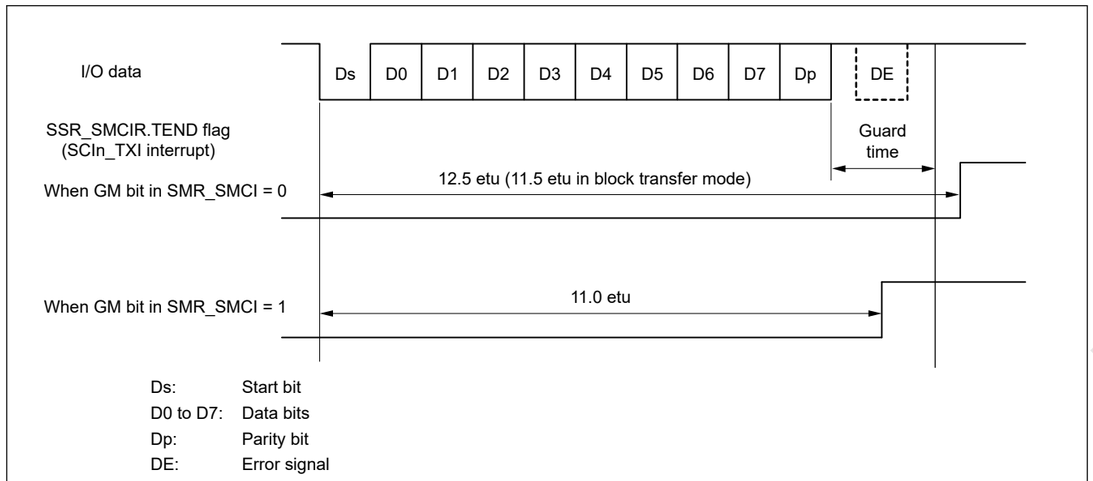

Figure 30.83 SSR.TEND flag generation timing during transmission

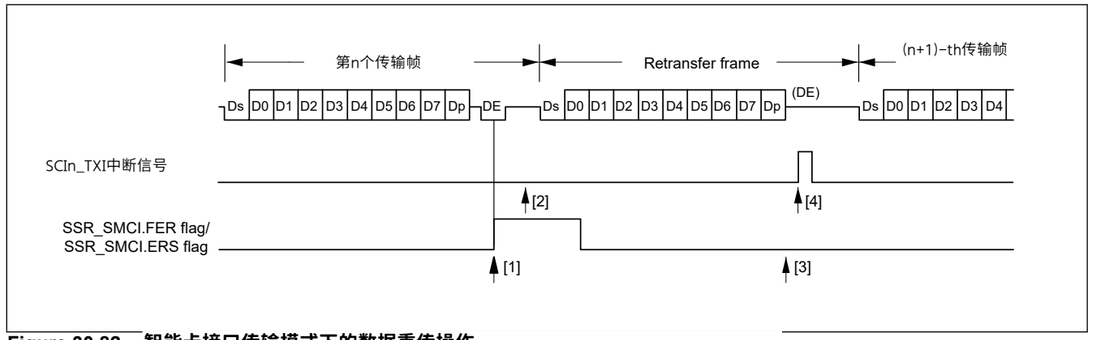

Figure 30.82 智能卡接口传输模式下的数据重传操作

SSR_SMCI.TEND标志根据SMR_SMCI.GM位设置在不同的时间设置。图30.83显示了TEND标志生成时序。

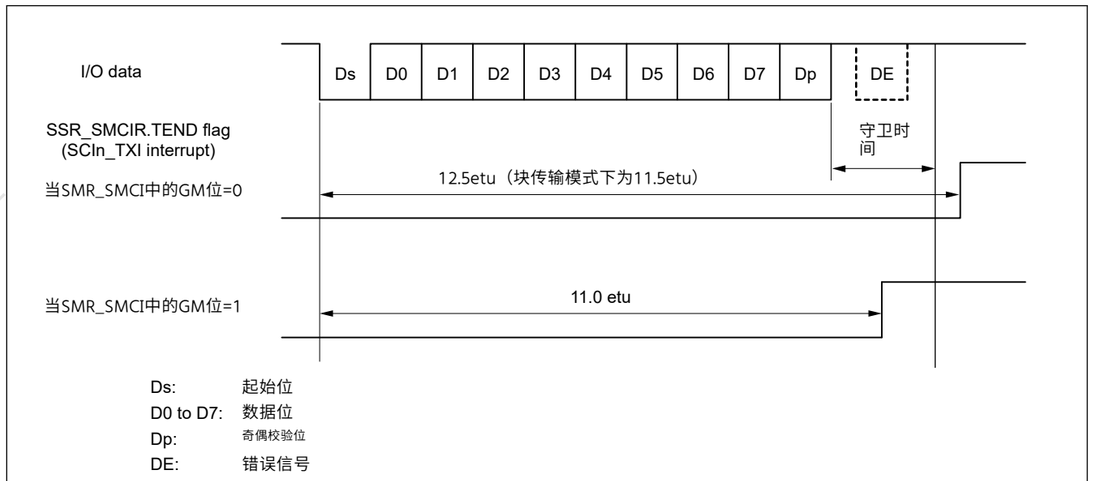

Figure 30.83 发送期间的SSR.TEND标志生成时序

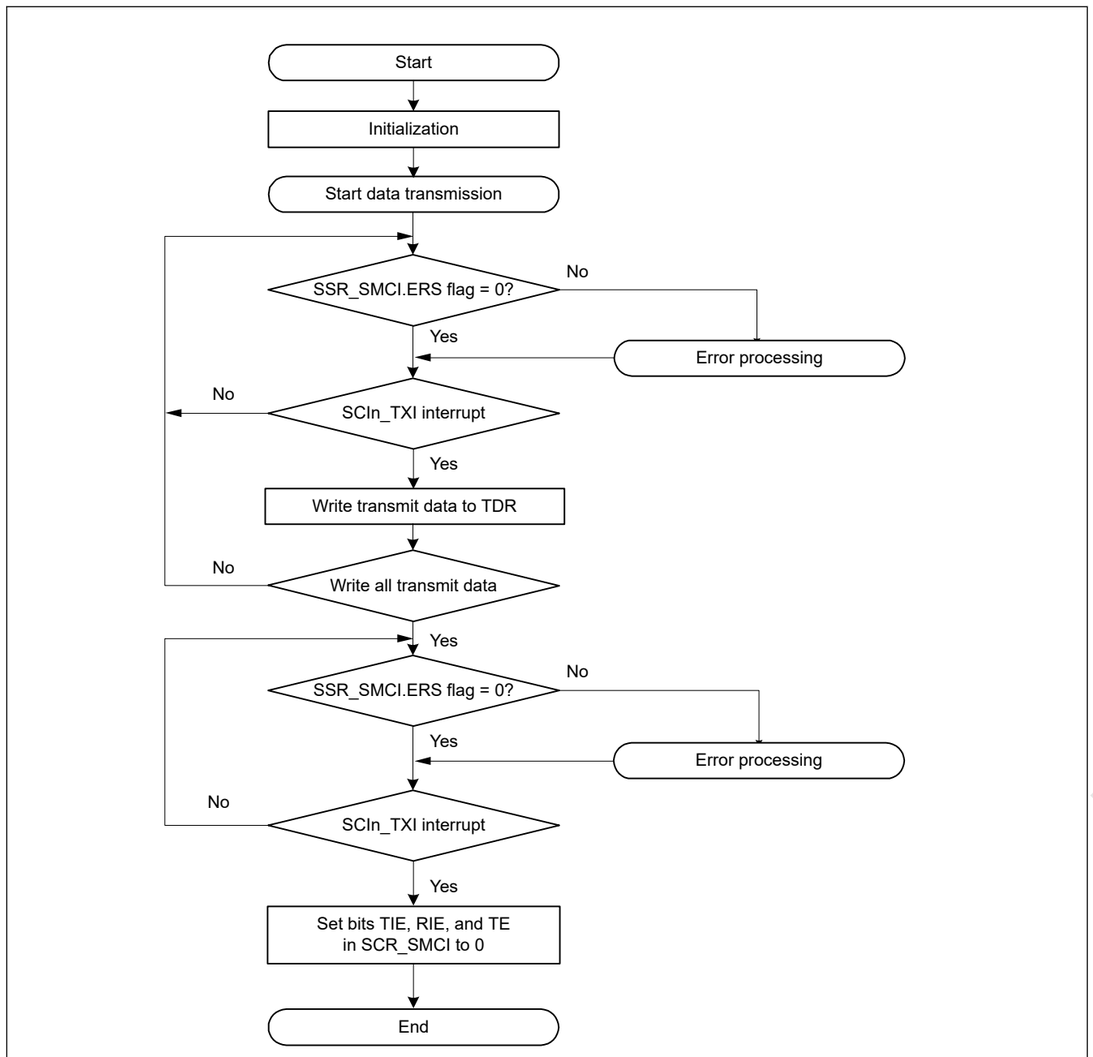

Figure 30.84 Example flow of smart card interface transmission

30.7.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 30.85 shows the data re-transfer operation in reception mode.

1. If a parity error is detected in the receive data, the SSR_SMCI.PER flag is set to 1. When the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
2. For a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
3. When no parity error is detected, the SCR_SMCI.PER flag is not set to 1.
4. In this case, data is determined to be received successfully. When the SCR_SMCI.RIE bit is 1, an SCIn_RXI interrupt request is generated.

Figure 30.86 shows an example flow of serial data reception. All the processing steps are automatically performed using an SCIn_RXI interrupt request to activate the DTC or DMAC.

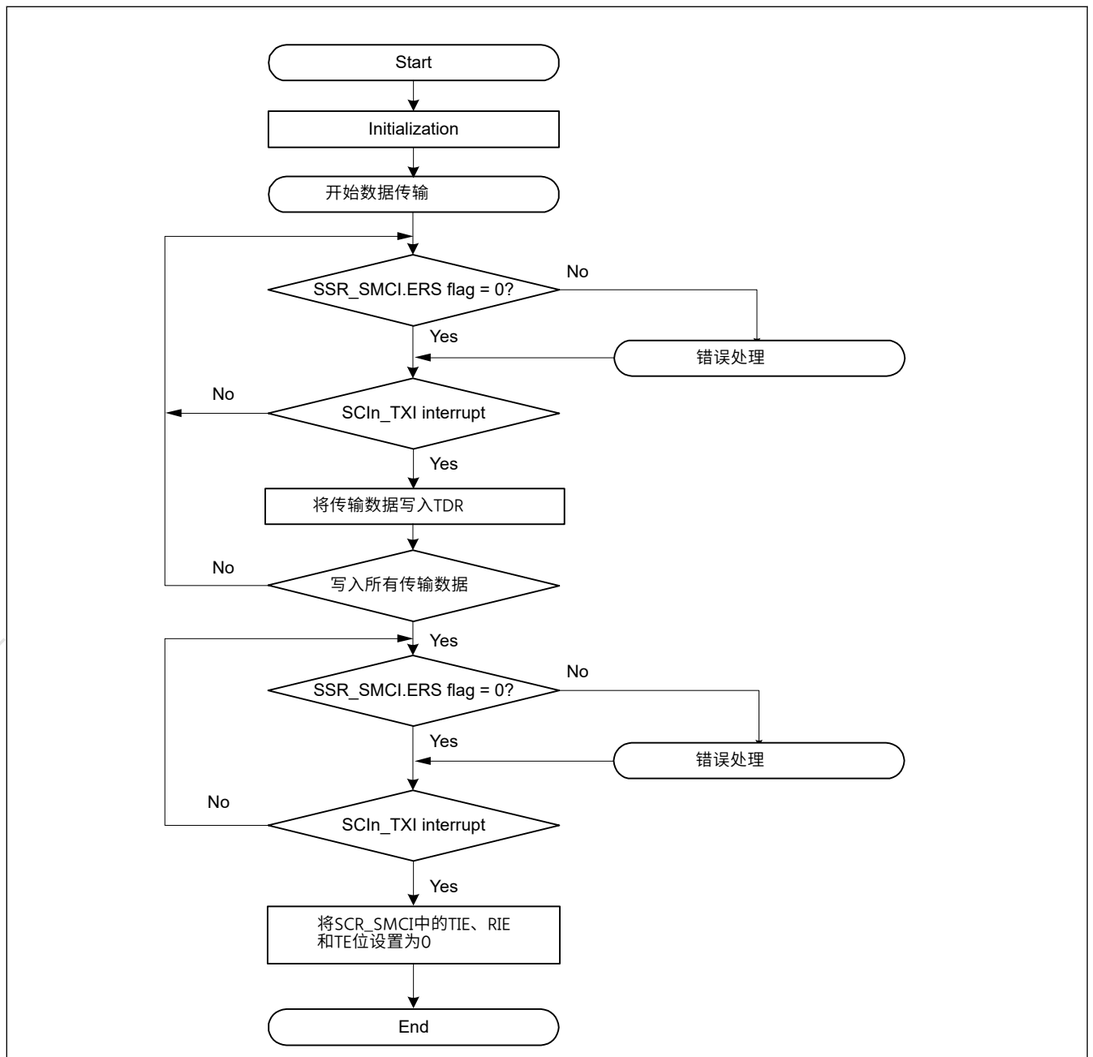

Figure 30.84 智能卡接口传输示例流程

30.7.7 串行数据接收（块传输模式除外）

智能卡接口模式下的串行数据接收与非智能卡接口模式下的串行数据接收类似。图30.85显示了接收模式下的数据重传操作。

1.如果在接收数据中检测到奇偶校验错误，则SSR_SMCI.PER标志设置为1。当SCR_SMCI.RIE位为1时，产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将PER标志清零。

2.对于检测到奇偶校验错误的帧，不产生SCIn_RXI中断。

3.未检测到奇偶校验错误时，SCR_SMCI.PER标志不设置为1。

4、在这种情况下，确定数据接收成功。当SCR_SMCI.RIE位为1时，产生SCIn_RXI中断请求。

图30.86显示了串行数据接收的示例流程。所有处理步骤都使用一个自动执行SCIn_RXI中断请求以激活DTC或DMAC。

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In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DTC or DMAC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC or DMAC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC or DMAC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, allowing the data to be read.

When a reception is forced to terminate by setting SCR_SMCI.RE to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 30.3.9. Serial Data Reception in Asynchronous Mode.

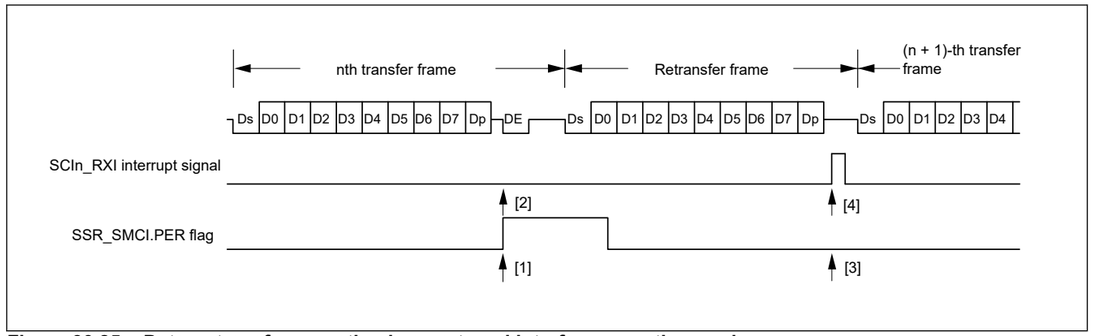

Figure 30.85 Data re-transfer operation in smart card interface reception mode

在接收时，将RIE位设置为1允许产生SCIn_RXI中断请求。如果先前将SCIn_RXI中断请求指定为DTC或DMAC激活源，则DTC或DMAC由SCIn_RXI中断请求激活，从而允许传输接收数据。

如果接收期间发生错误并且SSR_SMCI中的ORER或PER标志设置为1，则会生成接收错误中断(SCIn_ERI)请求。错误发生后清除错误标志。如果发生错误，则不会激活DTC或DMAC并跳过接收数据。因此，将传输DTC或DMAC中指定的接收数据字节数。

如果在接收过程中发生奇偶校验错误并且PER标志设置为1，则接收数据将传输到RDR，从而可以读取数据。

如果在操作期间通过将SCR_SMCI.RE设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的已接收数据可能留在RDR中。

Note: 关于块传输模式下的操作，请参见第30.3.9节。异步模式下的串行数据接收。

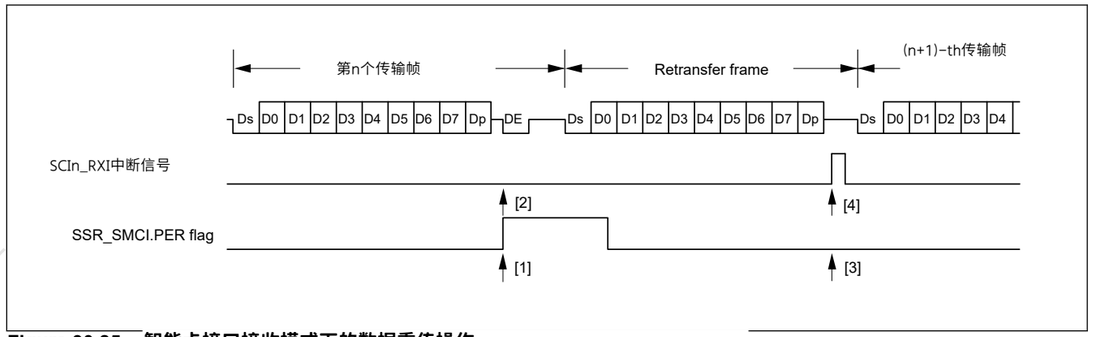

Figure 30.85 智能卡接口接收模式下的数据重传操作

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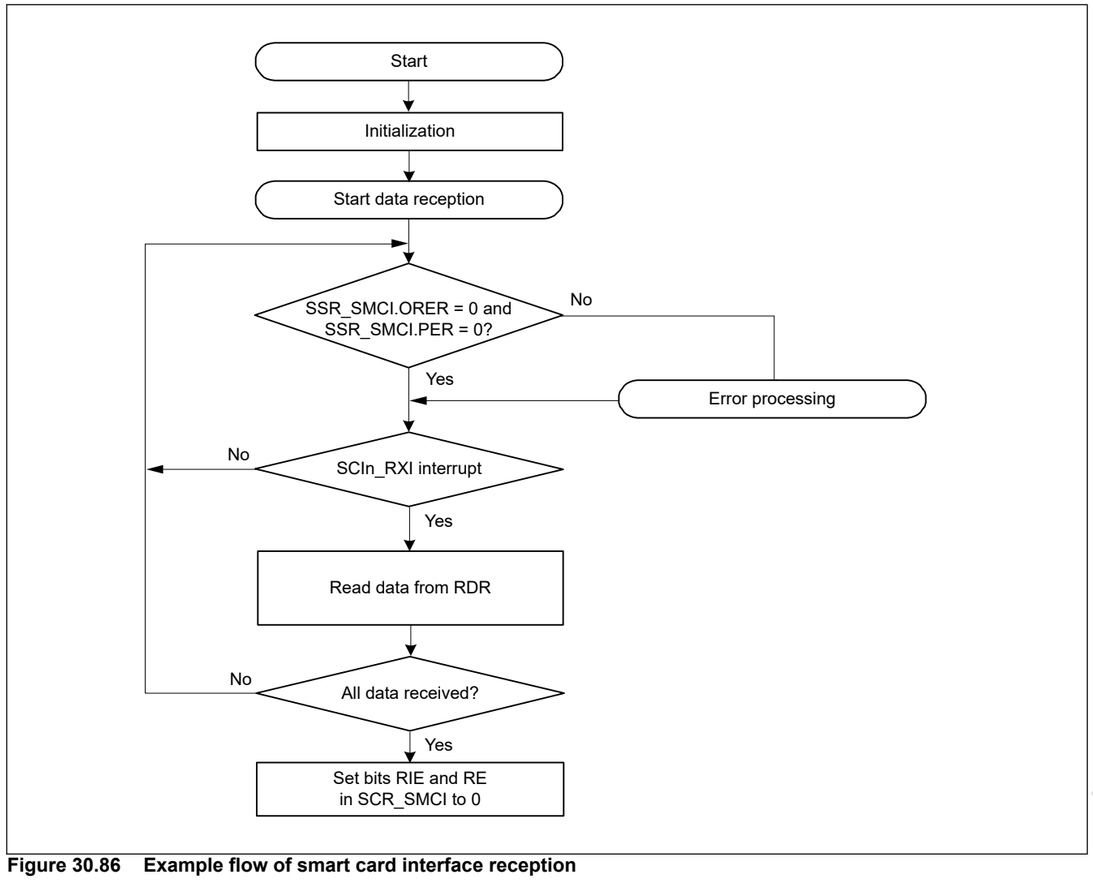


Figure 30.86 Example flow of smart card interface reception

30.7.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1:0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 30.2.12. SMR_SMCI : Serial Mode Register for Smart Card Interface Mode (SCMR.SMIF = 1). When setting the clock output, the base clock described in section 30.7.4. Receive Data Sampling Timing and Reception Margin is applied.

Figure 30.87 shows an example timing for the clock output control when the CKE[1] bit in SCR_SMCI is set to 0 and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected on the SCKn pin, so there is a possibility that pulses with an unintended width may be output from the SCKn pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

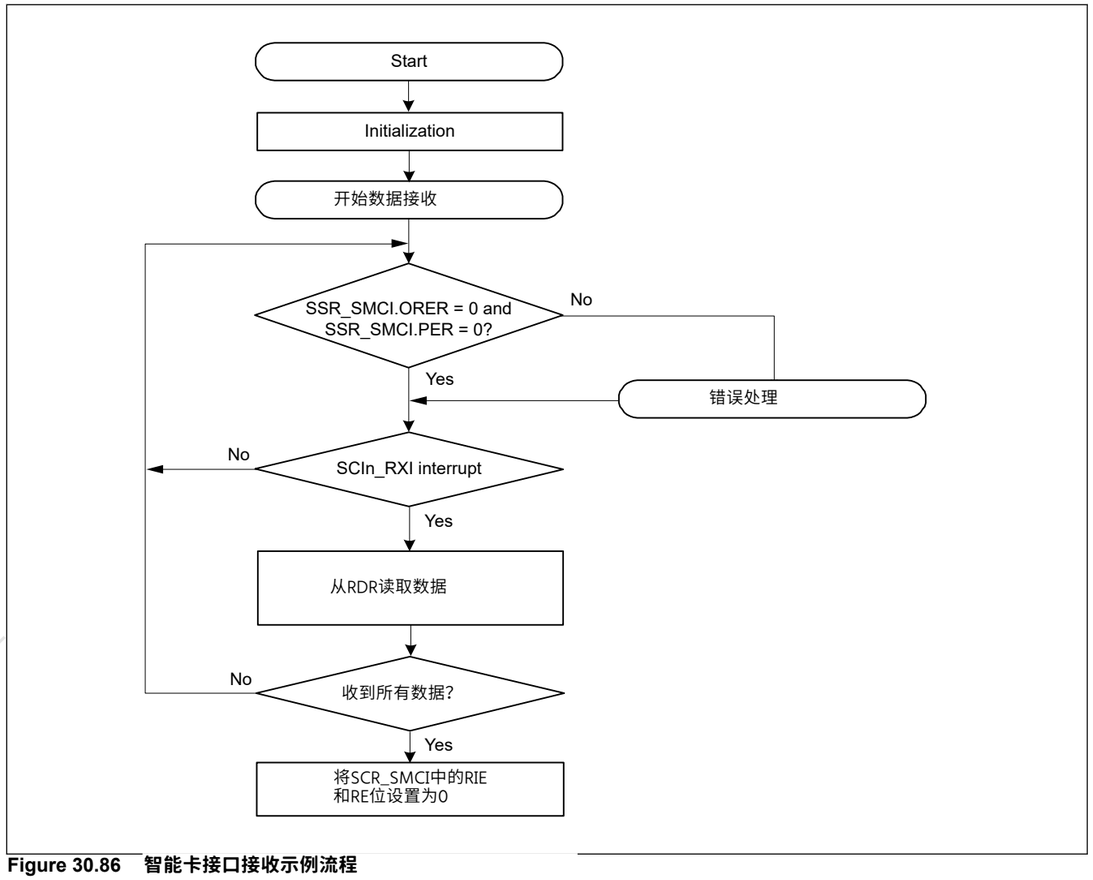


Figure 30.86 智能卡接口接收示例流程

30.7.8 时钟输出控制

当SMR_SMCI中的GM位设置为1时，时钟输出可以由SCR_SMCI中的CKE[1:0]位控制。有关CKE[1:0]位的详细信息，请参见第30.2.12节。SMR_SMCI：智能卡接口模式的串行模式寄存器(SCMR.SMIF=1)。设置时钟输出时，使用第30.7.4节中描述的基本时钟。应用接收数据采样时序和接收裕度。

图30.87显示了当SCR_SMCI中的CKE[1]位设置为0且控制SCR_SMCI中的CKE[0]位。

当SMR_SMCI中的GM位为0时，SCR_SMCI中CKE[0]位的输出控制立即反映在SCKn引脚，因此有可能会从SCKn引脚输出具有意外宽度的脉冲。

当SMR_SMCI中的GM位为1时，即使SCR_SMCI中的CKE[0]位发生变化，也会输出与基本时钟脉冲宽度相同的时钟。

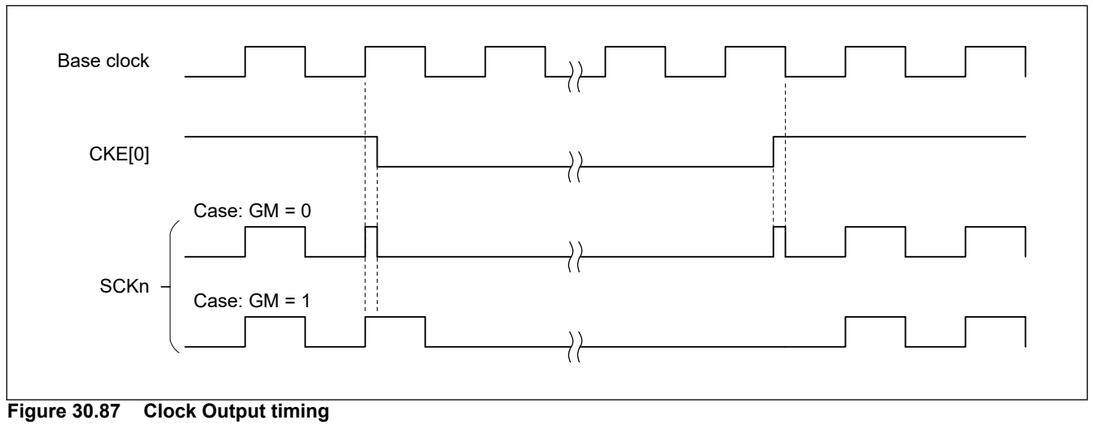


Figure 30.87 Clock Output timing

30.8 Operation in Simple IIC Mode

Simple IIC mode format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I^2C bus format and timing of the I^2C bus are shown in Figure 30.88 and Figure 30.89.

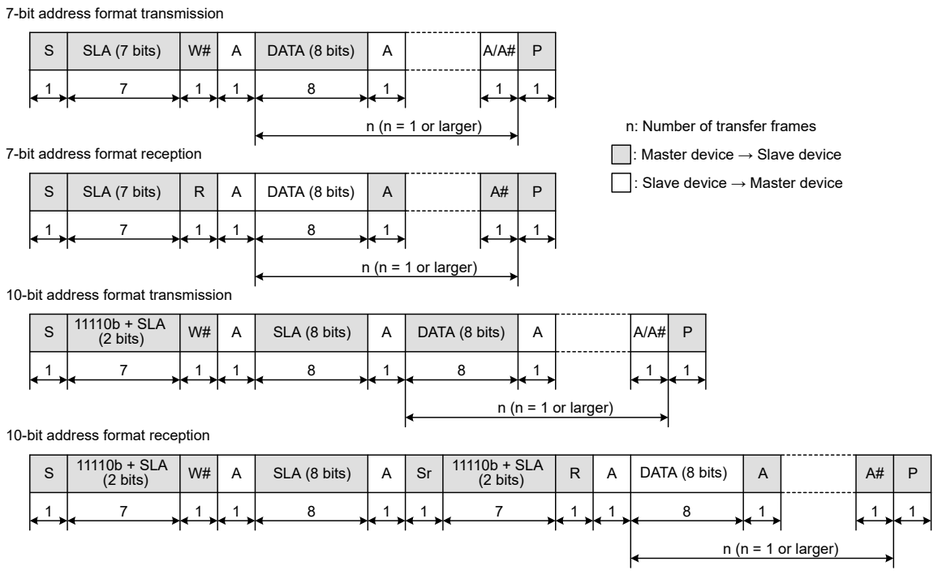


Figure 30.88 IIC bus format

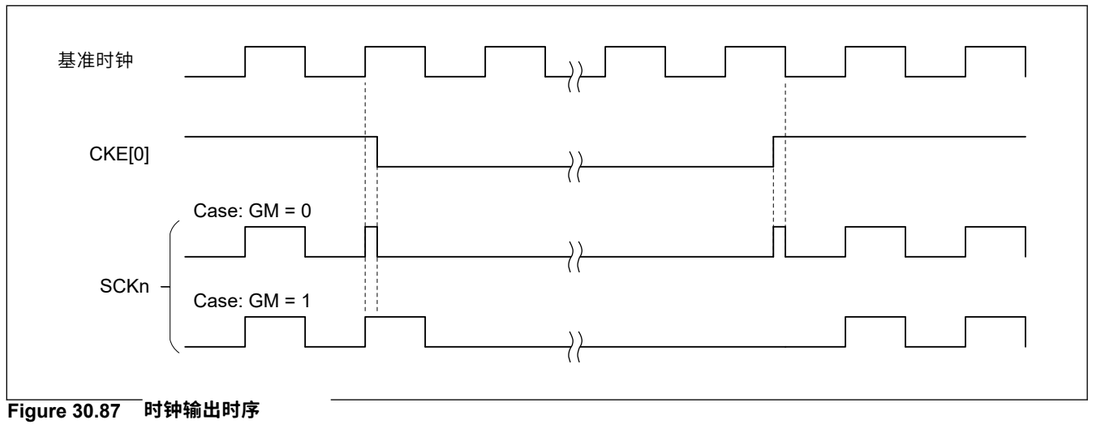


Figure 30.87 时钟输出时序

30.8 简单IIC模式下的操作

简单IIC模式格式由8个数据位和一个确认位组成。通过在启动条件或重新启动条件之后继续进入从地址帧，主设备可以指定从设备作为通信伙伴。当前指定的从设备保持有效，直到指定新的从设备或满足停止条件。所有帧中的8个数据位从MSB开始按顺序传输。

I2C总线格式和I2C总线时序如图30.88和图30.89所示。

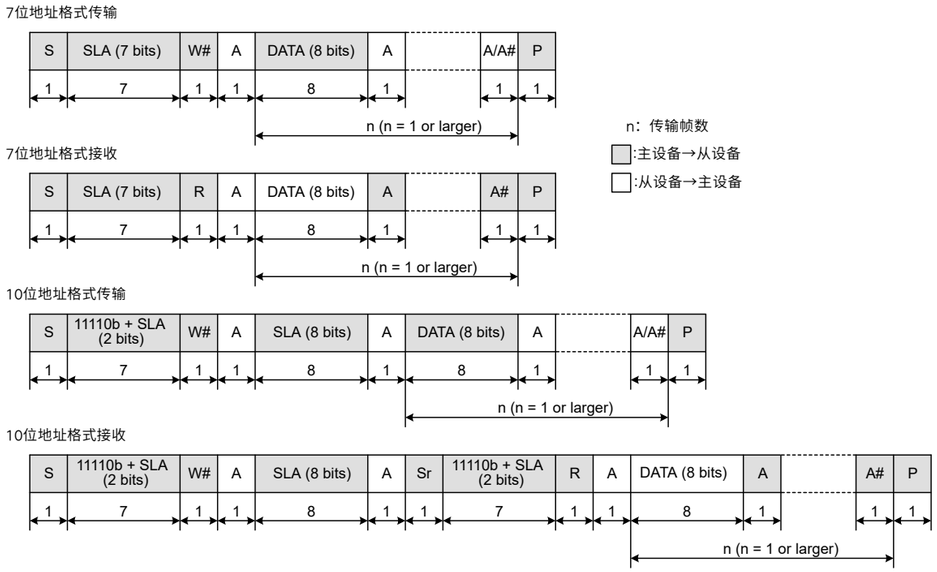


Figure 30.88 IIC总线格式

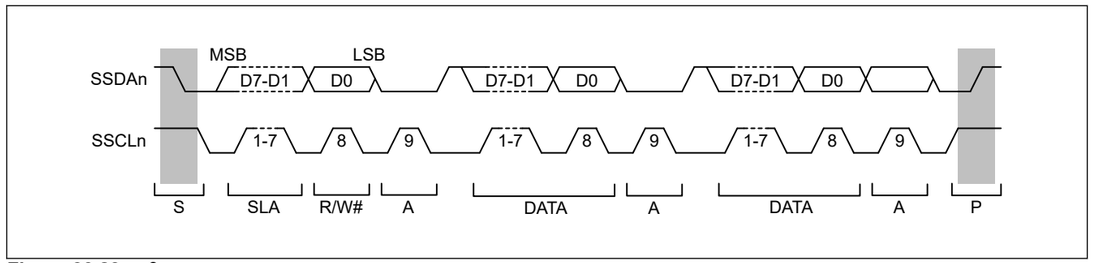


Figure 30.89 I^2C bus timing when SLA is 7 bits

- S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high
- SLA: Indicates a slave address, by which the master device selects a slave device
- R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.
- A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.
- Sr: Indicates a restart condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses
- DATA: Indicates the data being received or transmitted
- P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high while the SCLn line is high

30.8.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the SIMR3.IICSTAREQ bit causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the IICSTAREQ bit in SIMR3 is set to 0, and a start-condition generated interrupt is output

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from the high level to the low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the SIMR3.IICRSTAREQ bit is set to 0, and a restart-condition generated interrupt is output

Writing 1 to the SIMR3.IICSTPREQ bit causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)

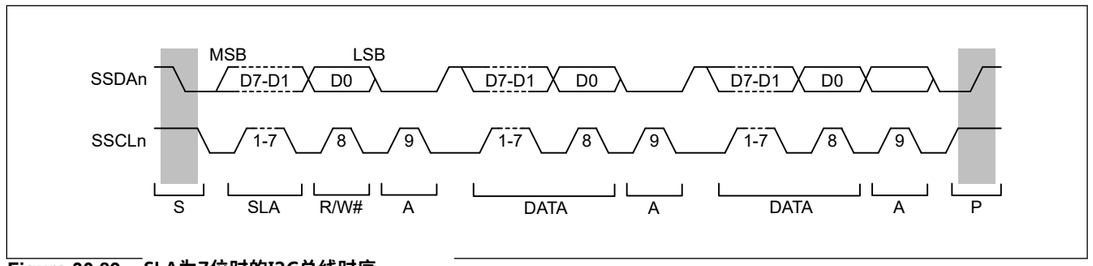


Figure 30.89 SLA为7位时的I2C总线时序

●S：表示启动条件，当主设备在SCLn线为高时将SDAn线上的电平从高电平变为低电平

●SLA：表示从地址，主设备通过该地址选择从设备

●RW#：指示传输方向（接收或传输）。值1表示从从设备传输到主设备，0表示从主设备传输到从设备。

●AA#：表示确认位。这由从设备返回用于主传输，并由主设备返回用于主接收。返回低电平表示ACK，返回高电平表示NACK。

●Sr：表示重启条件，当主设备将SDAn线上的电平从高电平变为低电平，而SCLn线为高电平且经过设置时间后

●DATA：表示正在接收或发送的数据

●P：表示停止条件，当主设备将SDAn线上的电平从低电平变为高电平而SCLn线为高电平时

30.8.1 启动、重启和停止条件的生成

将1写入SIMR3.IICSTAREQ位会导致产生启动条件。开始条件的生成通过以下操作进行：

●SDAn线上的电平下降（从高电平到低电平），SCLn线保持在释放状态

●开始条件的保持时间设置为比特周期的一半，比特率由BRR设置确定

●SCLn线上的电平下降（从高电平到低电平），SIMR3中的IICSTAREQ位设置为0，并输出一个起始条件产生的中断

将1写入SIMR3中的IICRSTAREQ位会导致产生重启条件。重新启动条件的生成通过以下操作进行：

●SDAn线释放，SCLn线保持低电平

●SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定

●SCLn线被释放（由低电平转变为高电平）

●当在SCLn线上检测到高电平时，重新启动条件的建立时间设置为BRR设置确定的比特率的半个比特周期

●SDAn线上的电平下降（从高电平到低电平）

●重启条件的保持时间设置为比特周期的一半，比特率由BRR设置确定

●SCLn线上的电平下降（从高电平变为低电平），SIMR3.IICRSTAREQ位设置为0，并输出重启条件产生的中断

将1写入SIMR3.IICSTPREQ位会导致产生停止条件。停止条件的生成通过以下操作进行：

●SDAn线上的电平下降（从高电平到低电平），SCLn线保持在低电平

●SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定

●SCLn线被释放（由低电平转变为高电平）

- When a high level is detected on the SCLn line, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn line is released (transition from the low to the high level), the SIMR3.IICSTPREQ bit is set to 0, and a stop-condition generated interrupt is output

Figure 30.90 shows the timing of operations in the generation of start, restart, and stop conditions.

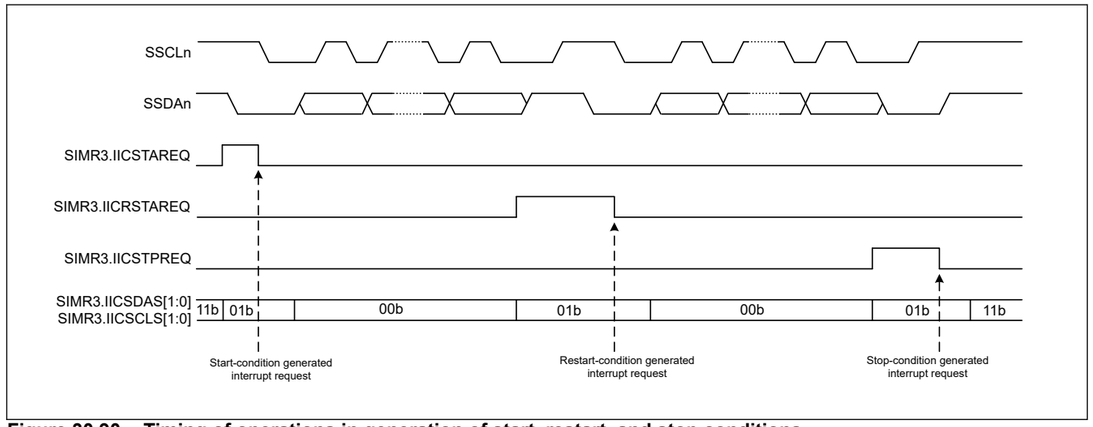


Figure 30.90 Timing of operations in generation of start, restart, and stop conditions

30.8.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the SIMR2.IICCSC bit to 1 applies control to obtain synchronization when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the SIMR2.IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is being input on the SCLn pin. Counting to determine the period at a high level starts after the transition of the input on the SCLn pin to the high level.

The interval from this time until counting to determine the period at high level starts on the transition of the SCLn pin to the high level, is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLK). The period at high level of the internal SCLn clock is extended even when other devices do not place the low level on the SCLn line.

If the SIMR2.IICCSC bit is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the SIMR2.IICCSC bit is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed.

Figure 30.91 shows an example operation for synchronizing the clocks.

●当在SCLn线上检测到高电平时，停止条件的建立时间设置为比特周期的一半，比特率由BRR设置确定

●SDAn线被释放（从低电平转换为高电平），SIMR3.IICSTPREQ位设置为0，并输出停止条件生成中断

图30.90显示了生成启动、重新启动和停止条件的操作时序。

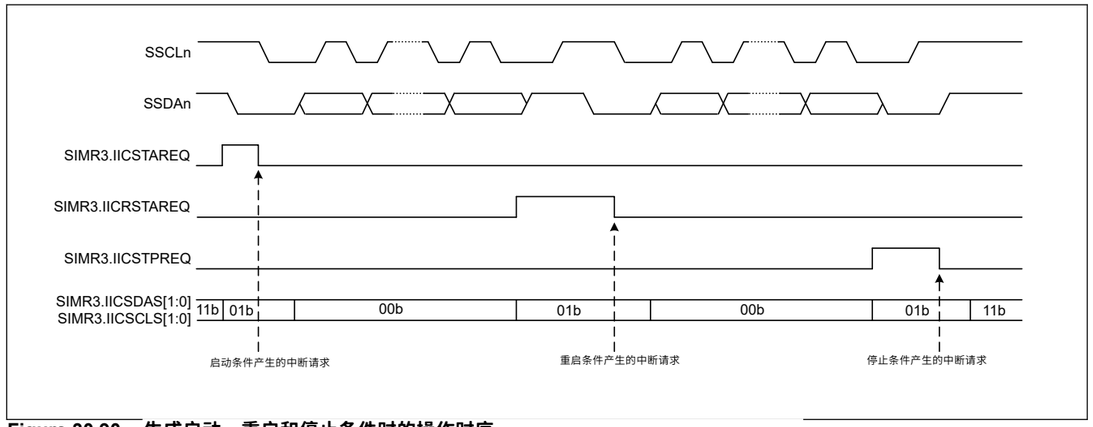


Figure 30.90 生成启动、重启和停止条件时的操作时序

30.8.2 时钟同步

如果从设备在传输的另一侧插入等待，则可以将SCLn线驱动为低电平。设置
当内部电平之间出现差异时，SIMR2.IICCSC位为1应用控制以获得同步
SCLn时钟信号和输入到SCLn引脚的电平。

当SIMR2.IICCSC位设置为1时，内部SCLn时钟信号的电平由低变为高。当SCLn引脚输入低电平时，停止计数以确定高电平周期。在SCLn引脚上的输入转换为高电平后，开始计数以确定高电平的周期。

从这个时间到从SCLn引脚转变为高电平开始计数确定高电平周期的时间间隔是SCLn输出延迟的总和，SCLn引脚上输入的噪声过滤延迟（2或3个周期的采样时钟用于噪声滤波器），以及延迟用于内部处理（1或2个PCLK周期）。即使其他设备没有将低电平置于SCLn线上，内部SCLn时钟的高电平周期也会延长。

如果SIMR2.IICCSC位为1，则通过取逻辑数据的发送和接收来获得同步
SCLn引脚上的输入与内部SCLn时钟的与。如果SIMR2.IICCSC位为0，则与内部SCLn时钟同步以进行数据的发送和接收。

如果从设备在发出启动、重启或停止条件的生成请求后，在内部SCLn时钟信号从低电平转变为高电平之前的间隔中插入一个等待周期，则直到生成的时间为延长了那个时期。

如果从设备在内部SCLn时钟信号从低电平转变为高电平之后插入等待周期，尽管在不停止等待周期的情况下发出生成完成中断，但不能保证条件本身的生成。

图30.91显示了同步时钟的示例操作。

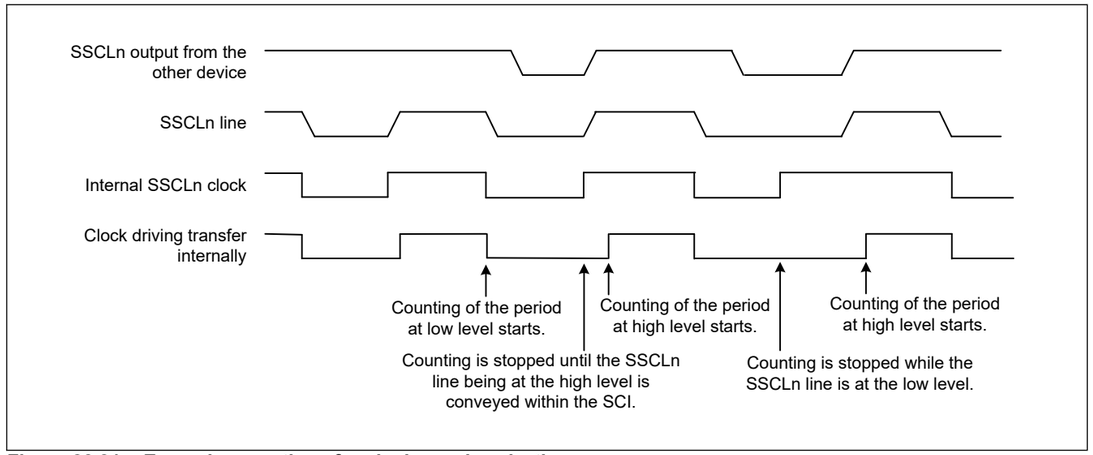


Figure 30.91 Example operations for clock synchronization

30.8.3 SDAn Output Delay

The SIMR1.IICDL[4:0] bits can be used to set a delay for output on the SDAn pin relative to falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLK, by the divisor selected in the SMR.CKS[1:0] bits). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and acknowledge bit.

If the SDAn output delay is shorter than the time for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SDAn pin specify times greater than the time output on the SCLn pin takes to fall (300 ns for IIC in normal mode and fast mode).

Figure 30.92 shows the timing of delays in SDAn output.

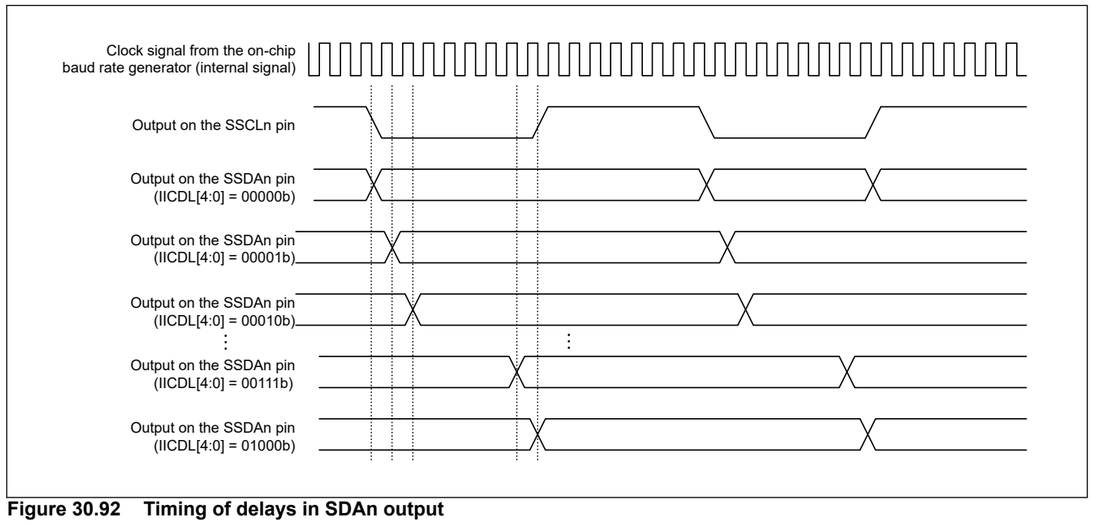


Figure 30.92 Timing of delays in SDAn output

30.8.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value 0x00 to SCR and initialize the interface following the example shown in Table 30.40.

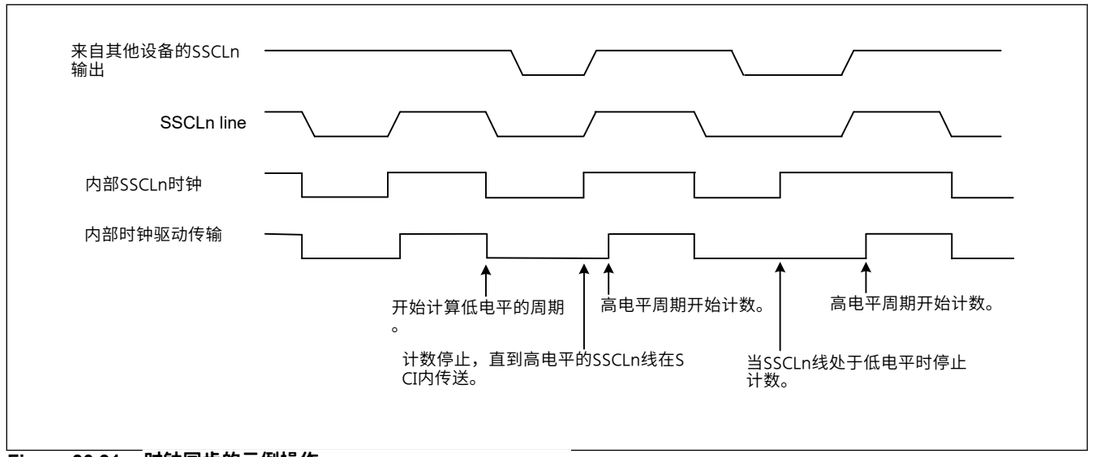


Figure 30.91 时钟同步的示例操作

30.8.3 SDAn输出延迟

SIMR1.IICDL[4:0]位可用于设置SDAn引脚输出相对于输出下降沿的延迟。
SCLn引脚。从0到31的延迟设置是可选的，表示来自片上波特率发生器的时钟信号的相应周期数的周期（通过在SMR.CKS中选择的除数对基本时钟PCLK进行分频得出[1:0]位）。SDAn引脚上的输出延迟适用于启动条件重启条件停止条件信号、8位发送数据和确认位。

如果SDAn输出延迟小于SCLn引脚电平下降的时间，则SDAn引脚上的输出变化会在SCLn引脚上的输出电平下降时开始，从而产生从设备错误操作的可能性.确保SDAn引脚上的输出延迟设置指定的时间大于SCLn引脚上输出的下降时间（IIC在正常模式和快速模式下为300ns）。

图30.92显示了SDAn输出中的延迟时序。

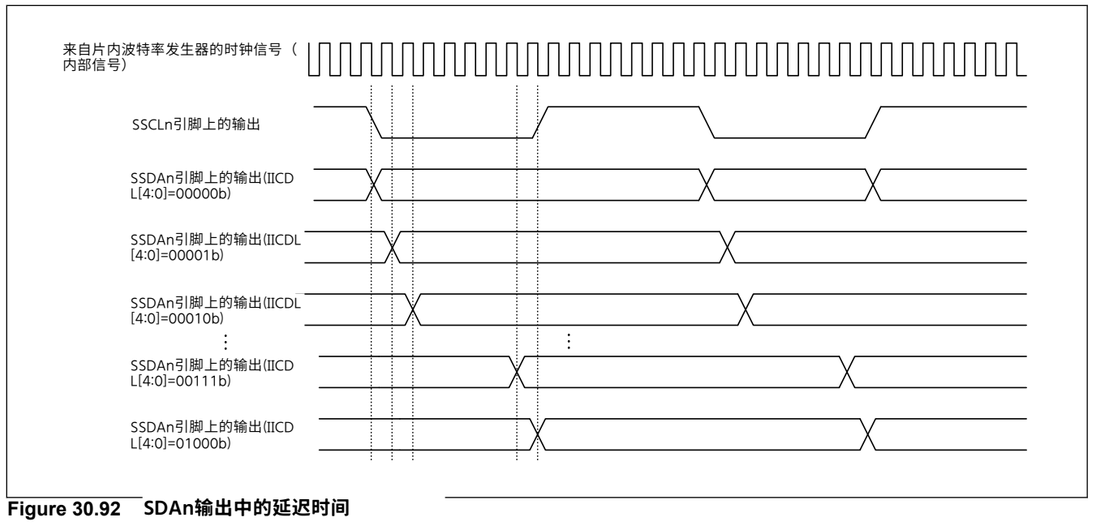


Figure 30.92 SDAn输出中的延迟时间

30.8.4 简单IIC模式下的SCI初始化

在传输数据之前，将初始值0x00写入SCR并按照中所示的示例初始化接口
Table 30.40.

Before making any changes to the operating mode or transfer format, be sure to set SCR to its initial value. In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

Table 30.40 Example flow of SCI initialization in simple IIC mode

No.	Step Name	Description
1	Start of initialization	
2	Set the TIE, RIE, TE, RE, TEIE and CKE[1:0] bits in SCR to 0	
3	Set the I/O port functions	Set the I/O port to allow use (on N-channel open-drain output pins) of the SSCLn and SSDAn pin functions.
4	Set the IICSDAS[1:0] and IICSCLS[1:0] bits in SIMR3 to 11b	Place the SSCLn and SSDAn pins in the high-impedance state until a start condition is to be generated.
5	Set up the transfer or reception format in SMR and SCMR	Set the format for transmission and reception in SMR and SCMR. In SMR, set the CKS[1:0] bits to the target value and set the other bits to 0. In SCMR, set the SDIR bit to 1 and the SINV and SMIF bits to 0.
6	Set the initial value to SPTR.	Set the Initial value to SPTR.
7	Set the value in BRR	Write the value for the targeted bit rate to BRR.
8	Set a value in MDDR	Write the value obtained by correcting a bit rate error in MDDR. This step is not required if the BRME bit in SEMR is set to 0.
9	Set the values in SEMR, SNFR, SIMR1, SIMR2, and SPMR	Set the values in SEMR, SNFR, SIMR1, SIMR2, and SPMR. Set the NFEN and BRME bits in SEMR. In SNFR, set the NFCS[2:0] bits. In SIMR1, set the IICM bit to 1 and the IICDL[4:0] bits as required. In SIMR2, set the IICACKT and IICCSC bits to 1 and the IICINTM bits as required. In SPMR, set all the bits to 0.
10	Set the SCR.RE and TE bit to 1 and set the SCR.TIE, RIE and TEIE bits	Set the RE and TE bits in the SCR to 1. Then, set the SCR.TIE, RIE, and TEIE bits (for transmission and when the SIMR2.IICINTM bit is 1, set the RIE bit to 0). Setting the TE and RE bits to 1 enables the SSCLn and SSDAn pin functions.
11	Start of transmission or reception	

30.8.5 Operation in Master Transmission in Simple IIC Mode

Figure 30.93 and Figure 30.94 show examples of master transmission and Figure 30.95 shows an example flow of data transmission.

Figure 30.93 shows the operation example when SIMR2.IICINTM bit is 1 (use reception and transmission interrupts) and the value of the SCR.RIE bit is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled).

See Table 30.45 for more information on the STI interrupt.

Figure 30.95 shows a flow chart in the case of SIMR2.IICINTM is 1 and address transmission by CPU and data transmission by DTC or DMAC. When 10-bit slave addresses are in use, steps [3] and [4] are repeated twice.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.

在对操作模式或传输格式进行任何更改之前，请务必将SCR设置为其初始值。在简单IIC模式下，通信端口的开漏设置应在端口侧进行。

Table 30.40 简单IIC模式下SCI初始化示例流程

No.	步骤名称	Description
1	初始化开始	
2	将SCR中的TIE、RIE、TE、RE、TEIE和CKE[1:0]位设置为0	
3	设置IO端口功能	设置IO端口以允许使用（在N通道开漏输出引脚上）SSCLn和SSDAn引脚功能。
4	设置IICSDAS[1:0]和SIMR3至11b中的IICSCLS[1:0]位	将SSCLn和SSDAn引脚置于高阻抗状态，直到产生启动条件。
5	在SMR和SCMR中设置传输或接收格式	在SMR和SCMR中设置发送和接收的格式。在SMR中，将CKS[1:0]位设置为目标值，并将其他位设置为0。 在SCMR中，将SDIR位设置为1，将SINV和SMIF位设置为0。
6	将初始值设置为SPTR。	将初始值设置为SPTR。
7	设置BRR中的值	将目标比特率的值写入BRR。
8	在MDDR中设置一个值	在MDDR中写入通过纠正比特率错误获得的值。此步骤不是必需的，如果SEMR中的BRME位设置为0。
9	设置SEMR中的值，SNFR, SIMR1, SIMR2, and SPMR	设置SEMR、SNFR、SIMR1、SIMR2和SPMR中的值。 设置SEMR中的NFEN和BRME位。在SNFR中，设置NFCS[2:0]位。 在SIMR1中，根据需要将IICM位和IICDL[4:0]位设置为1。 在SIMR2中，根据需要将IICACKT和IICCSC位设置为1，并将IICINTM位设置为。 在SPMR中，将所有位设置为0。
10	将SCR.RE和TE位设置为1，并设置SCR.TIE、RIE和TEIE位	将SCR中的RE和TE位设置为1。然后，设置SCR.TIE、RIE和TEIE位（用于传输且当SIMR2.IICINTM位为1时，将RIE位设置为0）。将TE和RE位设置为1启用SSCLn和SSDAn引脚功能。
11	开始发送或接收	

30.8.5 简单IIC模式下的主传输操作

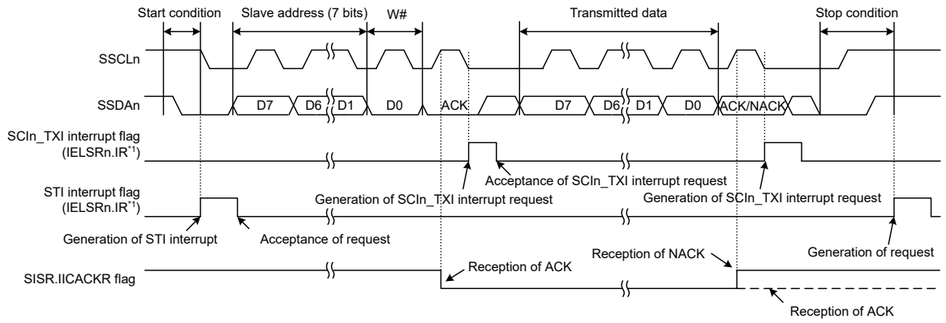
图30.93和图30.94显示了主传输的示例，图30.95显示了数据传输的示例流程。

图30.93显示了SIMR2.IICINTM位为1（使用接收和发送中断）且SCR.RIE位的值假定为0（SCIn_RXI和SCIn_ERI中断请求被禁用）时的操作示例。

有关STI中断的更多信息，请参见表30.45。

图30.95显示了SIMR2.IICINTM为1，CPU传输地址，DTC或DMAC传输数据时的流程图。当使用10位从地址时，步骤[3]和[4]重复两次。

在简单IIC模式下，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同，当一帧的通信完成时产生发送数据空中断（SCIn_TXI）。



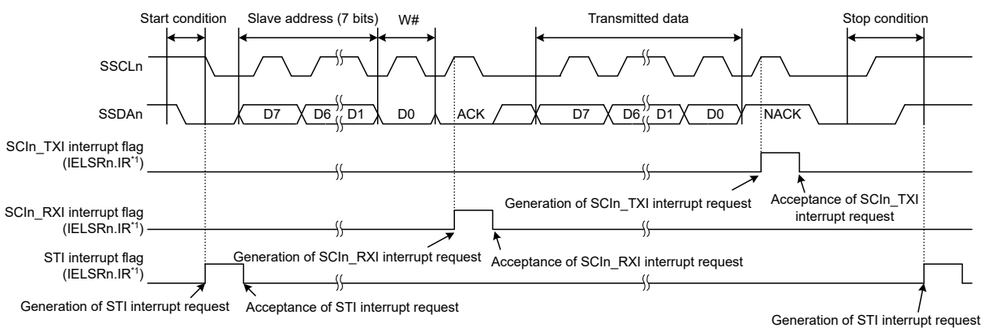
Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.93 Example 1 of operations for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the SIMR2.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC or DMAC is activated by the ACK interrupt as the trigger and required number of data bytes are transmitted. When the NACK is received, error processing such as transmission stop and retransmission is performed using the NACK interrupt as the trigger.

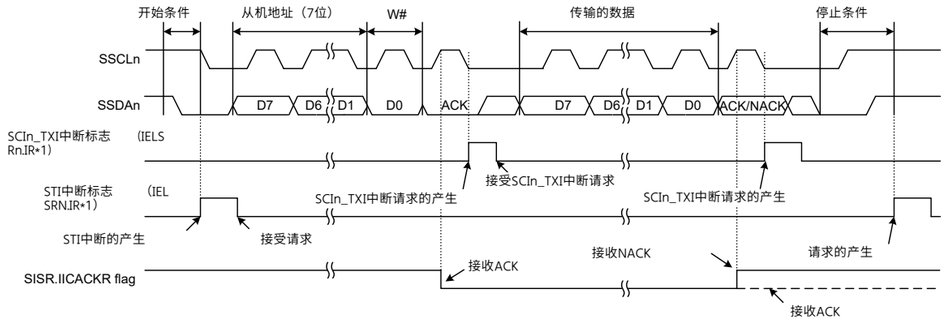
To restart communication for some reason after writing data in the TDR register, use the following procedure:

1. Set the TE and RE bits in the SCR register to 0 to stop communication.
2. Set 0xF0 in the SIMR3 register, release the IIC bus, and clear the generation of a condition.
3. If the RDRF flag in the SSR register is set to 1, clear it.
4. Set the TE and RE bits in the SCR register to 1 and start the next communication.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.94 Example 2 of operations for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.93 简单IIC模式下主机发送操作示例1，具有7位从机地址、发送中断和接收中断

当在主机传输期间SIMR2.IICINTM位设置为0（使用ACKNACK中断）时，DTC或DMAC由ACK中断作为触发器激活并传输所需的数据字节数。接收到NACK时，以NACK中断为触发进行发送停止、重发等错误处理。

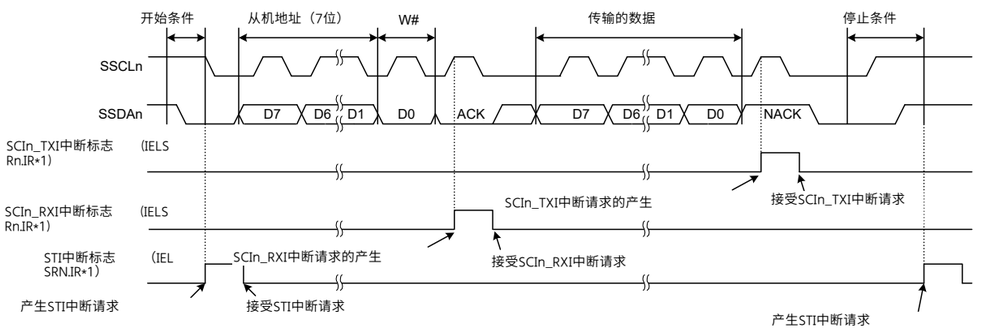
要在将数据写入TDR寄存器后出于某种原因重新启动通信，请使用以下过程：

1.将SCR寄存器中的TE和RE位设置为0以停止通信。

2.将SIMR3寄存器中的0xF0置位，释放IIC总线，并清除条件的产生。

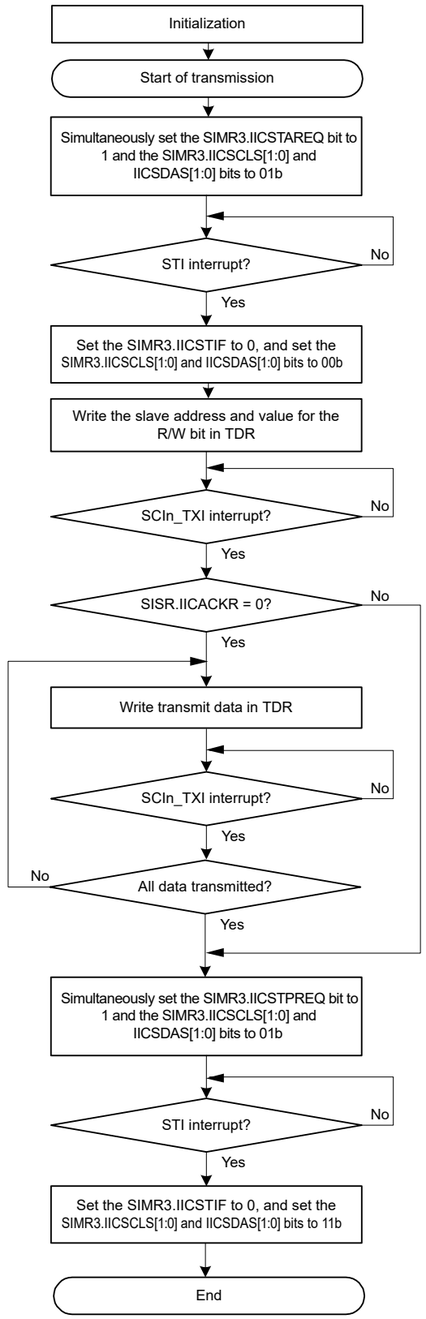
3.如果SSR寄存器中的RDRF标志设置为1，则清除它。

4.将SCR寄存器中的TE和RE位设置为1，开始下一次通信。



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.94 使用7位从机地址、ACK中断和NACK中断的简单IIC模式下主机传输操作示例2



[1] [1] Initialization in simple IIC mode:
For transmission, set the SCR.RIE to 0 to disable the SCIn_RXI and ERI interrupts.

[2] [2] Generate a start condition.

[3] Writing to TDR:
Write the slave address and value for the R/W bit to TDR.

[3] [4] Confirming ACK response from the slave device:
Check the SISR.IICACKR bit. If SISR.IICACKR is 0, it indicates that the slave device responded with ACK and operations proceed. If SISR.IICACKR is 1, it indicates that there was no response from the slave device so the next transition is to generate a stop condition.

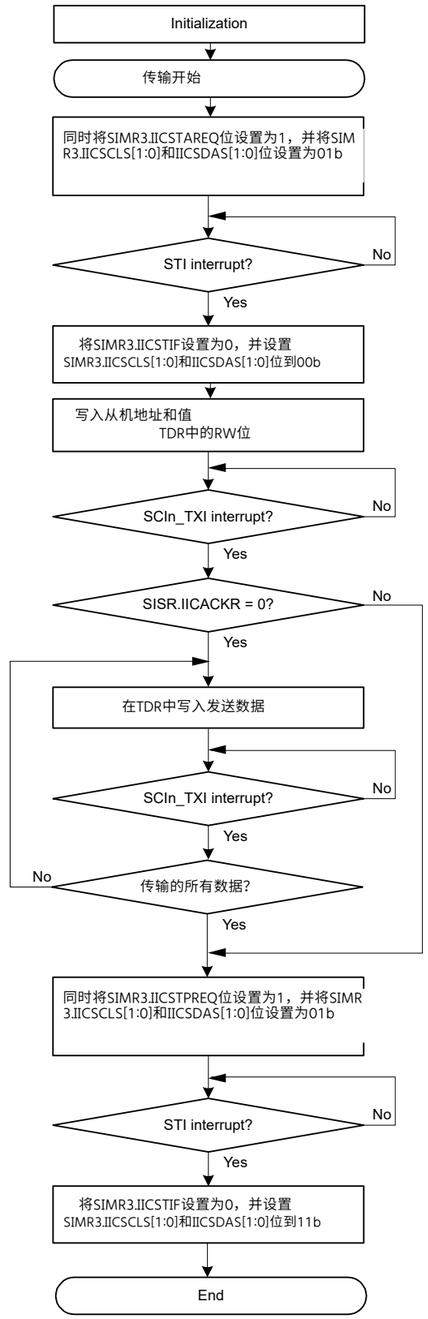
[4] If 10-bit slave addresses are in use, processing of [3] and [4] is repeated twice.

[5] [5] Continuing with serial transmission:
When transmission is to continue, write additional transmit data to TDR. Except for the first data to be transmitted, a SCIn_TXI interrupt request can activate the DMAC or DTC to handle writing of data to TDR. But it cannot be confirmed status of ACK or NACK.

[6] [6] Generate a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt is generated when communication completes.

Figure 30.95 Example flow of master transmission in simple IIC mode with transmission interrupts and reception interrupts



[1] [1]简单IIC模式下的初始化：对于传输，将SCR.RIE设置为0以禁用
SCIn_RXI和ERI中断。

[2] [2]生成开始条件。

[3]写入TDR：将RW位的从机地址和值写入TDR。

[3] [4]确认来自从设备的ACK响应：检查SISR.IICACKR位。如果SISR.IICACKR为0，则表明从设备响应ACK并继续操作。如果SISR.IICACKR为1，则表明从设备没有响应，因此下一个转换是生成停止条件。

[4] 如果使用10位从地址，则[3]和[4]的处理重复两次。

[5] [5]继续串行传输：当要继续传输时，将额外的传输数据写入TDR。除了要传输的第一个数据外，SCIn_TXI中断请求可以激活DMAC或DTC来处理向TDR写入数据。但不能确认ACK或NACK的状态。

[6] [6]生成停止条件。

Note: 在简单IIC模式下，SCIn_TXI中断在通信完成时产生。

Figure 30.95 带有发送中断和接收中断的简单IIC模式下的主机发送示例流程

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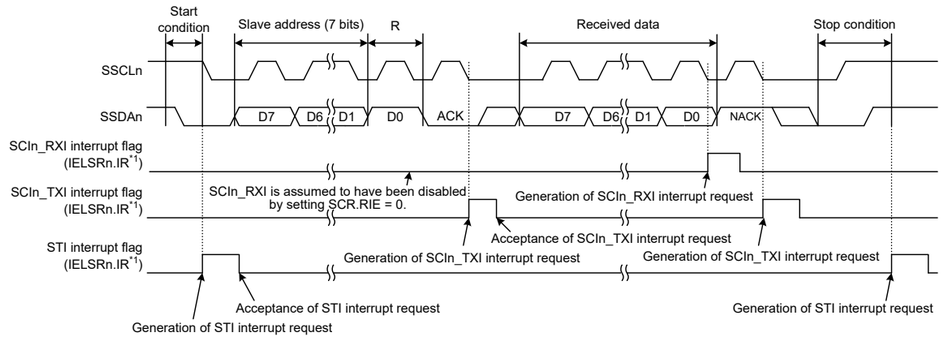
30.8.6 Master Reception in Simple IIC Mode

Figure 30.96 shows an example operation in simple IIC mode master reception and Figure 30.97 shows an example flow of master reception.

The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts).

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

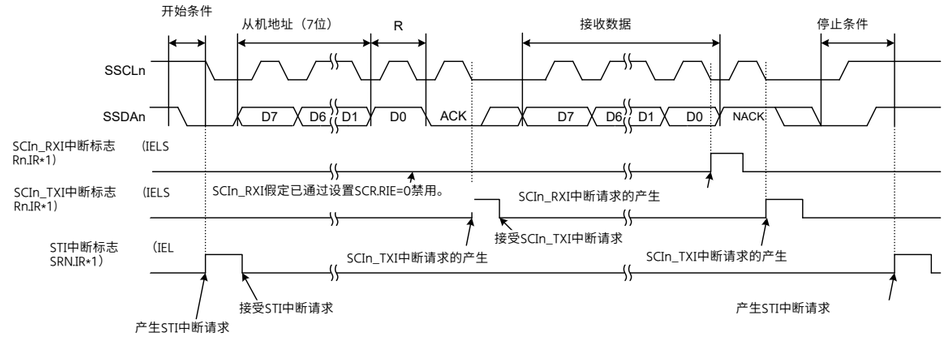
Figure 30.96 Example operations for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

30.8.6 简单IIC模式下的主接收

图30.96显示了简单IIC模式主机接收的示例操作，图30.97显示了主机接收的示例流程。

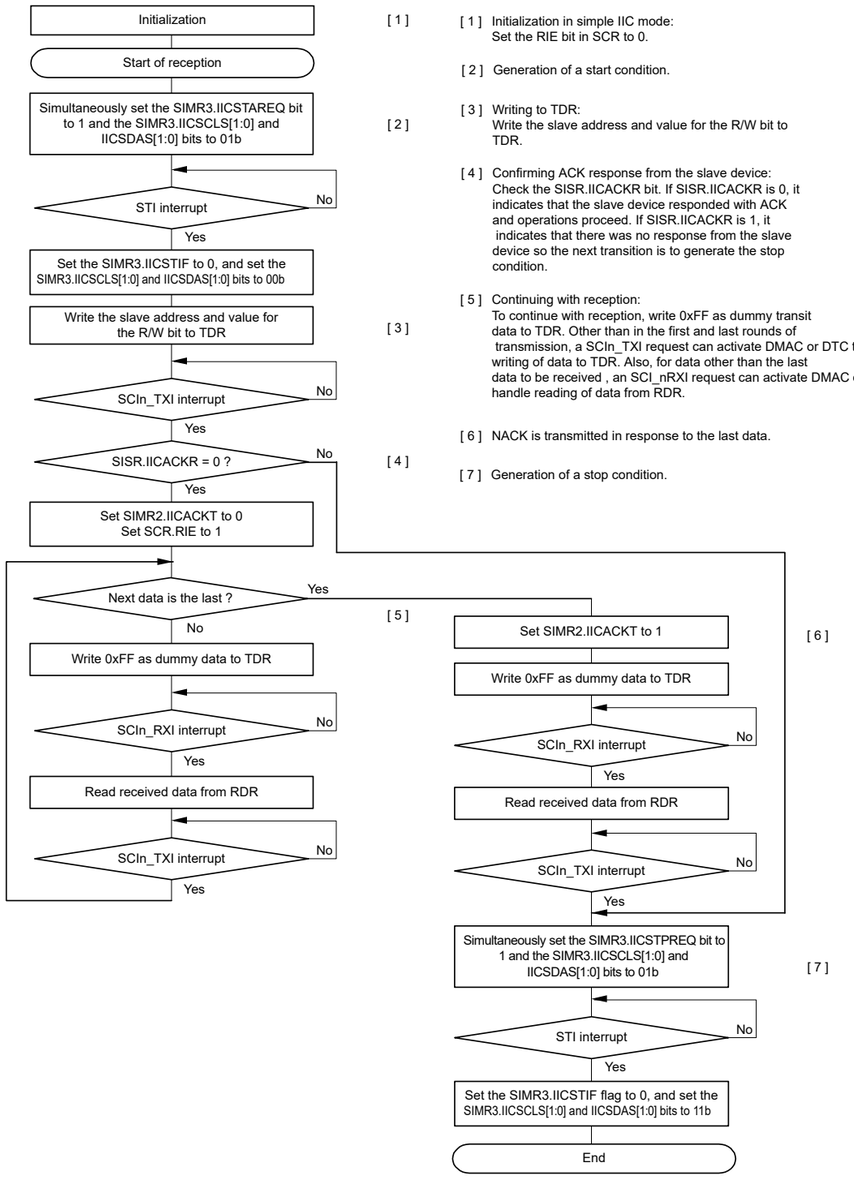
SIMR2.IICINTM位的值假定为1（使用接收和发送中断）。

在简单IIC模式下，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同，当一帧的通信完成时产生发送数据空中断（SCIn_TXI）。



注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

Figure 30.96 使用7位从地址、发送中断和接收中断的简单IIC模式下的主机接收示例操作



[1] Initialization in simple IIC mode:
Set the RIE bit in SCR to 0.

[2] Generation of a start condition.

[3] Writing to TDR:
Write the slave address and value for the R/W bit to TDR.

[4] Confirming ACK response from the slave device:
Check the SISR.IICACKR bit. If SISR.IICACKR is 0, it indicates that the slave device responded with ACK and operations proceed. If SISR.IICACKR is 1, it indicates that there was no response from the slave device so the next transition is to generate the stop condition.

[5] Continuing with reception:
To continue with reception, write 0xFF as dummy transit data to TDR. Other than in the first and last rounds of transmission, a SCIn_TXI request can activate DMAC or DTC to handle writing of data to TDR. Also, for data other than the last data to be received , an SCI_nRXI request can activate DMAC or DTC to handle reading of data from RDR.

[6] NACK is transmitted in response to the last data.

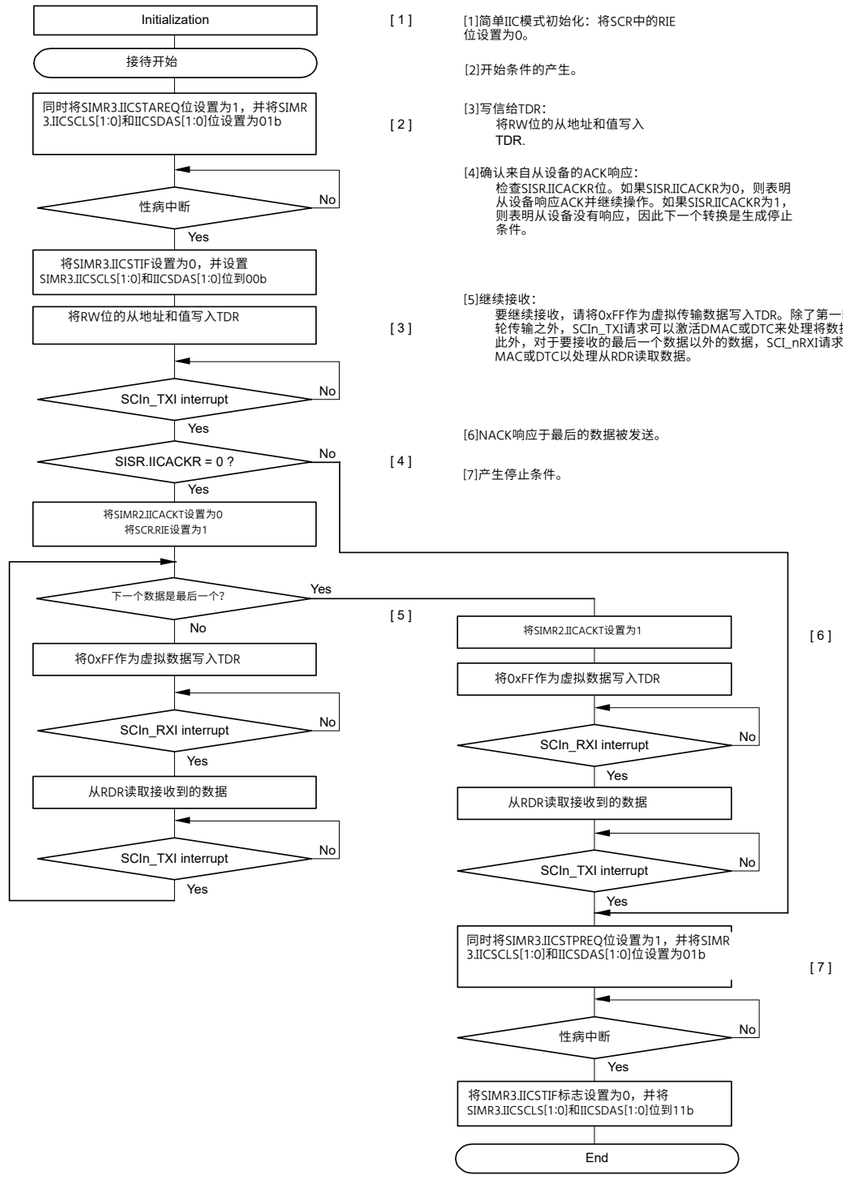
[7] Generation of a stop condition.

Note: In simple IIC mode, the SCIn_TXI interrupt request is generated when communication is complete.

Figure 30.97 Example flow of master reception in simple IIC mode with transmission interrupts and reception interrupts

30.9 Operation in Simple SPI Mode

As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.



[1] [1]简单IIC模式初始化：将SCR中的RIE位设置为0。

[2]开始条件的产生。

[2] [3]写信给TDR：
将RW位的从地址和值写入TDR.

[4]确认来自从设备的ACK响应：
检查SISR.IICACKR位。如果SISR.IICACKR为0，则表明从设备响应ACK并继续操作。如果SISR.IICACKR为1，则表明从设备没有响应，因此下一个转换是生成停止条件。

[3] [5]继续接收：
要继续接收，请将0xFF作为虚拟传输数据写入TDR。除了第一轮和最后一轮传输之外，SCIn_TXI请求可以激活DMAC或DTC来处理将数据写入TDR。此外，对于要接收的最后一个数据以外的数据，SCI_nRXI请求可以激活DMAC或DTC以处理从RDR读取数据。

[6]NACK响应于最后的数据被发送。

[4] [7]产生停止条件。

Note: 在简单IIC模式下，通信完成时会产生SCIn_TXI中断请求。

Figure 30.97 带有发送中断和接收中断的简单IIC模式下的主机接收示例流程

30.9 简单SPI模式下的操作

作为一项扩展功能，SCI支持简单的SPI模式，可处理一个或多个主设备与多个从设备之间的传输。

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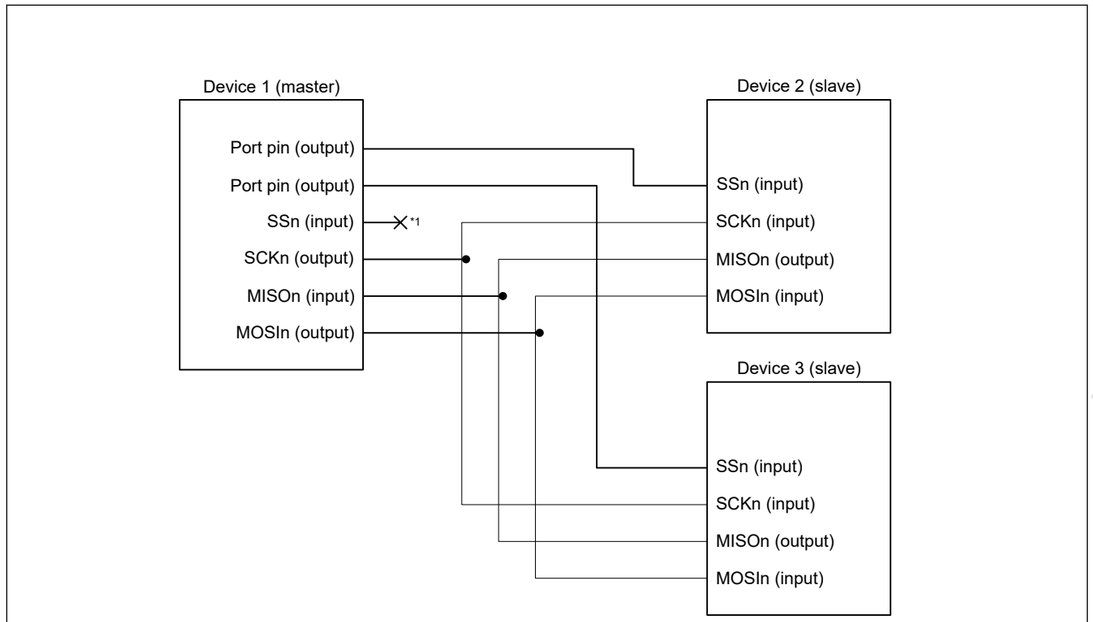
Using the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) and setting the SPMR.SSE bit to 1 place the SCI in simple SPI mode. However, the SSn pin function on the master side is not required for connection of the device used as the master in simple SPI mode when the configuration only has a single master. Therefore, set the SPMR.SSE bit to 0 in such cases.

Figure 30.98 shows an example of connections for simple SPI mode. Control a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the SCMR.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a shared clock signal. Additionally, because both the transmitter and receiver have a buffered structure, writing the next transmit data while transmission is in progress and reading previously received data while reception is in progress are both possible. This enables continuous transfer.



Note 1. The SSn pin input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 30.98 Example connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

30.9.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] bits = 00b or 01b and SPMR.MSS bit = 0) or slave (SCR.CKE[1:0] bits = 10b or 11b and SPMR.MSS bit = 1).

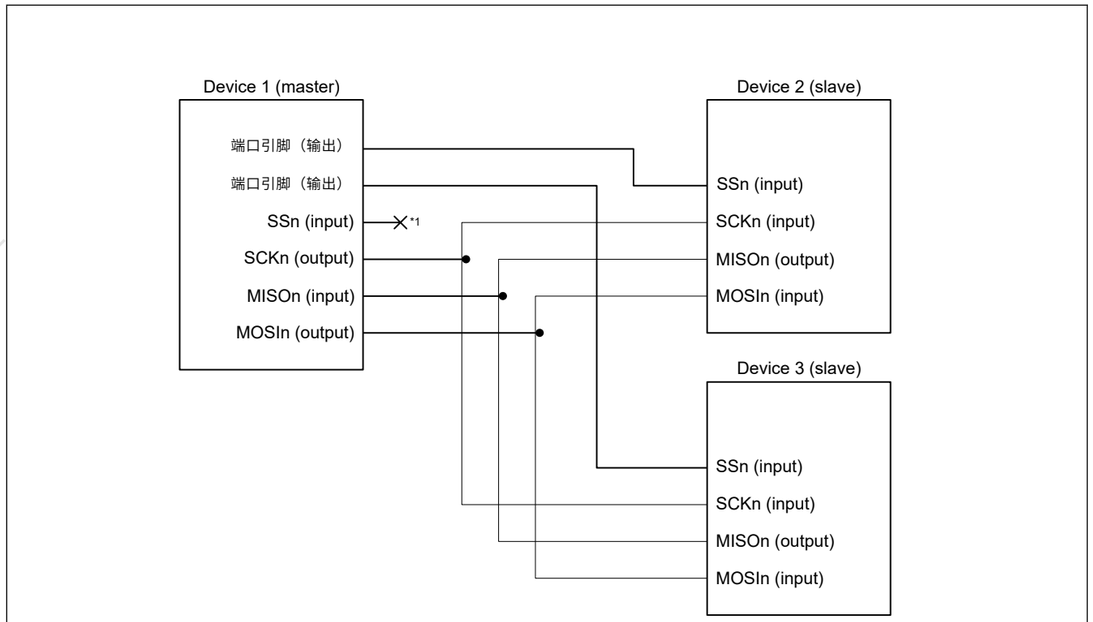
Table 30.41 lists the relationship between the pin states, mode, and level on the SSn pin.

使用时钟同步模式的设置(SCMR.SMIF=0 SIMR1.IICM=0 SMR.CM=1)并设置SPMR.SSE位为1将SCI置于简单SPI模式。但是，当配置只有一个主控时，在简单SPI模式下连接用作主控的设备不需要主控侧的SSn引脚功能。因此，在这种情况下，将SPMR.SSE位设置为0。

图30.98显示了简单SPI模式的连接示例。控制一个通用端口引脚以产生来自主机的SSn输出信号。

在简单SPI模式下，数据与时钟脉冲同步传输，方式与时钟同步模式相同。1个字符的传输数据由8位数据组成，不能附加奇偶校验位。可以通过将SCMR.SINV位设置为1来反转数据。

由于接收器和发送器在SCI模块中彼此独立，因此可以使用共享时钟信号进行全双工通信。此外，由于发送器和接收器都具有缓冲结构，因此在发送过程中写入下一个发送数据和在接收过程中读取先前接收到的数据都是可能的。这使得连续传输成为可能。



注1.在单主机系统中不需要SSn引脚输入（该接口在设置SPMR.SSE=0时使用）。

Figure 30.98 在SPMR.SSE位=0的单主模式下使用简单SPI模式的示例连接

30.9.1 主从模式下的引脚状态

简单SPI模式接口的引脚方向（输入或输出）根据设备是主设备（SCR.CKE[1:0]位=00b或01b且SPMR.MSS位=0）还是从设备（SCR.CKE[1:0]位=10b或11b且SPMR.MSS位=1)。

表30.41列出了SSn引脚上的引脚状态、模式和电平之间的关系。

Table 30.41 States of pins by mode and input level on SSn pin

Mode	Input on SSn pin	State of MOSIn pin	State of MISOn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin.
Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit =0 andSCRRE bit = 0) in a multi-master configuration (SPMR.SSE = 1).

30.9.2 SS Function in Master Mode

Setting the CKE[1:0] bits in the SCR to 00b or 01b and the MSS bit in the SPMR to 0 selects master mode operation. The SSn pin is not used in single-master configurations (SPMR.SSE = 0), so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and a transmission or reception is in progress. The MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. In addition, the value of the SPMR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. If a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn outputs are in the high-impedance state after completion of the transfer.

Use a general port pin to produce the SS output signal from the master.

30.9.3 SS Function in Slave Mode

Setting the SCR.CKE[1:0] bits to 10b or 11b and the SPMR.MSS bit to 1 selects slave operation. When the SSn pin is high, the MISOn output pin is in the high-impedance state and clock input through the SCKn pin is ignored. When the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high during transmission or reception, the MISOn output pin is placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the character being transmitted or received is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, or SCIn_TEI) is generated.

30.9.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR register can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 30.99. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

Table 30.41 SSn引脚上的模式和输入电平的引脚状态

Mode	SSn引脚上的输入	MOSIn管脚状态	MISon引脚的状态	SCKn引脚状态
主模式*1	高电平（可以进行转移）	数据传输用输出*2	接收数据的输入	时钟输出*3
	低电平（传输无法进行）	High-impedance	接收数据的输入（但禁用）	High-impedance
从机模式	高电平（传输无法进行）	接收数据的输入（但禁用）	High-impedance	时钟输入（但禁用）
	低电平（可以继续传输）	接收数据的输入	数据传输输出	时钟输入

注1.当只有一个主机(SPMR.SSE=0)时，无论SSn引脚上的输入电平如何，都可以进行传输。这相当于在SSn引脚上输入高电平。

注2.当串行传输被禁用（SCR.TE位=0）时，MOSIn引脚输出处于高阻抗状态。
注3.在多主机配置(SPMR.SSE=1)中禁用串行传输(SCR.TE位=0和SCRRE位=0)时，SCKn引脚输出处于高阻抗状态。

30.9.2 主控模式下的SS功能

将SCR中的CKE[1:0]位设置为00b或01b并将SPMR中的MSS位设置为0选择主机模式操作。这SSn引脚不用于单主机配置(SPMR.SSE=0)，因此无论SSn引脚的值如何，都可以进行发送或接收。

在多主机配置（SPMR.SSE=1）中，当SSn引脚上的电平为高电平时，主机设备在开始发送或接收之前从SCKn引脚输出时钟信号，以指示没有其他主机或另一个主机在进行接收或发送。

在多主机配置（SPMR.SSE=1）中，当SSn引脚上的电平为低电平时，存在其他主机，并且正在进行发送或接收。MOSIn输出和SCKn引脚处于高阻状态，无法开始发送或接收。此外，SPMR.MFF位的值为1，表示模式故障错误。在多主机配置中，通过读取SPMR.MFF标志开始错误处理。如果在发送或接收过程中发生模式故障错误，则发送或接收不会停止，但MOSIn和SCKn输出在传输完成后处于高阻抗状态。

使用通用端口引脚从主机产生SS输出信号。

30.9.3 从模式下的SS功能

将SCR.CKE[1:0]位设置为10b或11b并将SPMR.MSS位设置为1选择从机操作。当SSn引脚为高电平时，MIOn输出引脚处于高阻状态，通过SCKn引脚输入的时钟被忽略。当SSn引脚为低电平时，通过SCKn引脚输入的时钟有效，可以进行发送或接收。

如果SSn引脚上的输入在发送或接收期间从低电平变为高电平，则MISOn输出引脚处于高阻抗状态。同时，发送或接收的内部处理以通过SCKn引脚输入的时钟速率继续进行，直到对正在发送或接收的字符的处理完成，之后它停止，并出现适当的中断（SCIn_TXI、SCIn_RXI或SCIn_TEI）生成。

30.9.4 时钟与发送接收数据的关系

SPMR寄存器中的CKPOL和CKPH位可用于以四种不同的方式设置用于发送和接收的时钟。时钟信号与数据收发的关系如图30.99所示。主从操作的关系是相同的。这与SSn引脚上的电平为高电平时相同。

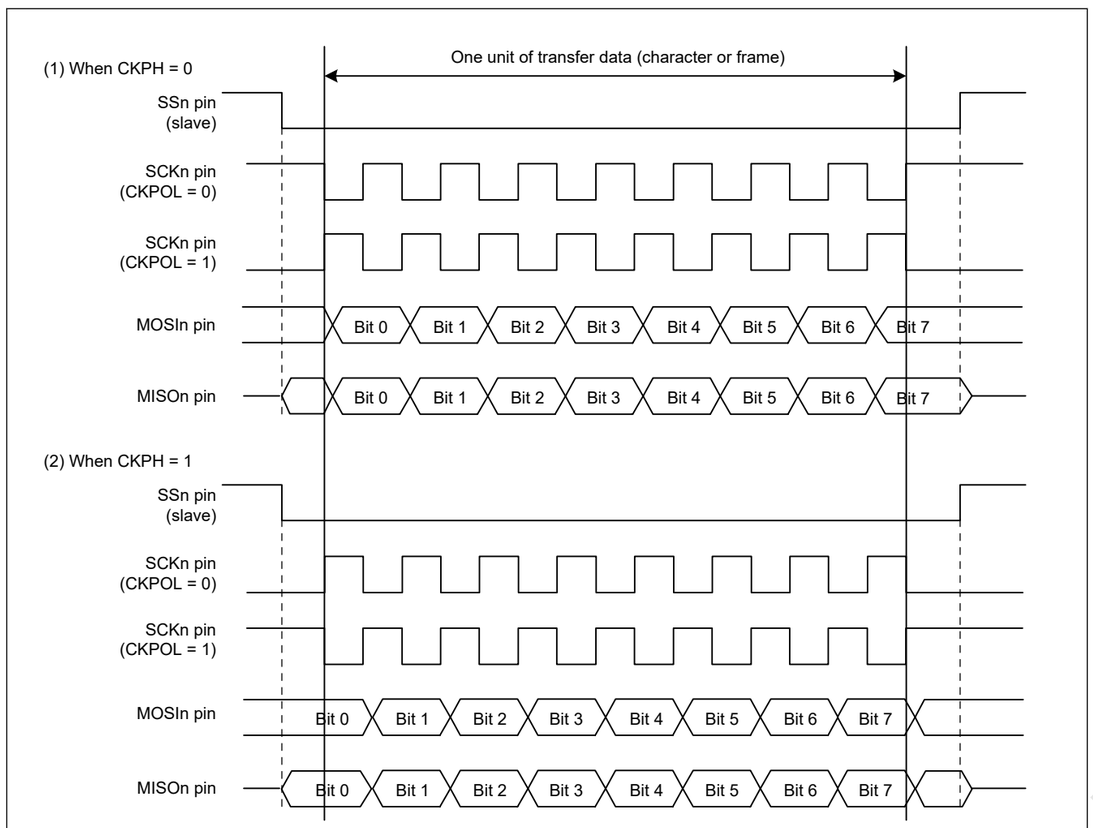


Figure 30.99 Relation between clock signal and transmit or receive data in simple SPI mode

30.9.5 SCI Initialization in Simple SPI Mode

Initialization in simple SPI mode is the same as in clock synchronous mode. See section 30.6.3. SCI Initialization in Clock Synchronous Mode for an example initialization flow. The CKPOL and CKPH bits in the SPMR register must be set to ensure that the clock signal is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note: Only the RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.

Changing the value of the TE bit from 1 to 0 or from 0 to 1 when the TIE bit in the SCR register is 1 at the same time, leads to the generation of a transmit data empty interrupt (SCIn_TXI).

30.9.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

30.10 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register among 256 clock cycles of internal clocks which is selected by the CKS[1:0] bits in SMR/SMR_SMCI.

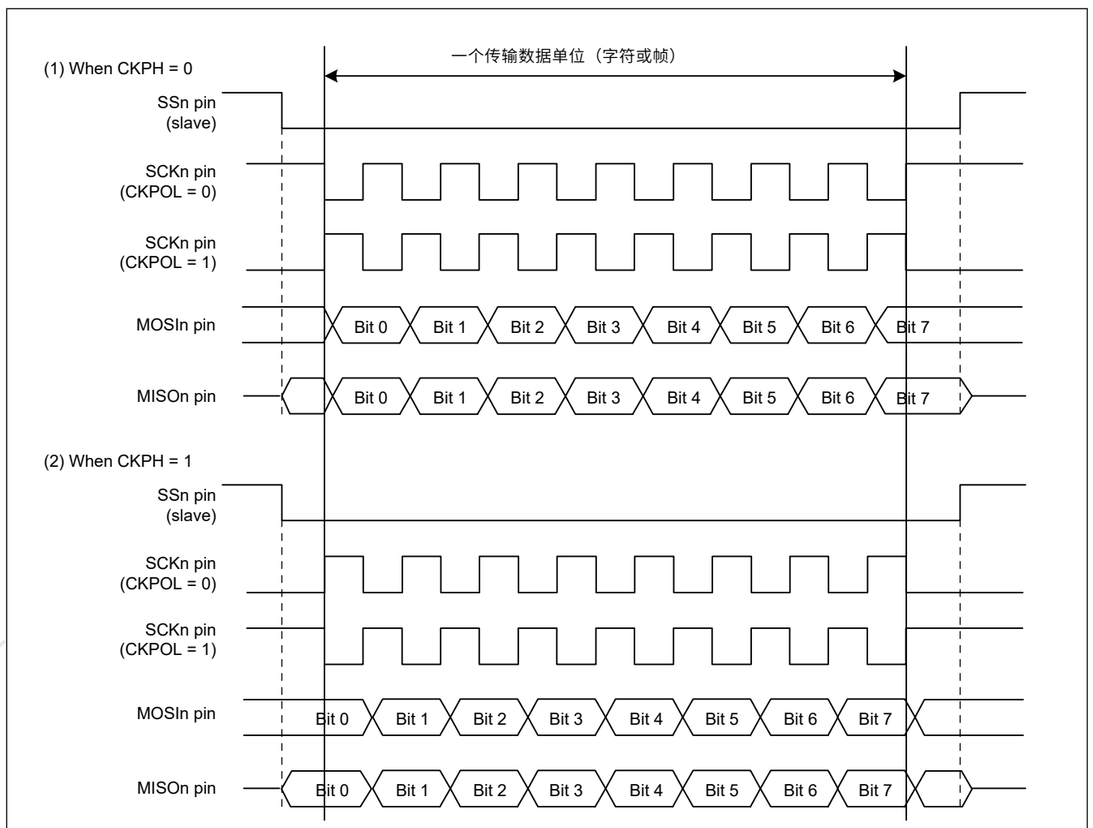


Figure 30.99 简单SPI模式下时钟信号与发送或接收数据的关系

30.9.5 简单SPI模式下的SCI初始化

简单SPI模式的初始化与时钟同步模式相同。请参阅第30.6.3节。时钟中的SCI初始化
示例初始化流程的同步模式。必须设置SPMR寄存器中的CKPOL和CKPH位，以确保时钟信号适用于主设备和从设备。

在对操作模式或传输格式进行任何更改之前，始终初始化SCR寄存器。

Note: 只有RE位设置为0。SSR.ORER、FER、PER和RDR标志未初始化。

当SCR寄存器中的TIE位同时为1时，将TE位的值从1更改为0或从0更改为1，会导致产生发送数据空中断（SCIn_TXI）。

30.9.6 简单SPI模式下串行数据的发送和接收

在主机操作中，确保传输另一侧的从设备的SSn管脚在开始传输前为低电平，在传输完成时为高电平。否则，过程与时钟同步模式相同。

30.10 比特率调制功能

使用比特率调制功能，可以在SMRSMR_SMCI中的CKS[1:0]位选择的内部时钟的256个时钟周期中，使用MDDR寄存器中指定的数量均匀地校正比特率。

Figure 30.100 shows an example where the PCLK is selected in the CKS[1:0] bits in SMR/SMR_SMCI, the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias, and expansion and contraction are generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

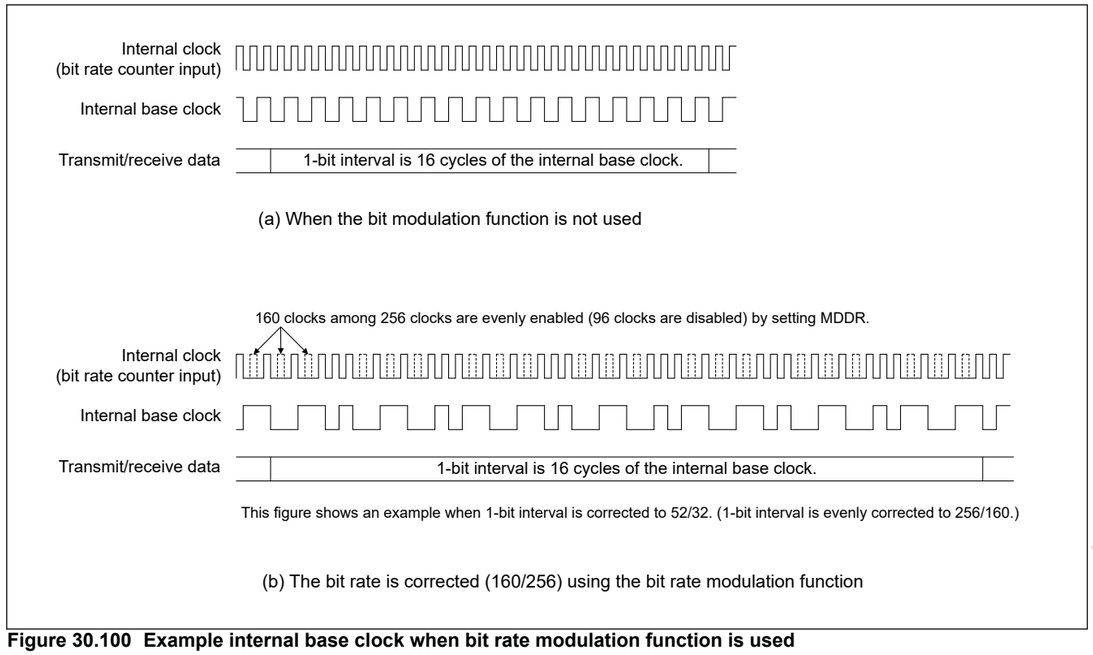


Figure 30.100 Example internal base clock when bit rate modulation function is used

30.11 Extended Serial Mode Control Section: Description of Operation

30.11.1 Serial Transfer Protocol

In conjunction with the SCIg module, the extended serial mode control section of the SCIh module can realize the serial transfer protocol composed of Start Frames and Information Frames that is shown in Figure 30.101.

A Start Frame is composed of a Break Field, Control Field 0, and Control Field 1. An Information Frame is composed of a number of Data Fields, a CRC16 Upper Field, and a CRC16 Lower Field.

图30.100显示了一个示例，其中在SMRSMR_SMCI的CKS[1:0]位中选择PCLK，BRR位设置为0，异步模式下MDDR设置为160。在这个例子中，基本时钟的周期被均匀地校正（256160）并且比特率也被校正（160256）。

Note: 启用内部时钟会导致偏差，并且会在内部基本时钟的脉冲宽度中产生扩展和收缩。

不要在时钟同步模式和简单SPI模式的最高速度设置（SMR.CKS[1:0]=00b，SCR.CKE[1]=0和BRR=0）中使用此功能。

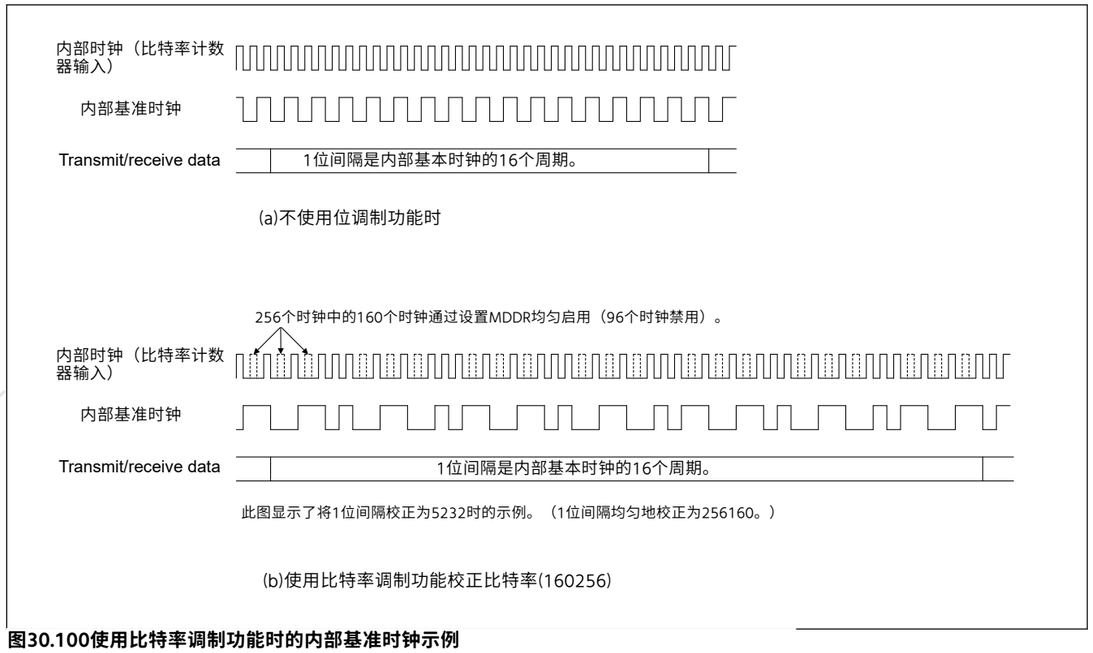


图30.100使用比特率调制功能时的内部基准时钟示例

30.11 扩展串行模式控制部分：操作说明

30.11.1 串行传输协议

结合SCIg模块，SCIh模块的扩展串行模式控制部分可以实现由StartFrames和InformationFrames组成的串行传输协议，如图30.101所示。

起始帧由中断字段、控制字段0和控制字段1组成。信息帧由多个数据字段、CRC16上字段和CRC16下字段组成。

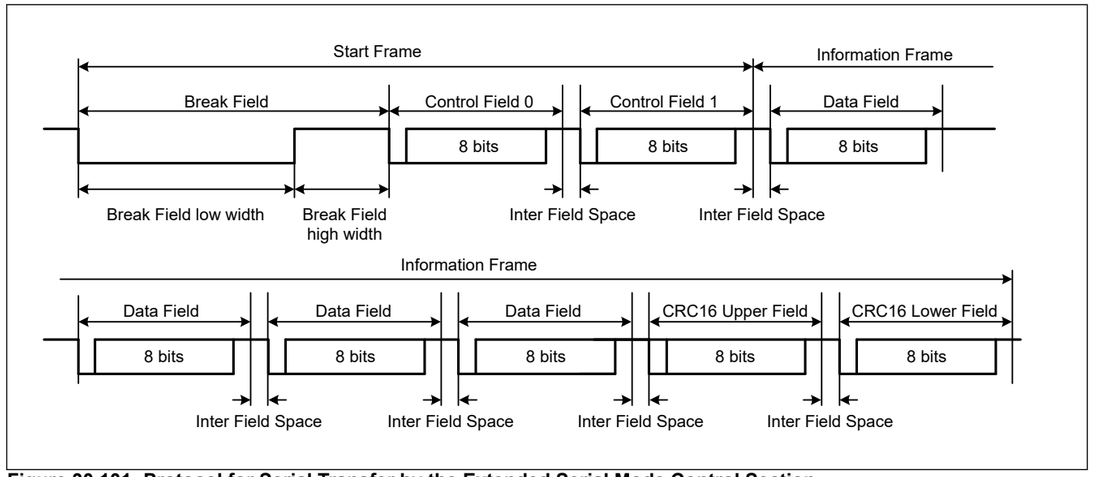


Figure 30.101 Protocol for Serial Transfer by the Extended Serial Mode Control Section

30.11.2 Transmitting a Start Frame

Figure 30.102 shows an example of operations to transmit a Start Frame, which is composed of the Break Field low width, Control Field 0, and Control Field 1. Figure 30.103 and Figure 30.104 are flowcharts for the transmission of a Start Frame.

Operations when the extended serial mode control section is to be used to transmit a Start Frame are as listed below. Be sure to use the SCIn (n = 1, 2) in asynchronous mode.

1. With Break Field low width output mode as the operating mode for the timer, writing 1 to the TCR.TCST bit starts counting by the timer, and the low level will be output from the TXDXn (n = 1, 2) pin over the period corresponding to registers TCNT and TPRE settings.
2. The output on the TXDXn pin is inverted when the timer counter underflows, and the STR.BFDF flag is set to 1. An SCIX0 interrupt is also generated if the value of the ICR.BFDIE bit is 1.
3. Write 0 to the TCR.TCST bit to stop counting by the timer, and send the data for Control Field 0 by using SCIn. After the Break Field low width output, stop counting before the next underflow occurs.
4. When the data for Control Field 0 have been transmitted, send the data for Control Field 1.
5. When the data for Control Field 1 have been transmitted, send an Information Frame.

Omit the Break Field and Control Field 0 to suit the structure of the Start Frame.

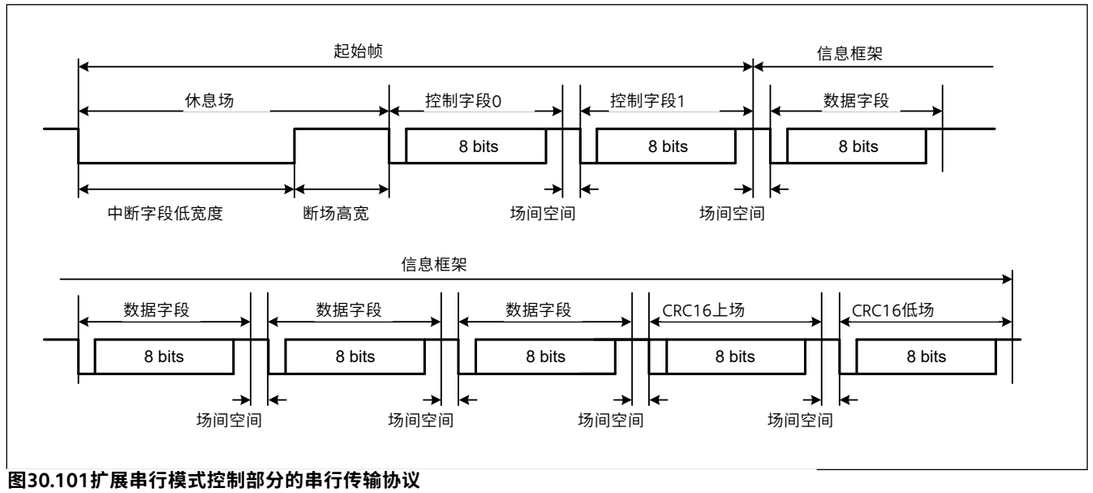


图30.101扩展串行模式控制部分的串行传输协议

30.11.2 发送起始帧

图30.102显示了发送起始帧的操作示例，起始帧由中断字段低宽度、控制字段0和控制字段1组成。图30.103和图30.104是发送起始帧的流程图。

使用扩展串行模式控制部分发送起始帧时的操作如下所列。请务必在异步模式下使用SCIn(n=1 2)。

1.以中断场低宽度输出模式作为定时器的工作模式，开始向TCR.TCST位写入1
由定时器计数，在对应于寄存器TCNT和TPRE设置的周期内，低电平将从TXDXn(n=1 2)引脚输出。

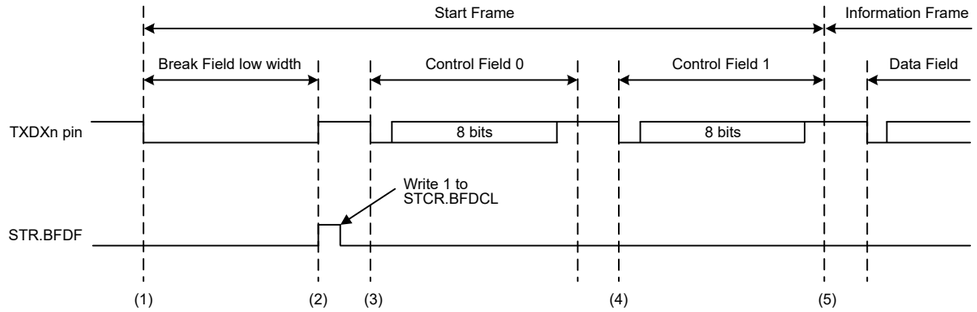
2.当定时器计数器下溢时，TXDXn引脚的输出反相，STR.BFDF标志设置为1。如果ICR.BFDIE位的值为1，也会产生SCIX0中断。

3.将0写入TCR.TCST位以停止定时器计数，并使用SCIn发送控制字段0的数据。在BreakField低宽度输出之后，在下一次下溢发生之前停止计数。

4.当控制字段0的数据传输完毕后，发送控制字段1的数据。

5.当控制字段1的数据传输完毕后，发送一个信息帧。

省略BreakField和ControlField0以适应起始帧的结构。

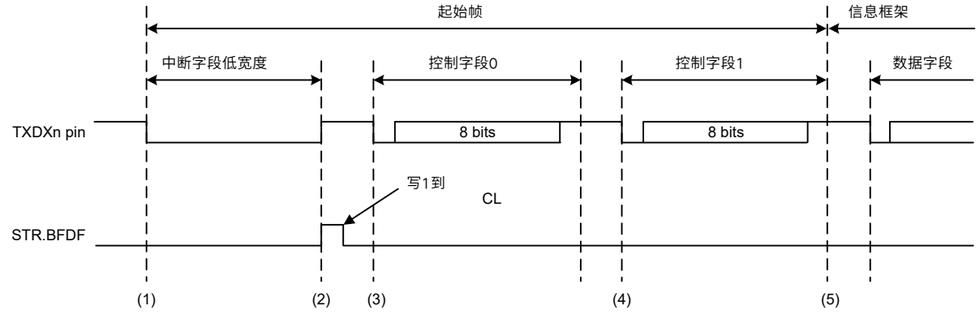


The above diagram assumes the following:

ESMER: ESME = 1
PCR: TXDXPS = 0
ICR: BFDIE = 1
TMR: TOMS[1:0] = 10b

Note: n = 1, 2

Figure 30.102 Example of Operations When Transmitting a Start Frame



上图假设如下：

ESMER: ESME = 1
PCR: TXDXPS = 0
ICR: BFDIE = 1
TMR: TOMS[1:0] = 10b

Note: n = 1, 2

图30.102发送起始帧时的操作示例

RA生态工作室

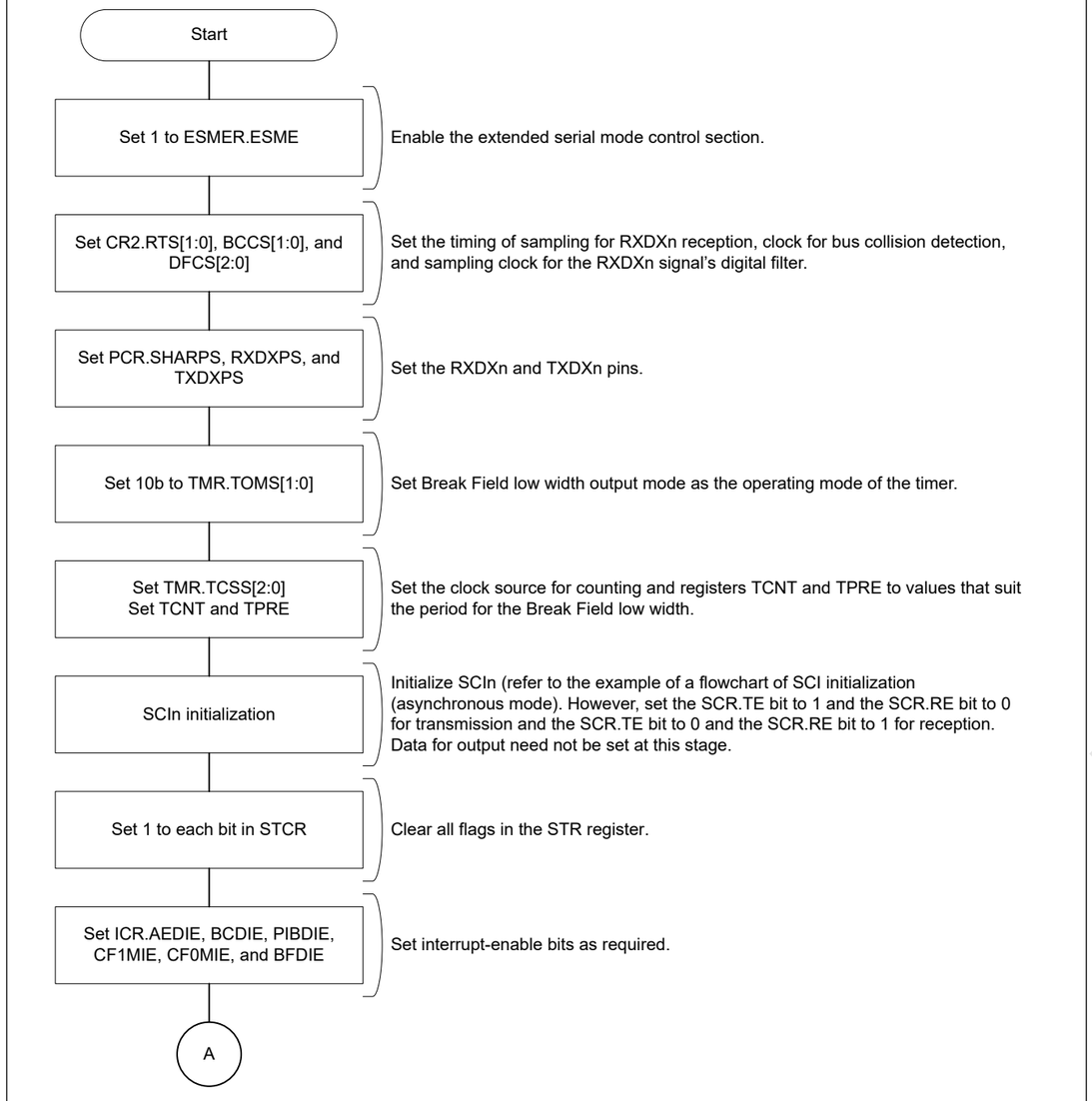


Figure 30.103 Example of Start Frame Transmission (1/2)

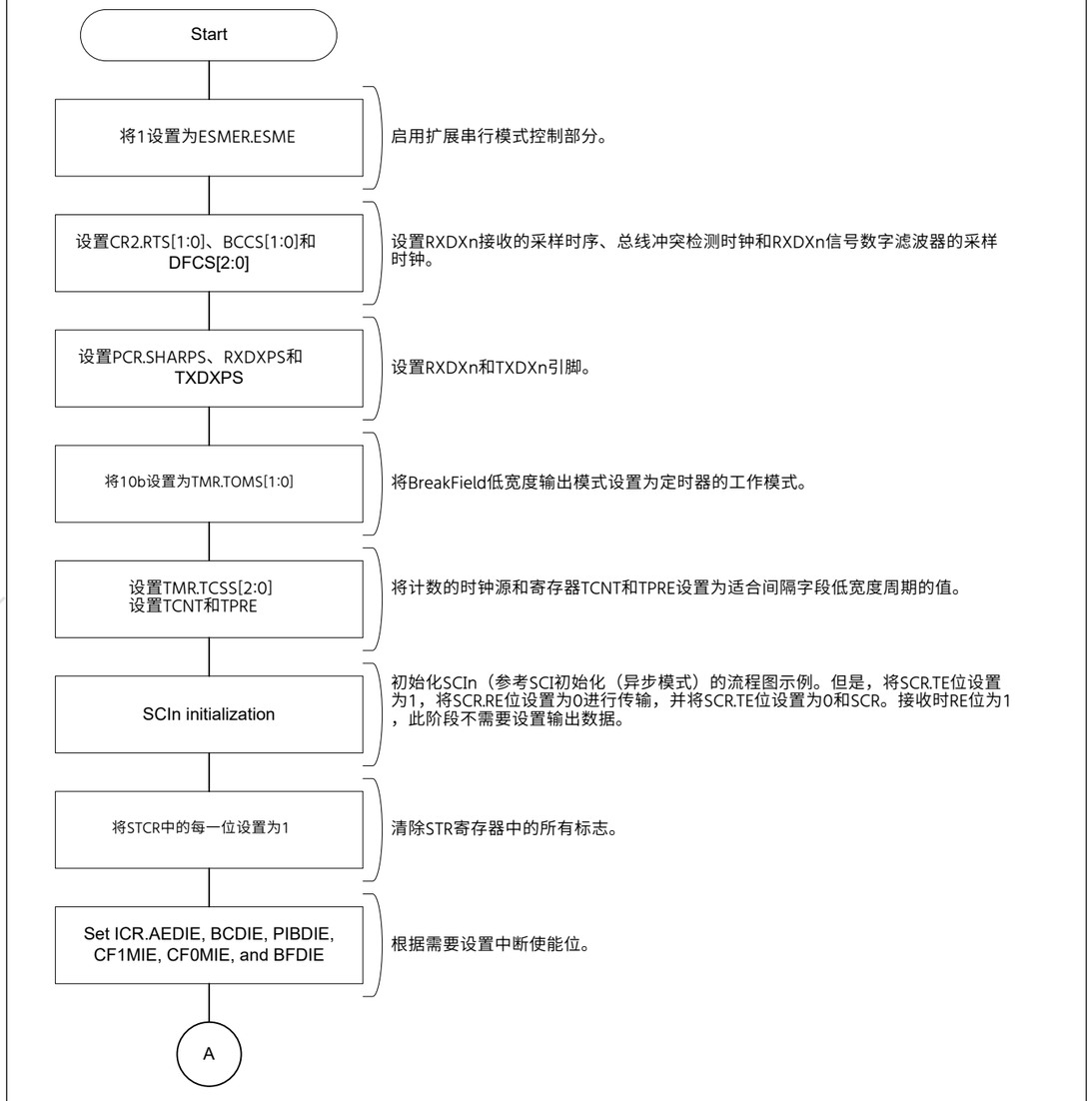


图30.103起始帧传输示例(12)

RA生态工作室

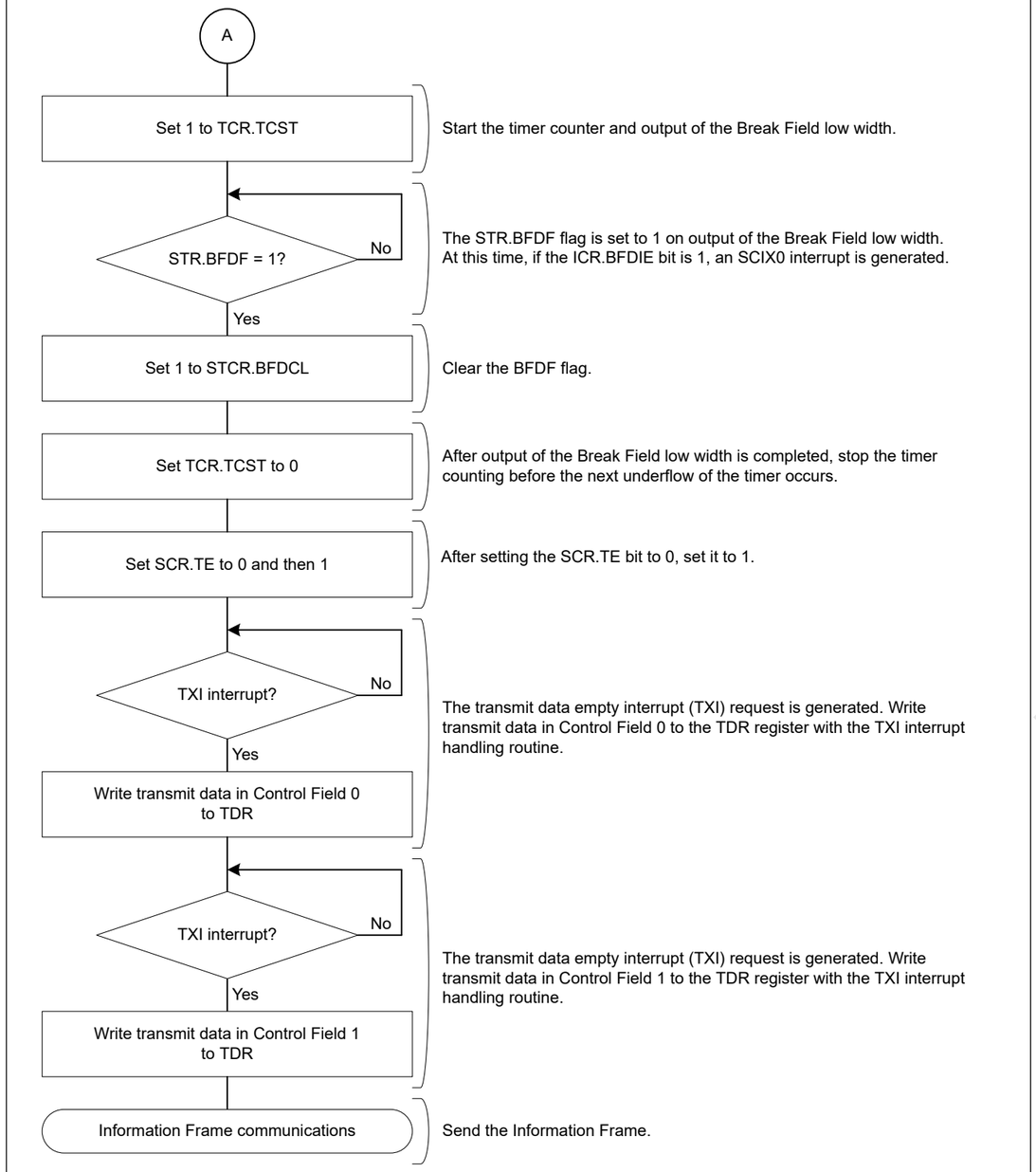


Figure 30.104 Example of Start Frame Transmission (2/2)

30.11.3 Receiving a Start Frame

The extended serial mode control section is capable of receiving Start Frames with the structures listed in Figure 30.105.

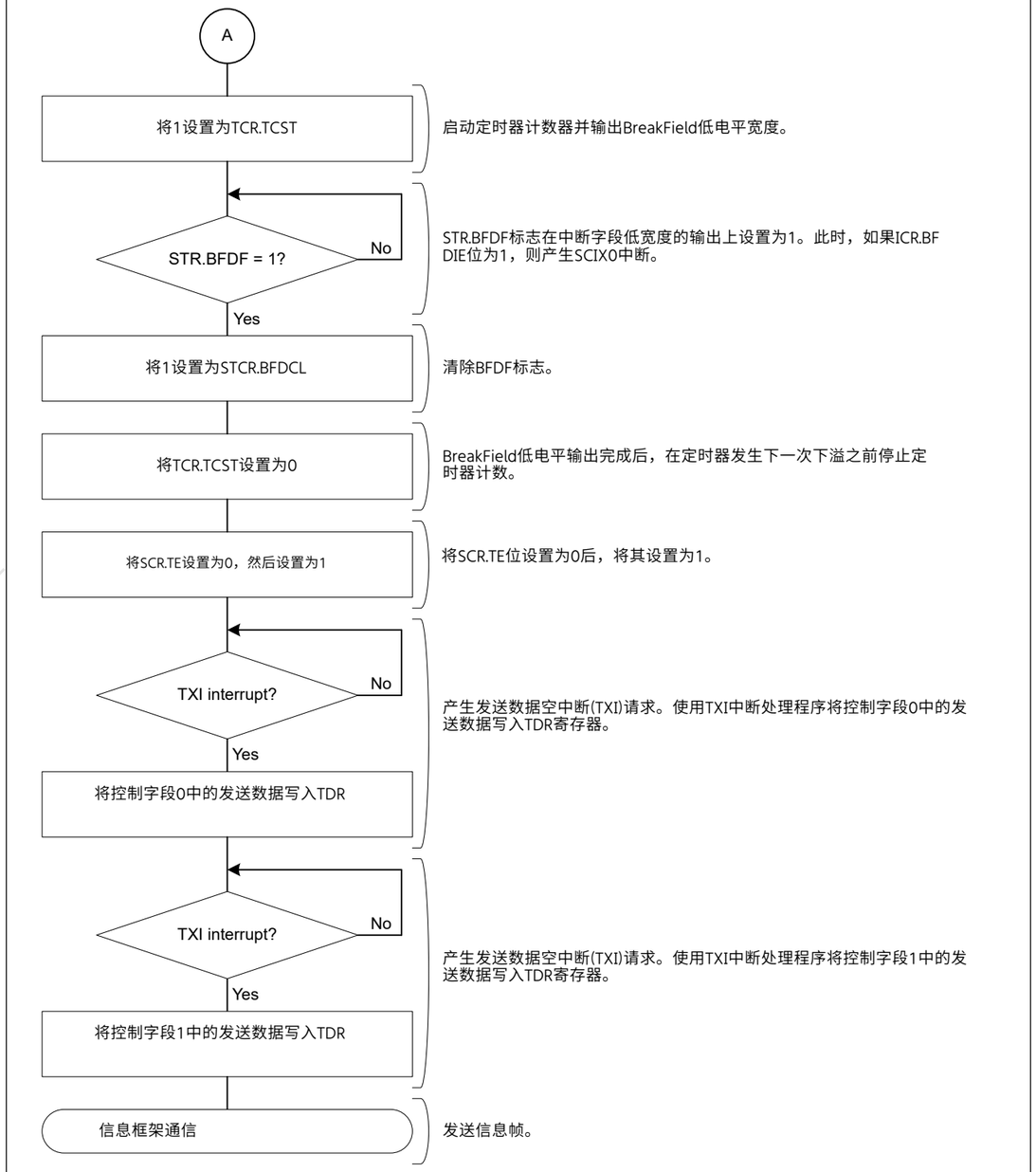


图30.104起始帧传输示例(22)

30.11.3 接收起始帧

扩展串行模式控制部分能够接收具有图30.105中列出的结构的起始帧。

RA生态工作室

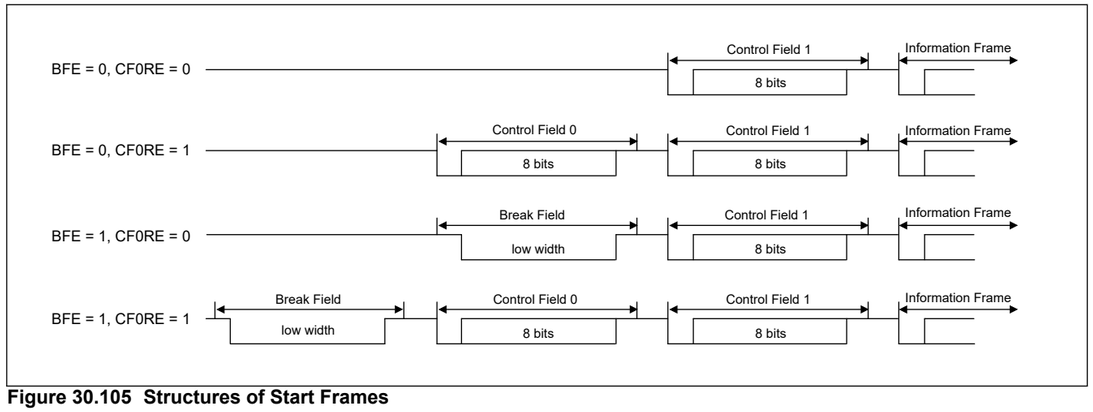


Figure 30.105 Structures of Start Frames

Figure 30.106 shows an example of operations to receive a Start Frame, which is composed of the Break Field low width, Control Field 0, and Control Field 1. Figure 30.107 and Figure 30.108 are flowcharts for the reception of a Start Frame, and Figure 30.109 is a state transition diagram for the extended serial mode control section.

Operations when the extended serial mode control section is to be used to receive a Start Frame are as listed below. Be sure to use the SCIn (n = 1, 2) in asynchronous mode.

1. With Break Field low width detection mode as the operating mode for the timer, writing 1 to the CR3.SDST bit enables detection of the Break Field low width. RXDXn input to the SCIn is disabled at this time.
2. Low-level input on the RXDXn pin continuing over a period longer than that corresponding to the settings of registers TCNT and TPRE is detected as the Break Field low width. At this time, the STR.BFDF flag is set to 1. An SCIX0 interrupt is also generated if the value of the ICR.BFDIE bit is 1.
3. When the input from the RXDXn pin goes high after the Break Field low width, the CR0.RXDSF flag becomes 0 and reception of Control Field 0 by the SCIn starts.
4. If the data received in Control Field 0 match the data set in the CF0DR register, the STR.CF0MF flag is set to 1. An SCIX1 interrupt is also generated if the value of the ICR.CF0MIE bit is 1. Reception of Control Field 1 by the SCIn starts after that. If the data received in Control Field 0 do not match the data set in the CF0DR register, a transition to the state prior to Break Field low width detection proceeds.
5. If the data received in Control Field 1 match the data set in registers PCF1DR and SCF1DR, the STR.CF1MF flag is set to 1. An SCIX1 interrupt is also generated if the value of the ICR.CF1MIE bit is 1. Transfer of the Information Frame by the SCIn starts after that. If the data received in Control Field 1 do not match the data set in either or both of registers PCF1DR and SCF1DR, a transition to the state prior to Break Field low width detection proceeds.

Omit the Break Field and Control Field 0 to suit the structure of the Start Frame.

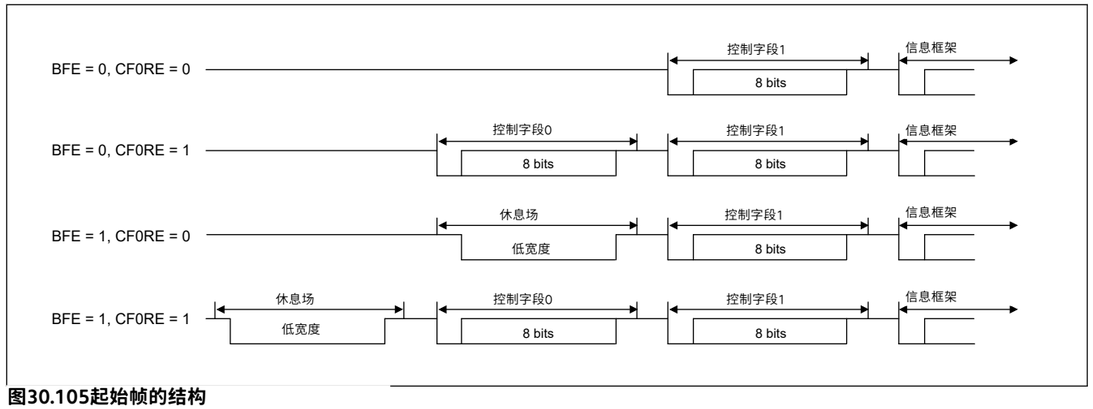


图30.105起始帧的结构

图30.106显示了接收起始帧的操作示例，起始帧由中断字段低宽度组成，控制字段0和控制字段1。图30.107和图30.108是接收起始帧的流程图，以及图30.109是扩展串行模式控制部分的状态转换图。

使用扩展串行模式控制部分接收起始帧时的操作如下所列。请务必在异步模式下使用SCIn(n=1 2)。

1.使用间隔场低宽度检测模式作为定时器的操作模式，向CR3.SDST位写入1可启用间隔场低宽度检测。此时SCIn的RXDXn输入被禁用。

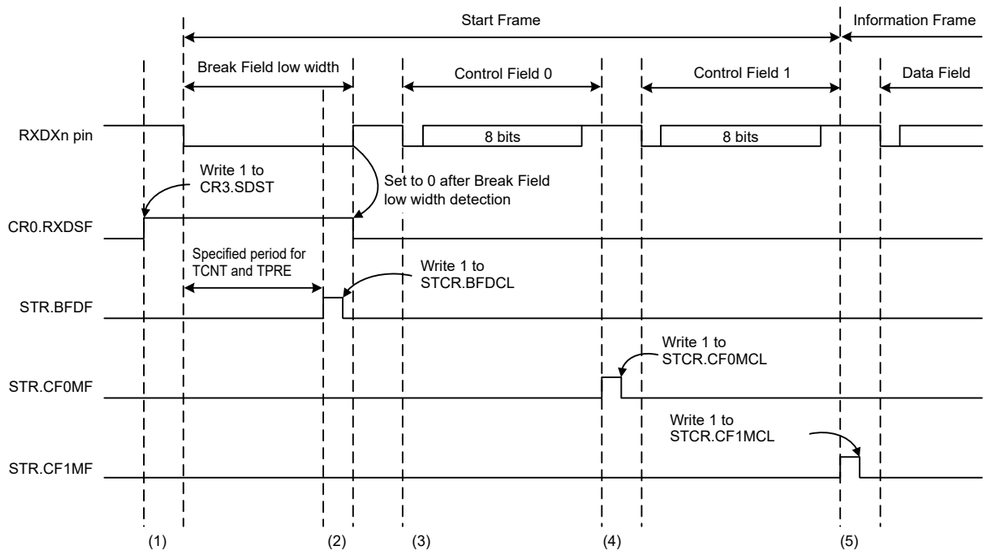
2.RXDXn引脚上的低电平输入持续时间长于对应寄存器TCNT和TPRE的设置的时间被检测为中断场低电平宽度。此时，STR.BFDF标志置1。如果ICR.BFDIE位的值为1，也会产生SCIX0中断。

3.当来自RXDXn引脚的输入在BreakField低电平宽度之后变为高电平时，CR0.RXDSF标志变为0，并且SCIn开始接收ControlField0。

4.如果控制域0中接收的数据与CF0DR寄存器中设置的数据匹配，则STR.CF0MF标志设置为1。如果ICR.CF0MIE位的值为1，也会产生SCIX1中断。接收控制SCIn的字段1在那之后开始。如果在控制字段0中接收到的数据与CF0DR寄存器中设置的数据不匹配，则转换到中断字段低宽度检测之前的状态。

5.如果控制字段1中接收的数据与寄存器PCF1DR和SCF1DR中设置的数据匹配，则STR.CF1MF标志设置为1。如果ICR.CF1MIE位的值为1，也会产生SCIX1中断。SCIn的信息帧在此之后开始。如果在控制字段1中接收到的数据与寄存器PCF1DR和SCF1DR中的一个或两个中设置的数据不匹配，则转换到中断字段低宽度检测之前的状态。

省略BreakField和ControlField0以适应起始帧的结构。

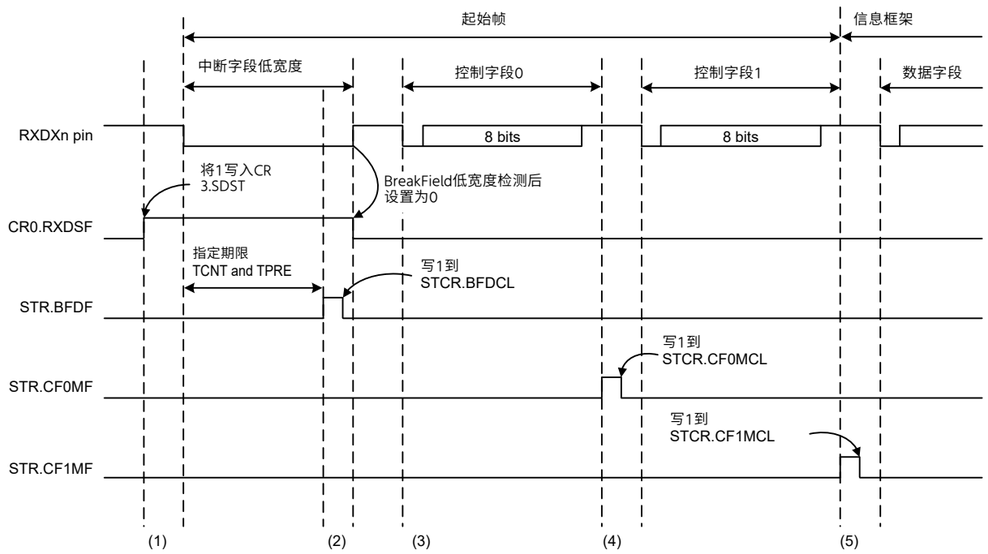


The above diagram assumes the following:

ESMER: ESME = 1
CR1: BFE = 1, CF0RE = 1, CF1DS[1:0] = 10b
PCR: RXDXPS = 0
ICR: BFDIE = 1, CF0MIE = 1, CF1MIE = 1
TMR: TOMS[1:0] = 01b

Note: n = 1, 2

Figure 30.106 Example of Operations at the Time of Start Frame Reception



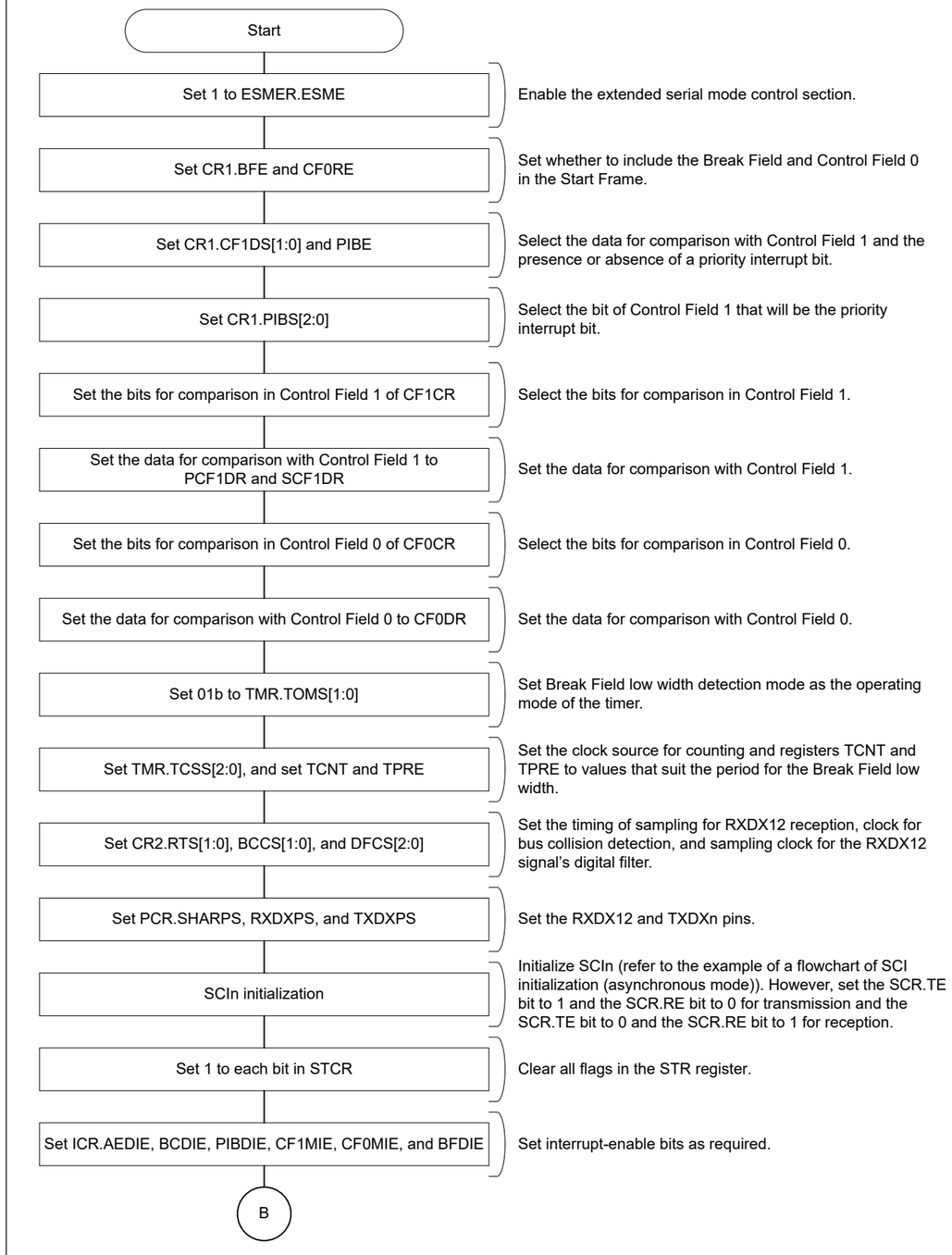
上图假设如下：

ESMER: ESME = 1
CR1: BFE = 1, CF0RE = 1, CF1DS[1:0] = 10b
PCR: RXDXPS = 0
ICR: BFDIE = 1, CF0MIE = 1, CF1MIE = 1
TMR: TOMS[1:0] = 01b

Note: n = 1, 2

图30.106开始帧接收时的操作示例

RA生态工作室



Note: n = 1, 2

Figure 30.107 Sample Flowchart for Reception of a Start Frame (1)

Note: n = 1, 2

图30.107接收起始帧的示例流程图(1)

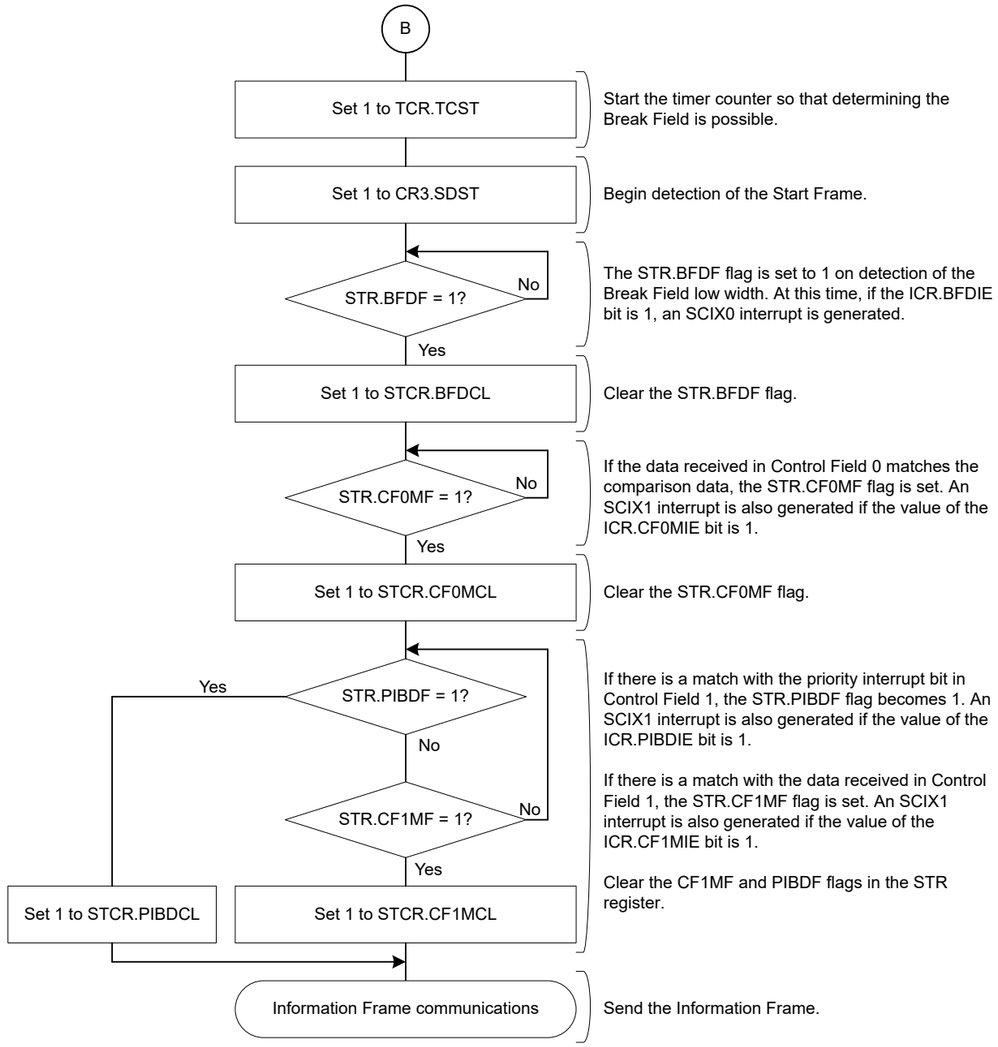


Figure 30.108 Sample Flowchart for Reception of a Start Frame (2)

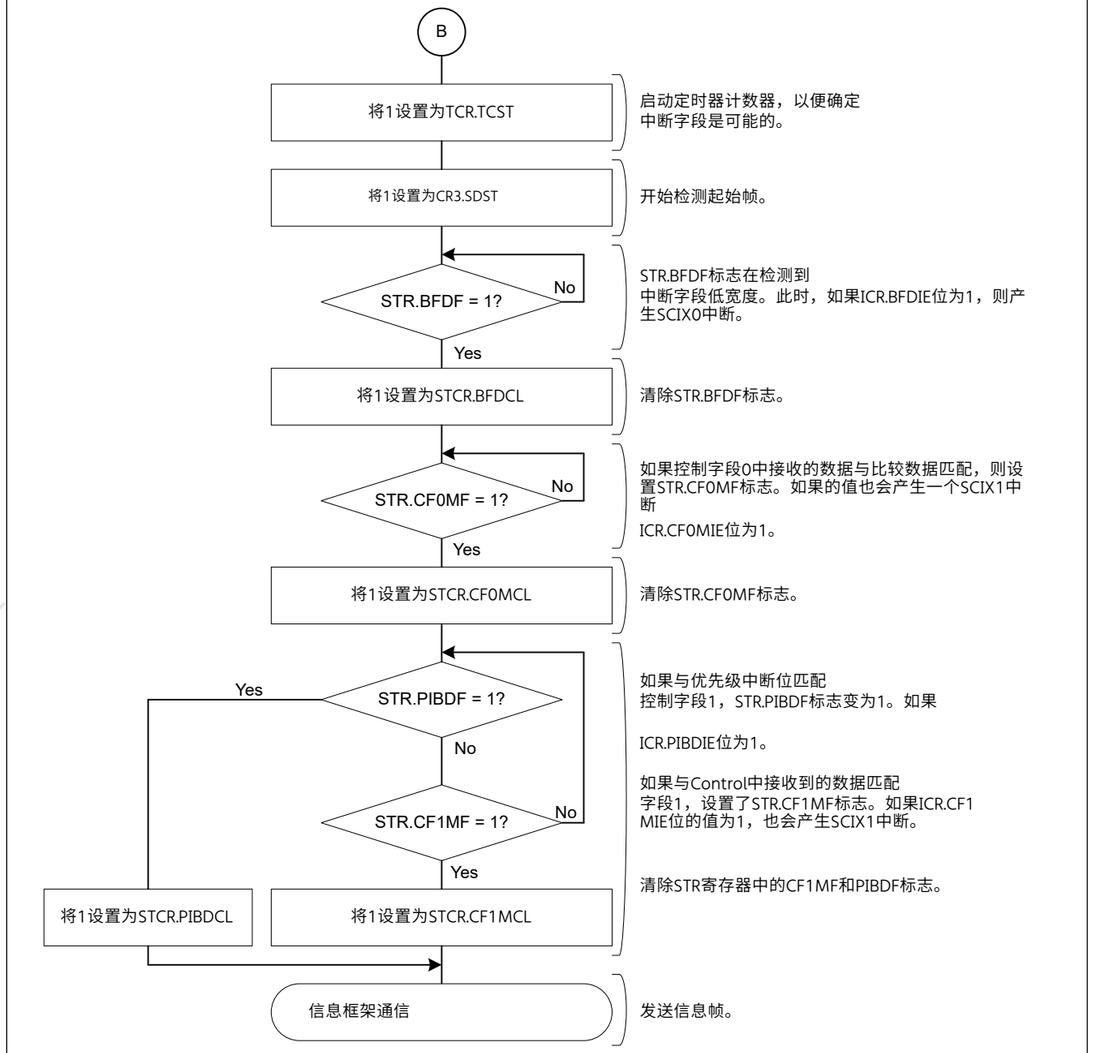


图30.108接收起始帧的示例流程图(2)

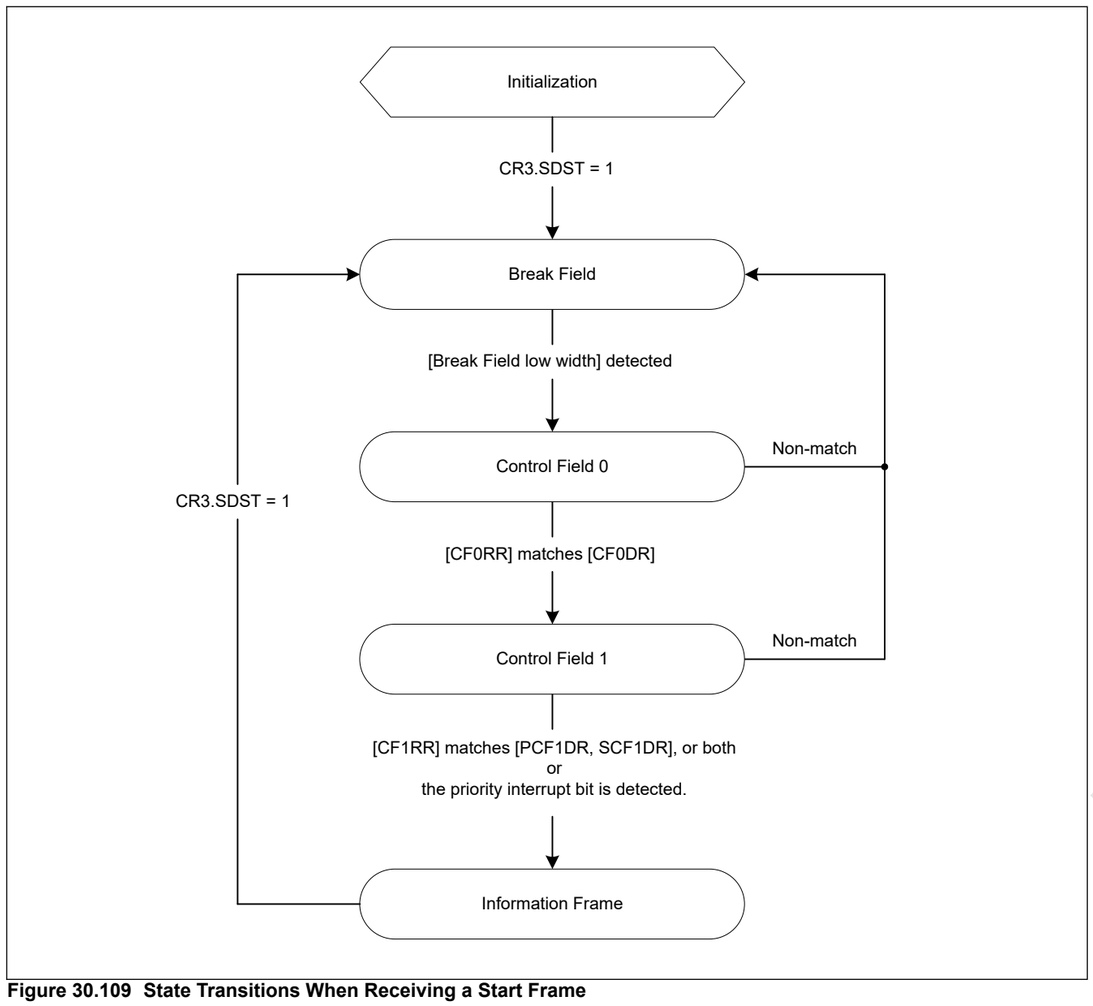


Figure 30.109 State Transitions When Receiving a Start Frame

30.11.3.1 Priority Interrupt Bit

Figure 30.110 shows an example of operation in Start Frame reception where a priority interrupt bit is in use. Setting the CR1.PIBE bit to 1 enables the use of a priority interrupt bit.

Operations of the extended serial mode control section in start Frame reception where a priority interrupt bit is in use are as described below.

Steps (1) to (4) are the same as in Figure 30.106, for Start Frame reception.

(5) If the value of the bit selected by the CR1.PIBS[2:0] bits matches the corresponding bit in the PCF1DR register, the STR.PIBDF flag is set to 1. An SCIX1 interrupt is also generated if the value of the ICR.PIBDIE bit is 1. Transfer of the Information Frame by the SCIn (n = 1, 2) starts after that. If the data received in Control Field 1 do not match the data set in either or both of registers PCF1DR and SCF1DR and the priority interrupt bit is not detected, a transition to the state prior to Break Field low width detection proceeds.

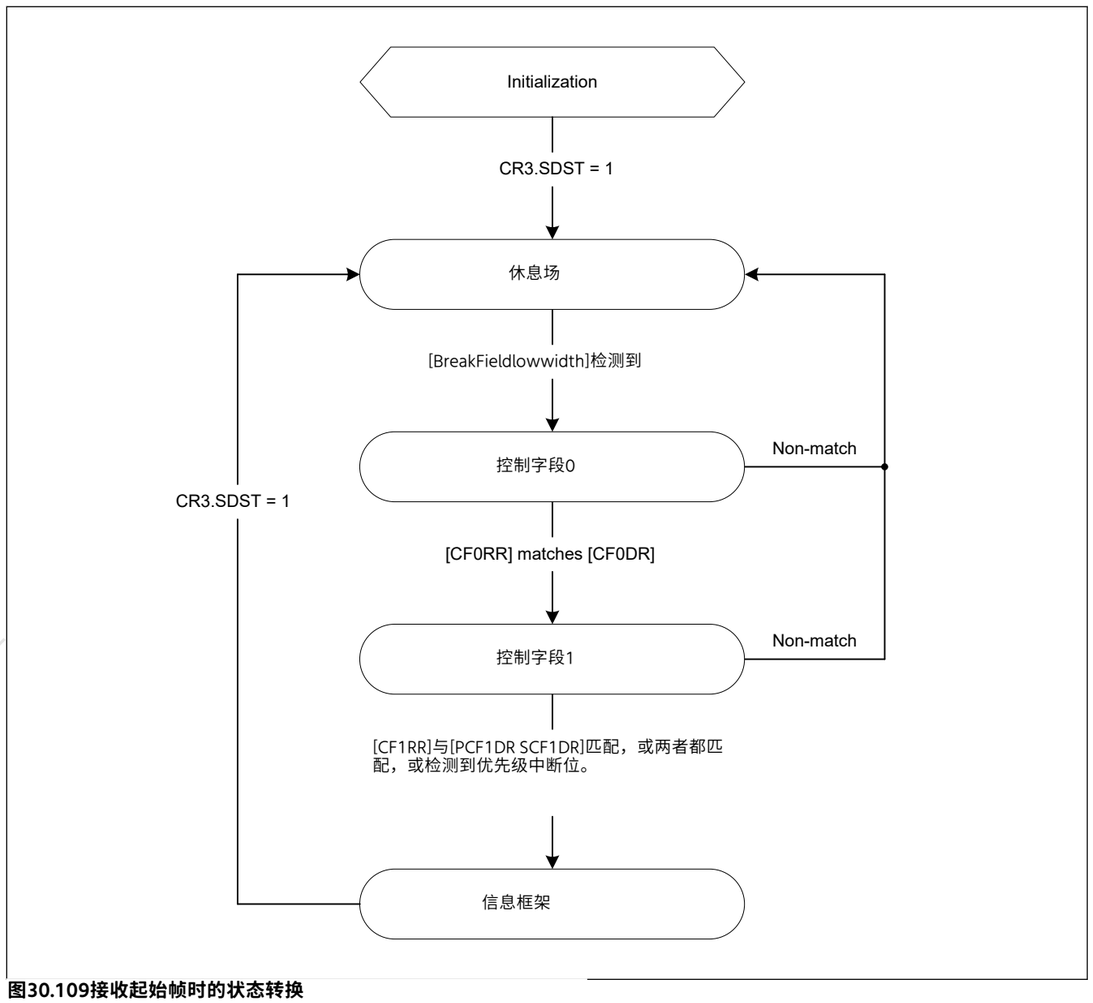


图30.109接收起始帧时的状态转换

30.11.3.1 优先中断位

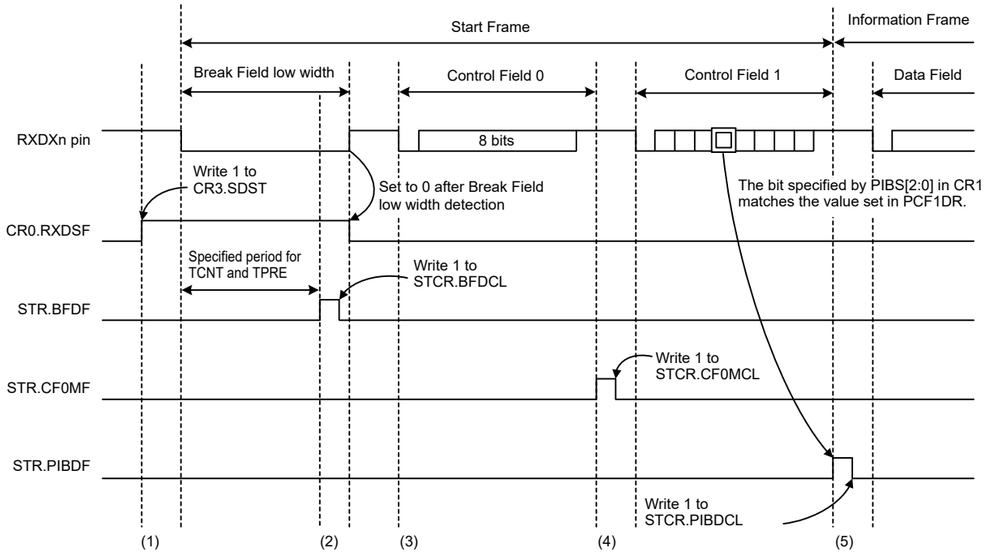
图30.110显示了使用优先中断位的起始帧接收操作示例。设置CR1.PIBE位为1启用优先级中断位。

在使用优先中断位的开始帧接收中扩展串行模式控制部分的操作如下所述。

步骤(1)到(4)与图30.106中的相同，用于接收起始帧。

(5)如果CR1.PIBS[2:0]位选择的位的值与PCF1DR寄存器中的相应位相匹配，则STR.PIBDF标志设置为1。如果ICR.PIBDIE位为1。

SCIn(n=1 2)的信息帧在此之后开始。如果在控制字段1中接收的数据与寄存器PCF1DR和SCF1DR中的一个或两个中设置的数据不匹配，并且未检测到优先级中断位，则转换到中断字段低宽度检测之前的状态。



The above diagram assumes the following:

ESMER: ESME = 1

CR1: BFE = 1, PIBE = 1, CF0RE = 0, CF1DS[1:0] = 10b, PIBS[2:0] = 011b

PCR: RXDXPS = 0

ICR: BFDIE = 1, CF0MIE = 1, PIBDIE = 1

TMR: TOMS[1:0] = 01b

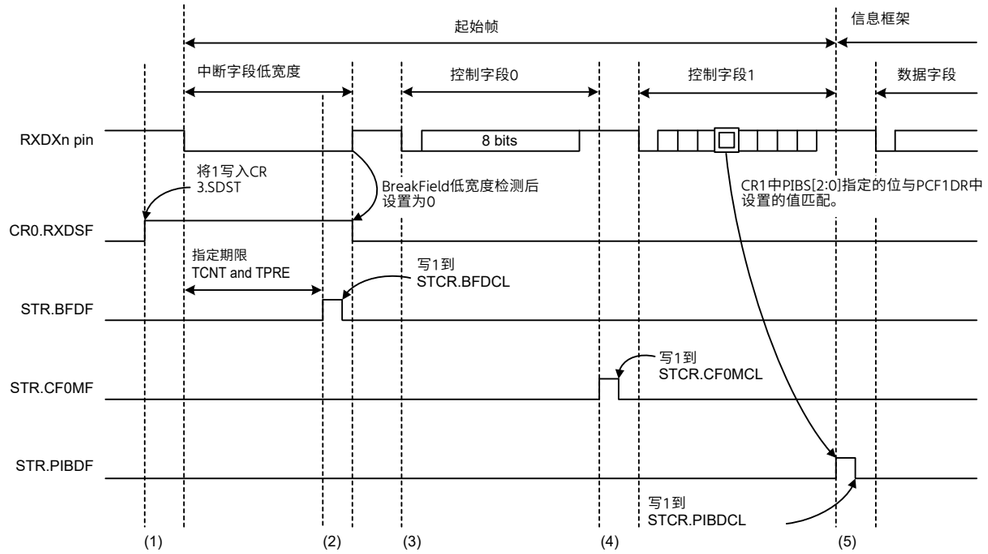
Note: n = 1, 2

Figure 30.110 Example of Operations When Receiving a Start Frame While the CR1.PIBE Bit is 1

30.11.4 Detection of Bus Collisions

Detection of bus collisions operate for cases where output of the Break Field low width and transmission of data by the SCIn (n = 1, 2) are in progress when the ESMER.ESME bit and the SCIn.SCI.TE bit are set to 1.

Figure 30.111 shows an example of operations with bus collision detection. Signals output through TXDXn and input through RXDXn are sampled with the bus collision detection clock set with the CR2.BCCS[1:0] bits as the sampling clock, and the STR.BCDF flag is set to 1 if the signals fail to match three times in a row. An SCIX2 interrupt is also generated if the value of the ICR.BCDIE bit is 1.



上图假设如下：

ESMER: ESME = 1

CR1: BFE = 1, PIBE = 1, CF0RE = 0, CF1DS[1:0] = 10b, PIBS[2:0] = 011b

PCR: RXDXPS = 0

ICR: BFDIE = 1, CF0MIE = 1, PIBDIE = 1

TMR: TOMS[1:0] = 01b

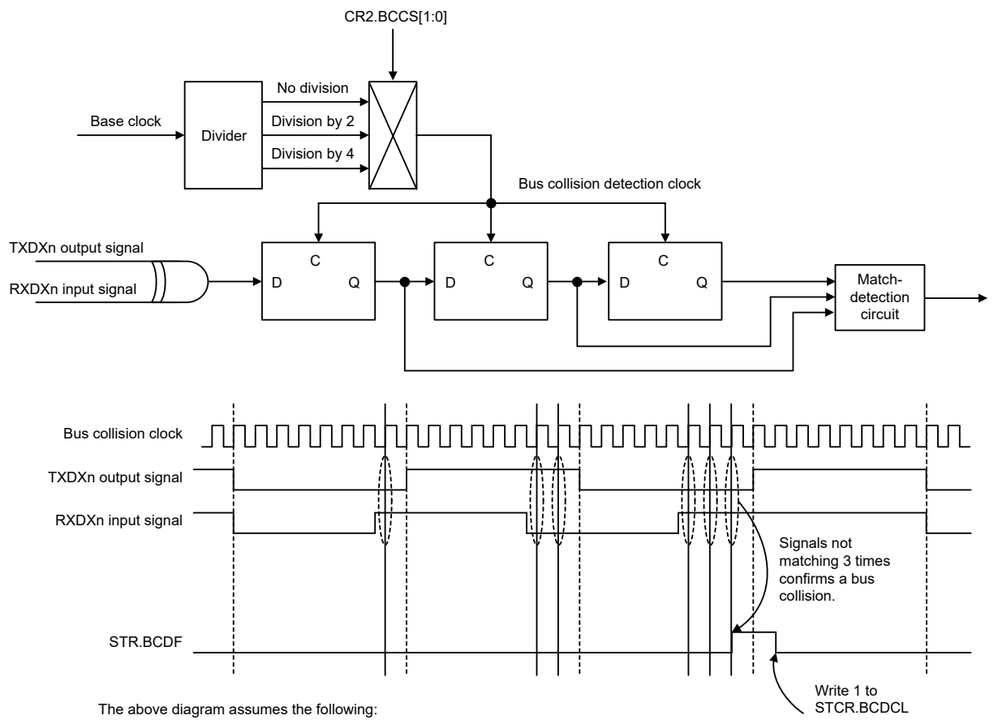
Note: n = 1, 2

图30.110CR1.PIBE位为1时接收起始帧时的操作示例

30.11.4 总线碰撞检测

总线冲突检测适用于中断字段低宽度的输出和数据传输的情况
当ESMER.ESME位和SCIn.SCI.TE位设置为1时，SCIn(n=1 2)正在进行。

图30.111显示了带有总线冲突检测的操作示例。通过TXDXn输出和通过RXDXn输入的信号以CR2.BCCS[1:0]位设置的总线冲突检测时钟作为采样时钟进行采样，如果信号不匹配三个，则STR.BCDF标志设置为1连续几次。如果ICR.BCDIE位的值为1，也会产生SCIX2中断。



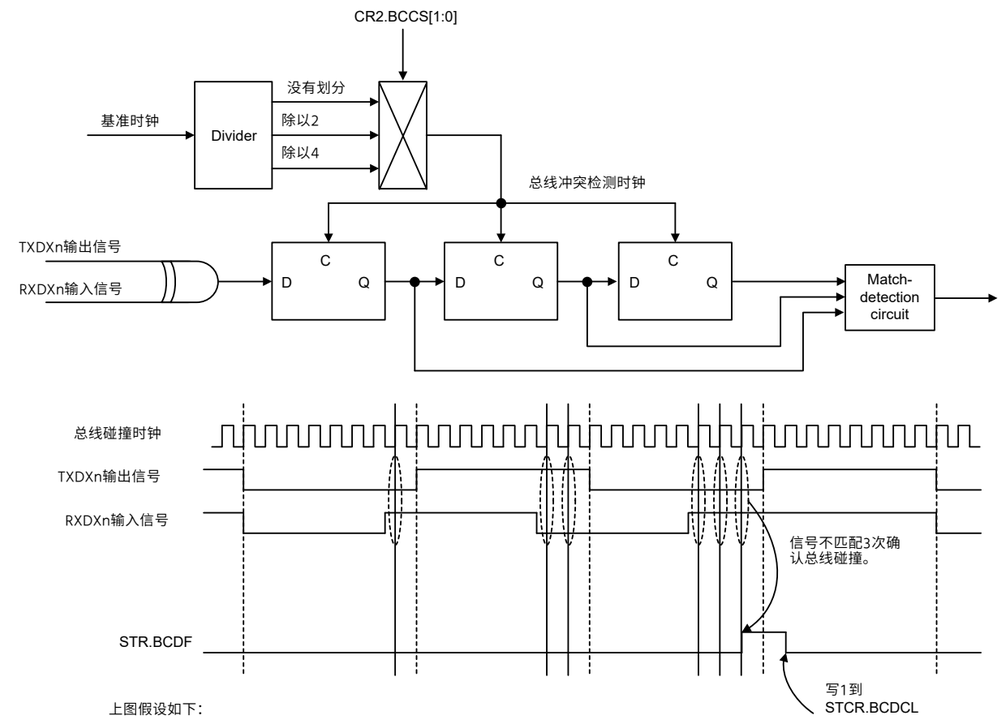
The above diagram assumes the following:
ESMER: ESME = 1
CR2: BCCS[1:0] = 01b
PCR: TXDXPS = 0, RXDXPS = 0
ICR: BCDIE = 1

Note: n = 1, 2

Figure 30.111 Example of Operations with Bus Collision Detection

30.11.5 Digital Filter for Input on the RXDXn (n = 1, 2) Pin

Signals input through the RXDXn pin can be passed through a digital filter before they are conveyed to the internal circuits. The digital filter consists of three flip-flop circuit stages connected in series and a match-detecting circuit. The CR2.DFCS[2:0] bits select the sampling clock for the RXDXn pin input signals. If the outputs of all three latches match, the given level is conveyed to subsequent circuits. If the levels do not match, the previous value is retained. In other words, levels are confirmed as being the signal if they are retained for at least three cycles of the sampling clock but judged to be noise rather than changes in the signal level if they change within three cycles of the sampling clock. Figure 30.112 shows an example of operations with the digital filter.



上图假设如下：
ESMER: ESME = 1
CR2: BCCS[1:0] = 01b
PCR: TXDXPS = 0, RXDXPS = 0
ICR: BCDIE = 1

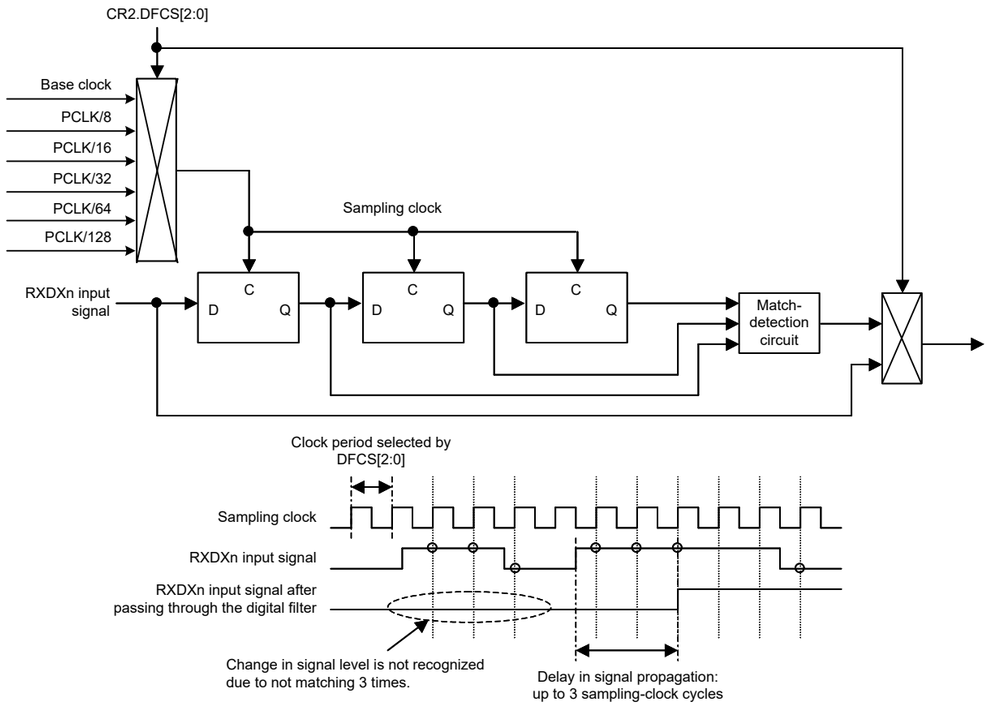
Note: n = 1, 2

图30.111带有总线冲突检测的操作示例

30.11.5 RXDXn(n=1 2)引脚上的输入数字滤波器

通过RXDXn引脚输入的信号在传送到内部电路之前可以通过数字滤波器。数字滤波器由三个串联的触发器电路级和一个匹配检测电路组成。这

CR2.DFCS[2:0]位选择RXDXn引脚输入信号的采样时钟。如果所有三个锁存器的输出都匹配，则将给定电平传送到后续电路。如果级别不匹配，则保留先前的值。换言之，如果电平在采样时钟的至少三个周期内保持，则确认电平为信号，但如果在采样时钟的三个周期内变化，则判断为噪声而不是信号电平的变化。图30.112显示了使用数字滤波器的操作示例。



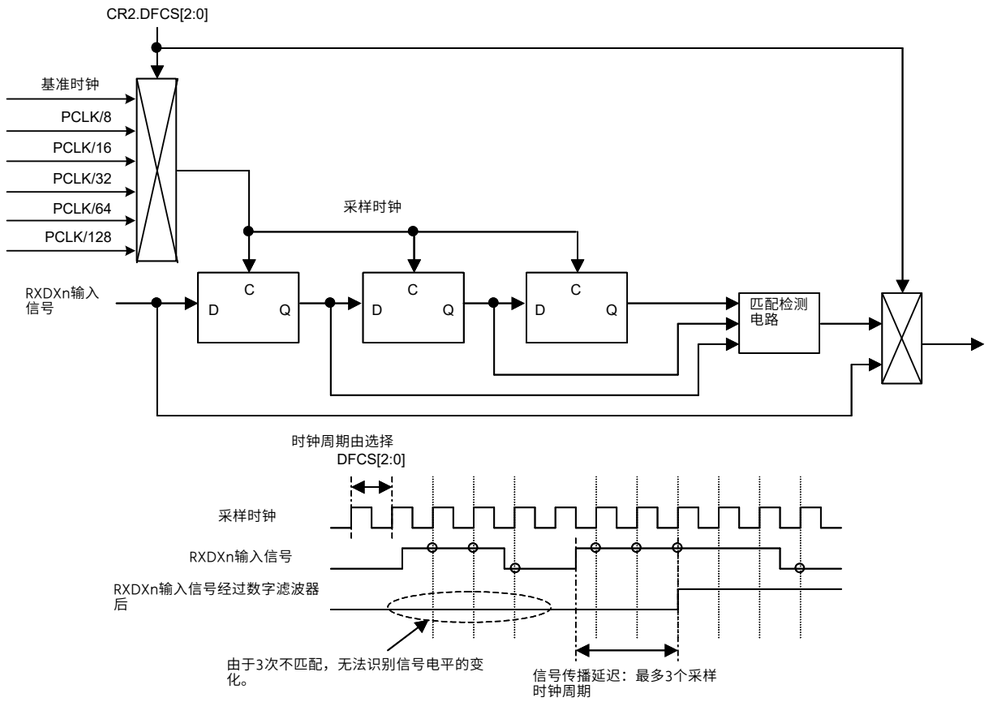
Note: n = 1, 2

Figure 30.112 Example of Operations with the Digital Filter

30.11.6 Bit Rate Measurement

The bit rate measurement function measures the intervals between rising and falling edges and between falling and rising edges of the signal input from the RXDXn (n = 1, 2) pin. Figure 30.113 shows an example of operations for bit rate measurement.

1. Writing 1 to the CR0.BRME bit enables bit rate measurement. Only set the BRME bit to 1 when you wish to proceed with bit rate measurement. Furthermore, bit rate measurement will not proceed during a Break Field, even if the BRME bit is set to 1.
2. After detection of the Break Field low width, bit rate measurement starts when the level input on the RXDXn pin becomes high.
3. Once bit rate measurement has started, counter values from the timer are retained in the read buffers on the input of valid edges from the RXDXn pin (rising and falling edges) and the counter is reloaded. An SCIX3 interrupt is also generated if the value of the ICR.AEDIE bit is 1. Retention by registers TCNT and TPRE is released by reading these registers.
4. The bit rate as calculated from the values counted during intervals between valid edges can be used for adjusting the rate by changing the settings of the SCIn. To disable the bit rate measurement after a match with Control Field 1, write 0 to the CR0.BRME bit.



Note: n = 1, 2

图30.112使用数字滤波器的操作示例

30.11.6 比特率测量

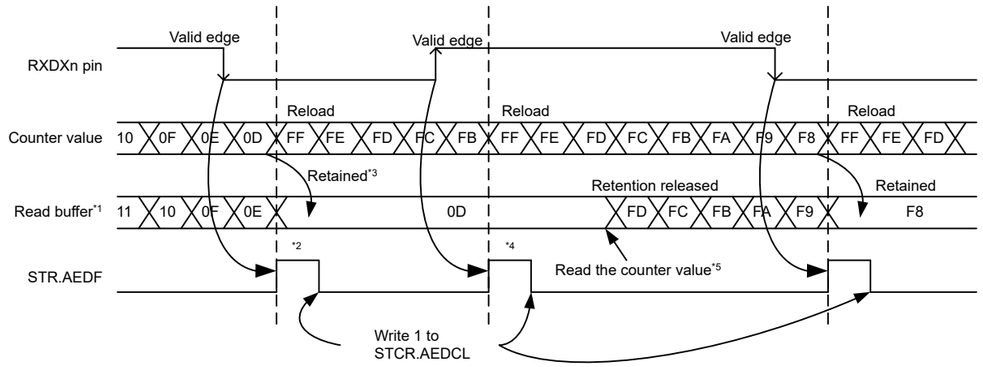
比特率测量功能测量从RXDXn(n=1 2)引脚输入的信号的上升沿和下降沿之间以及下降沿和上升沿之间的间隔。图30.113显示了比特率测量的操作示例。

1.将1写入CR0.BRME位启用比特率测量。仅当您希望继续进行比特率测量时，才将BRME位设置为1。此外，即使BRME位设置为1，在中断字段期间也不会进行比特率测量。

2.检测到BreakField低电平宽度后，当RXDXn引脚上的电平输入变为高电平时开始比特率测量。

3.一旦比特率测量开始，来自定时器的计数器值在来自RXDXn引脚的有效边沿（上升沿和下降沿）的输入上保留在读缓冲器中，并且计数器被重新加载。如果ICR.AEDIE位的值为1，也会产生SCIX3中断。寄存器TCNT和TPRE的保留通过读取这些寄存器来释放。

4.根据有效边沿之间的间隔期间计数的值计算的比特率可用于通过更改SCIn的设置来调整速率。要在与控制字段1匹配后禁用比特率测量，请将0写入CR0.BRME位。

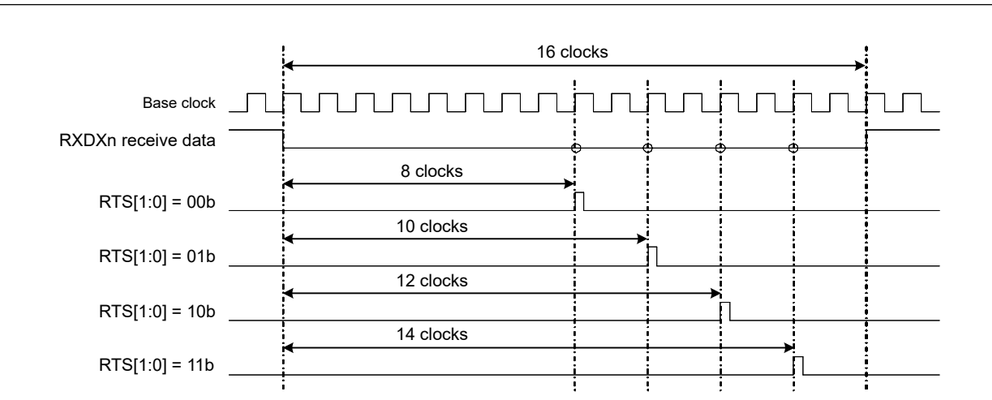


Note: n = 1, 2
Note 1. The TCNT or TPRE register indicates the contents of the read buffers.
Note 2. The STR.AEDF flag becomes 1 on detection of a valid edge.
Note 3. When an effective edge is detected, the current value of the counter is stored in the read buffer.
Note 4. The value retained in the read buffers due to one valid edge is not updated to the new value even if a further valid edge is detected.
Note 5. Retention of a value in a read buffer due to a valid edge is released by reading the TCNT or TPRE register.

Figure 30.113 Example of Operations for Bit Rate Measurement

30.11.7 Selectable Timing for Sampling Data Received through RXDXn (n = 1, 2)

The extended serial mode control section provides a way of adjusting the timing for the sampling of data received through the RXDXn pin of an SCIn by setting the CR2.RTS[1:0] bits to select the rising edges of 8th, 10th, 12th, or 14th cycle of the SCI base clock. If the value of the SEMR.ABCS bit is 1, the bits select the rising edges of 4th, 5th, 6th, or 7th cycle of the PCLK clock of the SCIn. Figure 30.114 shows timing for the sampling of data received through RXDXn.

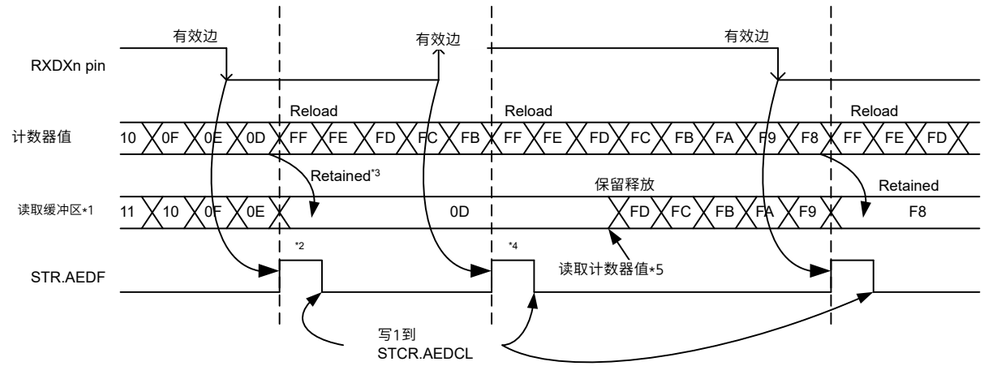


Note: n = 1, 2

Figure 30.114 Timing for Sampling of Data Received through RXDXn

30.11.8 Timer

The timer has the following operating modes.



Note: n = 1, 2
注1.TCNT或TPRE寄存器指示读取缓冲区的内容。
注2.STR.AEDF标志在检测到有效边沿时变为1。
注3.当检测到有效边沿时，计数器的当前值存储在读缓冲区中。
注4.即使检测到另一个有效边沿，由于一个有效边沿而保留在读取缓冲区中的值也不会更新为新值。

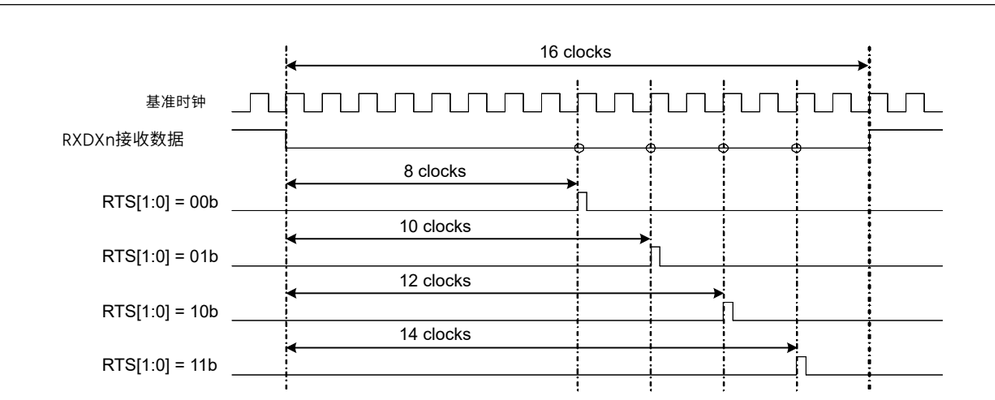
注5.通过读取TCNT或TPRE寄存器来释放由于有效边沿而在读取缓冲区中保留的值。

图30.113比特率测量操作示例

30.11.7 对通过RXDXn(n=1 2)接收的数据进行采样的可选时序

扩展串行模式控制部分通过设置CR2.RTS[1:0]位来选择第8、10、12、或SCI基本时钟的第14个周期。如果SEMR.ABCS位的值为1，则这些位选择第4、第5、第6或第7个周期的上升沿

SCIn的PCLK时钟。图30.114显示了对通过RXDXn接收的数据进行采样的时序。



Note: n = 1, 2

图30.114对通过RXDXn接收的数据进行采样的时序

30.11.8 Timer

定时器具有以下操作模式。

(1) Break Field Low Width Output Mode

This mode is for output through the TXDXn (n = 1, 2) pin of the low level over the Break Field low width at the transmission of a Start Frame. Setting the TMR.TOMS[1:0] bits to 10b switches operation to Break Field low width output mode. The TMR.TCSS[2:0] bits select the clock source for the counter. When the TCR.TCST bit is set to 1, the output on the TXDXn pin goes to the low level and counting starts. When the timer underflows, the output on the TXDXn pin goes to the high level and the STR.BFDF flag is set to 1. An SCIX0 interrupt is also generated if the value of the ICR.BFDIE bit is 1. When 0 is written to the TCR.TCST bit, counting stops after reloading of registers TPRE and TCNT. After output of the Break Field low width is completed, stop the timer before it underflows again. Figure 30.115 shows an example of operations in Break Field low width output mode.

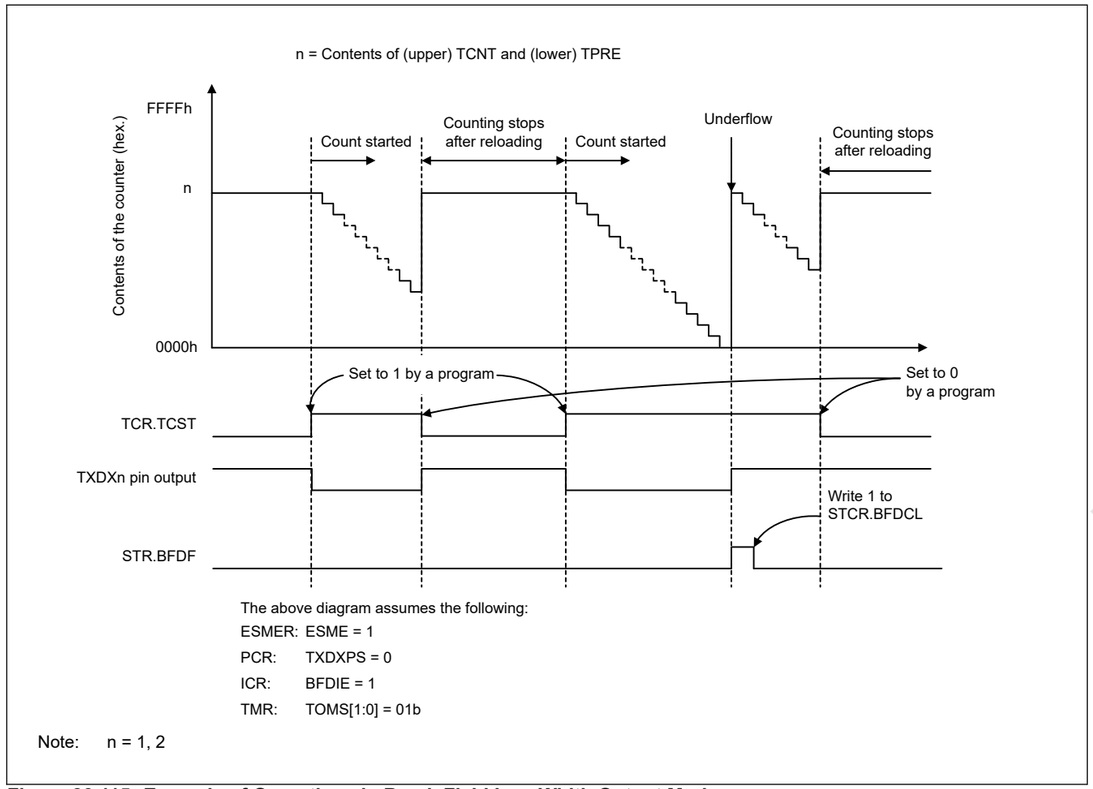


Figure 30.115 Example of Operations in Break Field Low Width Output Mode

(2) Break Field Low Width Determination Mode

This mode is for determining the Break Field low width in the input signal on the RXDXn (n = 1, 2) pin at the reception of a Start Frame. Setting the TMR.TOMS[1:0] bits to 01b switches operation to Break Field low width determination mode. The TMR.TCSS[2:0] bits select the clock source for the counter. When the TCR.TCST bit is set to 1, the interface enters the Break Field low width determinable state. Determination starts when a low level is input from the RXDXn pin. When a high level is then input on the RXDXn pin, registers TPRE and TCNT are reloaded and the interface enters the Break Field low width determinable state. When the timer underflows during Break Field low width determination, the STR.BFDF flag is set to 1. An SCIX0 interrupt is also generated if the value of the ICR.BFDIE bit is 1. If an underflow of the timer during data transfer cause a problem in the form of interrupt generation, stop the timer after Break Field low width determination. Figure 30.116 shows an example of operations in Break Field low width output mode.

(1) 断场低宽度输出模式

此模式用于在传输起始帧时通过中断字段低电平宽度上的低电平TXDXn(n=1 2)引脚输出。将TMR.TOMS[1:0]位设置为10b会将操作切换到BreakField低宽度输出模式。TMR.TCSS[2:0]位选择计数器的时钟源。当TCR.TCST位设置为1时，TXDXn引脚上的输出变为低电平并开始计数。当定时器下溢时，TXDXn引脚上的输出变为高电平，STR.BFDF标志设置为1。如果ICR.BFDIE位的值为1，也会产生SCIX0中断。当写入0时TCR.TCST位，重新加载寄存器TPRE和TCNT后计数停止。BreakField低宽度输出完成后，在定时器再次下溢之前停止定时器。图30.115显示了BreakField低宽度输出模式下的操作示例。

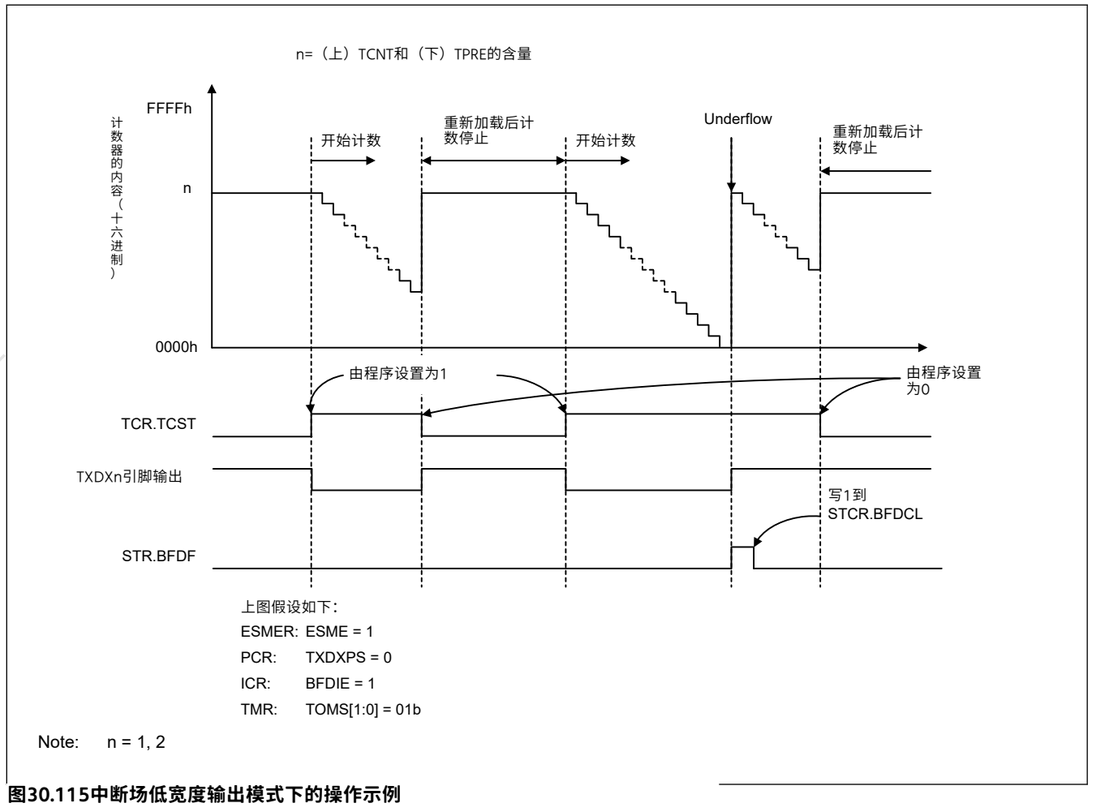
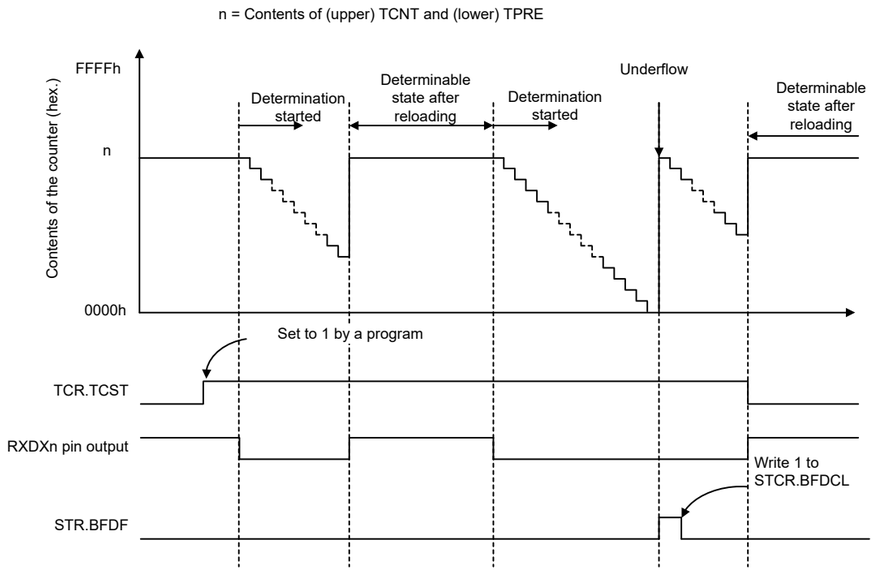


图30.115中断场低宽度输出模式下的操作示例

(2) 断场低宽度测定模式

该模式用于在接收起始帧时确定RXDXn(n=1 2)引脚上的输入信号中的中断场低电平宽度。将TMR.TOMS[1:0]位设置为01b会将操作切换到中断字段低宽度确定模式。TMR.TCSS[2:0]位选择计数器的时钟源。当TCR.TCST位设置为1时，接口进入

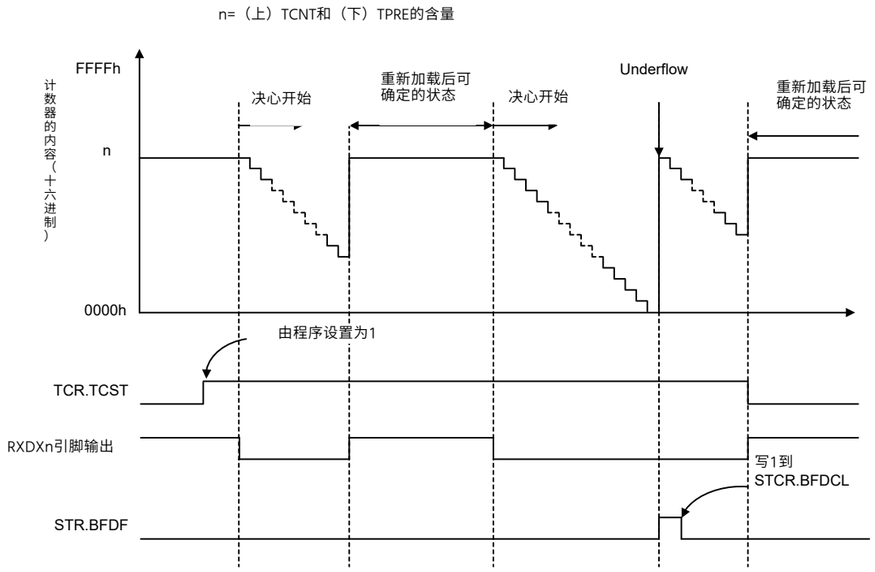
BreakField低宽度可确定状态。当从RXDXn引脚输入低电平时开始确定。当RXDXn引脚输入高电平时，寄存器TPRE和TCNT被重新加载，接口进入中断字段低宽度可确定状态。在中断字段低宽度确定期间定时器下溢时，STR.BFDF标志设置为1。如果ICR.BFDIE位的值为1，也会产生SCIX0中断。如果在数据传输期间定时器下溢导致中断产生形式的问题，在BreakField低宽度确定后停止定时器。图30.116显示了BreakField低宽度输出模式下的操作示例。



The above diagram assumes the following:
ESMER: ESME = 1
CR1: BFE = 0
PCR: RXDXPS = 0
ICR: BFDIE = 1
TMR: TOMS[1:0] = 01b

Note: n = 1, 2

Figure 30.116 Example of Operations in Break Field Low Width Determination Mode



上图假设如下：
ESMER: ESME = 1
CR1: BFE = 0
PCR: RXDXPS = 0
ICR: BFDIE = 1
TMR: TOMS[1:0] = 01b

Note: n = 1, 2

图30.116中断场低宽度确定模式下的操作示例

(3) Timer Mode

This mode is for counting cycles of the internal clock as the clock source. Setting the TMR.TOMS[1:0] bits to 00b switches operation to timer mode. The TMR.TCSS[2:0] bits select the clock source for the counter. Counting starts when 1 is written to the TCR.TCST bit and stops when 0 is written to the TCST bit. Registers TPRE and TCNT both count down. The TPRE register counts cycles of the clock source for counting, and underflows of the TPRE register provide the clock source for counting by the TCNT register. When the timer underflows, the STR.BFDF flag is set to 1. An SCIX0 interrupt is also generated if the value of the ICR.BFDIE bit is 1.

(3) 定时器模式

该模式用于计数内部时钟作为时钟源的周期。将TMR.TOMS[1:0]位设置为00b会将操作切换到定时器模式。TMR.TCSS[2:0]位选择计数器的时钟源。将1写入TCR.TCST位时开始计数，将0写入TCST位时停止计数。寄存器TPRE和TCNT都倒计时。TPRE寄存器对时钟源的周期计数进行计数，TPRE寄存器的下溢为TCNT寄存器的计数提供时钟源。当定时器下溢时，STR.BFDF标志设置为1。如果ICR.BFDIE位的值为1，也会产生SCIX0中断。

30.12 Interrupt Sources

30.12 中断源

30.12.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the ICU is 1, the ICU does not output the interrupt request but saves it internally with a capacity for retention of one request per source.

When the interrupt status flag in the ICU is set to 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

30.12.1 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择非FIFO）

如果在ICU中的中断状态标志为1时满足SCIn_TXI和SCIn_RXI中断的条件，则ICU不输出中断请求，而是将其保存在内部，每个源可以保留一个请求。

当ICU中的中断状态标志设置为0时，输出ICU中保留的中断请求。当实际中断输出时，内部保留的中断请求会被自动丢弃。清除相关中断使能位（SCRSCR_SMCI中的TIE或RIE位）也可用于丢弃内部保留的中断请求。

30.12.2 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected)

When an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the ICU is set to 0, and if the conditions for an SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

30.12.2 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择FIFO）

当ICU中的中断状态标志设置为1时，SCIn_TXI和SCIn_RXI中断不会向ICU输出中断请求。当ICU的中断状态标志设置为0，并且满足SCIn_TXI和SCIn_RXI中断的条件时，将产生中断请求。

30.12.3 Interrupts in Asynchronous, Manchester, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

Table 30.42 lists interrupt sources in asynchronous mode, Manchester mode, clock synchronous mode, and simple SPI mode.

A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the enable bits in the SCR register.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR or TDRHL register*1 to the TSR register. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TE and SCR.TIE bits to 1 at the same time. An SCIn_TXI interrupt request can activate the DTC or DMAC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting the SCR.TE bit to 1 when SCR.TIE is 0 or by setting the SCR.TIE bit to 1 when the SCR.TE is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and SCR.TEIE is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated. Additionally, when SCR.TE is 1, the SSR.TEND flag retains the value 1 until more transmit data is written to the TDR or TDRHL register*1, and setting SCR.TEIE to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR register. An SCIn_RXI interrupt request can activate the DTC or DMAC to handle data transfer.

Setting any of the SSR.ORER, FER, PER and MER*3 flags to 1 when the SCR.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request.

An SCIn_RXI interrupt request is not generated in this case. Clearing all these flags (ORER, FER, PER, MER*3, SYER*3, PFER*3 and SBER*3) leads to discarding of the SCIn_ERI interrupt request.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the SCR.TIE bit. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.
Note 3. MER, SYER, PFER, and SBER work as a factor of SCIn_ERI interrupt only in Manchester mode. SYER, PFER, and SBER also only work if its enable bits (SYEREN, PFEREN, SBEREN in MECR) are set to "1".

(2) FIFO selected

Table 30.43 lists interrupt sources in FIFO selected mode.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when the stored amount of data in the FTDRL register becomes the threshold value indicated in FCR.TTRG or below. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TIE and SCR.TE bits to 1 simultaneously or by setting SCR.TIE to 1 when SCR.TE is 1.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 when SCR.TIE is 0.

If SCR.TEIE is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmit data is sent, the SSR_FIFO.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If SCR.RIE is 1, the SCIn_RXI interrupt request is generated when the stored amount of data in the FRDRL register is equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the SCR.RIE bit is 1, when the SSR_FIFO.ORER flag is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, the SCIn_ERI interrupt request is generated. When the amount of data stored in the FRDRL register is at the threshold value or above, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case SSR_FIFO.ORER, FER, and PER flags are all cleared.

30.12.3 异步、曼彻斯特、时钟同步和简单SPI中的中断 Modes

(1) Non-FIFO selected

表30.42列出了异步模式、曼彻斯特模式、时钟同步模式和简单SPI模式下的中断源。

可以为每个中断源分配不同的中断向量。可以使用SCR寄存器中的启用位启用或禁用各个中断源。

如果SCR.TIE位为1，则当发送数据从TDR传输或
TDRHL寄存器*1到TSR寄存器。也可以使用一条指令同时将SCR.TE和SCR.TIE位设置为1，从而产生SCIn_TXI中断请求。SCIn_TXI中断请求可以激活DTC或DMAC来处理数据传输。

当SCR.TIE为0时将SCR.TE位设置为1或通过设置
当SCR.TE为1时，SCR.TIE位为1。*2

当当前发送数据的最后一位发送时尚未写入新数据且SCR.TEIE为1，则
SSR.TEND标志设置为1并产生SCIn_TEI中断请求。此外，当SCR.TE为1时，SSR.TEND标志保持值1，直到更多的发送数据写入TDR或TDRHL寄存器*1，并且将SCR.TEIE设置为1会导致产生SCIn_TEI中断请求。

将数据写入TDR或TDRHL寄存器*1会导致SSR.TEND标志清零，并在一定时间后丢弃SCIn_TEI中断请求。

如果SCR.RIE位为1，则当接收到的数据存储在RDR寄存器中时会产生SCIn_RXI中断请求。一个
SCIn_RXI中断请求可以激活DTC或DMAC来处理数据传输。

当SCR.RIE位为1时，将任何SSR.ORER、FER、PER和MER*3标志设置为1会导致生成
SCIn_ERI中断请求。

在这种情况下不会产生SCIn_RXI中断请求。清除所有这些标志(ORER FER PER MER*3 SYER*3
PFER*3和SBER*3)导致丢弃SCIn_ERI中断请求。

注意1.选择异步模式和9位数据长度时。
注2.为了在新一轮传输开始时，在传输最后一个数据时暂时禁止SCIn_TXI中断，在处理完传输完成中断后，使用ICU中的中断请求使能位控制中断的激活而不是使用SCR.TIE位。这种方法可以防止在传输新数据时抑制SCIn_TXI中断请求。

注3.MER、SYER、PFER和SBER仅在曼彻斯特模式下作为SCIn_ERI中断的一个因素起作用。SYER、PFER和
SBER也仅在其启用位（MECR中的SYEREN、PFEREN、SBEREN）设置为“1”时才起作用。

(2) FIFO selected

表30.43列出了FIFO选择模式下的中断源。

如果SCR.TIE位为1，当FTDRL寄存器中存储的数据量变为FCR.TTRG中指示的阈值或更低时，将产生SCIn_TXI中断请求。SCIn_TXI中断请求也可以通过使用一条指令同时将SCR.TIE和SCR.TE位设置为1或在SCR.TE为1时将SCR.TIE设置为1来生成。

当SCR.TIE为0时，将SCR.TE设置为1不会产生SCIn_TXI中断请求。

如果SCR.TEIE为1，并且在发送数据的最后一位时下一个数据未写入FTDRL寄存器，则SSR_FIFO.TEND标志设置为1，并产生SCIn_TEI中断请求。

如果SCR.RIE为1，则当FRDRL寄存器中存储的数据量等于或大于FCR.RTRG中指示的阈值时，将产生SCIn_RXI中断请求。当RTRG为0时，即使接收FIFO中的数据量等于0，也不会发生SCIn_RXI中断。

如果SCR.RIE位为1，当SSR_FIFO.ORER标志设置为1或帧错误或奇偶校验错误的数据存储在FRDRL寄存器中时，将产生SCIn_ERI中断请求。当FRDRL寄存器中存储的数据量在阈值或以上时，也会产生SCIn_RXI中断请求。SCIn_ERI中断请求可以被取消，在这种情况下SSR_FIFO.ORER、FER和PER标志都被清除。

Table 30.42 SCI interrupt sources with non-FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0 to 9)	Receive error*1	SSR.ORER, SSR.FER, SSR.PER, DCCR.DFER, DCCR.DPER, (SSR.MER, MESR.SYER, MESR.PFER, MESR.SBER)*2	SCR.RIE	Not possible
SCIn_RXI (n = 0 to 9)	Receive data full	SSR.RDRF	SCR.RIE	Possible
	Address match	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0, 3 to 9)	Address match	DCCR.DCMF	—	Not possible
SCIn_TXI (n = 0 to 9)	Transmit data empty	SSR.TDRE	SCR.TIE	Possible
SCIn_TEI (n = 0 to 9)	Transmit end	SSR.TEND	SCR.TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.
Note 2. MER, SYER, PFER, and SBER work as a factor of ERI interrupt only in Manchester mode. SYER, PFER, and SBER also only work if its enable bits (SYEREN, PFEREN, SBEREN in MECR) are set to 1.

Table 30.43 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0 to 9)	Receive error*1	SSR_FIFO.ORER, SSR_FIFO.FER, SSR_FIFO.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	Not possible
		SSR_FIFO.DR (when FCR.DRES = 1)	SCR.RIE	Not possible
SCIn_RXI (n = 0 to 9)	Receive data full	SSR_FIFO.RDF	SCR.RIE	Possible
	Receive data ready	SSR_FIFO.DR (when FCR.DRES = 0)	SCR.RIE	Possible
	Address match	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0, 3 to 9)	Address match	DCCR.DCMF	—	Not possible
SCIn_TXI (n = 0 to 9)	Transmit data empty	SSR_FIFO.TDFE	SCR.TIE	Possible
SCIn_TEI (n = 0 to 9)	Transmit end	SSR_FIFO.TEND	SCR.TEIE	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.

30.12.4 Interrupts in Smart Card Interface Mode

Table 30.44 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 30.44 SCI Interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_ERI (n = 0 to 9)	Receive error or error signal detection	SSR_SMCI.ORER, SSR_SMCI.PER, SSR_SMCI.ERS	SCR_SMCI.RIE	Not possible
SCIn_RXI (n = 0 to 9)	Receive data full	SSR_SMCI.RDRF	SCR_SMCI.RIE	Possible
SCIn_TXI (n = 0 to 9)	Transmit data empty	SSR_SMCI.TEND	SCR_SMCI.TIE	Possible

Data transmission or reception using the DTC or DMAC is also possible in smart card interface mode, similar to normal SCI mode. In transmission, when the SSR_SMCI.TEND flag is set to 1, an SCIn_TXI interrupt request is generated. This

Table 30.42 选择了非FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_ERI (n = 0 to 9)	接收错误*1	SSR.ORER, SSR.FER, SSR.PER, DCCR.DFER, DCCR.DPER, (SSR.MER, MESR.SYER, MESR.PFER, MESR.SBER)*2	SCR.RIE	不可能
SCIn_RXI (n = 0 to 9)	接收数据已满	SSR.RDRF	SCR.RIE	Possible
	地址匹配	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0, 3 to 9)	地址匹配	DCCR.DCMF	—	不可能
SCIn_TXI (n = 0 to 9)	传输数据为空	SSR.TDRE	SCR.TIE	Possible
SCIn_TEI (n = 0 to 9)	发射端	SSR.TEND	SCR.TEIE	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。
注2.MER、SYER、PFER和SBER仅在曼彻斯特模式下作为ERI中断的一个因素起作用。SYER、PFER和SBER也仅在其启用位（MECR中的SYEREN、PFEREN、SBEREN）设置为1时才起作用。

Table 30.43 选择了FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_ERI (n = 0 to 9)	接收错误*1	SSR_FIFO.ORER, SSR_FIFO.FER, SSR_FIFO.PER, DCCR.DFER, DCCR.DPER	SCR.RIE	不可能
		SSR_FIFO.DR (when FCR.DRES = 1)	SCR.RIE	不可能
SCIn_RXI (n = 0 to 9)	接收数据已满	SSR_FIFO.RDF	SCR.RIE	Possible
	接收数据就绪	SSR_FIFO.DR (when FCR.DRES = 0)	SCR.RIE	Possible
	地址匹配	DCCR.DCMF	SCR.RIE	Possible
SCIn_AM (n = 0, 3 to 9)	地址匹配	DCCR.DCMF	—	不可能
SCIn_TXI (n = 0 to 9)	传输数据为空	SSR_FIFO.TDFE	SCR.TIE	Possible
SCIn_TEI (n = 0 to 9)	发射端	SSR_FIFO.TEND	SCR.TEIE	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

30.12.4 智能卡接口模式中的中断

表30.44列出了智能卡接口模式下的中断源。在此模式下不能使用发送结束中断(SCIn_TEI)请求和地址匹配(SCIn_AM)请求。

Table 30.44 SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_ERI (n = 0 to 9)	接收错误或错误信号检测	SSR_SMCI.ORER, SSR_SMCI.PER, SSR_SMCI.ERS	SCR_SMCI.RIE	不可能
SCIn_RXI (n = 0 to 9)	接收数据已满	SSR_SMCI.RDRF	SCR_SMCI.RIE	Possible
SCIn_TXI (n = 0 to 9)	传输数据为空	SSR_SMCI.TEND	SCR_SMCI.TIE	Possible

在智能卡接口模式下也可以使用DTC或DMAC进行数据传输或接收，类似于正常SCI模式。在发送过程中，当SSR_SMCI.TEND标志设置为1时，会产生一个SCIn_TXI中断请求。这个

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SCIn_TXI interrupt request activates the DTC or DMAC, allowing transfer of transmit data if the SCIn_TXI request is previously specified as a source of DTC or DMAC activation. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission after an error occurrence. However, the SSR_SMCI.ERS flag is not automatically set to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the SCR_SMCI.RIE bit to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings. For DTC or DMAC settings, see section 17, Data Transfer Controller (DTC), section 16, DMA Controller (DMAC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to the RDR register. This SCIn_RXI interrupt request activates the DTC or DMAC, allowing transfer of the receive data if the SCIn_RXI request is previously specified as a source of DTC or DMAC activation. If an error occurs, the error flag is set. Therefore, the DTC or DMAC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

30.12.5 Interrupts in Simple IIC Mode

Table 30.45 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DTC or DMAC can also be used to handle transfer in simple IIC mode.

When the SIMR2.IICINTM bit is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 9th bit. If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DTC or DMAC, the SCIn_TXI request activates the DTC or DMAC to handle transfer of the transmit data.

When the SIMR2.IICINTM bit is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.

If the DTC or DMAC is used for data transfer in reception or transmission, always set up and enable the DTC or DMAC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 30.45 SCI interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC or DMAC activation
SCIn_RXI (n = 0 to 9)	Reception, ACK detection	—	SCMR.RIE	Possible*1
SCIn_TXI (n = 0 to 9)	Transmission, NACK detection	—	SCMR.TIE	Possible
SCIn_TEI(STIn) (n = 0 to 9)	Completion of generation of a start, restart, or stop condition	SIMR3.IICSTIF	SCMR.TEIE	Not possible

Note 1. Activation of the DTC or DMAC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts)

SCIn_TXI中断请求激活DTC或DMAC，如果之前将SCIn_TXI请求指定为DTC或DMAC激活源，则允许传输数据。当DTC或DMAC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在重传期间，TEND标志保持为0，并且DTC或DMAC不被激活。因此，SCI和DTC或DMAC会自动传输指定的字节数，包括发生错误后的重传。但是，发生错误时，SSR_SMCI.ERS标志不会自动设置为0。因此，必须通过预先将SCR_SMCI.RIE位设置为1来清除ERS 标志，以在发生错误时启用SCIn_ERI中断请求。

使用DTC或DMAC发送或接收数据时，请务必在进行SCI设置之前启用DTC或DMAC。对于DTC或DMAC设置，请参阅第17节，数据传输控制器(DTC)，第16节，DMA控制器(DMAC)。

在接收中，当接收数据设置到RDR寄存器时，会产生SCIn_RXI中断请求。该SCIn_RXI中断请求激活DTC或DMAC，如果先前将SCIn_RXI请求指定为DTC或DMAC激活源，则允许传输接收数据。如果发生错误，则设置错误标志。因此，不会激活DTC或DMAC，而是向CPU发出SCIn_ERI中断请求。必须清除错误标志。

30.12.5 简单IIC模式下的中断

表30.45列出了简单IIC模式下的中断源。STI中断分配给发送结束中断(SCIn_TEI)请求。不能使用接收错误中断(SCIn_ERI)和地址匹配(SCIn_AM)请求。

DTC或DMAC也可用于处理简单IIC模式下的传输。

当SIMR2.IICINTM位为1时：

●SCIn_RXI请求在第8位的SCLn信号下降沿产生。如果SCIn_RXI先前设置为DTC或DMAC的激活源，则SCIn_RXI请求将激活DTC或DMAC以处理接收数据的传输。

●SCIn_TXI请求在第9位（确认位）的SCLn信号的下降沿产生。如果SCIn_TXI先前设置为DTC或DMAC的激活源，则SCIn_TXI请求将激活DTC或DMAC以处理传输数据的传输。

当SIMR2.IICINTM位为0时：

●如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿为低电平，则生成SCIn_RXI请求（ACK检测）

●如果SDAn引脚上的输入在第9位（确认位）的SCLn信号的上升沿为高电平，则生成SCIn_TXI请求（NACK检测）

●如果先前将SCIn_RXI设置为DTC或DMAC的激活源，则SCIn_RXI请求将激活DTC或DMAC以处理接收数据的传输。

如果DTC或DMAC用于接收或传输中的数据传输，请务必在设置SCI之前设置并启用DTC或DMAC。

当SIMR3中的IICSTAREQ、IICRSTAREQ和IICSTPREQ位用于生成开始条件、重新启动条件或停止条件时，生成完成时会发出STI请求。

Table 30.45 SCI中断源

Name	中断源	中断标志	中断使能	DTC或DMAC激活
SCIn_RXI (n = 0 to 9)	接收、ACK检测	—	SCMR.RIE	Possible*1
SCIn_TXI (n = 0 to 9)	传输、NACK检测	—	SCMR.TIE	Possible
SCIn_TEI(STIn) (n = 0 to 9)	完成启动、重新启动或停止条件的生成	SIMR3.IICSTIF	SCMR.TEIE	不可能

注1.仅当SIMR2.IICINTM位为1时才可能激活DTC或DMAC（使用接收和发送中断）

30.12.6 Interrupt Requests from the Extended Serial Mode Control Section

The extended serial mode control section has a total of six types of interrupt request for generating the SCIX0 interrupt (Break Field low width detected), SCIX1 interrupt (Control Field 0 match, Control Field 1 match, priority interrupt bit detected), SCIX2 interrupt (bus collision detected), and SCIX3 interrupt (valid edge detected). When any of the interrupt factors is generated, the corresponding status flag is set to 1. Details of all of the interrupt requests are listed in Table 30.46.

Table 30.46 Interrupt Sources of the Extended Serial Mode Control Section

Interrupt Request	Status Flag	Interrupt Factors
SCIX0 interrupt (Break Field low width detected)	BFDF	• Detection of a Break Field low width longer than the interval corresponding to the timer setting • Completion of the output of a Break Field low width over the interval corresponding to the timer setting • Underflow of the timer
SCIX1 interrupt (Control Field 0 match)	CF0MF	The data received in Control Field 0 matching the value set in CF0DR
SCIX1 interrupt (Control Field 1 match)	CF1MF	The data received in Control Field 1 matching the value set in PCF1DR or SCF1DR
SCIX1 interrupt (priority interrupt bit detected)	PIBDF	The value of the bit specified as the priority interrupt bit matching the value set in PCF1DR
SCIX2 interrupt (bus collision detected)	BCDF	The output level on the RXDXn (n = 1, 2) pin and the input level on the RXDXn pin not matching on three consecutive cycles of the bus collision detection clock
SCIX3 interrupt (valid edge detected)	AEDF	Detection of a valid edge during bit rate measurement

30.13 Event Linking

By using interrupt request signals as event signals, the SCIn can provide linked operation through the ELC for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected) (SCIn_ERI, n = 0 to 9)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- The SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is set in a reception FIFO buffer, and it indicates that 15 ETUs elapse when FIFO is selected and the FCR.DRES bit is 1

(2) Receive data full event output (SCIn_RXI, n = 0 to 9)

- Indicates that ACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode
- When the SIMR2.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used

Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR or RDRHL).

FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output (SCIn_TXI, n = 0 to 9)

- Indicates that the SCR/SCR_SMCI.TE bit is changed from 0 to 1

30.12.6 来自扩展串行模式控制部分的中断请求

扩展串行模式控制部分共有六种中断请求，用于产生SCIX0中断（BreakFieldlowwidthdetected）、SCIX1中断（ControlField0match、ControlField1match、优先级中断位检测）、SCIX2中断（检测到总线冲突）和SCIX3中断（检测到有效边沿）。当产生任何中断因素时，相应的状态标志设置为1。所有中断请求的详细信息如表30.46所示。

Table 30.46 扩展串行模式控制部分的中断源

中断请求	状态标志	中断因素
SCIX0中断（检测到断场低宽度）	BFDF	• 检测到比定时器设置对应的间隔长的中断字段低宽度 • 在与定时器设置对应的时间间隔内完成中断字段低宽度的输出 • 定时器下溢
SCIX1中断（控制字段0匹配）	CF0MF	在控制字段0中接收到的数据与设置的值匹配CF0DR
SCIX1中断（控制字段1匹配）	CF1MF	控制字段1中接收的数据与设置的值匹配PCF1DR or SCF1DR
SCIX1中断（检测到优先中断位）	PIBDF	指定为优先级中断位的位的值与PCF1DR中设置的值匹配
SCIX2中断（检测到总线冲突）	BCDF	RXDXn(n=1 2)引脚上的输出电平和RXDXn引脚上的输入电平在总线冲突检测时钟的三个连续周期上不匹配
SCIX3中断（检测到有效边沿）	AEDF	在比特率测量期间检测有效边沿

30.13 事件链接

通过使用中断请求信号作为事件信号，SCIn可以通过ELC为预先选择的模块提供联动操作。

无论相关中断请求使能位的值如何，都可以输出事件信号。

(1) 错误事件输出（接收错误或检测到错误信号）（SCIn_ERI，n=0到9）

●表示异步模式接收时奇偶校验错误导致异常终止

●表示异步模式接收时因帧错误而异常终止

●表示接收过程中由于溢出错误而异常终止

●指示在智能卡接口模式下传输过程中检测到错误信号

●ssr_fifo.fer和每个标志为0，并且接收数据少于接收FIFO缓冲区中的接收FIFO数据触发号码，它表明选择FIFO时15EtusEplapsenefefifo被选择，而FCR.DRES位置为1

(2) 接收数据满事件输出(SCIn_RXI n=0to9)

●简单IIC模式下SIMR2.IICINTM位为0表示检测到ACK

●如果SIMR2.IICINTM位在simpleIIC模式下为1，则表示检测到第8位SCLn下降沿

●当SIMR2.IICINTM位在simpleIIC模式下主机发送期间为1时，设置ELC以便不使用接收数据满事件

Non-FIFO selected

●表示接收数据设置在接收数据寄存器（RDR或RDRHL）中。

FIFO selected

●禁止使用该事件输出。

(3) 发送数据空事件输出(SCIn_TXI n=0to9)

●表示SCRSCR_SMCI.TE位由0变为1

- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode

Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output (SCIn_TEI, n = 0 to 9)

- Indicates the completion of transmission
- Indicates that the starting condition, resumption condition, or termination condition is generated in simple IIC mode

Note: When FIFO is selected, using this event output is prohibited

(5) Address match event output (SCIn_AM, n = 0, 3 to 9)

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode.

30.14 Address Non-match Event Output (SCI0_DCUF)

SCI0_DCUF indicates the non-match of comparison data (CDR.CMPD) with receive data that is one frame of the data that is received when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for Snooze end request only. In detail, see section 10, Low Power Modes.

30.15 Noise Cancellation Function

Figure 30.117 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2- stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

In Asynchronous mode, the noise cancellation function can be applied to the receive signal input to the RXDn pin. The receive level of the RXDn is taken in the flip-flop circuit of the noise filter on the base clock of asynchronous mode.

- When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 of a 1-bit period.
- When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 of a 1-bit period.
- When SEMR.ABCSE = 1, the cycle is 1/6 of a 1-bit period.

In simple IIC mode, this function can be used for each input on SDAn and SCLn. The sampling clock is selected from divided clock of baud rate generator settings SNFR.NFCS[2:0].

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is conveyed as an internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive sampling cycles.

●表示在智能卡接口模式下传输完成

●SIMR2.IICINTM位在simpleIIC模式下为0表示检测到NACK

●如果SIMR2.IICINTM位在simpleIIC模式下为1，则表示检测到第9位SCLn下降沿

Non-FIFO selected

●表示发送数据从发送数据寄存器（TDR或TDRHL）传送到发送移位寄存器（TSR）。

FIFO selected

●禁止使用该事件输出。

(4) 发送结束事件输出（SCIn_TEI，n=0到9）

●表示传输完成

●表示在简单IIC模式下产生启动条件、恢复条件或终止条件

Note: 选择FIFO时，禁止使用该事件输出

(5) 地址匹配事件输出(SCIn_AM n=0 3to9)

●在异步模式下，包括多处理器模式，当DCCR.DCME置1时，表示比较数据（CDR.CMPD）与一帧接收数据匹配。

30.14 地址不匹配事件输出(SCI0_DCUF)

SCI0_DCUF表示比较数据(CDR.CMPD)与接收数据不匹配，接收数据是在异步模式（包括多处理器模式）下DCCR.DCME设置为1时接收到的数据的一帧。此事件仅可用于贪睡结束请求。详细信息，请参见第10节，低功耗模式

30.15 降噪功能

图30.117显示了用于噪声消除的噪声滤波器的配置。噪声滤波器由一个2级触发器电路和一个匹配检测电路组成。当噪声滤波器的输入信号和2级触发器电路的输出信号完全匹配时，匹配的电平作为内部信号传送。除非另有匹配，否则将保留先前的值。当相同电平在噪声滤波器的采样时钟上保持3个周期或更长时间时，它被认为是有效的接收信号。3个周期或更短的脉冲变化被认为是噪声，而不是接收信号。

在异步模式下，可以对输入到RXDn引脚的接收信号应用噪声消除功能。RXDn的接收电平是在异步模式的基本时钟上的噪声滤波器的触发器电路中获取的。

●当SEMR.ABCS=0且SEMR.ABCSE=0时，周期为1位周期的116。

●当SEMR.ABCS=1且SEMR.ABCSE=0时，周期为1位周期的18。

●当SEMR.ABCSE=1时，周期为1位周期的16。

在简单IIC模式下，该功能可用于SDAn和SCLn上的每个输入。采样时钟从波特率发生器设置SNFR.NFCS[2:0]的分频时钟中选择。

如果在启用噪声滤波器的情况下基准时钟停止一次，然后再次重新启动基准时钟输入，则噪声滤波器操作将从时钟停止的状态恢复。当SCR.TE和SCR.RE在基本时钟输入期间设置为0时，所有噪声滤波器触发器值都被初始化为1。因此，如果在接收操作恢复时输入数据为1，则该函数确定一个电平检测到匹配并将结果作为内部信号传送。当输入的电平对应于0时，保留噪声滤波器的初始输出，直到电平在三个连续的采样周期中匹配。

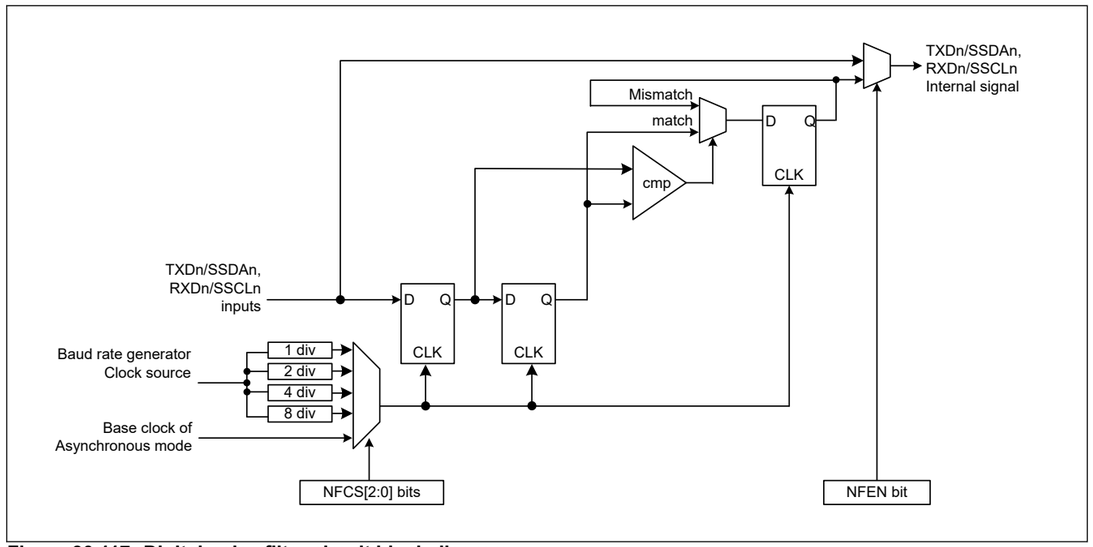


Figure 30.117 Digital noise filter circuit block diagram

30.16 Usage Notes

30.16.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

30.16.2 SCI Operation during Low Power State

(1) Transmission

When setting the module to the stopped state or in transitions to Software Standby, stop operations (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting I/O port as an SCI connection, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register and the TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected, and the value is retained, with FIFO selected. Depending on the port settings and SPTR register settings, output pins might output the level before a transition to the low-power state is made after release from the module-stopped state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

To transmit data in the same transmission mode after cancellation of the low-power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

To transmit data with a different transmission mode, initialize the SCI first.

Figure 30.118 shows an example flow of transition to Software Standby mode during transmission. Figure 30.119 and Figure 30.120 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or making a transition to Software Standby mode from the transmission mode using DTC or DMAC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC or DMAC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC or DMAC.

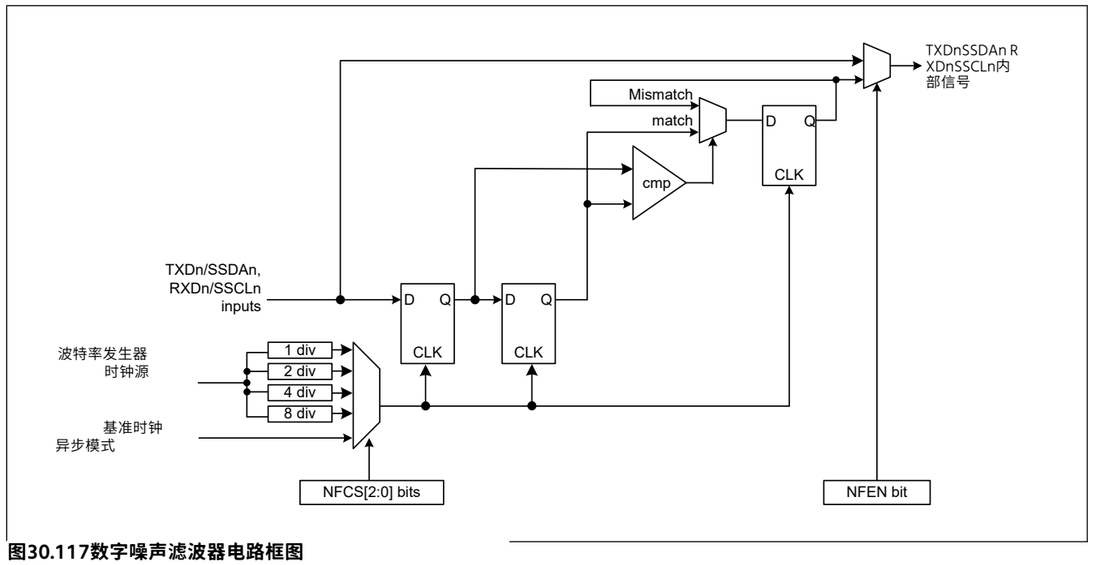


图30.117数字噪声滤波器电路框图

30.16 使用说明

30.16.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SCI操作。SCI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

30.16.2 低功耗状态下的SCI操作

(1) Transmission

当将模块设置为停止状态或转换为软件待机时，在将TXDn引脚切换为通用IO端口引脚功能后停止操作（通过将SCRSCR_SMCI中的TIE、TE和TEIE位设置为0）。当设置IO端口为SCI连接时，SPTR寄存器可以控制TXDn引脚的状态。将TE位设置为0初始化TSR寄存器，并且SSRSSR_SMCI中的TEND位在选择非FIFO时初始化为1，而在选择FIFO时保持该值。根据端口设置和SPTR寄存器设置，输出引脚可能会在从模块停止状态或软件待机模式释放后转换到低功耗状态之前输出电平。在传输过程中转换到这些状态时，传输的数据变得不确定。

在取消低功耗状态后以相同的传输模式传输数据：

1.将TE位设置为1。

2. Read SSR/SSR_FIFO/SSR_SMCI.

3.将数据依次写入TDR，开始数据传输。

要以不同的传输模式传输数据，请先初始化SCI。

图30.118显示了传输期间转换到软件待机模式的示例流程。图30.119和
图30.120显示了转换到软件待机模式期间的端口引脚状态。

在指定模块停止状态或从传输模式转换到软件待机模式之前，使用
DTC或DMAC传输，停止传输操作(TE=0)。要在取消后使用DTC或
DMAC，将TE位设置为1。SCIn_TXI中断标志 设置为1，并使用DTC或DMAC开始传输。

(2) Reception

When address match function is not used as wake-up condition

Before specifying the module-stop state or making a transition to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the received data is invalid.

Figure 30.121 shows an example flow of transition to Software Standby mode during reception.

When address match function is used as wake-up condition

Before specifying the module-stop state or making a transition to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When SCI transfers to low power mode, if the receive data pin (RXD) is at the low level, set SEMR.RXDESEL = 0.

When setting SEMR.RXDESEL = 1, there is a possibility that a start bit (falling edge of RXD pin) cannot be detected on release of the low power mode.

Figure 30.122 shows an example flow of transition to Software Standby mode during reception with address match.

When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions apply, including maximum bit rates. For details, see section 10, Low Power Modes.

(2) Reception

地址匹配功能不用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前，停止接收操作（SCRSCR_SMCI中的RE=0）。如果在数据接收期间进行转换，则接收到的数据无效。

图30.121显示了接收期间转换到软件待机模式的示例流程。

当地址匹配功能用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前：

1.设置取消低功耗状态后的操作。

2.将CDR.CMPD和DCCR.DCME设置为1。

3.设置接收操作（在SCRSCR_SMCI中RE=1）。

4.设置模块停止状态或软件待机模式。

当SCI转移到低功耗模式时，如果接收数据引脚(RXD)为低电平，则设置SEMR.RXDESEL=0。

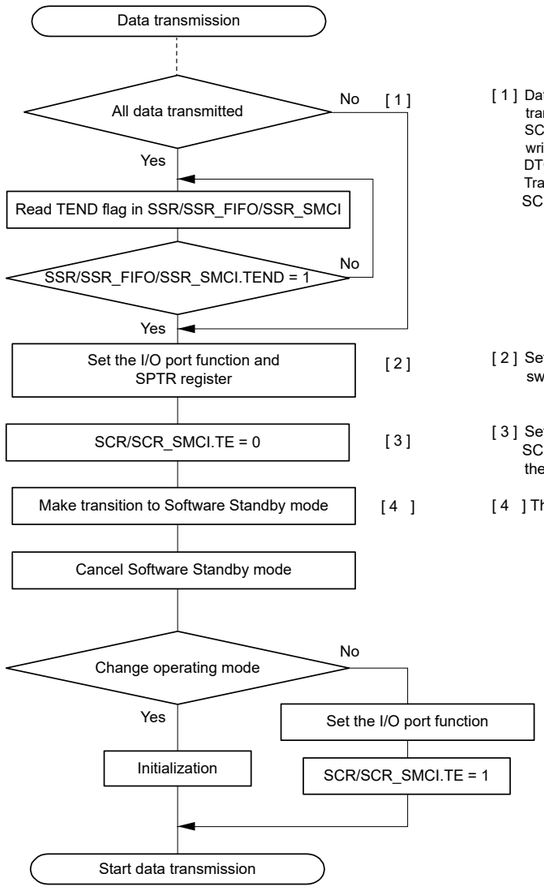
当设置SEMR.RXDESEL=1时，有可能在解除低功耗模式时无法检测到起始位（RXD引脚的下降沿）。

图30.122显示了在地址匹配的接收期间转换到软件待机模式的示例流程。

在贪睡模式下使用SCI0时

在贪睡模式下使用SCI0时，有一些限制，包括最大比特率。有关详细信息，请参阅第10节，低电源模式。

RA生态工作室



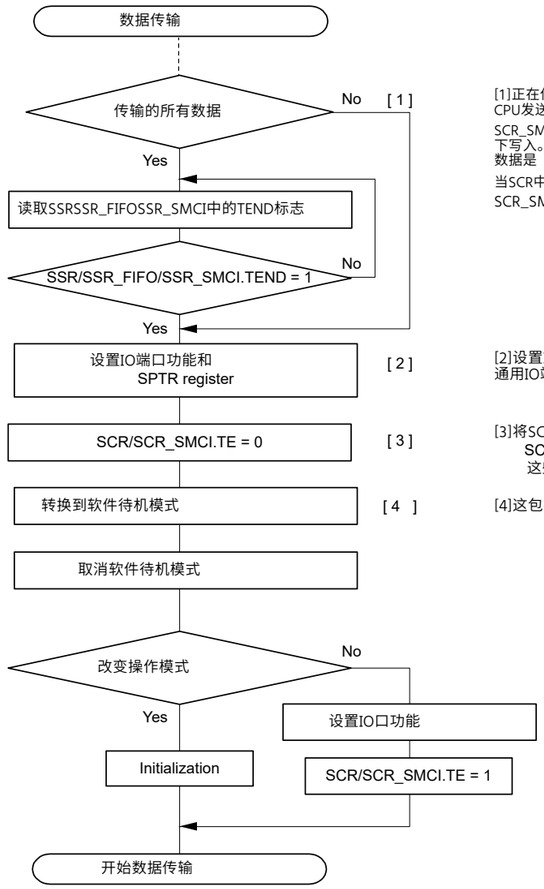
[1] Data being transmitted is lost. Data can be normally transmitted from the CPU by setting the TE bit in SCR/SCR_SMCI to 1, reading SSR/SSR_FIFO/ SSR_SMCI, and writing in Software Standby mode. However, if the DMAC or DTC is activated, the data remaining in the DMAC or DTC is Transmitted when both the TE and TIE bits in SCR/SCR_SMCI are set to 1.

[2] Set the I/O port function and SPTR register settings to switch the TXDn pin to operate as a general I/O port.

[3] Set SCR/SCR_SMCI.TE bit to 0. If SCR/SCR_SMCI.TIE = 1 and SCR/SCR_SMCI.TEIE = 1, these are set to 0 simultaneously with the SCR.TE bit.

[4] This includes the setting for the module-stop state.

Figure 30.118 Example flow of transition to Software Standby mode during transmission



[1]正在传输的数据丢失。通过设置SCR中的TE位可以正常从CPU发送数据
SCR_SMCI为1，读取SSRSSR_FIFOSSR_SMCI，并在软件待机模式下写入。但是，如果DMAC或DTC被激活，则DMAC或DTC中剩余的数据是
当SCR中的TE和TIE位都发送时
SCR_SMCI设置为1。

[2]设置IO端口功能和SPTR寄存器设置以切换TXDn引脚作为通用IO端口操作。

[3]将SCRSCR_SMCI.TE位设置为0。如果SCR
SCR_SMCI.TIE = 1 and SCR/SCR_SMCI.TEIE = 1,
这些与SCR.TE位同时设置为0。

[4]这包括模块停止状态的设置。

图30.118传输期间转换到软件待机模式的示例流程

RA生态工作室

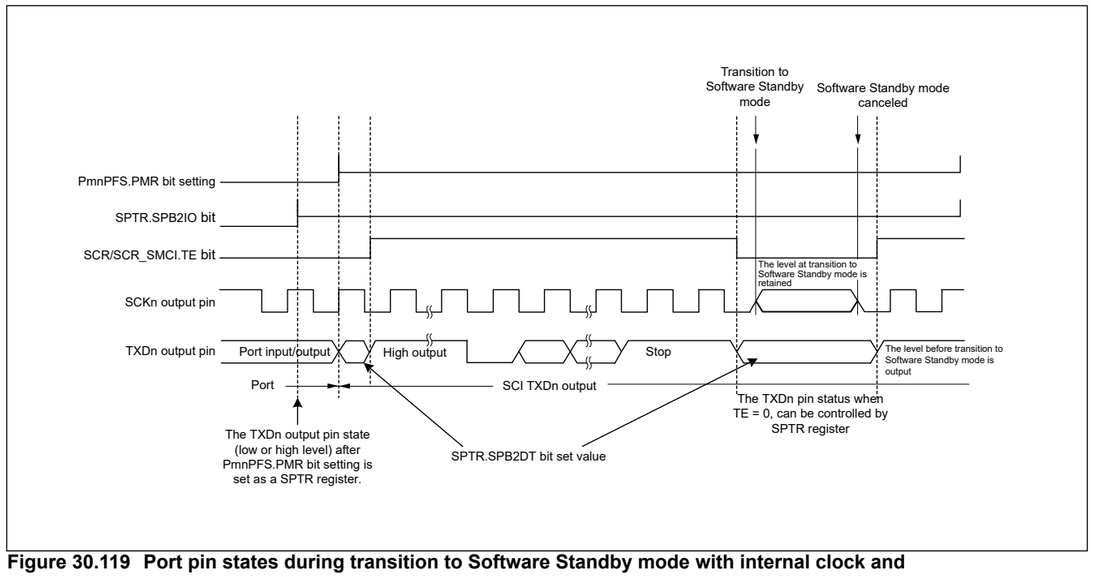


Figure 30.119 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

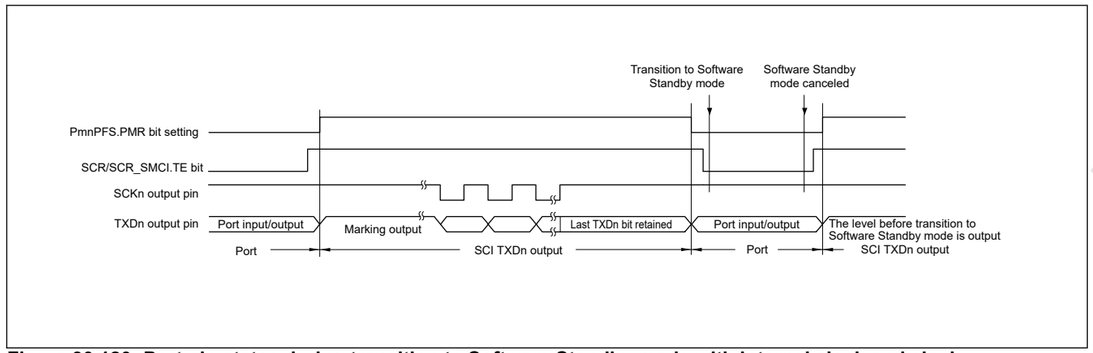


Figure 30.120 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

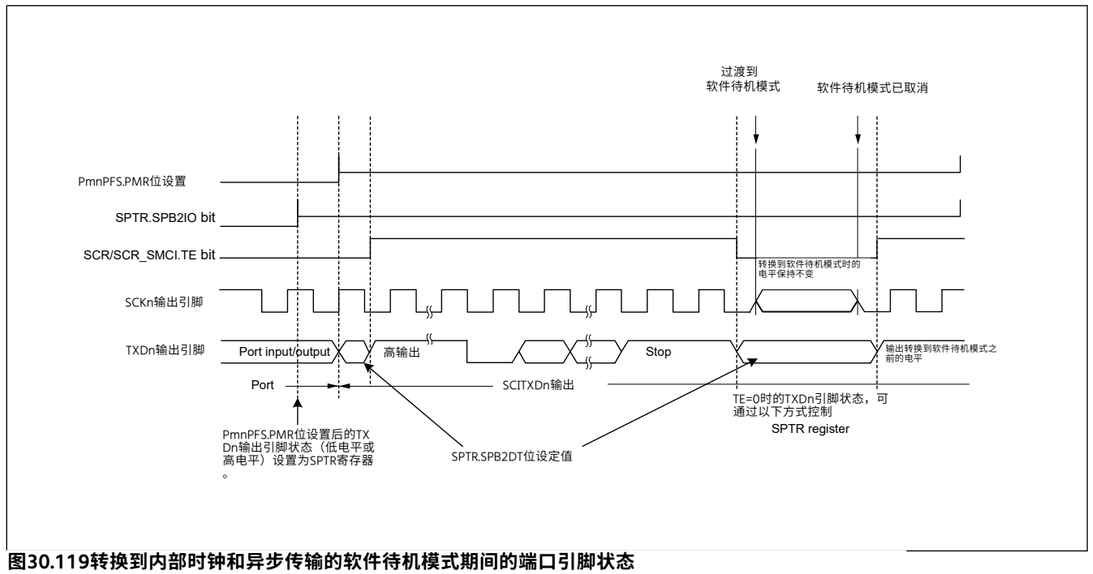


图30.119转换到内部时钟和异步传输的软件待机模式期间的端口引脚状态

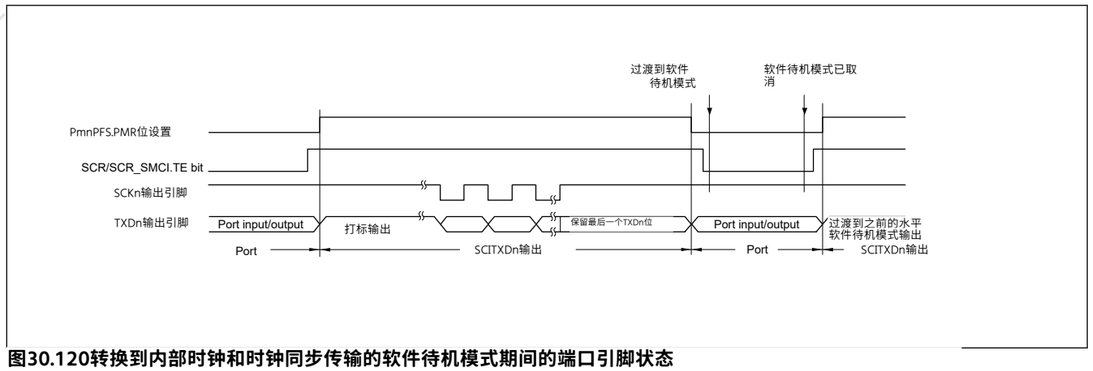
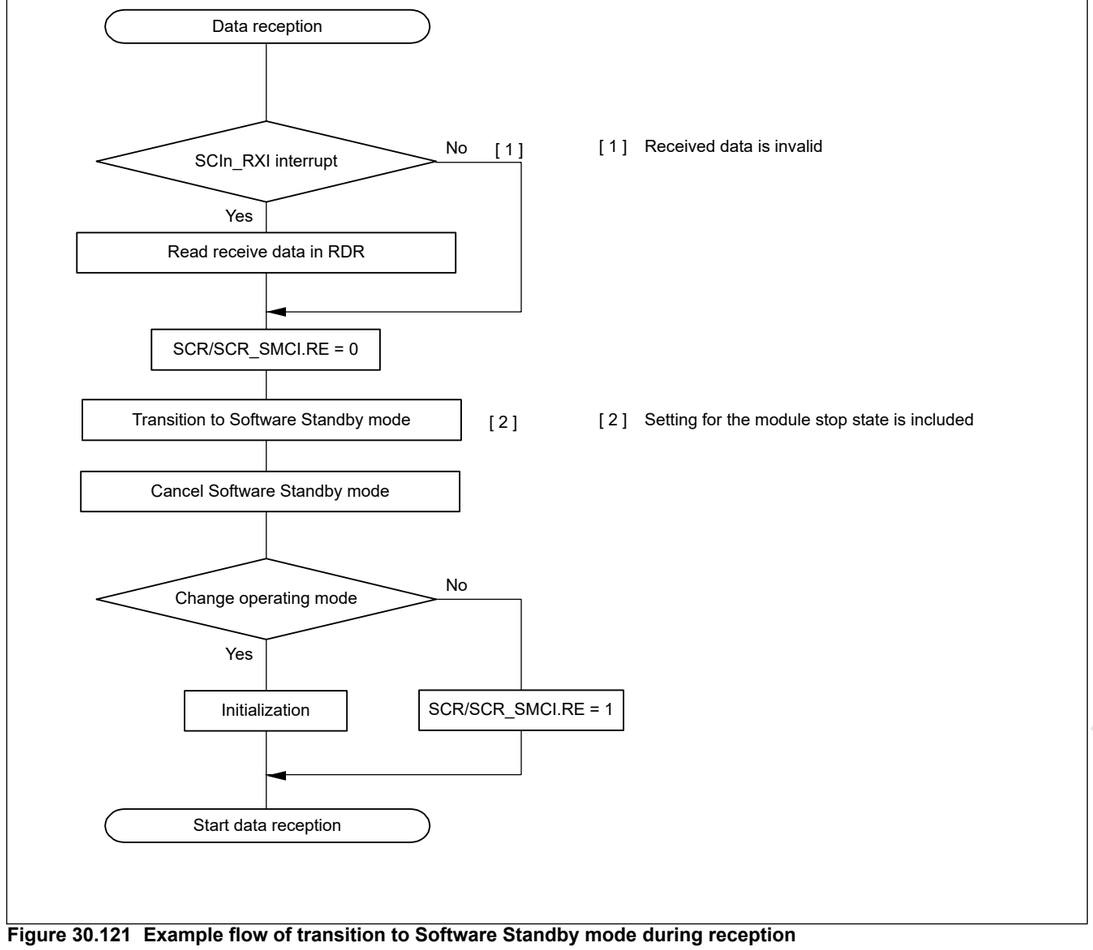


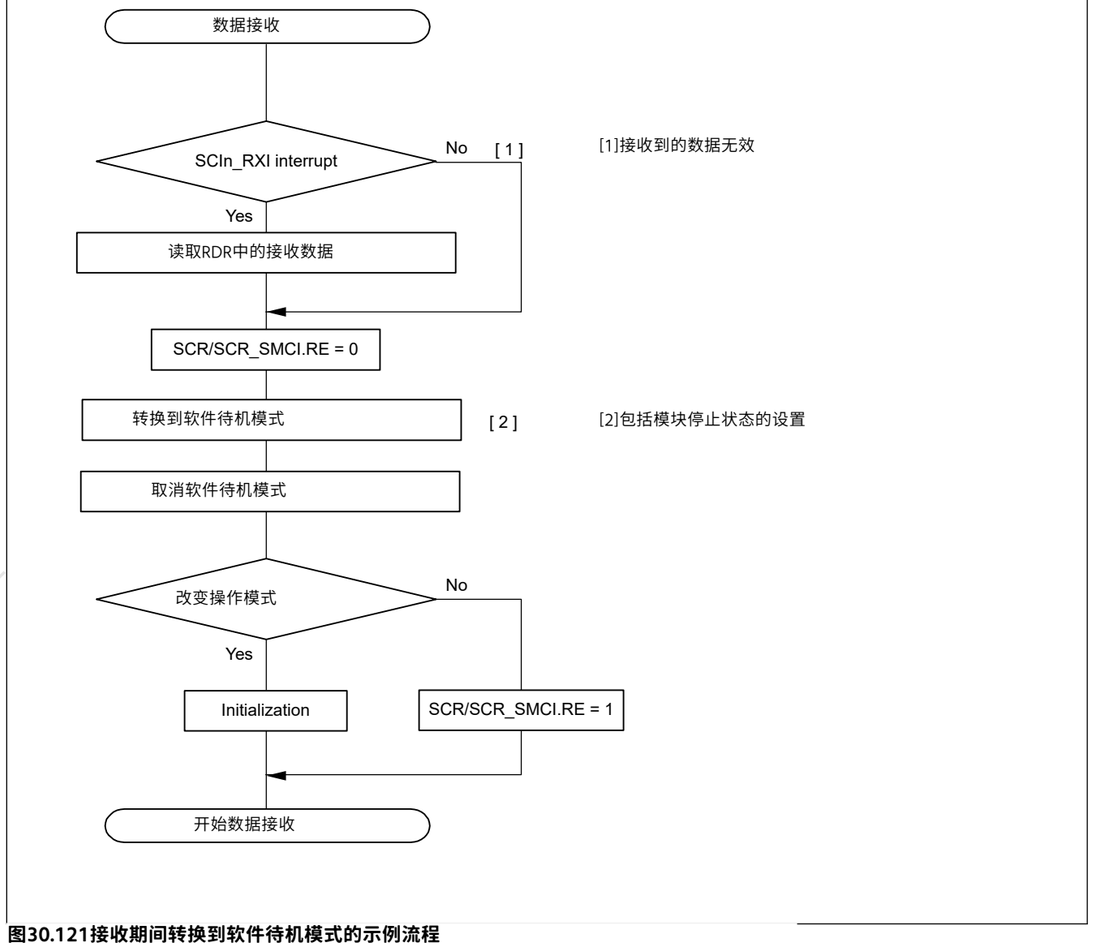
图30.120转换到内部时钟和时钟同步传输的软件待机模式期间的端口引脚状态



[1] Received data is invalid

[2] Setting for the module stop state is included

Figure 30.121 Example flow of transition to Software Standby mode during reception

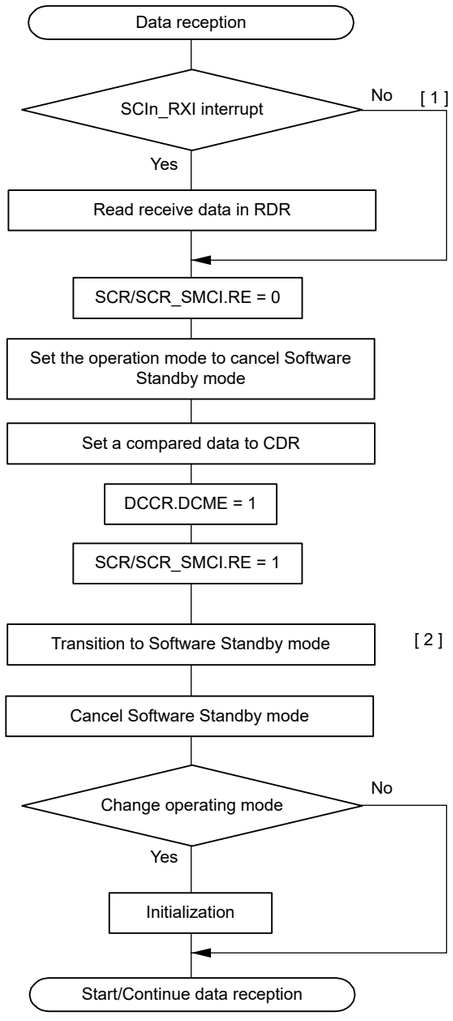


[1]接收到的数据无效

[2]包括模块停止状态的设置

图30.121接收期间转换到软件待机模式的示例流程

RA生态工作室



[1] Received data is invalid

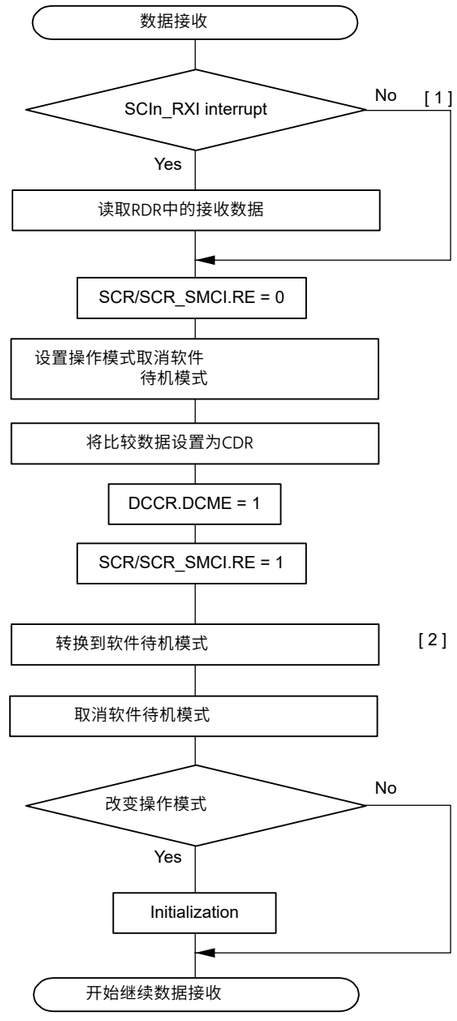
[2] Setting for the module-stop state is included

Figure 30.122 Example flow of transition to Software Standby mode during reception with address match

30.16.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and the SSR.FER flag is set to 1 to indicate a framing error, and the SSR.PER flag might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even if the FER flag is 0, indicating that no framing error occurred, it is set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops receiving operations until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0, the SSR.FER flag retains 0 during the break.



[1]接收到的数据无效

[2]包括模块停止状态的设置

图30.122在地址匹配的接收期间转换到软件待机模式的示例流程

30.16.3 断裂检测和处理

(1) Non-FIFO selected

当检测到帧错误时，可以通过直接读取RXDn引脚值来检测中断。在中断时，来自RXDn引脚的输入变为全0，并且SSR.FER标志设置为1表示帧错误，SSR.PER标志也可能设置为1表示奇偶校验错误。即使在收到中断后，SCI仍继续接收操作。因此，即使FER标志为0，表示没有发生帧错误，它也会再次设置为1。当SEMR.RXDESEL位为1时，SCI将SSR.FER标志设置为1并停止接收操作，直到检测到下一个数据帧的起始位。如果

SSR.FER标志设置为0，SSR.FER标志在中断期间保持0。

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for 1 frame, reception stops. When a framing error is detected, a break can be detected by reading the SPTR.RXDMON flag value. After the RXDn signal is in high and the break is finished, data reception to the FRDRHL register resumes.

30.16.4 Mark State and Production of Breaks

When the SCR/SCR_SMCI.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the SPTR.SPB2IO and SPTR.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the SCR/SCR_SMCI.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put the communication line in the mark state (the state of 1), and change the TXDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the SCR/SCR_SMCI.TE bit to 0. When the SCR/SCR_SMCI.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

30.16.5 Receive Error Flags and Transmit Operation in Clock Synchronous Mode and Simple SPI Mode

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even when data is written to TDR or FTDRL*1. Always set the receive error flags to 0 before starting transmission.

Note: The receive error flags cannot be set to 0 when the RE bit in SCR/SCR_SMCI is set to 0 (serial reception is disabled).

Note 1. Do not use the FTDRH register in simple SPI mode.

30.16.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous Mode and Simple SPI Mode

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLK cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}). See Figure 30.123.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock for bit [7] . See Figure 30.123.

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit [7]) to 4 PCLK cycles or longer. See Figure 30.123.

当RXDn引脚设置为1且中断结束时，在第一个下降沿检测起始位的开始
RXDn引脚允许SCI开始接收操作。

(2) FIFO selected

检测到帧错误后，当SCI检测到1帧连续接收数据为0时，接收停止。当检测到帧错误时，可以通过读取SPTR.RXDMON标志值来检测中断。RXDn信号为高电平且中断完成后，FRDRHL寄存器的数据接收恢复。

30.16.4 标记状态和产生的中断

当SCRSCR_SMCI.TE位为0时，禁用串行传输，TXDn引脚的状态可以使用
SPTR.SPB2IO和SPTR.SPB2DT位。使用这种方法，可以将TXDn引脚置于标记状态以发送中断。

在设置SCRSCR_SMCI.TE位为1，使能串行传输之前，设置SPB2IO和SPB2DT位使通信线处于标记状态（状态为1），并使用IO端口功能改变TXDn引脚。要输出数据传输中断，通过设置SPB2IO和SPB2DT位将TXDn引脚设置为输出0后，使用IO端口功能更改TXDn引脚并将SCRSCR_SMCI.TE位设置为0。当SCRSCR_SMCI.TE位设置为0，无论当前的传输状态如何，都初始化发送器。

30.16.5 在时钟同步模式下接收错误标志和发送操作和简单SPI模式

当SSRSSR_FIFO中的接收错误标志(ORER)设置为1时，传输无法开始，即使数据已写入TDR或FTDRL*1。在开始传输之前，始终将接收错误标志设置为0。

Note: 当SCRSCR_SMCI中的RE位设置为0（禁用串行接收）时，接收错误标志不能设置为0。

注1.不要在简单SPI模式下使用FTDRH寄存器。

30.16.6 时钟同步模式和简单SPI模式下时钟同步传输的限制

当外部时钟源用作同步时钟时，有以下限制。

(1) 传输开始

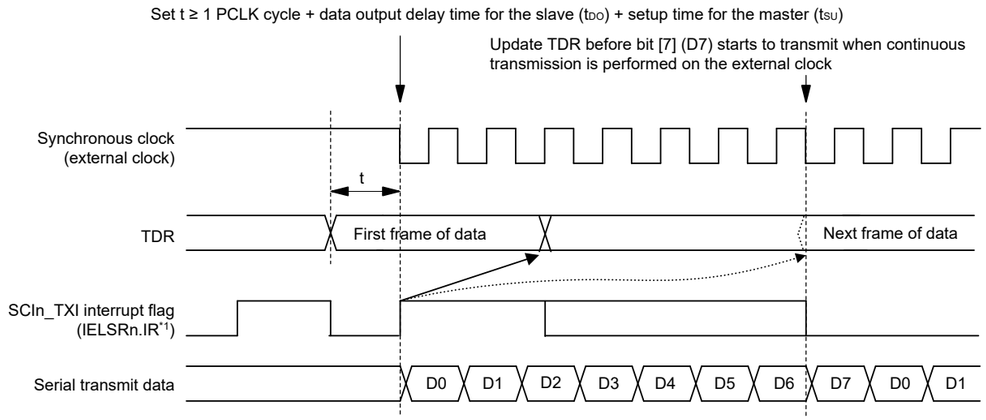
从将发送数据写入TDR到外部时钟输入开始，至少等待以下时间：

1个PCLK周期+从机的数据输出延迟时间(tDO)+主机的建立时间(tSU)。请参见图30.123。

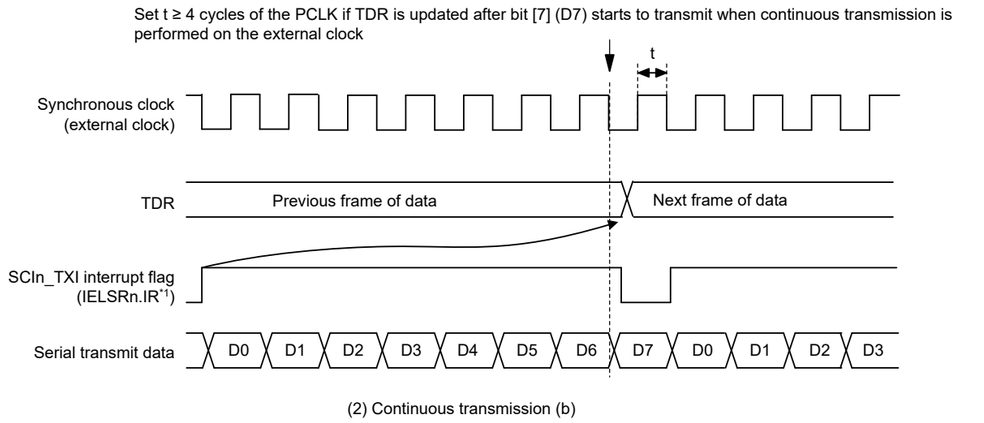
(2) 连续传输

在位[7]的发送时钟下降沿之前将下一个发送数据写入TDR或TDRHL。请参见图30.123。

在bit[7]开始发送后更新TDR时，在同步时钟处于低电平期间更新TDR，并将发送时钟（bit[7]）的高电平宽度设置为4个PCLK周期或更长.请参见图30.123。



(1) Start of transmission and (2) Continuous transmission (a)



(2) Continuous transmission (b)

Note 1. See section 13, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 30.123 Restraints on use of external clock in clock synchronous transmission

30.16.7 Restrictions on Using DTC or DMAC

During transmission or reception operations using the DTC or DMAC, do not set transfer data for the DTC or DMAC.

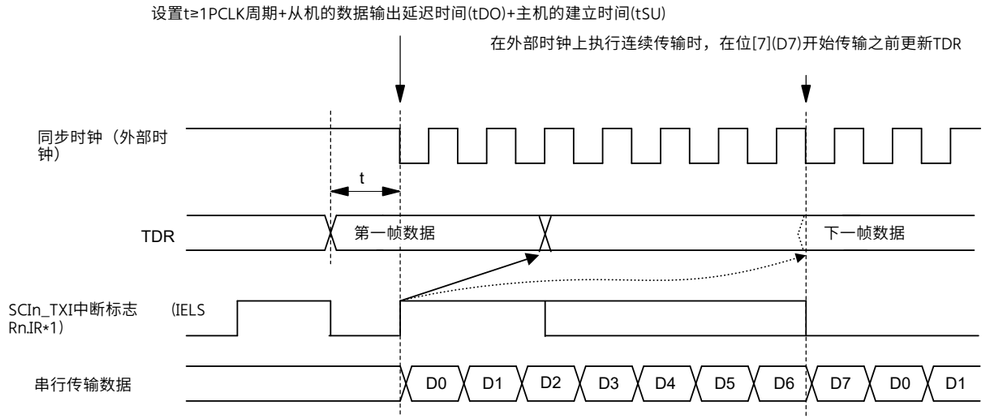
(1) Writing data to TDR (FTDRHL)

Non-FIFO selected

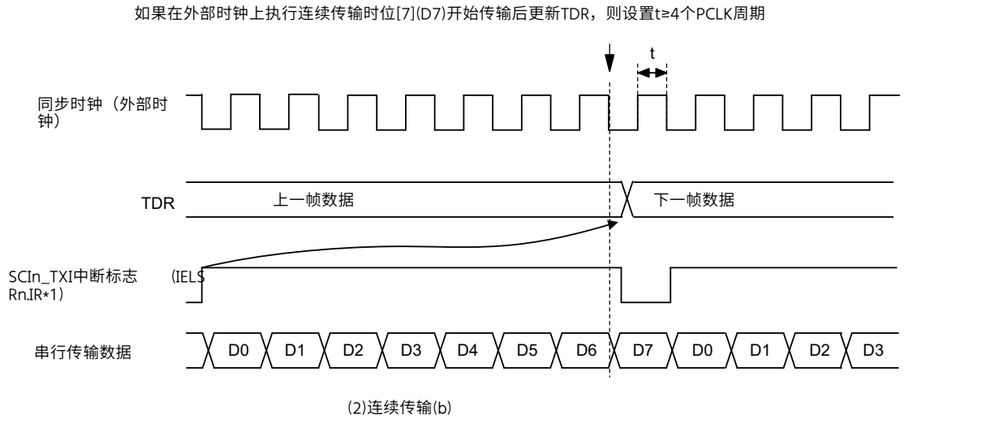
Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not transferred to TSR yet. When using DTC or DMAC, always write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data using the FDR.T[4:0] bits.



(1)传输开始和(2)连续传输(a)



(2)连续传输(b)

注1.有关相应中断事件编号的信息，请参见第13节，中断控制器单元(ICU)。

图30.123时钟同步传输中使用外部时钟的限制

30.16.7 使用DTC或DMAC的限制

在使用DTC或DMAC进行发送或接收操作期间，请勿为DTC或DMAC设置传输数据。

(1) 将数据写入TDR(FTDRHL)

Non-FIFO selected

数据可以写入TDR和TDRHL。但是，如果在发送数据保留在TDR或TDRHL中时将新数据写入TDR或TDRHL，则TDR和TDRHL中的先前数据将丢失，因为它尚未传输到TSR。使用DTC或DMAC时，始终在SCIn_TXI中断请求处理程序中将发送数据写入TDR或TDRHL。

FIFO selected

当SCR.TE为1时，可以将数据写入FTDRH和FTDRL寄存器。使用FDR.T[4:0]位确认可写入的数据量。

(2) Reading data from RDR (FRDRHL)

When using the DTC or DMAC to read RDR and RDRHL, always set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI.

30.16.8 Notes on Starting Transfer

At the point where transfer starts when the interrupt status flag (IELSRn.IR flag) in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1). For details on the interrupt status flag, see section 13, Interrupt Controller Unit (ICU).

1. Confirm that transfer has stopped (the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0)
2. Set the associated interrupt enable bit (SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit) to 0
3. Read the associated interrupt enable bit (SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit) to check that it actually becomes 0
4. Set the interrupt status flag, IELSRn.IR, in the ICU to 0

30.16.9 External Clock Input in Clock Synchronous Mode and Simple SPI Mode

In clock synchronous mode and simple SPI mode, the external clock SCKn must be input as follows:

High-pulse period, low-pulse period = 2 PCLK cycles or more, period = 6 PCLK cycles or more.

30.16.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set in the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1.
  This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit changes from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.
- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 30.124. If the TE and RE bits in the SCR register become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while a character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

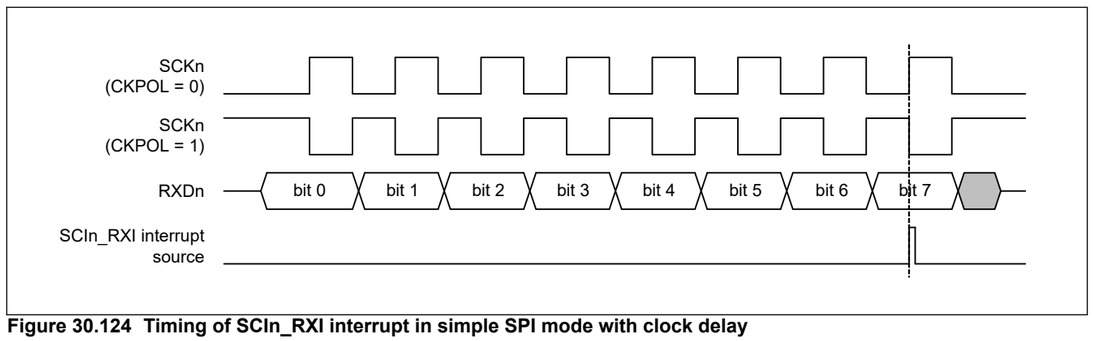


Figure 30.124 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

(2) 从RDR(FRDRHL)读取数据

使用DTC或DMAC读取RDR和RDRHL时，始终将接收数据满中断（SCIn_RXI）设置为相关SCI的激活源。

30.16.8 开始转移注意事项

在ICU中的中断状态标志（IELSRn.IR标志）为1时开始传输的点，按照本节中的步骤在允许操作之前清除中断请求（通过设置SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位到1)。有关中断状态标志的详细信息，请参见第13节，中断控制器单元(ICU)。

1.确认传输已停止（SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位为0）

2.将相关的中断使能位（SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位）设置为0

3.读取相关的中断使能位（SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位）以检查它是否实际变为0

4.将ICU中的中断状态标志IELSRn.IR设置为0

30.16.9 时钟同步模式和简单SPI模式下的外部时钟输入

在时钟同步模式和简单SPI模式下，外部时钟SCKn必须输入如下：

高脉冲周期，低脉冲周期=2个PCLK周期或更多，周期=6个PCLK周期或更多。

30.16.10 简单SPI模式的限制

(1) 主模式

●当SPMR.SSE位为1时，使用电阻上拉或下拉与SPMR.CKPH和CKPOL位中设置的传输时钟的初始设置相匹配的时钟线。
这可以防止当SCR.TE位设置为0时时钟线处于高阻抗状态，或者当SCR.TE位从0变为1时在时钟线上产生意外边沿。SSE位在单主机模式下为0，不需要上拉或下拉时钟线，因为即使SCR.TE位设置为0，时钟线也不会处于高阻状态。

●对于时钟延迟设置（SPMR.CKPH位为1），接收数据满中断（SCIn_RXI）在SCKn引脚的最后一个时钟沿之前产生，如图30.124所示。如果SCR寄存器中的TE和RE位在SCKn引脚上的时钟信号的最后一个边沿之前变为0，则SCKn引脚处于高阻状态，因此传输时钟的最后一个时钟脉冲的宽度为缩短。此外，SCIn_RXI中断可能会导致所连接从机的SSn引脚上的输入信号在SCKn引脚上的时钟信号的最后一个边沿之前变为高电平，从而导致从机的错误操作。

●在多主机配置中，如果在传输字符时发生模式故障错误，则SCKn引脚输出变为高阻态，而SSn引脚上的输入处于低电平，从而停止向主机提供时钟信号。连接的奴隶。重新启动传输时，重置连接的从机以避免未对齐的位。

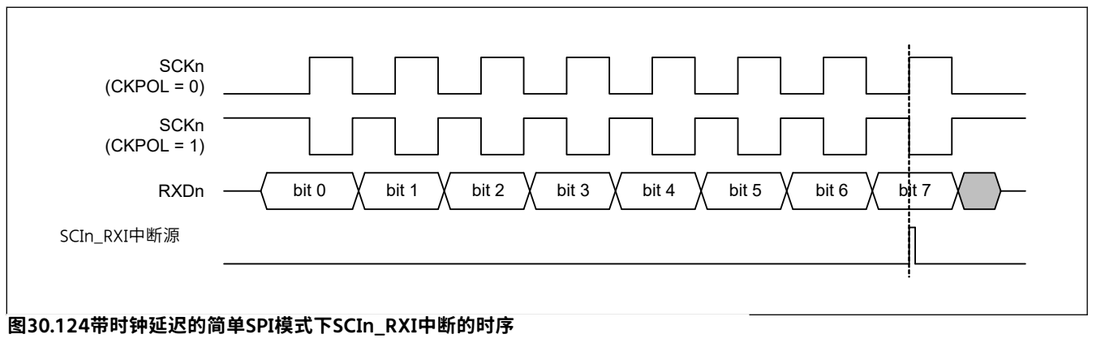


图30.124带时钟延迟的简单SPI模式下SCIn_RXI中断的时序

(2) Slave mode

- Wait at least the following time from writing transmit data in the TDR register to the start of the external clock input.
  1 PCLK cycle + data output delay for the slave (t_{DO}) + setup time for the master (t_{SU})
  Also wait at least 5 PCLK cycles from the input of the low level on the SSn pin to the start of the external clock input.
- Provide an external clock signal to the master the same as the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin is to be changed from low to high while a character is being transferred, set the TE and RE bits in the SCR register to 0 and, after restoring the settings, restart transfer of the first byte

30.16.11 Notes on Transmitt Enable bit (SCR.TE)

In initial register value, when SCR.TE bit is “0”, the terminal as “TXDn” outputs high impedance.

So please make sure that the TXDn line won’t be high impedance by the following one of ways.

1. The pull-up resistance is connected to the TXDn line.
2. Before SCR.TE bit is “0”, the function of the terminal is changed to general-purpose input port or output port. And after SCR.TE bit is “1”, thr function of the terminal is changed to “TXDn”.
3. In asynchronous mode, you can set SPTR and decided level of TXDn terminal during SCR.TE is “0”.

In the Simple SPI mode slave operation, the RXDn terminal operates in the same way as the above TXDn terminal, so please deal with 1 or 2 in the same way. (3 can not be used.)

30.16.12 Limitation 1 on Usage of the Extended Serial Mode Control Section

When the PCR.SHARPS bit is set to 1, output on the TXDXn/RXDXn (n = 1, 2) pin is only possible when the following conditions apply.

- The timer of the SCIh module is in Break Field low width output mode and the value of the TCR.TCST bit is 1 (when the TCST bit is set to 1, the high level continues to be output for up to one cycle of the clock source for counting by the timer counter before output of the low level)
- The value of the SCIn.SCR.TE bit is 1.

30.16.13 Limitation 2 on Usage of the Extended Serial Mode Control Section

An SCIg interrupt request is generated even if the extended serial mode is enabled. However, the SCIg interrupt should not be used during reception of a Start Frame because SCIh uses an SCIg interrupt request.

The two ways of dealing with this are described below. When a receive error is detected, clear the error flag of the SCIg and initialize the control section of the SCIh.

1. Set the SCR.RIE bit of the SCIg to 0 to disable the output of interrupt requests. Check the error flags in the SSR register for SCIg on completion of the reception of a Start Frame, because an ERI interrupt is not generated if a receive error occurs. After reception of the Start Frame is completed, set the SCR.RIE bit of the SCIg to 1 by the time the first byte of the Information Frame is received.
2. Set the SCR.RIE bit of the SCIg to 1 to disable RXI interrupts and enable ERI interrupts for ICU.
   Clear the IRn.IR flag to enable the acceptance of RXI interrupts by ICU by the time the first byte of the Information Frame is received after the completion of Start Frame reception.

(2) 从机模式

●从将发送数据写入TDR寄存器到外部时钟输入开始，至少等待以下时间。
1个PCLK周期+从机的数据输出延迟(tDO)+主机的建立时间(tSU)
还要等待至少5个PCLK周期，从SSn引脚上的低电平输入到外部时钟输入开始。

●向主机提供与传输数据长度相同的外部时钟信号

●在数据传输开始前和结束后控制SSn引脚上的输入

●当在字符传输过程中SSn引脚的输入电平由低变为高时，将SCR寄存器中的TE和RE位设置为0，并在恢复设置后重新开始传输第一个字节

30.16.11 发送使能位(SCR.TE)的注意事项

在初始寄存器值中，当SCR.TE位为“0”时，“TXDn”端输出高阻抗。

所以请通过以下方式之一确保TXDn线不会高阻。

1.上拉电阻连接到TXDn线。

2.SCR.TE位为“0”之前，端子功能变为通用输入端口或输出端口。并且在SCR.TE位为“1”后，终端的thr功能变为“TXDn”。

3.在异步模式下，可以设置SPTR和SCR.TE期间TXDn端子的决定电平为“0”。

在SimpleSPI模式从机操作中，RXDn端子与上述TXDn端子的操作方式相同，因此请按相同方式处理1或2。（3个不能用。）

30.16.12 使用扩展串行模式控制部分的限制1

当PCR.SHARPS位设置为1时，TXDXnRXDXn(n=1 2)引脚上的输出只有在以下条件适用时才可能。

●SCIh模块的定时器处于BreakField低宽度输出模式，TCR.TCST位的值为1（当TCST位设置为1时，最多持续输出高电平一个周期）低电平输出前由定时器计数器计数的时钟源）

●SCIn.SCR.TE位的值为1。

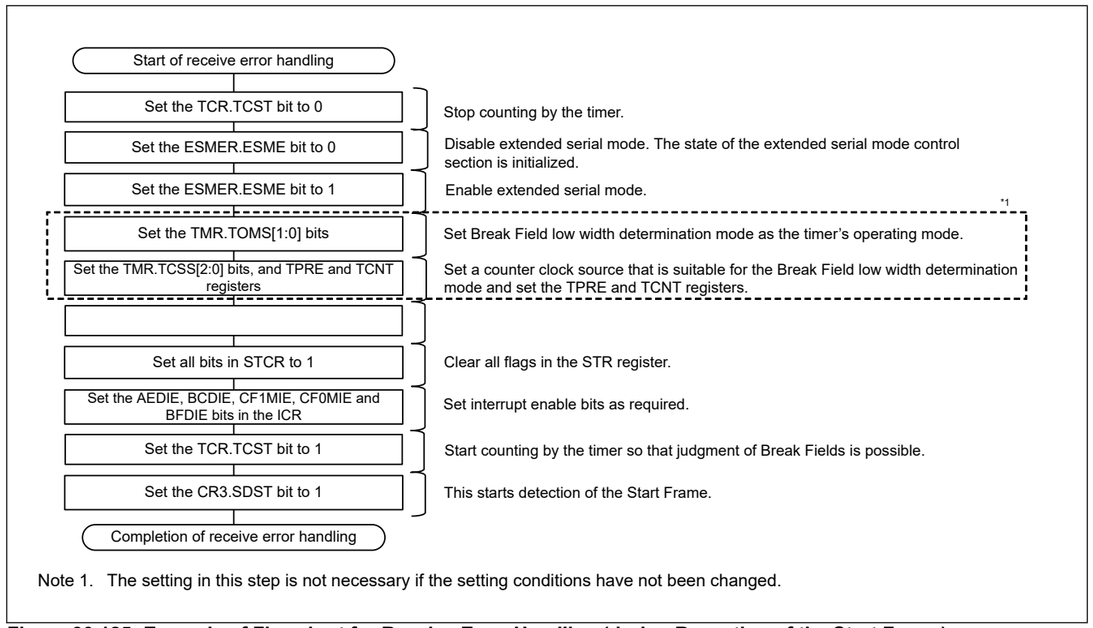
30.16.13 使用扩展串行模式控制部分的限制2

即使启用了扩展串行模式，也会产生SCIg中断请求。但是，在接收起始帧期间不应使用SCIg中断，因为SCIh使用SCIg中断请求。

下面介绍两种处理方法。当检测到接收错误时，清除SCIg的错误标志并初始化SCIh的控制部分。

1.将SCIg的SCR.RIE位设置为0，以禁用中断请求的输出。在完成接收起始帧时检查SSR寄存器中的错误标志是否有SCIg，因为如果发生接收错误，则不会产生ERI中断。开始帧接收完成后，在接收到信息帧的第一个字节时将SCIg的SCR.RIE位设置为1。

2.将SCIg的SCR.RIE位设置为1，以禁用RXI中断并启用ICU的ERI中断。
清除IRn.IR标志以使ICU在信息的第一个字节之前接受RXI中断
开始帧接收完成后接收帧。



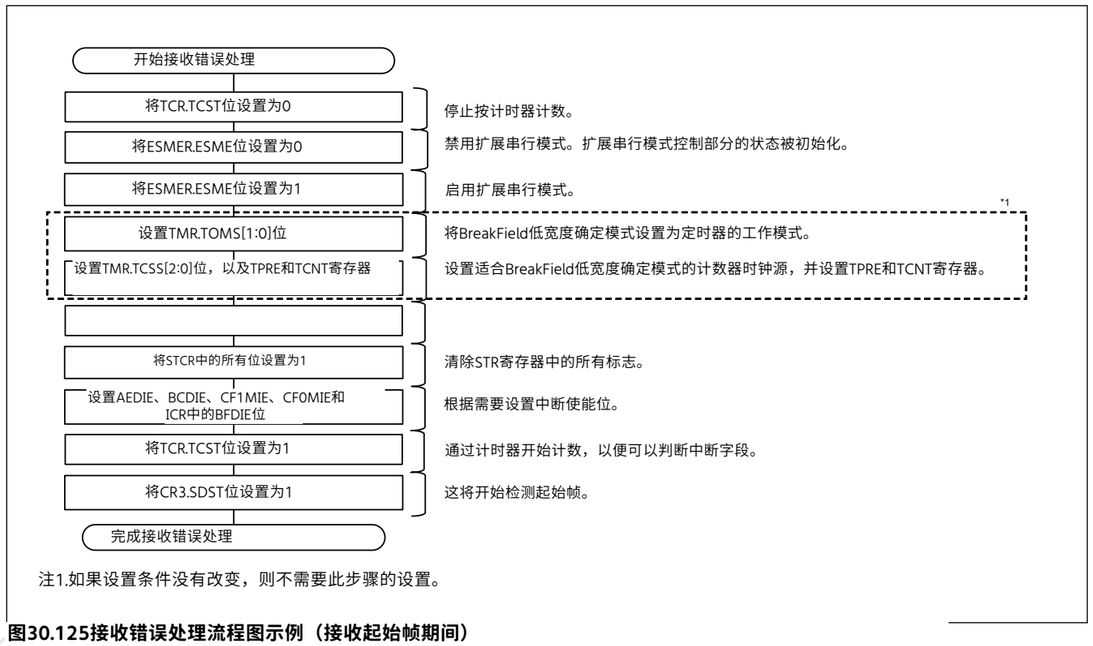
Note 1. The setting in this step is not necessary if the setting conditions have not been changed.

Figure 30.125 Example of Flowchart for Receive Error Handling (during Reception of the Start Frame)

30.16.14 Note on Stopping Reception When Using the RTS Function in Asynchronous Mode

One clock cycle of PCLK is required for the time from setting the SCR.RE bit to 0 to stopping the RTS signal generator in asynchronous mode.

When reading the RDR (or RDRL) register after setting the SCR.RE bit to 0, confirm that the RE bit has been set to 0 before reading the RDR (or RDRL) register to prevent these two processes from being performed consecutively.



注1.如果设置条件没有改变，则不需要此步骤的设置。

图30.125接收错误处理流程图示例（接收起始帧期间）

30.16.14 异步使用RTS函数时停止接收的注意事项 Mode

从将SCR.RE位设置为0到在异步模式下停止RTS信号发生器，需要一个PCLK时钟周期。

在将SCR.RE位设置为0后读取RDR（或RDRL）寄存器时，请在读取RDR（或RDRL）寄存器之前确认RE位已设置为0，以防止这两个过程连续执行。

31. I²C Bus Interface (IIC)

31.1 Overview

The I²C bus interface (IIC) has 3 channels. The IIC module conforms with and provides a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions.

Table 31.1 lists the IIC specifications, Figure 31.1 shows a block diagram, and Figure 31.2 shows an example of I/O pin connections to external circuits, with an I²C bus configuration. Table 31.2 lists the I/O pins.

Table 31.1 IIC specifications (1 of 2)

Parameter	Specifications
Communications format	• I²C-bus format or SMBus format • Master or slave mode selectable • Automatic securing of the setup times, hold times, and bus-free times for the transfer rate
Transfer rate	• Fast-mode Plus supported, up to 1 Mbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated • Start conditions (including restart conditions) and stop conditions are detectable
Slave address	• Configurable for up to three different slave addresses • 7- and 10-bit address formats supported, including simultaneous use • General call addresses, device ID addresses, and SMBus host addresses detectable
Acknowledgment	• For transmission, automatic loading of the acknowledge bit Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatic transmission of the acknowledge bit If a wait between the 8th and 9th clock cycles is selected, the software can control the value in the acknowledge field in response to the received value.
Wait function	During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the 1st clock cycle of the next transfer
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed
Arbitration	• For multi-master operation: – SCL clock synchronization is possible when conflict occurs with the SCL signal from another master – When issuing the start condition creates conflict on the bus, loss of arbitration is detected by testing for a mismatch between the internal signal for the SDA line and the level on the SDA line – In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line • Loss of arbitration because the start condition occurs while the bus is busy is detectable, to prevent the issuing of double start conditions • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match • Loss of arbitration because a mismatch of internal and line levels for data is detectable in slave transmission
Timeout function	Internal detection of long-interval stops of the SCL clock
Noise cancellation	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters
Interrupt sources	• Transfer error or event occurrence (arbitration-lost, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end
Module-stop function	Module-stop state can be set
IIC operating modes	• Master transmit • Master receive • Slave transmit • Slave receive

31. I2C总线接口(IIC)

31.1 Overview

I2C总线接口(IIC)有3个通道。IIC模块符合并提供NXPI2C(Inter
集成电路）总线接口功能。

表31.1列出了IIC规范，图31.1显示了框图，图31.2显示了IO引脚连接到外部电路的示例，具有I2C总线配置。
表31.2列出了IO引脚。

Table 31.1 IIC规格(1of2)

Parameter	Specifications
通讯格式	• I2C-bus格式或SMBus格式 • 可选择主从模式 • 自动保护传输速率的设置时间、保持时间和无总线时间
传输率	• 支持快速模式Plus，最高1Mbps
SCL clock	对于主机操作，SCL时钟的占空比可在4%至96%的范围内选择
发布和检测条件	• 自动生成启动、重启和停止条件 • 可检测启动条件（包括重启条件）和停止条件
从机地址	• 最多可配置三个不同的从地址 • 支持7位和10位地址格式，包括同时使用 • 可检测到广播呼叫地址、设备ID地址和SMBus主机地址
Acknowledgment	• 对于传输，自动加载确认位 检测到未确认位时，可以自动暂停下一个发送数据的传输。 • 对于接收，确认位的自动传输 如果选择了第8和第9个时钟周期之间的等待，软件可以控制确认字段中的值以响应接收到的值。
等待功能	在接收期间，将SCL时钟保持为低电平可获得以下等待周期：● 在第八和第九个时钟周期之间等待 • 在第9个时钟周期和下一次传输的第1个时钟周期之间等待
SDA输出延迟功能	传输数据的输出时序，包括确认位，可以延迟
Arbitration	• For multi-master operation: – 当与来自另一个主机的SCL信号发生冲突时，可以进行SCL时钟同步 – 当发出启动条件在总线上产生冲突时，通过测试SDA线的内部信号和SDA线上的电平之间的不匹配来检测仲裁丢失 – 在主机操作中，通过测试SDA线路上的信号与SDA线路的内部信号之间的不匹配来检测仲裁丢失 • 可检测到由于在总线繁忙时出现启动条件而导致的仲裁丢失，以防止发出双启动条件 • 由于SDA线的内部信号和SDA线上的电平不匹配，在传输未确认位时可检测到仲裁丢失 • 在从传输中可检测到数据的内部电平和线路电平不匹配而导致仲裁丢失
超时功能	内部检测SCL时钟的长间隔停止
噪音消除	• SCL和SDA信号的数字噪声滤波器 • 通过滤波器消除噪声的可编程窗口
中断源	• 传输错误或事件发生（仲裁丢失、NACK、超时、启动或重启条件或停止条件） • 接收数据已满，包括与从地址匹配 • 发送数据为空，包括匹配从机地址 • 发射端
Module-stop function	模块停止状态可设置
IIC操作模式	• 主传输 • 主接收 • 从机发送 • 从机接收

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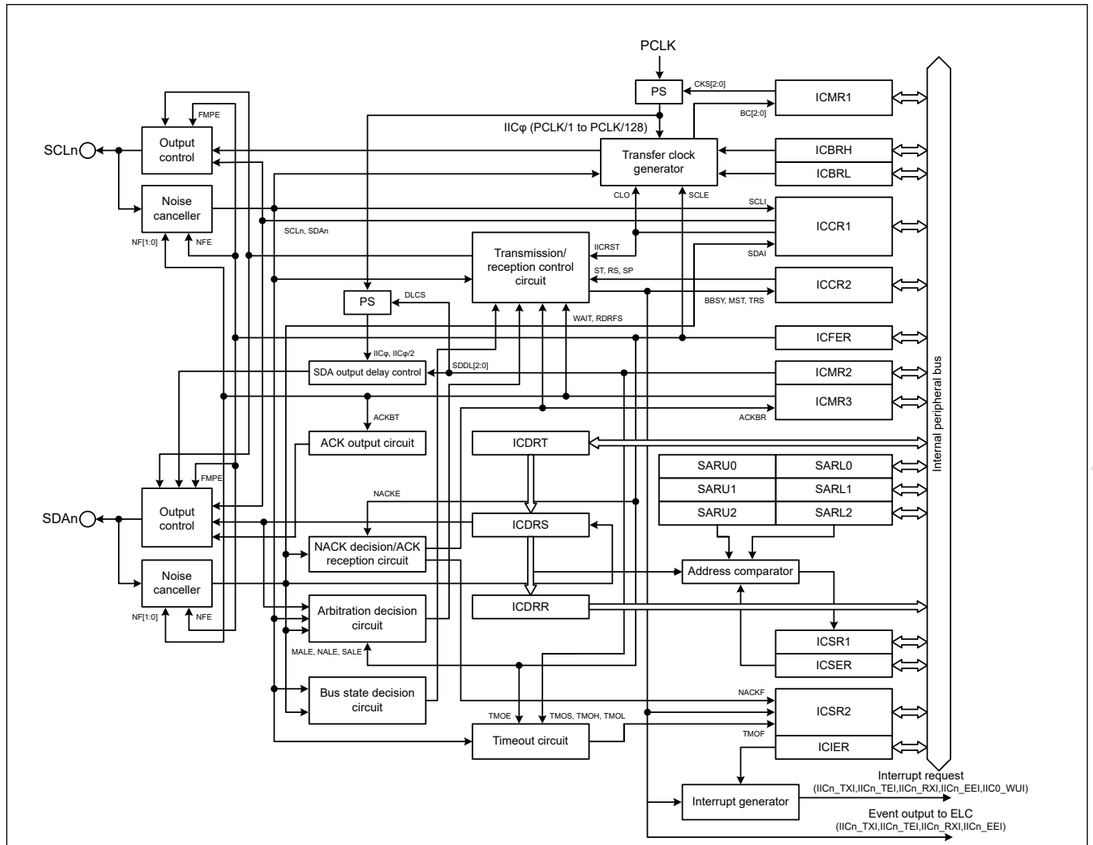
Table 31.1 IIC specifications (2 of 2)

Parameter	Specifications
Event link function (output)	• Transfer error or event occurrence (arbitration-lost, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end
Wakeup function*1	CPU can return from Software Standby mode using a wakeup event
TrustZone Filter	Security attribution can be set for each channels

Note 1. This function is only available for IIC channel IIC0. IIC1 is not supported.



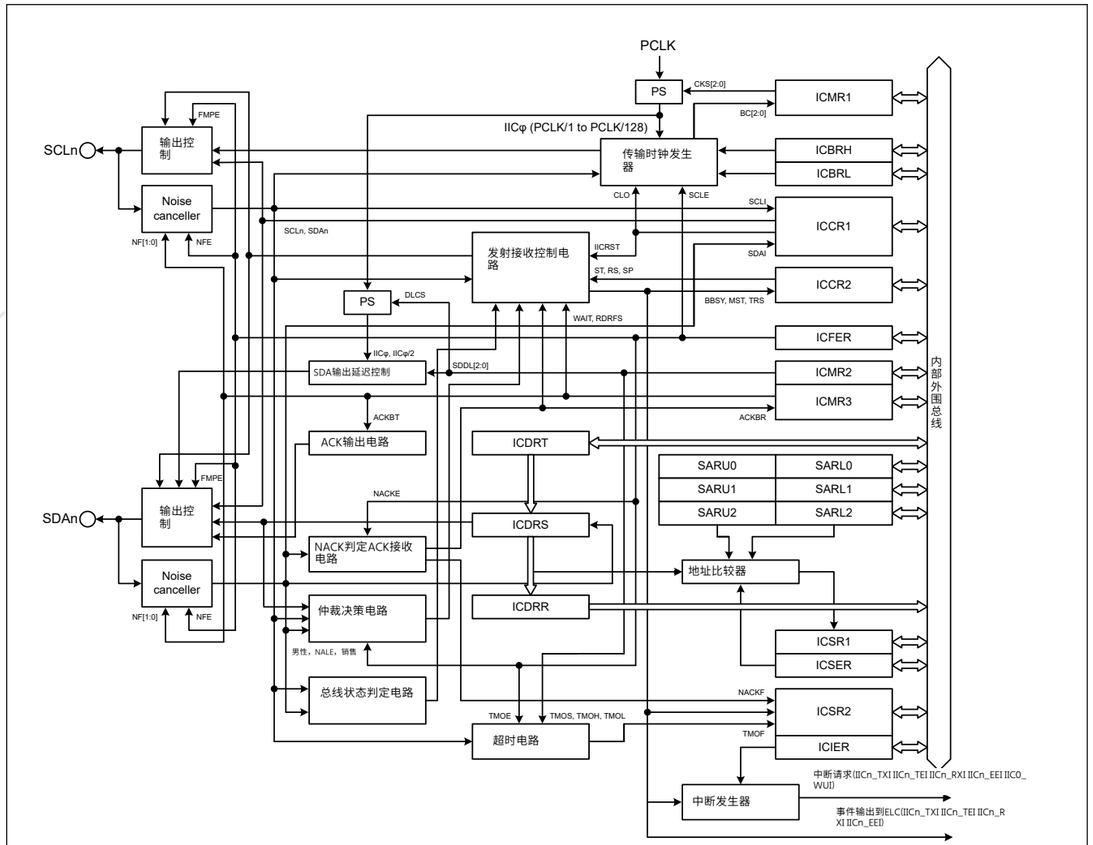
Note: n = 0 to 2
PCLK = PCLKB

Figure 31.1 IIC block diagram

Table 31.1 IIC规格（2个中的2个）

Parameter	Specifications
事件链接功能（输出）	• 传输错误或事件发生（仲裁丢失、NACK、超时、启动或重启条件或停止条件） • 接收数据已满，包括与从地址匹配 • 发送数据为空，包括匹配从机地址 • 发射端
唤醒功能*1	CPU可以使用唤醒事件从软件待机模式返回
TrustZone Filter	可以为每个通道设置安全属性

注1.此功能仅适用于IIC通道IIC0。不支持IIC1。



Note: n = 0 to 2
PCLK = PCLKB

Figure 31.1 IIC框图

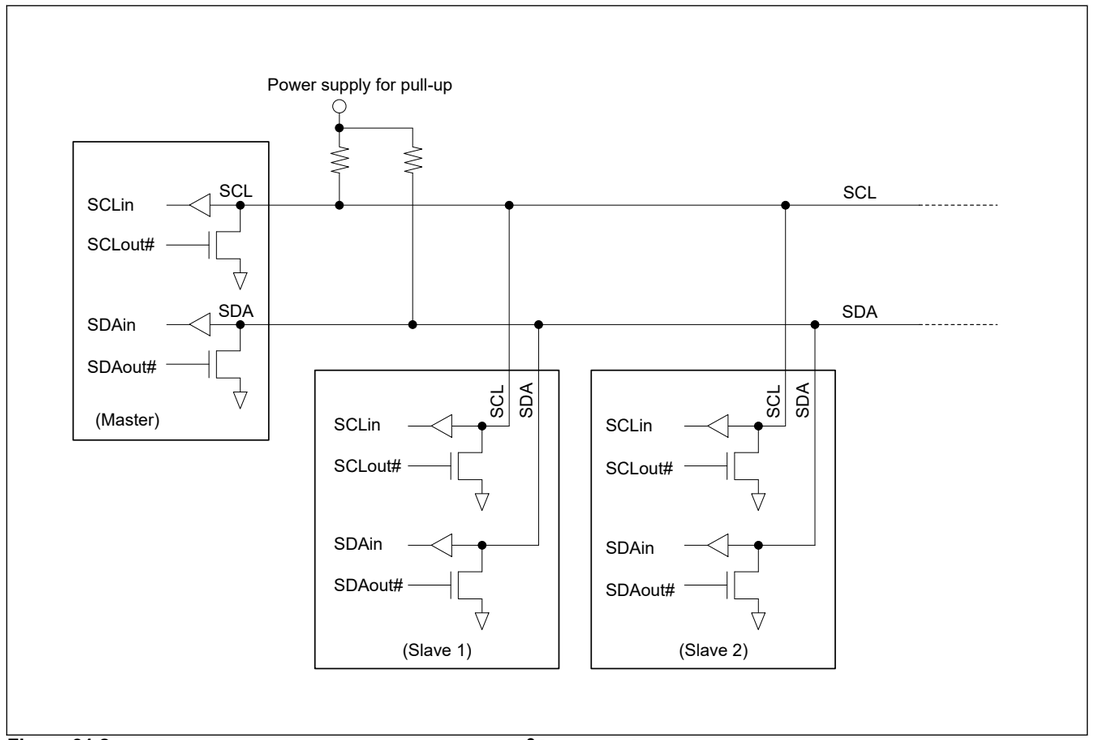


Figure 31.2 I/O pin connection to an external circuit (I²C bus configuration example)

The input level of the signals for IIC is CMOS when I²C bus is selected (ICMR3.SMBS = 0), or TTL when SMBus is selected (ICMR3.SMBS = 1).

Table 31.2 IIC I/O pins

Channel	Pin name	I/O	Function
IICn	SCLn	I/O	IICn serial clock I/O pin
	SDAn	I/O	IICn serial data I/O pin

Note: n = 0 to 2

31.2 Register Descriptions

31.2.1 ICCR1 : I²C Bus Control Register 1

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SDAI	SDA Line Monitor 0: SDAn line is low 1: SDAn line is high	R

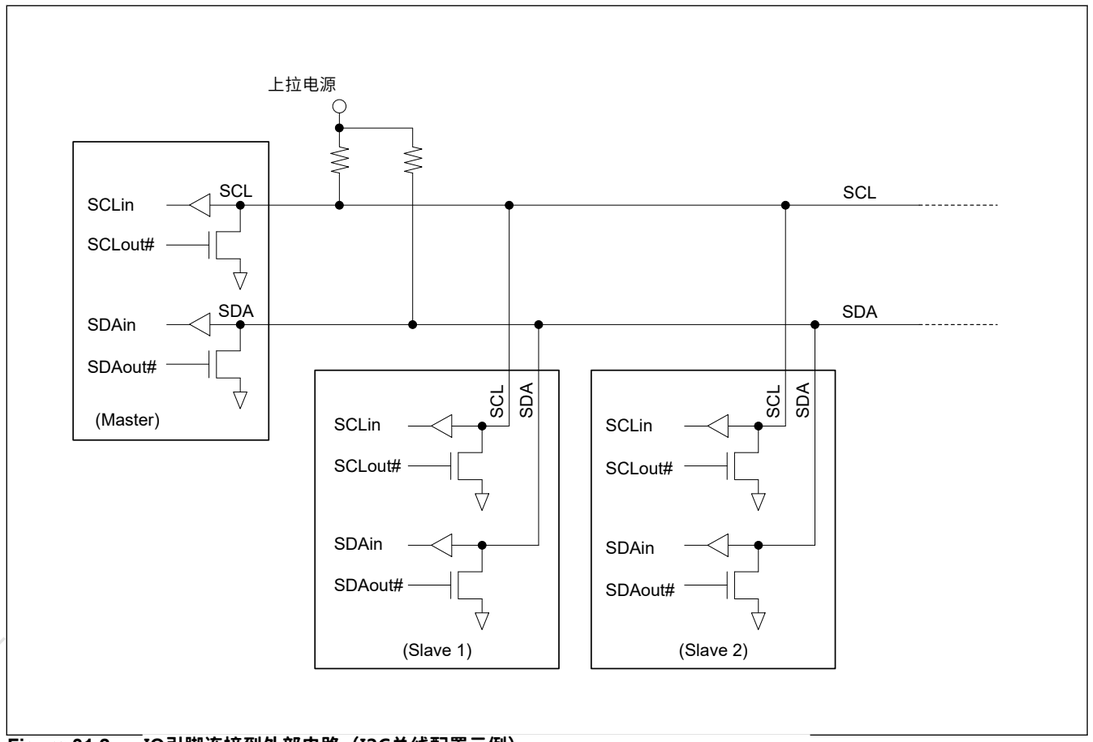


Figure 31.2 IO引脚连接到外部电路（I2C总线配置示例）

TheinputlevelofthesignalsforIICisCMOSwhenI2Cbusisselected(ICMR3.SMBS=0) orTTLwhenSMBusisselected (ICMR3.SMBS=1).

Table 31.2 IIC I/O pins

Channel	引脚名称	I/O	Function
IICn	SCLn	I/O	IICn串行时钟IO引脚
	SDAn	I/O	IICn串行数据IO引脚

Note: n = 0 to 2

31.2 注册说明

31.2.1 ICCR1:I2C总线控制寄存器1

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
重置后的值:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SDAI	SDA线路监视器 0：SDAn线低1：SD An线高	R

Bit	Symbol	Function	R/W
1	SCLI	SCL Line Monitor 0: SCLn line is low 1: SCLn line is high	R
2	SDAO	SDA Output Control/Monitor 0: Read: IIC drives SDAn pin low Write: IIC drives SDAn pin low 1: Read: IIC releases SDAn pin Write: IIC releases SDAn pin	R/W
3	SCLO	SCL Output Control/Monitor Use an external pull-up resistor to drive the signal high. 0: Read: IIC drives SCLn pin low Write: IIC drives SCLn pin low 1: Read: IIC releases SCLn pin Write: IIC releases SCLn pin	R/W
4	SOWP	SCLO/SDAO Write Protect This bit is read as 1. 0: Write enable SCLO and SDAO bits 1: Write protect SCLO and SDAO bits	W
5	CLO	Extra SCL Clock Cycle Output This bit clears automatically after 1 clock cycle is output. 0: Do not output extra SCL clock cycle (default) 1: Output extra SCL clock cycle	R/W
6	IICRST	I^2C Bus Interface Internal Reset This setting clears the bit counter and the SCLn/SDAn output latch. 0: Release IIC reset or internal reset 1: Initiate IIC reset or internal reset	R/W
7	ICE	I^2C Bus Interface Enable Used in combination with the IICRST bit to select either IIC or internal reset. 0: Disable (SCLn and SDAn pins in inactive state) 1: Enable (SCLn and SDAn pins in active state)	R/W

SDAO bit (SDA Output Control/Monitor) and SCLO bit (SCL Output Control/Monitor)

The SDAO and SCLO bits directly control the SDAn and SCLn signals output from the IIC. When writing to these bits, also write 0 to the SOWP bit. Setting these bits results in input to the IIC by the input buffer. When slave mode is selected, a start condition might be detected and the bus might be released, depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, transmission, or reception. Operation after rewriting under these conditions is not guaranteed. When reading these bits, the state of signals output from the IIC can be read.

CLO bit (Extra SCL Clock Cycle Output)

The CLO bit allows output of an extra SCL clock cycle for debugging or error processing. Normally, set this bit to 0. Setting the bit to 1 in a normal communication state causes a communication error. For details on this function, see section 31.12.2. Extra SCL Clock Cycle Output Function.

IICRST bit (I^2C Bus Interface Internal Reset)

The IICRST bit initiates an internal state reset of the IIC. Setting this bit to 1 initiates an IIC reset or internal reset. Whether an IIC reset or internal reset is initiated is determined by the settings of this bit in combination with the ICE bit. Table 31.3 lists the IIC resets.

The IIC reset initializes all registers except ICCR1.ICE and ICCR1.IICRST bits and internal states of the IIC. In addition to the internal states of the IIC, the internal reset initializes the following:

- Bit counter (ICMR1.BC[2:0] bits)
- I^2C Bus Shift Register (ICDRS)
- I^2C Bus Status Registers (ICSR1 and ICSR2)
- SDAO and SCLO Output Control/Monitor (ICCR1.SDAO and ICCR1.SCLO bits)

Bit	Symbol	Function	R/W
1	SCLI	SCL线路监视器 0：SCLn线低1：SC Ln线高	R
2	SDAO	SDA Output Control/Monitor 0：读：IIC将SDAn引脚驱动为低电平 写：IIC将SDAn引脚驱动为低电平 1：读：IIC释放SDAn引脚写：I C释放SDAn引脚	R/W
3	SCLO	SCL Output Control/Monitor 使用外部上拉电阻将信号驱动为高电平。 0：读：IIC将SCLn引脚驱动为低电平写 ：IIC将SCLn引脚驱动为低电平 1：读：IIC释放SCLn引脚写：IIC 释放SCLn引脚	R/W
4	SOWP	SCLOSDAO写保护 该位读为1。 0：写使能SCLO和SDAO位1：写保护S CLO和SDAO位	W
5	CLO	额外的SCL时钟周期输出 该位在输出1个时钟周期后自动清零。 0：不输出额外的SCL时钟周期（默认）1：输出 额外的SCL时钟周期	R/W
6	IICRST	I2C总线接口内部复位 该设置清除位计数器和SCLnSDAn输出锁存器。 0：释放IIC复位或内部复位1：启动IIC 复位或内部复位	R/W
7	ICE	I2C总线接口使能 与IICRST位结合使用来选择IIC或内部复位。 0：禁用（SCLn和SDAn引脚处于非活动状态）1： 启用（SCLn和SDAn引脚处于活动状态）	R/W

SDAO位（SDA输出控制监视器）和SCLO位（SCL输出控制监视器）

SDAO和SCLO位直接控制IIC输出的SDAn和SCLn信号。写入这些位时，还要向SOWP位写入0。设置这些位会导致输入缓冲器向IIC输入。选择从模式时，可能会检测到启动条件并释放总线，具体取决于位设置。

不要在开始条件、停止条件、重启条件、发送或接收期间重写这些位。不保证在这些条件下重写后的操作。读取这些位时，可以读取IIC输出的信号状态。

CLO位（额外SCL时钟周期输出）

CLO位允许输出额外的SCL时钟周期用于调试或错误处理。通常，将此位设置为0。在正常通信状态下将此位设置为1会导致通信错误。有关此功能的详细信息，请参阅第31.12.2节。额外的SCL时钟周期输出功能。

IICRST位（I2C总线接口内部复位）

IICRST位启动IIC的内部状态复位。将此位设置为1会启动IIC复位或内部复位。是IIC复位还是内部复位由该位的设置和ICE位共同决定。表31.3列出了IIC复位。

IIC复位初始化除ICCR1.ICE和ICCR1.IICRST位和IIC内部状态之外的所有寄存器。除了IIC的内部状态之外，内部复位还会初始化以下内容：

- ●位计数器（ICMR1.BC[2:0]位）
- ●I2C总线移位寄存器(ICDRS)
- ●I2C总线状态寄存器（ICSR1和ICSR2）
- ●SDAO和SCLO输出控制监视器（ICCR1.SDAO和ICCR1.SCLO位）

- I2C Bus Control Register 2 (except ICCR2.BBSY bit)

●I2C总线控制寄存器2（ICCR2.BBSY位除外）

For the reset conditions for each register, see section 31.15. State of Registers When Issuing Each Condition.

关于各寄存器的复位条件，请参阅31.15节。发出每个条件时的寄存器状态。

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the IIC without initializing the port settings and the control and setting registers of the IIC. If the IIC hangs in a low-level output state, resetting the internal states cancels the low-level output state and releases the bus with the SCLn pin and SDAn pin at high impedance.

在操作期间将IICRST位设置为1（ICE位设置为1）启动的内部复位会复位IIC的内部状态，而无需初始化IIC的端口设置以及控制和设置寄存器。如果IIC在低电平输出状态下挂起，复位内部状态会取消低电平输出状态并释放总线，同时SCLn引脚和SDAn引脚处于高阻抗状态。

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up that occurs during communication with the master device in slave mode, the slave and master devices might enter different states, because the bit counter information differs. For this reason, do not initiate an internal reset in slave mode. Initiate recovery processing from the master device. If an internal reset is required because the IIC hangs with the SCLn line in a low-level output state in slave mode, initiate an internal reset, then issue a restart condition from the master device, or issue a stop condition and resume communication from the start condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start or restart condition from the master device, synchronization is lost because the master and slave devices operate asynchronously.

Note: 如果在从模式下与主设备通信期间发生的总线挂断使用IICRST位启动内部复位，则从设备和主设备可能会进入不同的状态，因为位计数器信息不同。因此，不要在从模式下启动内部复位。从主设备启动恢复处理。如果由于IIC在从模式下挂起且SCLn线处于低电平输出状态而需要内部复位，则启动内部复位，然后从主设备发出重新启动条件，或者发出停止条件并从主设备恢复通信开始条件。如果通过仅在从设备中启动复位来重新启动通信，而没有从主设备发出启动或重启条件，则由于主设备和从设备异步操作而失去同步。

Table 31.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	Resets all registers except ICCR1.IICRST and ICCR1.ICE bits, and the internal states of the IIC
	1	Internal reset	Reset the following: ● ICMR1.BC[2:0] bits ● ICSR1, ICSR2, ICDRS registers ● SDAO and SCLO Output Control/Monitor (ICCR1.SDAO and ICCR1.SCLO bits) ● I2C Bus Control Register 2 (except ICCR2.BBSY bit) ● Internal states of the IIC

Table 31.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	复位除ICCR1.IICRST和ICCR1.ICE位之外的所有寄存器，以及IIC的内部状态
	1	内部复位	重置以下内容：● bits ● ICSR1, ICSR2, ICDRS registers ● SDAO和SCLO输出控制监视器（ICCR1.SDAO和ICCR1.SCLO bits) ● I2C总线控制寄存器2（ICCR2.BBSY位除外） ● IIC的内部状态

ICE bit (I2C Bus Interface Enable)

The ICE bit selects the active or inactive state of the SCLn and SDAn pins. It can also be combined with the IICRST bit to initiate two types of resets. See Table 31.3 for the reset descriptions.

Set the ICE bit to 1 when using the IIC. The SCLn and SDAn pins are placed in the active state when the ICE bit is set to 1. Set the ICE bit to 0 when the IIC is not used. The SCLn and SDAn pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCLn or SDAn pin to the IIC when setting up the pin function control. Slave address comparison is performed if the pins are assigned to the IIC.

ICE位（I2C总线接口使能）

ICE位选择SCLn和SDAn引脚的有效或无效状态。它也可以与IICRST位组合来启动两种类型的复位。复位说明见表31.3。

使用IIC时将ICE位设置为1。当ICE位设置为1时，SCLn和SDAn引脚处于活动状态。不使用IIC时，将ICE位设置为0。当ICE位设置为0时，SCLn和SDAn引脚处于非活动状态。在设置引脚功能控制时，不要将SCLn或SDAn引脚分配给IIC。如果引脚分配给IIC，则执行从地址比较。

31.2.2 ICCR2 : I2C Bus Control Register 2

31.2.2 ICCR2:I2C总线控制寄存器2

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)
Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)
Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	BBSY	MST	TRS	—	SP	RS	ST	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	ST	Start Condition Issuance Request 0: Do not issue a start condition request 1: Issue a start condition request	R/W
2	RS	Restart Condition Issuance Request 0: Do not issue a restart condition request 1: Issue a restart condition request	R/W

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	ST	开始条件发布请求 0：不发出启动条件请求1：发出启动条件请求	R/W
2	RS	重启条件发布请求 0：不发出重启条件请求1：发出重启条件请求	R/W

Bit	Symbol	Function	R/W
3	SP	Stop Condition Issuance Request 0: Do not issue a stop condition request 1: Issue a stop condition request	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W
5	TRS	Transmit/Receive Mode 0: Receive mode 1: Transmit mode	R/W*1
6	MST	Master/Slave Mode 0: Slave mode 1: Master mode	R/W*1
7	BBSY	Bus Busy Detection Flag 0: I2C bus released (bus free state) 1: I2C bus occupied (bus busy state)	R

Note 1. The MST and TRS bits can be written to when the ICMR1.MTWP bit is set to 1.

ST bit (Start Condition Issuance Request)

The ST bit requests transition to master mode and triggers a start condition. When this bit is set to 1, a start condition is issued when the BBSY flag is set to 0 (bus free state). For details on this function, see section 31.11. Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit.

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Only set the ST bit to 1 (start condition request) when the BBSY flag is set to 0 (bus free state). Arbitration might be lost if the ST bit is set to 1 (start condition request) when the BBSY flag is 1 (bus busy state).

RS bit (Restart Condition Issuance Request)

The RS bit requests that a restart condition be issued in master mode. When this bit is set to 1 to request a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 31.11. Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (restart condition request) is written to the RS bit in slave mode, the restart condition is not issued, but the RS bit remains set to 1. If the operating mode changes to master mode without the bit being cleared, a restart condition might be issued.

Bit	Symbol	Function	R/W
3	SP	停止条件发出请求 0：不发出停止条件请求1：发出停止条件请求	R/W
4	—	该位读取为0。写入值应为0。	R/W
5	TRS	Transmit/Receive Mode 0：接收模式1：发送模式	R/W*1
6	MST	Master/Slave Mode 0：从模式1：主模式	R/W*1
7	BBSY	总线忙检测标志 0：I2C总线释放（总线空闲状态）1：I2C总线占用（总线忙状态）	R

注1.当ICMR1.MTWP位设置为1时，可以写入MST和TRS位。

ST位（开始条件发布请求）

ST位请求转换到主模式并触发启动条件。当该位设置为1时，当BBSY标志设置为0（总线空闲状态）时发出启动条件。有关此功能的详细信息，请参阅第31.11节。启动、重启和停止条件发布功能。

[Setting condition]

●ST位写入1时。

[Clearing conditions]

●ST位写入0时

●发出启动条件时（检测到启动条件）

●ICSR2中的AL（仲裁失败）标志设置为1时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 仅当BBSY标志设置为0（总线空闲状态）时，才将ST位设置为1（启动条件请求）。如果在BBSY标志为1（总线繁忙状态）时将ST位设置为1（开始条件请求），则仲裁可能会丢失。

RS位（重启条件发布请求）

RS位请求在主机模式下发出重启条件。当该位设置为1以请求重新启动条件时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出重新启动条件。有关此功能的详细信息，请参阅第31.11节。启动、重启和停止条件发布功能。

[Setting condition]

●当ICCR2中的BBSY标志设置为1时，将1写入RS位。

[Clearing conditions]

●向RS位写入0时

●发出重新启动条件时（检测到启动条件）

●ICSR2中的AL（仲裁失败）标志设置为1时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 发出停止条件时不要将RS位设置为1。
Note: 如果在从模式下将1（重新启动条件请求）写入RS位，则不会发出重新启动条件，但RS位保持设置为1。如果操作模式更改为主模式而未清除该位，则重新启动条件可能会发出。

SP bit (Stop Condition Issuance Request)

The SP bit requests that a stop condition be issued in master mode. When this bit is set to 1, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 31.11. Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition is issued (a stop condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Writing to the SP bit is not possible while the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 while a restart condition is being issued.

TRS bit (Transmit/Receive Mode)

The TRS bit indicates transmit or receive mode. The IIC is in receive mode when the TRS bit is 0 and in transmit mode when the bit is 1. The combination of this bit and the MST bit indicates the IIC operating mode.

The value of the TRS bit automatically changes to 1 for transmit mode or 0 for receive mode when a start condition is issued or detected and the R/W# bit is set. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not required during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally because of a restart condition request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit appended to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When the R/W# bit appended to the slave address is set to 1 in master mode
- In slave mode, on a match between the received address and the address enabled in ICSER when the value of the received R/W# bit is 0, including when the received address is the general call address
- In slave mode, when a restart condition is detected (a restart condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

MST bit (Master/Slave Mode)

The MST bit indicates master or slave mode. The IIC is in slave mode when the MST bit is 0 and is in master mode when the bit is 1. The combination of this bit and the TRS bit indicates the IIC operating mode.

The value of the MST bit automatically changes to 1 for master mode or 0 for slave mode when a start condition is issued or a stop condition is issued or detected. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not required during normal usage.

SP位（停止条件发布请求）

SP位请求在主机模式下发出停止条件。当该位设置为1时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出停止条件。有关此功能的详细信息，请参阅第31.11节。启动、重启和停止条件发布功能。

[Setting condition]

●当ICCR2中的BBSY标志和MST位都设置为1时，将1写入SP位。

[Clearing conditions]

●SP位写入0时
●发出停止条件时（检测到停止条件）
●ICSR2中的AL（仲裁失败）标志设置为1时
●检测到启动条件和重启条件时
●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当BBSY标志为0（总线空闲状态）时，不能写入SP位。
Note: 发出重启条件时不要将SP位设置为1。

TRS bit (Transmit/Receive Mode)

TRS位指示发送或接收模式。TRS位为0时IIC处于接收模式，该位为1时IIC处于发送模式。该位和MST位的组合表示IIC工作模式。

当发出或检测到启动条件并且设置RW#位时，TRS位的值自动更改为1（发送模式）或0（接收模式）。虽然当ICMR1的MTWP位设置为1时可以写入TRS位，但在正常使用期间不需要写入该位。

[Setting conditions]

●因启动条件请求而正常发出启动条件时（ST位设置为1时检测到启动条件时）

●因重新启动条件请求而正常发出重新启动条件时（在RS位设置为1的情况下检测到重新启动条件时）

●在主机模式下，附加在从机地址上的RW#位设置为0时
●从机模式接收到的地址与ICSER中使能的地址匹配时，RW#位设置为1
●当ICMR1中的MTWP位设置为1时将1写入TRS位。

[Clearing conditions]

●检测到停止条件时
●ICSR2中的AL（仲裁失败）标志设置为1时
●在主机模式下，附加在从机地址上的RW#位设置为1时
●从机模式下，当接收到的RW#位的值为0时，接收到的地址与ICSER中使能的地址匹配，包括当接收到的地址是广播地址时
●在从模式下，检测到重启条件时（检测到重启条件时ICCR2.BBSY=1和ICCR2.MST=0）

●当ICMR1中的MTWP位设置为1时，将0写入TRS位时
●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

MST bit (Master/Slave Mode)

MST位指示主机或从机模式。当MST位为0时，IIC处于从机模式，当该位为1时，IIC处于主机模式。该位和TRS位的组合表示IIC工作模式。

当发出启动条件或发出或检测到停止条件时，MST位的值自动变为1（主机模式）或0（从机模式）。虽然当ICMR1中的MTWP位设置为1时可以写入MST位，但在正常使用期间不需要写入该位。

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

BBSY flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I^2C bus is occupied (bus busy state) or released (bus free state). The flag is set to 1 when the SDAn line changes from high to low when the SCLn line is high, assuming that a start condition was issued. The flag is set to 0 if a start condition is not detected for the bus free time (ICBRL setting), assuming that a stop condition was issued.

[Setting condition]

- When a start condition is detected.

[Clearing conditions]

- When a start condition is not detected for the bus free time (ICBRL setting) after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (IIC reset).

31.2.3 ICMR1 : I^2C Bus Mode Register 1

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	BC[2:0]	Bit Counter 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W*1
3	BCWP	BC Write Protect This bit is read as 1. 0: Write enable BC[2:0] bits 1: Write protect BC[2:0] bits	W*1
6:4	CKS[2:0]	Internal Reference Clock Select Select the internal reference clock source (IICφ) for the IIC. IICφ = (PCLKB / $2^{CKS[2:0]}$) clock	R/W
7	MTWP	MST/TRS Write Protect 0: Write protect MST and TRS bits in ICCR2 1: Write enable MST and TRS bits in ICCR2	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

[Setting conditions]

●因启动条件请求而正常发出启动条件时（ST位设置为1时检测到启动条件时）

●当ICMR1中的MTWP位设置为1时将1写入MST位。

[Clearing conditions]

●检测到停止条件时

●ICSR2中的AL（仲裁失败）标志设置为1时

●当ICMR1中的MTWP位设置为1时，将0写入MST位时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

BBSY标志（总线忙检测标志）

BBSY标志指示I2C总线是被占用（总线繁忙状态）还是被释放（总线空闲状态）。当SCLn线为高时SDAn线从高变为低时，该标志设置为1，假设发出了启动条件。如果在总线空闲时间（ICBRL设置）没有检测到启动条件，则该标志设置为0，假设发出了停止条件。

[Setting condition]

●检测到启动条件时。

[Clearing conditions]

●检测到停止条件后，在总线空闲时间（ICBRL设置）内未检测到启动条件时

●当ICCR1的IICRST位写入1且ICCR1的ICE位设置为0时（IIC复位）。

31.2.3 ICMR1:I2C总线模式寄存器1

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MTWP	CKS[2:0]			BCWP	BC[2:0]		
重置后的值:	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
2:0	BC[2:0]	位计数器 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W*1
3	BCWP	BC写保护 该位读为1。 0：写使能BC[2:0]位1：写保护BC[2:0]位	W*1
6:4	CKS[2:0]	内部参考时钟选择 选择IIC的内部参考时钟源(IICφ)。 IICφ = (PCLKB / $2^{CKS[2:0]}$) clock	R/W
7	MTWP	MSTTRS写保护 0：写保护ICCR2中的MST和TRS位1：写使能ICCR2中的MST和TRS位	R/W

注1.重写BC[2:0]位，同时将BCWP位设置为0。

BC[2:0] bits (Bit Counter)

The BC[2:0] bits function as a counter indicating the number of bits remaining to be transferred on detection of a rising edge on the SCLn line. Although BC[2:0] are read/write bits, it is not required to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one, for an additional acknowledge bit, between transferred frames when the SCLn line is at a low level. The value in the BC[2:0] bits returns to 000b at the end of a data transfer, including the acknowledge bit, or when a start or restart condition is detected.

31.2.4 ICMR2 : I²C Bus Mode Register 2

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Function	R/W
0	TMOS	Timeout Detection Time Select 0: Select long mode 1: Select short mode	R/W
1	TMOL	Timeout L Count Control 0: Disable count while SCLn line is low 1: Enable count while SCLn line is low	R/W
2	TMOH	Timeout H Count Control 0: Disable count while SCLn line is high 1: Enable count while SCLn line is high	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	SDDL[2:0]	SDA Output Delay Counter 0 0 0: No output delay 0 0 1: 1 IICφ cycle (When ICMR2.DLCS = 0 (IICφ)) 1 or 2 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 0 1 0: 2 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 3 or 4 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 0 1 1: 3 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 5 or 6 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 0 0: 4 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 7 or 8 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 0 1: 5 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 9 or 10 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 1 0: 6 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 11 or 12 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2)) 1 1 1: 7 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 13 or 14 IICφ cycles (When ICMR2.DLCS = 1 (IICφ/2))	R/W
7	DLCS	SDA Output Delay Clock Source Select 0: Select internal reference clock (IICφ) as the clock source for SDA output delay counter 1: Select internal reference clock divided by 2 (IICφ/2) as the clock source for SDA output delay counter*1	R/W

Note 1. The setting DLCS = 1 (IICφ/2) is only valid when SCL is low. When SCL is high, the DLCS = 1 setting becomes invalid and the clock source becomes the internal reference clock (IICφ).

TMOS bit (Timeout Detection Time Select)

The TMOS bit selects long or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE = 1). When this bit is set to 0, long mode is selected. When it is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14- bit counter. While the SCLn line is in the state that enables this counter as specified in the TMOH and TMOL bits, the counter

BC[2:0] bits (Bit Counter)

BC[2:0]位用作计数器，指示在检测到SCLn线上的上升沿时要传输的剩余位数。虽然BC[2:0]是读写位，但在正常情况下不需要访问这些位。

要写入这些位，在SCLn线处于低电平时，指定要传输的位数加1，作为附加确认位，在传输的帧之间。BC[2:0]位中的值在数据传输结束时返回到000b，包括确认位，或者当检测到启动或重启条件时。

31.2.4 ICMR2:I2C总线模式寄存器2

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
重置后的值:	0	0	0	0	0	1	1	0

Bit	Symbol	Function	R/W
0	TMOS	超时检测时间选择 0：选择长模式1：选择短模式	R/W
1	TMOL	超时L计数控制 0：SCLn线为低电平时禁止计数1：SCLn线为低电平时使能计数	R/W
2	TMOH	超时H计数控制 0：SCLn线为高电平时禁止计数1：SCLn线为高电平时使能计数	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	SDDL[2:0]	SDA输出延迟计数器 000：无输出延迟001：1个IICφ周期（当ICMR2.DLCS=0(IICφ)时） 1或2个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 0 1 0: 2 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 3或4个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 0 1 1: 3 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 5或6个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 0 0: 4 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 7或8个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 0 1: 5 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 9或10个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 1 0: 6 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 11或12个IICφ周期（当ICMR2.DLCS=1(IICφ2)时） 1 1 1: 7 IICφ cycles (When ICMR2.DLCS = 0 (IICφ)) 13或14个IICφ周期（当ICMR2.DLCS=1(IICφ2)时）	R/W
7	DLCS	SDA输出延迟时钟源选择 0：选择内部参考时钟（IICφ）作为SDA输出延迟计数器的时钟源 1：选择内部参考时钟除以2(IICφ2)作为SDA输出延迟计数器的时钟源*1	R/W

注1.设置DLCS=1(IICφ2)仅在SCL为低电平时有效。当SCL为高电平时，DLCS=1设置无效，时钟源变为内部参考时钟(IICφ)。

TMOS位（超时检测时间选择）

当使能超时功能（ICFER.TMOE=1）时，TMOS位为超时检测时间选择长模式或短模式。当该位设置为0时，选择长模式。当设置为1时，选择短模式。在长模式下，超时检测内部计数器用作16位计数器。在短模式下，计数器用作14位计数器。当SCLn线处于启用TMOH和TMOL位中指定的计数器的状态时，计数器

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counts up in synchronization with the internal reference clock (IICφ) as a count source. For details on this function, see section 31.12.1. Timeout Function.

TMOL bit (Timeout L Count Control)

The TMOL bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held low and the timeout function is enabled (ICFER.TMOE = 1).

TMOH bit (Timeout H Count Control)

The TMOH bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held high and the timeout function is enabled (ICFER.TMOE = 1).

SDDL[2:0] bits (SDA Output Delay Counter)

The SDDL[2:0] bits can be used to delay the SDA output. This counter works with the clock source selected in the DLCS bit. This setting can be used for all types of SDA output, including transmission of the acknowledge bit.

Set the SDA output delay to meet the I²C bus standard for the data enable time/acknowledge enable time,*1 or the SMBus standard, within [data hold time (300 ns or more + the SCL clock low-level period) - the data setup time (250 ns)]. If a value outside the standard is set, communication between devices might malfunction or falsely indicate a start or stop condition, depending on the bus state.

For details on this function, see section 31.5. SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time.
3,450 ns for up to 100 kbps: Standard mode (Sm)
900 ns for up to 400 kbps: Fast mode (Fm)
450 ns for up to 1 Mbps: Fast-mode Plus (Fm+)

31.2.5 ICMR3 : I²C Bus Mode Register 3

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	NF[1:0]	Noise Filter Stage Select 0 0: Filter out noise of up to 1 IICφ cycle (single-stage filter) 0 1: Filter out noise of up to 2 IICφ cycles (2-stage filter) 1 0: Filter out noise of up to 3 IICφ cycles (3-stage filter) 1 1: Filter out noise of up to 4 IICφ cycles (4-stage filter)	R/W
2	ACKBR	Receive Acknowledge 0: 0 received as the acknowledge bit (ACK reception) 1: 1 received as the acknowledge bit (NACK reception)	R
3	ACKBT	Transmit Acknowledge 0: Send 0 as the acknowledge bit (ACK transmission) 1: Send 1 as the acknowledge bit (NACK transmission)	R/W*1
4	ACKWP	ACKBT Write Protect 0: Write protect ACKBT bit 1: Write enable ACKBT bit	R/W
5	RDRFS	RDRF Flag Set Timing Select Low-hold is released by writing to ACKBT. 0: Set the RDRF flag on the rising edge of the 9th SCL clock cycle. The SCLn line is not held low on the falling edge of the 8th clock cycle. 1: Set the RDRF flag on the rising edge of the 8th SCL clock cycle. The SCLn line is held low on the falling edge of the 8th clock cycle.	R/W*2

与作为计数源的内部参考时钟(IICφ)同步计数。有关此功能的详细信息，请参阅第31.12.1节。超时功能。

TMOL位（超时L计数控制）

TMOL位启用或禁用超时功能内部计数器的递增计数，同时SCLn线保持低电平且启用超时功能(ICFER.TMOE=1)。

TMOH位（超时H计数控制）

TMOH位启用或禁用超时功能内部计数器的递增计数，同时SCLn线保持高电平且启用超时功能(ICFER.TMOE=1)。

SDDL[2:0]位（SDA输出延迟计数器）

SDDL[2:0]位可用于延迟SDA输出。该计数器与在DLCS位中选择的时钟源一起工作。该设置可用于所有类型的SDA输出，包括确认位的传输。

将SDA输出延迟设置为满足I2C总线标准的数据使能时间确认使能时间，*1或SMBus标准，在[数据保持时间（300 ns或更长+SCL时钟低电平周期）内的数据建立时间（250ns）]。如果设置了超出标准的值，则设备之间的通信可能会发生故障或错误地指示开始或停止条件，具体取决于总线状态。

有关此功能的详细信息，请参阅第31.5节。SDA输出延迟功能。

注1.数据使能时间确认使能时间。
3 450ns，最高100kbps：标准模式(Sm)
900ns，最高400kbps：快速模式(Fm)
高达1Mbps时为450ns：Fast-modePlus(Fm+)

31.2.5 ICMR3:I2C总线模式寄存器3

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	NF[1:0]	噪声过滤级选择 00：最多过滤1个IICφ周期的噪声（单级滤波器）01：最多过滤2个IICφ周期的噪声（2级滤波器）10：最多过滤3个IICφ周期的噪声（3级滤波器）11：过滤掉最多4个IICφ周期的噪声（4级滤波器）	R/W
2	ACKBR	接收确认 0：0作为确认位接收（ACK接收）1：1作为确认位接收（NACK接收）	R
3	ACKBT	发送确认 0：发送0作为确认位（ACK发送）1：发送1作为确认位（NACK发送）	R/W*1
4	ACKWP	ACKBT写保护 0：写保护ACKBT位1：写使能ACKBT位	R/W
5	RDRFS	RDRF标志设置时序选择 通过写入ACKBT释放低保持。 0：在第9个SCL时钟周期的上升沿设置RDRF标志。SCLn线在第8个时钟周期的下降沿不保持低电平。 1：在第8个SCL时钟周期的上升沿设置RDRF标志。SCLn线在第8个时钟周期的下降沿保持低电平。	R/W*2

Bit	Symbol	Function	R/W
6	WAIT	Low-hold is released by reading ICDRR. 0: No wait (The SCLn line is not held low during the period between the 9th clock cycle and the 1st clock cycle.) 1: Wait (The SCLn line is held low during the period between the 9th clock cycle and the 1st clock cycle.)	R/W*2
7	SMBS	SMBus/I2C Bus Select 0: Select I2C Bus 1: Select SMBus	R/W

Note 1. Write to the ACKBT bit only while the ACKWP bit is already 1. If the application writes 1 to the ACKWP and ACKBT bits at the same time, the ACKBT bit is not set to 1.
Note 2. The WAIT and RDRFS bits are only valid in receive mode (invalid in transmit mode).

NF[1:0] bits (Noise Filter Stage Select)

The NF[1:0] bits select the number of stages in the digital noise filter. For details on this function, see section 31.6. Digital Noise Filter Circuits

Note: Set the noise range to be filtered within a range less than the SCLn line high- or low-level period. If the noise range is set to a value of [SCL clock width: high- or low-level period, whichever is shorter] - [1.5 internal reference clock (IICφ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise, which might prevent the IIC from operating normally.

ACKBR bit (Receive Acknowledge)

The ACKBR bit stores the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKBT bit (Transmit Acknowledge)

The ACKBT bit sets the acknowledge bit to be sent in receive mode

[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1.

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition request is detected with the SP bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKWP bit (ACKBT Write Protect)

The ACKWP bit controls write enabling of the ACKBT bit.

RDRFS bit (RDRF Flag Set Timing Select)

The RDRFS bit selects the RDRF flag set timing in receive mode and also selects whether to hold the SCLn line low on the falling edge of the 8th SCL clock cycle.

When the RDRFS bit is 0, the SCLn line is not held low on the falling edge of the 8th SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

When the RDRFS bit is 1, the RDRF flag is set to 1 on the rising edge of the 8th SCL clock cycle, and the SCLn line is held low on the falling edge of the 8th SCL clock cycle. The low-hold of the SCLn line is released by a write to the ACKBT bit.

After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1), based on the receive data.

Bit	Symbol	Function	R/W
6	WAIT	通过读取ICDRR释放低保持。 0：无等待（在第9个时钟周期和第1个时钟周期之间的时间段内，SCLn线不保持低电平。） 1：等待（SCLn线在第9个时钟周期和第1个时钟周期之间保持低电平。）	R/W*2
7	SMBS	SMBusI2C总线选择 0：选择I2C总线1 ：选择SMBus	R/W

注1.仅当ACKWP位已经为1时才写入ACKBT位。如果应用程序同时向ACKWP和ACKBT位写入1，则ACKBT位不会设置为1。

注2.WAIT和RDRFS位仅在接收模式下有效（在发送模式下无效）。

NF[1:0]位（噪声滤波器级选择）

NF[1:0]位选择数字噪声滤波器的级数。关于该功能的详细内容，请参阅31.6节。数字的噪声滤波电路

Note: 将要过滤的噪声范围设置在小于SCLn线高电平或低电平周期的范围内。如果噪声范围设置为[SCL时钟宽度：高电平或低电平周期，以较短者为准][1.5内部参考时钟(IICφ)周期+模拟噪声滤波器：120ns（参考值）]或更大的值，则SCL时钟被视为噪声，可能会妨碍IIC正常工作。

ACKBR bit (Receive Acknowledge)

ACKBR位存储在发送模式下从接收设备接收到的确认位信息。

[Setting condition]

●当ICCR2中的TRS位设置为1接收到1作为确认位时。

[Clearing conditions]

●当ICCR2中的TRS位设置为1接收到0作为确认位时

●当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKBT bit (Transmit Acknowledge)

ACKBT位设置要在接收模式下发送的确认位

[Setting condition]

●当1写入该位且ACKWP位设置为1时。

[Clearing conditions]

●当0写入该位且ACKWP位设置为1时

●ICCR2的SP位设置为1时检测到停止条件请求时

●当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKWP位（ACKBT写保护）

ACKWP位控制ACKBT位的写使能。

RDRFS位（RDRF标志设置时序选择）

RDRFS位选择接收模式下的RDRF标志设置时序，并选择是否在第8个SCL时钟周期的下降沿保持SCLn线为低电平。

当RDRFS位为0时，SCLn线在第8个SCL时钟周期的下降沿不保持低电平，并且RDRF标志在第9个SCL时钟周期的上升沿设置为1。

当RDRFS位为1时，RDRF标志在第8个SCL时钟周期的上升沿设置为1，并且SCLn线在第8个SCL时钟周期的下降沿保持低电平。SCLn线的低保持通过写ACKBT位来释放。

使用此设置接收数据后，SCLn线在发送确认位之前自动保持低电平。这使处理能够根据接收数据发送ACK(ACKBT=0)或NACK(ACKBT=1)。

WAIT bit (WAIT)

The WAIT bit controls whether to force a low-hold between the ninth SCL clock cycle and the first SCL clock cycle, until the receive data buffer (ICDRR) is completely read each time single-byte data is received in receive mode.

When the WAIT bit is 0, the receive operation continues without a low-hold between the ninth and the first SCL clock cycle. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.

When the WAIT bit is 1, the SCLn line is held low from the falling edge of the ninth clock cycle until the ICDRR value is read each time single-byte data is received. This enables receive operation in byte units.

Note: When the value of the WAIT bit is to be read, always read ICDRR first.

SMBS bit (SMBus/I²C Bus Select)

Setting the SMBS bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

31.2.6 ICFER : I²C Bus Function Enable Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FMPE	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	TMOE	Timeout Function Enable 0: Disable 1: Enable	R/W
1	MALE	Master Arbitration-Lost Detection Enable 0: Disable the arbitration-lost detection function and disable automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost 1: Enable the arbitration-lost detection function and enable automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost	R/W
2	NALE	NACK Transmission Arbitration-Lost Detection Enable 0: Disable 1: Enable	R/W
3	SALE	Slave Arbitration-Lost Detection Enable 0: Disable 1: Enable	R/W
4	NACKE	NACK Reception Transfer Suspension Enable 0: Do not suspend transfer operation during NACK reception (disable transfer suspension) 1: Suspend transfer operation during NACK reception (enable transfer suspension)	R/W
5	NFE	Digital Noise Filter Circuit Enable 0: Do not use the digital noise filter circuit 1: Use the digital noise filter circuit	R/W
6	SCLE	SCL Synchronous Circuit Enable 0: Do not use the SCL synchronous circuit 1: Use the SCL synchronous circuit	R/W
7	FMPE*1	Fast-Mode Plus Enable 0: Do not use the Fm+ slope control circuit for the SCLn and SDAn pins 1: Use the Fm+ slope control circuit for the SCLn and SDAn pins.	R/W

Note 1. The Fast-mode Plus enable bit (FMPE) is supported by IIC0 (SCL0_A, SDA0_A) and IIC1(SCL1_A, SDA1_A). Bit [7] is the reserved bit in the not supported channel.

TMOE bit (Timeout Function Enable)

The TMOE bit enables or disables the timeout function. For details on this function, see section 31.12.1. Timeout Function.

等待位（等待）

WAIT位控制是否在第9个SCL时钟周期和第一个SCL时钟周期之间强制保持低电平，直到每次在接收模式下接收到单字节数据时完全读取接收数据缓冲区(ICDRR)。

当WAIT位为0时，接收操作继续，在第9个和第一个SCL时钟周期之间没有低电平保持。当RDRFS和WAIT位都为0时，双缓冲器使能连续接收操作。

当WAIT位为1时，SCLn线从第9个时钟周期的下降沿保持低电平，直到每次接收到单字节数据时读取ICDRR值。这启用了以字节为单位的接收操作。

Note: 当要读取WAIT位的值时，总是先读取ICDRR。

SMBS位（SMBusI2C总线选择）

将SMBS位设置为1可选择SMBus并启用ICSER中的HOAE位。

31.2.6 ICFER:I2C总线功能使能寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FMPE	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
重置后的值:	0	1	1	1	0	0	1	0

Bit	Symbol	Function	R/W
0	TMOE	超时功能启用 0：禁用1 ：启用	R/W
1	MALE	主仲裁丢失检测启用 0：禁止仲裁丢失检测功能，禁止仲裁丢失时自动清除ICCR2中的MST和TRS位 1：使能仲裁丢失检测功能，并在仲裁丢失时自动清除ICCR2中的MST和TRS位	R/W
2	NALE	NACK传输仲裁丢失检测使能 0：禁用1 ：启用	R/W
3	SALE	从设备仲裁丢失检测使能 0：禁用1 ：启用	R/W
4	NACKE	NACK接收传输暂停使能 0：在NACK接收期间不暂停传输操作（禁用传输暂停） 1：在NACK接收期间暂停传输操作（启用传输暂停）	R/W
5	NFE	数字噪声滤波器电路使能 0：不使用数字噪声滤波电路1：使用数字噪声滤波电路	R/W
6	SCLE	SCL同步电路使能 0：不使用SCL同步电路1：使用SCL同步电路	R/W
7	FMPE*1	快速模式加启用 0：SCLn和SDAn引脚不使用Fm+斜率控制电路1：SCLn和SDAn引脚使用Fm+斜率控制电路。	R/W

注1.IIC0(SCL0_A SDA0_A)和IIC1(SCL1_A SDA1_A)支持Fast-modePlus使能位(FMPE)。位[7]是不支持通道中的保留位。

TMOE位（超时功能使能）

TMOE位启用或禁用超时功能。有关此功能的详细信息，请参阅第31.12.1节。超时功能。

MALE bit (Master Arbitration-Lost Detection Enable)

The MALE bit specifies whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

The NALE bit specifies whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode, for example when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with a different number of receive bytes.

SALE bit (Slave Arbitration-Lost Detection Enable)

The SALE bit specifies whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode, for example when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs because of noise.

NACKE bit (NACK Reception Transfer Suspension Enable)

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received in transmit mode. Normally, set this bit to 1.

When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended. When the NACKE bit is 0, the next transfer operation continues regardless of the received acknowledge content.

For details, see section 31.9.2. NACK Reception Transfer Suspension Function.

SCLE bit (SCL Synchronous Circuit Enable)

The SCLE bit specifies whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCLE bit is set to 0 (no SCL synchronous circuit used), the IIC does not synchronize the SCL clock with the SCL input clock. With this setting, the IIC outputs the SCL clock at the transfer rate set in ICBRH and ICBRL, regardless of the SCLn line state. For this reason, if the bus load of the I^2C bus line is much larger than the specification value, or if the SCL clock output overlaps in multiple masters, a short-cycle SCL clock that does not meet the specification might be output.

When no SCL synchronous circuit is used, it also affects the issuing of the start, restart, and stop conditions, and the continuous output of extra SCL clock cycles.

Do not set this bit to 0 except when checking the output of the set transfer rate.

FMPE bit (Fast-Mode Plus Enable)

The FMPE bit specifies whether to use a slope control circuit for Fast-mode Plus (Fm+).

When this bit is set to 1, a slope control circuit conforming to the I^2C bus Fast-mode Plus (Fm+) standard (tof) is selected.
When this bit is set to 0, a slope control circuit conforming to the I^2C bus Standard-mode (Sm) and Fast-mode (Fm) standards (tof) is selected.

Set this bit to 1 when using transmission rates up to 1 Mbps (Fast-mode Plus (Fm+) standard). Set it to 0 when using other transmission rates (up to 100 kbps (Sm) or up to 400 kbps (Fm)) or for SMBus (10 to 100 kbps).

31.2.7 ICSER : I^2C Bus Status Enable Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Function	R/W
0	SAR0E	Slave Address Register 0 Enable 0: Disable slave address in SARL0 and SARU0 1: Enable slave address in SARL0 and SARU0	R/W

MALE位（主仲裁丢失检测使能）

MALE位指定是否在主机模式下使用仲裁丢失检测功能。通常，将此位设置为1。

NALE位（NACK传输仲裁丢失检测使能）

NALE位指定在接收模式下发送NACK期间检测到ACK时是否导致仲裁丢失，例如，当总线上存在具有相同地址的从设备时，或者当两个或多个主设备同时选择相同的从设备时接收字节数。

SALE位（从设备仲裁丢失检测使能）

SALE位指定当在从发送模式下在总线上检测到与正在发送的值不同的值时，是否导致仲裁丢失，例如，当总线上存在具有相同地址的从机或与发送数据不匹配时由于噪音而发生。

NACKE位（NACK接收传输暂停使能）

NACKE位指定在发送模式下接收到NACK时是继续还是停止传输操作。通常，将此位设置为1。

当在NACKE位设置为1的情况下接收到NACK时，暂停下一个传输操作。当NACKE位为0时，无论接收到的确认内容如何， 下一次传输操作都会继续进行。

有关详细信息，请参阅第31.9.2节。NACK接收传输暂停功能。

SCLE位（SCL同步电路使能）

SCLE位指定是否将SCL时钟与SCL输入时钟同步。通常，将此位设置为1。

当SCLE位设置为0（不使用SCL同步电路）时，IIC不会将SCL时钟与SCL输入时钟同步。使用此设置，无论SCLn线路状态如何，IIC都以ICBRH和ICBRL中设置的传输速率输出SCL时钟。因此，如果I2C总线的总线负载远大于规格值，或者多个主机的SCL时钟输出重叠，则可能会输出不符合规格的短周期SCL时钟。当不使用SCL同步电路时，也会影响启动、重启和停止条件的发出，以及额外SCL时钟周期的连续输出。

除非检查设置传输速率的输出，否则不要将此位设置为0。

FMPE位（Fast-ModePlusEnable）

FMPE位指定是否对Fast-modePlus(Fm+)使用斜率控制电路。

当该位设置为1时，选择符合I2C总线快速模式加(Fm+)标准(tof)的斜率控制电路。
当该位设置为0时，选择符合I2C总线标准模式(Sm)和快速模式(Fm)标准(tof)的斜率控制电路。

当使用高达1Mbps的传输速率（Fast-modePlus(Fm+)标准）时，将此位设置为1。当使用其他传输速率（最高100kbps(Sm)或最高400kbps(Fm)）或SMBus（10至100kbps）时，将其设置为0。

31.2.7 ICSER:I2C总线状态使能寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
重置后的值:	0	0	0	0	1	0	0	1

Bit	Symbol	Function	R/W
0	SAR0E	从地址寄存器0使能 0：禁用SARL0和SARU0中的从地址1：启用SARL0和SARU0中的从地址	R/W

Bit	Symbol	Function	R/W
1	SAR1E	Slave Address Register 1 Enable 0: Disable slave address in SARL1 and SARU1 1: Enable slave address in SARL1 and SARU1	R/W
2	SAR2E	Slave Address Register 2 Enable 0: Disable slave address in SARL2 and SARU2 1: Enable slave address in SARL2 and SARU2	R/W
3	GCAE	General Call Address Enable 0: Disable general call address detection 1: Enable general call address detection	R/W
4	—	This bit is read as 0. The write value should be 0.	R/W
5	DIDE	Device-ID Address Detection Enable 0: Disable device-ID address detection 1: Enable device-ID address detection	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	HOAE	Host Address Enable 0: Disable host address detection 1: Enable host address detection	R/W

SARyE bit (Slave Address Register y Enable) (y = 0 to 2)

The SARyE bit enables or disables the received slave address and the slave address set in SARLy and SARUy.

When this bit is set to 1, the slave address set in SARLy and SARUy is enabled and is compared with the received slave address. When this bit is set to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

GCAE bit (General Call Address Enable)

The GCAE bit specifies whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the IIC recognizes the received slave address as the general call address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the data receive operation. When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE bit (Device-ID Address Detection Enable)

The DIDE bit specifies whether to recognize and execute the device-ID address when a device ID (1111 100b) is received in the first frame after a start or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the IIC recognizes that the device-ID address was received. When the next R/W# bit is 0 (W), the IIC recognizes the second and the subsequent frames as slave addresses and continues the receive operation. When this bit is set to 0, the IIC ignores the received first frame even if it matches the device-ID address, and it recognizes the first frame as a normal slave address.

For details on this function, see section 31.7.3. Device-ID Address Detection.

HOAE bit (Host Address Enable)

The HOAE bit specifies whether to ignore the received host address (0001 000b) when the SMBS bit in ICMR3 is 1.

When this bit is set to 1 while the SMBS bit in ICMR3 is 1, if the received slave address matches the host address, the IIC recognizes the received slave address as the host address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the receive operation.

When the SMBS bit in ICMR3 or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

Bit	Symbol	Function	R/W
1	SAR1E	从地址寄存器1使能 0：禁用SARL1和SARU1中的从地址1：启用SARL1和SARU1中的从地址	R/W
2	SAR2E	从地址寄存器2使能 0：禁用SARL2和SARU2中的从地址1：启用SARL2和SARU2中的从地址	R/W
3	GCAE	广播呼叫地址启用 0：禁用广播地址检测1：启用广播地址检测	R/W
4	—	该位读取为0。写入值应为0。	R/W
5	DIDE	设备ID地址检测启用 0：禁用设备ID地址检测1：启用设备ID地址检测	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	HOAE	主机地址启用 0：禁用主机地址检测1：启用主机地址检测	R/W

SARyE位（从地址寄存器y使能）（y=0到2）

SARyE位启用或禁用接收到的从机地址和设置在SARLy和SARUy中的从机地址。

当该位设置为1时，设置在SARLy和SARUy中的从机地址被启用，并与接收到的从机地址进行比较。当该位设置为0时，设置在SARLy和SARUy中的从机地址被禁用并被忽略，即使它与接收到的从机地址匹配。

GCAE位（广播呼叫地址使能）

GCAE位指定接收到的广播调用地址（0000000b+0[W]：全0）是否忽略。

当该位设置为1时，如果接收到的从机地址与广播呼叫地址匹配，则IIC将接收到的从机地址识别为广播呼叫地址，而与在SARLy和SARUy中设置的从机地址（y=0到2）无关，并执行数据接收操作。当该位设置为0时，即使接收到的从机地址与广播呼叫地址匹配，也会忽略它。

DIDE位（设备ID地址检测使能）

DIDE位指定在检测到启动或重新启动条件后的第一帧中接收到设备ID(1111100b)时是否识别和执行设备ID地址。

当该位设置为1时，如果接收到的第一个帧与设备ID匹配，则IIC识别出设备ID地址已被接收。当下一个RW#位为0(W)时，IIC将第二个和后续帧识别为从地址并继续接收操作。当该位设置为0时，IIC忽略接收到的第一帧，即使它与设备ID地址匹配，并将第一帧识别为正常的从地址。

有关此功能的详细信息，请参阅第31.7.3节。设备ID地址检测。

HOAE位（主机地址使能）

HOAE位指定当ICMR3中的SMBS位为1时是否忽略接收到的主机地址（0001000b）。

当该位设置为1而ICMR3中的SMBS位为1时，如果接收到的从机地址与主机地址匹配，则IIC将接收到的从机地址识别为主机地址，而与SARLy和SARUy中设置的从机地址无关（y=0到2)并执行接收操作。

当ICMR3中的SMBS位或HOAE位设置为0时，即使接收到的从机地址与主机地址匹配，也会忽略它。

31.2.8 ICIER : I²C Bus Interrupt Enable Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOIE	Timeout Interrupt Request Enable 0: Disable timeout interrupt (TMOI) request 1: Enable timeout interrupt (TMOI) request	R/W
1	ALIE	Arbitration-Lost Interrupt Request Enable 0: Disable arbitration-lost interrupt (ALI) request 1: Enable arbitration-lost interrupt (ALI) request	R/W
2	STIE	Start Condition Detection Interrupt Request Enable 0: Disable start condition detection interrupt (STI) request 1: Enable start condition detection interrupt (STI) request	R/W
3	SPIE	Stop Condition Detection Interrupt Request Enable 0: Disable stop condition detection interrupt (SPI) request 1: Enable stop condition detection interrupt (SPI) request	R/W
4	NAKIE	NACK Reception Interrupt Request Enable 0: Disable NACK reception interrupt (NAKI) request 1: Enable NACK reception interrupt (NAKI) request	R/W
5	RIE	Receive Data Full Interrupt Request Enable 0: Disable receive data full interrupt (IICn_RXI) request 1: Enable receive data full interrupt (IICn_RXI) request	R/W
6	TEIE	Transmit End Interrupt Request Enable 0: Disable transmit end interrupt (IICn_TEI) request 1: Enable transmit end interrupt (IICn_TEI) request	R/W
7	TIE	Transmit Data Empty Interrupt Request Enable 0: Disable transmit data empty interrupt (IICn_TXI) request 1: Enable transmit data empty interrupt (IICn_TXI) request	R/W

TMOIE bit (Timeout Interrupt Request Enable)

The TMOIE bit enables or disables timeout interrupt (TMOI) requests when the TMOF flag in ICSR2 is 1. To cancel a TMOI interrupt request, set the TMOF flag or the TMOIE bit to 0.

ALIE bit (Arbitration-Lost Interrupt Request Enable)

The ALIE bit enables or disables arbitration-lost interrupt (ALI) requests when the AL flag in ICSR2 is 1. To cancel an ALI interrupt request, set the AL flag or the ALIE bit to 0.

STIE bit (Start Condition Detection Interrupt Request Enable)

The STIE bit enables or disables start condition detection interrupt (STI) requests when the START flag in ICSR2 is 1. To cancel an STI interrupt request, set the START flag or the STIE bit to 0.

SPIE bit (Stop Condition Detection Interrupt Request Enable)

The SPIE bit enables or disables stop condition detection interrupt (SPI) requests when the STOP flag in ICSR2 is 1. To cancel an SPI interrupt request, set the STOP flag or the SPIE bit to 0.

NAKIE bit (NACK Reception Interrupt Request Enable)

The NAKIE bit enables or disables NACK reception interrupt (NAKI) requests when the NACKF flag in ICSR2 is 1. To cancel an NAKI interrupt request, set the NACKF flag or the NAKIE bit to 0.

31.2.8 ICIER:I2C总线中断使能寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOIE	超时中断请求使能 0：禁用超时中断（TMOI）请求1：启用超时中断（TMOI）请求	R/W
1	ALIE	仲裁丢失中断请求使能 0：禁用仲裁丢失中断(ALI)请求1：启用仲裁丢失中断(ALI)请求	R/W
2	STIE	启动条件检测中断请求使能 0：禁止启动条件检测中断（STI）请求1：允许启动条件检测中断（STI）请求	R/W
3	SPIE	停止条件检测中断请求使能 0：禁止停止条件检测中断（SPI）请求1：使能停止条件检测中断（SPI）请求	R/W
4	NAKIE	NACK接收中断请求使能 0：禁止NACK接收中断（NAKI）请求1：允许NACK接收中断（NAKI）请求	R/W
5	RIE	接收数据满中断请求使能 0：禁止接收数据满中断（IICn_RXI）请求1：使能接收数据满中断（IICn_RXI）请求	R/W
6	TEIE	发送结束中断请求使能 0：禁止发送结束中断（IICn_TEI）请求1：允许发送结束中断（IICn_TEI）请求	R/W
7	TIE	发送数据空中断请求使能 0：禁止发送数据空中断（IICn_TXI）请求1：使能发送数据空中断（IICn_TXI）请求	R/W

TMOIE位（超时中断请求使能）

当ICSR2中的TMOF标志为1时，TMOIE位启用或禁用超时中断(TMOI)请求。取消一个TMOI中断请求，设置TMOF标志或TMOIE位为0。

ALIE位（仲裁失败中断请求使能）

当ICSR2中的AL标志为1时，ALIE位启用或禁用仲裁丢失中断(ALI)请求。要取消ALI中断请求，请将AL标志或ALIE位设置为0。

STIE位（启动条件检测中断请求使能）

当ICSR2中的START标志为1时，STIE位启用或禁用启动条件检测中断(STI)请求。要取消STI中断请求，请将START标志或STIE位设置为0。

SPIE位（停止条件检测中断请求使能）

当ICSR2中的STOP标志为1时，SPIE位启用或禁用停止条件检测中断(SPI)请求。要取消SPI中断请求，请将STOP标志或SPIE位设置为0。

NAKIE位（NACK接收中断请求使能）

当ICSR2中的NACKF标志为1时，NAKIE位启用或禁用NACK接收中断(NAKI)请求。要取消NAKI中断请求，请将NACKF标志或NAKIE位设置为0。

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RIE bit (Receive Data Full Interrupt Request Enable)

The RIE bit enables or disables receive data full interrupt (IICn_RXI) requests when the RDRF flag in ICSR2 is 1.

TEIE bit (Transmit End Interrupt Request Enable)

The TEIE bit enables or disables transmit end interrupt (IICn_TEI) requests when the TEND flag in ICSR2 is 1. To cancel an IICn_TEI interrupt request, set the TEND flag or the TEIE bit to 0.

TIE bit (Transmit Data Empty Interrupt Request Enable)

The TIE bit enables or disables transmit data empty interrupt (IICn_TXI) requests when the TDRE flag in ICSR2 is 1.

31.2.9 ICSR1 : I2C Bus Status Register 1

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AAS0	Slave Address 0 Detection Flag 0: Slave address 0 not detected 1: Slave address 0 detected	R/(W)*1
1	AAS1	Slave Address 1 Detection Flag 0: Slave address 1 not detected 1: Slave address 1 detected	R/(W)*1
2	AAS2	Slave Address 2 Detection Flag 0: Slave address 2 not detected 1: Slave address 2 detected	R/(W)*1
3	GCA	General Call Address Detection Flag 0: General call address not detected 1: General call address detected	R/(W)*1
4	—	This bit is read as 0. The write value should be 0.	R/W
5	DID	Device-ID Address Detection Flag This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0[W]). 0: Device-ID command not detected 1: Device-ID command detected	R/(W)*1
6	—	This bit is read as 0. The write value should be 0.	R/W
7	HOA	Host Address Detection Flag This bit is set to 1 when the received slave address matches the host address (0001 000b). 0: Host address not detected 1: Host address detected	R/(W)*1

Note 1. Only 0 can be written to clear the flag.

AASy flag (Slave Address y Detection flag) (y = 0 to 2)

The AASy flag indicates whether slave address y was detected.

[Setting conditions]

For 7-bit address format (SARUy.FS = 0):

- When the received slave address matches the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format: (SARUy.FS = 1):

RIE位（接收数据满中断请求使能）

当ICSR2中的RDRF标志为1时，RIE位启用或禁用接收数据完整中断(IICn_RXI)请求。

TEIE位（发送结束中断请求使能）

当ICSR2中的TEND标志为1时，TEIE位启用或禁用发送结束中断(IICn_TEI)请求。要取消IICn_TEI中断请求，请将TEND标志或TEIE位设置为0。

TIE位（发送数据空中断请求使能）

当ICSR2中的TDRE标志为1时，TIE位启用或禁用发送数据空中断（IICn_TXI）请求。

31.2.9 ICSR1:I2C总线状态寄存器1

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	AAS0	从地址0检测标志 0：未检测到从地址01：检测到从地址0	R/(W)*1
1	AAS1	从地址1检测标志 0：未检测到从地址11：检测到从地址1	R/(W)*1
2	AAS2	从地址2检测标志 0：未检测到从地址21：检测到从地址2	R/(W)*1
3	GCA	广播呼叫地址检测标志 0：未检测到广播呼叫地址1：检测到广播呼叫地址	R/(W)*1
4	—	该位读取为0。写入值应为0。	R/W
5	DID	设备ID地址检测标志 当检测到开始条件后立即接收到的第一个帧与(设备ID(1111100b)+0[W])的值匹配时，该位设置为1。 0：未检测到设备ID命令1：检测到设备ID命令	R/(W)*1
6	—	该位读取为0。写入值应为0。	R/W
7	HOA	主机地址检测标志 当接收到的从机地址与主机地址(0001000b)匹配时，该位设置为1。 0：未检测到主机地址1：检测到主机地址	R/(W)*1

注1.只能写入0来清除标志。

AASy标志（从机地址y检测标志）（y=0到2）

AASy标志指示是否检测到从地址y。

[Setting conditions]

对于7位地址格式(SARUy.FS=0)：

●当接收到的从地址与SARLy中的SVA[6:0]值匹配时，ICSER中的SARyE位设置为1（从地址y检测使能）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为1。

对于10位地址格式：(SARUy.FS=1)：

- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address matches the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy flag after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

For 7-bit address format (SARUy.FS = 0):

- When the received slave address does not match the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address does not match a value of (11110b + SVA[1:0] in SARUy), with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address does not match the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

GCA flag (General Call Address Detection Flag)

The GCA flag indicates whether the general call address was detected.

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled).
  The GCA flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA flag after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled)
  The GCA flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

DID flag (Device-ID Address Detection Flag)

The DID flag indicates whether the device-ID address was detected.

[Setting condition]

- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled).
  The DID flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID flag after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start or restart condition is detected does not match a value of (device ID (1111 100b)), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled)
  The DID flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

●当接收到的从地址与（SARUy中的11110b+SVA[1:0]）值匹配，并且后续地址与SARLy值匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取AASy=1后向AASy标志写入0时

●检测到停止条件时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

对于7位地址格式(SARUy.FS=0)：

●当接收到的从地址与SARLy中的SVA[6:0]值不匹配时，将ICSER中的SARyE位设置为1（启用从地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

对于10位地址格式(SARUy.FS=1)：

●当接收到的从地址与（SARUy中的11110b+SVA[1:0]）的值不匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）
AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

●当接收到的从地址与（SARUy中的11110b+SVA[1:0]）值匹配，且后续地址与SARLy值不匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）.AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

GCA标志（广播呼叫地址检测标志）

GCA标志指示是否检测到广播呼叫地址。

[Setting condition]

●当接收到的从机地址与广播呼叫地址（0000000b+0[W]）匹配时，ICSER中的GCAE位设置为1（启用广播呼叫地址检测）。GCA标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取GCA=1后将0写入GCA标志时

●检测到停止条件时

●当接收到的从机地址与广播呼叫地址（0000000b+0[W]）不匹配时，将ICSER中的GCAE位设置为1（启用广播呼叫地址检测）
GCA标志在帧中第9个SCL时钟周期的上升沿设置为0。

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

DID标志（设备ID地址检测标志）

DID标志指示是否检测到设备ID地址。

[Setting condition]

●当检测到启动或重启条件后立即接收到的第一帧与（设备ID(1111100b)+0[W]）的值匹配，且ICSER中的DIDE位设置为1（启用设备ID地址检测）.DID标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取DID=1后向DID标志写入0时

●检测到停止条件时

●当检测到启动或重启条件后立即接收的第一帧与（设备ID（1111100b））的值不匹配时，ICSER中的DIDE位设置为1（启用设备ID地址检测）
DID标志在帧中第9个SCL时钟周期的上升沿设置为0。

- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), and the second frame does not match any slave address from 0 to 2, with the DIDE bit in ICSER set to 1 (device-ID address detection enabled)
  The DID flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

HOA flag (Host Address Detection Flag)

The HOA flag indicates whether the host address was detected.

[Setting condition]

- When the received slave address matches the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled).
  The HOA flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA flag after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled)
  The HOA flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

31.2.10 ICSR2 : I2C Bus Status Register 2

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOF	Timeout Detection Flag 0: Timeout not detected 1: Timeout detected	R/(W)*1
1	AL	Arbitration-Lost Flag 0: Arbitration not lost 1: Arbitration lost	R/(W)*1
2	START	Start Condition Detection Flag 0: Start condition not detected 1: Start condition detected	R/(W)*1
3	STOP	Stop Condition Detection Flag 0: Stop condition not detected 1: Stop condition detected	R/(W)*1
4	NACKF	NACK Detection Flag 0: NACK not detected 1: NACK detected	R/(W)*1
5	RDRF	Receive Data Full Flag 0: ICDRR contains no receive data 1: ICDRR contains receive data	R/(W)*1
6	TEND	Transmit End Flag 0: Data being transmitted 1: Data transmit complete	R/(W)*1

●当检测到启动或重启条件后立即接收到的第一帧与（设备ID）的值匹配时
（1111100b)+0[W]），并且第二帧不匹配从0到2的任何从机地址，且ICSER中的DIDE位设置为1（启用设备ID地址检测）DID标志设置为0在帧的第9个SCL时钟周期的上升沿。

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

HOA标志（主机地址检测标志）

HOA标志指示是否检测到主机地址。

[Setting condition]

●当接收到的从机地址与主机地址（0001000b）匹配时，ICSER中的HOAE位设置为1（主机地址检测使能）。HOA标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

●读取HOA=1后向HOA标志写入0时

●检测到停止条件时

●当接收到的从机地址与主机地址（0001000b）不匹配时，ICSER中的HOAE位设置为1（主机地址检测使能）在第9个SCL时钟周期的上升沿将HOA标志设置为0框架。

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

31.2.10 ICSR2：I2C总线状态寄存器2

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMOF	超时检测标志 0：未检测到超时1：检测到超时	R/(W)*1
1	AL	Arbitration-Lost Flag 0：仲裁未丢失1：仲裁丢失	R/(W)*1
2	START	启动条件检测标志 0：未检测到启动条件1：检测到启动条件	R/(W)*1
3	STOP	停止条件检测标志 0：未检测到停止条件1：检测到停止条件	R/(W)*1
4	NACKF	NACK检测标志 0：未检测到NACK1：检测到NACK	R/(W)*1
5	RDRF	接收数据满标志 0：ICDRR不包含接收数据1：ICDRR包含接收数据	R/(W)*1
6	TEND	发送结束标志 0：数据发送中1：数据发送完成	R/(W)*1

Bit	Symbol	Function	R/W
7	TDRE	Transmit Data Empty Flag 0: ICDRT contains transmit data 1: ICDRT contains no transmit data	R

Note 1. Only 0 can be written, to clear the flag.

TMOF flag (Timeout Detection Flag)

The TMOF flag is set to 1 when the IIC detects a timeout because the SCLn line state remains unchanged for the set period.

[Setting condition]

- When the SCLn line state remains unchanged for the period specified in the ICMR2.TMOH, TMOL, and TMOS bits while the ICFER.TMOE bit is 1 (timeout function enabled) in master or in slave mode and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF flag after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

AL flag (Arbitration-Lost Flag)

The AL flag indicates that bus mastership was lost in arbitration because of a bus conflict or some other reason when a start condition was issued or an address and data was transmitted. The IIC monitors the level on the SDAn line during transmission and, if the level on the line does not match the value of the bit being output, is set the value of the AL flag to 1 to indicate that the bus is occupied by another device.

The IIC can also set the AL flag to indicate the detection of arbitration loss during NACK transmission or during data transmission.

[Setting conditions]

When master arbitration-lost detection is enabled (ICFER.MALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock except for the ACK period during data transmission in master transmit mode
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition requested) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is 1 (start condition requested), with the BBSY flag in ICCR2 set to 1.

When NACK arbitration-lost detection is enabled (ICFER.NALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled (ICFER.SALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock, except for the ACK period during data transmission in slave transmit mode.

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Bit	Symbol	Function	R/W
7	TDRE	传输数据空标志 0：ICDRT包含发送数据1：ICDRT不包含发送数据	R

注1.只能写入0，清除标志。

TMOF标志（超时检测标志）

当IIC检测到超时时，TMOF标志设置为1，因为SCLn线路状态在设置的周期内保持不变。

[Setting condition]

●SCLn线路状态在ICMR2.TMOH、TMOL和TMOS位指定的时间段内保持不变，而ICFER.TMOE位在主机或从机模式下为1（使能超时功能）并且接收到的从机地址匹配。

[Clearing conditions]

●读取TMOF=1后向TMOF标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

AL标志（仲裁失败标志）

AL标志表明在发出启动条件或传输地址和数据时，由于总线冲突或其他原因，总线控制权在仲裁中丢失。IIC在传输过程中监视SDAn线上的电平，如果线上的电平与正在输出的位的值不匹配，则将AL标志的值设置为1，以指示总线被另一个设备占用.

IIC还可以设置AL标志以指示在NACK传输或数据传输期间检测到仲裁丢失。

[Setting conditions]

当启用主机仲裁丢失检测时(ICFER.MALE=1)：

●主机传输模式下数据传输期间，除了ACK周期外，当内部SDA输出状态在SCL时钟的上升沿与SDAn线电平不匹配时

●当ICCR2的ST位为1（请求启动条件）或内部SDA输出状态与SDAn线电平不匹配时检测到启动条件

●ICCR2中的ST位为1（请求启动条件）时，ICCR2中的BBSY标志设置为1。

当启用NACK仲裁丢失检测时(ICFER.NALE=1)：

●在接收模式下的NACK传输过程中，当内部SDA输出状态在ACK周期的SCL时钟上升沿与SDAn线电平不匹配时。

当启用从设备仲裁丢失检测时(ICFER.SALE=1)：

●当内部SDA输出状态在SCL时钟的上升沿与SDAn线电平不匹配时，除了在从机传输模式下数据传输期间的ACK周期。

[Clearing conditions]

●读取AL=1后向AL标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Table 31.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
1	x	x	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected, while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 while BBSY in ICCR2 is 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
x	1	x	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master or slave receive mode
x	x	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

x: Don’t care

START flag (Start Condition Detection Flag)

The START flag indicates whether a start or restart condition was detected.

[Setting condition]

- When a start or restart condition is detected.

[Clearing conditions]

- When 0 is written to the START flag after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

STOP flag (Stop Condition Detection Flag)

The STOP flag indicates whether a stop condition was detected.

[Setting condition]

- When a stop condition is detected.

[Clearing conditions]

- When 0 is written to the STOP flag after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

NACKF flag (NACK Detection Flag)

The NACKF flag indicates whether a NACK was detected.

[Setting condition]

- When acknowledge is not received (NACK received) from the receive device in transmit mode, with the NACKE bit in ICFER set to 1 (transfer suspension enabled).

[Clearing conditions]

- When 0 is written to the NACKF flag after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1, the IIC suspends data transmission and reception. Writing to ICDRT in transmit mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit or receive operation. To restart data transmission or reception, set the NACKF flag to 0.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates whether the ICDRR contains receive data.

Table 31.4 仲裁丢失生成源和仲裁丢失使能函数之间的关系

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	仲裁失败的生成源
1	x	x	1	开始条件发布错误	当检测到启动条件时内部SDA输出状态与SDAn线电平不匹配，而ICCR2中的ST位为1
					ICCR2中的ST设置为1而ICCR2中的BBSY为1时
			1	传输数据不匹配	当发送数据（包括从地址）与主发送模式下的总线状态不匹配时
x	1	x	1	NACK传输不匹配	在主机或从机接收模式下发送NACK期间检测到ACK时
x	x	1	1	传输数据不匹配	当发送数据与从发送模式下的总线状态不匹配时

x: Don’t care

START标志（开始条件检测标志）

START标志指示是否检测到启动或重新启动条件。

[Setting condition]

●检测到启动或重启条件时。

[Clearing conditions]

●读取START=1后向START标志写入0时

●检测到停止条件时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

STOP标志（停止条件检测标志）

STOP标志指示是否检测到停止条件。

[Setting condition]

●检测到停止条件时。

[Clearing conditions]

●读取STOP=1后向STOP标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

NACKF标志（NACK检测标志）

NACKF标志指示是否检测到NACK。

[Setting condition]

●当在发送模式下未从接收设备接收到确认（NACK接收）时，ICFER中的NACKE位设置为1（启用传输暂停）。

[Clearing conditions]

●读取NACKF=1后向NACKF标志写入0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当NACKF标志设置为1时，IIC暂停数据发送和接收。在NACKF标志设置为1的情况下，在发送模式下写入ICDRT或在接收模式下从ICDRR读取不会启用数据发送或接收操作。要重新开始数据发送或接收，请将NACKF标志设置为0。

RDRF标志（接收数据满标志）

RDRF标志指示ICDRR是否包含接收数据。

[Setting conditions]

- When receive data is transferred from ICDRS to ICDRR
  The RDRF flag is set to 1 on the rising edge of the eighth or ninth SCL clock cycle (selected in the RDRFS bit in ICMR3).
- When the received slave address matches after a start or restart condition is detected with the TRS bit in ICCR2 set to 0.

[Clearing conditions]

- When 0 is written to the RDRF flag after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting condition]

- On the rising edge of the ninth SCL clock cycle while the TDRE flag is 1.

[Clearing conditions]

- When 0 is written to the TEND flag after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates whether the ICDRT contains transmit data.

[Setting conditions]

- When data is transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1.

[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the IIC suspends data transmission and reception. In this case, if the TDRE flag is 0 (next transmit data written), data is transferred to the ICDRS register and the ICDRT register becomes empty on the rising edge of the 9th clock cycle, but the TDRE flag does not set to 1.

31.2.11 ICWUR : I2C Bus Wakeup Unit Register

Base address: IIC0WU = 0x4009_F014

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
Value after reset:	0	0	0	1	0	0	0	0

[Setting conditions]

●接收数据从ICDRS传输到ICDRR时
RDRF标志在第8个或第9个SCL时钟周期的上升沿设置为1（在RDRFS位中选择ICMR3).

●当ICCR2中的TRS位设置为0检测到启动或重启条件后接收到的从机地址匹配时。

[Clearing conditions]

●读取RDRF=1后向RDRF标志写入0时

●从ICDRR读取数据时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

TEND标志（发送结束标志）

TEND标志表示传输完成。

[Setting condition]

●在第9个SCL时钟周期的上升沿，同时TDRE标志为1。

[Clearing conditions]

●读取TEND=1后向TEND标志写入0时

●数据写入ICDRT时

●检测到停止条件时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

TDRE标志（传输数据空标志）

TDRE标志指示ICDRT是否包含发送数据。

[Setting conditions]

●当数据从ICDRT传输到ICDRS并且ICDRT变为空时

●ICCR2的TRS位为1时

●TRS位为1时接收到的从机地址匹配时。

[Clearing conditions]

●数据写入ICDRT时

●ICCR2的TRS位设置为0时

●当ICCR1的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当ICFER的NACKE位为1时NACKF标志设置为1，IIC暂停数据发送和接收。在这种情况下，如果TDRE标志为0（写入下一个发送数据），则数据被传送到ICDRS寄存器，并且ICDRT寄存器在第9个时钟周期的上升沿变为空，但TDRE标志不设置为1。

31.2.11 ICWUR:I2C总线唤醒单元寄存器

Base address: IIC0WU = 0x4009_F014

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
重置后的值:	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	WUAFA	Wakeup Analog Filter Additional Selection 0: Do not add the wakeup analog filter 1: Add the wakeup analog filter	R/W
3:1	—	These bits are read as 0. The write value should be 0.	R/W
4	WUACK	ACK Bit for Wakeup Mode Choice of four response modes in combination with ICCR1.IICRST and WUACK. See Table 31.5.	R/W
5	WUF	Wakeup Event Occurrence Flag 0: Slave address not matching during wakeup 1: Slave address matching during wakeup	R/W
6	WUIE	Wakeup Interrupt Request Enable 0: Disable wakeup interrupt request (IIC0_WUI) 1: Enable wakeup interrupt request (IIC0_WUI)	R/W
7	WUE	Wakeup Function Enable 0: Disable wakeup function 1: Enable wakeup function	R/W

Table 31.5 Wakeup mode

IICRST	WUACK	Operation mode	Description
0	0	Normal wakeup mode 1	ACK response on 9th SCL, and SCL low-hold after 9th SCL.
0	1	Normal wakeup mode 2	No ACK response immediately and SCL low-hold between 8th and 9th SCL. SCL low-hold release and ACK response on 9th SCL.
1	0	Command recovery mode	ACK response on 9th SCL and no SCL low-hold.
1	1	EEP response mode	NACK response on 9th SCL and no SCL low-hold.

WUF flag (Wakeup Event Occurrence Flag)

The WUF flag indicates whether the slave address is matching during wakeup.

[Setting condition]

- When PCLKB is supplied after a slave-address match in the first 8th SCL low during wakeup mode.

[Clearing conditions]

- When 0 is written t o the WUF flag after reading WUF = 1
- When ICE = 0 and IICRST = 1.

31.2.12 ICWUR2 : I2C Bus Wakeup Unit Register 2

Base address: IIC0WU = 0x4009_F014

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	WUSYF	WUASYF	WUSEN
Value after reset:	1	1	1	1	1	1	0	1

Bit	Symbol	Function	R/W
0	WUSEN	Wakeup Function Synchronous Enable 0: IIC asynchronous circuit enable 1: IIC synchronous circuit enable	R/W
1	WUASYF	Wakeup Function Asynchronous Operation Status Flag 0: IIC synchronous circuit enable condition 1: IIC asynchronous circuit enable condition	R

Bit	Symbol	Function	R/W
0	WUAFA	唤醒模拟滤波器附加选择 0：不加唤醒模拟滤波器1：加唤醒模拟滤波器	R/W
3:1	—	这些位被读取为0。写入值应为0。	R/W
4	WUACK	唤醒模式的ACK位 结合ICCR1.IICRST和WUACK可选择四种响应模式。见表31.5。	R/W
5	WUF	唤醒事件发生标志 0：唤醒期间从机地址不匹配1：唤醒期间从机地址匹配	R/W
6	WUIE	唤醒中断请求使能 0：禁用唤醒中断请求（IIC0_WUI）1：启用唤醒中断请求（IIC0_WUI）	R/W
7	WUE	唤醒功能启用 0：禁用唤醒功能1：启用唤醒功能	R/W

Table 31.5 唤醒模式

IICRST	WUACK	操作模式	Description
0	0	正常唤醒模式1	第9个SCL的ACK响应，以及第9个SCL之后的SCL低保持。
0	1	正常唤醒模式2	在第8和第9个SCL之间没有立即ACK响应并且SCL保持低电平。SCL低保持释放和第9个SCL的ACK响应。
1	0	命令恢复模式	第9个SCL的ACK响应且没有SCL低保持。
1	1	EEP响应模式	第9个SCL的NACK响应且没有SCL低保持。

WUF标志（唤醒事件发生标志）

WUF标志指示在唤醒期间从地址是否匹配。

[Setting condition]

●在唤醒模式期间，在第一个第8个SCL低电平的从机地址匹配后提供PCLKB时。

[Clearing conditions]

●读取WUF=1后向WUF标志写入0时

●当ICE=0且IICRST=1时。

31.2.12 ICWUR2:I2C总线唤醒单元寄存器2

Base address: IIC0WU = 0x4009_F014

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	WUSYF	WUASYF	WUSEN
重置后的值:	1	1	1	1	1	1	0	1

Bit	Symbol	Function	R/W
0	WUSEN	唤醒功能同步使能 0：IIC异步电路使能1：IIC同步电路使能	R/W
1	WUASYF	唤醒功能异步操作状态标志 0：IIC同步电路使能条件1：IIC异步电路使能条件	R

Bit	Symbol	Function	R/W
2	WUSYF	Wakeup Function Synchronous Operation Status Flag 0: IIC asynchronous circuit enable condition 1: IIC synchronous circuit enable condition	R
7:3	—	These bits are read as 1. The write value should be 1.	R/W

WUSEN bit (Wakeup Function Synchronous Enable)

The WUSEN bit is used in combination with the WUASYF flag (or WUSYF flag) to switch between the PCLKB synchronous and asynchronous operation, when the wakeup effective function is enabled (ICWUR.WUE = 1).

The PCLKB operation switches from synchronous to asynchronous operation:

When the ICCR2.BBSY flag is 0, if 0 is written to the WUSEN bit while the WUASYF flag is 0. The reception occurs independently of the operation of PCLKB (with PCLKB stopped) after it switches to the PCLKB asynchronous operation, on wakeup event detection.

The PCLKB operation switches from asynchronous to synchronous operation:

- When 1 is written to the WUSEN bit, with the WUASYF flag at 1, when a wakeup event is detected. After writing 1, the WUASYF flag immediately becomes 0.
- When the stop condition is detected with a wakeup event undetected.

WUASYF flag (Wakeup Function Asynchronous Operation Status Flag)

The WUASYF flag can place the IIC in PCLKB asynchronous operation when the wakeup effective function is enabled (ICWUR.WUE = 1).

[Setting condition]

- When the ICCR2.BBSY flag is 0, and the WUSEN bit is set to 0 with the ICWUR.WUE bit set to 1.

[Clearing conditions]

- When 1 is written to the WUSEN bit after detecting the wake-up event with ICWUR.WUE bit set to 1.
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wake-up event with WUASY flag set to 1 with ICWUR.WUE bit set to 1.
- When you write 1 in the WUSEN bit with the WUASYF flag detected 1 and the wake-up event in the state of ICWUR.WUE = 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

WUSYF flag (Wakeup Function Synchronous Operation Status Flag)

It is shown that IIC is in the PCLKB synchronous operation at wake-up effective function (ICWUR.WUE = 1). This flag is a value in which the WUASYF flag is always reserved.

[Setting conditions]

- When 1 is written to the WUSEN bit after detecting the wake-up event with ICWUR.WUE bit set to 1 with WUSYF flag set to 0 with ICWUR.WUE bit set to 1.
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wake-up event with WUSYF flag set to 0 with ICWUR.WUE bit set to 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

- When the ICCR2.BBSY flag is 0 with the ICWUR.WUE bit set to 1 after writing 0 to the WUSEN bit.

Bit	Symbol	Function	R/W
2	WUSYF	唤醒功能同步操作状态标志 0：IIC异步电路使能条件1：IIC同步电路使能条件	R
7:3	—	这些位被读取为1。写入值应为1。	R/W

WUSEN位（唤醒功能同步使能）

WUSEN位与WUASYF标志（或WUSYF标志）结合使用，在启用唤醒有效功能（ICWUR.WUE=1）时在PCLKB同步和异步操作之间切换。

PCLKB操作从同步操作切换到异步操作：

当ICCR2.BBSY标志为0时，如果在WUASYF标志为0时将0写入WUSEN位。在唤醒事件切换到PCLKB异步操作后，接收发生独立于PCLKB的操作（PCLKB停止）检测。

PCLKB操作从异步操作切换到同步操作：

●当WUSEN位写入1且WUASYF标志为1时，检测到唤醒事件。写入1后，WUASYF标志立即变为0。

●当检测到停止条件且未检测到唤醒事件时。

WUASYF标志（唤醒功能异步操作状态标志）

WUASYF标志可以在启用唤醒有效功能（ICWUR.WUE=1）时将IIC置于PCLKB异步操作中。

[Setting condition]

●ICCR2.BBSY标志为0且WUSEN位设置为0且ICWUR.WUE位设置为1时。

[Clearing conditions]

●当检测到唤醒事件后将1写入WUSEN位，且ICWUR.WUE位设置为1。

●在检测到WUASY标志设置为1且ICWUR.WUE位设置为1的唤醒事件之前检测到WUSEN位设置为1的停止条件时。

●当您在WUSEN位写入1时，检测到WUASYF标志为1，并且唤醒事件处于ICWUR.WUE=1的状态。

- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

WUSYF标志（唤醒功能同步操作状态标志）

表明IIC在唤醒有效功能(ICWUR.WUE=1)时处于PCLKB同步操作。此标志是WUASYF标志始终保留的值。

[Setting conditions]

●当检测到唤醒事件后将1写入WUSEN位时，将ICWUR.WUE位设置为1，将WUSYF标志设置为0，并将ICWUR.WUE位设置为1。

●在检测到WUSYF标志设置为0且ICWUR.WUE位设置为1的唤醒事件之前检测到WUSEN位设置为1的停止条件时。

- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

●当ICCR2.BBSY标志为0且ICWUR.WUE位在WUSEN位写入0后设置为1时。

31.2.13 SARLy : Slave Address Register Ly (y = 0 to 2)

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x0A + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SVA[6:0]							SVA0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SVA0	10-bit Address LSB Slave address setting.	R/W
7:1	SVA[6:0]	7-bit Address/10-bit Address Lower Bits Slave address setting.	R/W

SVA0 bit (10-bit Address LSB)

When the 10-bit address format is selected (SARUy.FS = 1), the SVA0 bit functions as the LSB of a 10-bit address and is combined with the SVA[6:0] bits to form the lower 8 bits of a 10-bit address.

This bit is valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in this bit is ignored.

SVA[6:0] bits (7-bit Address/10-bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), the SVA[6:0] bits function as a 7-bit address. When the 10- bit address format is selected (SARUy.FS = 1), these bits combine with the SVA0 bit to form the lower 8 bits of a 10-bit address.

When the SARyE bit in ICSER is 0, the setting in these bits is ignored.

31.2.14 SARUy : Slave Address Register Uy (y = 0 to 2)

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x0B + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	7-bit/10-bit Address Format Select 0: Select 7-bit address format 1: Select 10-bit address format	R/W
2:1	SVA[1:0]	10-bit Address Upper Bits Slave address setting.	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

FS bit (7-bit/10-bit Address Format Select)

The FS bit selects 7- or 10-bit format for slave address y (in SARLy and SARUy).

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the SVA[1:0] and SVA0 settings in SARLy are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the SVA[1:0] and SARLy settings are valid.

When the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the SARUy.FS setting is invalid.

31.2.13 SARLy：从地址寄存器Ly（y=0到2）

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x0A + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SVA[6:0]							SVA0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SVA0	10位地址LSB从机地址 设置。	R/W
7:1	SVA[6:0]	7位地址10位地址低位从机地址设置。	R/W

SVA0位（10位地址LSB）

Whenthe10-bitaddressformatisselected(SARUy.FS=1) theSVA0bitfunctionsastheLSBofa10-bitaddressandiscombinedwiththeSVA[6:0]bitstoformthelower8bitsofa10位地址。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，该位有效。当SARUy.FS或SARyE位为0时，忽略该位的设置。

SVA[6:0]位（7位地址10位地址低位）

Whenthe7-bitaddressformatisselected(SARUy.FS=0) theSVA[6:0]bitsfunctionasa7-bitaddress.Whenthe10bitaddressformatisselected(SARUy.FS=1) thesebitscombinewiththeSVA0bittoformthelower8bitsofa10-bitaddress.

当ICSER中的SARyE位为0时，这些位中的设置将被忽略。

31.2.14 SARUy：从地址寄存器Uy（y=0到2）

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x0B + 0x02 × y

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SVA[1:0]		FS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FS	7位10位地址格式选择 0：选择7位地址格式1：选择10位地址格式	R/W
2:1	SVA[1:0]	10位地址高位从机地址设置。	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

FS位（7位10位地址格式选择）

FS位为从地址y选择7位或10位格式（在SARLy和SARUy中）。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为0时，从机地址y选择7位地址格式，SARLy中的SVA[6:0]设置有效 并且忽略SARLy中的SVA[1:0]和SVA0设置。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，从机地址y选择10位地址格式且SVA[1:0]和SARLy设置有效.

当ICSER中的SARyE位为0（SARLy和SARUy禁用）时，SARUy.FS设置无效。

SVA[1:0] bits (10-bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), the SVA[1:0] bits function as the upper 2 bits of a 10-bit address.

These bits are valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in these bits is ignored.

31.2.15 ICBRL : I2C Bus Bit Rate Low-Level Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRL[4:0]	Bit Rate Low-Level Period Low-level period of SCL clock.	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W

BRL[4:0] bits (Bit Rate Low-Level Period)

The BRL[4:0] bits set the low-level period of the SCL clock. ICBRL counts the low-level period with the internal reference clock source (IICφ) specified by the CKS[2:0] bits in ICMR1. ICBRL also generates the data setup time for automatic SCL low-hold operation, see section 31.9. Automatic Low-Hold Function for SCL. When the IIC is used in slave mode, the BRL[4:0] bits must be set to a value longer than the data setup time*1.

If the digital noise filter is enabled (NFE bit in ICFER is 1), set the BRL[4:0] bits to a value at least one greater than the number of stages in the noise filter. For details on the number of stages, see the description of the NF[1:0] bits in section 31.2.5. ICMR3 : I2C Bus Mode Register 3.

Note 1. Data setup time (t_{SU}: DAT)

250 ns for up to 100 kbps: Standard-mode (Sm)

100 ns for up to 400 kbps: Fast-mode (Fm)

50 ns for up to 1 Mbps: Fast-mode Plus (Fm+)

31.2.16 ICBRH : I2C Bus Bit Rate High-Level Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRH[4:0]	Bit Rate High-Level Period High-level period of SCL clock.	R/W
7:5	—	These bits are read as 1. The write value should be 1.	R/W

BRH[4:0] bits (Bit Rate High-Level Period)

The BRH[4:0] bits set the high-level period of SCL clock. BRH[4:0] bits are valid in master mode. If the IIC is used only in slave mode, do not set the BRH[4:0] bits.

SVA[1:0]位（10位地址高位）

Whenthe10-bitaddressformatisselected(FS=1) theSVA[1:0]bitsfunctionastheupper2bitsofa10-bitaddress.

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，这些位有效。
当SARUy.FS或SARyE位为0时，这些位中的设置将被忽略。

31.2.15 ICBRL：I2C总线比特率低电平寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRL[4:0]				
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRL[4:0]	比特率低电平周期 SCL时钟的低电平周期。	R/W
7:5	—	这些位被读取为1。写入值应为1。	R/W

BRL[4:0]位（比特率低电平周期）

BRL[4:0]位设置SCL时钟的低电平周期。ICBRL使用由ICMR1中的CKS[2:0]位指定的内部参考时钟源(IICφ)对低电平周期进行计数。ICBRL还为自动SCL低保持操作生成数据建立时间，请参见第31.9节。SCL的自动低保持功能。当IIC在从机模式下使用时，BRL[4:0]位必须设置为比数据建立时间*1更长的值。

如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将BRL[4:0]位设置为至少比噪声滤波器中的级数大1的值。关于阶段数的详细信息，请参见第31.2.5节中对NF[1:0]位的描述。ICMR3：I2C总线模式寄存器3。

注1.数据建立时间(tSU:DAT)

250ns，最高100kbps：标准模式(Sm)

100ns，最高400kbps：快速模式(Fm)

高达1Mbps时为50ns：Fast-modePlus(Fm+)

31.2.16 ICBRH：I2C总线比特率高级寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	BRH[4:0]				
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	BRH[4:0]	比特率高级期 SCL时钟的高电平周期。	R/W
7:5	—	这些位被读取为1。写入值应为1。	R/W

BRH[4:0]位（比特率高电平周期）

BRH[4:0]位设置SCL时钟的高电平周期。BRH[4:0]位在主机模式下有效。如果IIC仅用于从机模式，则不要设置BRH[4:0]位。

ICBRH counts the high-level period with the internal reference clock source (IICφ) specified in the CKS[2:0] bits in ICMR1.

If the digital noise filter is enabled (the NFE bit in ICFER is 1), set these bits to a value at least one greater than the number of stages in the noise filter. For the number of stages in the noise filter, see the description of the NF[1:0] bits in section 31.2.5. ICMR3 : I²C Bus Mode Register 3.

The IIC transfer rate and the SCL clock duty are calculated using the following expressions (1) to (5):

1. ICFER.SCLE = 0
   Transfer rate = 1/[{(BRH + 1) + (BRL + 1)}/IICφ*1 + tr*2 + tf*2]
   Duty cycle = [tr + {(BRH + 1)/IICφ}]/[tr + tf + {(BRH + 1) + (BRL + 1)}/IICφ]
2. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
   Transfer rate = 1/[{(BRH + 3) + (BRL+ 3)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 3)/IICφ}]/[tr + tf + {(BRH + 3) + (BRL + 3)}/IICφ]
3. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
   Transfer rate = 1/[{(BRH + 3 + nf*3) + (BRL + 3 + nf)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 3 + nf)/IICφ}]/[tr + tf + {(BRH + 3 + nf) + (BRL + 3 + nf)}/IICφ]
4. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
   Transfer rate = 1/[{(BRH + 2) + (BRL + 2)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 2)/IICφ}]/[tr + tf + {(BRH + 2) + (BRL + 2)}/IICφ]
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
   Transfer rate = 1/[{(BRH + 2 + nf) + (BRL + 2 + nf)}/IICφ + tr + tf]
   Duty cycle = [tr + {(BRH + 2 + nf)/IICφ}]/[tr + tf + {(BRH + 2 + nf) + (BRL + 2 + nf)}/IICφ]

Note 1. IICφ = PCLKB × division ratio
Note 2. The SCLn line rise time (tr) and SCLn line fall time (tf) depend on the total bus line capacitance (Cb) and the pull-up resistor (Rp). For details, see the I²C bus standard from NXP Semiconductors.
Note 3. nf = Number of digital noise filters selected in the ICMR3.NF bit.

Table 31.6 Example of ICBRH/ICBRL Settings for Transfer Rate IIC when SCLE = 0

Transfer rate (kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011b	24 (0xF8)	30 (0xFE)	50	—	(1)
400	010b	7 (0xE7)	15 (0xEF)	50	—	(1)
1000	000b	12 (0xEC)	24 (0xF8)	50	—	(1)

Table 31.7 Example of ICBRH/ICBRL Settings for Transfer Rate when SCLE = 1 and NFE = 0

Transfer rate (kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	11 (0xEB)	13 (0xED)	50	—	(4)
400	001b	13 (0xED)	31 (0xFF)	50	—	(4)
1000	000b	10 (0xEA)	22 (0xF6)	50	—	(2)

Table 31.8 Example of ICBRH/ICBRL Settings for Transfer Rate when SCLE = 1 and NFE = 1

Transfer rate (kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	011b	21 (0xF5)	26 (0xFA)	50	01b	(5)
400	001b	11 (0xEB)	29 (0xFD)	50	01b	(5)
1000	000b	8 (0xE8)	20 (0xF4)	50	01b	(3)

ICBRH使用CKS[2:0]位中指定的内部参考时钟源(IICφ)计算高电平周期
ICMR1.

如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将这些位设置为至少比噪声滤波器中的级数大1的值。关于噪声滤波器的级数，请参见第31.2.5节中对NF[1:0]位的说明。ICMR3：I2C总线模式寄存器3。

IIC传输速率和SCL时钟占空比使用以下表达式(1)到(5)计算：

1. ICFER.SCLE = 0
   传输率=1[{(BRH+1)+(BRL+1) IICφ*1+tr*2+tf*2]
   占空比=[tr+{(BRH+1)IICφ][tr+tf+{(BRH+1)+(BRL+1) IICφ]
2. ICFER.SCLE=1且ICFER.NFE=0且CKS[2:0]=000b(IICφ=PCLKB)传输速率=1[{(BRH+3)+(BRL+3) IICφ+tr+tf]
   占空比=[tr+{(BRH+3)IICφ][tr+tf+{(BRH+3)+(BRL+3) IICφ]
3. ICFER.SCLE=1且ICFER.NFE=1且CKS[2:0]=000b(IICφ=PCLKB)传输速率=1[{(BRH+3+nf*3)+(BRL+3+nf) IICφ+tr+tf]
   占空比=[tr+{(BRH+3+nf)IICφ][tr+tf+{(BRH+3+nf)+(BRL+3+nf) IICφ]
4. ICFER.SCLE=1andICFER.NFE=0andCKS[2:0]≠000b传输率=1[{(BRH+2)+(BRL+2) IICφ+tr+tf]
   占空比=[tr+{(BRH+2)IICφ][tr+tf+{(BRH+2)+(BRL+2) IICφ]
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
   传输率=1[{(BRH+2+nf)+(BRL+2+nf) IICφ+tr+tf]
   占空比=[tr+{(BRH+2+nf)IICφ][tr+tf+{(BRH+2+nf)+(BRL+2+nf) IICφ]

注1.IICφ=PCLKB×分频比
注2.SCLn线路上升时间(tr)和SCLn线路下降时间(tf)取决于总总线电容(Cb)和上拉电阻(Rp)。有关详细信息，请参阅NXPSemiconductors的I2C总线标准。
注3.nf=在ICMR3.NF位中选择的数字噪声滤波器的数量。

Table 31.6 SCLE=0时传输速率IIC的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011b	24 (0xF8)	30 (0xFE)	50	—	(1)
400	010b	7 (0xE7)	15 (0xEF)	50	—	(1)
1000	000b	12 (0xEC)	24 (0xF8)	50	—	(1)

Table 31.7 SCLE=1和NFE=0时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	100b	11 (0xEB)	13 (0xED)	50	—	(4)
400	001b	13 (0xED)	31 (0xFF)	50	—	(4)
1000	000b	10 (0xEA)	22 (0xF6)	50	—	(2)

Table 31.8 SCLE=1和NFE=1时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0] (ICMR1)	BRH[4:0] (ICBRH)	BRL[4:0] (ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	011b	21 (0xF5)	26 (0xFA)	50	01b	(5)
400	001b	11 (0xEB)	29 (0xFD)	50	01b	(5)
1000	000b	8 (0xE8)	20 (0xF4)	50	01b	(3)

31.2.17 ICDRT : I2C Bus Transmit Data Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the I2C Bus Shift Register (ICDRS), it transfers the transmit data that was written to ICDRT to ICDRS and starts transmitting data in transmit mode. The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data is written to ICDRT while the ICDRS data is being transmitted.

ICDRT can always be read and written to. Write transmit data to ICDRT once when a transmit data empty interrupt (IICn_TXI) request is generated.

31.2.18 ICDRR : I2C Bus Receive Data Register

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data is received, the received data is transferred from the I2C Bus Shift Register (ICDRS) to ICDRR to enable the next data to be received. The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data is read from ICDRR while ICDRS is receiving data. ICDRR cannot be written to. Read data from ICDRR once when a receive data full interrupt (IICn_RXI) request is generated.

If ICDRR receives the next receive data before the current data is read from ICDRR (while the RDRF flag in ICSR2 is 1), the IIC automatically holds the SCL clock low 1 cycle before the RDRF flag is set to 1 next.

31.2.19 ICDRS : I2C Bus Shift Register

Base address: n/a

Offset address: n/a

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	—	—	—	—	—	—	—	—

ICDRS is an 8-bit shift register for data transmit and receive. During transmission, transmit data is transferred from ICDRT to ICDRS and is transmitted from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data is received. ICDRS cannot be accessed directly.

31.3 Operation

31.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start or restart condition is an address frame that specifies a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.

Figure 31.3 shows the I2C bus format, and Figure 31.4 shows the I2C bus timing.

31.2.17 ICDRT：I2C总线发送数据寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x12

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	1	1	1	1	1	1	1	1

当ICDRT检测到I2C总线移位寄存器(ICDRS)中有空间时，它将写入ICDRT的发送数据传输到ICDRS，并开始在发送模式下发送数据。ICDRT和ICDRS的双缓冲结构允许在传输ICDRS数据的同时将下一个传输数据写入ICDRT的连续传输操作。

ICDRT始终可以被读取和写入。当产生发送数据空中断（IICn_TXI）请求时，将发送数据写入ICDRT。

31.2.18 ICDRR:I2C总线接收数据寄存器

Base address: IICn = 0x4009_F000 + 0x0100 × n (n = 0 to 2)

Offset address: 0x13

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	0	0	0	0	0	0	0	0

当接收到1个字节的数据时，接收到的数据会从I2C总线移位寄存器(ICDRS)传输到ICDRR，以便接收下一个数据。如果在ICDRS正在接收数据时从ICDRR读取接收到的数据，ICDRS和ICDRR的双缓冲结构允许连续接收操作。无法写入ICDRR。当产生接收数据完全中断(IICn_RXI)请求时，从ICDRR读取数据一次。

如果ICDRR在从ICDRR读取当前数据之前接收到下一个接收数据（此时ICSR2中的RDRF标志为1），则IIC在下一个RDRF标志设置为1之前自动将SCL时钟保持低1个周期。

31.2.19 ICDRS:I2C总线移位寄存器

Base address: n/a

Offset address: n/a

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	—	—	—	—	—	—	—	—

ICDRS是一个用于数据发送和接收的8位移位寄存器。在传输期间，传输数据从ICDRT传输到ICDRS，并从SDAn引脚传输。在接收过程中，接收到1个字节的数据后，数据从ICDRS传输到ICDRR。ICDRS不能直接访问。

31.3 Operation

31.3.1 通讯数据格式

I2C总线格式由8位数据和1位确认组成。开始或重启条件之后的帧是地址帧，它指定与主设备通信的从设备。指定的从站有效，直到指定新的从站或发出停止条件。

图31.3显示了I2C总线格式，图31.4显示了I2C总线时序。

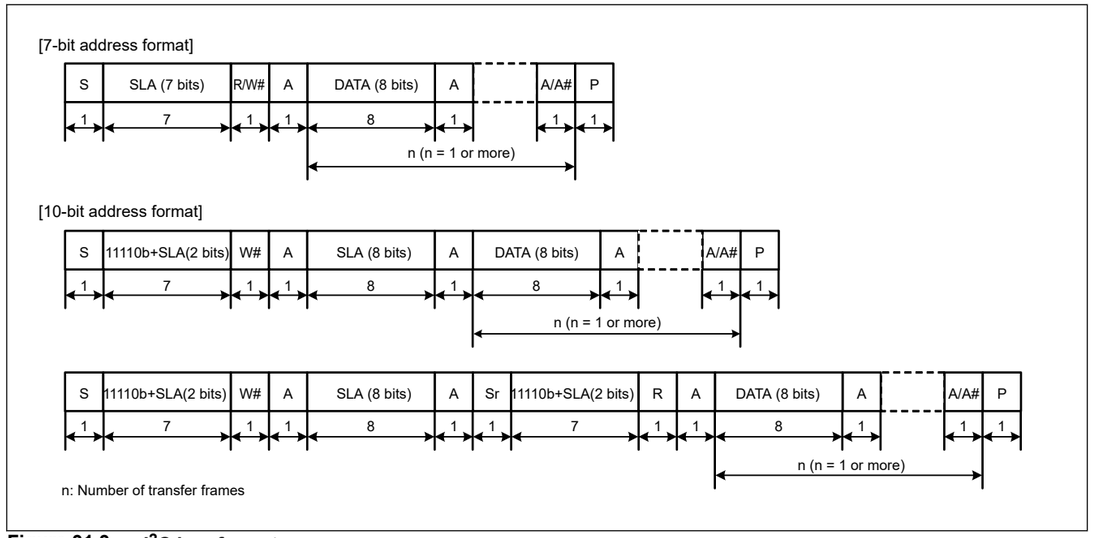

Figure 31.3 I^2C bus format

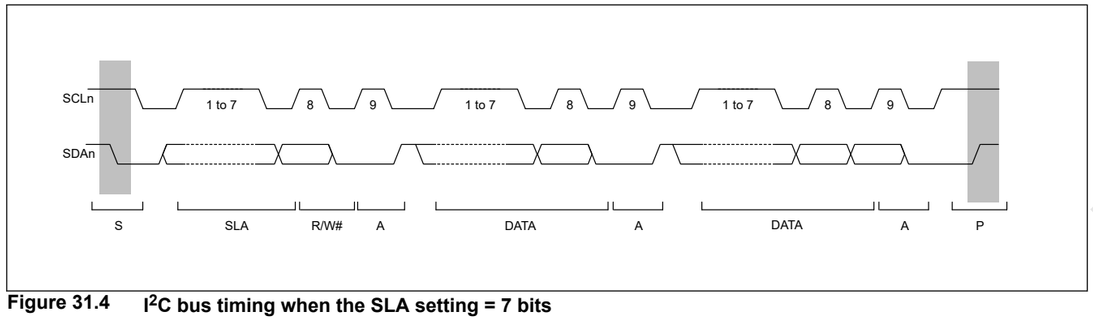

Figure 31.4 I^2C bus timing when the SLA setting = 7 bits

S:	Start condition. The master device drives the SDAn line low from high while the SCLn line is high.
SLA:	Slave address, by which the master device selects a slave device.
R/W#:	Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0.
A:	Acknowledge. The receive device drives the SDAn line low. In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.
A#:	Not Acknowledge. The receive device drives the SDAn line high.
Sr:	Restart condition. The master device drives the SDAn line low from the high level after the setup time has elapsed with the SCLn line high.
DATA:	Transmitted or received data.
P:	Stop condition. The master device drives the SDAn line high from low while the SCLn line is high.

31.3.2 Initial Settings

Before starting data transmission or reception, initialize the IIC using the procedure shown in Figure 31.5.

1. Set the ICCR1.ICE bit to 0 to set the SCLn and SDAn pins to the inactive state.
2. Set the ICCR1.IICRST bit to 1 to initiate IIC reset.
3. Set the ICCR1.ICE bit to 1 to initiate internal reset.
4. Set the SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL registers (y = 0 to 2), and set the other registers as required. For initial settings of the IIC, see Figure 31.5.

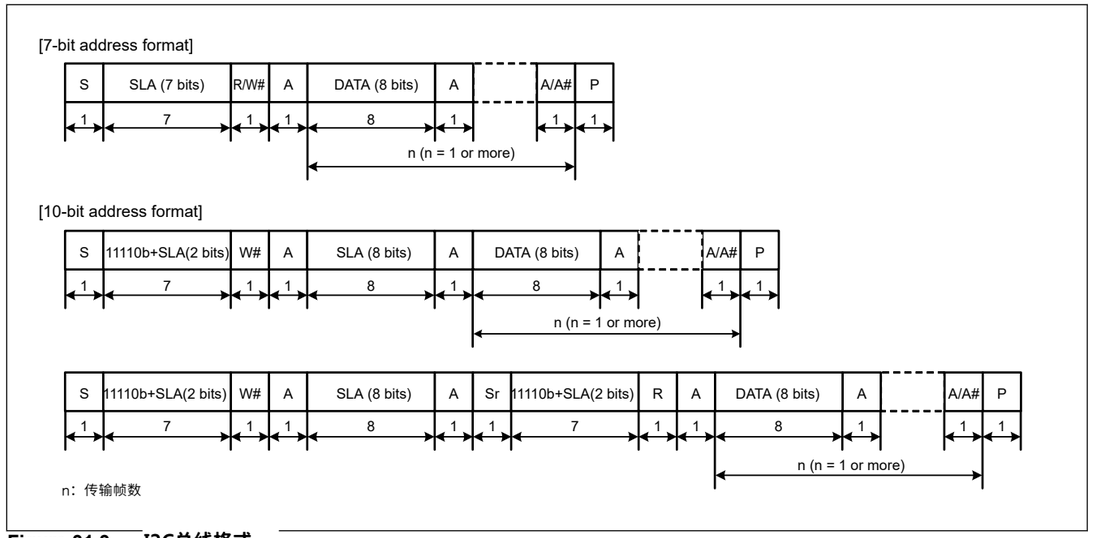

Figure 31.3 I2C总线格式

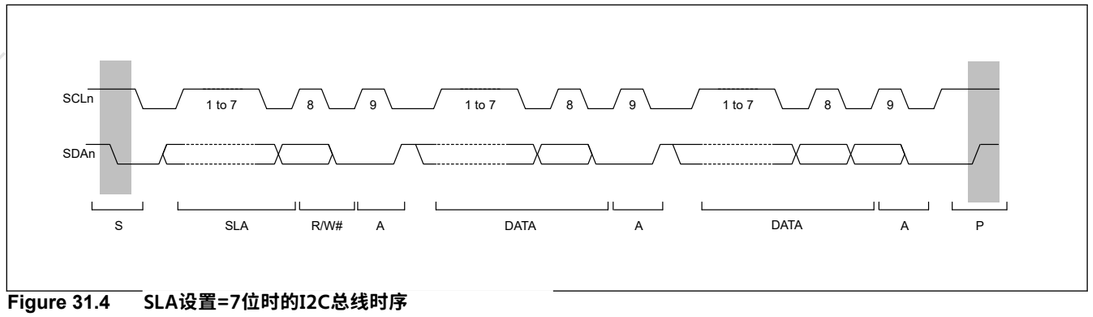

Figure 31.4 SLA设置=7位时的I2C总线时序

S:	启动条件。主设备将SDAn线从高电平驱动为低电平，而SCLn线为高电平。
SLA:	从地址，主设备通过该地址选择从设备。
R/W#:	指示数据传输的方向：当RW#为1时从从设备到主设备，或者当RW#为0时从主设备到从设备。
A:	承认。接收设备将SDAn线驱动为低电平。在主发送模式下，从设备返回确认。在主接收模式下，主设备返回确认。
A#:	不承认。接收设备将SDAn线驱动为高电平。
Sr:	重启条件。建立时间过后，主设备将SDAn线从高电平驱动为低电平SCLn线高。
DATA:	传输或接收的数据。
P:	停止条件。主设备将SDAn线从低电平驱动至高电平，而SCLn线为高电平。

31.3.2 初始设置

在开始数据发送或接收之前，使用图31.5所示的过程初始化IIC。

1.将ICCR1.ICE位设置为0，将SCLn和SDAn引脚设置为无效状态。

2.将ICCR1.IICRST位设置为1以启动IIC复位。

3.将ICCR1.ICE位设置为1以启动内部复位。

4.设置SARLy、SARUy、ICSER、ICMR1、ICBRH和ICBRL寄存器（y=0到2），并根据需要设置其他寄存器。IIC的初始设置见图31.5。

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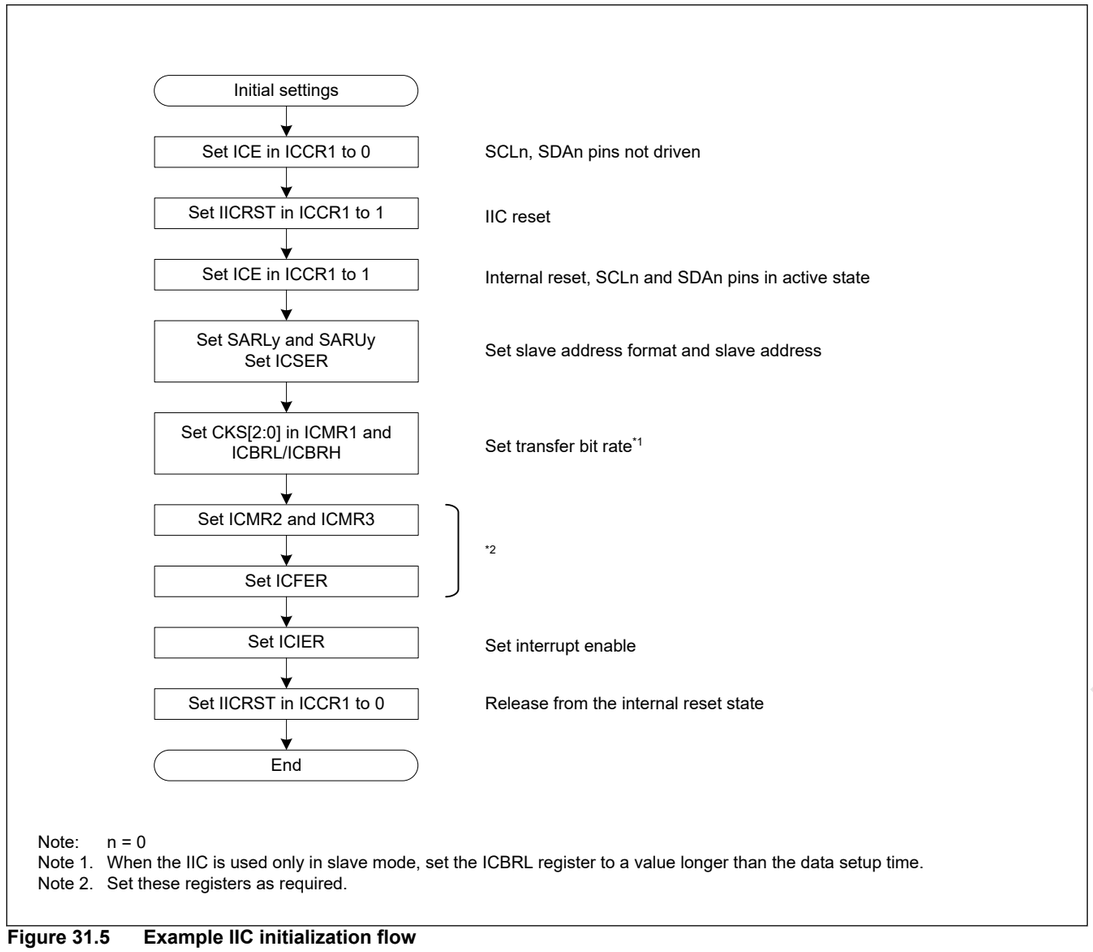
5. When the required register settings are complete, set the ICCR1.IICRST bit to 0 to release the IIC reset.

This procedure is not required if the IIC initialization is already complete.



Note: n = 0
Note 1. When the IIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.
Note 2. Set these registers as required.

Figure 31.5 Example IIC initialization flow

31.3.3 Master Transmit Operation

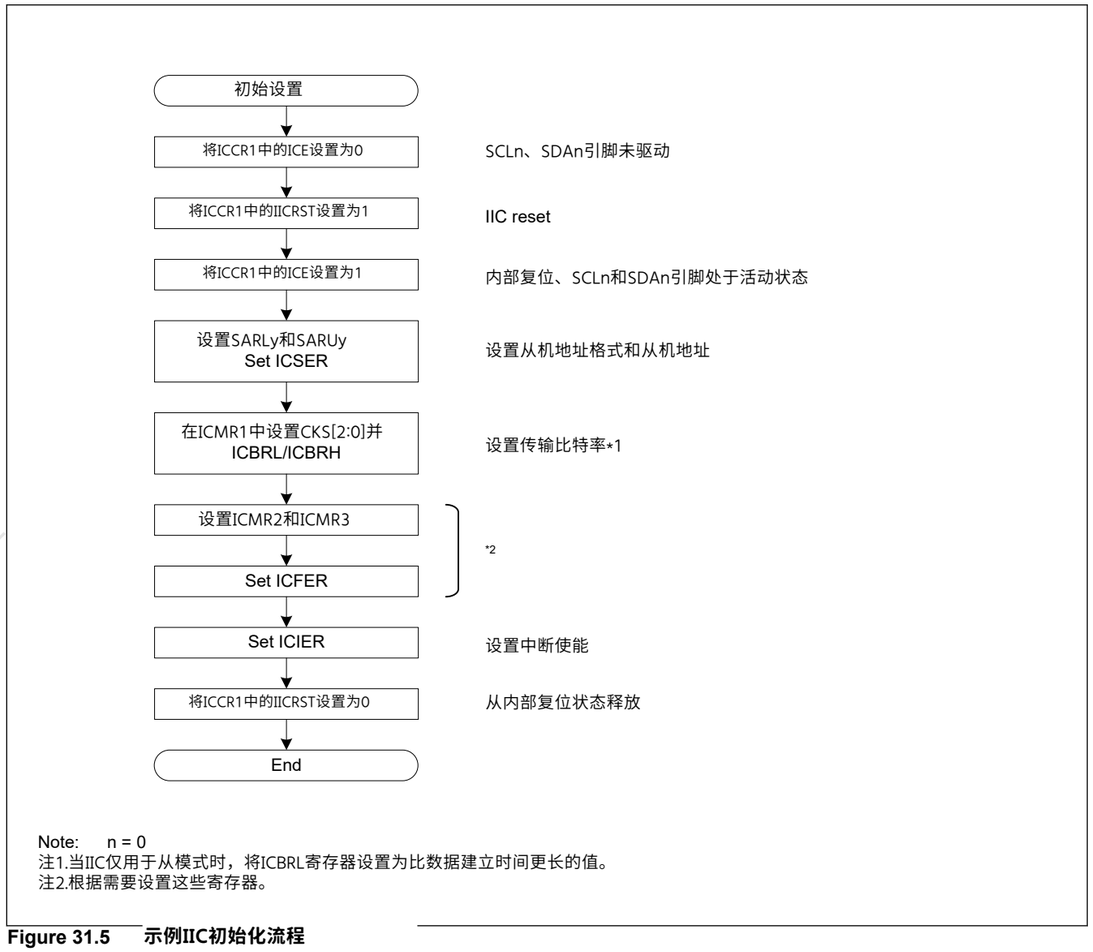
In master transmit operation, the IIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 31.6 shows an example of master transmission, and Figure 31.7 to Figure 31.9 show the operation timing in master transmission.

To set up and perform master transmission:

1. Process initial settings. For details, see section 31.3.2. Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and START flags in ICSR2 automatically set to 1 and the ST bit automatically is set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that issuance of the start condition as requested by the ST bit is successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 also automatically is set to 1 in response to the setting of the TRS bit to 1.

5.完成所需的寄存器设置后，将ICCR1.IICRST位设置为0以释放IIC复位。

如果IIC初始化已经完成，则不需要此过程。



Note: n = 0
注1.当IIC仅用于从模式时，将ICBRL寄存器设置为比数据建立时间更长的值。
注2.根据需要设置这些寄存器。

Figure 31.5 示例IIC初始化流程

31.3.3 主发送操作

在主设备发送操作中，IIC作为主设备输出SCL时钟和发送的数据信号，从设备返回确认。图31.6显示了主传输的示例，图31.7至图31.9显示了主传输的操作时序。

设置和执行主传输：

1.处理初始设置。有关详细信息，请参阅第31.3.2节。初始设置。

2.读取ICCR2中的BBSY标志，检查总线是否空闲，然后将ICCR2中的ST位设置为1（启动条件要求）。收到请求后，IIC发出一个开始条件。同时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。此时，如果检测到启动条件，内部电平为SDA输出状态和当ST位为1时SDAn线匹配，IIC识别出ST位请求的启动条件的发布已成功完成，并且ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。

3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag automatically is set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. After the byte containing the slave address and R/W# bit is transmitted, the value of the TRS bit automatically updates to select master transmit or master receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the IIC continues in master transmit mode. Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For data transmission with an address in the 10-bit format, start by writing 11110b, the 2 higher-order bits of the slave address, and W to ICDRT as the first address transmission. For the second address transmission, write the 8 lower-order bits of the slave address to ICDRT.
4. Check that the TDRE flag in ICSR2 is 1, and then write the transmit data to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready or a stop condition is issued.
5. After all bytes of transmit data are written to the ICDRT register, wait until the value in the TEND flag in ICSR2 returns to 1, and then set the SP bit in ICCR2 to 1 (stop condition requested). On receiving a stop condition request, the IIC issues the stop condition. Regarding issuing a stop condition, see section 31.11.3. Issuing a Stop Condition.
6. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, it automatically sets the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
7. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

3.检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。在发送包含从机地址和RW#位的字节后，TRS位的值会自动更新，以根据发送的RW#位的值选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。因为此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信中有错误，所以向ICCR2.SP位写入1以发出停止条件。对于地址为10位格式的数据传输，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。对于第二次地址传输，将从地址的低8位写入ICDRT。

4.检查ICSR2中的TDRE标志是否为1，然后将发送数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到发送数据准备好或发出停止条件。

5.将发送数据的所有字节写入ICDRT寄存器后，等待ICSR2中的TEND标志中的值返回1，然后将ICCR2中的SP位设置为1（请求停止条件）。在收到停止条件请求时，IIC发出停止条件。关于发出停止条件，请参阅第31.11.3节。发出停止条件。

6.在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机
接收模式。此外，它自动将TDRE和TEND标志设置为0，并将ICSR2中的STOP标志设置为1。

7.检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

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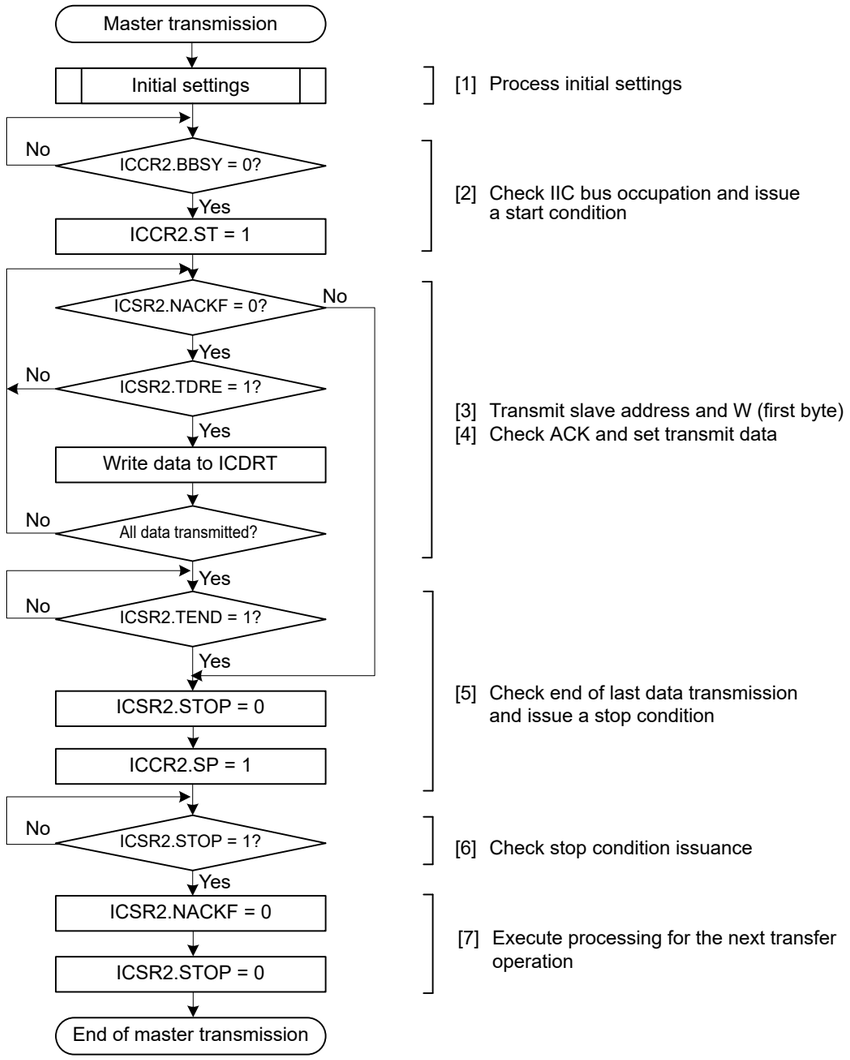

Figure 31.6 Example master transmission flow

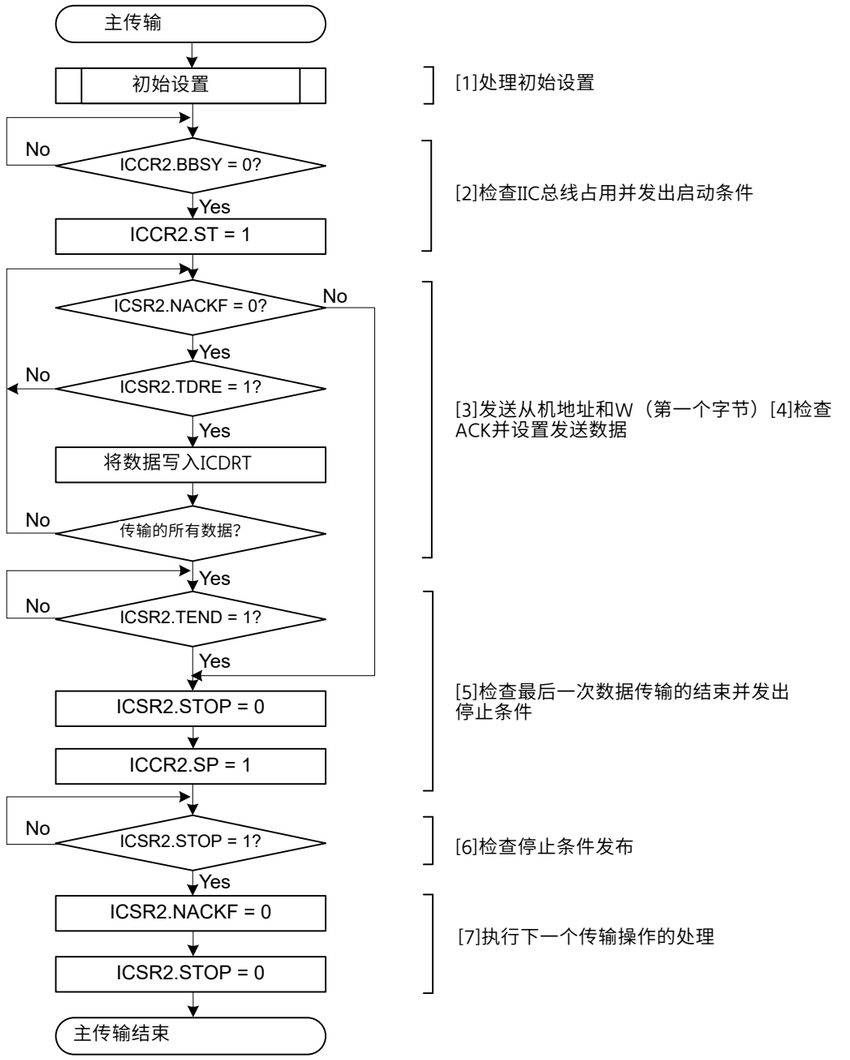

Figure 31.6 示例主传输流程

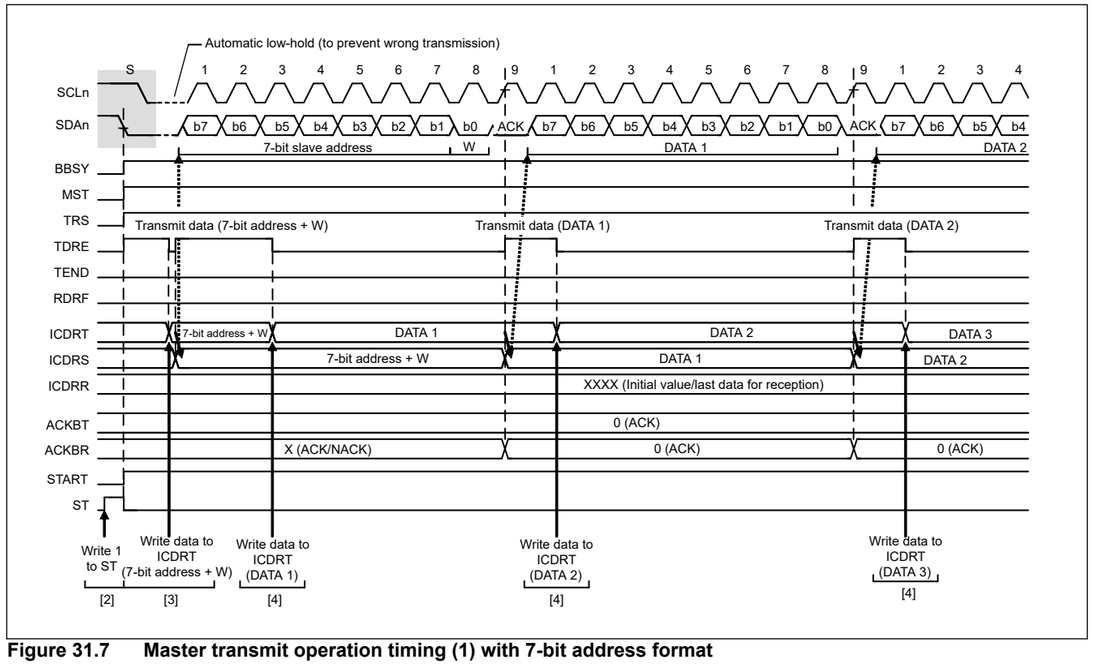

Figure 31.7 Master transmit operation timing (1) with 7-bit address format

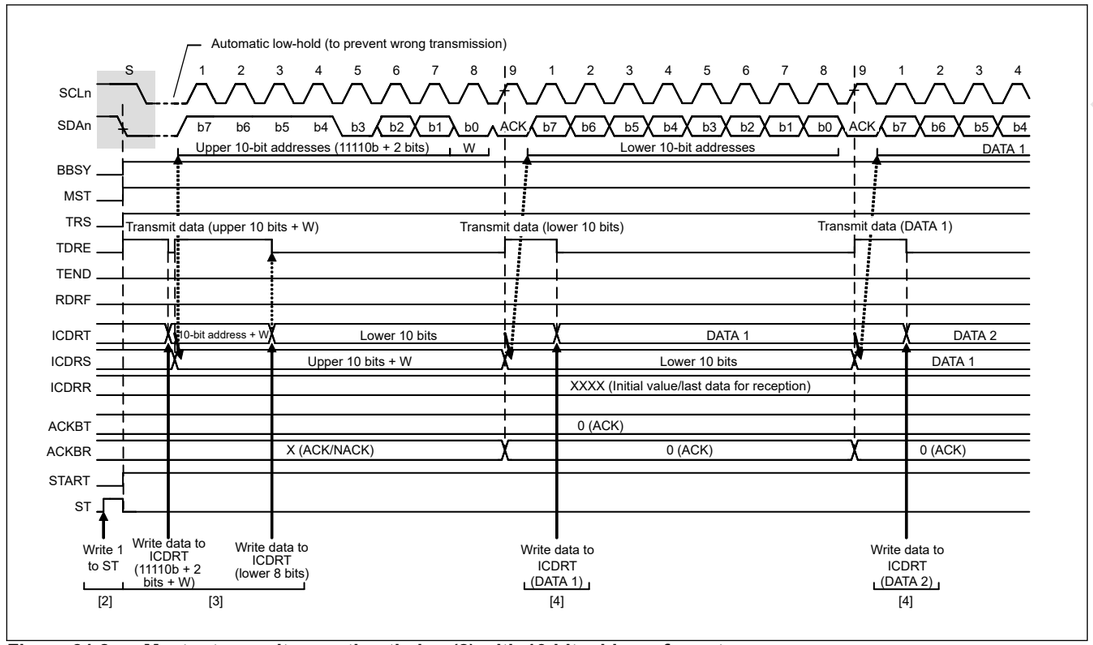

Figure 31.8 Master transmit operation timing (2) with 10-bit address format

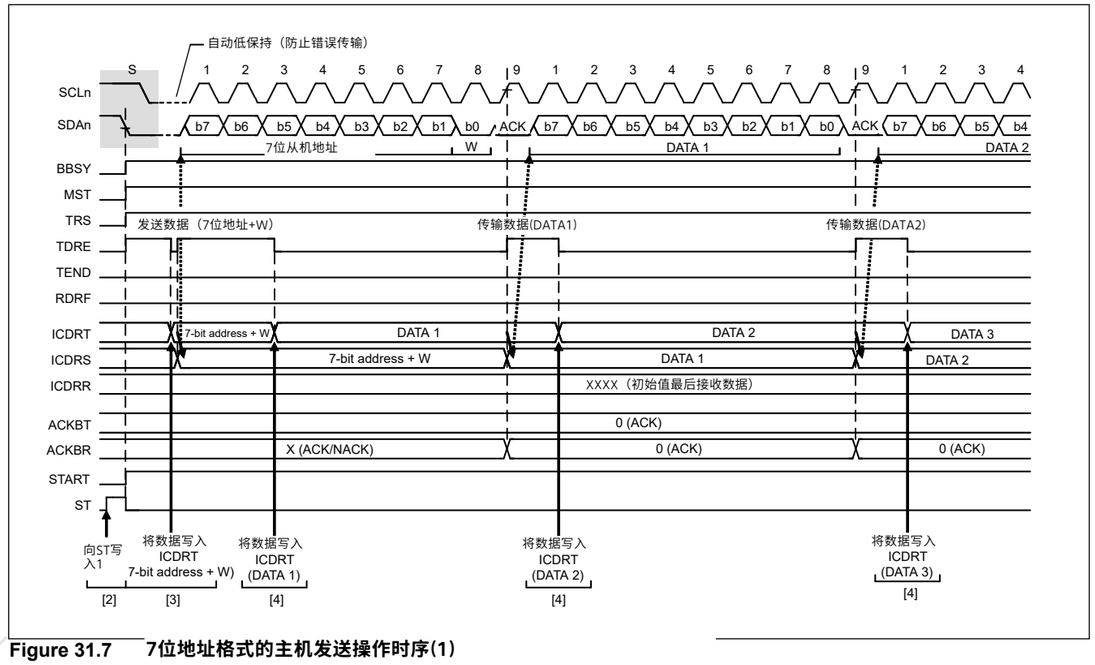

Figure 31.7 7位地址格式的主机发送操作时序(1)

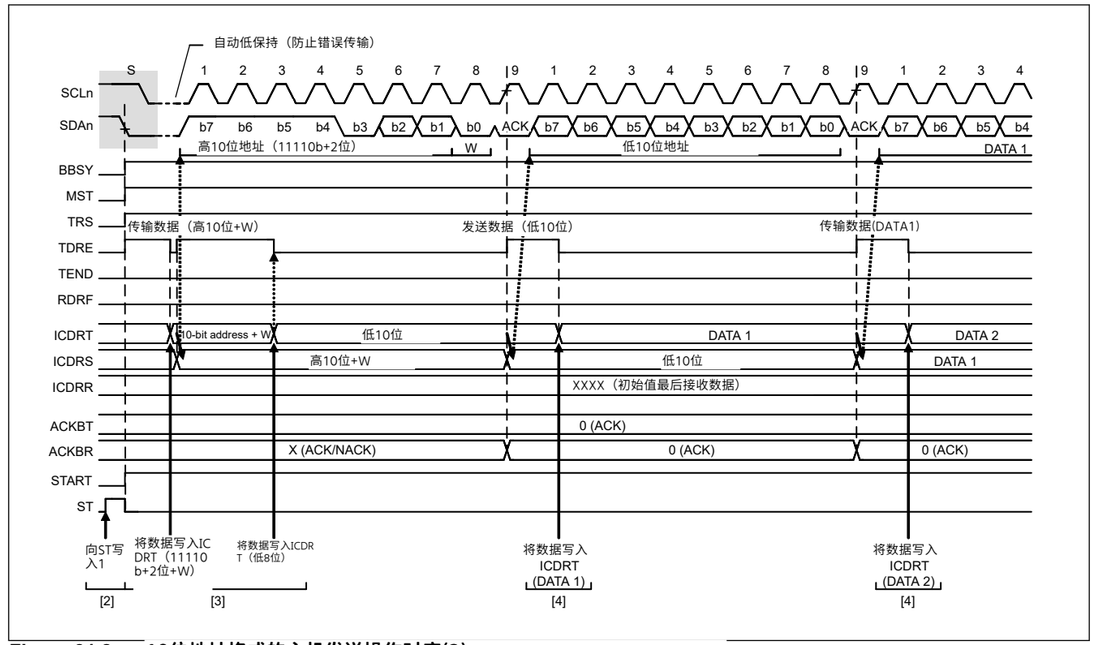

Figure 31.8 10位地址格式的主机发送操作时序(2)

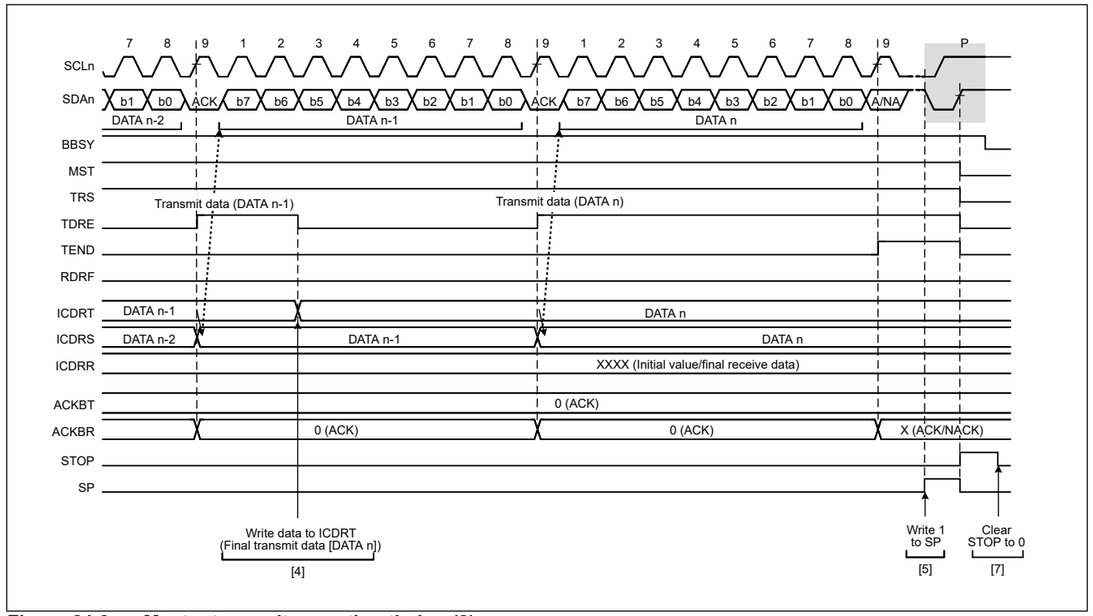

Figure 31.9 Master transmit operation timing (3)

31.3.4 Master Receive Operation

In master receive operation, the IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the IIC must start by sending a slave address to the associated slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 31.10 and Figure 31.11 show examples of master reception (7-bit address format), and Figure 31.12 to Figure 31.14 show the operation timing in master reception.

To set up and perform master reception:

1. Process initial settings. For details, see section 31.3.2. Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. When the IIC detects the start condition, the BBSY and START flags in ICSR2 automatically set to 1, and the ST bit automatically is set to 0. At this time, if the start condition is detected and the levels for the SDA output and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that issuance of the start condition as requested by the ST bit is successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 also automatically is set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag automatically is set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. When the byte containing the slave address and R/W# bit is transmitted, the value of the ICCR2.TRS bit automatically updates to select transmit or receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit is 1, the TRS bit is set to 0 on the rising edge of the ninth cycle of the SCL clock, placing the IIC in master receive mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag automatically is set to 1.
   Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmitting 11110b, the two higher-order bits of the slave address, and the R bit places the IIC in master receive mode.
4. Dummy read ICDRR after confirming that the RDRF flag in ICSR2 is 1. This makes the IIC start output of the SCL clock and start data reception.

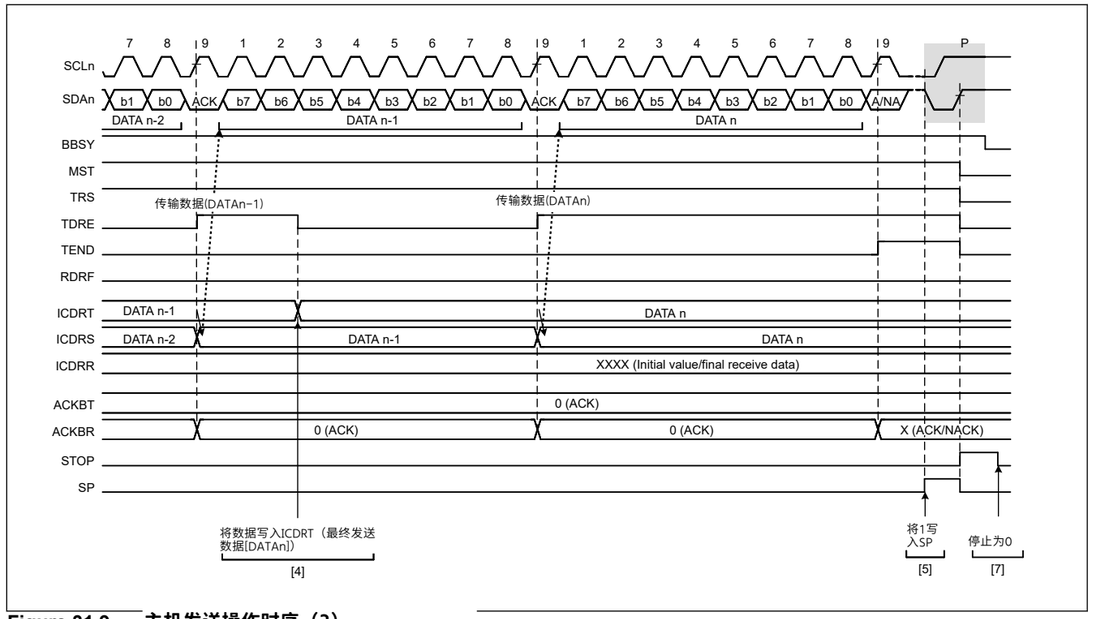

Figure 31.9 主机发送操作时序（3）

31.3.4 主接收操作

在主设备接收操作中，作为主设备的IIC输出SCL时钟，从从设备接收数据，并返回确认。因为IIC必须首先向相关的从设备发送一个从地址，所以这部分程序在主发送模式下执行，但后续步骤在主接收模式下执行。

图31.10和图31.11显示了主机接收的示例（7位地址格式），图31.12至图31.14显示了主机接收的操作时序。

设置和执行主接收：

1.处理初始设置。有关详细信息，请参阅第31.3.2节。初始设置。

2.读取ICCR2中的BBSY标志，检查总线是否空闲，然后将ICCR2中的ST位设置为1（启动条件要求）。收到请求后，IIC发出一个开始条件。当IIC检测到启动条件时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。此时，如果检测到启动条件，则SDA输出的电平和电平在ST位为1时SDAn线匹配时，IIC识别出由ST位请求的启动条件的发布已成功完成，并且MST和

ICCR2中的TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。

3、检查ICSR2中的TDRE标志为1，然后写入值进行发送（第一个字节表示从机RW#位的地址和值）到ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。当发送包含从机地址和RW#位的字节时，ICCR2.TRS位的值自动更新以根据发送的RW#位的值选择发送或接收模式。如果RW#位的值为1，则在SCL时钟的第9个周期的上升沿将TRS位设置为0，将IIC置于主机接收模式。此时TDRE标志置0，ICSR2.RDRF标志自动置1。因为此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信出现错误，向ICCR2.SP位写入1以发出停止条件。对于来自具有10位地址的设备的主机接收，首先使用主机发送来发出10位地址，然后发出重启条件。之后，发送11110b、从机地址的两个高阶位和R位将IIC置于主机接收模式。

4.确认ICSR2中的RDRF标志为1后伪读ICDRR。这使得IIC开始输出SCL时钟并开始数据接收。

5. After 1 byte of data is received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the 8th or 9th cycle of the SCL clock, as selected in the RDRFS bit in ICMR3. Reading ICDRR at this time produces the received data, and the RDRF flag is automatically set to 0 at the same time. Additionally, the value of the acknowledgment field received during the ninth cycle of the SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the second-to-last byte, set the ICMR3.WAIT bit to 1 for wait insertion before reading ICDRR, containing the second-to-last byte. In addition to enabling NACK output, even when interrupts or other operations result in delays in setting the ICMR3.ACKBT bit to 1 (NACK) in step (6), this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, which enables the issuing of a stop condition.
6. When the ICMR3.RDRFS bit is 0, and the slave device must be notified that it is to end transfer for data reception after transfer of the next and final byte, set the ICMR3.ACKBT bit to 1 (NACK).
7. After reading the second-to-last byte from the ICDRR register, if the value of the ICSR2.RDRF flag is 1, write 1 to the SP bit in ICCR2 (stop condition requested), and then read the last byte from ICDRR. When ICDRR is read, the IIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is complete or the SCLn line is released from the low-hold state.
8. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, detection of the stop condition sets the ICSR2.STOP flag to 1.
9. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

5.接收到1个字节的数据后，在SCL时钟的第8或第9个周期的上升沿将ICSR2中的RDRF标志设置为1，这由ICMR3中的RDRFS位选择。此时读取ICDRR产生接收数据，同时RDRF标志位自动置0。此外，在SCL时钟的第9个周期内接收到的确认字段的值作为ICMR3.ACKBT位中设置的值返回。如果要接收的下一个字节是倒数第二个字节，则在读取包含倒数第二个字节的ICDRR之前将ICMR3.WAIT位设置为1以等待插入。除了使能NACK输出外，即使在中断或其他操作导致在步骤(6)中将ICMR3.ACKBT位设置为1(NACK)时出现延迟，这也会在第9次的上升沿将SCLn线固定为低电平接收最后一个字节的时钟周期，它可以发出停止条件。

6.当ICMR3.RDRFS位为0时，必须通知从设备在传输下一个和最后一个字节后结束传输以进行数据接收，将ICMR3.ACKBT位设置为1(NACK)。

7.从ICDRR寄存器中读取倒数第二个字节后，如果ICSR2.RDRF标志的值为1，则将1写入ICCR2中的SP位（请求停止条件），然后从ICDRR中读取最后一个字节.当读取ICDRR时，IIC从等待状态中释放，并在第9个时钟周期的低电平输出完成或SCLn线从低保持状态释放后发出停止条件。

8.在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机接收模式。此外，检测到停止条件会将ICSR2.STOP标志设置为1。

9.检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

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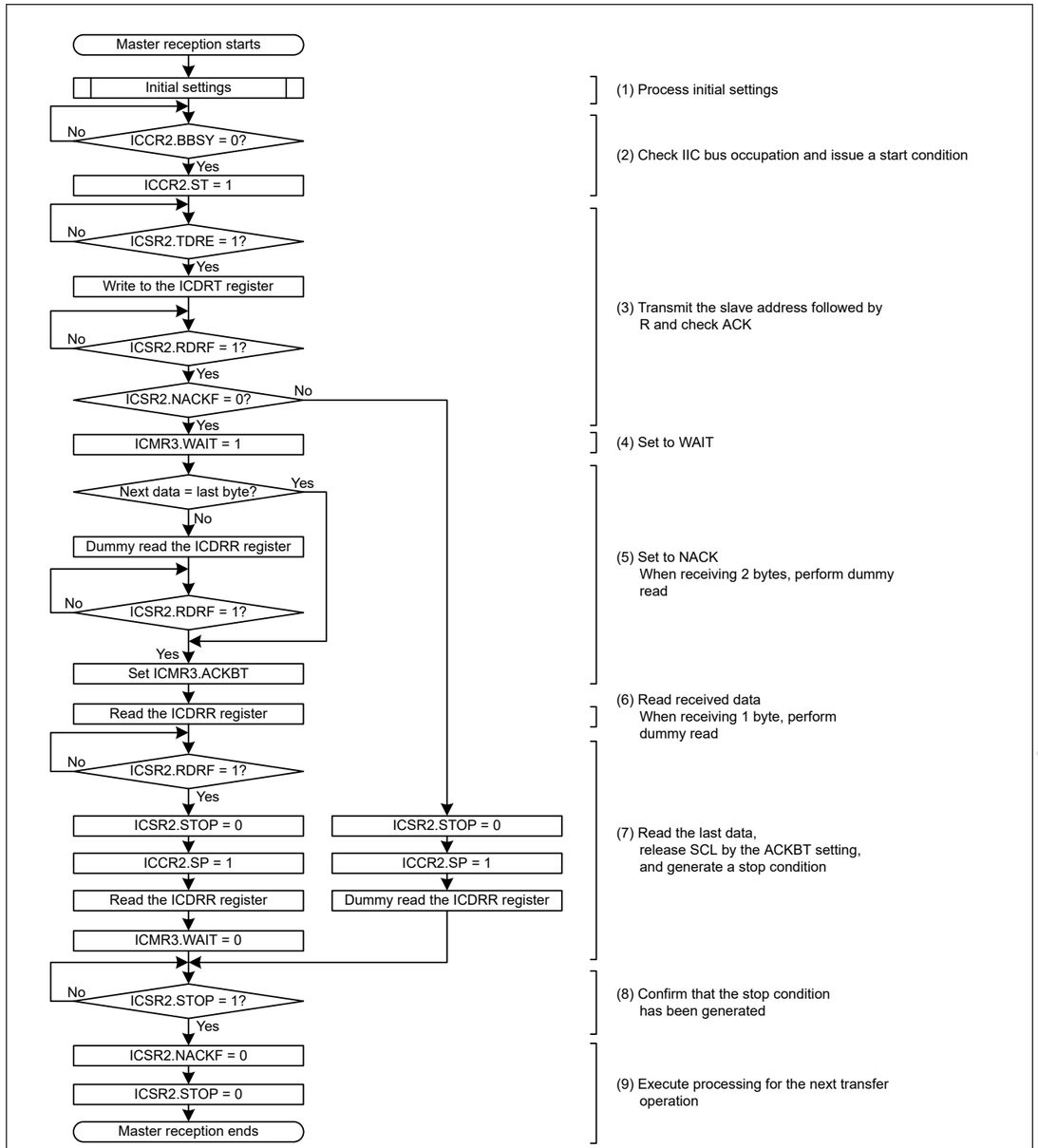


Figure 31.10 Example master reception flow with 7-bit address format of 1 byte or 2 bytes

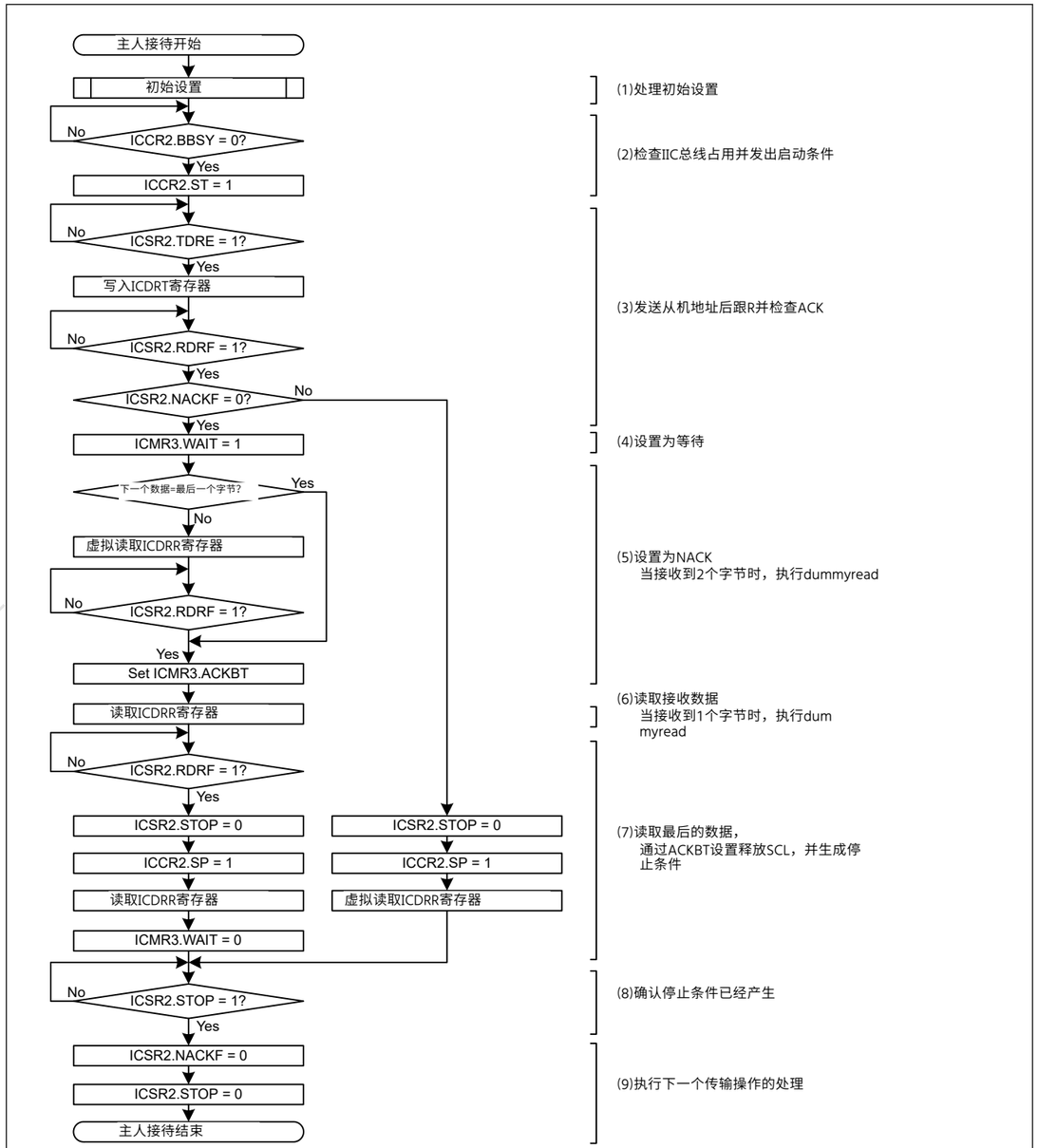


Figure 31.10 具有1字节或2字节的7位地址格式的主机接收流程示例

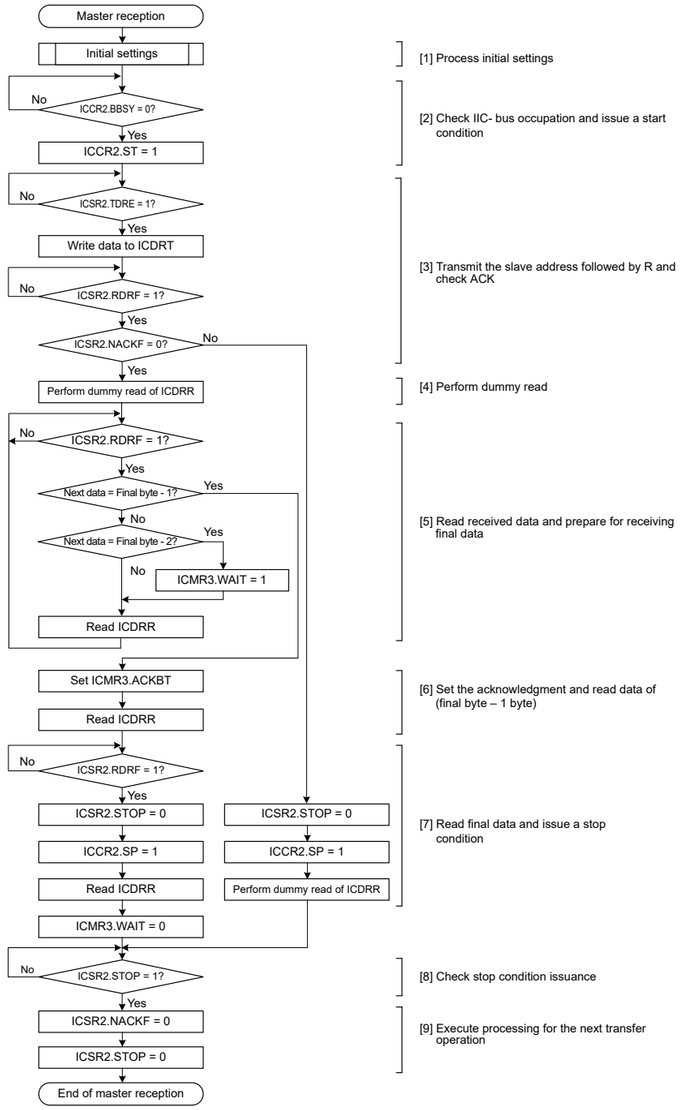


Figure 31.11 Example master reception flow with 7-bit address format of 3 or more bytes

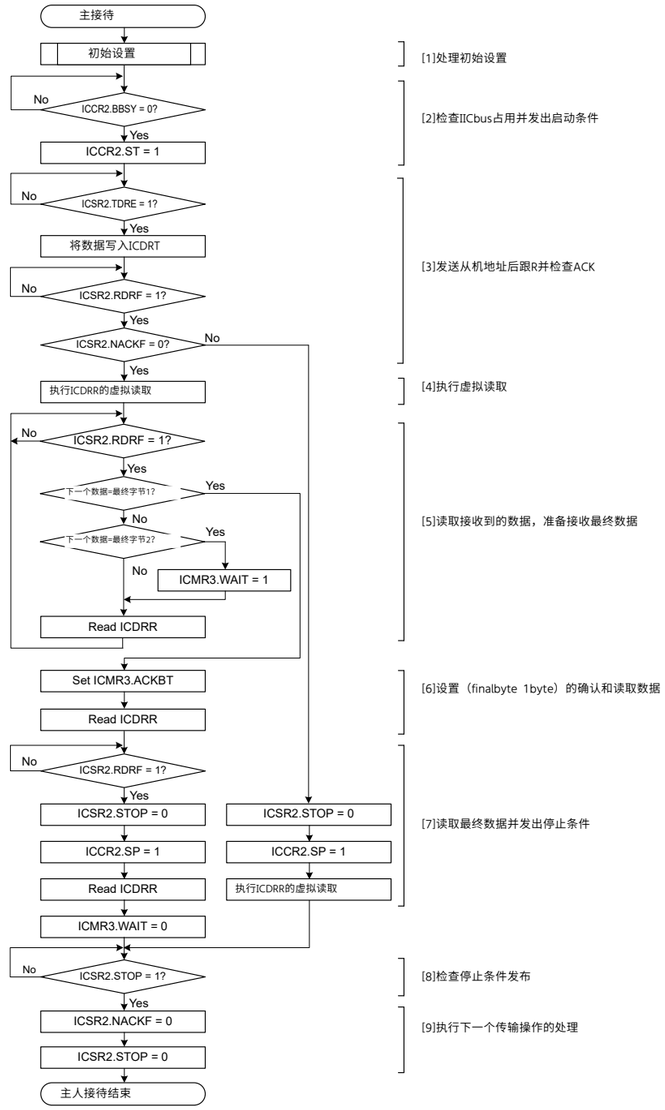


Figure 31.11 具有3个或更多字节的7位地址格式的示例主机接收流程

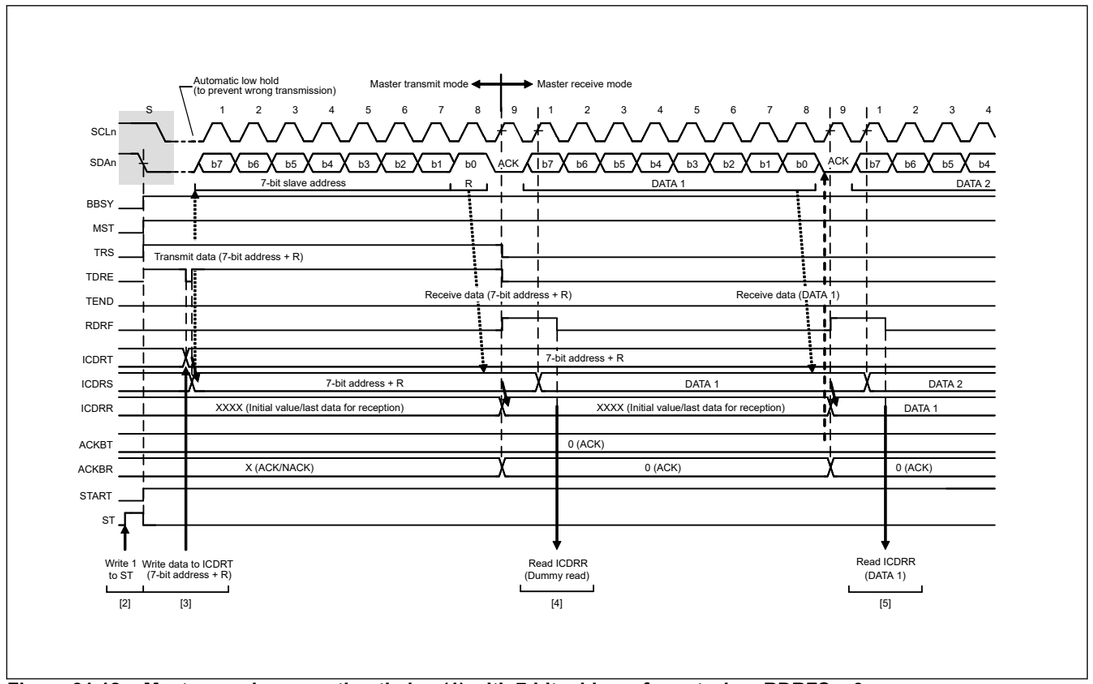


Figure 31.12 Master receive operation timing (1) with 7-bit address format when RDRFS = 0

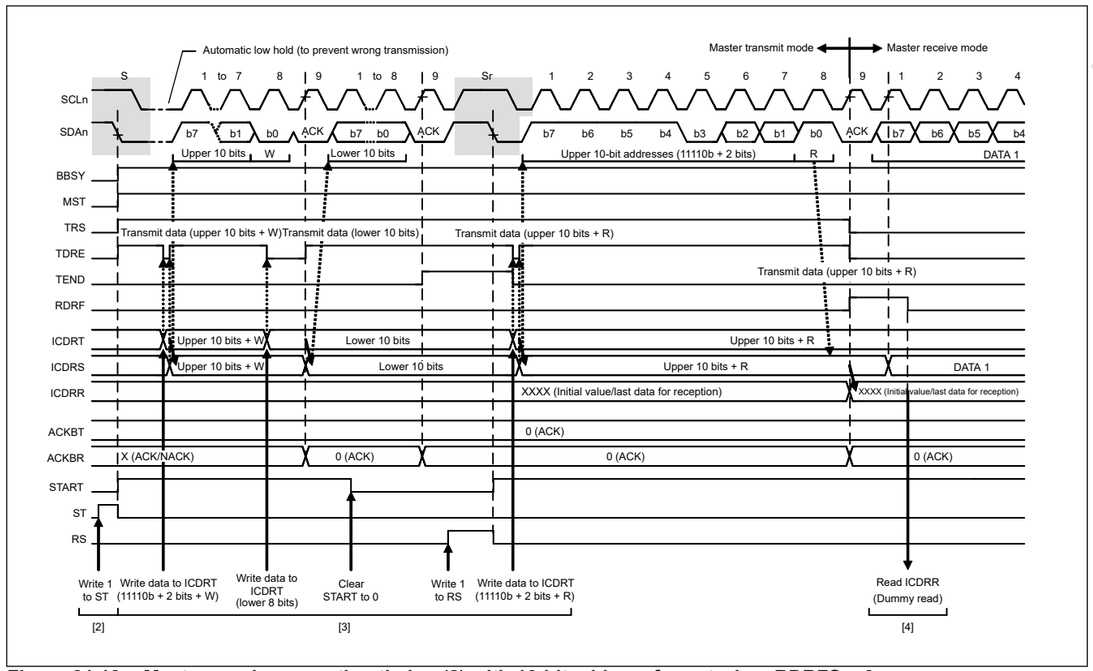


Figure 31.13 Master receive operation timing (2) with 10-bit address format when RDRFS = 0

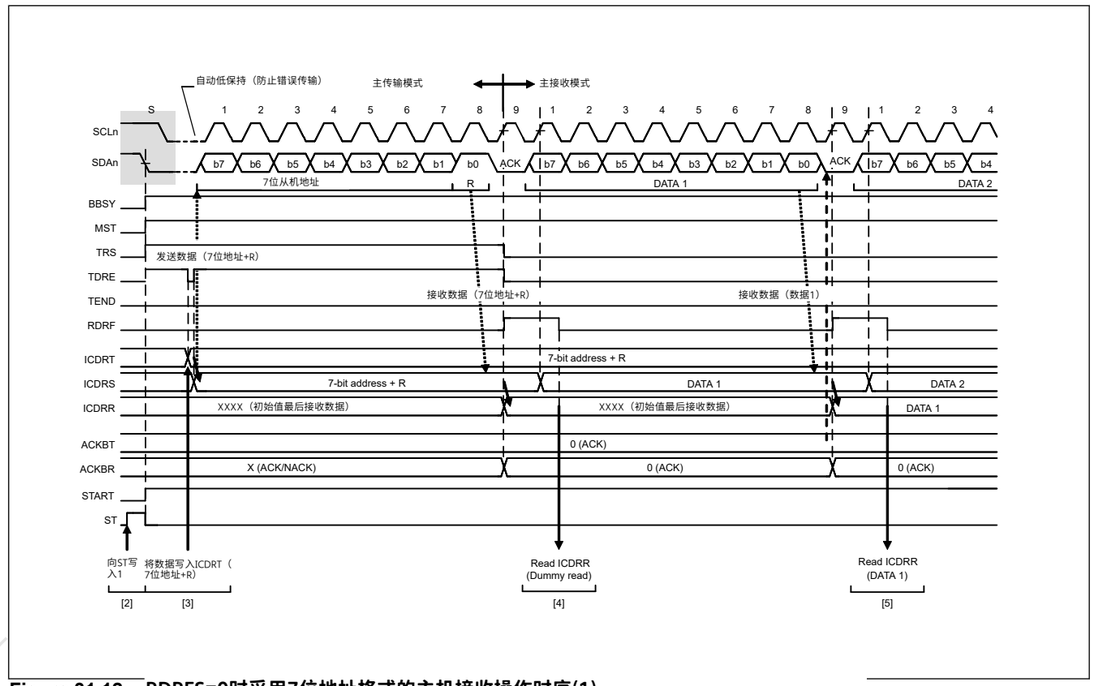


Figure 31.12 RDRFS=0时采用7位地址格式的主机接收操作时序(1)

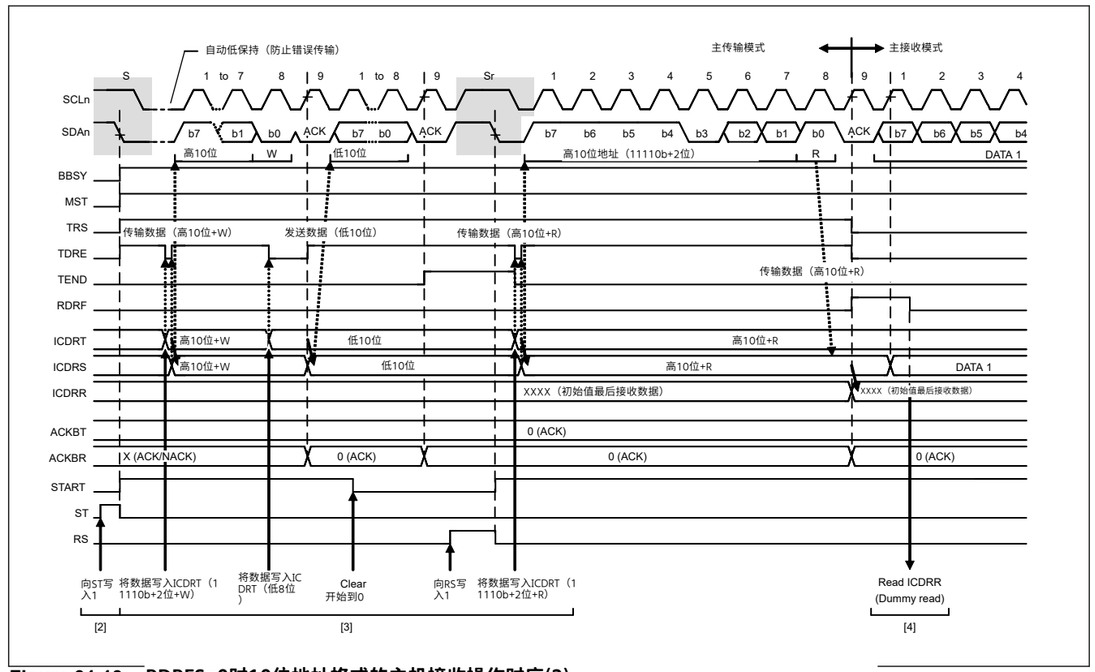


Figure 31.13 RDRFS=0时10位地址格式的主机接收操作时序(2)

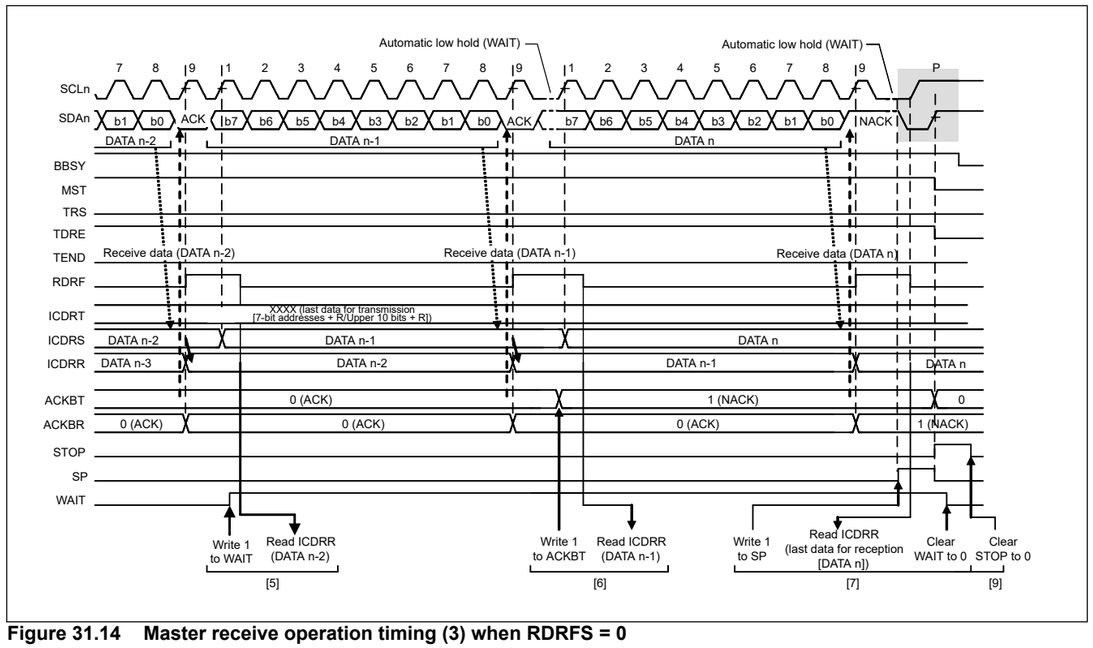


Figure 31.14 Master receive operation timing (3) when RDRFS = 0

31.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the IIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 31.15 shows an example of slave transmission, and Figure 31.16 and Figure 31.17 show the operation timing in slave transmission.

To set up and perform slave transmission:

1. Initialize the IIC using the procedure in section 31.3.2. Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the R/W# bit is 1, the IIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.
3. Check that the ICSR2.TDRE flag is 1, then write the transmit data to the ICDRT register. If the IIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the IIC suspends transfer of the next data.
4. Wait until the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the IIC drives the SCLn line low on the ninth falling edge of the SCL clock.
5. When the ICSR2.NACKF or ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.
6. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy flags (y = 0 to 2), the ICSR2.TDRE and TEND flags, and the ICCR2.TRS bit to 0, and enters slave receive mode.
7. Check that the ICSR2.STOP flag is 1, then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

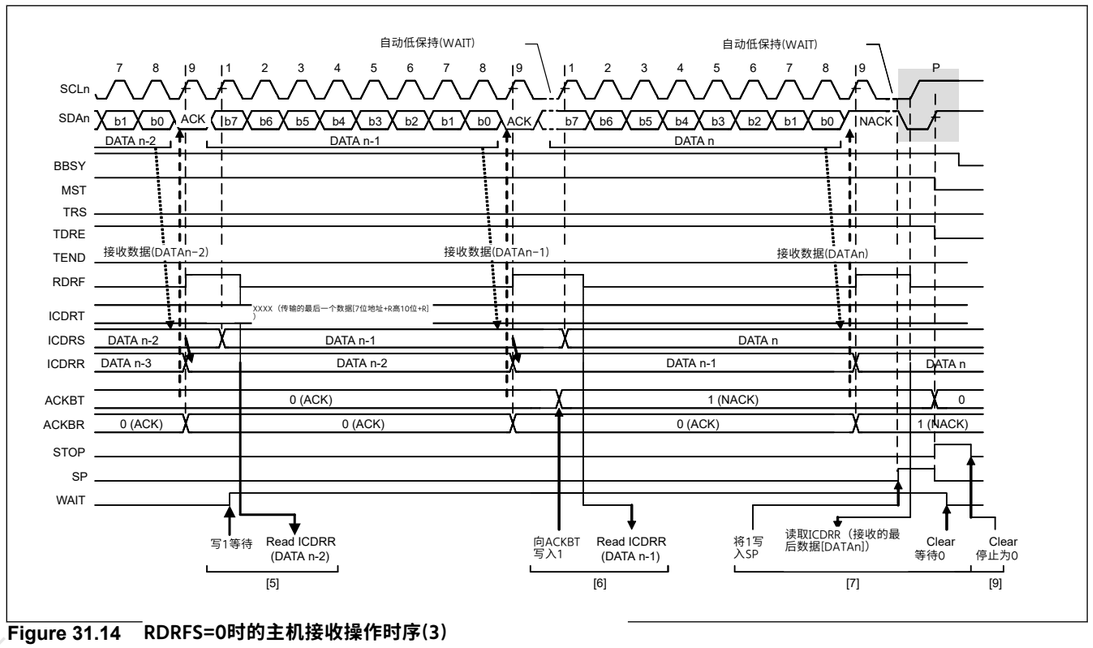


Figure 31.14 RDRFS=0时的主机接收操作时序(3)

31.3.5 从机发送操作

在从发送操作中，主设备输出SCL时钟，IIC作为从设备发送数据，主设备返回确认。

图31.15显示了从机传输的示例，图31.16和图31.17显示了从机传输的操作时序。

设置和执行从属传输：

1.使用第31.3.2节中的过程初始化IIC。初始设置。
初始化后，IIC一直处于待机状态，直到收到匹配的从机地址。

2.接收到匹配的从地址后，IIC在SCL时钟的第9个周期的上升沿将相关的ICSR1.HOA、GCA和AASy标志之一（y=0到2）设置为1，并输出该值在SCL时钟的第9个周期将ICMR3.ACKBT位设置为确认位。如果RW#位的值为1，则IIC通过将ICCR2.TRS位和ICSR2.TDRE标志都设置为1自动将自身置于从发送模式。

3.检查ICSR2.TDRE标志是否为1，然后将发送数据写入ICDRT寄存器。如果IIC没有收到
当ICFER.NACKE位为1时，来自主设备的确认（接收NACK信号），IIC暂停下一个数据的传输。

4.等到ICSR2.TEND标志设置为1，而ICSR2.TDRE标志为1，在ICSR2.NACKF标志设置为1或将要发送的最后一个字节写入ICDRT寄存器之后。当ICSR2.NACKF标志或TEND标志为1时，IIC在SCL时钟的第九个下降沿将SCLn线驱动为低电平。

5.当ICSR2.NACKF或ICSR2.TEND标志为1时，假读ICDRR完成处理。这将释放SCLn线。

6.在检测到停止条件时，IIC自动将ICSR1.HOA、GCA和AASy标志（y=0到2）、ICSR2.TDRE和TEND标志以及ICCR2.TRS位设置为0，并进入从机接收模式。

7.检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

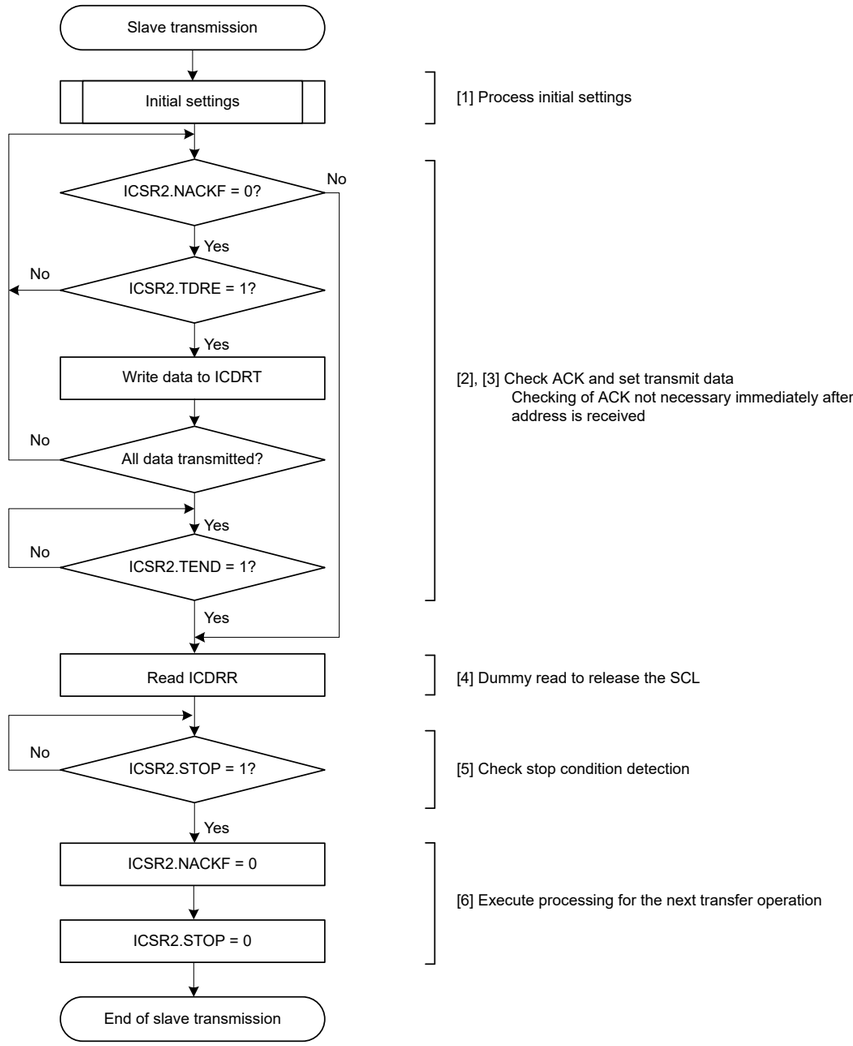


Figure 31.15 Example slave transmission flow

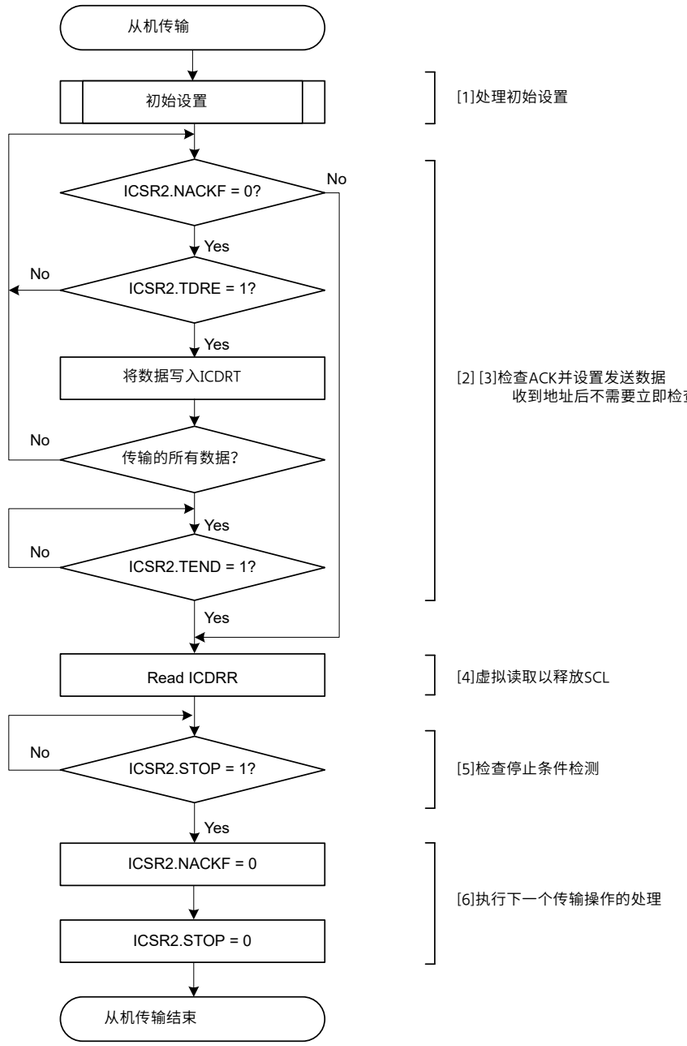


Figure 31.15 从机传输流程示例

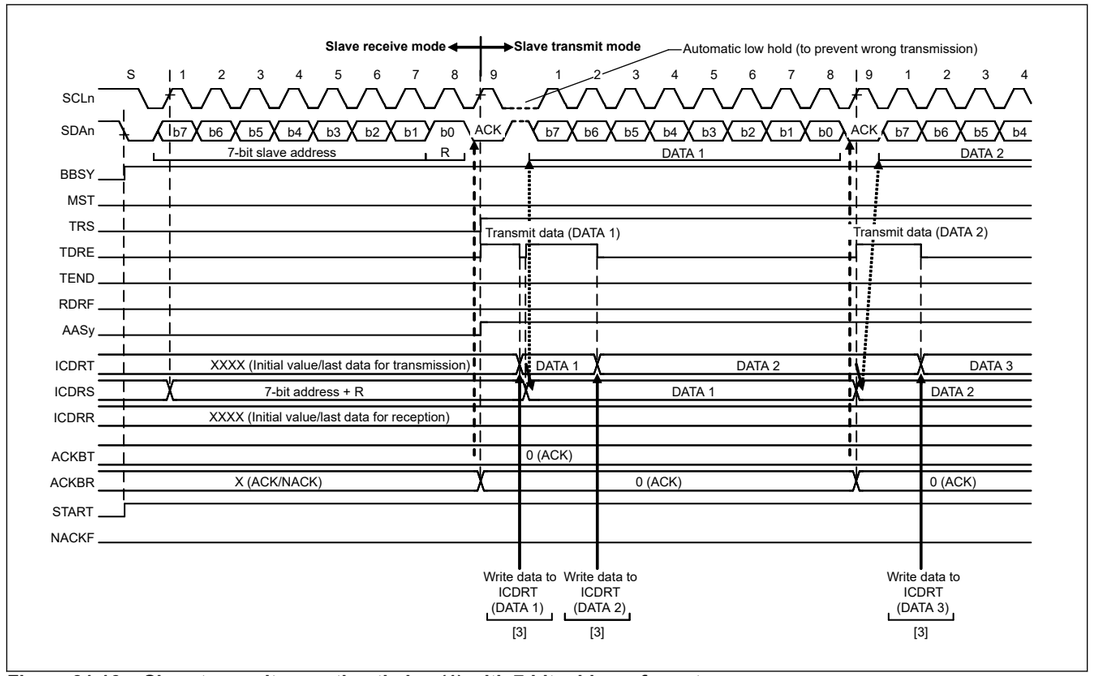


Figure 31.16 Slave transmit operation timing (1) with 7-bit address format

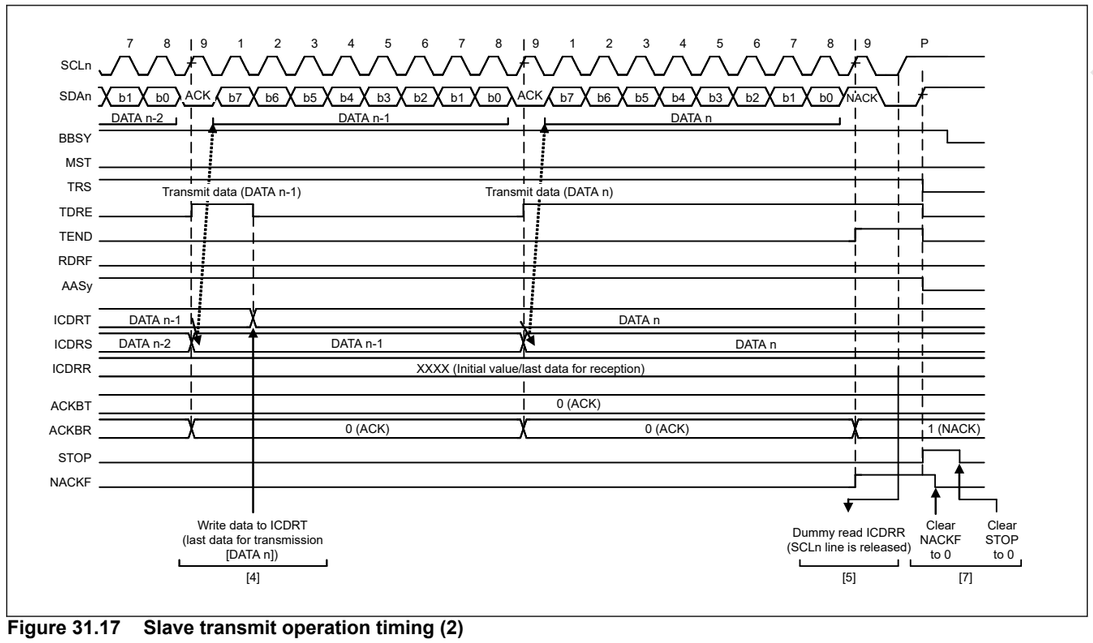


Figure 31.17 Slave transmit operation timing (2)

31.3.6 Slave Receive Operation

In slave receive operation, the master device outputs the SCL clock and transmit data, and the IIC returns acknowledgments as a slave device.

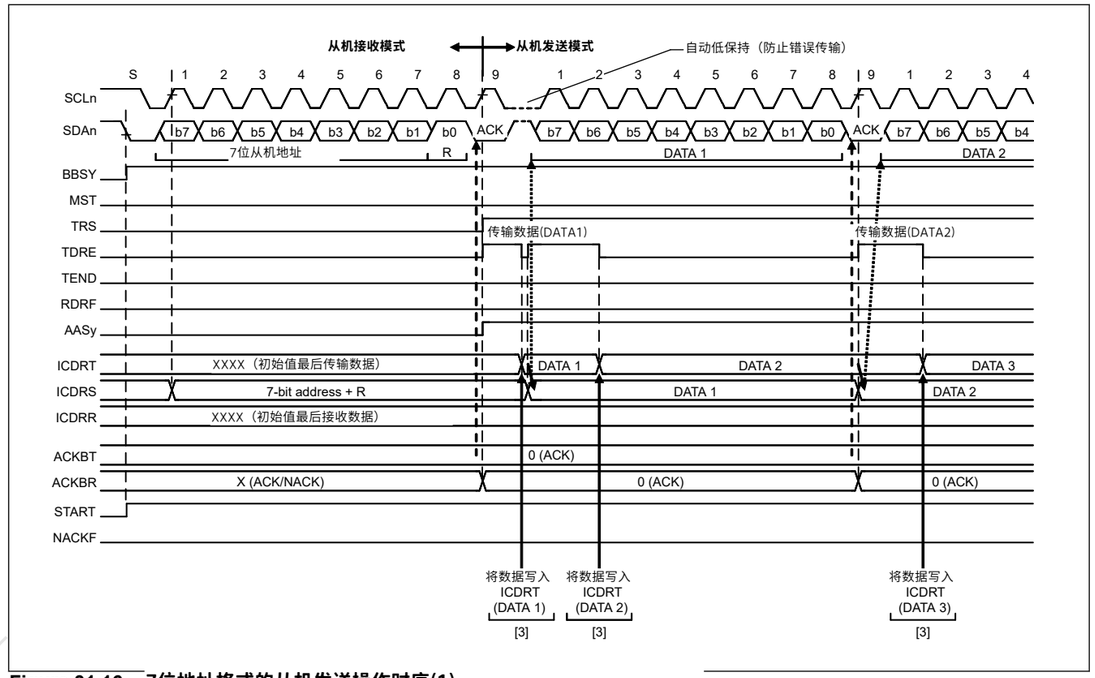


Figure 31.16 7位地址格式的从机发送操作时序(1)

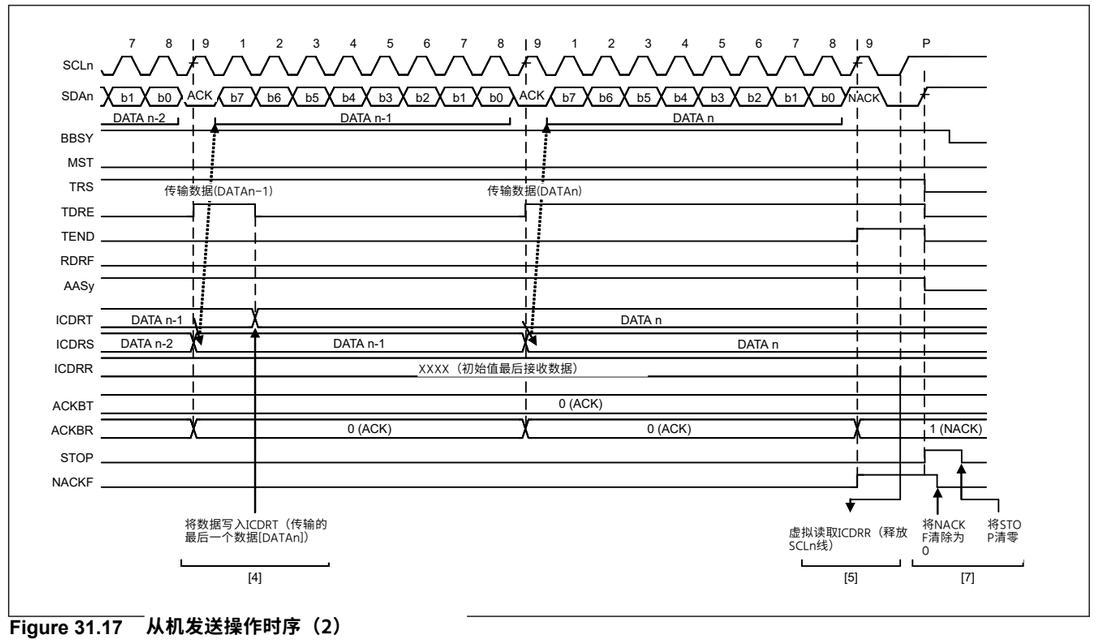


Figure 31.17 从机发送操作时序（2）

31.3.6 从机接收操作

在从机接收操作中，主设备输出SCL时钟并发送数据，IIC作为从设备返回确认。

Figure 31.18 shows an example of slave reception, and Figure 31.19 and Figure 31.20 show the operation timing in slave reception.

To set up and perform slave reception:

1. Initialize the IIC using the procedure in section 31.3.2. Initial Settings.
   After initialization, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the R/W# bit is 0, the IIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.
3. Check that the ICSR2.STOP flag is 0 and the ICSR2.RDRF flag is 1, then dummy read ICDRR. The dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected.
4. When ICDRR is read, the IIC automatically sets the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and a next byte is received while the RDRF flag is still set to 1, the IIC holds the SCLn line low until 1 SCL cycle before the point where RDRF must be set. In this case, reading ICDRR releases the SCLn line from being held low.
   When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.
5. On detecting the stop condition, the IIC automatically clears the ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 0.
6. Check that the ICSR2.STOP flag is 1, then set the ICSR2.STOP flag to 0 for the next transfer operation.

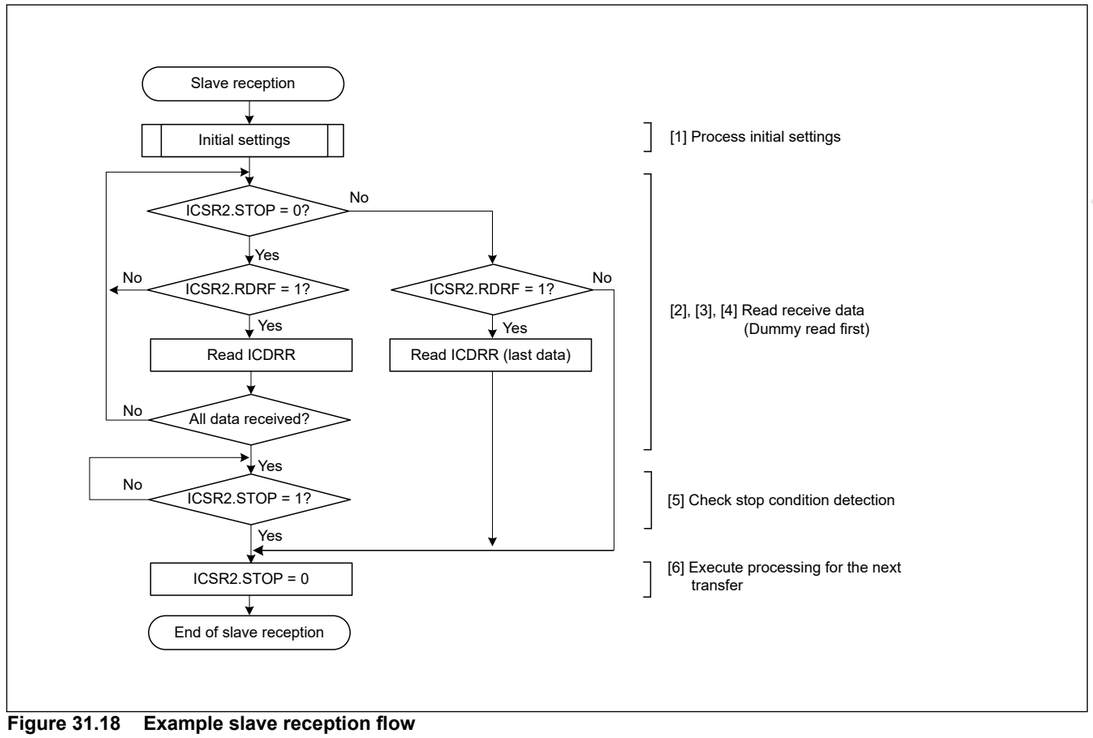


Figure 31.18 Example slave reception flow

图31.18显示了从机接收的示例，图31.19和图31.20显示了从机接收的操作时序。

设置和执行从属接收：

1.使用第31.3.2节中的过程初始化IIC。初始设置。
初始化后，IIC一直处于待机状态，直到收到匹配的从机地址。

2.接收到匹配的从地址后，IIC在SCL时钟的第9个周期的上升沿将相关的ICSR1.HOA、GCA和AASy标志之一（y=0到2）设置为1，并输出该值在SCL时钟的第9个周期将ICMR3.ACKBT位设置为确认位。如果RW#位的值为0，则IIC继续将自身置于从机接收模式并将ICSR2中的RDRF标志设置为1。

3.检查ICSR2.STOP标志为0且ICSR2.RDRF标志为1，然后虚拟读取ICDRR。虚拟值
选择7位地址格式时由从机地址和RW#位组成，选择10位地址格式时由低8位组成。

4.读取ICDRR时，IIC自动将ICSR2.RDRF标志设置为0。如果ICDRR的读取延迟并且在RDRF标志仍设置为1时接收到下一个字节，则IIC将SCLn线保持为低电平直到1SCL在必须设置RDRF的点之前循环。在这种情况下，读取ICDRR会释放SCLn线的低电平。当ICSR2.STOP标志为1且ICSR2.RDRF标志也为1时，读取ICDRR直到完全接收到所有数据。

5.在检测到停止条件时，IIC自动将ICSR1.HOA、GCA和AASy标志（y=0到2）清除为0。

6.检查ICSR2.STOP标志是否为1，然后将ICSR2.STOP标志设置为0以进行下一次传输操作。

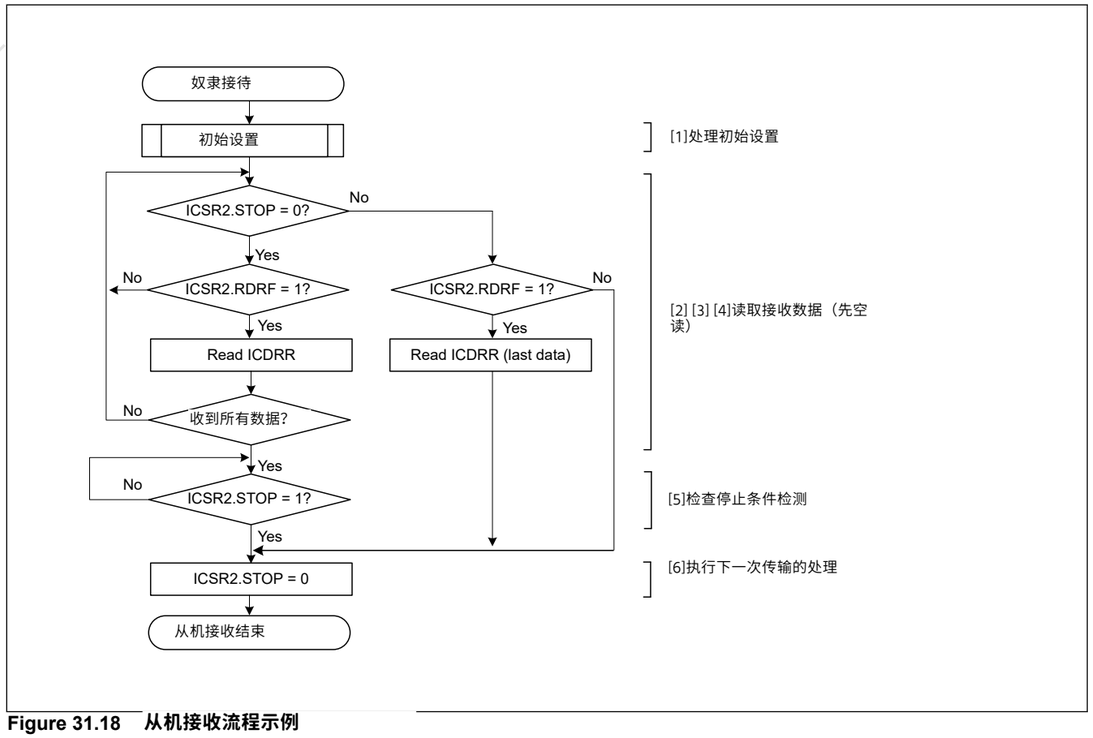


Figure 31.18 从机接收流程示例

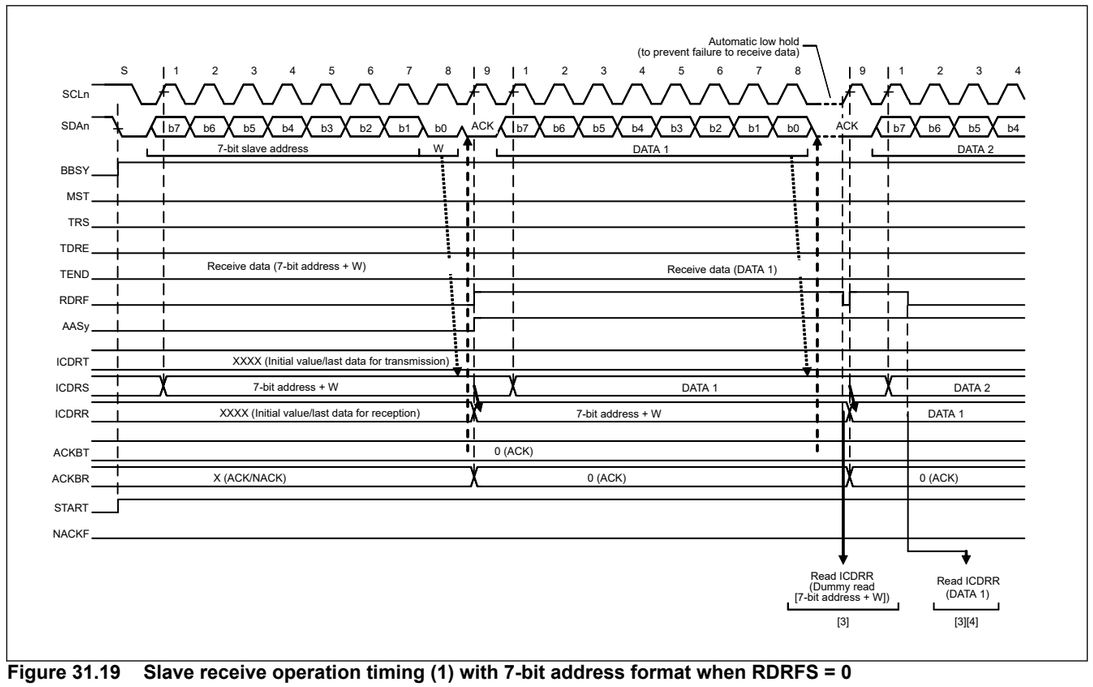


Figure 31.19 Slave receive operation timing (1) with 7-bit address format when RDRFS = 0

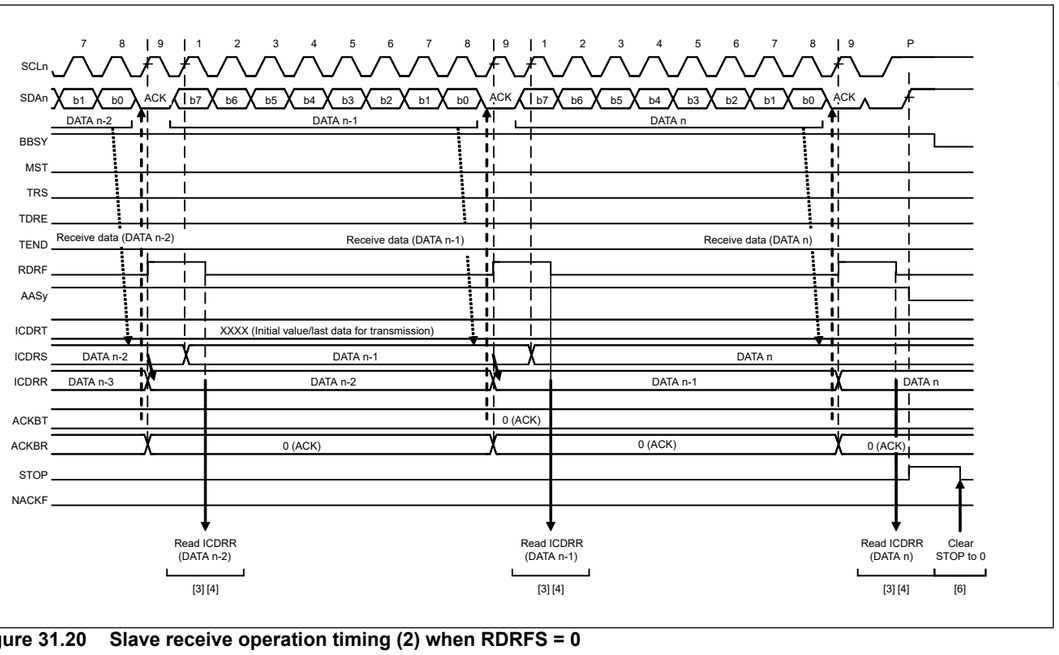


Figure 31.20 Slave receive operation timing (2) when RDRFS = 0

31.4 SCL Synchronization Circuit

For generation of the SCL clock, the IIC starts counting the value for the high-level period specified in ICBRH when it detects a rising edge on the SCLn line, and it drives the SCLn line low when it completes counting. When the IIC detects the falling edge of the SCLn line, it starts counting the value for the low-level period specified in ICBRL, and then it stops

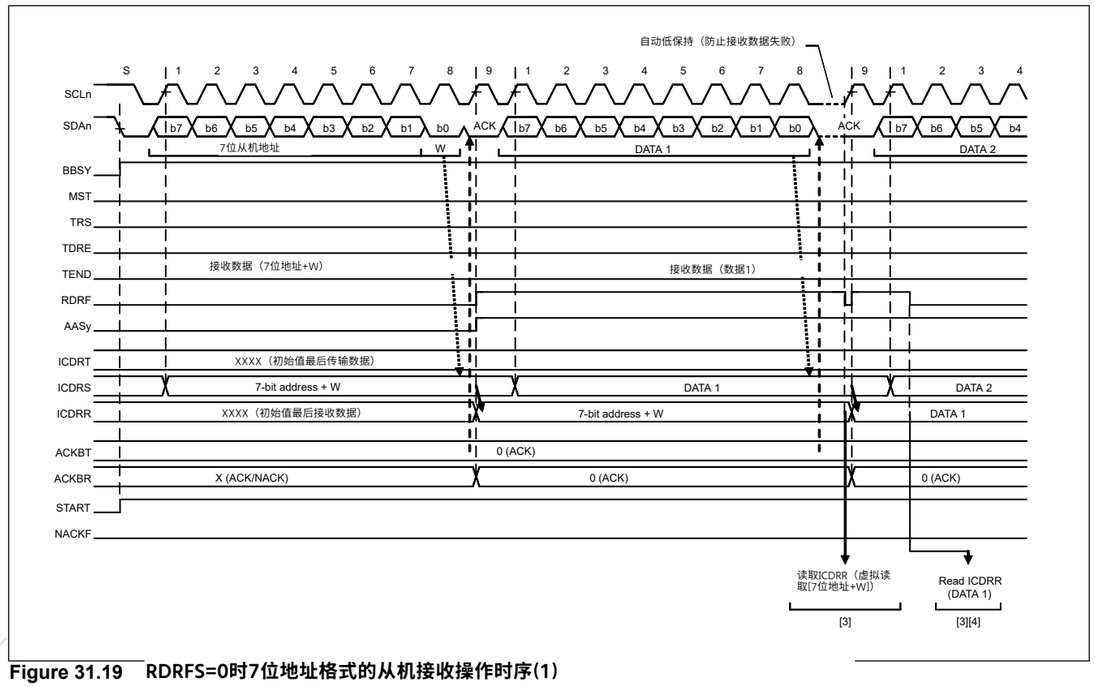


Figure 31.19 RDRFS=0时7位地址格式的从机接收操作时序(1)

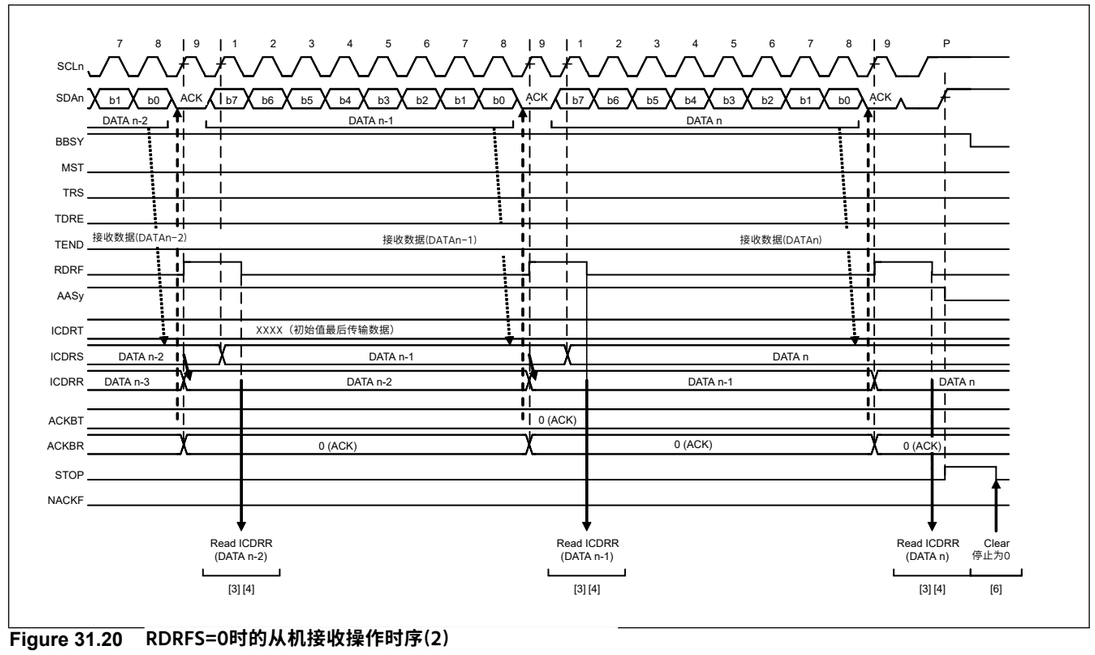


Figure 31.20 RDRFS=0时的从机接收操作时序(2)

31.4 SCL同步电路

为了生成SCL时钟，IIC在检测到SCLn线上的上升沿时开始对ICBRH中指定的高电平周期的值进行计数，并在完成计数时将SCLn线驱动为低电平。当IIC检测到SCLn线的下降沿时，它开始计数ICBRL中指定的低电平周期的值，然后停止

driving the SCLn line, releasing the line, when it completes counting. The IIC repeats this process to generate the SCL clock.

If multiple master devices are connected to the I2C bus, a collision of SCL signals might arise because of contention with another master device. In such cases, the master devices must synchronize their SCL signals. Because this synchronization of SCL signals must be bit-by-bit, the IIC is equipped with an SCL synchronization circuit to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the IIC detects a rising edge on the SCLn line and starts counting the high-level period specified in ICBRH.BRH[4:0], and the level on the SCLn line falls because an SCL signal is being generated by another master device, the IIC performs the following:

1. Stops counting when it detects the falling edge.
2. Drives the level on the SCLn line low.
3. Starts counting the low-level period specified in ICBRL.BRL[4:0].

When the IIC finishes counting the low-level period, it stops driving the SCLn line low to release the line. If the low-level period of the SCL clock signal from the other master device is longer than the low-level period set in the IIC, the low-level period of the SCL signal is extended. When the low-level period for the other master device ends, the SCL signal rises because the SCLn line is released.

When the IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, when SCL signals from more than one master are contending, the high-level period of the SCL signal is synchronized with that of the clock with the narrower period, and the low-level period of the SCL signal is synchronized with that of the clock with the broader period. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

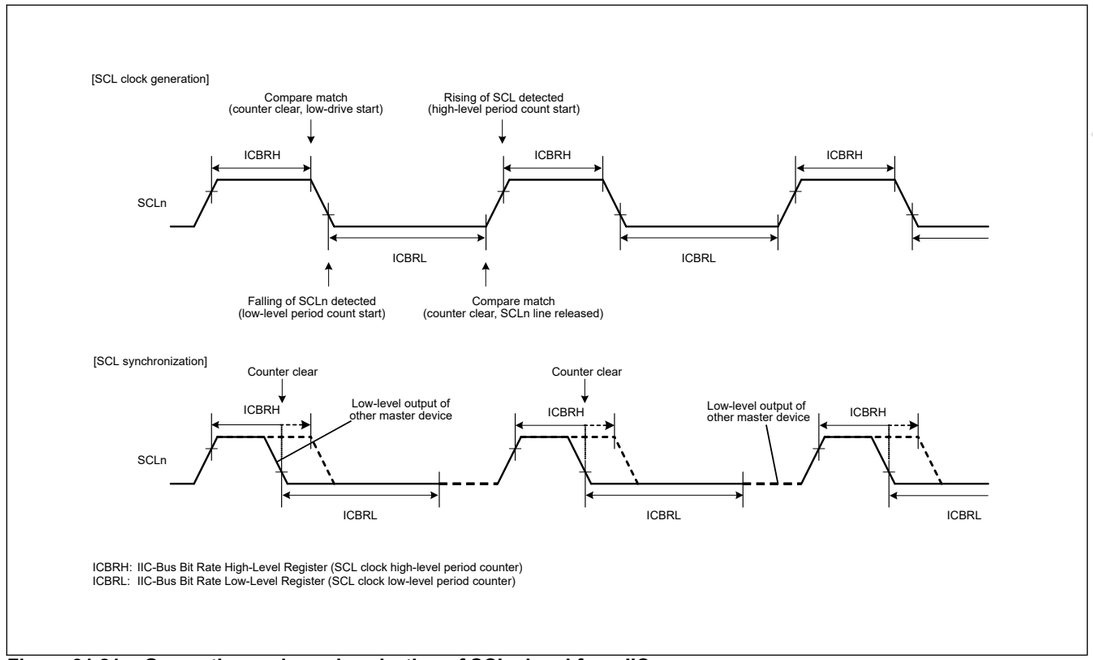


Figure 31.21 Generation and synchronization of SCL signal from IIC

31.5 SDA Output Delay Function

The IIC module incorporates a function for delaying output on the SDA line. The delay can be applied to all output on the SDA line, including issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals.

完成计数后，驱动SCLn线，释放线。IIC重复此过程以生成SCL时钟。

如果多个主设备连接到I2C总线，由于与另一个主设备争用，可能会出现SCL信号冲突。在这种情况下，主设备必须同步它们的SCL信号。因为SCL信号的这种同步必须是逐位的，所以IIC配备了一个SCL同步电路，通过在主机模式下监视SCLn线来获得SCL时钟信号的逐位同步。

当IIC检测到SCLn线上的上升沿并开始计数指定的高电平周期时
ICBRH.BRH[4:0]，并且SCLn线上的电平下降，因为另一个主设备正在生成SCL信号，IIC执行以下操作：

1.检测到下降沿停止计数。

2.将SCLn线上的电平拉低。

3.开始计算ICBRL.BRL[4:0]中指定的低电平周期。

当IIC完成对低电平周期的计数时，它停止将SCLn线驱动为低电平以释放该线。如果来自其他主设备的SCL时钟信号的低电平周期长于IIC中设置的低电平周期，则延长SCL信号的低电平周期。当另一个主设备的低电平周期结束时，SCL信号上升，因为SCLn线被释放。

当IIC输出完SCL时钟的低电平周期后，SCLn线被释放，SCL时钟上升。
即当来自多个主控的SCL信号竞争时，SCL信号的高电平周期与周期较窄的时钟同步，SCL信号的低电平周期与主控的低电平周期同步。具有更广泛周期的时钟。但是，只有当ICFER中的SCLE位设置为1时，才会启用SCL信号的这种同步。

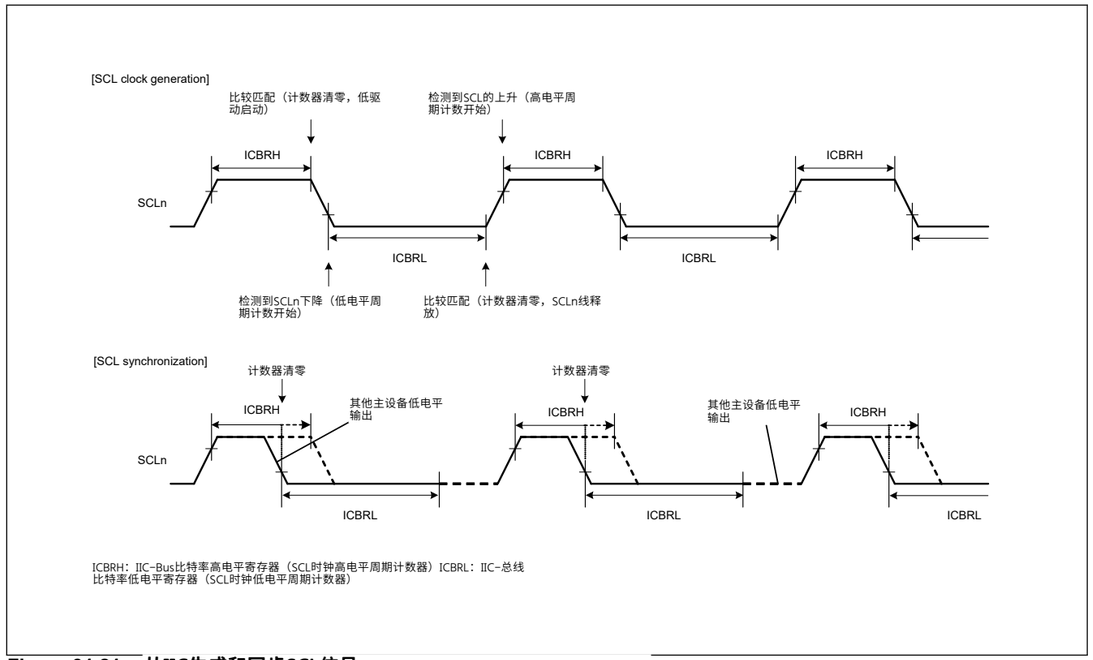


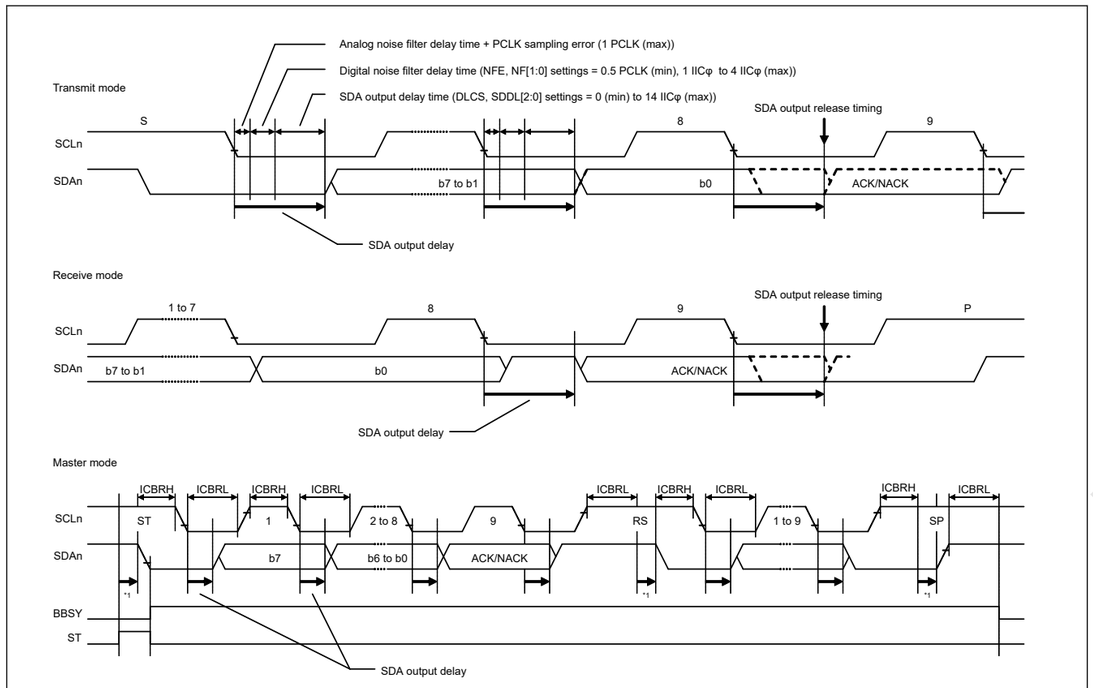
Figure 31.21 从IIC生成和同步SCL信号

31.5 SDA输出延迟功能

IIC模块包含延迟SDA线上输出的功能。延迟可以应用于所有输出SDA线，包括发出启动、重新启动和停止条件、数据以及ACK和NACK信号。

With this function, SDA output is delayed from the detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval during which the SCL clock is low. This approach helps prevent erroneous operation of communications devices, with the aim of satisfying the 300-ns minimum data-hold time requirement of the SMBus specification. The output delay function is enabled by setting the SDDL[2:0] bits in ICMR2 to a value other than 000b, and disabled by setting the same bits to 000b.

When the SDA output delay function is enabled, for example, the DLCS bit in ICMR2 selects the clock source for the SDA output delay counter, either as the internal base clock (IICφ) for the IIC module or as the internal base clock divided by 2 (IICφ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. When the delay cycles count is reached, the IIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.



Note: PCLK = PCLKB
Note 1. The output delay function is set by the DLCS and SDDL[2:0] bits when a start (ST), restart (RS), or stop (SP) condition is issued.

Figure 31.22 SDA output delay function

31.6 Digital Noise Filter Circuits

The internal circuitry sees the states of the SCLn and SDAn pins through analog and digital noise-filter circuits. Figure 31.23 shows a block diagram of the digital noise-filter circuit.

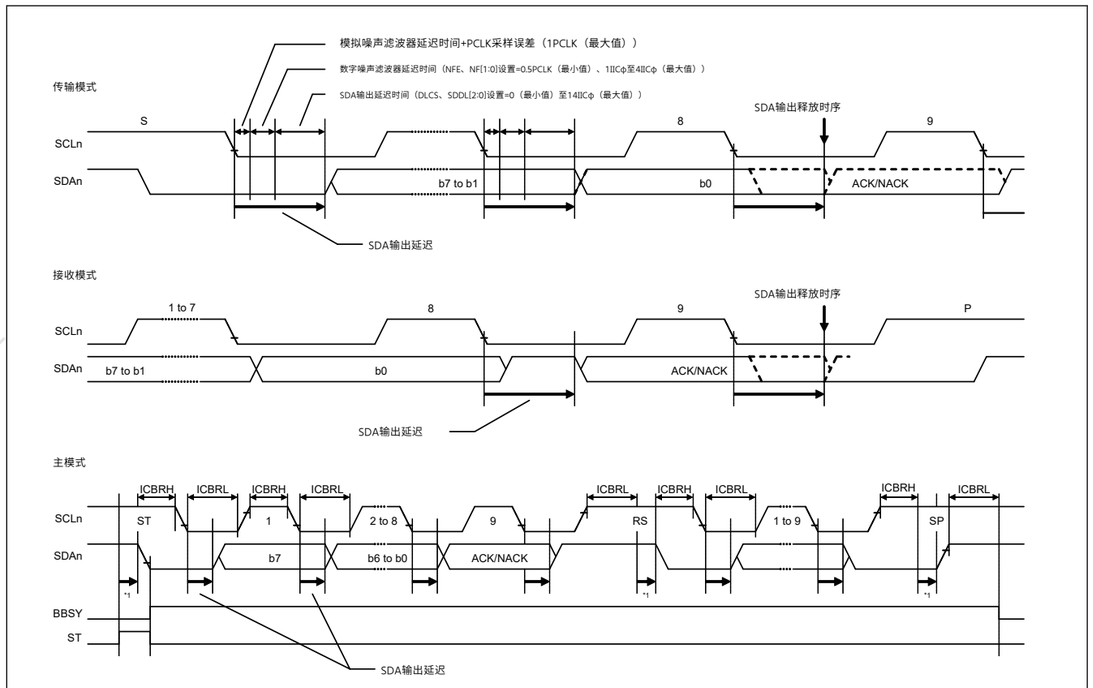
The on-chip digital noise-filter circuit of the IIC consists of four flip-flop circuit stages connected in series and a match-detection circuit. The number of valid stages in the digital noise filter is selected in the NF[1:0] bits in ICMR3. The selected number of valid stages determines the noise-filtering capability as a period from 1 to 4 IICφ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICφ signal. When the input signal level matches the output level of the number of valid flip-flop circuit stages as selected in the NF[1:0] bits in ICMR3, the signal level is seen in the the subsequent stage. If the signal levels do not match, the previous value is saved.

If the ratio between the frequency of the internal operating clock (PCLKB) and the transfer rate is small, for example, if data transfer is 400 kbps with PCLKB = 4 MHz, the characteristics of the digital noise filter might lead to the elimination of

使用此功能，SDA输出从检测到SCL信号的下降沿开始延迟，以确保在SCL时钟为低电平的时间间隔内输出SDA信号。这种方法有助于防止通信设备的错误操作，旨在满足SMBus规范的300ns最小数据保持时间要求。通过将ICMR2中的SDDL[2:0]位设置为000b以外的值来启用输出延迟功能，通过将相同位设置为000b来禁用输出延迟功能。

例如，当SDA输出延迟功能使能时，ICMR2中的DLCS位选择SDA输出延迟计数器的时钟源，或者作为IIC模块的内部基准时钟(IICφ)，或者作为内部基准时钟除以2(IICφ2)。计数器计算ICMR2中SDDL[2:0]位中设置的周期数。当达到延迟周期计数时，IIC模块将所需的输出（启动、重启或停止条件、数据或ACK或NACK信号）放在SDA线上。



Note: PCLK = PCLKB
注1.当发出启动(ST)、重启(RS)或停止(SP)条件时，输出延迟功能由DLCS和SDDL[2:0]位设置。

Figure 31.22 SDA输出延迟功能

31.6 数字噪声滤波器电路

内部电路通过模拟和数字噪声滤波器电路查看SCLn和SDAn引脚的状态。图31.23显示了数字噪声滤波器电路的框图。

IIC的片上数字噪声滤波器电路由四个串联的触发器电路级和一个匹配检测电路组成。数字噪声滤波器的有效级数在ICMR3的NF[1:0]位中选择。选定的有效级数决定了噪声过滤能力，周期为1到4个IICφ周期。

SCLn引脚（或SDAn引脚）的输入信号在IICφ信号的下降沿采样。当输入信号电平与在ICMR3的NF[1:0]位中选择的有效触发器电路级数的输出电平相匹配时，将在后续级中看到信号电平。如果信号电平不匹配，则保存先前的值。

如果内部工作时钟(PCLKB)的频率与传输速率之间的比率很小，例如，如果数据传输为400kbps，PCLKB=4MHz，则数字噪声滤波器的特性可能会导致消除

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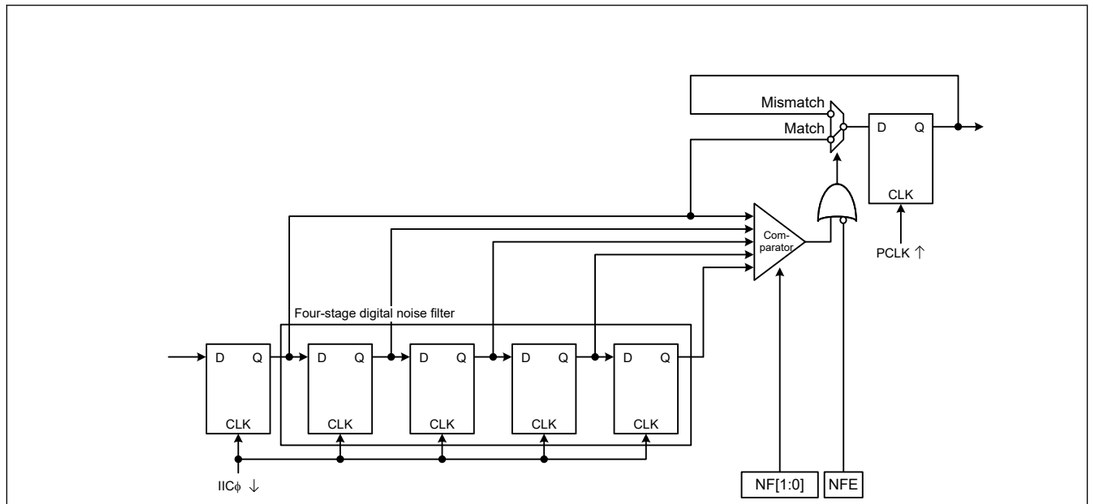
required signals as noise. In such cases, it is possible to disable the digital noise-filter circuit by setting the ICFER.NFE bit to 0, and use only the analog noise filter circuit.



Note: PCLK = PCLKB

Figure 31.23 Digital noise filter circuit block diagram

31.7 Address Match Detection

The IIC can set three unique slave addresses in addition to the general call address and host address. The slave addresses can be 7-bit or 10-bit slave addresses.

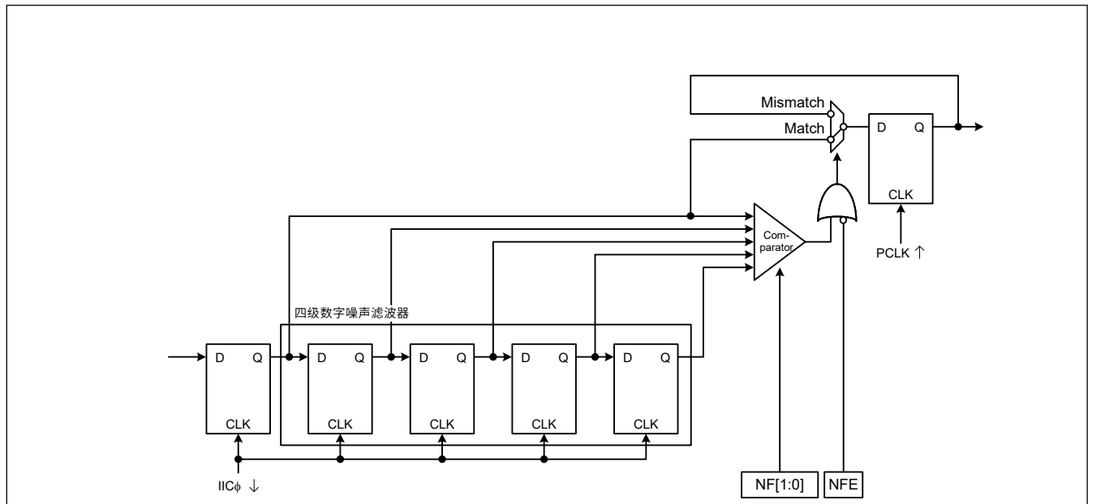
31.7.1 Slave-Address Match Detection

The IIC can set three unique slave addresses and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the IIC detects a match of the set slave address, the associated AASy flag (y = 0 to 2) in ICSR1 is set to 1 on the rising edge of the ninth SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the subsequent R/W# bit. This causes a receive data full interrupt (IICn_RXI) or transmit data empty interrupt (IICn_TXI) to be generated. The AASy flag identifies which slave address is specified.

Figure 31.24 to Figure 31.26 show the AASy flag set timing in three cases.

所需的信号作为噪声。在这种情况下，可以通过将ICFER.NFE位设置为0来禁用数字噪声滤波器电路，并仅使用模拟噪声滤波器电路。



Note: PCLK = PCLKB

Figure 31.23 数字噪声滤波器电路框图

31.7 地址匹配检测

IIC除了广播地址和主机地址外，还可以设置三个唯一的从机地址。从地址可以是7位或10位从地址。

31.7.1 从地址匹配检测

IIC可以设置三个唯一的从机地址，并对每个唯一的从机地址具有从机地址检测功能。当ICSER中的SARyE位（y=0到2）设置为1时，可以检测到设置在SARUy和SARLy（y=0到2）中的从机地址。

当IIC检测到与设置的从地址匹配时，ICSR1中相关的AASy标志（y=0到2）在第9个SCL时钟周期的上升沿设置为1，并且ICSR2中的RDRF标志或TDRE标志ICSR2中的1由随后的RW#位设置为1。这会导致产生接收数据满中断（IICn_RXI）或发送数据空中断（IICn_TXI）。AASy标志标识指定了哪个从地址。

图31.24至图31.26显示了三种情况下的AASy标志设置时序。

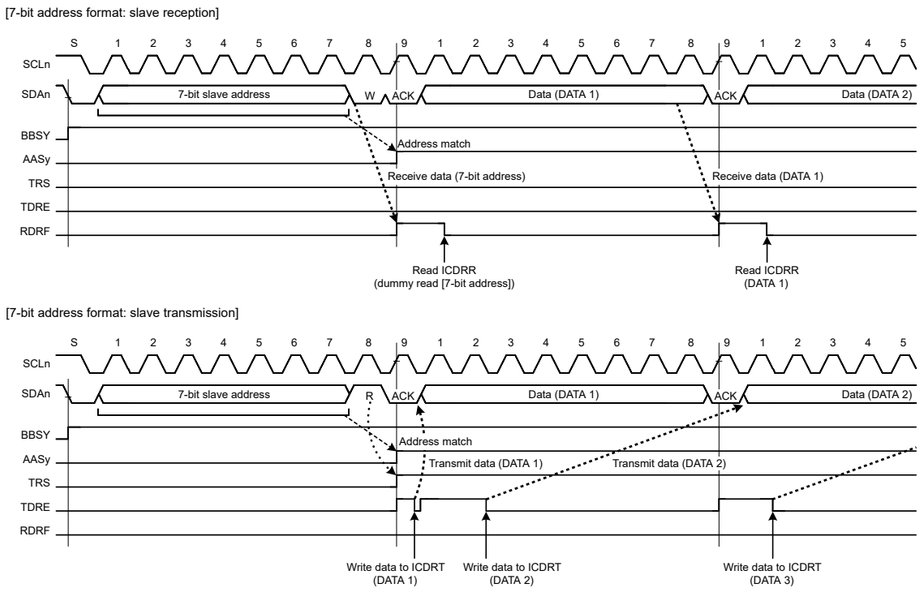


Figure 31.24 AASy flag set timing with 7-bit address format

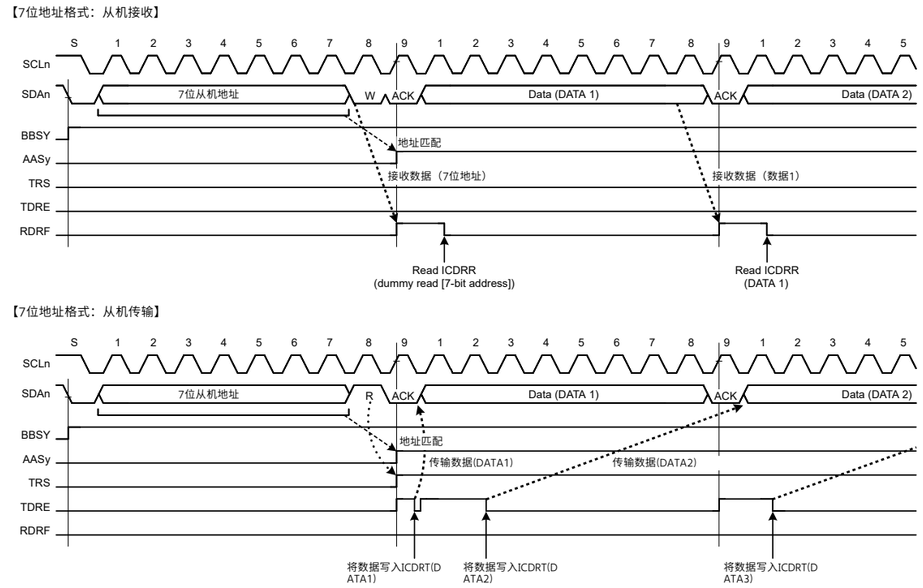


Figure 31.24 7位地址格式的AASy标志设置时序

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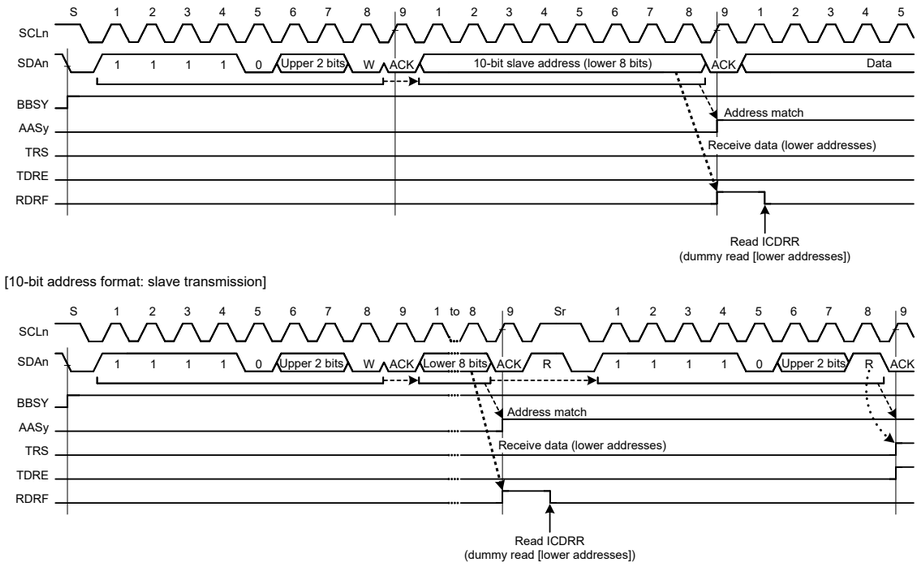

Figure 31.25 AASy flag set timing with 10-bit address format

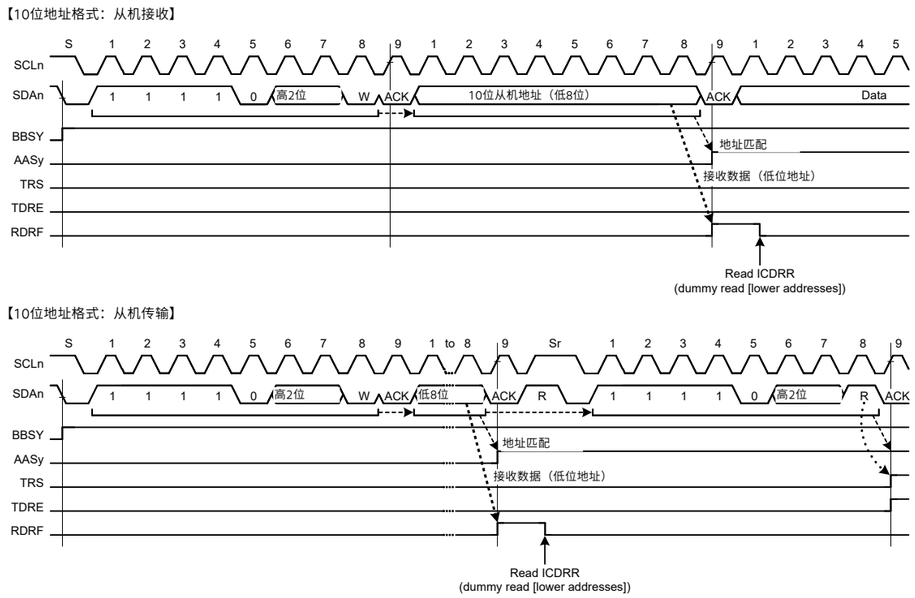

Figure 31.25 10位地址格式的AASy标志设置时序

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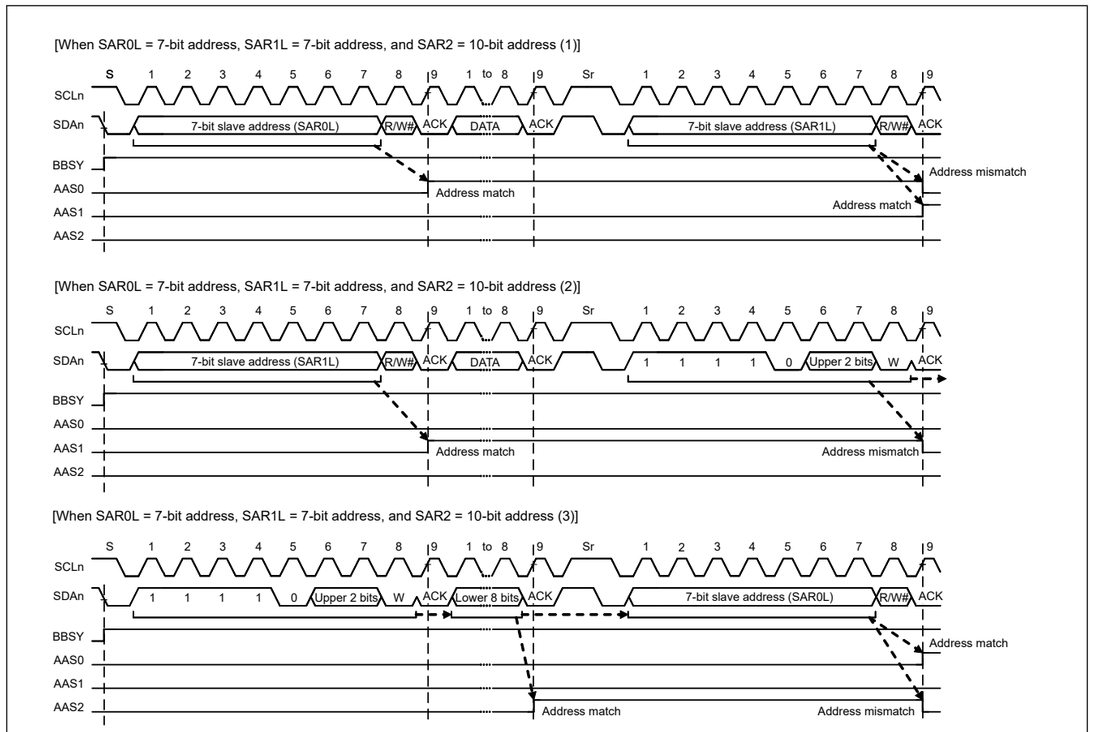


Figure 31.26 AASy flag set and clear timing with mixed 7-bit and 10-bit address formats

31.7.2 Detection of General Call Address

The IIC provides detection of the general call address (0000 000b + 0 [W]). This is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the IIC recognizes this as the address of a slave device with an all-zero address, but not as the general call address.

When the IIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 set to 1 on the rising edge of the ninth cycle of the SCL clock. This leads to the generation of a receive data full interrupt (IICn_RXI). The value of the GCA flag can be checked to confirm that the general call address was transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

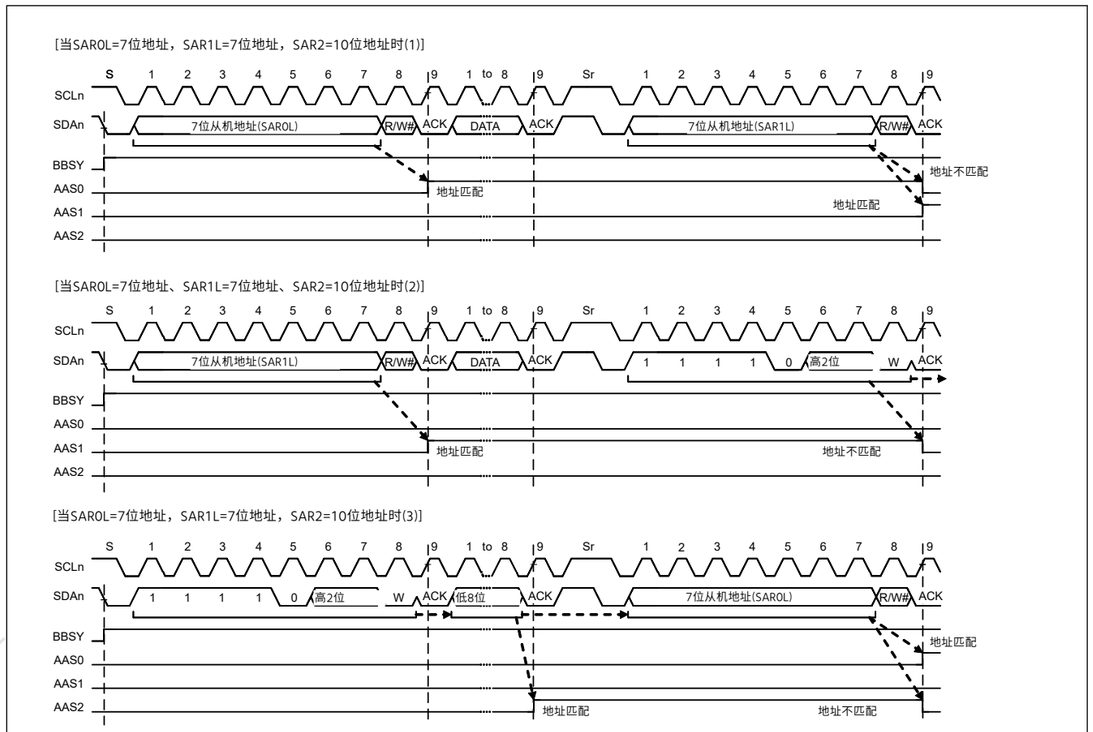


Figure 31.26 混合7位和10位地址格式的AASy标志设置和清除时序

31.7.2 广播呼叫地址检测

IIC提供对广播呼叫地址(0000000b+0[W])的检测。这是通过设置GCAE位启用
ICSER to 1.

如果在发出启动或重新启动条件后接收到的地址是0000000b+1[R]（起始字节），则IIC将其识别为具有全零地址的从设备的地址，但不是广播地址.

当IIC检测到广播呼叫地址时，ICSR1中的GCA标志和ICSR2中的RDRF标志都在SCL时钟的第9个周期的上升沿设置为1。这会导致接收数据完全中断(IICn_RXI)的产生。可以检查GCA标志的值以确认广播呼叫地址已被传输。

检测到广播呼叫地址后的操作与正常的从机接收操作相同。

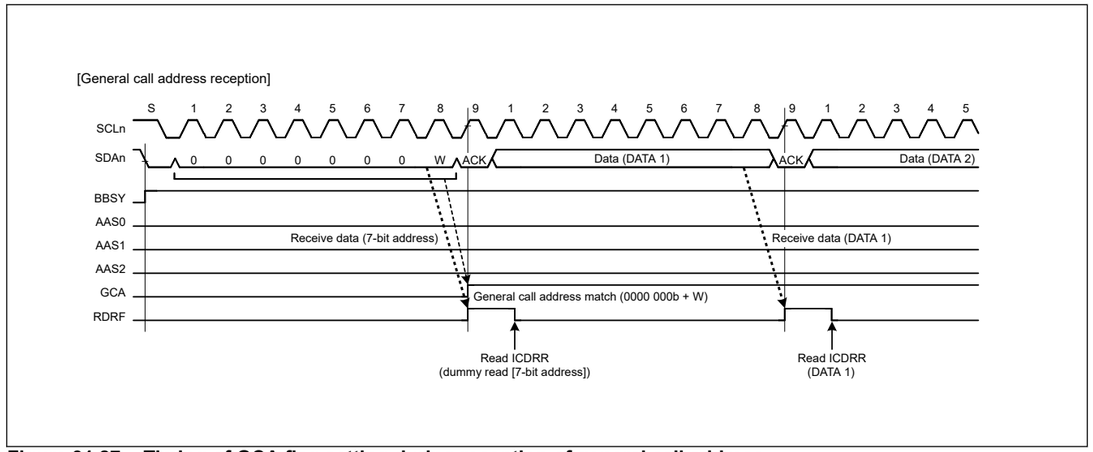


Figure 31.27 Timing of GCA flag setting during reception of general call address

31.7.3 Device-ID Address Detection

The IIC module provides detection of device-ID address compliant with the I^2C bus specification (revision 03). When the IIC receives 1111 100b as the first byte after a start or restart condition is issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the ninth SCL clock cycle when the subsequent R/W# bit is 0, then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the IIC sets the associated AASy flag (y = 0 to 2) in ICSR1 to 1.

When the first byte received after the issue of a start or restart condition matches the device ID address (1111 100b) again and the subsequent R/W# bit is 1, the IIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device ID address detection function, the IIC sets the DID flag to 0 if a match with the IIC slave address is not obtained or a match with the device ID address is not obtained after a match with the IIC slave address and a restart condition is not detected. If the first byte after detection of a start or restart condition matches the device ID address (1111 100b), and the R/W# bit is 0, the IIC sets the DID flag to 1 and compares the second and subsequent bytes with the slave address of the IIC. If the R/W# bit is 1, the DID flag holds the previous value and the IIC does not compare the second and subsequent bytes. Therefore, the reception of a device ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Additionally, prepare the device ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal transmit data. For details on the information that must be included in device ID fields, contact NXP Semiconductors.

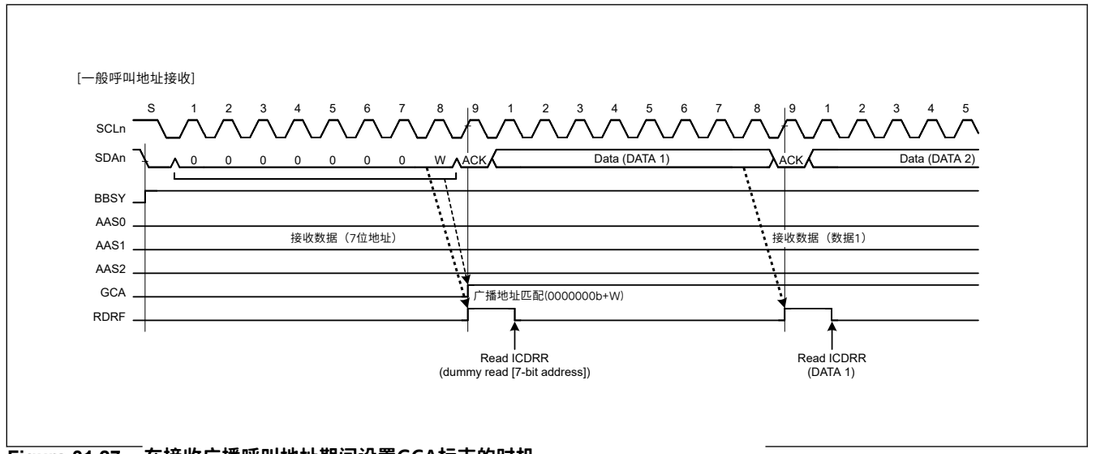


Figure 31.27 在接收广播呼叫地址期间设置GCA标志的时机

31.7.3 设备ID地址检测

IIC模块提供符合I2C总线规范（修订版03）的设备ID地址检测。当。。。的时候

IIC在ICSER中的DIDE位设置为1的情况下，在发出启动或重启条件后接收1111100b作为第一个字节，它将地址识别为设备ID，在第9个上升沿将ICSR1中的DID标志设置为1当后续的RW#位为0时，SCL时钟周期，然后将第二个和后续字节与其自己的从地址进行比较。如果地址与从地址寄存器中的值匹配，则IIC将ICSR1中相关的AASy标志（y=0到2）设置为1。

当发出启动或重启条件后接收到的第一个字节再次与设备ID地址(1111100b)匹配且后续RW#位为1时，IIC不比较第二个和后续字节并设置ICSR2.TDRE标志为1。

在设备ID地址检测功能中，如果没有获得与IIC从机地址匹配或在与IIC从机地址匹配和重启条件后未获得与设备ID地址匹配，则IIC将DID标志设置为0未检测到。如果检测到启动或重启条件后的第一个字节与设备ID地址(1111100b)匹配，并且RW#位为0，则IIC将DID标志设置为1，并将第二个和后续字节与从机地址进行比较IIC。如果RW#位为1，则DID标志保持前一个值，并且IIC不比较第二个和后续字节。因此，在确认TDRE=1后，可以通过读取DID标志来检查设备ID地址的接收。

此外，准备设备ID字段（3个字节：12位表示制造商+9位表示部件+3位表示版本）在接收到连续的设备ID字段作为正常发送数据后必须发送到主机。有关必须包含在设备ID字段中的信息的详细信息，请联系NXPSemiconductors。

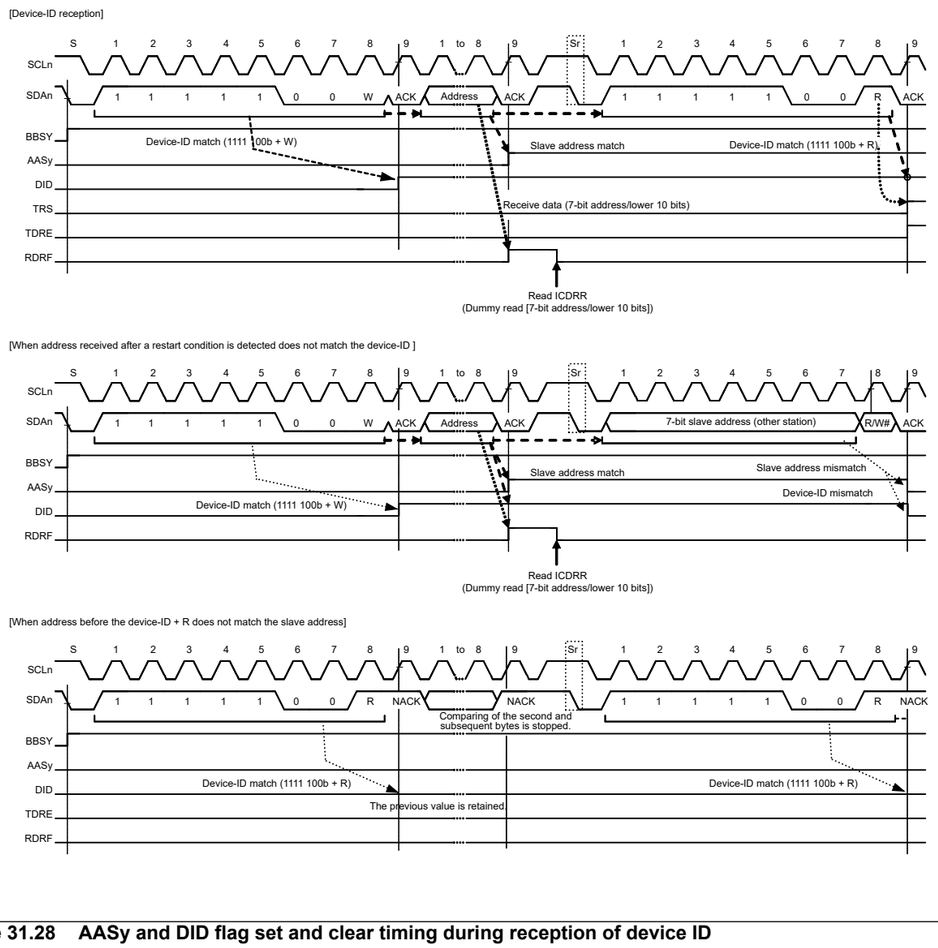


Figure 31.28 AASy and DID flag set and clear timing during reception of device ID

31.7.4 Host Address Detection

The IIC provides host address detection when operating in SMBus. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the IIC can detect the host address (0001 000b) in slave receive mode (MST and TRS bits = 00b in ICCR2).

When the IIC detects the host address, the HOA flag in ICSR1 is set to 1 on the rising edge of the 9th SCL clock cycle, and at the same time, the RDRF flag in ICSR2 is set to 1 when the R/W# bit is 0 (Wr bit). This causes a receive data full interrupt (IICn_RXI) to be generated. The HOA flag indicates that the host address was sent from another device.

If the bit following the host address (0001 000b) is an Rd bit (R/W# bit = 1), the IIC can also detect the host address. After the host address is detected, the IIC operates in the same manner as in normal slave operation.

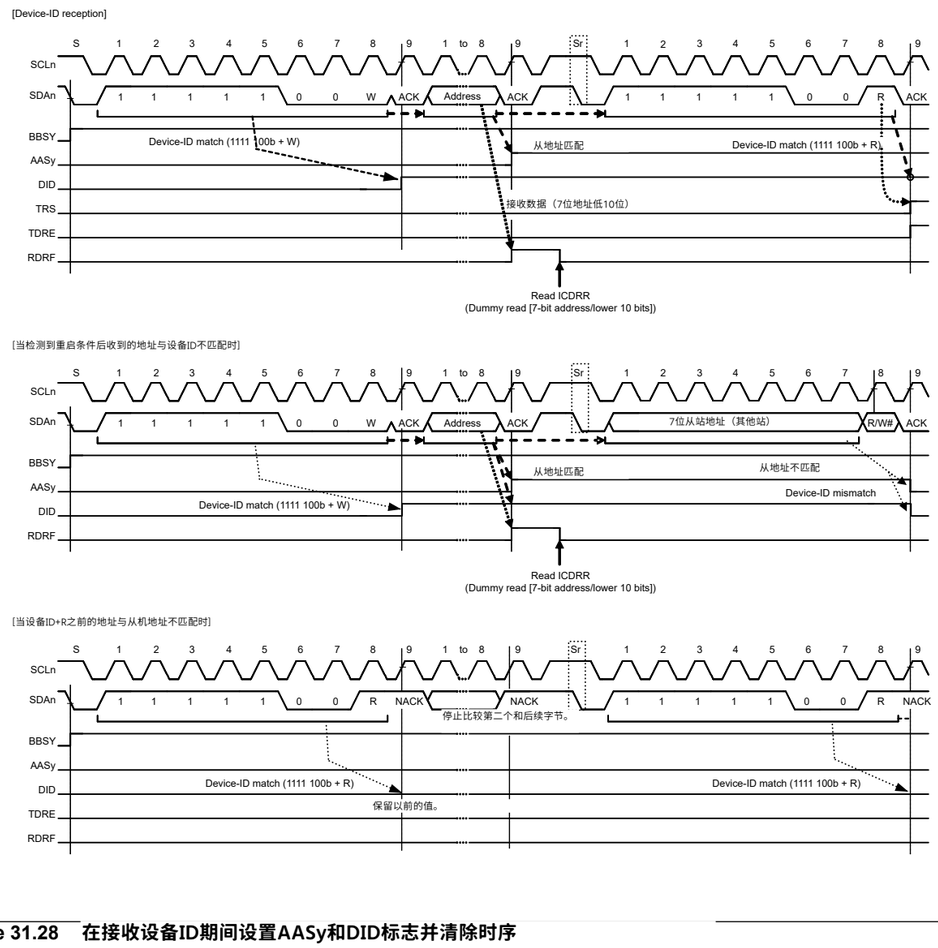


Figure 31.28 在接收设备ID期间设置AASy和DID标志并清除时序

31.7.4 主机地址检测

IIC在SMBus中运行时提供主机地址检测。当ICSER中的HOAE位设置为1而ICMR3中的SMBS位为1，IIC可以在从机接收模式下检测主机地址（0001000b）（ICCR2中的MST和TRS位=00b）。

当IIC检测到主机地址时，ICSR1中的HOA标志在第9个SCL时钟周期的上升沿置1，同时ICSR2中的RDRF标志在RW#位为0时置1（写位）。这会导致产生接收数据完全中断（IICn_RXI）。HOA标志表明主机地址是从另一个设备发送的。

如果主机地址（0001000b）后面的位是Rd位（RW#位=1），则IIC也可以检测主机地址。检测到主机地址后，IIC以与正常从机操作相同的方式运行。

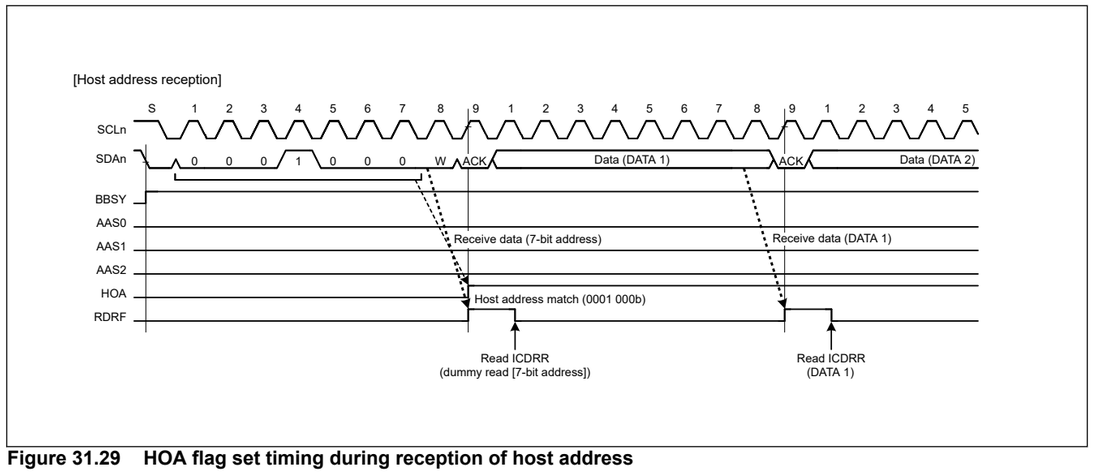


Figure 31.29 HOA flag set timing during reception of host address

31.8 Wakeup Function

The IIC provides a wakeup function that causes the MCU to transition from Software Standby mode or Snooze mode to normal operation. The wakeup function enables the reception of data when the system clock (PCLKB) is stopped, and generates a wakeup interrupt signal on a match of the slave address of the received data. This wakeup interrupt signal triggers the return to normal operation. After the wakeup interrupt occurs, switch the IIC to PCLKB synchronous operation so that communication can continue.

The wakeup function has four operation modes:

- Normal wakeup mode 1
- Normal wakeup mode 2
- Command recovery mode
- EEP response mode

Table 31.9 describes the behavior in these modes.

Table 31.9 Wakeup operation modes

Operation mode	ACK response timing	ACK response before wakeup to PCLKB synchronous operation	SCL state during wakeup to PCLKB synchronous operation
Normal wakeup mode 1	Before wakeup to PCLKB synchronous operation*1	ACK	Fixed low
Normal wakeup mode 2	After wakeup to PCLKB synchronous operation*2	Before wakeup: no response (NACK level retained) After wakeup: ACK response	Fixed low
Command recovery mode	Before wakeup to PCLKB synchronous operation*1	ACK	Open
EEP response mode	Before recovery to PCLKB synchronous operation*1	NACK	Open

Note 1. Switching timing from PCLKB asynchronous operation to PCLKB synchronous operation is the falling edge of the 9th clock of the SCL.
Note 2. Switching timing from PCLKB asynchronous operation to PCLKB synchronous operation is the falling edge of the 8th clock of the SCL.

The following can be selected as wakeup interrupt sources:

- Host address detection (valid when ICSER.HOAE = 1)
- General call address detection (valid when ICSER.GCAE = 1)
- Slave address 0*1 detection (valid when ICSER.SAR0E = 1)

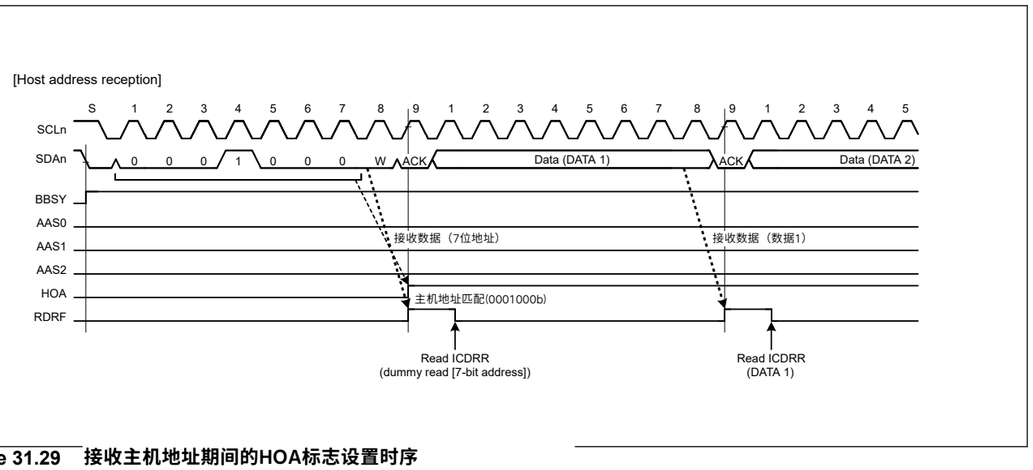


Figure 31.29 接收主机地址期间的HOA标志设置时序

31.8 唤醒功能

IIC提供唤醒功能，使MCU从软件待机模式或贪睡模式转换到正常操作。唤醒功能在系统时钟（PCLKB）停止时启用数据接收，并在接收到的数据的从地址匹配时产生唤醒中断信号。该唤醒中断信号触发恢复正常操作。唤醒中断发生后，将IIC切换为PCLKB同步操作，以便继续通信。

唤醒功能有四种操作模式：

- ●正常唤醒模式1
- ●正常唤醒模式2
- ●命令恢复模式
- ●EEP响应方式

表31.9描述了这些模式下的行为。

Table 31.9 唤醒操作模式

操作模式	ACK响应时间	唤醒前的ACK响应到PCLKB同步操作	唤醒到PCLKB同步操作期间的SCL状态
正常唤醒模式1	唤醒到PCLKB同步操作之前*1	ACK	固定低
正常唤醒模式2	唤醒到PCLKB同步操作后*2	唤醒前：无响应（保留NACK电平） 唤醒后：ACK响应	固定低
命令恢复模式	唤醒到PCLKB同步操作之前*1	ACK	Open
EEP响应模式	恢复到PCLKB同步操作之前*1	NACK	Open

注1.从PCLKB异步操作切换到PCLKB同步操作的时序是第9个时钟的下降沿SCL.
注2.从PCLKB异步操作切换到PCLKB同步操作的时序是第8个时钟的下降沿SCL.

可以选择以下作为唤醒中断源：

- ●主机地址检测（当ICSER.HOAE=1时有效）
- ●广播地址检测（ICSER.GCAE=1时有效）
- ●从机地址0*1检测（在ICSER.SAR0E=1时有效）

- Slave address 1*1 detection (valid when ICSER.SAR1E = 1)
- Slave address 2*1 detection (valid when ICSER.SAR2E = 1)

Note 1. Only 7-bit address can be set. Set the FS bit in SARUy (y = 0 to 2) to 0.

Precautions on the use of the wakeup function

- Do not change the content of the IIC registers except the WUSEN bit in ICWUR2 while the WUASYF flag in ICWUR2 is 1 (during PCLKB asynchronous operation).
- Set ICWUR.WUE and ICWUR.WUIE to 1, and ICCR2.MST and ICCR2.TRS to 0 (slave reception mode) before switching to PCLKB asynchronous mode.
- The device ID and the 10-bit slave address cannot be selected for the wakeup interrupt source. Set the DIDE bit in ICSER and FS bit in SARUy (y = 0 to 2) to 0.
- Set bits TIE, TEIE, RIE, NAKIE, SPIE, STIE, ALIE, and TMOIE in the ICIER register to 0 (interrupt disabled) before switching to the asynchronous operation.
- When the wakeup function is enabled, do not use the timeout function (ICWUR.WUE = 1)
- Even when a wakeup interrupt is generated during PCLKB asynchronous operation (when ICWUR2.WUASYF = 1), if the slave addresses match in PCLKB synchronous mode (ICWUR2.WUASYF = 0), the wakeup interrupt does not occur and the WUF flag is not set.
- If the timing of writing 0 to the ICWUR2.WUSEN bit and the timing of detecting a start condition conflict, the IIC might start the next reception in PCLKB synchronous operation mode. In this case, ICWUR2.WUASYF flag becomes 1 (switch to PCLKB asynchronous mode) when data communication is complete, a stop condition is detected, and detection of a wakeup event starts.
- After writing 0 to the WUSEN bit in ICWUR2, do not change registers relate to the IIC operation mode setting (ICMR3, ICSER, and SARLy) until the mode is switched to PCLKB asynchronous operation from PCLKB synchronous operation (while the ICWUR2.WUASYF flag is 1). If the register value changes during this period by an interrupt handling or another factor, the IIC might malfunction before switching to the asynchronous operation.

31.8.1 Normal Wakeup Mode 1

This section describes the behavior, the timing, and an example operation of normal wakeup mode 1.

In normal wakeup mode 1, a wakeup interrupt triggered by the match of the slave address initiates the transition to normal operation as follows:

Before wakeup:	ACK is sent in response to the data received with its own slave address of the IIC.
During wakeup:	ACK response is made on the 9th clock cycle of SCL, after which SCL is held low*1.
After wakeup:	Normal operation continues.

Note 1. Between the 9th clock cycle and 1st clock cycle during wakeup, WAIT = 1 is invalid.

If the slave address does not match, the SCL line is not held low after the 9th clock cycle of SCL, and the slave operation continues. Figure 31.30 shows an operation example, and Figure 31.32 shows the detailed timing.

If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, for example the IRQn, the WUF flag is not set to 1. Figure 31.31 shows an operation example.

●从机地址1*1检测（当ICSER.SAR1E=1时有效）

●从机地址2*1检测（当ICSER.SAR2E=1时有效）

注1.只能设置7位地址。将SARUy（y=0到2）中的FS位设置为0。

唤醒功能使用注意事项

●当ICWUR2的WUASYF标志为1时（PCLKB异步操作期间），不要改变ICWUR2中除WUSEN位以外的IIC寄存器的内容。

●在切换到PCLKB异步模式之前，将ICWUR.WUE和ICWUR.WUIE设置为1，并将ICCR2.MST和ICCR2.TRS设置为0（从接收模式）。

●唤醒中断源不能选择设备ID和10位从机地址。将ICSER中的DIDE位和SARUy（y=0到2）中的FS位设置为0。

●在切换到异步操作之前，将ICIER寄存器中的TIE、TEIE、RIE、NAKIE、SPIE、STIE、ALIE和TMOIE位设置为0（禁止中断）。

●启用唤醒功能时，不要使用超时功能（ICWUR.WUE=1）

●即使在PCLKB异步操作期间（ICWUR2.WUASYF=1）产生唤醒中断，如果在PCLKB同步模式下从机地址匹配（ICWUR2.WUASYF=0），唤醒中断不会发生并且WUF标志不放。

●如果向ICWUR2.WUSEN位写入0的时序与检测启动条件的时序冲突，则IIC可能会在PCLKB同步操作模式下开始下一次接收。在这种情况下，当数据通信完成时，ICWUR2.WUASYF标志变为1（切换到PCLKB异步模式），检测到停止条件，并开始检测唤醒事件。

●在ICWUR2的WUSEN位写入0后，不要更改与IIC操作模式设置相关的寄存器（ICMR3、ICSER和SARLy），直到模式从PCLKB同步操作切换到PCLKB异步操作（同时ICWUR2.WUASYF标志是1）。如果在此期间寄存器值因中断处理或其他因素而发生变化，则IIC可能会在切换到异步操作之前发生故障。

31.8.1 正常唤醒模式1

本节介绍正常唤醒模式1的行为、时序和示例操作。

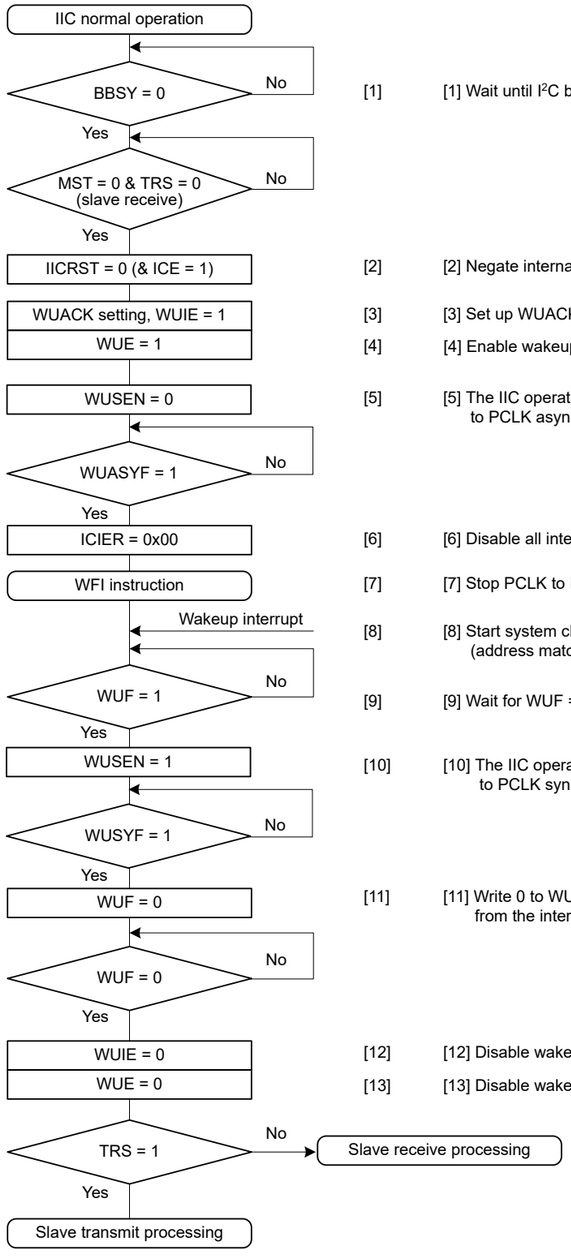
在正常唤醒模式1中，由匹配从机地址触发的唤醒中断启动到正常操作的转换，如下所示：

Before wakeup:	ACK是响应接收到的带有IIC从机地址的数据而发送的。
During wakeup:	在SCL的第9个时钟周期做出ACK响应，之后SCL保持低电平*1。
After wakeup:	正常操作继续。

注1.在唤醒期间的第9个时钟周期和第1个时钟周期之间，WAIT=1无效。

如果从机地址不匹配，则SCL线在SCL的第9个时钟周期后不保持低电平，从机操作继续。图31.30显示了一个操作示例，图31.32显示了详细的时序。

如果从软件待机模式或贪睡模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。图31.31显示了一个操作示例。



[1] [1] Wait until I²C bus is open and stay in standby state.

[2] [2] Negate internal reset (if asserted).

[3] [3] Set up WUACK for the desired wakeup mode. Enable wakeup interrupt.

[4] [4] Enable wakeup function.

[5] [5] The IIC operating state is changed from PCLK synchronous to PCLK asynchronous.

[6] [6] Disable all interrupt requests except WUI.

[7] [7] Stop PCLK to IIC. IIC continues to receive.

[8] [8] Start system clock and PCLK supply to IIC on wakeup interrupt (address match).

[9] [9] Wait for WUF = 1.

[10] [10] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.

[11] [11] Write 0 to WUF. Read and check that WUF = 0 before returning from the interrupt handling.

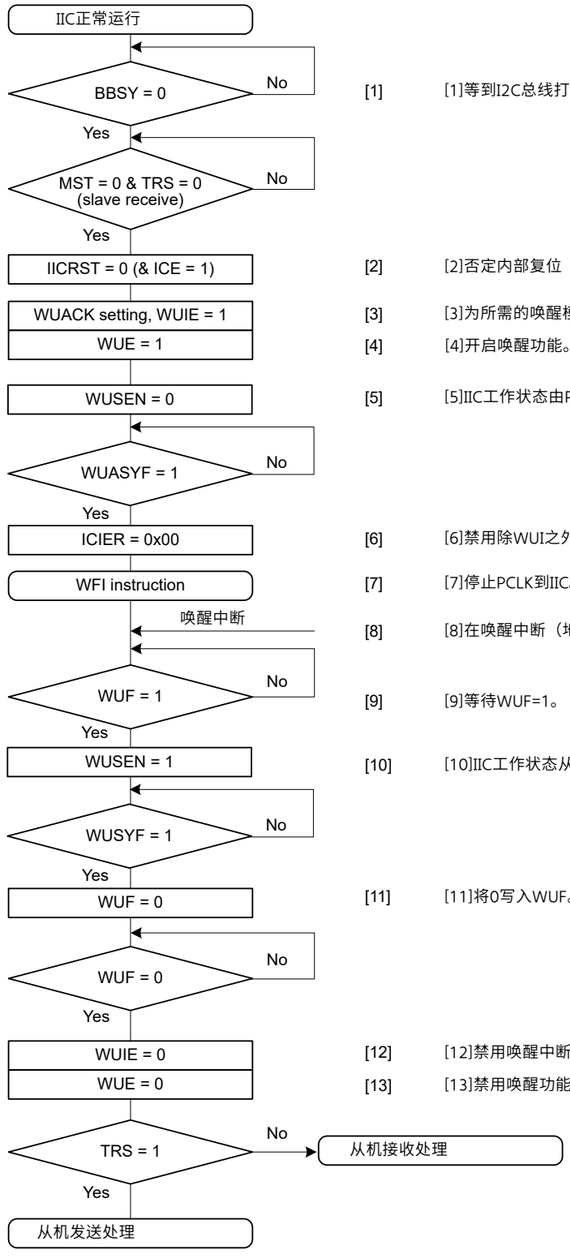
[12] [12] Disable wakeup Interrupt.

[13] [13] Disable wakeup function.

Note: PCLK = PCLKB

Figure 31.30 Example operation of normal wakeup mode 1 when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



[1] [1]等到I2C总线打开并保持待机状态。

[2] [2]否定内部复位（如果已断言）。

[3] [3]为所需的唤醒模式设置WUACK。启用唤醒中断。

[4] [4]开启唤醒功能。

[5] [5]IIC工作状态由PCLK同步变为PCLK异步。

[6] [6]禁用除WUI之外的所有中断请求。

[7] [7]停止PCLK到IIC。IIC继续接收。

[8] [8]在唤醒中断（地址匹配）时启动系统时钟和向IIC提供PCLK。

[9] [9]等待WUF=1。

[10] [10]IIC工作状态从PCLK异步变为PCLK同步。

[11] [11]将0写入WUF。在从中断处理返回之前读取并检查WUF=0。

[12] [12]禁用唤醒中断。

[13] [13]禁用唤醒功能。

Note: PCLK = PCLKB

Figure 31.30 正常唤醒模式1的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

Note: 请参阅唤醒功能使用注意事项。

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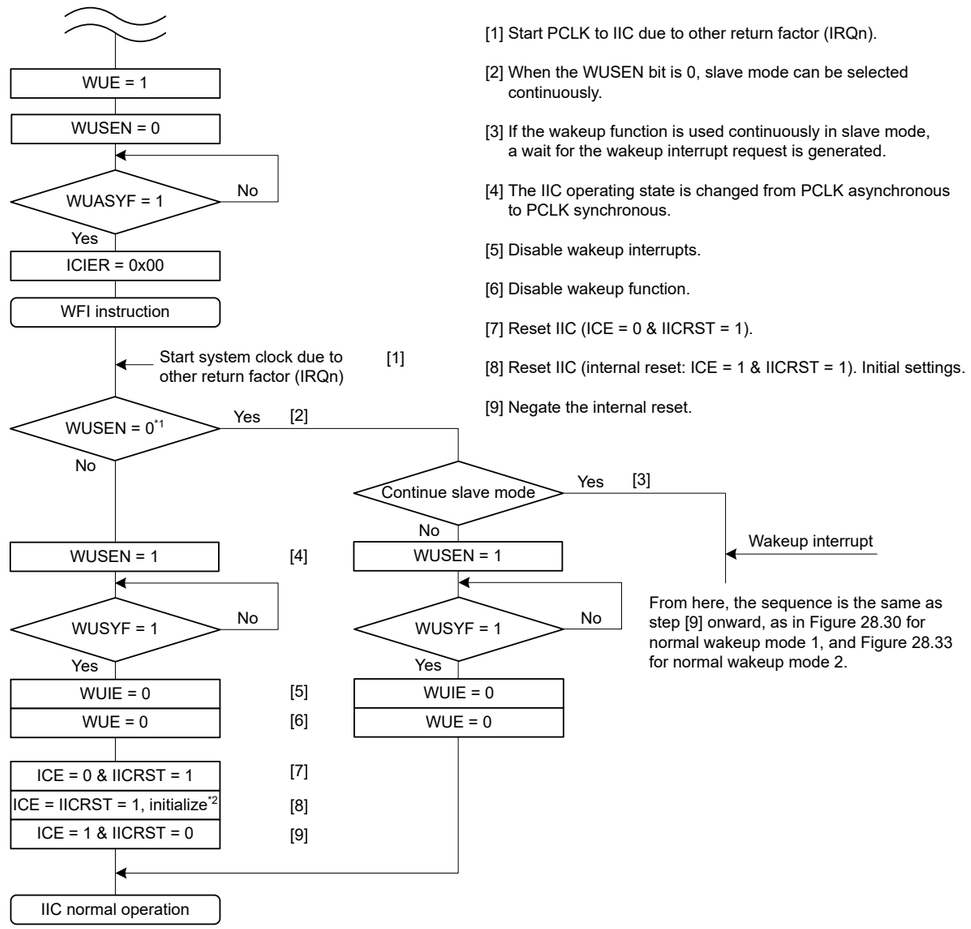


[1] Start PCLK to IIC due to other return factor (IRQn).

[2] When the WUSEN bit is 0, slave mode can be selected continuously.

[3] If the wakeup function is used continuously in slave mode, a wait for the wakeup interrupt request is generated.

[4] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.

[5] Disable wakeup interrupts.

[6] Disable wakeup function.

[7] Reset IIC (ICE = 0 & IICRST = 1).

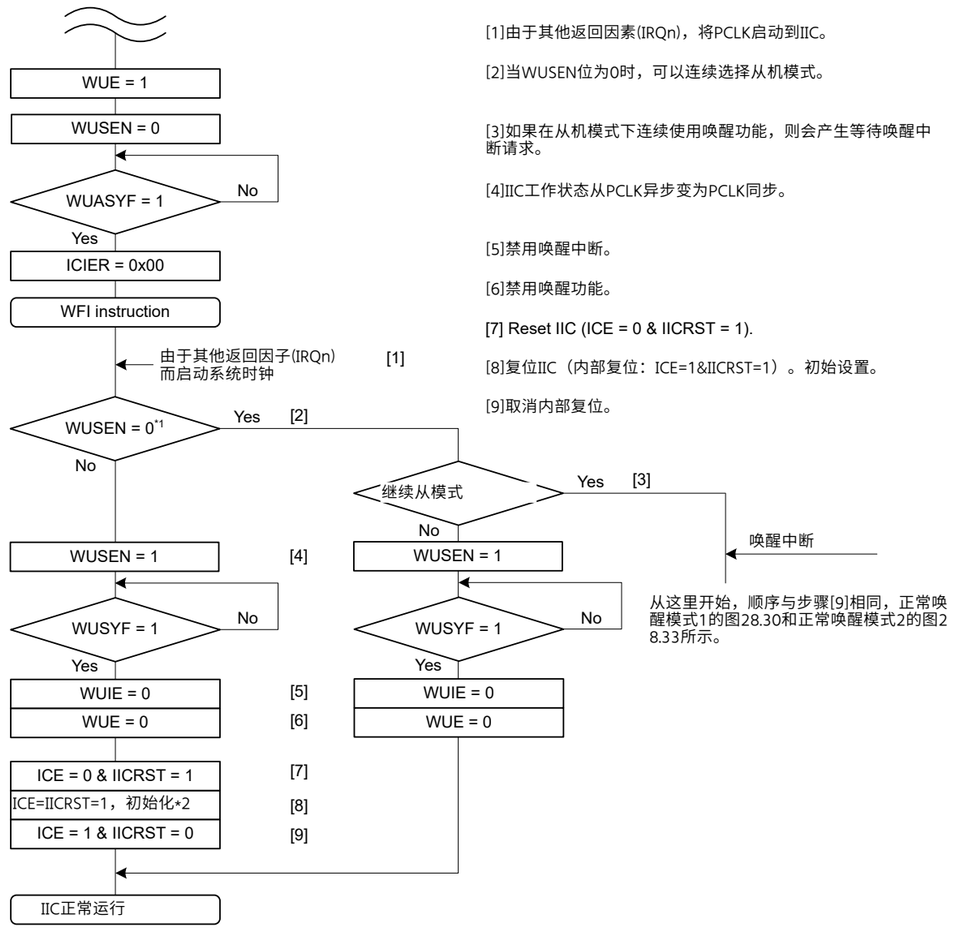
[8] Reset IIC (internal reset: ICE = 1 & IICRST = 1). Initial settings.

[9] Negate the internal reset.

Note: PCLK = PCLKB
Note 1. In the MCU, WUSEN bit is always 0 in the IIC.
Note 2. For details on the IIC initial settings, see section 31.3.2. Initial Settings.

Figure 31.31 Example operation of normal wakeup modes 1 and 2 when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, the IRQn

Note: For details on the IIC initial settings, see section 31.3.2. Initial Settings.



[1]由于其他返回因素(IRQn)，将PCLK启动到IIC。

[2]当WUSEN位为0时，可以连续选择从机模式。

[3]如果在从机模式下连续使用唤醒功能，则会产生等待唤醒中断请求。

[4]IIC工作状态从PCLK异步变为PCLK同步。

[5]禁用唤醒中断。

[6]禁用唤醒功能。

[7] Reset IIC (ICE = 0 & IICRST = 1).

[8]复位IIC（内部复位：ICE=1&IICRST=1）。初始设置。

[9]取消内部复位。

Note: PCLK = PCLKB
注1.在MCU中，IIC中的WUSEN位始终为0。
注2.IIC初始设置的详细信息，请参阅第31.3.2节。初始设置。

Figure 31.31 当唤醒由IIC唤醒中断以外的中断（例如IRQn）触发时，正常唤醒模式1和2的示例操作

Note: 有关IIC初始设置的详细信息，请参阅第31.3.2节。初始设置。

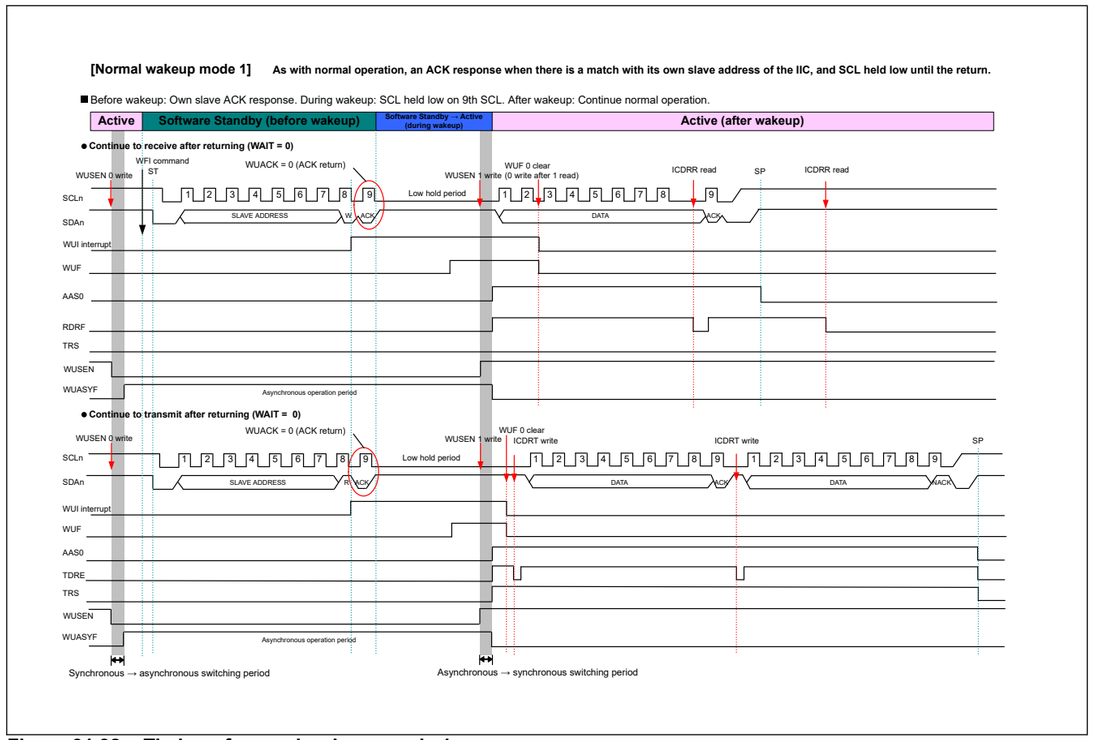


Figure 31.32 Timing of normal wakeup mode 1

31.8.2 Normal Wakeup Mode 2

This section describes the behavior, the timing, and an example operation of normal wakeup mode 2.

In normal wakeup mode 2, a wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows:

Before wakeup:	No response to data received with its own slave address until the end of the 8th SCL cycle.
During wakeup:	SCL line held low during the 8th and 9th clock cycles.
After wakeup:	ACK returns on the 9th clock cycle of SCL, and normal operation continues.

If the slave address does not match, the SCL line is not held low after the 8 th SCL clock cycle, and the slave operation continues. Figure 31.33 shows an example operation, and Figure 31.34 shows the detailed timing.

If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, such as the IRQn, for example, the WUF flag is not set to 1. Figure 31.31 shows an operation example.

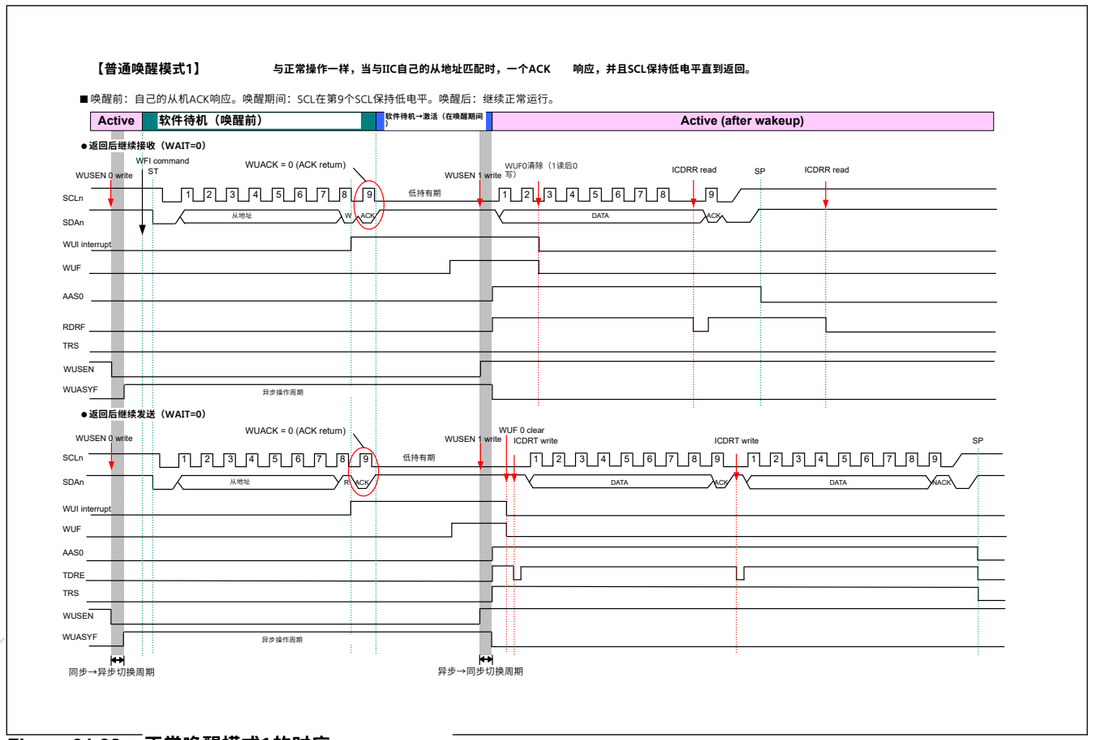


Figure 31.32 正常唤醒模式1的时序

31.8.2 正常唤醒模式2

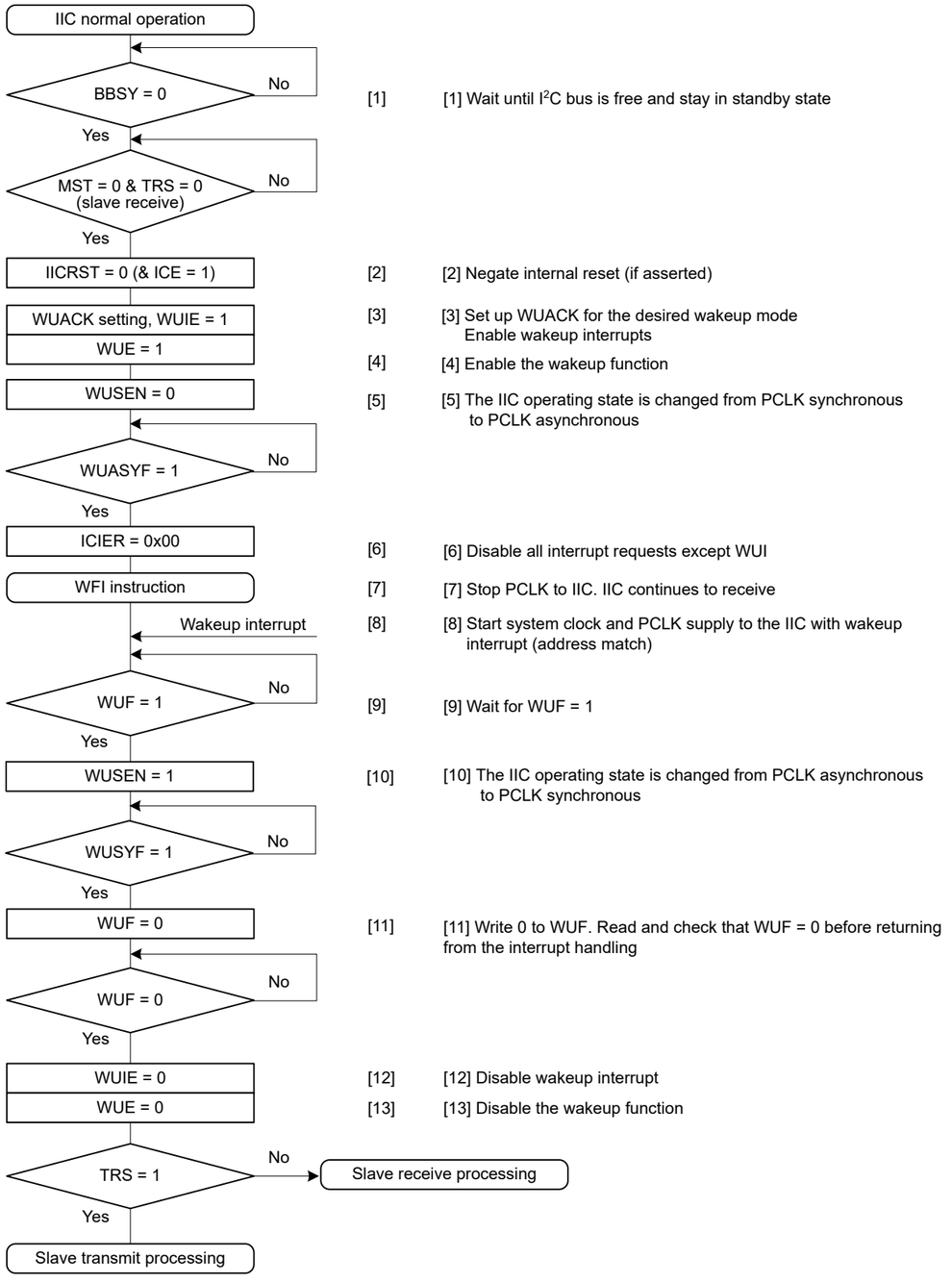
本节介绍正常唤醒模式2的行为、时序和示例操作。

在正常唤醒模式2中，由匹配从机地址触发的唤醒中断会启动到正常操作的转换，如下所示：

Before wakeup:	直到第8个SCL周期结束，才对接收到的带有自己的从地址的数据作出响应。
During wakeup:	SCL线在第8和第9个时钟周期内保持低电平。
After wakeup:	ACK在SCL的第9个时钟周期返回，并继续正常操作。

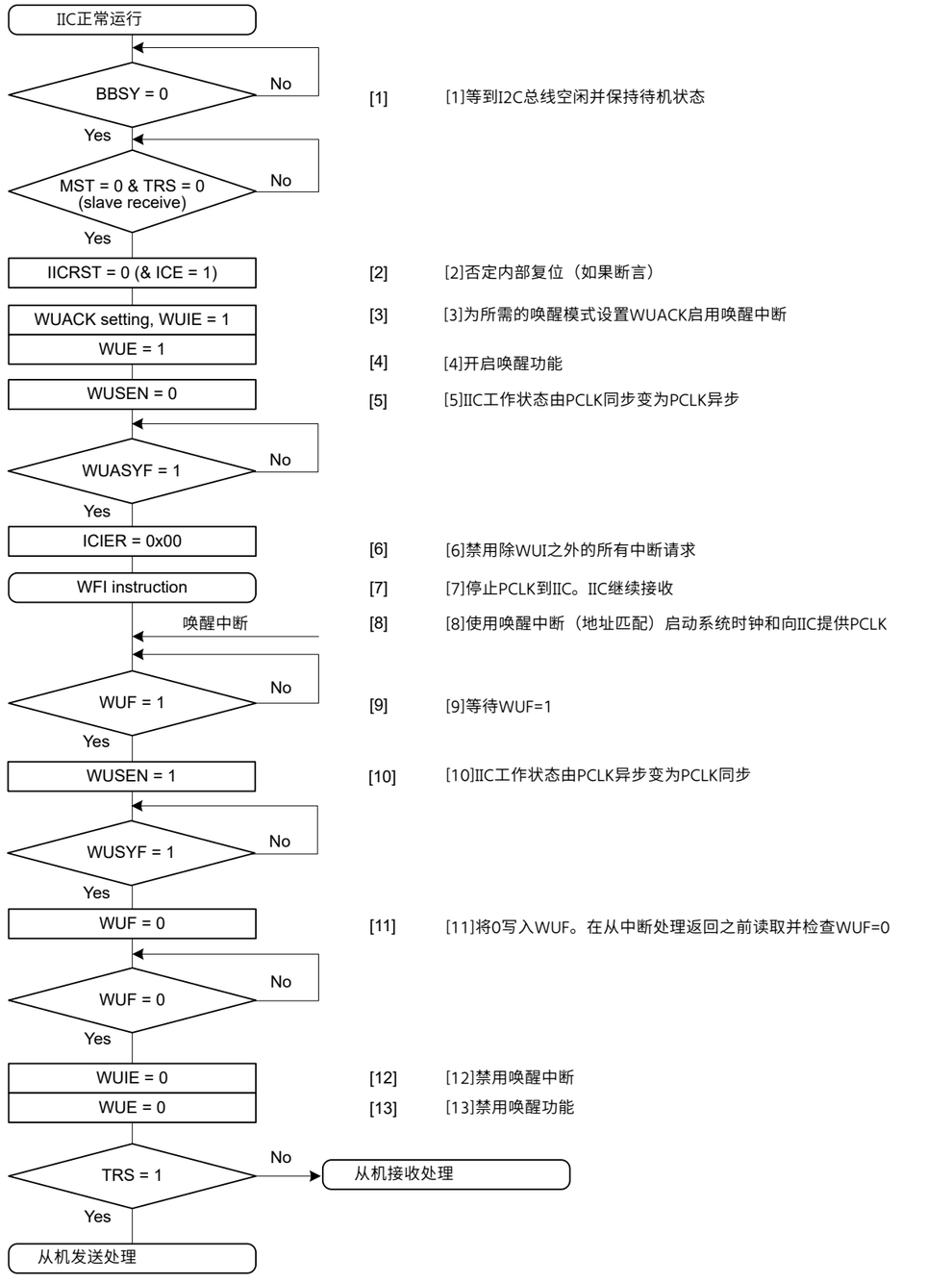
如果从机地址不匹配，则SCL线在第8个SCL时钟周期后不会保持低电平，从机操作继续。图31.33显示了一个示例操作，图31.34显示了详细的时序。

如果从软件待机模式或贪睡模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。图31.31显示了一个操作示例。



Note: PCLK = PCLKB

Figure 31.33 Example operation of normal wakeup mode 2 when wakeup is triggered by a wakeup interrupt on match of the slave address



Note: PCLK = PCLKB

Figure 31.33 正常唤醒模式2的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

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Note: See Precautions on the use of the wakeup function.

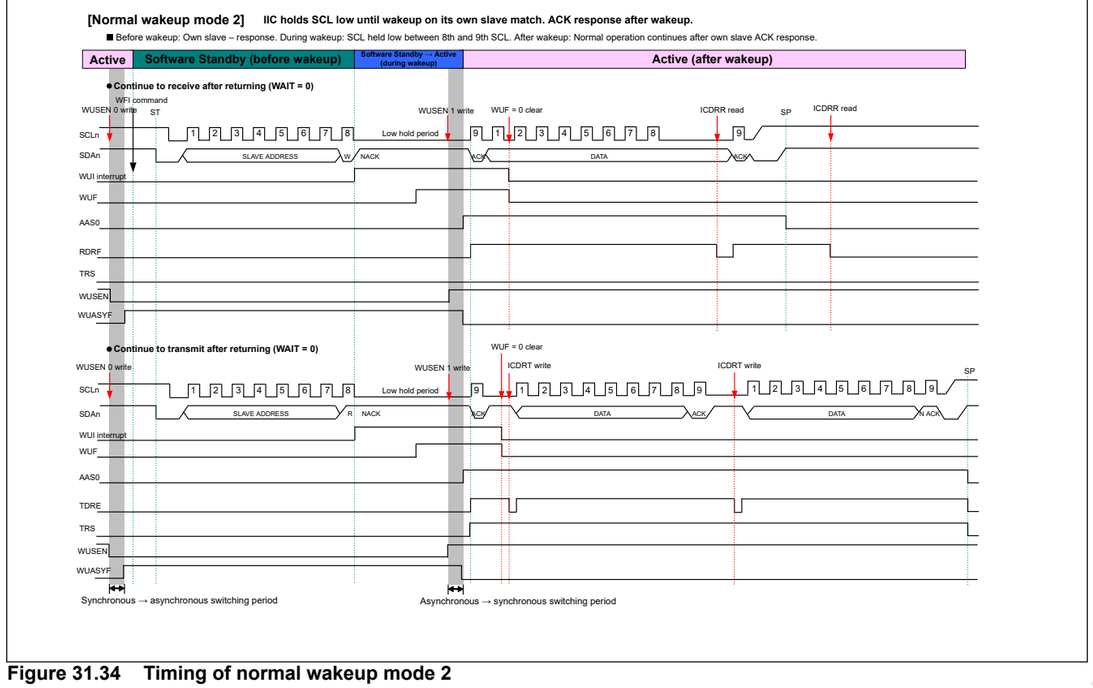


Figure 31.34 Timing of normal wakeup mode 2

31.8.3 Command Recovery Mode and EEP Response Mode (Special Wakeup Modes)

This section describes the behavior, the timing, and example operations of the command recovery and EEP response modes.

In the command recovery and EEP response modes, the SCL line is not held low during the wakeup period (after the rise of the 9th clock cycle of SCL). Therefore, other IIC devices can use the I^2C bus during this period.

A wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows:

Before wakeup:	In response to the data received with its own slave address, the IIC returns ACK (command recovery mode) or NACK (EEP response mode).
During wakeup:	The SCL line is not held low.
After wakeup:	Normal operation continues after IIC initialization.

If the slave address does not match, the slave operation continues.

Note: Because the SCL line is not held low during wakeup, transmission or reception of the data that follows the slave address is not possible.

Note: The command recovery and EEP response modes are internal reset states (ICE = IICRST = 1). Therefore, the match of the slave address does not set the flags, HOA, GCA, ASS0, ASS1, and ASS2 in the ICSR1 register.

Figure 31.35 shows an example operation in recovery and EEP response modes. Figure 31.37 shows the detailed timing.

If the transition from Software Standby mode or Snooze mode is triggered by an interrupt other than a wakeup interrupt, such as IRQn for example, the WUF flag is not set to 1. Follow the processing shown in Figure 31.36.

Note: 请参阅唤醒功能使用注意事项。

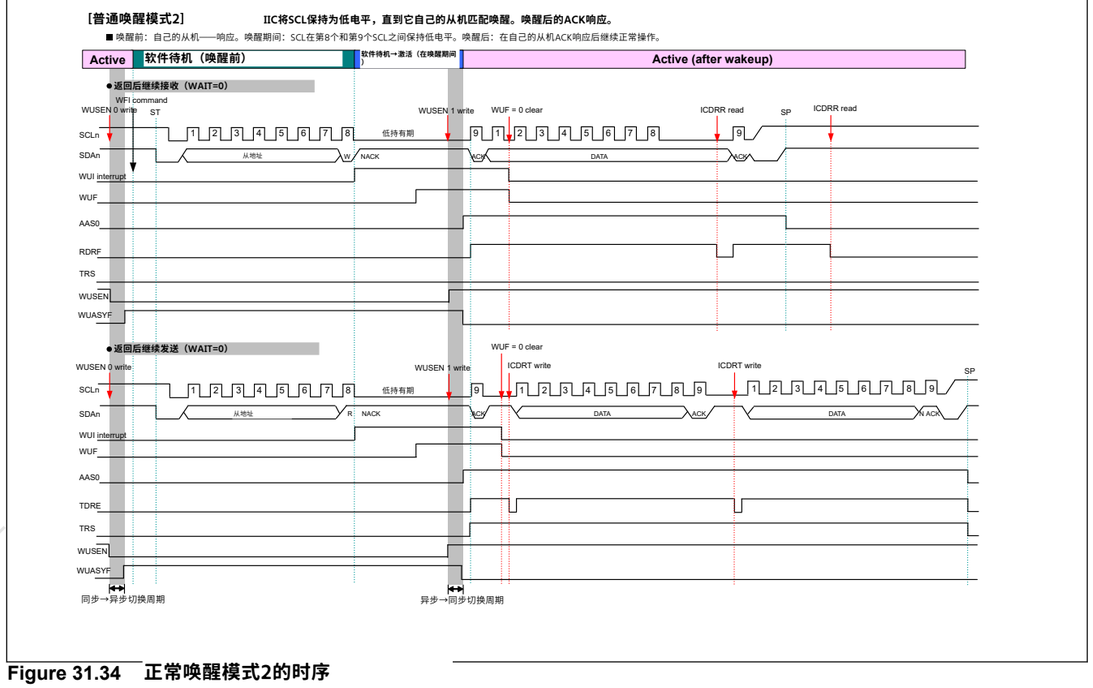


Figure 31.34 正常唤醒模式2的时序

31.8.3 命令恢复模式和EEP响应模式（特殊唤醒模式）

本节介绍命令恢复和EEP响应模式的行为、时序和示例操作。

在命令恢复和EEP响应模式下，SCL线在唤醒期间（在SCL的第9个时钟周期上升之后）不保持低电平。因此，其他IIC设备在此期间可以使用I2C总线。

由匹配从地址触发的唤醒中断会启动到正常操作的转换，如下所示：

Before wakeup:	IIC响应使用自己的从机地址接收到的数据，返回ACK（命令恢复模式）或NACK（EEP响应模式）。
During wakeup:	SCL线没有保持低电平。
After wakeup:	IIC初始化后继续正常操作。

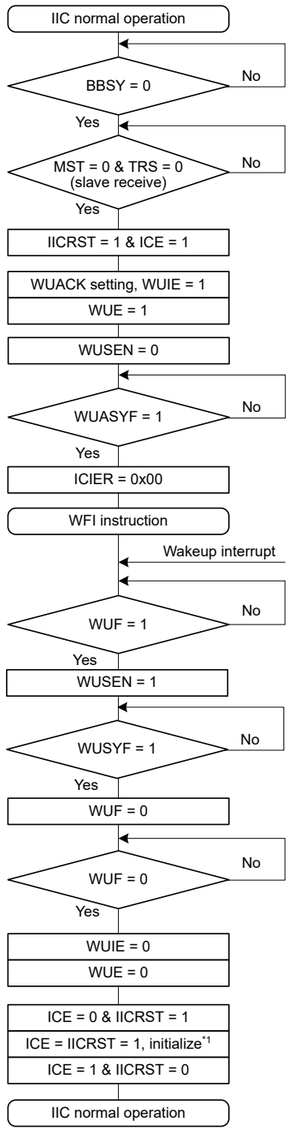
如果从机地址不匹配，从机操作继续。

Note: 因为SCL线在唤醒期间没有保持低电平，所以无法发送或接收跟随从地址的数据。

Note: 命令恢复和EEP响应模式是内部复位状态(ICE=IICRST=1)。因此，从地址的匹配不会设置ICSR1寄存器中的标志位HOA、GCA、ASS0、ASS1和ASS2。

图31.35显示了恢复和EEP响应模式下的示例操作。图31.37显示了详细的时序。

如果从软件待机模式或贪睡模式的转换是由唤醒中断以外的中断触发的，例如IRQn，则WUF标志不设置为1。按照图31.36中所示的处理。



[1] [1] Wait until I^2C bus is open and stay in standby state.

[2] [2] Internal reset is asserted.

[3] [3] Set up WUACK for the desired wakeup mode. Enable wakeup interrupt.

[4] [4] Enable wakeup function.

[5] [5] The IIC operating state is changed from PCLK synchronous to PCLK asynchronous.

[6] [6] Disable all interrupt requests except WUI.

[7] [7] Stop PCLK to IIC. IIC continues to receive.

[8] [8] Start system clock and PCLK supply to the IIC with wakeup interrupt (address match).

[9] [9] Wait for WUF = 1.

[10] [10] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.

[11] [11] Write 0 to WUF. Read and check that WUF = 0 before returning from the interrupt handling.

[12] [12] Disable wakeup interrupt.

[13] [13] Disable wakeup function.

[14] [14] Reset IIC (ICE = 0 & IICRST = 1).

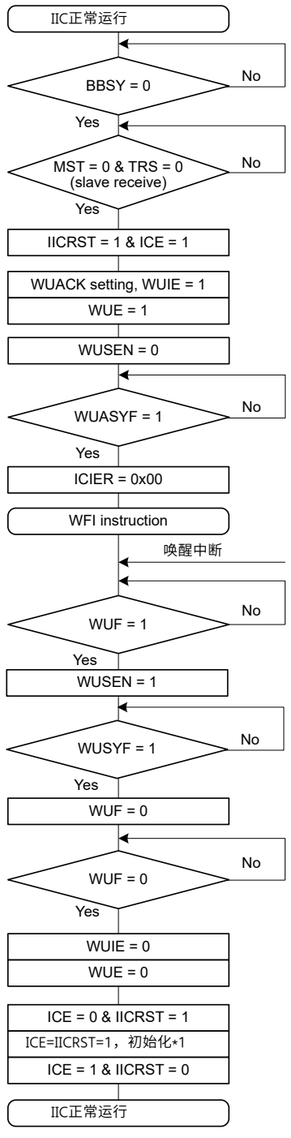
[15] [15] Reset IIC (internal reset: ICE = 1 & IICRST = 1). Initial settings.

[16] [16] Negate the internal reset.

Note: PCLK = PCLKB
Note 1. For details on IIC initialization, see section 31.3.2. Initial Settings.

Figure 31.35 Example operation of command recovery mode and EEP response mode when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



[1] [1]等到I2C总线打开并保持待机状态。

[2] [2]内部复位被断言。

[3] [3]为所需的唤醒模式设置WUACK。启用唤醒中断。

[4] [4]开启唤醒功能。

[5] [5]IIC工作状态由PCLK同步变为PCLK异步。

[6] [6]禁用除WUI之外的所有中断请求。

[7] [7]停止PCLK到IIC。IIC继续接收。

[8] [8]通过唤醒中断（地址匹配）启动向IIC提供系统时钟和PCLK。

[9] [9]等待WUF=1。

[10] [10]IIC工作状态从PCLK异步变为PCLK同步。

[11] [11]将0写入WUF。在从中断处理返回之前读取并检查WUF=0。

[12] [12]禁用唤醒中断。

[13] [13]禁用唤醒功能。

[14] [14] Reset IIC (ICE = 0 & IICRST = 1).

[15] [15]复位IIC（内部复位：ICE=1&IICRST=1）。初始设置。

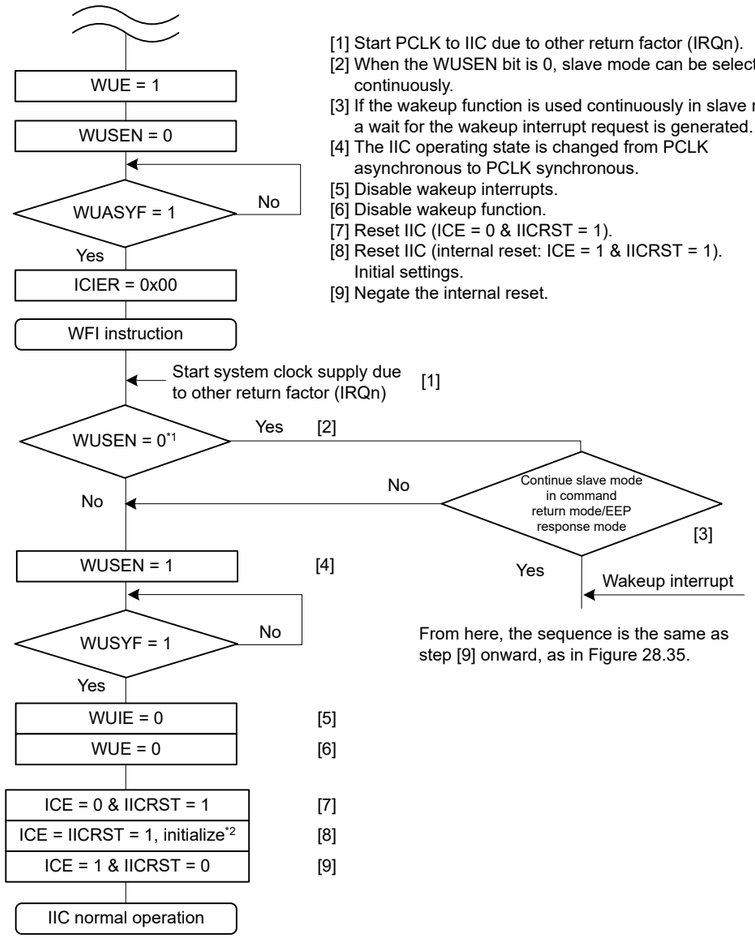
[16] [16]取消内部复位。

Note: PCLK = PCLKB
注1.关于IIC初始化的详细信息，请参阅第31.3.2节。初始设置。

Figure 31.35 从地址匹配时唤醒中断触发唤醒时命令恢复模式和EEP响应模式的示例操作

Note: 请参阅唤醒功能使用注意事项。

RA生态工作室

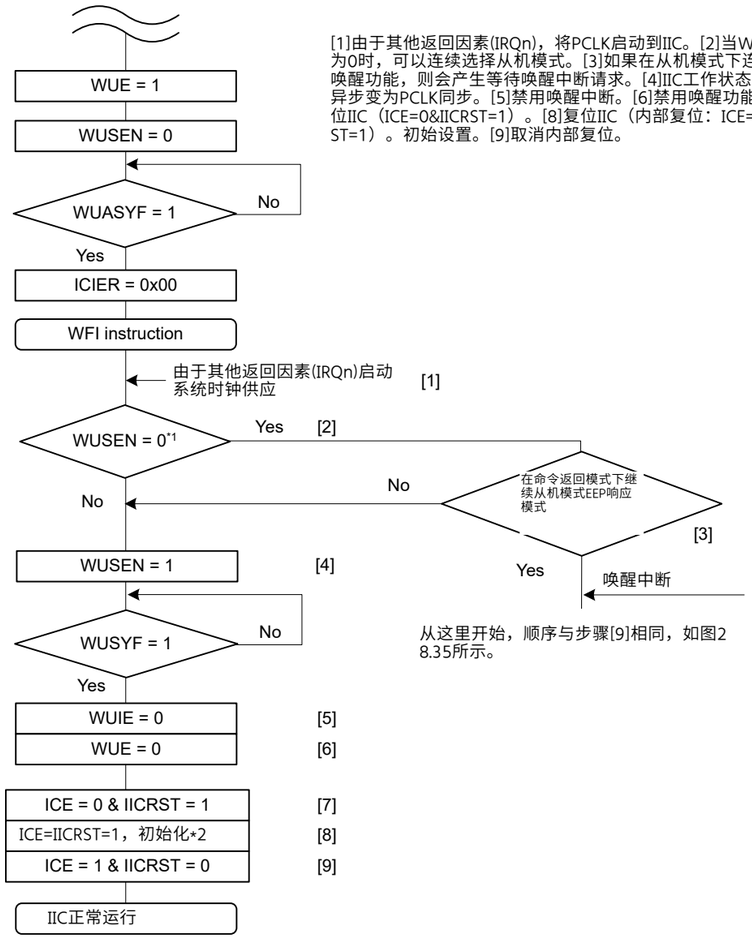


From here, the sequence is the same as step [9] onward, as in Figure 28.35.

[1] Start PCLK to IIC due to other return factor (IRQn).
[2] When the WUSEN bit is 0, slave mode can be selected continuously.
[3] If the wakeup function is used continuously in slave mode, a wait for the wakeup interrupt request is generated.
[4] The IIC operating state is changed from PCLK asynchronous to PCLK synchronous.
[5] Disable wakeup interrupts.
[6] Disable wakeup function.
[7] Reset IIC (ICE = 0 & IICRST = 1).
[8] Reset IIC (internal reset: ICE = 1 & IICRST = 1). Initial settings.
[9] Negate the internal reset.

Note: PCLK = PCLKB
Note 1. In the MCU, WUSEN bit is always 0 in the IIC.
Note 2. For details on IIC initialization, see section 31.3.2. Initial Settings.

Figure 31.36 Example operation of command recovery and EEP response modes when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example, the IRQn



从这里开始，顺序与步骤[9]相同，如图28.35所示。

[1]由于其他返回因素(IRQn)，将PCLK启动到IIC。[2]当WUSEN位为0时，可以连续选择从机模式。[3]如果在从机模式下连续使用唤醒功能，则会产生等待唤醒中断请求。[4]IIC工作状态从PCLK异步变为PCLK同步。[5]禁用唤醒中断。[6]禁用唤醒功能。[7]复位IIC（ICE=0&IICRST=1）。[8]复位IIC（内部复位：ICE=1&IICRST=1）。初始设置。[9]取消内部复位。

Note: PCLK = PCLKB
注1.在MCU中，IIC中的WUSEN位始终为0。
注2.关于IIC初始化的详细信息，请参阅第31.3.2节。初始设置。

Figure 31.36 由IIC唤醒中断以外的中断（例如IRQn）触发唤醒时的命令恢复和EEP响应模式的示例操作

RA生态工作室

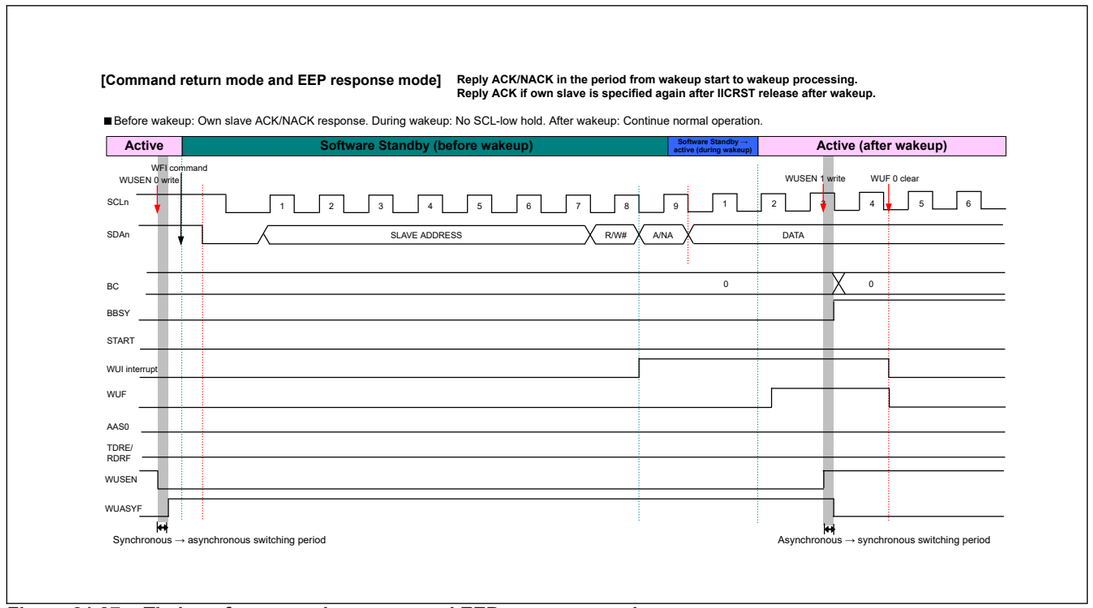


Figure 31.37 Timing of command recovery and EEP response modes

31.9 Automatic Low-Hold Function for SCL

31.9.1 Function to Prevent Wrong Transmission of Transmit Data

If the I²C Bus Shift Register (ICDRS) is empty and data has not been written to the I²C Bus Transmit Data Register (ICDRT) with the IIC in transmission mode (TRS bit = 1 in ICCR2), the SCLn line is automatically held low over the subsequent intervals. This low-hold period is extended until the transmit data is written, which prevents the unintended transmission of erroneous data.

Master transmit mode:

- Low-level interval after a start or restart condition is issued
- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

Slave transmit mode:

- Low-level interval between the 9th clock cycle of one transfer and the 1st clock cycle of the next.

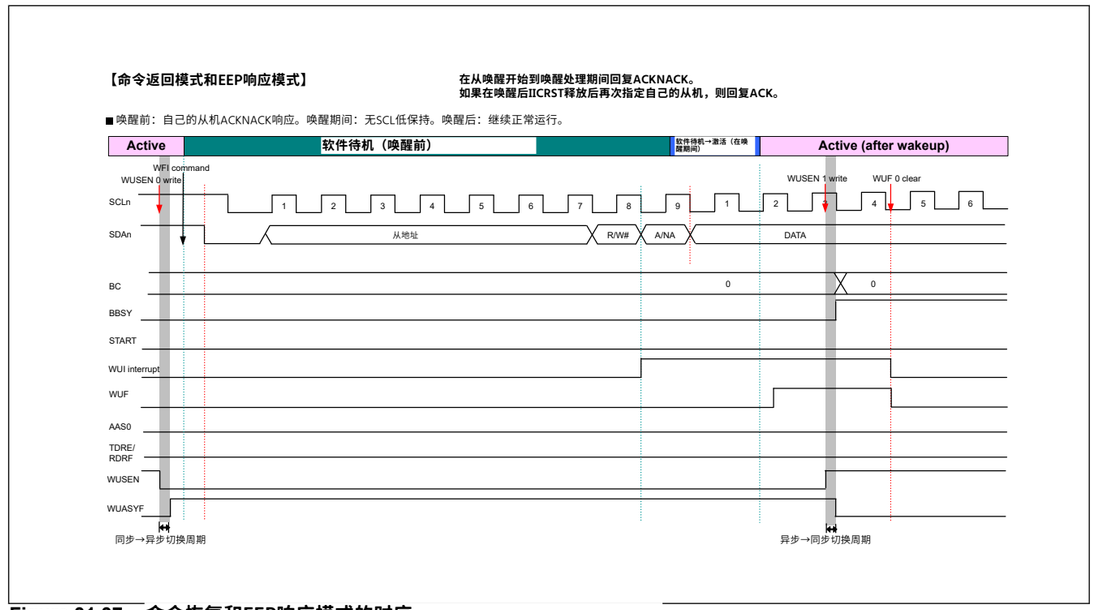


Figure 31.37 命令恢复和EEP响应模式的时序

31.9 SCL的自动低保持功能

31.9.1 防止传输数据错误传输的功能

如果I2C总线移位寄存器(ICDRS)为空且数据尚未写入I2C总线发送数据寄存器(ICDRT)且IIC处于传输模式（TRS位=ICCR2中的1），则SCLn线为在随后的时间间隔内自动保持低电平。这个低保持期一直延长到发送数据被写入，这样可以防止错误数据的意外传输。

主传输模式：

●发出启动或重启条件后的低电平间隔

●一次传输的第9个时钟周期和下一次传输的第1个时钟周期之间的低电平间隔。

从机发送模式：

●一次传输的第9个时钟周期和下一次传输的第1个时钟周期之间的低电平间隔。

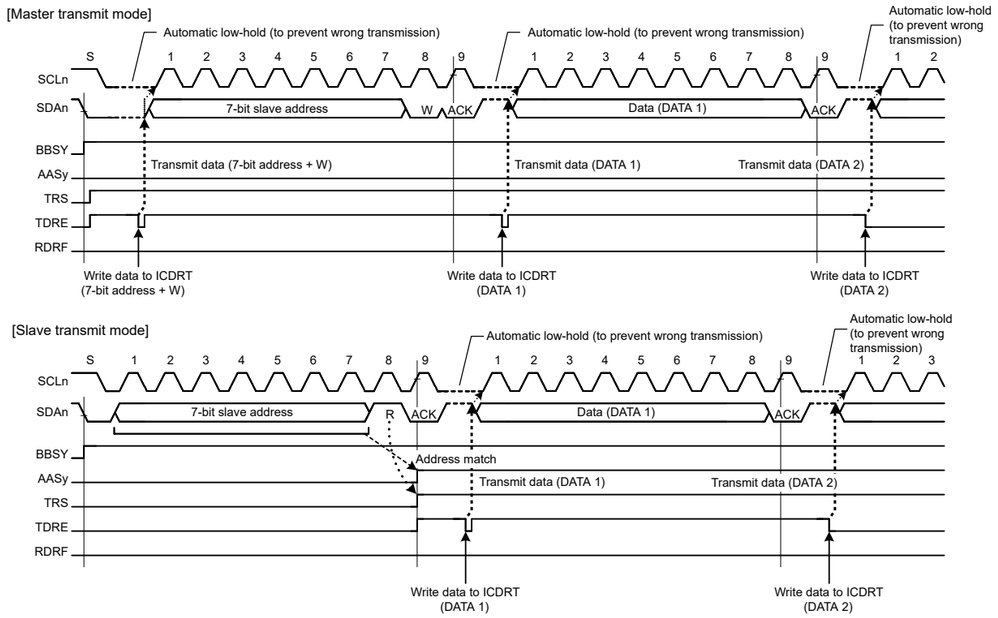


Figure 31.38 Automatic low-hold operation in transmit mode

31.9.2 NACK Reception Transfer Suspension Function

This function suspends transfer operation when NACK is received in transmit mode (TRS bit = 1 in ICCR2). This function is enabled when the NACKE bit in ICFER is set to 1. If the next transmit data is already written (TDRE flag = 0 in ICSR2) when NACK is received, the next data transmission on the falling edge of the 9th SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit and receive operations are discontinued. To restore transmit or receive operation, after issuing the restart condition, you need to set the NACKF flag to 0 and try again, or set the NACKF flag to 0 after issuing the stop condition and then start again from issuing the start condition..

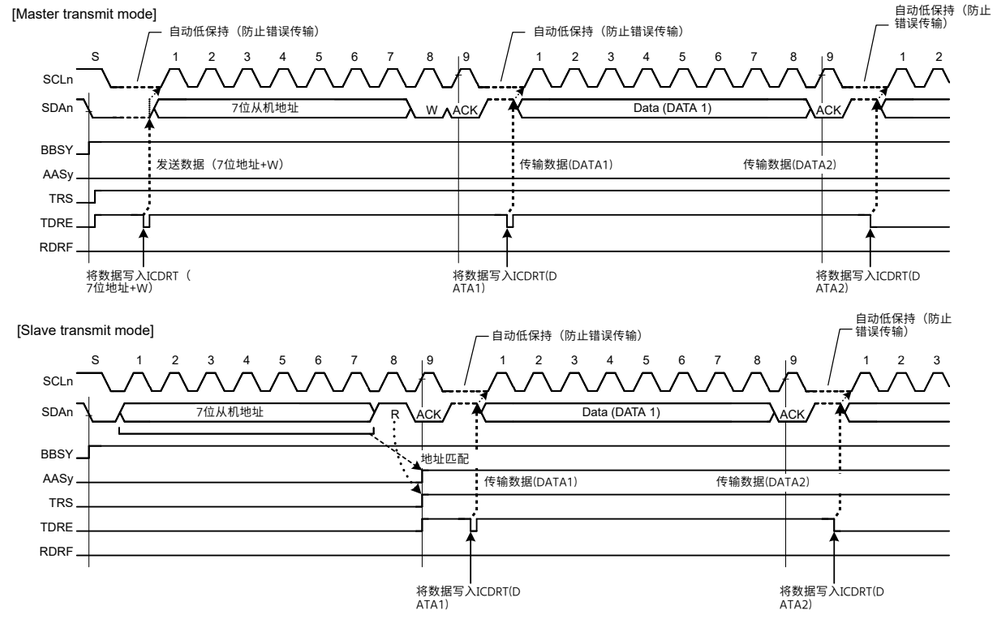


Figure 31.38 发送模式下的自动低保持操作

31.9.2 NACK接收传输暂停功能

当在发送模式下接收到NACK（ICCR2中的TRS位=1）时，该函数暂停传输操作。当ICFER中的NACKE位设置为1时，此功能使能。如果在收到NACK时已经写入下一个发送数据（ICSR2中的TDRE标志=0），则在第9个SCL时钟周期的下降沿进行下一个数据发送被自动挂起。这可以防止SDAn线路输出电平在下一个发送数据的MSB为0时保持低电平。

如果传输操作被该函数挂起（ICSR2中的NACKF标志=1），发送和接收操作将中断。要恢复发送或接收操作，在发出重启条件后，您需要将NACKF标志设置为0并重试，或者在发出停止条件后将NACKF标志设置为0，然后从发出启动条件重新开始。

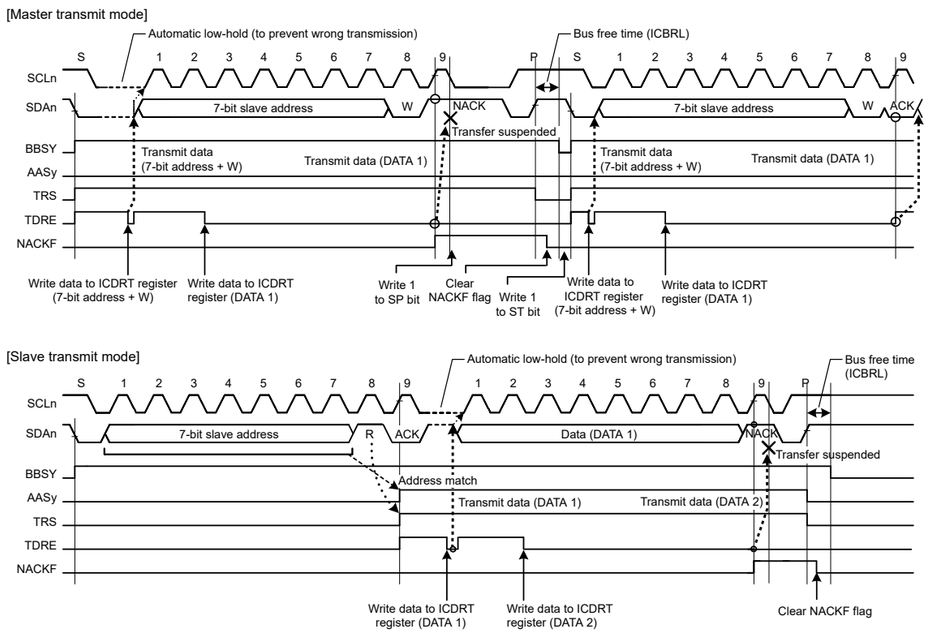


Figure 31.39 Suspension of data transfer when NACK is received, when NACKE = 1

31.9.3 Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in receive mode (TRS = 0 in ICCR2), the IIC holds the SCLn line low automatically immediately before the next data is received to prevent a failure to receive data.

This function is enabled even if the read processing of the final receive data is delayed and, in the meantime, the IIC slave address is designated after a stop condition is issued. This function does not interfere with other communication because the IIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Periods in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) 1-byte receive operation and automatic low-hold function using the WAIT bit

When the WAIT bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the WAIT bit function. Additionally, when the ICMR3.RDRFS bit is 0, the IIC automatically sends the ACKBT bit value in ICMR3 for the acknowledge bit in the period from the falling edge of the 8th SCL clock cycle to the falling edge of the 9th SCL clock cycle, and automatically holds the SCLn line low on the falling edge of the 9th SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables byte-wise receive operation.

The WAIT bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master or slave receive mode.

(2) 1-byte receive operation (ACK/NACK transmission control) and automatic low-hold function using the RDRFS bit

When the RDRFS bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF flag in ICSR2 is set to 1 (receive data full) on the rising edge of the eighth SCL clock cycle, and the SCLn line is automatically held low on the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation through the ACK or NACK transmission control based on the data received in byte units.

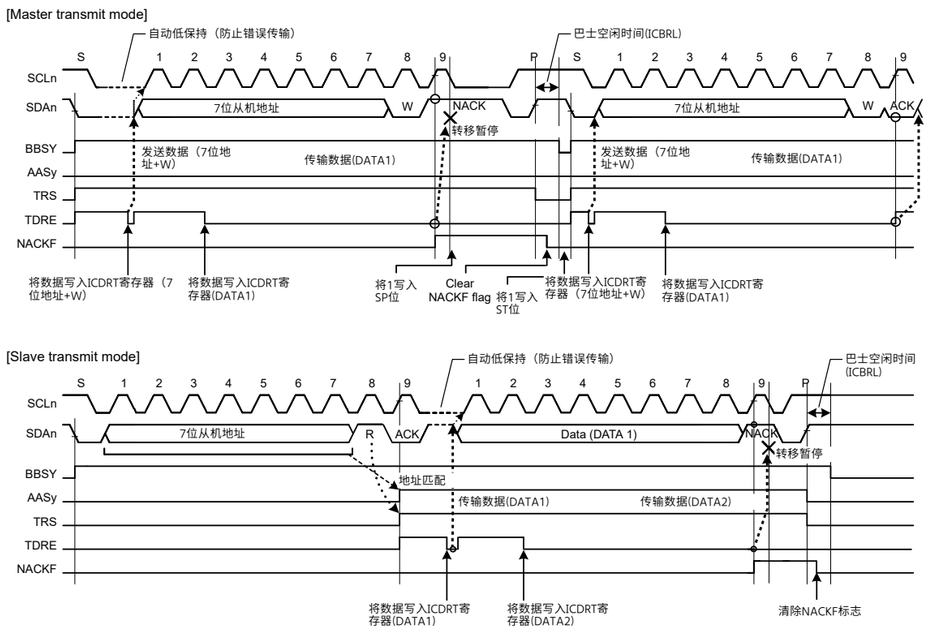


Figure 31.39 接收到NACK时暂停数据传输，当NACKE=1

31.9.3 防止数据接收失败的功能

如果在接收模式（ICCR2中的TRS=0）下接收数据（ICDRR）读取延迟一个传输帧或更长时间且接收数据已满（ICSR2中的RDRF标志=1）时响应处理延迟，则IIC保持在接收到下一个数据之前，SCLn线自动变为低电平，以防止接收数据失败。

即使最终接收数据的读取处理延迟，该功能也有效，同时，在发出停止条件后指定IIC从机地址。此功能不会干扰其他通信，因为在发出停止条件后发生与其自己的从地址不匹配时，IIC不会将SCLn线保持为低电平。

SCLn线保持低电平的周期可以通过ICMR3中的WAIT和RDRFS位的组合来选择。

(1) 使用WAIT位的1字节接收操作和自动低保持功能

当ICMR3中的WAIT位设置为1时，IIC使用WAIT位功能执行1字节接收操作。此外，当ICMR3.RDRFS位为0时，IIC会在第8个SCL时钟周期的下降沿到第9个SCL时钟周期的下降沿期间自动发送ICMR3中的ACKBT位值作为确认位，并且使用WAIT位功能在第9个SCL时钟周期的下降沿自动将SCLn线保持为低电平。该低保持通过从ICDRR读取数据来释放，从而启用逐字节接收操作。

在主机或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧启用WAIT位功能。

(2) 1字节接收操作（ACKNACK传输控制）和使用RDRFS位的自动低保持功能

当ICMR3中的RDRFS位设置为1时，IIC使用RDRFS位功能执行1字节接收操作。当RDRFS位为1时，ICSR2中的RDRF标志位在第8个SCL时钟周期的上升沿置1（接收数据满），并且SCLn线在第8个SCL的下降沿自动保持为低时钟周期。该低保持通过向ICMR3中的ACKBT位写入值来释放，但不能通过从ICDRR读取数据来释放，ICDRR可以根据以字节为单位接收的数据通过ACK或NACK传输控制进行接收操作。

The RDRFS bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master or slave receive mode.

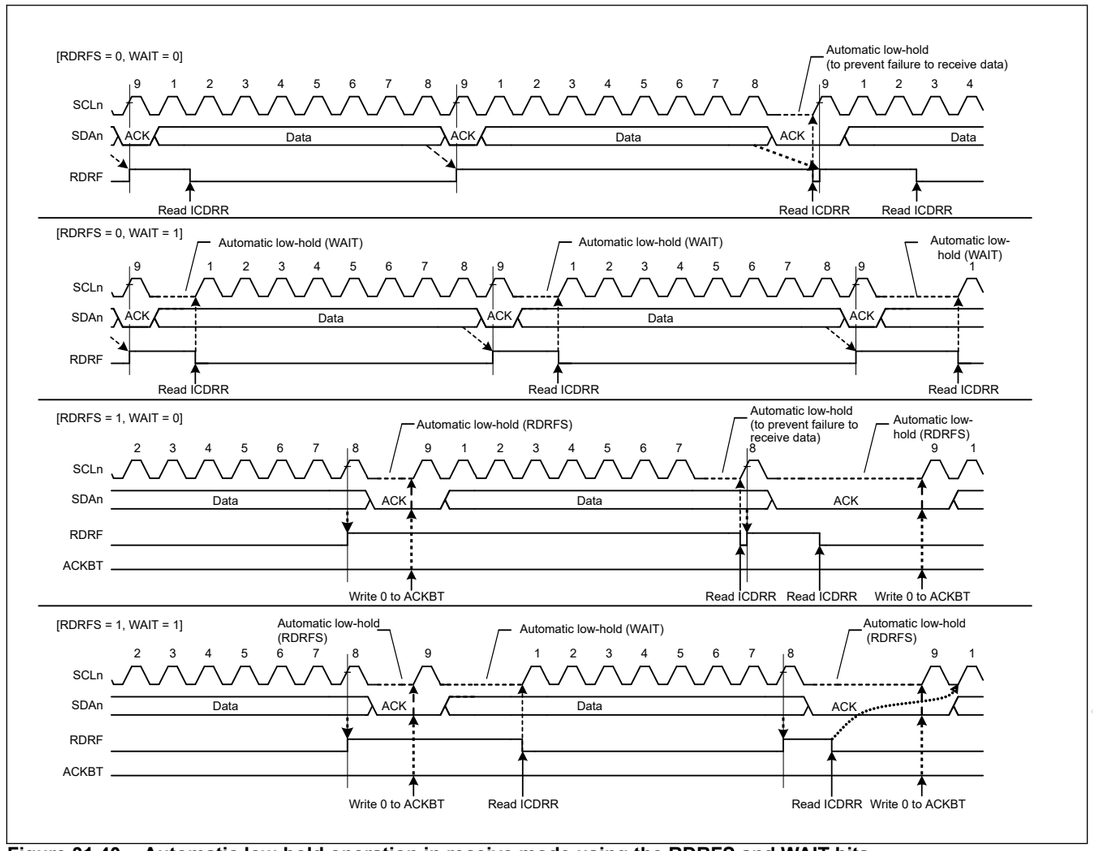


Figure 31.40 Automatic low-hold operation in receive mode using the RDRFS and WAIT bits

31.10 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I^2C bus standard, the IIC provides functions to prevent double-issue of a start condition, detect arbitration-lost during transmission of NACK, and detect arbitration-lost in slave transmit mode.

31.10.1 Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line was already driven low by another master device issuing a start condition, the IIC regards its own start condition as an error and considers this a loss in arbitration. Priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the IIC regards this as a double-issuing-of-start-condition error and considers itself to have lost in arbitration. This prevents a failure of transfer resulting from a start condition being issued while transfer is in progress.

When a start condition is issued successfully, if the transmit data including the address bits (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and a low level is detected on the SDAn line, the IIC loses in arbitration.

After a loss in arbitration of mastership, the IIC immediately enters slave receive mode. If a slave address, including the general call address, matches its own address at this time, the IIC continues in slave operation.

在主机或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧启用RDRFS位功能。

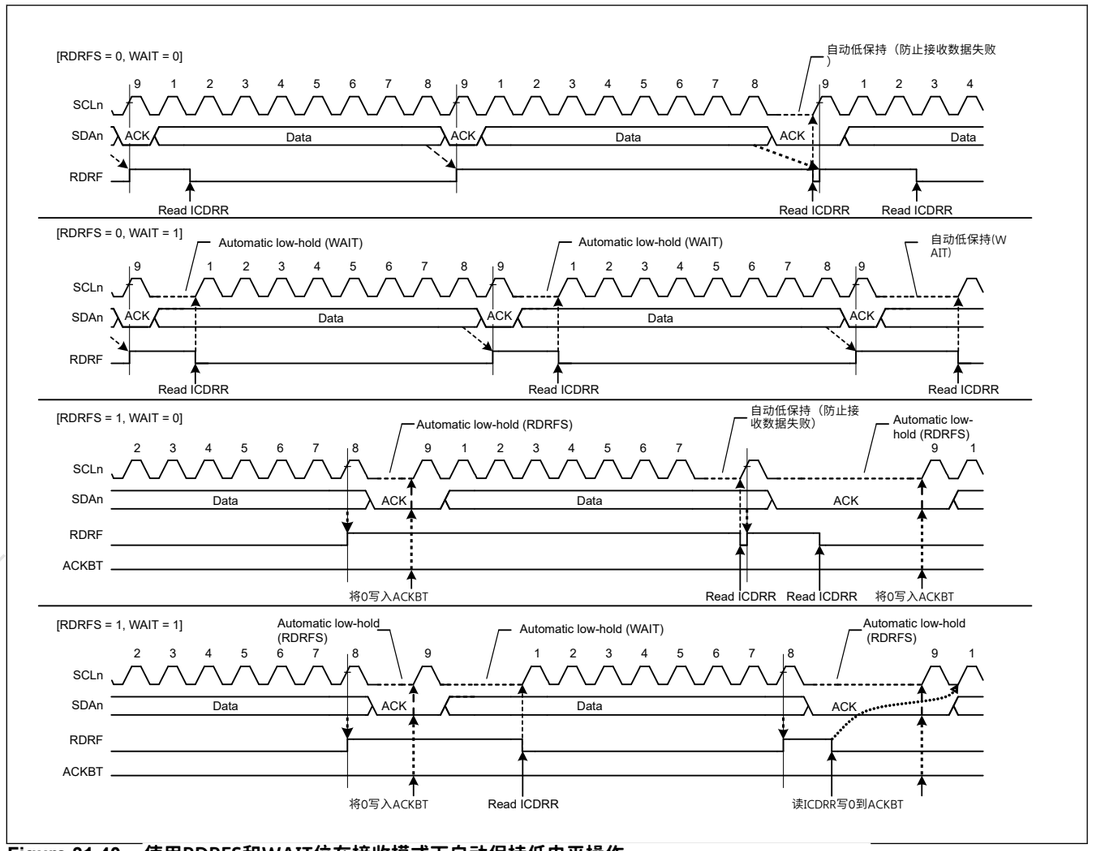


Figure 31.40 使用RDRFS和WAIT位在接收模式下自动保持低电平操作

31.10 仲裁丢失检测功能

除了I2C总线标准定义的正常仲裁丢失检测功能外，IIC还提供防止重复发出启动条件、在NACK传输期间检测仲裁丢失以及在从机发送中检测仲裁丢失的功能模式。

31.10.1 主仲裁丢失检测（MALE位）

IIC将SDAn线驱动为低电平以发出启动条件。但是，如果SDAn线已经被另一个发出启动条件的主设备驱动为低电平，则IIC将其自己的启动条件视为错误，并认为这是仲裁失败。其他主设备优先传输。类似地，如果在总线繁忙时通过将ICCR2中的ST位设置为1来请求发出启动条件（ICCR2中的BBSY标志=1），则IIC将此视为双重发出启动条件错误，并且认为自己在仲裁中败诉。这可以防止由于在传输过程中发出启动条件而导致传输失败。

当启动条件成功发出时，如果发送数据包括地址位（内部SDA输出电平）与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻抗状态)并且在SDAn线上检测到低电平，则IIC在仲裁中失败。

在主控权仲裁失败后，IIC立即进入从机接收模式。如果此时从机地址（包括广播地址）与自己的地址匹配，则IIC继续从机操作。

A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).

[Master arbitration-lost conditions]

- Mismatching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ST bit in ICCR2 to 1 while the BBSY flag in ICCR2 is set to 0 (erroneous issuing of a start condition)
- Setting of the ST bit in ICCR2 to 1 (start condition double-issue error) while the BBSY flag is 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2).

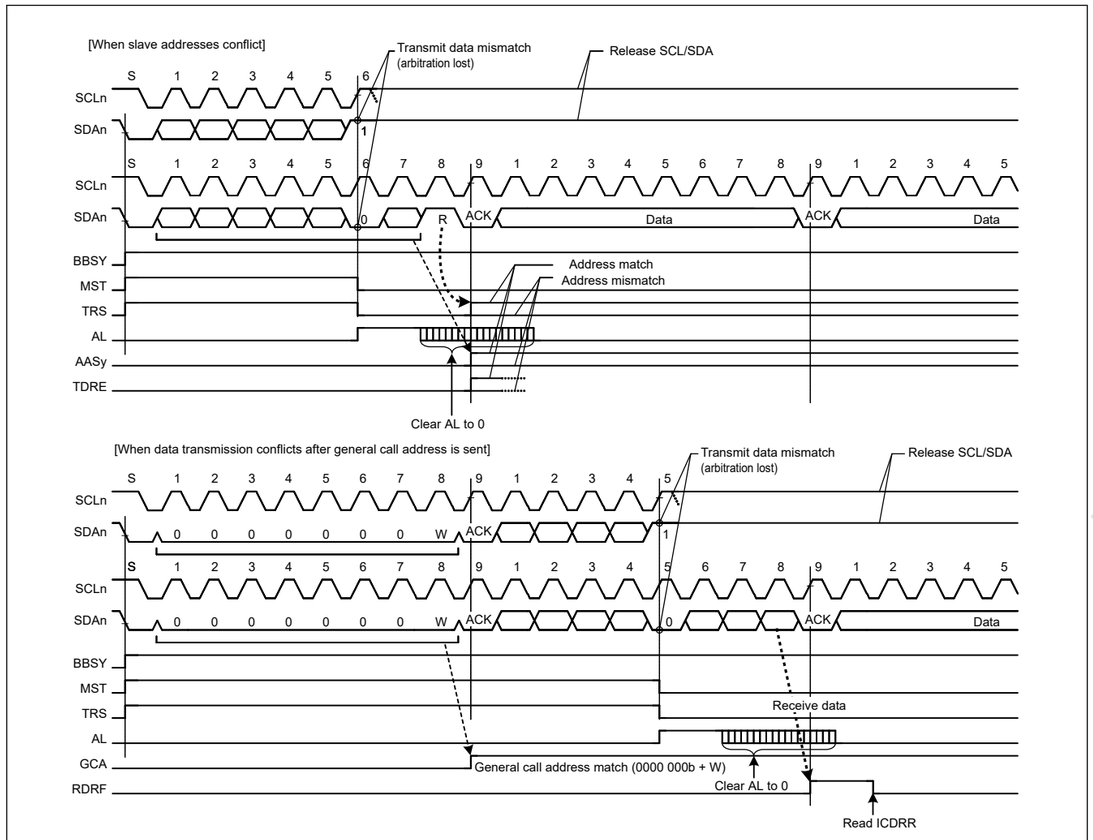


Figure 31.41 Examples of master arbitration-lost detection when MALE = 1

当ICFER中的MALE位为1（启用主仲裁丢失检测）时满足以下条件时，检测到主控仲裁丢失。

[Master arbitration-lost conditions]

●通过将ICCR2中的ST位设置为1，同时将ICCR2中的BBSY标志设置为0，发出启动条件后，SDA输出的内部电平与SDAn线上的电平不匹配（错误发出启动条件）

●在BBSY标志为1时将ICCR2中的ST位设置为1（启动条件双发错误）

●当发送数据不包括确认（内部SDA输出电平）与主发送模式下SDAn线上的电平不匹配时（ICCR2中的MST和TRS位=11b）。

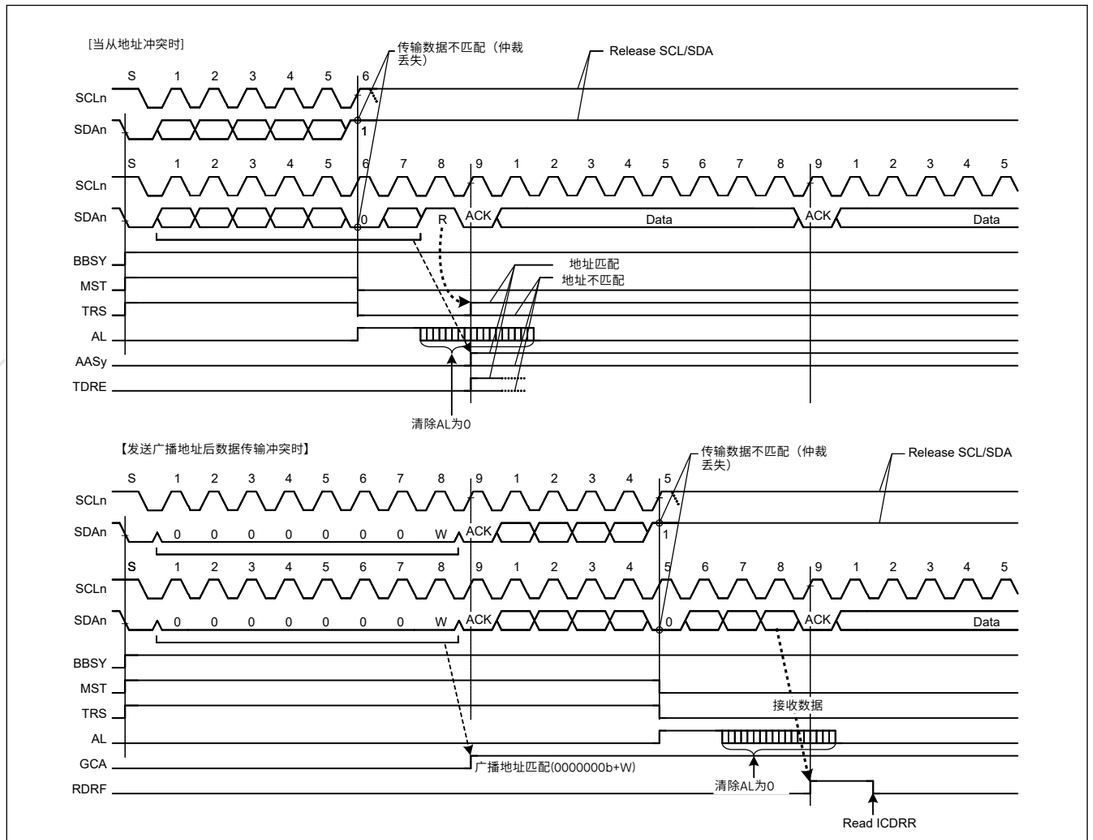


Figure 31.41 MALE=1时的主仲裁丢失检测示例

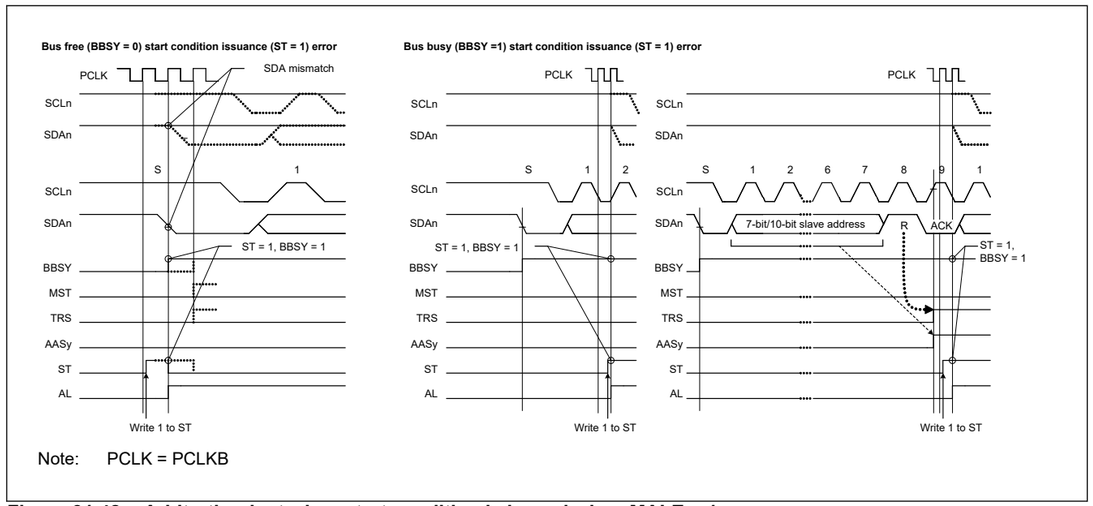


Figure 31.42 Arbitration-lost when start condition is issued when MALE = 1

31.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

This function causes arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and the low level is detected on the SDAn line during transmission of NACK in receive mode. Arbitration is lost because of a conflict between NACK and ACK transmissions when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such a conflict occurs when multiple master devices send or receive the same information through a single slave device. Figure 31.43 shows an example of arbitration-lost detection during transmission of NACK.

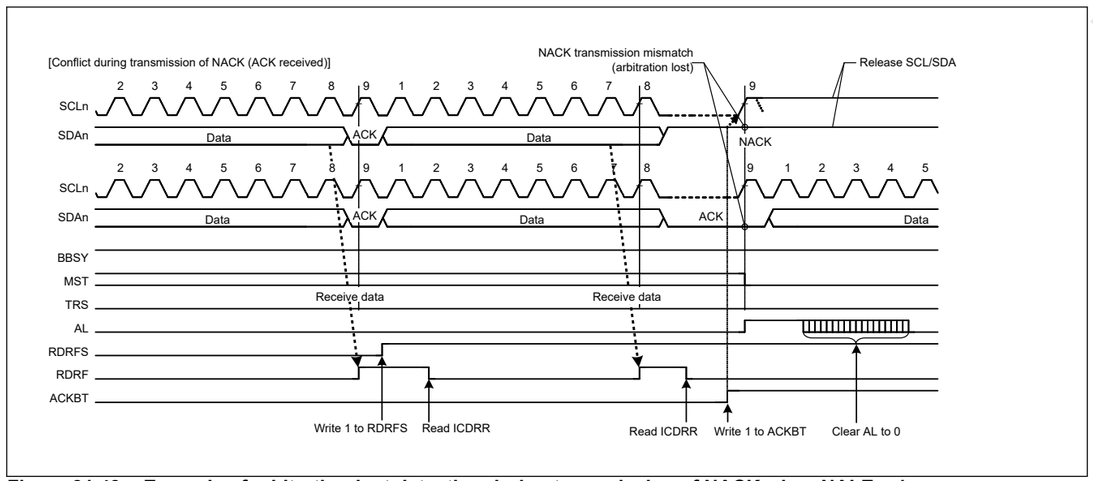


Figure 31.43 Example of arbitration-lost detection during transmission of NACK when NALE = 1

The following explains arbitration-lost detection using an example in which two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in either master A or master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the required 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like

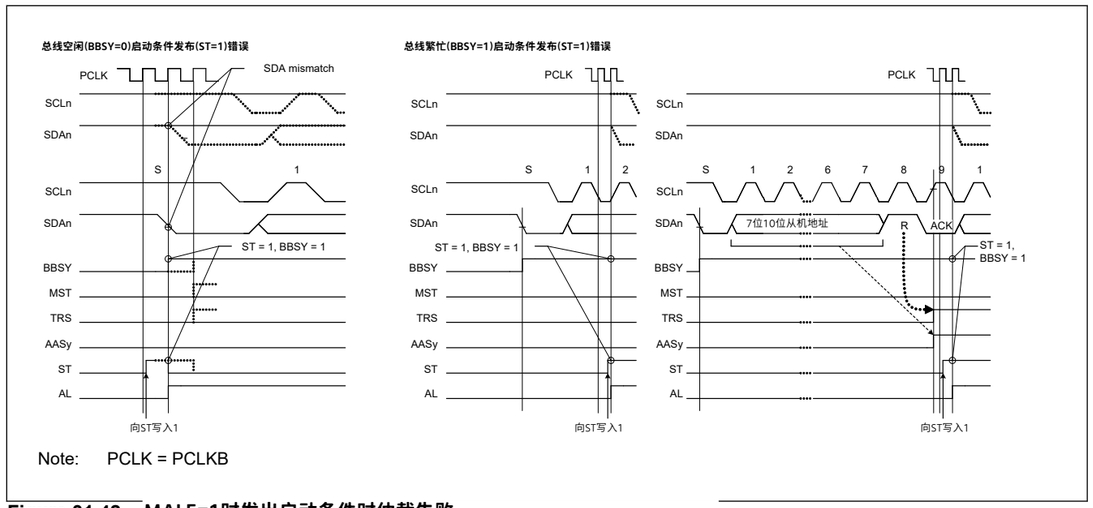


Figure 31.42 MALE=1时发出启动条件时仲裁失败

31.10.2 在NACK传输期间检测仲裁丢失的功能（NALE位）

如果内部SDA输出电平与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻抗状态）并且在上检测到低电平，此功能会导致仲裁丢失在接收模式下发送NACK期间的SDAn线。当多主控系统中两个或多个主控设备同时从同一从属设备接收数据时，由于NACK和ACK传输之间的冲突，仲裁会丢失。当多个主设备通过单个从设备发送或接收相同的信息时，就会发生这种冲突。图31.43显示了在NACK传输期间检测仲裁丢失的示例。

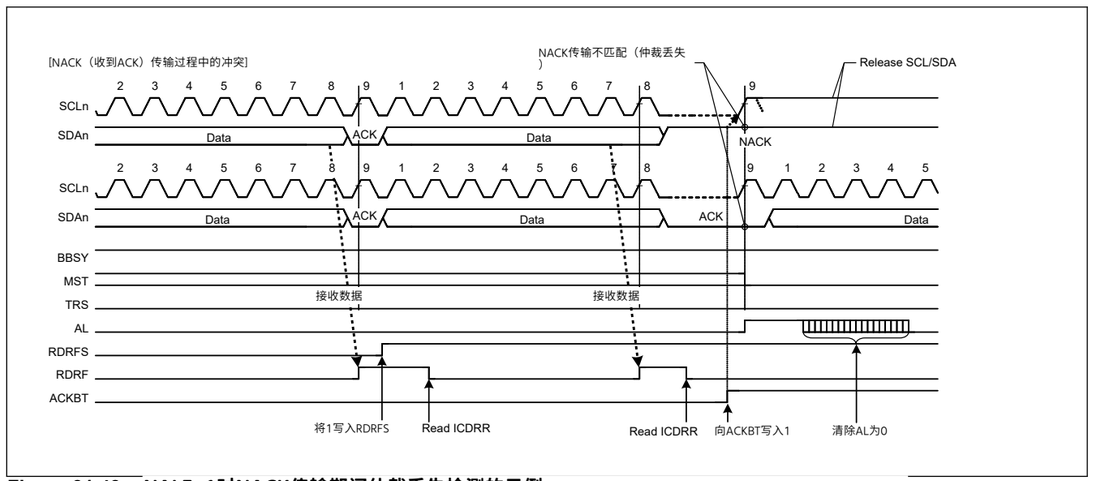


Figure 31.43 NALE=1时NACK传输期间仲裁丢失检测的示例

下面以两个主设备（主设备A和主设备B）和一个从设备通过总线连接的示例来说明仲裁丢失检测。在本例中，主设备A从从设备接收2个字节的数据，主设备B从从设备接收4个字节的数据。

如果主设备A和主设备B同时访问从设备，因为从设备地址相同，在访问从设备期间，主设备A或主设备B都不会丢失仲裁。因此，主机A和主机B都承认他们已经获得了总线控制权并照此运行。主设备A在从从设备接收到2个最终字节的数据时发送NACK。同时，masterB发送ACK，因为它没有收到所需的4字节数据。此时，来自masterA的NACK传输和来自masterB的ACK传输冲突。一般来说，如果像这样的冲突

this occurs, master A cannot detect the ACK transmitted by master B and issues a stop condition. The stop condition issue conflicts with the SCL clock output of master B, which disrupts communication.

When the IIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost. If arbitration is lost during transmission of NACK, the IIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing, such as 0xFF transmission processing, which is required if the UDID (Unique Device Identifier) of the assigned address does not match in the Get UDID general processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3).

31.10.3 Slave Arbitration-Lost Detection (SALE Bit)

This function causes arbitration to be lost if the transmit data (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state), and the low level is detected on the SDAn line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

When the IIC loses slave arbitration, the IIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing for the transmission of 0xFF.

The IIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2).

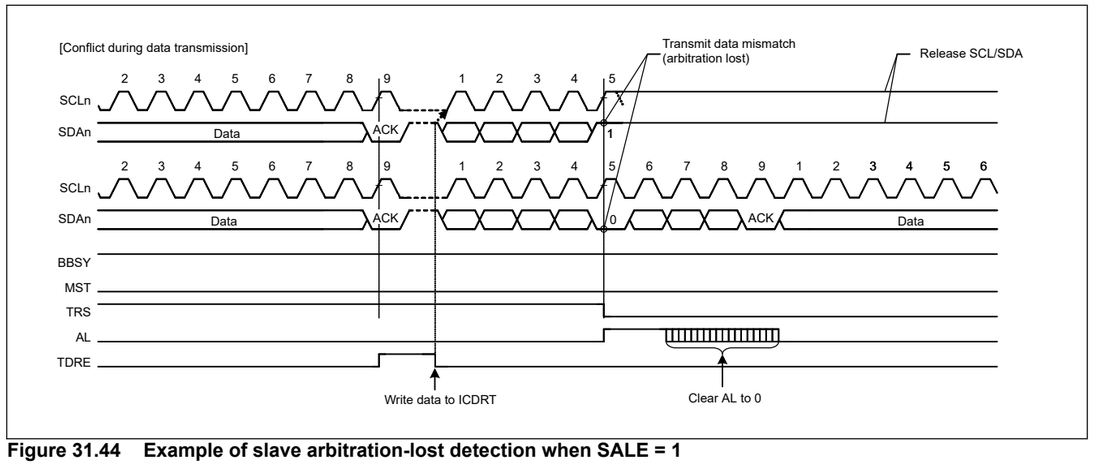


Figure 31.44 Example of slave arbitration-lost detection when SALE = 1

发生这种情况时，主机A无法检测到主机B发送的ACK并发出停止条件。停止条件问题与主B的SCL时钟输出冲突，从而中断通信。

当IIC在NACK传输过程中收到ACK时，它会检测到与其他主设备冲突的失败并导致仲裁丢失。如果在NACK传输过程中仲裁丢失，IIC立即取消从机匹配条件并进入从机接收模式。这可以防止发出停止条件，从而防止总线上的通信故障。

同样，在SMBus的ARP命令处理中，检测传输过程中仲裁丢失的功能
NACK也可用于消除额外的时钟周期处理，例如0xFF传输处理，如果分配地址的UDID（唯一设备标识符）在分配地址命令后的获取UDID常规处理中不匹配，则需要此处理。

IIC在NACK传输期间检测到仲裁丢失，当满足以下条件时
ICFER设置为1（启用NACK传输期间的仲裁丢失检测）。

[在NACK传输期间仲裁丢失的条件]

●在发送NACK（ICMR3中的ACKBT位=1）期间，当内部SDA输出电平与SDAn线不匹配时（接收到ACK）。

31.10.3 从设备仲裁丢失检测（SALE位）

如果发送数据（内部SDA输出电平）与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻状态），此功能会导致仲裁丢失，并且在从机发送模式下，SDAn线上检测到低电平。这种仲裁丢失检测功能主要用于通过SMBus传输UDID（唯一设备标识符）时。

当IIC失去从机仲裁时，IIC立即从从机匹配状态中释放并进入从机接收模式。该功能可以检测通过SMBus传输UDID期间的数据冲突，并消除后续对0xFF传输的冗余处理。

当ICFER中的SALE位设置为1（启用从设备仲裁丢失检测）满足以下条件时，IIC检测从设备仲裁丢失。

[从机仲裁失败的条件]

●当发送数据不包括确认（内部SDA输出电平）与从发送模式下的SDAn线不匹配时（MST和TRS位=ICCR2中的01b）。

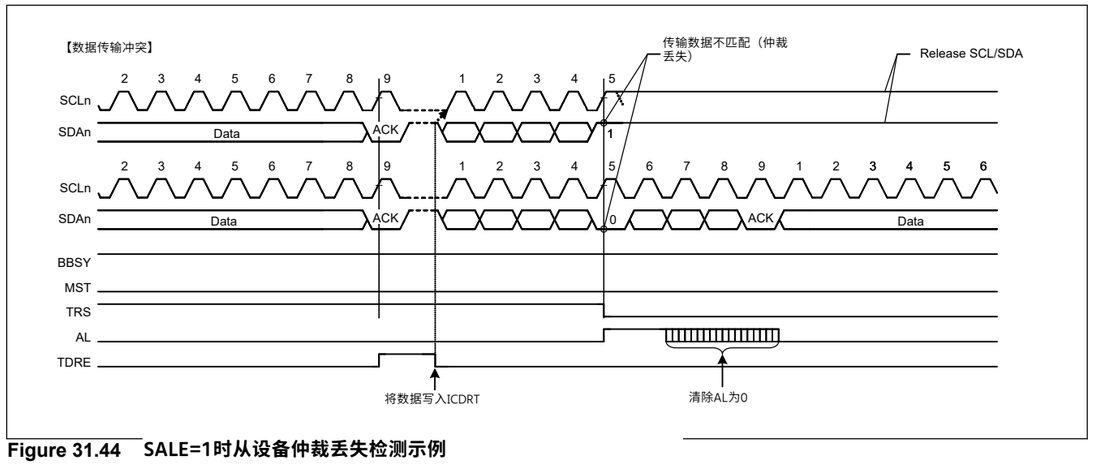


Figure 31.44 SALE=1时从设备仲裁丢失检测示例

31.11 Start, Restart, and Stop Condition Issuing Function

31.11.1 Issuing a Start Condition

The IIC issues a start condition when the ST bit in ICCR2 is set to 1. When the ST bit is set to 1, a start condition request is made, and the IIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the IIC automatically shifts to the master transmit mode.

To issue a start condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the time set in ICBRH and the start condition hold time elapse.
3. Drive the SCLn line low (high level to low level).
4. Detect low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

31.11.2 Issuing a Restart Condition

The IIC issues a restart condition when the RS bit in ICCR2 is set to 1. When the RS bit is set to 1, a restart condition request is made, and the IIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a restart condition:

1. Release the SDAn line.
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRL and the restart condition setup time elapse.
5. Drive the SDAn line low (high level to low level).
6. Ensure the time set in ICBRH and the restart condition hold time elapse.
7. Drive the SCLn line low (high level to low level).
8. Detect a low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

Note: When issuing restart condition requests, write the slave address to ICDRT after confirming that ICCR2.RS = 0. Data written while ICCR2.RS = 1 is not forwarded because of the retransmission condition before the occurrence.

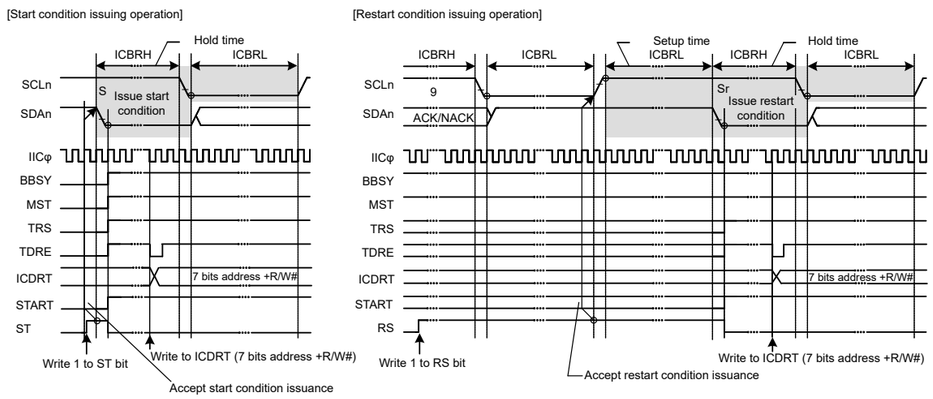


Figure 31.45 Start and restart condition issue timing using the ST and RS bits

31.11 启动、重启和停止条件发布功能

31.11.1 发出开始条件

当ICCR2中的ST位设置为1时，IIC发出启动条件。 当ST位设置为1时，发出启动条件请求，当ICCR2中的BBSY标志为0时，IIC发出启动条件（总线自由状态）。当启动条件正常发出时，IIC自动切换到主机发送模式。

发出开始条件：

1.将SDAn线拉低（高电平转低电平）。

2.确保ICBRH中设置的时间和启动条件保持时间已过。

3.将SCLn线拉低（高电平转低电平）。

4.检测SCLn线的低电平，确保ICBRL中设置的SCLn线的低电平周期过去。

31.11.2 发出重启条件

当ICCR2中的RS位设置为1时，IIC发出重启条件。当RS位设置为1时，发出重启条件请求，当ICCR2中的BBSY标志为1时，IIC发出重启条件（总线忙状态）并且ICCR2中的MST位为1（主模式）。

发出重启条件：

1.释放SDAn线。

2.确保ICBRL中设置的SCLn线的低电平周期已过。

3.释放SCLn线（低电平到高电平）。

4.检测SCLn线上的高电平并确保ICBRL中设置的时间和重启条件设置时间已过。

5.将SDAn线拉低（高电平转低电平）。

6.确保ICBRH中设置的时间和重启条件保持时间已过。

7.将SCLn线拉低（从高电平到低电平）。

8.检测SCLn线上的低电平，确保ICBRL中设置的SCLn线的低电平周期过去。

Note: 发出重启条件请求时，确认ICCR2.RS=0后，将从机地址写入ICDRT。在ICCR2.RS=1时写入的数据由于发生前的重传条件而不会转发。

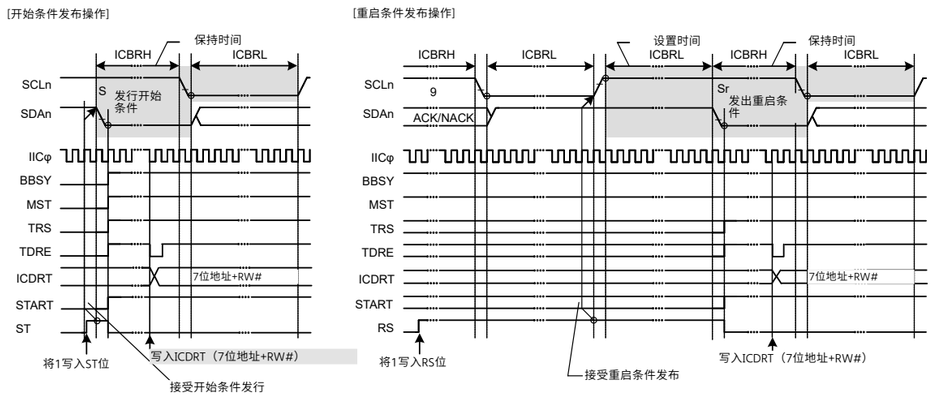


Figure 31.45 使用ST和RS位的启动和重启条件发出时序

Figure 31.46 shows the operation timing when a restart condition is issued after the master transmission.

[To issue a restart condition after the master transmission:]

1. Initialize the IIC using the procedure in section 31.3.2. Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is open, then set the ST bit in ICCR2 to 1 (start condition issuance request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and the START flags in ICSR2 are automatically set to 1 and the ST bit is automatically set to 0. If the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that a start condition is successfully issued as requested by the ST bit has been successfully completed. The MST and TRS bits in ICCR2 are automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 when the TRS bit is set to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. After the data for transmission is written to ICDRT, the TDRE flag is automatically set to 0, data is transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode according to the value of the transmitted R/W# bit. If the value of the R/W# bit is 0, the IIC continues in master transmit mode. If the ICSR2.NACKF flag is 1 at this time, indicating that no slave device recognized the address or that there was an error in communications, write 1 to ICCR2.SP bit to issue a stop condition. To transmit data with an address in the 10-bit format, start by writing 1111 0b, the 2 upper bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower bits of the slave address to ICDRT.
4. After confirming that the TDRE flag in ICSR2 is 1, write data for transmission to the ICDRT register. The IIC automatically holds the SCLn line low until data for transmission is ready, a restart condition is issued or a stop condition is issued.
5. After all bytes of data for transmission are written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1. Then after checking that the START flag in ICSR2 is 1, set the START flag in ICSR2 to 0.
6. Set the RS bit in ICCR2 to 1 (restart condition issue request). On receiving the request, the IIC issues a restart condition.
7. After checking that the START flag in ICSR2 is 1, write the value for transmission (the slave address and the R/W# bit) to ICDRT.

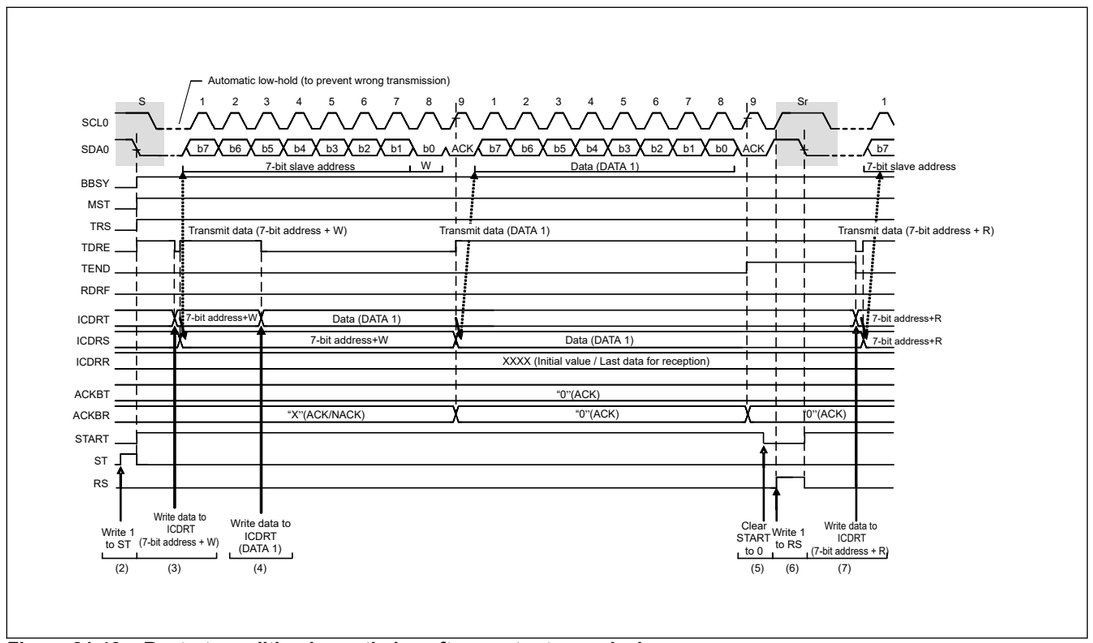


Figure 31.46 Restart condition issue timing after master transmission.

图31.46显示了在主机发送后发出重新启动条件时的操作时序。

[在主传输后发出重启条件：]

1.使用第31.3.2节中的过程初始化IIC。初始设置。

2.读取ICCR2中的BBSY标志以检查总线是否打开，然后将ICCR2中的ST位设置为1（开始条件发出请求）。收到请求后，IIC发出一个开始条件。同时，ICSR2中的BBSY和START标志位自动设置为1，ST位自动设置为0。如果检测到启动条件，则内部电平为SDA输出状态和SDAn线上的电平当ST位为1时匹配，IIC识别成功发出启动条件，因为ST位请求已成功完成。ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。当TRS位设置为1时，ICSR2中的TDRE标志也自动设置为1。

3.检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。待传输数据写入ICDRT后，TDRE标志自动置0，数据从ICDRT传输到ICDRS，TDRE标志再次置1。发送时，TRS位的值会根据发送的RW#位的值自动更新以选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。如果此时ICSR2.NACKF标志位为1，表示没有从设备识别该地址或通信出现错误，向ICCR2.SP位写入1发出停止条件。要使用10位格式的地址传输数据，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。然后，作为第二次地址传输，将从地址的低8位写入ICDRT。

4.确认ICSR2中的TDRE标志为1后，将要发送的数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到传输数据准备好、发出重启条件或发出停止条件。

5.待发送的所有字节数据写入ICDRT寄存器后，等待ICSR2中的TEND标志的值返回1。然后检查ICSR2中的START标志为1后，将ICSR2中的START标志设置为0.

6.将ICCR2中的RS位设置为1（重新启动条件发出请求）。收到请求后，IIC发出重启条件。

7.检查ICSR2中的START标志为1后，将要发送的值（从机地址和RW#位）写入ICDRT。

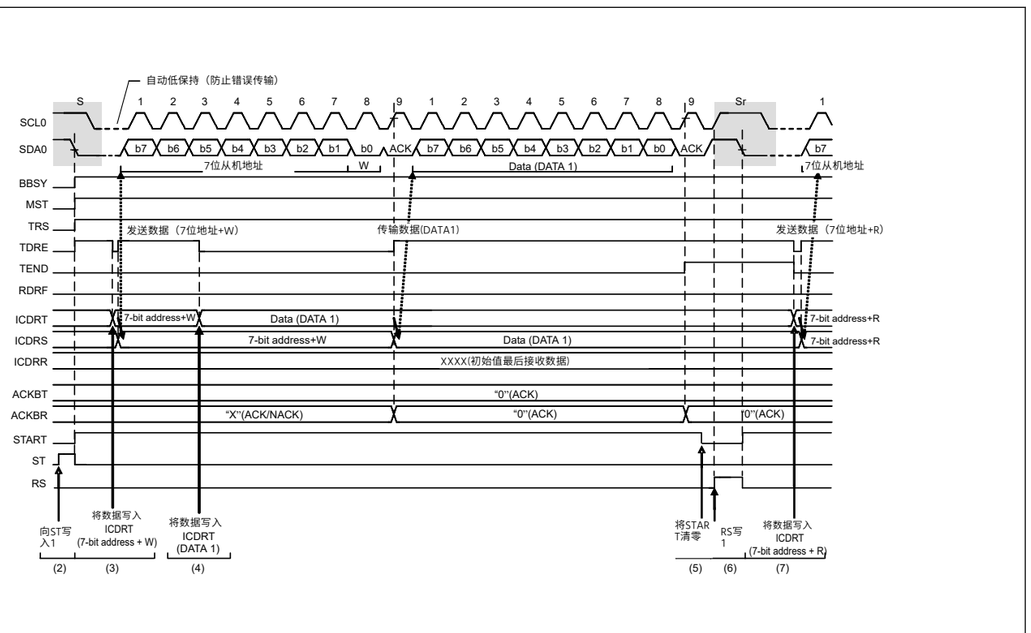


Figure 31.46 主传输后重启条件发出时序。

31.11.3 Issuing a Stop Condition

The IIC issues a stop condition when the SP bit in ICCR2 is set to 1. When the SP bit is set to 1, a stop condition request is made, and the IIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a stop condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRH and the stop condition setup time elapse.
5. Release the SDAn line (low level to high level).
6. Ensure the time set in ICBRL and the bus free time elapse.
7. Clear the BBSY flag to 0 to release the bus mastership.

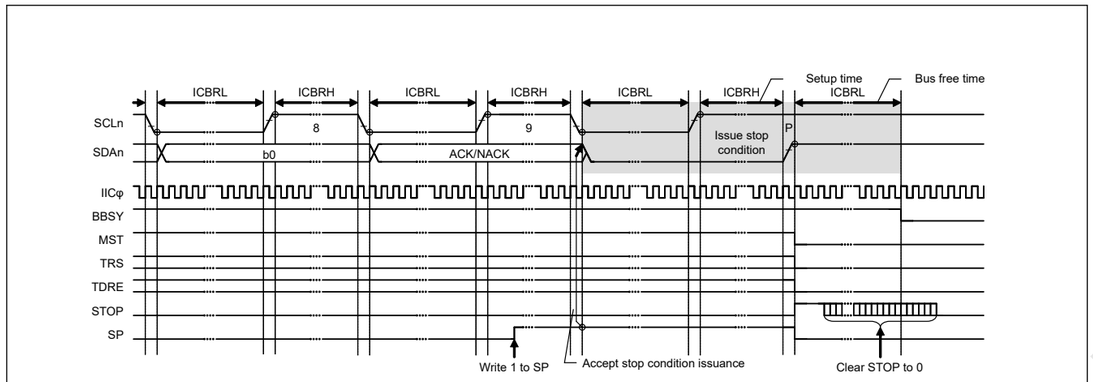


Figure 31.47 Stop condition issue timing using the SP bit

31.12 Bus Hanging

If the clock signals from the master and slave devices are out of synchronization because of noise or other factors, the I^2C bus might hang with a fixed level on the SCLn line or SDAn line.

To manage bus hanging, the IIC has a timeout function to detect hanging by monitoring the SCLn line, and a function for outputting an extra SCL clock cycle to release the bus from:

- A timeout function to detect hanging by monitoring the SCLn line
- The IIC reset function
- An internal reset function.

By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to see whether the IIC or its communicating partner is placing the low level on the SCLn or SDAn line.

31.12.1 Timeout Function

The timeout function can detect when the SCLn line is stuck longer than the predetermined time. The IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low- or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rises or falls), but continues to count unless the SCLn line changes. If the internal counter overflows because no SCLn line changes, the IIC can detect the timeout and report the bus hung state.

31.11.3 发出停止条件

当ICCR2中的SP位设置为1时，IIC发出停止条件。当SP位设置为1时，发出停止条件请求，当ICCR2中的BBSY标志为1时，IIC发出停止条件（总线忙状态）并且ICCR2中的MST位为1（主模式）。

发出停止条件：

1.将SDAn线拉低（高电平转低电平）。

2.确保ICBRL中设置的SCLn线的低电平周期已过。

3.释放SCLn线（低电平到高电平）。

4.检测SCLn线上的高电平并确保ICBRH中设置的时间和停止条件设置时间已过。

5.释放SDAn线（低电平到高电平）。

6.确保ICBRL中设置的时间和巴士空闲时间已过。

7.将BBSY标志清为0以释放总线控制权。

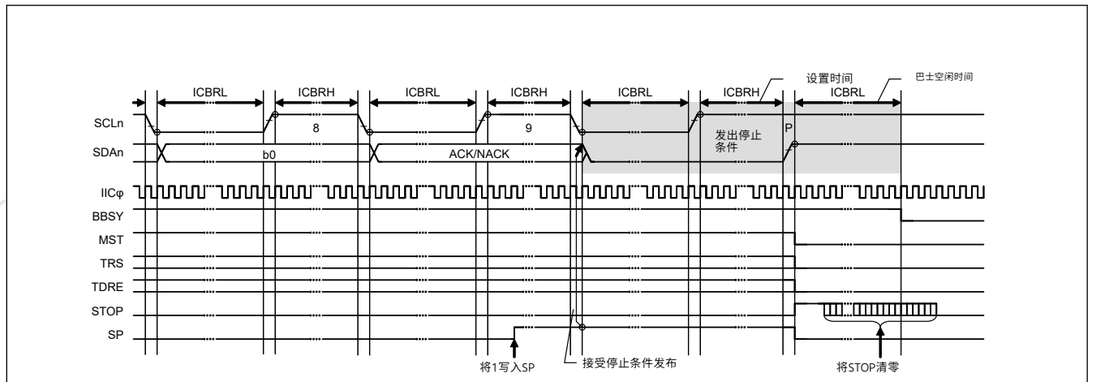


Figure 31.47 使用SP位的停止条件发出时序

31.12 巴士挂

如果来自主从设备的时钟信号由于噪声或其他因素不同步，则I2C总线可能会在SCLn线或SDAn线上以固定电平挂起。

为了管理总线挂起，IIC具有通过监视SCLn线检测挂起的超时功能，以及输出额外SCL时钟周期以释放总线的功能：

●通过监控SCLn线路来检测挂起的超时功能

●IIC复位功能

●内部复位功能。

通过检查ICCR1中的SCLO、SDAO、SCLI和SDAI位，可以查看IIC或其通信伙伴是否将SCLn或SDAn线置于低电平。

31.12.1 超时功能

超时功能可以检测SCLn线路何时卡住超过预定时间。IIC可以通过监视SCLn线在预定时间内保持低电平或高电平来检测异常总线状态。

超时功能监控SCLn线路状态并使用内部计数器计算低电平或高电平周期。每次SCLn线改变（上升或下降）时，超时功能都会复位内部计数器，但除非SCLn线改变，否则会继续计数。如果内部计数器因为SCLn线没有变化而溢出，IIC可以检测到超时并报告总线挂起状态。

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This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state when the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1)
- The IIC slave address is detected (ICSR1 register is not 0x00) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0)
- The bus is open (ICCR2.BBSY flag is 0) while a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function uses the internal reference clock (IICφ) set in the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).

The SCLn line level (low, high, or both levels) during which this counter is activated can be selected in the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter is disabled.

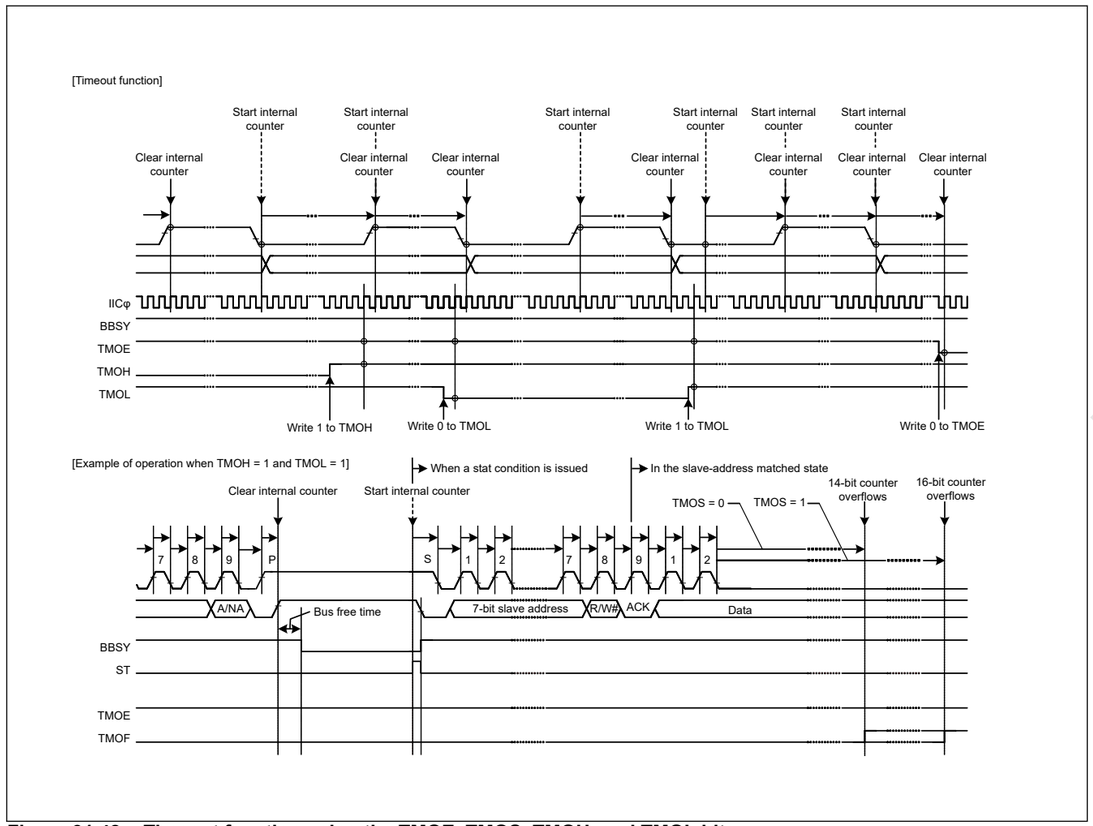

Figure 31.48 Timeout function using the TMOE, TMOS, TMOH, and TMOL bits

31.12.2 Extra SCL Clock Cycle Output Function

In master mode, this function outputs extra SCL clock cycles to release the SDAn line of the slave device from being held low because the master is out of synchronization with the slave device. This function is mainly used in master mode to release the SDAn line of the slave device from being fixed low by including extra cycles of SCL output from the IIC. It uses single cycles of the SCL clock for a bus error where the IIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this function in normal situations. Using it when communications are proceeding correctly leads to malfunctions.

When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the frequency specified in the CKS[2:0] bits in ICMR1, and in the ICBRH and ICBRL registers, is output as an extra clock cycle. After output of this

此超时功能在ICFER.TMOE位为1时启用。在以下情况下，当SCLn线卡在低电平或高电平时，它会检测到挂起状态：

●总线繁忙（ICCR2.BBSY标志为1）在主机模式（ICCR2.MST位为1）

●检测到IIC从机地址（ICSR1寄存器不是0x00）并且在从机模式下总线忙（ICCR2.BBSY标志为1）（ICCR2.MST位为0）

●请求启动条件时（ICCR2.ST位为1），总线打开（ICCR2.BBSY标志为0）。

超时功能的内部计数器使用ICMR1的CKS[2:0]位中设置的内部参考时钟(IICφ)作为计数源。Itfunctionsasa16-bitcounterwhenlongmodeisselected(TMOSbit=0inICMR2)ora14-bitcounterwhenshortmodeisselected(TMOSbit=1).

可以在TMOH和
ICMR2中的TMOL位。如果TMOL和TMOH位都设置为0，则内部计数器被禁用。

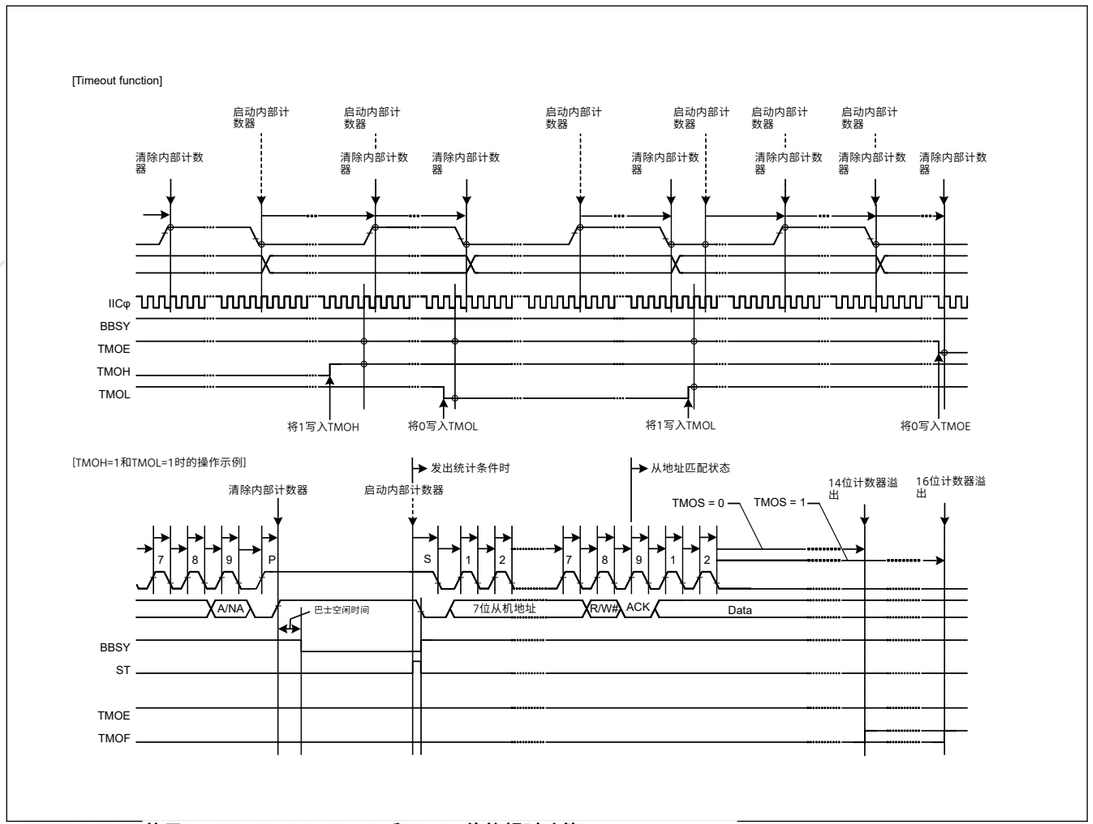

Figure 31.48 使用TMOE、TMOS、TMOH和TMOL位的超时功能

31.12.2 额外的SCL时钟周期输出功能

在主模式下，该函数输出额外的SCL时钟周期，以释放从设备的SDAn线保持低电平，因为主设备与从设备不同步。该功能主要用于主机模式，通过包含IIC的额外SCL输出周期来释放从机设备的SDAn线固定为低电平。它使用SCL时钟的单个周期来处理IIC无法发出停止条件的总线错误，因为从设备将SDAn线保持在低电平。在正常情况下不要使用此功能。在通信正常进行时使用它会导致故障。

当ICCR1中的CLO位在主机模式下设置为1时，以ICMR1中的CKS[2:0]位以及ICBRH和ICBRL寄存器中指定的频率的SCL时钟的单个周期作为额外输出输出时钟周期。这个输出后

single cycle of the SCL clock, the CLO bit is automatically set to 0. At this time, if ICCR2.BBSY = 1, the SCL pin goes low, and when ICCR2.BBSY = 0, the SCL pin goes high. After confirming that the CLO bit is 0 by software, write 1 to the CLO bit to output the additional clock continuously.

When the IIC module is in master mode and the slave device is holding the SDAn line low because synchronization with the slave device is lost because of effects like noise, the output of a stop condition is not possible. This function can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held low, and so recover the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming the release of the SDAn line by the slave device, complete communications by reissuing the stop condition.

[Output conditions for using the CLO bit in ICCR1]

- When the bus is open (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low.

Figure 31.49 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

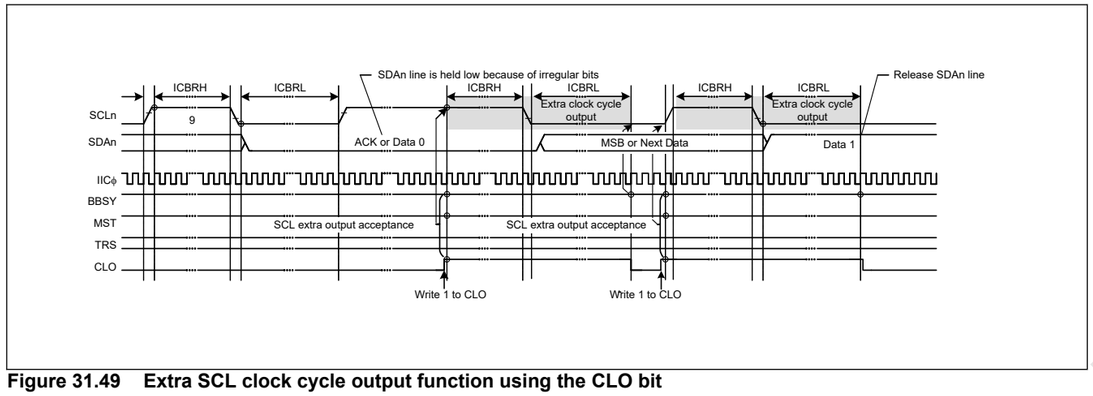

Figure 31.49 Extra SCL clock cycle output function using the CLO bit

31.12.3 IIC Reset and Internal Reset

The IIC module incorporates a function for resetting itself. It uses two types of resets:

- An IIC reset, which initializes all registers, including the BBSY flag in ICCR2.
- An internal reset, which releases the IIC from the slave-address matched state and initializes the internal counter while saving other settings.

After issuing a reset, always set the IICRST bit in ICCR1 to 0. Both types of resets are valid for release from bus-hung states, because both restore the output state of the SCLn and SDAn pins to the high-impedance state.

Issuing a reset during slave operation might lead to a loss of synchronization between the master device clock and the slave device clock, so avoid this when possible. In addition, monitoring of the bus state, such as for the presence of a start condition, is not possible during an IIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the IIC and internal resets, see section 31.15. State of Registers When Issuing Each Condition.

31.13 SMBus Operation

The IIC supports data communication conforming to the SMBus Specification (version 2.0). To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 to 100 kbps of the SMBus standard, set the CKS[2:0] bits in ICMR1, the ICBRH, and ICBRL registers. In addition, specify the values in the DLCS bit in ICMR2 and the SDDL[2:0] bits in ICMR2 to meet the data hold time specification of 300 ns or more. When the IIC is used only as a slave device, the transfer rate setting is not required, but ICBRL must be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the associated FS bit (7- or 10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).

在SCL时钟的一个周期内，CLO位自动设置为0。此时，如果ICCR2.BBSY=1，SCL引脚变为低电平，当ICCR2.BBSY=0时，SCL引脚变为高电平。通过软件确认CLO位为0后，向CLO位写入1以连续输出附加时钟。

当IIC模块处于主模式且从设备保持SDAn线为低电平时，由于噪声等影响与从设备失去同步，因此无法输出停止条件。该功能可用于逐个输出额外的SCL周期，使从设备释放SDAn线的低电平状态，从而将总线从不可用状态恢复。从设备释放SDAn线可以通过读取ICCR1中的SDAI位来监控。从设备确认SDAn线的释放后，通过重新发出停止条件完成通信。

[使用ICCR1中CLO位的输出条件]

●当总线打开（ICCR2中的BBSY标志=0）或主机模式（ICCR2中的MST位=1和BBSY标志=1）时

●当通信设备不保持SCLn线为低电平时。

图31.49显示了额外SCL时钟周期输出功能（CLO位）的操作时序。

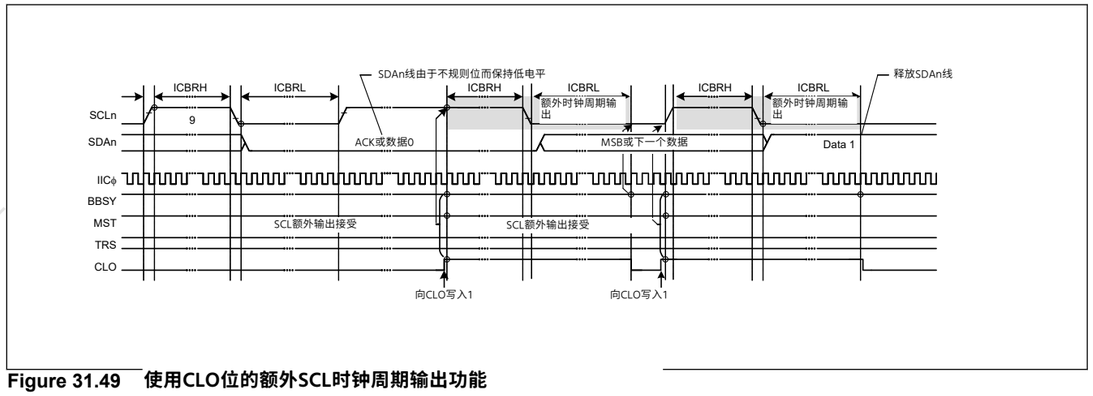

Figure 31.49 使用CLO位的额外SCL时钟周期输出功能

31.12.3 IIC复位和内部复位

IIC模块包含一个自我复位功能。它使用两种类型的重置：

●IIC复位，初始化所有寄存器，包括ICCR2中的BBSY标志。

●内部复位，将IIC从从地址匹配状态释放并初始化内部计数器，同时保存其他设置。

发出复位后，始终将ICCR1中的IICRST位设置为0。两种类型的复位都对从总线挂起状态释放有效，因为两者都将SCLn和SDAn引脚的输出状态恢复为高阻状态。

在从机操作期间发出复位可能会导致主设备时钟和从设备时钟之间失去同步，因此请尽可能避免这种情况。此外，在IIC复位（ICE和IICRST位=ICCR1中的01b）期间无法监控总线状态，例如是否存在启动条件。

有关IIC和内部复位的详细说明，请参见第31.15节。发出每个条件时的寄存器状态。

31.13 SMBus Operation

IIC支持符合SMBus规范（2.0版）的数据通信。要执行SMBus通信，请将ICMR3中的SMBS位设置为1。要使用SMBus标准的10至100kbps范围内的传输速率，请设置ICMR1、ICBRH和ICBRL寄存器中的CKS[2:0]位.此外，请指定ICMR2中的DLCS位和ICMR2中的SDDL[2:0]位中的值，以满足300ns或更长的数据保持时间规范。当IIC仅用作从设备时，不需要设置传输速率，但必须将ICBRL设置为比数据建立时间（250ns）更长的值。

对于SMBus器件默认地址(1100001b)，使用从地址寄存器L0到L2之一（SARL0、SARL1和SARL2），并将SARUy(y=0to2)中相关的FS位（7位或10位地址格式选择）设置为0（7位地址格式）。

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When transmitting the UDID (Unique Device Identifier), set the SALE bit in ICFER to 1 to enable the slave arbitration-lost detection function.

31.13.1 SMBus Timeout Measurement

(1) Measuring slave device timeout

The following period (timeout interval: $T_{LOW: SEXT}$) must be measured for slave devices in SMBus communication:

- From start condition to stop condition.

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the GPT using the IIC start condition detection interrupt (STIn) and stop condition detection interrupt (SPIn). The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW: SEXT}$: 25 ms (maximum) of the SMBus standard.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the slave device must release the bus by writing 1 to the IICRST bit in ICCR1 to issue an internal reset of the IIC. When an internal reset is issued, the IIC stops driving the bus for the SCLn and SDAn pins, making them output high-impedance, which releases the bus.

(2) Measuring master device timeout

The following periods (timeout interval: $T_{LOW: MEXT}$) must be measured for master devices in SMBus communication:

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition.

To measure timeout for master devices, measure these periods with the GPT using the IIC start condition detection interrupt (STIn), stop condition detection interrupt (SPIn), transmit end interrupt (IICn_TEI), or receive data full interrupt (IICn_RXI). The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard, and the total of all $T_{LOW: MEXT}$ values from start condition to stop condition must be within $T_{LOW: SEXT}$: 25 ms (maximum).

For the ACK receive timing (rising edge of the 9th SCL clock cycle), monitor the TEND flag in ICSR2 in master transmit mode (master transmitter) and the RDRF flag in ICSR2 in master receive mode (master receiver). Perform byte-wise transmit operations in master transmit mode, and hold the RDRFS bit in ICMR3 at 0 until the byte immediately before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 on the rising edge of the 9th SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (stop writing data to ICDRT).

发送UDID（UniqueDeviceIdentifier）时，将ICFER中的SALE位设置为1，以使能从机仲裁丢失检测功能。

31.13.1 SMBus超时测量

(1) 测量从设备超时

对于SMBus通信中的从设备，必须测量以下周期（超时间隔：TLOW:SEXT）：

●从开始条件到停止条件。

要测量从设备的超时，请使用GPT使用IIC启动条件检测中断(STIn)和停止条件检测中断(SPIn)测量从启动条件检测到停止条件检测的周期。测得的超时周期必须在总时钟低电平周期[从设备]TLOW:SEXT:SMBus标准的25ms（最大值）内。

如果用GPT测量的时间超过时钟低电平检测超时TTIMEOUT:25ms（最小值）
SMBus标准，从设备必须通过向ICCR1中的IICRST位写入1来释放总线，以发出IIC的内部复位。当发出内部复位时，IIC停止驱动SCLn和SDAn引脚的总线，使它们输出高阻抗，从而释放总线。

(2) 测量主设备超时

对于SMBus通信中的主设备，必须测量以下周期（超时间隔：TLOW:MEXT）：

●从开始条件到确认位
●确认位之间
●从确认位到停止条件。

要测量主设备的超时，请使用GPT使用IIC开始条件检测中断(STIn)、停止条件检测中断(SPIn)、发送结束中断(IICn_TEI)或接收数据完整中断(IICn_RXI)来测量这些周期。测量的超时周期必须在总时钟低电平扩展周期（主设备）TLOW内：

MEXT：SMBus标准的10毫秒（最大值），从开始条件到停止条件的所有TLOW：MEXT值的总和必须在TLOW：SEXT：25毫秒（最大值）内。

对于ACK接收时序（第9个SCL时钟周期的上升沿），在主机发送模式（主机发送器）下监控ICSR2中的TEND标志，在主机接收模式（主机接收器）下监控ICSR2中的RDRF标志。在主机发送模式下执行逐字节发送操作，并将ICMR3中的RDRFS位保持为0，直到在主机接收模式下接收到最后一个字节之前的字节。当RDRFS位为0时，RDRF标志在第9个SCL时钟周期的上升沿设置为1。

如果用GPT测量的周期超过总时钟低电平延长周期（主设备）TLOW:MEXT:SMBus标准的10ms（最大值）或总测量周期超过时钟低电平检测超时TTIMEOUT：SMBus标准的25ms（最小值），主设备必须通过发出停止条件来停止事务。在主机发送模式下，立即停止发送操作（停止向ICDRT写入数据）。

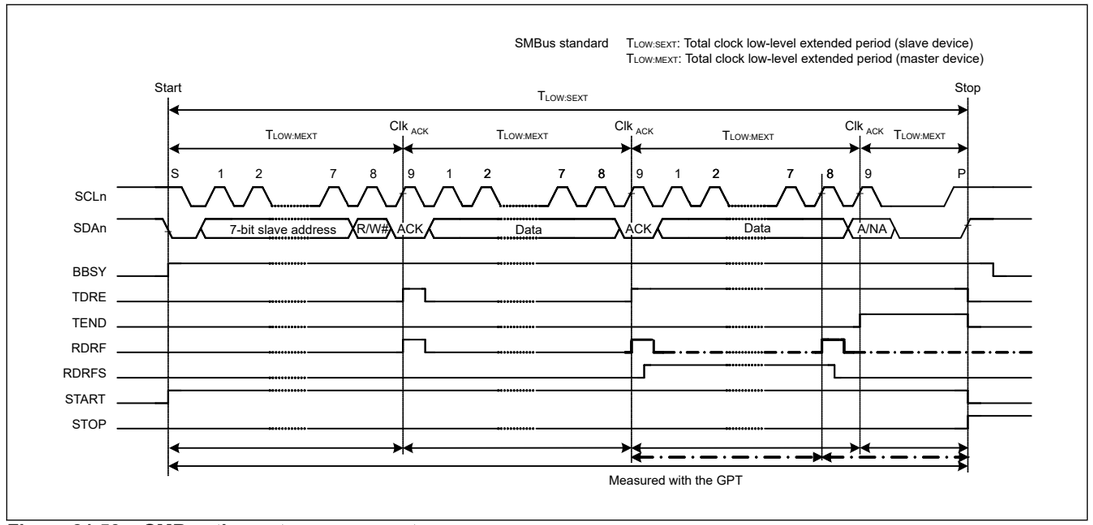

Figure 31.50 SMBus timeout measurement

31.13.2 Packet Error Code (PEC)

The MCU provides a CRC calculator that enables transmission of a Packet Error Code (PEC) or allows checking of the received data in SMBus data communication for the IIC. For the CRC-generating polynomials of the CRC calculator, see section 40, Cyclic Redundancy Check (CRC).

In master transmit mode, the PEC data can be generated by writing all transmit data to the CRC Data Input Register (CRCDIR) in the CRC calculator.

In master receive mode, the PEC data can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC Data Output Register (CRCDOR) with the received PEC data.

To send ACK or NACK based on the match or mismatch result when the final byte is received as a result of the PEC code check, set the RDRFS bit in ICMR3 to 1 before the rising edge of the 8th SCL clock cycle during reception of the final byte, and hold the SCLn line low on the falling edge of the 8th clock cycle.

31.13.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communicating over an SMBus, a slave device can temporarily act as a master device to notify the SMBus host (or ARP master) of its own slave address, or to request its own slave address from the SMBus host.

For a product using the MCU to operate as an SMBus host or ARP master, the host address (0001 000b) sent from the slave device must be detected as a slave address, and so the IIC provides a function for detecting the host address. To detect the host address as a slave address, set the SMBS bit in ICMR3 and the HOAE bit in ICSER to 1. Operation after the host address is detected is the same as normal slave operation.

31.14 Interrupt Sources

The IIC issues five types of interrupt requests:

- Transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection)
- Receive data full
- Transmit data empty
- Transmit end
- Address match during wakeup function

Table 31.10 lists details about the interrupt requests. The receive data full and transmit data empty interrupts can activate data transfer by the DTC or DMAC.

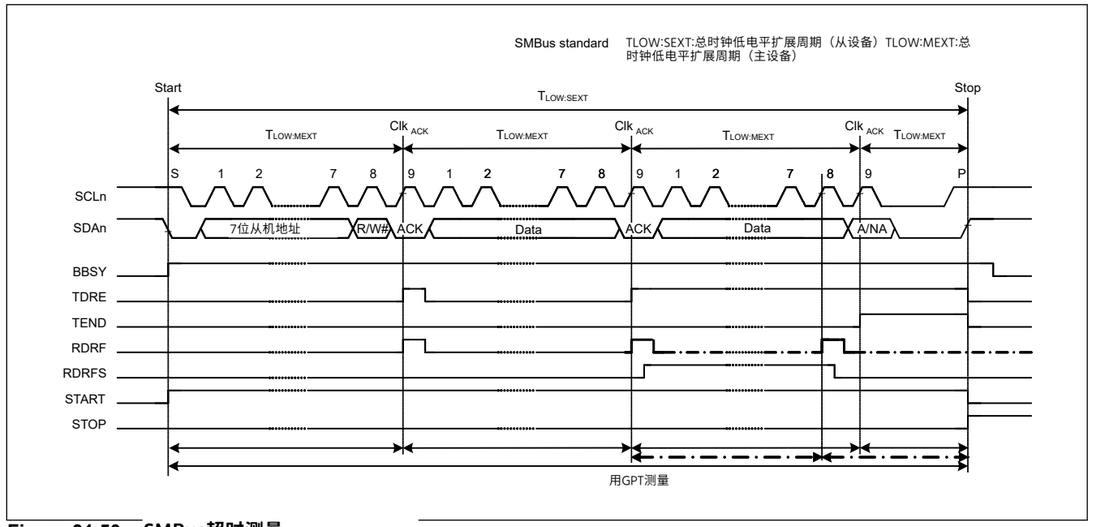

Figure 31.50 SMBus超时测量

31.13.2 数据包错误代码(PEC)

MCU提供了一个CRC计算器，可以传输数据包错误代码(PEC)或检查IIC的SMBus数据通信中接收到的数据。有关CRC计算器的CRC生成多项式，请参阅第40节，循环冗余校验(CRC)。

在主机发送模式下，可以通过将所有发送数据写入CRC计算器中的CRC数据输入寄存器(CRCDIR)来生成PEC数据。

在主机接收模式下，可以通过将所有接收数据写入CRC计算器中的CRCDIR并将获得的CRC数据输出寄存器(CRCDOR)中的值与接收到的PEC数据进行比较来检查PEC数据。

当作为PEC代码检查的结果接收到最后一个字节时，要根据匹配或不匹配结果发送ACK或NACK，请在接收最后一个字节期间的第8个SCL时钟周期的上升沿之前将ICMR3中的RDRFS位设置为1字节，并在第8个时钟周期的下降沿保持SCLn线为低电平。

31.13.3 SMBus主机通知协议（通知ARP主机命令）

在通过SMBus进行通信时，从设备可以临时充当主设备来通知SMBus主机（或ARP主机）它自己的从地址，或者从SMBus主机请求它自己的从地址。

对于使用MCU作为SMBus主机或ARP主机的产品，从机发送的主机地址（0001000b）必须被检测为从机地址，因此IIC提供了主机地址检测功能。要将主机地址检测为从机地址，请将ICMR3中的SMBS位和ICSER中的HOAE位设置为1。检测到主机地址后的操作与正常从机操作相同。

31.14 中断源

IIC发出五种类型的中断请求：

- 传输错误或事件发生（仲裁丢失、NACK检测、超时检测、开始条件检测和停止条件检测）
- 接收数据已满
- 传输数据为空
- 发送端
- 唤醒功能期间的地址匹配

表31.10列出了有关中断请求的详细信息。接收数据满和发送数据空中断可以通过DTC或DMAC激活数据传输。

Table 31.10 Interrupt sources

Symbol	Interrupt source	Interrupt flag	DTC or DMAC activation	Interrupt condition
IICn_EEI*5	Transfer error or event occurrence	AL	Not possible	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2 *5	Receive data full	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1 *5	Transmit data empty	RDRF	Possible	TDRE = 1, TIE = 1
IICn_TEI*3 *5	Transmit end	TEND	Not possible	TEND = 1, TEIE = 1
IIC0_WUI*4	Slave address match during wakeup function	WUF	Not possible	Slave address match Slave receive complete RWAK operation ASY0 = 1 WUIE = 1

Note: There is a delay between the execution of a write instruction for a peripheral module by the CPU and the actual writing to the module. When an interrupt flag is cleared or masked, read the relevant flag again to check whether clearing or masking is complete, then return from interrupt handling. Not doing so creates the possibility of repeated processing of the same interrupt.

Note 1. Because IICn_TXI is edge-detected, it does not require clearing. Additionally, the TDRE flag in ICSR2 (condition for IICn_TXI) is automatically set to 0 when transmit data is written to the ICDRT register or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 2. Because IICn_RXI is edge-detected, it does not require clearing. Additionally, the RDRF flag in ICSR2 (condition for IICn_RXI) is automatically set to 0 when data is read from ICDRR.

Note 3. When using the IICn_TEI interrupt, clear the TEND flag in ICSR2 in the IICn_TEI interrupt handling. The TEND flag in ICSR2 automatically is set to 0 when transmit data is written to the ICDRT register or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 4. Only channel 0 has a wakeup function, so IIC0_WUI is for channel 0 only.

Note 5. Channel number (n = 0 to 2).

Clear or mask each flag during interrupt handling.

31.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts

If the conditions for generating an IICn_TXI or IICn_RXI interrupt are satisfied while the associated IR flag is 1, the interrupt request is not output for the ICU but is saved internally. One request per source can be saved internally.

An interrupt request that is saved in the ICU is output when the ICU.IELSRn.IR flag becomes 0. Internally saved interrupt requests are automatically cleared under normal conditions. They can also be cleared by writing 0 to the interrupt enable bit within the associated peripheral module.

31.15 State of Registers When Issuing Each Condition

The IIC has two dedicated resets, IIC reset and Internal reset. Table 31.11 lists the registers states when issuing each condition.

Table 31.11 Register states when issuing each condition (1 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	In reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		In reset	In reset		
	Others			Saved		
ICCR2	BBSY	In reset	In reset	Saved	Set	In reset
	ST, RS			In reset	In reset	Saved
	SP					In reset
	TRS				Set or saved	
	MST					

Table 31.10 中断源

Symbol	中断源	中断标志	DTC或DMAC激活	中断条件
IICn_EEI*5	传输错误或事件发生	AL	不可能	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2 *5	接收数据已满	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1 *5	传输数据为空	RDRF	Possible	TDRE = 1, TIE = 1
IICn_TEI*3 *5	发射端	TEND	不可能	TEND = 1, TEIE = 1
IIC0_WUI*4	唤醒功能期间的从机地址匹配	WUF	不可能	从地址匹配 从机接收完成 RWAK operation ASY0 = 1 WUIE = 1

Note: CPU执行外围模块的写指令与实际写入模块之间存在延迟。当一个中断标志被清除或屏蔽时，再次读取相关标志，检查清除或屏蔽是否完成，然后从中断处理返回。不这样做会产生重复处理同一中断的可能性。

注1.因为IICn_TXI是边沿检测，所以不需要清零。此外，当发送数据写入ICDRT寄存器或检测到停止条件（ICSR2中的STOP标志=1）时，ICSR2中的TDRE标志（IICn_TXI的条件）自动设置为0。

注2.因为IICn_RXI是边沿检测，所以不需要清零。此外，从ICDRR读取数据时，ICSR2中的RDRF标志（IICn_RXI的条件）自动设置为0。

注3.使用IICn_TEI中断时，在IICn_TEI中断处理中清除ICSR2中的TEND标志。当发送数据写入ICDRT寄存器或检测到停止条件（ICSR2中的STOP标志=1）时，ICSR2中的TEND标志自动设置为0。

注4.只有通道0有唤醒功能，所以IIC0_WUI仅适用于通道0。

注5.通道编号（n=0至2）。

在中断处理期间清除或屏蔽每个标志。

31.14.1 IICn_TXI和IICn_RXI中断的缓冲区操作

如果在相关的IR标志为1时满足产生IICn_TXI或IICn_RXI中断的条件，则中断请求不会输出给ICU，而是在内部保存。每个源的一个请求可以在内部保存。

当ICU.IELSRn.IR标志变为0时，输出ICU中保存的中断请求。在正常情况下，内部保存的中断请求会自动清除。它们也可以通过向相关外围模块中的中断使能位写入0来清除。

31.15 发布每个条件时的寄存器状态

IIC有两个专用复位，IIC复位和内部复位。表31.11列出了发出每个条件时的寄存器状态。

Table 31.11 发出每个条件时注册状态（2个中的1个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICCR1	ICE, IICRST	复位中	Saved	Saved	Saved	Saved
	SCLO, SDAO		复位中	复位中		
	Others			Saved		
ICCR2	BBSY	复位中	复位中	Saved	Set	复位中
	ST, RS			复位中	复位中	Saved
	SP					复位中
	TRS				设置或保存	
	MST					

Table 31.11 Register states when issuing each condition (2 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICMR1	BC[2:0]	In reset	In reset	In reset	In reset	Saved
	Others			Saved	Saved	
ICMR2		In reset	In reset	Saved	Saved	Saved
ICMR3	ACKBT	In reset	In reset	Saved	Saved	In reset
	Others					Saved
ICFER		In reset	In reset	Saved	Saved	Saved
ICSER		In reset	In reset	Saved	Saved	Saved
ICIER		In reset	In reset	Saved	Saved	Saved
ICSR1		In reset	In reset	In reset	Saved	In reset
ICSR2	TEND	In reset	In reset	In reset	Saved	In reset
	TDRE				Set or saved	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		In reset	In reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		In reset	In reset	Saved	Saved	Saved
ICBRH, ICBRL		In reset	In reset	Saved	Saved	Saved
ICDRT		In reset	In reset	Saved	Saved	Saved
ICDRR		In reset	In reset	Saved	Saved	Saved
ICDRS		In reset	In reset	In reset	Saved	Saved
Timeout function		In reset	In reset	In reset	Operating	Operating
Bus free time measurement		In reset	In reset	Operating	Operating	Operating
ICWUR2	WUSEN	In reset	In reset	Saved	Saved	Saved
	Others					Saved or set or reset

31.16 Event Link Output

The IIC0 module handles the event output for the Event Link Controller (ELC) for the following sources:

(1) Transfer error event

When a transfer error event occurs, the associated event signal can be output to another module by the ELC.

(2) Receive data full

When a receive data register becomes full, the associated event signal can be output to another module by the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the associated event signal can be output to another module by the ELC.

(4) Transmit end

On completion of the transfer, the associated event signal can be output to another module by the ELC.

31.16.1 Interrupt Handling and Event Linking

Each of the IIC interrupt types (see Table 31.10) has an enable bit to control enabling and disabling of the associated interrupt signal. An interrupt request signal is output to the CPU when an interrupt source condition is satisfied while the associated enable bit is set.

Table 31.11 发布每个条件时注册状态（2个中的2个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICMR1	BC[2:0]	复位中	复位中	复位中	复位中	Saved
	Others			Saved	Saved	
ICMR2		复位中	复位中	Saved	Saved	Saved
ICMR3	ACKBT	复位中	复位中	Saved	Saved	复位中
	Others					Saved
ICFER		复位中	复位中	Saved	Saved	Saved
ICSER		复位中	复位中	Saved	Saved	Saved
ICIER		复位中	复位中	Saved	Saved	Saved
ICSR1		复位中	复位中	复位中	Saved	复位中
ICSR2	TEND	复位中	复位中	复位中	Saved	复位中
	TDRE				设置或保存	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		复位中	复位中	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		复位中	复位中	Saved	Saved	Saved
ICBRH, ICBRL		复位中	复位中	Saved	Saved	Saved
ICDRT		复位中	复位中	Saved	Saved	Saved
ICDRR		复位中	复位中	Saved	Saved	Saved
ICDRS		复位中	复位中	复位中	Saved	Saved
超时功能		复位中	复位中	复位中	Operating	Operating
公交车空闲时间测量		复位中	复位中	Operating	Operating	Operating
ICWUR2	WUSEN	复位中	复位中	Saved	Saved	Saved
	Others					保存或设置或重置

31.16 事件链接输出

IIC0模块为以下源处理事件链接控制器(ELC)的事件输出：

(1) 传输错误事件

当发生传输错误事件时，ELC可以将相关事件信号输出到另一个模块。

(2) 接收数据已满

当接收数据寄存器变满时，ELC可以将相关的事件信号输出到另一个模块。

(3) 传输数据为空

当发送数据寄存器变为空时，ELC可以将相关的事件信号输出到另一个模块。

(4) 发射端

传输完成后，ELC可以将相关的事件信号输出到另一个模块。

31.16.1 中断处理和事件链接

每种IIC中断类型（见表31.10）都有一个启用位来控制相关中断信号的启用和禁用。当相关的使能位设置时，中断源条件成立时，将向CPU输出中断请求信号。

The associated event link output signals are sent to other modules as event signals by the ELC when the interrupt source conditions are satisfied, regardless of the interrupt enable bit settings. For details on interrupt sources, see Table 31.10.

31.17 Usage Notes

31.17.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable IIC operation. The IIC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

31.17.2 Notes on Starting Transfer

If the IR flag associated with the IIC interrupt is 1 when transfer is started (ICCR1.ICE bit = 1), follow the procedure in this section to clear the interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unexpected behavior of the IR flag.

To clear interrupts before starting transfer operation:

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits, such as ICIER.TIE to 0.
3. Read the relevant interrupt enable bits, such as ICIER.TIE, and confirm that the value is 0.
4. Set the IR flag to 0.

当满足中断源条件时，ELC将关联的事件链接输出信号作为事件信号发送到其他模块，而不管中断使能位设置如何。有关中断源的详细信息，请参见表31.10。

31.17 使用说明

31.17.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用IIC操作。IIC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

31.17.2 开始转移注意事项

如果在传输开始时与IIC中断相关的IR标志为1（ICCR1.ICE位=1），请按照本节中的步骤在使能操作之前清除中断。在ICCR1.ICE位为1时将IR标志设置为1开始传输会导致在传输开始后内部保存中断请求，这可能导致IR标志的意外行为。

在开始传输操作之前清除中断：

1.确认ICCR1.ICE位为0。

2.设置相关的中断使能位，如ICIER.TIE为0。

3、读取相关的中断使能位，如ICIER.TIE，确认值为0。

4.将IR标志设置为0。

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32. CAN-FD

32.1 Overview

The Controller Area Network-Flexible Data (CAN-FD) module supports the following functions:

- Multiple channel operation
- Gateway function
- CAN with Flexible Data rate.*1

Note 1. This feature is not available in the classical CAN function.

The CAN-FD module has a flexible message buffer and FIFO structure that meet the requirements of various applications. It also provides test modes to achieve high testability of the module that can be useful for power-on testing.

This specification describes a 2 channel implementation of the CAN-FD module.

The CAN-FD mode is only available in certain products that support it.

32.1.1 CAN-FD Module

Table 32.1 CAN-FD module specifications (1 of 2)

Parameter	Specifications
Communication	CAN functionality conforms to CAN-FD ISO 11898-1 (2015)
Gateway function	CAN 2.0 ↔ CAN 2.0 CAN 2.0 ↔ CAN-FD gateway (only 8-byte payload)*1 CAN-FD ↔ CAN-FD*1
Data transfer rate	Up to 1 Mbps for arbitration phase and up to 8 Mbps for data phase, individually for each CAN channel
Operation frequency Peripheral clock/APB clock	50 MHz (PCLKB) RAM clock: 100 MHz (PCLKA)
Data Link Layer (DLL) clock	Max ≤ 40 MHz
Input/Output pins	TX/RX
CAN channels	2 channels
Selectable ID type	11-bit Standard ID
	11-bit Standard ID + 18-bit Extended ID
Selectable frame type	Data frame (RTR = 0) (CAN and CAN-FD frames)
	Remote frame (RTR = 1) (only CAN frames)
Variable data byte count for data frames	DLC range: 0 to F
Message buffer	Up to 16 × 2 reception message buffers, shared among all the CAN channels
	16 transmit message buffers per channel
	4 transmission queues per channel Automatic message transfer into transmission queues supported
FIFO number	8 reception FIFO buffers Up to 3 × 2 FIFOs individually configurable as: ● Reception FIFO ● Transmission FIFO ● CAN-to-CAN Gateway FIFO
Automatic delay interval timer for transmission	The delay timer can be applied to: ● Transmission FIFO ● CAN-to-CAN Gateway FIFO

32. CAN-FD

32.1 Overview

控制器局域网灵活数据(CAN-FD)模块支持以下功能：

●多通道操作

●网关功能

●具有灵活数据速率的CAN。*1

注1.此功能在经典CAN功能中不可用。

CAN-FD模块具有灵活的报文缓冲区和FIFO结构，可满足各种应用的要求。它还提供了测试模式来实现模块的高可测试性，这对于上电测试很有用。

本规范描述了CAN-FD模块的2通道实现。

CAN-FD模式仅在支持它的某些产品中可用。

32.1.1 CAN-FD Module

Table 32.1 CAN-FD模块规格(1of2)

Parameter	Specifications
Communication	CAN功能符合CAN-FDISO11898-1(2015)
网关功能	CAN 2.0 ↔ CAN 2.0 CAN2.0↔CAN-FD网关（仅8字节有效负载）*1 CAN-FD ↔ CAN-FD*1
数据传输率	仲裁阶段高达1Mbps，数据阶段高达8Mbps，每个CAN通道单独
运行频率 外设时钟APB时钟	50 MHz (PCLKB) RAM clock: 100 MHz (PCLKA)
数据链路层(DLL)时钟	Max ≤ 40 MHz
Input/Output pins	TX/RX
CAN通道	2 channels
可选择的ID类型	11位标准ID
	11位标准ID+18位扩展ID
可选择的框架类型	数据帧(RTR=0)（CAN和CAN-FD帧）
	远程帧(RTR=1)（仅限CAN帧）
数据帧的可变数据字节数	DLC range: 0 to F
消息缓冲区	多达16×2个接收消息缓冲区，在所有CAN通道之间共享
	每个通道16个传输消息缓冲区
	每个通道4个传输队列支持自动将消息传输到传输队列
FIFO number	8个接收FIFO缓冲区最多3×2个FIFO，可单独配置为：● ● Transmission FIFO ● CAN-to-CAN Gateway FIFO
传输的自动延迟间隔定时器	延时定时器可应用于：● ● CAN-to-CAN Gateway FIFO

Table 32.1 CAN-FD module specifications (2 of 2)

Parameter	Specifications
Enhanced reception filtering	Support of 11 bits and 29 bits CAN identifier
	Programmable 29 bits CAN identifier acceptance filter mask for each entry
	Programmable gateway routing capability for each channel (up to 8 routing destinations)
	RTR and IDE masking
	Data Length Code (DLC) filter
	Message buffer payload overload protection
	Payload filter
	Updating Acceptance Filter List (AFL) entry during communication
General software support	Automatic label information added to receive message (for upper software layer support)
Timer	TX and RX Timestamp function
Power down function	Module start stop function for each CAN node (Channel and Global Sleep modes)
RAM	RAM ECC protected (2 bits error detection, 1-bit error correction)
Bus traffic measurement	CAN bus traffic measurement of each channel is possible
TrustZone Filter	One security attribution can be set, and the attribution of the two channels are the same

Note 1. This feature is not available in the classical CAN function.

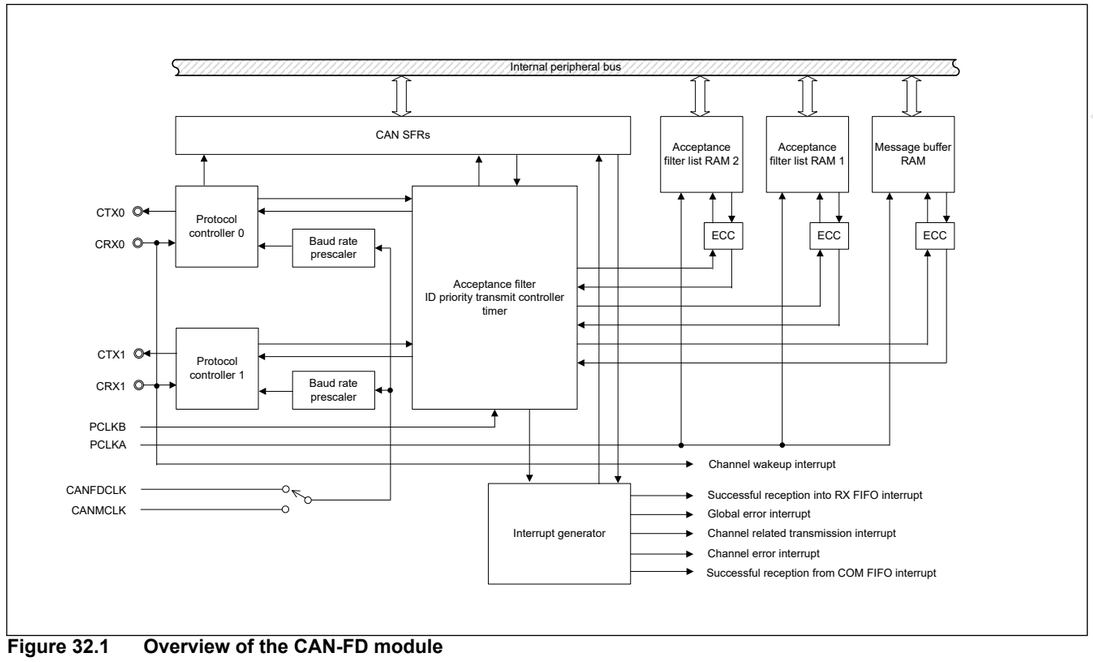

Figure 32.1 Overview of the CAN-FD module

- TX/RX:
  Input/Output, CRXn/CTXn, pins of the CAN module
- Protocol controller:
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, error handling

Table 32.1 CAN-FD模块规格（2之2）

Parameter	Specifications
增强的接收过滤	支持11位和29位CAN标识符
	每个条目的可编程29位CAN标识符接受过滤器掩码
	每个通道的可编程网关路由功能（最多8个路由目的地）
	RTR和IDE掩码
	数据长度代码(DLC)过滤器
	消息缓冲区负载过载保护
	有效负载过滤器
	在通信期间更新接受过滤器列表(AFL)条目
通用软件支持	接收消息自动添加标签信息（用于上层软件层支持）
Timer	TX和RX时间戳功能
断电功能	每个CAN节点的模块启动停止功能（通道和全局睡眠模式）
RAM	RAMECC保护（2位错误检测，1位错误纠正）
公交车流量测量	可以对每个通道进行CAN总线流量测量
TrustZone Filter	可设置一个安全属性，两个通道的属性相同

注1.此功能在经典CAN功能中不可用。

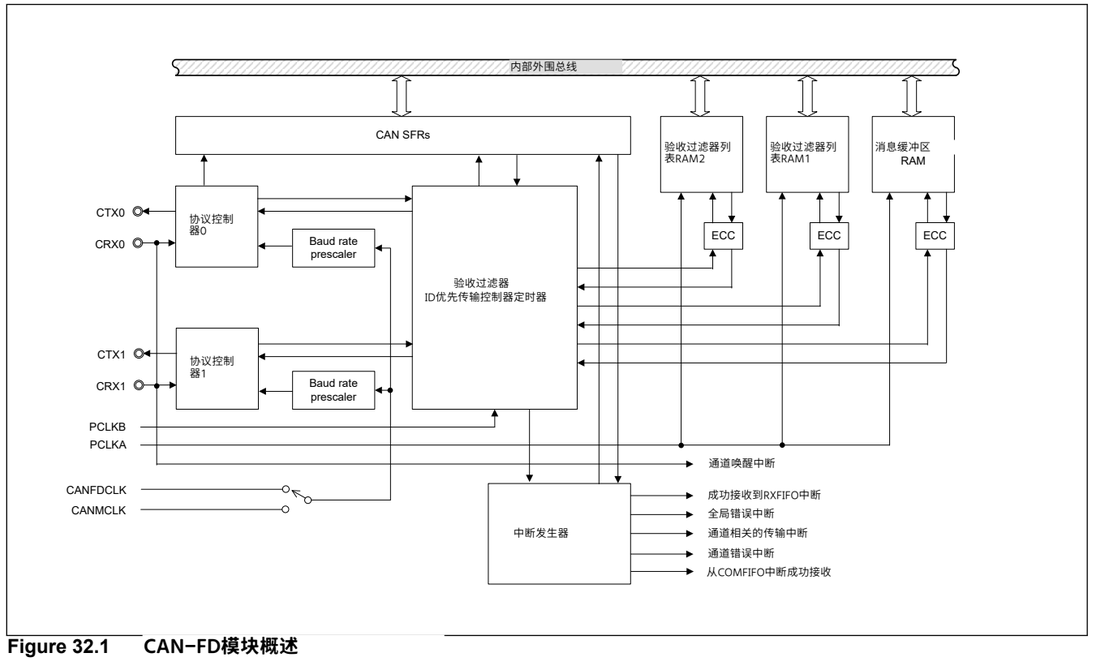

Figure 32.1 CAN-FD模块概述

- TX/RX:
  输入输出，CRXnCTXn，CAN模块的引脚
- Protocol controller:
  处理CAN协议处理，例如总线仲裁、发送和接收时的位时序、填充、错误处理

- Acceptance filter list RAM:
  This RAM is used to store the message acceptance filtering entries for all channels. Each acceptance filter entry has an individual ID, data length code, data field, message pointer for upper layer application usage and message direction pointer. The AFLRAM is divided in two parts to accelerate the Acceptance Filter List (AFL) access process.
- Message buffer RAM:
  This RAM is used to store messages after reception or for transmission using a normal message buffer or a FIFO. Each message entry has an individual ID, data length code, data field, message pointer for upper layer application usage and a time stamp.
- Acceptance filter:
  Performs filtering of received messages. The entries in the Acceptance filter list RAM are used for the filtering process.
- Two timers:
  - Reception Timestamp function
  - Transmission separation time for FIFO buffers
- Interrupt generator:
  Generates several types of global and channel interrupts
- CAN Special Function Registers (SFRs):
  Registers associated with CAN. See section 32.2.87. Message Buffer Component Structure.

32.2 Register Descriptions

32.2.1 Register Table

The reset value shown for the RAM area, consisting of CFDGAFLIDn, CFDGAFLMn, CFDGAFLP0n, CFDGAFLP1n, CFDRMBCPn, CFDRFMBCPn, CFDCFMBCPn, CFDTMBCPn, CFDTHLACC0n, CFDTHLACC1n and CFDRPGACCn is valid after initialization of a hardware reset. See section 32.4.2. CAN Module Configuration after Hardware Reset for details of the initialization process.

If a write access with a size of 8 or 16 bits is performed for the RAM area, then the CAN-FD module does a read-modify write-access to the RAM location, because the RAM requires a 32-bit access through the ECC module.

For single bit error, the correct data is written back. For multiple bit errors, unknown data is written back.

Do not access the space where the register is not assigned.

The read data from the space where the register is not assigned is unknown.

32.2.2 Legend

For all repetitive registers and bits, a lowercase index is used to indicate which slice is being referenced. If an index is being used, it is defined and described in the Register table it is being used in.

There is one global index used across all the registers and bits that need it.

Table 32.2 CANFD Registers (1 of 4)

Register name	Symbol	Reset value	Offset Address	Access size
Channel n Nominal Bitrate Configuration Register n	CFDCnNCFG	0x00000000	0x0000 + n × 0x0010	8, 16, 32
Channel n Control Registers	CFDCnCTR	0x00000005	0x0004 + n × 0x0010	8, 16, 32
Channel n Status Registers	CFDCnSTS	0x00000005	0x0008 + n × 0x0010	8, 16, 32
Channel n Error Flag Registers	CFDCnERFL	0x00000000	0x000C + n × 0x0010	8, 16, 32
Global Configuration Register	CFDGCFG	0x00000000	0x0084	8, 16, 32
Global Control Register	CFDGCTR	0x00000005	0x0088	8, 16, 32
Global Status Register	CFDGSTS	0x0000000D	0x008C	8, 16, 32
Global Error Flag Register	CFDGERFL	0x00000000	0x0090	8, 16, 32
Global Timestamp Counter Register	CFDGTSC	0x00000000	0x0094	16, 32

●验收过滤器列表RAM：
此RAM用于存储所有通道的消息接受过滤条目。每个接受过滤器条目都有一个单独的ID、数据长度代码、数据字段、供上层应用程序使用的消息指针和消息方向指针。AFLRAM分为两部分以加速接受过滤器列表(AFL)访问过程。

●消息缓冲区RAM：
此RAM用于在接收后存储消息或使用普通消息缓冲区或FIFO进行传输。每个消息条目都有一个单独的ID、数据长度代码、数据字段、供上层应用程序使用的消息指针和时间戳。

- Acceptance filter:
  对收到的消息执行过滤。接受过滤器列表RAM中的条目用于过滤过程。
- Two timers:
  -接收时间戳功能
  FIFO缓冲区的传输分离时间
- Interrupt generator:
  生成多种类型的全局和通道中断

●CAN特殊功能寄存器(SFR)：
与CAN相关的寄存器。请参阅第32.2.87节。消息缓冲区组件结构。

32.2 注册说明

32.2.1 寄存器表

RAM区域的复位值，包括CFDGAFLIDn、CFDGAFLMn、CFDGAFLP0n、CFDGAFLP1n、CFDRMBCPn、CFDRFMBCPn、CFDCMBCPn、CFDTMBCPn、CFDTHLACC0n、CFDTHLACC1n和CFDRPGACCn，在硬件复位初始化后有效。请参见第32.4.2节。有关初始化过程的详细信息，请参阅硬件复位后的CAN模块配置。

如果对RAM区域执行8位或16位大小的写访问，则CAN-FD模块会对RAM位置执行读修改写访问，因为RAM需要通过ECC进行32位访问模块。

对于单位错误，正确的数据被写回。对于多位错误，将写回未知数据。

不要访问未分配寄存器的空间。

从未分配寄存器的空间读取的数据是未知的。

32.2.2 Legend

对于所有重复的寄存器和位，小写索引用于指示正　　在引用哪个切片。如果正在使用索引，则在使用它的寄存器表中对其进行定义和描述。

所有需要它的寄存器和位都使用一个全局索引。

Table 32.2 CANFD寄存器(1of4)

注册名称	Symbol	重置值	偏移地址	访问大小
通道n标称比特率配置 Register n	CFDCnNCFG	0x00000000	0x0000 + n × 0x0010	8, 16, 32
通道n控制寄存器	CFDCnCTR	0x00000005	0x0004 + n × 0x0010	8, 16, 32
通道n状态寄存器	CFDCnSTS	0x00000005	0x0008 + n × 0x0010	8, 16, 32
通道n错误标志寄存器	CFDCnERFL	0x00000000	0x000C + n × 0x0010	8, 16, 32
全局配置寄存器	CFDGCFG	0x00000000	0x0084	8, 16, 32
全局控制寄存器	CFDGCTR	0x00000005	0x0088	8, 16, 32
全局状态寄存器	CFDGSTS	0x0000000D	0x008C	8, 16, 32
全局错误标志寄存器	CFDGERFL	0x00000000	0x0090	8, 16, 32
全局时间戳计数器寄存器	CFDGTSC	0x00000000	0x0094	16, 32

Table 32.2 CANFD Registers (2 of 4)

Register name	Symbol	Reset value	Offset Address	Access size
Global Acceptance Filter List Entry Control Register	CFDGAFLECTR	0x00000000	0x0098	8, 16, 32
Global Acceptance Filter List Configuration Register n	CFDGAFLCFG0	0x00000000	0x009C	8, 16, 32
RX Message Buffer Number Register	CFDRMNB	0x00000000	0x00AC	8, 16, 32
RX Message Buffer New Data Register n	CFDRMNDn	0x00000000	0x00B0 + n × 0x0004	8, 16, 32
RX FIFO Configuration/Control Registers n	CFDRFCCn	0x00000000	0x00C0 + n × 0x0004	8, 16, 32
RX FIFO Status Registers n	CFDRFSTSn	0x00000001	0x00E0 + n × 0x0004	8, 16, 32
RX FIFO Pointer Control Registers n	CFDRFPCTRn	0x00000000	0x0100 + n × 0x0004	8, 16, 32
Common FIFO Configuration/Control Registers n	CFDCFCCn	0x00000000	0x0120 + n × 0x0004	8, 16, 32
Common FIFO Configuration/Control Enhancement Registers n	CFDCFCCEn	0x00000000	0x0180 + n × 0x0004	8, 16, 32
Common FIFO Status Registers n	CFDCFSTSn	0x00000001	0x01E0 + n × 0x0004	8, 16, 32
Common FIFO Pointer Control Registers n	CFDCFPCTRn	0x00000000	0x0240 + n × 0x0004	8, 16, 32
FIFO Empty Status Register	CFDFESTS	0x00003FFF	0x02A0	8, 16, 32
FIFO Full Status Register	CFDFFSTS	0x00000000	0x02A4	8, 16, 32
FIFO Message Lost Status Register	CFDFMSTS	0x00000000	0x02A8	8, 16, 32
RX FIFO Interrupt Flag Status Register	CFDRFISTS	0x00000000	0x02AC	8, 16, 32
Common FIFO RX Interrupt Flag Status Register	CFDCFRISTS	0x00000000	0x02B0	8, 16, 32
Common FIFO TX Interrupt Flag Status Register	CFDCFTISTS	0x00000000	0x02B4	8, 16, 32
Common FIFO One Frame RX Interrupt Flag Status Register	CFDCFOFRISTS	0x00000000	0x02B8	8, 16, 32
Common FIFO One Frame TX Interrupt Flag Status Register	CFDCFOFTISTS	0x00000000	0x02BC	8, 16, 32
Common FIFO Message Over Write Status Register	CFDCFMOWSTS	0x00000000	0x02C0	8, 16, 32
FIFO FDC Full Status Register	CFDFFFSTS	0x00000000	0x02C4	8, 16, 32
TX Message Buffer Control Registers n	CFDTMCn	0x00	0x02D0 + n × 0x0001	8
TX Message Buffer Status Registers n	CFDTMSTSn	0x00	0x07D0 + n × 0x0001	8
TX Message Buffer Transmission Request Status Register f	CFDTMTRSTSf	0x00000000	0x0CD0 + f × 0x0004	8, 16, 32
TX Message Buffer Transmission Abort Request Status Register f	CFDTMTARSTSf	0x00000000	0x0D70 + f × 0x0004	8, 16, 32
TX Message Buffer Transmission Completion Status Register f	CFDTMTCSTSf	0x00000000	0x0E10 + f × 0x0004	8, 16, 32
TX Message Buffer Transmission Abort Status Register f	CFDTMTASTSf	0x00000000	0x0EB0 + f × 0x0004	8, 16, 32
TX Message Buffer Interrupt Enable Configuration Register f	CFDTMIECf	0x00000000	0x0F50 + f × 0x0004	8, 16, 32
TX Queue Configuration/Control Registers 0 [n]	CFDTXQCC0n	0x00000000	0x1000 + n × 0x0004	8, 16, 32
TX Queue Status Registers 0 [n]	CFDTXQSTS0n	0x00000001	0x1020 + n × 0x0004	8, 16, 32
TX Queue Pointer Control Registers 0 [n]	CFDTXQPCTR0n	0x00000000	0x1040 + n × 0x0004	8, 16, 32

Table 32.2 CANFD寄存器(2of4)

注册名称	Symbol	重置值	偏移地址	访问大小
全局接受过滤器列表条目控制寄存器	CFDGAFLECTR	0x00000000	0x0098	8, 16, 32
全局接受过滤器列表配置寄存器n	CFDGAFLCFG0	0x00000000	0x009C	8, 16, 32
RX消息缓冲区编号寄存器	CFDRMNB	0x00000000	0x00AC	8, 16, 32
RX报文缓冲区新数据寄存器n	CFDRMNDn	0x00000000	0x00B0 + n × 0x0004	8, 16, 32
RX FIFO Configuration/Control Registers n	CFDRFCCn	0x00000000	0x00C0 + n × 0x0004	8, 16, 32
RXFIFO状态寄存器n	CFDRFSTSn	0x00000001	0x00E0 + n × 0x0004	8, 16, 32
RXFIFO指针控制寄存器n	CFDRFPCTRn	0x00000000	0x0100 + n × 0x0004	8, 16, 32
Common FIFO Configuration/Control Registers n	CFDCFCCn	0x00000000	0x0120 + n × 0x0004	8, 16, 32
Common FIFO Configuration/Control 增强寄存器n	CFDCFCCEn	0x00000000	0x0180 + n × 0x0004	8, 16, 32
通用FIFO状态寄存器n	CFDCFSTSn	0x00000001	0x01E0 + n × 0x0004	8, 16, 32
通用FIFO指针控制寄存器n	CFDCFPCTRn	0x00000000	0x0240 + n × 0x0004	8, 16, 32
FIFO空状态寄存器	CFDFESTS	0x00003FFF	0x02A0	8, 16, 32
FIFO满状态寄存器	CFDFFSTS	0x00000000	0x02A4	8, 16, 32
FIFO消息丢失状态寄存器	CFDFMSTS	0x00000000	0x02A8	8, 16, 32
RXFIFO中断标志 状态寄存器	CFDRFISTS	0x00000000	0x02AC	8, 16, 32
通用FIFORX中断标志 状态Register	CFDCFRISTS	0x00000000	0x02B0	8, 16, 32
通用FIFOTX中断标志 状态Register	CFDCFTISTS	0x00000000	0x02B4	8, 16, 32
通用FIFO一帧RX中断标志状态寄存器	CFDCFOFRISTS	0x00000000	0x02B8	8, 16, 32
通用FIFO一帧TX中断标志状态寄存器	CFDCFOFTISTS	0x00000000	0x02BC	8, 16, 32
通用FIFO消息覆盖状态寄存器	CFDCFMOWSTS	0x00000000	0x02C0	8, 16, 32
FIFOFDC满状态寄存器	CFDFFFSTS	0x00000000	0x02C4	8, 16, 32
TX报文缓冲区控制寄存器n	CFDTMCn	0x00	0x02D0 + n × 0x0001	8
TX报文缓冲区状态寄存器n	CFDTMSTSn	0x00	0x07D0 + n × 0x0001	8
TX消息缓冲区传输请求状态寄存器f	CFDTMTRSTSf	0x00000000	0x0CD0 + f × 0x0004	8, 16, 32
TX消息缓冲区传输中止请求状态寄存器f	CFDTMTARSTSf	0x00000000	0x0D70 + f × 0x0004	8, 16, 32
TX消息缓冲区传输完成状态寄存器f	CFDTMTCSTSf	0x00000000	0x0E10 + f × 0x0004	8, 16, 32
TX消息缓冲区传输中止状态寄存器f	CFDTMTASTSf	0x00000000	0x0EB0 + f × 0x0004	8, 16, 32
TX报文缓冲区中断使能配置寄存器f	CFDTMIECf	0x00000000	0x0F50 + f × 0x0004	8, 16, 32
TX Queue Configuration/Control Registers 0 [n]	CFDTXQCC0n	0x00000000	0x1000 + n × 0x0004	8, 16, 32
TX队列状态寄存器0[n]	CFDTXQSTS0n	0x00000001	0x1020 + n × 0x0004	8, 16, 32
TX队列指针控制寄存器0[n]	CFDTXQPCTR0n	0x00000000	0x1040 + n × 0x0004	8, 16, 32

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Table 32.2 CANFD Registers (3 of 4)

Register name	Symbol	Reset value	Offset Address	Access size
TX Queue Configuration/Control Registers 1 [n]	CFDTXQCC1n	0x00000000	0x1060 + n × 0x0004	8, 16, 32
TX Queue Status Registers 1 [n]	CFDTXQSTS1[n]	0x00000001	0x1080 + n × 0x0004	8, 16, 32
TX Queue Pointer Control Registers 1 [n]	CFDTXQPCTR1n	0x00000000	0x10A0 + n × 0x0004	8, 16, 32
TX Queue Configuration/Control Registers 2 [n]	CFDTXQCC2n	0x00000000	0x10C0 + n × 0x0004	8, 16, 32
TX Queue Status Registers 2 [n]	CFDTXQSTS2n	0x00000001	0x10E0 + n × 0x0004	8, 16, 32
TX Queue Pointer Control Registers 2 [n]	CFDTXQPCTR2n	0x00000000	0x1100 + n × 0x0004	8, 16, 32
TX Queue Configuration/Control Registers 3 [n]	CFDTXQCC3n	0x00000000	0x1120 + n × 0x0004	8, 16, 32
TX Queue Status Registers 3 [n]	CFDTXQSTS3n	0x00000001	0x1140 + n × 0x0004	8, 16, 32
TX Queue Pointer Control Registers 3 [n]	CFDTXQPCTR3n	0x00000000	0x1160 + n × 0x0004	8, 16, 32
TX Queue Empty Status Register	CFDTXQESTS	0x000000FF	0x1180	8, 16, 32
TX Queue Full Interrupt Status Register	CFDTXQFISTS	0x00000000	0x1184	8, 16, 32
TX Queue Message Lost Status Register	CFDTXQMSTS	0x00000000	0x1188	8, 16, 32
TX Queue Interrupt Status Register	CFDTXQISTS	0x00000000	0x1190	8, 16, 32
TX Queue One Frame TX Interrupt Status Register	CFDTXQOFTISTS	0x00000000	0x1194	8, 16, 32
TX Queue One Frame RX Interrupt Status Register	CFDTXQOFRISTS	0x00000000	0x1198	8, 16, 32
TX Queue Full Status Register	CFDTXQFSTS	0x00000000	0x119C	8, 16, 32
TX History List Configuration/Control Register n	CFDTHLCCn	0x00000000	0x1200 + n × 0x0004	8, 16, 32
TX History List Status Register n	CFDTHLSTSn	0x00000001	0x1220 + n × 0x0004	8, 16, 32
TX History List Pointer Control Registers n	CFDTHLPCTRn	0x00000000	0x1240 + n × 0x0004	8, 16, 32
Global TX Interrupt Status Register 0	CFDGTINTSTS0	0x00000000	0x1300	8, 16, 32
Global Test Configuration Register	CFDGTSTCFG	0x00000000	0x1308	8, 16, 32
Global Test Control Register	CFDGTSTCTR	0x00000000	0x130C	8, 16, 32
Global FD Configuration Register	CFDGFDCFG	0x00000000	0x1314	8, 16, 32
Global FD CRC Configuration Register	CFDGCRCCFG	0x00000000	0x1318	8, 16, 32
Global Lock Key Register	CFDGLOCKK	0x00000000	0x131C	16, 32
Global AFL Ignore Entry Register	CFDGAFLIGNENT	0x00000000	0x1324	8, 16, 32
Global AFL Ignore Control Register	CFDGAFLIGNCTR	0x00000000	0x1328	16, 32
DMA Transfer Control Register	CFDCDTCT	0x00000000	0x1330	8, 16, 32
DMA Transfer Status Register	CFDCDTSTS	0x00000000	0x1334	8, 16, 32
DMA TX Transfer Control Register	CFDCDTTCT	0x00000000	0x1340	8, 16, 32
DMA TX Transfer Status Register	CFDCDTTSTS	0x00000000	0x1344	8, 16, 32
Global RX Interrupt Status Register n	CFDGRINTSTSn	0x00000000	0x1350 + n × 0x0004	8, 16, 32
Global SW Reset Register	CFDGRSTC	0x00000000	0x1380	16, 32
Channel n Data Bitrate Configuration Register*2	CFDCnDCFG	0x00000000	0x1400 + n × 0x0020	8, 16, 32
Channel n CAN-FD Configuration Register	CFDCnFDCFG	0x00000000	0x1404 + n × 0x0020	8, 16, 32
Channel n CAN-FD Control Register	CFDCnFDCTR	0x00000000	0x1408 + n × 0x0020	8, 16, 32

Table 32.2 CANFD寄存器(3of4)

注册名称	Symbol	重置值	偏移地址	访问大小
TX Queue Configuration/Control Registers 1 [n]	CFDTXQCC1n	0x00000000	0x1060 + n × 0x0004	8, 16, 32
TX队列状态寄存器1[n]	CFDTXQSTS1[n]	0x00000001	0x1080 + n × 0x0004	8, 16, 32
TX队列指针控制寄存器1[n]	CFDTXQPCTR1n	0x00000000	0x10A0 + n × 0x0004	8, 16, 32
TX Queue Configuration/Control Registers 2 [n]	CFDTXQCC2n	0x00000000	0x10C0 + n × 0x0004	8, 16, 32
TX队列状态寄存器2[n]	CFDTXQSTS2n	0x00000001	0x10E0 + n × 0x0004	8, 16, 32
TX队列指针控制寄存器2[n]	CFDTXQPCTR2n	0x00000000	0x1100 + n × 0x0004	8, 16, 32
TX Queue Configuration/Control Registers 3 [n]	CFDTXQCC3n	0x00000000	0x1120 + n × 0x0004	8, 16, 32
TX队列状态寄存器3[n]	CFDTXQSTS3n	0x00000001	0x1140 + n × 0x0004	8, 16, 32
TX队列指针控制寄存器3[n]	CFDTXQPCTR3n	0x00000000	0x1160 + n × 0x0004	8, 16, 32
TX队列空状态寄存器	CFDTXQESTS	0x000000FF	0x1180	8, 16, 32
TX队列满中断状态寄存器	CFDTXQFISTS	0x00000000	0x1184	8, 16, 32
TX队列消息丢失状态寄存器	CFDTXQMSTS	0x00000000	0x1188	8, 16, 32
TX队列中断状态寄存器	CFDTXQISTS	0x00000000	0x1190	8, 16, 32
TX队列一帧TX中断状态 Register	CFDTXQOFTISTS	0x00000000	0x1194	8, 16, 32
TX队列一帧RX中断状态 Register	CFDTXQOFRISTS	0x00000000	0x1198	8, 16, 32
TX队列满状态寄存器	CFDTXQFSTS	0x00000000	0x119C	8, 16, 32
TX历史列表配置控制 Register n	CFDTHLCCn	0x00000000	0x1200 + n × 0x0004	8, 16, 32
TX历史列表状态寄存器n	CFDTHLSTSn	0x00000001	0x1220 + n × 0x0004	8, 16, 32
TX历史列表指针控制寄存器 n	CFDTHLPCTRn	0x00000000	0x1240 + n × 0x0004	8, 16, 32
全局TX中断状态寄存器0	CFDGTINTSTS0	0x00000000	0x1300	8, 16, 32
全局测试配置寄存器	CFDGTSTCFG	0x00000000	0x1308	8, 16, 32
全局测试控制寄存器	CFDGTSTCTR	0x00000000	0x130C	8, 16, 32
全局FD配置寄存器	CFDGFDCFG	0x00000000	0x1314	8, 16, 32
全局FDCRC配置寄存器	CFDGCRCCFG	0x00000000	0x1318	8, 16, 32
全局锁定密钥寄存器	CFDGLOCKK	0x00000000	0x131C	16, 32
全局AFL忽略条目寄存器	CFDGAFLIGNENT	0x00000000	0x1324	8, 16, 32
全局AFL忽略控制寄存器	CFDGAFLIGNCTR	0x00000000	0x1328	16, 32
DMA传输控制寄存器	CFDCDTCT	0x00000000	0x1330	8, 16, 32
DMA传输状态寄存器	CFDCDTSTS	0x00000000	0x1334	8, 16, 32
DMATX传输控制寄存器	CFDCDTTCT	0x00000000	0x1340	8, 16, 32
DMATX传输状态寄存器	CFDCDTTSTS	0x00000000	0x1344	8, 16, 32
全局RX中断状态寄存器n	CFDGRINTSTSn	0x00000000	0x1350 + n × 0x0004	8, 16, 32
全局软件复位寄存器	CFDGRSTC	0x00000000	0x1380	16, 32
通道n数据比特率配置 Register*2	CFDCnDCFG	0x00000000	0x1400 + n × 0x0020	8, 16, 32
通道nCAN-FD配置 Register	CFDCnFDCFG	0x00000000	0x1404 + n × 0x0020	8, 16, 32
通道nCAN-FD控制寄存器	CFDCnFDCTR	0x00000000	0x1408 + n × 0x0020	8, 16, 32

Table 32.2 CANFD Registers (4 of 4)

Register name	Symbol	Reset value	Offset Address	Access size
Channel n CAN-FD Status Register	CFDCnFDSTS	0x00000000	0x140C + n × 0x0020	8, 16, 32
Channel n CAN-FD CRC Register*2	CFDCnFDCRC	0x00000000	0x1410 + n × 0x0020	8, 16, 32
Channel n Bus Load Control Register	CFDCnBLCT	0x00000000	0x1418h + n × 0x0020	8, 16, 32
Channel n Bus Load Status Register	CFDCnBLSTS	0x00000000	0x141C + n × 0x0020	8, 16, 32
Global Acceptance Filter List ID Registers n	CFDGAFLIDn	0x00000000*1	0x1800 + (n - 1) × 0x0010	8, 16, 32
Global Acceptance Filter List Mask Registers n	CFDGAFLMn	0x00000000*1	0x1804 + (n - 1) × 0x0010	8, 16, 32
Global Acceptance Filter List Pointer 0 Registers n	CFDGAFLP0n	0x00000000*1	0x1808 + (n - 1) × 0x0010	8, 16, 32
Global Acceptance Filter List Pointer 1 Registers n	CFDGAFLP1n	0x00000000*1	0x180C + (n - 1) × 0x0010	8, 16, 32
Channel n TX History List Access Registers 0	CFDTHLACC0n	0x00000000*1	0x8000 + n × 0x0008	8, 16, 32
Channel n TX History List Access Registers 1	CFDTHLACC1n	0x00000000*1	0x8004 + n × 0x0008	8, 16, 32
RAM Test Page Access Registers n	CFDRPGACCn	0x00000000*1	0x8400 + n × 0x0004	8, 16, 32
RX Message Buffer ID Registers	CFDRMID	0x00000000*1	See section 32.2.87.2. CFDRMIDn_i : RX Message Buffer ID Register n Channel i (n = 0 to 15, i = 0, 1)	8, 16, 32
RX Message Buffer Pointer Registers	CFDRMPTR	0x00000000*1	See section 32.2.87.3. CFDRMPTRn_i : RX Message Buffer Pointer Register n Channel i (n = 0 to 15, i = 0, 1)	8, 16, 32
RX Message Buffer CAN-FD Status Register	CFDRMFDSTS	0x00000000*1	See section 32.2.87.4. CFDRMFDSTSn_i : RX Message Buffer CAN-FD Status Register n Channel i (n = 0 to 15, i = 0, 1)	8, 16, 32
RX Message Buffer Data Field p Registers Channel i	CFDRMDFpn_i	0x00000000*1	See section 32.2.87.5. CFDRMDFpn_i : RX Message Buffer Data Field p Register n Channel i (p = 0 to 15, n = 0 to 15, i = 0, 1)	8, 16, 32
TX Message Buffer ID Registers	CFDTMID	0x00000000*1	See section 32.2.87.14. CFDTMIDn_i : TX Message Buffer ID Register n Channel i (n = 0 to 7, 32 to 39, i = 0, 1)	8, 16, 32
TX Message Buffer Pointer Registers	CFDTMPTR	0x00000000*1	See section 32.2.87.15. CFDTMPTRn_i : TX Message Buffer Pointer Register n Channel i (n = 0 to 7, 32 to 39, i = 0, 1)	8, 16, 32
TX Message Buffer CAN-FD Control Register	CFDTMFDCTR	0x00000000*1	See section 32.2.87.16. CFDTMFDCTRn_i : TX Message Buffer CAN-FD Control Register n Channel i (n = 0 to 7, 32 to 39, i = 0, 1)	8, 16, 32
TX Message Buffer Data Field p Registers n Channel i	CFDTMDFpn_i	0x00000000*1	See section 32.2.87.17. CFDTMDFpn_i : TX Message Buffer Data Field p Register n Channel i (p = 0 to 15, n = 0 to 7, 32 to 39, i = 0, 1)	8, 16, 32

Note: For the range of subscripts (n, f, i, p), refer to the explanation of each register.
Note 1. The RAM area is initialized after a hardware reset, see section 32.4.2. CAN Module Configuration after Hardware Reset.
Note 2. These registers are not available in the classical CAN function.

Table 32.2 CANFD寄存器(4of4)

注册名称	Symbol	重置值	偏移地址	访问大小
通道nCAN-FD状态寄存器	CFDCnFDSTS	0x00000000	0x140C + n × 0x0020	8, 16, 32
通道nCAN-FDCRC寄存器*2	CFDCnFDCRC	0x00000000	0x1410 + n × 0x0020	8, 16, 32
通道n总线负载控制寄存器	CFDCnBLCT	0x00000000	0x1418h + n × 0x0020	8, 16, 32
通道n总线负载状态寄存器	CFDCnBLSTS	0x00000000	0x141C + n × 0x0020	8, 16, 32
全局接受过滤器列表ID寄存器 n	CFDGAFLIDn	0x00000000*1	0x1800 + (n - 1) × 0x0010	8, 16, 32
全局接受过滤器列表掩码 Registers n	CFDGAFLMn	0x00000000*1	0x1804 + (n - 1) × 0x0010	8, 16, 32
全局接受过滤器列表指针0 Registers n	CFDGAFLP0n	0x00000000*1	0x1808 + (n - 1) × 0x0010	8, 16, 32
全局接受过滤器列表指针1 Registers n	CFDGAFLP1n	0x00000000*1	0x180C + (n - 1) × 0x0010	8, 16, 32
通道nTX历史列表访问 Registers 0	CFDTHLACC0n	0x00000000*1	0x8000 + n × 0x0008	8, 16, 32
通道nTX历史列表访问 Registers 1	CFDTHLACC1n	0x00000000*1	0x8004 + n × 0x0008	8, 16, 32
RAM测试页访问寄存器n	CFDRPGACCn	0x00000000*1	0x8400 + n × 0x0004	8, 16, 32
RX报文缓冲区ID寄存器	CFDRMID	0x00000000*1	请参阅第32.2.87.2节。CFDRMIDn_i : RX Message 缓冲区ID寄存器n通道i(n=0到15 i=0 1)	8, 16, 32
RX消息缓冲区指针寄存器	CFDRMPTR	0x00000000*1	请参阅第32.2.87.3节。CFDRMPTRn_i:RX消息缓冲区指针寄存器n 通道i(n=0到15 i=0 1)	8, 16, 32
RX消息缓冲区CAN-FD状态 Register	CFDRMFDSTS	0x00000000*1	请参阅第32.2.87.4节。CFDRMFDSTSn_i：RX消息缓冲区CAN-FD状态寄存器n 通道i(n=0到15 i=0 1)	8, 16, 32
RX消息缓冲区数据字段p 注册通道i	CFDRMDFpn_i	0x00000000*1	请参阅第32.2.87.5节。CFDRMDFpn_i:RX消息缓冲区数据字段p寄存器n通道i(p=0到15 n=0到15 i=0 1)	8, 16, 32
TX报文缓冲区ID寄存器	CFDTMID	0x00000000*1	请参阅第32.2.87.14节。CFDTMIDn_i : TX Message 缓冲区ID寄存器n通道i(n=0到7 32到39 i=0 1)	8, 16, 32
TX报文缓冲区指针寄存器	CFDTMPTR	0x00000000*1	请参阅第32.2.87.15节。CFDTMPTRn_i:发送消息 缓冲区指针寄存器n 通道i(n=0到7 32到39 i=0 1)	8, 16, 32
TX报文缓冲器CAN-FD控制 Register	CFDTMFDCTR	0x00000000*1	请参阅第32.2.87.16节。CFDTMFDCTRn_i:TX报文缓冲器CAN-FD控制寄存器n通道i(n=0到7 32到39 i=0 1)	8, 16, 32
TX消息缓冲区数据字段p 寄存器n通道i	CFDTMDFpn_i	0x00000000*1	请参阅第32.2.87.17节。CFDTMDFpn_i：TX消息缓冲区数据字段p寄存器n 通道i(p=0到15 n=0到7 32到39 i=0 1)	8, 16, 32

Note: 下标（n、f、i、p）的范围请参考各寄存器的说明。
注1.RAM区域在硬件复位后初始化，见32.4.2节。硬件复位后的CAN模块配置。
注2：这些寄存器在经典CAN功能中不可用。

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32.2.3 CFDCnNCFG : Channel n Nominal Bitrate Configuration Register (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x0000 + 0x10 × n

Bit position:	31 … 25	24 … 17	16 … 10	9 … 0
Bit field:	NTSEG2[6:0]	NTSEG1[7:0]	NSJW[6:0]	NBRP[9:0]
Value after reset:	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
9:0	NBRP[9:0]	Channel Nominal Baud Rate Prescaler Nominal baud rate prescaler division ratio	R/W
16:10	NSJW[6:0]	Resynchronization Jump Width 0x00: 1 Tq 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W
24:17	NTSEG1[7:0]	Timing Segment 1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0xFE: 255 Tq 0xFF: 256 Tq	R/W
31:25	NTSEG2[6:0]	Timing Segment 2 0x00: Reserved 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W

Note: Tq means time quantum.

This register configures the transmission/reception nominal baud rate parameters of the channels.

NBRP[9:0] bits (Channel Nominal Baud Rate Prescaler)

The NBRP[9:0] bits are used to define the peripheral bus clock periods contained in a time quantum.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CAN-FD channel is in CH_RESET or CH_HALT mode.

NSJW[6:0] bits (Resynchronization Jump Width)

The NSJW[6:0] bits set the synchronization jump width. A value from 1 to 128 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CAN-FD channel is in CH_RESET or CH_HALT mode.

NTSEG1[7:0] bits (Timing Segment 1)

The NTSEG1[7:0] bits set the segment TSEG1 to compensate for edges on the CAN bus with a positive phase error. These bits contain the propagation segment.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CAN-FD channel is in CH_RESET or CH_HALT mode.

Additionally, configure a Tq value only between 2 and 256, inclusive. See section 32.4.1.2. CAN Bit Timing for more details.

32.2.3 CFDCnNCFG:通道n标称比特率配置寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x0000 + 0x10 × n

Bit position:	31 … 25	24 … 17	16 … 10	9 … 0
Bit field:	NTSEG2[6:0]	NTSEG1[7:0]	NSJW[6:0]	NBRP[9:0]
重置后的值:	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
9:0	NBRP[9:0]	通道标称波特率预分频器 标称波特率预分频比	R/W
16:10	NSJW[6:0]	再同步跳转宽度 0x00: 1 Tq 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W
24:17	NTSEG1[7:0]	时序段1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0xFE: 255 Tq 0xFF: 256 Tq	R/W
31:25	NTSEG2[6:0]	计时段2 0x00: Reserved 0x01: 2 Tq ⋮ 0x7E: 127 Tq 0x7F: 128 Tq	R/W

Note: Tq表示时间量。

该寄存器配置通道的发送接收标称波特率参数。

NBRP[9:0]位（通道标称波特率预分频器）

NBRP[9:0]位用于定义包含在时间片中的外围总线时钟周期。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

NSJW[6:0]位（重新同步跳转宽度）

NSJW[6:0]位设置同步跳转宽度。可以设置1到128个时间量子的值。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

NTSEG1[7:0]位（时序段1）

NTSEG1[7:0]位设置段TSEG1以补偿CAN总线上具有正相位误差的边沿。这些位包含传播段。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

此外，仅在2和256之间配置Tq值（包括2和256）。请参阅第32.4.1.2节。CAN位时序了解更多详情。

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NTSEG2[6:0] bits (Timing Segment 2)

The NTSEG2[6:0] bits set the segment TSEG2 to compensate for edges on the CAN bus with a negative phase error.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CAN-FD channel is in CH_RESET or CH_HALT mode.

Additionally, configure a Tq value only between 2 and 128, inclusive.

32.2.4 CFDCnCTR : Channel n Control Registers (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x0004 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ROM	CRCT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCV FIE	SOCO IE	EOCO IE	TAIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLP R	CHMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	CHMDC[1:0]	Channel Mode Control 0 0: Channel operation mode request 0 1: Channel reset request 1 0: Channel halt request 1 1: Keep current value	R/W
2	CSLPR	Channel Sleep Request 0: Channel sleep request disabled 1: Channel sleep request enabled	R/W
3	RTBO	Return from Bus-Off 0: Channel is not forced to return from bus-off 1: Channel is forced to return from bus-off	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	BEIE	Bus Error Interrupt Enable 0: Bus error interrupt disabled 1: Bus error interrupt enabled	R/W
9	EWIE	Error Warning Interrupt Enable 0: Error warning interrupt disabled 1: Error warning interrupt enabled	R/W
10	EPIE	Error Passive Interrupt Enable 0: Error passive interrupt disabled 1: Error passive interrupt enabled	R/W
11	BOEIE	Bus-Off Entry Interrupt Enable 0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	R/W
12	BORIE	Bus-Off Recovery Interrupt Enable 0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	R/W
13	OLIE	Overload Interrupt Enable 0: Overload interrupt disabled 1: Overload interrupt enabled	R/W
14	BLIE	Bus Lock Interrupt Enable 0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	R/W

NTSEG2[6:0]位（时序段2）

NTSEG2[6:0]位设置段TSEG2以补偿CAN总线上的边沿与负相位误差。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

此外，仅将Tq值配置在2到128之间（包括2到128）。

32.2.4 CFDCnCTR:通道n控制寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x0004 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ROM	CRCT	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	TDCV FIE	SOCO IE	EOCO IE	TAIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLP R	CHMDC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	CHMDC[1:0]	通道模式控制 00：通道操作模式请求01：通道复位请求10：通道停止请求11：保持当前值	R/W
2	CSLPR	通道休眠请求 0：禁用通道睡眠请求1：启用通道睡眠请求	R/W
3	RTBO	从巴士下车返回 0：通道不强制从总线关闭返回1：通道强制从总线关闭返回	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	BEIE	总线错误中断使能 0：禁止总线错误中断1：允许总线错误中断	R/W
9	EWIE	错误警告中断使能 0：禁止错误警告中断1：允许错误警告中断	R/W
10	EPIE	错误被动中断使能 0：禁用错误被动中断1：启用错误被动中断	R/W
11	BOEIE	总线关闭进入中断使能 0：禁止总线关闭进入中断1：允许总线关闭进入中断	R/W
12	BORIE	总线关闭恢复中断使能 0：禁止总线关闭恢复中断1：允许总线关闭恢复中断	R/W
13	OLIE	过载中断使能 0：禁止过载中断1：允许过载中断	R/W
14	BLIE	总线锁定中断使能 0：禁止总线锁定中断1：使能总线锁定中断	R/W

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Bit	Symbol	Function	R/W
15	ALIE	Arbitration Lost Interrupt Enable 0: Arbitration lost interrupt disabled 1: Arbitration lost interrupt enabled	R/W
16	TAIE	Transmission Abort Interrupt Enable 0: TX abort interrupt disabled 1: TX abort interrupt enabled	R/W
17	EOCOIE	Error Occurrence Counter Overflow Interrupt Enable 0: Error occurrence counter overflow interrupt disabled 1: Error occurrence counter overflow interrupt enabled	R/W
18	SOCOIE	Successful Occurrence Counter Overflow Interrupt Enable 0: Successful occurrence counter overflow interrupt disabled 1: Successful occurrence counter overflow interrupt enabled	R/W
19	TDCVFIE*1	Transceiver Delay Compensation Violation Interrupt Enable 0: Transceiver delay compensation violation interrupt disabled 1: Transceiver delay compensation violation interrupt enabled	R/W
20	—	This bit is read as 0. The write value should be 0.	R/W
22:21	BOM[1:0]	Channel Bus-Off Mode 0 0: Normal mode (comply with ISO 11898-1) 0 1: Entry to Halt mode automatically at bus-off start 1 0: Entry to Halt mode automatically at bus-off end 1 1: Entry to Halt mode (during bus-off recovery period) by software	R/W
23	ERRD	Channel Error Display 0: Only the first set of error codes displayed 1: Accumulated error codes displayed	R/W
24	CTME	Channel Test Mode Enable 0: Channel test mode disabled 1: Channel test mode enabled	R/W
26:25	CTMS[1:0]	Channel Test Mode Select 0 0: Basic test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (External loopback mode) 1 1: Self-test mode 1 (Internal loopback mode)	R/W
29:27	—	These bits are read as 0. The write value should be 0.	R/W
30	CRCT	CRC Error Test 0: First data bit of reception stream not inverted 1: First data bit of reception stream inverted	R/W
31	ROM*1	Restricted Operation Mode 0: Restricted operation mode disabled 1: Restricted operation mode enabled	R/W

Note 1. These bits are not available in the classical CAN function.

Each Channel Control register controls the modes of the related channel. It is used to enable generation of interrupts if errors are detected on the CAN bus connected to this channel. It is also used to configure the channel in test mode.

CHMDC[1:0] bits (Channel Mode Control)

The CHMDC[1:0] bits can be used to configure modes of the CAN channel.

CAN mode transitions are described in more details in section 32.3.3. Channel Modes.

Setting CHMDC[1:0] bits to 11b has no effect. When the CAN-FD module is in GL_HALT mode, these bits can only be set to 10b or 01b. These bits cannot be set in CH_SLEEP mode.

These bits can change automatically when transitioning to Halt mode by the CFDCnCTR.BOM settings.

If CPU write access to CFDCnCTR.CHMDC occurs at the same time when the CAN channel enters Halt mode (at the start of bus-off when CFDCnCTR.BOM = 01b, or at the end of bus-off when CFDCnCTR.BOM = 10b), then the CPU write access has the highest priority.

Bit	Symbol	Function	R/W
15	ALIE	仲裁丢失中断使能 0：禁止仲裁丢失中断1：使能仲裁丢失中断	R/W
16	TAIE	传输中止中断使能 0：禁用TX中止中断1：启用TX中止中断	R/W
17	EOCOIE	错误发生计数器溢出中断使能 0：错误发生计数器溢出中断禁止1：错误发生计数器溢出中断允许	R/W
18	SOCOIE	成功发生计数器溢出中断使能 0：禁止成功发生计数器溢出中断1：使能成功发生计数器溢出中断	R/W
19	TDCVFIE*1	收发器延迟补偿违规中断使能 0：禁止收发器延迟补偿违规中断1：使能收发器延迟补偿违规中断	R/W
20	—	该位读取为0。写入值应为0。	R/W
22:21	BOM[1:0]	通道总线关闭模式 00：正常模式（符合ISO11898-1）01：在总线关闭开始时自动进入停止模式10：在总线关闭结束时自动进入停止模式11：进入停止模式（在总线关闭期间）关闭恢复期）通过软件	R/W
23	ERRD	通道错误显示 0：只显示第一组错误码1：显示累计错误码	R/W
24	CTME	通道测试模式启用 0：禁用通道测试模式1：启用通道测试模式	R/W
26:25	CTMS[1:0]	通道测试模式选择 00：基本测试模式01：只听模式10：自测模式0（外部环回模式）11：自测模式1（内部环回模式）	R/W
29:27	—	这些位被读取为0。写入值应为0。	R/W
30	CRCT	CRC错误测试 0：接收流的第一个数据位不反转1：接收流的第一个数据位反转	R/W
31	ROM*1	受限操作模式 0：禁用限制操作模式1：启用限制操作模式	R/W

注1.这些位在经典CAN功能中不可用。

每个通道控制寄存器控制相关通道的模式。如果在连接到此通道的CAN总线上检测到错误，它用于启用中断生成。它还用于在测试模式下配置通道。

CHMDC[1:0]位（通道模式控制）

CHMDC[1:0]位可用于配置CAN通道的模式。

CAN模式转换在第32.3.3节中有更详细的描述。频道模式。

将CHMDC[1:0]位设置为11b无效。当CAN-FD模块处于GL_HALT模式时，这些位只能设置为10b或01b。这些位不能在CH_SLEEP模式下设置。

当通过CFDCnCTR.BOM设置转换到暂停模式时，这些位可以自动更改。

如果CPU对CFDCnCTR.CHMDC的写访问发生在CAN通道进入Halt模式的同时（当CFDCnCTR.BOM=01b时在总线关闭开始时，或者当CFDCnCTR.BOM=10b时在总线关闭结束时），则CPU写访问的优先级最高。

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The CAN channel changes the value of CFDCnCTR.CHMDC within the Channel Control Registers for the specified cases only if the CFDCnCTR.CHMDC value is 00b (Operation mode).

CSLPR bit (Channel Sleep Request)

When the CSLPR bit is 1, a Sleep mode request is generated for the corresponding CAN channel

When this bit is 0, a request to exit Sleep mode is generated for the related CAN-FD channel.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_SLEEP mode.

RTBO bit (Return from Bus-Off)

When the protocol controller of the CAN channel enters bus-off state, you can force a recovery from bus-off state by setting the RTBO bit in the Channel Control Register to 1.

The error state changes from bus-off state to integrating with a maximum delay of 1 CAN bit time.

When the RTBO bit is set to 1, the REC and TEC registers are initialized and the Bus-Off Status bit (Channel Bus-off Status, CFDCnSTS.BOSTS) is set to 0.

Registers other than the REC and TEC registers are not initialized by this command. Even if CFDCnCTR.BORIE is set, a bus-off recovery interrupt is not generated by this recovery from the bus-off state.

The RTBO bit cannot be set in CH_SLEEP mode. Setting this bit in any state other than bus-off state has no effect and the bit is cleared immediately. The read value is always 0.

Return from the Bus-Off command should be used only when CFDCnCTR.BOM is set to 00b.

Only write to this bit when the related CAN-FD channel is in CH_OPERATION mode. This bit is automatically cleared when set by software.

BEIE bit (Bus Error Interrupt Enable)

When the BEIE and the CFDCnERFL.BEF bits are both 1, an error interrupt request is generated.

This bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

EWIE bit (Error Warning Interrupt Enable)

When the EWIE and the CFDCnERFL.EWF bits are both 1, an error interrupt request is generated.

The EWIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

EPIE bit (Error Passive Interrupt Enable)

An error interrupt request is generated when the EPIE bit and the CFDCnERFL.EPF are both 1.

The EPIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE and the CFDCnERFL.BOEF bits are both 1, an error interrupt request is generated.

The BOEIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE and the CFDCnERFL.BORF bits are both 1, an error interrupt request is generated.

The BORIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

OLIE bit (Overload Interrupt Enable)

When the OLIE and the CFDCnERFL.OVLF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

仅当CFDCnCTR.CHMDC值为00b（操作模式）时，CAN通道才会在指定情况下更改通道控制寄存器中CFDCnCTR.CHMDC的值。

CSLPR位（通道休眠请求）

当CSLPR位为1时，为相应的CAN通道生成休眠模式请求

当该位为0时，会为相关的CAN-FD通道生成退出休眠模式的请求。

仅当相关CAN-FD通道处于CH_RESET或CH_SLEEP模式时才写入该位。

RTBO位（从总线关闭返回）

当CAN通道的协议控制器进入总线关闭状态时，您可以通过将通道控制寄存器中的RTBO位设置为1来强制从总线关闭状态恢复。

错误状态从总线关闭状态变为积分，最大延迟为1个CAN位时间。

当RTBO位设置为1时，REC和TEC寄存器被初始化并且总线关闭状态位（通道总线关闭状态，CFDCnSTS.BOSTS)设置为0。

该命令不初始化REC和TEC寄存器以外的寄存器。即使设置了CFDCnCTR.BORIE，从总线关闭状态恢复也不会产生总线关闭恢复中断。

在CH_SLEEP模式下不能设置RTBO位。将该位设置为总线关闭状态以外的任何状态均无效，并且该位立即被清除。读取值始终为0。

只有当CFDCnCTR.BOM设置为00b时，才应使用从总线关闭命令返回。

仅当相关CAN-FD通道处于CH_OPERATION模式时才写入该位。该位由软件置位时自动清零。

BEIE位（总线错误中断使能）

当BEIE和CFDCnERFL.BEF位均为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置该位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

EWIE位（错误警告中断使能）

当EWIE和CFDCnERFL.EWF位都为1时，会产生错误中断请求。

在CH_SLEEP模式下不能设置EWIE位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

EPIE位（错误被动中断使能）

当EPIE位和CFDCnERFL.EPF都为1时产生错误中断请求。

在CH_SLEEP模式下不能设置EPIE位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

BOEIE位（总线关闭进入中断允许）

当BOEIE和CFDCnERFL.BOEF位均为1时，会产生错误中断请求。

在CH_SLEEP模式下不能设置BOEIE位。仅当相关CAN-FD通道在时才写入该位
CH_RESET mode.

BORIE位（总线关闭恢复中断使能）

当BORIE和CFDCnERFL.BORF位均为1时，会产生错误中断请求。

在CH_SLEEP模式下不能设置BORIE位。仅当相关CAN-FD通道在时才写入该位
CH_RESET mode.

OLIE位（过载中断使能）

当OLIE和CFDCnERFL.OVLF位都为1时，产生错误中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE and the CFDCnERFL.BLF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

ALIE bit (Arbitration Lost Interrupt Enable)

When the ALIE and the CFDCnERFL.ALF bits are both 1, an error interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

TAIE bit (Transmission Abort Interrupt Enable)

When the TAIE bit is 1 and a transmission is successfully aborted from a TX MB belonging to the corresponding CAN channel, an interrupt request is generated.

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

EOCOIE bit (Error Occurrence Counter Overflow Interrupt Enable)

When the EOCOIE bit is 1 and the CFDCnFDSTS.EOCO bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The EOCOIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

SOCOIE bit (Successful Occurrence Counter Overflow Interrupt Enable)

When the SOCOIE bit is 1 and the CFDCnFDSTS.SOCO bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The SOCOIE bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

TDCVFIE bit (Transceiver Delay Compensation Violation Interrupt Enable)

When the TDCVFIE bit is 1 and the CFDCnFDSTS.TDCVF bit belonging to the corresponding CAN channel is 1, an error interrupt request is generated.

The TDCVFIE bit cannot be set in CH_SLEEP mode.

Only write to this bit when the related CAN-FD channel is in CH_RESET mode. Do not set this bit when in Classical-only mode.

Note: This bit is not available in the classical CAN function.

BOM[1:0] bits (Channel Bus-Off Mode)

The BOM[1:0]bits control the timing of the recovery from Bus-Off mode of the CAN-FD Channel.

Do not write to these bits in CH_SLEEP mode. Only write to these bits when the related CAN-FD channel is in CH_RESET mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET mode.

ERRD bit (Channel Error Display)

The ERRD bit controls the display mode of the error flag bits [14:8] in the Channel Error Flag Register (CFDCnERFL).

If the ERRD bit is 0 and more than one error occur at the same time, the error flag bits are set for all the errors that occurred at the same time. No further errors are flagged until CFDCnERFL[14:8] is cleared.

Do not write to the ERRD bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

CTME bit (Channel Test Mode Enable)

The CTME bit enables the channel test modes.

BLIE位（总线锁定中断使能）

当BLIE和CFDCnERFL.BLF位都为1时，会产生错误中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

ALIE位（仲裁丢失中断使能）

当ALIE和CFDCnERFL.ALF位都为1时，会产生错误中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

TAIE位（发送中止中断使能）

当TAIE位为1并且从属于相应CAN通道的TXMB成功中止传输时，将产生中断请求。

在CH_SLEEP模式下不要写入该位。仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

EOCOIE位（错误发生计数器溢出中断使能）

当EOCOIE位为1且属于相应CAN通道的CFDCnFDSTS.EOCO位为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置EOCOIE位。仅当相关CAN-FD通道在时才写入该位
CH_RESET mode.

SOCOIE位（成功发生计数器溢出中断使能）

当SOCOIE位为1且属于相应CAN通道的CFDCnFDSTS.SOCO位为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置SOCOIE位。仅当相关CAN-FD通道在时才写入该位
CH_RESET mode.

TDCVFIE位（收发器延迟补偿违反中断允许）

当TDCVFIE位为1且属于相应CAN通道的CFDCnFDSTS.TDCVF位为1时，产生错误中断请求。

在CH_SLEEP模式下不能设置TDCVFIE位。

仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。在仅经典模式下不要设置该位。

Note: 该位在经典CAN功能中不可用。

BOM[1:0] bits (Channel Bus-Off Mode)

BOM[1:0]位控制CAN-FD通道从总线关闭模式恢复的时序。

请勿在CH_SLEEP模式下写入这些位。仅当相关CAN-FD通道处于CH_RESET模式时才写入这些位。

仅当相关CAN-FD通道处于CH_RESET模式时才写入这些位。

ERRD位（通道错误显示）

ERRD位控制通道错误标志寄存器(CFDCnERFL)中错误标志位[14:8]的显示模式。

如果ERRD位为0并且同时发生多个错误，则为同时发生的所有错误设置错误标志位。在清除CFDCnERFL[14:8]之前不会标记更多错误。

请勿在CH_SLEEP模式下写入ERRD位。仅当相关CAN-FD通道在时才写入该位
CH_RESET或CH_HALT模式。

CTME位（通道测试模式启用）

CTME位启用通道测试模式。

Do not write to this bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_HALT mode.

CTMS[1:0] bits (Channel Test Mode Select)

The CTMS[1:0] bits are used to select the required test mode.

Do not write to these bits in CH_SLEEP or CH_RESET mode. Only write to these bits when the related CAN-FD channel is in CH_HALT mode.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

CRCT bit (CRC Error Test)

The CRCT bit checks the internal CRC generator logic of the protocol controller.

The internal generated CRC value is always observed in the following registers:

- CFDCnERFL.CRCREG (Classical CAN frames)
- CFDCnFDCRC.CRCREG (CAN-FD frames).*1

Note 1. This feature is not available in the classical CAN function.

Some restriction exist when using this bit:

- It is not possible to use this feature with CAN nodes connected to the MCU externally, only with nodes connected to the internal CAN bus communication can be used
- One CAN node can send a reference message and the receiver node can invert one bit of the incoming bit stream.

Note: The transmitter and receiver modes share the same CRC generator, therefore it is not necessary to consider the modes separately when testing.

The CRC Error test mode is enabled if the CRCT (new control signal that inverts the first bit of the bit stream) and CTME bits are both 1.

Do not write to the CRCT bit in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_HALT mode.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

ROM bit (Restricted Operation Mode)

When the ROM and CTME bits are both 1, the restricted operation mode is enabled. This mode should only be used in basic test mode (CFDCnCTR.CTMS[1:0] = 00b).

The ROM bit cannot be set in CH_SLEEP mode. Only write to this bit when the related CAN-FD channel is in CH_HALT mode.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. Do not set this bit when in Classical-only mode.

Note: This bit is not available in the classical CAN function.

32.2.5 CFDCnSTS : Channel n Status Registers (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x0008 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TEC[7:0]								REC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

在CH_SLEEP模式下不要写入该位。仅当相关CAN-FD通道处于CH_HALT模式时才写入该位。

CTMS[1:0]位（通道测试模式选择）

CTMS[1:0]位用于选择所需的测试模式。

不要在CH_SLEEP或CH_RESET模式下写入这些位。仅当相关CAN-FD通道处于CH_HALT模式时才写入这些位。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

CRCT位（CRC错误测试）

CRCT位检查协议控制器的内部CRC生成器逻辑。

内部生成的CRC值始终在以下寄存器中观察：

- CFDCnERFL.CRCREG (Classical CAN frames)
- CFDCnFDCRC.CRCREG (CAN-FD frames).*1

注1.此功能在经典CAN功能中不可用。

使用该位时存在一些限制：

●外接单片机的CAN节点无法使用此功能，只能使用内接CAN总线通讯的节点

●一个CAN节点可以发送参考消息，接收节点可以反转输入比特流的一位。

Note: 发送器和接收器模式共享相同的CRC生成器，因此在测试时无需单独考虑这些模式。

如果CRCT（反转比特流第一位的新控制信号）和CTME位均为1，则启用CRC错误测试模式。

请勿在CH_SLEEP模式下写入CRCT位。仅当相关CAN-FD通道在时才写入该位
CH_HALT mode.

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

ROM位（受限操作模式）

当ROM和CTME位都为1时，限制操作模式被使能。该模式只能用于基本测试模式（CFDCnCTR.CTMS[1:0]=00b）。

在CH_SLEEP模式下不能设置ROM位。仅当相关CAN-FD通道处于CH_HALT模式时才写入该位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。不要设置该位时
Classical-only mode.

Note: 该位在经典CAN功能中不可用。

32.2.5 CFDCnSTS:通道n状态寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x0008 + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TEC[7:0]								REC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ESIF	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
0	CRSTSTS	Channel Reset Status 0: Channel not in Reset mode 1: Channel in Reset mode	R
1	CHLTSTS	Channel Halt Status 0: Channel not in Halt mode 1: Channel in Halt mode	R
2	CSLPSTS	Channel Sleep Status 0: Channel not in Sleep mode 1: Channel in Sleep mode	R
3	EPSTS	Channel Error Passive Status 0: Channel not in error passive state 1: Channel in error passive state	R
4	BOSTS	Channel Bus-Off Status 0: Channel not in bus-off state 1: Channel in bus-off state	R
5	TRMSTS	Channel Transmit Status 0: Channel is not transmitting 1: Channel is transmitting	R
6	RECSTS	Channel Receive Status 0: Channel is not receiving 1: Channel is receiving	R
7	COMSTS	Channel Communication Status 0: Channel is not ready for communication 1: Channel is ready for communication	R
8	ESIF*1	Error State Indication Flag 0: No CAN-FD message has been received when the ESI flag was set 1: At least one CAN-FD message was received when the ESI flag was set	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
23:16	REC[7:0]	Reception Error Count These bits increment or decrement the counter value according to error status of the CAN channel during reception.	R
31:24	TEC[7:0]	Transmission Error Count These bits increment or decrement the counter value according to error status of the CAN channel during transmission.	R

Note 1. This bit is not available in the classical CAN function.

Each Channel Status Register shows the mode, error and transmission or reception status of the related channel together with its reception and transmission error count values.

CRSTSTS bit (Channel Reset Status)

The CRSTSTS bit indicates whether the related CAN channel is in Reset mode.

This bit is set automatically when the related CAN channel enters Channel Reset mode. When the mode is changed from Reset mode to Sleep mode, the CRSTSTS bit remains 1.

This bit is cleared automatically when the related CAN channel exits the Channel Reset mode, except when changing to Sleep mode.

CHLTSTS bit (Channel Halt Status)

The CHLTSTS bit indicates whether the related CAN channel is in Halt mode.

This bit is set automatically when the related CAN module enters Halt mode, and is cleared automatically when the related CAN module exits Halt mode.

CSLPSTS bit (Channel Sleep Status)

The CSLPSTS bit indicates whether the related CAN channel is in Sleep mode.

Bit	Symbol	Function	R/W
0	CRSTSTS	通道复位状态 0：通道不处于复位模式1：通道处于复位模式	R
1	CHLTSTS	通道暂停状态 0：通道未处于暂停模式1：通道处于暂停模式	R
2	CSLPSTS	通道休眠状态 0：通道不处于休眠模式1：通道处于休眠模式	R
3	EPSTS	通道错误被动状态 0：通道未处于错误被动状态1：通道处于错误被动状态	R
4	BOSTS	通道总线关闭状态 0：通道未处于总线关闭状态1：通道处于总线关闭状态	R
5	TRMSTS	通道传输状态 0：通道未发送1：通道正在发送	R
6	RECSTS	频道接收状态 0：通道未接收1：通道正在接收	R
7	COMSTS	通道通讯状态 0：通道未准备好通讯1：通道准备好通讯	R
8	ESIF*1	错误状态指示标志 0：设置ESI标志时未接收到CAN-FD消息1：设置ESI标志时至少接收到一条CAN-FD消息	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
23:16	REC[7:0]	接收错误计数 这些位根据接收期间CAN通道的错误状态递增或递减计数器值。	R
31:24	TEC[7:0]	传输错误计数 这些位在传输过程中根据CAN通道的错误状态递增或递减计数器值。	R

注1.该位在经典CAN功能中不可用。

每个通道状态寄存器显示相关通道的模式、错误和发送或接收状态及其接收和发送错误计数值。

CRSTSTS位（通道复位状态）

CRSTSTS位指示相关CAN通道是否处于复位模式。

当相关CAN通道进入通道复位模式时，该位自动置位。当模式从将模式复位为休眠模式，CRSTSTS位保持为1。

当相关CAN通道退出通道复位模式时，该位自动清零，除非更改为睡眠模式。

CHLTSTS位（通道暂停状态）

CHLTSTS位指示相关CAN通道是否处于暂停模式。

该位在相关CAN模块进入Halt模式时自动置位，当相关CAN模块进入Halt模式时自动清零CAN模块退出暂停模式。

CSLPSTS位（通道休眠状态）

CSLPSTS位指示相关CAN通道是否处于休眠模式。

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This bit is set automatically when the related CAN-FD channel enters Sleep mode, and is cleared automatically when the related CAN-FD channel exits Sleep mode.

EPSTS bit (Channel Error Passive Status)

The EPSTS bit indicates whether the related CAN-FD channel has entered the error passive state.

This bit is set automatically when the value of the CAN Transmission or Reception Counter Register exceeds the value of 0x7F.

This bit is cleared automatically when the related CAN-FD channel exits the error passive state or enters Reset mode.

BOSTS bit (Channel Bus-Off Status)

The BOSTS bit indicates whether the related CAN-FD channel has entered the error bus-off state.

This bit is set automatically when the value of the related CAN Transmission Error Count Register exceeds 0xFF and the related CAN-FD channel is in the bus-off state (CAN Transmission Error Count Register > 0xFF).

This bit is cleared automatically when the related CAN-FD channel exits bus-off state.

TRMSTS bit (Channel Transmit Status)

The TRMSTS bit indicates whether the related CAN-FD channel is transmitting a message.

This bit is set automatically when the related CAN-FD channel is operating as a transmitter node or is in the bus-off state.

This bit is cleared automatically when the related CAN-FD channel is in the bus-idle state or starts operating as a receiver node.

RECSTS bit (Channel Receive Status)

The RECSTS bit indicates whether the related CAN-FD channel is receiving a message.

This bit is set automatically when the related CAN-FD channel is operating as a receiver node.

This bit is cleared automatically when the related CAN-FD channel is in the bus-idle state or starts operating as a transmitter node.

COMSTS bit (Channel Communication Status)

The COMSTS bit indicates whether the related CAN-FD channel is ready for communication.

This bit is set automatically when the related CAN-FD channel is ready to perform communication following the detection of 11 consecutive recessive bits after exiting the Reset or Halt mode.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET or CD_HALT mode.

Note: This bit is 1 during bus-off state.

ESIF bit (Error State Indication Flag)

The ESIF bit is set when the ESI bit is sampled recessively for a reception CAN message without any error. When in Loopback or Mirror mode, the self-transmitted messages are considered reception messages.

If a set from the CAN-FD channel occurs simultaneously with a clear by a write access, then the bit is set.

This bit is cleared by writing 0 to it. This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Note: This bit is not available in the classical CAN function.

REC[7:0] bits (Reception Error Count)

The REC[7:0] bits increment or decrement the counter value according to error status of the CAN-FD channel during reception, and display the value of the REC error counter.

The value in bus-off state is indeterminate.

该位在相关CAN-FD通道进入休眠模式时自动置位，并在相关CAN-FD通道退出休眠模式时自动清零。

EPSTS位（通道错误被动状态）

EPSTS位指示相关的CAN-FD通道是否已进入错误被动状态。

当CAN发送或接收计数器寄存器的值超过0x7F的值时，该位自动置位。

当相关CAN-FD通道退出错误被动状态或进入复位模式时，该位自动清零。

BOSTS bit (Channel Bus-Off Status)

BOSTS位指示相关CAN-FD通道是否已进入错误总线关闭状态。

当相关CAN传输错误计数寄存器的值超过0xFF且相关CAN-FD通道处于总线关闭状态（CAN传输错误计数寄存器>0xFF）时，该位自动设置。

当相关CAN-FD通道退出总线关闭状态时，该位自动清零。

TRMSTS位（通道发送状态）

TRMSTS位指示相关的CAN-FD通道是否正在发送消息。

当相关CAN-FD通道作为发送器节点运行或处于总线关闭状态时，该位自动设置。

当相关CAN-FD通道处于总线空闲状态或开始作为接收器节点运行时，该位自动清零。

RECSTS位（通道接收状态）

RECSTS位指示相关的CAN-FD通道是否正在接收消息。

当相关CAN-FD通道作为接收器节点运行时，该位自动设置。

当相关CAN-FD通道处于总线空闲状态或开始作为发送器节点运行时，该位自动清零。

COMSTS位（通道通信状态）

COMSTS位指示相关的CAN-FD通道是否已准备好进行通信。

当相关CAN-FD通道在退出复位或暂停模式后检测到11个连续隐性位后准备好执行通信时，该位自动置位。

当相关CAN-FD通道处于CH_RESET或CD_HALT模式时，该位自动清零。

Note: 该位在总线关闭状态下为1。

ESIF位（错误状态指示标志）

当ESI位被隐性采样以接收CAN报文且没有任何错误时，设置ESIF位。当在Loopback或Mirror模式下，自发的消息被认为是接收消息。

如果来自CAN-FD通道的设置与写访问清除同时发生，则设置该位。

该位通过写入0清零。当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

Note: 该位在经典CAN功能中不可用。

REC[7:0]位（接收错误计数）

REC[7:0]位根据接收时CAN-FD通道的错误状态递增或递减计数器值，并显示REC错误计数器的值。

总线关闭状态的值是不确定的。

These bits are cleared automatically when the CAN-FD module enters GL_RESET or the CAN-FD channel is in CH_RESET mode.

TEC[7:0] bits (Transmission Error Count)

The TEC[7:0] bits increment or decrement the counter value according to error status of the CAN-FD channel during transmission, and display the value of the TEC error counter.

Only write to these bits when in test mode and CAN-FD channel is in CH_HALT mode.

These bits are cleared automatically when CAN-FD module is in GL_RESET or CAN-FD channel is in CH_RESET mode.

32.2.6 CFDCnERFL : Channel n Error Flag Registers (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x000C + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CRCREG[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BEF	Bus Error Flag 0: Channel bus error not detected 1: Channel bus error detected	R/W
1	EWF	Error Warning Flag 0: Channel error warning not detected 1: Channel error warning detected	R/W
2	EPF	Error Passive Flag 0: Channel error passive not detected 1: Channel error passive detected	R/W
3	BOEF	Bus-Off Entry Flag 0: Channel bus-off entry not detected 1: Channel bus-off entry detected	R/W
4	BORF	Bus-Off Recovery Flag 0: Channel bus-off recovery not detected 1: Channel bus-off recovery detected	R/W
5	OVLF	Overload Flag 0: Channel overload not detected 1: Channel overload detected	R/W
6	BLF	Bus Lock Flag 0: Channel bus lock not detected 1: Channel bus lock detected	R/W
7	ALF	Arbitration Lost Flag 0: Channel arbitration lost not detected 1: Channel arbitration lost detected	R/W
8	SERR	Stuff Error 0: Channel stuff error not detected 1: Channel stuff error detected	R/W
9	FERR	Form Error 0: Channel form error not detected 1: Channel form error detected	R/W

当CAN-FD模块进入GL_RESET或CAN-FD通道处于CH_RESET mode.

TEC[7:0]位（传输错误计数）

TEC[7:0]位在传输过程中根据CAN-FD通道的错误状态递增或递减计数器值，并显示TEC错误计数器的值。

仅当处于测试模式且CAN-FD通道处于CH_HALT模式时写入这些位。

当CAN-FD模块处于GL_RESET或CAN-FD通道处于CH_RESET模式时，这些位会自动清除。

32.2.6 CFDCnERFL:通道n错误标志寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x000C + 0x10 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CRCREG[14:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BEF	总线错误标志 0：未检测到通道总线错误1：检测到通道总线错误	R/W
1	EWF	错误警告标志 0：未检测到通道错误警告1：检测到通道错误警告	R/W
2	EPF	错误被动标志 0：未检测到被动通道错误1：检测到被动通道错误	R/W
3	BOEF	总线关闭进入标志 0：未检测到通道总线关闭条目1：检测到通道总线关闭条目	R/W
4	BORF	总线关闭恢复标志 0：未检测到通道总线关闭恢复1：检测到通道总线关闭恢复	R/W
5	OVLF	过载标志 0：未检测到通道过载1：检测到通道过载	R/W
6	BLF	总线锁标志 0：未检测到通道总线锁定1：检测到通道总线锁定	R/W
7	ALF	仲裁丢失标志 0：未检测到通道仲裁丢失1：检测到通道仲裁丢失	R/W
8	SERR	东西错误 0：未检测到通道填充错误1：检测到通道填充错误	R/W
9	FERR	表格错误 0：未检测到通道形式错误1：检测到通道形式错误	R/W

Bit	Symbol	Function	R/W
10	AERR	Acknowledge Error 0: Channel acknowledge error not detected 1: Channel acknowledge error detected	R/W
11	CERR	CRC Error 0: Channel CRC error not detected 1: Channel CRC error detected	R/W
12	B1ERR	Bit 1 Error 0: Channel bit 1 error not detected 1: Channel bit 1 error detected	R/W
13	B0ERR	Bit 0 Error 0: Channel bit 0 error not detected 1: Channel bit 0 error detected	R/W
14	ADERR	Acknowledge Delimiter Error 0: Channel acknowledge delimiter error not detected 1: Channel acknowledge delimiter error detected	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W
30:16	CRCREG[14:0]	CRC Register value These bits show the CRC value calculated for the CAN2.0 CAN frame.	R
31	—	This bit is read as 0. The write value should be 0.	R/W

Each Channel Error Flag register shows the status of various error conditions detectable regardless of the setting of the related CAN Channel Error Interrupt Enable Register. It also shows the status of the various bus errors detectable by the CAN channel. Refer to the CAN specification (ISO 11898-1) to check when each error condition occurs.

For this register, only a single bit can be cleared by software. Do not use the bit clear instruction to clear the bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Example in assembler language to clear the CFDCnERFL.BEF bit:

mov.b #0x0FE, CFDCnERFL ;

BEF bit (Bus Error Flag)

The BEF bit indicates a detection of a CAN channel bus error state, flagged by bits [14:8] in this register.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

This bit is set automatically when a bus error is detected, and is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

EWF bit (Error Warning Flag)

The EWF bit indicates whether an error warning condition has been detected for the CAN channel.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

This bit is set automatically when either TEC or REC exceeds 0x5F.

The setting of this bit only occurs when the TEC or REC initially exceeds 0x5F. Therefore, if the TEC or REC remains > 0x5F and the EWF bit is cleared by software, it is not set again until both the TEC and REC go below 0x60 and either TEC or REC crosses over again from a value 0x5F to a value > 0x5F.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

EPF bit (Error Passive Flag)

The EPF bit indicates a detection of a CAN channel error passive state.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

Bit	Symbol	Function	R/W
10	AERR	确认错误 0：未检测到通道确认错误1：检测到通道确认错误	R/W
11	CERR	CRC Error 0：未检测到通道CRC错误1：检测到通道CRC错误	R/W
12	B1ERR	位1错误 0：未检测到通道位1错误1：检测到通道位1错误	R/W
13	B0ERR	位0错误 0：未检测到通道位0错误1：检测到通道位0错误	R/W
14	ADERR	确认分隔符错误 0：未检测到通道确认分隔符错误1：检测到通道确认分隔符错误	R/W
15	—	该位读取为0。写入值应为0。	R/W
30:16	CRCREG[14:0]	CRC寄存器值 这些位显示为CAN2.0CAN帧计算的CRC值。	R
31	—	该位读取为0。写入值应为0。	R/W

每个通道错误标志寄存器显示各种可检测到的错误条件的状态，无论相关CAN通道错误中断启用寄存器的设置如何。它还显示CAN通道可检测到的各种总线错误的状态。请参阅CAN规范(ISO11898-1)以检查每个错误情况何时发生。

对于该寄存器，软件只能清零一个位。不要使用位清除指令来清除位。使用MOV指令确保只清除指定位。其他位保持1。

用汇编语言清除CFDCnERFL.BEF位的示例：

mov.b #0x0FE, CFDCnERFL ;

BEF位（总线错误标志）

BEF位指示检测到CAN通道总线错误状态，由该寄存器中的位[14:8]标记。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

该位在检测到总线错误时自动置位，并在相关CAN-FD通道处于CH_RESET模式时自动清零。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

EWF位（错误警告标志）

EWF位指示是否检测到CAN通道的错误警告条件。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

当TEC或REC超过0x5F时，该位自动置位。

该位的设置仅在TEC或REC最初超过0x5F时发生。因此，如果TEC或REC保持>0x5F并且EWF位由软件清零，则不会再次设置，直到TEC和REC都低于0x60并且TEC或REC再次从值0x5F跨越到值>0x5F.

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除CAN-FD通道处于CH_RESET模式。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

EPF位（错误被动标志）

EPF位指示检测到CAN通道错误被动状态。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

This bit is set automatically when the CAN error state becomes error passive state.

The setting of this bit only occurs when the TEC or REC initially exceeds 0x7F. Therefore, if the TEC or REC remains > 0x7F and the bit is cleared by software, it is not set again until both the TEC and REC go below 0x80 and either TEC or REC crosses over again from a value ≤ 0x7F to a value > 0x7F.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

BOEF bit (Bus-Off Entry Flag)

The BOEF bit indicates a detection of a CAN channel bus-off entry state.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

This bit is set automatically when the CAN error state enters the bus-off state.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If a set condition occurs simultaneously with a clear condition, then the bit is set.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

BORF bit (Bus-Off Recovery Flag)

The BORF bit indicates a detection of a CAN channel bus-off recovery state.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

This bit is set automatically if CAN channel recovers from bus-off state in the following conditions:

- When CFDCnCTR.BOM is 00b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs
- When CFDCnCTR.BOM is 10b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs
- When CFDCnCTR.BOM is 11b and normal recovery (11 consecutive recessive bits x 128 times detected) occurs.

The bit is not set if CAN channel recovers from bus-off state in the following conditions:

- When CAN Reset mode is requested
- When CFDCnCTR.RTBO is set to 1 (the CAN channel returns to error active)
- When CFDCnCTR.BOM is 01b
- When CFDCnCTR.BOM is 11b and a halt request is asserted before the CAN channel reaches the end of the bus-off state.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If a set condition occurs simultaneously with a clear condition, the flag is set.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

OVLF bit (Overload Flag)

The OVLF flag indicates a detection of a CAN channel overload state.

The OVLF bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

This bit is set automatically when an overload condition is detected. If a set condition occurs simultaneously with a clear condition, then the bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

BLF bit (Bus Lock Flag)

The BLF bit indicates a detection of a CAN channel bus lock condition.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

This bit is set automatically when 32 consecutive dominant bits are detected on the CAN bus while the CAN channel is in Operation mode.

当CAN错误状态变为错误被动状态时，该位自动设置。

该位的设置仅在TEC或REC最初超过0x7F时发生。因此，如果TEC或REC保持>0x7F并且该位由软件清除，则不会再次设置，直到TEC和REC都低于0x80并且TEC或REC再次从值≤0x7F跨越到值>0x7F.

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除
CAN-FD通道处于CH_RESET模式。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

BOEF位（总线关闭进入标志）

BOEF位指示检测到CAN通道总线关闭进入状态。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

当CAN错误状态进入总线关闭状态时，该位自动置位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果设置条件与清除条件同时出现，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

BORF位（总线关闭恢复标志）

BORF位指示检测到CAN通道总线关闭恢复状态。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

如果CAN通道在以下情况下从总线关闭状态恢复，则该位自动设置：

●当CFDCnCTR.BOM为00b并且发生正常恢复（11个连续隐性位x检测128次）时

●当CFDCnCTR.BOM为10b且发生正常恢复（11个连续隐性位x128次检测）时

●当CFDCnCTR.BOM为11b并且发生正常恢复（11个连续隐性位x检测到128次）时。

如果CAN通道在以下情况下从总线关闭状态恢复，则不会设置该位：

●请求CAN复位模式时

●当CFDCnCTR.RTBO设置为1时（CAN通道返回错误激活）

●当CFDCnCTR.BOM为01b时

●当CFDCnCTR.BOM为11b并且在CAN通道到达总线关闭状态结束之前发出停止请求时。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果设置条件与清除条件同时出现，则设置标志。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

OVLF bit (Overload Flag)

OVLF标志指示检测到CAN通道过载状态。

OVLF位通过向其写入0来清除，并且只能由CAN-FD模块逻辑设置。写1无效。

当检测到过载情况时，该位自动置位。如果设置条件与清除条件同时出现，则设置该位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时写入该位。

BLF位（总线锁定标志）

BLF位指示检测到CAN通道总线锁定条件。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

当CAN通道在CAN总线上检测到32个连续显性位时，该位自动设置
操作模式。

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

It is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

ALF bit (Arbitration Lost Flag)

The ALF bit indicates a detection of a CAN channel bus arbitration lost condition.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

The bit is set automatically when an arbitration lost condition is detected on the CAN bus while the CAN channel is in Operation mode.

If a set condition occurs simultaneously with a clear condition, then the bit is set. It is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

SERR bit (Stuff Error)

The SERR bit indicates a detection of a CAN stuff error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a stuff error is detected. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

FERR bit (Form Error)

The FERR bit indicates a detection of a CAN form error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a form error is detected. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

AERR bit (Acknowledge Error)

The AERR bit indicates a detection of a CAN acknowledge error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除CAN-FD通道处于CH_RESET模式。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

当相关CAN-FD通道处于CH_RESET模式时，它会自动清除。

ALF位（仲裁丢失标志）

ALF位指示检测到CAN通道总线仲裁丢失情况。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

当CAN通道在CAN总线上检测到仲裁丢失条件时，该位自动设置操作模式。

如果设置条件与清除条件同时出现，则设置该位。相关时自动清除CAN-FD通道处于CH_RESET模式。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

SERR bit (Stuff Error)

SERR位指示检测到CAN填充错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到填充错误时，该位自动设置。如果CFDCnCTR.ERRD位为1，并且该位的置位和清除条件同时发生，则该位被置位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

FERR bit (Form Error)

FERR位指示检测到CAN格式错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到表格错误时，该位自动置位。如果CFDCnCTR.ERRD位为1，并且该位的置位和清除条件同时发生，则该位被置位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

AERR bit (Acknowledge Error)

AERR位指示检测到CAN确认错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when an acknowledge error is detected. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION.

CERR bit (CRC Error)

The CERR bit indicates a detection of a CAN CRC error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a CRC error is detected. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

B1ERR bit (Bit 1 Error)

The B1ERR bit indicates a detection of a recessive bit error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a recessive bit error (expected recessive bit, sampled as dominant bit) is detected. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

B0ERR bit (Bit 0 Error)

The B0ERR bit indicates a detection of a dominant bit error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a dominant bit error (expected dominant bit, sampled as recessive bit) is detected. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到确认错误时，该位自动置位。如果CFDCnCTR.ERRD位为1，并且该位的置位和清除条件同时发生，则该位被置位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION时才写入该位。

CERR bit (CRC Error)

CERR位指示检测到CANCRC错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到CRC错误时，该位自动置位。如果CFDCnCTR.ERRD位为1，并且该位的置位和清除条件同时发生，则该位被置位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

B1ERR bit (Bit 1 Error)

B1ERR位指示检测到隐性位错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到隐性位错误（预期的隐性位，采样为显性位）时，该位自动置位。如果CFDCnCTR.ERRD位为1，如果该位的设置和清除条件同时发生，则该位被设置。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

B0ERR bit (Bit 0 Error)

B0ERR位指示检测到显性位错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当检测到显性位错误（预期显性位，采样为隐性位）时，该位自动置位。如果CFDCnCTR.ERRD位为1，如果该位的设置和清除条件同时发生，则该位被设置。

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This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

ADERR bit (Acknowledge Delimiter Error)

The ADERR bit indicates a detection of an acknowledge delimiter bit error.

This bit is cleared by writing 0 to it, and can only be set by CAN-FD module logic. Writing 1 has no effect.

To clear this bit, use the following sequence:

1. Clear the corresponding flag bit.
2. Read if the flag bit is cleared.
3. If yes, continue, else go back to step 1.

This bit is set automatically when a form error is detected during the acknowledge delimiter state of frame transmission. If CFDCnCTR.ERRD bit is 1 and if the set and clear conditions occur at the same time for this bit, then this bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode. If CFDCnCTR.ERRD bit is 0 and the set and clear conditions occur at the same time for this bit, then it is cleared if a bit at CFDCnERFL[14:8] is already set. Otherwise, this bit is set if CFDCnERFL[14:8] is 0000000b.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

CRCREG[14:0] bits (CRC Register value)

The CRCREG[14:0] bits read the calculated CRC value when CFDCnCTR.CTME bit is 1 for the channel.

If CFDCnCTR.CTME bit is 0, then these bits are always read as 0.

These bits show the CAN2.0 CRC value calculated by the CAN-FD channel logic when the CTME bit is enabled.

The CFDCnERFL.CRCREG value is updated in the first bit of the CRC field of the CAN frame (reception and transmission).

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

32.2.7 CFDCnDCFG : Channel n Data Bitrate Configuration Register (n = 0, 1)

This register is not available in the classical CAN function.

Base address: CANFD = 0x400B_0000

Offset address: 0x1400 + 0x20 × n

Bit position:	31				27				24				19				16				12				8	7						0
Bit field:	—	—	—	—	DSJW[3:0]				—	—	—	—	DTSEG2[3:0]				—	—	—	—	DTSEG1[4:0]					DBRP[7:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DBRP[7:0]	Channel Data Baud Rate Prescaler Data Baud Rate Prescaler division ratio	R/W
12:8	DTSEG1[4:0]	Timing Segment 1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0x1E: 31 Tq 0x1F: 32 Tq	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

ADERR bit (Acknowledge Delimiter Error)

ADERR位指示检测到确认分隔符位错误。

该位通过写入0清零，并且只能由CAN-FD模块逻辑设置。写1无效。

要清除该位，请使用以下序列：

1.清除对应的标志位。

2.读取标志位是否被清除。

3.如果是，继续，否则返回步骤1。

当在帧传输的确认分隔符状态期间检测到格式错误时，该位自动设置。如果CFDCnCTR.ERRD位为1，如果该位的设置和清除条件同时发生，则该位被设置。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。如果CFDCnCTR.ERRD位为0并且该位的置位和清零条件同时发生，则如果CFDCnERFL[14:8]的位已经置位，则清零。否则，如果CFDCnERFL[14:8]为0000000b，则设置该位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

CRCREG[14:0]位（CRC寄存器值）

当通道的CFDCnCTR.CTME位为1时，CRCREG[14:0]位读取计算的CRC值。

如果CFDCnCTR.CTME位为0，则这些位始终读为0。

这些位显示CTME位使能时CAN-FD通道逻辑计算的CAN2.0CRC值。

CFDCnERFL.CRCREG值在CAN帧（接收和发送）的CRC字段的第一位更新。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

32.2.7 CFDCnDCFG:通道n数据比特率配置寄存器(n=0 1)

该寄存器在经典CAN功能中不可用。

Base address: CANFD = 0x400B_0000

Offset address: 0x1400 + 0x20 × n

Bit position:	31				27				24				19				16				12				8	7						0
Bit field:	—	—	—	—	DSJW[3:0]				—	—	—	—	DTSEG2[3:0]				—	—	—	—	DTSEG1[4:0]					DBRP[7:0]						
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DBRP[7:0]	通道数据波特率预分频器 数据波特率预分频比	R/W
12:8	DTSEG1[4:0]	时序段1 0x00: Reserved 0x01: 2 Tq 0x02: 3 Tq 0x03: 4 Tq ⋮ 0x1E: 31 Tq 0x1F: 32 Tq	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
19:16	DTSEG2[3:0]	Timing Segment 2 0x0: Reserved 0x1: 2 Tq ⋮ 0xE: 15 Tq 0xF: 16 Tq	R/W
23:20	—	These bits are read as 0. The write value should be 0.	R/W
27:24	DSJW[3:0]	Resynchronization Jump Width 0x0: 1 Tq 0x1: 2 Tq ⋮ 0xF: 16 Tq	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

Note: Tq means time quantum.

The Channel n Data Bitrate Configuration Register (n = 0, 1) configures the transmission/reception data baud rate parameters of the channels.

The channel of Classical-only mode does not perform configuration of this register.

DBRP[7:0] bits (Channel Data Baud Rate Prescaler)

The DBRP[7:0] bits define the peripheral bus clock periods contained in a time quantum.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

DTSEG1[4:0] bits (Timing Segment 1)

The DTSEG1[4:0] bits set the segment TSEG1 to compensate for edges on the CAN bus with a positive phase error. A value from 2 to 32 time quanta can be set.

The DTSEG1[4:0] bits are also used to set the propagation segment.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode. Do not write any other value to these bits. See section 32.4.1.2. CAN Bit Timing for more details.

DTSEG2[3:0] bits (Timing Segment 2)

The DTSEG2[3:0] bits set the segment TSEG2 to compensate for edges on the CAN bus with a negative phase error. A value from 2 to 16 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode. Do not write any other value to these bits.

DSJW[3:0] bits (Resynchronization Jump Width)

The DSJW[3:0] bits set the synchronization jump width. A value from 1 to 16 time quanta can be set.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

32.2.8 CFDCnFDCFG : Channel n CAN-FD Configuration Register (n = 0, 1)

This register is not available in the classical CAN function.

Bit	Symbol	Function	R/W
19:16	DTSEG2[3:0]	计时段2 0x0: Reserved 0x1: 2 Tq ⋮ 0xE: 15 Tq 0xF: 16 Tq	R/W
23:20	—	这些位被读取为0。写入值应为0。	R/W
27:24	DSJW[3:0]	再同步跳转宽度 0x0: 1 Tq 0x1: 2 Tq ⋮ 0xF: 16 Tq	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

Note: Tq表示时间量。

通道n数据比特率配置寄存器(n=0 1)配置通道的发送接收数据波特率参数。

Classical-only模式的通道不执行该寄存器的配置。

DBRP[7:0]位（通道数据波特率预分频器）

DBRP[7:0]位定义包含在时间片中的外围总线时钟周期。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

DTSEG1[4:0]位（时序段1）

DTSEG1[4:0]位设置段TSEG1以补偿CAN总线上的正相位误差边沿。可以设置2到32个时间量的值。

DTSEG1[4:0]位也用于设置传播段。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。不要将任何其他值写入这些位。请参阅第32.4.1.2节。CAN位时序了解更多详情。

DTSEG2[3:0]位（时序段2）

DTSEG2[3:0]位设置段TSEG2以补偿CAN总线上具有负相位误差的边沿。可以设置2到16个时间量子的值。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。不要将任何其他值写入这些位。

DSJW[3:0]位（再同步跳转宽度）

DSJW[3:0]位设置同步跳转宽度。可以设置1到16个时间量的值。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

32.2.8 CFDCnFDCFG:通道nCAN-FD配置寄存器(n=0 1)

该寄存器在经典CAN功能中不可用。

Base address: CANFD = 0x400B_0000

Offset address: 0x1404 + 0x20 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDTE	CLOE	REFE	FDOE	—	GWBRS	GWFDF	GWEN	TDCO[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0][2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EOCCFG[2:0]	Error Occurrence Counter Configuration 0 0 0: All transmitter or receiver CAN frames 0 0 1: All transmitter CAN frames 0 1 0: All receiver CAN frames 0 1 1: Reserved 1 0 0: Only transmitter or receiver CAN-FD data-phase (fast bits) 1 0 1: Only transmitter CAN-FD data-phase (fast bits) 1 1 0: Only receiver CAN-FD data-phase (fast bits) 1 1 1: Reserved	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	TDCOC*1	Transceiver Delay Compensation Offset Configuration 0: Measured + offset 1: Offset-only	R/W
9	TDCE*1	Transceiver Delay Compensation Enable 0: Transceiver delay compensation disabled 1: Transceiver delay compensation enabled	R/W
10	ESIC*1	Error State Indication Configuration 0: The ESI bit in the frame represents the error state of the node itself 1: The ESI bit in the frame represents the error state of the message buffer if the node itself is not in error passive. If the node is in error passive, then the ESI bit is driven by the node itself.	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
23:16	TDCO[7:0]*1	Transceiver Delay Compensation Offset	R/W
24	GWEN*1	CAN2.0, CAN-FD Multi-Gateway Enable 0: Multi-gateway disabled 1: Multi-gateway enable	R/W
25	GWFDF*1	Gateway FDF Configuration Bit 0: Gateway frame is transmitted as Classical CAN frame 1: Gateway frame is transmitted as CAN-FD frame	R/W
26	GWBRS*1	Gateway BRS Configuration Bit 0: Gateway frame is transmitted with BRS = 0 1: Gateway frame is transmitted with BRS = 1	R/W
27	—	This bit is read as 0. The write value should be 0.	R/W
28	FDOE*1	FD-Only Enable 0: FD-only mode disabled 1: FD-only mode enabled	R/W
29	REFE	RX Edge Filter Enable 0: RX edge filter disabled 1: RX edge filter enabled	R/W

Base address: CANFD = 0x400B_0000

Offset address: 0x1404 + 0x20 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDTE	CLOE	REFE	FDOE	—	GWBRS	GWFDF	GWEN	TDCO[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ESIC	TDCE	TDCOC	—	—	—	—	—	EOCCFG[2:0][2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	EOCCFG[2:0]	错误发生计数器配置 000：所有发送器或接收器CAN帧001：所有发送器CAN帧010：所有接收器CAN帧011：保留100：仅发送器或接收器CAN-FD数据阶段（快速位）101：仅发送器CAN-FD数据阶段（快速位）110：仅接收器CAN-FD数据阶段（快速位）111：保留	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	TDCOC*1	收发器延迟补偿偏移配置 0：测量+偏移1：仅偏移	R/W
9	TDCE*1	收发器延迟补偿使能 0：收发器延迟补偿禁用1：收发器延迟补偿启用	R/W
10	ESIC*1	错误状态指示配置 0：帧中的ESI位表示节点本身的错误状态1：帧中的ESI位表示消息缓冲区的错误状态，如果 节点本身没有错误被动。如果节点处于被动错误，则ESI位由节点本身驱动。	R/W
11	—	该位读取为0。写入值应为0。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
23:16	TDCO[7:0]*1	收发器延迟补偿偏移	R/W
24	GWEN*1	CAN2.0, CAN-FD Multi-Gateway Enable 0：禁用多网关1：启用多网关	R/W
25	GWFDF*1	网关FDF配置位 0：网关帧作为经典CAN帧传输1：网关帧作为CAN-FD帧传输	R/W
26	GWBRS*1	网关BRS配置位 0：发送网关帧，BRS=01：发送网关帧，BRS=1	R/W
27	—	该位读取为0。写入值应为0。	R/W
28	FDOE*1	FD-Only Enable 0：FD-only模式禁用1：FD-only模式启用	R/W
29	REFE	RX边缘滤波器启用 0：RX边缘过滤器禁用1：RX边缘过滤器启用	R/W

Bit	Symbol	Function	R/W
30	CLOE*1	Classical CAN-Only Enable 0: Classical-only mode disabled 1: Classical-only mode enabled	R/W
31	CFDTE	CAN-FD Frame Distinction Enable 0: CAN-FD frame distinction disabled 1: CAN-FD frame distinction enabled	R/W

Note 1. These bits are not available in the classical CAN function.

The Channel n CAN-FD Configuration Register (n = 0, 1) configures which communication direction (transmitter/receiver) errors are counted.

EOCCFG[2:0] bits (Error Occurrence Counter Configuration)

The EOCCFG[2:0] bits select which type of CAN frame configuration and direction, including protocol errors are counted.

Do not write to these bits in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

TDCOC bit (Transceiver Delay Compensation Offset Configuration)*1

The TDCOC bit selects which offset is used when defining the position of the secondary sample point (SSP) for the CAN-FD channel. If the bit is set to 0, the position of the SSP is the measured transceiver delay plus the fixed offset. If the bit is 1, the position of the SSP is defined only by the offset.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical-only mode.

TDCE bit (Transceiver Delay Compensation Enable)*1

The TDCE bit enables the transceiver delay compensation for the CAN-FD channel.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical-only mode.

ESIC bit (Error State Indication Configuration)*1

Bus controllers that are used as CAN-to-CAN gateway support that in every forwarded CAN-FD message. The ESI flag does not change to reflect the status of the gateway, bridge, or router but instead the flag is sent as it was in the original message.

The ESIC bit controls the transmission of either the ESI flag information or the message of ESI flag information (CFDCFFDCSTSn.CFESI or CFDTMFDCTRn.TMESI).

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode. Do not set this bit when in Classical-only mode.

TDCO[7:0] bits (Transceiver Delay Compensation Offset)*1

The TDCO[7:0] bits set the secondary sample point offset. How this value is used, depends on the CFDCnFDCFG.TDCOC setting.

If CFDCnFDCFG.TDCOC = 0, the transceiver delay compensation result is equal to the Trv_Delay (measured delay) + the value in CFDCnFDCFG.TDCO, rounded down to the nearest integer number of time quanta. Otherwise, the result is equal to the value in CFDCnFDCFG.TDCO. See section 32.4.1.5. Transmitter Delay Compensation for details on how CFDCnFDCFG.TDCO is used.

The actual offset value is interpreted as TDCO + 1. For example, if 4 is set in TDCO, the offset is 5 clock cycles. Clock cycle is 1 cycle of CAN channel DLL clock.

Do not write to the TDCO[7:0] bits in CH_OPERATION or CH_SLEEP mode.

Bit	Symbol	Function	R/W
30	CLOE*1	经典CAN-Only启用 0：仅经典模式禁用1：仅经典模式启用	R/W
31	CFDTE	CAN-FD帧区分启用 0：禁用CAN-FD帧识别1：启用CAN-FD帧识别	R/W

注1.这些位在经典CAN功能中不可用。

通道nCAN-FD配置寄存器(n=0 1)配置计算哪个通信方向（发送器接收器）错误。

EOCCFG[2:0]位（错误发生计数器配置）

EOCCFG[2:0]位选择计算哪种类型的CAN帧配置和方向，包括协议错误。

不要在CH_OPERATION或CH_SLEEP模式下写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

TDCOC位（收发器延迟补偿偏移配置）*1

TDCOC位选择在为CAN定义辅助采样点(SSP)的位置时使用哪个偏移量
FD频道。如果该位设置为0，则SSP的位置是测量的收发器延迟加上固定偏移。如果该位为1，则SSP的位置仅由偏移量定义。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。不要设置该位时
Classical-only mode.

TDCE位（收发器延迟补偿启用）*1

TDCE位使能CAN-FD通道的收发器延迟补偿。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。不要设置该位时
Classical-only mode.

ESIC位（错误状态指示配置）*1

用作CAN-to-CAN网关的总线控制器在每个转发的CAN-FD消息中都支持这一点。ESI标志不会更改以反映网关、网桥或路由器的状态，而是按照原始消息中的状态发送标志。

ESIC位控制ESI标志信息或ESI标志信息消息（CFDCFFDCSTSn.CFESI或CFDTMFDCTRn.TMESI）的传输。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。不要设置该位时
Classical-only mode.

TDCO[7:0]位（收发器延迟补偿偏移）*1

TDCO[7:0]位设置辅助采样点偏移。该值的使用方式取决于CFDCnFDCFG.TDCOC设置。

如果CFDCnFDCFG.TDCOC=0，则收发器延迟补偿结果等于Trv_Delay（测量延迟）+CFDCnFDCFG.TDCO中的值，向下舍入到最接近的时间量子整数。否则，结果等于CFDCnFDCFG.TDCO中的值。请参阅第32.4.1.5节。有关如何使用CFDCnFDCFG.TDCO的详细信息，请参阅发送器延迟补偿。

实际偏移值被解释为TDCO+1。例如，如果TDCO设置为4，则偏移为5个时钟周期。时钟周期为CAN通道DLL时钟的1个周期。

请勿在CH_OPERATION或CH_SLEEP模式下写入TDCO[7:0]位。

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode. Do not set to this bit when in Classical-only mode.

GWEN bit (CAN2.0, CAN-FD Multi-Gateway Enable)*1

When the GWEN bit is enabled, a multi-gateway is enabled. Message received on one node can be routed to another node using the COM FIFO when they are configured as gateway FIFO (CFDCFCCn.CFM = 10b). Furthermore, when TX Queue is set as gateway mode, the message received on one node can be stored in TX Queue and can be sent to another node.

The FDF and BRS bits of the routed message can be changed by the configuration value of the CFDCnFDCFG.GWFDF and CFDCnFDCFG.GWBRS bits. By this, the transmitted value of these bits can be replaced.

Example :

CFDCnFDCFG.GWEN = 1 on channel y

CFDCnFDCFG.GWFDF = 1

If a Classical CAN frame is received on channel x and routed to a gateway FIFO or TX Queue of channel y. Then this CAN frame is sent on channel y as a CAN-FD frame because of the CFDCnFDCFG.GWFDF bit.

Table 32.3 shows how the message information is changed depending on the received and configured data.

Table 32.3 Modified message information by received and configured data

Routed CAN frame	Routed received DLC	CAN BRS bit	Configured CFDCnFDCFG.GWFDF bit	Gateway message DLC	Gateway message BRS bit	Gateway message frame type
CAN2.0	≤ 8	N/A	1	≤ 8	Based on configuration of CFDCnFDCFG.GWBRS	FD
CAN2.0	> 8	N/A	1	= 8	Based on configuration of CFDCnFDCFG.GWBRS	FD
FD	≤ 8	None	1	≤ 8	Based on configuration of CFDCnFDCFG.GWBRS	FD
FD	> 8	None	1	> 8	Based on configuration of CFDCnFDCFG.GWBRS	FD
CAN2.0	≤ 8	N/A	0	≤ 8	N/A	CAN2.0
CAN2.0	> 8	N/A	0	> 8	N/A	CAN2.0
FD	≤ 8	None	0	≤ 8	N/A	CAN2.0
FD	> 8	None	0	= 8	N/A	CAN2.0

Note: This gateway is limited to an 8-byte data payload for different frame type. If routing and target frame type is the same, the data length code (DLC) value remains the same. If the source frame is a CAN-FD with more than 8 data bytes, then on classical destination node, the data payload is reduced to 8 bytes. Only the first 8 bytes of data perform gateway transmission.

Note: Transmission buffers other than the gateway FIFO are not affected by this feature.

Do not route remote frames through the gateway when CFDCnFDCFG.GWEN is set. When a destination node is CFDCnFDCFG.FDOE = 1, set CFDCnFDCFG.GWEN and CFDCnFDCFG.GWFDF to 1. When a destination node is CFDCnFDCFG.CLOE = 1, set CFDCnFDCFG.GWEN=1 and CFDCnFDCFG.GWFDF = 0.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CAN-FD channel is in CH_RESET mode.

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。在仅经典模式下不要设置此位。

GWEN位（CAN2.0、CAN-FD多 网关使能）*1

启用GWEN位时，启用多网关。当一个节点上接收到的消息被配置为网关FIFO(CFDCFCCn.CFM=10b)时，可以使用COMFIFO将它们路由到另一个节点。此外，当TXQueue设置为网关模式时，一个节点上接收到的消息可以存储在TXQueue中，并可以发送到另一个节点。

路由消息的FDF和BRS位可以通过CFDCnFDCFG.GWFDF和CFDCnFDCFG.GWBRS位的配置值进行更改。这样，可以替换这些位的传输值。

Example :

CFDCnFDCFG.GWEN=1在通道y

CFDCnFDCFG.GWFDF = 1

如果在通道x上接收到经典CAN帧并路由到通道y的网关FIFO或TX队列。然后，由于CFDCnFDCFG.GWFDF位，此CAN帧在通道y上作为CAN-FD帧发送。

表32.3显示了如何根据接收和配置的数据更改消息信息。

Table 32.3 通过接收和配置的数据修改消息信息

路由CAN帧	路由接收DLC	CANBRS位	Configured CFDCnFDCFG.GWFDF bit	网关消息DLC	网关消息BRS位	网关消息帧类型
CAN2.0	≤ 8	N/A	1	≤ 8	基于CFDCnFDCFG.G的配置 WBRS	FD
CAN2.0	> 8	N/A	1	= 8	基于CFDCnFDCFG.G的配置 WBRS	FD
FD	≤ 8	None	1	≤ 8	基于CFDCnFDCFG.G的配置 WBRS	FD
FD	> 8	None	1	> 8	基于CFDCnFDCFG.G的配置 WBRS	FD
CAN2.0	≤ 8	N/A	0	≤ 8	N/A	CAN2.0
CAN2.0	> 8	N/A	0	> 8	N/A	CAN2.0
FD	≤ 8	None	0	≤ 8	N/A	CAN2.0
FD	> 8	None	0	= 8	N/A	CAN2.0

Note: 此网关仅限于不同帧类型的8字节数据有效负载。如果路由和目标帧类型相同，则数据长度代码(DLC)值保持不变。如果源帧是具有超过8个数据字节的CAN-FD，那么在经典目标节点上，数据有效负载减少到8个字节。只有前8个字节的数据执行网关传输。

Note: 网关FIFO以外的传输缓冲区不受此功能的影响。

当设置了CFDCnFDCFG.GWEN时，不要通过网关路由远程帧。当目标节点是CFDCnFDCFG.FDOE=1，设置CFDCnFDCFG.GWEN和CFDCnFDCFG.GWFDF为1。当目的节点为CFDCnFDCFG.CLOE=1，设置CFDCnFDCFG.GWEN=1和CFDCnFDCFG.GWFDF=0。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。

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GWFDF bit (Gateway FDF Configuration Bit)*1

When the GWEN bit is set to 1, the FDF bit of the transmitting gateway frame is replaced by the value of the GWFDF bit.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to these bits when the CAN-FD module is in CH_RESET mode. Do not set this bit when in Classical-only mode.

GWBRS bit (Gateway BRS Configuration Bit)*1

When the GWEN bit is set to 1, the BRS bit of the transmitting gateway frame is replaced by the value of CFDCnFDCFG.GWBRS.

In classical CAN frames, the GWBRS bit is invalid.

Do not write to this bit in CH_OPERATION or CH_SLEEP mode.

Only write to this bit when the related CAN-FD channel is in CH_RESET mode. Do not set this bit when in Classical-only mode.

FDOE bit (FD-Only Enable)*1

The FDOE bit enables the reception and transmission of CAN-FD-only frames. If enabled, communication in Classical CAN frame format is disabled. Transmission of Classical CAN frames is not possible because the FDF bit of the message buffer is a don't care (CFDCFFDCSTSn.CFFDF/CFDTMFDCTRn.TMFDF).

If messages with Classical CAN frame format are received, the protocol controller treats them as invalid frames and response with error frames. When a Classical CAN frame is configured for transmitting, the FDF bit is sent as recessive, therefore an FD frame is sent. If the data length code (DLC) is configured of greater than 8 bytes, the remaining data bytes are padded with 0xCC.

The FDOE bit cannot be written in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Do not set CFDCnFDCFG.FDOE and CFDCnFDCFG.CLOE simultaneously.

REFE bit (RX Edge Filter Enable)

The REFE bit enables the RX edge filter during the IDLE detection (bus integration). When the bit is enabled, two consecutive dominant time quanta are required to detect a synchronization edge.

The REFE bit cannot be written in CH_OPERATION, CH_HALT and CH_SLEEP mode. Do not set this bit when in Classical-only mode and when CFDCnFDCFG.CFDTE = 0 (disabled CAN-FD frame distinction).

CLOE bit (Classical CAN-Only Enable)*1

The CLOE bit enables the Classical CAN-only mode. If this bit is 1, the protocol controller can only send classical frames and response with a form or CRC error on FD frames.

Do not set CFDCnFDCFG.CLOE and CFDCnFDCFG.FDOE simultaneously.

CFDCnFDCFG.CLOE	CFDCnFDCFG.FDOE	Channel mode
0	0	CAN-FD mode
0	1	FD-only mode
1	0	Classical CAN-only mode
1	1	Reserved

The CANFD mode is available only for CANFD supported product.

Do not write to this bit in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Only write to these bits when the CAN-FD channel is in CH_RESET mode.

CFDTE bit (CAN-FD Frame Distinction Enable)

The CFDTE bit enables the CAN-FD frame distinction function. The CFDTE bit is required for Classical CAN-only mode (CFDCnFDCFG.CLOE = 1).

If this bit is 0, the protocol controller can only send Classical frames and response with a Form or CRC error on FD frames.

GWFDF位（网关FDF配置位）*1

当GWEN位设置为1时，发送网关帧的FDF位被GWFDF位的值替换。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当CAN-FD模块处于CH_RESET模式时才写入这些位。在仅经典模式下不要设置该位。

GWBRS位（网关BRS配置位）*1

当GWEN位设置为1时，发送网关帧的BRS位被替换为CFDCnFDCFG.GWBRS.

在经典CAN帧中，GWBRS位无效。

请勿在CH_OPERATION或CH_SLEEP模式下写入该位。

仅当相关CAN-FD通道处于CH_RESET模式时才写入该位。在仅经典模式下不要设置该位。

FDOE bit (FD-Only Enable)*1

FDOE位启用CAN-FD-only帧的接收和发送。如果启用，以经典方式进行通信CAN帧格式被禁用。传统CAN帧的传输是不可能的，因为消息缓冲区的FDF位是无关紧要的(CFDCFFDCSTSn.CFFDFCFDTMFDCTRn.TMFDF)。

如果接收到具有经典CAN帧格式的消息，协议控制器会将其视为无效帧并以错误帧响应。当经典CAN帧配置为发送时，FDF位作为隐性发送，因此发送FD帧。如果数据长度代码(DLC)配置为大于8个字节，则剩余的数据字节用0xCC填充。

FDOE位不能在CH_OPERATION、CH_HALT或CH_SLEEP模式下写入。

不要同时设置CFDCnFDCFG.FDOE和CFDCnFDCFG.CLOE。

REFE位（RX边沿过滤器使能）

在空闲检测（总线集成）期间，REFE位使能RX边沿滤波器。当该位使能时，需要两个连续的显性时间量来检测同步边沿。

在CH_OPERATION、CH_HALT和CH_SLEEP模式下不能写入REFE位。不要设置该位时仅经典模式和当CFDCnFDCFG.CFDTE=0（禁用CAN-FD帧区分）时。

CLOE bit (Classical CAN-Only Enable)*1

CLOE位启用经典CAN-only模式。如果该位为1，则协议控制器只能发送经典帧并在FD帧上带有格式或CRC错误的响应。

不要同时设置CFDCnFDCFG.CLOE和CFDCnFDCFG.FDOE。

CFDCnFDCFG.CLOE	CFDCnFDCFG.FDOE	频道模式
0	0	CAN-FD mode
0	1	FD-only mode
1	0	经典CAN-only模式
1	1	Reserved

CANFD模式仅适用于支持CANFD的产品。

请勿在CH_OPERATION、CH_HALT或CH_SLEEP模式下写入该位。

仅当CAN-FD通道处于CH_RESET模式时才写入这些位。

CFDTE位（CAN-FD帧区分使能）

CFDTE位使能CAN-FD帧识别功能。经典CAN-only模式(CFDCnFDCFG.CLOE=1)需要CFDTE位。

如果该位为0，协议控制器只能发送Classical帧和响应FD帧上的Form或CRC错误。

If this bit is 1, the protocol controller behaves according to the ISO 11898-1 (DIS 2015) specification. If the FDF bit is detected recessive, then the protocol controller enters the protocol exception state, and attempts to integrate back to the CAN communication.

Do not write this bit in CH_OPERATION, CH_HALT or CH_SLEEP mode.

Only write to these bits when the related CAN-FD channel is in CH_RESET mode.

Note 1. These bits are not available in the classical CAN function.

32.2.9 CFDCnFDCTR : Channel n CAN-FD Control Register (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1408 + 0x20 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOCCLR	Error Occurrence Counter Clear 0: No error occurrence counter clear 1: Clear error occurrence counter	R/W
1	SOCCLR	Successful Occurrence Counter Clear 0: No successful occurrence counter clear 1: Clear successful occurrence counter	R/W
31:2	—	These bits are read as 0. The write value should be 0.	R/W

The Channel n CAN-FD Control Register (n = 0, 1) controls the error and successful occurrence counters.

EOCCLR bit (Error Occurrence Counter Clear)

The EOCCLR bit is used to clear the error occurrence counter.

Do not write to this bit in CH_SLEEP or CH_RESET mode. The read value is always 0.

This bit is cleared automatically by the RS-CAN-FD logic and when the related CAN-FD channel is in CH_RESET mode.

SOCCLR bit (Successful Occurrence Counter Clear)

The SOCCLR bit is used to clear the successful occurrence counter.

Do not write to this bit in CH_SLEEP or CH_RESET mode. The read value is always 0.

This bit is cleared automatically by the RS-CAN-FD logic and when the related CAN-FD channel is in CH_RESET mode.

如果该位为1，则协议控制器的行为符合ISO11898-1(DIS2015)规范。如果检测到FDF位为隐性，则协议控制器进入协议异常状态，并尝试集成回CAN通信。

请勿在CH_OPERATION、CH_HALT或CH_SLEEP模式下写入该位。

仅当相关CAN-FD通道处于CH_RESET模式时才写入这些位。

注1.这些位在经典CAN功能中不可用。

32.2.9 CFDCnFDCTR:通道nCAN-FD控制寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1408 + 0x20 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOCCLR	EOCCLR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOCCLR	错误发生计数器清除 0：不清除错误发生计数器1：清除错误发生计数器	R/W
1	SOCCLR	成功发生计数器清除 0：无成功发生计数器清零1：清零成功发生计数器	R/W
31:2	—	这些位被读取为0。写入值应为0。	R/W

通道nCAN-FD控制寄存器(n=0 1)控制错误和成功发生计数器。

EOCCLR位（错误发生计数器清除）

EOCCLR位用于清除错误发生计数器。

请勿在CH_SLEEP或CH_RESET模式下写入该位。读取值始终为0。

当相关CAN-FD通道处于CH_RESET模式时，该位由RS-CAN-FD逻辑自动清零。

SOCCLR位（成功发生计数器清零）

SOCCLR位用于清除成功发生计数器。

请勿在CH_SLEEP或CH_RESET模式下写入该位。读取值始终为0。

当相关CAN-FD通道处于CH_RESET模式时，该位由RS-CAN-FD逻辑自动清零。

32.2.10 CFDCnFDSTS : Channel n CAN-FD Status Register (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x140C + 0x20 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SOC[7:0]								EOC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TDCVF	—	—	—	—	—	SOCO	EOCO	TDCR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TDCR[7:0]*1	Transceiver Delay Compensation Result	R
8	EOCO	Error Occurrence Counter Overflow 0: Error occurrence counter has not overflowed 1: Error occurrence counter has overflowed	R/W
9	SOCO	Successful Occurrence Counter Overflow 0: Successful occurrence counter has not overflowed 1: Successful occurrence counter has overflowed	R/W
14:10	—	These bits are read as 0. The write value should be 0.	R/W
15	TDCVF*1	Transceiver Delay Compensation Violation Flag 0: Transceiver delay compensation violation has not occurred 1: Transceiver delay compensation violation has occurred	R/W
23:16	EOC[7:0]	Error Occurrence Counter These bits show the error occurrence counter value.	R
31:24	SOC[7:0]	Successful occurrence counter register These bits show the successful occurrence counter value.	R

Note 1. These bits are not available in the classical CAN function.

The Channel n CAN-FD Status Register (n = 0, 1) indicates the transceiver compensation delay result and its related FIFO message lost status.

TDCR[7:0] bits (Transceiver Delay Compensation Result)

The TDCR[7:0] bits are set when the transceiver delay has been measured.

The measured delay is a multiple of the CAN channel DLL clock. The result depends on the CFDCnFDCFG.TDCOC configuration and the offset value in CFDCnFDCFG.TDCO. See section 32.4.1.5. Transmitter Delay Compensation for details on how this value is derived.

The TDCR[7:0] bits are updated at the falling edge between FDF and the RES bit when CFDCnFDCFG.TDCOC = 0 and the transceiver delay compensation is enabled (CFDCnFDCFG.TDCE = 1).

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Note: These bits are not available in the classical CAN function.

EOCO bit (Error Occurrence Counter Overflow)

The EOCO bit indicates whether the related CAN channel error occurrence counter has overflowed. This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when CFDCnFDSTS.EOC is 0xFF and a CAN bus error is detected based on the configuration defined in CFDCnFDCFG.EOCCFG.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

32.2.10 CFDCnFDSTS:通道nCAN-FD状态寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x140C + 0x20 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	SOC[7:0]								EOC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TDCVF	—	—	—	—	—	SOCO	EOCO	TDCR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TDCR[7:0]*1	收发器延迟补偿结果	R
8	EOCO	错误发生计数器溢出 0：错误发生计数器未溢出1：错误发生计数器已溢出	R/W
9	SOCO	成功发生计数器溢出 0：成功发生计数器未溢出1：成功发生计数器已溢出	R/W
14:10	—	这些位被读取为0。写入值应为0。	R/W
15	TDCVF*1	收发器延迟补偿违规标志 0：未发生收发器延迟补偿违规1：已发生收发器延迟补偿违规	R/W
23:16	EOC[7:0]	错误发生计数器 这些位显示错误发生计数器的值。	R
31:24	SOC[7:0]	成功发生计数器寄存器 这些位显示成功发生计数器的值。	R

注1.这些位在经典CAN功能中不可用。

通道nCAN-FD状态寄存器(n=0 1)指示收发器补偿延迟结果及其相关的FIFO消息丢失状态。

TDCR[7:0]位（收发器延迟补偿结果）

TDCR[7:0]位在测量到收发器延迟后置位。

测得的延迟是CAN通道DLL时钟的倍数。结果取决于CFDCnFDCFG.TDCOC配置和CFDCnFDCFG.TDCO中的偏移值。请参阅第32.4.1.5节。TransmitterDelayCompensation了解有关如何得出此值的详细信息。

当CFDCnFDCFG.TDCOC=0并且使能收发器延迟补偿(CFDCnFDCFG.TDCE=1)时，TDCR[7:0]位在FDF和RES位之间的下降沿更新。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

Note: 这些位在经典CAN功能中不可用。

EOCO位（错误发生计数器溢出）

EOCO位指示相关的CAN通道错误发生计数器是否溢出。该位通过写入0清零。写1无效。

当CFDCnFDSTS.EOC为0xFF且根据CFDCnFDCFG.EOCCFG中定义的配置检测到CAN总线错误时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

SOCO bit (Successful Occurrence Counter Overflow)

The SOCO bit indicates whether the related CAN channel successful occurrence counter has overflowed. This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when CFDCnFDSTS.SOC is 0xFF and a successful message reception or successful message transmission occurs.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Write to this bit only when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

TDCVF bit (Transceiver Delay Compensation Violation Flag)

The CAN-FD module captures internally the transmitted data bit-by-bit. This data is then compared against the received CAN bus level which is delayed by the transceiver loop delay.

The transceiver delay has some variations depending on the physical parameters such as temperature. The result bit CFDCnFDSTS.TDCR is updated by each message. However, temporary maximum delay violation could be missed. Therefore, the TDCVF bit captures this violation.

This bit is cleared by writing 0 to it. Writing 1 has no effect.

This bit is set automatically when the transceiver delay compensation is greater than the maximum delay compensation (6 data bit times - 2 clk_dlc) and the internal bit is overrun.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

Note: This bit is not available in the classical CAN function.

EOC[7:0] bits (Error Occurrence Counter)

The EOC[7:0] bits are used together with the SOC[7:0] bits to support an option for host-controlled fall-back to payload bit rate identical to arbitration bit rate when messages utilizing the reduced payload bit length have significant higher error rates compared to other messages.

This higher error rate can be detected depending on the configuration of the CFDCnFDCFG.EOCCFG bits.

The EOC[7:0] bits are set only by CAN-FD module logic. These bits are cleared by writing 1 to CFDCnFDCTR.EOCCLR. Writing any other value has no effect.

These bits are updated when an error occurs, according to the configuration of the CFDCnFDCFG.EOCCFG bits. When the counter reaches the value of 0xFF, the update stops.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

SOC[7:0] bits (Successful occurrence counter register)

The SOC[7:0] bits are used together with the EOC[7:0] bits to support an option for host-controlled fall-back to payload bit rate identical to arbitration bit rate when messages utilizing the reduced payload bit length have significant higher error rates compared to other messages.

The SOC[7:0] bits are set only by CAN-FD module logic. Writing any other value has no effect.

These bits are updated when the occurrence of any error-free messages on the bus is detected through reception or transmission. When the counter reaches the value of 0xFF, the update stops.

Note: In Loopback mode, the counter is incremented twice.

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

SOCO位（成功发生计数器溢出）

SOCO位指示相关CAN通道成功发生计数器是否溢出。该位通过写入0清零。写1无效。

当CFDCnFDSTS.SOC为0xFF且成功接收消息或成功发送消息时，该位自动置位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

TDCVF位（收发器延迟补偿违规标志）

CAN-FD模块在内部逐位捕获传输的数据。然后将该数据与接收到的数据进行比较
由收发器环路延迟延迟的CAN总线电平。

收发器延迟有一些变化，具体取决于温度等物理参数。结果位CFDCnFDSTS.TDCR由每个消息更新。但是，
可能会错过临时最大延迟违规。
因此，TDCVF位捕获此违规。

该位通过写入0清零。写1无效。

当收发器延迟补偿大于最大延迟补偿（6个数据位乘以2个clk_dlc）并且内部位溢出时，该位自动置位。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

Note: 该位在经典CAN功能中不可用。

EOC[7:0]位（错误发生计数器）

EOC[7:0]位与SOC[7:0]位一起使用，以支持当使用减少的有效负载位长度的消息具有重要与其他消息相比，错误率更高。

根据CFDCnFDCFG.EOCCFG位的配置，可以检测到这种较高的错误率。

EOC[7:0]位仅由CAN-FD模块逻辑设置。这些位通过向CFDCnFDCTR.EOCCLR写入1来清除。
写入任何其他值均无效。

根据CFDCnFDCFG.EOCCFG位的配置，这些位在发生错误时更新。当计数器达到0xFF的值时，更新停止。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

SOC[7:0]位（成功发生计数器寄存器）

SOC[7:0]位与EOC[7:0]位一起使用，以支持主机控制的回退到与仲裁比特率相同的有效负载比特率选项，当使用减少的有效负载位长度的消息具有显着性时与其他消息相比，错误率更高。

SOC[7:0]位仅由CAN-FD模块逻辑设置。写入任何其他值均无效。

当通过接收或传输检测到总线上出现任何无错误消息时，这些位将被更新。当计数器达到0xFF的值时，
更新停止。

Note: 在环回模式下，计数器增加两次。

These bits are cleared by writing 1 to CFDCnFDCTR.SOCCLR.

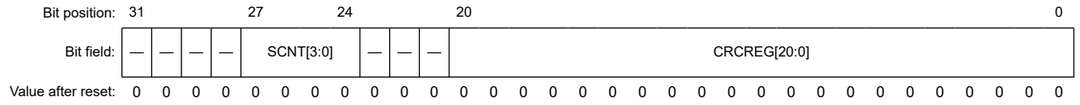
These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

32.2.11 CFDCnFDCRC : Channel n CAN-FD CRC Register (n = 0, 1)

This register is not available in the classical CAN function.

Base address: CANFD = 0x400B_0000

Offset address: 0x1410 + 0x20 × n



Bit	Symbol	Function	R/W
20:0	CRCREG[20:0]	CRC Register value These bits show the CRC value calculated for the CAN-FD frame.	R
23:21	—	These bits are read as 0. The write value should be 0.	R/W
27:24	SCNT[3:0]	Stuff bit count These bits shows the stuff bit count (mod 8) for the CAN-FD frame.	R
31:28	—	These bits are read as 0. The write value should be 0.	R/W

The Channel n CAN-FD CRC Register (n = 0, 1) holds the CRC value calculated for the CAN-FD frame.

CRCREG[20:0] bits (CRC Register value)

The CRCREG[20:0] bits contain the CRC value calculated by the CAN-FD channel logic when the CFDCnCTR.CTME bit is enabled.

The CFDCnFDCRC.CRCREG value is updated in the first bit of the CRC field of the CAN-FD frame (reception and transmission).

When the CFDCnCTR.CTME bit is 0, the CRCREG[20:0] bits are always read as 0.

When bit 17th of the CRC field is used, CRCREG[20:17] are always read as 0.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

SCNT[3:0] bits (Stuff bit count)

The SCNT[3:0] bits contain the stuff count value of the CAN-FD frame. These bits indicate the number of inserted stuff bits (modulo 8, Graycoded) for a CAN-FD frame when the CFDCnCTR.CTME bit is enabled in CFDCnFDCRC.SCNT[3:1]. SCNT[0] is the parity bit.

When the CFDCnCTR.CTME bit is 0, the SCNT[3:0] bits are always read as 0.

The SCNT value is updated in the first bit of CRC field of the CAN-FD frame (reception and transmission).

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

这些位通过向CFDCnFDCTR.SOCCLR写入1来清除。

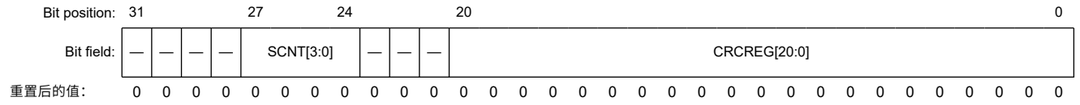
当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

32.2.11 CFDCnFDCRC:通道nCAN-FDCRC寄存器(n=0 1)

该寄存器在经典CAN功能中不可用。

Base address: CANFD = 0x400B_0000

Offset address: 0x1410 + 0x20 × n



Bit	Symbol	Function	R/W
20:0	CRCREG[20:0]	CRC寄存器值 这些位显示为CAN-FD帧计算的CRC值。	R
23:21	—	这些位被读取为0。写入值应为0。	R/W
27:24	SCNT[3:0]	东西位数 这些位显示CAN-FD帧的填充位计数(mod8)。	R
31:28	—	这些位被读取为0。写入值应为0。	R/W

通道nCAN-FDCRC寄存器(n=0 1)保存为CAN-FD帧计算的CRC值。

CRCREG[20:0]位（CRC寄存器值）

CRCREG[20:0]位包含使能CFDCnCTR.CTME位时由CAN-FD通道逻辑计算的CRC值。

CFDCnFDCRC.CRCREG值在CAN-FD帧（接收和发送）的CRC字段的第一位更新。

当CFDCnCTR.CTME位为0时，CRCREG[20:0]位总是读为0。

当使用CRC字段的第17位时，CRCREG[20:17]总是读为0。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

SCNT[3:0]位（填充位计数）

SCNT[3:0]位包含CAN-FD帧的填充计数值。当在CFDCnFDCRC.SCNT[3:1]中启用CFDCnCTR.CTME位时，这些位指示CAN-FD帧的插入填充位（模8，格雷编码）的数量。SCNT[0]是奇偶校验位。

当CFDCnCTR.CTME位为0时，SCNT[3:0]位总是读为0。

SCNT值在CAN-FD帧（接收和发送）的CRC字段的第一位更新。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

32.2.12 CFDGCFG : Global Configuration Register

Base address: CANFD = 0x400B_0000

Offset address: 0x0084

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ITRCP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSBTCS[2:0]			TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TPRI	Transmission Priority 0: ID priority 1: Message buffer number priority	R/W
1	DCE	DLC Check Enable 0: DLC check disabled 1: DLC check enabled	R/W
2	DRE	DLC Replacement Enable 0: DLC replacement disabled 1: DLC replacement enabled	R/W
3	MME	Mirror Mode Enable 0: Mirror mode disabled 1: Mirror mode enabled	R/W
4	DCS	Data Link Controller Clock Select 0: Internal clean clock 1: External clock source connected to CANMCLK pin	R/W
5	CMPOC*1	CAN-FD Message Payload Overflow Configuration 0: Message is rejected 1: Message payload is cut to fit to configured message size	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
11:8	TSP[3:0]	Timestamp Prescaler 0x0: Timestamp prescaler = 1 0x1: Timestamp prescaler = 2 0x2: Timestamp prescaler = 4 0x3: Timestamp prescaler = 8 ⋮ 0xD: Timestamp prescaler = 8192 0xE: Timestamp prescaler = 16384 0xF: Timestamp prescaler = 32768	R/W
12	TSSS	Timestamp Source Select 0: Source clock for timestamp counter is peripheral clock 1: Source clock for timestamp counter is bit time clock	R/W
15:13	TSBTCS[2:0]	Timestamp Bit Time Channel Select 0 0 0: Select clock from channel 0 0 0 1: Select clock from channel 1 Others: Setting prohibited	R/W
31:16	ITRCP[15:0]	Interval Timer Reference Clock Prescaler FIFO interval timer prescaler value	R/W

Note 1. This bit are not available in the classical CAN function.

The Global Configuration Register is used to select the transmission priority to be used for all the TX message buffers and the clock source for the CAN protocol engine of all CAN channels. The CFDGCFG register is also used to select the source for the timestamp clock and to configure the frequency for the timestamp clock and interval timer reference clock.

32.2.12 CFDGCFG:全局配置寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x0084

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	ITRCP[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSBTCS[2:0]			TSSS	TSP[3:0]				—	—	CMPOC	DCS	MME	DRE	DCE	TPRI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TPRI	传输优先级 0：ID优先1：消息缓冲区编号优先	R/W
1	DCE	DLC检查启用 0：禁用DLC检查1：启用DLC检查	R/W
2	DRE	DLC替换启用 0：禁用DLC替换1：启用DLC替换	R/W
3	MME	镜像模式启用 0：镜像模式关闭1：镜像模式开启	R/W
4	DCS	数据链路控制器时钟选择 0：内部清洁时钟1：连接到CANMCLK引脚的外部时钟源	R/W
5	CMPOC*1	CAN-FD消息负载溢出配置 0：消息被拒绝1：消息负载被剪切以适合配置的消息大小	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
11:8	TSP[3:0]	Timestamp Prescaler 0x0: Timestamp prescaler = 1 0x1: Timestamp prescaler = 2 0x2: Timestamp prescaler = 4 0x3: Timestamp prescaler = 8 ⋮ 0xD: Timestamp prescaler = 8192 0xE: Timestamp prescaler = 16384 0xF: Timestamp prescaler = 32768	R/W
12	TSSS	时间戳源选择 0：时间戳计数器的源时钟为外设时钟1：时间戳计数器的源时钟为位时钟	R/W
15:13	TSBTCS[2:0]	时间戳位时间通道选择 000：从通道0中选择时钟001：从通道1中选择时钟 其他：禁止设置	R/W
31:16	ITRCP[15:0]	间隔定时器参考时钟预分频器 FIFO间隔定时器预分频器值	R/W

注1.该位在经典CAN功能中不可用。

全局配置寄存器用于选择用于所有TX报文缓冲区的传输优先级和所有CAN通道的CAN协议引擎的时钟源。CFDGCFG寄存器还用于选择时间戳时钟源以及配置时间戳时钟和间隔定时器参考时钟的频率。

TPRI bit (Transmission Priority)

The TPRI bit selects the transmission priority for all CAN channels.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

Message buffer number priority should not be used together with TX queue transmission.

DCE bit (DLC Check Enable)

The DCE bit enables data length code (DLC) check for all CAN channels.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

DRE bit (DLC Replacement Enable)

When the DRE bit is 1 and the DCE is 1, the CAN-FD stores the configured value (CFDGAFLP0n.GAFLDLC) of the DLC in the destination RX message buffer or FIFO buffer if the DLC check passes. Otherwise, the DLC value in the destination RX message buffer or FIFO buffer is unchanged.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

MME bit (Mirror Mode Enable)

The MME bit enables the Mirror mode for all CAN channels.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

DCS bit (Data Link Controller Clock Select)

The DCS bit selects the clock source for CAN communication. Internal clean clock has a smaller clock jitter than the peripheral clock B (PCLKB).

Do not write to this bit in GL_SLEEP or GL_OPERATION mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

CMPOC bit (CAN-FD Message Payload Overflow Configuration)

The CMPOC bit controls the message payload acceptance mechanism when the received payload is higher than the message buffer payload size CFDRMNB.RMPLS, CFDRFCCn.RFPLS, and CFDCFCCn.CFPLS. The received message payload is always compared with the available message payload size in the message buffer.

Do not write to this bit in GL_SLEEP or GL_OPERATION mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

When this bit is set and payload overflow occurs, the DLC value is stored in the RX message buffer or FIFO buffer unchanged.

Note: This bit is not available in the classical CAN function.

TSP[3:0] bits (Timestamp Prescaler)

The value configured in the TSP[3:0] bits defines the period of the clock source used for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

TSSS bit (Timestamp Source Select)

The TSSS bit allows the selection of the clock source for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode. Additionally, do not set this bit to 1 when CAN-FD communication is used.*1

Note: The bit time clock varies depending on the nominal and data rate bit configuration.

Note 1. This feature is not available in the classical CAN function.

TSBTCS[2:0] bits (Timestamp Bit Time Channel Select)

The TSBTCS[2:0] bits allow the selection of the bit time clock of a particular channel for the timestamp counter.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

TPRI bit (Transmission Priority)

TPRI位选择所有CAN通道的传输优先级。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

消息缓冲区编号优先级不应与TX队列传输一起使用。

DCE位（DLC检查启用）

DCE位启用所有CAN通道的数据长度代码(DLC)检查。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

DRE位（DLC替换启用）

当DRE位为1且DCE为1时，如果DLC检查通过，CAN-FD将DLC的配置值(CFDGAFLP0n.GAFLDLC)存储在目标RX消息缓冲区或FIFO缓冲区中。否则，目标RX消息缓冲区或FIFO缓冲区中的DLC值不变。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

MME位（镜像模式启用）

MME位使能所有CAN通道的镜像模式。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

DCS位（数据链路控制器时钟选择）

DCS位选择CAN通信的时钟源。内部干净时钟的时钟抖动小于外设时钟B(PCLKB)。

不要在GL_SLEEP或GL_OPERATION模式下写入该位。仅当CAN-FD模块处于工作状态时写入该位
GL_RESET mode.

CMPOC位（CAN-FD消息有效负载溢出配置）

当接收到的有效载荷高于消息缓冲区有效载荷大小CFDRMNB.RMPLS、CFDRFCCn.RFPLS和CFDCFCCn.CFPLS时，CMPOC位控制消息有效载荷接受机制。接收到的消息负载总是与消息缓冲区中可用的消息负载大小进行比较。

不要在GL_SLEEP或GL_OPERATION模式下写入该位。仅当CAN-FD模块处于工作状态时写入该位
GL_RESET mode.

当该位被置位并发生有效载荷溢出时，DLC值不变地存储在RX报文缓冲区或FIFO缓冲区中。

Note: 该位在经典CAN功能中不可用。

TSP[3:0] bits (Timestamp Prescaler)

TSP[3:0]位中配置的值定义了用于时间戳计数器的时钟源的周期。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

TSSS位（时间戳源选择）

TSSS位允许选择时间戳计数器的时钟源。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。
此外，使用CAN-FD通信时，请勿将此位设置为1。*1

Note: 位时钟取决于标称和数据速率位配置。

注1.此功能在经典CAN功能中不可用。

TSBTCS[2:0]位（时间戳位时间通道选择）

TSBTCS[2:0]位允许为时间戳计数器选择特定通道的位时钟。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

ITRCP[15:0] bits (Interval Timer Reference Clock Prescaler)

The ITRCP[15:0] bits allow the definition of a reference clock for the FIFO interval timer source clock.

When these bits are 0x0000, the timer is disabled.

Do not write to this bit in GL_SLEEP mode. Only write to this bit when CAN-FD module is in GL_RESET mode.

32.2.13 CFDGCTR : Global Control Register

Base address: CANFD = 0x400B_0000

Offset address: 0x0088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MOWEIE	QMEIE	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	GMDC[1:0]	Global Mode Control 0 0: Global operation mode request 0 1: Global reset mode request 1 0: Global halt mode request 1 1: Keep current value	R/W
2	GSLPR	Global Sleep Request 0: Global sleep request disabled 1: Global sleep request enabled	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	DEIE	DLC Check Interrupt Enable 0: DLC check interrupt disabled 1: DLC check interrupt enabled	R/W
9	MEIE	Message Lost Error Interrupt Enable 0: Message lost error interrupt disabled 1: Message lost error interrupt enabled	R/W
10	THLEIE	TX History List Entry Lost Interrupt Enable 0: TX history list entry lost interrupt disabled 1: TX history list entry lost interrupt enabled	R/W
11	CMPOFIE*1	CAN-FD Message Payload Overflow Flag Interrupt Enable 0: CAN-FD message payload overflow flag interrupt disabled 1: CAN-FD message payload overflow flag interrupt enabled	R/W
13:12	—	These bits are read as 0. The write value should be 0.	R/W
14	QMEIE	TXQ Message Lost Error Interrupt Enable 0: TXQ message lost error interrupt disabled 1: TXQ message lost error interrupt enabled	R/W
15	MOWEIE	GW FIFO Message Overwrite Error Interrupt Enable 0: GW FIFO message overwrite error interrupt disabled 1: GW FIFO message overwrite error interrupt enabled	R/W
16	TSRST	Timestamp Reset 0: Timestamp not reset 1: Timestamp reset	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in the classical CAN function.

ITRCP[15:0]位（间隔定时器参考时钟预分频器）

ITRCP[15:0]位允许为FIFO间隔定时器源时钟定义参考时钟。

当这些位为0x0000时，定时器被禁用。

不要在GL_SLEEP模式下写入该位。仅当CAN-FD模块处于GL_RESET模式时写入该位。

32.2.13 CFDGCTR:全局控制寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x0088

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	MOWEIE	QMEIE	—	—	CMPOFIE	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Function	R/W
1:0	GMDC[1:0]	全局模式控制 00：全局操作模式请求01：全局复位模式请求10：全局停止模式请求11：保持当前值	R/W
2	GSLPR	全局睡眠请求 0：禁用全局睡眠请求1：启用全局睡眠请求	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	DEIE	DLC检查中断启用 0：禁用DLC检查中断1：启用DLC检查中断	R/W
9	MEIE	消息丢失错误中断使能 0：禁用消息丢失错误中断1：启用消息丢失错误中断	R/W
10	THLEIE	TX历史列表条目丢失中断启用 0：禁用TX历史列表条目丢失中断1：启用TX历史列表条目丢失中断	R/W
11	CMPOFIE*1	CAN-FD消息负载溢出标志中断使能 0：禁止CAN-FD消息负载溢出标志中断1：使能CAN-FD消息负载溢出标志中断	R/W
13:12	—	这些位被读取为0。写入值应为0。	R/W
14	QMEIE	TXQ消息丢失错误中断使能 0：禁止TXQ消息丢失错误中断1：使能TXQ消息丢失错误中断	R/W
15	MOWEIE	GWFIFO消息覆盖错误中断使能 0：禁用GWFIFO消息覆盖错误中断1：启用GWFIFO消息覆盖错误中断	R/W
16	TSRST	时间戳重置 0：时间戳不复位1：时间戳复位	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

注1.该位在经典CAN功能中不可用。

RA生态工作室

The Global Control Register controls the global mode of the CAN-FD module and the timestamp function. The register also enables and disables the global error interrupts.

GMDC bits (Global Mode Control)

The GMDC bits can be used to configure the modes for the CAN-FD module. Additionally, if CFDGCTR.GSLPR bit is 1 when the CAN-FD module is in Reset mode, the CAN-FD module enters Global Sleep mode. Additionally, if CFDGCTR.GSLPR is 1 when the CAN-FD module is in Reset Mode, then the CAN-FD module enters Global Sleep Mode.

Setting the GMDC bits to 11b has no effect. Mode transition is described in detail in section 32.3.2. Global Modes.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

GSLPR bit (Global Sleep Request)

The GSLPR bit globally selects the sleep request for CAN-FD module including all CAN channels. Channel sleep request is set automatically for all channels.

Only write to this bit when the CAN-FD module is in GL_RESET or GL_SLEEP mode.

DEIE bit (DLC Check Interrupt Enable)

When the DEIE bit is 1, an interrupt is generated if a DLC error is detected in the received frames.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

MEIE bit (Message Lost Error Interrupt Enable)

When the MEIE bit is 1, an interrupt is generated if a message lost condition occurs.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

THLEIE bit (TX History List Entry Lost Interrupt Enable)

When the THLEIE bit is 1, an interrupt is generated if a TX history list entry lost condition occurs.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

CMPOFIE bit (CAN-FD Message Payload Overflow Flag Interrupt Enable)

When the CMPOFIE bit is 1, an interrupt is generated when a CAN-FD message payload overflow condition occurs.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

Note: This bit is not available in the classical CAN function

QMEIE bit (TXQ Message Lost Error Interrupt Enable)

When the QMEIE bit is 1, an interrupt is generated when a TXQ message lost condition occurs.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

MOWEIE bit (GW FIFO Message Overwrite Error Interrupt Enable)

When the MOWEIE bit is 1, an interrupt is generated in GW mode and a GW FIFO message over write condition occurs.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

TSRST bit (Timestamp Reset)

When the TSRST bit is 1, the Global Timestamp Register is reset to 0x0000.

Do not write to this bit when the CAN-FD module is in GL_SLEEP or GL_RESET mode.

Read value is always 0.

This bit is cleared automatically by the RS-CAN-FD logic.

全局控制寄存器控制CAN-FD模块的全局模式和时间戳功能。该寄存器还启用和禁用全局错误中断。

GMDC位（全局模式控制）

GMDC位可用于配置CAN-FD模块的模式。此外，如果当CAN-FD模块处于复位模式时CFDGCTR.GSLPR位为1，则CAN-FD模块进入全局休眠模式。此外，如果当CAN-FD模块处于复位模式时CFDGCTR.GSLPR为1，则CAN-FD模块进入全局休眠模式。

将GMDC位设置为11b无效。模式转换在第32.3.2节中有详细描述。全局模式。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

GSLPR位（全局休眠请求）

GSLPR位全局选择CAN-FD模块的睡眠请求，包括所有CAN通道。为所有通道自动设置通道睡眠请求。

仅当CAN-FD模块处于GL_RESET或GL_SLEEP模式时写入该位。

DEIE位（DLC检查中断使能）

当DEIE位为1时，如果在接收的帧中检测到DLC错误，则产生中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

MEIE位（消息丢失错误中断使能）

当MEIE位为1时，如果发生信息丢失情况，将产生中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

THLEIE位（TX历史列表条目丢失中断使能）

当THLEIE位为1时，如果发生TX历史列表条目丢失情况，将产生中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

CMPOFIE位（CAN-FD消息有效负载溢出标志中断使能）

当CMPOFIE位为1时，当CAN-FD报文有效负载溢出条件发生时产生中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

Note: 该位在经典CAN功能中不可用

QMEIE位（TXQ消息丢失错误中断使能）

当QMEIE位为1时，当发生TXQ报文丢失情况时会产生中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

MOWEIE位（GWFIFO消息覆盖错误中断使能）

当MOWEIE位为1时，在GW模式下会产生一个中断，并且会出现一个GWFIFO消息覆盖写入条件。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

TSRST bit (Timestamp Reset)

当TSRST位为1时，全局时间戳寄存器复位为0x0000。

当CAN-FD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。

读取值始终为0。

该位由RS-CAN-FD逻辑自动清零。

32.2.14 CFDGSTS : Global Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x008C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	GRAM INIT	GSLP STS	GHLT STS	GRST STS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	GRSTSTS	Global Reset Status 0: Not in Reset mode 1: In Reset mode	R
1	GHLTSTS	Global Halt Status 0: Not in Halt mode 1: In Halt mode	R
2	GSLPSTS	Global Sleep Status 0: Not in Sleep mode 1: In Sleep mode	R
3	GRAMINIT	Global RAM Initialization 0: RAM initialization is complete 1: RAM initialization is ongoing	R
31:4	—	These bits are read as 0. The write value should be 0.	R/W

The Global Status Register indicates the global status of the CAN-FD module.

GRSTSTS bit (Global Reset Status)

The GRSTSTS bit indicates the status of Global CAN-FD module Reset mode.

This bit is set automatically when the CAN-FD module enters GL_RESET mode. When the mode changes from GL_RESET mode to GL_SLEEP mode, this bit remains set.

This bit is cleared automatically when the CAN-FD module exits the GL_RESET mode.

GHLTSTS bit (Global Halt Status)

The GHLTSTS bit indicates the status of Global CAN-FD module Halt mode.

This bit is set automatically when the CAN-FD module enters GL_HALT mode.

This bit is cleared automatically when the CAN-FD module exits the GL_HALT mode.

GSLPSTS bit (Global Sleep Status)

The GSLPSTS bit indicates the status of Global CAN-FD module Sleep mode.

This bit is set automatically when the CAN-FD module enters GL_SLEEP mode.

This bit is cleared automatically when the CAN-FD module exits the GL_SLEEP mode.

GRAMINIT bit (Global RAM Initialization)

The GRAMINIT bit indicates the status of Global CAN-FD module RAM initialization.

This bit is set automatically when the CAN-FD module enters GL_SLEEP mode after a hardware reset.

This bit is cleared automatically when the CAN-FD module completed RAM initialization.

This bit is cleared when the test_mode input port is set to 1.

32.2.14 CFDGSTS:全局状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x008C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	克初始化	GSLP STS	GHLT STS	GRST STS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	GRSTSTS	全局重置状态 0：不处于复位模式1 ：处于复位模式	R
1	GHLTSTS	全局停止状态 0：不处于暂停模式 1：处于暂停模式	R
2	GSLPSTS	全局睡眠状态 0：不处于休眠模式1 ：处于休眠模式	R
3	GRAMINIT	全局RAM初始化 0：RAM初始化完成1：RAM初始化正在进行	R
31:4	—	这些位被读取为0。写入值应为0。	R/W

全局状态寄存器指示CAN-FD模块的全局状态。

GRSTSTS位（全局复位状态）

GRSTSTS位指示全局CAN-FD模块复位模式的状态。

当CAN-FD模块进入GL_RESET模式时，该位自动设置。当模式从GL_RESET模式到GL_SLEEP模式，该位保持设置。

当CAN-FD模块退出GL_RESET模式时，该位自动清零。

GHLTSTS位（全局停止状态）

GHLTSTS位指示全局CAN-FD模块暂停模式的状态。

当CAN-FD模块进入GL_HALT模式时，该位自动置位。

当CAN-FD模块退出GL_HALT模式时，该位自动清零。

GSLPSTS位（全局休眠状态）

GSLPSTS位指示全局CAN-FD模块休眠模式的状态。

当CAN-FD模块进入GL_SLEEP模式时，该位自动置位。

当CAN-FD模块退出GL_SLEEP模式时，该位自动清零。

GRAMMINIT位（全局RAM初始化）

GRAMMINIT位指示全局CAN-FD模块RAM初始化的状态。

当CAN-FD模块在硬件复位后进入GL_SLEEP模式时，该位会自动设置。

当CAN-FD模块完成RAM初始化时，该位自动清零。

当test_mode输入端口设置为1时，该位清零。

32.2.15 CFDGERFL : Global Error Flag Register

Base address: CANFD = 0x400B_0000

Offset address: 0x0090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEF1	EEF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	QMES	—	QOWES	CMPOF	THLES	MES	DEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEF	DLC Error Flag 0: DLC error not detected 1: DLC error detected	R/W
1	MES	Message Lost Error Status 0: Message lost error not detected 1: Message lost error detected	R
2	THLES	TX History List Entry Lost Error Status 0: TX history list entry lost error not detected 1: TX history list entry lost error detected	R
3	CMPOF*1	CAN-FD Message Payload Overflow Flag 0: CAN-FD message payload overflow not detected 1: CAN-FD message payload overflow detected	R/W
4	QOWES	TXQ Message Overwrite Error Status 0: TXQ message overwrite error not detected 1: TXQ message overwrite error detected	R
5	—	This bit is read as 0. The write value should be 0.	R
6	QMES	TXQ Message Lost Error Status 0: TXQ message lost error not detected 1: TXQ message lost error detected	R
15:7	—	These bits are read as 0. The write value should be 0.	R/W
16	EEF0	ECC Error Flag for Channel 0 0: ECC error not detected during TX-SCAN 1: ECC error detected during TX-SCAN	R/W
17	EEF1	ECC Error Flag for Channel 1 0: ECC error not detected during TX-SCAN 1: ECC error detected during TX-SCAN	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is not available in the classical CAN function.

The Global Error Flag register indicates the detection of global errors.

DEF bit (DLC Error Flag)

The DEF bit indicates the error status of the DLC.

Do not write to this bit when the CAN-FD module is in GL_SLEEP or GL_RESET mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when a DLC error is detected in a received frame.

If the set from the CAN channel occurs simultaneously with the clear by the write access, then the bit is set

The bit is cleared by writing 0 to it.

32.2.15 CFDGERFL:全局错误标志寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x0090

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEF1	EEF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	QMES	—	QOWES	CMPOF	THLES	MES	DEF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DEF	DLC错误标志 0：未检测到DLC错误1： 检测到DLC错误	R/W
1	MES	消息丢失错误状态 0：未检测到消息丢失错误1：检测 到消息丢失错误	R
2	THLES	TX历史列表条目丢失错误状态 0：未检测到TX历史列表条目丢失错误1：检 测到TX历史列表条目丢失错误	R
3	CMPOF*1	CAN-FD消息有效负载溢出标志 0：未检测到CAN-FD消息负载溢出1：检测到CAN-F D消息负载溢出	R/W
4	QOWES	TXQ消息覆盖错误状态 0：未检测到TXQ消息覆盖错误1：检测到TXQ 消息覆盖错误	R
5	—	该位读取为0。写入值应为0。	R
6	QMES	TXQ消息丢失错误状态 0：未检测到TXQ消息丢失错误1：检测 到TXQ消息丢失错误	R
15:7	—	这些位被读取为0。写入值应为0。	R/W
16	EEF0	通道0的ECC错误标志 0：在TX-SCAN期间未检测到ECC错误1：在 TX-SCAN期间检测到ECC错误	R/W
17	EEF1	通道1的ECC错误标志 0：在TX-SCAN期间未检测到ECC错误1：在 TX-SCAN期间检测到ECC错误	R/W
31:18	—	这些位被读取为0。写入值应为0。	R/W

注1.该位在经典CAN功能中不可用。

全局错误标志寄存器指示全局错误的检测。

DEF位（DLC错误标志）

DEF位指示DLC的错误状态。

当CAN-FD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当在接收帧中检测到DLC错误时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置

该位通过向其写入0来清除。

This bit is cleared automatically in GL_RESET mode.

MES bit (Message Lost Error Status)

The MES bit indicates status of the message lost error.

This bit is set automatically when a FIFO message lost error is detected.

This bit is cleared automatically when:

- All FIFO message lost flags are cleared
- The CAN-FD module is in GL_RESET mode.

THLES bit (TX History List Entry Lost Error Status)

The THLES bit indicates status of the TX history list entry lost error.

This bit is set automatically when a TX history list entry lost error is detected.

This bit is cleared automatically when:

- All TX history list entry lost flags are cleared
- The CAN-FD module is in GL_RESET mode.

CMPOF bit (CAN-FD Message Payload Overflow Flag)

The CMPOF bit is set automatically when a CAN-FD message payload overflow is detected on at least one channel.

Do not write to this bit when the CAN-FD module is in GL_SLEEP or GL_RESET mode.

This bit is cleared by writing 0 to it. Writing 1 to this bit has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is cleared automatically in GL_RESET mode.

Note: This bit is not available in the classical CAN function

QOWES bit (TXQ Message Overwrite Error Status)

The QOWES bit is set automatically when a TXQ message overwrite error is detected.

This bit is cleared automatically when all TXQ message overwrite flags are cleared.

This bit is cleared automatically in GL_RESET mode.

QMES bit (TXQ Message Lost Error Status)

The QMES bit is set automatically when a TXQ message lost error is detected.

This bit is cleared automatically when all TXQ message lost flags are cleared.

This bit is cleared automatically in GL_RESET mode.

EEF0 bit (ECC Error Flag for Channel 0)

The EEF0 bit specifies whether an ECC error has occurred on Channel 0.

Do not write to this bit when the CAN-FD module is in GL_SLEEP or GL_RESET mode. Writing 1 to this bit has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The bit is cleared by writing 0 to it. This bit is cleared automatically in GL_RESET mode.

EEF1 bit (ECC Error Flag for Channel 1)

The EEF1 bit specifies whether an ECC error has occurred on Channel 1.

Do not write to this bit when the CAN-FD module is in GL_SLEEP or GL_RESET mode. Writing 1 to this bit has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The bit is cleared by writing 0 to it. This bit is cleared automatically in GL_RESET mode.

该位在GL_RESET模式下自动清除。

MES位（消息丢失错误状态）

MES位指示消息丢失错误的状态。

当检测到FIFO消息丢失错误时，该位自动置位。

该位在以下情况下自动清零：

●清除所有FIFO消息丢失标志

●CAN-FD模块处于GL_RESET模式。

THLES位（TX历史列表条目丢失错误状态）

THLES位指示TX历史列表条目丢失错误的状态。

当检测到TX历史列表条目丢失错误时，该位自动设置。

该位在以下情况下自动清零：

●清除所有TX历史列表条目丢失标志

●CAN-FD模块处于GL_RESET模式。

CMPOF位（CAN-FD消息有效负载溢出标志）

当在至少一个通道上检测到CAN-FD消息有效负载溢出时，CMPOF位自动置位。

当CAN-FD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。

该位通过写入0清零。向该位写入1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位在GL_RESET模式下自动清除。

Note: 该位在经典CAN功能中不可用

QOWES位（TXQ报文覆盖错误状态）

当检测到TXQ报文覆盖错误时，QOWES位自动置位。

当所有TXQ报文覆盖标志被清除时，该位自动清除。

该位在GL_RESET模式下自动清除。

QMES位（TXQ消息丢失错误状态）

当检测到TXQ消息丢失错误时，QMES位自动置位。

当所有TXQ消息丢失标志被清除时，该位自动清除。

该位在GL_RESET模式下自动清除。

EEF0位（通道0的ECC错误标志）

EEF0位指定通道0上是否发生ECC错误。

当CAN-FD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。向该位写入1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位通过向其写入0来清除。该位在GL_RESET模式下自动清除。

EEF1位（通道1的ECC错误标志）

EEF1位指定通道1上是否发生ECC错误。

当CAN-FD模块处于GL_SLEEP或GL_RESET模式时，请勿写入该位。向该位写入1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位通过向其写入0来清除。该位在GL_RESET模式下自动清除。

32.2.16 CFDGTINTSTS0 : Global TX Interrupt Status Register 0

Base address: CANFD = 0x400B_0000

Offset address: 0x1300

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CFOTIF1	TQOFIF1	THIF1	CFTIF1	TQIF1	TAIF1	TSIF1	—	CFOTIFO	TQOFIFO	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSIF0	TX Successful Interrupt Flag Channel 0 0: Channel n TX Successful Interrupt flag not set 1: Channel n TX Successful Interrupt flag set	R
1	TAI0	TX Abort Interrupt Flag Channel 0 0: Channel n TX Abort Interrupt flag not set 1: Channel n TX Abort Interrupt flag set	R
2	TQIF0	TX Queue Interrupt Flag Channel 0 0: Channel n TX Queue Interrupt flag not set 1: Channel n TX Queue Interrupt flag set	R
3	CFTIF0	COM FIFO TX/GW Mode Interrupt Flag Channel 0 0: Channel n COM FIFO TX/GW Mode Interrupt flag not set 1: Channel n COM FIFO TX/GW Mode Interrupt flag set	R
4	THIF0	TX History List Interrupt Channel 0 0: Channel n TX History List Interrupt flag not set 1: Channel n TX History List Interrupt flag set	R
5	TQOFIFO	TX Queue One Frame Transmission Interrupt Flag Channel 0 0: Channel n TX Queue One Frame Transmission Interrupt flag not set 1: Channel n TX Queue One Frame Transmission Interrupt flag set	R
6	CFOTIFO	COM FIFO One Frame Transmission Interrupt Flag Channel 0 0: Channel n COM FIFO One Frame Transmission Interrupt flag not set 1: Channel n COM FIFO One Frame Transmission Interrupt flag set	R
7	—	This bit is read as 0. The write value should be 0.	R/W
8	TSIF1	TX Successful Interrupt Flag Channel 1 0: Channel n TX Successful Interrupt flag not set 1: Channel n TX Successful Interrupt flag set	R
9	TAIF1	TX Abort Interrupt Flag Channel 1 0: Channel n TX Abort Interrupt flag not set 1: Channel n TX Abort Interrupt flag set	R
10	TQIF1	TX Queue Interrupt Flag Channel 1 0: Channel n TX Queue Interrupt flag not set 1: Channel n TX Queue Interrupt flag set	R
11	CFTIF1	COM FIFO TX/GW Mode Interrupt Flag Channel 1 0: Channel n COM FIFO TX/GW Mode Interrupt flag not set 1: Channel n COM FIFO TX/GW Mode Interrupt flag set	R
12	THIF1	TX History List Interrupt Channel 1 0: Channel n TX History List Interrupt flag not set 1: Channel n TX History List Interrupt flag set	R
13	TQOFIF1	TX Queue One Frame Transmission Interrupt Flag Channel 1 0: Channel n TX Queue One Frame Transmission Interrupt flag not set 1: Channel n TX Queue One Frame Transmission Interrupt flag set	R

32.2.16 CFDGTINTSTS0：全局TX中断状态寄存器0

Base address: CANFD = 0x400B_0000

Offset address: 0x1300

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CFOTIF1	TQOFIF1	THIF1	CFTIF1	TQIF1	TAIF1	TSIF1	—	CFOTIFO	TQOFIFO	THIF0	CFTIF0	TQIF0	TAI0	TSIF0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSIF0	TX成功中断标志通道0 0：未设置通道nTX成功中断标志1：设置了通道nTX成功中断标志	R
1	TAI0	TX中止中断标志通道0 0：未设置通道nTX中止中断标志1：设置了通道nTX中止中断标志	R
2	TQIF0	TX队列中断标志通道0 0：未设置通道nTX队列中断标志1：设置了通道nTX队列中断标志	R
3	CFTIF0	COMFIFOTXGW模式中断标志通道0 0：未设置通道nCOMFIFOTXGW模式中断标志1：设置了通道nCOMFIFOTXGW模式中断标志	R
4	THIF0	TX历史列表中断通道0 0：通道nTX历史列表中断标志未设置1：通道nTX历史列表中断标志设置	R
5	TQOFIFO	TX队列一帧传输中断标志通道0 0：通道nTX队列一帧传输中断标志未设置1：通道nTX队列一帧传输中断标志设置	R
6	CFOTIFO	COMFIFO一帧传输中断标志通道0 0：未设置通道nCOMFIFO一帧传输中断标志1：设置通道nCOMFIFO一帧传输中断标志	R
7	—	该位读取为0。写入值应为0。	R/W
8	TSIF1	TX成功中断标志通道1 0：未设置通道nTX成功中断标志1：设置了通道nTX成功中断标志	R
9	TAIF1	TX中止中断标志通道1 0：未设置通道nTX中止中断标志1：设置了通道nTX中止中断标志	R
10	TQIF1	TX队列中断标志通道1 0：未设置通道nTX队列中断标志1：设置了通道nTX队列中断标志	R
11	CFTIF1	COMFIFOTXGW模式中断标志通道1 0：未设置通道nCOMFIFOTXGW模式中断标志1：设置了通道nCOMFIFOTXGW模式中断标志	R
12	THIF1	TX历史列表中断通道1 0：通道nTX历史列表中断标志未设置1：通道nTX历史列表中断标志设置	R
13	TQOFIF1	TX队列一帧传输中断标志通道1 0：通道nTX队列一帧传输中断标志未设置1：通道nTX队列一帧传输中断标志设置	R

RA生态工作室

Bit	Symbol	Function	R/W
14	CFOTIF1	COM FIFO One Frame Transmission Interrupt Flag Channel 1 0: Channel n COM FIFO One Frame Transmission Interrupt flag not set 1: Channel n COM FIFO One Frame Transmission Interrupt flag set	R
31:15	—	These bits are read as 0. The write value should be 0.	R/W

The Global TX Interrupt Status register indicates the detection of transmit specific interrupts.

TSIF0 bit (TX Successful Interrupt Flag Channel 0)

The TSIF0 bit is set to 1 when the TX Successful Interrupt flag of the related channel is set (when the interrupt is enabled).
This bit is cleared automatically:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TAI0 bit (TX Abort Interrupt Flag Channel 0)

The TAIF0 bit is set to 1 when the TX Abort Interrupt flag of the related channel is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TQIF0 bit (TX Queue Interrupt Flag Channel 0)

The TQIF0 bit is set to 1 when the TX Queue Interrupt flag of the related channel is set (when the interrupt is enabled).
This bit is cleared automatically:

- When the related TX Queue Interrupt flag is cleared (when the interrupt is enable disabled)
- When in GL_RESET or CH_RESET mode.

CFTIF0 bit (COM FIFO TX/GW Mode Interrupt Flag Channel 0)

The CFTIF0 bit is set to 1 when the related COM TX/GW FIFO Mode Interrupt flag (CFDCFSTSn.CFTXIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related COM TX/GW FIFO Mode Interrupt flag (CFDCFSTSn.CFTXIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

THIF0 bit (TX History List Interrupt Channel 0)

The THIF0 bit is set to 1 when the related TX History List Interrupt flag (CFDTHLSTSn.THLIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX History List Interrupt flag (CFDTHLSTSn.THLIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

CFDGTINTSTS0.TQOFIFn bit (TX Queue One Frame Transmission Interrupt Flag Channel n (n = 0, 1))

The CFDGTINTSTS0.TQOFIFn bit is set to 1 when the TX Queue One Frame Transmission Interrupt flag of the related channel is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX Queue One Frame Transmission Interrupt flag is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

Bit	Symbol	Function	R/W
14	CFOTIF1	COMFIFO一帧传输中断标志通道1 0：未设置通道nCOMFIFO一帧传输中断标志1：设置通道nCOMFIFO一帧传输中断标志	R
31:15	—	这些位被读取为0。写入值应为0。	R/W

全局TX中断状态寄存器指示发送特定中断的检测。

TSIF0位（TX成功中断标志通道0）

当相关通道的TX成功中断标志置位时（中断使能时），TSIF0位设置为1。
该位自动清零：

●当相关的TXMBResultStatus位被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

TAI0位（TX中止中断标志通道0）

当相关通道的TXAbortInterrupt标志置位时（中断使能时），TAIF0位被置1。

该位自动清零：

●当相关的TXMBResultStatus位被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

TQIF0位（TX队列中断标志通道0）

当相关通道的TX队列中断标志置位（中断使能时）时，TQIF0位被置1。
该位自动清零：

●相关TXQueueInterrupt标志清零时（中断使能禁止时）

●在GL_RESET或CH_RESET模式下。

CFTIF0位（COMFIFOTXGW模式中断标志通道0）

当相关的COMTXGWFIFO模式中断标志(CFDCFSTSn.CFTXIF)置位时（中断使能时），CFTIF0位设置为1。

该位自动清零：

●当相关的COMTXGWFIFO模式中断标志(CFDCFSTSn.CFTXIF)被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

THIF0位（TX历史列表中断通道0）

当相关的TX历史列表中断标志(CFDTHLSTSn.THLIF)置位时（中断使能时），THIF0位设置为1。

该位自动清零：

●当相关的TX历史列表中断标志(CFDTHLSTSn.THLIF)被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

CFDGTINTSTS0.TQOFIFn位（TX队列一帧传输中断标志通道n(n=0 1)）

当相关通道的TX队列一帧传输中断标志置位时（中断使能时），CFDGTINTSTS0.TQOFIFn位设置为1。

该位自动清零：

●当相关的TXQueue一帧传输中断标志被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

CFDGTINTSTS0.CFOTIFn bit (COM FIFO One Frame Transmission Interrupt Flag Channel n (n = 0, 1))

The CFDGTINTSTS0.CFOTIFn bit is set to 1 when the related COM FIFO One Frame Transmission Interrupt flag (CFDCFSTSn.CFOFTXIF) is set (when the Interrupt is enabled).

This bit is cleared automatically:

- When the related COM FIFO One Frame Transmission Interrupt flag (CFDCFSTSn.CFOFTXIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TSIF1 bit (TX Successful Interrupt Flag Channel 1)

The TSIF1 bit is set to 1 when the TX Successful Interrupt flag of the related channel is set (when the interrupt is enabled).
This bit is cleared automatically:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TAIF1 bit (TX Abort Interrupt Flag Channel 1)

The TAIF1 bit is set to 1 when the TX Abort Interrupt flag of the related channel is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX MB Result Status bits are cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

TQIF1 bit (TX Queue Interrupt Flag Channel 1)

The TQIF1 bit is set to 1 when the TX Queue Interrupt flag of the related channel is set (when the interrupt is enabled).
This bit is cleared automatically:

- When the related TX Queue Interrupt flag is cleared (when the interrupt is enable disabled)
- When in GL_RESET or CH_RESET mode.

CFTIF1 bit (COM FIFO TX/GW Mode Interrupt Flag Channel 1)

The CFTIF1 bit is set to 1 when the related COM TX/GW FIFO Mode Interrupt flag (CFDCFSTSn.CFTXIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related COM TX/GW FIFO Mode Interrupt flag (CFDCFSTSn.CFTXIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

THIF1 bit (TX History List Interrupt Channel 1)

The THIF1 bit is set to 1 when the related TX History List Interrupt flag (CFDTHLSTSn.THLIF) is set (when the interrupt is enabled).

This bit is cleared automatically:

- When the related TX History List Interrupt flag (CFDTHLSTSn.THLIF) is cleared (when the interrupt enable is disabled)
- When in GL_RESET or CH_RESET mode.

CFDGTINTSTS0.CFOTIFn位（COMFIFO一帧传输中断标志通道n(n=0 1)）

当相关的COMFIFO一帧传输中断标志(CFDCFSTSn.CFOFTXIF)设置时（中断使能时），CFDGTINTSTS0.CFOTIFn位设置为1。

该位自动清零：

●当相关的COMFIFO一帧传输中断标志（CFDCFSTSn.CFOFTXIF）被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

TSIF1位（TX成功中断标志通道1）

当相关通道的TX成功中断标志置位时（中断使能时），TSIF1位设置为1。
该位自动清零：

●当相关的TXMBResultStatus位被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

TAIF1位（TX中止中断标志通道1）

当相关通道的TXAbortInterrupt标志置位时（允许中断时），TAIF1位设置为1。

该位自动清零：

●当相关的TXMBResultStatus位被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

TQIF1位（TX队列中断标志通道1）

当相关通道的TX队列中断标志置位（中断使能时）时，TQIF1位设置为1。
该位自动清零：

●相关TXQueueInterrupt标志清零时（中断使能禁止时）

●在GL_RESET或CH_RESET模式下。

CFTIF1位（COMFIFOTXGW模式中断标志通道1）

当相关的COMTXGWFIFO模式中断标志(CFDCFSTSn.CFTXIF)置位时（中断使能时），CFTIF1位设置为1。

该位自动清零：

●当相关的COMTXGWFIFO模式中断标志(CFDCFSTSn.CFTXIF)被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

THIF1位（TX历史列表中断通道1）

当相关的TX历史列表中断标志(CFDTHLSTSn.THLIF)置位时（当允许中断时），THIF1位设置为1。

该位自动清零：

●当相关的TX历史列表中断标志(CFDTHLSTSn.THLIF)被清除时（当中断使能被禁用时）

●在GL_RESET或CH_RESET模式下。

32.2.17 CFDGTSC : Global Timestamp Counter Register

Base address: CANFD = 0x400B_0000

Offset address: 0x0094

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TS[15:0]	Timestamp value	R
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The Global Timestamp Counter register stores the timestamp based on the selected configuration.

TS[15:0] bits (Timestamp value)

The Timestamp value is stored in the Global Timestamp Counter register based on the configuration of TSSS, TSBTCS and TSP. The accuracy of the timestamp counter cannot be guaranteed when transitioning to halt state.

The Timestamp value is stored in this register based on the configuration of TSSS, TSBTCS and TSP.

Do not write to bits TS[15:0] when the CAN-FD module is in GL_RESET or GL_SLEEP mode.

The TS[15:0] bits are cleared automatically in GL_RESET mode.

32.2.18 CFDGAFLECTR : Global Acceptance Filter List Entry Control Register

Base address: CANFD = 0x400B_0000

Offset address: 0x0098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AFLDAE	—	—	—	—	AFLPN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	AFLPN[3:0]	Acceptance Filter List Page Number Select an Acceptance Filter List page	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
8	AFLDAE	Acceptance Filter List Data Access Enable 0: Acceptance Filter List data access disabled 1: Acceptance Filter List data access enabled	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Entry Control Register is used to select the Global Acceptance Filter List page for reading or writing entries into the Global Acceptance Filter List.

AFLPN[3:0] bits (Acceptance Filter List Page Number)

The AFLPN[3:0] bits select the page number to access the desired RAM area of the Acceptance Filter List. One Acceptance Filter List page consists of 16 Acceptance Filter List entries.

Read/write accesses to the Acceptance Filter List can only be performed through a fixed window.

32.2.17 CFDGTSC:全球时间戳计数器寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x0094

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TS[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TS[15:0]	时间戳值	R
31:16	—	这些位被读取为0。写入值应为0。	R/W

全局时间戳计数器寄存器存储基于所选配置的时间戳。

TS[15:0] bits (Timestamp value)

Timestamp值根据TSSS、TSBTCS和
茶多酚。转换到停止状态时，无法保证时间戳计数器的准确性。

Timestamp值根据TSSS、TSBTCS和TSP的配置存储在该寄存器中。

当CAN-FD模块处于GL_RESET或GL_SLEEP模式时，请勿写入位TS[15:0]。

TS[15:0]位在GL_RESET模式下自动清零。

32.2.18 CFDGAFLECTR:全局接受过滤器列表条目控制寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x0098

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	AFLDAE	—	—	—	—	AFLPN[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	AFLPN[3:0]	接受过滤器列表页码选择接受过滤器 列表页面	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
8	AFLDAE	接受过滤器列表数据访问启用 0：禁用接受过滤器列表数据访问1：启用接受 过滤器列表数据访问	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

全局接受过滤器列表条目控制寄存器用于选择全局接受过滤器列表页面，以将条目读取或写入全局接受过滤器列表。

AFLPN[3:0]位（接受过滤器列表页码）

AFLPN[3:0]位选择页码以访问验收过滤器列表的所需RAM区域。一次验收过滤器列表页面由16个接受过滤器列表条目组成。

只能通过固定窗口执行对接受过滤器列表的读写访问。

Do not write to these bits when the CAN-FD module is in GL_SLEEP mode. Enter only the values between 0x00 and 0x07, inclusive.

AFLDAE bit (Acceptance Filter List Data Access Enable)

The AFLDAE bit prevents write access to the Acceptance Filter List when cleared after configuration of the Acceptance Filter List.

Data can be read from the Acceptance Filter List independent of the status of this bit.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode. Set this bit to enable write access for the Acceptance Filter List.

32.2.19 CFDGAFLCFG0 : Global Acceptance Filter List Configuration Register 0

Base address: CANFD = 0x400B_0000

Offset address: 0x009C

Bit position:	31							24								16								8								0
Bit field:	—	—	—	—	—	—	—	RNC0[8:0]								—	—	—	—	—	—	—	RNC1[8:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RNC1[8:0]	Rule Number for Channel 1 Number of rules dedicated to channel 1	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
24:16	RNC0[8:0]	Rule Number for Channel 0 Number of rules dedicated to channel 0	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Configuration Register 0 is used to define the number of rules for entries in the Acceptance Filter List, applicable for channels 0 to 1.

The total number of available entries in the Acceptance Filter List is 64 × (n + 1), 128 for 2 CAN channels. However, the filters can be allocated flexibly to the different channels depending on requirements as long as both of the following conditions are satisfied:

- The maximum number of acceptance filter per channel is 384
- The total number of rules defined for all channels is not exceeding the number of available entries in the Acceptance Filter List.

RNC0[8:0] bits (Rule Number for Channel n (n = 0, 1))

The RNC0[8:0] bits define the number of rules in the Acceptance Filter List for channel n.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

当CAN-FD模块处于GL_SLEEP模式时，不要写入这些位。仅输入0x00和0x07之间的值（包括0x00和0x07）。

AFLDAE位（接受过滤器列表数据访问使能）

AFLDAE位在配置接受后清除时可防止对接受过滤器列表的写访问
过滤器列表。

可以从接受过滤器列表中读取数据，而与该位的状态无关。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。设置该位以启用写访问
接受过滤器列表。

32.2.19 CFDGAFLCFG0：全局接受过滤器列表配置寄存器0

Base address: CANFD = 0x400B_0000

Offset address: 0x009C

Bit position:	31							24								16								8								0
Bit field:	—	—	—	—	—	—	—	RNC0[8:0]								—	—	—	—	—	—	—	RNC1[8:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	RNC1[8:0]	通道1的规则编号 专用于通道1的规则数	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
24:16	RNC0[8:0]	通道0的规则编号 专用于通道0的规则数	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

全局接受过滤器列表配置寄存器0用于定义条目中的规则数量
接受过滤器列表，适用于通道0到1。

接受过滤器列表中可用条目的总数为64×(n+1)，2个CAN通道为128。但是，只要同时满足以下两个条件，就可以根据需要将滤波器灵活分配给不同的通道：

●每通道最大接收滤波器数为384

●为所有通道定义的规则总数不超过接受过滤器列表中可用条目的数量。

RNC0[8:0]位（通道n(n=0 1)的规则编号）

RNC0[8:0]位定义通道n的接受过滤器列表中的规则数量。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

32.2.20 CFDGAFLIDn : Global Acceptance Filter List ID Registers (n = 1 to 16)

Base address: CANFD = 0x400B_0000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLID[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLID[28:0]	Global Acceptance Filter List Entry ID Field ID part of the Global Acceptance Filter List entry	R/W
29	GAFLLB	Global Acceptance Filter List Entry Loopback Configuration 0: Global Acceptance Filter List entry ID for acceptance filtering with attribute RX 1: Global Acceptance Filter List entry ID for acceptance filtering with attribute TX	R/W
30	GAFLRTR	Global Acceptance Filter List Entry RTR Field 0: Data frame 1: Remote frame	R/W
31	GAFLIDE	Global Acceptance Filter List Entry IDE Field 0: Standard identifier of rule entry ID is valid for acceptance filtering 1: Extended identifier of rule entry ID is valid for acceptance filtering	R/W

The Global Acceptance Filter List ID Registers (n = 1 to 16) are used to configure the ID field for the rules of entries in the Global Acceptance Filter List.

GAFLID[28:0] bits (Global Acceptance Filter List Entry ID Field)

The GAFLID[28:0] bits represent the CAN identifier (ID) field of each entry in the Global Acceptance Filter List.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLLB bit (Global Acceptance Filter List Entry Loopback Configuration)

The GAFLLB bit selects whether entry in the Global Acceptance Filter List gets the attribute RX or TX.

This attribute determines the validity of the entry in Mirror mode, Loopback test mode, and during standard (non-loopback) reception. See section 32.5.5. Loopback Modes for detailed description of the validity of the Global Acceptance Filter List entry depending on transmitter/receiver case, the type of loopback mode, and RX/TX attribute.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLRTR bit (Global Acceptance Filter List Entry RTR Field)

The GAFLRTR bit allows the configuration of the specified frame format (data frame or remote frame) for each entry of the Global Acceptance Filter List. For each rule entry in a CAN channel, the acceptance filter process compares this bit against the RTR bit of the received CAN message.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLIDE bit (Global Acceptance Filter List Entry IDE Field)

The GAFLIDE bit allows the configuration of the ID format (standard ID or extended ID) for each entry in the Global Acceptance Filter List. For each rule entry in a CAN channel, the acceptance filter process compares this bit against the IDE bit of the received CAN message.

32.2.20 CFDGAFLIDn：全局接受过滤器列表ID寄存器（n=1到16）

Base address: CANFD = 0x400B_0000

Offset address: 0x1800 + 0x10 × (n - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:16]												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLID[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLID[28:0]	全局接受过滤器列表条目ID字段 全局接受过滤器列表条目的ID部分	R/W
29	GAFLLB	全局接受过滤器列表条目环回配置 0：全局接受过滤器列表条目ID，用于带有属性RX的接受过滤1：全局接受过滤器列表条目ID，用于带有属性TX的接受过滤	R/W
30	GAFLRTR	全局接受过滤器列表条目RTR字段 0：数据帧1：远程帧	R/W
31	GAFLIDE	全局验收过滤器列表条目IDE字段 0：规则条目ID的标准标识符对接受过滤有效1：规则条目ID的扩展标识符对接受过滤有效	R/W

全局接受过滤器列表ID寄存器（n=1到16）用于配置ID字段以用于全局接受过滤器列表。

GAFLID[28:0]位（全局接受过滤器列表条目ID字段）

GAFLID[28:0]位代表全局接受过滤器列表中每个条目的CAN标识符(ID)字段。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLLB位（全局接受过滤器列表条目环回配置）

GAFLLB位选择全局接受过滤器列表中的条目是否获得属性RX或TX。

此属性确定条目在镜像模式、环回测试模式和标准（非环回）接收期间的有效性。请参阅第32.5.5节。Loopback Modes用于详细描述GlobalAcceptanceFilterList条目的有效性，具体取决于发送器接收器情况、环回模式的类型和RXTX属性。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLRTR位（全局接受过滤器列表条目RTR字段）

GAFLRTR位允许为全局接受过滤器列表的每个条目配置指定的帧格式（数据帧或远程帧）。对于CAN通道中的每个规则条目，接受过滤器进程将该位与接收到的CAN消息的RTR位进行比较。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLIDE位（全局接受过滤器列表条目IDE字段）

GAFLIDE位允许为全局中的每个条目配置ID格式（标准ID或扩展ID）接受过滤器列表。对于CAN通道中的每个规则条目，接受过滤器进程将该位与接收到的CAN消息的IDE位进行比较。

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

32.2.21 CFDGAFLMn : Global Acceptance Filter List Mask Registers (n = 1 to 16)

Base address: CANFD = 0x400B_0000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDEM	GAFLRTRM	GAFLIFL1	GAFLIDM[28:16]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLIDM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLIDM[28:0]	Global Acceptance Filter List ID Mask Field Global Acceptance Filter List Mask field bits for ID field	R/W
29	GAFLIFL1	Global Acceptance Filter List Information Label 1 Global Acceptance Filter List information label bit 1	R/W
30	GAFLRTRM	Global Acceptance Filter List Entry RTR Mask 0: RTR bit is not used for ID matching 1: RTR bit is used for ID matching	R/W
31	GAFLIDEM	Global Acceptance Filter List IDE Mask 0: IDE bit is not used for ID matching 1: IDE bit is used for ID matching	R/W

The Global Acceptance Filter List Mask Registers are used to configure the Mask field of each rule for entries in the Global Acceptance Filter List.

GAFLIDM[28:0] bits (Global Acceptance Filter List ID Mask Field)

GAFLIDM[28:0] bits are the filter mask bits for the related bits in the CAN Identifier field of each Global Acceptance Filter List entry.

0	Corresponding STD-ID/EXT-ID bit is not used for ID matching
1	Corresponding STD-ID/EXT-ID bit is used for ID matching

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLIFL1 bit (Global Acceptance Filter List Information Label 1)

The GAFLIFL1 bit allows the configuration of a 2-bit information label to be attached to a received message accepted by the associated entry in the Global Acceptance Filter List. This bit is a MSB bit of an information label.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

This bit is stored in the Information Label Field [1] (CFDRMFDSTSn.RMIFL [1], CFDRFFDSTSn.RFIFL [1], CFDCFFDCSTSn.CFIFL [1]) of the storage location of an incoming message.

Note: This bit is stored in CFDTHLACC1n.TIFL [1] when CFDTHLCCn.THLDGE = 1 is set up using Gateway function.

GAFLRTRM bit (Global Acceptance Filter List Entry RTR Mask)

The GAFLRTRM bit allows the configuration of the RTR mask bit for each entry in the Global Acceptance Filter List.

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

32.2.21 CFDGAFLMn：全局验收过滤器列表屏蔽寄存器（n=1到16）

Base address: CANFD = 0x400B_0000

Offset address: 0x1804 + 0x10 × (n - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLIDEM	GAFLRTRM	GAFLIFL1	GAFLIDM[28:16]												
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFLIDM[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
28:0	GAFLIDM[28:0]	全局接受过滤器列表ID掩码字段 ID字段的全局接受过滤器列表掩码字段位	R/W
29	GAFLIFL1	全局接受过滤器列表信息标签1 全局接受过滤器列表信息标签位1	R/W
30	GAFLRTRM	全局接受过滤器列表条目RTR掩码 0：RTR位不用于ID匹配1：RTR位用于ID匹配	R/W
31	GAFLIDEM	全局接受过滤器列表IDE掩码 0：IDE位不用于ID匹配1：IDE位用于ID匹配	R/W

全局接受过滤器列表掩码寄存器用于为全局中的条目配置每个规则的掩码字段
接受过滤器列表。

GAFLIDM[28:0]位（全局接受过滤器列表ID掩码字段）

GAFLIDM[28:0]位是每个全局接受过滤器的CAN标识符字段中相关位的过滤器掩码位
列表条目。

0	对应的STD-IDEXT-ID位不用于ID匹配
1	对应的STD-IDEXT-ID位用于ID匹配

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLIFL1位（全局接受过滤器列表信息标签1）

GAFLIFL1位允许将2位信息标签的配置附加到由全局接受过滤器列表中的相关条目接受的接收消息。该位是信息标签的MSB位。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

该位存储在信息标签字段[1]（CFDRMFDSTSn.RMIFL[1]、CFDRFFDSTSn.RFIFL[1]、CFDCFFDCSTSn.CFIFL[1])传入消息的存储位置。

Note: 当使用网关功能设置CFDTHLCCn.THLDGE=1时，该位存储在CFDTHLACC1n.TIFL[1]中。

GAFLRTRM位（全局接受过滤器列表条目RTR掩码）

GAFLRTRM位允许为全局接受过滤器列表中的每个条目配置RTR掩码位。

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLIDEM bit (Global Acceptance Filter List IDE Mask)

The GAFLIDEM bit allows the configuration of the IDE mask bit for each entry in the Global Acceptance Filter List.

When the IDE mask bit is 0, the ID comparison depends on the received IDE bit.

If the received IDE bit is 0, the STD-ID comparison takes place.

If the received IDE bit is 1, the EXT-ID comparison takes place.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to this bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

32.2.22 CFDGAFLP0n : Global Acceptance Filter List Pointer 0 Registers (n = 1 to 16)

Base address: CANFD = 0x400B_0000

Offset address: 0x1808 + 0x10 × (n - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFL RMV	—	—	GAFLRMDP[4:0]					GAFLI FL0	GAFL SRD2	GAFL SRD1	GAFL SRD0	GAFLDLC[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	GAFLDLC[3:0]	Global Acceptance Filter List DLC Field Minimum number of data bytes in a data frame required for acceptance	R/W
4	GAFLSRD0	Global Acceptance Filter List Select Routing Destination 0 0: Routing target is CFIFO0 1: Routing target is TX Queue 0 instead of CFIFO0	R/W
5	GAFLSRD1	Global Acceptance Filter List Select Routing Destination 1 0: Routing target is CFIFO1 1: Routing target is TX Queue 1 instead of CFIFO1	R/W
6	GAFLSRD2	Global Acceptance Filter List Select Routing Destination 2 0: Routing target is CFIFO2 1: Routing target is TX Queue 2 instead of CFIFO2	R/W
7	GAFLIFL0	Global Acceptance Filter List Information Label 0	R/W
12:8	GAFLRMDP[4:0]	Global Acceptance Filter List RX Message Buffer Direction Pointer RX message buffer number for storage of received messages	R/W
14:13	—	These bits are read as 0. The write value should be 0.	R/W
15	GAFLRMV	Global Acceptance Filter List RX Message Buffer Valid 0: Single message buffer direction pointer is invalid 1: Single message buffer direction pointer is valid	R/W
31:16	GAFLPTR[15:0]	Global Acceptance Filter List Pointer	R/W

The Global Acceptance Filter List Pointer 0 Registers (n = 1 to 16) are used to configure the data length code (DLC), software pointer, single message buffer select, and message buffer direction pointer for each rule entry in the Global Acceptance Filter List.

GAFLDLC[3:0] bits (Global Acceptance Filter List DLC Field)

The GAFLDLC[3:0] bits allow the configuration of a minimum data length code (DLC) value for a message to be accepted by the associated entry in the Global Acceptance Filter List (automatic DLC filter function).

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLIDEM位（全局接受过滤器列表IDE掩码）

GAFLIDEM位允许为全局接受过滤器列表中的每个条目配置IDE掩码位。

当IDE掩码位为0时，ID比较取决于接收到的IDE位。

如果接收到的IDE位为0，则进行STD-ID比较。

如果接收到的IDE位为1，则进行EXT-ID比较。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

32.2.22 CFDGAFLP0n：全局验收过滤器列表指针0寄存器（n=1到16）

Base address: CANFD = 0x400B_0000

Offset address: 0x1808 + 0x10 × (n - 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	GAFLPTR[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GAFL RMV	—	—	GAFLRMDP[4:0]					GAFLI FL0	GAFL SRD2	GAFL SRD1	GAFL SRD0	GAFLDLC[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	GAFLDLC[3:0]	全局接受过滤器列表DLC字段 接受所需的数据帧中的最小数据字节数	R/W
4	GAFLSRD0	全局接受过滤器列表选择路由目的地0 0：路由目标是CFIFO01：路由目标是TXQueue0而不是CFIFO0	R/W
5	GAFLSRD1	全局接受过滤器列表选择路由目的地1 0：路由目标是CFIFO11：路由目标是TXQueue1而不是CFIFO1	R/W
6	GAFLSRD2	全局接受过滤器列表选择路由目的地2 0：路由目标是CFIFO21：路由目标是TXQueue2而不是CFIFO2	R/W
7	GAFLIFL0	全局接受过滤器列表信息标签0	R/W
12:8	GAFLRMDP[4:0]	全局接受过滤器列表RX消息缓冲区方向指针 RX消息缓冲区号，用于存储接收到的消息	R/W
14:13	—	这些位被读取为0。写入值应为0。	R/W
15	GAFLRMV	全局接受过滤器列表RX消息缓冲区有效 0：单报文缓冲区方向指针无效1：单报文缓冲区方向指针有效	R/W
31:16	GAFLPTR[15:0]	全局接受过滤器列表指针	R/W

全局接受过滤器列表指针0寄存器（n=1到16）用于为全局接受过滤器列表中的每个规则条目配置数据长度代码(DLC)、软件指针、单个消息缓冲区选择和消息缓冲区方向指针.

GAFLDLC[3:0]位（全局接受过滤器列表DLC字段）

GAFLDLC[3:0]位允许配置消息的最小数据长度代码(DLC)值，以便被全局接受过滤器列表中的相关条目接受（自动DLC过滤器功能）。

DLC filter process is only passed if the DLC value of the message accepted by an entry in the Global Acceptance Filter List is equal to or higher than the DLC value configured for this associated Global Acceptance Filter List entry. Automatic DLC filter function is disabled for the corresponding rule entry when this field is set to 0.

Table 32.4 shows DLC value that can be configured.

Table 32.4 Configuration of DLC value

Format	DLC[3]	DLC[2]	DLC[1]	DLC[0]	Description
CAN and CAN-FD	0	0	0	0	DLC of received message = 0 or more (DLC filter check is disabled)
CAN and CAN-FD	0	0	0	1	DLC of received message = 1 or more
CAN and CAN-FD	0	0	1	0	DLC of received message = 2 or more
CAN and CAN-FD	0	0	1	1	DLC of received message = 3 or more
CAN and CAN-FD	0	1	0	0	DLC of received message = 4 or more
CAN and CAN-FD	0	1	0	1	DLC of received message = 5 or more
CAN and CAN-FD	0	1	1	0	DLC of received message = 6 or more
CAN and CAN-FD	0	1	1	1	DLC of received message = 7 or more
CAN	1	x	x	x	DLC of received message = 8 or more
CAN-FD	1	0	0	0	DLC of received message = 8 or more*1
CAN-FD	1	0	0	1	DLC of received message = 12 or more*1
CAN-FD	1	0	1	0	DLC of received message = 16 or more*1
CAN-FD	1	0	1	1	DLC of received message = 20 or more*1
CAN-FD	1	1	0	0	DLC of received message = 24 or more*1
CAN-FD	1	1	0	1	DLC of received message = 32 or more*1
CAN-FD	1	1	1	0	DLC of received message = 48 or more*1
CAN-FD	1	1	1	1	DLC of received message = 64*1

Note 1. This setting is not available in the classical CAN function.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLSRD0 bit (Global Acceptance Filter List Select Routing Destination 0)

The GAFLSRD0 bit changes a copy destination to CFIFO0 or TXQ0 by routing.

If this bit is set as 1, the preset value of CFDGAFLP1n.GAFLFDP selects TX Queue.

If this bit is set to 0, the preset value of CFDGAFLP1n.GAFLFDP selects CFIFO0.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to the bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLSRD1 bit (Global Acceptance Filter List Select Routing Destination 1)

The GAFLSRD1 bit changes a copy destination to CFIFO1 or TXQ1 by routing.

If this bit is set to 1, the preset value of CFDGAFLP1n.GAFLFDP selects TXQ1.

If this bit is set to 0, the preset value of CFDGAFLP1n.GAFLFDP selects CFIFO1.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

仅当全局接受过滤器列表中的条目所接受的消息的DLC值等于或高于为此关联的全局接受过滤器列表条目配置的DLC值时，才通过DLC过滤器过程。该字段设置为0时，对应规则条目禁用DLC自动过滤功能。

表32.4显示了可配置的DLC值。

Table 32.4 DLC值的配置

Format	DLC[3]	DLC[2]	DLC[1]	DLC[0]	Description
CAN和CAN FD	0	0	0	0	收到消息的DLC=0或更多（DLC过滤器检查已禁用）
CAN和CAN FD	0	0	0	1	收到消息的DLC=1或更多
CAN和CAN FD	0	0	1	0	收到消息的DLC=2或更多
CAN和CAN FD	0	0	1	1	收到消息的DLC=3或更多
CAN和CAN FD	0	1	0	0	收到消息的DLC=4或更多
CAN和CAN FD	0	1	0	1	收到消息的DLC=5或更多
CAN和CAN FD	0	1	1	0	收到消息的DLC=6或更多
CAN和CAN FD	0	1	1	1	收到消息的DLC=7或更多
CAN	1	x	x	x	收到消息的DLC=8或更多
CAN-FD	1	0	0	0	收到消息的DLC=8个或更多*1
CAN-FD	1	0	0	1	收到消息的DLC=12或更多*1
CAN-FD	1	0	1	0	收到消息的DLC=16或更多*1
CAN-FD	1	0	1	1	收到消息的DLC=20或更多*1
CAN-FD	1	1	0	0	收到消息的DLC=24或更多*1
CAN-FD	1	1	0	1	收到消息的DLC=32或更多*1
CAN-FD	1	1	1	0	收到消息的DLC=48或更多*1
CAN-FD	1	1	1	1	收到消息的DLC=64*1

注1.此设置在经典CAN功能中不可用。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLSRD0位（全局接受过滤器列表选择路由目的地0）

GAFLSRD0位通过路由将复制目标更改为CFIFO0或TXQ0。

如果该位设置为1，则CFDGAFLP1n.GAFLFDP的预设值选择TXQueue。

如果该位设置为0，则CFDGAFLP1n.GAFLFDP的预设值选择CFIFO0。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLSRD1位（全局接受过滤器列表选择路由目的地1）

GAFLSRD1位通过路由将复制目标更改为CFIFO1或TXQ1。

如果该位设置为1，则CFDGAFLP1n.GAFLFDP的预设值选择TXQ1。

如果该位设置为0，则CFDGAFLP1n.GAFLFDP的预设值选择CFIFO1。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

Only write to the bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLSRD2 bit (Global Acceptance Filter List Select Routing Destination 2)

The GAFLSRD2 bit changes a copy destination to CFIFO2 or TXQ2 by routing.

If this bit is set to 1, the preset value of CFDGAFLP1n.GAFLFDP selects TXQ2.

If this bit is set to 0, the preset value of CFDGAFLP1n.GAFLFDP selects CFIFO2.

Do not write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to the bit when the CAN-FD module is in CH_RESET or CH_HALT mode.

GAFLIFL0 bit (Global Acceptance Filter List Information Label 0)

The GAFLIFL0 bit allows the configuration of a 2-bit information label that can be attached to a received message accepted by the related Global Acceptance Filter List entry. This bit is a LSB bit of an information label.

You cannot write to this bit when CFDGAFLECTR.AFLDAE bit is 0.

Only write to the bit when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

This bit is stored in Information Label Field[0] (CFDRMFDSTSn.RMIFL[0], CFDRFFDSTSn.RFIFL[0],CFDCFFDCSTSn.CFIFL[0]) of the storage location of an incoming message.

This bit is stored in CFDTHLACC1n.TIFL[0] when CFDTHLCCn.THLDGE = 1 is set up using the gateway function.

GAFLRMDP[4:0] bits (Global Acceptance Filter List RX Message Buffer Direction Pointer)

The GAFLRMDP[4:0] bits allow the configuration of a single reception message buffer as the destination target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry. The value entered is the single destination message buffer number.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

CFDRMNB.NRXMB[7:0] is the value entered in the RX Message Buffer Number Register to configure the number of RX message buffers. The value to be entered in CFDGAFLP0n.GAFLRMDP[6:0] bits should only be between 0x00 and CFDMNB.NMB[7:0] to 1 less.

If CFDRMNB.NRXMB[7:0] = 0x00, the GAFLRMV bit should be configured as 0.

GAFLRMV bit (Global Acceptance Filter List RX Message Buffer Valid)

The GAFLRMV bit allows the enabling or disabling of a single reception message buffer as the target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

GAFLPTR[15:0] bits (Global Acceptance Filter List Pointer)

The GAFLPTR[15:0] bits allow the configuration of a 16-bit pointer to be attached to a received message accepted by the related Global Acceptance Filter List entry. The pointer is added during message storage in the Message Buffer area and can be used by the application as a support function. The pointer information can be used for example, to support PDU Identifier allocation for the received message in AUTOSAR systems.

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0.

Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

GAFLSRD2位（全局接受过滤器列表选择路由目的地2）

GAFLSRD2位通过路由将复制目标更改为CFIFO2或TXQ2。

如果该位设置为1，则CFDGAFLP1n.GAFLFDP的预设值选择TXQ2。

如果该位设置为0，则CFDGAFLP1n.GAFLFDP的预设值选择CFIFO2。

当CFDGAFLECTR.AFLDAE位为0时，请勿写入该位。

仅当CAN-FD模块处于CH_RESET或CH_HALT模式时写入该位。

GAFLIFL0位（全局接受过滤器列表信息标签0）

GAFLIFL0位允许配置2位信息标签，该标签可以附加到相关全局接受过滤器列表条目接受的接收消息。该位是信息标签的LSB位。

当CFDGAFLECTR.AFLDAE位为0时，您不能写入该位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入该位。

该位存储在信息标签字段[0](CFDRMFDSTSn.RMIFL[0] CFDRFFDSTSn.RFIFL[0] CFDCFFDCSTSn.CFIFL[0])传入消息的存储位置。

当使用网关功能设置CFDTHLCCn.THLDGE=1时，该位存储在CFDTHLACC1n.TIFL[0]中。

GAFLRMDP[4:0]位（全局接受过滤器列表RX消息缓冲区方向指针）

GAFLRMDP[4:0]位允许将单个接收消息缓冲区配置为接收消息的目标目标，该消息通过相关全局接受过滤器列表条目的接受检查。输入的值是单个目标消息缓冲区号。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

CFDRMNB.NRXMB[7:0]是在RX消息缓冲区编号寄存器中输入的值，用于配置RX消息缓冲区的数量。要在CFDGAFLP0n.GAFLRMDP[6:0]位中输入的值只能在0x00和CFDMNB.NMB[7:0]之间减去1。

如果CFDRMNB.NRXMB[7:0]=0x00，则GAFLRMV位应配置为0。

GAFLRMV位（全局接受过滤器列表RX消息缓冲区有效）

GAFLRMV位允许启用或禁用单个接收消息缓冲区作为通过相关全局接受过滤器列表条目的接受检查的接收消息的目标。

当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

GAFLPTR[15:0]位（全局接受过滤器列表指针）

GAFLPTR[15:0]位允许配置一个16位指针，以附加到相关全局接受过滤器列表条目所接受的接收消息。该指针是在消息缓冲区中的消息存储期间添加的，并且可以由应用程序用作支持功能。例如，指针信息可用于支持AUTOSAR系统中接收到的消息的PDU标识符分配。

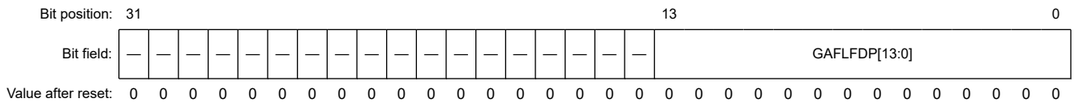
当CFDGAFLECTR.AFLDAE位为0时，不要写入这些位。

仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

32.2.23 CFDGAFLP1n : Global Acceptance Filter List Pointer 1 Registers (n = 1 to 16)

Base address: CANFD = 0x400B_0000

Offset address: 0x180C + 0x10 × (n - 1)



Bit	Symbol	Function	R/W
13:0	GAFLFDP[13:0]	Global Acceptance Filter List FIFO Direction Pointer FIFO direction pointer bits for received message storage	R/W
31:14	—	These bits are read as 0. The write value should be 0.	R/W

The Global Acceptance Filter List Pointer 1 registers are used to configure the FIFO direction pointer fields in each Rule Entry of the Global Acceptance Filter List.

GAFLFDP[13:0] bits (Global Acceptance Filter List FIFO Direction Pointer)

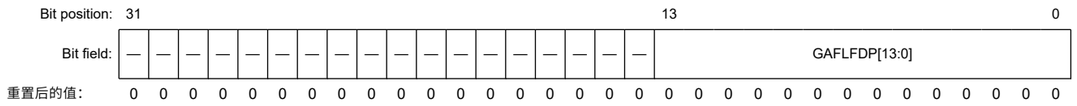
The GAFLFDP[13:0] bits allow the configuration of FIFO buffers as the target for a received message that passes the acceptance check of the related Global Acceptance Filter List entry. Each bit of the CFDGAFLP1n.GAFLFDP[13:0] is configured as dedicated FIFO.

Bit	Value (binary)	Function
0	0	Disable RX FIFO 0 as target for reception
	1	Enable RX FIFO 0 as target for reception
1	0	Disable RX FIFO 1 as target for reception
	1	Enable RX FIFO 1 as target for reception
2	0	Disable RX FIFO 2 as target for reception
	1	Enable RX FIFO 2 as target for reception
3	0	Disable RX FIFO 3 as target for reception
	1	Enable RX FIFO 3 as target for reception
4	0	Disable RX FIFO 4 as target for reception
	1	Enable RX FIFO 4 as target for reception
5	0	Disable RX FIFO 5 as target for reception
	1	Enable RX FIFO 5 as target for reception
6	0	Disable RX FIFO 6 as target for reception
	1	Enable RX FIFO 6 as target for reception
7	0	Disable RX FIFO 7 as target for reception
	1	Enable RX FIFO 7 as target for reception
8	0	Disable Common FIFO 0 and Channel 0 TX Queue 0 as target for reception
	1	GAFLSRD0 = 0: Enable Common FIFO 0 as target for reception GAFLSRD0 = 1: Enable Channel 0 TX Queue 0 as target for reception
9	0	Disable Common FIFO 1 and Channel 0 TX Queue 1 as target for reception
	1	GAFLSRD1 = 0: Enable Common FIFO 1 as target for reception GAFLSRD1 = 1: Enable Channel 0 TX Queue 1 as target for reception
10	0	Disable Common FIFO 2 and Channel 0 TX Queue 2 as target for reception
	1	GAFLSRD2 = 0: Enable Common FIFO 2 as target for reception GAFLSRD2 = 1: Enable Channel 0 TX Queue 2 as target for reception

32.2.23 CFDGAFLP1n：全局验收过滤器列表指针1寄存器（n=1到16）

Base address: CANFD = 0x400B_0000

Offset address: 0x180C + 0x10 × (n - 1)



Bit	Symbol	Function	R/W
13:0	GAFLFDP[13:0]	全局验收过滤器列表FIFO方向指针 用于接收消息存储的FIFO方向指针位	R/W
31:14	—	这些位被读取为0。写入值应为0。	R/W

全局接受过滤器列表指针1寄存器用于配置每个规则中的FIFO方向指针字段
全局接受过滤器列表的条目。

GAFLFDP[13:0]位（全局接受过滤器列表FIFO方向指针）

GAFLFDP[13:0]位允许将FIFO缓冲区配置为接收消息的目标，该消息通过相关全局接受过滤器列表条目的接受检查。CFDGAFLP1n.GAFLFDP[13:0]的每一位都配置为专用FIFO。

Bit	Value (binary)	Function
0	0	禁用RXFIFO0作为接收目标
	1	启用RXFIFO0作为接收目标
1	0	禁用RXFIFO1作为接收目标
	1	启用RXFIFO1作为接收目标
2	0	禁用RXFIFO2作为接收目标
	1	启用RXFIFO2作为接收目标
3	0	禁用RXFIFO3作为接收目标
	1	启用RXFIFO3作为接收目标
4	0	禁用RXFIFO4作为接收目标
	1	启用RXFIFO4作为接收目标
5	0	禁用RXFIFO5作为接收目标
	1	启用RXFIFO5作为接收目标
6	0	禁用RXFIFO6作为接收目标
	1	启用RXFIFO6作为接收目标
7	0	禁用RXFIFO7作为接收目标
	1	启用RXFIFO7作为接收目标
8	0	禁用CommonFIFO0和Channel0TXQueue0作为接收目标
	1	GAFLSRD0=0：启用CommonFIFO0作为接收目标 GAFLSRD0=1：启用通道0TX队列0作为接收目标
9	0	禁用CommonFIFO1和Channel0TXQueue1作为接收目标
	1	GAFLSRD1=0：启用CommonFIFO1作为接收目标 GAFLSRD1=1：启用通道0TX队列1作为接收目标
10	0	禁用CommonFIFO2和Channel0TXQueue2作为接收目标
	1	GAFLSRD2=0：启用CommonFIFO2作为接收目标 GAFLSRD2=1：启用通道0TX队列2作为接收目标

RA生态工作室

Bit	Value (binary)	Function
11	0	Disable Common FIFO 3 and Channel 1 TX Queue 0 as target for reception
	1	GAFLSRD0 = 0: Enable Common FIFO 3 as target for reception GAFLSRD0 = 1: Enable Channel 1 TX Queue 0 as target for reception
12	0	Disable Common FIFO 4 and Channel 1 TX Queue 1 as target for reception
	1	GAFLSRD1 = 0: Enable Common FIFO 4 as target for reception GAFLSRD1 = 1: Enable Channel 1 TX Queue 1 as target for reception
13	0	Disable Common FIFO 5 and Channel 1 TX Queue 2 as target for reception
	1	GAFLSRD2 = 0: Enable Common FIFO 5 as target for reception GAFLSRD2 = 1: Enable Channel 1 TX Queue 2 as target for reception

Do not write to these bits when CFDGAFLECTR.AFLDAE bit is 0. Only write to these bits when the related CAN-FD channel is in CH_RESET or CH_HALT mode.

For storage in TX queue, TX queue buffers of a target that is in GW mode is possible.

For storage in TX Queue, when these TX Queue buffers of a target are in GW mode, it can do.

Only one of the following configurations is valid:

- Up to 8 destination FIFO buffers
- 7 destination FIFO buffers plus one RX message buffer
- 8 destination TX queue buffers
- 7 destination TX queue buffers plus one RX message buffer
- A maximum of 8 destinations in all at FIFO buffer and TX queue buffer.

32.2.24 CFDRMNB : RX Message Buffer Number Register

Base address: CANFD = 0x400B_0000

Offset address: 0x00AC

Bit position:	31																				10	8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMPLS[2:0]		NRXMB[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	NRXMB[7:0]	Number of RX Message Buffers	R/W
10:8	RMPLS[2:0]*1	Reception Message Buffer Payload Data Size 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits are not available in the classical CAN function.

The RX Message Buffer Number register is used to configure the total number of RX message buffers allocated to all channels.

NRXMB[7:0] bits (Number of RX Message Buffers)

The NRXMB[7:0] bits are used to configure the number of RX message buffers.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

Bit	Value (binary)	Function
11	0	禁用CommonFIFO3和Channel1TXQueue0作为接收目标
	1	GAFLSRD0=0：启用CommonFIFO3作为接收目标 GAFLSRD0=1：启用通道1TX队列0作为接收目标
12	0	禁用CommonFIFO4和Channel1TXQueue1作为接收目标
	1	GAFLSRD1=0：启用CommonFIFO4作为接收目标 GAFLSRD1=1：启用通道1TX队列1作为接收目标
13	0	禁用CommonFIFO5和Channel1TXQueue2作为接收目标
	1	GAFLSRD2=0：启用CommonFIFO5作为接收目标 GAFLSRD2=1：启用通道1TX队列2作为接收目标

当CFDGAFLECTR.AFLDAE位为0时不要写入这些位。仅当相关CAN-FD通道处于CH_RESET或CH_HALT模式时才写入这些位。

对于TX队列中的存储，可以使用处于GW模式的目标的TX队列缓冲区。

对于TXQueue中的存储，当一个目标的这些TXQueue缓冲区处于GW模式时，它可以做到。

只有以下配置之一有效：

- ●多达8个目标FIFO缓冲区
- ●7个目标FIFO缓冲区和1个RX消息缓冲区
- ●8个目标TX队列缓冲区
- ●7个目标TX队列缓冲区和1个RX消息缓冲区
- ●FIFO缓冲区和TX队列缓冲区总共最多8个目的地。

32.2.24 CFDRMNB:RX消息缓冲区编号寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x00AC

Bit position:	31																				10	8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMPLS[2:0]		NRXMB[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	NRXMB[7:0]	RX消息缓冲区的数量	R/W
10:8	RMPLS[2:0]*1	接收消息缓冲区有效负载数据大小 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
31:11	—	这些位被读取为0。写入值应为0。	R/W

注1.这些位在经典CAN功能中不可用。

RX消息缓冲区编号寄存器用于配置分配给所有通道的RX消息缓冲区的总数。

NRXMB[7:0]位（RX消息缓冲区的数量）

NRXMB[7:0]位用于配置RX消息缓冲区的数量。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

Enter only values between 0 and 32 inclusive, with 0x00 indicating that no RX message buffer is allocated.

RMPLS[2:0] bits (Reception Message Buffer Payload Data Size)

The RMPLS[2:0] bits are used to configure the message buffer payload data size.

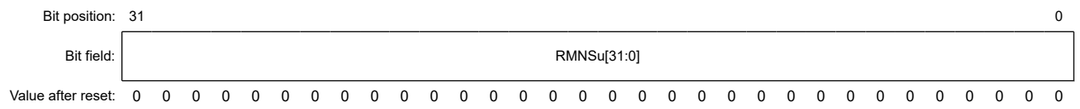
Only write to these bits when the CAN-FD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

32.2.25 CFDRMNDn : RX Message Buffer New Data Register n (n = 0)

Base address: CANFD = 0x400B_0000

Offset address: 0x00B0



Bit	Symbol	Function	R/W
31:0	RMNSu[31:0]	RX Message Buffer New Data Status 0: New data not stored in corresponding RX message buffer 1: New data stored in corresponding RX message buffer	R/W

The RX Message Buffer New Data Status Register (n = 0) specifies the new data storage status of the RX message buffers.

RMNSu[31:0] bits (RX Message Buffer New Data Status)

The RMNSu[31:0] bits indicate the status of new data for the corresponding RX message buffer. RMNS bit [0] corresponds to RX message buffer [0] and so on.

The bit position of CFDRMND corresponds to the buffer number of RXMB.

Do not write to these bits when the CAN-FD module is in GL_RESET or GL_SLEEP mode. Writing 1 has no effect.

These bits cannot be cleared when message storage in the corresponding RX message buffer is in progress.
Do not use the bit clear instruction to clear these bits. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

These bits are set automatically when storage of new messages are in the corresponding RX message buffer. These bits are cleared by writing 0. These bits are cleared automatically when the CAN-FD module is in GL_RESET mode.

When CFDRMNB.RMPLS = 000b (maximum 8 bytes payload), the duration of message storage is 6 PCLKB cycles.

When CFDRMNB.RMPLS > 000b, the duration of message storage is 6 PCLKB cycles + 1 for each 4 bytes (maximum of 20 PCLKB cycles for 64 bytes).

Note: This feature is not available in the classical CAN function.

仅输入介于0和32之间的值，其中0x00表示未分配RX消息缓冲区。

RMPLS[2:0]位（接收消息缓冲区有效负载数据大小）

RMPLS[2:0]位用于配置消息缓冲区有效负载数据大小。

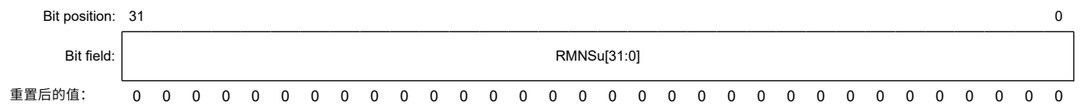
仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

Note: 这些位在经典CAN功能中不可用。

32.2.25 CFDRMNDn：RX消息缓冲区新数据寄存器n(n=0)

Base address: CANFD = 0x400B_0000

Offset address: 0x00B0



Bit	Symbol	Function	R/W
31:0	RMNSu[31:0]	RX消息缓冲区新数据状态 0：新数据未存储在相应的RX报文缓冲区中1：新数据存储在相应的RX报文缓冲区中	R/W

RX报文缓冲区新数据状态寄存器(n=0)指定RX报文缓冲区的新数据存储状态。

RMNSu[31:0]位（RX报文缓冲区新数据状态）

RMNSu[31:0]位指示相应RX消息缓冲区的新数据状态。RMNS位[0]对应于RX消息缓冲区[0]等等。

CFDRMND的位位置对应于RXMB的缓冲区号。

当CAN-FD模块处于GL_RESET或GL_SLEEP模式时，请勿写入这些位。写1无效。

当相应RX消息缓冲区中的消息存储正在进行时，这些位不能被清除。
不要使用位清除指令来清除这些位。使用MOV指令确保只清除指定位。其他位保持1。

当新消息存储在相应的RX消息缓冲区中时，这些位会自动设置。这些位通过写入0清除。当CAN-FD模块处于GL_RESET模式时，这些位会自动清除。

当CFDRMNB.RMPLS=000b（最大8字节有效载荷）时，消息存储的持续时间为6个PCLKB周期。

当CFDRMNB.RMPLS>000b时，消息存储的持续时间为6个PCLKB周期+每4个字节1个（64个字节最多20个PCLKB周期）。

Note: 此功能在经典CAN功能中不可用。

32.2.26 CFDRFCCn : RX FIFO Configuration/Control Registers n (n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x00C0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPLS[2:0]			—	—	RFIE	RFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFE	RX FIFO Enable 0: FIFO disabled 1: FIFO enabled	R/W
1	RFIE	RX FIFO Interrupt Enable 0: FIFO interrupt generation disabled 1: FIFO interrupt generation enabled	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
6:4	RFPLS[2:0]*1	Rx FIFO Payload Data Size Configuration 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
10:8	RFDC[2:0]	RX FIFO Depth Configuration 0 0 0: FIFO Depth = 0 message 0 0 1: FIFO Depth = 4 messages 0 1 0: FIFO Depth = 8 messages 0 1 1: FIFO Depth = 16 messages 1 0 0: FIFO Depth = 32 essages 1 0 1: FIFO Depth = 48 messages 1 1 0: FIFO Depth = 64 messages 1 1 1: FIFO Depth = 128 messages	R/W
11	—	This bit is read as 0. The write value should be 0.	R/W
12	RFIM	RX FIFO Interrupt Mode 0: Interrupt generated when RX FIFO counter reaches RFIGCV value from values smaller than RFIGCV 1: Interrupt generated at the end of every received message storage	R/W
15:13	RFIGCV[2:0]	RX FIFO Interrupt Generation Counter Value 0 0 0: Interrupt generated when FIFO is 1/8th full 0 0 1: Interrupt generated when FIFO is 1/4th full 0 1 0: Interrupt generated when FIFO is 3/8th full 0 1 1: Interrupt generated when FIFO is 1/2 full 1 0 0: Interrupt generated when FIFO is 5/8th full 1 0 1: Interrupt generated when FIFO is 3/4th full 1 1 0: Interrupt generated when FIFO is 7/8th full 1 1 1: Interrupt generated when FIFO is full	R/W
16	RFFIE	RX FIFO Full Interrupt Enable 0: FIFO interrupt generation disabled 1: FIFO interrupt generation enabled	R/W

32.2.26 CFDRFCCn：RXFIFO配置控制寄存器n（n=0到7）

Base address: CANFD = 0x400B_0000

Offset address: 0x00C0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFIE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	RFPLS[2:0]			—	—	RFIE	RFE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFE	RX FIFO Enable 0：禁用FIFO1： 启用FIFO	R/W
1	RFIE	RXFIFO中断使能 0：禁用FIFO中断生成1：启用FIFO中 断生成	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
6:4	RFPLS[2:0]*1	RxFIFO有效负载数据大小配置 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	该位读取为0。写入值应为0。	R/W
10:8	RFDC[2:0]	RXFIFO深度配置 000：FIFO深度=0条消息001：FIFO 深度=4条消息010：FIFO深度=8条消 息011：FIFO深度=16条消息100：FI FO深度=32条消息101：FIFO深度=4 8条消息110：FIFO深度=64条消息1 11：FIFO深度=128条消息	R/W
11	—	该位读取为0。写入值应为0。	R/W
12	RFIM	RXFIFO中断模式 0：当RXFIFO计数器从小于RFIGCV的值到达RFIGCV值时产生中断 1：在每个接收到的消息存储结束时产生中断	R/W
15:13	RFIGCV[2:0]	RXFIFO中断产生计数器值 000：FIFO1第8满时产生中断001：FIFO1第4满时 产生中断010：FIFO3第8满时产生中断011：FIFO 12满时产生中断100：当FIFO为5第8个满时产生 中断101：当FIFO第3个满时产生中断110：当FIF O第8个满时产生中断111：当FIFO满时产生中断	R/W
16	RFFIE	RXFIFO完全中断使能 0：禁用FIFO中断生成1：启用FIFO中 断生成	R/W

Bit	Symbol	Function	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits are not available in the classical CAN function.

The RX FIFO Configuration/Control Registers (n = 0 to 7) are used to configure and control the eight RX FIFOs.

RFE bit (RX FIFO Enable)

The RFE bit enables the FIFO. When this bit is set to 0, the RX FIFO is cleared to empty.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode.

This bit can only be set if the configured FIFO depth is greater than 0x000 (CFDRFCCn.RFDC > 0x000).

Set the RFE bit with a separate write access to the CFDRFCCn register, after all the other bits in the CFDRFCCn register are set.

This bit is cleared automatically when the CAN-FD module is in GL_RESET mode.

RFIE bit (RX FIFO Interrupt Enable)

The RFIE bit enables generation of the FIFO interrupt.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

RFPLS[2:0] bits (Rx FIFO Payload Data Size Configuration)

The RFPLS[2:0] bits define the message data payload allocation in the RAM.

This is the maximum number of bytes which can be received by this FIFO.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

RFDC[2:0] bits (RX FIFO Depth Configuration)

The RFDC[2:0] bits select the depth of the FIFO in terms of the number of messages. If the FIFO depth is configured to 0 messages, the FIFO cannot be used.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

RFIM bit (RX FIFO Interrupt Mode)

The RFIM bit selects the interrupt generation condition for the FIFO.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

Only write to this bit when the CAN-FD module is in GL_RESET mode.

RFIGCV[2:0] bits (RX FIFO Interrupt Generation Counter Value)

The RFIGCV[2:0] bits select the counter value of the FIFO for generation of FIFO interrupts. These values represent fractions of the FIFO depth for which an interrupt is generated.

Do not write to these bits when the CAN-FD module is in GL_SLEEP mode.

The setting of the RFIGCV[2:0] bits should be synchronized with the RFDC[2:0] bits.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

RFFIE bit (RX FIFO Full Interrupt Enable)

The RFFIE bit enables generation of the RXFIFO full interrupt. Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

The following content shows examples of interruptions:

- Interruption output in number of arbitrary stages (CFDRFCCn.RFIGCV)
- Interruption output in FIFO full state.

Note: Management of the receiving data of FIFO can be performed by these notices of interruption.

Bit	Symbol	Function	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

注1.这些位在经典CAN功能中不可用。

RXFIFO配置控制寄存器（n=0到7）用于配置和控制8个RXFIFO。

RFE bit (RX FIFO Enable)

RFE位使能FIFO。当该位设置为0时，RXFIFO被清空。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式时写入该位。

仅当配置的FIFO深度大于0x000(CFDRFCCn.RFDC>0x000)时才能设置该位。

在设置CFDRFCCn寄存器中的所有其他位之后，通过对CFDRFCCn寄存器的单独写访问来设置RFE位。

当CAN-FD模块处于GL_RESET模式时，该位会自动清零。

RFIE位（RXFIFO中断允许）

RFIE位使能FIFO中断的产生。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

RFPLS[2:0]位（RxFIFO有效负载数据大小配置）

RFPLS[2:0]位定义RAM中的消息数据有效负载分配。

这是该FIFO可以接收的最大字节数。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

Note: 这些位在经典CAN功能中不可用。

RFDC[2:0]位（RXFIFO深度配置）

RFDC[2:0]位根据消息数量选择FIFO的深度。如果FIFO深度配置为0消息，则无法使用FIFO。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

RFIM位（RXFIFO中断模式）

RFIM位选择FIFO的中断产生条件。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

仅当CAN-FD模块处于GL_RESET模式时写入该位。

RFIGCV[2:0]位（RXFIFO中断生成计数器值）

RFIGCV[2:0]位选择FIFO的计数器值以生成FIFO中断。这些值代表产生中断的FIFO深度的分数。

当CAN-FD模块处于GL_SLEEP模式时，不要写入这些位。

RFIGCV[2:0]位的设置应与RFDC[2:0]位同步。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

RFFIE位（RXFIFO完全中断使能）

RFFIE位使能RXFIFO满中断的产生。当CAN-FD模块处于工作状态时，请勿写入该位
GL_SLEEP mode.

以下内容显示了中断的示例：

●任意级数的中断输出(CFDRFCCn.RFIGCV)

●FIFO满状态下的中断输出。

Note: 可以通过这些中断通知来管理FIFO的接收数据。

32.2.27 CFDRFSTSn : RX FIFO Status Registers n (n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x00E0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFMC[7:0]								—	—	—	—	RFIF	RFML T	RFFLL	RFEM P
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	RFEMP	RX FIFO Empty 0: FIFO not empty 1: FIFO empty	R
1	RFFLL	RX FIFO Full 0: FIFO not full 1: FIFO full	R
2	RFMLT	RX FIFO Message Lost 0: No message lost in FIFO 1: FIFO message lost	R/W
3	RFIF	RX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied 1: FIFO interrupt condition satisfied	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
15:8	RFMC[7:0]	RX FIFO Message Count Number of messages stored in FIFO	R
16	RFFIF	RX FIFO Full Interrupt Flag 0: FIFO full interrupt condition not satisfied 1: FIFO full interrupt condition satisfied	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

The RX FIFO Status Registers (n = 0 to 7) show the status of messages stored in the corresponding FIFO buffers.

RFEMP bit (RX FIFO Empty)

The RFEMP bit is set automatically when:

- The RFMC bit is 0
- RX FIFO is disabled by setting the CFDRFCCn.RFE bit to is 0
- The CAN-FD module is in GL_RESET mode.

The RFEMP bit is cleared automatically when the first message is stored in the RX FIFO buffer.

RFFLL bit (RX FIFO Full)

The RFFLL bit is set automatically when the number of CAN messages stored in the FIFO buffer matches the configured FIFO depth.

The RFFLL is cleared automatically when:

- The number of CAN messages stored in the FIFO buffer is less than the configured FIFO depth
- RX FIFO is disabled by setting the CFDRFCCn.RFE bit to 0
- The CAN-FD module is in GL_RESET mode.

32.2.27 CDFRFTSn:RXFIFO状态寄存器n(n=0到7)

Base address: CANFD = 0x400B_0000

Offset address: 0x00E0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFIF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	RFMC[7:0]								—	—	—	—	RFIF	RFML T	RFFLL	RFEM P
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	RFEMP	RX FIFO Empty 0：FIFO非空1：FIF O空	R
1	RFFLL	RX FIFO Full 0：FIFO未满1 ：FIFO已满	R
2	RFMLT	RXFIFO消息丢失 0：FIFO中没有消息丢失1：FIFO消息丢失	R/W
3	RFIF	RXFIFO中断标志 0：不满足FIFO中断条件1：满足FIFO中断条件	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
15:8	RFMC[7:0]	RXFIFO消息计数 存储在FIFO中的消息数	R
16	RFFIF	RXFIFO满中断标志 0：不满足FIFO满中断条件1：满足FIFO满中断条件	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

RXFIFO状态寄存器（n=0到7）显示存储在相应FIFO缓冲区中的消息的状态。

RFEMP bit (RX FIFO Empty)

RFEMP位在以下情况下自动设置：

- RFMC位为0
- 通过将CFDRFCCn.RFE位设置为0来禁用RXFIFO
- CAN-FD模块处于GL_RESET模式。

当第一条消息存储在RXFIFO缓冲区中时，RFEMP位会自动清零。

RFFLL bit (RX FIFO Full)

当存储在FIFO缓冲区中的CAN报文数量与配置的匹配时，RFFLL位会自动设置FIFO depth.

RFFLL在以下情况下自动清除：

- FIFO缓冲区中存储的CAN报文数小于配置的FIFO深度
- 通过将CFDRFCCn.RFE位设置为0来禁用RXFIFO
- CAN-FD模块处于GL_RESET模式。

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RFMLT bit (RX FIFO Message Lost)

Only write to the RFMLT bit when CAN-FD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically whenever a message is lost due to attempted storage when the FIFO buffer is already full. If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode.

RFIF bit (RX FIFO Interrupt Flag)

The RFIF bit is set automatically when the configured interrupt condition is satisfied. This bit is not automatically cleared when the RX FIFO buffer is disabled.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then this bit is set.

The bit is cleared by writing 0 to it. The bit is also cleared when CAN-FD module is in GL_RESET mode.

RFMC[7:0] bits (RX FIFO Message Count)

The RFMC[7:0] bits indicate the number of CAN messages stored in the RX FIFO buffer that can be read by the CPU.

These bits are cleared automatically when the FIFO is disabled and when the CAN-FD module is in GL_RESET mode.

RFFIF bit (RX FIFO Full Interrupt Flag)

The RFFIF bit is not cleared automatically when the RX FIFO buffer is disabled.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the FIFO full interrupt condition is satisfied. If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The bit is cleared by writing 0 to it.

The bit is also cleared when the CAN-FD module is in GL_RESET mode.

32.2.28 CFDRFPCTRn : RX FIFO Pointer Control Registers n (n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x0100 + 0x04 × n

Bit position:	31	…	7	…	0
Bit field:	—	…	—	RFPC[7:0]	
Value after reset:	0	…	0	0	0

Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RX FIFO Pointer Control Increments read pointer of the corresponding RX FIFO buffers	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The RX FIFO Pointer Control Registers (n = 0 to 7) can be used to increment the read pointer of the corresponding RX FIFO buffers.

RFMLT位（RXFIFO消息丢失）

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式时写入RFMLT位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当FIFO缓冲区已满时，每当由于尝试存储而导致消息丢失时，该位会自动设置。如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

该位被清除：

●写入0

●CAN-FD模块处于GL_RESET模式时。

RFIF位（RXFIFO中断标志　　）

当配置的中断条件满足时，RFIF位自动置位。当RXFIFO缓冲器被禁用时，该位不会自动清除。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

如果来自CAN通道的设置与写访问清除同时发生，则设置该位。

该位通过向其写入0来清除。当CAN-FD模块处于GL_RESET模式时，该位也会被清除。

RFMC[7:0]位（RXFIFO消息计数）

RFMC[7:0]位指示存储在RXFIFO缓冲区中可供CPU读取的CAN报文数量。

当FIFO被禁用并且CAN-FD模块处于GL_RESET模式时，这些位会自动清除。

RFFIF位（RXFIFO满中断标志）

当RXFIFO缓冲区被禁用时，RFFIF位不会自动清除。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当满足FIFO满中断条件时，该位自动置位。如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

该位通过向其写入0来清除。

当CAN-FD模块处于GL_RESET模式时，该位也会被清除。

32.2.28 CFDRFPCTRn：RXFIFO指针控制寄存器n（n=0到7）

Base address: CANFD = 0x400B_0000

Offset address: 0x0100 + 0x04 × n

Bit position:	31	…	7	…	0
Bit field:	—	…	—	RFPC[7:0]	
重置后的值：	0	…	0	0	0

Bit	Symbol	Function	R/W
7:0	RFPC[7:0]	RXFIFO指针控制 增加相应RXFIFO缓冲区的读指针	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

RXFIFO指针控制寄存器（n=0到7）可用于递增相应RX的读指针
FIFO buffers.

RFPC bits (RX FIFO Pointer Control)

When the value 0xFF is written to the RFPC bits, the pointer of the corresponding RX FIFO buffer is moved to the next FIFO entry. Only write 0xFF to these registers when the corresponding RX FIFO buffer is enabled and not empty.

The read value from these bits is always 0x00.

Only write to these bits when the CAN-FD module is in GL_HALT or GL_OPERATION mode.

Do not write to the RX FIFO Pointer Control registers when DMA is enabled.

32.2.29 CFDCFCCn : Common FIFO Configuration/Control Registers n (n = 0 to 5)

Base address: CANFD = 0x400B_0000

Offset address: 0x0120 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFITT[7:0]								CFDC[2:0]			CFTML[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFIGCV[2:0]			CFIM	CFITR	CFITSS	CFM[1:0]		—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFE	Common FIFO Enable 0: FIFO disabled 1: FIFO enabled	R/W
1	CFRXIE	Common FIFO RX Interrupt Enable 0: FIFO interrupt generation disabled for Frame RX 1: FIFO interrupt generation enabled for Frame RX	R/W
2	CFTXIE	Common FIFO TX Interrupt Enable 0: FIFO interrupt generation disabled for Frame TX 1: FIFO interrupt generation enabled for Frame TX	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	CFPLS[2:0]*1	Common FIFO Payload Data Size Configuration 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
9:8	CFM[1:0]	Common FIFO Mode 0 0: RX FIFO mode 0 1: TX FIFO mode 1 0: CAN – CAN GW FIFO mode 1 1: Reserved	R/W
10	CFITSS	Common FIFO Interval Timer Source Select 0: Reference clock (× 1 / × 10 period) 1: Bit time clock of related channel (FIFO is linked to fixed channel)	R/W
11	CFITR	Common FIFO Interval Timer Resolution 0: Reference clock period × 1 1: Reference clock period × 10	R/W

RFPC位（RXFIFO指针控制）

当值0xFF写入RFPC位时，相应的RXFIFO缓冲区的指针移动到下一个
先进先出入口。仅当相应的RXFIFO缓冲区启用且不为空时，才将0xFF写入这些寄存器。

从这些位读取的值始终为0x00。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式时才写入这些位。

启用DMA时不要写入RXFIFO指针控制寄存器。

32.2.29 CFDCFCCn：通用FIFO配置控制寄存器n（n=0到5）

Base address: CANFD = 0x400B_0000

Offset address: 0x0120 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFITT[7:0]								CFDC[2:0]			CFTML[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFIGCV[2:0]			CFIM	CFITR	CFITSS	CFM[1:0]		—	CFPLS[2:0]			—	CFTXIE	CFRXIE	CFE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFE	通用FIFO使能 0：禁用FIFO1： 启用FIFO	R/W
1	CFRXIE	通用FIFORX中断使能 0：禁用帧RX的FIFO中断生成1：启用帧RX的FIFO中 断生成	R/W
2	CFTXIE	通用FIFOTX中断使能 0：禁用帧TX的FIFO中断生成1：启用帧TX的FIFO中 断生成	R/W
3	—	该位读取为0。写入值应为0。	R/W
6:4	CFPLS[2:0]*1	通用FIFO有效负载数据大小配置 0 0 0: 8 bytes 0 0 1: 12 bytes 0 1 0: 16 bytes 0 1 1: 20 bytes 1 0 0: 24 bytes 1 0 1: 32 bytes 1 1 0: 48 bytes 1 1 1: 64 bytes	R/W
7	—	该位读取为0。写入值应为0。	R/W
9:8	CFM[1:0]	普通先进先出模式 00：RXFIFO模式01：TXFIFO模式 10：CAN CANGWFIFO模式11： 保留	R/W
10	CFITSS	通用FIFO间隔定时器源选择 0：参考时钟（×1×10周期）1：相关通道的位时钟（FIFO链接到固定 通道）	R/W
11	CFITR	通用FIFO间隔定时器分辨率 0：参考时钟周期×11：参考时 钟周期×10	R/W

Bit	Symbol	Function	R/W
12	CFIM	Common FIFO Interrupt Mode 0: RX FIFO mode: RX interrupt generated when Common FIFO counter reaches CFIGCV value from a lower value TX FIFO mode: TX interrupt generated when Common FIFO transmits the last message successfully GW FIFO mode: For RX interrupt flag: Interrupt generated when FIFO counter increments and reaches the value configured in CFIGCV For TX interrupt flag: Interrupt generated when FIFO transmits the last message successfully 1: RX FIFO mode: RX interrupt generated at the end of every received message storage TX FIFO mode: interrupt generated for every successfully transmitted message GW FIFO mode: For RX interrupt flag: Interrupt generated when a message is stored in the FIFO For TX interrupt flag: Interrupt generated when a message is successfully transmitted from the FIFO	R/W
15:13	CFIGCV[2:0]	Common FIFO Interrupt Generation Counter Value 0 0 0: Interrupt generated when FIFO is 1/8th full 0 0 1: Interrupt generated when FIFO is 1/4th full 0 1 0: Interrupt generated when FIFO is 3/8th full 0 1 1: Interrupt generated when FIFO is 1/2 full 1 0 0: Interrupt generated when FIFO is 5/8th full 1 0 1: Interrupt generated when FIFO is 3/4th full 1 1 0: Interrupt generated when FIFO is 7/8th full 1 1 1: Interrupt generated when FIFO is full	R/W
20:16	CFTML[4:0]	Common FIFO TX Message Buffer Link Transmission scan link position of the corresponding channel	R/W
23:21	CFDC[2:0]	Common FIFO Depth Configuration 0 0 0: FIFO Depth = 0 messages 0 0 1: FIFO Depth = 4 messages 0 1 0: FIFO Depth = 8 messages 0 1 1: FIFO Depth = 16 messages 1 0 0: FIFO Depth = 32 messages 1 0 1: FIFO Depth = 48 messages 1 1 0: FIFO Depth = 64 messages 1 1 1: FIFO Depth = 128 messages	R/W
31:24	CFITT[7:0]	Common FIFO Interval Transmission Time Delay the start of transmission from the FIFO if configured in TX or GW mode, delay is a multiple of basic Interval Timer Clock Source unit	R/W

Note 1. These bits are not available in the classical CAN function.

CFE bit (Common FIFO Enable)

The CFE bit enables the FIFO when set. FIFO is disabled when this bit is cleared.

This bit can also be used, by clearing it, to abort transmission from Common FIFO when configured in TX mode or GW mode, or to stop reception into the Common FIFO in RX mode.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFOs configured as TX or GW FIFO.

This bit can only be set if the configured FIFO depth is greater than 0 (CFDC bit > 0).

Set the CFE bit with a separate write access to the CFDCFCCn register, after all the other bits in this register are set.

This bit is cleared automatically when the CAN-FD module is in GL_RESET mode.

This bit is also cleared automatically when the related channel is in CH_RESET mode if the FIFO is configured in TX or GW mode.

Bit	Symbol	Function	R/W
12	CFIM	通用FIFO中断模式 0：RXFIFO模式：CommonFIFO计数器从较低值到达CFIGCV值时产生RX中断 TXFIFO模式：CommonFIFO成功发送最后一条报文时产生TX中断GWFIFO模式： 对于RX中断标志 ：当FIFO计数器递增并达到CFIGCV中配置的值时产生中断 对于TX中断标志 ： FIFO成功发送最后一条报文时产生中断 1：RXFIFO模式：在每个接收到的消息存储结束时产生RX中断TXFIFO模式：在每个成功发送的消息产生中断 GW FIFO mode: 对于RX中断标志 ：消息存储在FIFO中时产生的中断 对于TX中断标志 ： 当消息从FIFO成功传输时产生中断	R/W
15:13	CFIGCV[2:0]	通用FIFO中断生成计数器值 000：FIFO1第8满时产生中断001：FIFO1第4满时产生中断010：FIFO3第8满时产生中断011：FIFO12满时产生中断100：当FIFO为5第8个满时产生中断101：当FIFO第3个满时产生中断110：当FIFO第8个满时产生中断111：当FIFO满时产生中断	R/W
20:16	CFTML[4:0]	通用FIFOTX消息缓冲区链接 对应通道的传输扫描链接位置	R/W
23:21	CFDC[2:0]	通用FIFO深度配置 000：FIFO深度=0条消息001：FIFO深度=4条消息010：FIFO深度=8条消息011：FIFO深度=16条消息100：FIFO深度=32条消息101：FIFO深度=48条消息110：FIFO深度=64条消息111：FIFO深度=128条消息	R/W
31:24	CFITT[7:0]	公共FIFO间隔传输时间 如果配置为TX或GW模式，则延迟从FIFO开始传输，延迟是基本间隔定时器时钟源单元的倍数	R/W

注1.这些位在经典CAN功能中不可用。

CFE bit (Common FIFO Enable)

CFE位在设置时启用FIFO。当该位清零时，FIFO被禁用。

当配置为TX模式或GW模式时，通过清零该位也可用于中止来自CommonFIFO的传输，或在RX模式下停止接收到CommonFIFO。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关CAN-FD通道未处于配置为TX或GWFIFO的FIFO的CH_RESET模式时写入该位。

仅当配置的FIFO深度大于0（CFDC位>0）时，才能设置该位。

在设置该寄存器中的所有其他位之后，通过对CFDCFCCn寄存器的单独写访问来设置CFE位。

当CAN-FD模块处于GL_RESET模式时，该位会自动清零。

如果FIFO配置为TX或
GW mode.

CFRXIE bit (Common FIFO RX Interrupt Enable)

The CFRXIE bit enables generation of FIFO interrupts when the interrupt flag is set after reception of a frame in the corresponding FIFO buffer.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

CFTXIE bit (Common FIFO TX Interrupt Enable)

The CFTXIE bit enables generation of common FIFO interrupts when the interrupt flag is set after transmission of a frame from the corresponding FIFO buffer.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

CFPLS[2:0] bits (Common FIFO Payload Data Size Configuration)

The CFPLS[2:0] bits define the message data payload allocation in the RAM. This is the maximum number of bytes which can be received or transmitted by the FIFO buffer.

For details, see section 32.6. FIFO Buffers and Normal Message Buffer Configuration.

Only write to this bit when the CAN-FD module is in GL_RESET mode.

Note: These bits are not available in the classical CAN function.

CFM[1:0] bits (Common FIFO Mode)

The CFM[1:0] bits select the mode of the FIFO. When a hardware reset is applied, all the Common FIFO buffers are configured in RX FIFO mode. Do not configure these bits to 11b.

Do not write to these bits in GL_OPERATION or GL_SLEEP mode.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

CFITSS bit (Common FIFO Interval Timer Source Select)

The CFITSS bit selects the basic clock source for the Interval Transmission Timer.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode. In addition, do not write to this bit when the CFE bit is set to 1.

Do not write 1 to this bit when CAN-FD communication is used.*1

Note: The bit time clock can vary depending on the nominal and data rate bit configuration.

Note 1. This feature is not available in the classical CAN function.

CFITR bit (Common FIFO Interval Timer Resolution)

The CFITR bit selects the resolution of the reference clock for the Interval Transmission Timer (peripheral clock is the source for the reference clock).

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode. Also, do not write to this bit when the CFE bit is set to 1.

CFIM bit (Common FIFO Interrupt Mode)

The CFIM bit selects the interrupt generation condition for the FIFO buffer.

Do not write to this bit in GL_SLEEP mode.

Only write to this bit when the CAN-FD module is in GL_RESET mode.

CFIGCV[2:0] bits (Common FIFO Interrupt Generation Counter Value)

The CFIGCV[2:0] bits select the message counter value for the generation of FIFO interrupts. These values represent fractions of the FIFO depth at which the interrupt is to be generated.

Do not write to these bits when the CAN-FD module is in GL_SLEEP mode.

The setting of these bits should be synchronized with the CFDC[2:0] bits.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

CFRXIE位（通用FIFORX中断使能）

当在相应的FIFO缓冲区中接收到帧后设置中断标志时，CFRXIE位允许生成FIFO中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

CFTXIE位（通用FIFOTX中断使能）

当从相应的FIFO缓冲区传输帧后设置中断标志时，CFTXIE位使能通用FIFO中断的生成。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

CFPLS[2:0]位（通用FIFO有效负载数据大小配置）

CFPLS[2:0]位定义RAM中的消息数据有效负载分配。这是FIFO缓冲区可以接收或发送的最大字节数。

有关详细信息，请参阅第32.6节。FIFO缓冲区和正常消息缓冲区配置。

仅当CAN-FD模块处于GL_RESET模式时写入该位。

Note: 这些位在经典CAN功能中不可用。

CFM[1:0] bits (Common FIFO Mode)

CFM[1:0]位选择FIFO的模式。应用硬件复位时，所有通用FIFO缓冲区都配置为RXFIFO模式。不要将这些位配置为11b。

不要在GL_OPERATION或GL_SLEEP模式下写入这些位。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

CFITSS位（通用FIFO间隔定时器源选择）

CFITSS位选择间隔传输定时器的基本时钟源。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。此外，当CFE位设置为1时，请勿写入该位。

使用CAN-FD通信时，请勿向该位写入1。*1

Note: 位时钟可以根据标称和数据速率位配置而变化。

注1.此功能在经典CAN功能中不可用。

CFITR位（通用FIFO间隔定时器分辨率）

CFITR位为间隔传输定时器选择参考时钟的分辨率（外围时钟是参考时钟的来源）。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。此外，当CFE位设置为1时，请勿写入该位。

CFIM位（通用FIFO中断模式）

CFIM位选择FIFO缓冲器的中断产生条件。

不要在GL_SLEEP模式下写入该位。

仅当CAN-FD模块处于GL_RESET模式时写入该位。

CFIGCV[2:0]位（通用FIFO中断生成计数器值）

CFIGCV[2:0]位选择用于生成FIFO中断的消息计数器值。这些值表示要生成中断的FIFO深度的分数。

当CAN-FD模块处于GL_SLEEP模式时，不要写入这些位。

这些位的设置应与CFDC[2:0]位同步。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

CFTML[4:0] bits (Common FIFO TX Message Buffer Link)

The CFTML[4:0] bits select the normal transmit message buffer position where the TX or GW FIFO is linked to, for transmission scanning.

Do not write to these bits in GL_OPERATION or GL_SLEEP mode.

Only write to this bit when the CAN-FD module is in GL_RESET mode.

CFDC[2:0] bits (Common FIFO Depth Configuration)

The CFDC[2:0] bits select the depth of the common FIFO in terms of the number of messages. If the FIFO depth is configured to 0 message, the FIFO cannot be used.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

CFITT[7:0] bits (Common FIFO Interval Transmission Time)

The CFITT[7:0] bits select the delay in the start of transmission for all messages transmitted from this FIFO buffer when configured in TX or GW mode. The delay is a multiple of the basic interval timer clock source period (reference clock × 1, reference clock × 10, or bit time clock of the related CAN channel).

Do not write to these bits when the CAN-FD module is in GL_SLEEP mode.

Do not write to these bits when the CFE bit is set to 1.

When CFDGCFG.ITRCP[15:0] = 0x0000, set the CFITT[7:0] bits to 0x0000.

32.2.30 CFDCFCCEn : Common FIFO Configuration/Control Enhancement Registers n (n = 0 to 5)

Base address: CANFD = 0x400B_0000

Offset address: 0x0180 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFBME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFMOWM	—	—	—	—	—	CFOFTXIE	CFOFRXIE	CFFIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFFIE	Common FIFO Full Interrupt Enable 0: FIFO Interrupt generation disabled 1: FIFO Interrupt generation enabled	R/W
1	CFOFRXIE	Common FIFO One Frame Reception Interrupt Enable 0: One Frame RX interrupt generation disabled 1: One Frame RX interrupt generation enabled	R/W
2	CFOFTXIE	Common FIFO One Frame Transmission Interrupt Enable 0: One Frame TX interrupt generation disabled 1: One Frame TX interrupt generation enabled	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	CFMOWM	Common FIFO Message Overwrite Mode 0: Message discarded mode 1: Message overwrite mode	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
16	CFBME	Common FIFO Buffering Mode Enable 0: Transmission from Common FIFO 1: Transmission halt from Common FIFO	R/W

CFTML[4:0]位（通用FIFOTX报文缓冲区链接）

CFTML[4:0]位选择TX或GWFIFO链接到的正常发送消息缓冲区位置，用于发送扫描。

不要在GL_OPERATION或GL_SLEEP模式下写入这些位。

仅当CAN-FD模块处于GL_RESET模式时写入该位。

CFDC[2:0]位（通用FIFO深度配置）

CFDC[2:0]位根据消息数量选择公共FIFO的深度。如果FIFO深度配置为0报文，则无法使用FIFO。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

CFITT[7:0]位（通用FIFO间隔传输时间）

当配置为TX或GW模式时，CFTT[7:0]位选择从此FIFO缓冲区发送的所有消息的开始发送延迟。延迟是基本间隔定时器时钟源周期（参考时钟×1，参考时钟×10，或相关CAN通道的位时钟）的倍数。

当CAN-FD模块处于GL_SLEEP模式时，不要写入这些位。

当CFE位设置为1时，请勿写入这些位。

当CFDGCFG.ITRCP[15:0]=0x0000时，将CFITT[7:0]位设置为0x0000。

32.2.30 CFDCFCCEn：通用FIFO配置控制增强寄存器n（n=0到5）

Base address: CANFD = 0x400B_0000

Offset address: 0x0180 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFBME
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CFMOWM	—	—	—	—	—	CFOFTXIE	CFOFRXIE	CFFIE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFFIE	通用FIFO完全中断使能 0：禁用FIFO中断生成1：启用FIFO中断生成	R/W
1	CFOFRXIE	通用FIFO一帧接收中断使能 0：禁止产生一帧RX中断1：允许产生一帧RX中断	R/W
2	CFOFTXIE	通用FIFO一帧传输中断使能 0：禁用一帧TX中断生成1：启用一帧TX中断生成	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	CFMOWM	通用FIFO报文覆盖模式 0：报文丢弃模式1：报文覆盖模式	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
16	CFBME	通用FIFO缓冲模式使能 0：来自CommonFIFO的传输1：来自CommonFIFO的传输停止	R/W

Bit	Symbol	Function	R/W
31:17	—	These bits are read as 0. The write value should be 0.	R/W

The Common FIFO Configuration/Control Enhancement Registers (n = 0 to 5) are used to configure the Common FIFOs.

no_of_channels = 2

no_of_CFIFOs_per_channel = Number of Common FIFOs per channel = 3

Where the total number of CFIFOs = no_of_CFIFOs_per_channel × no_of_channels = 3 × 2 = 6 as shown in Figure 32.28.

n = Common FIFO index = [0 .. no_of_CFIFOs - 1]

CFFIE bit (Common FIFO Full Interrupt Enable)

The CFFIE bit enables generation of the FIFO full interrupt when the interrupt flag is set after reception of a frame in the corresponding FIFO buffer.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

The following content shows examples of interruptions:

1. Interruption output in number of arbitrary stages (CFDCFCCn.CFIGCV)
2. Interruption output in FIFO full state.

Management of the receiving data of FIFO can be performed by these notices of interruption.

CFOFRXIE bit (Common FIFO One Frame Reception Interrupt Enable)

The CFOFRXIE bit enables generation of the one frame reception interrupt when the interrupt flag is set after reception of a frame in the corresponding FIFO buffer.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

CFOFTXIE bit (Common FIFO One Frame Transmission Interrupt Enable)

The CFOFTXIE bit enables generation of the one frame transmission interrupt when the interrupt flag is set after transmission of a frame in the corresponding FIFO buffer.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

CFMOWM bit (Common FIFO Message Overwrite Mode)

When the CFMOWM bit is 0, a receiving message is discarded and FIFO is full. When the CFMOWM bit is 1, a receiving message is overwritten and FIFO is full.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode.

Only write 1 to this bit when the common FIFO is in GW mode.

Do not write 1 to this bit when the CFE bit is 1.

CFBME bit (Common FIFO Buffering Mode Enable)

When the CFBME bit is 0, messages are transmitted from FIFO. When the CFBME bit is 1, messages are not transmitted from FIFO.

Do not write to this bit when the CAN-FD module is in GL_SLEEP mode. Additionally, do not write 1 to this bit when the CFE bit is 1.

Bit	Symbol	Function	R/W
31:17	—	这些位被读取为0。写入值应为0。	R/W

通用FIFO配置控制增强寄存器（n=0到5）用于配置通用FIFO。

no_of_channels = 2

no_of_CFIFOs_per_channel=每个通道的公共FIFO数量=3

其中CFIFO的总数=no_of_CFIFOs_per_channel×no_of_channels=3×2=6，如图32.28所示。

n=通用FIFO索引=[0..no_of_CFIFOs1]

CFFIE位（通用FIFO满中断使能）

当在相应的FIFO缓冲区中接收到帧后设置中断标志时，CFFIE位使能生成FIFO满中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

以下内容显示了中断的示例：

1.任意级数的中断输出（CFDCFCCn.CFIGCV）

2.FIFO满状态下的中断输出。

可以通过这些中断通知来管理FIFO的接收数据。

CFOFRXIE位（通用FIFO一帧接收中断使能）

CFOFRXIE位允许在相应FIFO缓冲区中接收到一帧后设置中断标志时生成一帧接收中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

CFOFTXIE位（通用FIFO一帧传输中断使能）

CFOFTXIE位允许在相应FIFO缓冲区中传输一帧后设置中断标志时生成一帧传输中断。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

CFMOWM位（通用FIFO消息覆盖模式）

当CFMOWM位为0时，接收报文被丢弃且FIFO已满。当CFMOWM位为1时，接收报文被覆盖且FIFO已满。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。

仅当通用FIFO处于GW模式时向该位写入1。

当CFE位为1时，请勿向该位写入1。

CFBME位（通用FIFO缓冲模式使能）

当CFBME位为0时，消息从FIFO发送。当CFBME位为1时，不从FIFO发送消息。

当CAN-FD模块处于GL_SLEEP模式时，请勿写入该位。此外，当CFE位为1。

32.2.31 CFDCFSTSn : Common FIFO Status Registers n (n = 0 to 5)

Base address: CANFD = 0x400B_0000

Offset address: 0x01E0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	CFMOW	—	—	—	—	—	CFOFTXIF	CFOFRXIF	CFFIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFMC[7:0]								—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CFEMP	Common FIFO Empty 0: FIFO not empty 1: FIFO empty	R
1	CFFLL	Common FIFO Full 0: FIFO not full 1: FIFO full	R
2	CFMLT	Common FIFO Message Lost 0: Number of message lost in FIFO 1: FIFO message lost	R/W
3	CFRXIF	Common RX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied after frame reception 1: FIFO interrupt condition satisfied after frame reception	R/W
4	CFTXIF	Common TX FIFO Interrupt Flag 0: FIFO interrupt condition not satisfied after frame transmission 1: FIFO Interrupt condition satisfied after frame transmission	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
15:8	CFMC[7:0]	Common FIFO Message Count Number of messages stored in FIFO	R
16	CFFIF	Common FIFO Full Interrupt Flag 0: Interrupt condition not satisfied for FIFO full interrupt 1: Interrupt condition satisfied for FIFO full interrupt	R/W
17	CFOFRXIF	Common FIFO One Frame Reception Interrupt Flag For each FIFO that receives a frame, a corresponding interrupt is set.	R/W
18	CFOFTXIF	Common FIFO One Frame Transmission Interrupt Flag For each FIFO that transmits a frame, a corresponding interrupt is set.	R/W
23:19	—	These bits are read as 0. The write value should be 0.	R/W
24	CFMOW	Common FIFO Message Overwrite 0: No message overwrite occurred in FIFO 1: Message overwrite occurred in FIFO	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

CFEMP bit (Common FIFO Empty)

The CFEMP bit is set automatically when:

- The CPU has read all messages from the FIFO configured in RX mode
- All messages have been transmitted from the FIFO configured in TX or GW mode
- The FIFO is disabled by setting the CFE bit to 0
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET when FIFO configured in TX or GW mode.

32.2.31 CFDCFSTSn：通用FIFO状态寄存器n（n=0到5）

Base address: CANFD = 0x400B_0000

Offset address: 0x01E0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	CFMOW	—	—	—	—	—	CFOFTXIF	CFOFRXIF	CFFIF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CFMC[7:0]								—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CFEMP	普通FIFO空 0：FIFO非空1：FIFO空	R
1	CFFLL	通用FIFO已满 0：FIFO未满1：FIFO已满	R
2	CFMLT	普通FIFO消息丢失 0：FIFO中丢失的报文数1：FIFO报文丢失	R/W
3	CFRXIF	通用RXFIFO中断标志 0：接收帧后不满足FIFO中断条件1：接收帧后满足FIFO中断条件	R/W
4	CFTXIF	通用TXFIFO中断标志 0：帧发送后不满足FIFO中断条件1：帧发送后满足FIFO中断条件	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
15:8	CFMC[7:0]	通用FIFO消息计数 存储在FIFO中的消息数	R
16	CFFIF	通用FIFO满中断标志 0：FIFO满中断不满足中断条件1：FIFO满中断满足中断条件	R/W
17	CFOFRXIF	通用FIFO一帧接收中断标志 对于每个接收到帧的FIFO，都会设置一个相应的中断。	R/W
18	CFOFTXIF	通用FIFO一帧传输中断标志 对于每个传输帧的FIFO，都会设置一个相应的中断。	R/W
23:19	—	这些位被读取为0。写入值应为0。	R/W
24	CFMOW	通用FIFO消息覆盖 0：FIFO中未发生报文覆盖1：FIFO中发生报文覆盖	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

CFEMP bit (Common FIFO Empty)

CFEMP位在以下情况下自动设置：

- ●CPU已从配置为RX模式的FIFO中读取所有消息
- ●所有消息均已从配置为TX或GW模式的FIFO发送
- ●通过将CFE位设置为0来禁用FIFO
- ●CAN-FD模块处于GL_RESET模式
- ●当FIFO配置为TX或GW模式时，相关CAN-FD通道处于CH_RESET状态。

The CFEMP bit is cleared automatically when:

- The first reception message is stored in the FIFO buffer when configured in RX mode
- The first message to be transmitted is stored in the FIFO buffer when configured in TX or GW mode.

CFFLL bit (Common FIFO Full)

The CFFLL bit is set automatically when the number of CAN messages stored in the FIFO matches the configured FIFO depth.

The CFFLL bit is cleared automatically when:

- The number of CAN messages stored in the FIFO is less than the configured FIFO depth
- The FIFO is disabled by setting the CFE bit to 0
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode when FIFO buffer is configured in TX or GW mode.

CFMLT bit (Common FIFO Message Lost)

The CFMLT bit is set automatically whenever a message is lost due to attempted storage of a new message when FIFO is already full in RX or GW mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then this bit is set.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFO configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The CFMLT bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in TX or GW mode.

CFRXIF bit (Common RX FIFO Interrupt Flag)

The CFRXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFO configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the configured interrupt condition is satisfied for Common FIFO buffers when configured in GW mode or RX mode.

The CFRXIF bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in GW mode.

CFTXIF bit (Common TX FIFO Interrupt Flag)

The CFTXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFO buffer configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the configured interrupt condition is satisfied for Common FIFO buffers configured in GW or TX mode.

CFEMP位在以下情况下自动清零：

●当配置为RX模式时，第一个接收报文存储在FIFO缓冲区中

●当配置为TX或GW模式时，要发送的第一个消息存储在FIFO缓冲区中。

CFFLL bit (Common FIFO Full)

当存储在FIFO中的CAN报文数量与配置的FIFO深度匹配时，CFFLL位会自动设置。

CFFLL位在以下情况下自动清零：

●FIFO中存储的CAN报文数量小于配置的FIFO深度

●通过将CFE位设置为0来禁用FIFO

●CAN-FD模块处于GL_RESET模式

●当FIFO缓冲区配置为TX或GW模式时，相关CAN-FD通道处于CH_RESET模式。

CFMLT位（通用FIFO消息丢失）

当RX或GW模式下FIFO已满时，每当由于尝试存储新消息而导致消息丢失时，CFMLT位会自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则设置该位。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关CAN-FD通道未处于CH_RESET模式（对于配置为TX或GWFIFO的FIFO）时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

CFMLT位清零：

●写入0

●CAN-FD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX或GW模式，则相关CAN-FD通道处于CH_RESET模式时。

CFRXIF位（通用RXFIFO中断标志 ）

如果禁用通用FIFO缓冲区，则CFRXIF位不会自动清除。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关CAN-FD通道未处于CH_RESET模式（对于配置为TX或GWFIFO的FIFO）时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置为GW模式或RX模式时，当配置的通用FIFO缓冲区满足配置的中断条件时，该位自动设置。

CFRXIF位清零：

●写入0

●CAN-FD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为GW模式，则相关CAN-FD通道处于CH_RESET模式时。

CFTXIF位（通用TXFIFO中断标志 ）

如果禁用通用FIFO缓冲区，CFTXIF位不会自动清除。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关的CAN-FD通道未处于CH_RESET模式时才写入该位，以用于配置为TX或GWFIFO的FIFO缓冲区。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置中配置的通用FIFO缓冲区满足配置的中断条件时，该位自动设置
GW或TX模式。

The CFTXIF bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in TX or GW mode.

CFMC[7:0] bits (Common FIFO Message Count)

The CFMC[7:0] bits indicate the following:

- Number of CAN messages stored by the CPU in the FIFO buffer configured in TX mode pending for transmission
- Number of CAN messages stored in the FIFO buffer configured in RX mode by RS-CAN-FD to be read by the CPU
- Number of CAN messages stored by the RS-CAN-FD in the GW FIFO pending for transmission.

The CFMC[7:0] bits are cleared automatically when:

- The FIFO is disabled
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in TX or GW mode.

CFFIF bit (Common FIFO Full Interrupt Flag)

The CFFIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFO configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the FIFO Full Interrupt condition is satisfied for Common FIFO buffers when configured in GW or RX mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The CFFIF bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in TX or GW mode.

CFOFRXIF bit (Common FIFO One Frame Reception Interrupt Flag)

The CFOFRXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for the FIFO buffer configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the One Frame Reception Interrupt condition is satisfied for the Common FIFO buffers when configured in GW or RX mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The CFOFRXIF bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in TX or GW mode.

CFOFTXIF bit (Common FIFO One Frame Transmission Interrupt Flag)

The CFOFTXIF bit is not cleared automatically if the Common FIFO buffer is disabled.

CFTXIF位清零：

●写入0

●CAN-FD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX或GW模式，则相关CAN-FD通道处于CH_RESET模式时。

CFMC[7:0]位（通用FIFO消息计数）

CFMC[7:0]位指示以下内容：

●CPU存储在TX模式下配置的FIFO缓冲区中等待传输的CAN报文数

●RS-CAN-FD在RX模式下配置的FIFO缓冲区中存储的可供CPU读取的CAN报文数

●RS-CAN-FD存储在GWFIFO中等待传输的CAN消息数。

CFMC[7:0]位在以下情况下自动清零：

●FIFO被禁用

●CAN-FD模块处于GL_RESET模式

●如果FIFO缓冲区配置为TX或GW模式，则相关CAN-FD通道处于CH_RESET模式。

CFFIF位（通用FIFO满中断标志）

如果禁用通用FIFO缓冲区，则CFFIF位不会自动清除。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关CAN-FD通道未处于CH_RESET模式（对于配置为TX或GWFIFO的FIFO）时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置为GW或RX模式时，当满足通用FIFO缓冲区的FIFO满中断条件时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

CFFIF位清零：

●写入0

●CAN-FD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX或GW模式，则相关CAN-FD通道处于CH_RESET模式时。

CFOFRXIF位（通用FIFO一帧接收中断标志）

如果禁用通用FIFO缓冲区，CFOFRXIF位不会自动清除。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关CAN-FD通道未处于配置为TX或GWFIFO的FIFO缓冲区的CH_RESET模式时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置为GW或RX模式时，当满足通用FIFO缓冲区的一帧接收中断条件时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

CFOFRXIF位清零：

●写入0

●CAN-FD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX或GW模式，则相关CAN-FD通道处于CH_RESET模式时。

CFOFTXIF位（通用FIFO一帧传输中断标志）

如果禁用通用FIFO缓冲区，则CFOFTXIF位不会自动清除。

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFOs configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is set automatically when the One Frame Transmission Interrupt condition is satisfied for Common FIFO buffers configured in GW mode or TX mode.

If a set from the CAN channel occurs simultaneously with a clear by a write access, then the bit is set.

The bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO is configured in TX or GW mode.

CFMOW bit (Common FIFO Message Overwrite)

The CFMOW bit is set automatically whenever a message is an overwrite storage of a new message when CFDCFCCEn.CFMOWM = 1 and FIFO is already full in GW mode.

If the set from the CAN channel occurs simultaneously with the clear by a write access, the bit is set.

Only write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode and the related CAN-FD channel is not in CH_RESET mode for FIFO buffer configured as TX or GW FIFO. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

The CFMOW bit is cleared:

- By writing 0 to it
- When the CAN-FD module is in GL_RESET mode
- When the related CAN-FD channel is in CH_RESET mode if the FIFO buffer is configured in TX or GW mode.

32.2.32 CFDCFPCTRn : Common FIFO Pointer Control Registers n (n = 0 to 5)

Base address: CANFD = 0x400B_0000

Offset address: 0x0240 + 0x04 × n

Bit position:	31																								7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	Common FIFO Pointer Control Increments read or write pointer of the corresponding Common FIFO buffers depending on the mode configuration.	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The Common FIFO Pointer Control Registers (n = 0 to 5) can be used to increment the read or write pointer of the corresponding Common FIFO buffer.

CFPC[7:0] bits (Common FIFO Pointer Control)

When the value 0xFF is written into the CFPC[7:0] bits, the read pointer of the corresponding Common FIFO buffer (when configured in RX mode), or the write pointer of the corresponding Common FIFO buffer (when configured in TX mode) moves to the next FIFO entry.

The read value from these bits is always 0x00.

Only write to these bits when the CAN-FD module is in GL_HALT or GL_OPERATION mode.

Only write 0xFF to this register when:

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关CAN-FD通道未处于配置为TX或GWFIFO的FIFO的CH_RESET模式时写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

当配置为GW模式或TX模式的通用FIFO缓冲区满足单帧传输中断条件时，该位自动设置。

如果来自CAN通道的设置与写访问清除同时发生，则该位被设置。

该位被清除：

●写入0

●CAN-FD模块处于GL_RESET模式时

●当FIFO配置为TX或GW模式时，相关CAN-FD通道为CH_RESET模式。

CFMOW位（通用FIFO消息覆盖）

每当一条消息是新消息的覆盖存储时，CFMOW位就会自动设置
CFDCFCCEn.CFMOWM=1，在GW模式下FIFO已满。

如果来自CAN通道的设置与通过写访问清除同时发生，则设置该位。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式且相关的CAN-FD通道未处于CH_RESET模式时才写入该位，以用于配置为TX或GWFIFO的FIFO缓冲区。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

CFMOW位清零：

●写入0

●CAN-FD模块处于GL_RESET模式时

●如果FIFO缓冲区配置为TX或GW模式，则相关CAN-FD通道处于CH_RESET模式时。

32.2.32 CFDCFPCTRn：通用FIFO指针控制寄存器n（n=0到5）

Base address: CANFD = 0x400B_0000

Offset address: 0x0240 + 0x04 × n

Bit position:	31																								7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFPC[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFPC[7:0]	通用FIFO指针控制 根据模式配置增加相应通用FIFO缓冲区的读取或写入指针。	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

通用FIFO指针控制寄存器（n=0到5）可用于递增相应通用FIFO缓冲区的读或写指针。

CFPC[7:0]位（通用FIFO指针控制）

当值0xFF写入CFPC[7:0]位时，对应CommonFIFO缓冲区的读指针（配置为RX模式时），或对应的CommonFIFO缓冲区的写指针（配置为TX模式时）移动到下一个FIFO条目。

从这些位读取的值始终为0x00。

仅当CAN-FD模块处于GL_HALT或GL_OPERATION模式时才写入这些位。

仅在以下情况下向该寄存器写入0xFF：

- The Common FIFO buffer is enabled and is not empty if configured in RX mode
- The Common FIFO buffer is enabled and is not full if configured in TX mode
- The Common FIFO buffer is enabled and is not configured in GW mode.

Do not write to the Common FIFO Pointer Control registers when DMA is enabled.

32.2.33 CFDFESTS : FIFO Empty Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXEMP[5:0]						RFXEMP[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	RFXEMP[7:0]	RX FIFO Empty Status 0: Corresponding FIFO not empty 1: Corresponding FIFO empty	R
13:8	CFXEMP[5:0]	Common FIFO Empty Status 0: Corresponding FIFO not empty 1: Corresponding FIFO empty	R
31:14	—	These bits are read as 0. The write value should be 0.	R

The FIFO Empty Status register shows status of the empty bits of the FIFO buffers.

RFXEMP[7:0] bits (RX FIFO Empty Status)

Bit 7 (RFXEMP[7]) is associated with FIFO index 7 and bit 0 (RFXEMP[0]) is associated with FIFO index 0.

The RFXEMP[7:0] bits are set when the CAN-FD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFXEMP[5:0] bits (Common FIFO Empty Status)

Bit 13 (CFXEMP[5]) is associated with common FIFO index 5 and bit 8 (CFXEMP[0]) is associated with common FIFO index 0.

The CFXEMP[5:0] bits are set when the CAN-FD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

32.2.34 CFDFFSTS : FIFO Full Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXFLL[5:0]						RFXFLL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

●如果配置为RX模式，则CommonFIFO缓冲区已启用且不为空

●如果配置为TX模式，则CommonFIFO缓冲区已启用且未满

●CommonFIFO缓冲区使能，GW模式下未配置。

启用DMA时不要写入通用FIFO指针控制寄存器。

32.2.33 CFDFESTS:FIFO空状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02A0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXEMP[5:0]						RFXEMP[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	RFXEMP[7:0]	RXFIFO空状态 0：对应的FIFO不为空1：对应的FIFO为空	R
13:8	CFXEMP[5:0]	常见FIFO空状态 0：对应的FIFO不为空1：对应的FIFO为空	R
31:14	—	这些位被读取为0。写入值应为0。	R

FIFOEmptyStatus寄存器显示FIFO缓冲区的空位状态。

RFXEMP[7:0]位（RXFIFO空状态）

位7(RFXEMP[7])与FIFO索引7相关联，位0(RFXEMP[0])与FIFO索引0相关联。

当CAN-FD模块处于GL_RESET模式时，RFXEMP[7:0]位被设置。

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

CFXEMP[5:0]位（通用FIFO空状态）

位13(CFXEMP[5])与通用FIFO索引5相关联，位8(CFXEMP[0])与通用FIFO索引0相关联。

CFXEMP[5:0]位在CAN-FD模块处于GL_RESET模式时置位。

当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

32.2.34 CFDFFSTS:FIFO满状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02A4

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXFLL[5:0]						RFXFLL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RFXFLL[7:0]	RX FIFO Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
13:8	CFXFLL[5:0]	Common FIFO Full Status 0: Corresponding FIFO not full 1: Corresponding FIFO full	R
31:14	—	These bits are read as 0. The write value should be 0.	R

The FIFO Full Status Register shows status of the full bits of the FIFO buffers.

RFXFLL[7:0] bits (RX FIFO Full Status)

The RFXFLL[7:0] bits are cleared when CAN-FD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFXFLL[5:0] bits (Common FIFO Full Status)

The CFXFLL[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

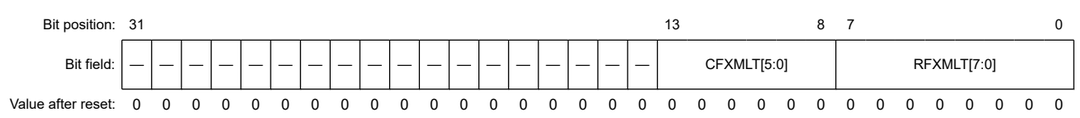
Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

32.2.35 CFDFMSTS : FIFO Message Lost Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02A8



Bit	Symbol	Function	R/W
7:0	RFXMLT[7:0]	RX FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
13:8	CFXMLT[5:0]	Common FIFO Message Lost Status 0: Corresponding FIFO Message Lost flag not set 1: Corresponding FIFO Message Lost flag set	R
31:14	—	These bits are read as 0. The write value should be 0.	R

The FIFO Message Lost Status Register shows status of the Msg Lost bits of the FIFO buffers.

RFXMLT[7:0] bits (RX FIFO Message Lost Status)

The RFXMLT[7:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

CFXMLT[5:0] bits (Common FIFO Message Lost Status)

The CFXMLT[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

Bit	Symbol	Function	R/W
7:0	RFXFLL[7:0]	RXFIFO满状态 0：对应FIFO未满1：对应FIFO已满	R
13:8	CFXFLL[5:0]	通用FIFO满状态 0：对应FIFO未满1：对应FIFO已满	R
31:14	—	这些位被读取为0。写入值应为0。	R

FIFO满状态寄存器显示FIFO缓冲器的满位状态。

RFXFLL[7:0]位（RXFIFO满状态）

当CAN-FD模块处于GL_RESET模式时，RFXFLL[7:0]位被清除。

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

CFXFLL[5:0]位（通用FIFO满状态）

当CAN-FD模块处于GL_RESET模式时，CFXFLL[5:0]位被清除。

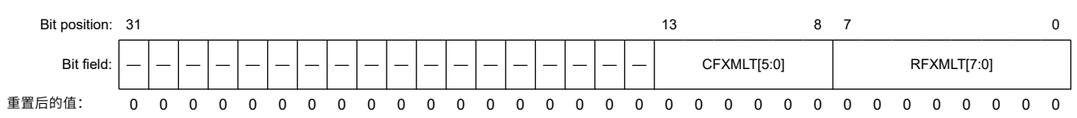
当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

32.2.35 CFDFMSTS:FIFO消息丢失状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02A8



Bit	Symbol	Function	R/W
7:0	RFXMLT[7:0]	RXFIFO消息丢失状态 0：未设置对应的FIFO报文丢失标志1：设置了对应的FIFO报文丢失标志	R
13:8	CFXMLT[5:0]	常见FIFO消息丢失状态 0：未设置对应的FIFO报文丢失标志1：设置了对应的FIFO报文丢失标志	R
31:14	—	这些位被读取为0。写入值应为0。	R

FIFO消息丢失状态寄存器显示FIFO缓冲区的MsgLost位的状态。

RFXMLT[7:0]位（RXFIFO消息丢失状态）

当CAN-FD模块处于GL_RESET模式时，RFXMLT[7:0]位被清除。

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

CFXMLT[5:0]位（通用FIFO消息丢失状态）

当CAN-FD模块处于GL_RESET模式时，CFXMLT[5:0]位被清除。

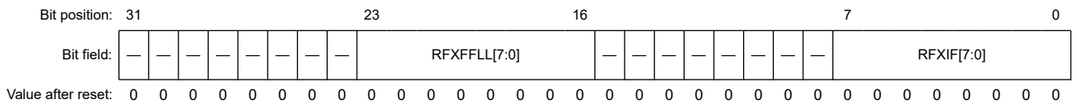
当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

32.2.36 CFDRFISTS : RX FIFO Interrupt Flag Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02AC



Bit	Symbol	Function	R/W
7:0	RFXIF[7:0]	RX FIFO[x] Interrupt Flag Status 0: Corresponding RX FIFO Interrupt flag not set 1: Corresponding RX FIFO Interrupt flag set	R
15:8	—	These bits are read as 0. The write value should be 0.	R/W
23:16	RFXFFLL[7:0]	RX FIFO[x] Interrupt Full Flag Status 0: Corresponding RX FIFO Interrupt Full flag not set 1: Corresponding RX FIFO Interrupt Full flag set	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The FIFO Interrupt Flag Status Register shows status of the interrupt flag bits of the RX FIFO buffers.

RFXIF[7:0] bits (RX FIFO[x] Interrupt Flag Status)

Each bit is set automatically when the corresponding interrupt flag bit is set in the RX FIFO Status Registers.

The RFXIF[7:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding interrupt flag bit is cleared in the RX FIFO Status Registers.

RFXFFLL[7:0] bits (RX FIFO[x] Interrupt Full Flag Status)

Each bit is set automatically when the corresponding interrupt full flag bit is set in the RX FIFO Status Registers.

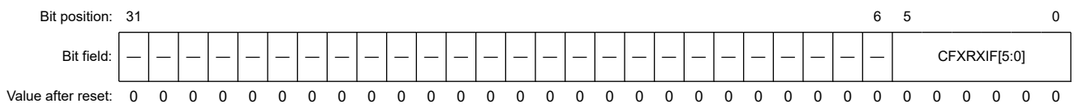
The RFXFFLL[7:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding interrupt full flag bit is cleared in the RX FIFO Status Registers.

32.2.37 CFDCFRISTS : Common FIFO RX Interrupt Flag Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02B0



Bit	Symbol	Function	R/W
5:0	CFXRXIF[5:0]	Common FIFO RX Interrupt Flag Status 0: Corresponding Common FIFO RX Interrupt flag is not set 1: Corresponding Common FIFO RX Interrupt flag is set	R
31:6	—	These bits are read as 0. The write value should be 0.	R/W

The Common FIFO RX Interrupt Flag Status Register shows status of the interrupt flag bits of the Common FIFO buffers.

CFXRXIF[5:0] bits (Common FIFO RX Interrupt Flag Status)

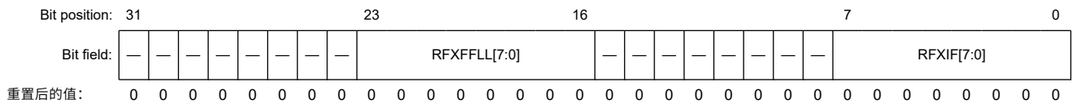
Each bit is set automatically when the corresponding RX interrupt flag bit is set in the Common FIFO Status Registers.

The CFXRXIF[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

32.2.36 CFDRFISTS:RXFIFO中断标志 状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02AC



Bit	Symbol	Function	R/W
7:0	RFXIF[7:0]	RXFIFO[x]中断标志 状态 0：未设置相应的RXFIFO中断标志 1：设置了相应的RXFIFO中断标志	R
15:8	—	这些位被读取为0。写入值应为0。	R/W
23:16	RFXFFLL[7:0]	RXFIFO[x]中断满标志状态 0：未设置对应的RXFIFO中断满标志1：设置了相应的RXFIFO中断满标志	R
31:24	—	这些位被读取为0。写入值应为0。	R/W

FIFO中断标志 状态寄存器显示RXFIFO缓冲区的中断标志位的状态。

RFXIF[7:0]位（RXFIFO[x]中断标志 状态）

当在RXFIFO状态寄存器中设置相应的中断标志位时，每个位都会自动设置。

当CAN-FD模块处于GL_RESET模式时，RFXIF[7:0]位被清除。

当RXFIFO状态寄存器中相应的中断标志位被清零时，每个位都会自动清零。

RFXFFLL[7:0]位（RXFIFO[x]中断满标志状态）

当在RXFIFO状态寄存器中设置相应的中断满标志位时，每个位都会自动设置。

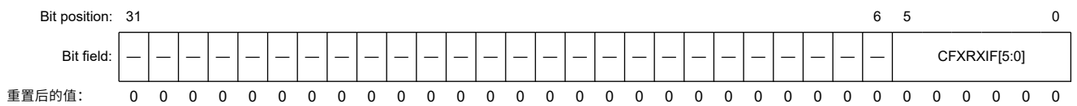
当CAN-FD模块处于GL_RESET模式时，RFXFFLL[7:0]位被清除。

当RXFIFO状态寄存器中相应的中断满标志位被清零时，每个位都会自动清零。

32.2.37 CFDCFRISTS：通用FIFORX中断标志 状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02B0



Bit	Symbol	Function	R/W
5:0	CFXRXIF[5:0]	通用FIFORX中断标志 状态 0：未设置对应的CommonFIFORX中断标志 1：设置了对应的CommonFIFORX中断标志	R
31:6	—	这些位被读取为0。写入值应为0。	R/W

公共FIFORX中断标志 状态寄存器显示公共FIFO缓冲区的中断标志位的状态。

CFXRXIF[5:0]位（通用FIFORX中断标志 状态）

当在通用FIFO状态寄存器中设置相应的RX中断标志 位时，每个位都会自动设置。

当CAN-FD模块处于GL_RESET模式时，CFXRXIF[5:0]位被清除。

Each bit is cleared automatically when the corresponding RX interrupt flag bit is cleared in the Common FIFO Status Registers.

32.2.38 CFDCFTISTS : Common FIFO TX Interrupt Flag Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02B4

Bit position:	31																								6	5		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXTXIF[5:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXTXIF[5:0]	Common FIFO [x] TX Interrupt Flag Status 0: Corresponding Common FIFO TX Interrupt flag is not set 1: Corresponding Common FIFO TX Interrupt flag is set	R
31:6	—	These bits are read as 0. The write value should be 0.	R/W

The Common FIFO TX Interrupt Flag Status Register shows status of the interrupt flag bits of the Common FIFO buffers.

CFXTXIF[5:0] bits (Common FIFO [x] TX Interrupt Flag Status)

Each bit is set automatically when the corresponding TX interrupt flag bit is set in the Common FIFO Status Registers.

The CFXTXIF[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding TX interrupt flag bit is cleared in the Common FIFO Status Registers.

32.2.39 CFDFFFSTS : FIFO FDC Full Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02C4

Bit position:	31																			13					8	7			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXFFLL[5:0]						RFXFFLL[7:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RFXFFLL[7:0]	RX FIFO FDC Level Full Status 0: Corresponding FIFO full interrupt not set 1: Corresponding FIFO full interrupt is set	R
13:8	CFXFFLL[5:0]	COMMON FIFO FDC Level Full Status 0: Corresponding FIFO full interrupt not set 1: Corresponding FIFO full interrupt is set	R
31:14	—	These bits are read as 0. The write value should be 0.	R

The FIFO FDC Full Status Register shows status of the full interrupt flag bits of the FIFO buffers.

RFXFFLL[7:0] bits (RX FIFO FDC Level Full Status)

Each bit is set automatically when the corresponding bit is set in the RX FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the RX FIFO Status Registers.

The RFXFFLL[7:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

CFXFFLL[5:0] bits (COMMON FIFO FDC Level Full Status)

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

当CommonFIFOStatus中相应的RX中断标志 位被清除时，每个位都会自动清除 Registers.

32.2.38 CFDCFTISTS：通用FIFOTX中断标志 状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02B4

Bit position:	31																								6	5		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXTXIF[5:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXTXIF[5:0]	通用FIFO[x]TX中断标志 状态 0：未设置相应的CommonFIFOTX中断标志 1：设置了相应的CommonFIFOTX中断标志	R
31:6	—	这些位被读取为0。写入值应为0。	R/W

公共FIFOTX中断标志 状态寄存器显示公共FIFO缓冲区的中断标志位的状态。

CFXTXIF[5:0]位（通用FIFO[x]TX中断标志 状态）

当在通用FIFO状态寄存器中设置相应的TX中断标志 位时，每个位都会自动设置。

当CAN-FD模块处于GL_RESET模式时，CFXTXIF[5:0]位被清除。

当CommonFIFOStatus中相应的TX中断标志 位清零时，每个位都会自动清零 Registers.

32.2.39 CFDFFFSTS:FIFOFDC满状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02C4

Bit position:	31																			13					8	7			0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXFFLL[5:0]						RFXFFLL[7:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	RFXFFLL[7:0]	RXFIFOFDC电平满状态 0：未设置相应的FIFO满中断1：设置了相应的FIFO满中断	R
13:8	CFXFFLL[5:0]	COMMONFIFOFDC级别满状态 0：未设置相应的FIFO满中断1：设置了相应的FIFO满中断	R
31:14	—	这些位被读取为0。写入值应为0。	R

FIFOFDC满状态寄存器显示FIFO缓冲器的满中断标志位的状态。

RFXFFLL[7:0]位（RXFIFOFDC电平满状态）

当在RXFIFO状态寄存器中设置相应位时，每个位都会自动设置。

当RXFIFO状态寄存器中的相应位清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，RFXFFLL[7:0]位被清除。

CFXFFLL[5:0]位（COMMONFIFOFDC电平满状态）

当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

The CFXFFLL[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

32.2.40 CFDCFMOWSTS : Common FIFO Message Over Write Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02C0

Bit position:	31																									5	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXMOW[5:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXMOW[5:0]	Common FIFO Massage Overwrite Status 0: Corresponding FIFO Overwrite flag is not set 1: Corresponding FIFO Overwrite flag is set	R
31:6	—	These bits are read as 0. The write value should be 0.	R

CFXMOW[5:0] bits (Common FIFO Massage Overwrite Status)

The CFXMOW[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode. This register is only valid in GW mode.

Each bit is set automatically when the corresponding bit is set in the Common FIFO Status Registers.

Each bit is cleared automatically when the corresponding bit is cleared in the Common FIFO Status Registers.

32.2.41 CFDCFOFRISTS : Common FIFO One Frame RX Interrupt Flag Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02B8

Bit position:	31																									5	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXOFRXIF[5:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXOFRXIF[5:0]	Common FIFO One Frame RX Interrupt Flag Status 0: Corresponding Common FIFO One Frame RX Interrupt flag is not set 1: Corresponding Common FIFO One Frame RX Interrupt flag is set	R
31:6	—	These bits are read as 0. The write value should be 0.	R

The Common FIFO One Frame RX Interrupt Flag Status register shows status of the interrupt flag bits of the Common FIFO buffers.

CFXOFRXIF[5:0] bits (Common FIFO One Frame RX Interrupt Flag Status)

Each bit is set automatically when the corresponding One Frame RX Interrupt flag bit is set in the Common FIFO Status Registers.

The CFXOFRXIF[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding One Frame RX Interrupt flag bit is cleared in the Common FIFO Status Registers.

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，CFXFFLL[5:0]位被清除。

32.2.40 CFDCFMOWSTS:通用FIFO消息覆盖写入状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02C0

Bit position:	31																									5	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXMOW[5:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXMOW[5:0]	通用FIFO按摩覆盖状态 0：不设置对应的FIFO覆盖标志1：设置对应的FIFO覆盖标志	R
31:6	—	这些位被读取为0。写入值应为0。	R

CFXMOW[5:0]位（通用FIFO消息覆盖状态）

当CAN-FD模块处于GL_RESET模式时，CFXMOW[5:0]位被清除。该寄存器仅在GW模式下有效。

当在通用FIFO状态寄存器中设置相应位时，每个位都会自动设置。

当公共FIFO状态寄存器中的相应位清零时，每个位都会自动清零。

32.2.41 CFDCFOFRISTS:通用FIFO一帧RX中断标志 状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02B8

Bit position:	31																									5	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXOFRXIF[5:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXOFRXIF[5:0]	通用FIFO一帧RX中断标志 状态 0：未设置对应的CommonFIFO一帧RX中断标志 1：设置了对应的CommonFIFO一帧RX中断标志	R
31:6	—	这些位被读取为0。写入值应为0。	R

通用FIFO一帧RX中断标志 状态寄存器显示通用中断标志位的状态

FIFO buffers.

CFXOFRXIF[5:0]位（通用FIFO一帧RX中断标志 状态）

当在通用FIFO状态中设置相应的一帧RX中断标志 位时，每个位都会自动设置

Registers.

当CAN-FD模块处于GL_RESET模式时，CFXOFRXIF[5:0]位被清除。

当CommonFIFO中相应的OneFrameRX中断标志 位清零时，每个位都会自动清零

状态寄存器。

32.2.42 CFDCFOFTISTS : Common FIFO One Frame TX Interrupt Flag Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x02BC

Bit position:	31																								5	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXOFTXIF[5:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXOFTXIF[5:0]	Common FIFO One Frame TX Interrupt Flag Status 0: Corresponding Common FIFO One Frame TX Interrupt flag is not set 1: Corresponding Common FIFO One Frame TX Interrupt flag is set	R
31:6	—	These bits are read as 0. The write value should be 0.	R

The Common FIFO One Frame TX Interrupt Flag Status Register shows status of the interrupt flag bits of the Common FIFO buffers.

CFXOFTXIF[5:0] bits (Common FIFO One Frame TX Interrupt Flag Status)

Each bit is set automatically when the corresponding One Frame TX Interrupt flag bit is set in the Common FIFO Status Registers.

The CFXOFTXIF[5:0] bits are cleared when the CAN-FD module is in GL_RESET mode.

Each bit is cleared automatically when the corresponding One Frame TX Interrupt flag bit is cleared in the Common FIFO Status Registers.

32.2.43 CFDCDTCT : DMA Transfer Control Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1330

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFDMAE1	CFDMAE0	RFDMAE7	RFDMAE6	RFDMAE5	RFDMAE4	RFDMAE3	RFDMAE2	RFDMAE1	RFDMAE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMAE0	DMA Transfer Enable for RXFIFO 0 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
1	RFDMAE1	DMA Transfer Enable for RXFIFO 1 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
2	RFDMAE2	DMA Transfer Enable for RXFIFO 2 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
3	RFDMAE3	DMA Transfer Enable for RXFIFO 3 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W

32.2.42 CFDCFOFTISTS：通用FIFO一帧TX中断标志 状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x02BC

Bit position:	31																								5	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFXOFTXIF[5:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CFXOFTXIF[5:0]	通用FIFO一帧TX中断标志 状态 0：未设置对应的CommonFIFO一帧TX中断标志 1：设置了对应的CommonFIFO一帧TX中断标志	R
31:6	—	这些位被读取为0。写入值应为0。	R

CommonFIFOOneFrameTX中断标志 状态寄存器显示Common的中断标志位的状态 FIFO buffers.

CFXOFTXIF[5:0]位（通用FIFO一帧TX中断标志 状态）

当在通用FIFO状态中设置相应的一帧TX中断标志 位时，每个位都会自动设置 Registers.

当CAN-FD模块处于GL_RESET模式时，CFXOFTXIF[5:0]位被清除。

当公共FIFO中相应的一帧TX中断标志 位被清除时，每个位都会自动清除 状态寄存器。

32.2.43 CFDDTCT:DMA传输控制寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1330

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFDMAE1	CFDMAE0	RFDMAE7	RFDMAE6	RFDMAE5	RFDMAE4	RFDMAE3	RFDMAE2	RFDMAE1	RFDMAE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMAE0	RXFIFO0的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
1	RFDMAE1	RXFIFO1的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
2	RFDMAE2	RXFIFO2的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
3	RFDMAE3	RXFIFO3的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W

Bit	Symbol	Function	R/W
4	RFDMAE4	DMA Transfer Enable for RXFIFO 4 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
5	RFDMAE5	DMA Transfer Enable for RXFIFO 5 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
6	RFDMAE6	DMA Transfer Enable for RXFIFO 6 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
7	RFDMAE7	DMA Transfer Enable for RXFIFO 7 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
8	CFDMAE0	DMA Transfer Enable for Common FIFO 0 of Channel 0 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
9	CFDMAE1	DMA Transfer Enable for Common FIFO 0 of Channel 1 0: DMA transfer request disabled 1: DMA transfer request enabled	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

The DMA Transfer Control Register controls the start and stop of DMA transfer operation.

RFDMAEn (n = 0 to 7) bit (DMA Transfer Enable for RXFIFOn)

The RFDMAEn bit cannot be set in GL_SLEEP or GL_RESET mode.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

CFDMAEn (n = 0, 1) bit (DMA Transfer Enable for Common FIFO 0 of Channel 0, 1)

The CFDMAEn bit enables or disables DMA transfer request for common FIFO 0 of channel 0 or 1. Only Common FIFO 0 can be linked to a DMA channel with this bit. Common FIFO 1 cannot be linked to a DMA channel.

To link Common FIFO 2, see bit CFDCDTTCT.CFDMAEn in section 32.2.45. CFDCDTTCT : DMA TX Transfer Control Register.

The CFDMAEn bit cannot be set in GL_SLEEP or GL_RESET mode.

Do not enable a DMA transfer for a Common FIFO that is configured as TX or GW FIFO.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

32.2.44 CFDCDTSTS : DMA Transfer Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1334

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFDMASTS1	CFDMASTS0	RFDMASTS7	RFDMASTS6	RFDMASTS5	RFDMASTS4	RFDMASTS3	RFDMASTS2	RFDMASTS1	RFDMASTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4	RFDMAE4	RXFIFO4的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
5	RFDMAE5	RXFIFO5的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
6	RFDMAE6	RXFIFO6的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
7	RFDMAE7	RXFIFO7的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
8	CFDMAE0	通道0的公共FIFO0的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
9	CFDMAE1	通道1的公共FIFO0的DMA传输使能 0：禁用DMA传输请求1：启用DMA传输请求	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

DMA传输控制寄存器控制DMA传输操作的开始和停止。

RFDMAEn（n=0到7）位（RXFIFOn的DMA传输使能）

RFDMAEn位不能在GL_SLEEP或GL_RESET模式下设置。

当CAN-FD模块处于GL_RESET模式时，该位清零。

CFDMAEn(n=0 1)位（通道0 1的公共FIFO0的DMA传输使能）

CFDMAEn位启用或禁用通道0或1的公共FIFO0的DMA传输请求。只有公共FIFO0可以通过该位链接到DMA通道。通用FIFO1不能链接到DMA通道。

要链接CommonFIFO2，请参见第32.2.45节中的位CFDCDTTCT.CFDMAEn。CFDCDTTCT:DMATX传输控制Register.

CFDMAEn位不能在GL_SLEEP或GL_RESET模式下设置。

不要为配置为TX或GWFIFO的CommonFIFO启用DMA传输。

当CAN-FD模块处于GL_RESET模式时，该位清零。

32.2.44 CFDCDTSTS:DMA传输状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1334

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFDMASTS1	CFDMASTS0	RFDMASTS7	RFDMASTS6	RFDMASTS5	RFDMASTS4	RFDMASTS3	RFDMASTS2	RFDMASTS1	RFDMASTS0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFDMASTS0	DMA Transfer Status for RX FIFO 0 0: DMA transfer stopped 1: DMA transfer on going	R
1	RFDMASTS1	DMA Transfer Status for RX FIFO 1 0: DMA transfer stopped 1: DMA transfer on going	R
2	RFDMASTS2	DMA Transfer Status for RX FIFO 2 0: DMA transfer stopped 1: DMA transfer on going	R
3	RFDMASTS3	DMA Transfer Status for RX FIFO 3 0: DMA transfer stopped 1: DMA transfer on going	R
4	RFDMASTS4	DMA Transfer Status for RX FIFO 4 0: DMA transfer stopped 1: DMA transfer on going	R
5	RFDMASTS5	DMA Transfer Status for RX FIFO 5 0: DMA transfer stopped 1: DMA transfer on going	R
6	RFDMASTS6	DMA Transfer Status for RX FIFO 6 0: DMA transfer stopped 1: DMA transfer on going	R
7	RFDMASTS7	DMA Transfer Status for RX FIFO 7 0: DMA transfer stopped 1: DMA transfer on going	R
8	CFDMASTS0	DMA Transfer Status only for Common FIFO 0 of Channel 0 0: DMA transfer stopped 1: DMA transfer on going	R
9	CFDMASTS1	DMA Transfer Status only for Common FIFO 0 of Channel 1 0: DMA transfer stopped 1: DMA transfer on going	R
31:10	—	These bits are read as 0.	R

The DMA Transfer Status Register shows the status of the DMA transfer.

RFDMASTSn (n = 0 to 7) bit (DMA Transfer Status for RX FIFO n)

Each bit is set automatically when the corresponding DMA enable bit is set and the corresponding DMA FIFO is not empty.

Each bit is cleared automatically when the DMA transfer stops either because the DMA is disabled or the DMA FIFO is empty.

When CFDCDTCT.RFDMAEn (see CFDCDTCT.RFDMAEn bit in section 32.2.43. CFDCDTCT : DMA Transfer Control Register) is set to 0 while DMA transfer for the corresponding FIFO is on going, the RFDMASTSn bit becomes 0 when the DMA transfer is complete.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

CFDMASTSn bit (DMA Transfer Status only for Common FIFO 0 of Channel 0, 1)

Each bit is set automatically when the corresponding DMA enable bit is set and the corresponding DMA FIFO is not empty.

Each bit is cleared automatically when the DMA transfer stops either because the DMA is disabled or the DMA FIFO is empty.

When CFDCDTCT.CFDMAEn (see CFDCDTCT.CFDMAEn bit in section 32.2.43. CFDCDTCT : DMA Transfer Control Register) is set to 0 while DMA transfer for the corresponding FIFO is on going, the CFDMASTSn bit becomes 0 when the DMA transfer is complete.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit	Symbol	Function	R/W
0	RFDMASTS0	RXFIFO0的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
1	RFDMASTS1	RXFIFO1的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
2	RFDMASTS2	RXFIFO2的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
3	RFDMASTS3	RXFIFO3的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
4	RFDMASTS4	RXFIFO4的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
5	RFDMASTS5	RXFIFO5的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
6	RFDMASTS6	RXFIFO6的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
7	RFDMASTS7	RXFIFO7的DMA传输状态 0：DMA传输停止1：DMA传输正在进行	R
8	CFDMASTS0	DMA传输状态仅适用于通道0的CommonFIFO0 0：DMA传输停止1：DMA传输正在进行	R
9	CFDMASTS1	DMA传输状态仅适用于通道1的CommonFIFO0 0：DMA传输停止1：DMA传输正在进行	R
31:10	—	这些位读为0。	R

DMA传输状态寄存器显示DMA传输的状态。

RFDMASTSn(n=0to7)位（RXFIFOn的DMA传输状态）

当设置相应的DMA使能位且相应的DMAFIFO不为空时，每个位都会自动设置。

当DMA传输停止时，每个位都会自动清除，因为DMA被禁用或DMAFIFO为空。

当CFDCDTCT.RFDMAEn（参见第32.2.43节中的CFDCDTCT.RFDMAEn位。CFDCDTCT：DMA传输控制寄存器）设置为0，同时相应FIFO的DMA传输正在进行时，RFDMASTSn位变为0。
DMA传输完成。

当CAN-FD模块处于GL_RESET模式时，该位清零。

CFDMASTSn位（DMA传输状态仅适用于通道0、1的CommonFIFO0）

当设置相应的DMA使能位且相应的DMAFIFO不为空时，每个位都会自动设置。

当DMA传输停止时，每个位都会自动清除，因为DMA被禁用或DMAFIFO为空。

当CFDCDTCT.CFDMAEn（参见第32.2.43节中的CFDCDTCT.CFDMAEn位。CFDCDTCT：DMA传输控制寄存器）设置为0，同时相应FIFO的DMA传输正在进行时，CFDMASTSn位变为0。
DMA传输完成。

当CAN-FD模块处于GL_RESET模式时，该位清零。

32.2.45 CFDCDTTCT : DMA TX Transfer Control Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1340

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDMAE1	CFDMAE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TQ3DMAE1	TQ3DMAE0	—	—	—	—	—	—	TQ0DMAE1	TQ0DMAE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TQ0DMAE0	DMA TX Transfer Enable for TXQ 0 of Channel 0 0: DMA TX transfer request disabled 1: DMA TX transfer request enabled	R/W
1	TQ0DMAE1	DMA TX Transfer Enable for TXQ 0 of Channel 1 0: DMA TX transfer request disabled 1: DMA TX transfer request enabled	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	TQ3DMAE0	DMA TX Transfer Enable for TXQ 3 of Channel 0 0: DMA TX transfer request disabled 1: DMA TX transfer request enabled	R/W
9	TQ3DMAE1	DMA TX Transfer Enable for TXQ 3 of Channel 1 0: DMA TX transfer request disabled 1: DMA TX transfer request enabled	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
16	CFDMAE0	DMA TX Transfer Enable for Common FIFO 2 of Channel 0 0: DMA TX transfer request disabled 1: DMA TX transfer request enabled	R/W
17	CFDMAE1	DMA TX Transfer Enable for Common FIFO 2 of Channel 1 0: DMA TX transfer request disabled 1: DMA TX transfer request enabled	R/W
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The DMA TX Transfer Control Register controls the start and stop of DMA transfer operation.

TQ0DMAEn (n = 0, 1) bit (DMA TX Transfer Enable for TXQ 0 of Channel n)

The TQ0DMAEn bit cannot be set in GL_SLEEP or GL_RESET mode.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

TQ3DMAEn (n = 0, 1) bit (DMA TX Transfer Enable for TXQ 3 of Channel n)

The TQ3DMAEn bit cannot be set in GL_SLEEP or GL_RESET mode.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

CFDMAEn (n = 0, 1) bit (DMA TX Transfer Enable for Common FIFO 2 of Channel n)

The CFDMAEn bit cannot be set in GL_SLEEP or GL_RESET mode.

Only common FIFO 2 can be linked to a DMA channel with this bit. Common FIFO 1 cannot be linked to a DMA channel.

To link Common FIFO 0, see CFDCDTCT.CFDMAEn bit in section 32.2.43. CFDCDTCT : DMA Transfer Control Register.

Do not enable a DMA transfer for a Common FIFO that is configured as RX or GW FIFO.

32.2.45 CFDCDTTCT:DMATX传输控制寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1340

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDMAE1	CFDMAE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TQ3DMAE1	TQ3DMAE0	—	—	—	—	—	—	TQ0DMAE1	TQ0DMAE0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TQ0DMAE0	通道0的TXQ0的DMATX传输使能 0：禁用DMATX传输请求1：启用DMATX传输请求	R/W
1	TQ0DMAE1	通道1的TXQ0的DMATX传输使能 0：禁用DMATX传输请求1：启用DMATX传输请求	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	TQ3DMAE0	通道0的TXQ3的DMATX传输使能 0：禁用DMATX传输请求1：启用DMATX传输请求	R/W
9	TQ3DMAE1	通道1的TXQ3的DMATX传输使能 0：禁用DMATX传输请求1：启用DMATX传输请求	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
16	CFDMAE0	通道0的通用FIFO2的DMATX传输使能 0：禁用DMATX传输请求1：启用DMATX传输请求	R/W
17	CFDMAE1	通道1的通用FIFO2的DMATX传输使能 0：禁用DMATX传输请求1：启用DMATX传输请求	R/W
31:18	—	这些位被读取为0。写入值应为0。	R/W

DMATX传输控制寄存器控制DMA传输操作的开始和停止。

TQ0DMAEn(n=0 1)位（通道n的TXQ0的DMATX传输使能）

TQ0DMAEn位不能在GL_SLEEP或GL_RESET模式下设置。

当CAN-FD模块处于GL_RESET模式时，该位清零。

TQ3DMAEn(n=0 1)位（通道n的TXQ3的DMATX传输使能）

TQ3DMAEn位不能在GL_SLEEP或GL_RESET模式下设置。

当CAN-FD模块处于GL_RESET模式时，该位清零。

CFDMAEn(n=0 1)位（通道n的公共FIFO2的DMATX传输使能）

CFDMAEn位不能在GL_SLEEP或GL_RESET模式下设置。

只有通用FIFO2可以通过该位链接到DMA通道。通用FIFO1不能链接到DMA通道。

要链接CommonFIFO0，请参见第32.2.43节中的CFDCDTCT.CFDMAEn位。CFDCDTCT:DMA传输控制Register.

不要为配置为RX或GWFIFO的CommonFIFO启用DMA传输。

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The CFDMAEn bit is cleared when the CAN-FD module is in GL_RESET mode.

32.2.46 CFDCDTTSTS : DMA TX Transfer Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1344

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDMASTS1	CFDMASTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TQ3DMASTS1	TQ3DMASTS0	—	—	—	—	—	—	TQ0DMASTS1	TQ0DMASTS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TQ0DMASTS0	DMA TX Transfer Status for TXQ0 of Channel 0 0: DMA transfer stopped 1: DMA transfer enabled	R
1	TQ0DMASTS1	DMA TX Transfer Status for TXQ0 of Channel 1 0: DMA transfer stopped 1: DMA transfer enabled	R
7:2	—	These bits are read as 0. The write value should be 0.	R
8	TQ3DMASTS0	DMA TX Transfer Status for TXQ3 of Channel 0 0: DMA transfer stopped 1: DMA transfer enabled	R
9	TQ3DMASTS1	DMA TX Transfer Status for TXQ3 of Channel 1 0: DMA transfer stopped 1: DMA transfer enabled	R
15:10	—	These bits are read as 0. The write value should be 0.	R
16	CFDMASTS0	DMA TX Transfer Status only for Common FIFO 2 of Channel 0 0: DMA transfer stopped 1: DMA transfer enabled	R
17	CFDMASTS1	DMA TX Transfer Status only for Common FIFO 2 of Channel 1 0: DMA transfer stopped 1: DMA transfer enabled	R
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The DMA TX Transfer Status Register shows the status of the DMA transfer.

TQ0DMASTSn (n = 0, 1) bit (DMA TX Transfer Status for TXQ 0 of Channel n)

The TQ0DMASTSn bit is set when the CFDCDTTCT.TQ0DMAEn bit in the corresponding CFDCDTTCT register is set (see section 32.2.45. CFDCDTTCT : DMA TX Transfer Control Register).

This bit is cleared when:

- The CFDCDTTCT.TQ0DMAEn bit in the corresponding CFDCDTTCT register is cleared
- The CAN-FD module is in GL_RESET mode.

TQ3DMASTSn (n = 0, 1) bit (DMA TX Transfer Status for TXQ 3 of Channel n)

The TQ3DMASTSn bit is set when the CFDCDTTCT.TQ3DMAEn bit in the corresponding CFDCDTTCT register is set (see section 32.2.45. CFDCDTTCT : DMA TX Transfer Control Register).

This bit is cleared when:

- The CFDCDTTCT.TQ3DMAEn bit in the corresponding CFDCDTTCT register is cleared

当CAN-FD模块处于GL_RESET模式时，CFDMAEn位被清除。

32.2.46 CFDDTTSTS:DMATX传输状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1344

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDMASTS1	CFDMASTS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TQ3DMASTS1	TQ3DMASTS0	—	—	—	—	—	—	TQ0DMASTS1	TQ0DMASTS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TQ0DMASTS0	通道0的TXQ0的DMATX传输状态 0：DMA传输停止1：DMA传输启用	R
1	TQ0DMASTS1	通道1的TXQ0的DMATX传输状态 0：DMA传输停止1：DMA传输启用	R
7:2	—	这些位被读取为0。写入值应为0。	R
8	TQ3DMASTS0	通道0的TXQ3的DMATX传输状态 0：DMA传输停止1：DMA传输启用	R
9	TQ3DMASTS1	通道1的TXQ3的DMATX传输状态 0：DMA传输停止1：DMA传输启用	R
15:10	—	这些位被读取为0。写入值应为0。	R
16	CFDMASTS0	DMATX传输状态仅适用于通道0的CommonFIFO2 0：DMA传输停止1：DMA传输启用	R
17	CFDMASTS1	DMATX传输状态仅适用于通道1的CommonFIFO2 0：DMA传输停止1：DMA传输启用	R
31:18	—	这些位被读取为0。写入值应为0。	R/W

DMATX传输状态寄存器显示DMA传输的状态。

TQ0DMASTSn(n=0 1)位（通道n的TXQ0的DMATX传输状态）

当相应CFDCDTTCT寄存器中的CFDCDTTCT.TQ0DMAEn位置位时，TQ0DMASTSn位置位（参见第32.2.45节。CFDCDTTCT：DMATX传输控制寄存器）。

该位在以下情况下清零：

●对应CFDCDTTCT寄存器中的CFDCDTTCT.TQ0DMAEn位清零

●CAN-FD模块处于GL_RESET模式。

TQ3DMASTSn(n=0 1)位（通道n的TXQ3的DMATX传输状态）

当相应CFDCDTTCT寄存器中的CFDCDTTCT.TQ3DMAEn位置位时，TQ3DMASTSn位置位（参见第32.2.45节。CFDCDTTCT：DMATX传输控制寄存器）。

该位在以下情况下清零：

●相应CFDCDTTCT寄存器中的CFDCDTTCT.TQ3DMAEn位清零

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- The CAN-FD module is in GL_RESET mode.

CFDMASTSn (n = 0, 1) bit (DMA TX Transfer Status only for Common FIFO 2 of Channel n)

The CFDMASTSn bit is set when the CFDCDTTCT.CFDMAEn bit in the corresponding CFDCDTTCT register is set (see section 32.2.45. CFDCDTTCT : DMA TX Transfer Control Register).

This bit is cleared when:

- The CFDCDTTCT.CFDMAEn bit in the corresponding CFDCDTTCT register is cleared
- The CAN-FD module is in GL_RESET mode.

32.2.47 CFDGRINTSTSn : Global RX Interrupt Status Register n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1350 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CFOFRIF[30:28]			—	CFRFIF[26:24]			—	—	—	—	—	CFRIF[18:16]			—	—	—	—	—	QOFRIF[10:8]			—	—	—	—	—	QFIF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	QFIF[2:0]	TXQ Full Interrupt Flag Channel n (n = 0, 1) 0: Corresponding TXQ Full Interrupt flag is not set 1: Corresponding TXQ Full Interrupt flag is set	R
7:3	—	These bits are read as 0. The write value should be 0.	R/W
10:8	QOFRIF[10:8]	TXQ One Frame RX Interrupt Flag Channel n (n = 0, 1) 0: Corresponding TXQ One Frame RX Interrupt flag is not set 1: Corresponding TXQ One Frame RX Interrupt flag is set	R
15:11	—	These bits are read as 0. The write value should be 0.	R/W
18:16	CFRIF[18:16]	Common FIFO RX Interrupt Flag Channel n (n = 0, 1) 0: Corresponding Common FIFO RX Interrupt flag is not set 1: Corresponding Common FIFO RX Interrupt flag is set	R
23:19	—	These bits are read as 0. The write value should be 0.	R/W
26:24	CFRFIF[26:24]	Common FIFO FDC Level Full Interrupt Flag Channel n (n = 0, 1) 0: Corresponding Common FIFO Full Interrupt flag is not set 1: Corresponding Common FIFO Full Interrupt flag is set	R
27	—	This bit is read as 0. The write value should be 0.	R/W
30:28	CFOFRIF[30:28]	Common FIFO One Frame RX Interrupt Flag Channel n (n = 0, 1) 0: Corresponding Common FIFO One Frame RX Interrupt flag is not set 1: Corresponding Common FIFO One Frame RX Interrupt flag is set	R
31	—	This bit is read as 0. The write value should be 0.	R/W

QFIF[2:0] bits (TXQ Full Interrupt Flag Channel n (n = 0, 1))

The QFIF[2:0] bits are set automatically when the TXQ Full Interrupt flag of the related channel is set when the interrupt is enabled.

The QFIF[2:0] bits are cleared automatically when:

- The related TXQ result status bits are cleared or the interrupt enable is disabled
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

QOFRIF[10:8] bits (TXQ One Frame RX Interrupt Flag Channel n (n = 0, 1))

The QOFRIF[10:8] bits are set automatically when the TXQ One Frame RX Interrupt flag of the related channel is set when the interrupt is enabled.

●CAN-FD模块处于GL_RESET模式。

CFDMASTSn(n=0 1)位（DMATX传输状态仅适用于通道n的CommonFIFO2）

当相应的CFDCDTTCT寄存器中的CFDCDTTCT.CFDMAEn位置位时，CFDMASTSn位置位（参见第32.2.45节。CFDCDTCT：DMATX传输控制寄存器）。

该位在以下情况下清零：

●相应CFDCDTCT寄存器中的CFDCDTTCT.CFDMAEn位清零

●CAN-FD模块处于GL_RESET模式。

32.2.47 CFDGRINTSTSn:全局RX中断状态寄存器n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1350 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CFOFRIF[30:28]			—	CFRFIF[26:24]			—	—	—	—	—	CFRIF[18:16]			—	—	—	—	—	QOFRIF[10:8]			—	—	—	—	—	QFIF[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	QFIF[2:0]	TXQ全中断标志通道n(n=0 1) 0：未设置相应的TXQ完全中断标志1：设置了相应的TXQ完全中断标志	R
7:3	—	这些位被读取为0。写入值应为0。	R/W
10:8	QOFRIF[10:8]	TXQ一帧RX中断标志 通道n(n=0 1) 0：对应的TXQ一帧RX中断标志 未置位1：对应的TXQ一帧RX中断标志 置位	R
15:11	—	这些位被读取为0。写入值应为0。	R/W
18:16	CFRIF[18:16]	公共FIFORX中断标志 通道n(n=0 1) 0：未设置对应的CommonFIFORX中断标志 1：设置了对应的CommonFIFORX中断标志	R
23:19	—	这些位被读取为0。写入值应为0。	R/W
26:24	CFRFIF[26:24]	通用FIFOFDC电平满中断标志通道n(n=0 1) 0：未设置相应的通用FIFO满中断标志1：设置了相应的通用FIFO满中断标志	R
27	—	该位读取为0。写入值应为0。	R/W
30:28	CFOFRIF[30:28]	通用FIFO一帧RX中断标志 通道n(n=0 1) 0：未设置对应的CommonFIFO一帧RX中断标志 1：设置了对应的CommonFIFO一帧RX中断标志	R
31	—	该位读取为0。写入值应为0。	R/W

QFIF[2:0]位（TXQ全中断标志通道n(n=0 1)）

QFIF[2:0]位会在相关通道的TXQ完全中断标志位在中断使能时自动置位。

QFIF[2:0]位在以下情况下自动清零：

●相关的TXQ结果状态位被清除或中断使能被禁止

●CAN-FD模块处于GL_RESET模式

●相关的CAN-FD通道处于CH_RESET模式。

QOFRIF[10:8]位（TXQ一帧RX中断标志 通道n(n=0 1)）

QOFRIF[10:8]位在相关通道的TXQ单帧接收中断标志位在中断使能时自动置位。

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The QOFRIF[10:8] bits are cleared automatically when:

- The related TXQ result status bits are cleared or the interrupt enable is disabled
- The CAN-FD module is in GL_RESET or CH_RESET mode.

CFRIF[18:16] bits (Common FIFO RX Interrupt Flag Channel n (n = 0, 1))

The CFRIF[18:16] bits are set automatically when the Common FIFO RX Interrupt flag of the related channel is set when the interrupt is enabled.

The CFRIF[18:16] bits are cleared automatically when:

- The related Common FIFO RX result status bits are cleared or the interrupt enable is disabled
- The CAN-FD module is in GL_RESET or CH_RESET mode.

CFRFIF[26:24] bits (Common FIFO FDC Level Full Interrupt Flag Channel n (n = 0, 1))

The CFRFIF[26:24] bits are set automatically when the Common FIFO Full Interrupt flag of the related channel is set when the interrupt is enabled.

The CFRFIF[26:24] bits are cleared automatically when:

- The related Common FIFO RX result status bits are cleared or the interrupt enable is disabled
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

CFOFRIF[30:28] bits (Common FIFO One Frame RX Interrupt Flag Channel n (n = 0, 1))

The CFOFRIF[30:28] bits are set automatically when the Common FIFO One Frame RX Interrupt flag of the related channel is set when the interrupt is enabled.

The CFOFRIF[30:28] bits are cleared automatically when:

- The related Common FIFO RX result status bits are cleared or the interrupt enable is disabled
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

32.2.48 CFDTMCn : TX Message Buffer Control Registers n (n = 0 to 7, 32 to 39, 64 to 71, 96 to 103)

Base address: CANFD = 0x400B_0000

Offset address: 0x02D0 + 0x01 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TMOM	TMTAR	TMTR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTR	TX Message Buffer Transmission Request 0: TX Message buffer transmission not requested 1: TX message buffer transmission requested	R/W
1	TMTAR	TX Message Buffer Transmission Abort Request 0: TX message buffer transmission request abort not requested 1: TX message buffer transmission request abort requested	R/W
2	TMOM	TX Message Buffer One-shot Mode 0: TX message buffer not configured in one-shot mode 1: TX message buffer configured in one-shot mode	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

The TX Message Buffer Control Registers configure the TX message buffer functions.

QOFRIF[10:8]位在以下情况下自动清零：

●相关的TXQ结果状态位被清除或中断使能被禁止

●CAN-FD模块处于GL_RESET或CH_RESET模式。

CFRIF[18:16]位（通用FIFORX中断标志 通道n(n=0 1)）

CFRIF[18:16]位会在相关通道的通用FIFORX中断标志 位在中断使能时自动置位。

CFRIF[18:16]位在以下情况下自动清零：

●相关的CommonFIFORX结果状态位被清除或中断使能被禁用

●CAN-FD模块处于GL_RESET或CH_RESET模式。

CFRFIF[26:24]位（通用FIFOFDC电平满中断标志通道n(n=0 1)）

CFRFIF[26:24]位会在相关通道的通用FIFO满中断标志位在中断使能时自动置位。

CFRFIF[26:24]位在以下情况下自动清除：

●相关的CommonFIFORX结果状态位被清除或中断使能被禁用

●CAN-FD模块处于GL_RESET模式

●相关的CAN-FD通道处于CH_RESET模式。

CFOFRIF[30:28]位（通用FIFO一帧RX中断标志 通道n(n=0 1)）

CFOFRIF[30:28]位会在相关通道的通用FIFO一帧RX中断标志 位在中断使能时自动置位。

CFOFRIF[30:28]位在以下情况下自动清零：

●相关的CommonFIFORX结果状态位被清除或中断使能被禁用

●CAN-FD模块处于GL_RESET模式

●相关的CAN-FD通道处于CH_RESET模式。

32.2.48 CFDTMCn：TX消息缓冲区控制寄存器n（n=0到7、32到39、64到71、96到103）

Base address: CANFD = 0x400B_0000

Offset address: 0x02D0 + 0x01 × i

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	TMOM	TMTAR	TMTR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTR	TX消息缓冲区传输请求 0：未请求TX报文缓冲区传输1：已请求TX报文缓冲区传输	R/W
1	TMTAR	TX消息缓冲区传输中止请求 0：未请求TX报文缓冲区传输请求中止1：已请求TX报文缓冲区传输请求中止	R/W
2	TMOM	TX消息缓冲区一次性模式 0：TX报文缓冲区未配置为one-shot模式1：TX报文缓冲区配置为one-shot模式	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

TX报文缓冲区控制寄存器配置TX报文缓冲区功能。

TMTR bit (TX Message Buffer Transmission Request)

When the TMTR bit is set, the CAN-FD module logic tries to transmit the message stored in the corresponding message buffer.

Only write to this bit when the related CAN-FD module is in CH_HALT or CH_OPERATION mode.

Do not set this bit if the corresponding TX message buffer is linked to a COM FIFO in TX or GW mode or is a part of TX Queue.

This bit cannot be directly cleared by a CPU write access.

This bit can only be set when the Transmission Result flag bits (CFDTMSTSn.TMTRF) in the CFDTMSTSn register corresponding to the message buffer are cleared to 00b.

The TMTR bit is automatically cleared by the:

- CAN-FD module logic at the end of a successful transmission
- CAN-FD module logic at the end of a transmission abort, requested by the corresponding CFDTMCn.TMTAR bit
- CAN-FD module logic when there is a detection of a CAN bus error or arbitration loss if CFDTMCn.TMOM bit is set for the message buffer
- CAN-FD module logic when the CAN-FD module is in GL_RESET mode or the related channel is in CH_RESET mode.

TMTAR bit (TX Message Buffer Transmission Abort Request)

When the TMTAR bit is set, the CAN-FD module logic tries to abort the transmission of the frame stored in the corresponding message buffer.

In most cases, transmission cannot be aborted if the internal scan for transmission is complete and the message buffer has already been selected for transmission. In this case, frame may be transmitted successfully from the message buffer. The message buffer selection is released by entering CH_HALT mode.

However, message buffer selected for transmission can be aborted by an abort request when the CAN node detects a new message on the bus (RX pin) before it starts transmission from the selected message buffer.

Only write to the TMTAR bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode. This bit can only be set when the related transmit request TMTR bit is set.

The TMTAR bit cannot be cleared by a CPU write access. Clearing of this bit by CAN-FD has priority over setting by a CPU write access.

The TMTAR bit is automatically cleared by:

- The CAN-FD module logic at the end of a successful transmission
- The CAN-FD module logic at the end of a transmission abort
- The CAN-FD module logic when there is detection of a CAN bus error or arbitration loss
- The CAN-FD module logic when the CAN-FD module is in GL_RESET mode or the related channel enters CH_RESET mode.

TMOM bit (TX Message Buffer One-shot Mode)

When the TMOM bit is set, the CAN-FD module logic tries to transmit the message only once.

If the transmission is successful, the CFDTMSTSn.TMTRF bits are set to 10b or 11b. Otherwise, the transmission is automatically aborted and CFDTMSTSn.TMTRF bits are set to 01b due to a bus error or a bus arbitration lost.

The TMOM bit remains set if the transmission has completed successfully or aborted due to an error or a loss of arbitration.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

Set this bit at the same time as the TMTR bit. Clear this bit with a write access.

If a message has already been requested for transmission, do not write to this bit until the message has been successfully transmitted or transmission has been aborted.

The TMOM bit is automatically cleared by the CAN-FD module logic when the CAN-FD module is in GL_RESET mode or the related channel is in CH_RESET mode.

TMTR位（TX报文缓冲区传输请求）

当设置TMTR位时，CAN-FD模块逻辑尝试发送存储在相应消息缓冲区中的消息。

仅当相关CAN-FD模块处于CH_HALT或CH_OPERATION模式时写入该位。

如果相应的TX消息缓冲区在TX或GW模式下链接到COMFIFO或者是TX的一部分，则不要设置该位
Queue.

该位不能通过CPU写访问直接清除。

只有当报文缓冲区对应的CFDTMSTSn寄存器中的传输结果标志位(CFDTMSTSn.TMTRF)被清零时，才能设置该位。

TMTR位通过以下方式自动清零：

●成功传输结束时的CAN-FD模块逻辑

●发送中止结束时的CAN-FD模块逻辑，由相应的CFDTMCn.TMTAR位请求

●如果CFDTMCn.TMOM位为消息缓冲区设置，则检测到CAN总线错误或仲裁丢失时的CAN-FD模块逻辑

●CAN-FD模块处于GL_RESET模式或相关通道处于CH_RESET模式时的CAN-FD模块逻辑。

TMTAR位（TX报文缓冲区传输中止请求）

当设置TMTAR位时，CAN-FD模块逻辑尝试中止存储在相应消息缓冲区中的帧的传输。

在大多数情况下，如果内部扫描传输完成并且消息缓冲区已被选择用于传输，则无法中止传输。在这种情况下，可以从消息缓冲区成功传输帧。通过进入CH_HALT模式释放消息缓冲区选择。

但是，当CAN节点在从选定的消息缓冲区开始传输之前检测到总线（RX引脚）上的新消息时，可以通过中止请求中止选择用于传输的消息缓冲区。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入TMTAR位。只有当相关的发送请求TMTR位被置位时，该位才能被置位。

CPU写访问不能清除TMTAR位。CAN-FD清零该位优先于设置
CPU写访问。

TMTAR位通过以下方式自动清零：

●成功传输结束时的CAN-FD模块逻辑

●传输中止结束时的CAN-FD模块逻辑

●检测到CAN总线错误或仲裁丢失时的CAN-FD模块逻辑

●CAN-FD模块处于GL_RESET模式或相关通道进入CH_RESET模式时的CAN-FD模块逻辑。

TMOM位（TX消息缓冲区一次性模式）

当TMOM位置位时，CAN-FD模块逻辑尝试仅发送一次消息。

如果传输成功，CFDTMSTSn.TMTRF位设置为10b或11b。否则，由于总线错误或总线仲裁丢失，传输将自动中止并且CFDTMSTSn.TMTRF位设置为01b。

如果传输成功完成或由于错误或仲裁丢失而中止，则TMOM位保持设置。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。

该位与TMTR位同时置位。通过写访问清除该位。

如果已请求发送消息，则在消息成功发送或发送中止之前不要写入该位。

当CAN-FD模块处于GL_RESET模式或相关通道处于CH_RESET模式时，TMOM位由CAN-FD模块逻辑自动清零。

32.2.49 CFDTMSTSn : TX Message Buffer Status Registers n (n = 0 to 7, 32 to 39, 64 to 71, 96 to 103)

Base address: CANFD = 0x400B_0000

Offset address: 0x07D0 + 0x01 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTSTS	TX Message Buffer Transmission Status 0: No on-going transmission 1: On-going transmission	R
2:1	TMTRF[1:0]	TX Message Buffer Transmission Result Flag 0 0: No result 0 1: Transmission aborted from the TX message buffer 1 0: Transmission successful from the TX message buffer and transmission abort was not requested 1 1: Transmission successful from the TX message buffer and transmission abort was requested	R/W
3	TMTRM	TX Message Buffer Transmission Request Mirrored 0: TX message buffer transmission not requested 1: TX message buffer transmission requested	R
4	TMTARM	TX Message Buffer Transmission Abort Request Mirrored 0: TX message buffer transmission request abort not requested 1: TX message buffer transmission request abort requested	R
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The TX Message Buffer Status Registers show status of the transmission and transmission abort for the corresponding message buffers.

TMTSTS bit (TX Message Buffer Transmission Status)

The TMTSTS bit is set automatically at the start of the transmission from the corresponding TX message buffer.

This bit is cleared automatically when:

- Transmission stops
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

TMTRF[1:0] bits (TX Message Buffer Transmission Result Flag)

The TMTRF[1:0] bits show the result for the corresponding TX message buffer. The status is as follows:

- 00: Transmission in progress or has not been requested
- 01: Transmission has been aborted from the corresponding TX message buffer
- 10: Transmission was successful from the corresponding TX message buffer and the CFDTMCn.TMTAR bit was not set for this TX message buffer
- 11: Transmission was successful from the corresponding TX message buffer, but the CFDTMCn.TMTAR bit was set for this TX message buffer.

Only write to these bits when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

The TMTRF[1:0] bits are cleared automatically when the CAN-FD module is in GL_RESET mode or the related channel is in CH_RESET mode.

32.2.49 CFDTMSTSn：TX消息缓冲区状态寄存器n（n=0到7、32到39、64到71、96到103）

Base address: CANFD = 0x400B_0000

Offset address: 0x07D0 + 0x01 × n

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMTSTS	TX消息缓冲区传输状态 0：没有进行中的传输1：进行中的传输	R
2:1	TMTRF[1:0]	TX消息缓冲区传输结果标志 00：无结果01：从TX报文缓冲区中止传输10：从TX报文缓冲区传输成功并且未请求传输中止 11：从TX报文缓冲区传输成功并请求传输中止	R/W
3	TMTRM	TX消息缓冲区传输请求已镜像 0：未请求TX消息缓冲区传输1：请求TX消息缓冲区传输	R
4	TMTARM	TX消息缓冲区传输中止请求已镜像 0：未请求TX报文缓冲区传输请求中止1：已请求TX报文缓冲区传输请求中止	R
7:5	—	这些位被读取为0。写入值应为0。	R/W

TX报文缓冲区状态寄存器显示相应报文缓冲区的传输和传输中止状态。

TMTSTS位（TX报文缓冲区传输状态）

TMTSTS位在相应TX报文缓冲区的传输开始时自动设置。

该位在以下情况下自动清零：

●传输停止

●CAN-FD模块处于GL_RESET模式

●相关的CAN-FD通道处于CH_RESET模式。

TMTRF[1:0]位（TX报文缓冲区传输结果标志）

TMTRF[1:0]位显示相应TX报文缓冲区的结果。状态如下：

●00：传输中或未请求

●01：已从相应的TX消息缓冲区中止传输

●10：从相应的TX报文缓冲区发送成功，并且没有为该TX报文缓冲区设置CFDTMCn.TMTAR位

●11：从相应的TX报文缓冲区发送成功，但为该TX报文缓冲区设置了CFDTMCn.TMTAR位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入这些位。

当CAN-FD模块处于GL_RESET模式或相关通道处于CH_RESET模式时，TMTRF[1:0]位会自动清零。

TMTRM bit (TX Message Buffer Transmission Request Mirrored)

The TMTRM bit is set when the CFDTMCn.TMTR bit in the corresponding CFDTMCn register is set.

This bit is cleared when the CFDTMCn.TMTR bit in the corresponding CFDTMCn register is cleared.

TMTARM bit (TX Message Buffer Transmission Abort Request Mirrored)

The TMTARM bit is set when the CFDTMCn.TMTAR bit in the corresponding CFDTMCn register is set.

This bit is cleared when the CFDTMCn.TMTAR bit in the corresponding CFDTMCn register is cleared.

32.2.50 CFDTMTRSTSf : TX Message Buffer Transmission Request Status Register f (f = 0 to 3)

Base address: CANFD = 0x400B_0000

Offset address: 0x0CD0 + 0x04 × f

Bit position:	31																						8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTRSTSg[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFDTMTRSTSg[7:0]	TX Message Buffer Transmission Request Status 0: Transmission not requested for corresponding TX message buffer 1: Transmission requested for corresponding TX message buffer	R
31:8	—	These bits are read as 0. The write value should be 0.	R

CFDTMTRSTSg[7:0] bits (TX Message Buffer Transmission Request Status)

The CFDTMTRSTSg[7:0] bits show status of the CFDTMCn.TMTR bits of the TX Message Buffer Control Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Control Registers (CFDTMCn), and only when the message buffer does not belong to a TX Queue.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Control Registers
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

32.2.51 CFDTMTARSTSf : TX Message Buffer Transmission Abort Request Status Register f (f = 0 to 3)

Base address: CANFD = 0x400B_0000

Offset address: 0x0D70 + 0x04 × f

Bit position:	31																						8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTARSTSg[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFDTMTARSTSg[7:0]	TX Message Buffer Transmission Abort Request Status 0: Transmission abort not requested for corresponding TX message buffer 1: Transmission abort requested for corresponding TX message buffer	R
31:8	—	These bits are read as 0. The write value should be 0.	R

TMTRM位（镜像的TX消息缓冲区传输请求）

当相应CFDTMCn寄存器中的CFDTMCn.TMTR位置位时，TMTRM位置位。

当相应CFDTMCn寄存器中的CFDTMCn.TMTR位清零时，该位清零。

TMTARM位（已镜像TX消息缓冲区传输中止请求）

当相应的CFDTMCn寄存器中的CFDTMCn.TMTAR位被置位时，TMTARM位被置位。

当相应CFDTMCn寄存器中的CFDTMCn.TMTAR位清零时，该位清零。

32.2.50 CFDTMTRSTSf：TX报文缓冲区传输请求状态寄存器f（f=0到3）

Base address: CANFD = 0x400B_0000

Offset address: 0x0CD0 + 0x04 × f

Bit position:	31																						8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTRSTSg[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFDTMTRSTSg[7:0]	TX消息缓冲区传输请求状态 0：对应的TX报文缓冲区未请求传输1：对应的TX报文缓冲区请求传输	R
31:8	—	这些位被读取为0。写入值应为0。	R

CFDTMTRSTSg[7:0]位（TX消息缓冲区传输请求状态）

CFDTMTRSTSg[7:0]位显示TX报文缓冲区控制寄存器的CFDTMCn.TMTR位的状态。

当TX报文缓冲区控制寄存器(CFDTMCn)中的相应位置位时，每个位都会自动设置，并且仅当报文缓冲区不属于TX队列时。

在以下情况下，每个位都会自动清除：

- TX报文缓冲区控制寄存器中的相应位清零
- CAN-FD模块处于GL_RESET模式
- 相关的CAN-FD通道处于CH_RESET模式。

32.2.51 CFDTMTARSTSf:TX消息缓冲区传输中止请求状态寄存器f（f=0到3）

Base address: CANFD = 0x400B_0000

Offset address: 0x0D70 + 0x04 × f

Bit position:	31																						8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CFDTMTARSTSg[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFDTMTARSTSg[7:0]	TX消息缓冲区传输中止请求状态 0：对应的TX报文缓冲区未请求发送中止1：对应的TX报文缓冲区请求发送中止	R
31:8	—	这些位被读取为0。写入值应为0。	R

CFDTMTARSTSg[7:0] bits (TX Message Buffer Transmission Abort Request Status)

The CFDTMTARSTSg[7:0] bits show status of the CFDTMCn.TMTAR bits of the TX Message Buffer Control Registers.

Alignment of the CFDTMTARSTSg[7:0] bits is shown in Table 32.5.

Table 32.5 Alignment of CFDTMTARSTSg[7:0] mirror bits

Bit position	g = TX message buffer number
n*64-fmin*32	n*64+0
n*64+1-fmin*32	n*64+1
⋮	⋮
n*64+31-fmin*32	n*64+31
n*64+32-fmax*32	n*64+32
n*64+33-fmax*32	n*64+33
⋮	⋮
n*64+62-fmax*32	n*64+62
n*64+63-fmax*32	n*64+63

Note: When n = 0, fmin = 0, fmax = 1
When n = 1, fmin = 2, fmax = 3

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Control Registers, and when the message buffer belongs to a TX Queue.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Control Registers
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

32.2.52 CFDTMTCSTSf : TX Message Buffer Transmission Completion Status Register f (f = 0 to 3)

Base address: CANFD = 0x400B_0000

Offset address: 0x0E10 + 0x04 × f

Bit position:	31 … 8	7 … 0
Bit field:	—	CFDTMTCSTSf[7:0]
Value after reset:	0	0

Bit	Symbol	Function	R/W
7:0	CFDTMTCSTSf[7:0]	TX Message Buffer Transmission Completion Status 0: Transmission not complete for corresponding TX message buffer 1: Transmission completed for corresponding TX message buffer	R
31:8	—	These bits are read as 0. The write value should be 0.	R

CFDTMTCSTSf[7:0] bits (TX Message Buffer Transmission Completion Status)

The CFDTMTCSTSf[7:0] bits show status of successful completion of the TX Message Buffer Status Registers.

Each bit is set automatically when the corresponding bit is set in the TX Message Buffer Status Registers.

Each bit is cleared automatically when:

- The corresponding bit is cleared in the TX Message Buffer Status Registers
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

CFDTMTARSTSg[7:0]位（TX报文缓冲区传输中止请求状态）

CFDTMTARSTSg[7:0]位显示TX报文缓冲区控制寄存器的CFDTMCn.TMTAR位的状态。

CFDTMTARSTSg[7:0]位的对齐方式如表32.5所示。

Table 32.5 CFDTMTARSTSg[7:0]镜像位的对齐

位位置	g=TX消息缓冲区编号
n*64-fmin*32	n*64+0
n*64+1-fmin*32	n*64+1
⋮	⋮
n*64+31-fmin*32	n*64+31
n*64+32-fmax*32	n*64+32
n*64+33-fmax*32	n*64+33
⋮	⋮
n*64+62-fmax*32	n*64+62
n*64+63-fmax*32	n*64+63

Note: When n = 0, fmin = 0, fmax = 1
When n = 1, fmin = 2, fmax = 3

当TX报文缓冲区控制寄存器中的相应位被设置时，并且报文缓冲区属于TX队列时，每个位都会自动设置。

在以下情况下，每个位都会自动清除：

- TX报文缓冲区控制寄存器中的相应位清零
- CAN-FD模块处于GL_RESET模式
- 相关的CAN-FD通道处于CH_RESET模式。

32.2.52 CFDTMTCSTSf：TX报文缓冲区传输完成状态寄存器f（f=0到3）

Base address: CANFD = 0x400B_0000

Offset address: 0x0E10 + 0x04 × f

Bit position:	31 … 8	7 … 0
Bit field:	—	CFDTMTCSTSf[7:0]
重置后的值:	0	0

Bit	Symbol	Function	R/W
7:0	CFDTMTCSTSf[7:0]	TX消息缓冲区传输完成状态 0：对应的TX报文缓冲区的传输未完成1：对应的TX报文缓冲区的传输完成	R
31:8	—	这些位被读取为0。写入值应为0。	R

CFDTMTCSTSf[7:0]位（TX消息缓冲区传输完成状态）

CFDTMTCSTSf[7:0]位显示成功完成TX报文缓冲区状态寄存器的状态。

当在TX报文缓冲区状态寄存器中设置相应位时，每个位都会自动设置。

在以下情况下，每个位都会自动清除：

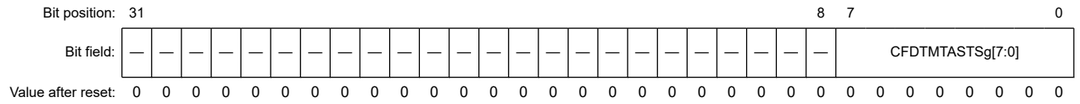
- TX报文缓冲区状态寄存器中的相应位清零
- CAN-FD模块处于GL_RESET模式
- 相关的CAN-FD通道处于CH_RESET模式。

If a CAN channel enters CH_RESET mode, then the bits related to that channel are cleared.

32.2.53 CFDTMTASTSf : TX Message Buffer Transmission Abort Status Register f (f = 0 to 3)

Base address: CANFD = 0x400B_0000

Offset address: 0x0EB0 + 0x04 × f



Bit	Symbol	Function	R/W
7:0	CFDTMTASTSg[7:0]	TX Message Buffer Transmission Abort Status 0: Transmission not aborted for corresponding TX message buffer 1: Transmission aborted for corresponding TX message buffer	R
31:8	—	These bits are read as 0. The write value should be 0.	R

CFDTMTASTSg[7:0] bits (TX Message Buffer Transmission Abort Status)

The CFDTMTASTSg[7:0] bits show status of the successful transmission abort of the corresponding TX message buffer.

Alignment of the CFDTMTASTSg[7:0] bits is shown in Table 32.6.

Table 32.6 Alignment of CFDTMTASTSg[7:0] mirror bits

Bit position	g = TX message buffer number
n*64-fmin*32	n*64+0
n*64+1-fmin*32	n*64+1
⋮	⋮
n*64+31-fmin*32	n*64+31
n*64+32-fmax*32	n*64+32
n*64+33-fmax*32	n*64+33
⋮	⋮
n*64+62-fmax*32	n*64+62
n*64+63-fmax*32	n*64+63

Note: When n = 0, fmin = 0, fmax = 1
When n = 1, fmin = 2, fmax = 3

Each bit is set automatically when the CFDTMSTSn.TMTRF bits are set to 01b in the corresponding TX Message Buffer Status Register.

Each bit is cleared automatically when:

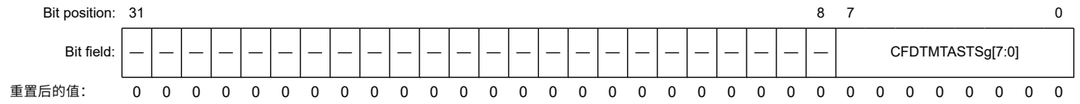
- The CFDTMSTSn.TMTRF bits are cleared in the corresponding TX Message Buffer Status Register
- The CAN-FD module is in GL_RESET mode
- The related CAN-FD channel is in CH_RESET mode.

如果CAN通道进入CH_RESET模式，则与该通道相关的位被清除。

32.2.53 CFDTMTASTSf：TX报文缓冲区传输中止状态寄存器f（f=0到3）

Base address: CANFD = 0x400B_0000

Offset address: 0x0EB0 + 0x04 × f



Bit	Symbol	Function	R/W
7:0	CFDTMTASTSg[7:0]	TX报文缓冲区传输中止状态 0：相应的TX报文缓冲区的传输未中止1：相应的TX报文缓冲区的传输中止	R
31:8	—	这些位被读取为0。写入值应为0。	R

CFDTMTASTSg[7:0]位（TX报文缓冲区传输中止状态）

CFDTMTASTSg[7:0]位显示相应TX消息缓冲区的成功发送中止状态。

CFDTMTASTSg[7:0]位的对齐如表32.6所示。

Table 32.6 CFDTMTASTSg[7:0]镜像位的对齐

位位置	g=TX消息缓冲区编号
n*64-fmin*32	n*64+0
n*64+1-fmin*32	n*64+1
⋮	⋮
n*64+31-fmin*32	n*64+31
n*64+32-fmax*32	n*64+32
n*64+33-fmax*32	n*64+33
⋮	⋮
n*64+62-fmax*32	n*64+62
n*64+63-fmax*32	n*64+63

Note: When n = 0, fmin = 0, fmax = 1
When n = 1, fmin = 2, fmax = 3

当相应的TX报文缓冲区中的CFDTMSTSn.TMTRF位设置为01b时，每个位都会自动设置状态寄存器。

在以下情况下，每个位都会自动清除：

- CFDTMSTSn.TMTRF位在相应的TX报文缓冲区状态寄存器中清零
- CAN-FD模块处于GL_RESET模式
- 相关的CAN-FD通道处于CH_RESET模式。

32.2.54 CFDTMIECf : TX Message Buffer Interrupt Enable Configuration Register f (f = 0 to 3)

Base address: CANFD = 0x400B_0000

Offset address: 0x0F50 + 0x04 × f

Bit position:	31	…	8	7	…	0
Bit field:	—	…	—	TMIEf[7:0]		
Value after reset:	0	…	0	0	…	0

Bit	Symbol	Function	R/W
7:0	TMIEf[7:0]	TX Message Buffer Interrupt Enable 0: TX message buffer interrupt disabled for corresponding TX message buffer 1: TX message buffer interrupt enabled for corresponding TX message buffer	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R

TMIEf[7:0] bits (TX Message Buffer Interrupt Enable)

If the TMIEf[7:0] bits are set, an interrupt is generated at the end of a successful transmission from the corresponding message buffer.

See section 32.7. Interrupts and DMA for TX Message Buffer Interrupt specification.

Do not write to the TMIEf[7:0] bits when:

- The CAN-FD module is in GL_SLEEP mode
- The related CAN-FD channel is in CH_SLEEP mode
- The corresponding TX message buffer is part of a TX Queue
- The corresponding TX message buffer is linked to a Common FIFO with the CFDCFCCn.CFTML bits.

32.2.55 CFDTXQCC0n : TX Queue Configuration/Control Registers 0n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1000 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	TXQOFRXIE	TXQFIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	TXQGWE	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX Queue Enable 0: TX Queue disabled 1: TX Queue enabled	R/W
1	TXQGWE	TX Queue Gateway Mode Enable 0: TX Queue GW mode disabled 1: TX Queue GW mode enabled	R/W
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	TXQTXIE	TX Queue TX Interrupt Enable 0: TX Queue TX interrupt disabled 1: TX Queue TX interrupt enabled	R/W

32.2.54 CFDTMIECf：TX报文缓冲区中断使能配置寄存器f（f=0到3）

Base address: CANFD = 0x400B_0000

Offset address: 0x0F50 + 0x04 × f

Bit position:	31	…	8	7	…	0
Bit field:	—	…	—	TMIEf[7:0]		
重置后的值：	0	…	0	0	…	0

Bit	Symbol	Function	R/W
7:0	TMIEf[7:0]	TX报文缓冲区中断使能 0：禁用相应TX报文缓冲区的TX报文缓冲区中断1：启用相应TX报文缓冲区的TX报文缓冲区中断	R/W
31:8	—	这些位被读取为0。写入值应为0。	R

TMIEf[7:0]位（TX报文缓冲区中断使能）

如果TMIEf[7:0]位被设置，则在从相应的消息缓冲区成功传输结束时会产生中断。

请参见第32.7节。TX消息缓冲区中断规范的中断和DMA。

在以下情况下不要写入TMIEf[7:0]位：

- ●CAN-FD模块处于GL_SLEEP模式
- ●相关CAN-FD通道处于CH_SLEEP模式
- ●对应的TX消息缓冲区是TXQueue的一部分
- ●相应的TX报文缓冲区通过CFDCFCCn.CFTML位链接到CommonFIFO。

32.2.55 CFDTXQCC0n：TX队列配置控制寄存器0n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1000 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	TXQOFRXIE	TXQFIE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	TXQGWE	TXQE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX队列启用 0：禁用TX队列1：启用TX队列	R/W
1	TXQGWE	TX队列网关模式启用 0：禁用TXQueueGW模式1：启用TXQueueGW模式	R/W
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	TXQTXIE	TX队列TX中断使能 0：禁止发送队列发送中断1：允许发送队列发送中断	R/W

Bit	Symbol	Function	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	TXQIM	TX Queue Interrupt Mode 0: When the last message is successfully transmitted 1: At every successful transmission	R/W
12:8	TXQDC[12:8]	TX Queue Depth Configuration 0x00: 0 messages 0x01: Reserved 0x02: 3 messages 0x03: 4 messages ⋮ 0x0F: 16 messages Others: Setting prohibited	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
16	TXQFIE	TXQ Full Interrupt Enable 0: TX Queue full interrupt generation disabled 1: TX Queue full interrupt generation enabled	R/W
17	TXQOFRXIE	TXQ One Frame Reception Interrupt Enable 0: One Frame RX interrupt generation disabled 1: One Frame RX interrupt generation enabled	R/W
18	TXQOFTXIE	TXQ One Frame Transmission Interrupt Enable 0: One Frame TX interrupt generation disabled 1: One Frame TX interrupt generation enabled	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Configuration/Control Registers 0n (n = 0, 1) are used to configure the TX Queue transmission.

TXQ0 is composed of TXMB0 to TXMB31 (at the maximum) when TXQE is enabled.

TXQE bit (TX Queue Enable)

The TXQE bit cannot be set if the configured TX Queue depth is 0x00 (CFDTXQCC0n.TXQDC == 0x00).

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_RESET or CH_SLEEP mode.

The TXQE bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

TXQGWE bit (TX Queue Gateway Mode Enable)

When the TXQGWE bit is set, the TX Queue is in TX Queue GW mode.

When this bit is set, CPU must not access the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQTXIE bit (TX Queue TX Interrupt Enable)

When the TXQTXIE bit is set, an interrupt is generated based on the setting of the TXQIM bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

TXQIM bit (TX Queue Interrupt Mode)

The TXQIM bit selects the interrupt generation condition for the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

Bit	Symbol	Function	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	TXQIM	TX队列中断模式 0：最后一条信息发送成功时1：每次发送成功时	R/W
12:8	TXQDC[12:8]	TX队列深度配置 0x00：0条消息0x0 1：保留0x02：3条 消息0x03：4条消 息 ⋮ 0x0F: 16 messages 其他：禁止设置	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W
16	TXQFIE	TXQ全中断使能 0：禁用TX队列满中断生成1：启用TX队列满中 断生成	R/W
17	TXQOFRXIE	TXQ一帧接收中断使能 0：禁止产生一帧RX中断1：允许产生一帧RX中 断	R/W
18	TXQOFTXIE	TXQ一帧传输中断使能 0：禁用一帧TX中断生成1：启用一帧TX中断生 成	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

TX队列配置控制寄存器0n(n=0 1)用于配置TX队列传输。

当TXQE使能时，TXQ0由TXMB0到TXMB31（最大）组成。

TXQE位（TX队列使能）

如果配置的TX队列深度为0x00(CFDTXQCC0n.TXQDC==0x00)，则无法设置TXQE位。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_RESET或CH_SLEEP模式时，请勿写入该位。

当相关CAN-FD通道处于CH_RESET模式时，TXQE位会自动清零。

TXQGWE位（TX队列网关模式启用）

当TXQGWE位置位时，TXQueue处于TXQueueGW模式。

当该位置位时，CPU不得访问TX队列。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQTXIE位（TX队列TX中断允许）

当TXQTXIE位置位时，会根据TXQIM位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

TXQIM位（TX队列中断模式）

TXQIM位选择TX队列的中断产生条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[12:8] bits (TX Queue Depth Configuration)

The TXQDC[12:8] bits select the depth of the transmission queue. The message buffer selection starts from MB[0] up to MB[7] depending on the configured depth.

When using TXQ1 and TXQ0 simultaneously, the total depth of TXQ1 and TXQ0 should be 8 or less.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQFIE bit (TXQ Full Interrupt Enable)

When the TXQFIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS0n.TXQFIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

Only write 1 to this bit in Gateway mode (CFDTXQCC0n.TXQGWE = 1).

TXQOFRXIE bit (TXQ One Frame Reception Interrupt Enable)

When the TXQOFRXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS0n.TXQOFRXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

Only write 1 to this bit in GW mode (CFDTXQCC0n.TXQGWE = 1).

TXQOFTXIE bit (TXQ One Frame Transmission Interrupt Enable)

When the TXQOFTXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS0n.TXQOFTXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

32.2.56 CFDTXQCC1n : TX Queue Configuration/Control Registers 1n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1060 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	TXQOFRXIE	TXQFIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	TXQGWE	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX Queue Enable 0: TX Queue disabled 1: TX Queue enabled	R/W

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[12:8]位（TX队列深度配置）

TXQDC[12:8]位选择传输队列的深度。消息缓冲区选择从MB[0]开始直到MB[7]取决于配置的深度。

当同时使用TXQ1和TXQ0时，TXQ1和TXQ0的总深度应小于等于8。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQFIE位（TXQ完全中断允许）

当TXQFIE位置位时，会根据CFDTXQSTS0n.TXQFIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

仅在网关模式下向该位写入1(CFDTXQCC0n.TXQGWE=1)。

TXQOFRXIE位（TXQ一帧接收中断允许）

当TXQOFRXIE位置位时，会根据CFDTXQSTS0n.TXQOFRXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

仅在GW模式下（CFDTXQCC0n.TXQGWE=1）向该位写入1。

TXQOFTXIE位（TXQ一帧传输中断允许）

当TXQOFTXIE位置位时，会根据CFDTXQSTS0n.TXQOFTXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

32.2.56 CFDTXQCC1n：TX队列配置控制寄存器1n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1060 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	TXQOFRXIE	TXQFIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	TXQGWE	TXQE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX队列启用 0：禁用TX队列1：启用TX队列	R/W

Bit	Symbol	Function	R/W
1	TXQGWE	TX Queue Gateway Mode Enable 0: TX Queue GW mode disabled 1: TX Queue GW mode enabled	R/W
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	TXQTXIE	TX Queue TX Interrupt Enable 0: TX Queue TX interrupt disabled 1: TX Queue TX interrupt enabled	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	TXQIM	TX Queue Interrupt Mode 0: When the last message is successfully transmitted 1: At every successful transmission	R/W
12:8	TXQDC[12:8]	TX Queue Depth Configuration 0x00: 0 messages 0x01: Reserved 0x02: 3 messages 0x03: 4 messages ⋮ 0x0F: 16 messages Others: Setting prohibited	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
16	TXQFIE	TXQ Full Interrupt Enable 0: TX Queue full interrupt generation disabled 1: TX Queue full interrupt generation enabled	R/W
17	TXQOFRXIE	TXQ One Frame Reception Interrupt Enable 0: One Frame RX interrupt generation disabled 1: One Frame RX interrupt generation enabled	R/W
18	TXQOFTXIE	TXQ One Frame Transmission Interrupt Enable 0: One Frame TX interrupt generation disabled 1: One Frame TX interrupt generation enabled	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Configuration/Control Registers 1n (n = 0, 1) are used to configure the TX Queue transmission.

TXQ1 is composed of TXMB31 to TXMB0 (at the maximum) when TXQE is enabled.

TXQE bit (TX Queue Enable)

The TXQE bit cannot be set if the configured TX Queue depth is 0x00 (CFDTXQCC1n.TXQDC == 0x00).

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do write to this bit when the related CAN-FD channel is in CH_RESET or CH_SLEEP mode.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

TXQGWE bit (TX Queue Gateway Mode Enable)

When the TXQGWE bit is set, the TX Queue is in TX Queue Gateway mode.

When this bit is set, CPU must not access the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQTXIE bit (TX Queue TX Interrupt Enable)

When the TXQTXIE bit is set, an interrupt is generated based on the setting of the TXQIM bit.

Bit	Symbol	Function	R/W
1	TXQGWE	TX队列网关模式启用 0：禁用TXQueueGW模式1：启用TXQueueGW模式	R/W
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	TXQTXIE	TX队列TX中断使能 0：禁止发送队列发送中断1：允许发送队列发送中断	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	TXQIM	TX队列中断模式 0：最后一条信息发送成功时1：每次发送成功时	R/W
12:8	TXQDC[12:8]	TX队列深度配置 0x00：0条消息0x01：保留0x02：3条消息0x03：4条消息 ⋮ 0x0F: 16 messages 其他：禁止设置	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W
16	TXQFIE	TXQ全中断使能 0：禁用TX队列满中断生成1：启用TX队列满中断生成	R/W
17	TXQOFRXIE	TXQ一帧接收中断使能 0：禁止产生一帧RX中断1：允许产生一帧RX中断	R/W
18	TXQOFTXIE	TXQ一帧传输中断使能 0：禁用一帧TX中断生成1：启用一帧TX中断生成	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

TX队列配置控制寄存器1n(n=0 1)用于配置TX队列传输。

当TXQE使能时，TXQ1由TXMB31到TXMB0（最大）组成。

TXQE位（TX队列使能）

如果配置的TX队列深度为0x00(CFDTXQCC1n.TXQDC==0x00)，则无法设置TXQE位。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_RESET或CH_SLEEP模式时，请写入该位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

TXQGWE位（TX队列网关模式启用）

当TXQGWE位置位时，TX队列处于TX队列网关模式。

当该位置位时，CPU不得访问TX队列。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQTXIE位（TX队列TX中断允许）

当TXQTXIE位置位时，会根据TXQIM位的设置产生中断。

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

TXQIM bit (TX Queue Interrupt Mode)

The TXQIM bit selects the interrupt generation condition for the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_SLEEP
- CH_OPERATION.

TXQDC[12:8] bits (TX Queue Depth Configuration)

The TXQDC[12:8] bits select the depth of the transmission queue. The message buffer selection starts from MB[7] down to MB[0] depending on the configured depth.

When using TXQ1 and TXQ0 simultaneously, the total depth of TXQ1 and TXQ0 should be 8 or less.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQFIE bit (TXQ Full Interrupt Enable)

When the TXQFIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS1n.TXQFIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

Only write 1 to this bit when in Gateway mode (CFDTXQCC1n.TXQGWE = 1)..

TXQOFRXIE bit (TXQ One Frame Reception Interrupt Enable)

When the TXQOFRXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS1n.TXQOFRXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

Only write 1 to this bit when in Gateway mode (CFDTXQCC1n.TXQGWE = 1).

TXQOFTXIE bit (TXQ One Frame Transmission Interrupt Enable)

When the TXQOFTXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS1n.TXQOFTXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

TXQIM位（TX队列中断模式）

TXQIM位选择TX队列的中断产生条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_SLEEP
- CH_OPERATION.

TXQDC[12:8]位（TX队列深度配置）

TXQDC[12:8]位选择传输队列的深度。消息缓冲区选择从MB[7]开始到MB[0]取决于配置的深度。

当同时使用TXQ1和TXQ0时，TXQ1和TXQ0的总深度应小于等于8。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQFIE位（TXQ完全中断允许）

当TXQFIE位置位时，根据CFDTXQSTS1n.TXQFIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

仅在网关模式下（CFDTXQCC1n.TXQGWE=1）时向该位写入1..

TXQOFRXIE位（TXQ一帧接收中断允许）

当TXQOFRXIE位置位时，会根据CFDTXQSTS1n.TXQOFRXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

仅在网关模式(CFDTXQCC1n.TXQGWE=1)时向该位写入1。

TXQOFTXIE位（TXQ一帧传输中断允许）

当TXQOFTXIE位置位时，会根据CFDTXQSTS1n.TXQOFTXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

32.2.57 CFDTXQCC2n : TX Queue Configuration/Control Registers 2n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x10C0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	TXQOFRXIE	TXQFIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	TXQGWE	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX Queue Enable 0: TX Queue disabled 1: TX Queue enabled	R/W
1	TXQGWE	TX Queue Gateway Mode Enable 0: TX Queue GW mode disabled 1: TX Queue GW mode enabled	R/W
4:2	—	These bits are read as 0. The write value should be 0.	R/W
5	TXQTXIE	TX Queue TX Interrupt Enable 0: TX Queue TX interrupt disabled 1: TX Queue TX interrupt enabled	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	TXQIM	TX Queue Interrupt Mode 0: When the last message is successfully transmitted 1: At every successful transmission	R/W
12:8	TXQDC[12:8]	TX Queue Depth Configuration 0x00: 0 messages 0x01: Reserved 0x02: 3 messages 0x03: 4 messages ⋮ 0x0F: 16 messages Others: Setting prohibited	R/W
15:13	—	These bits are read as 0. The write value should be 0.	R/W
16	TXQFIE	TXQ Full Interrupt Enable 0: TX Queue full interrupt generation disabled 1: TX Queue full interrupt generation enabled	R/W
17	TXQOFRXIE	TXQ One Frame Reception Interrupt Enable 0: One Frame RX interrupt generation disabled 1: One Frame RX interrupt generation enabled	R/W
18	TXQOFTXIE	TXQ One Frame Transmission Interrupt Enable 0: One Frame TX interrupt generation disabled 1: One Frame TX interrupt generation enabled	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Configuration/Control Registers 2n (n = 0, 1) are used to configure the TX Queue transmission.

TXQ2 is composed of TXMB32 to TXMB63 (at the maximum) when TXQE is enabled.

TXQE bit (TX Queue Enable)

The TXQE bit cannot be set if the configured TX Queue depth is 0x00 (CFDTXQCC2n.TXQDC == 0x00).

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

32.2.57 CFDTXQCC2n：TX队列配置控制寄存器2n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x10C0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	TXQOFRXIE	TXQFIE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	TXQGWE	TXQE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX队列启用 0：禁用TX队列1：启用TX队列	R/W
1	TXQGWE	TX队列网关模式启用 0：禁用TXQueueGW模式1：启用TXQueueGW模式	R/W
4:2	—	这些位被读取为0。写入值应为0。	R/W
5	TXQTXIE	TX队列TX中断使能 0：禁止发送队列发送中断1：允许发送队列发送中断	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	TXQIM	TX队列中断模式 0：最后一条信息发送成功时1：每次发送成功时	R/W
12:8	TXQDC[12:8]	TX队列深度配置 0x00：0条消息0x01：保留0x02：3条消息0x03：4条消息 ⋮ 0x0F：16 messages 其他：禁止设置	R/W
15:13	—	这些位被读取为0。写入值应为0。	R/W
16	TXQFIE	TXQ全中断使能 0：禁用TX队列满中断生成1：启用TX队列满中断生成	R/W
17	TXQOFRXIE	TXQ一帧接收中断使能 0：禁止产生一帧RX中断1：允许产生一帧RX中断	R/W
18	TXQOFTXIE	TXQ一帧传输中断使能 0：禁用一帧TX中断生成1：启用一帧TX中断生成	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

TX队列配置控制寄存器2n(n=0 1)用于配置TX队列传输。

当TXQE使能时，TXQ2由TXMB32到TXMB63（最大）组成。

TXQE位（TX队列使能）

如果配置的TX队列深度为0x00(CFDTXQCC2n.TXQDC==0x00)，则无法设置TXQE位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

RA生态工作室

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_RESET or CH_SLEEP mode.

TXQGWE bit (TX Queue Gateway Mode Enable)

When the TXQGWE bit is set, the TX Queue is in TX Queue Gateway mode. When this bit is set, CPU must not access the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQTXIE bit (TX Queue TX Interrupt Enable)

When the TXQTXIE bit is set, an interrupt is generated based on the setting of the TXQIM bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

TXQIM bit (TX Queue Interrupt Mode)

The TXQIM bit selects the interrupt generation condition for the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[12:8] bits (TX Queue Depth Configuration)

The TXQDC[12:8] bits select the depth of the transmission queue. The message buffer selection starts from MB[32] up to MB[39] depending on the configured depth.

When using TXQ3 and TXQ2 simultaneously, the total depth of TXQ3 and TXQ2 should be 8 or less.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_HALT
- CH_OPERATION
- CH_SLEEP.

TXQFIE bit (TXQ Full Interrupt Enable)

When the TXQFIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS2n.TXQFIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

Only write 1 to this bit when in GW mode (CFDTXQCC2n.TXQGWE = 1).

TXQOFRXIE bit (TXQ One Frame Reception Interrupt Enable)

When the TXQOFRXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS2n.TXQOFRXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

Only write 1 to this bit when in GW mode (CFDTXQCC2n.TXQGWE = 1).

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_RESET或CH_SLEEP模式时，请勿写入该位。

TXQGWE位（TX队列网关模式启用）

当TXQGWE位置位时，TX队列处于TX队列网关模式。当该位置位时，CPU不得访问TX Queue.

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQTXIE位（TX队列TX中断允许）

当TXQTXIE位置位时，会根据TXQIM位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

TXQIM位（TX队列中断模式）

TXQIM位选择TX队列的中断产生条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION.

TXQDC[12:8]位（TX队列深度配置）

TXQDC[12:8]位选择传输队列的深度。消息缓冲区选择从MB[32]开始直到MB[39]取决于配置的深度。

当同时使用TXQ3和TXQ2时，TXQ3和TXQ2的总深度应小于等于8。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_HALT
- CH_OPERATION
- CH_SLEEP.

TXQFIE位（TXQ完全中断允许）

当TXQFIE位置位时，会根据CFDTXQSTS2n.TXQFIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

仅在GW模式(CFDTXQCC2n.TXQGWE=1)时向该位写入1。

TXQOFRXIE位（TXQ一帧接收中断允许）

当TXQOFRXIE位置位时，会根据CFDTXQSTS2n.TXQOFRXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

仅在GW模式(CFDTXQCC2n.TXQGWE=1)时向该位写入1。

TXQOFTXIE bit (TXQ One Frame Transmission Interrupt Enable)

When the TXQOFTXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS2n.TXQOFTXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

32.2.58 CFDTXQCC3n : TX Queue Configuration/Control Registers 3n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1120 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	—	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX Queue Enable 0: TX Queue disabled 1: TX Queue enabled	R/W
4:1	—	These bits are read as 0. The write value should be 0.	R/W
5	TXQTXIE	TX Queue TX Interrupt Enable 0: TX Queue TX interrupt disabled 1: TX Queue TX interrupt enabled	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	TXQIM	TX Queue Interrupt Mode 0: When the last message is successfully transmitted 1: At every successful transmission	R/W
12:8	TXQDC[12:8]	TX Queue Depth Configuration 0x00: 0 messages 0x01: Reserved 0x02: 3 messages 0x03: 4 messages ⋮ 0x0F: 16 messages Others: Setting prohibited	R/W
17:13	—	These bits are read as 0. The write value should be 0.	R/W
18	TXQOFTXIE	TXQ One Frame Transmission Interrupt Enable 0: One Frame TX interrupt generation disabled 1: One Frame TX interrupt generation enabled	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The TX QueueConfiguration/Control Registers 3n (n = 0, 1) are used to configure the TX Queue transmission.

TXQ3 is composed of TXMB63 to TXMB32 (at the maximum) when TXQE is enabled.

TXQE bit (TX Queue Enable)

The TXQE bit cannot be set if the configured TX Queue depth is 0x00 (CFDTXQCC3n.TXQDC == 0x00).

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_RESET or CH_SLEEP mode.

TXQOFTXIE位（TXQ一帧传输中断允许）

当TXQOFTXIE位置位时，会根据CFDTXQSTS2n.TXQOFTXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

32.2.58 CFDTXQCC3n：TX队列配置控制寄存器3n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1120 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIE	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TXQDC[12:8]					TXQIM	—	TXQTXIE	—	—	—	—	TXQE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TXQE	TX队列启用 0：禁用TX队列1：启用TX队列	R/W
4:1	—	这些位被读取为0。写入值应为0。	R/W
5	TXQTXIE	TX队列TX中断使能 0：禁止发送队列发送中断1：允许发送队列发送中断	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	TXQIM	TX队列中断模式 0：最后一条信息发送成功时1：每次发送成功时	R/W
12:8	TXQDC[12:8]	TX队列深度配置 0x00：0条消息0x01：保留0x02：3条消息0x03：4条消息 ⋮ 0x0F：16 messages 其他：禁止设置	R/W
17:13	—	这些位被读取为0。写入值应为0。	R/W
18	TXQOFTXIE	TXQ一帧传输中断使能 0：禁用一帧TX中断生成1：启用一帧TX中断生成	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

TXQueueConfiguration控制寄存器3n(n=0 1)用于配置TXQueue传输。

当TXQE使能时，TXQ3由TXMB63到TXMB32（最大）组成。

TXQE位（TX队列使能）

如果配置的TX队列深度为0x00(CFDTXQCC3n.TXQDC==0x00)，则无法设置TXQE位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_RESET或CH_SLEEP模式时，请勿写入该位。

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TXQTXIE bit (TX Queue TX Interrupt Enable)

When the TXQTXIE bit is set, an interrupt is generated based on the setting of the TXQIM bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

TXQIM bit (TX Queue Interrupt Mode)

The TXQIM bit selects the interrupt generation condition for the TX Queue.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION mode.

TXQDC[12:8] bits (TX Queue Depth Configuration)

The TXQDC[12:8] bits select the depth of the transmission queue. The message buffer selection starts from MB[39] down to MB[32] depending on the configured depth.

When using TXQ3 and TXQ2 simultaneously, the total depth of TXQ3 and TXQ2 should be 8 or less.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in any of the following modes:

- CH_SLEEP
- CH_HALT
- CH_OPERATION mode.

TXQOFTXIE bit (TXQ One Frame Transmission Interrupt Enable)

When the TXQOFTXIE bit is set, an interrupt is generated based on the setting of the CFDTXQSTS3n.TXQOFTXIF bit.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the related CAN-FD channel is in CH_SLEEP mode.

32.2.59 CFDTXQSTS0n : TX Queue Status Registers 0n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1020 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	TXQMLT	TXQOFTXIF	TXQOFRXIF	TXQFIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX Queue Empty 0: TX Queue not empty 1: TX Queue empty	R
1	TXQFLL	TX Queue Full 0: TX Queue not full 1: TX Queue full	R

TXQTXIE位（TX队列TX中断允许）

当TXQTXIE位置位时，会根据TXQIM位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

TXQIM位（TX队列中断模式）

TXQIM位选择TX队列的中断产生条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION mode.

TXQDC[12:8]位（TX队列深度配置）

TXQDC[12:8]位选择传输队列的深度。根据配置的深度，消息缓冲区选择从MB[39]开始到MB[32]。

当同时使用TXQ3和TXQ2时，TXQ3和TXQ2的总深度应小于等于8。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于以下任一模式时，请勿写入该位：

- CH_SLEEP
- CH_HALT
- CH_OPERATION mode.

TXQOFTXIE位（TXQ一帧传输中断允许）

当TXQOFTXIE位置位时，会根据CFDTXQSTS3n.TXQOFTXIF位的设置产生中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入该位。

32.2.59 CFDTXQSTS0n：TX队列状态寄存器0n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1020 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	TXQMLT	TXQOFTXIF	TXQOFRXIF	TXQFIF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX队列空 0：TX队列不为空1：TX队列为空	R
1	TXQFLL	TX队列已满 0：TX队列未满1：TX队列已满	R

Bit	Symbol	Function	R/W
2	TXQTXIF	TX Queue TX Interrupt Flag 0: TX Queue interrupt condition not satisfied after a frame TX 1: TX Queue interrupt condition satisfied after a frame TX	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
13:8	TXQMC[13:8]	TX Queue Message Count Number of messages in the TX Queue.	R
15:14	—	These bits are read as 0. The write value should be 0.	R/W
16	TXQFIF	TXQ Full Interrupt Flag When TXQ is in full status, an interrupt is set.	R/W
17	TXQOFRXIF	TXQ One Frame Reception Interrupt Flag When TXQ receives one frame, an interrupt is set.	R/W
18	TXQOFTXIF	TXQ One Frame Transmission Interrupt Flag When one frame transmits from TXQ, an interrupt is set.	R/W
19	TXQMLT	TXQ Message Lost 0: No message lost in TXQ 1: TXQ message lost	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Status Registers 0n (n = 0, 1) show the status of the TX Queue of corresponding CAN channel.

TXQEMP bit (TX Queue Empty)

The TXQEMP bit is set automatically when the TX Queue is disabled or no messages are stored in the TX Queue.

This bit is set automatically when:

- The last message is transmitted from the TX Queue
- The related CAN-FD channel is in CH_RESET mode.

The bit is cleared automatically when the first message to be transmitted is stored in the TX Queue.

TXQFLL bit (TX Queue Full)

The TXQFLL bit is set automatically when the number of CAN messages stored in the TX Queue matches the configured TX Queue depth.

This bit is cleared automatically when:

- The number of CAN messages stored in the TX Queue is less than the configured TX Queue depth
- The related CAN-FD channel is in CH_RESET mode.

TXQTXIF bit (TX Queue TX Interrupt Flag)

The TXQTXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

This bit is set automatically when the configured interrupt condition is satisfied for the TX Queue.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMC[13:8] bits (TX Queue Message Count)

The TXQMC[13:8] bits show the number of CAN messages in the TX Queue.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Bit	Symbol	Function	R/W
2	TXQTXIF	TX队列TX中断标志 0：一帧TX后不满足TX队列中断条件1：一帧TX后满足TX队列中断条件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
13:8	TXQMC[13:8]	TX队列消息计数 TX队列中的消息数。	R
15:14	—	这些位被读取为0。写入值应为0。	R/W
16	TXQFIF	TXQ完全中断标志 当TXQ处于满状态时，会设置一个中断。	R/W
17	TXQOFRXIF	TXQ一帧接收中断标志 当TXQ接收到一帧时，设置中断。	R/W
18	TXQOFTXIF	TXQ一帧传输中断标志 当从TXQ发送一帧时，设置中断。	R/W
19	TXQMLT	TXQ消息丢失 0：TXQ中没有消息丢失1：TXQ消息丢失	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

TX队列状态寄存器0n(n=0 1)显示相应CAN通道的TX队列状态。

TXQEMP位（TX队列空）

当TX队列被禁用或没有消息存储在TX队列中时，TXQEMP位自动置位。

该位在以下情况下自动设置：

●最后一条消息是从TXQueue发送的

●相关的CAN-FD通道处于CH_RESET模式。

当要发送的第一个消息存储在TX队列中时，该位会自动清除。

TXQFLL位（TX队列已满）

当存储在TX队列中的CAN报文数量与配置的匹配时，自动设置TXQFLL位
TX队列深度。

该位在以下情况下自动清零：

●TXQueue中存储的CAN报文数量小于配置的TXQueue深度

●相关的CAN-FD通道处于CH_RESET模式。

TXQTXIF位（TX队列TX中断标志 ）

如果TX队列被禁止，TXQTXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当为TX队列配置的中断条件满足时，该位自动置位。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMC[13:8]位（TX队列消息计数）

TXQMC[13:8]位显示TX队列中的CAN报文数。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

TXQFIF bit (TXQ Full Interrupt Flag)

The TXQFIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of the TX Queue.

Only in GW mode (CFDTXQCC0n.TXQGWE = 1) that this bit is set automatically when the TX Queue enters a buffer full status.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQOFRXIF bit (TXQ One Frame Reception Interrupt Flag)

The TXQOFRXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue. When receiving data is stored in the TX Queue in Gateway mode, this bit is set automatically.

This function can only be used in GW mode of the TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQOFTXIF bit (TXQ One Frame Transmission Interrupt Flag)

The TXQOFTXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue. When transmission is successful in the TX Queue, this bit is set automatically.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMLT bit (TXQ Message Lost)

The TXQMLT bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue. When a message lost occurs in GW mode of the TX Queue, this bit is set automatically.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQFIF位（TXQ满中断标志）

如果TX队列被禁止，TXQFIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX的空状态后清除该位
Queue.

只有在GW模式下（CFDTXQCC0n.TXQGWE=1），当TX队列进入缓冲区满状态时，该位才会自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQOFRXIF位（TXQ一帧接收中断标志）

如果TX队列被禁止，TXQOFRXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当接收数据在网关模式下存储在TX队列中时，该位自动设置。

该功能只能在TXQueue的GW模式下使用。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQOFTXIF位（TXQ一帧发送中断标志）

如果TX队列被禁止，TXQOFTXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当TXQueue中的传输成功时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMLT位（TXQ消息丢失）

如果TX队列被禁止，TXQMLT位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当TXQueue的GW模式下发生消息丢失时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

32.2.60 CFDTXQSTS1n : TX Queue Status Registers 1n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1080 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	TXQMLT	TXQOFTXIF	TXQOFRXIF	TXQFIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX Queue Empty 0: TX Queue not empty 1: TX Queue empty	R
1	TXQFLL	TX Queue Full 0: TX Queue not full 1: TX Queue full	R
2	TXQTXIF	TX Queue TX Interrupt Flag 0: TX Queue interrupt condition not satisfied after a frame TX 1: TX Queue interrupt condition satisfied after a frame TX	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
13:8	TXQMC[13:8]	TX Queue Message Count Number of messages in the TX Queue	R
15:14	—	These bits are read as 0. The write value should be 0.	R/W
16	TXQFIF	TXQ Full Interrupt Flag When TXQ is in full status, an interrupt is set.	R/W
17	TXQOFRXIF	TXQ One Frame Reception Interrupt Flag When TXQ receives one frame, an interrupt is set.	R/W
18	TXQOFTXIF	TXQ One Frame Transmission Interrupt Flag When one frame transmits from TXQ, an interrupt is set.	R/W
19	TXQMLT	TXQ Message Lost 0: No message lost in TXQ 1: TXQ message lost	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Status Registers 1n (n = 0, 1) show the status of the TX Queue of corresponding CAN channel.

TXQEMP bit (TX Queue Empty)

The TXQEMP bit is set automatically when the TX Queue is disabled or no messages are stored in the TX Queue.

The bit is cleared automatically when the first message to be transmitted is stored in the TX Queue.

This bit is set automatically when:

- The last message is transmitted from the TX Queue
- The related CAN-FD channel is in CH_RESET mode.

TXQFLL bit (TX Queue Full)

The TXQFLL bit is set automatically when the number of CAN messages stored in the TX Queue matches the configured TX Queue depth.

This bit is cleared automatically when:

- The number of CAN messages stored in the TX Queue is less than the configured TX Queue depth

32.2.60 CFDTXQSTS1n：TX队列状态寄存器1n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1080 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	TXQMLT	TXQOFTXIF	TXQOFRXIF	TXQFIF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX队列空 0：TX队列不为空1：TX队列为空	R
1	TXQFLL	TX队列已满 0：TX队列未满1：TX队列已满	R
2	TXQTXIF	TX队列TX中断标志 0：一帧TX后不满足TX队列中断条件1：一帧TX后满足TX队列中断条件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
13:8	TXQMC[13:8]	TX队列消息计数 TX队列中的消息数	R
15:14	—	这些位被读取为0。写入值应为0。	R/W
16	TXQFIF	TXQ完全中断标志 当TXQ处于满状态时，会设置一个中断。	R/W
17	TXQOFRXIF	TXQ一帧接收中断标志 当TXQ接收到一帧时，设置中断。	R/W
18	TXQOFTXIF	TXQ一帧传输中断标志 当从TXQ发送一帧时，设置中断。	R/W
19	TXQMLT	TXQ消息丢失 0：TXQ中没有消息丢失1：TXQ消息丢失	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

TX队列状态寄存器1n(n=0 1)显示相应CAN通道的TX队列状态。

TXQEMP位（TX队列空）

当TX队列被禁用或没有消息存储在TX队列中时，TXQEMP位自动置位。

当要发送的第一个消息存储在TX队列中时，该位会自动清除。

该位在以下情况下自动设置：

- ●最后一条消息是从TXQueue发送的
- ●相关的CAN-FD通道处于CH_RESET模式。

TXQFLL位（TX队列已满）

当存储在TX队列中的CAN报文数量与配置的匹配时，自动设置TXQFLL位TX队列深度。

该位在以下情况下自动清零：

- ●TXQueue中存储的CAN报文数量小于配置的TXQueue深度

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- The related CAN-FD channel is in CH_RESET mode.

TXQTXIF bit (TX Queue TX Interrupt Flag)

The TXQTXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.

This bit is set automatically when the configured interrupt condition is satisfied for the TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMC[13:8] bits (TX Queue Message Count)

The TXQMC[13:8] bits show the number of CAN messages in the TX Queue.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

TXQFIF bit (TXQ Full Interrupt Flag)

The TXQFIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.

Only in Gateway mode (CFDTXQCC1n.TXQGWE = 1) that this bit is set automatically when TX Queue enters a buffer full status.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQOFRXIF bit (TXQ One Frame Reception Interrupt Flag)

The TXQOFRXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.
When receiving data is stored in the TX Queue in Gateway mode, this bit is set automatically.

This function can only be used in GW mode of the TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQOFTXIF bit (TXQ One Frame Transmission Interrupt Flag)

The TXQOFTXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.
When transmission is successful in the TX Queue, this bit is set automatically.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

●相关的CAN-FD通道处于CH_RESET模式。

TXQTXIF位（TX队列TX中断标志 ）

如果TX队列被禁止，TXQTXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。

当为TX队列配置的中断条件满足时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMC[13:8]位（TX队列消息计数）

TXQMC[13:8]位显示TX队列中的CAN报文数。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

TXQFIF位（TXQ满中断标志）

如果TX队列被禁止，TXQFIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。

只有在网关模式（CFDTXQCC1n.TXQGWE=1）下，当TXQueue进入缓冲区满状态时，该位才会自动设置。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQOFRXIF位（TXQ一帧接收中断标志）

如果TX队列被禁止，TXQOFRXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当接收数据在网关模式下存储在TX队列中时，该位自动设置。

该功能只能在TXQueue的GW模式下使用。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQOFTXIF位（TXQ一帧发送中断标志）

如果TX队列被禁止，TXQOFTXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当TXQueue中的传输成功时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMLT bit (TXQ Message Lost)

The TXQMLT bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue. When a message lost occurs in GW mode of the TX Queue, this bit is set automatically.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

32.2.61 CFDTXQSTS2n : TX Queue Status Registers 2n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x10E0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	TXQMLT	TXQOFTXIF	TXQOFRXIF	TXQFIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX Queue Empty 0: TX Queue not empty 1: TX Queue empty	R
1	TXQFLL	TX Queue Full 0: TX Queue not full 1: TX Queue full	R
2	TXQTXIF	TX Queue TX Interrupt Flag 0: TX Queue interrupt condition not satisfied after a frame TX 1: TX Queue interrupt condition satisfied after a frame TX	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
13:8	TXQMC[13:8]	TX Queue Message Count Number of messages in the TX Queue.	R
15:14	—	These bits are read as 0. The write value should be 0.	R/W
16	TXQFIF	TXQ Full Interrupt Flag When TXQ is in full status, an interrupt is set.	R/W
17	TXQOFRXIF	TXQ One Frame Reception Interrupt Flag When TXQ receives one frame, an interrupt is set.	R/W
18	TXQOFTXIF	TXQ One Frame Transmission Interrupt Flag When one frame transmits from TXQ, an interrupt is set.	R/W

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMLT位（TXQ消息丢失）

如果TX队列被禁止，TXQMLT位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当TXQueue的GW模式下发生消息丢失时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

32.2.61 CFDTXQSTS2n：TX队列状态寄存器2n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x10E0 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	TXQMLT	TXQOFTXIF	TXQOFRXIF	TXQFIF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX队列空 0：TX队列不为空1：TX队列为空	R
1	TXQFLL	TX队列已满 0：TX队列未满1：TX队列已满	R
2	TXQTXIF	TX队列TX中断标志 0：一帧TX后不满足TX队列中断条件1：一帧TX后满足TX队列中断条件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
13:8	TXQMC[13:8]	TX队列消息计数 TX队列中的消息数。	R
15:14	—	这些位被读取为0。写入值应为0。	R/W
16	TXQFIF	TXQ完全中断标志 当TXQ处于满状态时，会设置一个中断。	R/W
17	TXQOFRXIF	TXQ一帧接收中断标志 当TXQ接收到一帧时，设置中断。	R/W
18	TXQOFTXIF	TXQ一帧传输中断标志 当从TXQ发送一帧时，设置中断。	R/W

Bit	Symbol	Function	R/W
19	TXQMLT	TXQ Message Lost 0: No message lost in TXQ 1: TXQ message lost	R/W
31:20	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Status Registers 2n (n = 0, 1) show the status of the TX Queue of corresponding CAN Channel.

TXQEMP bit (TX Queue Empty)

The TXQEMP bit is set automatically when the TX Queue is disabled or no messages are stored in the TX Queue.

This bit is cleared automatically when the first message to be transmitted is stored in the TX Queue.

This bit is set automatically when:

- The last message is transmitted from the TX Queue
- The related CAN-FD channel is in CH_RESET mode.

TXQFLL bit (TX Queue Full)

The TXQFLL bit is set automatically when the number of CAN messages stored in the TX Queue matches the configured TX Queue depth

This bit is cleared automatically when:

- The number of CAN messages stored in the TX Queue is less than the configured TX Queue depth
- The related CAN-FD channel is in CH_RESET mode.

TXQTXIF bit (TX Queue TX Interrupt Flag)

The TXQTXIF bit is not cleared automatically if the TX Queue is disabled.

This bit is set automatically when the configured interrupt condition is satisfied for the TX Queue.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of the TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMC[13:8] bits (TX Queue Message Count)

The TXQMC[13:8] bits show the number of CAN messages in the TX Queue.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

TXQFIF bit (TXQ Full Interrupt Flag)

The TXQFIF bit is not cleared automatically if the TX Queue is disabled.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of the TX Queue.

Only in Gateway mode (CFDTXQCC2n.TXQGWE = 1) that this bit is set automatically when the TX Queue enters a buffer full status.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

The bit is cleared:

Bit	Symbol	Function	R/W
19	TXQMLT	TXQ消息丢失 0：TXQ中没有消息丢失1： TXQ消息丢失	R/W
31:20	—	这些位被读取为0。写入值应为0。	R/W

TX队列状态寄存器2n(n=0 1)显示相应CAN通道的TX队列状态。

TXQEMP位（TX队列空）

当TX队列被禁用或没有消息存储在TX队列中时，TXQEMP位自动置位。

当要发送的第一个消息存储在TX队列中时，该位会自动清零。

该位在以下情况下自动设置：

●最后一条消息是从TXQueue发送的

●相关的CAN-FD通道处于CH_RESET模式。

TXQFLL位（TX队列已满）

当存储在TX队列中的CAN报文数量与配置的匹配时，自动设置TXQFLL位
TX队列深度

该位在以下情况下自动清零：

●TXQueue中存储的CAN报文数量小于配置的TXQueue深度

●相关的CAN-FD通道处于CH_RESET模式。

TXQTXIF位（TX队列TX中断标志 ）

如果TX队列被禁止，TXQTXIF位不会自动清零。

当为TX队列配置的中断条件满足时，该位自动置位。

停止TX队列时，应在禁用TXQE并检查TX的空状态后清除该位
Queue.

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMC[13:8]位（TX队列消息计数）

TXQMC[13:8]位显示TX队列中的CAN报文数。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

TXQFIF位（TXQ满中断标志）

如果TX队列被禁止，TXQFIF位不会自动清零。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

停止TX队列时，应在禁用TXQE并检查TX的空状态后清除该位
Queue.

只有在网关模式（CFDTXQCC2n.TXQGWE=1）下，当TX队列进入缓冲区满状态时，该位才会自动设置。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

该位被清除：

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQOFRXIF bit (TXQ One Frame Reception Interrupt Flag)

The TXQOFRXIF bit is not cleared automatically if the TX Queue is disabled.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.
When receiving data is stored in the TX Queue in Gateway mode, this bit is set automatically.

This function can only be used in Gateway mode of the TX queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared.
Other bits remain 1. Writing 1 has no effect.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQOFTXIF bit (TXQ One Frame Transmission Interrupt Flag)

The TXQOFTXIF bit is not cleared automatically if the TX Queue is disabled.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.
When transmission is successful in the TX Queue, this bit is set automatically.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared.
Other bits remain 1. Writing 1 has no effect.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMLT bit (TXQ Message Lost)

The TXQMLT bit is not cleared automatically if the TX Queue is disabled.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.
When a message lost occurs in Gateway mode of the TX Queue, this bit is set automatically.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared.
Other bits remain 1. Writing 1 has no effect.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

32.2.62 CFDTXQSTS3n : TX Queue Status Registers 3n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1140 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIF	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQOFRXIF位（TXQ一帧接收中断标志）

如果TX队列被禁止，TXQOFRXIF位不会自动清零。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当接收数据在网关模式下存储在TX队列中时，该位自动设置。

此功能只能在TX队列的网关模式下使用。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQOFTXIF位（TXQ一帧发送中断标志）

如果TX队列被禁止，TXQOFTXIF位不会自动清零。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当TXQueue中的传输成功时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMLT位（TXQ消息丢失）

如果TX队列被禁止，TXQMLT位不会自动清零。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

停止TX队列时，应在禁用TXQE并检查TX队列的空状态后清除该位。
当TXQueue的网关模式下发生消息丢失时，该位自动置位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

32.2.62 CFDTXQSTS3n：TX队列状态寄存器3n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1140 + 0x04 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQOFTXIF	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TXQMC[13:8]						—	—	—	—	—	TXQTXIF	TXQFLL	TXQEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	TXQEMP	TX Queue Empty 0: TX Queue not empty 1: TX Queue empty	R
1	TXQFLL	TX Queue Full 0: TX Queue not full 1: TX Queue full	R
2	TXQTXIF	TX Queue TX Interrupt Flag 0: TX Queue interrupt condition not satisfied after a frame TX 1: TX Queue interrupt condition satisfied after a frame TX	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
13:8	TXQMC[13:8]	TX Queue Message Count Number of messages in the TX Queue	R
17:14	—	These bits are read as 0. The write value should be 0.	R/W
18	TXQOFTXIF	TXQ One Frame Transmission Interrupt Flag When one frame transmits from TXQ, an interrupt is set.	R/W
31:19	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Status Registers 3n (n = 0, 1) show the status of the TX Queue of corresponding CAN Channel.

TXQEMP bit (TX Queue Empty)

The TXQEMP bit is cleared automatically when the first message to be transmitted is stored in the TX Queue.

This bit is set automatically when:

- The TX Queue is disabled or no messages are stored in the TX Queue
- The last message is transmitted from the TX Queue
- The related CAN-FD channel is in CH_RESET mode.

TXQFLL bit (TX Queue Full)

The TXQFLL bit is set automatically when the number of CAN messages stored in the TX Queue matches the configured TX Queue depth.

This bit is cleared automatically when:

- The number of CAN messages stored in the TX Queue is less than the configured TX Queue depth
- The related CAN-FD channel is in CH_RESET mode.

TXQTXIF bit (TX Queue TX Interrupt Flag)

The TXQTXIF bit is not cleared automatically if the TX Queue is disabled.

This bit is set automatically when the configured interrupt condition is satisfied for the TX Queue.

When stopping TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of TX Queue.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

TXQMC[13:8] bits (TX Queue Message Count)

The TXQMC[13:8] bits show the number of CAN messages in the TX Queue.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

Bit	Symbol	Function	R/W
0	TXQEMP	TX队列空 0：TX队列不为空1：TX队列为空	R
1	TXQFLL	TX队列已满 0：TX队列未满1：TX队列已满	R
2	TXQTXIF	TX队列TX中断标志 0：一帧TX后不满足TX队列中断条件1：一帧TX后满足TX队列中断条件	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
13:8	TXQMC[13:8]	TX队列消息计数 TX队列中的消息数	R
17:14	—	这些位被读取为0。写入值应为0。	R/W
18	TXQOFTXIF	TXQ一帧传输中断标志 当从TXQ发送一帧时，设置中断。	R/W
31:19	—	这些位被读取为0。写入值应为0。	R/W

TX队列状态寄存器3n(n=0 1)显示相应CAN通道的TX队列状态。

TXQEMP位（TX队列空）

当要发送的第一个消息存储在TX队列中时，TXQEMP位会自动清零。

该位在以下情况下自动设置：

●TXQueue被禁用或TXQueue中没有消息存储

●最后一条消息是从TXQueue发送的

●相关的CAN-FD通道处于CH_RESET模式。

TXQFLL位（TX队列已满）

当存储在TX队列中的CAN报文数量与配置的匹配时，自动设置TXQFLL位
TX队列深度。

该位在以下情况下自动清零：

●TXQueue中存储的CAN报文数量小于配置的TXQueue深度

●相关的CAN-FD通道处于CH_RESET模式。

TXQTXIF位（TX队列TX中断标志 ）

如果TX队列被禁止，TXQTXIF位不会自动清零。

当为TX队列配置的中断条件满足时，该位自动置位。

停止TXQueue时，应在禁用TXQE并检查TXQueue的空状态后清除该位。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

TXQMC[13:8]位（TX队列消息计数）

TXQMC[13:8]位显示TX队列中的CAN报文数。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

TXQOFTXIF bit (TXQ One Frame Transmission Interrupt Flag)

The TXQOFTXIF bit is not cleared automatically if the TX Queue is disabled. When transmission is successful in the TX Queue, this bit is set automatically.

You cannot write to this bit when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode. When stopping the TX Queue, this bit should be cleared, after disabling TXQE and checking an empty state of the TX Queue.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1. Writing 1 has no effect.

The bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

32.2.63 CFDTXQPCTR0n : TX Queue Pointer Control Registers 0n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1040 + 0x04 × n

Bit position:	31																								7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers 0n (n = 0, 1) are used to confirm storage of a full message in the corresponding TX Queue buffers.

TXQPC[7:0] bits (TX Queue Pointer Control)

When the value 0xFF is written to the TXQPC[7:0] bits, the write pointer of the corresponding TX Queue buffer is updated and a transmit request is initiated for this message.

The read value from these bits is always 0x00. Do not write to the FIFO control registers when DMA is enabled.

You cannot write to these bits when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

Only write 0xFF to this register when:

- The corresponding TX Queue is enabled and not full
- The Common FIFO is enabled and is not configured in GW mode.

32.2.64 CFDTXQPCTR1n : TX Queue Pointer Control Registers 1n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x10A0 + 0x04 × n

Bit position:	31																								7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W

TXQOFTXIF位（TXQ一帧发送中断标志）

如果TX队列被禁止，TXQOFTXIF位不会自动清零。当TX传输成功时
队列，这个位是自动设置的。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入该位。当停止
TXQueue，在禁用TXQE并检查TXQueue的空状态后，应清除该位。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。写1无效。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

32.2.63 CFDTXQPCTR0n：TX队列指针控制寄存器0n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1040 + 0x04 × n

Bit position:	31																								7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX队列指针控制 将写入指针递增到相应通道中的TX队列缓冲区	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列指针控制寄存器0n(n=0 1)用于确认在相应的TX中存储完整消息
队列缓冲区。

TXQPC[7:0]位（TX队列指针控制）

当值0xFF写入TXQPC[7:0]位时，相应的TX队列缓冲区的写指针被更新，并为此消息启动发送请求。

从这些位读取的值始终为0x00。启用DMA时不要写入FIFO控制寄存器。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入这些位。

仅在以下情况下向该寄存器写入0xFF：

●对应的TXQueue已启用且未满

●CommonFIFO已使能，GW模式下未配置。

32.2.64 CFDTXQPCTR1n：TX队列指针控制寄存器1n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x10A0 + 0x04 × n

Bit position:	31																								7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQPC[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX队列指针控制 将写入指针递增到相应通道中的TX队列缓冲区	W

Bit	Symbol	Function	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers 1n (n = 0, 1) are used to confirm storage of a full message in the corresponding TX Queue buffers.

TXQPC[7:0] bits (TX Queue Pointer Control)

When the value 0xFF is written to the TXQPC[7:0] bits, the write pointer of the corresponding TX Queue buffer is updated and a transmit request is initiated for this message.

The read value from these bits is always 0x00.

Only write 0xFF to this register when:

- The corresponding TX Queue is enabled and not full
- The Common FIFO is enabled and is not configured in GW mode.

32.2.65 CFDTXQPCTR2n : TX Queue Pointer Control Registers 2n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1100 + 0x04 × n

Bit position:	31 … 7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TXQPC[7:0]
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers 2n (n = 0, 1) are used to confirm storage of a full message in the corresponding TX Queue buffers.

TXQPC[7:0] bits (TX Queue Pointer Control)

When the value 0xFF is written to the TXQPC[7:0] bits, the write pointer of the corresponding TX Queue buffer is updated and a transmit request is initiated for this message.

The read value from these bits is always 0x00.

You cannot write to these bits when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

Only write 0xFF to this register when:

- The corresponding TX Queue is enabled and not full
- The Common FIFO is enabled and is not configured in GW mode.

32.2.66 CFDTXQPCTR3n : TX Queue Pointer Control Registers 3n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1160 + 0x04 × n

Bit position:	31 … 7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TXQPC[7:0]
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列指针控制寄存器1n(n=0 1)用于确认在相应的TX中存储完整消息
队列缓冲区。

TXQPC[7:0]位（TX队列指针控制）

当值0xFF写入TXQPC[7:0]位时，相应的TX队列缓冲区的写指针被更新，并为此消息启动发送请求。

从这些位读取的值始终为0x00。

仅在以下情况下向该寄存器写入0xFF：

●对应的TXQueue已启用且未满

●CommonFIFO已使能，GW模式下未配置。

32.2.65 CFDTXQPCTR2n：TX队列指针控制寄存器2n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1100 + 0x04 × n

Bit position:	31 … 7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TXQPC[7:0]
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX队列指针控制 将写入指针递增到相应通道中的TX队列缓冲区	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列指针控制寄存器2n(n=0 1)用于确认在相应的TX中存储完整消息
队列缓冲区。

TXQPC[7:0]位（TX队列指针控制）

当值0xFF写入TXQPC[7:0]位时，相应的TX队列缓冲区的写指针被更新，并为此消息启动发送请求。

从这些位读取的值始终为0x00。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入这些位。

仅在以下情况下向该寄存器写入0xFF：

●对应的TXQueue已启用且未满

●CommonFIFO已使能，GW模式下未配置。

32.2.66 CFDTXQPCTR3n：TX队列指针控制寄存器3n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1160 + 0x04 × n

Bit position:	31 … 7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TXQPC[7:0]
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX Queue Pointer Control Increments the write pointer to the TX Queue buffer in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Pointer Control Registers 3n (n = 0, 1) are used to confirm storage of a full message in the corresponding TX Queue buffers.

TXQPC[7:0] bits (TX Queue Pointer Control)

When the value 0xFF is written to the TXQPC[7:0] bits, the write pointer of the corresponding TX Queue buffer is updated and a transmit request is initiated for this message.

The read value from these bits is always 0x00. Do not write to the FIFO control registers when DMA is enabled.

You cannot write to these bits when the related CAN-FD channel is in CH_SLEEP or CH_RESET mode.

Only write 0xFF to this register when the corresponding TX Queue is enabled and not full.

32.2.67 CFDTXQESTS : TX Queue Empty Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1180

Bit position:	31	…	8	7	…	0
Bit field:	—	…	—	TXQxEMP[7:0]		
Value after reset:	0	…	0	1	…	1

Bit	Symbol	Function	R/W
7:0	TXQxEMP[7:0]	TXQ Empty Status 0: TXQ not empty 1: TXQ empty	R
31:8	—	These bits are read as 0.	R

TX Queue Empty Status Register shows the status of the empty bits of the TXQ buffers.

TXQxEMP (x = (n+1) * TXQ Number = 0 to (((n+1)*4 -1)) bits (TXQ Empty Status)

Each bit is set automatically when the corresponding bit is set in the TX Queue Empty Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue Empty Status Register.

This bit is set when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

Bit	Symbol	Function	R/W
7:0	TXQPC[7:0]	TX队列指针控制 将写入指针递增到相应通道中的TX队列缓冲区	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列指针控制寄存器3n(n=0 1)用于确认在相应的TX中存储完整消息
队列缓冲区。

TXQPC[7:0]位（TX队列指针控制）

当值0xFF写入TXQPC[7:0]位时，相应的TX队列缓冲区的写指针被更新，并为此消息启动发送请求。

从这些位读取的值始终为0x00。启用DMA时不要写入FIFO控制寄存器。

当相关CAN-FD通道处于CH_SLEEP或CH_RESET模式时，您无法写入这些位。

仅当相应的TXQueue使能且未满时才向该寄存器写入0xFF。

32.2.67 CFDTXQESTS:TX队列空状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1180

Bit position:	31	…	8	7	…	0
Bit field:	—	…	—	TXQxEMP[7:0]		
重置后的值：	0	…	0	1	…	1

Bit	Symbol	Function	R/W
7:0	TXQxEMP[7:0]	TXQ空状态 0：TXQ不为空1： TXQ为空	R
31:8	—	这些位读为0。	R

TXQueueEmptyStatusRegister显示TXQ缓冲区的空位状态。

TXQxEMP(x=(n+1)*TXQNumber=0到(((n+1)*4−1))位（TXQ空状态）

当在TX队列空状态寄存器中设置相应位时，每个位都会自动设置。

当TX队列空状态寄存器中的相应位被清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，该位置位。

位位置	对应的TX队列
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

32.2.68 CFDTXQFISTS : TX Queue Full Interrupt Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1184

Bit position:	31																								7	6	4	3	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1FULL[2:0]		—	TXQ0FULL[2:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TXQ0FULL[2:0]	TXQ Full Interrupt Status for Channel 0 0: TXQ full interrupt is not set 1: TXQ full interrupt is set	R
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	TXQ1FULL[2:0]	TXQ Full Interrupt Status for Channel 1 0: TXQ full interrupt is not set 1: TXQ full interrupt is set	R
31:7	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Full Interrupt Status Register shows the status of the full interrupt bits of the TXQ buffers.

TXQxFULL (x = 0, 1) bits (TXQ Full Interrupt Status)

Each bit is set automatically when the corresponding bit is set in the TX Queue Full Interrupt Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue Full Interrupt Status Register.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Reserved
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Reserved

32.2.69 CFDTXQMSTS : TX Queue Message Lost Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1188

Bit position:	31	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1ML[2:0]	—	TXQ0ML[2:0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TXQ0ML[2:0]	TXQ Message Lost Status for Channel 0 0: TXQ message lost flag is not set 1: TXQ message lost flag is set	R
3	—	This bit is read as 0. The write value should be 0.	R/W

32.2.68 CFDTXQFISTS:TX队列满中断状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1184

Bit position:	31																								7	6	4	3	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1FULL[2:0]		—	TXQ0FULL[2:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TXQ0FULL[2:0]	通道0的TXQ完全中断状态 0：未设置TXQ全中断1：设置了TXQ全中断	R
3	—	该位读取为0。写入值应为0。	R/W
6:4	TXQ1FULL[2:0]	通道1的TXQ完全中断状态 0：未设置TXQ全中断1：设置了TXQ全中断	R
31:7	—	这些位被读取为0。写入值应为0。	R/W

TX队列满中断状态寄存器显示TXQ缓冲区的满中断位的状态。

TXQxFULL(x=0 1)位（TXQ完全中断状态）

当在TX队列满中断状态寄存器中设置相应位时，每个位都会自动设置。

当TX队列满中断状态寄存器中的相应位被清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，该位清零。

位位置	对应的TX队列
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Reserved
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Reserved

32.2.69 CFDTXQMSTS:TX队列消息丢失状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1188

Bit position:	31	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1ML[2:0]	—	TXQ0ML[2:0]
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TXQ0ML[2:0]	通道0的TXQ消息丢失状态 0：未设置TXQ消息丢失标志1：设置了TXQ消息丢失标志	R
3	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
6:4	TXQ1ML[2:0]	TXQ Message Lost Status for Channel 1 0: TXQ message lost flag is not set 1: TXQ message lost flag is set	R
31:7	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Message Lost Status Register shows the status of the message lost bits of the TXQ buffers.

TXQxML (x = 0, 1) bits (TXQ message lost Status)

Each bit is set automatically when the corresponding bit is set in the TX Queue Message Lost Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue Message Lost Status Register.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Reserved
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Reserved

32.2.70 CFDTXQISTS : TX Queue Interrupt Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1190

Bit position:	31	…	8	7	6	5	4	3	2	1	0
Bit field:	—	…	—	TXQ1ISF[3:0]				TXQ0ISF[3:0]			
Value after reset:	0	…	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TXQ0ISF[3:0]	TXQ Interrupt Status Flag for Channel 0 0: TXQ Interrupt flag is not set 1: TXQ Interrupt flag is set	R
7:4	TXQ1ISF[3:0]	TXQ Interrupt Status Flag for Channel 1 0: TXQ Interrupt flag is not set 1: TXQ Interrupt flag is set	R
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue Interrupt Status Register shows the status of the interrupt flag of the TXQ buffers.

TXQxISF[3:0] (x = 0, 1) bits (TXQ Interrupt Status Flag)

Each bit is set automatically when the corresponding bit is set in the TX Queue Interrupt Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue Interrupt Status Register.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0

Bit	Symbol	Function	R/W
6:4	TXQ1ML[2:0]	通道1的TXQ消息丢失状态 0：未设置TXQ消息丢失标志1：设置了TXQ消息丢失标志	R
31:7	—	这些位被读取为0。写入值应为0。	R/W

TX队列消息丢失状态寄存器显示TXQ缓冲区的消息丢失位的状态。

TXQxML(x=0 1)位（TXQ消息丢失状态）

当在TXQueueMessageLostStatusRegister中设置相应位时，每个位都会自动设置。

当TXQueueMessageLostStatusRegister中的相应位清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，该位清零。

位位置	对应的TX队列
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Reserved
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Reserved

32.2.70 CFDTXQISTS：TX队列中断状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1190

Bit position:	31	…	8	7	6	5	4	3	2	1	0
Bit field:	—	…	—	TXQ1ISF[3:0]				TXQ0ISF[3:0]			
重置后的值：	0	…	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TXQ0ISF[3:0]	通道0的TXQ中断状态标志 0：未设置TXQ中断标志 1：设置了TXQ中断标志	R
7:4	TXQ1ISF[3:0]	通道1的TXQ中断状态标志 0：未设置TXQ中断标志 1：设置了TXQ中断标志	R
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列中断状态寄存器显示TXQ缓冲区的中断标志的状态。

TXQxISF[3:0](x=0 1)位（TXQ中断状态标志）

当TX队列中断状态寄存器中的相应位被设置时，每个位都会自动设置。

当TX队列中断状态寄存器中的相应位被清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，该位清零。

位位置	对应的TX队列
0	Channel 0 TX Queue0

Bit position	Corresponding TX Queue
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

32.2.71 CFDTXQOFTISTS : TX Queue One Frame TX Interrupt Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1194

Bit position:	31																						8	7		4	3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1OFTISF[3:0]			TXQ0OFTISF[3:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TXQ0OFTISF[3:0]	TXQ One Frame TX Interrupt Status Flag for Channel 0 0: TXQ One Frame TX Interrupt flag is not set 1: TXQ One Frame TX Interrupt flag is set	R
7:4	TXQ1OFTISF[3:0]	TXQ One Frame TX Interrupt Status Flag for Channel 1 0: TXQ One Frame TX Interrupt flag is not set 1: TXQ One Frame TX Interrupt flag is set	R
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue One Frame TX Interrupt Status Register shows the status of the One Frame TX Interrupt flag of the TXQ buffers.

TXQxOFTISF[3:0] (x = 0, 1) bits (TXQ One Frame TX Interrupt Status Flag)

Each bit is set automatically when the corresponding bit is set in the TX Queue One Frame TX Interrupt Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue One Frame TX Interrupt Status Register.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

位位置	对应的TX队列
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

32.2.71 CFDTXQOFTISTS:TX队列一帧TX中断状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1194

Bit position:	31																						8	7		4	3		0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1OFTISF[3:0]			TXQ0OFTISF[3:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TXQ0OFTISF[3:0]	TXQ通道0的一帧TX中断状态标志 0：TXQ一帧发送中断标志未置位1：TXQ一帧发送中断标志置位	R
7:4	TXQ1OFTISF[3:0]	通道1的TXQ一帧TX中断状态标志 0：TXQ一帧发送中断标志未置位1：TXQ一帧发送中断标志置位	R
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX队列一帧TX中断状态寄存器显示TXQ缓冲区的一帧TX中断标志 的状态。

TXQxOFTISF[3:0](x=0 1)位（TXQ一帧TX中断状态标志）

当在TXQueueOneFrameTX中断状态寄存器中设置相应位时，每个位都会自动设置。

当TXQueue一帧TX中断状态中的相应位被清零时，每个位都会自动清零
Register.

当CAN-FD模块处于GL_RESET模式时，该位清零。

位位置	对应的TX队列
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

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32.2.72 CFDTXQOFRISTS : TX Queue One Frame RX Interrupt Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1198

Bit position:	31																								6	4	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1OFRISF[2:0]		—	TXQ0OFRISF[2:0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TXQ0OFRISF[2:0]	TXQ One Frame RX Interrupt Status Flag 0: TXQ One Frame RX Interrupt flag is not set 1: TXQ One Frame RX Interrupt flag is set	R
3	—	This bit is read as 0. The write value should be 0.	R/W
6:4	TXQ1OFRISF[2:0]	TXQ One Frame RX Interrupt Status Flag 0: TXQ One Frame RX Interrupt flag is not set 1: TXQ One Frame RX Interrupt flag is set	R
31:7	—	These bits are read as 0. The write value should be 0.	R/W

The TX Queue One Frame RX Interrupt Status Register shows the status of the One Frame RX Interrupt flag of the TXQ buffers.

TXQxOFRISF[2:0] (x = 0, 1) bits (TXQ One Frame RX Interrupt Status Flag)

Each bit is set automatically when the corresponding bit is set in the TX Queue One Frame RX Interrupt Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue One Frame RX Interrupt Status Register.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Reserved
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Reserved

32.2.73 CFDTXQFSTS : TX Queue Full Status Register

Base address: CANFD = 0x400B_0000

Offset address: 0x119C

Bit position:	31																								8	7	4	3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1FSF[3:0]			TXQ0FSF[3:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

32.2.72 CFDTXQOFRISTS:TX队列一帧RX中断状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1198

Bit position:	31																								6	4	2	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1OFRISF[2:0]		—	TXQ0OFRISF[2:0]
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	TXQ0OFRISF[2:0]	TXQ一帧接收中断状态标志 0：未设置TXQ一帧RX中断标志 1：设置了TXQ一帧RX中断标志	R
3	—	该位读取为0。写入值应为0。	R/W
6:4	TXQ1OFRISF[2:0]	TXQ一帧接收中断状态标志 0：未设置TXQ一帧RX中断标志 1：设置了TXQ一帧RX中断标志	R
31:7	—	这些位被读取为0。写入值应为0。	R/W

TX队列一帧RX中断状态寄存器显示TXQ缓冲区的一帧RX中断标志 的状态。

TXQxOFRISF[2:0](x=0 1)位（TXQ一帧RX中断状态标志）

当TXQueueOneFrameRX中断状态寄存器中的相应位置位时，每个位都会自动设置。

当TXQueue一帧RX中断状态中的相应位被清零时，每个位都会自动清零

Register.

当CAN-FD模块处于GL_RESET模式时，该位清零。

位位置	对应的TX队列
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Reserved
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Reserved

32.2.73 CFDTXQFSTS：TX队列满状态寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x119C

Bit position:	31																								8	7	4	3	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQ1FSF[3:0]			TXQ0FSF[3:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	TXQ0FSF[3:0]	TXQ Full Status Flag for Channel 0 0: TXQ Full flag is not set 1: TXQ Full flag is set	R
7:4	TXQ1FSF[3:0]	TXQ Full Status Flag for Channel 1 0: TXQ Full flag is not set 1: TXQ Full flag is set	R
31:8	—	These bits are read as 0.	R

The TX Queue Full Status Register shows the status of the Full Status flag bits of the TXQ buffers.

TXQxFSF[31:0] (x = 0, 1) bits (TXQ Full Status Flag)

Each bit is set automatically when the corresponding bit is set in the TX Queue Full Status Register.

Each bit is cleared automatically when the corresponding bit is cleared in the TX Queue Full Status Register.

This bit is cleared when the CAN-FD module is in GL_RESET mode.

Bit position	Corresponding TX Queue
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

32.2.74 CFDTHLCCn : TX History List Configuration/Control Register n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1200 + 0x04 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	THLD GE	THLD TE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	THLE	TX History List Enable 0: TX History List disabled 1: TX History List enabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	THLIE	TX History List Interrupt Enable 0: TX History List Interrupt disabled 1: TX History List Interrupt enabled	R/W
9	THLIM	TX History List Interrupt Mode 0: Interrupt generated if TX History List level reaches ¾ of the TX History List depth 1: Interrupt generated for every successfully stored entry	R/W

Bit	Symbol	Function	R/W
3:0	TXQ0FSF[3:0]	通道0的TXQ完整状态标志 0：未设置TXQ满标志1： 设置了TXQ满标志	R
7:4	TXQ1FSF[3:0]	通道1的TXQ完整状态标志 0：未设置TXQ满标志1： 设置了TXQ满标志	R
31:8	—	这些位读为0。	R

TX队列满状态寄存器显示TXQ缓冲区的满状态标志位的状态。

TXQxFSF[31:0](x=0 1)位（TXQ满状态标志）

当在TX队列满状态寄存器中设置相应位时，每个位都会自动设置。

当TX队列满状态寄存器中的相应位清零时，每个位都会自动清零。

当CAN-FD模块处于GL_RESET模式时，该位清零。

位位置	对应的TX队列
0	Channel 0 TX Queue0
1	Channel 0 TX Queue1
2	Channel 0 TX Queue2
3	Channel 0 TX Queue3
4	Channel 1 TX Queue0
5	Channel 1 TX Queue1
6	Channel 1 TX Queue2
7	Channel 1 TX Queue3

32.2.74 CFDTHLCCn:TX历史列表配置控制寄存器n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1200 + 0x04 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	THLD GE	THLD TE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	THLE	TX历史列表启用 0：禁用TX历史列表1：启 用TX历史列表	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	THLIE	TX历史列表中断使能 0：禁止发送历史列表中断1：允许 发送历史列表中断	R/W
9	THLIM	TX历史列表中断模式 0：如果TX历史列表级别达到TX历史列表深度的3/4，则生成中断1：为每个成功存储 的条目生成中断	R/W

Bit	Symbol	Function	R/W
10	THLDTE	TX History List Dedicated TX Enable 0: TX FIFO + TX Queue 1: Flat TX MB + TX FIFO + TX Queue	R/W
11	THLDGE	TX History List Dedicated Gateway Enable 0: Not dedicated Gateway FIFO + Gateway TX Queue 1: Dedicated Gateway FIFO + Gateway TX Queue	R/W
31:12	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Configuration/Control Register n (n = 0, 1) configures the TX History List functions.

THLE bit (TX History List Enable)

The THLE bit enables the TX History List buffer when it is set.

You cannot write to this bit when the related CAN-FD channel is in CH_RESET or CH_SLEEP mode.

This bit is cleared automatically when the related CAN-FD channel is in CH_RESET mode.

THLIE bit (TX History List Interrupt Enable)

The THLIE bit enables the generation of the TX History List interrupt when it is set.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

THLIM bit (TX History List Interrupt Mode)

The THLIM bit selects the interrupt generation condition for the FIFO.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode.

THLDTE bit (TX History List Dedicated TX Enable)

The THLDTE bit selects the condition for storing an entry in the TX History List after successful transmission.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode.

THLDGE bit (TX History List Dedicated Gateway Enable)

The THLDGE bit selects the condition for storing an entry in the TX History List after successful transmission.

You cannot write to this bit when the CAN-FD module is in GL_SLEEP mode.

Do not write to this bit when the CAN-FD module is in GL_HALT or GL_OPERATION mode.

32.2.75 CFDTHLSTSn : TX History List Status Register n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1220 + 0x04 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	THLMC[5:0]						—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
10	THLDTE	TX历史列表专用TX启用 0：TXFIFO+TX队列1：平坦TXMB+TXFIFO+TX队列	R/W
11	THLDGE	TX历史列表专用网关启用 0：非专用网关FIFO+网关TX队列1：专用网关FIFO+网关TX队列	R/W
31:12	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表配置控制寄存器n(n=0 1)配置TX历史列表功能。

THLE位（TX历史列表启用）

THLE位在设置时启用TX历史列表缓冲区。

当相关CAN-FD通道处于CH_RESET或CH_SLEEP模式时，您无法写入该位。

当相关CAN-FD通道处于CH_RESET模式时，该位自动清零。

THLIE位（TX历史列表中断允许）

THLIE位在设置时允许生成TX历史列表中断。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

THLIM位（TX历史列表中断模式）

THLIM位选择FIFO的中断产生条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当CAN-FD模块处于GL_HALT或GL_OPERATION模式时，请勿写入该位。

THLDTE位（TX历史列表专用TX使能）

THLDTE位选择在成功发送后将条目存储在TX历史列表中的条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当CAN-FD模块处于GL_HALT或GL_OPERATION模式时，请勿写入该位。

THLDGE位（TX历史列表专用网关启用）

THLDGE位选择在成功传输后将条目存储在TX历史列表中的条件。

当CAN-FD模块处于GL_SLEEP模式时，您无法写入该位。

当CAN-FD模块处于GL_HALT或GL_OPERATION模式时，请勿写入该位。

32.2.75 CFDTHLSTSn:TX历史列表状态寄存器n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1220 + 0x04 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	THLMC[5:0]						—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	THLEMP	TX History List Empty 0: TX History List not empty 1: TX History List empty	R
1	THLFLL	TX History List Full 0: TX History List not full 1: TX History List full	R
2	THLELT	TX History List Entry Lost 0: No entry lost in TX History List 1: TX History List entry Lost	R/W
3	THLIF	TX History List Interrupt Flag 0: TX History List interrupt condition not satisfied 1: TX History List interrupt condition satisfied	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W
13:8	THLMC[5:0]	TX History List Message Count Number of messages stored in TX History List	R
31:14	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Status register shows the status of data stored in the TX History List buffer.

THLEMP bit (TX History List Empty)

The THLEMP bit is set automatically when the CPU has read all the entries from the TX History List buffer.

This bit is cleared automatically when the first entry is stored to the TX History List.

This bit is set automatically when:

- TX History List is disabled
- The related CAN-FD channel is in CH_RESET mode.

THLFLL bit (TX History List Full)

The THLFLL bit is set automatically when the number of entries in the TX History List buffer matches the TX History List depth.

Each TX History List can store up to 32 entries (each channel has a dedicated TX History List).

This bit is cleared automatically when:

- The number of entries in the TX History List buffer is less than the TX History List depth
- The TX History List is disabled
- The related CAN-FD channel is in CH_RESET mode.

THLELT bit (TX History List Entry Lost)

The THLELT bit is set when a new entry cannot be stored because the related TX History List buffer is already full.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode. Writing 1 has no effect.

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

THLIF bit (TX History List Interrupt Flag)

The THLIF bit is set when the configured interrupt condition is satisfied.

Only write to this bit when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode. Writing 1 has no effect.

Bit	Symbol	Function	R/W
0	THLEMP	TX历史列表空 0：TX历史列表不为空1：TX 历史列表为空	R
1	THLFLL	TX历史列表完整 0：TX历史列表未满1：T X历史列表已满	R
2	THLELT	TX历史列表条目丢失 0：TX历史列表中没有条目丢失1 ：TX历史列表条目丢失	R/W
3	THLIF	TX历史列表中断标志 0：不满足TX历史列表中断条件1：满足TX历史列 表中断条件	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W
13:8	THLMC[5:0]	TX历史列表消息计数 TX历史列表中存储的信息数量	R
31:14	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表状态寄存器显示TX历史列表缓冲区中存储的数据的状态。

THLEMP位（TX历史列表空）

当CPU从TXHistoryList缓冲区读取所有条目时，THLEMP位自动置位。

当第一个条目存储到TX历史列表时，该位自动清零。

该位在以下情况下自动设置：

●TX历史列表被禁用

●相关的CAN-FD通道处于CH_RESET模式。

THLFLL位（TX历史列表已满）

当TX历史列表缓冲区中的条目数与TX历史列表深度匹配时，自动设置THLFLL位。

每个TX历史列表最多可以存储32个条目（每个通道都有一个专用的TX历史列表）。

该位在以下情况下自动清零：

●TX历史列表缓冲区中的条目数小于TX历史列表深度

●TX历史列表被禁用

●相关的CAN-FD通道处于CH_RESET模式。

THLELT位（TX历史列表条目丢失）

当由于相关的TX历史列表缓冲区已满而无法存储新条目时，将设置THLELT位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。写1无效。

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

THLIF位（TX历史列表中断标志）

当配置的中断条件满足时，THLIF位置位。

仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入该位。写1无效。

Do not use the bit clear instruction to clear this bit. Use the MOV instruction to ensure that only the specified bit is cleared. Other bits remain 1.

This bit is cleared:

- By writing 0 to it
- When the related CAN-FD channel is in CH_RESET mode.

The bit is cleared by writing 0 to it.

This bit is automatically cleared in CH_RESET mode.

THLMC[5:0] bits (TX History List Message Count)

The THLMC[5:0] bits show the number of transmitted messages stored in the TX History List.

These bits are cleared automatically when the related CAN-FD channel is in CH_RESET mode.

32.2.76 CFDTHLACC0n : TX History List Access Registers 0 (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x8000 + 0x08 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TGW	—	—	—	—	—	BN[6:0]							BT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	BT[2:0]	Buffer Type 0 0 1: Flat TX message buffer 0 1 0: TX FIFO message buffer number and gateway FIFO message number 1 0 0: TX Queue message buffer number	R
9:3	BN[6:0]	Buffer Number Number of the message buffer	R
14:10	—	These bits are read as 0. The write value should be 0.	R
15	TGW	Transmit Gateway Buffer Indication 0: No transmission from gateway 1: Transmission from gateway	R
31:16	TMTS[15:0]	Transmit Timestamp Transmit timestamp value for software drivers	R

The TX History List Access Registers 0 (n = 0, 1) provide access to the entry in the TX History List based on the read timestamp value.

BT[2:0] bits (Buffer Type)

The BT[2:0] bits indicate whether data has been stored following a transmission from a FIFO buffer, a TX Queue or a TX message buffer.

BN[6:0] bits (Buffer Number)

The BN[6:0] bits show the message buffer from which transmission was successfully completed. If a message from a Common FIFO is transmitted, then these bits show the message buffer that is linked to the Common FIFO for transmission.

TGW bit (Transmit Gateway Buffer Indication)

The TGW bit is automatically set to 1 when transmission is completed in GW mode.

不要使用位清除指令清除该位。使用MOV指令确保只清除指定位。
其他位保持1。

该位被清除：

●写入0

●当相关CAN-FD通道处于CH_RESET模式时。

该位通过向其写入0来清除。

该位在CH_RESET模式下自动清零。

THLMC[5:0]位（TX历史列表消息计数）

THLMC[5:0]位显示存储在TX历史列表中的已发送消息的数量。

当相关CAN-FD通道处于CH_RESET模式时，这些位会自动清零。

32.2.76 CFDTHLACC0n：TX历史列表访问寄存器0(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x8000 + 0x08 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMTS[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TGW	—	—	—	—	—	BN[6:0]							BT[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	BT[2:0]	缓冲器类型 001：平坦的TX消息缓冲区010：TXFIFO消息缓冲区号和网关FIFO消息号100 ：TXQueue消息缓冲区号	R
9:3	BN[6:0]	缓冲区号 消息缓冲区的编号	R
14:10	—	这些位被读取为0。写入值应为0。	R
15	TGW	发送网关缓冲区指示 0：网关不发送1：网关发送	R
31:16	TMTS[15:0]	传输时间戳 传输软件驱动程序的时间戳值	R

TX历史列表访问寄存器0(n=0 1)根据读取的时间戳值提供对TX历史列表中条目的访问。

BT[2:0] bits (Buffer Type)

BT[2:0]位指示数据是否已在从FIFO缓冲区、TX队列或TX消息缓冲区传输后存储。

BN[6:0] bits (Buffer Number)

BN[6:0]位显示成功完成传输的消息缓冲区。如果一个消息来自
传输通用FIFO，然后这些位显示链接到通用FIFO以进行传输的消息缓冲区。

TGW位（发送网关缓冲区指示）

在GW模式下传输完成时，TGW位自动设置为1。

TMTS[15:0] bits (Transmit Timestamp)

The TMTS[15:0] bits indicate the timestamp for use by software drivers.

32.2.77 CFDTHLACC1n : TX History List Access Registers 1 (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x8004 + 0x08 × n (n = 0, 1)

Bit position:	31														17	16	15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TIFL[1:0]			TID[15:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TID[15:0]	Transmit ID These bits indicate that message buffer reference ID, TX FIFO reference ID, or AFL pointer field is stored for software drivers.	R
17:16	TIFL[1:0]	Transmit Information Label These bits indicate that message buffer information label, TX FIFO information label, or AFL information label is stored for software drivers.	R
31:18	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Access Registers 1 provide access to entry in the TX History List based on the read pointer value.

TID[15:0] bits (Transmit ID)

The TID[15:0] bits indicate whether the message buffer reference ID (CFDTMFDCTRn.TMPTR) or the TX FIFO reference ID (CFDCFFDCSTSn.CFPTR) is for use by software drivers.

When transmission in GW mode, these bits indicate the AFL pointer field (CFDGAFLP0n.GAFLPTR) instead of the message buffer reference ID (CFDTMFDCTRn.TMPTR).

TIFL[1:0] bits (Transmit Information Label)

The TIFL[1:0] bits indicate whether the message buffer information label (CFDTMFDCTRn.TMIFL) or the TX FIFO information label (CFDCFFDCSTSn.CFIFL) is for use by software drivers.

When transmission in GW mode, these bits indicate the AFL pointer field (CFDGAFLMn.GAFLIFL1 and CFDGAFLP0n.GAFLIFL0) instead of the MB information label (CFDTMFDCTRn.TMIFL).

32.2.78 CFDTHLPCTRn : TX History List Pointer Control Registers n (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1240 + 0x04 × n (n = 0, 1)

Bit position:	31																								7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	THLPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX History List Pointer Control Increments the write pointer to the TX History List in the corresponding channel	W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

The TX History List Pointer Control Registers n (n = 0, 1) are used to increment the read pointer of the TX History List.

TMTS[15:0] bits (Transmit Timestamp)

TMTS[15:0]位指示软件驱动程序使用的时间戳。

32.2.77 CFDTHLACC1n:TX历史列表访问寄存器1(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x8004 + 0x08 × n (n = 0, 1)

Bit position:	31														17	16	15														0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TIFL[1:0]			TID[15:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	TID[15:0]	传输ID 这些位指示为软件驱动程序存储消息缓冲区参考ID、TXFIFO参考ID或AFL指针字段。	R
17:16	TIFL[1:0]	传输信息标签 这些位指示为软件驱动程序存储消息缓冲区信息标签、TXFIFO信息标签或AFL信息标签。	R
31:18	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表访问寄存器1根据读取的指针值提供对TX历史列表中条目的访问。

TID[15:0] bits (Transmit ID)

TID[15:0]位指示消息缓冲区参考ID(CFDTMFDCTRn.TMPTR)还是TXFIFO参考ID(CFDCFFDCSTSn.CFPTR)供软件驱动程序使用。

在GW模式下传输时，这些位指示AFL指针字段(CFDGAFLP0n.GAFLPTR)，而不是消息缓冲区引用ID(CFDTMFDCTRn.TMPTR)。

TIFL[1:0]位（发送信息标签）

TIFL[1:0]位指示消息缓冲区信息标签(CFDTMFDCTRn.TMIFL)或TXFIFO信息标签(CFDCFFDCSTSn.CFIFL)是否供软件驱动程序使用。

在GW模式下传输时，这些位指示AFL指针字段（CFDGAFLMn.GAFLIFL1和CFDGAFLP0n.GAFLIFL0)代替MB信息标签(CFDTMFDCTRn.TMIFL)。

32.2.78 CFDTHLPCTRn:TX历史列表指针控制寄存器n(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1240 + 0x04 × n (n = 0, 1)

Bit position:	31																								7						0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	THLPC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	THLPC[7:0]	TX历史列表指针控制 将写入指针递增到相应通道中的TX历史列表	W
31:8	—	这些位被读取为0。写入值应为0。	R/W

TX历史列表指针控制寄存器n(n=0 1)用于递增TX历史列表的读指针。

THLPC[7:0] bits (TX History List Pointer Control)

When 0xFF is written to the THLPC[7:0] bits, the read pointer of the TX History List is moved to the next TX History List entry address.

The read value from these bits is always 0x00. Only write to these bits when the related CAN-FD channel is in CH_HALT or CH_OPERATION mode.

Only write 0xFF to these registers when the corresponding TX History List is enabled and not empty.

32.2.79 CFDGRSTC : Global SW reset Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1380

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRST	SW Reset 0: Normal state 1: SW reset state	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code These bits control the validity of rewriting of a SRST bit.	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

SRST bit (SW Reset)

When the SRST bit is set, the CAN-FD module is in the same state as hardware reset. When a reset is required, write 1 then write 0 to this bit.

This bit is cleared when the CAN-FD module is in GL_SLEEP mode.

When this bit is cleared, the RAM initialization sequence does not operate. The configuration of RAM is performed by software.

The RAM is not initialized when software reset is performed during the initialization of RAM. Software must perform the initialization of RAM.

KEY[7:0] bits (Key Code)

When 0xC4 is written in the KEY[15:8] bits, a write to the SRST bit is valid.

The read value from these bits is always 0x00.

CFDGRSTC.SRST bit and the CFDGRSTC.KEY bit should be written simultaneously.

THLPC[7:0]位（TX历史列表指针控制）

当0xFF写入THLPC[7:0]位时，TX历史列表的读指针将移动到下一个TX历史列表条目地址。

从这些位读取的值始终为0x00。仅当相关CAN-FD通道处于CH_HALT或CH_OPERATION模式时才写入这些位。

仅当相应的TX历史列表启用且不为空时，才向这些寄存器写入0xFF。

32.2.79 CFDGRSTC:全局软件复位寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1380

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRST	SW Reset 0：正常状态1： 软件复位状态	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码 这些位控制SRST位重写的有效性。	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

SRST bit (SW Reset)

当SRST位置位时，CAN-FD模块处于与硬件复位相同的状态。当需要复位时，先写1然后写0到该位。

当CAN-FD模块处于GL_SLEEP模式时，该位清零。

当该位清零时，RAM初始化序列不工作。RAM的配置由软件执行。

在RAM初始化过程中执行软件复位时，RAM不会被初始化。软件必须执行RAM的初始化。

KEY[7:0] bits (Key Code)

当KEY[15:8]位写入0xC4时，写入SRST位有效。

从这些位读取的值始终为0x00。

CFDGRSTC.SRST位和CFDGRSTC.KEY位应同时写入。

32.2.80 CFDGTSTCFG : Global Test Configuration Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1308

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	RTMPS[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ICBCE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ICBCE[1:0]	Channel n Internal CAN Bus Communication Test Mode Enable 0: Channel n internal CAN bus communication disabled 1: Channel n internal CAN bus communication enabled	R/W
15:2	—	These bits are read as 0. The write value should be 0.	R/W
25:16	RTMPS[9:0]	RAM Test Mode Page Select Select a RAM test mode page	R/W
31:26	—	These bits are read as 0. The write value should be 0.	R/W

The Global Test Configuration Register is used to configure the CAN channels joining the internal CAN bus communication test mode and the RAM test mode page.

ICBCE[1:0] bits (Channel n Internal CAN Bus Communication Test Mode Enable)

When the ICBCE[1:0] bits are set and CAN-FD module is configured in the internal CAN bus communication test mode, then CAN channel n joins the internal CAN bus communication test mode operation.

Do not write to these bits when the CAN-FD module is in GL_RESET or GL_SLEEP mode.

Only write to these bits when the CAN-FD module is in GL_HALT mode.

These bits are cleared automatically when the CAN-FD module is in GL_RESET mode.

RTMPS[9:0] bits (RAM Test Mode Page Select)

The RTMPS[9:0] bits select the RAM page mode for CPU read/write access when the CAN-FD module is configured in RAM test mode.

See section 32.9.2.1. RAM Test Mode for the RAM test mode specification.

Do not write to these bits when the CAN-FD module is in GL_RESET or GL_SLEEP mode.

Only enter values from 0 to 7 (0x007) for the AFL RAM and 8 to 39 (0x027) for the message buffer RAM.

Only write to these bits when the CAN-FD module is in GL_HALT mode.

These bits are cleared automatically when the related CAN-FD channel is in GL_RESET mode.

32.2.80 CFDGTSTCFG:全局测试配置寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1308

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	RTMPS[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ICBCE[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ICBCE[1:0]	通道n内部CAN总线通信测试模式启用 0：通道n内部CAN总线通讯禁用1：通道n内部CAN总线通讯启用	R/W
15:2	—	这些位被读取为0。写入值应为0。	R/W
25:16	RTMPS[9:0]	RAM测试模式页面Select选择 RAM测试模式页面	R/W
31:26	—	这些位被读取为0。写入值应为0。	R/W

全局测试配置寄存器用于配置加入内部CAN总线通信测试模式和RAM测试模式页面的CAN通道。

ICBCE[1:0]位（通道n内部CAN总线通信测试模式启用）

当ICBCE[1:0]位置位且CAN-FD模块配置为内部CAN总线通信测试模式时，CAN通道n加入内部CAN总线通信测试模式操作。

当CAN-FD模块处于GL_RESET或GL_SLEEP模式时，请勿写入这些位。

仅当CAN-FD模块处于GL_HALT模式时才写入这些位。

当CAN-FD模块处于GL_RESET模式时，这些位会自动清除。

RTMPS[9:0]位（RAM测试模式页面选择）

当CAN-FD模块配置为
RAM测试模式。

请参阅第32.9.2.1节。RAM测试模式用于RAM测试模式规范。

当CAN-FD模块处于GL_RESET或GL_SLEEP模式时，请勿写入这些位。

只为AFLRAM输入0到7(0x007)的值，为消息缓冲区RAM输入8到39(0x027)的值。

仅当CAN-FD模块处于GL_HALT模式时才写入这些位。

当相关CAN-FD通道处于GL_RESET模式时，这些位会自动清除。

32.2.81 CFDGTSTCTR : Global Test Control Register

Base address: CANFD = 0x400B_0000

Offset address: 0x130C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	ICBCTME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICBCTME	Internal CAN Bus Communication Test Mode Enable 0: Internal CAN Bus Communication test mode disabled 1: Internal CAN Bus Communication test mode enabled	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	RTME	RAM Test Mode Enable 0: RAM test mode disabled 1: RAM test mode enabled	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

The Global Test Control register is used to control the global test modes of the CAN-FD module.

ICBCTME bit (Internal CAN Bus Communication Test Mode Enable)

When the ICBCTME bit is set, internal CAN bus communication is enabled for the CAN channels that are configured for internal CAN bus communication participation. See section 32.9.2.2. Internal CAN Bus Communication Test Mode for the specification of internal CAN bus communication test mode.

Only write to this bit when the CAN-FD module is in GL_HALT mode.

Clear this bit when the CAN-FD module is in GL_HALT mode.

This bit is cleared automatically when the CAN-FD module is in GL_RESET mode.

RTME bit (RAM Test Mode Enable)

When the RTME bit is set, the CAN-FD module is configured in RAM test mode. See section 32.9.2.1. RAM Test Mode for RAM test mode specification.

Only write to this bit when the CAN-FD module is in GL_HALT mode.

Clear this bit when the CAN-FD module is in GL_HALT mode.

This bit is cleared automatically when the CAN-FD module is in GL_RESET mode.

32.2.81 CFDGTTSTCTR:全局测试控制寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x130C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	ICBCTME
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ICBCTME	内部CAN总线通信测试模式启用 0：内部CAN总线通信测试模式禁用1：内部CAN总线通信测试模式启用	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	RTME	RAM测试模式启用 0：禁用RAM测试模式1：启用RAM测试模式	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

全局测试控制寄存器用于控制CAN-FD模块的全局测试模式。

ICBCTME位（内部CAN总线通信测试模式启用）

当ICBCTME位被设置时，内部CAN总线通信被配置用于内部CAN总线通信参与的CAN通道启用。请参阅第32.9.2.2节。内部CAN总线通信测试模式用于指定内部CAN总线通信测试模式。

仅当CAN-FD模块处于GL_HALT模式时写入该位。

当CAN-FD模块处于GL_HALT模式时清零该位。

当CAN-FD模块处于GL_RESET模式时，该位会自动清零。

RTME位（RAM测试模式启用）

当RTME位置位时，CAN-FD模块配置为RAM测试模式。请参阅第32.9.2.1节。RAM测试模式RAM测试模式规范。

仅当CAN-FD模块处于GL_HALT模式时写入该位。

当CAN-FD模块处于GL_HALT模式时清零该位。

当CAN-FD模块处于GL_RESET模式时，该位会自动清零。

32.2.82 CFDGFDCFG : Global FD Configuration Register

Base address: CANFD = 0x400B_0000

Offset address: 0x1314

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPED	RES Bit Protocol Exception Disable 0: Protocol exception event detection enabled 1: Protocol exception event detection disabled	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
9:8	TSCCFG[1:0]	Timestamp Capture Configuration 0 0: Timestamp capture at the sample point of SOF (start of frame) 0 1: Timestamp capture at frame valid indication 1 0: Timestamp capture at the sample point of RES bit 1 1: Reserved	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

RPED bit (RES Bit Protocol Exception Disable)

The RPED bit configures the protocol exception event handling according to ISO 11898-1.

When this bit is enabled, the protocol exception event detection is disabled, and the protocol controller transmits an error frame when the protocol exception event is detected (RES bit is sampled recessive).

Only write to this bit when the CAN-FD module is in GL_RESET mode.

TSCCFG[1:0] bits (Timestamp Capture Configuration)

The TSCCFG[1:0] bits configure the different capture points of the timestamp for transmission and reception.

When CFDGFDCFG.TSCCFG[1:0] = 10b, the timestamp capture is performed for CAN-FD frames at RES bit and for Classical frames at the start of frame.

Only write to these bits when the CAN-FD module is in GL_RESET mode.

32.2.83 CFDGLOCKK : Global Lock Key Register

Base address: CANFD = 0x400B_0000

Offset address: 0x131C

Bit position:	31	15	0
Bit field:	—	LOCK[15:0]	
Value after reset:	0	0	0

Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	Lock Key Key bits for unlocking the protection of test modes	W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The Global Lock Key register is a write-only register that is used to unlock the protection for special test bits.

32.2.82 CFDGFDCFG:全局FD配置寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x1314

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TSCCFG[1:0]		—	—	—	—	—	—	—	RPED
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RPED	RES位协议异常禁用 0：启用协议异常事件检测1：禁用协议异常事件检测	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
9:8	TSCCFG[1:0]	时间戳捕获配置 00：在SOF（帧开始）采样点捕获时间戳01：在帧有效指示处捕获时间戳0：在RES位1采样点捕获时间戳1：保留	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

RPED位（RES位协议异常禁用）

RPED位根据ISO11898-1配置协议异常事件处理。

当该位使能时，协议异常事件检测被禁用，并且协议控制器在检测到协议异常事件时发送一个错误帧（RES位被采样为隐性）。

仅当CAN-FD模块处于GL_RESET模式时写入该位。

TSCCFG[1:0]位（时间戳捕获配置）

TSCCFG[1:0]位配置发送和接收时间戳的不同捕获点。

当CFDGFDCFG.TSCCFG[1:0]=10b时，对CAN-FD帧的RES位和帧开始处的经典帧。

仅当CAN-FD模块处于GL_RESET模式时才写入这些位。

32.2.83 CFDGLOCKK:全局锁定密钥寄存器

Base address: CANFD = 0x400B_0000

Offset address: 0x131C

Bit position:	31	15	0
Bit field:	—	LOCK[15:0]	
重置后的值:	0	0	0

Bit	Symbol	Function	R/W
15:0	LOCK[15:0]	钥匙 用于解锁测试模式保护的密钥位	W
31:16	—	这些位被读取为0。写入值应为0。	R/W

全局锁定密钥寄存器是一个只写寄存器，用于解锁对特殊测试位的保护。

See section 32.9.2. Global Test Modes for Lock key specification.

LOCK[15:0] bits (Lock Key)

The unlock key sequence must be written in the LOCK[15:0] bits to configure the CAN-FD module in FIFO OTB disable and RAM test modes.

The read value from these bits is always 0x0000.

You cannot write to these bits when the CAN-FD module is in GL_SLEEP or GL_RESET mode.

Do not write to these bits when the CAN-FD module is in GL_OPERATION mode.

32.2.84 CFDRPGACCn : RAM Test Page Access Registers n (n = 0 to 63)

Base address: CANFD = 0x400B_0000

Offset address: 0x8400 + 0x04 × n (n = 0 to 63)

Bit position:	31																													0
Bit field:	RDTA[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RDTA[31:0]	RAM Data Test Access RAM data bytes	R/W

RDTA[31:0] bits (RAM Data Test Access)

Data can be read from or written into the RDTA[31:0] bits when the CAN-FD module is configured in RAM test mode.

Only write to this bit when the CAN-FD module is in GL_HALT mode and RAM test mode is enabled.

Software data should be read/written in the RAM Test Page Access registers during RAM test mode.

32.2.85 CFDCnBLCT : Channel n Bus Load Control Register (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1418 + 0x20 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BLCLD	—	—	—	—	—	—	—	BLCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BLCE	Bus Load Counter Enable 0: Bus load counter disable 1: Bus load counter enable	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	BLCLD	BUS Load Counter Load When CFDCnBLCT.BLCLD is set, it is reset after a Bus load counter value is loaded.	W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

BLCE bit (Bus Load Counter Enable)

The BLCE bit indicates the enabling signal of a bus load counter. Write to this bit after setting up the CFDCnNCFG register.

请参阅第32.9.2节。锁键规范的全局测试模式。

LOCK[15:0] bits (Lock Key)

解锁密钥序列必须写入LOCK[15:0]位，以将CAN-FD模块配置为FIFOOTB禁用和RAM测试模式。

从这些位读取的值始终为0x0000。

当CAN-FD模块处于GL_SLEEP或GL_RESET模式时，您无法写入这些位。

当CAN-FD模块处于GL_OPERATION模式时，请勿写入这些位。

32.2.84 CFDRPGACCn：RAM测试页访问寄存器n（n=0到63）

Base address: CANFD = 0x400B_0000

Offset address: 0x8400 + 0x04 × n (n = 0 to 63)

Bit position:	31																													0
Bit field:	RDTA[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	RDTA[31:0]	RAM数据测试访问 RAM数据字节	R/W

RDTA[31:0]位（RAM数据测试访问）

当CAN-FD模块配置为RAM测试模式时，可以从RDTA[31:0]位读取或写入数据。

仅当CAN-FD模块处于GL_HALT模式并启用RAM测试模式时才写入该位。

在RAM测试模式期间，软件数据应被读取写入RAM测试页访问寄存器。

32.2.85 CFDCnBLCT:通道n总线负载控制寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1418 + 0x20 × n (n = 0, 1)

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BLCLD	—	—	—	—	—	—	—	BLCE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BLCE	总线负载计数器使能 0：总线负载计数器禁用1： 总线负载计数器启用	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	BLCLD	总线负载计数器负载 当CFDCnBLCT.BLCLD置位时，它会在加载总线加载计数器值后复位。	W
31:9	—	这些位被读取为0。写入值应为0。	R/W

BLCE位（总线负载计数器使能）

BLCE位指示总线负载计数器的使能信号。在设置CFDCnNCFG寄存器后写入该位。

When this bit is 0, the bus load counter stops but the counter is not clear.

The bit is cleared when the related CAN-FD channel is in CH_RESET mode.

You cannot write to this bit in CH_SLEEP mode.

BLCLD bit (BUS Load Counter Load)

When the BLCLD bit is set, the bus load counter value is loaded into CFDCnBLSTS.BLC and the bus load counter is reset.

The read value is always 0.

32.2.86 CFDCnBLSTS : Channel n Bus Load Status Register (n = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x141C + 0x20 × n (n = 0, 1)

Bit position:	31																										3		0
Bit field:	BLC[31:3]																										—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
31:3	BLC[31:3]	Bus Load Counter These bits indicate the bus load counter value.	R

BLC[31:3] bits (Bus Load Counter)

When the CFDCnBLCT.BLCLD bit is set, the bus load counter value is loaded to BLC bit and the bus load counter is reset.

Bits [2:0] are fixed to 000b.

The bus load counter increases by CANFDCLK period while the CAN bus is in an idle state.

These bits are set only by the CAN-FD module. Writing any value has no effect.

32.2.87 Message Buffer Component Structure

32.2.87.1 Start Addresses

The start address for each of the Message Buffer component is calculated using the number of related Message Buffer components and the number of channels.

no_of_channels	2
no_of_RMBCPs_per_channel	16
no_of_RFMBCPs	8
no_of_CFMBCPs_per_channel	3
no_of_TMBCPs_per_channel	16

The start addresses for each register in the Message Buffer component are depicted in Table 32.7.

Table 32.7 Message Buffer Component Register Start Addresses (1 of 2)

b = Message buffer component index	MBCP	Register	p	Regular Start Address n = [0…no_of_channels-1]
[0…no_of_RMBCPs_per_channel-1]	RMBCPb[i]	RMID	x	0x2000 + b*0x0080 + n*0x800
		RMPTR	x	0x2004 + b*0x0080 + n*0x800
		RMFDSTS	x	0x2008 + b*0x0080 + n*0x800
		RMDFp	[0…15]	0x200C + p*0x0004 + b*0x0080 + n*0x800

当该位为0时，总线加载计数器停止但计数器不清零。

当相关CAN-FD通道处于CH_RESET模式时，该位清零。

在CH_SLEEP模式下不能写入该位。

BLCLD位（总线加载计数器加载）

当设置BLCLD位时，总线加载计数器值被加载到CFDCnBLSTS.BLC并且总线加载计数器被复位。

读取值始终为0。

32.2.86 CFDCnBLSTS:通道n总线负载状态寄存器(n=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x141C + 0x20 × n (n = 0, 1)

Bit position:	31																										3		0
Bit field:	BLC[31:3]																										—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
31:3	BLC[31:3]	总线负载计数器 这些位指示总线负载计数器值。	R

BLC[31:3]位（总线负载计数器）

当CFDCnBLCT.BLCLD位置位时，总线加载计数器值被加载到BLC位并且总线加载计数器被复位。

位[2:0]固定为000b。

当CAN总线处于空闲状态时，总线负载计数器增加CANFDCLK周期。

这些位仅由CAN-FD模块设置。写入任何值都没有效果。

32.2.87 消息缓冲区组件结构

32.2.87.1 起始地址

每个消息缓冲区组件的起始地址是使用相关消息缓冲区组件的数量和通道数来计算的。

no_of_channels	2
no_of_RMBCPs_per_channel	16
no_of_RFMBCPs	8
no_of_CFMBCPs_per_channel	3
no_of_TMBCPs_per_channel	16

消息缓冲区组件中每个寄存器的起始地址如表32.7所示。

Table 32.7 消息缓冲区组件寄存器起始地址(1of2)

b=消息缓冲区组件索引	MBCP	Register	p	常规起始地址n=[0…no_of_channels-1]
[0…no_of_RMBCPs_per_channel-1]	RMBCPb[i]	RMID	x	0x2000 + b*0x0080 + n*0x800
		RMPTR	x	0x2004 + b*0x0080 + n*0x800
		RMFDSTS	x	0x2008 + b*0x0080 + n*0x800
		RMDFp	[0…15]	0x200C + p*0x0004 + b*0x0080 + n*0x800

Table 32.7 Message Buffer Component Register Start Addresses (2 of 2)

b = Message buffer component index	MBCP	Register	p	Regular Start Address n = [0…no_of_channels-1]
[0…no_of_RFMBCPs-1]	RFMBCPb[i]	RFIDE	x	0x6000 + b*0x0080
		RFPTRE	x	0x6004 + b*0x0080
		RFFDSTSE	x	0x6008 + b*0x0080
		RFDFpE	[0…15]	0x600C + p*0x0004 + b*0x0080
[0…no_of_CFMBCPs_per_channel-1]	CFMBCPb[i]	CFIDE	x	0x6400 + b*0x0080 + n*0x180
		CFPTRE	x	0x6404 + b*0x0080 + n*0x180
		CFFDCSTSE	x	0x6408 + b*0x0080 + n*0x180
		CFDFpE	[0…15]	0x640C + p*0x0004 + b*0x0080 + n*0x180
[0…no_of_TMBCPs_per_channel-1]	TMBCPb[i]	TMID	x	0x10000 + b*0x0080 + n*0x2000
		TMPTR	x	0x10004 + b*0x0080 + n*0x2000
		TMFDCTR	x	0x10008 + b*0x0080 + n*0x2000
		TMDFp	[0…15]	0x1000C + p*0x0004 + b*0x0080 + n*0x2000

Note: '-' means Not Applicable

The message buffer configuration consists of four types of Message Buffer components:

- RX Message Buffer Component (CFDRMBCPb[i])
- RX FIFO Access Message Buffer Component (CFDRFMBCPb[i])
- Common FIFO Access Message Buffer Component (CFDCFMBCPb[i])
- TX Message Buffer Component (CFDTMBCPb[i]).

Where b = the Message Buffer component index that has a range that varies based on the type of Message Buffer component and i = channel index that has a range from 0 to n.

For a summary of this configuration, see Figure 32.28. For a detailed description of the number of and the different types of message buffers, see section 32.6. FIFO Buffers and Normal Message Buffer Configuration.

As described in section 32.2. Register Descriptions, each Message Buffer component consists of the following registers:

- Identifier (ID)
- Pointer (PTR)
- Data Field (DFp).

Rc is the Message Buffer Component register where c = Message Buffer Component register index that has a range that varies based on the type of Message Buffer component.

A description of the registers, their associated bits and their accessibility are shown below the summary and detailed figures of each component.

In each of the figures, a cell that contains '-' means reserved and has the same behavio as reserved bits for registers in section 32.2.87. Message Buffer Component Structure.

Table 32.7 消息缓冲区组件寄存器起始地址(2of2)

b=消息缓冲区组件索引	MBCP	Register	p	常规起始地址n=[0…no_of_channels-1]
[0…no_of_RFMBCPs-1]	RFMBCPb[i]	RFIDE	x	0x6000 + b*0x0080
		RFPTRE	x	0x6004 + b*0x0080
		RFFDSTSE	x	0x6008 + b*0x0080
		RFDFpE	[0…15]	0x600C + p*0x0004 + b*0x0080
[0…no_of_CFMBCPs_per_channel-1]	CFMBCPb[i]	CFIDE	x	0x6400 + b*0x0080 + n*0x180
		CFPTRE	x	0x6404 + b*0x0080 + n*0x180
		CFFDCSTSE	x	0x6408 + b*0x0080 + n*0x180
		CFDFpE	[0…15]	0x640C + p*0x0004 + b*0x0080 + n*0x180
[0…no_of_TMBCPs_per_channel-1]	TMBCPb[i]	TMID	x	0x10000 + b*0x0080 + n*0x2000
		TMPTR	x	0x10004 + b*0x0080 + n*0x2000
		TMFDCTR	x	0x10008 + b*0x0080 + n*0x2000
		TMDFp	[0…15]	0x1000C + p*0x0004 + b*0x0080 + n*0x2000

Note: '–'表示不适用

消息缓冲区配置由四种类型的消息缓冲区组件组成：

●RX消息缓冲区组件(CFDRMBCPb[i])

●RXFIFO访问消息缓冲区组件(CFDRFMBCPb[i])

●通用FIFO访问消息缓冲区组件(CFDCCFMBCPb[i])

●TX消息缓冲区组件(CFDTMBCPb[i])。

其中b=消息缓冲区组件索引，其范围根据消息缓冲区组件的类型而变化，i=通道索引，范围从0到n。

有关此配置的摘要，请参见图32.28。有关消息缓冲区的数量和不同类型的详细说明，请参阅第32.6节。FIFO缓冲区和正常消息缓冲区配置。

如第32.2节所述。寄存器说明，每个MessageBuffer组件由以下寄存器组成：

- Identifier (ID)
- Pointer (PTR)

●数据字段(DFp)。

Rc是消息缓冲区组件寄存器，其中c=消息缓冲区组件寄存器索引，其范围根据消息缓冲区组件的类型而变化。

每个组件的摘要和详细图下方显示了寄存器、相关位及其可访问性的描述。

在每个图中，包含"–"的单元格表示保留，并且与第32.2.87节中的寄存器保留位具有相同的行为。消息缓冲区组件结构。

32.2.87.2 CFDRMIDn_i : RX Message Buffer ID Register n Channel i (n = 0 to 15, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x2000 + 0x080 × n + 0x800 × i

Bit position:	31	30	28	0
Bit field:	RMIDE	RMRTR	—	RMID[28:0]
Value after reset:	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
28:0	RMID[28:0]	RX Message Buffer ID Field STD-ID/EXT-ID fields	R
29	—	This bit is read as 0. The write value should be 0.	R
30	RMRTR	RX Message Buffer RTR Bit 0: Data frame 1: Remote frame	R
31	RMIDE	RX Message Buffer IDE Bit 0: STD-ID is stored 1: EXT-ID is stored	R

The RX Message Buffer ID Registers n (n = 0 to 15) store the ID field, IDE bit, and RTR bit of the received message.

RMID[28:0] bits (RX Message Buffer ID Field)

The RMID[28:0] are the bits of the STD-ID/EXT-ID fields of the message stored in the RX message buffer.

See section 32.2.87.1. Start Addresses for details on how to interpret the structure of this buffer component.

RMRTR bit (RX Message Buffer RTR Bit)

The RMRTR bit shows whether a data frame or a remote frame was stored in the RX message buffer.

Note: There are no remote frames in CAN-FD format. When a CAN-FD frame is received, the register reflects the state of the received value (the RRS bit in FD frame format).

RMIDE bit (RX Message Buffer IDE Bit)

The RMIDE bit shows whether message with Standard Identifier or Extended Identifier was stored in the RX message buffer.

32.2.87.3 CFDRMPTRn_i : RX Message Buffer Pointer Register n Channel i (n = 0 to 15, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x2004 + 0x080 × n + 0x800 × i

Bit position:	31	28	15	0
Bit field:	RMDLC[3:0]	—	RMTS[15:0]	
Value after reset:	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
15:0	RMTS[15:0]	RX Message Buffer Timestamp Field Timestamp value stored for the message in the RX message buffer	R
27:16	—	These bits are read as 0. The write value should be 0.	R
31:28	RMDLC[3:0]	RX Message Buffer DLC Field Number of data bytes received in a CAN frame.	R

32.2.87.2 CFDRMIDn_i:RX消息缓冲区ID寄存器n通道i(n=0到15 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x2000 + 0x080 × n + 0x800 × i

Bit position:	31	30	28	0
Bit field:	RMIDE	RMRTR	—	RMID[28:0]
重置后的值:	0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
28:0	RMID[28:0]	RX消息缓冲区ID字段 STD-ID/EXT-ID fields	R
29	—	该位读取为0。写入值应为0。	R
30	RMRTR	RX报文缓冲区RTR位 0：数据帧1：远程帧	R
31	RMIDE	RX消息缓冲区IDE位 0：存储STD-ID1：存储EXT-ID	R

RX报文缓冲区ID寄存器n（n=0到15）存储接收到的报文的ID字段、IDE位和RTR位。

RMID[28:0]位（RX消息缓冲区ID字段）

RMID[28:0]是存储在RX消息缓冲区中的消息的STD-IDEXT-ID字段的位。

请参阅第32.2.87.1节。起始地址以获取有关如何解释此缓冲区组件结构的详细信息。

RMRTR位（RX报文缓冲区RTR位）

RMRTR位显示数据帧或远程帧是否存储在RX报文缓冲区中。

Note: CAN-FD格式中没有远程帧。当接收到CAN-FD帧时，寄存器反映接收值的状态（FD帧格式中的RRS位）。

RMIDE位（RX报文缓冲区IDE位）

RMIDE位显示带有标准标识符或扩展标识符的消息是否存储在RX消息缓冲区中。

32.2.87.3 CFDRMPTRn_i:RX消息缓冲区指针寄存器n通道i(n=0到15 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x2004 + 0x080 × n + 0x800 × i

Bit position:	31	28	15	0
Bit field:	RMDLC[3:0]	—	RMTS[15:0]	
重置后的值:	0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bit	Symbol	Function	R/W
15:0	RMTS[15:0]	RX消息缓冲区时间戳字段 为RX消息缓冲区中的消息存储的时间戳值	R
27:16	—	这些位被读取为0。写入值应为0。	R
31:28	RMDLC[3:0]	RX消息缓冲区DLC字段 CAN帧中接收的数据字节数。	R

The RX Message Buffer Pointer Registers n (n = 0 to 15) store the DLC and Timestamp fields for the received message.

RMTS[15:0] bits (RX Message Buffer Timestamp Field)

The RMTS[15:0] bits store the timestamp value taken at the capture point as configured by CFDGFDCFG.TSCCFG of the received message.

RMDLC[3:0] bits (RX Message Buffer DLC Field)

The RMDLC[3:0] bits store the number of data bytes that were received in the RX message buffer.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes that were received.

Note: The maximum capacity of the buffer belongs to CFDRMNB.RMPLS and this is not available in the classical CAN function.

32.2.87.4 CFDRMFDSTSn_i : RX Message Buffer CAN-FD Status Register n Channel i (n = 0 to 15, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x2008 + 0x080 × n + 0x800 × i

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RMPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RMIFL[1:0]		—	—	—	—	—	RMFDF	RMBRS	RMESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMESI*1	Error State Indicator bit 0: CAN-FD frame received from error active node 1: CAN-FD frame received from error passive node	R
1	RMBRS*1	Bit Rate Switch bit 0: CAN-FD frame received with no bit rate switch 1: CAN-FD frame received with bit rate switch	R
2	RMFDF*1	CAN FD Format bit 0: Non CAN-FD frame received 1: CAN-FD frame received	R
7:3	—	These bits are read as 0. The write value should be 0.	R
9:8	RMIFL[1:0]	RX Message Buffer Information Label Field	R
15:10	—	These bits are read as 0. The write value should be 0.	R
31:16	RMPTR[15:0]	RX Message Buffer Pointer Field	R

Note 1. This bit is not available in the classical CAN function.

The RX Message Buffer CAN-FD Status Registers n (n = 0 to 2) show the status of the FDF, BRS and ESI bits, and pointer of the received CAN-FD frame.

RMESI bit (Error State Indicator bit)

The RMESI bit has the same value as the ESI bit of the received CAN-FD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RMBRS bit (Bit Rate Switch bit)

The RMBRS bit has the same value as the BRS bit of the received CAN-FD frame.

RX消息缓冲区指针寄存器n（n=0到15）存储接收消息的DLC和时间戳字段。

RMTS[15:0]位（RX消息缓冲区时间戳字段）

RMTS[15:0]位存储在捕获点获取的时间戳值，由接收到的消息的CFDGFDCFG.TSCCFG配置。

RMDLC[3:0]位（RX消息缓冲区DLC字段）

RMDLC[3:0]位存储在RX报文缓冲区中接收到的数据字节数。

有关定义接收的数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

Note: 缓冲区的最大容量属于CFDRMNB.RMPLS，这在经典CAN功能中不可用。

32.2.87.4 CFDRMFDSTSn_i:RX消息缓冲区CAN-FD状态寄存器n通道i(n=0到15 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x2008 + 0x080 × n + 0x800 × i

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	RMPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RMIFL[1:0]		—	—	—	—	—	RMFDF	RMBRS	RMESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RMESI*1	错误状态指示位 0：从错误主动节点接收到CAN-FD帧1：从错误被动节点接收到CAN-FD帧	R
1	RMBRS*1	比特率切换位 0：接收到的CAN-FD帧，没有比特率切换1：接收到的CAN-FD帧，有比特率切换	R
2	RMFDF*1	CANFD格式位 0：接收到非CAN-FD帧1：接收到CAN-FD帧	R
7:3	—	这些位被读取为0。写入值应为0。	R
9:8	RMIFL[1:0]	RX消息缓冲区信息标签字段	R
15:10	—	这些位被读取为0。写入值应为0。	R
31:16	RMPTR[15:0]	RX消息缓冲区指针字段	R

注1.该位在经典CAN功能中不可用。

RX消息缓冲区CAN-FD状态寄存器n（n=0到2）显示FDF、BRS和ESI位的状态，以及接收到的CAN-FD帧的指针。

RMESI位（错误状态指示位）

RMESI位与接收到的CAN-FD帧的ESI位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RMBRS位（比特率切换位）

RMBRS位与接收到的CAN-FD帧的BRS位具有相同的值。

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RMFDF bit (CAN FD Format bit)

The RMFDF bit has the same value as the FDF bit of the received CAN-FD frame.

Note: This bit is not available in the classical CAN function.

RMIFL[1:0] bits (RX Message Buffer Information Label Field)

The RMIFL[1:0] bits store the information label value from the related Global Acceptance Filter List entry.

RMPTR[15:0] bits (RX Message Buffer Pointer Field)

The RMPTR[15:0] bits store the pointer value from the related Global Acceptance Filter List entry.

32.2.87.5 CFDRMDFpn_i : RX Message Buffer Data Field p Register n Channel i (p = 0 to 15, n = 0 to 15, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x200C + 0x004 × p + 0x080 × n + 0x800 × i

Bit position:	31 to 24	23 to 16	15 to 8	7 to 0
Bit field:	RMDB((p * 4) + 3)[7:0]	RMDB((p * 4) + 2)[7:0]	RMDB((p *4) + 1)[7:0]	RMDB((p * 4))[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RMDB((p * 4))[7:0]	RX Message Buffer Data Byte (p * 4)	R
15:8	RMDB((p *4) + 1)[7:0]	RX Message Buffer Data Byte ((p * 4) + 1)	R
23:16	RMDB((p * 4) + 2)[7:0]	RX Message Buffer Data Byte ((p * 4) + 2)	R
31:24	RMDB*1((p * 4) + 3)[7:0]	RX Message Buffer Data Byte ((p * 4) + 3)	R

Note 1. These bits are not available in the classical CAN function.

The RX Message Buffer Data Field p Registers n (p = 0 to 15, n = 0 to 15) store the data bytes (p * 4) to data bytes ((p * 4) + 3) of the received message.

RMDB((p * 4))[7:0] bits (RX Message Buffer Data Byte (p * 4))

The RMDB(p * 4) [7:0] bits store data bytes (p*4) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

RMDB((p *4) + 1)[7:0] bits (RX Message Buffer Data Byte ((p * 4) + 1))

The RMDB((p * 4) + 1)[7:0] bits store data bytes ((p * 4) + 1) of the message in the RX message buffer.

Unused Data Bytes will be filled with 0x00.

RMDB((p * 4) + 2)[7:0] bits (RX Message Buffer Data Byte ((p * 4) + 2))

The RMDB((p * q) +2)[7:0] bits store data bytes ((p * 4 + 2) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

RMDB((p * 4) + 3)[7:0] bits (RX Message Buffer Data Byte ((p * 4) + 3))

The RMDB((p * 4) +3)[7:0] bits store data bytes ((p * 4) + 3) of the message in the RX message buffer.

Unused data bytes are filled with 0x00.

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RMFDF位（CANFD格式位）

RMFDF位与接收到的CAN-FD帧的FDF位具有相同的值。

Note: 该位在经典CAN功能中不可用。

RMIFL[1:0]位（RX消息缓冲区信息标签字段）

RMIFL[1:0]位存储来自相关全局接受过滤器列表条目的信息标签值。

RMPTR[15:0]位（RX消息缓冲区指针字段）

RMPTR[15:0]位存储来自相关全局接受过滤器列表条目的指针值。

32.2.87.5 CFDRMDFpn_i:RX消息缓冲区数据字段p寄存器n通道i(p=0到15 n=0到15 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x200C + 0x004 × p + 0x080 × n + 0x800 × i

Bit position:	31 to 24	23 to 16	15 to 8	7 to 0
Bit field:	RMDB((p * 4) + 3)[7:0]	RMDB((p * 4) + 2)[7:0]	RMDB((p *4) + 1)[7:0]	RMDB((p * 4))[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RMDB((p * 4))[7:0]	RX消息缓冲区数据字节(p*4)	R
15:8	RMDB((p *4) + 1)[7:0]	RX消息缓冲区数据字节((p*4)+1)	R
23:16	RMDB((p * 4) + 2)[7:0]	RX消息缓冲区数据字节((p*4)+2)	R
31:24	RMDB*1((p * 4) + 3)[7:0]	RX消息缓冲区数据字节((p*4)+3)	R

注1.这些位在经典CAN功能中不可用。

RX报文缓冲区数据字段p寄存器n（p=0到15，n=0到15）存储接收到的报文的数据字节（p*4）到数据字节（（p*4）+3）。

RMDB((p*4))[7:0]bits(RX报文缓冲区数据字节(p*4))

RMDB(p*4)[7:0]位将消息的数据字节(p*4)存储在RX消息缓冲区中。

未使用的数据字节用0x00填充。

RMDB((p*4)+1)[7:0]bits(RX报文缓冲区数据字节((p*4)+1))

RMDB((p*4)+1)[7:0]位将消息的数据字节((p*4)+1)存储在RX消息缓冲区中。

未使用的数据字节将用0x00填充。

RMDB((p*4)+2)[7:0]bits(RX报文缓冲区数据字节((p*4)+2))

RMDB((p*q)+2)[7:0]位将消息的数据字节((p*4+2)存储在RX消息缓冲区中。

未使用的数据字节用0x00填充。

RMDB((p*4)+3)[7:0]bits(RX报文缓冲区数据字节((p*4)+3))

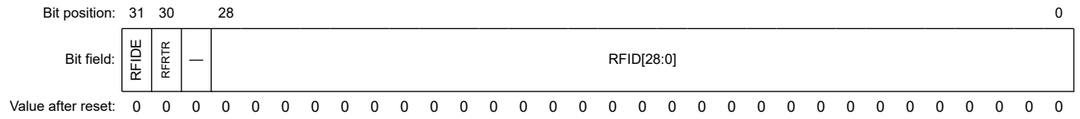
RMDB((p*4)+3)[7:0]位将消息的数据字节((p*4)+3)存储在RX消息缓冲区中。

未使用的数据字节用0x00填充。

32.2.87.6 CFDRFIDn : RX FIFO Access ID Register n (n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x6000 + 0x080 × n



Bit	Symbol	Function	R/W
28:0	RFID[28:0]	RX FIFO Buffer ID Field STD-ID/EXT-ID fields	R
29	—	This bit is read as 0.	R
30	RFRTR	RX FIFO Buffer RTR bit 0: Data frame 1: Remote frame	R
31	RFIDE	RX FIFO Buffer IDE bit 0: STD-ID has been received 1: EXT-ID has been received	R

The RX FIFO Access ID Registers n (n = 0 to 7) store the ID field, IDE bit and RTR bit of the message.

RFID[28:0] bits (RX FIFO Buffer ID Field)

The RFID[28:0] bits are the bits of the STD-ID/EXT-ID fields of the message in the FIFO buffer.

For alignment of these bits in standard and extended frame format, see Identifier Bits Alignment.

RFRTR bit (RX FIFO Buffer RTR bit)

The RFRTR bit shows whether a data frame or a remote frame was stored in the FIFO buffer.

Note: There are no remote frames in CAN-FD format. When a CAN-FD frame was received, the register reflects the state of the received value (RRS bit in FD frame format).

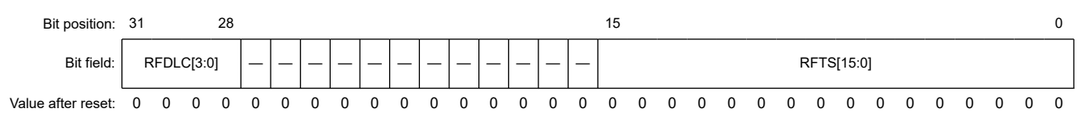
RFIDE bit (RX FIFO Buffer IDE bit)

The RFIDE bit shows whether message with the Standard Identifier or Extended Identifier was received in the FIFO buffer.

32.2.87.7 CFDRFPTRn : RX FIFO Access Pointer Register n (n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x6004 + 0x080 × n



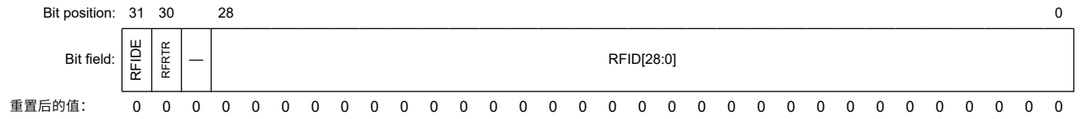
Bit	Symbol	Function	R/W
15:0	RFTS[15:0]	RX FIFO Timestamp Value Timestamp value of the received CAN frame	R
27:16	—	These bits are read as 0. The write value should be 0.	R
31:28	RFDLC[3:0]	RX FIFO Buffer DLC Field Number of data bytes received in a CAN frame	R

The FIFO Access Pointer Registers n (n = 0 to 7) store the DLC and Timestamp fields for the received message.

32.2.87.6 CFDRFIDn：RXFIFO访问ID寄存器n（n=0到7）

Base address: CANFD = 0x400B_0000

Offset address: 0x6000 + 0x080 × n



Bit	Symbol	Function	R/W
28:0	RFID[28:0]	RXFIFO缓冲区ID字段 STD-ID/EXT-ID fields	R
29	—	该位读为0。	R
30	RFRTR	RXFIFO缓冲区RTR位 0：数据帧1：远程帧	R
31	RFIDE	RXFIFO缓冲器IDE位 0：接收到STD-ID1：接收到EXT-ID	R

RXFIFO访问ID寄存器n（n=0到7）存储消息的ID字段、IDE位和RTR位。

RFID[28:0]位（RXFIFO缓冲区ID字段）

RFID[28:0]位是FIFO缓冲区中消息的STD-IDEXT-ID字段的位。

有关标准和扩展帧格式中这些位的对齐方式，请参阅标识符位对齐。

RFRTR位（RXFIFO缓冲器RTR位）

RFRTR位显示数据帧或远程帧是否存储在FIFO缓冲区中。

Note: CAN-FD格式中没有远程帧。当接收到CAN-FD帧时，寄存器反映接收值的状态（FD帧格式中的RRS位）。

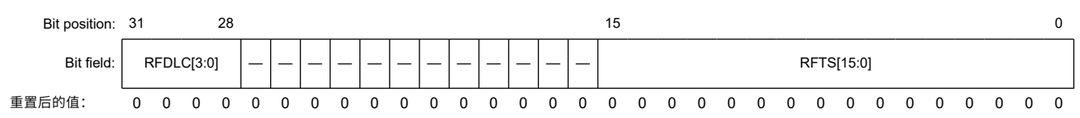
RFIDE位（RXFIFO缓冲器IDE位）

RFIDE位显示在FIFO缓冲区中是否接收到带有标准标识符或扩展标识符的消息。

32.2.87.7 CFDRFPTRn：RXFIFO访问指针寄存器n（n=0到7）

Base address: CANFD = 0x400B_0000

Offset address: 0x6004 + 0x080 × n



Bit	Symbol	Function	R/W
15:0	RFTS[15:0]	RXFIFO时间戳值 接收到的CAN帧的时间戳值	R
27:16	—	这些位被读取为0。写入值应为0。	R
31:28	RFDLC[3:0]	RXFIFO缓冲区DLC字段 CAN帧中接收的数据字节数	R

FIFO访问指针寄存器n（n=0到7）存储接收消息的DLC和时间戳字段。

RFTS[15:0] bits (RX FIFO Timestamp Value)

The RFTS[15:0] bits store the timestamp value taken at the capture point as configured by the CFDGFDCFG.TSCCFG bit of the received message.

RFDLC[3:0] bits (RX FIFO Buffer DLC Field)

The RFDLC[3:0] bits store the number of data bytes that were received in the RX FIFO buffer.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes that were received.

32.2.87.8 CFDRFFDSTSn : RX FIFO Access CAN-FD Status Register n (n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x6008 + 0x080 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDRFPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RFIFL[1:0]		—	—	—	—	—	RFFDF	RFBRS	RFESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFESI*1	Error State Indicator bit 0: CAN-FD frame received from error active node 1: CAN-FD frame received from error passive node	R
1	RFBRS*1	Bit Rate Switch bit 0: CAN-FD frame received with no bit rate switch 1: CAN-FD frame received with bit rate switch	R
2	RFFDF*1	CAN FD Format bit 0: Non CAN-FD frame received 1: CAN-FD frame received	R
7:3	—	These bits are read as 0. The write value should be 0.	R
9:8	RFIFL[1:0]	RX FIFO Buffer Information Label Field	R
15:10	—	These bits are read as 0. The write value should be 0.	R
31:16	CFDRFPTR[15:0]	RX FIFO Buffer Pointer Field	R

Note 1. This bit is not available in the classical CAN function.

The RX FIFO Access CAN-FD Status Registers n (n = 0 to 7) show the status of the FDF, BRS, and ESI bits, including the pointer of the received CAN-FD frame.

RFESI bit (Error State Indicator bit)

The RFESI bit has the same value as the ESI bit of the received CAN-FD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RFBRS bit (Bit Rate Switch bit)

The RFBRS bit has the same value as the BRS bit of the received CAN-FD frame.

When the received FDF bit is 0, this means a CAN2.0 frame is received and 0 is stored to this bit.

Note: This bit is not available in the classical CAN function.

RFTS[15:0]位（RXFIFO时间戳值）

RFTS[15:0]位存储在捕获点获取的时间戳值，由接收到的消息的CFDGFDCFG.TSCCFG位配置。

RFDLC[3:0]位（RXFIFO缓冲区DLC字段）

RFDLC[3:0]位存储在RXFIFO缓冲区中接收到的数据字节数。

有关定义接收的数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

32.2.87.8 CFDRFFDSTSn：RXFIFO访问CAN-FD状态寄存器n（n=0到7）

Base address: CANFD = 0x400B_0000

Offset address: 0x6008 + 0x080 × n

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFDRFPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	RFIFL[1:0]		—	—	—	—	—	RFFDF	RFBRS	RFESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFESI*1	错误状态指示位 0：从错误主动节点接收到CAN-FD帧1：从错误被动节点接收到CAN-FD帧	R
1	RFBRS*1	比特率切换位 0：接收到的CAN-FD帧，没有比特率切换1：接收到的CAN-FD帧，有比特率切换	R
2	RFFDF*1	CANFD格式位 0：接收到非CAN-FD帧1：接收到CAN-FD帧	R
7:3	—	这些位被读取为0。写入值应为0。	R
9:8	RFIFL[1:0]	RXFIFO缓冲区信息标签字段	R
15:10	—	这些位被读取为0。写入值应为0。	R
31:16	CFDRFPTR[15:0]	RXFIFO缓冲区指针字段	R

注1.该位在经典CAN功能中不可用。

RXFIFO访问CAN-FD状态寄存器n（n=0到7）显示FDF、BRS和ESI位的状态，包括接收到的CAN-FD帧的指针。

RFESI位（错误状态指示位）

RFESI位与接收到的CAN-FD帧的ESI位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

RFBRS位（比特率切换位）

RFBRS位与接收到的CAN-FD帧的BRS位具有相同的值。

当接收到的FDF位为0时，表示接收到CAN2.0帧，并将0存储到该位。

Note: 该位在经典CAN功能中不可用。

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RFFDF bit (CAN FD Format bit)

The RFFDF bit has the same value as the FDF bit of the received CAN-FD frame.

Note: This bit is not available in the classical CAN function.

RFIFL[1:0] bits (RX FIFO Buffer Information Label Field)

The RFIFL[1:0] bits store the information label value from the related Global Acceptance Filter List entry.

CFDRFPTR[15:0] bits (RX FIFO Buffer Pointer Field)

The CFDRFPTR[15:0] bits store the pointer value from the related Global Acceptance Filter List entry.

32.2.87.9 CFDRFDFpn : RX FIFO Access Data Field p Register n (p = 0 to 15, n = 0 to 7)

Base address: CANFD = 0x400B_0000

Offset address: 0x600C + 0x004 × p + 0x080 × n

Bit position:	31 24	23 16	15 8	7 0
Bit field:	RFDB((p * 4) + 3)[7:0]	RFDB((p * 4) + 2)[7:0]	RFDB((p * 4) + 1)[7:0]	RFDB((p * 4)[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RFDB((p * 4)[7:0]	RX FIFO Buffer Data Byte (p * 4)	R
15:8	RFDB((p * 4) + 1)[7:0]	RX FIFO Buffer Data Byte ((p * 4) + 1)	R
23:16	RFDB((p * 4) + 2)[7:0]	RX FIFO Buffer Data Byte ((p * 4) + 2)	R
31:24	RFDB((p * 4) + 3)[7:0]	RX FIFO Buffer Data Byte ((p * 4) + 3)	R

The RX FIFO Access Data Field p Registers n (p = 0 to 15, n = 0 to 7) store data bytes ((p * 4) to data byte ((p * 4) + 3) of the received message.

RFDB((p * 4)[7:0] bits (RX FIFO Buffer Data Byte (p * 4))

The RFDB(p * 4)[7:0] bits store data bytes (p * 4) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00 according to the configured data payload size CFDRFCCn.RFPLS.

RFDB((p * 4) + 1)[7:0] bits (RX FIFO Buffer Data Byte ((p * 4) + 1))

The RFDB((p * 4) + 1))[7:0] bits store data bytes ((p * 4) + 1)) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFDB((p * 4) + 2)[7:0] bits (RX FIFO Buffer Data Byte ((p * 4) + 2))

The RFDB((p * 4) + 2)[7:0] bits store data bytes ((p * 4) + 2) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFDB((p * 4) + 3)[7:0] bits (RX FIFO Buffer Data Byte ((p * 4) + 3))

The RFDB((p * 4) + 3)[7:0] bits store data bytes ((p * 4) + 3) of the message present in the FIFO buffer.

Unused data bytes are filled with 0x00.

RFFDF位（CANFD格式位）

RFFDF位与接收到的CAN-FD帧的FDF位具有相同的值。

Note: 该位在经典CAN功能中不可用。

RFIFL[1:0]位（RXFIFO缓冲区信息标签字段）

RFIFL[1:0]位存储来自相关全局接受过滤器列表条目的信息标签值。

CFDRFPTR[15:0]位（RXFIFO缓冲区指针字段）

CFDRFPTR[15:0]位存储来自相关全局接受过滤器列表条目的指针值。

32.2.87.9 CFDRFDFpn：RXFIFO访问数据字段p寄存器n（p=0到15，n=0到7）

Base address: CANFD = 0x400B_0000

Offset address: 0x600C + 0x004 × p + 0x080 × n

Bit position:	31 24	23 16	15 8	7 0
Bit field:	RFDB((p * 4) + 3)[7:0]	RFDB((p * 4) + 2)[7:0]	RFDB((p * 4) + 1)[7:0]	RFDB((p * 4)[7:0]
重置后的值：	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RFDB((p * 4)[7:0]	RXFIFO缓冲区数据字节(p*4)	R
15:8	RFDB((p * 4) + 1)[7:0]	RXFIFO缓冲区数据字节((p*4)+1)	R
23:16	RFDB((p * 4) + 2)[7:0]	RXFIFO缓冲区数据字节((p*4)+2)	R
31:24	RFDB((p * 4) + 3)[7:0]	RXFIFO缓冲区数据字节((p*4)+3)	R

RXFIFO访问数据字段p寄存器n(p=0到15，n=0到7)存储接收到的报文的数据字节((p*4)到数据字节((p*4)+3)。

RFDB((p*4)[7:0]bits(RXFIFO缓冲区数据字节(p*4))

RFDB(p*4)[7:0]位存储FIFO缓冲区中存在的消息的数据字节(p*4)。

根据配置的数据有效负载大小CFDRFCCn.RFPLS，未使用的数据字节用0x00填充。

RFDB((p*4)+1)[7:0]bits(RXFIFO缓冲区数据字节((p*4)+1))

RFDB((p*4)+1))[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)+1))。

未使用的数据字节用0x00填充。

RFDB((p*4)+2)[7:0]bits(RXFIFO缓冲区数据字节((p*4)+2))

RFDB((p*4)+2)[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)+2)。

未使用的数据字节用0x00填充。

RFDB((p*4)+3)[7:0]bits(RXFIFO缓冲区数据字节((p*4)+3))

RFDB((p*4)+3)[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)+3)。

未使用的数据字节用0x00填充。

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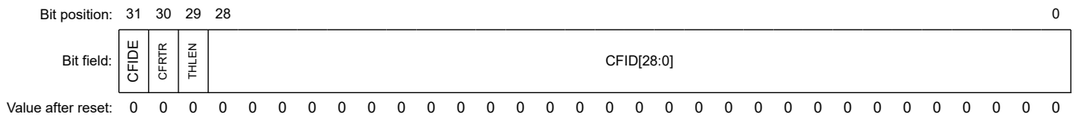
32.2.87.10 CFDCFIDn_i : Common FIFO Access ID Register n Channel i (n = 0 to 2, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x6400 + 0x080 × n + 0x180 × i



Bit	Symbol	Function	R/W
28:0	CFID[28:0]	Common FIFO Buffer ID Field STD-ID/EXT-ID fields	R/W
29	THLEN	THL Entry Enable TX FIFO mode: 0: Entry is not to be stored in THL after successful TX 1: Entry is to be stored in THL after successful TX RX FIFO mode: Reserved, this bit is read as 0.	R/W
30	CFRTR	Common FIFO Buffer RTR bit 0: Data frame 1: Remote frame	R/W
31	CFIDE	Common FIFO Buffer IDE bit 0: STD-ID is to be transmitted or has been received 1: EXT-ID is to be transmitted or has been received	R/W

The Common FIFO Access ID Registers n (n = 0 to 5) store the ID field, IDE bit and RTR bit of the message.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFID[28:0] bits (Common FIFO Buffer ID Field)

The CFID[28:0] bits are the bits of the STD-ID/EXT-ID fields of the message in the FIFO buffer.

In TX mode, you can write and read from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

THLEN bit (THL Entry Enable)

The THLEN bit controls the storage of an entry corresponding to the transmitted message in the TX History list at the end of a successful transmission.

In TX mode, you can write and read from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

CFRTR bit (Common FIFO Buffer RTR bit)

The CFRTR bit selects whether a data frame or a remote frame is to be transmitted from or was received in the FIFO buffer.

Note: There are no remote frames in CAN FD format. When a CAN-FD frame is received (RX mode), the register reflects the state of the received value (RRS bit in FD frame format). When CAN-FD transmission (TX or GW mode CFDCFID.CFFDF = 1), the bit is always transmitted dominant (data frame).

In TX mode, you can write and read from FIFO buffers.

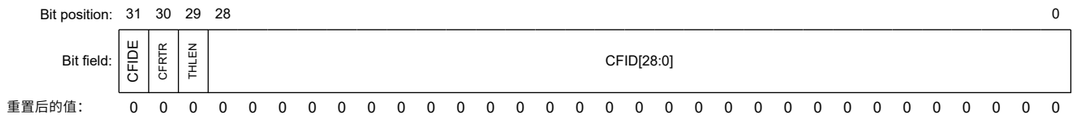
In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

32.2.87.10 CFDCFIDn_i:通用FIFO访问ID寄存器n通道i(n=0到2 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x6400 + 0x080 × n + 0x180 × i



Bit	Symbol	Function	R/W
28:0	CFID[28:0]	通用FIFO缓冲区ID字段 STD-ID/EXT-ID fields	R/W
29	THLEN	THL条目启用 TX FIFO mode: 0：TX成功后不存入THL1：TX成功后存入THL RX FIFO mode: 保留，该位读为0。	R/W
30	CFRTR	通用FIFO缓冲器RTR位 0：数据帧1：远程帧	R/W
31	CFIDE	通用FIFO缓冲器IDE位 0：STD-ID待发送或已接收1：EXT-ID待发送或已接收	R/W

通用FIFO访问ID寄存器n（n=0到5）存储消息的ID字段、IDE位和RTR位。

在TX模式下，您可以从FIFO中读取数据，仅针对基于写指针值的当前条目，而不能针对其他条目。

CFID[28:0]位（通用FIFO缓冲区ID字段）

CFID[28:0]位是FIFO缓冲区中消息的STD-IDEXT-ID字段的位。

在TX模式下，您可以写入和读取FIFO缓冲区。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

THLEN位（THL入口使能）

THLEN位控制在成功发送结束时将对应于发送消息的条目存储在TX历史列表中。

在TX模式下，您可以写入和读取FIFO缓冲区。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

CFRTR位（通用FIFO缓冲区RTR位）

CFRTR位选择是从FIFO缓冲区发送还是接收数据帧或远程帧。

Note: CANFD格式中没有远程帧。当接收到CAN-FD帧时（RX模式），寄存器反映接收值的状态（FD帧格式中的RRS位）。当CAN-FD传输（TX或GW模式CFDCFID.CFFDF=1）时，该位始终为显性传输（数据帧）。

在TX模式下，您可以写入和读取FIFO缓冲区。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

CFIDE bit (Common FIFO Buffer IDE bit)

The CFIDE bit selects whether a message with EXT-ID or STD-ID is to be transmitted from or was received in the FIFO buffer.

In TX mode, you can write and read from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

32.2.87.11 CFDCFPTRn_i : Common FIFO Access Pointer Register n Channel i (n = 0 to 2, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x6404 + 0x080 × n + 0x180 × i

Bit position:	31															15															0
Bit field:	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	CFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CFTS[15:0]	Common FIFO Timestamp Value Timestamp value of the received CAN frame (FIFO in RX mode).	R/W
27:16	—	These bits are read as 0. The write value should be 0.	R/W
31:28	CFDLC[3:0]	Common FIFO Buffer DLC Field Number of data bytes received in a CAN frame, or to be transmitted in a CAN frame.	R/W

The Common FIFO Access Pointer Registers n (n = 0 to 2) store the DLC and Timestamp fields.

In TX mode, you can read data from the FIFO buffer, only for the current entry based on the write pointer value, and not for the other entries.

CFTS[15:0] bits (Common FIFO Timestamp Value)

The CFTS[15:0] bits store the timestamp value taken at the capture point as configured by the CFDGFDCFG.TSCCFG bit of the received message (if FIFO is configured in RX mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

CFDLC[3:0] bits (Common FIFO Buffer DLC Field)

The CFDLC[3:0] bits store the number of data bytes that were received in the FIFO buffer or are to be transmitted.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes.

In TX mode, you can read and write from the FIFO buffers. Do not read data for the other entries in the FIFO when configured in TX mode.

In RX mode, you can only read data from the FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

CFIDE位（通用FIFO缓冲器IDE位）

CFIDE位选择带有EXT-ID或STD-ID的消息是从FIFO缓冲区发送还是在FIFO缓冲区中接收。

在TX模式下，您可以写入和读取FIFO缓冲区。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

32.2.87.11 CFDCFPTRn_i:公共FIFO访问指针寄存器n通道i(n=0到2 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x6404 + 0x080 × n + 0x180 × i

Bit position:	31															15															0
Bit field:	CFDLC[3:0]				—	—	—	—	—	—	—	—	—	—	—	CFTS[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CFTS[15:0]	通用FIFO时间戳值 接收到的CAN帧的时间戳值（RX模式下的FIFO）。	R/W
27:16	—	这些位被读取为0。写入值应为0。	R/W
31:28	CFDLC[3:0]	通用FIFO缓冲区DLC字段 在一个CAN帧中接收的数据字节数，或在一个CAN帧中传输的数据字节数。	R/W

公共FIFO访问指针寄存器n（n=0到2）存储DLC和时间戳字段。

在TX模式下，您可以从FIFO缓冲区读取数据，仅根据写指针值读取当前条目，而不能读取其他条目。

CFTS[15:0]位（通用FIFO时间戳值）

CFTS[15:0]位存储由接收消息的CFDGFDCFG.TSCCFG位配置的捕获点的时间戳值（如果FIFO配置为RX模式）。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

CFDLC[3:0]位（通用FIFO缓冲区DLC字段）

CFDLC[3:0]位存储已在FIFO缓冲区中接收或将要发送的数据字节数。

有关定义数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

在TX模式下，您可以从FIFO缓冲区读取和写入。在TX模式下配置时，不要读取FIFO中其他条目的数据。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

32.2.87.12 CFDCFFDCSTSn_i : Common FIFO Access CAN-FD Control/Status Register n Channel i (n = 0 to 2, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x6408 + 0x080 × n + 0x180 × i

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFIFL[1:0]		—	—	—	—	—	CFFDF	CFBRS	CFESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFESI*1	Error State Indicator bit 0: CAN-FD frame received or to transmit by error active node 1: CAN-FD frame received or to transmit by error passive node	R/W
1	CFBRS*1	Bit Rate Switch bit 0: CAN-FD frame received or to transmit with no bit rate switch 1: CAN-FD frame received or to transmit with bit rate switch	R/W
2	CFFDF*1	CAN FD Format bit 0: Non CAN-FD frame received or to transmit 1: CAN-FD frame received or to transmit	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CFIFL[1:0]	COMMON FIFO Buffer Information Label Field	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W
31:16	CFPTR[15:0]	Common FIFO Buffer Pointer Field	R/W

Note 1. This bit is not available in the classical CAN function.

The Common FIFO Access CAN-FD Control/Status Registers n (n = 0 to 2) show the status of the FDF, BRS and ESI bits, including the pointer of the received CAN-FD frame or the CAN-FD frame to transmit.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFESI bit (Error State Indicator bit)

In TX mode, you can read and write from FIFO buffers. In this mode, when the CAN-FD module is not in error passive, the CFESI bit equals the write value. Otherwise, it is a don't care and the bit is transmitted as 1 on the CAN bus, indicating this is an error passive node.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

In RX or GW mode, the CFESI bit is updated with the ESI bit value of the CAN-FD frame when it has been received, indicating the error state of the transmitting node. In RX or GW mode, 0 is stored to this bit when the received FDF bit is 0, this means a CAN 2.0 frame is received.

Note: This bit is not available in the classical CAN function.

CFBRS bit (Bit Rate Switch bit)

In TX mode, you can read and write from FIFO buffers. In this mode, the CAN-FD module either transmits a 0 to indicate no bit rate switch in the frame to be transmitted or a 1 to indicate a bit rate switch in the frame to be transmitted.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

32.2.87.12 CFDCFFDCSTSn_i:通用FIFO访问CAN-FD控制状态寄存器n通道i(n=0到2 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x6408 + 0x080 × n + 0x180 × i

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	CFPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CFIFL[1:0]		—	—	—	—	—	CFFDF	CFBRS	CFESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CFESI*1	错误状态指示位 0：CAN-FD帧接收或发送错误主动节点1：CAN-FD帧接收或发送错误被动节点	R/W
1	CFBRS*1	比特率切换位 0：接收或发送CAN-FD帧，不带比特率切换1：接收或发送CAN-FD帧，带比特率切换	R/W
2	CFFDF*1	CANFD格式位 0：接收或发送非CAN-FD帧1：接收或发送CAN-FD帧	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
9:8	CFIFL[1:0]	COMMONFIFO缓冲区信息标签字段	R/W
15:10	—	这些位被读取为0。写入值应为0。	R/W
31:16	CFPTR[15:0]	通用FIFO缓冲区指针字段	R/W

注1.该位在经典CAN功能中不可用。

通用FIFO访问CAN-FD控制状态寄存器n（n=0到2）显示FDF、BRS和ESI位的状态，包括接收到的CAN-FD帧或要发送的CAN-FD帧的指针。

在TX模式下，您可以从FIFO中读取数据，仅针对基于写指针值的当前条目，而不能针对其他条目。

CFESI位（错误状态指示位）

在TX模式下，您可以从FIFO缓冲区读取和写入。在这种模式下，当CAN-FD模块没有处于错误被动状态时，CFESI位等于写入值。否则，它是无关紧要的，该位在CAN总线上传输为1，表示这是一个错误被动节点。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

在RX或GW模式下，当CAN-FD帧接收到时，CFESI位会更新为ESI位值，指示发送节点的错误状态。在RX或GW模式下，当接收到的FDF位为0时，将0存储到该位，这意味着接收到CAN2.0帧。

Note: 该位在经典CAN功能中不可用。

CFBRS位（比特率切换位）

在TX模式下，您可以从FIFO缓冲区读取和写入。在这种模式下，CAN-FD模块要么发送0表示要发送的帧中没有比特率切换，要么发送1表示要发送的帧中的比特率切换。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

In RX or GW mode, the CFBRS bit is updated with the BRS bit value of the CAN-FD frame when it has been received, indicating whether there is a bit rate switch (1) or (0) on the CAN-FD frame.

In RX or GW mode, 0 is stored to the CFBRS bit when the received FDF bit is 0, this means a CAN 2.0 frame is received.

Note: This bit is not available in the classical CAN function.

CFFDF bit (CAN FD Format bit)

In TX mode, you can read and write from FIFO buffers. In this mode, the CAN-FD module either transmits a 0 to indicate a CAN 2.0 frame is to be transmitted or a 1 to indicate a CAN-FD frame is to be transmitted.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

In RX or GW mode, the CFFDF bit is updated with the FDF bit value of the CAN frame when it has been received, indicating whether it is a CAN 2.0 frame (0) or a CAN-FD frame (1).

Note: This bit is not available in the classical CAN function.

CFIFL[1:0] bits (COMMON FIFO Buffer Information Label Field)

If the Common FIFO is configured in TX mode, the value programmed in CFDCFFDCSTSn.CFIFL[1:0] is stored together with additional message information, to the TX History List after successful transmission of the message.

The information label value from the related Global Acceptance Filter List entry is stored in these bits (if FIFO is configured in either RX or GW mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

CFPTR[15:0] bits (Common FIFO Buffer Pointer Field)

If the Common FIFO is configured in TX mode, the value programmed in CFDCFFDCSTSn.CFPTR[15:0] is stored together with additional message information, to the TX History List after successful transmission of the message.

The pointer value from the related Global Acceptance Filter List entry is stored in these bits (if FIFO is configured in either RX or GW mode).

In TX mode, you can read and write from FIFO buffers.

In RX mode, you can only read data from FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

32.2.87.13 CFDCFDFpn_i : Common FIFO Access Data Field p Register n Channel i (p = 0 to 15, n = 0 to 2, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x640C + 0x004 × p + 0x080 × n + 0x180 × i

Bit position:	31							24	23							16	15							8	7							0
Bit field:	CFDB((p * 4) + 3)[7:0]								CFDB((p * 4) + 2)[7:0]								CFDB((p * 4) + 1)[7:0]								CFDB((p * 4)[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFDB((p * 4)[7:0]	Common FIFO Buffer Data Bytes ((p * 4)	R/W
15:8	CFDB((p * 4) + 1)[7:0]	Common FIFO Buffer Data Bytes ((p * 4) + 1)	R/W
23:16	CFDB((p * 4) + 2)[7:0]	Common FIFO Buffer Data Bytes ((p * 4) + 2)	R/W

在RX或GW模式下，CFBRS位在接收到CAN-FD帧后用BRS位值更新，指示CAN-FD帧上是否有比特率切换（1）或（0）。

在RX或GW模式下，当接收到的FDF位为0时，将0存储到CFBRS位，这意味着接收到CAN2.0帧。

Note: 该位在经典CAN功能中不可用。

CFFDF位（CANFD格式位）

在TX模式下，您可以从FIFO缓冲区读取和写入。在这种模式下，CAN-FD模块要么发送一个0来表示一个将发送CAN2.0帧或1表示要发送CAN-FD帧。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

在RX或GW模式下，CFFDF位在接收到CAN帧时更新为CAN帧的FDF位值，指示它是CAN2.0帧（0）还是CAN-FD帧（1）。

Note: 该位在经典CAN功能中不可用。

CFIFL[1:0]位（通用FIFO缓冲区信息标签字段）

如果CommonFIFO配置为TX模式，则在成功发送消息后，CFDCFFDCSTSn.CFIFL[1:0]中编程的值与附加消息信息一起存储到TX历史列表中。

来自相关GlobalAcceptanceFilterList条目的信息标签值存储在这些位中（如果FIFO配置为RX或GW模式）。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

CFPTR[15:0]位（通用FIFO缓冲区指针字段）

如果CommonFIFO配置为TX模式，则在成功传输消息后，CFDCFFDCSTSn.CFPTR[15:0]中编程的值与附加消息信息一起存储到TX历史列表中。

来自相关全局接受过滤器列表条目的指针值存储在这些位中（如果FIFO被配置为RX or GW mode).

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

32.2.87.13 CFDCFDFpn_i:公共FIFO访问数据字段p寄存器n通道i(p=0到15 n=0到2 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x640C + 0x004 × p + 0x080 × n + 0x180 × i

Bit position:	31							24	23							16	15							8	7							0
Bit field:	CFDB((p * 4) + 3)[7:0]								CFDB((p * 4) + 2)[7:0]								CFDB((p * 4) + 1)[7:0]								CFDB((p * 4)[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CFDB((p * 4)[7:0]	公共FIFO缓冲区数据字节((p*4)	R/W
15:8	CFDB((p * 4) + 1)[7:0]	公共FIFO缓冲区数据字节((p*4)+1)	R/W
23:16	CFDB((p * 4) + 2)[7:0]	公共FIFO缓冲区数据字节((p*4)+2)	R/W

Bit	Symbol	Function	R/W
31:24	CFDB((p * 4) + 3) [7:0]	Common FIFO Buffer Data Bytes ((p * 4) + 3)	R/W

i = Channel number

The FIFO Access Data Field p Registers n (p = 0 to 15, n = 0 to 2) store data bytes (p * 4) to data bytes ((p * q) + 3) of the message.

In TX mode, you can read data from the FIFO, only for the current entry based on the write pointer value, and not for the other entries.

CFDB((p * 4)[7:0] bits (Common FIFO Buffer Data Bytes ((p * 4))

The CFDB((p * 4)[7:0] bits store data bytes ((p * 4) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

In RX or GW mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCCn.CFPLS.*1

CFDB((p * 4) + 1)[7:0] bits (Common FIFO Buffer Data Bytes ((p * 4) + 1))

The CFDB((p * 4) + 1)[7:0] bits store data bytes ((p * 4) + 1) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

In RX or GW mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCCn.CFPLS.*1

CFDB((p * 4) + 2)[7:0] bits (Common FIFO Buffer Data Bytes ((p * 4) + 2))

The CFDB((p * 4) + 2)[7:0] bits store data bytes ((p * 4) + 2) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

In RX or GW mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCCn.CFPLS.*1

CFDB((p * 4) + 3)[7:0] bits (Common FIFO Buffer Data Bytes ((p * 4) + 3))

The CFDB((p * 4) + 3)[7:0] bits store data bytes ((p * 4) + 3) of the message present in the FIFO buffer.

In TX mode, you can read and write from the FIFO buffers.

In RX mode, you can only read data from the FIFO buffers.

In GW mode, you cannot write data to the FIFO buffers.

In RX or GW mode, unused data bytes are filled with 0x00, according to their configured data payload size CFDCFCCn.CFPLS.*1

Note 1. In RX or GW mode, unused data bytes are filled with 0x00 according to the configured data payload size CFDCFCCn.CFPLS, which is a CAN-FD feature not found in classical CAN.

Bit	Symbol	Function	R/W
31:24	CFDB((p * 4) + 3) [7:0]	公共FIFO缓冲区数据字节((p*4)+3)	R/W

i=通道号

FIFO访问数据字段p寄存器n(p=0到15，n=0到2)将数据字节(p*4)存储到消息的数据字节((p*q)+3)。

在TX模式下，您可以从FIFO中读取数据，仅针对基于写指针值的当前条目，而不能针对其他条目。

CFDB((p*4)[7:0]bits(通用FIFO缓冲区数据字节((p*4))

CFDB((p*4)[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

在RX或GW模式下，未使用的数据字节根据其配置的数据有效负载大小填充为0x00 CFDCFCCn.CFPLS.*1

CFDB((p*4)+1)[7:0]位（通用FIFO缓冲区数据字节((p*4)+1)）

CFDB((p*4)+1)[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)+1)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

在RX或GW模式下，未使用的数据字节根据其配置的数据有效负载大小填充为0x00 CFDCFCCn.CFPLS.*1

CFDB((p*4)+2)[7:0]位（通用FIFO缓冲区数据字节((p*4)+2)）

CFDB((p*4)+2)[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)+2)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

在RX或GW模式下，未使用的数据字节根据其配置的数据有效负载大小填充为0x00 CFDCFCCn.CFPLS.*1

CFDB((p*4)+3)[7:0]位（通用FIFO缓冲区数据字节((p*4)+3)）

CFDB((p*4)+3)[7:0]位存储FIFO缓冲区中存在的消息的数据字节((p*4)+3)。

在TX模式下，您可以从FIFO缓冲区读取和写入。

在RX模式下，您只能从FIFO缓冲区读取数据。

在GW模式下，您不能将数据写入FIFO缓冲区。

在RX或GW模式下，未使用的数据字节根据其配置的数据有效负载大小填充为0x00 CFDCFCCn.CFPLS.*1

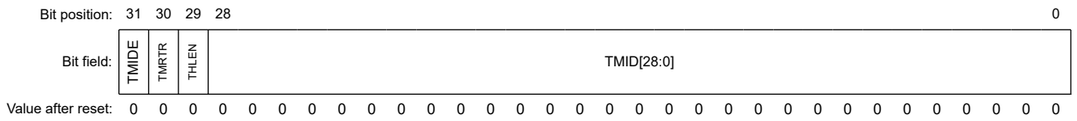
注1.在RX或GW模式下，未使用的数据字节根据配置的数据负载大小用0x00填充 CFDCFCCn.CFPLS，这是经典CAN中没有的CAN-FD功能。

RA生态工作室

32.2.87.14 CFDTMIDn_i : TX Message Buffer ID Register n Channel i (n = 0 to 7, 32 to 39, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0000 + 0x080 × n + 0x2000 × i



Bit	Symbol	Function	R/W
28:0	TMID[28:0]	TX Message Buffer ID Field STD-ID/EXT-ID fields	R/W
29	THLEN	Tx History List Entry 0: Entry not stored in THL after successful TX 1: Entry stored in THL after successful TX	R/W
30	TMRTR	TX Message Buffer RTR bit 0: Data frame 1: Remote frame	R/W
31	TMIDE	TX Message Buffer IDE bit 0: STD-ID is transmitted 1: EXT-ID is transmitted	R/W

Each TX Message Buffer ID Registers n (n = 0 to 7, 32 to 39) are used to store the ID, IDE, RTR fields and history configuration of the message to be transmitted from the associated buffer.

TMID[28:0] bits (TX Message Buffer ID Field)

The TMID[28:0] bits are bits of the STD-ID/EXT-ID fields of the message stored in this TX message buffer.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

THLEN bit (Tx History List Entry)

The THLEN bit controls the storage of an entry corresponding to the transmitted message in the TX History list at the end of a successful transmission.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

TMRTR bit (TX Message Buffer RTR bit)

The TMRTR bit selects whether a data frame or remote frame is to be transmitted from this TX message buffer.

Note: There are no remote frames in CAN-FD format. For a CAN-FD transmission (CFDTMFDCTRn.CFFDF = 1), this bit is always transmitted dominant (data frame).

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

TMIDE bit (TX Message Buffer IDE bit)

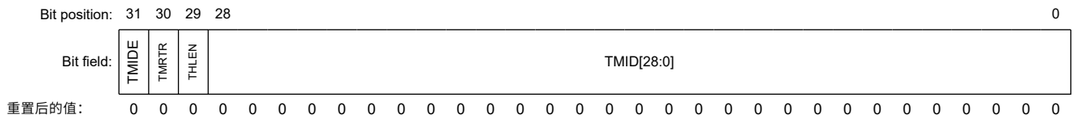
The TMIDE bit selects whether a message with EXT-ID or STD-ID is to be transmitted from this TX message buffer.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

32.2.87.14 CFDTMIDn_i:TX消息缓冲区ID寄存器n通道i(n=0到7 32到39 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0000 + 0x080 × n + 0x2000 × i



Bit	Symbol	Function	R/W
28:0	TMID[28:0]	TX消息缓冲区ID字段 STD-ID/EXT-ID fields	R/W
29	THLEN	Tx历史列表条目 0：成功TX后条目不存储在THL中1：成功TX后条目存储在THL	R/W
30	TMRTR	TX报文缓冲区RTR位 0：数据帧1：远程帧	R/W
31	TMIDE	TX消息缓冲区IDE位 0：发送STD-ID1：发送EXT-ID	R/W

每个TX报文缓冲区ID寄存器n（n=0到7、32到39）用于存储要从相关缓冲区发送的报文的ID、IDE、RTR字段和历史配置。

TMID[28:0]位（TX消息缓冲区ID字段）

TMID[28:0]位是存储在此TX消息缓冲区中的消息的STD-IDEXT-ID字段的位。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

THLEN位（Tx历史列表条目）

THLEN位控制在成功发送结束时将对应于发送消息的条目存储在TX历史列表中。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

TMRTR位（TX报文缓冲区RTR位）

TMRTR位选择是从该TX报文缓冲区发送数据帧还是远程帧。

Note: CAN-FD格式中没有远程帧。对于CAN-FD传输（CFDTMFDCTRn.CFFDF=1），该位始终为显性传输（数据帧）。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

TMIDE位（TX消息缓冲区IDE位）

TMIDE位选择是从该TX报文缓冲区发送带有EXT-ID还是STD-ID的报文。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

32.2.87.15 CFDTMPTRn_i : TX Message Buffer Pointer Register n Channel i (n = 0 to 7, 32 to 39, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0004 + 0x080 × n + 0x2000 × i

Bit position:	31																													0
Bit field:	TMDLC[3:0]	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	The read values are undefined. The write value should be 0.	R/W
31:28	TMDLC[3:0]	TX Message Buffer DLC Field Number of data bytes to be transmitted in a CAN frame.	R/W

Each TX Message Buffer Pointer Register n (n = 0 to 7, 32 to 39) is used to store the DLC fields of the message to transmit from the associated buffer.

TMDLC[3:0] bits (TX Message Buffer DLC Field)

The TMDLC[3:0] bits select the number of data bytes to be transmitted from this TX message buffer when the corresponding TMRTR bit is configured as 0.

See Table 5 in ISO 11898-1 (2015) Specification for details in defining the number of data bytes to be transmitted.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

32.2.87.16 CFDTMFDCTRn_i : TX Message Buffer CAN-FD Control Register n Channel i (n = 0 to 7, 32 to 39, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0008 + 0x080 × n + 0x2000 × i

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMPTR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TMIFL[1:0]		—	—	—	—	—	TMFDF	TMBRS	TMESI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMESI*1	Error State Indicator bit 0: CAN-FD frame to transmit by error active node 1: CAN-FD frame to transmit by error passive node	R/W
1	TMBRS*1	Bit Rate Switch bit 0: CAN-FD frame to transmit with no bit rate switch 1: CAN-FD frame to transmit with bit rate switch	R/W
2	TMFDF*1	CAN FD Format bit 0: Non CAN-FD frame to transmit 1: CAN-FD frame to transmit	R/W
7:3	—	The read values are undefined. The write value should be 0.	R/W
9:8	TMIFL[1:0]	TX Message Buffer Information Label Field	R/W
15:10	—	The read values are undefined. The write value should be 0.	R/W

32.2.87.15 CFDTMPTRn_i:TX消息缓冲区指针寄存器n通道i(n=0到7 32到39 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0004 + 0x080 × n + 0x2000 × i

Bit position:	31																													0
Bit field:	TMDLC[3:0]	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
27:0	—	读取的值未定义。写入值应为0。	R/W
31:28	TMDLC[3:0]	TX消息缓冲区DLC字段 CAN帧中要传输的数据字节数。	R/W

每个TX消息缓冲区指针寄存器n（n=0到7、32到39）用于存储要从相关缓冲区发送的消息的DLC字段。

TMDLC[3:0]位（TX消息缓冲区DLC字段）

当相应的TMRTR位配置为0时，TMDLC[3:0]位选择要从该TX报文缓冲区发送的数据字节数。

有关定义要传输的数据字节数的详细信息，请参见ISO11898-1(2015)规范中的表5。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

32.2.87.16 CFDTMFDCTRn_i:TX报文缓冲器CAN-FD控制寄存器n通道i(n=0到7 32到39 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0008 + 0x080 × n + 0x2000 × i

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	TMPTR[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	TMIFL[1:0]		—	—	—	—	—	TMFDF	TMBRS	TMESI
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TMESI*1	错误状态指示位 0：由错误主动节点发送的CAN-FD帧1：由错误被动节点发送的CAN-FD帧	R/W
1	TMBRS*1	比特率切换位 0：CAN-FD帧传输，无码率切换1：CAN-FD帧传输，码率切换	R/W
2	TMFDF*1	CANFD格式位 0：发送非CAN-FD帧1：发送CAN-FD帧	R/W
7:3	—	读取的值未定义。写入值应为0。	R/W
9:8	TMIFL[1:0]	TX消息缓冲区信息标签字段	R/W
15:10	—	读取的值未定义。写入值应为0。	R/W

Bit	Symbol	Function	R/W
31:16	TMPTR[15:0]	TX Message Buffer Pointer Field	R/W

Note 1. This bit is not available in the classical CAN function.

The TX Message Buffer CAN-FD Control Registers n (n = 0 to 7, 32 to 39) show the status of the FDF, BRS and ESI bits, including the pointer fields of the CAN-FD frame to be transmitted.

TMESI bit (Error State Indicator bit)

If the channel is not in error passive, then the TMESI bit equals the write value, otherwise it is a don't care and the bit is transmitted as 1 on the CAN bus, indicating this is an error passive node.

Do not write to the TMESI bit when the related CAN-FD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMBRS bit (Bit Rate Switch bit)

Do not write to the TMBRS bit when the related CAN-FD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMFDF bit (CAN FD Format bit)

Do not write to the TMFDF bit when the related CAN-FD channel is in CH_SLEEP mode.

Note: This bit is not available in the classical CAN function.

TMIFL[1:0] bits (TX Message Buffer Information Label Field)

The TMIFL[1:0] bits store the information label value to be copied, together with additional message information, in the TX History List after successful transmission of the message.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

TMPTR[15:0] bits (TX Message Buffer Pointer Field)

The TMPTR[15:0] bits store the pointer value to be copied, together with additional message information in the TX History List after successful transmission of the message.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

32.2.87.17 CFDTMDFpn_i : TX Message Buffer Data Field p Register n Channel i (p = 0 to 15, n = 0 to 7, 32 to 39, i = 0, 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0000C + 0x004 × p + 0x080 × n + 0x2000 × i

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	TMDB((p * 4) + 3)[7:0]	TMDB((p * 4) + 2)[7:0]	TMDB((p * 4) + 1)[7:0]	TMDB((p * 4)[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	TMDB((p * 4)[7:0]	TX Message Buffer Data Byte ((p * 4)	R/W
15:8	TMDB((p * 4) + 1)[7:0]	TX Message Buffer Data Byte ((p * 4) + 1)	R/W
23:16	TMDB((p * 4) + 2)[7:0]	TX Message Buffer Data Byte ((p * 4) + 2)	R/W
31:24	TMDB((p * 4) + 3)[7:0]	TX Message Buffer Data Byte ((p * 4) + 3)	R/W

i = Channel number

Bit	Symbol	Function	R/W
31:16	TMPTR[15:0]	TX消息缓冲区指针字段	R/W

注1.该位在经典CAN功能中不可用。

TX报文缓冲区CAN-FD控制寄存器n（n=0到7、32到39）显示FDF、BRS和ESI位的状态，包括要发送的CAN-FD帧的指针字段。

TMESI位（错误状态指示位）

如果通道不是被动错误，则TMESI位等于写入值，否则为无关位，该位在CAN总线上传输为1，表示这是一个错误被动节点。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入TMESI位。

Note: 该位在经典CAN功能中不可用。

TMBRS位（比特率切换位）

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入TMBRS位。

Note: 该位在经典CAN功能中不可用。

TMFDF位（CANFD格式位）

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入TMFDF位。

Note: 该位在经典CAN功能中不可用。

TMIFL[1:0]位（TX消息缓冲区信息标签字段）

TMIFL[1:0]位将要复制的信息标签值与附加消息信息一起存储在TX中成功传输消息后的历史列表。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

TMPTR[15:0]位（TX消息缓冲区指针字段）

TMPTR[15:0]位存储要复制的指针值，以及TX历史记录中的附加消息信息成功传输消息后的列表。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

32.2.87.17 CFDTMDFpn_i:TX消息缓冲区数据字段p寄存器n通道i(p=0到15 n=0到7 32到39 i=0 1)

Base address: CANFD = 0x400B_0000

Offset address: 0x1_0000C + 0x004 × p + 0x080 × n + 0x2000 × i

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	TMDB((p * 4) + 3)[7:0]	TMDB((p * 4) + 2)[7:0]	TMDB((p * 4) + 1)[7:0]	TMDB((p * 4)[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	TMDB((p * 4)[7:0]	TX消息缓冲区数据字节((p*4)	R/W
15:8	TMDB((p * 4) + 1)[7:0]	TX消息缓冲区数据字节((p*4)+1)	R/W
23:16	TMDB((p * 4) + 2)[7:0]	TX消息缓冲区数据字节((p*4)+2)	R/W
31:24	TMDB((p * 4) + 3)[7:0]	TX消息缓冲区数据字节((p*4)+3)	R/W

i=通道号

Each TX Message Buffer Data Field p Register n (p = 0 to 15, n = 0 to 7, 32 to 39) is used to store data bytes ((p * q) + (q - 4)) to data bytes ((p * q) + (q - 1)) of the message to transmit from the associated buffer.

TMDB((p * 4)[7:0] bits (TX Message Buffer Data Byte ((p * 4))

Data bytes ((p * 4)[7:0] of the message stored in the TX message buffer.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

TMDB((p * 4) + 1)[7:0] bits (TX Message Buffer Data Byte ((p * 4) + 1))

Data bytes ((p * 4) + 1)[7:0] of the message stored in the TX message buffer.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

TMDB((p * 4) + 2)[7:0] bits (TX Message Buffer Data Byte ((p * 4) + 2))

Data bytes ((p * 4) + 2)[7:0] of the message stored in the TX message buffer.

Do not write to these bits when the related CAN-FD channel is in CH_SLEEP mode.

TMDB((p * 4) + 3)[7:0] bits (TX Message Buffer Data Byte ((p * 4) + 3))

Data bytes ((p * 4) + 3)[7:0] of the message stored in the TX message buffer.

Do not write to these bits when the related CAN-FD hannel is in CH_SLEEP mode.

32.3 Modes of Operation

32.3.1 Overview

The modes of the CAN-FD module can be classified into 2 groups:

- Global modes
- Channel modes

32.3.2 Global Modes

These modes are applicable for the complete CAN-FD module and therefore are called Global modes. The global modes of the CAN-FD module are:

- Global Sleep
- Global Reset
- Global Halt
- Global Operation.

Figure 32.2 shows the possible transitions between the Global modes.

每个TX报文缓冲区数据字段p寄存器n(p=0到15 n=0到7 32到39)用于存储数据字节((p*q)+(q4))到数据字节((p*q)+(q1))从相关缓冲区传输的消息。

TMDB((p*4)[7:0]bits(TX报文缓冲区数据字节((p*4))

存储在TX消息缓冲区中的消息的数据字节((p*4)[7:0]。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

TMDB((p*4)+1)[7:0]bits(TX报文缓冲区数据字节((p*4)+1))

存储在TX消息缓冲区中的消息的数据字节((p*4)+1)[7:0]。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

TMDB((p*4)+2)[7:0]bits(TX报文缓冲区数据字节((p*4)+2))

存储在TX消息缓冲区中的消息的数据字节((p*4)+2)[7:0]。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

TMDB((p*4)+3)[7:0]bits(TX报文缓冲区数据字节((p*4)+3))

存储在TX消息缓冲区中的消息的数据字节((p*4)+3)[7:0]。

当相关CAN-FD通道处于CH_SLEEP模式时，请勿写入这些位。

32.3 运作模式

32.3.1 Overview

CAN-FD模块的模式可分为2组：

●全局模式

●频道模式

32.3.2 全局模式

这些模式适用于完整的CAN-FD模块，因此称为全局模式。CAN-FD模块的全局模式有：

●全局睡眠

●全局重置

●全球暂停

●全球运营。

图32.2显示了全局模式之间可能的转换。

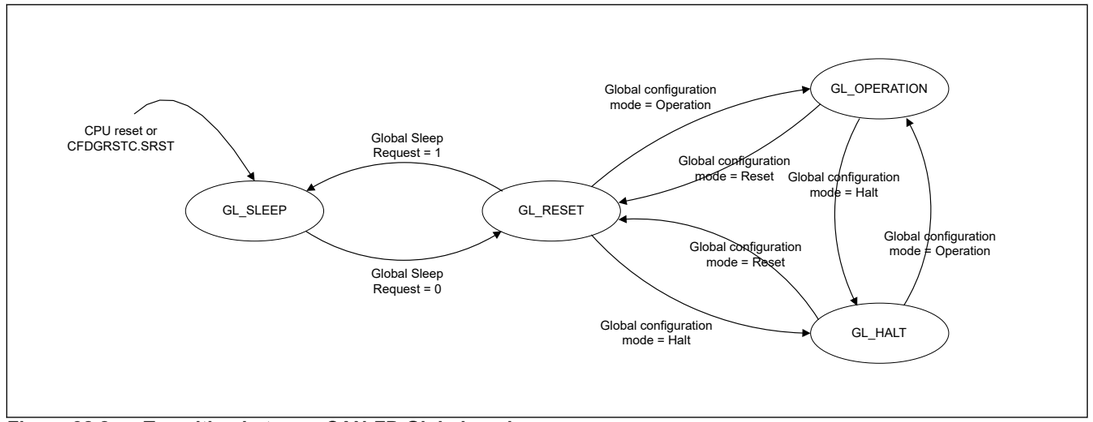


Figure 32.2 Transition between CAN-FD Global modes

Change in the Global mode can affect the Channel mode. Table 32.8 shows the effect of a Global mode transition on a Channel mode.

Table 32.8 Possible CAN-FD Channel modes and Global modes

Current Global mode	Target Global mode			
	Sleep	**Reset**	**Halt**	**Operation**
Sleep		Ch-Sleep: Keep Ch-Reset: N/A Ch-Halt: N/A Ch-Oper: N/A		
Reset	Ch-Sleep: Keep Ch-Reset: → Ch-Sleep Ch-Halt: N/A Ch-Oper: N/A		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A
Halt		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: N/A		Ch-Sleep:Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: N/A
Operation		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: → Ch-Reset	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: → Ch-Halt	

32.3.2.1 Global Sleep Mode

After the release of a hardware reset or after setting and clearing a CFDGRSTC.SRST bit, the CAN-FD module automatically enters Global Sleep mode.

The CAN-FD module also enters the Global Sleep mode when the Global Sleep Request bit is set while it is in Global Reset mode. This control bit cannot be set in Global Halt mode or Global Operation mode.

Setting the Global Sleep Request bit sets all Channel Sleep Request bits and forces all channels into the Channel Sleep mode.

Sleep mode is used for power saving purpose. When CAN-FD module is in Global Sleep mode, only the clock for CPU write access to the Global Sleep Mode Request bit is active. All other clocks are stopped and all other functions of the CAN-FD module are suspended.

Read access from all registers is still possible and all register values are preserved.

After setting the Global Sleep Request bit, it is necessary to confirm that the Global Sleep status has been updated, indicating successful transition to Global Sleep mode before the Global Sleep Request bit can be cleared again.

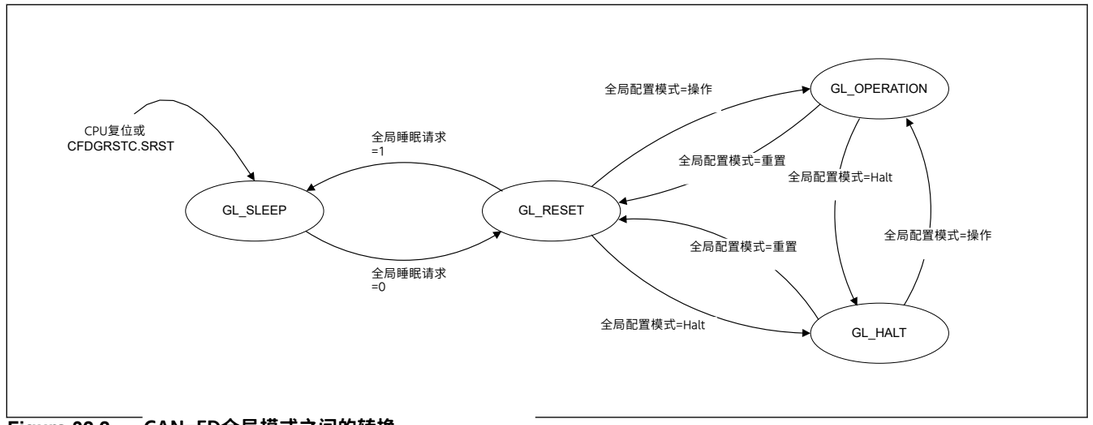


Figure 32.2 CAN-FD全局模式之间的转换

全局模式的变化会影响通道模式。表32.8显示了全局模式转换对频道模式。

Table 32.8 可能的CAN-FD通道模式和全局模式

当前全局模式	目标全局模式			
	Sleep	**Reset**	**Halt**	**Operation**
Sleep		Ch-Sleep: Keep Ch-Reset: N/A Ch-Halt: N/A Ch-Oper: N/A		
Reset	Ch-Sleep: Keep Ch-Reset: → Ch-Sleep Ch-Halt: N/A Ch-Oper: N/A		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: N/A Ch-Oper: N/A
Halt		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: N/A		Ch-Sleep:Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: N/A
Operation		Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: → Ch-Reset Ch-Oper: → Ch-Reset	Ch-Sleep: Keep Ch-Reset: Keep Ch-Halt: Keep Ch-Oper: → Ch-Halt	

32.3.2.1 全局睡眠模式

在释放硬件复位或设置和清除CFDGRSTC.SRST位后，CAN-FD模块自动进入全局休眠模式。

当CAN-FD模块处于全局复位模式时，如果全局睡眠请求位被置位，CAN-FD模块也会进入全局睡眠模式。该控制位不能在GlobalHalt模式或GlobalOperation模式下设置。

设置全局休眠请求位会设置所有通道休眠请求位并强制所有通道进入通道休眠模式。

睡眠模式用于省电目的。当CAN-FD模块处于全局休眠模式时，只有CPU对全局休眠模式请求位进行写访问的时钟有效。所有其他时钟停止，CAN-FD模块的所有其他功能暂停。

仍然可以从所有寄存器进行读取访问，并且所有寄存器值都被保留。

设置全局睡眠请求位后，需要确认全局睡眠状态已更新，表明成功转换到全局睡眠模式，然后才能再次清除全局睡眠请求位。

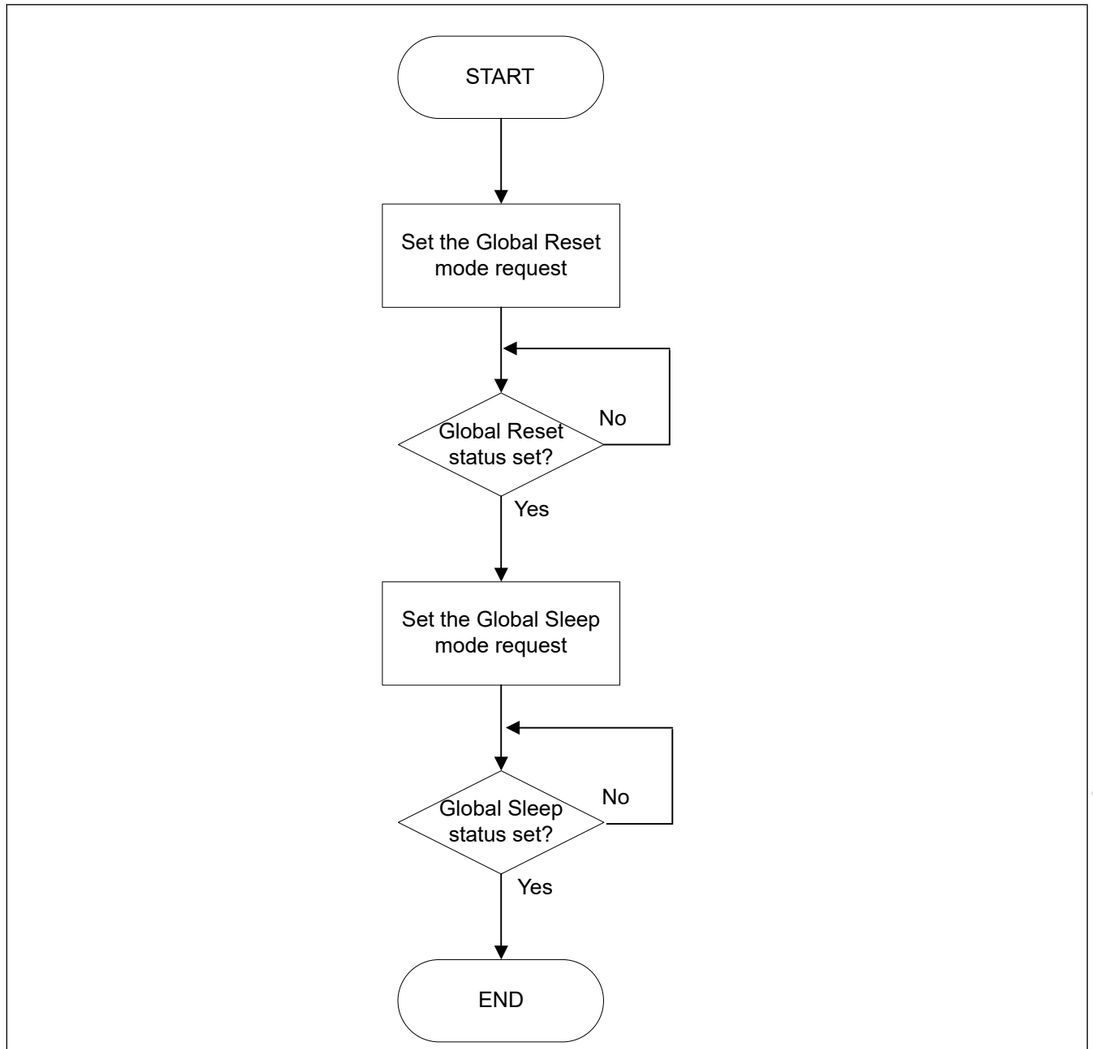


Figure 32.3 Procedure for entering Global Sleep mode

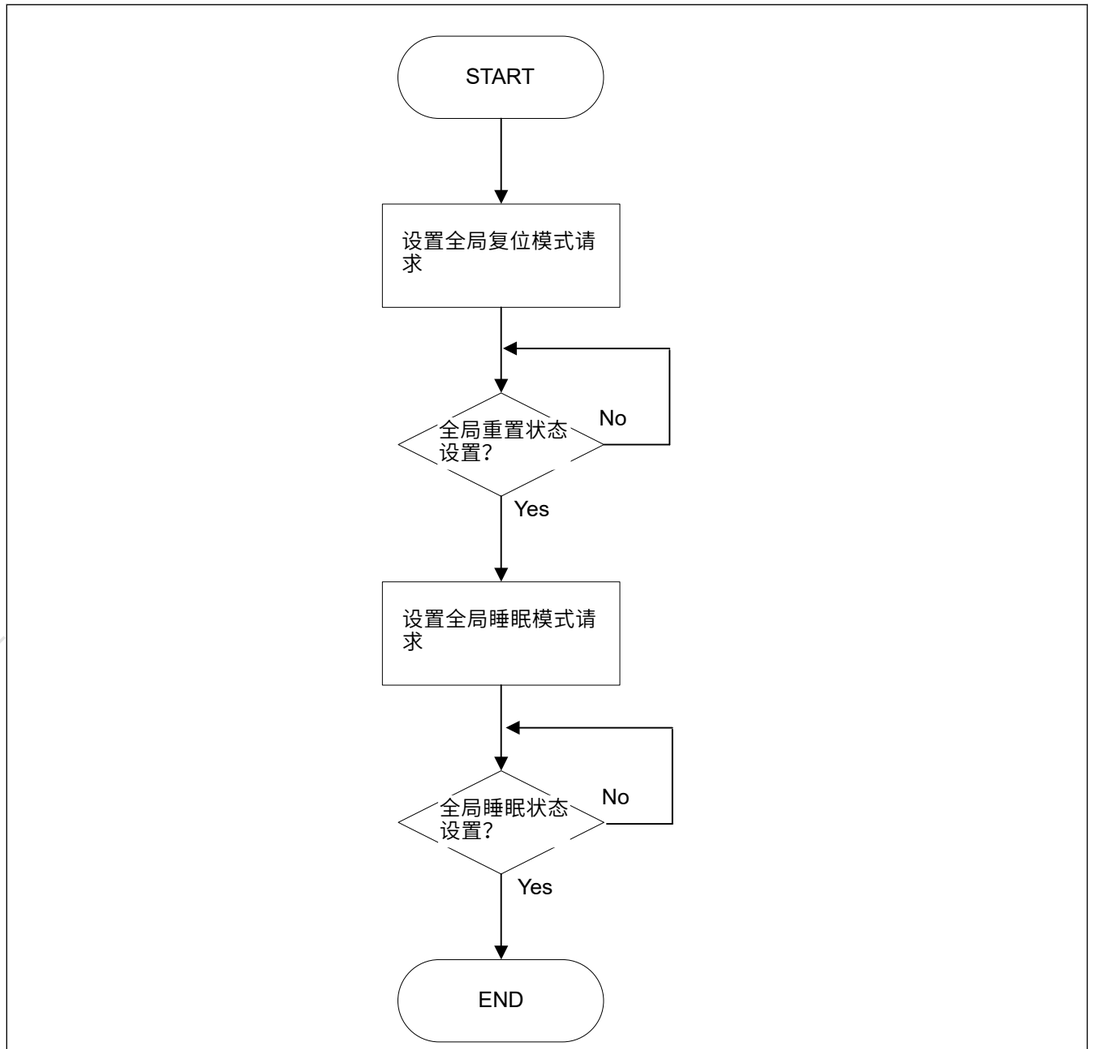


Figure 32.3 进入全局睡眠模式的步骤

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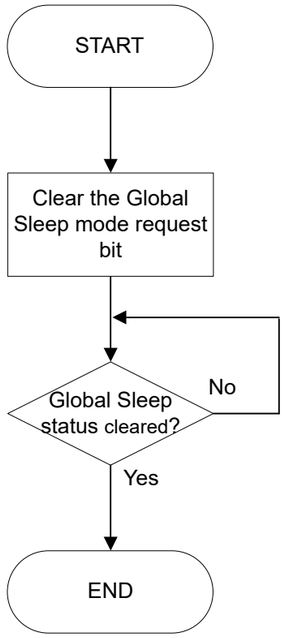

Figure 32.4 Procedure for exiting Global Sleep mode

32.3.2.2 Global Reset Mode

The CAN-FD module enters this mode in the following ways:

- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Reset mode while the CAN-FD module is in Global Halt or Global Operation mode
- Global Sleep Mode Request bit is cleared while CAN-FD module is in Global Sleep mode.

In Global Reset mode, all CAN-FD module functions are suspended and all status and flag registers are initialized.

Additionally all FIFOs and all channel TX Queues are disabled and transmission control bits are cleared.

Configuration registers (except the test mode registers) are not initialized in this mode to their MCU reset values and the CAN-FD module can be configured.

See section 32.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Global Reset mode is performed.

Setting the Global mode to Reset by setting the Global Mode Control bits CFDGCTR.GMDC in the Global Control Register to 01b sets all Channel Mode Control bits CFDCnCTR.CHMDC in the Channel Control Registers to 01b and forces all channels into the Channel Reset mode.

For channels that are already in Channel Reset mode or Channel Sleep mode, this automatic transition is not performed (CFDCnCTR.CHMDC of related channel already set to 01b).

After setting Global Mode Control bit CFDGCTR.GMDC to Reset mode, it is necessary to confirm that the Reset Mode Status bit CFDGSTS.GRSTSTS in the Global Status Register has been updated, indicating successful transition to Global Reset mode before CFDGCTR.GMDC can be changed again.

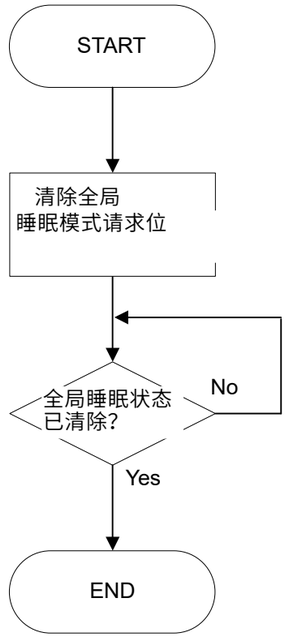

Figure 32.4 退出全局休眠模式的步骤

32.3.2.2 全局重置模式

CAN-FD模块通过以下方式进入该模式：

●全局控制寄存器中的全局模式控制位CFDGCTR.GMDC配置为全局复位模式，而CAN-FD模块处于全局暂停或全局操作模式

●CAN-FD模块处于全局休眠模式时，全局休眠模式请求位被清零。

在全局复位模式下，所有CAN-FD模块功能都被暂停，所有状态和标志寄存器都被初始化。

此外，所有FIFO和所有通道TX队列都被禁用，传输控制位被清除。

配置寄存器（测试模式寄存器除外）在此模式下未初始化为其MCU复位值，并且CAN-FD模块可配置。

请参见第32.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了当转换到全局复位模式时所有寄存器的行为。

通过设置全局控制中的全局模式控制位CFDGCTR.GMDC将全局模式设置为复位寄存器为01b将通道控制寄存器中的所有通道模式控制位CFDCnCTR.CHMDC设置为01b，并强制所有通道进入通道复位模式。

对于已经处于通道复位模式或通道休眠模式的通道，不执行此自动转换（相关通道的CFDCnCTR.CHMDC已设置为01b）。

将全局模式控制位CFDGCTR.GMDC设置为复位模式后，需要确认复位模式GlobalStatusRegister中的状态位CFDGSTS.GRSTSTS已更新，表示成功转换到Global可以再次更改CFDGCTR.GMDC之前的复位模式。

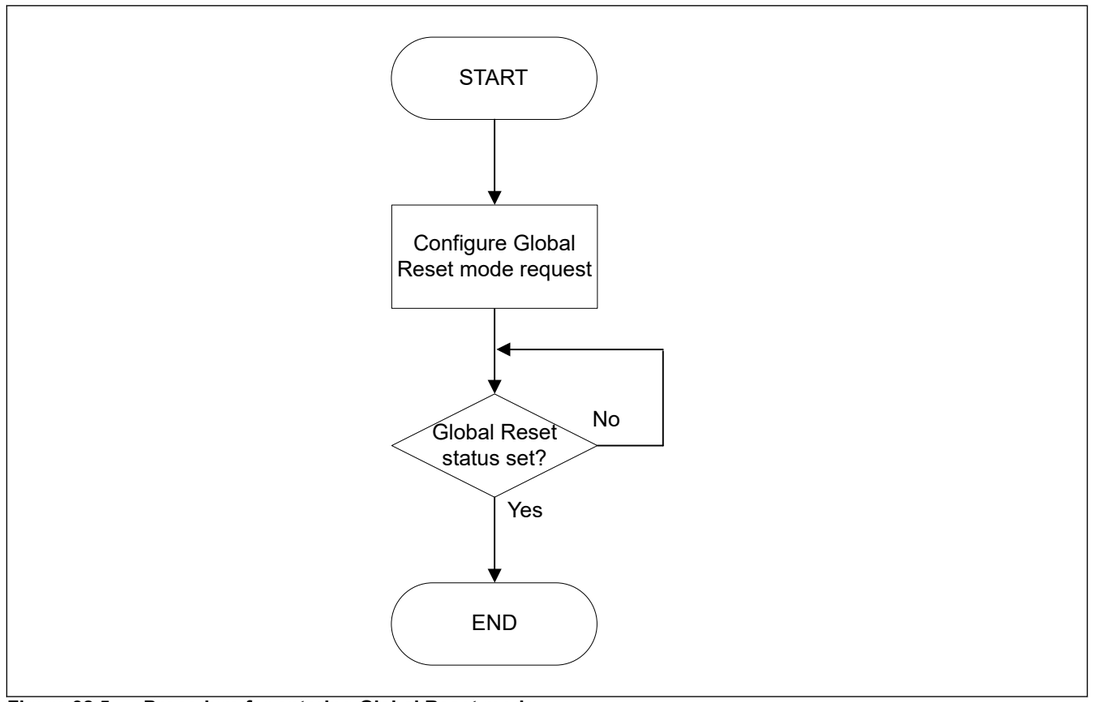

Figure 32.5 Procedure for entering Global Reset mode

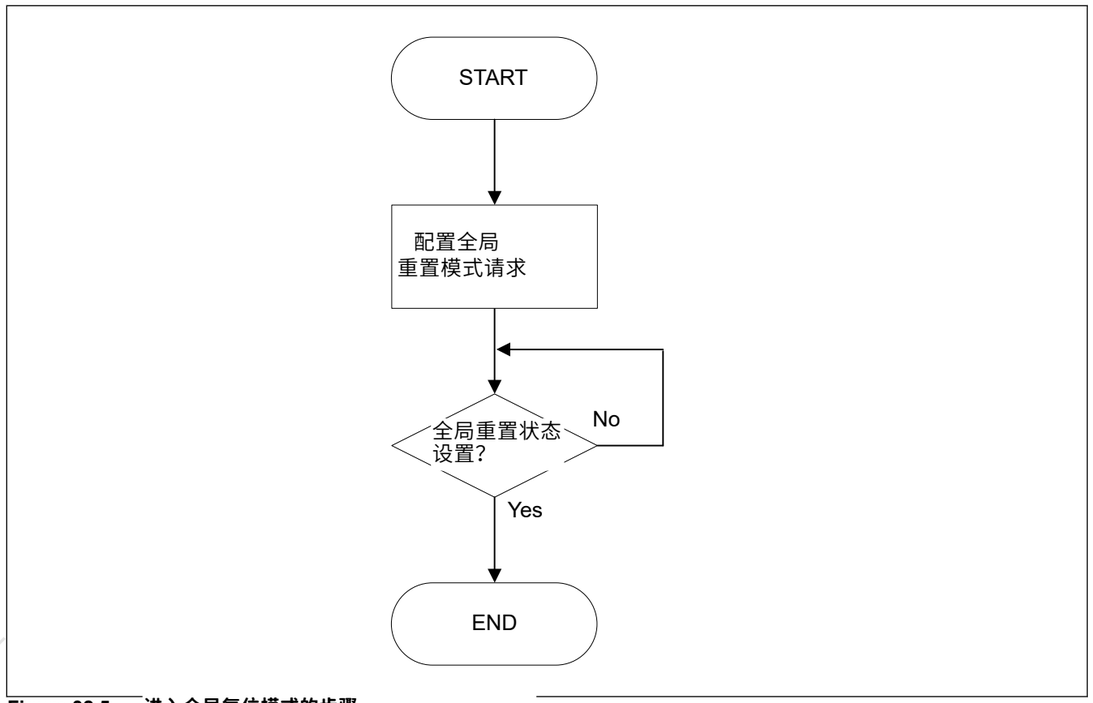

Figure 32.5 进入全局复位模式的步骤

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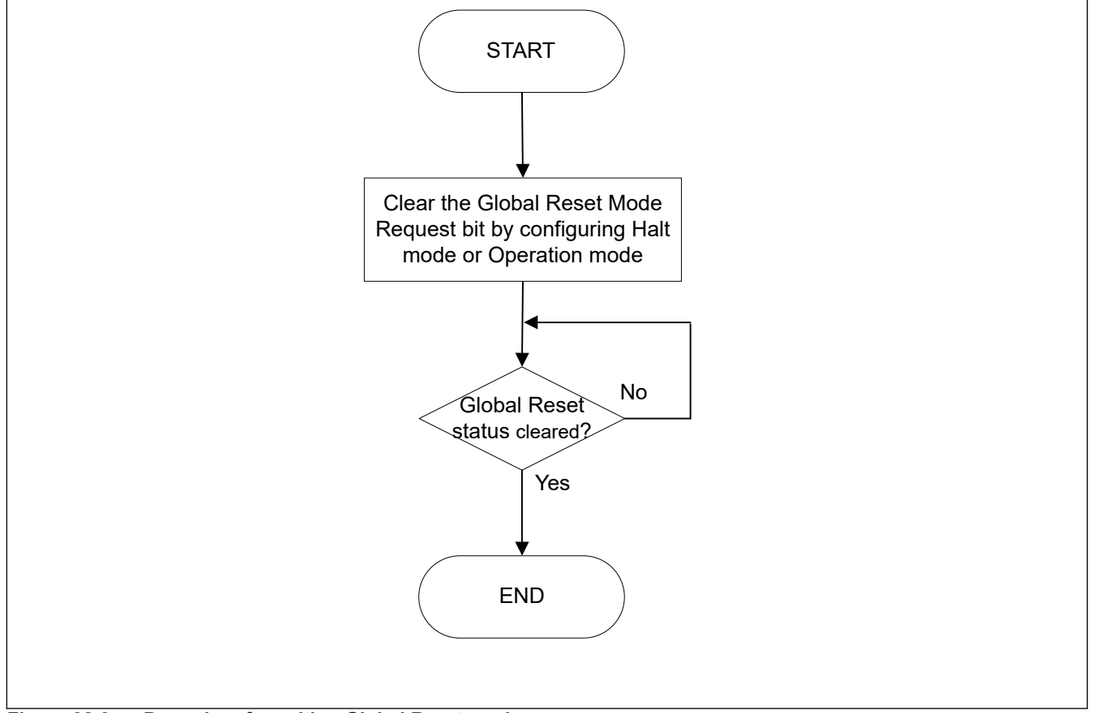

Figure 32.6 Procedure for exiting Global Reset mode

32.3.2.3 Global Halt Mode

The CAN-FD module enters this mode in the following ways:

- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Halt mode while the CAN-FD module is in Global Reset mode:
  - the channels is in either Channel Reset or Channel Sleep mode and remains in this mode
- Global Mode Control bit CFDGCTR.GMDC in the Global Control Register is configured for Global Halt mode while the CAN-FD module is in Global Operation mode:
  - all channels in Channel Reset, Channel Halt, or Channel Sleep mode remain in this mode
  - all channels in Channel Operation mode transit to Channel Halt mode
  - Global Halt Mode Status bit is set when all channels have left Channel Operation mode.

If a transmission or reception is ongoing for a channel, the transition to Channel Halt mode is delayed until completion of the communication.

Similarly, if a channel is in bus-off, the full bus-off recovery sequence may be delayed depending on the channel configuration.

In Global Halt mode, all communications are suspended and CAN-FD logic does not cause any change to the Status and Flag registers (only when a channel is in the bus-off that its REC and TEC values are cleared). Additionally, the test mode configuration and control registers are not initialized in this mode.

The Global Halt mode should be used to configure global module test modes.

See section 32.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Global Halt mode is performed.

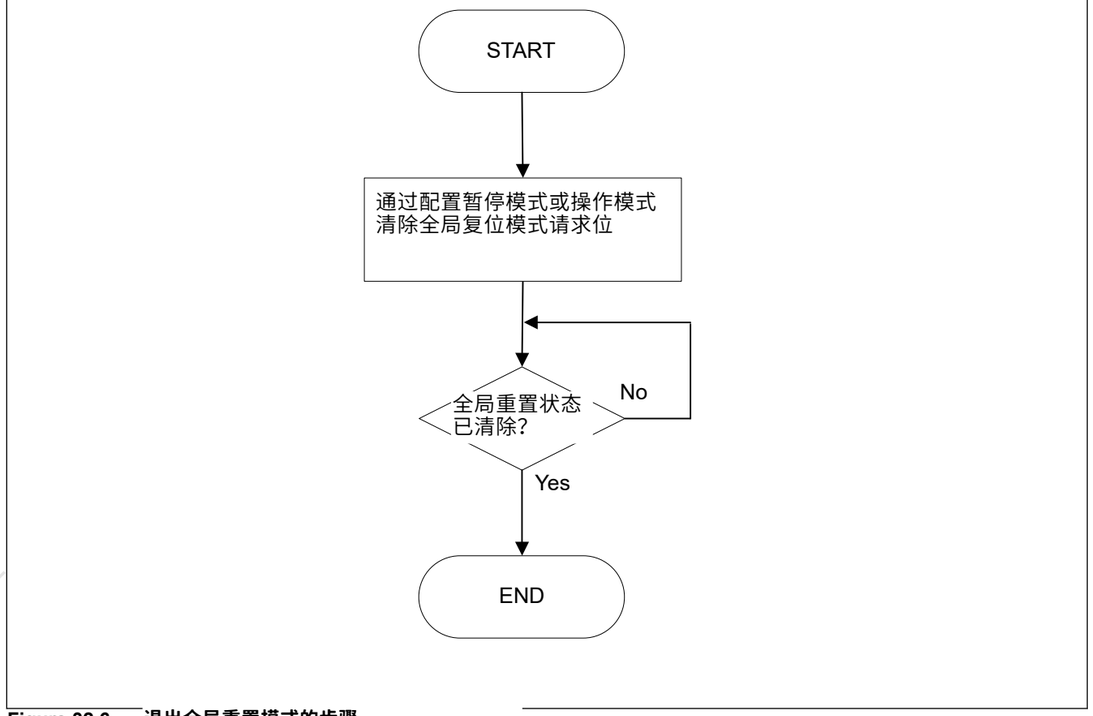

Figure 32.6 退出全局重置模式的步骤

32.3.2.3 全局停止模式

CAN-FD模块通过以下方式进入该模式：

●当CAN-FD模块处于全局复位模式时，全局控制寄存器中的全局模式控制位CFDGCTR.GMDC配置为全局暂停模式：

通道处于通道复位或通道休眠模式并保持在此模式

●当CAN-FD模块处于全局操作模式时，全局控制寄存器中的全局模式控制位CFDGCTR.GMDC配置为全局暂停模式：

处于通道复位、通道暂停或通道休眠模式的所有通道都保持在此模式

通道操作模式中的所有通道转换到通道暂停模式

当所有通道都离开通道操作模式时，设置全局暂停模式状态位。

如果通道正在进行传输或接收，则延迟到通道暂停模式的转换，直到通信完成。

类似地，如果通道处于总线关闭状态，则完全总线关闭恢复序列可能会延迟，具体取决于通道配置。

在GlobalHalt模式下，所有通信都暂停，CAN-FD逻辑不会导致Status和标志寄存器（仅当通道处于总线关闭状态时，其REC和TEC值才被清除）。此外，测试模式配置和控制寄存器在此模式下未初始化。

GlobalHalt模式应该用于配置全局模块测试模式。

请参见第32.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了在转换到全局暂停模式时所有寄存器的行为。

Setting the Global mode to Halt by setting the Global Mode Control bit CFDGCTR.GMDC in the Global Control Register to 10b sets all Channel Mode Control bits CFDCnCTR.CHMDC in the Channel Control Registers to 10b for the channels that are in Channel Operation mode and forces these channels into the Channel Halt mode.

For channels that are already in Channel Reset, Channel Halt, or Channel Sleep mode, this automatic transition is not performed.

Therefore, the Global Halt mode request can be used to shut down all CAN-FD channel communications without loss of messages and disruption on the related CAN bus (no interruption of reception/transmission processes on the channels).

After setting the Global Mode Control bit CFDGCTR.GMDC to Halt mode, it is necessary to confirm that the Halt Mode Status bit CFDGSTS.GHLTSTS in the Global Status Register has been updated to indicate a successful transition to Global Halt mode. Do not specify any other SFR setting until confirming CFDGSTS.GHLTSTS is set.

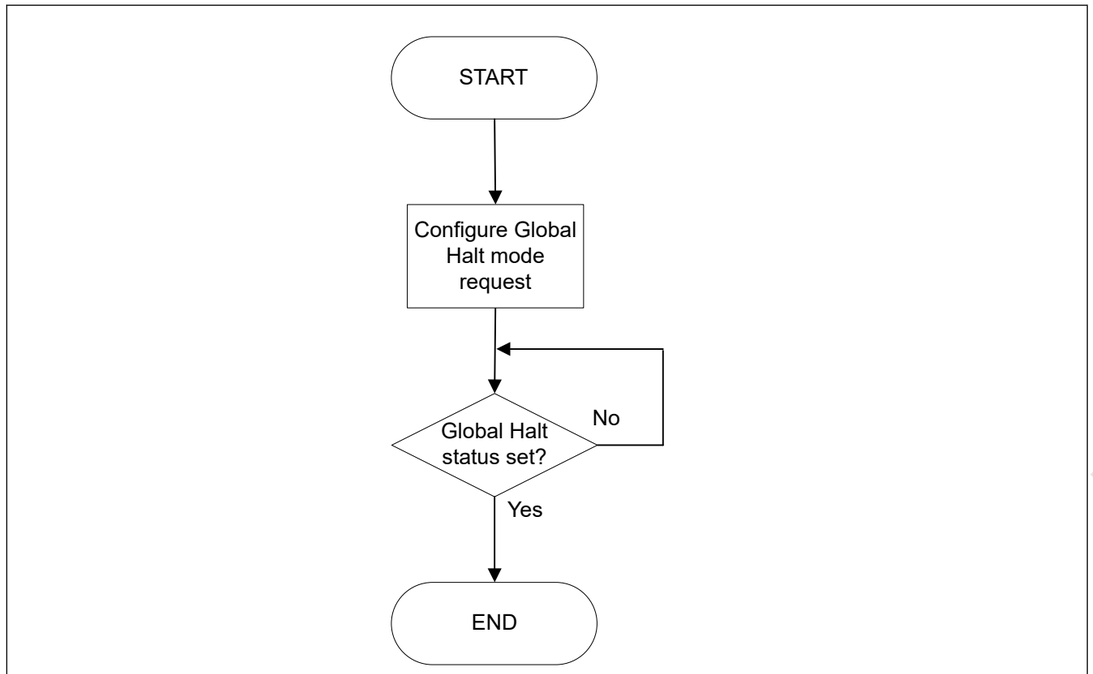

Figure 32.7 Procedure for entering Global Halt mode

通过将全局控制寄存器中的全局模式控制位CFDGCTR.GMDC设置为10b将全局模式设置为暂停，对于处于通道操作模式的通道，将通道控制寄存器中的所有通道模式控制位CFDCnCTR.CHMDC设置为10b并强制这些通道进入通道暂停模式。

对于已经处于通道复位、通道暂停或通道休眠模式的通道，不会执行此自动转换。

因此，全局暂停模式请求可用于关闭所有CAN-FD通道通信，而不会丢失消息和中断相关CAN总线（不会中断通道上的接收传输过程）。

将GlobalModeControl位CFDGCTR.GMDC设置为Halt模式后，需要确认HaltMode全局状态寄存器中的状态位CFDGSTS.GHLTTSTS已更新以指示成功转换到全局暂停模式。在确认设置CFDGSTS.GHLTTSTS之前，不要指定任何其他SFR设置。

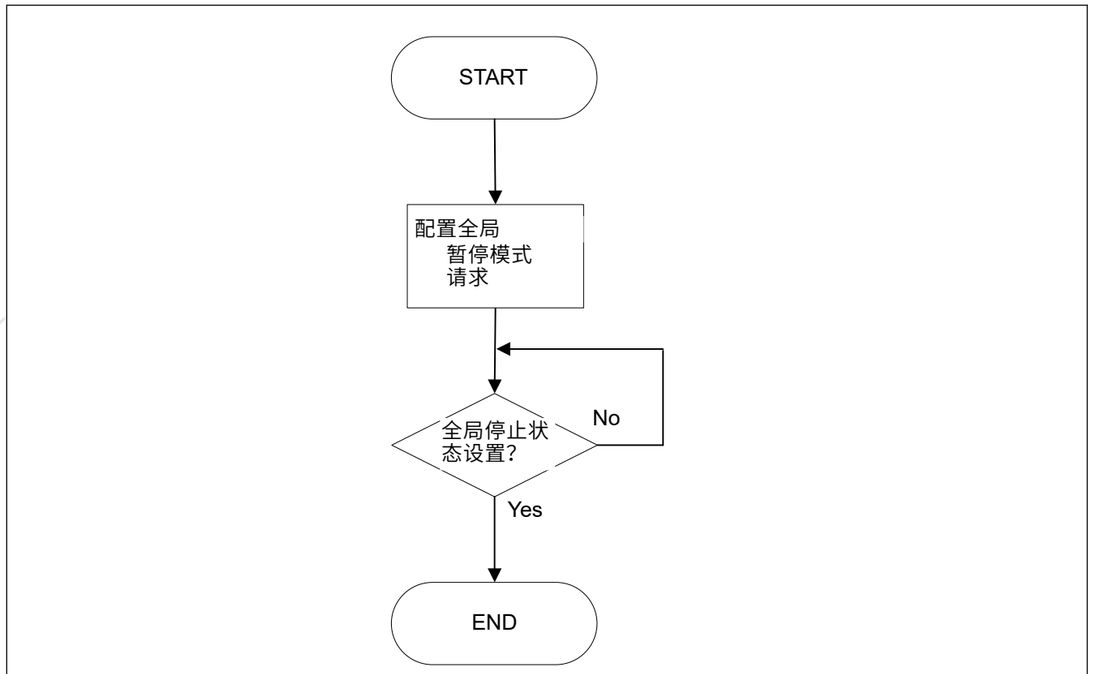

Figure 32.7 进入GlobalHalt模式的步骤

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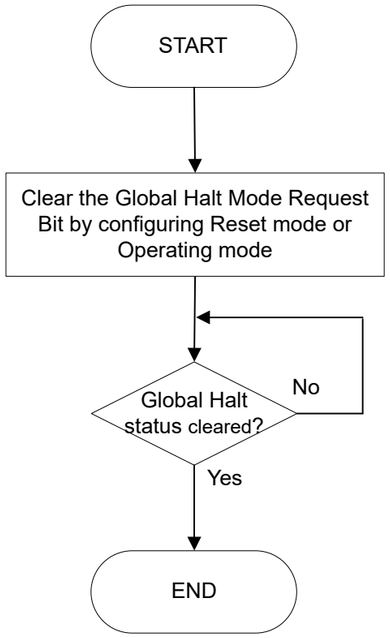

Figure 32.8 Procedure for exiting Global Halt mode

32.3.2.4 Global Operation Mode

The CAN-FD module enters this mode when the Global Mode Configuration bits are set to Global Operation mode.

The CAN-FD channels can only be set to Channel Operation mode and start CAN communication when CAN-FD is in Global Operation mode.

After setting the Global Mode Control bit CFDGCTR.GMDC to Global Operation mode, it is necessary to confirm that the Global Reset Mode Status bit CFDGSTS.GRSTSTS and the Global Halt Mode Status bit CFDGSTS.GHLTSTS in the Global Status Register have been cleared to indicate a successful transition to Global Operation mode before CFDGCTR.GMDC can be modified again.

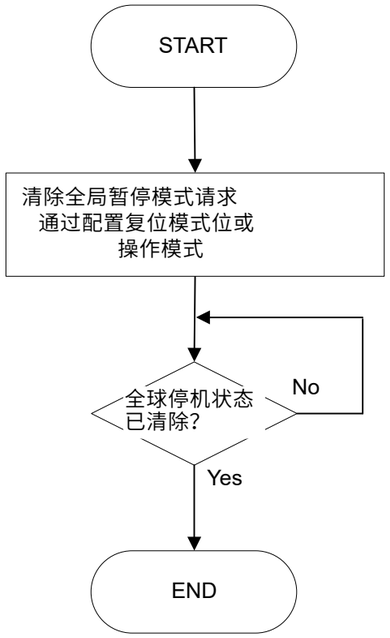

Figure 32.8 退出全局暂停模式的步骤

32.3.2.4 全球运营模式

当全局模式配置位设置为全局操作模式时，CAN-FD模块进入此模式。

CAN-FD通道只能设置为ChannelOperation模式并在CAN-FD处于工作状态时启动CAN通信
全局操作模式。

将全局模式控制位CFDGCTR.GMDC设置为全局操作模式后，需要确认
全局复位模式状态位CFDGSTS.GRSTSTS和全局暂停模式状态位CFDGSTS.GHLTSTS在
全局状态寄存器已被清除以指示成功转换到全局操作模式之前
CFDGCTR.GMDC可以再次修改。

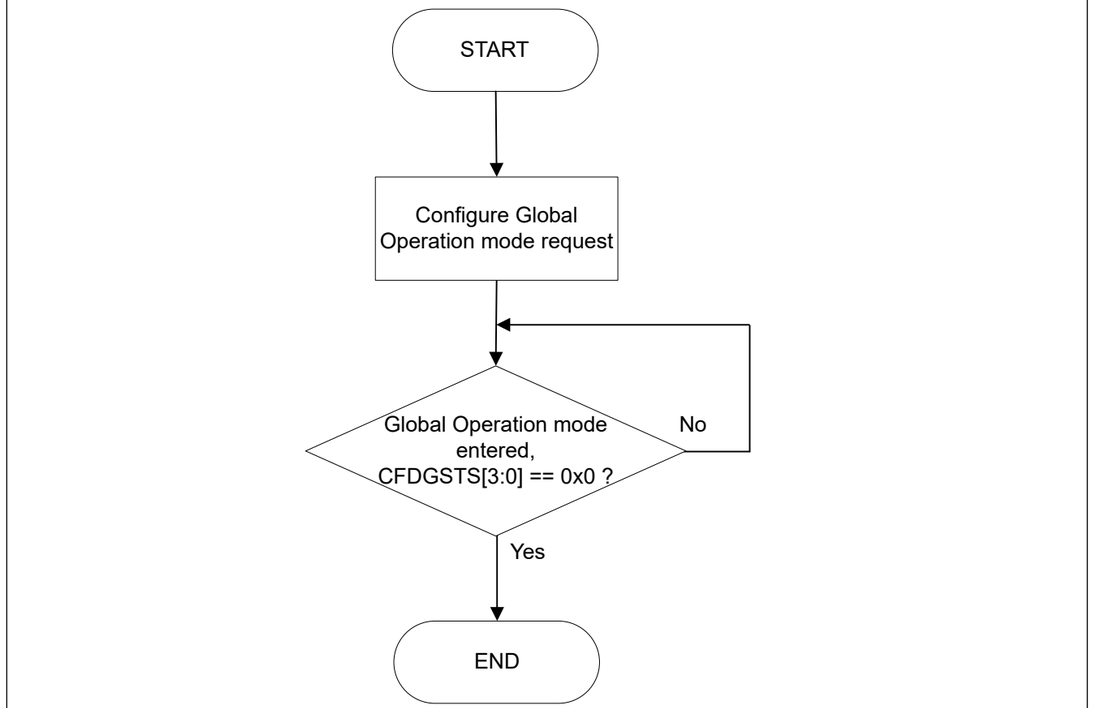

Figure 32.9 Procedure for entering Global Operation mode

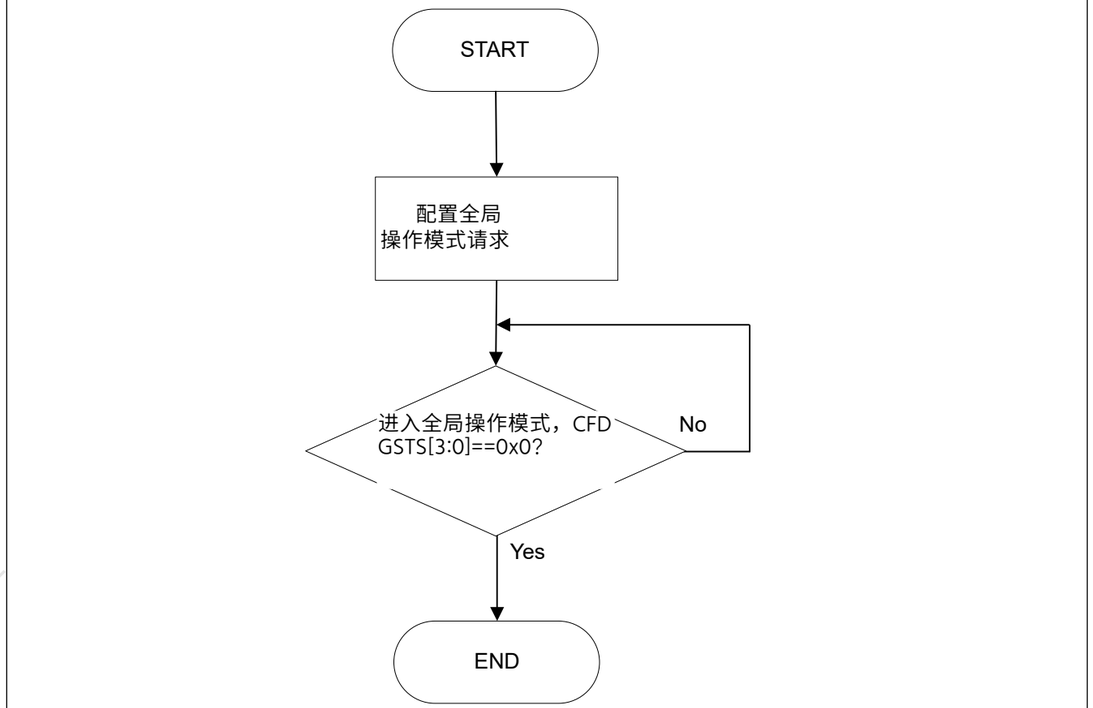

Figure 32.9 进入全局操作模式的步骤

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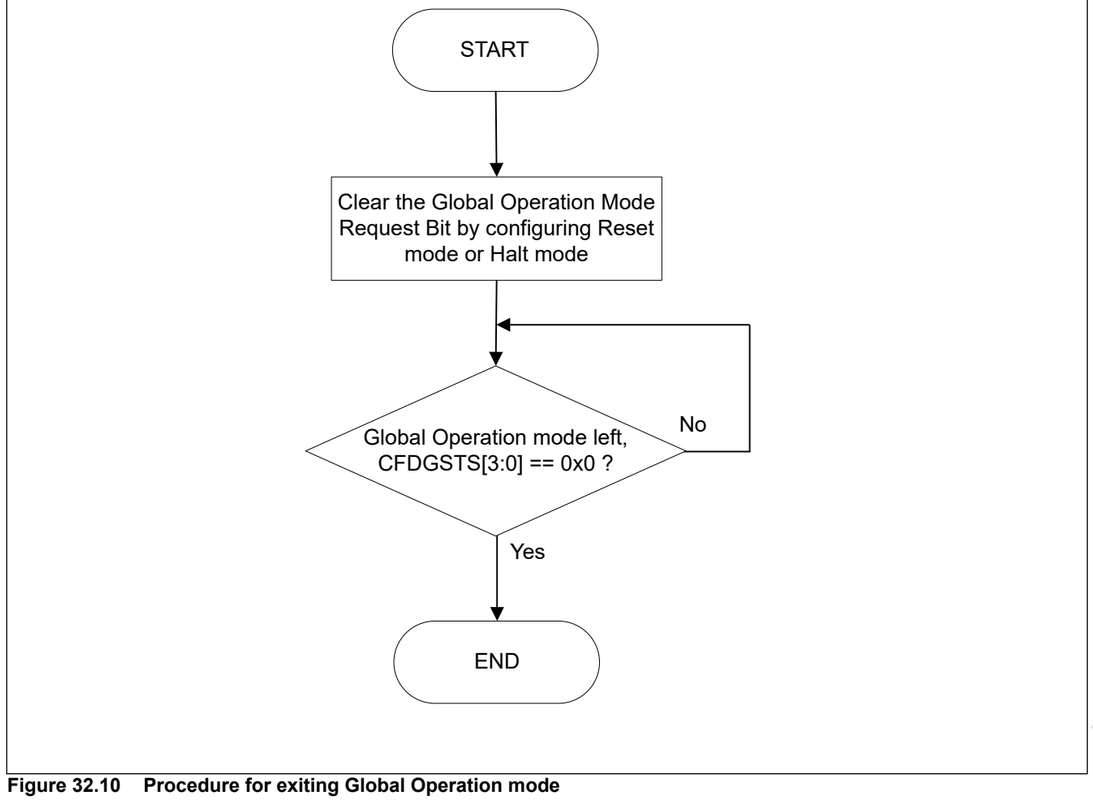


Figure 32.10 Procedure for exiting Global Operation mode

32.3.3 Channel Modes

Each CAN channel can be in one of the following four channel modes:

- Reset
- Halt
- Operation
- Sleep.

Figure 32.11 shows the possible transitions between the channel modes.

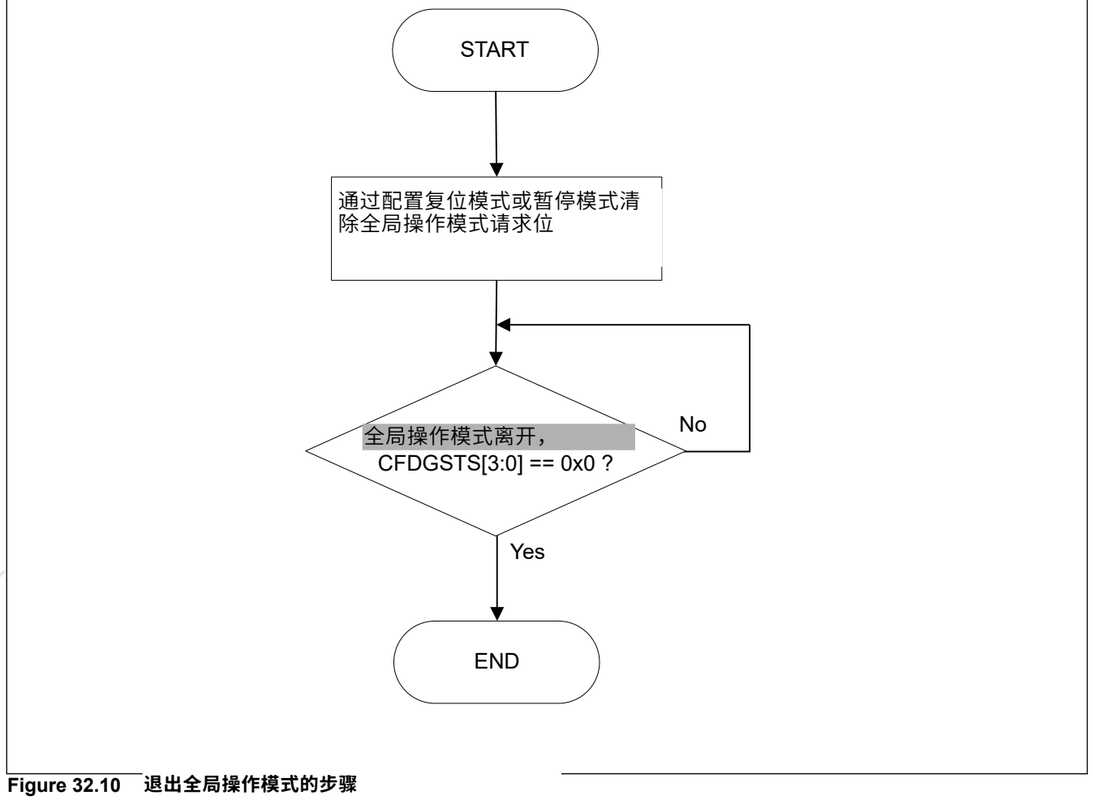


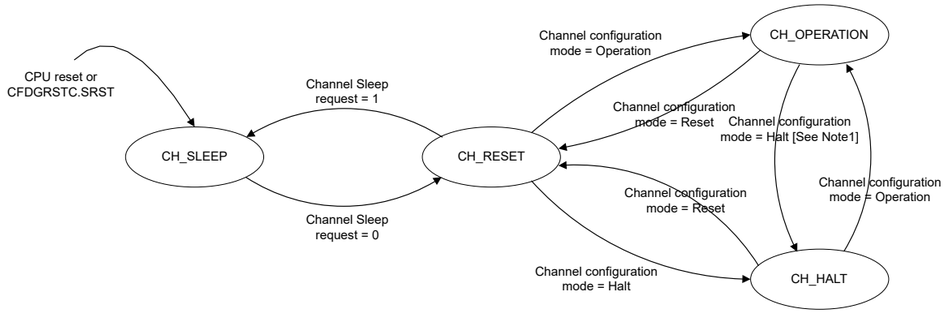
Figure 32.10 退出全局操作模式的步骤

32.3.3 频道模式

每个CAN通道可以处于以下四种通道模式之一：

- Reset
- Halt
- Operation
- Sleep.

图32.11显示了通道模式之间可能的转换。



Note 1. The transition timing depends on BOM setting in the Channel Configuration Register:
- when BOM = 01b, the state transition timing is immediate after entering bus-off state
- when BOM = 10b, the state transition timing is at the end of bus-off state
- when BOM = 11b, the state transition timing is matching with the setting of CHMDC to Halt mode.

Figure 32.11 Transition between CAN channel modes

32.3.3.1 CAN Channel Sleep Mode

After the release of a hardware reset or after setting and clearing the CFDGRSTC.SRST bit, each CAN channel of the CAN-FD module automatically enters Channel Sleep mode.

Each CAN channel also enters Channel Sleep mode when the related Channel Sleep Mode Request bit is set while the CAN channel is in Channel Reset mode. Do not set this control bit in Channel Halt mode or Channel Operation mode.

Entering the CAN Channel Sleep mode instantly stops the clock supplied to the CAN channel unit and therefore reduces power consumption.

After setting the Channel Sleep Mode Request bit, it is necessary to confirm that the Channel Sleep mode status has been updated to indicate a successful transition to Channel Sleep mode before the Channel Sleep Mode Request bit can be cleared again.

During Channel Sleep mode, do not write to channel related registers. Read operation is still possible.

32.3.3.2 CAN Channel Reset Mode

A CAN-FD CAN channel enters this mode in the following ways:

- Channel Mode Control bit CFDCnCTR.CHMDC in the Channel Control Registers is configured for Channel Reset mode while the related CAN channel is in Channel Halt mode or Channel Operation mode
- Channel Sleep Mode Request bit is cleared while the related CAN channel is in Channel Sleep mode
- Global Mode Control bit CFDGCTR.GMDC is set to Global Reset mode and CAN channel is not in Channel Sleep mode or Channel Reset mode.

In Channel Reset mode, all CAN channel status and flag registers are initialized.

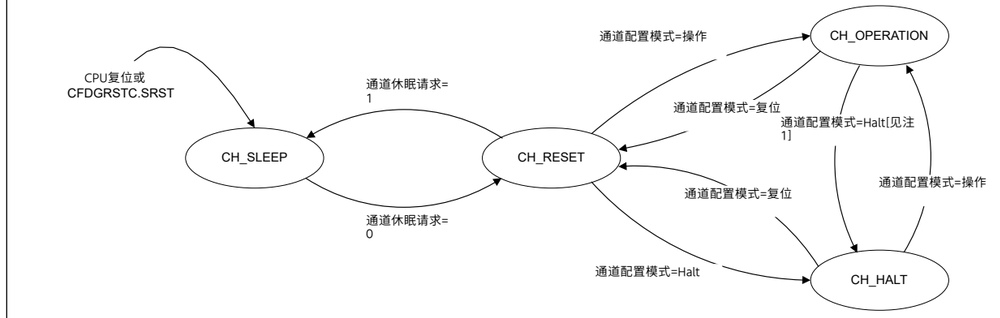
Additionally all channel related transmission control bits are cleared and the channel related TX Queue is disabled.

Configuration registers (except the Channel Test Mode registers) are not initialized in this mode and the CAN channel can be configured for communication.

See section 32.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Channel Reset mode is performed.

After setting the Channel Mode Control bit CFDCnCTR.CHMDC to Channel Reset mode, it is necessary to confirm that the Reset Mode Status bit CFDCnSTS.CRSTSTS in the related Channel Status Registers has been updated to indicate a successful transition to Channel Reset mode before the related CFDCnCTR.CHMDC bit can be modified again.

See Table 32.9 for the behavior of transitioning to Channel Reset mode while CAN communication is ongoing.



注1.转换时序取决于通道配置寄存器中的BOM设置：●
当BOM=01b时，状态转换时序在进入总线关闭状态后立即进行
- 当BOM=10b时，状态转换时序在总线关闭状态结束时
- 当BOM=11b时，状态转换时序与CHMDC设置为Halt模式相匹配。

Figure 32.11 CAN通道模式之间的转换

32.3.3.1 CAN通道休眠模式

在释放硬件复位或设置和清除CFDGRSTC.SRST位后，CAN的每个CAN通道FD模块自动进入通道休眠模式。

当CAN通道处于通道复位模式时，当相关通道休眠模式请求位置位时，每个CAN通道也会进入通道休眠模式。不要在ChannelHalt模式或ChannelOperation模式下设置该控制位。

进入CAN通道休眠模式会立即停止提供给CAN通道单元的时钟，从而降低功耗。

设置通道休眠模式请求位后，必须确认通道休眠模式状态已更新以指示成功转换到通道休眠模式，然后才能再次清除通道休眠模式请求位。

在通道休眠模式期间，不要写入通道相关寄存器。仍然可以进行读取操作。

32.3.3.2 CAN通道复位模式

CAN-FDCAN通道通过以下方式进入此模式：

●通道控制寄存器中的通道模式控制位CFDCnCTR.CHMDC配置为通道复位模式，而相关的CAN通道处于通道暂停模式或通道操作模式

●通道休眠模式请求位在相关CAN通道处于通道休眠模式时清零

●全局模式控制位CFDGCTR.GMDC设置为全局复位模式，CAN通道不处于通道休眠模式或通道复位模式。

在通道复位模式下，所有CAN通道状态和标志寄存器都被初始化。

此外，所有通道相关的传输控制位都被清除，通道相关的TX队列被禁用。

配置寄存器（通道测试模式寄存器除外）在此模式下未初始化，CAN通道可配置为进行通信。

请参见第32.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了当转换到通道复位模式时所有寄存器的行为。

将通道模式控制位CFDCnCTR.CHMDC设置为通道复位模式后，需要确认相关通道状态寄存器中的复位模式状态位CFDCnSTS.CRSTSTS已更新，以指示在相关CFDCnCTR.CHMDC位可以再次修改之前成功转换到通道复位模式。

有关在CAN通信进行时转换到通道复位模式的行为，请参见表32.9。

32.3.3.3 CAN Channel Halt Mode

An CAN-FD CAN channel enters this mode in the following ways:

- Channel Mode Control bit CFDCnCTR.CHMDC in the Channel Control Registers is configured for Channel Halt mode while the related CAN channel is in Channel Reset mode or Channel Operation mode
- Global Mode Control bit CFDGCTR.GMDC is set to Global Halt mode and CAN channel is in Channel Operation mode.

In Channel Halt mode, all channel CAN communication is suspended but all status and flag registers remain unchanged during Channel Halt mode entry (except for the bus-off case where REC and TEC values are cleared for this channel).

In addition, the Channel Test Mode Configuration and Control registers are not initialized in this mode.

The Channel Halt mode should be used to configure channel test modes.

See section 32.3.4. Global Mode and Channel Mode Transition Interactions for a detailed description of the behavior of all registers when transition to Channel Halt mode is performed.

After setting the Channel Mode Control bit CFDCnCTR.CHMDC to Channel Halt mode, it is necessary to confirm that the Halt Mode Status bit CFDCnSTS.CHLTSTS in the related Channel Status Register has been updated to indicate a successful transition to Channel Halt mode before the related CFDCnCTR.CHMDC can be modified again.

See Table 32.9 for the transition behavior to Channel Halt mode while CAN communication is ongoing.

Table 32.9 Transition behavior in CAN Reset mode and Halt mode

Mode	State		
	Receiver	Transmitter	Bus-Off
CAN Channel Reset mode (CFDCnCTR.CHMDC = 01b)	The CAN channel enters Channel Reset mode without waiting for the completion of the ongoing reception.*1	The CAN channel enters Channel Reset mode without waiting for the completion of the ongoing transmission.*1	The CAN channel enters Channel Reset mode without waiting for the completion of the bus-off recovery.
CAN Channel Halt mode (CFDCnCTR.CHMDC = 10b)	CAN channel enters Channel Halt mode at the end of the ongoing reception or error.*2	CAN channel enters Channel Halt mode after completion of the ongoing transmission.	When CFDCnCTR.BOM is set to 00b, a Channel Halt mode request is accepted only after the completion of the full bus-off recovery sequence. When CFDCnCTR.BOM is set to 10b, the CAN channel transits automatically to Channel Halt mode after waiting for the completion of the bus-off recovery. When CFDCnCTR.BOM is set to 01b, the CAN channel transits automatically to Channel Halt mode without waiting for the completion of the bus-off recovery. When CFDCnCTR.BOM is set to 11b, the CAN channel enters Channel Halt mode as soon as Channel Halt mode is requested (without waiting for the completion of the bus-off recovery).

Note 1. If the entry to Channel Reset mode is required only at the end of an ongoing communication, then Channel Halt mode can be requested first to prevent interruption of CAN communication by direct transition to Channel Reset mode. After the CAN channel enters Channel Halt mode, the Channel Reset mode can be requested.

Note 2. If CAN communication is locked at dominant level after an error flag, software can detect this situation by monitoring the channel related BusLock flag and resolve lock condition by setting the CAN channel to Channel Reset mode.

32.3.3.4 CAN Channel Operation Mode

The Channel Operation mode is activated by setting the CFDCnCTR.CHMDC bits to 00b. If 11 consecutive recessive bits are detected after entering the CAN Operation mode, the CFDCnSTS.COMSTS bit is set and the CAN channel:

32.3.3.3 CAN通道暂停模式

CAN-FDCAN通道通过以下方式进入此模式：

●通道控制寄存器中的通道模式控制位CFDCnCTR.CHMDC配置为通道暂停模式，而相关的CAN通道处于通道复位模式或通道操作模式

●全局模式控制位CFDGCTR.GMDC设置为全局暂停模式，CAN通道处于通道操作模式。

在ChannelHalt模式下，所有通道CAN通信都暂停，但在ChannelHalt模式进入期间所有状态和标志寄存器保持不变（总线关闭情况除外，该通道的REC和TEC值被清除）。

此外，通道测试模式配置和控制寄存器在此模式下未初始化。

通道暂停模式应该用于配置通道测试模式。

请参见第32.3.4节。GlobalModeandChannelModeTransitionInteractions详细描述了当转换到ChannelHalt模式时所有寄存器的行为。

将通道模式控制位CFDCnCTR.CHMDC设置为通道暂停模式后，需要确认
相关通道状态寄存器中的暂停模式状态位CFDCnSTS.CHLTSTS已更新，以指示在可以再次修改相关CFDCnCTR.CHMDC之前成功转换到通道暂停模式。

有关CAN通信正在进行时到通道暂停模式的转换行为，请参见表32.9。

Table 32.9 CAN复位模式和暂停模式下的转换行为

Mode	State		
	Receiver	Transmitter	Bus-Off
CAN通道复位模式(CFDCnCTR.CHMDC=01b)	CAN通道进入 通道复位模式无需等待正在进行的接收完成。*1	CAN通道进入 通道复位模式无需等待正在进行的传输完成。*1	CAN通道进入 通道复位模式无需等待总线关闭恢复完成。
CAN通道暂停模式(CFDCnCTR.CHMDC=10b)	CAN通道在正在进行的接收或错误结束时进入通道暂停模式。*2	CAN通道进入Channel 正在进行的传输完成后暂停模式。	当CFDCnCTR.BOM设置为00b时，仅在完成完整的总线关闭恢复序列后才接受通道暂停模式请求。当CFDCnCTR.BOM设置为10b时，CAN通道在等待总线关闭恢复完成后自动转换到通道暂停模式。当CFDCnCTR.BOM设置为01b时，CAN通道自动转换到通道暂停模式，无需等待总线关闭恢复完成。当CFDCnCTR.BOM设置为11b时，只要请求ChannelHalt模式，CAN通道就会进入ChannelHalt模式（无需等待总线关闭恢复完成）。

注1.如果仅在正在进行的通信结束时需要进入通道复位模式，则通道暂停模式可以是
首先请求通过直接转换到通道复位模式来防止CAN通信中断。CAN通道进入ChannelHalt模式后，可以请求ChannelReset模式。

注2.如果CAN通信在出现错误标志后被锁定在显性电平，软件可以通过监控通道相关的BusLock标志来检测这种情况，并通过将CAN通道设置为通道复位模式来解决锁定条件。

32.3.3.4 CAN通道操作模式

通道操作模式通过将CFDCnCTR.CHMDC位设置为00b来激活。如果在进入CAN操作模式后检测到11个连续的隐性位，则CFDCnSTS.COMSTS位置位并且CAN通道：

- Enables the functions of the channel communication by allowing the channel to become an active node on the CAN network
- Releases the internal fault confinement logic including receive and transmit error counters

At this point, the CAN channel can start transmission and reception of CAN messages.

Within the CAN Channel Operation mode, the channel may be in four different sub-modes, depending on which type of communication functions are performed (see Figure 32.12):

- Channel idle: The CAN channel is neither receiving nor transmitting
- Channel receives: The channel is receiving a CAN message sent by another CAN node
- Channel transmits: The channel is transmitting a CAN message

  Note: The channel may receive its own message simultaneously when Self-test mode is enabled.
- Channel is in bus-off state: The CAN channel is cut-off from CAN bus communication.

After setting the Channel Mode Control bit CFDCnCTR.CHMDC to Channel Operation mode, it is necessary to confirm that the Channel Reset Mode Status bit CFDCnSTS.CRSTSTS and the Channel Halt Mode Status bit CFDCnSTS.CHLTSTS in the Channel Status Register have been updated to indicate a successful transition to Channel Operation mode before the related CFDCnCTR.CHMDC bit can be changed again.

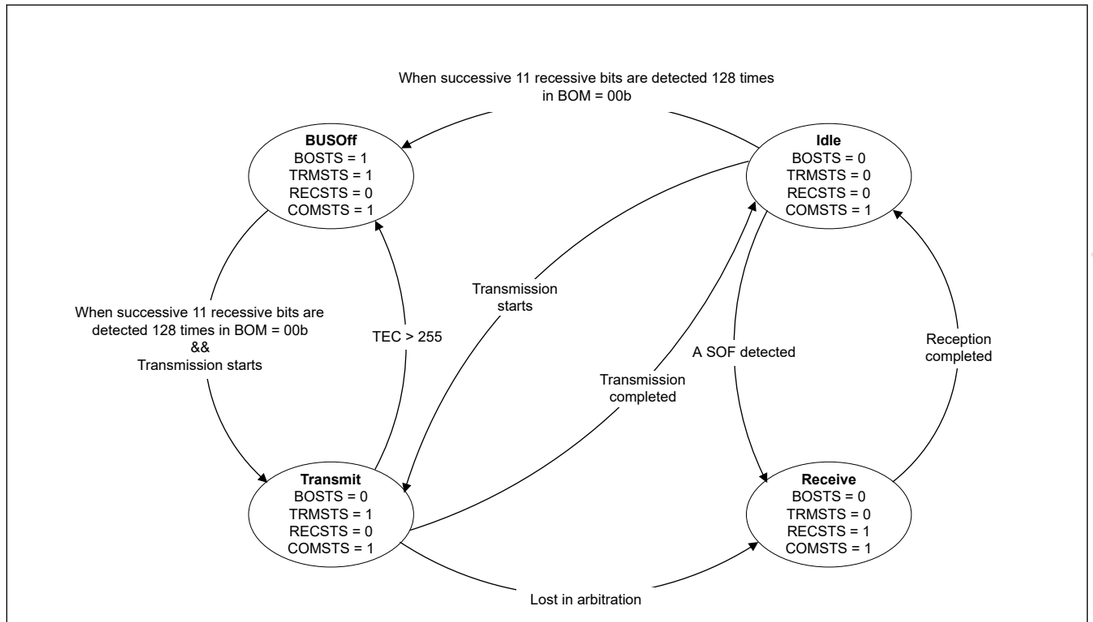


Figure 32.12 Sub-modes of CAN Channel Operation mode (only when BOM = 00b)

32.3.3.5 CAN Channel Bus-Off State

The CAN channel bus-off state is entered according to the fault confinement rules of the CAN specification. The following modes can be configured for returning to the CAN Channel Operation mode from the bus-off state:

- CFDCnCTR.BOM = 00b:
  Bus-Off recovery is compliant to ISO 11898-1, namely the CAN channel re-enters CAN communication (error active state) after 11 consecutive recessive bits are detected 128 times. TEC and REC counters are initialized to 0. The Bus-Off Recovery Flag CFDCnERFL.BORF is set in this case.
- CFDCnCTR.BOM = 01b:

●通过让通道成为CAN网络上的活动节点来启用通道通信的功能

●释放内部故障限制逻辑，包括接收和发送错误计数器

此时，CAN通道就可以开始发送和接收CAN报文了。

在CAN通道操作模式下，通道可能处于四种不同的子模式，具体取决于执行的通信功能类型（参见图32.12）：

●Channelidle：CAN通道既不接收也不发送

●通道接收：通道正在接收另一个CAN节点发送的CAN报文

●通道传输：通道正在传输CAN报文

Note: 启用自检模式后，通道可能会同时收到自己的消息。

●通道处于总线关闭状态：CAN通道与CAN总线通讯中断。

将通道模式控制位CFDCnCTR.CHMDC设置为通道操作模式后，需要确认通道状态寄存器中的通道复位模式状态位CFDCnSTS.CRSTSTS和通道暂停模式状态位CFDCnSTS.CHLTSTS已更新以指示成功过渡到频道

可以再次更改相关CFDCnCTR.CHMDC位之前的操作模式。

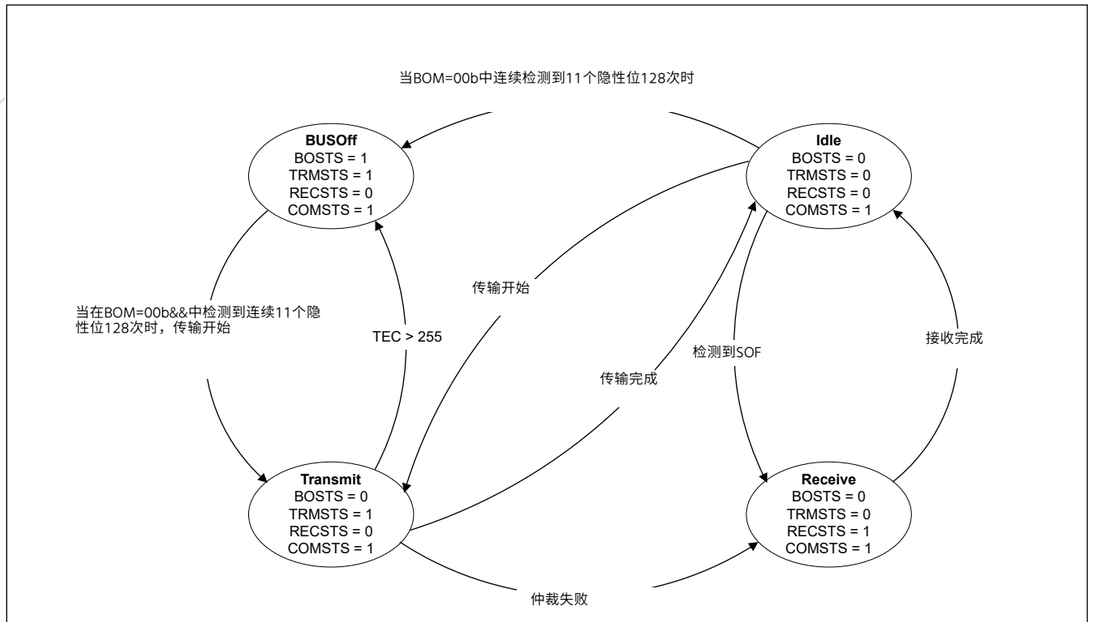


Figure 32.12 CAN通道操作模式的子模式（仅当BOM=00b时）

32.3.3.5 CAN通道总线关闭状态

根据CAN规范的故障限制规则进入CAN通道总线关闭状态。可以配置以下模式以从总线关闭状态返回到CAN通道操作模式：

- CFDCnCTR.BOM = 00b:
  Bus-Off恢复符合ISO11898-1标准，即CAN通道在连续检测到11个隐性位128次后重新进入CAN通信（错误激活状态）。TEC和REC计数器初始化为0。在这种情况下设置总线关闭恢复标志CFDCnERFL.BORF。
- CFDCnCTR.BOM = 01b:

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The CAN channel changes the value of the CFDCnCTR.CHMDC bits within the CAN Channel Control Register to 10b and switches immediately to Channel Halt mode automatically after entering bus-off state. TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDCnERFL.BORF is not set in this case.

- CFDCnCTR.BOM = 10b:
  The CAN channel changes the value of the CFDCnCTR.CHMDC bits within the CAN Channel Control Register to 10b as soon as it reaches bus-off state and enters Channel Halt mode automatically after the CAN channel has completed the bus-off recovery sequence (after 11 consecutive recessive bits are detected 128 times). TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDCnERFL.BORF is set in this case.
- CFDCnCTR.BOM = 11b:
  Bus-off recovery is initiated but CAN channel can immediately enter Channel Halt mode when still in bus-off state if a request is made to enter Channel Halt mode.
  TEC and REC counters are initialized to 0 and the Bus-Off Recovery Flag CFDCnERFL.BORF is not set.
  Without setting CFDCnCTR.CHMDC [1:0] = 10b and when 11 recessive bits is detected 128 times continuously, transition conditions become the same as CFDCnCTR.BOM = 00b.

Note: If the recovery from bus-off occurs normally in this mode (after waiting for 128 sequences of 11 consecutive recessive bits), and no halt request has been generated during this period, then the Bus-Off Recovery flag CFDCnERFL.BORF is set.

When software writes to the CFDCnCTR.CHMDC bit at the same time as the CAN channel enters Halt mode (at the start of bus-off when CFDCnCTR.BOM = 01b, or at the end of bus-off when CFDCnCTR.BOM = 10b), the software request has the highest priority.

Note: In the above case, the automatic setting of the CFDCnCTR.CHMDC bit to Channel Halt mode request is performed when the CFDCnCTR.CHMDC bit value is previously 00b (Channel Operation mode).

Additionally, it is possible to force the CAN channel to recover from the bus-off state by setting CFDCnCTR.RTBO to 1. The error state changes from bus-off state to integrating state with a maximum delay of 1 CAN bit time, and the CAN communication becomes possible again after 11 consecutive recessive bits are detected. The Bus-Off Recovery Flag is not set in this case, and the TEC and REC counters are initialized to 0.

Before setting CFDCnCTR.RTBO to 1, all pending transmissions from the TX message buffers, TX Queues and/or Common FIFO in TX or GW mode should be disabled.

The disable of the pending transmission message buffer, TX Queue or FIFO must be confirmed by the corresponding acknowledge flags.

For the TX message buffer, the acknowledge flags are the Transmission Result Flags (CFDTMSTSn.TMTRF). For the TX Queue, it is the TX Queue Empty flag (CFDTXQSTSn.TXQEMP). For the FIFO, it is the FIFO Empty flag (CFDCFSTSn.CFEMP).

The CFDCnCTR.RTBO bit should be used for bus-off recovery only when CFDCnCTR.BOM is set to 00b.

Setting this bit in any state other than bus-off has no effect and the bit is cleared immediately.

Table 32.10 shows the settings for the Bus-Off Entry flag CFDCnERFL.BOEF and the Bus-Off Recovery flag CFDCnERFL.BORF for the different configurations of CFDCnCTR.BOM.

Table 32.10 Behavior of Bus-off Entry and Recovery flags

BOM	BOEF bit set	BORF bit set
00b	Always (on entry to bus-off)	Always (on exit from bus-off)
00b CFDCnCTR.RTBO set to 1	Always (on entry to bus-off)	Only if normal bus-off recovery occurs before software sets CFDCnCTR.RTBO to 1'
01b	Always (on entry to bus-off)	Never
10b	Always (on entry to bus-off)	Always (on exit from bus-off)
11b	Always (on entry to bus-off)	Only if normal bus-off recovery occurs before software issues a Halt request

For an efficient software procedure, it is not necessary to wait for the bus-off recovery sequence to end.

CAN通道将CAN通道控制寄存器中的CFDCnCTR.CHMDC位的值更改为10b，并在进入总线关闭状态后立即自动切换到通道暂停模式。在这种情况下，TEC和REC计数器初始化为0，并且总线关闭恢复标志CFDCnERFL.BORF未设置。

- CFDCnCTR.BOM = 10b:
  CAN通道一旦达到总线关闭状态，就会将CAN通道控制寄存器中的CFDCnCTR.CHMDC位的值更改为10b，并在CAN通道完成总线关闭恢复序列后自动进入通道暂停模式（11连续的隐性位被检测到128次）。在这种情况下，TEC和REC计数器被初始化为0，并且总线关闭恢复标志CFDCnERFL.BORF被设置。
- CFDCnCTR.BOM = 11b:
  总线关闭恢复已启动，但如果请求进入通道暂停模式，CAN通道仍处于总线关闭状态时可立即进入通道暂停模式。TEC和REC计数器初始化为0，并且总线关闭恢复标志CFDCnERFL.BORF未设置。

  在不设置CFDCnCTR.CHMDC[1:0]=10b且连续128次检测到11个隐性位时，转换条件与CFDCnCTR.BOM=00b相同。

Note: 如果在此模式下从总线关闭中恢复正常（在等待128个序列的11个连续隐性位之后），并且在此期间没有产生暂停请求，则设置总线关闭恢复标志CFDCnERFL.BORF。

当软件在CAN通道进入暂停模式的同时写入CFDCnCTR.CHMDC位（当CFDCnCTR.BOM=01b时在总线关闭开始时，或者当CFDCnCTR.BOM=10b时在总线关闭结束时），软件请求具有最高优先级。

Note: 在上述情况下，当CFDCnCTR.CHMDC位的值先前为00b（通道操作模式）时，会执行将CFDCnCTR.CHMDC位自动设置为通道暂停模式请求。

此外，可以通过将CFDCnCTR.RTBO设置为1来强制CAN通道从总线关闭状态恢复。错误状态从总线关闭状态变为积分状态，最大延迟为1个CAN位时间，并且在检测到11个连续的隐性位后，CAN通信再次成为可能。在这种情况下，不设置总线关闭恢复标志，并且TEC和REC计数器初始化为0。

在将CFDCnCTR.RTBO设置为1之前，来自TX消息缓冲区、TX队列和或TX或GW模式下的通用FIFO应禁用。

未决传输消息缓冲区、TX队列或FIFO的禁用必须由相应的确认标志确认。

对于TX消息缓冲区，确认标志是传输结果标志(CFDTMSTSn.TMTRF)。对于TX Queue，它是TXQueueEmpty标志（CFDTXQSTSn.TXQEMP）。对于FIFO，它是FIFO空标志(CFDCFSTSn.CFEMP)。

只有当CFDCnCTR.BOM设置为00b时，才应使用CFDCnCTR.RTBO位进行总线关闭恢复。

将该位设置为除总线关闭以外的任何状态均无效，并且该位立即被清除。

表32.10显示了Bus-OffEntry标志CFDCnERFL.BOEF和Bus-OffRecovery标志的设置CFDCnERFL.BORF用于CFDCnCTR.BOM的不同配置。

Table 32.10 总线关闭进入和恢复标志的行为

BOM	BOEF位组	BORF位组
00b	总是（在进入巴士下车时）	总是（在巴士下车的出口处）
00bCFDCnCTR.RTBO设置为1	总是（在进入巴士下车时）	只有在软件设置之前发生正常的总线关闭恢复CFDCnCTR.RTBO to 1'
01b	总是（在进入巴士下车时）	Never
10b	总是（在进入巴士下车时）	总是（在巴士下车的出口处）
11b	总是（在进入巴士下车时）	只有在软件发出暂停请求之前发生正常的总线关闭恢复

对于有效的软件程序，不必等待总线关闭恢复序列结束。

It is possible to perform a transmission re-initialization during bus-off recovery. To do this, follow the recommended software flow in Figure 32.13.

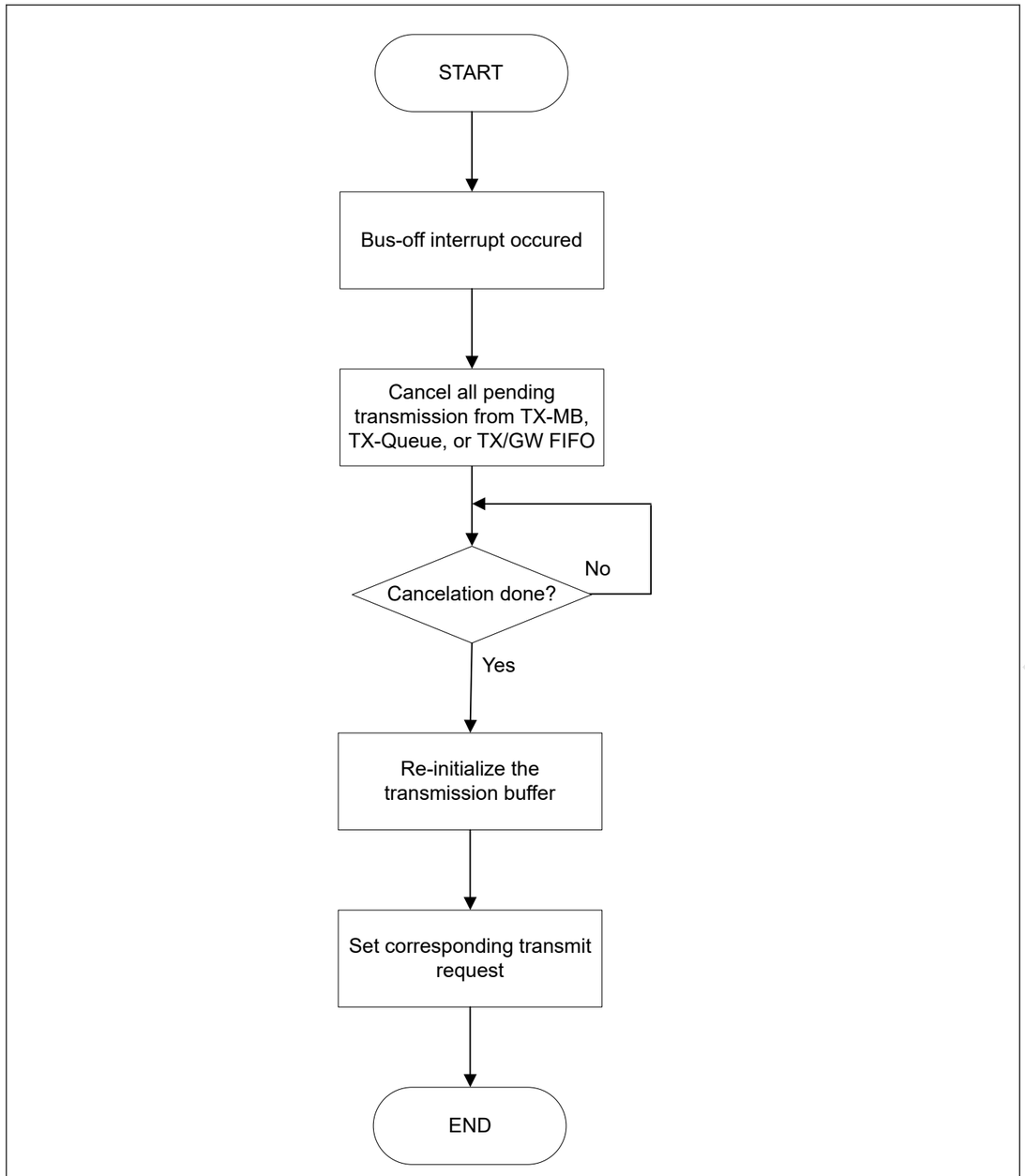

Figure 32.13 Transmission re-initialization during bus-off

32.3.4 Global Mode and Channel Mode Transition Interactions

The interaction between Global mode setting and Channel mode setting is as follows:

可以在总线关闭恢复期间执行传输重新初始化。为此，请遵循图32.13中推荐的软件流程。

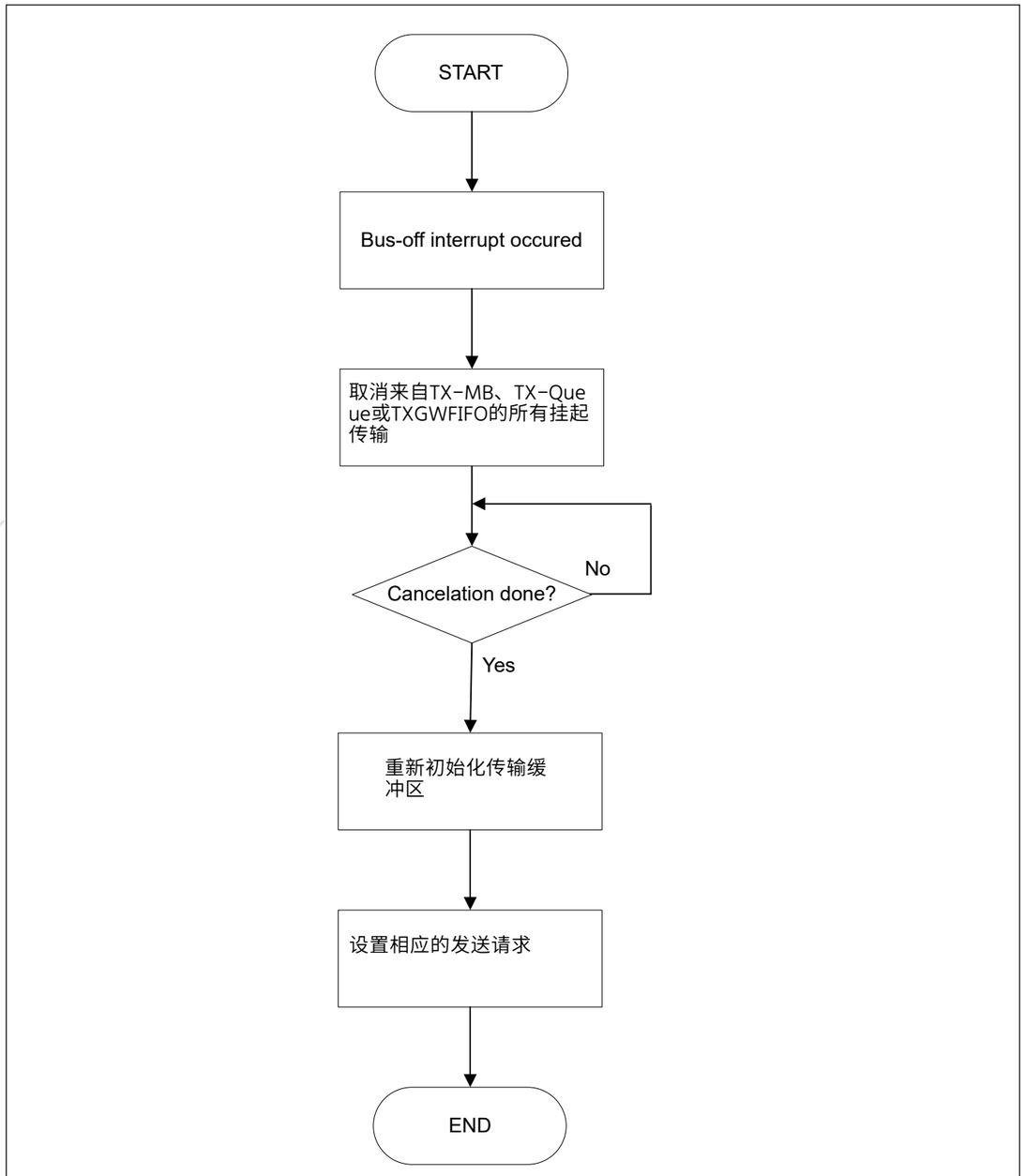

Figure 32.13 总线关闭期间的传输重新初始化

32.3.4 全局模式和通道模式转换交互

Global模式设置和Channel模式设置的交互如下：

- Changing the Channel Mode Control bit CFDCnCTR.CHMDC in the Channel Control Registers does not affect the Global Mode Control bit CFDGCTR.GMDC.
- Changing the Global Mode Control bit CFDGCTR.GMDC affects the channel mode control as described in Table 32.11.

Table 32.11 Interaction between Global and Channel mode transition

Global mode change	Channel mode	Channel mode transition action
Sleep → Reset	Sleep	Channel remains in Sleep mode
Sleep → Halt	— (Global mode change not possible)	
Sleep → Operation	— (Global mode change not possible)	
Reset → Sleep	Sleep	Channels remains in Sleep mode
	Reset	Channel Sleep request bit is set automatically, channel enters Sleep Mode
Reset → Halt	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
Reset → Operation	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
Halt → Sleep	— (Global mode change not possible)	
Halt → Reset	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel mode control is set to Reset mode, channel enters Reset mode
Halt → Operation	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel remains in Halt mode
Operation → Sleep	— (Global mode change not possible)	
Operation → Reset	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel mode control is set to Reset mode, channel enters Reset mode
	Operation	Channel mode control is set to Reset mode, channel enters Reset mode
Operation → Halt	Sleep	Channel remains in Sleep mode
	Reset	Channel remains in Reset mode
	Halt	Channel remains in Halt mode
	Operation	Channel mode control is set to Halt mode, channel enters Halt mode after communication finished

32.3.4.1 Timing of Global Mode Change

The transition time for the Global mode changes are shown in the following table.

Table 32.12 Maximum transition time for the global mode (1 of 2)

From	To	Maximum transition time
GL_SLEEP	GL_RESET	3 peripheral clock cycles*2
GL_RESET	GL_SLEEP	3 peripheral clock cycles
GL_RESET	GL_HALT	10 peripheral clock cycles
GL_RESET	GL_OPERATION	10 peripheral clock cycles

●更改通道控制寄存器中的通道模式控制位CFDCnCTR.CHMDC不会影响全局模式控制位CFDGCTR.GMDC。

●更改全局模式控制位CFDGCTR.GMDC会影响通道模式控制，如表32.11所述。

Table 32.11 全局和通道模式转换之间的交互

全局模式改变	频道模式	通道模式转换动作
睡眠→重置	Sleep	通道保持休眠模式
睡眠→暂停	—（无法更改全局模式）	
睡眠→操作	—（无法更改全局模式）	
重置→睡眠	Sleep	通道保持休眠模式
	Reset	通道休眠请求位自动置位，通道进入休眠状态 Mode
重置→停止	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
重置→操作	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
暂停→睡眠	—（无法更改全局模式）	
暂停→重置	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道模式控制设置为复位模式，通道进入复位模式
暂停→运行	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道保持暂停模式
运行→睡眠	—（无法更改全局模式）	
操作→复位	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道模式控制设置为复位模式，通道进入复位模式
	Operation	通道模式控制设置为复位模式，通道进入复位模式
运行→停止	Sleep	通道保持休眠模式
	Reset	通道保持在复位模式
	Halt	通道保持暂停模式
	Operation	通道模式控制设置为Halt模式，通讯结束后通道进入Halt模式

32.3.4.1 全局模式变化的时机

全局模式更改的转换时间如下表所示。

Table 32.12 全局模式的最大转换时间（1of2）

From	To	最长过渡时间
GL_SLEEP	GL_RESET	3个外设时钟周期*2
GL_RESET	GL_SLEEP	3个外设时钟周期
GL_RESET	GL_HALT	10个外设时钟周期
GL_RESET	GL_OPERATION	10个外设时钟周期

Table 32.12 Maximum transition time for the global mode (2 of 2)

From	To	Maximum transition time
GL_HALT	GL_RESET	2 CAN bit times
GL_HALT	GL_OPERATION	3 peripheral clock cycles
GL_OPERATION	GL_RESET	2 CAN bit times
GL_OPERATION	GL_HALT	3 CAN frames*1 *3

Note 1. The given transition time is the time without any errors on the bus. In case of an error condition, the transition time can lengthen to an uncalculated result. The transition time can also come to a stuck condition for locked RX lines or continued error conditions.
Note 2. Exit GL_SLEEP mode only when CFDGSTS.GRAMINIT is cleared.
Note 3. TQ, CAN frame and CAN bits are related to the individual channels. For the maximum transition time, the channel with the lowest baud rate must be used.

32.3.4.2 Timing of Channel Mode Change

The transition time for the Channel mode changes are shown in the following table.

Table 32.13 Maximum transition time for the channel mode

From	To	max. transition time
CH_SLEEP	CH_RESET	3 peripheral clock cycles
CH_RESET	CH_SLEEP	3 peripheral clock cycles
CH_RESET	CH_HALT	3 CAN bit times
CH_RESET	CH_OPERATION	4 CAN bit times
CH_HALT	CH_RESET	2 CAN bit times
CH_HALT	CH_OPERATION	4 CAN bit times*3
CH_OPERATION	CH_RESET	2 CAN bit times
CH_OPERATION	CH_HALT	2 CAN frames*1 *2

Note 1. The time specified for this transition does not include the case where channel enters bus-off state. For bus-off, the timing depends on the configuration of the CFDCnCTR.BOM[1:0] bits.
Note 2. The given transition time is the time without any errors on the bus. In case of an error condition, the transition time can lengthen to an uncalculated result. The transition time can also come to a stuck condition for locked RX lines or continued error conditions.
Note 3. In general, if the baudrate prescaler value CFDCnNCFG.NBRP is changed in CH_HALT mode, the transition time can deviate. The internal prescaler is a free running down counter that creates the TQ clock, and new BRP value is captured when the counter reaches the value 0.

32.4 Initialization

Before joining CAN communications, configure the following settings:

- Clock setting
- Bit timing setting (nominal and data rate)
- Baud Rate setting (nominal and data rate)
- CAN-FD setting
- Acceptance Filter setting (configuration of Global Acceptance Filter List)
- Reception, Transmission and GW-FIFO setting
- CAN Operation mode setting

32.4.1 Initialization of CAN Clock, Bit Timing and Baud Rate

32.4.1.1 Bit Timing Conditions

The following lines describe the composition of each segment and the restriction that apply to the segment setting.

1. Each segment setting
   SS = Fixed to 1 TQ

Table 32.12 全局模式的最大转换时间（2之2）

From	To	最长过渡时间
GL_HALT	GL_RESET	2个CAN位时间
GL_HALT	GL_OPERATION	3个外设时钟周期
GL_OPERATION	GL_RESET	2个CAN位时间
GL_OPERATION	GL_HALT	3个CAN帧*1*3

注1.给定的转换时间是总线上没有任何错误的时间。如果出现错误情况，转换时间可能会延长到无法计算的结果。对于锁定的RX线或持续的错误情况，转换时间也可能达到卡住状态。
注2.仅当CFDGSTS.GRAMINIT被清除时才退出GL_SLEEP模式。
注3.TQ、CAN帧和CAN位与各个通道相关。对于最大转换时间，必须使用具有最低波特率的通道。

32.3.4.2 频道模式改变的时机

通道模式更改的转换时间如下表所示。

Table 32.13 通道模式的最大转换时间

From	To	最大限度。过渡时间
CH_SLEEP	CH_RESET	3个外设时钟周期
CH_RESET	CH_SLEEP	3个外设时钟周期
CH_RESET	CH_HALT	3CAN位时间
CH_RESET	CH_OPERATION	4个CAN位时间
CH_HALT	CH_RESET	2个CAN位时间
CH_HALT	CH_OPERATION	4CAN位时间*3
CH_OPERATION	CH_RESET	2个CAN位时间
CH_OPERATION	CH_HALT	2个CAN帧*1*2

注1.为该转换指定的时间不包括通道进入总线关闭状态的情况。对于总线关闭，时序取决于CFDCnCTR.BOM[1:0]位的配置。

注2.给定的转换时间是总线上没有任何错误的时间。如果出现错误情况，转换时间可能会延长到无法计算的结果。对于锁定的RX线或持续的错误情况，转换时间也可能达到卡住状态。
注3.一般情况下，如果波特率预分频器值CFDCnNCFG.NBRP在CH_HALT模式下发生变化，则转换时间可能会发生偏差。内部预分频器是一个自由运行的递减计数器，它创建TQ时钟，当计数器达到值0时，捕获新的BRP值。

32.4 Initialization

在加入CAN通信之前，请配置以下设置：

●时钟设置
●位定时设置（标称和数据速率）
●波特率设置（标称和数据速率）
- CAN-FD setting
●验收过滤器设置（全局验收过滤器列表的配置）
●接收、发送和GW-FIFO设置
●CAN操作模式设置

32.4.1 CAN时钟、位时序和波特率的初始化

32.4.1.1 位时序条件

以下几行描述了每个段的组成以及适用于段设置的限制。

1.每段设置SS=Fixedto
1TQ

TSEG1 = See to (CFDCnNCFG) and (CFDCnDCFG)*1
TSEG2 = See to (CFDCnNCFG) and (CFDCnDCFG)*1
SJW = See to (CFDCnNCFG) and (CFDCnDCFG)*1
SS + TSEG1 + TSEG2 = 5 to 49 TQs for Data Bit Rate and 8 to 385 for Nominal Bit Rate

2. Restriction on TSEG1, TSEG2 and SJW
TSEG1(N) > TSEG2(N) ≥ SJW(N)
TSEG1(D) ≥ TSEG2(D) ≥ SJW(D)*1
When only classical frames are used, configure the bit fields TSEG1 and TSEG2 of CFDCnDCFG to valid values.

Note 1. This feature is not available in the classical CAN function.

Table 32.14 shows an example of how to set the bit timing to achieve the required Sample Point settings.

Table 32.14 Bit timing examples

1 bit	Set value (TQ)				Sample point*1(%)
	SS	TSEG1	TSEG2	SJW	
5TQ	1	2	2	1	60.00
8TQ	1	4	3	1	62.50
	1	5	2	1	75.00
10TQ	1	6	3	1	70.00
	1	7	2	1	80.00
12TQ	1	8	3	1	75.00
	1	9	2	1	83.33
15TQ	1	10	4	1	73.33
	1	11	3	1	80.00
16TQ	1	10	5	1	68.75
	1	11	4	1	75.00
20TQ	1	12	7	1	65.00
	1	13	6	1	70.00
24TQ	1	15	8	1	66.66
	1	16	7	1	70.83
50TQ	1	39	10	4	80.00

Note 1. Sample point (in case of 75%)

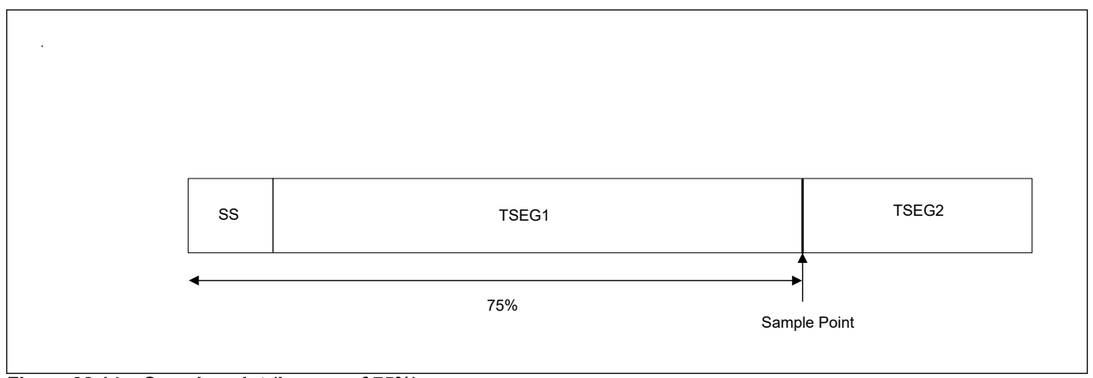

Figure 32.14 Sample point (in case of 75%)

TSEG1=参见(CFDCnNCFG)和(CFDCnDCFG)*1
TSEG2=参见(CFDCnNCFG)和(CFDCnDCFG)*1
SJW=参见(CFDCnNCFG)和(CFDCnDCFG)*1
SS+TSEG1+TSEG2=5到49个TQ用于数据比特率，8到385个用于标称比特率

2.对TSEG1、TSEG2和SJW的限制TSEG1(
N)>TSEG2(N)≥SJW(N)
TSEG1(D) ≥ TSEG2(D) ≥ SJW(D)*1
当仅使用经典帧时，将CFDCnDCFG的位域TSEG1和TSEG2配置为有效值。

注1.此功能在经典CAN功能中不可用。

表32.14显示了如何设置位时序以实现所需采样点设置的示例。

Table 32.14 位时序示例

1 bit	设定值(TQ)				采样点*1(%)
	SS	TSEG1	TSEG2	SJW	
5TQ	1	2	2	1	60.00
8TQ	1	4	3	1	62.50
	1	5	2	1	75.00
10TQ	1	6	3	1	70.00
	1	7	2	1	80.00
12TQ	1	8	3	1	75.00
	1	9	2	1	83.33
15TQ	1	10	4	1	73.33
	1	11	3	1	80.00
16TQ	1	10	5	1	68.75
	1	11	4	1	75.00
20TQ	1	12	7	1	65.00
	1	13	6	1	70.00
24TQ	1	15	8	1	66.66
	1	16	7	1	70.83
50TQ	1	39	10	4	80.00

注1.采样点（在75%的情况下）

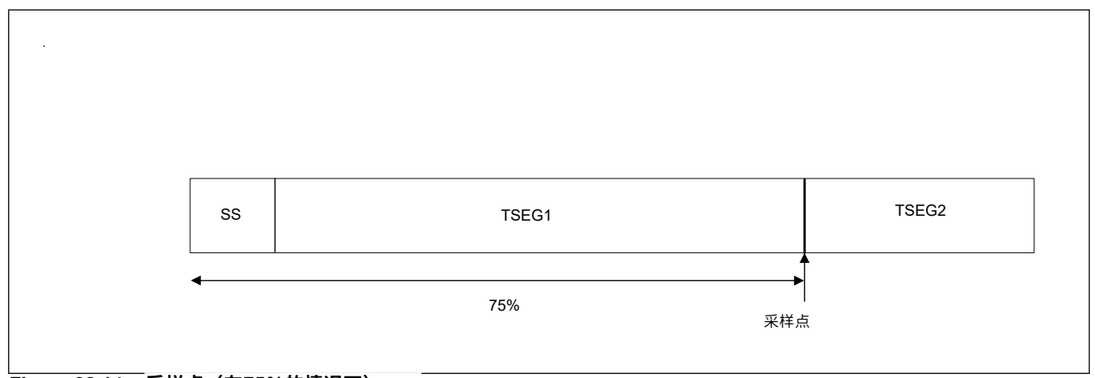

Figure 32.14 采样点（在75%的情况下）

32.4.1.2 CAN Bit Timing

In the CAN protocol, each bit in a communication frame is composed of three segments that can be configured individually for each channel using the related CFDCnNCFG and CFDCnDCFG*1 registers.

Note 1. This register is not available in the classical CAN function.

Figure 32.15 shows the segment composition of a bit and the sample point in it.

Of these segments, the Time Segment 1 (TSEG1) and Time Segment 2 (TSEG2) are used to specify the position of the sample point, so that the timing at which each bit on the CAN bus is sampled can be altered by changing the values of these segments.

The minimum resolution for this timing is referred to as Time Quantum (TQ), which is determined by the clock frequency supplied to the CAN channel and the divide-by-N value of the baud rate prescaler (nominal and data rate).

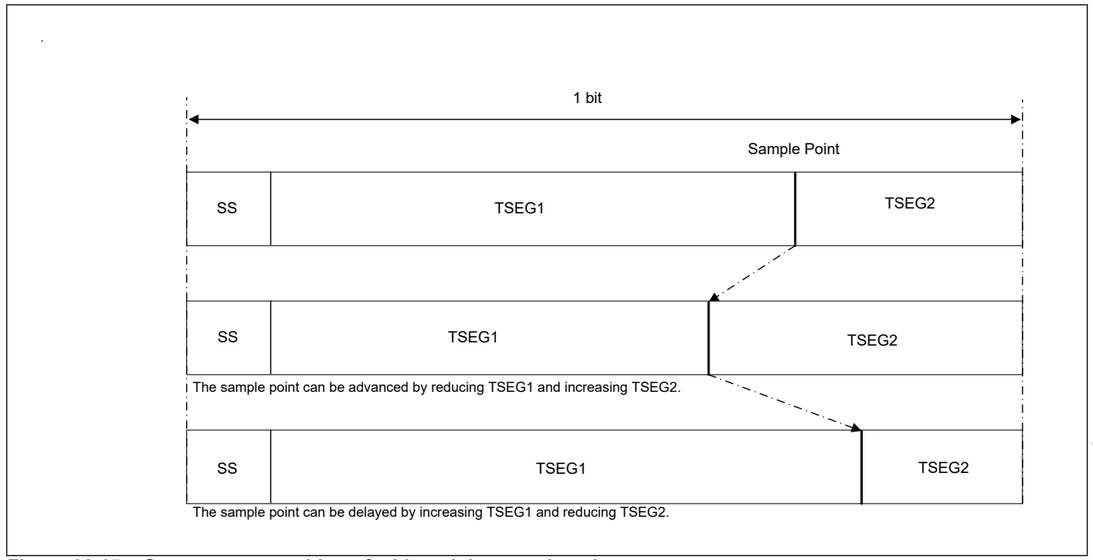

Figure 32.15 Segment composition of a bit and the sample point

1. SS: Synchronization Segment
   This segment is used to synchronize bits by monitoring a recessive-to-dominant edge during the interframe space. This comprises of intermission, suspend transmission, bus idle, during bus idle, and all nodes that can start transmission.
2. TSEG1: Time Segment 1
   This segment absorbs physical delays on the CAN network. A physical delay on the network is two times the total sum of a bus delay, input comparator delay, and output driver delay. It can be lengthened by SJW.
3. TSEG2: Time Segment 2
   This segment is used to correct a phase error by performing resynchronization. It can be shortened by SJW. While sending or receiving a message, communication frames between some nodes may get out of sync due to a drift in the oscillator frequency or a delay in the transmission path. This is referred to as a phase error.
4. SJW: Resynchronization Jump Width
   This is the maximum width by which bits that have become out of sync due to a phase error may be corrected.

Figure 32.15 shows only one symbolic sample point.

32.4.1.3 Baud Rate

Either the CAN channel system clock (clean clock) or the external oscillator clock can be selected globally for all CAN channels as CAN communication clock.

The transfer speed is determined by the DLL clock, the divide-by-N value of the baud rate prescaler, and the number of TQs in one bit.

32.4.1.2 CAN位时序

在CAN协议中，通信帧中的每个位由三个段组成，可以使用相关的CFDCnNCFG和CFDCnDCFG*1寄存器为每个通道单独配置。

注1.该寄存器在经典CAN功能中不可用。

图32.15显示了一个位的分段组成和其中的采样点。

在这些段中，时间段1(TSEG1)和时间段2(TSEG2)用于指定采样点的位置，因此可以通过更改值来更改CAN总线上每个位的采样时序这些细分市场。

此时序的最小分辨率称为时间量子(TQ)，它由提供给CAN通道的时钟频率和波特率预分频器的N分频值（标称和数据速率）决定。

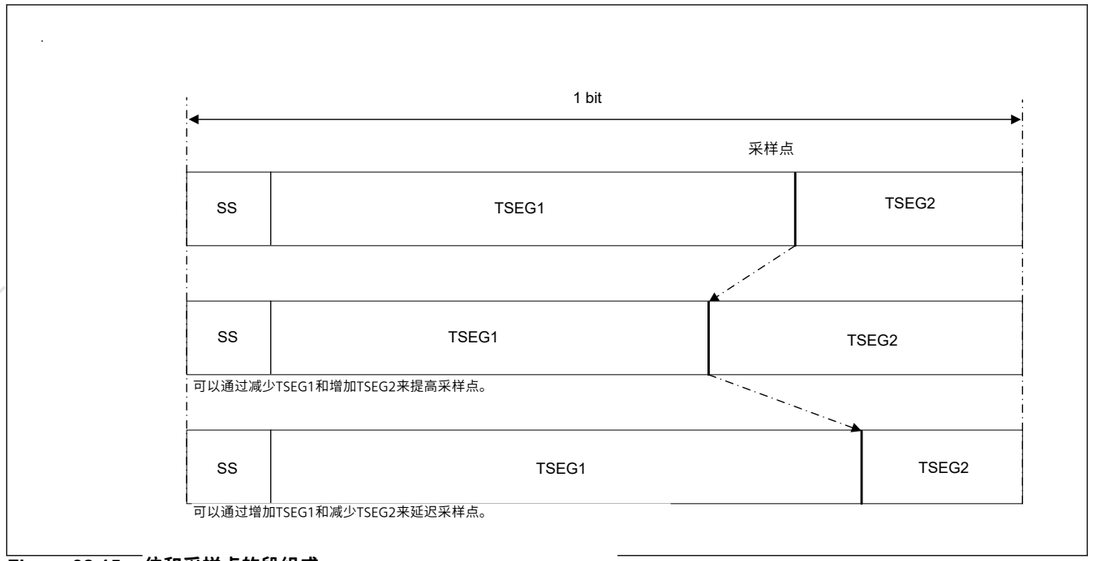

Figure 32.15 位和采样点的段组成

1.SS：同步段
该段用于通过监视帧间空间期间的隐性到显性边缘来同步位。这包括中断、暂停传输、总线空闲、总线空闲期间以及所有可以开始传输的节点。

2.TSEG1：时间段1
该段吸收CAN网络上的物理延迟。网络上的物理延迟是总线延迟、输入比较器延迟和输出驱动器延迟总和的两倍。它可以通过SJW加长。

3.TSEG2：时间段2
该段用于通过执行重新同步来纠正相位误差。它可以被SJW缩短。在发送或接收消息时，某些节点之间的通信帧可能会由于振荡器频率的漂移或传输路径的延迟而失去同步。这被称为相位误差。

4.SJW：再同步跳转宽度
这是由于相位误差而变得不同步的位可以被纠正的最大宽度。

图32.15只显示了一个符号采样点。

32.4.1.3 Baud Rate

CAN通道系统时钟（干净时钟）或外部振荡器时钟可以全局选择所有CAN通道作为CAN通信时钟。

传输速度由DLL时钟、波特率预分频器的N分频值和一位TQ的数量决定。

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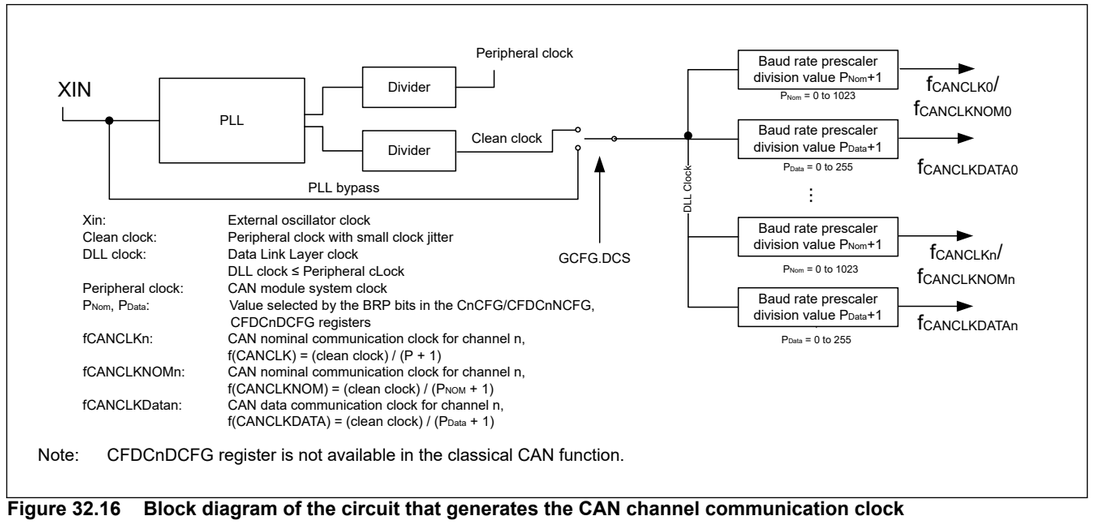
$$baudrate = \frac{DLL_Clock}{(number_of_time_quanta_per_bit) \times (BRP + 1)}$$

Figure 32.16 shows a block diagram of the circuit that generates the CAN channel system clock and Table 32.15 shows a baud rate examples.



Note: CFDCnDCFG register is not available in the classical CAN function.

Figure 32.16 Block diagram of the circuit that generates the CAN channel communication clock

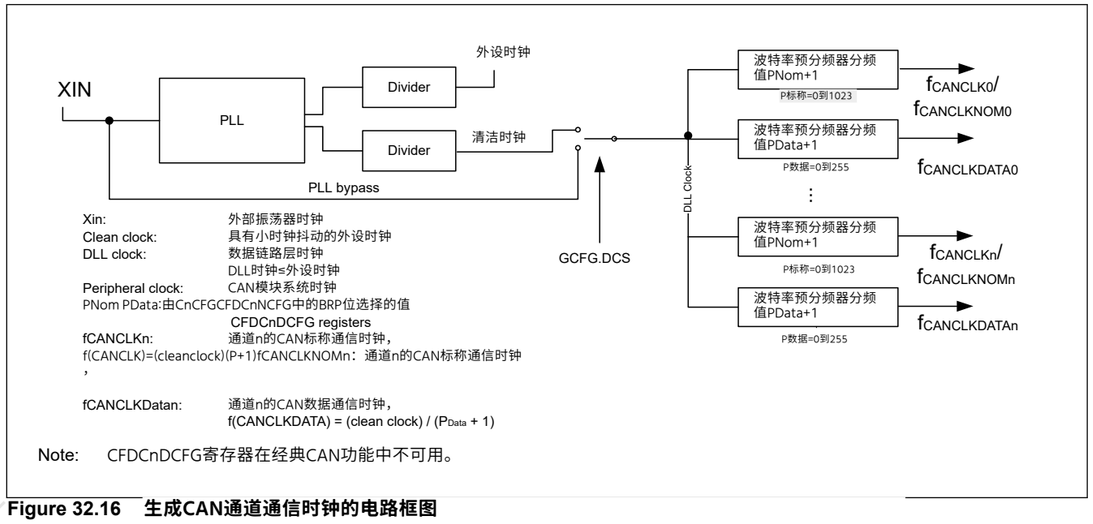
Table 32.15 Nominal baud rate calculation formula and example CAN communication configurations

Baud rate calculation formula	(DLL clock) (baud rate prescaler divide-by-N value*1) × (number of TQs in one bit)								
	80 MHz	40 MHz	32 MHz	30 MHz	24 MHz	20 MHz	16 MHz	10 MHz	8 MHz*2
1 Mbps	8TQ (10) 20TQ (4)	8TQ (5) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (3) 15TQ (2)	8TQ (3) 12TQ (2) 24TQ (1)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)	10TQ (1)	8TQ (1)
500 Kbps	8TQ (20) 20TQ (8)	8TQ (10) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (6) 15TQ (4) 20TQ (3)	8TQ (6) 12TQ (4) 24TQ (2)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)
250 Kbps	8TQ (40) 20TQ (16)	8TQ (20) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (12) 15TQ (8) 20TQ (6)	8TQ (12) 12TQ (8) 24TQ (4)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)
125 Kbps	8TQ (80) 20TQ (32)	8TQ (40) 20TQ (16)	8TQ (32) 16TQ (16)	10TQ (24) 15TQ (16) 20TQ (12)	8TQ (24) 12TQ (16) 24TQ (8)	10TQ (16) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)
83.3 Kbps	8TQ (120) 12TQ (80) 16TQ (60) 24TQ (40)	8TQ (60) 12TQ (40) 16TQ (30) 24TQ (20)	8TQ (48) 12TQ (32) 16TQ (24) 24TQ (16)	8TQ (45) 10TQ (36) 12TQ (30) 15TQ (24) 20TQ (18) 24TQ (15)	8TQ (36) 12TQ (24) 16TQ (18) 24TQ (12)	8TQ (30) 10TQ (24) 12TQ (20) 15TQ (16) 16TQ (15) 20TQ (12) 24TQ (10)	8TQ (24) 12TQ (16) 16TQ (12) 24TQ (8)	8TQ (15) 10TQ (12) 12TQ (10) 15TQ (8) 20TQ (6) 24TQ (5)	8TQ (12)
33.3 Kbps	8TQ (300) 12TQ (200) 16TQ (150) 20TQ (120) 24TQ (100)	8TQ (150) 12TQ (100) 16TQ (75) 20TQ (60) 24TQ (50)	8TQ (120) 10TQ (96) 12TQ (80) 15TQ (64) 16TQ (60) 20TQ (48) 24TQ (40)	10TQ (90) 12TQ (75) 15TQ (60) 20TQ (45)	8TQ (90) 10TQ (72) 12TQ (60) 15TQ (48) 16TQ (45) 20TQ (36) 24TQ (30)	8TQ (75) 10TQ (60) 12TQ (50) 15TQ (40) 20TQ (30) 24TQ (25)	8TQ (60) 10TQ (48) 12TQ (40) 15TQ (32) 16TQ (30) 20TQ (24) 24TQ (20)	10TQ (30) 12TQ (25) 15TQ (20) 20TQ (15)	8TQ (30)

Note: Shown in ( ) are the baud rate prescaler divide-by-N value.
Note 1. Baud rate prescaler divide-by-N value = P + 1 (P = 0 - 1023) P: value selected by the BRP bits in the Channel Configuration Registers.

$$baudrate = \frac{DLL_Clock}{(number_of_time_quanta_per_bit) \times (BRP + 1)}$$

图32.16显示了生成CAN通道系统时钟的电路框图，表32.15显示了波特率示例。



Note: CFDCnDCFG寄存器在经典CAN功能中不可用。

Figure 32.16 生成CAN通道通信时钟的电路框图

Table 32.15 标称波特率计算公式和示例CAN通信配置

波特率计算公式	（DLL时钟）（波特率预分频器除以N值*1）×（一位TQ的数量）								
	80 MHz	40 MHz	32 MHz	30 MHz	24 MHz	20 MHz	16 MHz	10 MHz	8 MHz*2
1 Mbps	8TQ (10) 20TQ (4)	8TQ (5) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (3) 15TQ (2)	8TQ (3) 12TQ (2) 24TQ (1)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)	10TQ (1)	8TQ (1)
500 Kbps	8TQ (20) 20TQ (8)	8TQ (10) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (6) 15TQ (4) 20TQ (3)	8TQ (6) 12TQ (4) 24TQ (2)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)	10TQ (2) 20TQ (1)	8TQ (2) 16TQ (1)
250 Kbps	8TQ (40) 20TQ (16)	8TQ (20) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (12) 15TQ (8) 20TQ (6)	8TQ (12) 12TQ (8) 24TQ (4)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)	10TQ (4) 20TQ (2)	8TQ (4) 16TQ (2)
125 Kbps	8TQ (80) 20TQ (32)	8TQ (40) 20TQ (16)	8TQ (32) 16TQ (16)	10TQ (24) 15TQ (16) 20TQ (12)	8TQ (24) 12TQ (16) 24TQ (8)	10TQ (16) 20TQ (8)	8TQ (16) 16TQ (8)	10TQ (8) 20TQ (4)	8TQ (8) 16TQ (4)
83.3 Kbps	8TQ (120) 12TQ (80) 16TQ (60) 24TQ (40)	8TQ (60) 12TQ (40) 16TQ (30) 24TQ (20)	8TQ (48) 12TQ (32) 16TQ (24) 24TQ (16)	8TQ (45) 10TQ (36) 12TQ (30) 15TQ (24) 20TQ (18) 24TQ (15)	8TQ (36) 12TQ (24) 16TQ (18) 24TQ (12)	8TQ (30) 10TQ (24) 12TQ (20) 15TQ (16) 16TQ (15) 20TQ (12) 24TQ (10)	8TQ (24) 12TQ (16) 16TQ (12) 24TQ (8)	8TQ (15) 10TQ (12) 12TQ (10) 15TQ (8) 20TQ (6) 24TQ (5)	8TQ (12)
33.3 Kbps	8TQ (300) 12TQ (200) 16TQ (150) 20TQ (120) 24TQ (100)	8TQ (150) 12TQ (100) 16TQ (75) 20TQ (60) 24TQ (50)	8TQ (120) 10TQ (96) 12TQ (80) 15TQ (64) 16TQ (60) 20TQ (48) 24TQ (40)	10TQ (90) 12TQ (75) 15TQ (60) 20TQ (45)	8TQ (90) 10TQ (72) 12TQ (60) 15TQ (48) 16TQ (45) 20TQ (36) 24TQ (30)	8TQ (75) 10TQ (60) 12TQ (50) 15TQ (40) 20TQ (30) 24TQ (25)	8TQ (60) 10TQ (48) 12TQ (40) 15TQ (32) 16TQ (30) 20TQ (24) 24TQ (20)	10TQ (30) 12TQ (25) 15TQ (20) 20TQ (15)	8TQ (30)

Note: ()中显示的是波特率预分频器除以N的值。
注1.波特率预分频器除以N值=P+1(P=01023)P：由通道配置中的BRP位选择的值
Registers.

Note 2. Minimum frequency to achieve maximum nominal baud rate of 1 Mbps.

Table 32.16 Baud rate calculation example for nominal and data bit rate CAN communication configurations

Baud rate calculation formula	(DLL clock) (baud rate prescaler divide-by-N value*1) × (number of TQs in one bit)		
	80 MHz	40 MHz	20 MHz
Nominal 1 Mbps Data 8 Mbps	80TQ (1)	40TQ (1)	20TQ (1)
	10TQ (1)	5TQ (1)	Not possible
Nominal 1 Mbps Data 5 Mbps	80TQ (1)	40TQ (1)	20TQ (1)
	16TQ (1)	8TQ (1)	Not possible
Nominal 500 Kbps Data 2 Mbps	160TQ (1)	80TQ (1)	40TQ (1)
	40TQ (1)	20TQ (1)	10TQ (1)

Note: Shown in ( ) are the baud rate prescaler divide-by-N values and this table is not available in the classical CAN function.
Note 1. Baud rate prescaler divide-by-N value = P + 1 (P = 0 - 1023) P: value selected by the BRP bits in the Channel Configuration Registers.

For optimum clock tolerance in networks using the FD frame format, the length of the time quantum should be the same in nominal bit time and in data bit time. This means CFDCnNCFG.NBRP = CFDCnDCFG.DBRP.

Additionally, if transceiver delay compensation is used, do not program the CFDCnDCFG.DBRP bit to be greater than 1, as 1 means divide by 2.

32.4.1.4 Setting of CAN Clock, Bit Timing and Baud Rate

Figure 32.17 shows the procedure for setting the CAN clock and the baud rate for each channel.

These settings should be performed during Channel Reset mode (Configuration mode) for the CAN channels.

Before going to channel communication state, the baud rate must be configured, otherwise the mode does not switch correctly.

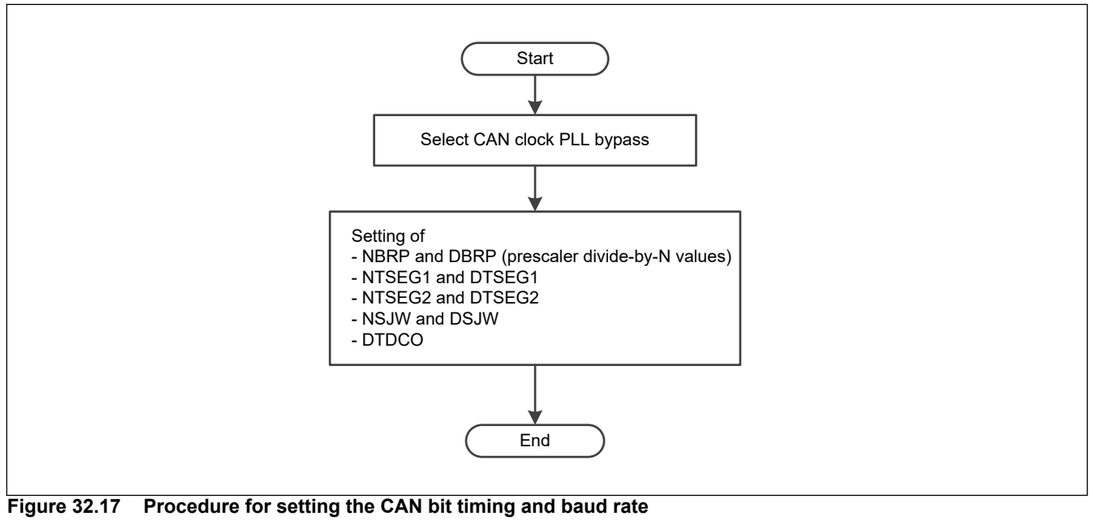


Figure 32.17 Procedure for setting the CAN bit timing and baud rate

32.4.1.5 Transmitter Delay Compensation

This chapter is not valid for classical CAN.

注2.实现1Mbps的最大标称波特率的最小频率。

Table 32.16 标称和数据比特率CAN通信配置的波特率计算示例

波特率计算公式	（DLL时钟）（波特率预分频器除以N值*1）×（一位TQ的数量）		
	80 MHz	40 MHz	20 MHz
Nominal 1 Mbps Data 8 Mbps	80TQ (1)	40TQ (1)	20TQ (1)
	10TQ (1)	5TQ (1)	不可能
Nominal 1 Mbps Data 5 Mbps	80TQ (1)	40TQ (1)	20TQ (1)
	16TQ (1)	8TQ (1)	不可能
Nominal 500 Kbps Data 2 Mbps	160TQ (1)	80TQ (1)	40TQ (1)
	40TQ (1)	20TQ (1)	10TQ (1)

Note: ()中显示的是波特率预分频器除以N的值，该表在经典CAN函数中不可用。
注1.波特率预分频器除以N值=P+1(P=01023)P：由通道配置中的BRP位选择的值
Registers.

为了在使用FD帧格式的网络中获得最佳时钟容限，时间片的长度在标称位时间和数据位时间中应该相同。这意味着CFDCnNCFG.NBRP=CFDCnDCFG.DBRP。

此外，如果使用收发器延迟补偿，请勿将CFDCnDCFG.DBRP位编程为大于1，因为1表示除以2。

32.4.1.4 CAN时钟、位时序和波特率的设置

图32.17显示了为每个通道设置CAN时钟和波特率的过程。

这些设置应在CAN通道的通道复位模式（配置模式）期间执行。

在进入通道通信状态之前，必须配置波特率，否则无法正确切换模式。

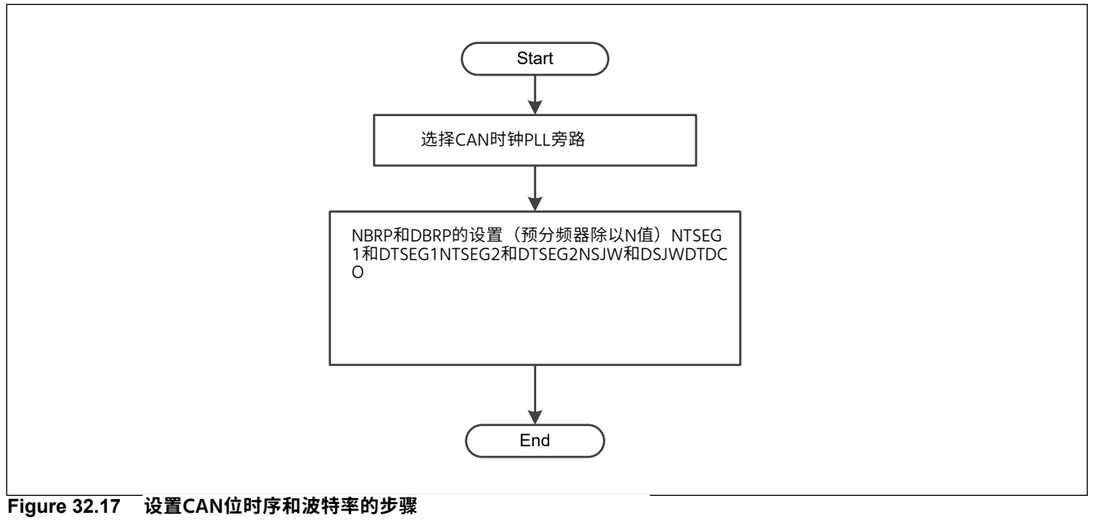


Figure 32.17 设置CAN位时序和波特率的步骤

32.4.1.5 发射机延迟补偿

本章不适用于经典CAN。

When a high baud rate is used such as 5 to 8 Mbps for the data phase, the transmitter delay can become greater than TSEG1. In this case, the transmitter always detects a bit-error in the data phase of the CAN-FD frame. The TDC compensates for the inability of the transmitter to receive its own transmitted bit at the sample point of that bit.

There is another symbolic sample point known as the Secondary Sample Point (SSP) that is used only during the data phase of CAN-FD frames. This is derived from the Transceiver Delay Compensation Result bit (CFDCnFDSTS.TDCR) as shown in Figure 32.18.

The resolution of the configuration, measured and offset values is based on the CAN channel DLL clock.

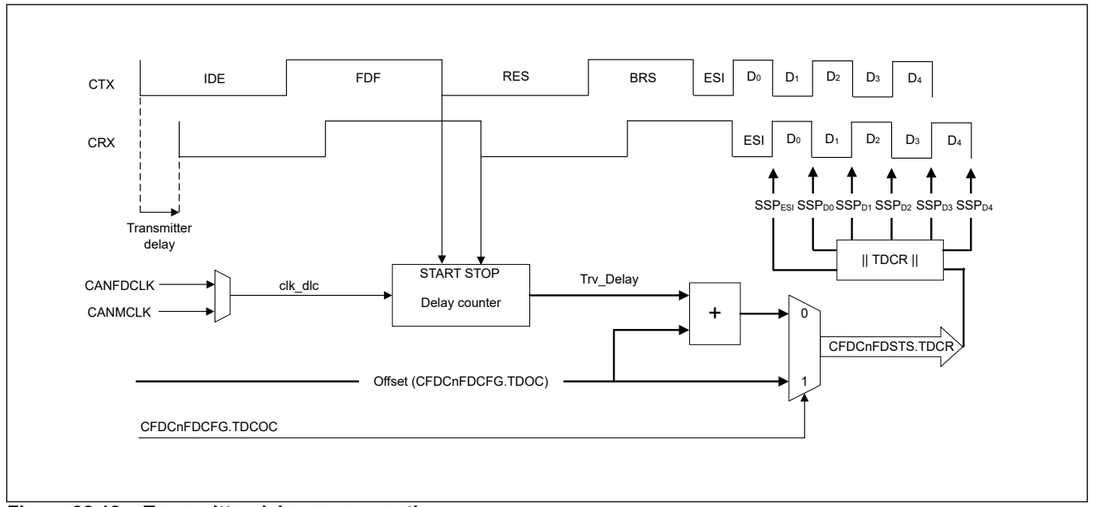


Figure 32.18 Transmitter delay compensation

The measured Trv_Delay is based on the number of clk_dlc clock cycles.The delay is counted up by one for each started clock until the dominant value is seen on CAN_RX. Figure 32.19 shows the measured result. Trv_Delay counted to maximum 127 with a clk_dlc clock.

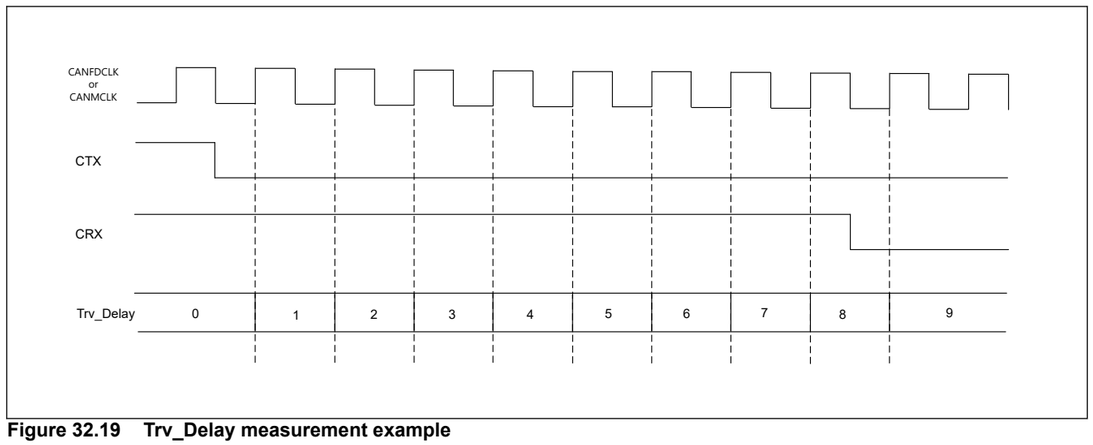


Figure 32.19 Trv_Delay measurement example

The SSP is calculated by taking the result from CFDCnFDSTS.TDCR and rounding the value down to the nearest integer number of data time quanta.

Figure 32.20 shows the positioning of the secondary sample point. When CFDCnFDCFG.TDCOC is equal to 0, the SSP is equal to the Trv_Delay (measured delay) + CFDCnFDCFG.TDCO, rounded down to the nearest integer number of time quanta. Usually, the TDCO value should have the size of (SyncSegmentdata + TSEG1data) to position the SSP to a theoretical location of the sample point.

当数据阶段使用高波特率（例如5到8Mbps）时，发送器延迟可能会大于TSEG1。在这种情况下，发送器总是在CAN-FD帧的数据阶段检测到位错误。TDC补偿发送器无法在该位的采样点接收其自己的发送位。

还有另一个符号采样点，称为辅助采样点(SSP)，仅在CAN-FD帧的数据阶段使用。这源自收发器延迟补偿结果位(CFDCnFDSTS.TDCR)，如图32.18所示。

配置、测量值和偏移值的分辨率基于CAN通道DLL时钟。

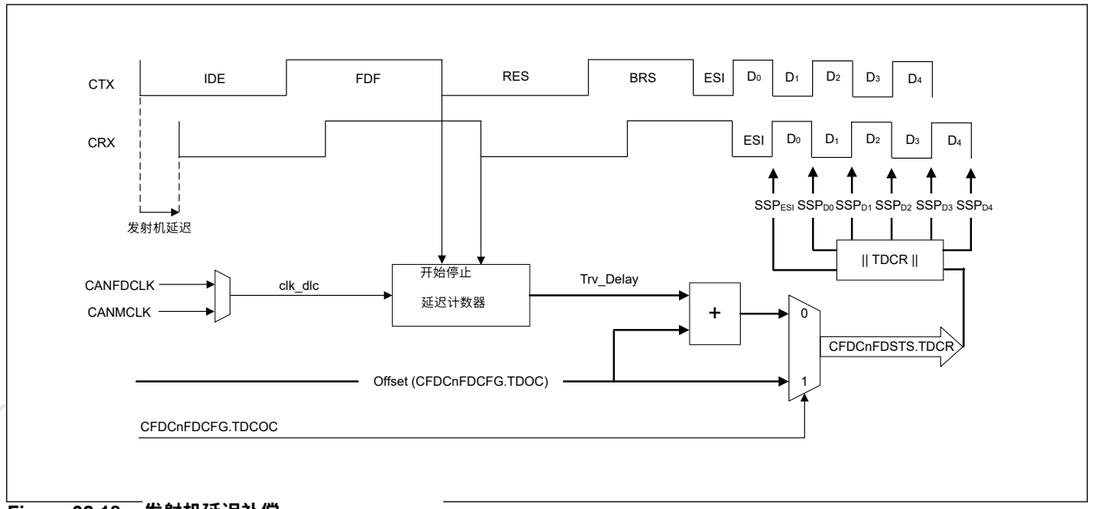


Figure 32.18 发射机延迟补偿

测得的Trv_Delay基于clk_dlc时钟周期数。对于每个启动的时钟，延迟将加一，直到在CAN_RX上看到显性值。图32.19显示了测量结果。使用clk_dlc时钟时，Trv_Delay最大计数为127。

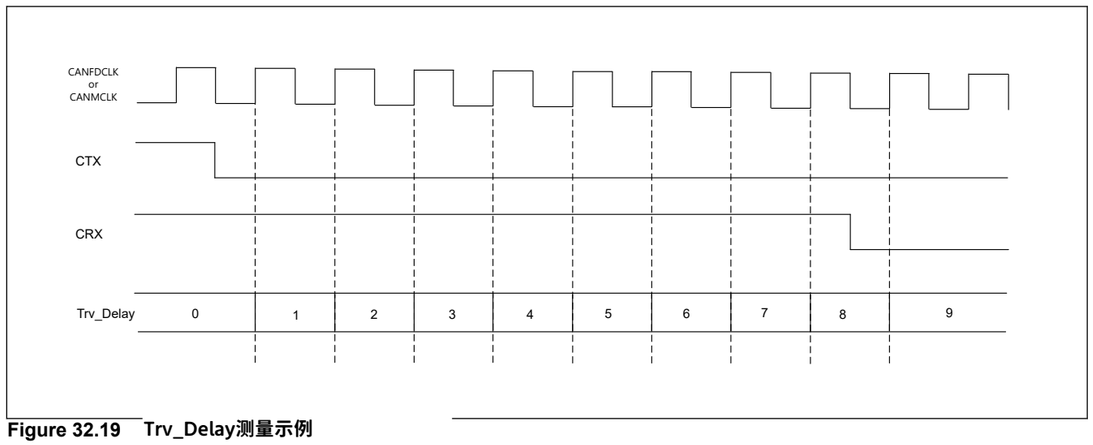


Figure 32.19 Trv_Delay测量示例

SSP的计算方法是从CFDCnFDSTS.TDCR获取结果并将该值向下舍入到最接近的数据时间量整数。

图32.20显示了辅助采样点的定位。当CFDCnFDCFG.TDCOC等于0时，SSP等于Trv_Delay（测量延迟）+CFDCnFDCFG.TDCO，向下舍入到最接近的整数时间量。通常，TDCO值的大小应为(SyncSegmentdata+TSEG1data)以将SSP定位到采样点的理论位置。

If the CFDCnFDCFG.TDCOC is equal to 1, the SSP is defined by CFDCnFDCFG.TDCO. If CFDCnDCFG.DBRP is greater than 0, the value is also rounded down to the nearest integer number of time quanta.

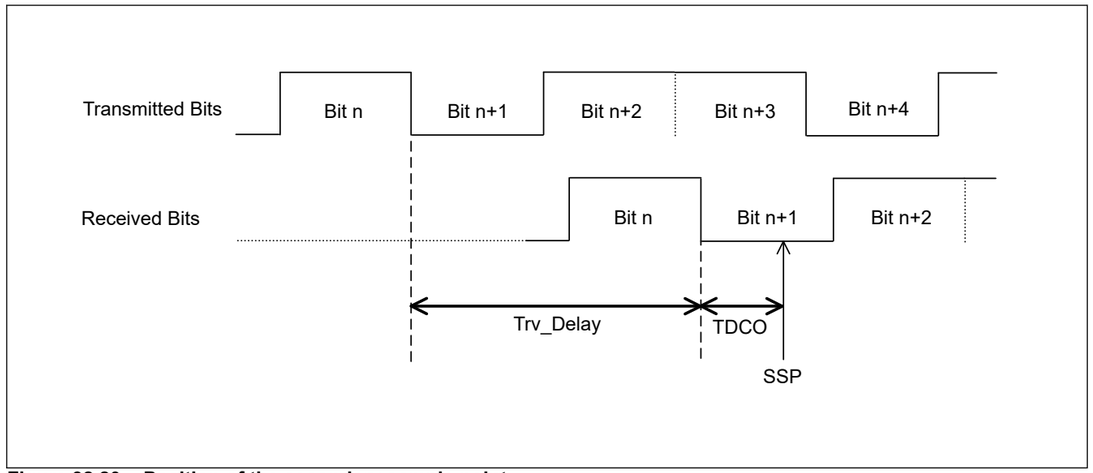


Figure 32.20 Position of the secondary sample point

The maximum delay (Trv_Delay + TDCO) which can be compensated by the CAN-FD module is (6 data bits - 2clk_dlc).

The ISO 11898-1 allows you to set different values for BRP_data and BRP_nom.

If different values are used for CFDCnNCFG.NBRP and CFDCnDCFG.DBRP, then two CAN nodes may be out of synchronization at the point when the bit rate changes from nominal bit rate to data bit rate after sample point of the BRS bit. This condition is shown in Figure 32.21.

The length of the time quantum should be the same in the nominal bit time and in the data bit time. This means CFDCnNCFG.NBRP = CFDCnDCFG.DBRP.

Different bit rates can be achieved by selecting different configuration values for the Time Segments. The nominal bit rate can be configured from 8 to 385 TQs and the data bit rate from 5 to 49 TQs.

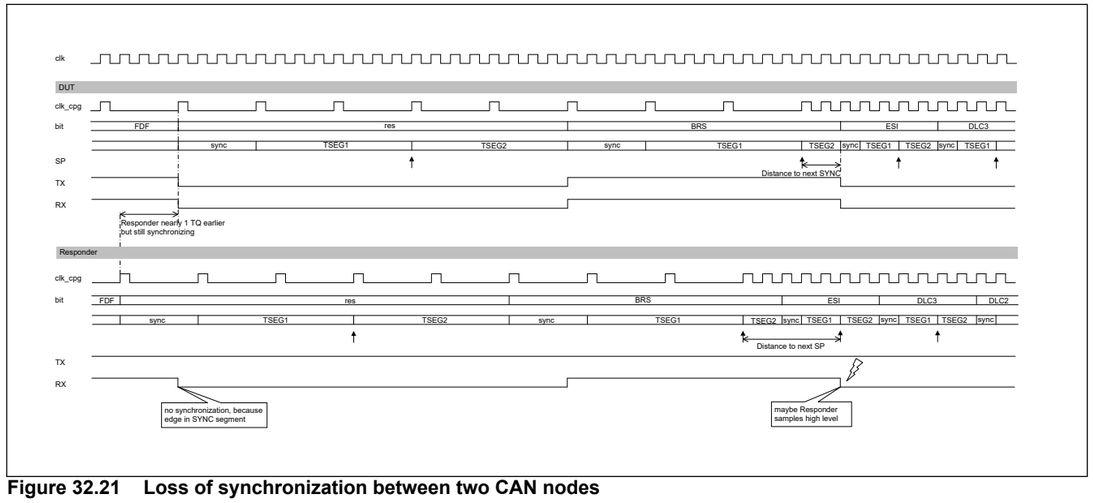


Figure 32.21 Loss of synchronization between two CAN nodes

The transmitter delay compensation measurement result is updated at the falling edge from FDF bit to RES bit when configured accordingly (CFDCnFDCFG.TDCE = 1, CFDCnFDCFG.TDCOC = 0).

Figure 32.22 shows the read flow to get the measured transmitter delay compensation result.

如果CFDCnFDCFG.TDCOC等于1，则SSP由CFDCnFDCFG.TDCO定义。如果CFDCnDCFG.DBRP大于0，则该值也向下舍入到最接近的整数时间量。

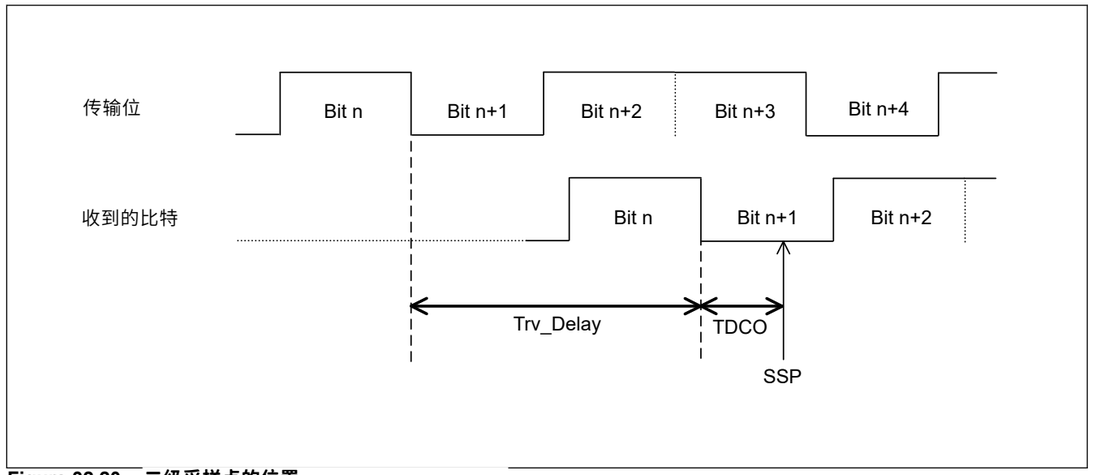


Figure 32.20 二级采样点的位置

CAN-FD模块可以补偿的最大延迟（Trv_Delay+TDCO）为（6个数据位2clk_dlc）。

ISO11898-1允许您为BRP_data和BRP_nom设置不同的值。

如果CFDCnNCFG.NBRP和CFDCnDCFG.DBRP使用不同的值，则在BRS位采样点之后，当比特率从标称比特率变为数据比特率时，两个CAN节点可能不同步。这种情况如图32.21所示。

时间段的长度在标称位时间和数据位时间中应该相同。这表示CFDCnNCFG.NBRP = CFDCnDCFG.DBRP.

通过为时间段选择不同的配置值可以实现不同的比特率。标称比特率可配置为8至385TQ，数据比特率可配置为5至49TQ。

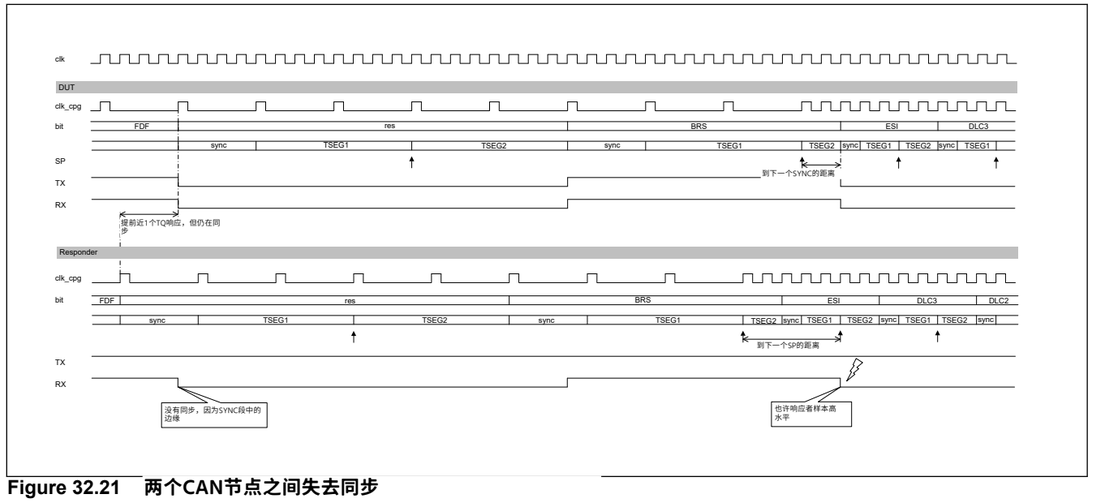


Figure 32.21 两个CAN节点之间失去同步

当相应配置时（CFDCnFDCFG.TDCE=1，CFDCnFDCFG.TDCOC=0），发送器延迟补偿测量结果在从FDF位到RES位的下降沿更新。

图32.22显示了读取流程以获得测量的发送器延迟补偿结果。

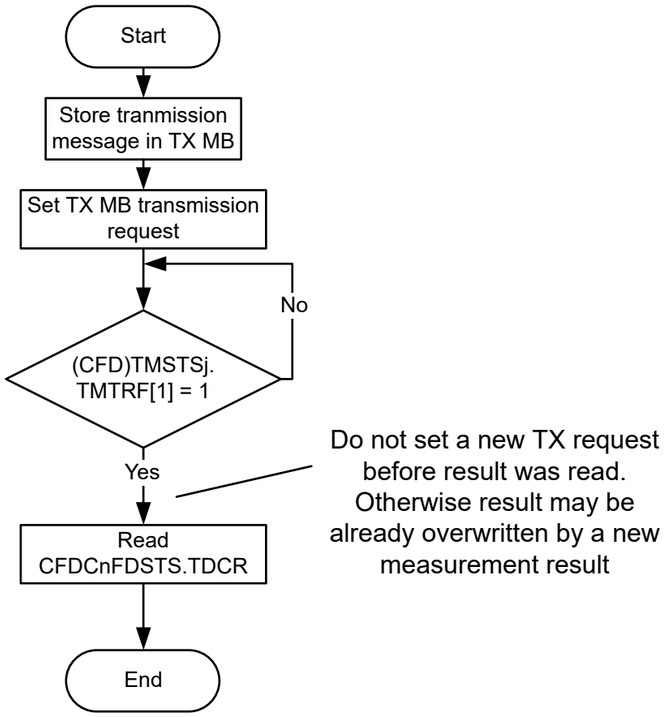


Figure 32.22 TDC result read flow

32.4.2 CAN Module Configuration after Hardware Reset

After a hardware reset (power on reset) or after setting and clearing a CFDGRSTC.SRST bit, the CAN-FD module enters Global Sleep mode automatically.

To enable configuration of the CAN-FD module, you must exit Sleep mode by clearing the Global Sleep Request bit CFDGCTR.GSLPR to 0.

After a hardware reset, the module starts RAM initialization, the CFDGSTS.GRAMINIT bit in the Global Status Register is set automatically to indicate that the CAN-FD logic is initializing the RAM.

After RAM initialization is complete, this bit is cleared automatically.

RAM initialization is necessary to avoid setting of false ECC error flag after HW reset the random data presented in the RAM.

Do not access registers of CAN-FD in either read or write until RAM initialization is complete and the CFDGSTS.GRAMINIT bit is cleared.

Before going to communication mode, the Global Acceptance Filter List and message FIFO buffers must be configured. In addition, each required CAN channel must be configured such as CAN bit timing. For this configuration, all required CAN channels must be released from Channel Sleep mode and must be configured for communication in Channel Reset mode (Configuration mode).

Figure 32.23 shows the configuration procedure. For details about each step, seesection 32.5. Acceptance Filtering Function using Global Acceptance Filter List (AFL), section 32.6. FIFO Buffers and Normal Message Buffer Configuration, section 32.7. Interrupts and DMA and section 32.4.1.3. Baud Rate.

The CAN-FD module does not perform the RAM initialization sequence after executing a software reset by setting CFDGRSTC.SRST.

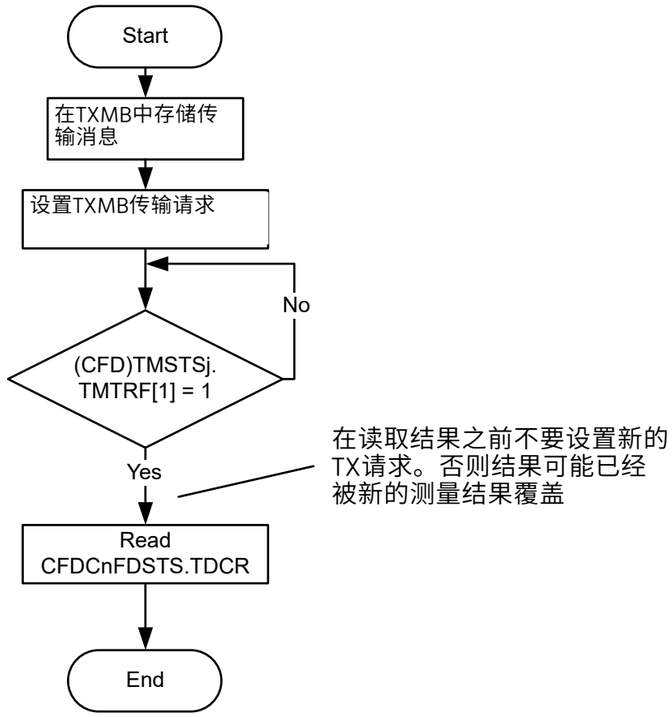


Figure 32.22 TDC结果读取流程

32.4.2 硬件复位后的CAN模块配置

硬件复位（上电复位）或设置和清除CFDGRSTC.SRST位后，CAN-FD模块进入全局睡眠模式自动。

要启用CAN-FD模块的配置，您必须通过清除全局休眠请求位来退出休眠模式CFDGCTR.GSLPR to 0.

硬件复位后，模块开始RAM初始化，全局状态寄存器中的CFDGSTS.GRAMINIT位自动置位，表示CAN-FD逻辑正在初始化RAM。

RAM初始化完成后，该位自动清零。

RAM初始化是必要的，以避免在硬件重置随机数据后设置错误的ECC错误标志RAM.

在RAM初始化完成之前，不要以读或写方式访问CAN-FD的寄存器并且CFDGSTS.GRAMINIT位清零。

在进入通信模式之前，必须配置全局接受过滤器列表和消息FIFO缓冲区。此外，必须配置每个所需的CAN通道，例如CAN位时序。对于此配置，所有必需的CAN通道必须从通道休眠模式中释放，并且必须配置为在通道复位模式（配置模式）下进行通信。

图32.23显示了配置过程。有关每个步骤的详细信息，请参见第32.5节。使用全局接受过滤器列表(AFL)的接受过滤功能，第32.6节。FIFO缓冲区和正常消息缓冲区配置，第32.7节。中断和DMA以及第32.4.1.3节。波特率。

CAN-FD模块在通过设置执行软件复位后不执行RAM初始化序列CFDGRSTC.SRST.

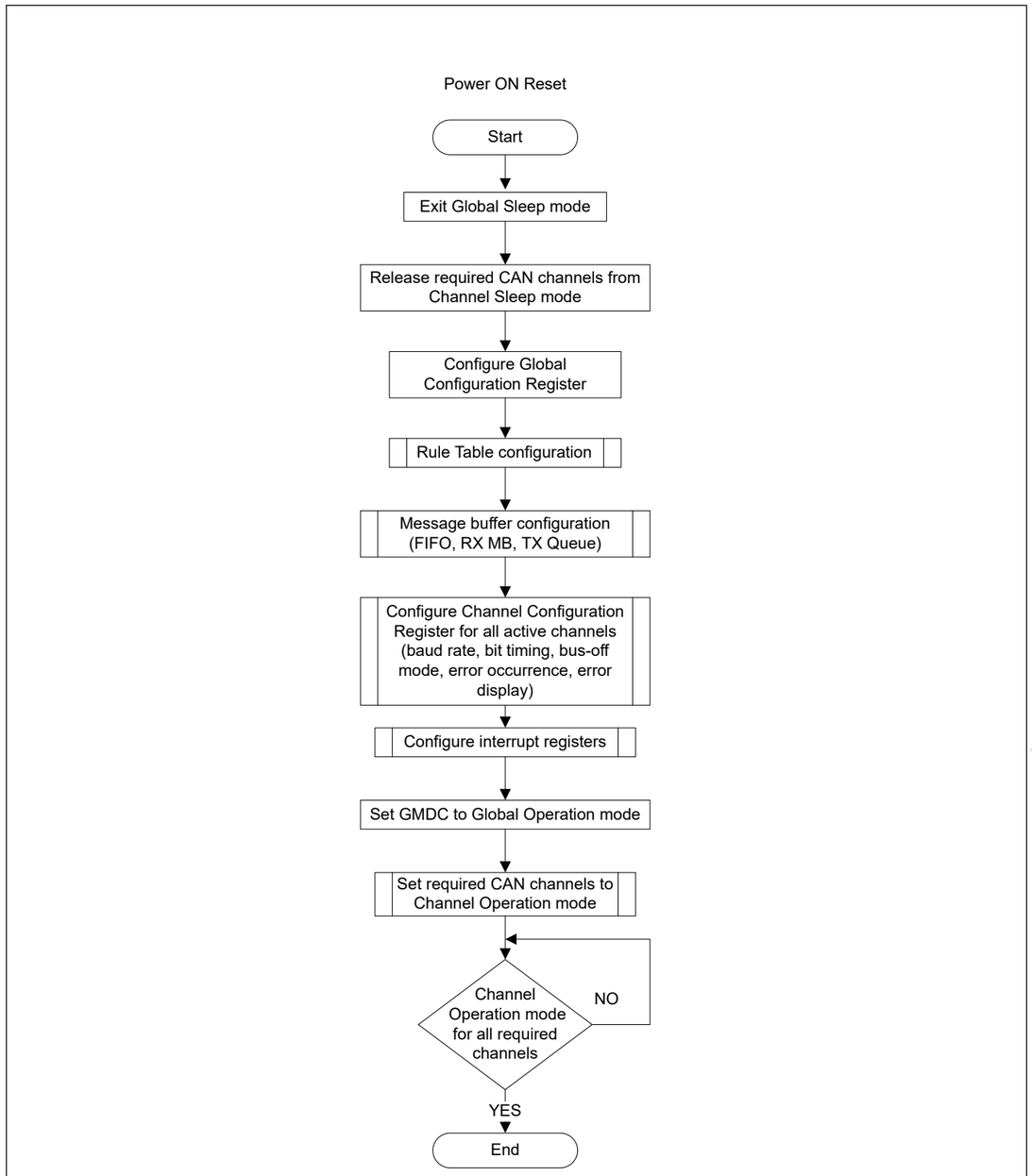


Figure 32.23 Configuration procedure after a hardware reset

32.5 Acceptance Filtering Function using Global Acceptance Filter List (AFL)

32.5.1 Overview

The CAN-FD module can handle message acceptance filtering for all channels with a global Acceptance Filter List (called AFL). Each element of the AFL defines a filter rule for messages received on a specific channel.

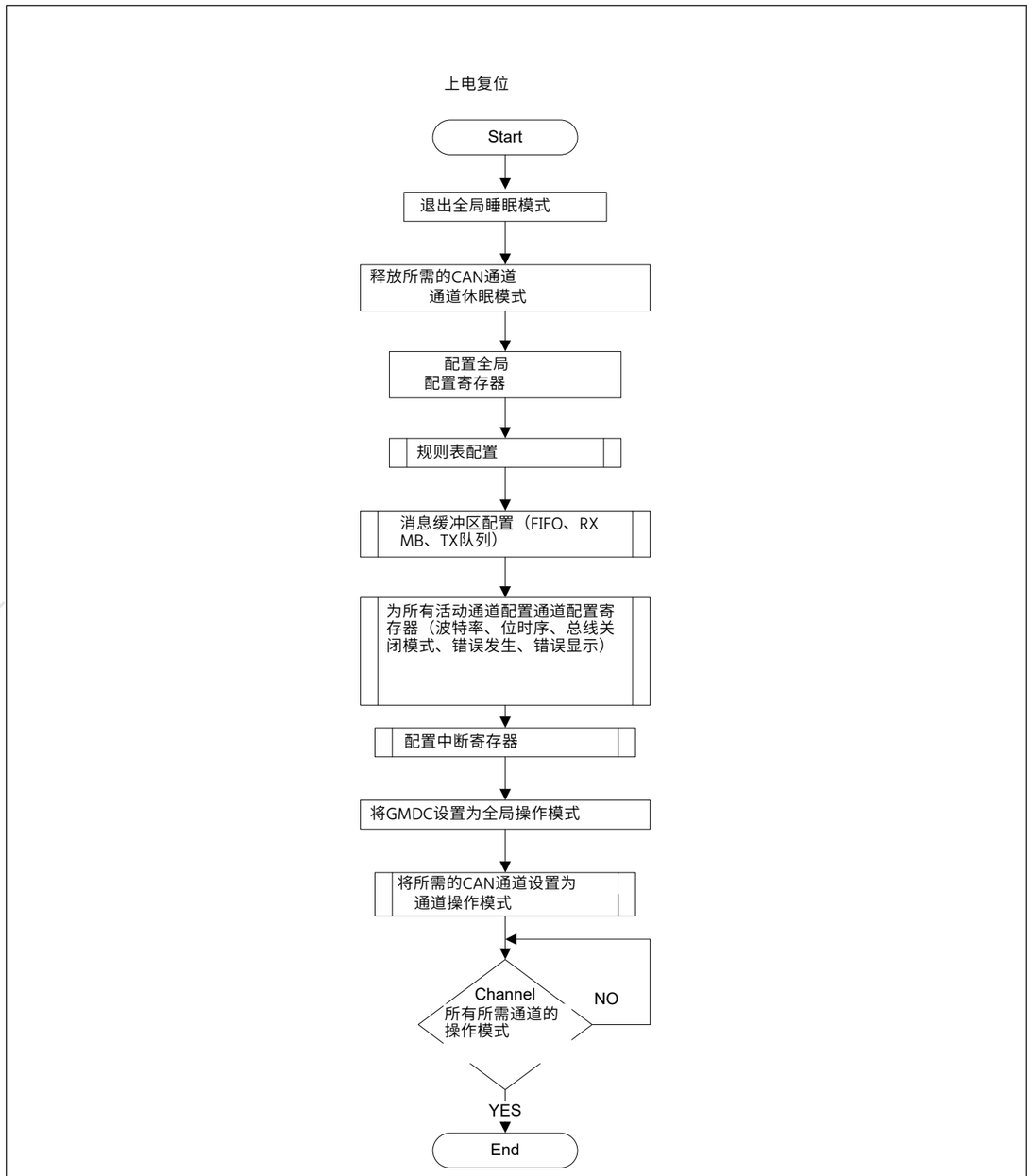


Figure 32.23 硬件复位后的配置过程

32.5 使用全局接受过滤器列表(AFL)的接受过滤功能

32.5.1 Overview

CAN-FD模块可以使用全局接受过滤器列表（称为AFL)。AFL的每个元素都为在特定通道上接收到的消息定义了一个过滤规则。

The following actions are performed based on the AFL entries:

- Acceptance filtering based on received CAN Identifier and masking
- DLC filtering based on received DLC value
- Message data payload according to the CFDGCFG.CMPOC bit*1
- Storage of accepted messages in the message buffer objects defined in the related AFL entry
- Attaching a 16-bit pointer to the stored messages defined in the related AFL entry, for example to support AUTOSAR applications
- Attaching a 2-bit information label to the stored messages defined in the related AFL entry

Note 1. This feature is not available in the classical CAN function.

The 2-channel CAN-FD module allows a maximum of 128 AFL entries across all channels with a maximum of 64 AFL entries per channel.

During acceptance filtering process, each AFL entry in a channel is checked against the received message by the acceptance filter unit. The check starts from the lowest AFL entry number for this channel.

AFL search stops when a match of the received identifier with a configured identifier/mask combination occurs or when the received identifier has been compared against all AFL entries defined for the related channel. If no match occurs, then the received message is rejected. No notification is given to the application in this case.

Additionally, an automatic DLC filtering is performed for each accepted message if DLC check is globally enabled. If the DLC value of the received message is equal to or higher than the configured DLC value in the matching AFL entry, the DLC check is passed.

If DLC replacement (CFDGCFG.DRE bit) is enabled, DLC value configured in the matching AFL entry is greater than 0x0 and DLC check passes, then the configured value of DLC in the matching AFL entry is stored in the destination RXMB or FIFO Buffer.

If the received value of DLC is greater than the configured DLC value in the matching AFL entry, then the additional data bytes received on the CAN Bus are not stored in the destination RXMB or FIFO Buffer. These additional data bytes are stored as 0x00 in the destination RXMB or FIFO Buffer.

If DLC replacement is enabled and DLC value of matching AFL entry is 0x0, then the received value of DLC is stored in the destination RX MB or FIFO Buffer.

If DLC replacement (the CFDGCFG.DRE bit) is disabled and DLC check passes, then the received value of DLC on the CAN bus is stored in the destination RXMB or FIFO buffer.

If the received value of DLC is greater than the configured DLC value in the matching AFL entry, then the additional data bytes received from the CAN bus are also stored in the destination RXMB or FIFO buffer.

If DLC value of the received message is less than the configured DLC value in the matching AFL entry, then DLC check fails. In this case, the received message is rejected and is not stored in any RXMB or FIFO buffer.

Additionally, DLC check failure is flagged by the DLC Error Flag in the Global Error Flag Register. If configured, an error interrupt is also generated. The DLC replacement configuration has no impact if the DLC check fails.

If a message has passed both acceptance filtering and DLC filtering, it is stored in a single reception message buffer and/or in FIFO buffers configured for reception or gateway function.

This message storage target information is also defined in the same AFL entry. Do not set a target at the AFL entry which is not configured.

Each accepted received message can be stored into a maximum of 8 different target destinations (single reception message buffer and/or FIFO buffers).

The programming of more than eight target destinations is not allowed. If more destinations are programmed, then the internal timing might lead to a race condition that prevents the storage of received messages in the message RAM.. Correct configuration of the numbers of target destination is the responsibility of the application.

Additional protection mechanism is made for the case when a received message contains more data payload Bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCn.RFPLS or CFDCFCCn.CFPLS).

If CFDGCFG.CMPOC = 0, the message is completely rejected and is stored in the target destination. When CFDGCFG.CMPOC = 0 and RX or Common FIFO full including the received message contains more data payload bytes

根据AFL条目执行以下操作：

●基于接收到的CAN标识符和掩码的接受过滤

●根据接收到的DLC值进行DLC过滤

●根据CFDGCFG.CMPOC位的消息数据有效负载*1

●将接受的消息存储在相关AFL条目中定义的消息缓冲区对象中

●将16位指针附加到相关AFL条目中定义的存储消息，例如以支持AUTOSAR应用程序

●将2位信息标签附加到相关AFL条目中定义的存储消息

注1.此功能在经典CAN功能中不可用。

2通道CAN-FD模块允许跨所有通道最多128个AFL条目，每个通道最多64个AFL条目。

在接受过滤过程中，接受过滤单元根据接收到的消息检查通道中的每个AFL条目。检查从该通道的最低AFL条目号开始。

当接收到的标识符与配置的标识符掩码组合发生匹配时，或者当接收到的标识符已与为相关通道定义的所有AFL条目进行比较时，AFL搜索停止。如果不匹配，则拒绝接收到的消息。在这种情况下，不会向应用程序发出通知。

此外，如果全局启用DLC检查，则会对每个接受的消息执行自动DLC过滤。如果接收到的消息的DLC值等于或高于匹配的AFL条目中配置的DLC值，则DLC检查通过。

如果启用DLC替换（CFDGCFG.DRE位），匹配AFL条目中配置的DLC值大于0x0并且DLC检查通过，则匹配AFL条目中的DLC配置值存储在目标RXMB或FIFO缓冲区中。

如果接收到的DLC值大于匹配AFL条目中配置的DLC值，则CAN总线上接收到的附加数据字节不会存储在目标RXMB或FIFO缓冲区中。这些额外的数据字节作为0x00存储在目标RXMB或FIFO缓冲区中。

如果启用DLC替换并且匹配AFL条目的DLC值为0x0，则接收到的DLC值存储在目标RXMB或FIFO缓冲区中。

如果DLC替换（CFDGCFG.DRE位）被禁用并且DLC检查通过，则接收到的DLC值在CAN总线存储在目标RXMB或FIFO缓冲区中。

如果接收到的DLC值大于匹配AFL条目中配置的DLC值，则从CAN总线接收的附加数据字节也将存储在目标RXMB或FIFO缓冲区中。

如果接收到的消息的DLC值小于匹配的AFL条目中配置的DLC值，则DLC检查失败。在这种情况下，接收到的报文被拒绝并且不存储在任何RXMB或FIFO缓冲区中。

此外，DLC检查失败由全局错误标志寄存器中的DLC错误标志标记。如果已配置，还会生成错误中断。如果DLC检查失败，则DLC替换配置没有影响。

如果消息已通过接受过滤和DLC过滤，则将其存储在单个接收消息缓冲区和/或为接收或网关功能配置的FIFO缓冲区中。

该消息存储目标信息也在同一个AFL条目中定义。不要在未配置的AFL条目上设置目标。

每个接受的接收消息最多可以存储到8个不同的目标目的地（单个接收消息缓冲区和/或FIFO缓冲区）。

不允许对超过8个目标目的地进行编程。如果对更多目的地进行了编程，则内部计时可能会导致竞争条件，从而阻止将接收到的消息存储在消息RAM中。正确配置目标目的地的数量是应用程序的责任。

当接收到的消息包含的数据有效负载字节多于可能存储在目标目的地（CFDRFCCn.RMPLS、CFDRFCCn.RFPLS或CFDCFCCn.CFPLS）中时，会采用额外的保护机制。

如果CFDGCFG.CMPOC=0，则消息被完全拒绝并存储在目标目的地中。什么时候CFDGCFG.CMPOC=0并且RX或CommonFIFOfull包括接收到的消息包含更多的数据有效负载字节

than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCn.RFPLS or CFDCFCCn.CFPLS), the corresponding CFDFMSTS.RFxMLT or CFDFMSTS.CFxMLT bit is not set to 1, respectively.

When CFDGCFG.CMPOC = 1, the received data bytes greater than CFDRMNB.RMPLS is rejected. When CFDGCFG.CMPOC = 1 and RX or Common FIFO full including the received message contains more data payload bytes than possible to store in the target destination (CFDRMNB.RMPLS, CFDRFCCn.RFPLS or CFDCFCCn.CFPLS), the corresponding CFDFMSTS.RFxMLT or CFDFMSTS.CFxMLT bit is set to 1, respectively.

Depending on the CFDGCFG.DRE bit, the original received DLC or the DLC value configured at the AFL entry is stored.

Regardless of the CFDGCFG.CMPOC bit setting, CFDGERFL.CMPOF is set to 1 if a payload overflow condition is detected.

The DLC filtering is performed before the payload overflow function. So for one reception frame, only one flag can be set at the same time with CFDGERFL.DEF or CFDGERFL.CMPOF*1.

Note 1. This bit is not available in the classical CAN function.

32.5.2 Allocation of AFL Entries to each CAN Channel

The number of AFL entries per channel can be configured using the dedicated field in the related Global Acceptance Filter Configuration Registers (see Figure 32.24).

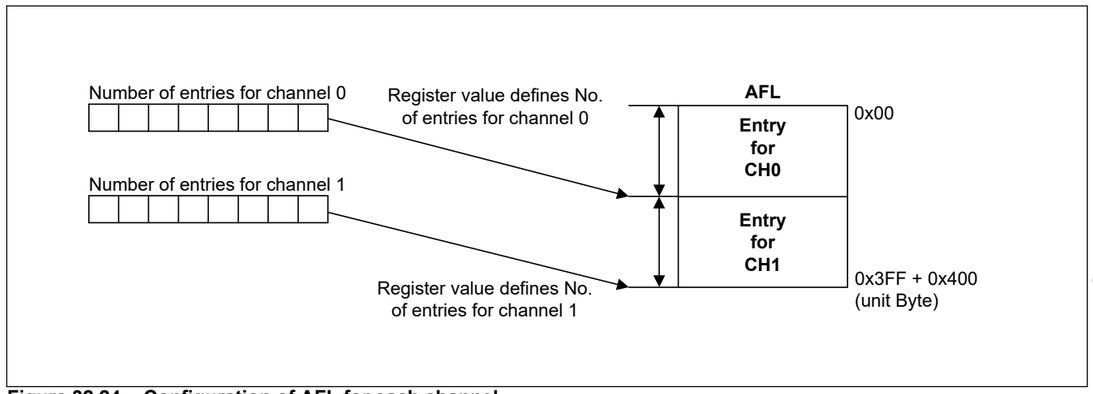


Figure 32.24 Configuration of AFL for each channel

The minimum number of entries for one channel is 0 (no entries defined for the channel) and the maximum number of entries for one channel is 64. The total number of entries for all channels should not exceed the maximum limit of (n + 1) × 64.

All entries are unique for a channel and overlapping or sharing of entries is not supported. Correct configuration of the AFL is the responsibility of the application.

The CAN-FD module does not flag errors related to the configuration of the AFL.

32.5.3 AFL Entry Description

Each AFL entry consists of 16 bytes. The fields in all entries are identical.

Each entry contains the following information for acceptance filtering and DLC filtering:

- Identifier (11 bits for Standard Frame format, 29 bits for Extended Frame format):
  Acceptance filter unit checks the identifier field of the received message against the identifier field of each AFL entry (full 29 bits masking of identifier bits is possible, see information that follows).
- IDE bit:
  Acceptance filter unit checks the IDE bit of the received message against this bit and selects the relevant part of the identifier field for acceptance filtering (masking of IDE bit is possible, see the information that follows).
- RTR bit:

比可能存储在目标目的地（CFRDRMNB.RMPLS、CFDRFCCn.RFPLS或CFDCFCCn.CFPLS）中，相应的CFDFMSTS.RFxMLT或CFDFMSTS.CFxMLT位分别不设置为1。

当CFDGCFG.CMPOC=1时，大于CFDRMNB.RMPLS的接收数据字节被拒绝。什么时候CFDGCFG.CMPOC=1并且RX或CommonFIFOfull（包括接收到的消息）包含的数据有效负载字节数超过了可能存储在目标目的地（CFDRMBG.RMPLS、CFDRFCCn.RFPLS或CFDCFCCn.CFPLS）、相应的CFDFMSTS.RFxMLT或CFDFMSTS中的数据。CFxMLT位分别设置为1。

根据CFDGCFG.DRE位，存储原始接收的DLC或在AFL条目中配置的DLC值。

无论CFDGCFG.CMPOC位设置如何，如果检测到有效负载溢出条件，CFDGERFL.CMPOF将设置为1。

DLC过滤在有效载荷溢出功能之前执行。因此对于一个接收帧，只能使用CFDGERFL.DEF或CFDGERFL.CMPOF*1同时设置一个标志。

注1.该位在经典CAN功能中不可用。

32.5.2 将AFL条目分配到每个CAN通道

可以使用相关全局接受过滤器中的专用字段配置每个通道的AFL条目数
配置寄存器（见图32.24）。

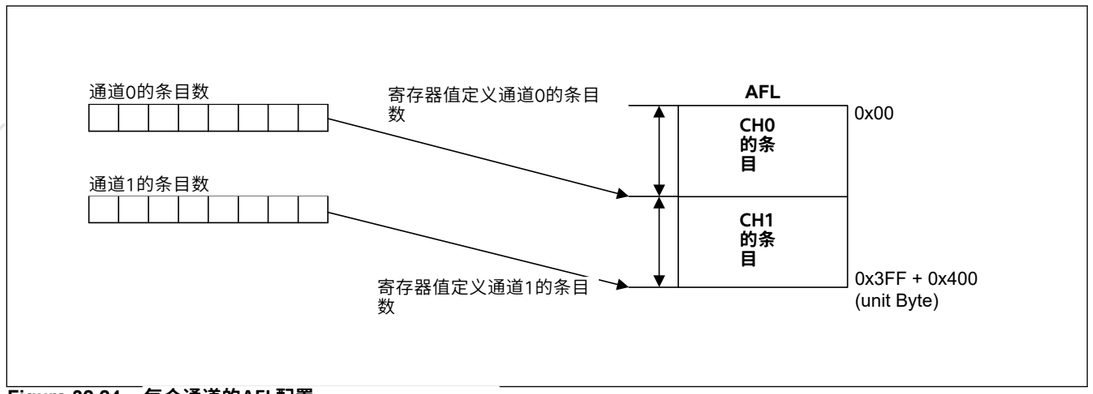


Figure 32.24 每个通道的AFL配置

一个通道的最小条目数为0（没有为通道定义条目），一个通道的最大条目数为64。所有通道的条目总数不应超过(n+1)的最大限制×64。

频道的所有条目都是唯一的，不支持条目的重叠或共享。正确配置AFL是应用程序的责任。

CAN-FD模块不会标记与AFL配置相关的错误。

32.5.3 AFL条目说明

每个AFL条目由16个字节组成。所有条目中的字段都是相同的。

每个条目都包含以下接受过滤和DLC过滤的信息：

- 标识符（标准帧格式为11位，扩展帧格式为29位）：
  接受过滤器单元根据每个AFL条目的标识符字段检查接收到的消息的标识符字段（标识符位的全29位掩码是可能的，请参阅以下信息）。
- IDE bit:
  接受过滤单元对照该位检查接收到的消息的IDE位，并选择标识符字段的相关部分进行接受过滤（可以屏蔽IDE位，参见以下信息）。
- RTR bit:

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Acceptance filter unit only accepts data frames (RTR = 0) or remote frames (RTR = 1) according to the setting of this bit (masking of RTR bit is possible, see the information that follows).

- Loopback Configuration bit:
  This bit can enable or disable the AFL entry depending on the Loopback Configuration or Mirror mode condition.

- Mask for Identifier bits (29 bits):
  Each bit in the identifier mask can mask the corresponding identifier bit in the AFL entry during acceptance filtering, see Figure 32.25.

- Mask for IDE bit:
  If this Mask bit masks the IDE bit of the AFL entry in both Standard Identifier and Extended Identifier format, messages can be accepted by this AFL entry. The identifier of the received message is compared against the Standard Identifier part of the AFL entry for Standard Identifier format messages and against the Extended Identifier part of the AFL entry for Extended Identifier format messages.

- Mask for RTR bit:
  If this Mask bit masks the RTR bit of the AFL entry in both frame formats, data frame and remote frame formats are accepted by this AFL entry.

- Pointer information (16 bits):
  This 16-bit pointer is attached to a received message accepted by the related AFL entry. The pointer is added during message storage in the message buffer area and can be used by application as support function. The pointer information can be used for example to support PDU identifier allocation for the received message in AUTOSAR systems.

- Information label (2 bits):
  This 2-bit label is attached to a received message accepted by the related AFL entry. The label is added during message storage in the message buffer area and can be used by application as support function.

- DLC value for automatic DLC filtering:
  If the DLC value of the received message is equal or higher than the configured DLC value, the DLC check is passed.

If the DLC value in this AFL entry is configured to 0, DLC filtering is effectively disabled for this entry (all accepted messages pass DLC filtering).

Each AFL entry contains the following information for the handling of received messages:

- Message buffer number of one single reception message buffer as target for received message storage
- Single reception message buffer enable bit to configure the single reception message buffer number to be valid or invalid, as target for received message storage
- FIFO direction pointer - each bit of the FIFO direction pointer configures a dedicated FIFO as possible target for a received message

Note: A message received on channel A can be routed to Common FIFO buffer of another channel. If this Common FIFO buffer is configured in Gateway mode, then the message stored in this Common FIFO Buffer is transmitted on that channel because Common FIFO buffer is associated with channel.

There is no hardware protection against such storage of message. Therefore, the FIFO direction pointer must be configured carefully.

接受过滤器单元仅根据该位的设置接受数据帧（RTR=0）或远程帧（RTR=1）（RTR位的屏蔽是可能的，参见下面的信息）。

- Loopback Configuration bit:
  该位可以根据环回配置或镜像模式条件启用或禁用AFL条目。

●标识符位掩码（29位）：
标识符掩码中的每个位都可以在接受过滤期间屏蔽AFL条目中的相应标识符位，请参见图32.25。

●IDE位掩码：
如果此掩码位以标准标识符和扩展标识符格式屏蔽AFL条目的IDE位，则此AFL条目可以接受消息。接收消息的标识符与标准标识符格式消息的AFL条目的标准标识符部分和扩展标识符部分进行比较

扩展标识符格式消息的AFL条目。

●RTR位掩码：
如果此掩码位在两种帧格式中屏蔽AFL条目的RTR位，则此AFL条目接受数据帧和远程帧格式。

●指针信息（16位）：
这个16位指针附加到相关AFL条目接受的接收消息。该指针是在消息存储过程中在消息缓冲区中添加的，可供应用程序用作支持函数。例如，指针信息可用于支持AUTOSAR系统中接收到的消息的PDU标识符分配。

●信息标签（2位）：
这个2位标签附加到相关AFL条目接受的接收消息。该标签是在消息存储过程中在消息缓冲区中添加的，可供应用程序用作支持功能。

●自动DLC过滤的DLC值：
如果接收到的消息的DLC值等于或大于配置的DLC值，则DLC检查通过。

如果此AFL条目中的DLC值配置为0，则有效禁用此条目的DLC过滤（所有接受的消息都通过DLC过滤）。

每个AFL条目都包含以下用于处理接收到的消息的信息：

●作为接收消息存储目标的单个接收消息缓冲区的消息缓冲区号

●单次接收报文缓冲区使能位，用于配置单次接收报文缓冲区号有效或无效，作为接收报文存储的目标

●FIFO方向指针FIFO方向指针的每一位配置一个专用的FIFO作为接收消息的可能目标

Note: 在通道A上接收到的消息可以路由到另一个通道的CommonFIFO缓冲区。如果此CommonFIFO缓冲区配置为网关模式，则存储在此CommonFIFO缓冲区中的消息将在该通道上传输，因为CommonFIFO缓冲区与通道相关联。

没有针对此类消息存储的硬件保护。因此，必须仔细配置FIFO方向指针。

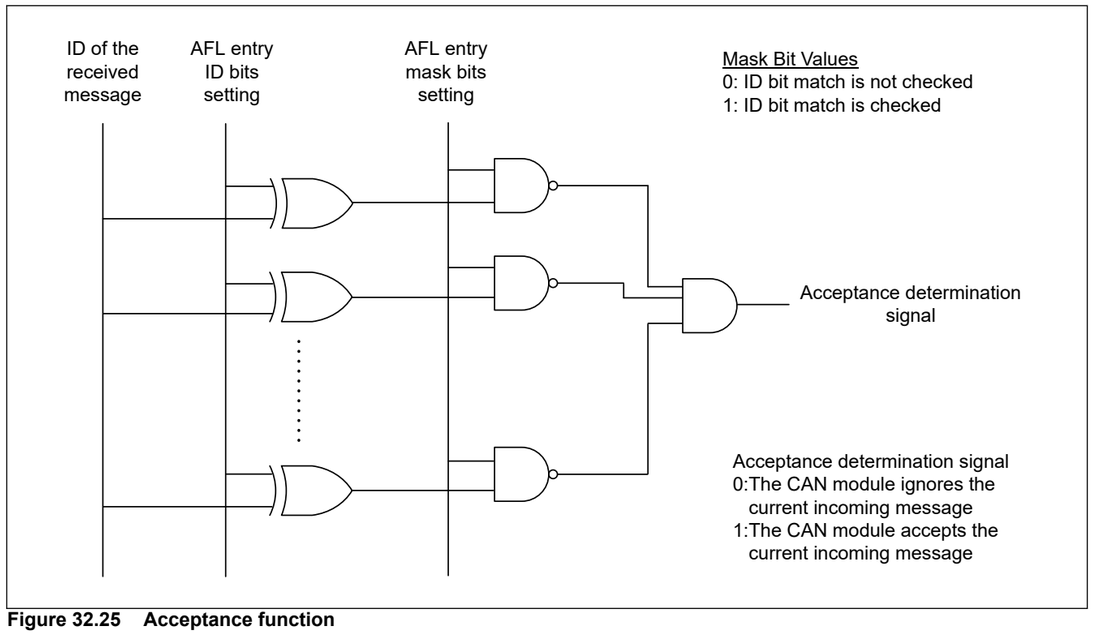

Figure 32.25 Acceptance function

32.5.4 Entering Entries in the AFL

Application software can enter one full entry into the AFL using the following registers:

- Global AFL ID Entry Register: Part 1 of the AFL entry
- Global AFL Mask Entry Register: Part 2 of the AFL entry
- Global AFL Pointer 0 Entry Register: Part 3 of the AFL entry
- Global AFL Pointer 1 Entry Register: Part 4 of the AFL entry.

16 sets of these registers form a group of AFL entries. Each group can be accessed through a page mechanism. For the CAN-FD module, 2-channel version, 8 of these pages exist to allow access to the whole AFL range. The AFL should only be configured in CH_RESET or CH_HALT mode. Pages are linked to the AFL entries in the following way:

Page 0	Entry 0 — 15
Page 1	Entry 16 — 31
Page 2	Entry 32 — 47
Page 3	Entry 48 — 63
Page 4	Entry 64 — 79
Page 5	Entry 80 — 95
Page 6	Entry 96 — 111
Page 7	Entry 112 — 127

The selection of the AFL access page is done using the Global Acceptance Filter List Entry Control Register (CFDGAFLECTR) (Figure 32.26). This register has the following fields:

- 7 bits to select the AFL page number
- 1 bit to enable or disable the AFL data access to prevent unwanted write access to the AFL.

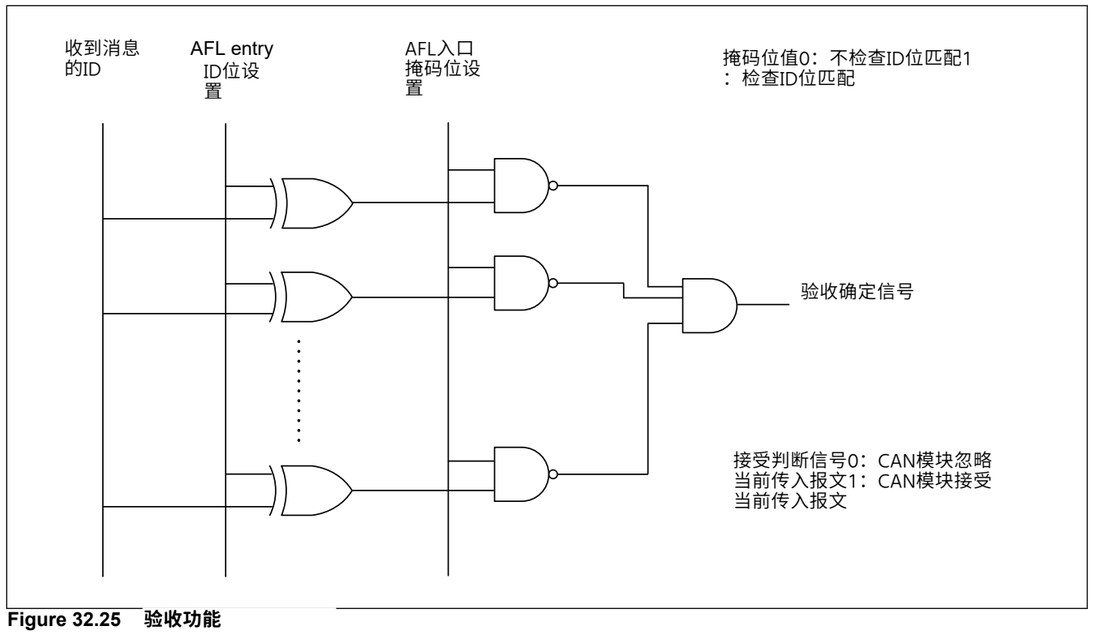

Figure 32.25 验收功能

32.5.4 在AFL中输入条目

应用软件可以使用以下寄存器将一个完整条目输入AFL：

●全球AFLID条目寄存器：AFL条目的第1部分

●全局AFL掩码条目寄存器：AFL条目的第2部分

●全局AFL指针0条目寄存器：AFL条目的第3部分

●全局AFL指针1条目寄存器：AFL条目的第4部分。

16组这些寄存器形成一组AFL条目。每个组都可以通过页面机制访问。对于CAN-FD模块，2通道版本，其中8个页面允许访问整个AFL范围。AFL只能在CH_RESET或CH_HALT模式下配置。页面通过以下方式链接到AFL条目：

Page 0	Entry 0 — 15
Page 1	Entry 16 — 31
Page 2	Entry 32 — 47
Page 3	Entry 48 — 63
Page 4	Entry 64 — 79
Page 5	Entry 80 — 95
Page 6	Entry 96 — 111
Page 7	Entry 112 — 127

AFL访问页面的选择是使用全局接受过滤器列表条目控制寄存器(CFDGAFLECTR)完成的（图32.26）。该寄存器具有以下字段：

●7位选择AFL页码

●1位启用或禁用AFL数据访问，以防止对AFL的不必要的写访问。

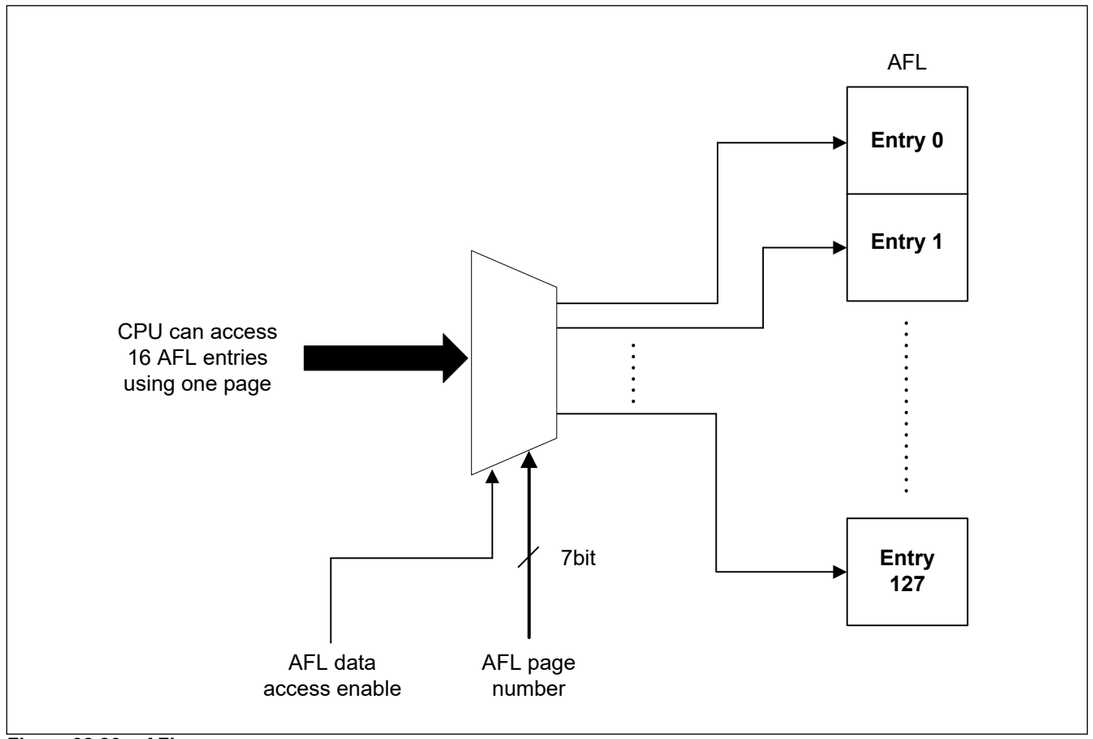

Figure 32.26 AFL page access

Application software should not write numbers higher than 0x5F for the AFL page number.

Follow the configuration shown in Figure 32.27 to program the AFL.

After entering all entries in Configuration mode, locking of the AFL access should be performed to protect unwanted write access to the AFL.

Write protection is active during all Global modes (GL_RESET, GL_HALT, and GL_OPERATION) if the lock bit is set.

Read access to AFL is still possible during all Global modes even when AFL data access is disabled (consistency check of AFL contents is possible during run time).

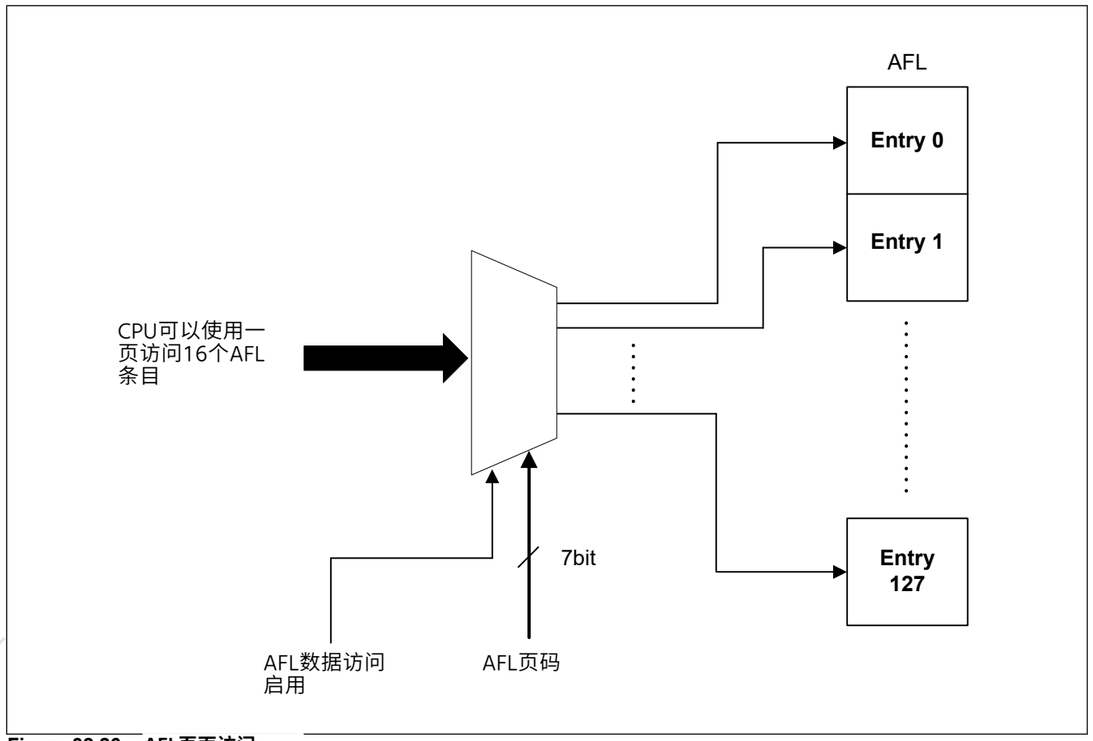

Figure 32.26 AFL页面访问

应用软件不应为AFL页号写入高于0x5F的数字。

按照图32.27所示的配置对AFL进行编程。

在配置模式下输入所有条目后，应执行AFL访问锁定以保护对AFL的不需要的写访问。

如果设置了锁定位，则写保护在所有全局模式（GL_RESET、GL_HALT和GL_OPERATION）期间都处于活动状态。

即使禁用AFL数据访问（一致性检查
AFL内容在运行时是可能的）。

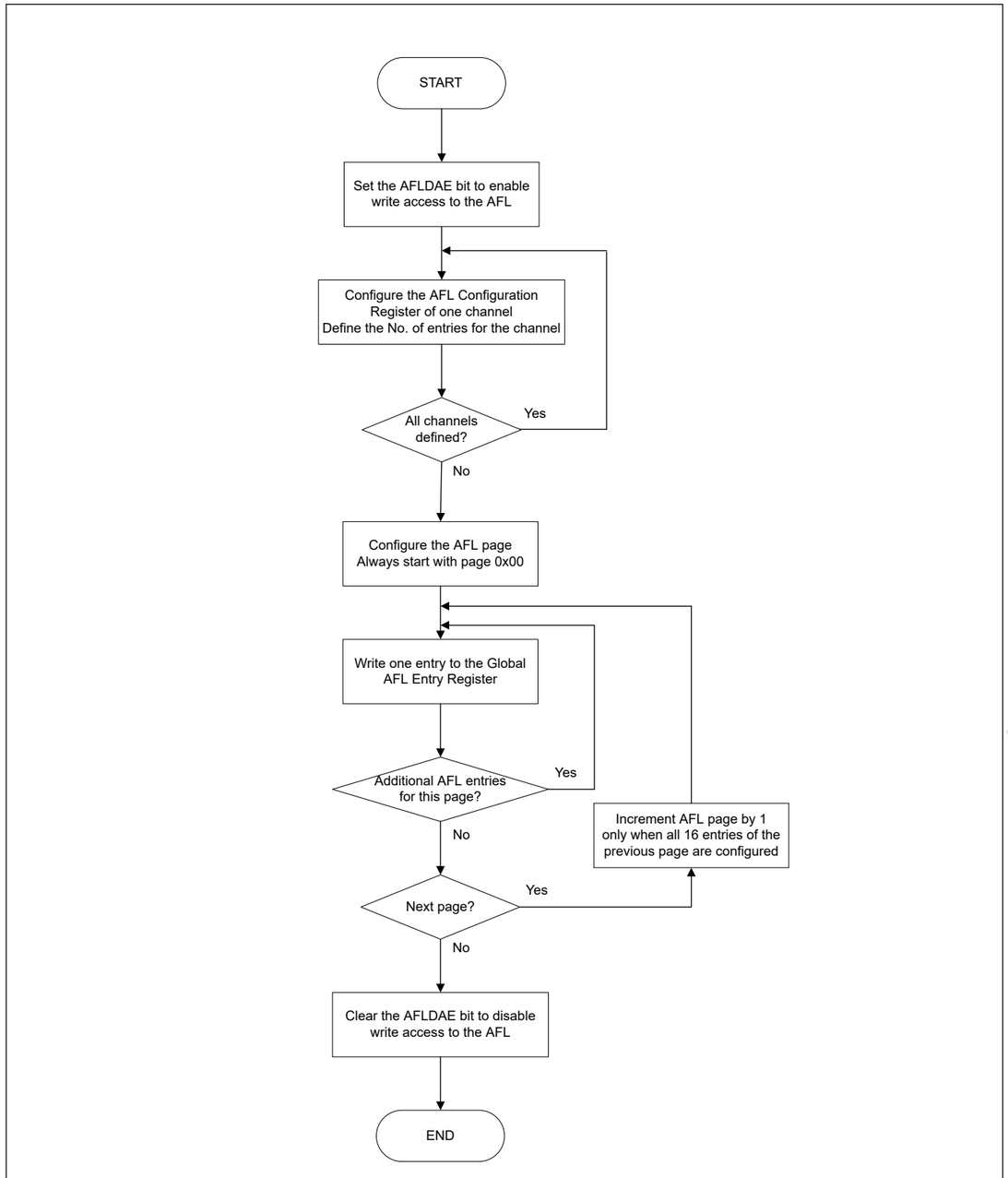

Figure 32.27 AFL configuration flow

32.5.5 Loopback Modes

If the Loopback Configuration bit is set, the AFL entry is only valid in Loopback test mode (Self-test mode 0 or Self-test mode 1) or in mirror mode when receiving messages that were transmitted by the respective CAN channel itself.

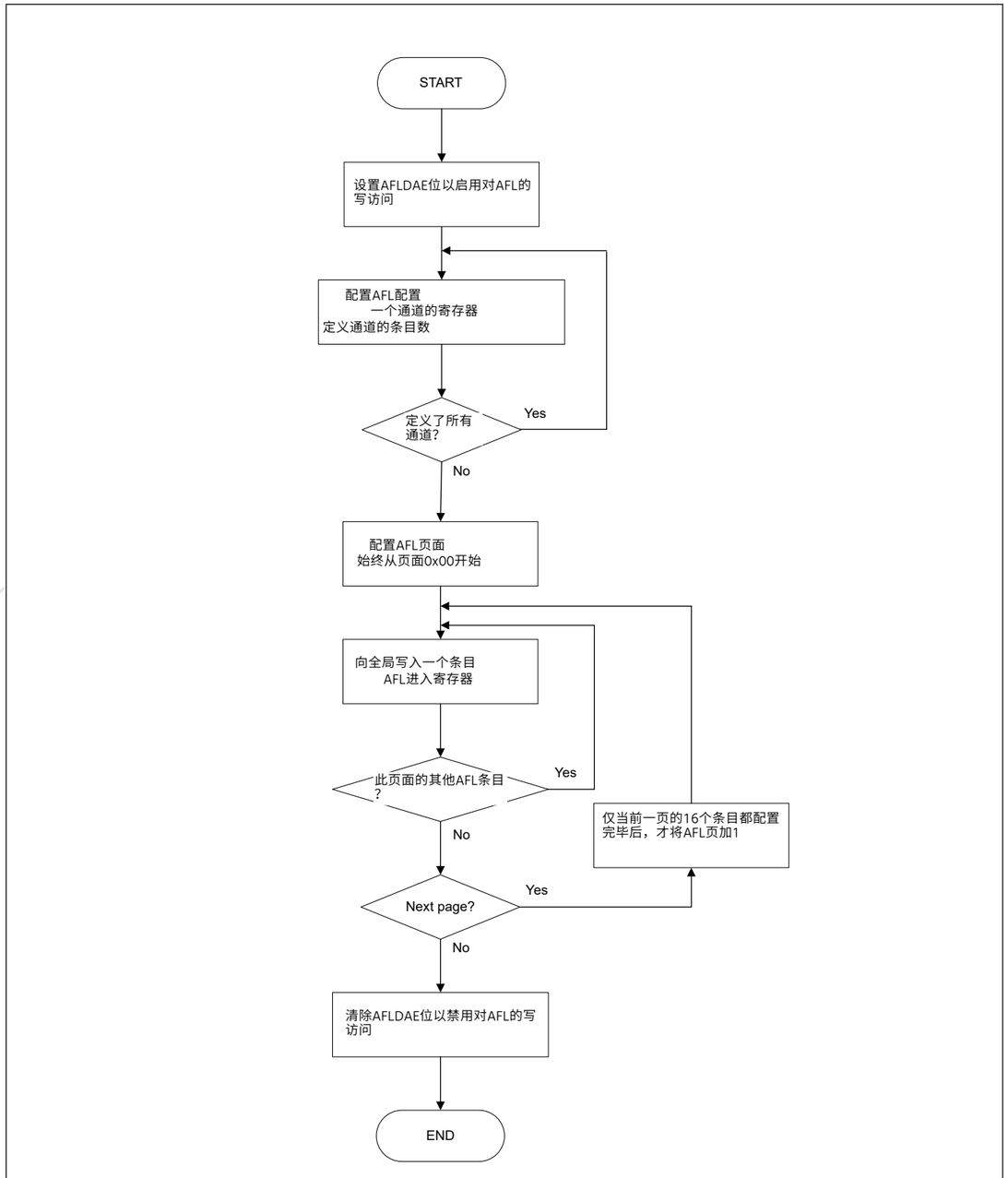

Figure 32.27 AFL配置流程

32.5.5 Loopback Modes

如果设置了环回配置位，则AFL条目仅在环回测试模式（自测模式0或自测模式1）或在接收由相应CAN通道本身发送的消息时的镜像模式下有效。

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The AFL entry is not valid for received messages in loopback mode transmitted by other CAN nodes on the bus. The expression valid or invalid for the related entry means that this AFL entry is or is not compared against the received message ID respectively.

If the Loopback Configuration bit is 0, the AFL entry is only valid for:

- Received messages transmitted by other CAN nodes on the bus in normal (non-loopback mode) and mirror modes
- Received messages transmitted by other CAN nodes or the CAN channel itself in Loopback test mode.

The mirror mode can be enabled with the CFDGCFG.MME bit in the Global Configuration Register. If CFDGCFG.MME bit is set, then a successfully transmitted message can be stored back in an RX message buffer or FIFO buffer if a matching entry is configured in the AFL for that channel.

The Loopback Configuration bit in the matching AFL entry must be set to store this frame.

If Mirror mode and Loopback test mode are configured at the same time, the Loopback test mode behavior applies.

Table 32.17 shows the behavior of the acceptance filter unit depending on the setting of the related input signals.

Table 32.17 Behavior of acceptance filter based on the loopback configuration setting in AFL entry

Mirror Mode Enable (MME Configuration bit)	Loopback in test mode (Self-test mode 0 or Self-test mode 1)	Channel mode	Loopback Configuration bit in AFL entry	AFL entry
0	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Invalid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid
1	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Valid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid

Note: The expression valid or invalid for the related entry means that this AFL entry is or is not compared against the received message ID, respectively.

32.5.6 IDE Masking

When the GAFLIDEM bit is 0 in an AFL entry, the IDE bit configured in the AFL entry is not used for ID matching. In this case, the use of ID[10:0] or ID[28:0] matching is based on the received IDE bit.

Consider the following example:

- The ID and Mask fields of an AFL entry x is configured as follows:
  - CFDGAFLID [x] = 0xC0553A20 → IDE = 1, RTR = 1, LLB = 0, ID[10:0] = 0x220 / ID[28:0] = 0x00553A20
  - CFDGAFLMn = 0x0000FFFF → IDEM = 0. RTRM = 0, IDM[10:0] = 0x7FF / IDM[28:0] = 0x0000FFFF
- The comparison result for the four different received IDs with AFL entry x is described as follows:
  - If a frame with IDE = 0 and ID = 0x220 is received, this is considered as a match
  - If a frame with IDE = 0 and ID = 0x320 is received, this is not a match

AFL条目对于总线上其他CAN节点发送的环回模式下接收到的消息无效。相关条目的表达式有效或无效表示该AFL条目分别与接收到的消息ID进行比较或不进行比较。

如果环回配置位为0，则AFL条目仅对以下情况有效：

●接收到总线上其他CAN节点在正常（非环回模式）和镜像模式下发送的报文

●Loopback测试模式下接收到其他CAN节点或CAN通道本身发送的报文。

可以使用全局配置寄存器中的CFDGCFG.MME位启用镜像模式。如果设置了CFDGCFG.MME位，则如果在AFL中为该通道配置了匹配条目，则成功传输的消息可以存储回RX消息缓冲区或FIFO缓冲区。

必须设置匹配AFL条目中的环回配置位以存储该帧。

如果同时配置了镜像模式和环回测试模式，则应用环回测试模式行为。

表32.17显示了接收滤波器单元的行为，具体取决于相关输入信号的设置。

Table 32.17 基于AFL条目中环回配置设置的验收过滤器的行为

镜像模式启用（MME配置位）	测试模式环回（自检模式0或自检模式1）	频道模式	AFL条目中的环回配置位	AFL entry
0	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Invalid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid
1	0	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Invalid
			1	Valid
	1	Receiver	0	Valid
			1	Invalid
		Transmitter	0	Valid
			1	Valid

Note: 相关条目的表达式有效或无效表示此AFL条目是否与接收到的消息进行比较身份证，分别。

32.5.6 IDE屏蔽

当AFL条目中的GAFLIDEM位为0时，AFL条目中配置的IDE位不用于ID匹配。在这种情况下，ID[10:0]或ID[28:0]匹配的使用基于接收到的IDE位。

考虑以下示例：

●AFL表项x的ID和Mask字段配置如下：

- CFDGAFLID [x] = 0xC0553A20 → IDE = 1, RTR = 1, LLB = 0, ID[10:0] = 0x220 / ID[28:0] = 0x00553A20
- CFDGAFLMn = 0x0000FFFF → IDEM = 0. RTRM = 0, IDM[10:0] = 0x7FF / IDM[28:0] = 0x0000FFFF

●四种不同的接收ID与AFL条目x的比较结果描述如下：

如果接收到IDE=0且ID=0x220的帧，则视为匹配

如果接收到IDE=0且ID=0x320的帧，则不匹配

- If a frame with IDE = 1 and ID = 0x1FFF3A20 is received, this is considered as a match
- If a frame with IDE = 1 and ID = 0x08803220 is received, this is not a match.

32.6 FIFO Buffers and Normal Message Buffer Configuration

This section describes the process for configuring the number of RX message buffers, the FIFO buffers, and the flat TX message buffers in the CAN-FD module. The message buffers are mapped as shown in Figure 32.28.

The RX message buffers can be accessed with the RX Message Buffer Registers.

The RX FIFO buffers and the common FIFO buffers configured in RX mode, TX mode, or GW mode can only be accessed with the FIFO Access Registers.

If the common FIFO is configured in TX mode, you can only write data into the FIFO buffer using the FIFO Access registers.

If the common FIFO is configured in GW mode or RX mode, you can only read data from the FIFO Access Registers.

The TX message buffers can be accessed with the TX Message Buffer Registers.

If unused message buffer locations are read, the message buffer locations are read as unknown values.

如果接收到IDE=1且ID=0x1FFF3A20的帧，则视为匹配

如果接收到IDE=1且ID=0x08803220的帧，则不匹配。

32.6 FIFO缓冲区和正常消息缓冲区配置

本节介绍在CAN-FD模块中配置RX报文缓冲区、FIFO缓冲区和平面TX报文缓冲区数量的过程。消息缓冲区的映射如图32.28所示。

RX报文缓冲区可以通过RX报文缓冲区寄存器访问。

RXFIFO缓冲区和配置为RX模式、TX模式或GW模式的通用FIFO缓冲区只能通过FIFO访问寄存器进行访问。

如果普通FIFO配置为TX模式，则只能使用FIFO访问寄存器将数据写入FIFO缓冲区。

如果普通FIFO配置为GW模式或RX模式，则只能从FIFO访问寄存器中读取数据。

TX报文缓冲区可以通过TX报文缓冲区寄存器访问。

如果读取未使用的消息缓冲区位置，则将消息缓冲区位置作为未知值读取。

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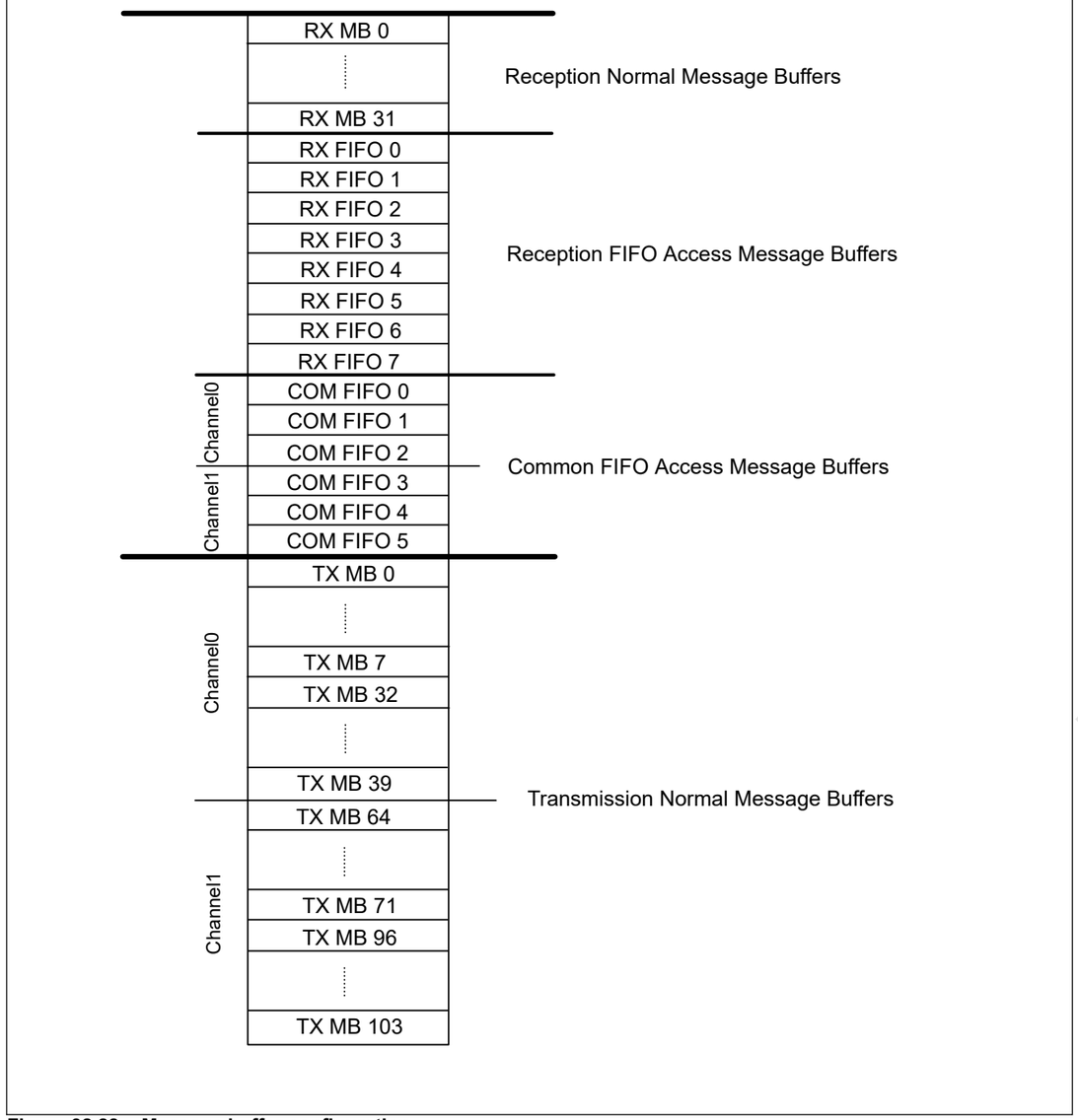

Figure 32.28 Message buffer configuration

32.6.1 Normal RX Message Buffers

In CAN-FD module, the frames received by various channels can be stored in normal RX message buffers based on the configuration of the AFL entries.

Additionally, the number of normal RX message buffers required in the system can be chosen up to a fixed maximum limit.

32.6.1.1 Normal RX Message Buffer Configuration

In CAN-FD module, the number of normal RX message buffers can be configured by writing to the RX Message Buffer Number Register.

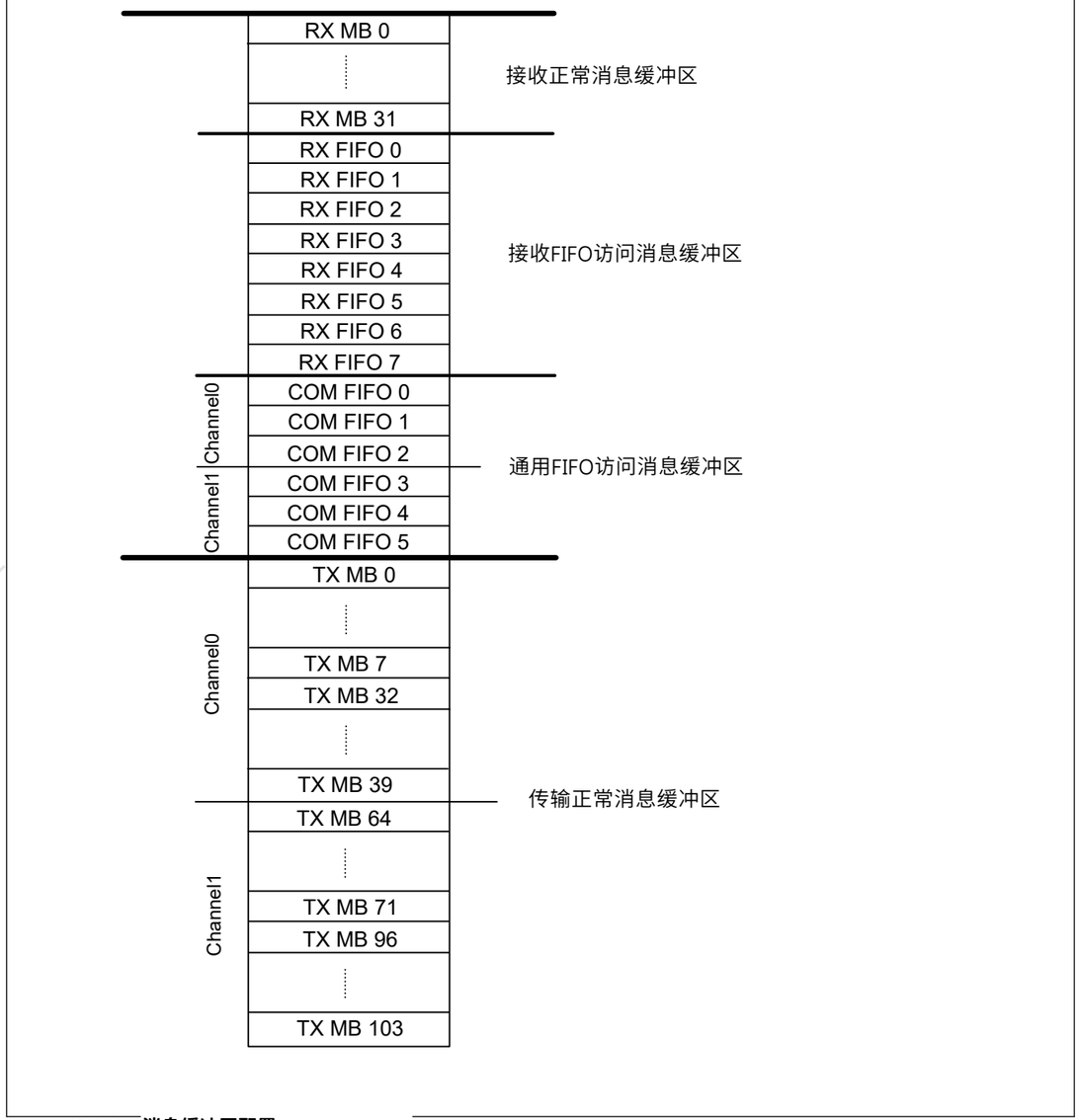

Figure 32.28 消息缓冲区配置

32.6.1 正常RX消息缓冲区

在CAN-FD模块中，各个通道接收到的帧可以根据AFL条目的配置存储在正常的RX消息缓冲区中。

此外，系统所需的正常RX消息缓冲区的数量可以选择为固定的最大限制。

32.6.1.1 正常RX报文缓冲区配置

在CAN-FD模块中，可以通过写入RX消息缓冲区来配置正常RX消息缓冲区的数量
号码寄存器。

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The limiting values for the configuration of number of message buffers are:

- Minimum value = 0x00 (no normal RX MB)
- Maximum value = (16 × No. of CAN channels) = 16 × 2 = 32
  = 0x20 (32 flat RX MBs for 2 channels)

Do not use values outside these limits.

The AFL entries for routing the received messages to normal RX message buffers must be configured to match the requirements of the system.

The AFL entries must also be configured properly, and an AFL entry for normal RX message buffers should not exceed the number of message buffers configured in the RX Message Buffer Number Register.

Note: There is no internal check procedure provided in CAN-FD module against wrong configuration of the AFL.

The data field size of the RX message buffer can be configured with the CFDRMNB.RMPLS bit. The default size is 8 bytes and the maximum data payload size is 64 bytes.

When the receiving frame exceeds the data field size, then the acceptance depends on the configuration of CFDGCFG.CMPOC (message rejecting or data payload cut).

Note: RMPLS and CMPOC bit is not available in the classical CAN function, so, these feature is not valid for classical CAN.

32.6.2 FIFO Buffers

The CAN-FD module provides a fixed number of FIFO buffers to support storage of frames for reception, transmission and gateway functions for various CAN channels.

The number of reception-only FIFO buffers is fixed to 8. However, 3 common FIFO buffers per channel can be configured to store messages for transmission, reception, or gateway function.

These FIFO buffers can be enabled or disabled, and the following parameters can be configured to match the system requirements:

- Size
- Interrupt structure
- Message lost mechanism
- Message overwrite mechanism of the FIFO buffers
- Location of the TX FIFO or GW FIFO.

When the receiving frame exceeds the data field size, the acceptance depends on the configuration of the CFDGCFG.CMPOC bit (message rejecting or data payload cut).

32.6.2.1 FIFO Buffers Configuration

In CAN-FD module, the FIFO buffers can be configured to match the system requirements.

The total number of FIFO buffers = 8 RX FIFO buffers + 6 common FIFO buffers = 14 FIFO buffers for 2 channels and message overwrite mechanism.

消息缓冲区数量配置的限制值为：

●最小值=0x00（非正常RXMB）

●最大值=（16×CAN通道数）=16×2=32=0x20（2个通道
的32个扁平RXMB）

不要使用超出这些限制的值。

用于将接收到的消息路由到正常RX消息缓冲区的AFL条目必须配置为匹配系统的要求。

AFL条目也必须正确配置，正常RX消息缓冲区的AFL条目不应超过RX消息缓冲区编号寄存器中配置的消息缓冲区数。

Note: CAN-FD模块中没有针对AFL的错误配置提供内部检查程序。

RX消息缓冲区的数据字段大小可以通过CFDRMNB.RMPLS位进行配置。默认大小为8字节，最大数据负载大小为64字节。

当接收帧超过数据字段大小时，则接受取决于配置
CFDGCFG.CMPOC（消息拒绝或数据有效负载切断）。

Note: RMPLS和CMPOC位在经典CAN功能中不可用，因此，这些功能对经典CAN功能无效
CAN.

32.6.2 FIFO Buffers

CAN-FD模块提供固定数量的FIFO缓冲区，以支持存储用于各种CAN通道的接收、传输和网关功能的帧。

仅接收FIFO缓冲区的数量固定为8。但是，每个通道可以配置3个通用FIFO缓冲区来存储用于传输、接收或网关功能的消息。

可以启用或禁用这些FIFO缓冲区，并且可以配置以下参数以匹配系统要求：

- Size

●中断结构

●消息丢失机制

●FIFO缓冲区的消息覆盖机制

●TXFIFO或GWFIFO的位置 。

当接收帧超过数据字段大小时，接受取决于配置的
CFDGCFG.CMPOC位（消息拒绝或数据有效负载切断）。

32.6.2.1 FIFO缓冲器配置

在CAN-FD模块中，可以配置FIFO缓冲区以匹配系统要求。

FIFO缓冲区的总数=8个RXFIFO缓冲区+6个通用FIFO缓冲区=2个通道和消息覆盖机制的14个FIFO缓冲区。

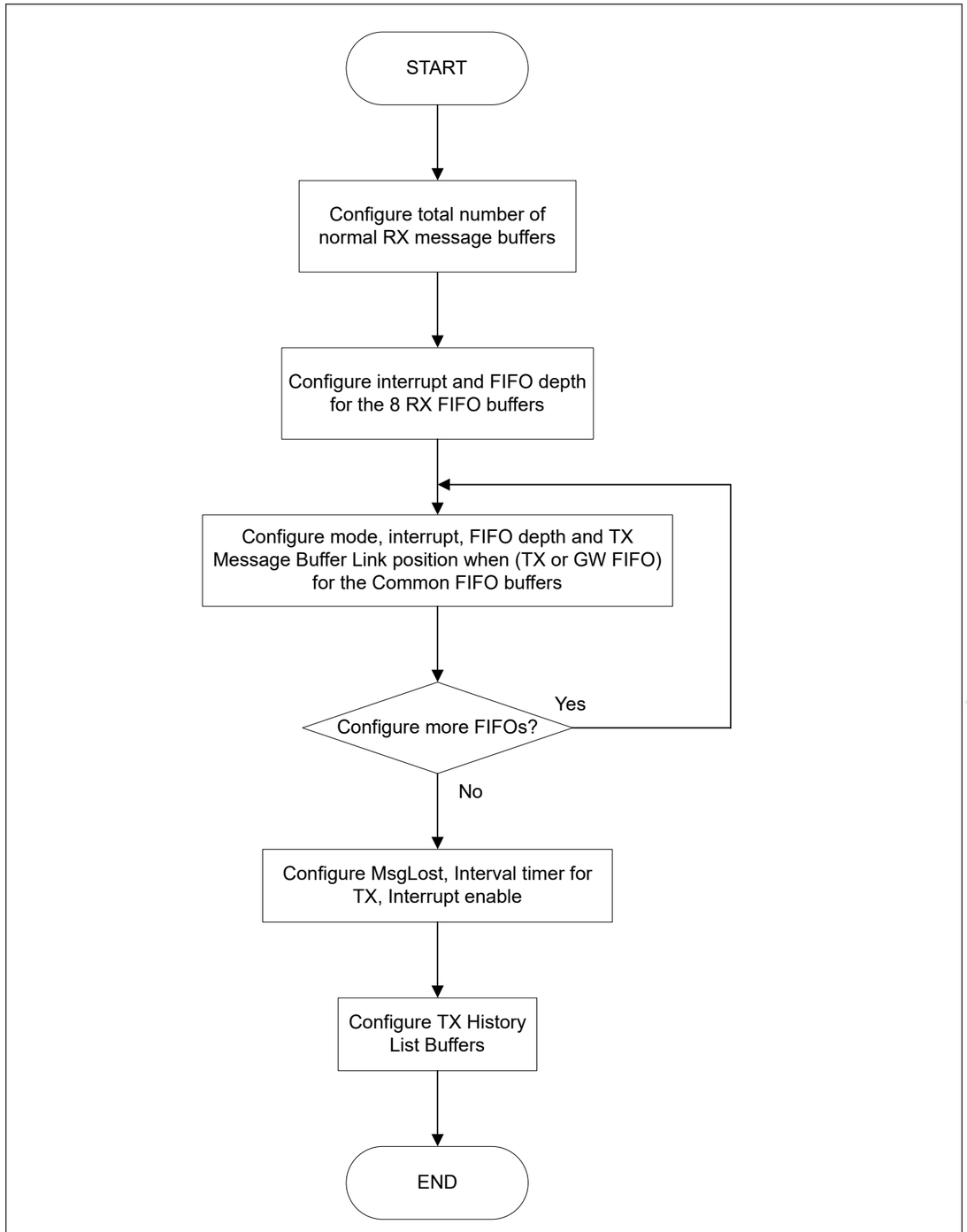

Figure 32.29 FIFO buffer configuration flow in CAN-FD module

As shown in Figure 32.29, the various FIFO buffers can be configured by writing to the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

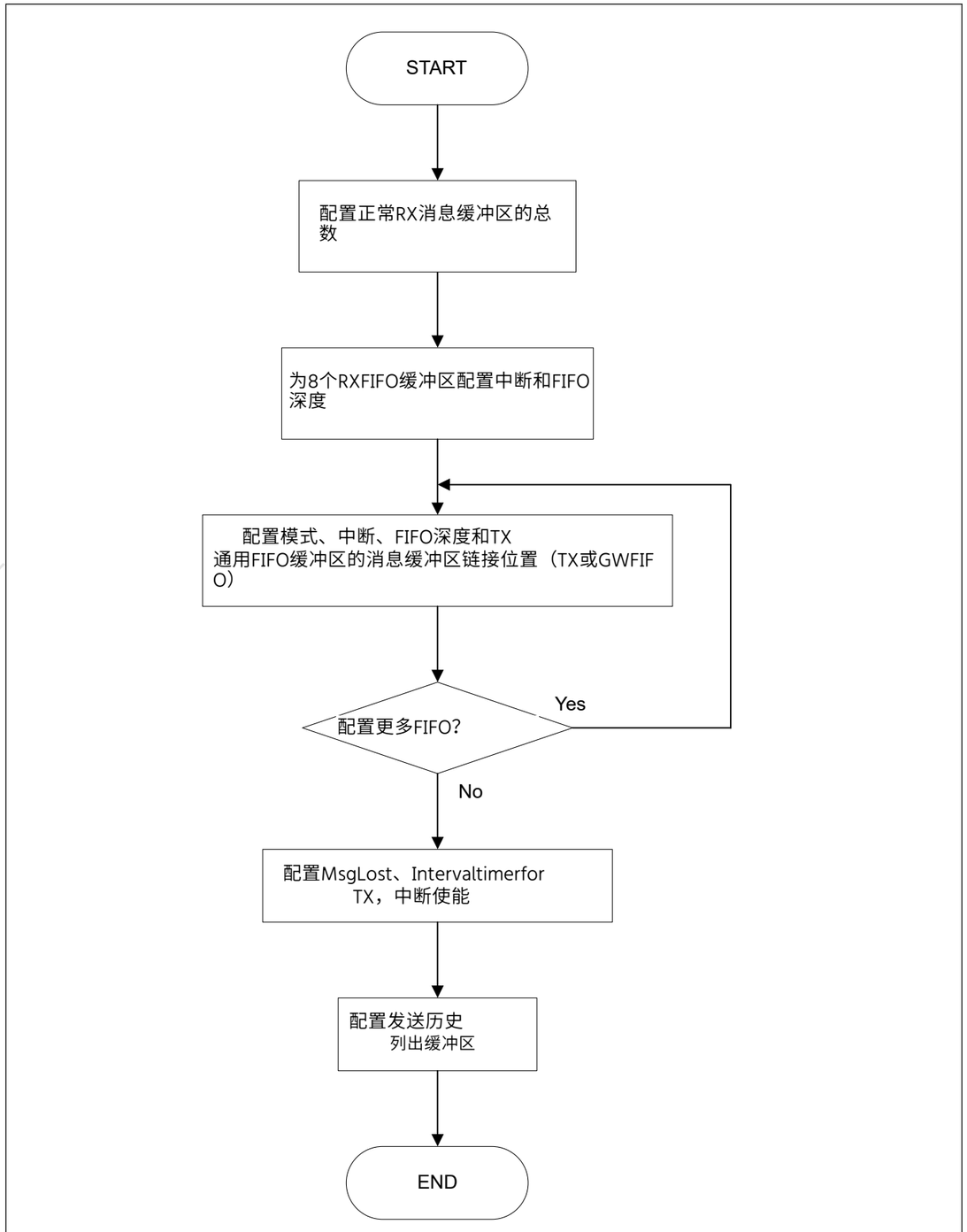

Figure 32.29 CAN-FD模块中的FIFO缓冲区配置流程

如图32.29所示，可以通过写入RXFIFO配置控制来配置各种FIFO缓冲区寄存器和通用FIFO配置控制寄存器。

For the 8 RX FIFO buffers, the following parameters can be configured:

- Interrupts
- FIFO depth
- FIFO payload data size.

For the common FIFO buffers, the following parameters can be configured:

- Mode
- Interrupts FIFO depth
- FIFO payload data size
- FIFO TX link position.

(1) FIFO mode configuration of Common FIFO buffers

The mode of the common FIFO buffers can be configured by writing to the CFDCFCCn.CFM[1:0] bits in the Common FIFO Configuration/Control Registers. The possible modes of configuration for Common FIFO buffers are:

- 00b RX mode (default mode after hardware reset)
- 100b TX mode
- 10b GW mode
- 11b Reserved (Do not write this value to the register bits)

Messages can only be read from the RX FIFO buffers and the Common FIFO buffers configured in RX mode. Messages are stored by the CAN module in these FIFO buffers based on the AFL entries.

Messages can be read and written into the Common FIFO buffers configured in TX mode. These messages are transmitted on the appropriate CAN channel.

Messages can only be read from the Common FIFO buffers configured in GW mode. However, the CPU read access has no impact on the read or write pointers. The pointers can only be incremented when a new message is stored in the FIFO buffer and decremented when a message is transmitted on the corresponding CAN channel by the CAN-FD module.

After a hardware reset, all the Common FIFO buffers are configured in RX mode by default. Only enable the FIFO buffers after configuring the Common FIFO buffers in the required modes.

In GW mode, when a transmit/receive FIFO buffer is trying to receive a new message while the transmit/receive FIFO buffer is already full of data, the oldest data of the buffer is overwritten with the message received or the message is discarded. The behavior is determined by setting the CFDCFCCEn.CFMOWM bit.

- When CFDCFCCEn.CFMOWM = 0:
  When writing of data is required due to reception of a new message while a transmit/receive FIFO buffer is full of data, the received message is discarded, and CFDCFSTSn.CFMLT bit is set to 1.

- When CFDCFCCEn.CFMOWM = 1:
  When writing of data is required due to reception of a new message while a transmit/receive FIFO buffer is full of data, the oldest data in the buffer is overwritten with the received message.
  The read pointer of the transmit/receive FIFO buffer simultaneously moves to the next oldest message.
  The CFDCFSTSn.CFMOW bit is then set to 1, which notifies that the oldest message has been overwritten with the received message.
  In addition, when a CAN bus error or arbitration-lost for the transmitting message occurs in the transmit/receive FIFO buffer full, the transmitting message is lost and retransmision for the message is not performed. The read point is then moves to the next message automatically.
  Do not write to this bit when the CFDCFCCn.CFE bit is 1.

(2) FIFO TX message buffer link configuration

When the common FIFO is configured as TX or GW FIFO, the FIFO buffer must be linked to a normal TX message buffer to participate in the transmission scan.

The link to a normal TX message buffer must be unique, for example the same TX message buffer cannot be shared between 2 or more common FIFO buffers.

对于8个RXFIFO缓冲区，可以配置以下参数：

- Interrupts
- FIFO depth

●FIFO有效负载数据大小。

对于常见的FIFO缓冲区，可以配置以下参数：

- Mode

●中断FIFO深度

●FIFO有效负载数据大小

●FIFOTX链路位置。

(1) CommonFIFO缓冲区的FIFO模式配置

通用FIFO缓冲区的模式可以通过写入Common中的CFDCFCCn.CFM[1:0]位来配置FIFO配置控制寄存器。通用FIFO缓冲区的可能配置模式有：

●00bRX模式（硬件复位后的默认模式）

- 100b TX mode
- 10b GW mode

●11b保留（不要将此值写入寄存器位）

只能从RXFIFO缓冲区和配置为RX模式的CommonFIFO缓冲区读取消息。CAN模块根据AFL条目将消息存储在这些FIFO缓冲区中。

可以在TX模式下配置的通用FIFO缓冲区中读取和写入消息。这些消息在适当的CAN通道上传输。

只能从配置为GW模式的CommonFIFO缓冲区读取消息。但是，CPU读取访问对读取或写入指针没有影响。只有当新消息存储在FIFO缓冲区中时，指针才能递增，而当CAN-FD模块在相应的CAN通道上传输消息时，指针才能递减。

硬件复位后，所有CommonFIFO缓冲区默认配置为RX模式。仅在所需模式下配置CommonFIFO缓冲区后才启用FIFO缓冲区。

在GW模式下，当发送接收FIFO缓冲区尝试接收新消息而发送接收FIFO缓冲区已满数据时，缓冲区中最旧的数据将被接收到的消息覆盖或丢弃该消息。该行为是通过设置CFDCFCCEn.CFMOWM位来确定的。

- When CFDCFCCEn.CFMOWM = 0:
  当发送接收FIFO缓冲区已满数据而由于接收到新报文而需要写入数据时，将丢弃接收到的报文，并将CFDCFSTSn.CFMLT位设置为1。

- When CFDCFCCEn.CFMOWM = 1:
  当发送接收FIFO缓冲区已满数据时，由于接收到新报文而需要写入数据时，缓冲区中最旧的数据将被接收到的报文覆盖。发送接收FIFO缓冲区的读指针同时移动到下一个最旧的消息。

  然后将CFDCFSTSn.CFMOW位设置为1，通知最旧的消息已被接收的消息覆盖。此外，当发送接收FIFO缓冲区满时发生CAN总线错误或发送报文仲裁丢失时，发送报文丢失且不进行报文重传。然后读取点自动移动到下一条消息。当CFDCFCCn.CFE位为1时不要写入该位。

(2) FIFOTX消息缓冲区链接配置

当普通FIFO配置为TX或GWFIFO时，FIFO缓冲区必须链接到正常的TX消息缓冲区才能参与传输扫描。

到普通TX消息缓冲区的链接必须是唯一的，例如，不能在2个或更多公共FIFO缓冲区之间共享相同的TX消息缓冲区。

Do not write data into a TX message buffer that is linked to a Common FIFO buffer. Also, the TX message buffer linked to a Common FIFO buffer should not be a part of the TX Queue.

The TX message buffer link of each Common FIFO buffer can be configured by writing to the CFDCFCCn.CFTML[4:0] bits in the Common FIFO Configuration/Control Registers. Available options for TX message buffer link configuration are:

- 0x00: TX Message Buffer 32
- 0x01: TX Message Buffer 33
- ⋮
- 0x07: TX Message Buffer 39

(3) FIFO depth configuration

The depth of each FIFO buffer can be configured by writing to the CFDRFCCn.RFDC[2:0] bits and CFDCFCCn.CFDC[2:0] bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/ Control Registers. The 8 available options for depth configuration are:

- 0x000: 0 Messages (FIFO buffer cannot be enabled)
- 0x001: 4 Messages
- 0x010: 8 Messages
- 0x011: 16 Messages
- 0x100: 32 Messages
- 0x101: 48 Messages
- 0x110: 64 Messages
- 0x111: 128 Messages

The RAM allocation for RX message buffers along with FIFO buffers is limited to (n + 1) × 256 messages. Configuration of the RX message buffers, along with FIFO buffers, that exceeds this maximum limit should not be done.

CAN-FD module logic does not check the validity of the configuration.

Note: If the FIFO depth of a common FIFO is 4 messages or more (CFDCFCCn.CFDC[2:0] > 000b), then the Common FIFO TX message buffer link is valid when the FIFO is disabled or enabled.

If FIFO depth is 0 messages, then the Common FIFO TX message buffer link is not valid when the FIFO is disabled or enabled.

(4) FIFO payload size configuration

The data size of each FIFO buffer can be configured by writing to the CFDRFCCn.RFPLS[2:0] bits and CFDCFCCn.CFPLS[2:0] bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/ Control Registers. The eight available options for depth configuration are:

- 000b: 8 bytes
- 001b: 12 bytes
- 010b: 16 bytes
- 011b: 20 bytes
- 100b: 24 bytes
- 101b: 32 bytes
- 110b: 48 bytes
- 111b: 64 bytes

The RAM allocation for RX message buffers along with FIFO buffers is limited to (n + 1) × 256 messages with 64 data bytes. Configuration of the RX message buffers, along with FIFO buffers, that exceeds this maximum limit should not be done.

CAN-FD module logic does not check the validity of the configuration.

不要将数据写入链接到通用FIFO缓冲区的TX消息缓冲区。此外，链接到通用FIFO缓冲区的TX消息缓冲区不应成为TX队列的一部分。

每个通用FIFO缓冲区的TX报文缓冲区链接可以通过写入通用FIFO配置控制寄存器中的CFDCFCCn.CFTML[4:0]位来配　　置。TX消息缓冲区链路配置的可用选项包括：

- 0x00：TX报文缓冲区32
- 0x01：TX报文缓冲区33
- ⋮
- 0x07：TX报文缓冲区39

(3) FIFO深度配置

每个FIFO缓冲区的深度可以通过写入CFDRFCCn.RFDC[2:0]位和RXFIFO配置控制寄存器和通用FIFO配置中的CFDCFCCn.CFDC[2:0]位控制寄存器。深度配置的8个可用选项是：

- 0x000：0条消息（无法启用FIFO缓冲区）
- 0x001: 4 Messages
- 0x010: 8 Messages
- 0x011: 16 Messages
- 0x100: 32 Messages
- 0x101: 48 Messages
- 0x110: 64 Messages
- 0x111: 128 Messages

RX消息缓冲区和FIFO缓冲区的RAM分配限制为(n+1)×256条消息。不应配置超过此最大限制的RX消息缓冲区以及FIFO缓冲区。

CAN-FD模块逻辑不检查配置的有效性。

Note: 如果公共FIFO的FIFO深度为4条或更多消息（CFDCFCCn.CFDC[2:0]>000b），则公共FIFOTX报文缓冲区链接在FIFO禁用或启用时有效。

如果FIFO深度为0消息，则通用FIFOTX消息缓冲区链接在FIFO禁用或启用时无效。

(4) FIFO有效载荷大小配置

每个FIFO缓冲区的数据大小可以通过写入CFDRFCCn.RFPLS[2:0]位和RXFIFO配置控制寄存器和通用FIFO配置中的CFDCFCCn.CFPLS[2:0]位控制寄存器。深度配置的八个可用选项是：

- 000b: 8 bytes
- 001b: 12 bytes
- 010b: 16 bytes
- 011b: 20 bytes
- 100b: 24 bytes
- 101b: 32 bytes
- 110b: 48 bytes
- 111b: 64 bytes

RX报文缓冲区和FIFO缓冲区的RAM分配限制为(n+1)×256条64数据字节的报文。不应配置超过此最大限制的RX消息缓冲区以及FIFO缓冲区。

CAN-FD模块逻辑不检查配置的有效性。

Note: This feature is not available in the classical CAN function.

(5) FIFO interrupt configuration

The Interrupt generation conditions for the FIFO buffers can be configured by writing to the CFDRFCCn.RFIM and CFDCFCCn.CFIM bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers. The two available options are:

- 0:
  - RX FIFO mode: Interrupt generated when the Common FIFO counter reaches CFDRFCCn.RFIGCV/ CFDCFCCn.CFIGCV value
  - TX FIFO mode: Interrupt generated when the Common FIFO transmits the last message successfully
  - GW FIFO mode
  - Frame RX: Interrupt generated when message counter increments and reaches the interrupt threshold value
  - Frame TX: Interrupt generated when the last message is transmitted successfully from FIFO.
- 1:
  - RX FIFO mode: Interrupt generated at the end of storage of every received message
  - TX FIFO mode: Interrupt generated for every successfully transmitted message
  - GW FIFO mode
  - Frame RX: Interrupt generated when message is stored in the FIFO
  - Frame TX: Interrupt generated when message is successfully transmitted from the FIFO.

If the Interrupt Mode bit is 0 for a RX FIFO, then interrupt is generated based on the configuration of the CFDRFCCn.RFIGCV[2:0] bits.

Similarly, if the Interrupt Mode bit is 0 for a Common FIFO configured in RX mode, then interrupt is generated based on the configuration of CFDCFCCn.CFIGCV[2:0] bits.

The eight available options for configuring the FIFO counter value for generation of an interrupt are:

- 000b: Interrupt generated when FIFO is 1/8th Full
- 001b: Interrupt generated when FIFO is 1/4th Full
- 010b: Interrupt generated when FIFO is 3/8th Full
- 011b: Interrupt generated when FIFO is 1/2 Full
- 100b: Interrupt generated when FIFO is 5/8th Full
- 101b: Interrupt generated when FIFO is 3/4th Full
- 110b: Interrupt generated when FIFO is 7/8th Full
- 111b: Interrupt generated when FIFO is Full.

In this case, an interrupt is generated when the message count matches the configured value.

However, there are some limitations on the configuration of the CFDRFCCn.RFIGCV[2:0] and CFDCFCCn.CFIGCV[2:0] bits depending on the FDC[2:0] bits (FIFO Depth Configuration), see Table 32.18.

Table 32.18 FIFO interrupt generation counter and FIFO depth configuration (1 of 2)

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
000b	Don't care (FIFO cannot be enabled)							
001b	Allowed	Not allowed	Allowed	Not allowed	Allowed	Not allowed	Allowed	Not allowed
010b	Allowed							
011b	Allowed							
100b	Allowed							

Note: 此功能在经典CAN功能中不可用。

(5) FIFO中断配置

FIFO缓冲区的中断生成条件可以通过写入CFDRFCCn.RFIM和RXFIFO配置控制寄存器和通用FIFO配置控制中的CFDCFCCn.CFIM位寄存器。两个可用选项是：

- 0:
  RXFIFO模式：CommonFIFO计数器达到CFDRFCCn.RFIGCVCFDCFCCn.CFIGCV值时产生中断

  TXFIFO模式：CommonFIFO成功发送最后一条报文时产生中断
  - GW FIFO mode

  FrameRX：当消息计数器递增并达到中断阈值时产生中断

  FrameTX：当最后一条消息从FIFO成功发送时产生中断。
- 1:
  RXFIFO模式：在每个接收到的消息存储结束时产生中断

  TXFIFO模式：为每个成功传输的消息生成中断
  - GW FIFO mode

  FrameRX：消息存储在FIFO中时产生的中断

  FrameTX：消息从FIFO成功传输时产生的中断。

如果RXFIFO的中断模式位为0，则根据配置生成中断CFDRFCCn.RFIGCV[2:0] bits.

同样，如果配置为RX模式的CommonFIFO的中断模式位为0，则根据CFDCFCCn.CFIGCV[2:0]位的配置生成中断。

配置FIFO计数器值以生成中断的八个可用选项是：

- ●000b：FIFO为18thFull时产生的中断
- ●001b：FIFO为14thFull时产生中断
- ●010b：FIFO为38thFull时产生中断
- ●011b：FIFO为12Full时产生中断
- ●100b：FIFO为58thFull时产生的中断
- ●101b：FIFO为34thFull时产生中断
- ●110b：FIFO为78thFull时产生中断
- ●111b：FIFO满时产生中断。

在这种情况下，当消息计数与配置值匹配时会产生中断。

但是，CFDRFCCn.RFIGCV[2:0]和CFDCFCCn.CFIGCV[2:0]位的配置有一些限制，具体取决于FDC[2:0]位（FIFO深度配置），请参见表32.18。

Table 32.18 FIFO中断生成计数器和FIFO深度配置（1of2）

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
000b	无关（无法启用FIFO）							
001b	Allowed	不允许	Allowed	不允许	Allowed	不允许	Allowed	不允许
010b	Allowed							
011b	Allowed							
100b	Allowed							

Table 32.18 FIFO interrupt generation counter and FIFO depth configuration (2 of 2)

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
101b	Allowed							
110b	Allowed							
111b	Allowed							

Common FIFO buffer can set an interrupt output at the completion time of transmitting one frame, or the completion of reception. In addition, Common FIFO and RX FIFO can set an interrupt output, when stored to the setup number (CFDC/RFDC) of FIFO stages.

32.6.2.2 FIFO Buffers Control

The FIFO interrupt must be enabled by setting any one of the following bits in the RX FIFO Configuration/Control Registers:

- CFDRFCCn.RFIE
- CFDRFCCn.RFFIE.

In addition, the FIFO interrupt must be enabled by setting any one of the following bits in the Common FIFO Configuration/Control Registers:

- CFDCFCCn.CFRXIE
- CFDCFCCn.CFTXIE
- CFDCFCCEn.CFFIE
- CFDCFCCEn.CFOFRXIE
- CFDCFCCEn.CFOFTXIE.

After configuration is complete, each FIFO can be enabled by setting the CFDRFCCn.RFE and CFDCFCCn.CFE bits in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers to allow transmission and reception of messages.

When CFDCFCCEn.CFBME = 1, it becomes FIFO buffering mode, send data is stored in the Common FIFO, and transmission is stopped. Transmission starts when CFDCFCCEn.CFBME = 0.

Do not write 1 from 0 for this bit when the CFDCFCCn.CFE bit is 1.

32.7 Interrupts and DMA

32.7.1 Interrupts

The CAN-FD module generates several interrupts. The interrupt output, which is connected to the Interrupt Controller Unit (ICU), can be controlled by the corresponding interrupt enable bit.

The status flag is set independent from this enable bit.

The channel transmission interrupt has an additional status flag register. The status bits are set when the corresponding interrupt enables are set.

The status flag register supports the identification of the interrupt source for the channel transmission, as this interrupt is driven by several trigger sources.

The interrupts in the CAN-FD module can be classified into two groups, global interrupts and channel interrupts:

- Global interrupts:
  The CAN-FD module can generate 2 global interrupts:
  - Global interrupt for successful reception into the 8 RX FIFO buffers
  - Global error interrupt.
- Channel interrupts:
  Each channel of the CAN-FD module can generate 3 channel interrupts:

Table 32.18 FIFO中断生成计数器和FIFO深度配置（2之2）

RFDC[2:0] (CFDC[2:0])	RFIGCV[2:0] (CFIGCV[2:0])							
	111b	110b	101b	100b	011b	010b	001b	000b
101b	Allowed							
110b	Allowed							
111b	Allowed							

普通FIFO缓冲器可以在发送一帧完成时设置中断输出，或者接收完成时输出中断。此外，CommonFIFO和RXFIFO可以设置中断输出，当存储到FIFO阶段的设置号(CFDCRFDC)时。

32.6.2.2 FIFO缓冲器控制

必须通过设置RXFIFO配置控制中的以下任一位来启用FIFO中断
Registers:

- CFDRFCCn.RFIE
- CFDRFCCn.RFFIE.

此外，必须通过设置CommonFIFO中的以下任一位来启用FIFO中断
Configuration/Control Registers:

- CFDCFCCn.CFRXIE
- CFDCFCCn.CFTXIE
- CFDCFCCEn.CFFIE
- CFDCFCCEn.CFOFRXIE
- CFDCFCCEn.CFOFTXIE.

配置完成后，可以通过设置CFDRFCCn.RFE和CFDCFCCn.CFE位来使能每个FIFO
RXFIFO配置控制寄存器和通用FIFO配置控制寄存器，以允许发送和接收消息。

当CFDCFCCEn.CFBME=1时，变为FIFO缓冲模式，发送数据存放在CommonFIFO中，停止发送。当CFDCFCCEn.CFBME=0时开始传输。

当CFDCFCCn.CFE位为1时，请勿对该位从0写入1。

32.7 中断和DMA

32.7.1 Interrupts

CAN-FD模块产生几个中断。连接到中断控制器单元（ICU）的中断输出可由相应的中断使能位控制。

状态标志的设置独立于该使能位。

通道传输中断有一个额外的状态标志寄存器。当相应的中断使能被设置时，状态位被设置。

状态标志寄存器支持识别通道传输的中断源，因为该中断由多个触发源驱动。

CAN-FD模块中的中断可以分为两类，全局中断和通道中断：

- Global interrupts:
  CAN-FD模块可以产生2个全局中断：
  成功接收到8个RXFIFO缓冲区的全局中断
  全局错误中断。
- Channel interrupts:
  CAN-FD模块的每个通道可以产生3个通道中断：

1. Channel transmission
   - Transmission completion from channel
   - Transmission abort from channel
   - Transmission from TX Queue for a channel
   - Channel THL interrupt
   - Successful transmission from a Common FIFO in TX or GW mode for a channel.
2. Channel error interrupt
3. Successful reception in a Common FIFO in RX or GW mode for a channel or successful routing in a TXQ.

The interrupts are cleared when the corresponding flag bits are cleared or the Interrupt enable bits are cleared.

Table 32.19 gives an overview of interrupt sources for the different interrupt outputs. The interrupt outputs are active-high.

Table 32.19 Interrupt source overview (1 of 2)

Parameter	Interrupt	Interrupt source	Interrupt clearing
Global interrupts	Successful reception into at least one RX FIFO	Interrupt flag of corresponding RX FIFO for which interrupt is enabled	Clear the interrupt flag of corresponding RX FIFO buffer for which interrupt is enabled
	FIFO full into at least one RX FIFO	FIFO Full Interrupt flag of corresponding RX FIFO for which interrupt is enabled	Clear the FIFO Full Interrupt flags of corresponding RX FIFO buffer for which interrupt is enabled
	Global error	Interrupt source is any of the following: • DLC Error flag • Message Lost Status bit • Message Overwrite Status bit • TXQ Message Lost Status bit • TXQ Message Overwrite Status bit • TX History Entry Lost Status bit • CAN-FD Message Payload Overflow flag*1	Clear all of the following: • DLC Error flag • Message Lost flags in all of the FIFO Status Registers • Message Overwrite flags in all of the Common FIFO Status Registers • Message Lost flags in all of the TXQ Status Registers • Message Overwrite flags in all of the TXQ Status Registers • TX History List Entry Lost flag • CAN-FD Message Payload Overflow flag.*1

1.渠道传输
   从通道传输完成
   从通道中止传输
   从通道的TX队列传输
   通道THL中断
   在TX或GW模式下从通用FIFO成功传输通道。
2.通道错误中断
3.通道在RX或GW模式下的通用FIFO中成功接收或TXQ中的成功路由。

当相应的标志位被清除或中断使能位被清除时，中断被清除。

表32.19概述了不同中断输出的中断源。中断输出为高电平有效。

Table 32.19 中断源概述(1of2)

Parameter	Interrupt	中断源	中断清除
全局中断	成功接收到至少一个RXFIFO	对应的RXFIFO的中断标志，中断使能	清除对应的中断标志 启用中断的RXFIFO缓冲区
	FIFO已满至至少一个RXFIFO	允许中断的相应RXFIFO的FIFOFull中断标志	清除启用中断的相应RXFIFO缓冲区的FIFOFullInterrupt标志
	全局错误	中断源为以下任意一种：● DLC错误标志 • 消息丢失状态位 • 消息覆盖状态位 • TXQ消息丢失状态位 • TXQ报文覆盖状态位 • TX历史条目丢失状态位 • CAN-FD消息有效负载溢出标志*1	清除以下所有内容：● DLC错误标志 • 在所有的消息丢失标志FIFO状态寄存器 • 所有通用FIFO状态寄存器中的消息覆盖标志 • 在所有的消息丢失标志TXQ状态寄存器 • 所有TXQ状态寄存器中的消息覆盖标志 • TX历史列表条目丢失标志 • CAN-FD消息负载溢出标志。*1

Table 32.19 Interrupt source overview (2 of 2)

Parameter	Interrupt	Interrupt source	Interrupt clearing
Channel transmission interrupts	Channel n successful transmission	Any channel related TX MB Successful flag when interrupt is enabled. Separate interrupts are provided for Common FIFO buffers and TX Queue. Note: These interrupts are only set for TX message buffers that do not belong to an enabled TX Queue and are not pointing to a Common FIFO.	Clear all channel related TX MB Result Status bits for which the interrupt is enabled
	Channel n abort	Any channel related TX MB Abort flag when interrupt is enabled Separate interrupts are provided for Common FIFO buffers and TX Queue Note: These interrupts are only set for TX message buffers that do not belong to an enabled TX Queue and are not pointing to a Common FIFO.	Clear all channel related TX MB Result Status bits for which the interrupt is enabled globally
	Channel n transmission from TX Queue	Related Channel TX Queue Interrupt flag	Clear related Channel TX Queue Interrupt flag
	Channel n THL Interrupt	Channel n THL Interrupt Status flag	Clear the relevant THL Interrupt Status flag
	Channel n COM FIFO TX Interrupt	Interrupt flag for Common FIFOs in TX or GW mode belonging to the related channel	Clear the interrupt flags of Common FIFOs in RX or GW mode belonging to the related channel
	Channel n COM FIFO One Frame TX Interrupt	One Frame Transmission Interrupt flag for Common FIFOs belonging to the related channel	Clear the One Frame Transmission Interrupt flags of Common FIFOs belonging to the related channel
	Channel n TXQ One Frame TX Interrupt	One Frame Transmission Interrupt flag for TXQs belonging to the related channel	Clear the One Frame Transmission Interrupt flags of TXQs belonging to the related channel
Channel COM RX FIFO Interrupt	Channel n COM FIFO RX Interrupt	Interrupt Flag for Common FIFOs in RX or GW mode belonging to the related channel	Clear the interrupt flags of Common FIFOs in RX or GW mode belonging to the related channel
	Channel n COM FIFO One Frame RX Interrupt	One Frame Reception Interrupt flag for Common FIFOs belonging to the related channel	Clear the One Frame Reception Interrupt flags of Common FIFOs belonging to the related channel
	Channel n COM FIFO Full Interrupt	FIFO Full Interrupt flag for Common FIFOs in RX or GW mode belonging to the related channel	Clear the FIFO Full Interrupt flags of Common FIFOs in RX or GW mode belonging to the related channel
	Channel n TXQ One Frame Routing Interrupt	One Frame Routing Interrupt flag for TXQs in GW mode belonging to the related channel	Clear the One Frame Routing Interrupt flags of TXQs in GW mode belonging to the related channel
	Channel n TXQ Full Interrupt	TXQ Full Interrupt flag for TXQs in GW mode belonging to the related channel	Clear the FIFO Full Interrupt flags of TXQs in GW mode belonging to the related channel
Channel Error Interrupt	Channel n Error	Any channel related error flag in the Channel Error Flag Register for which interrupt is enabled in the Channel Error Interrupt Enable Register	Clear all channel related error flags in the Channel Error Flag Register for which interrupt is enabled in the Channel Error Interrupt Enable Register

Note 1. This feature is not available in the classical CAN function.

Table 32.19 中断源概述(2of2)

Parameter	Interrupt	中断源	中断清除
通道传输中断	通道n传输成功	允许中断时任何与通道相关的TXMB成功标志。为公共提供单独的中断 FIFO缓冲区和TX队列。 Note: 这些中断仅针对不属于启用的TX队列且不指向CommonFIFO的TX消息缓冲区设置。	清除所有通道相关的TXMB结果 启用中断的状态位
	频道n中止	允许中断时任何与通道相关的TXMB中止标志为公共提供单独的中断 FIFO缓冲区和TX队列 Note: 这些中断仅针对不属于启用的TX队列且不指向CommonFIFO的TX消息缓冲区设置。	清除所有通道相关的TXMB结果 全局启用中断的状态位
	来自TXQueue的通道n传输	相关通道TX队列中断标志	清除相关ChannelTXQueue中断标志
	Channel n THL Interrupt	通道nTHL中断状态标志	清除相关的THL中断状态标志
	通道nCOMFIFO TX Interrupt	属于相关通道的TX或GW模式下CommonFIFO的中断标志	清除Common的中断标志 属于相关通道的RX或GW模式的FIFO
	通道nCOMFIFO一帧发送Interrupt	一帧传输中断标志 属于相关通道的通用FIFO	清除一帧传输 属于相关通道的CommonFIFO的中断标志
	通道nTXQ一帧TX中断	属于相关通道的TXQ的一帧传输中断标志	清除一帧传输 属于相关通道的TXQ的中断标志
通道COMRX FIFO Interrupt	通道nCOMFIFO RX Interrupt	属于相关通道的RX或GW模式下CommonFIFO的中断标志	清除Common的中断标志 属于相关通道的RX或GW模式的FIFO
	通道nCOMFIFO一帧接收Interrupt	通用的一帧接收中断标志 属于相关通道的FIFO	清除属于相关通道的CommonFIFO的一帧接收中断标志
	通道nCOMFIFO完全中断	属于相关通道的处于RX或GW模式的CommonFIFO的FIFOFull中断标志	清除属于相关通道的RX或GW模式下CommonFIFO的FIFOFullInterrupt标志
	通道nTXQ一帧路由Interrupt	属于相关通道的GW模式下TXQ的一帧路由中断标志	清除属于相关通道的GW模式TXQ的一帧路由中断标志
	通道nTXQ已满Interrupt	属于相关通道的GW模式下TXQ的TXQ完全中断标志	清除属于相关通道的GW模式下TXQ的FIFOFullInterrupt标志
通道错误Interrupt	通道n错误	通道错误标志寄存器中的任何通道相关错误标志，其中断被启用 通道错误中断使能寄存器	清除通道错误标志寄存器中所有通道相关的错误标志，在通道错误中断允许寄存器中允许中断

注1.此功能在经典CAN功能中不可用。

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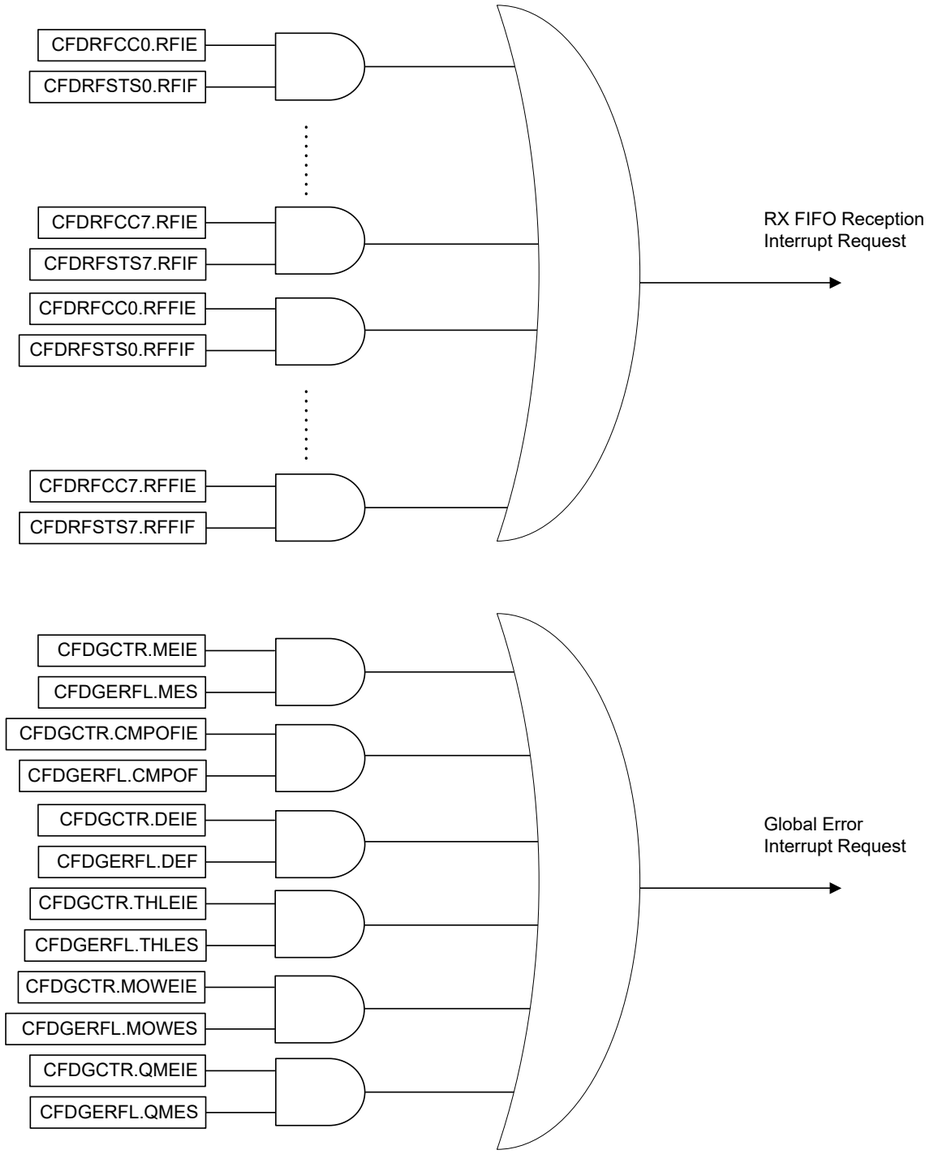
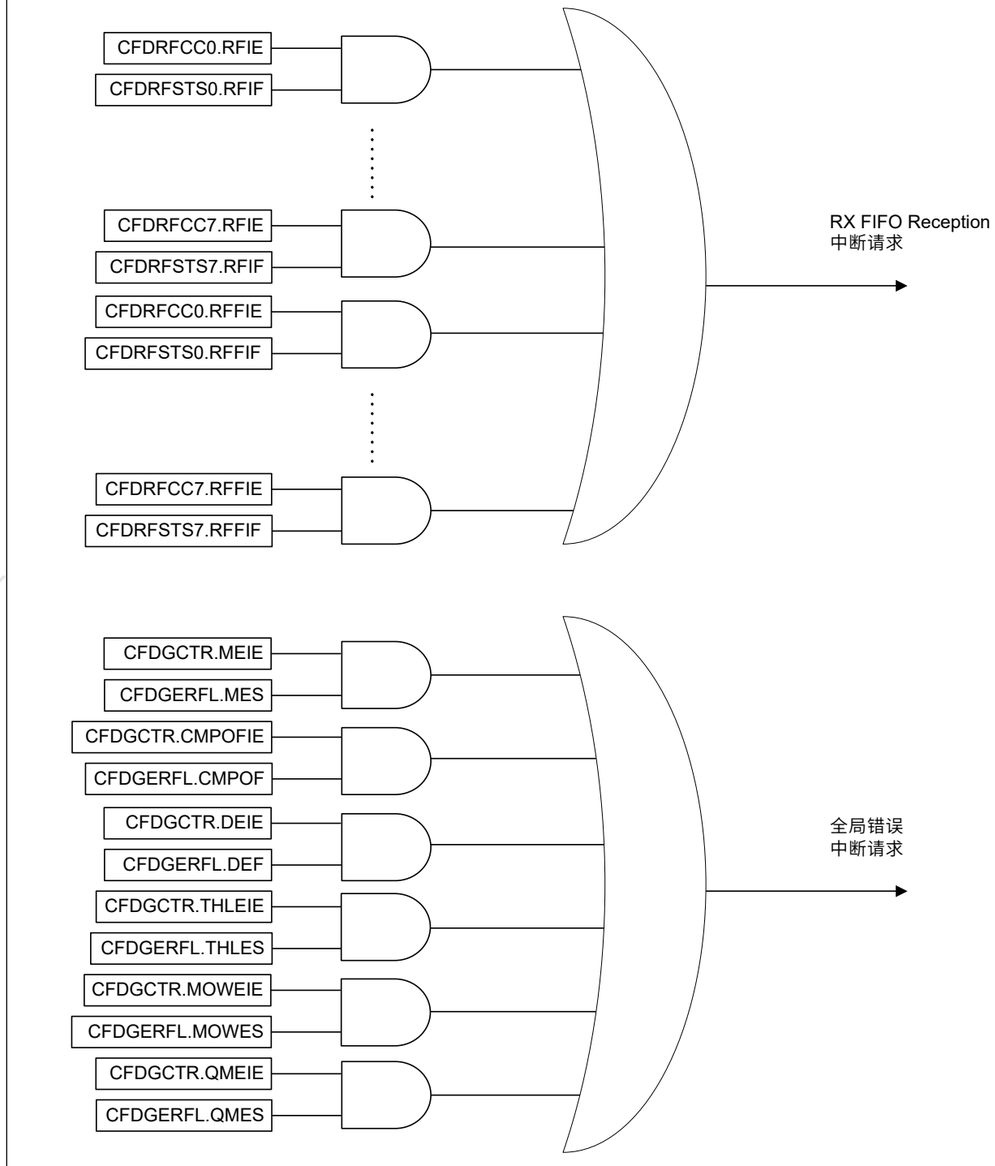


Note: CFDGCTR.CMPOFIE and CFDGERFL.CMPOF bits are not available in the classical CAN function. For this reason, these signals and the AMD circuit to which these signals are connected are not in the classical CAN function.

Figure 32.30 Global interrupt block diagram



Note: CFDGCTR.CMPOFIE和CFDGERFL.CMPOF位在经典CAN功能中不可用。由于这个原因，这些信号和这些信号所连接的AMD电路不在经典的CAN功能中。

Figure 32.30 全局中断框图

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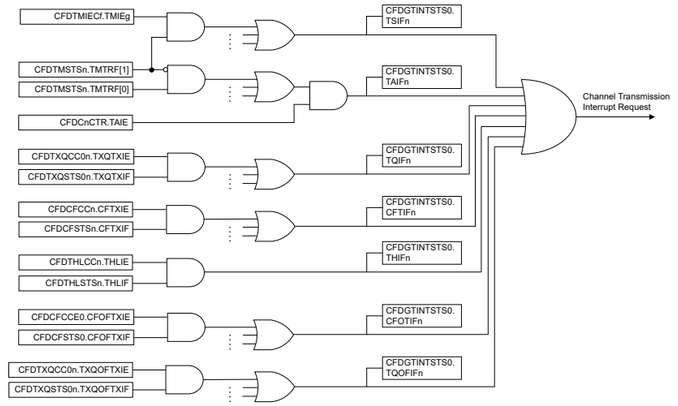
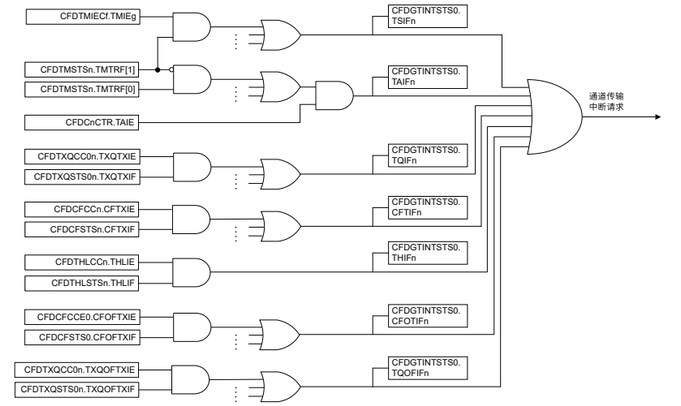


Note: CFDCnCTR.TDCVFIE and CFDCnFDSTS.TDCVF bits are not available in the classical CAN function. For this reason, these signals and the AMD circuit to which these signals are connected are not in the classical CAN function.

Figure 32.31 Channel interrupt block diagram



Note: CFDCnCTR.TDCVFIE和CFDCnFDSTS.TDCVF位在经典CAN功能中不可用。由于这个原因，这些信号和这些信号所连接的AMD电路不在经典的CAN功能中。

Figure 32.31 通道中断框图

RA生态工作室

32.7.2 DMA Transfer

The CAN-FD module has message buffers that can be associated with a DMA channel:

- Reception DMA
  - 8 RX FIFO message buffers
  - 8 Common FIFO message buffers
- Transmission DMA
  - 16 TXQ message buffers (TXQ0, TXQ3)
  - 8 Common FIFO message buffers.

Figure 32.32 shows the potential DMA channels.

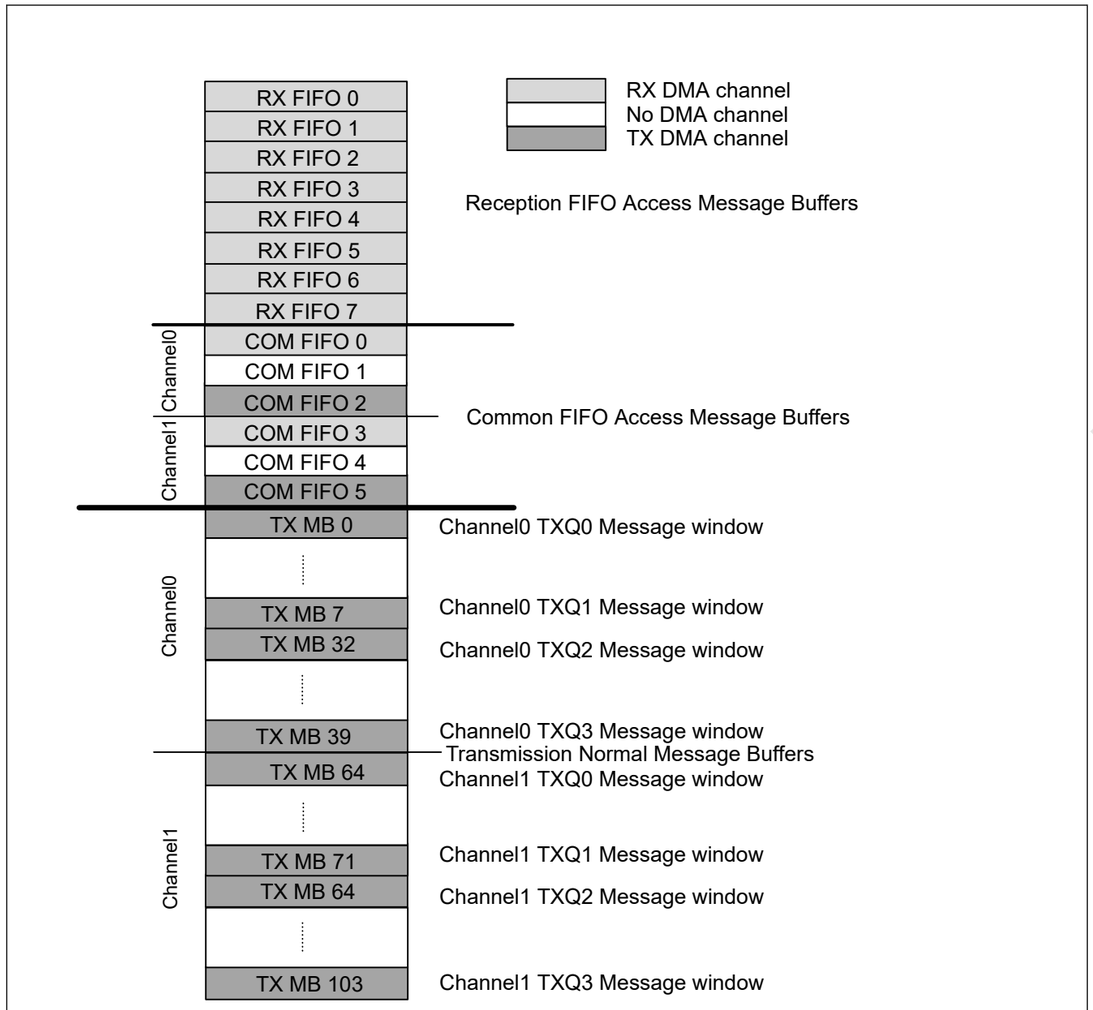


Figure 32.32 Message buffer connectable to a DMA channel

32.7.2 DMA Transfer

CAN-FD模块具有可与DMA通道关联的消息缓冲区：

- Reception DMA
  8个RXFIFO消息缓冲区
  8个通用FIFO消息缓冲区
- Transmission DMA
  16个TXQ消息缓冲区（TXQ0、TXQ3）
  8个通用FIFO消息缓冲区。

图32.32显示了潜在的DMA通道。

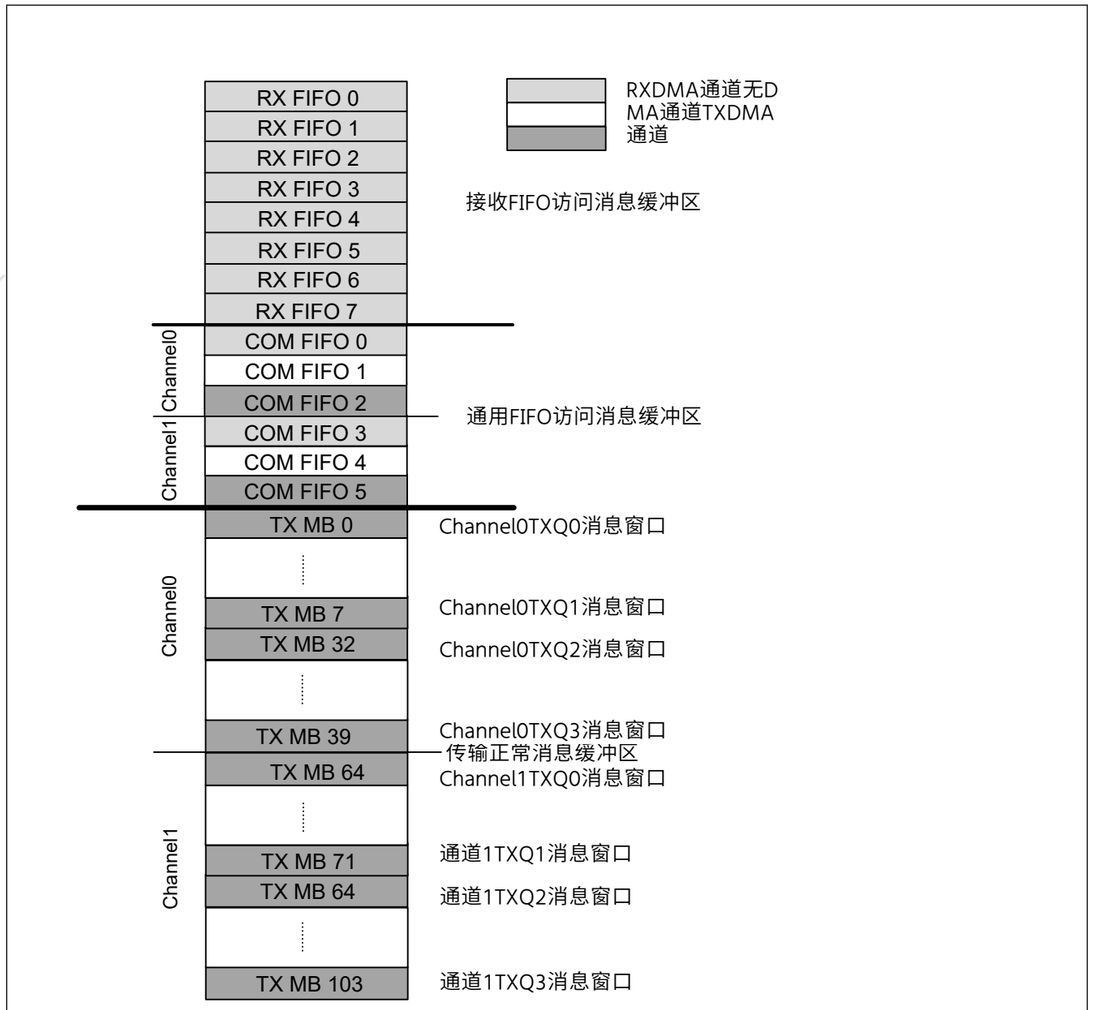


Figure 32.32 可连接到DMA通道的消息缓冲区

A DMA channel transfer request is generated for each FIFO entry to the DMAC when the related CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE is set to 1 and the belonging FIFO is not empty.

Reception FIFO Interrupt should be disabled for this particular FIFO (CFDRFCCn.RFIE or CFDCFCCn.CFRXIE)

Use the regular start address for the DMA access window address and add 0x8000 to the regular start address for the debugger access window. See Figure 32.33.

Table 32.20 DMA channel access window address

b = Message buffer component index	MBCP	Register	P	Regular start address n = [0, 1]
[0…7]	FRMBCPb[i]	RFIDE	x	0x6000 + b*0x0080
		RFPTRE	x	0x6004 + b*0x0080
		RFFDSTSE	x	0x6008 + b*0x0080
		RFDFpE	[0…15]	0x600C + b*0x0004 + b*0x0080
[0…2]	CFMBCPb[i]	CFIDE	x	0x6400 + b*0x0080 + n*0x180
		CFPTRE	x	0x6404 + b*0x0080 + n*0x180
		CFFDCSTSE	x	0x6408 + b*0x0080 + n*0x180
		CFDFpE	[0…15]	0x640C + b*0x0004 + b*0x0080 + n*0x180

DMA FIFO pointer decrement is done automatically by reading the last configured data payload byte (CFDRFCCn.RFPLS or CFDCFCCn.CFPLS).

Note: The DMA must read the exact length of the configured data payload size (CFDRFCCn.RFPLS or CFDCFCCn.CFPLS).

Note: This feature is not available for classical CAN function because CFDRFCCn.RFPLS and CFDCFCCn.CFPLS are not in classical CAN.

Do not write to the FIFO and TXQ control registers when DMA is enabled. The DMA enable of the particular DMA FIFO (CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE) can be set at any time. Figure 32.33 shows a configuration flow for an initial setup.

When CFDCDTTCT.TQ0DMAE or CFDCDTTCT.TQ3DMAE or CFDCDTTCT.CFDMAE is set, the messages of the corresponding TXQ or Common FIFO can be handled by a DMA controller.

The following procedure shows when the TXQ or the Common FIFO can be handled by a DMA controller.

1. CPU checks the TXQ or the Common FIFO is not full.
2. When transmit data can be used, the CPU sets this data to Common FIFO or TXQ.
   When using Common FIFO, transmit data is write in CFDCFID, CFDCFPTR, CFDCFFDCSTS and CFDTMBCPb[i] register.
   When using TXQ, transmit data is write in CFDTMID, CFDTMPTR, CFDTMFDCTR and CFDTMDFp register.
3. For Common FIFO, the common FIFO pointer is incremented automatically when DMA controller writes the last data payload byte configured by CFDCFCCn.CFPLS.
   For TXQ, if the data of 64 data payload is written, a TXQ pointer increases automatically. When payload data is less than 64 bytes, dummy data must be written in and 64 data payload size must be done.

Note: Only 32-bit write-access can be possible on the DMA message handling.

当相关的CFDCDTCT.RFDMAE或
CFDCDTCT.CFDMAE设置为1并且所属的FIFO不为空。

应禁用此特定FIFO（CFDRFCCn.RFIE或CFDCFCCn.CFRXIE）的接收FIFO中断

使用常规起始地址作为DMA访问窗口地址，并将0x8000添加到调试器访问窗口的常规起始地址。请参见图32.33。

Table 32.20 DMA通道访问窗口地址

b=消息缓冲区组件索引	MBCP	Register	P	常规起始地址n=[0 1]
[0…7]	FRMBCPb[i]	RFIDE	x	0x6000 + b*0x0080
		RFPTRE	x	0x6004 + b*0x0080
		RFFDSTSE	x	0x6008 + b*0x0080
		RFDFpE	[0…15]	0x600C + b*0x0004 + b*0x0080
[0…2]	CFMBCPb[i]	CFIDE	x	0x6400 + b*0x0080 + n*0x180
		CFPTRE	x	0x6404 + b*0x0080 + n*0x180
		CFFDCSTSE	x	0x6408 + b*0x0080 + n*0x180
		CFDFpE	[0…15]	0x640C + b*0x0004 + b*0x0080 + n*0x180

DMAFIFO指针递减是通过读取最后配置的数据有效负载字节（CFDRFCCn.RFPLS或CFDCFCCn.CFPLS）自动完成的。

Note: DMA必须读取配置的数据有效负载大小（CFDRFCCn.RFPLS或CFDCFCCn.CFPLS).

Note: 此功能不适用于经典CAN功能，因为CFDRFCCn.RFPLS和CFDCFCCn.CFPLS不在经典CAN中。

启用DMA时不要写入FIFO和TXQ控制寄存器。可以随时设置特定DMAFIFO（CFDCDTCT.RFDMAE或CFDCDTCT.CFDMAE）的DMA使能。图32.33显示了初始设置的配置流程。

当CFDCDTTCT.TQ0DMAE或CFDCDTTCT.TQ3DMAE或CFDCDTTCT.CFDMAE置位时，相应的TXQ或CommonFIFO的消息可以由DMA控制器处理。

以下过程显示了DMA控制器何时可以处理TXQ或通用FIFO。

1.CPU检查TXQ或CommonFIFO未满。

2.当可以使用发送数据时，CPU将此数据设置为CommonFIFO或TXQ。
使用CommonFIFO时，发送数据写入CFDCFID、CFDCFPTR、CFDCFDCSTS和CFDTMBCPb[i]寄存器。使用TXQ时，发送数据写入CFDTMID、CFDTMPTR、CFDTMFDCTR和CFDTMDFp寄存器。

3.对于CommonFIFO，当DMA控制器写入由CFDCFCCn.CFPLS配置的最后一个数据负载字节时，commonFIFO指针会自动递增。对于TXQ，如果写入64位数据载荷的数据，则TXQ指针自动增加。当有效载荷数据小于64字节时，必须写入虚拟数据，并且必须完成64数据有效载荷大小。

Note: DMA消息处理只能进行32位写访问。

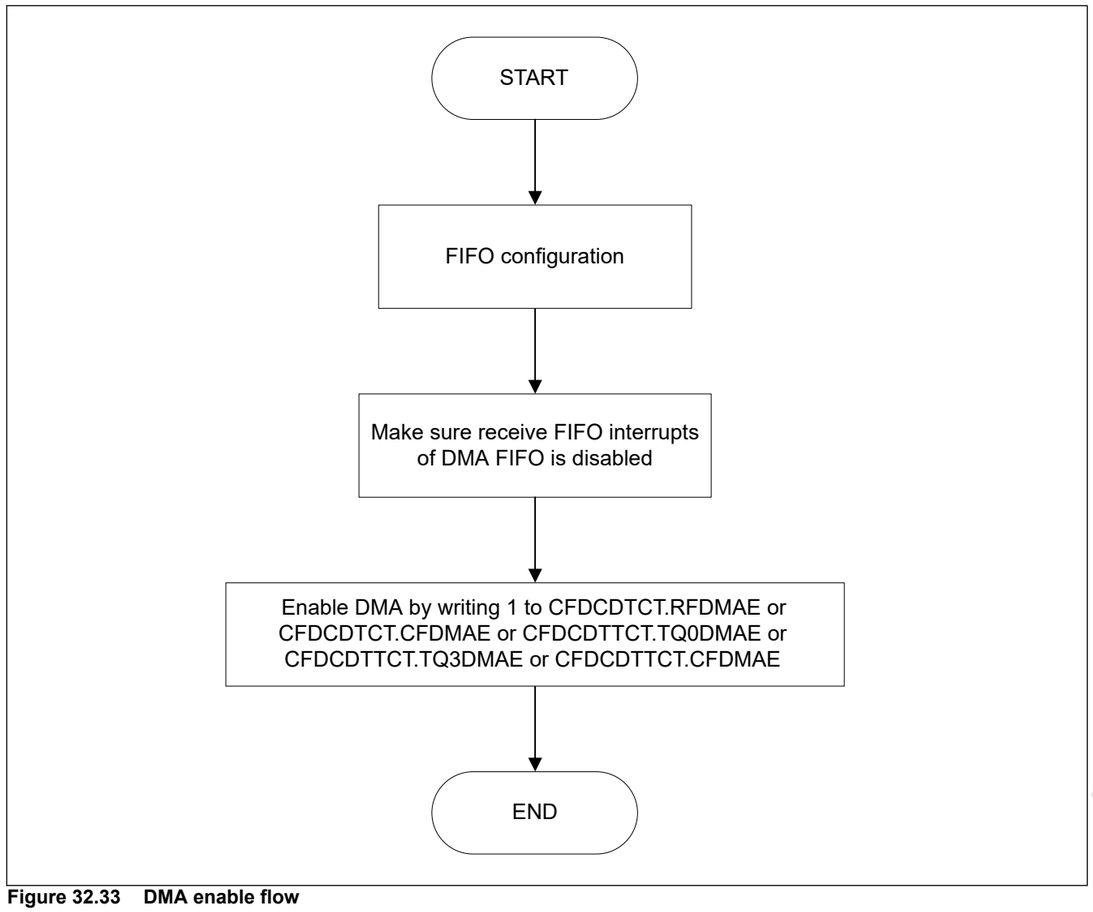


Figure 32.33 DMA enable flow

To disable a DMA transfer request, you must disable the particular DMA enable bit (CFDCDTCT.RFDMAE or CFDCDTCT.CFDMAE). If the disable is made during an ongoing transfer, then the transfer must be completed first before further action can be taken. The transfer status can be identified by the CFDCDTSTS.RFDMASTS or CFDCDTSTS.CFDMASTS bit. See Figure 32.34 for the DMA disable flow. When the DMA is disabled, consideration should be made for the remaining or new incoming messages to this particular reception FIFO.

When the FIFO is not disabled, reception to the FIFO continues.

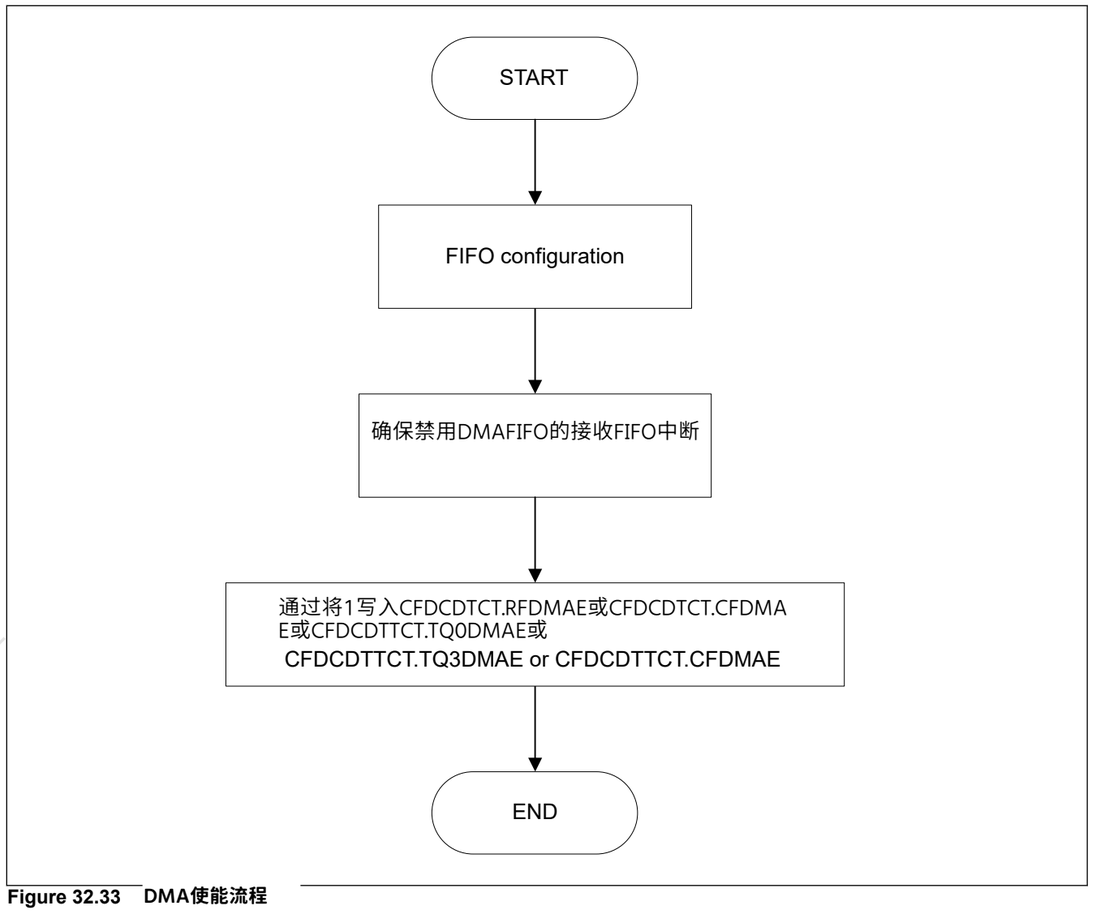


Figure 32.33 DMA使能流程

要禁用DMA传输请求，您必须禁用特定的DMA启用位（CFDCDTCT.RFDMAE或CFDCDTCT.CFDMAE)。如果在正在进行的传输过程中进行了禁用，则必须先完成传输，然后才能采取进一步的操作。传输状态可以通过CFDCDTSTS.RFDMASTS或CFDCDTSTS.CFDMASTS位来识别。有关DMA禁用流程，请参见图32.34。禁用DMA时，应考虑到此特定接收FIFO的剩余或新传入消息。

当FIFO未被禁用时，继续接收FIFO。

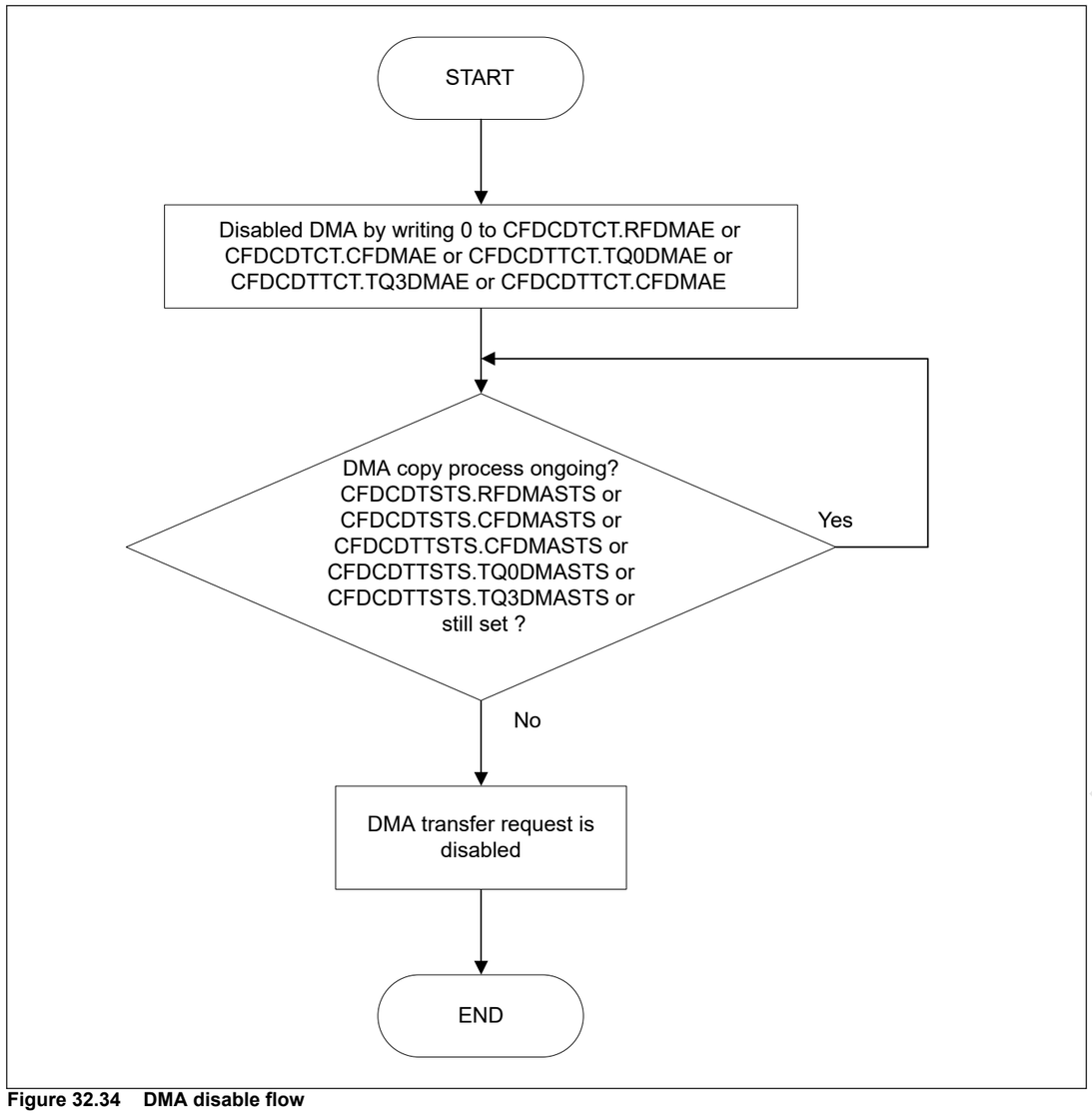


Figure 32.34 DMA disable flow

32.8 Reception and Transmission

32.8.1 Reception

In the CAN-FD module, CAN messages received on any of the channels are stored in RX message buffers, RX FIFO buffers, or Common FIFO buffers configured in RX mode or GW mode depending on the Acceptance Filter List entries.

- Up to 32 RX message buffers can be configured
- 8 RX FIFO buffers available
- Up to 6 Common FIFO buffers can be configured in RX mode or GW mode
- Up to 4 TX Queue can be configured in GW mode.

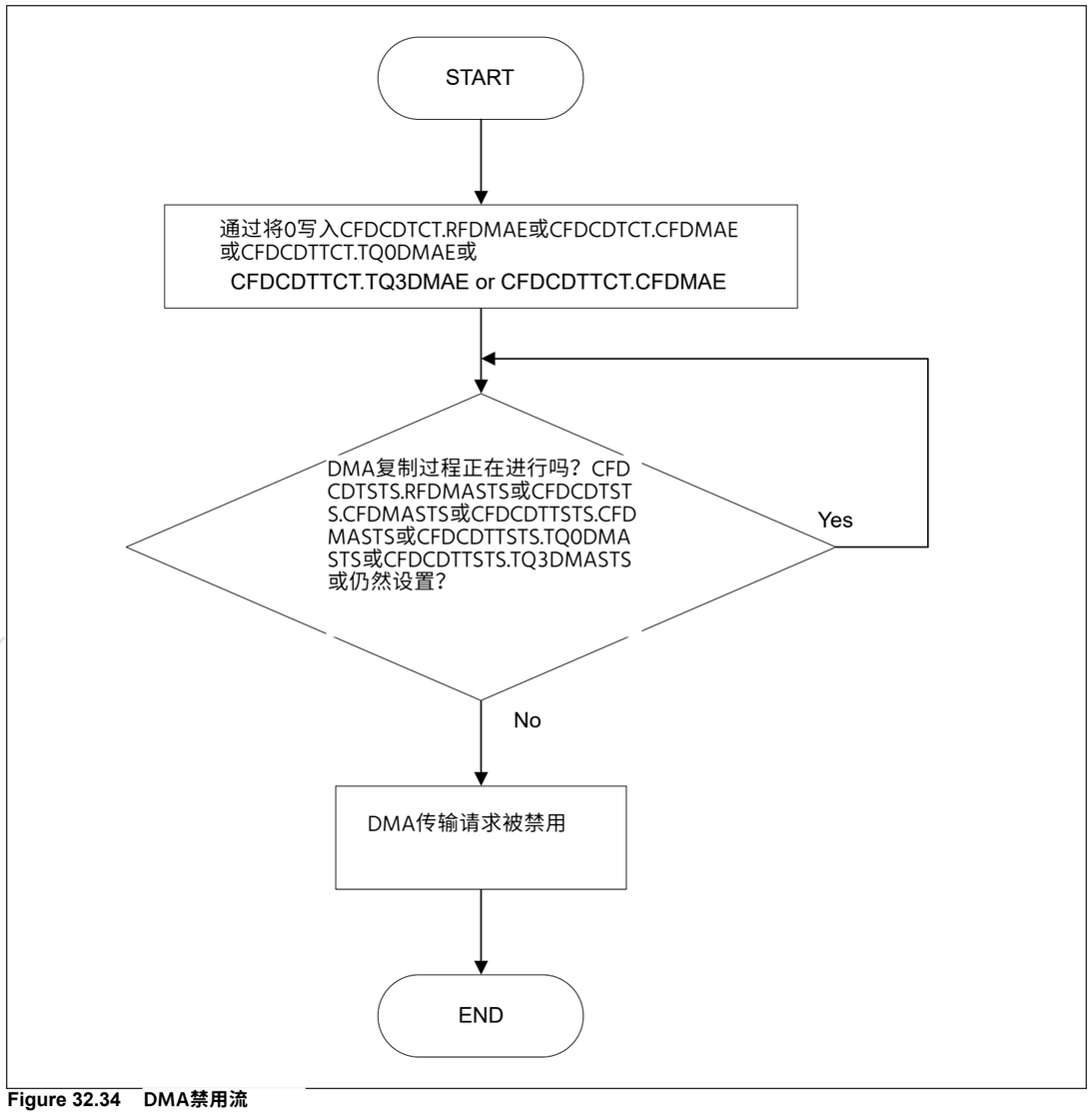


Figure 32.34 DMA禁用流

32.8 接收和传输

32.8.1 Reception

在CAN-FD模块中，在任何通道上接收到的CAN消息都存储在RX消息缓冲区、RXFIFO缓冲区或配置为RX模式或GW模式的CommonFIFO缓冲区中，具体取决于AcceptanceFilterList条目。

- ●最多可配置32个RX报文缓冲区
- ●8个RXFIFO缓冲器可用
- ●RX模式或GW模式下最多可配置6个CommonFIFO缓冲区
- ●GW模式下最多可以配置4个TXQueue。

32.8.1.1 Message Storage in RX Message Buffers

When a message is successfully received and stored in a RX message buffer, the corresponding New Data flag is set in the RX Message Buffer New Data Register.

The CAN message can be read from the corresponding RX message buffer.

If a new message is stored into a RX message buffer before the previous message in this message buffer can be read, then the original message is overwritten. There is no mechanism for preventing a new message from overwriting the current message in the RX message buffer. If such a loss of messages is not acceptable, then RX FIFO should be used for storing related messages.

Note: Interrupts are not provided for the RX message buffers in the CAN-FD module and therefore, the RX Message Buffer New Data Registers should be accessed periodically to check if a new message has been stored in the RX message buffers.

Note: Unused data bytes are filled with 0x00 depending on the DLC value.

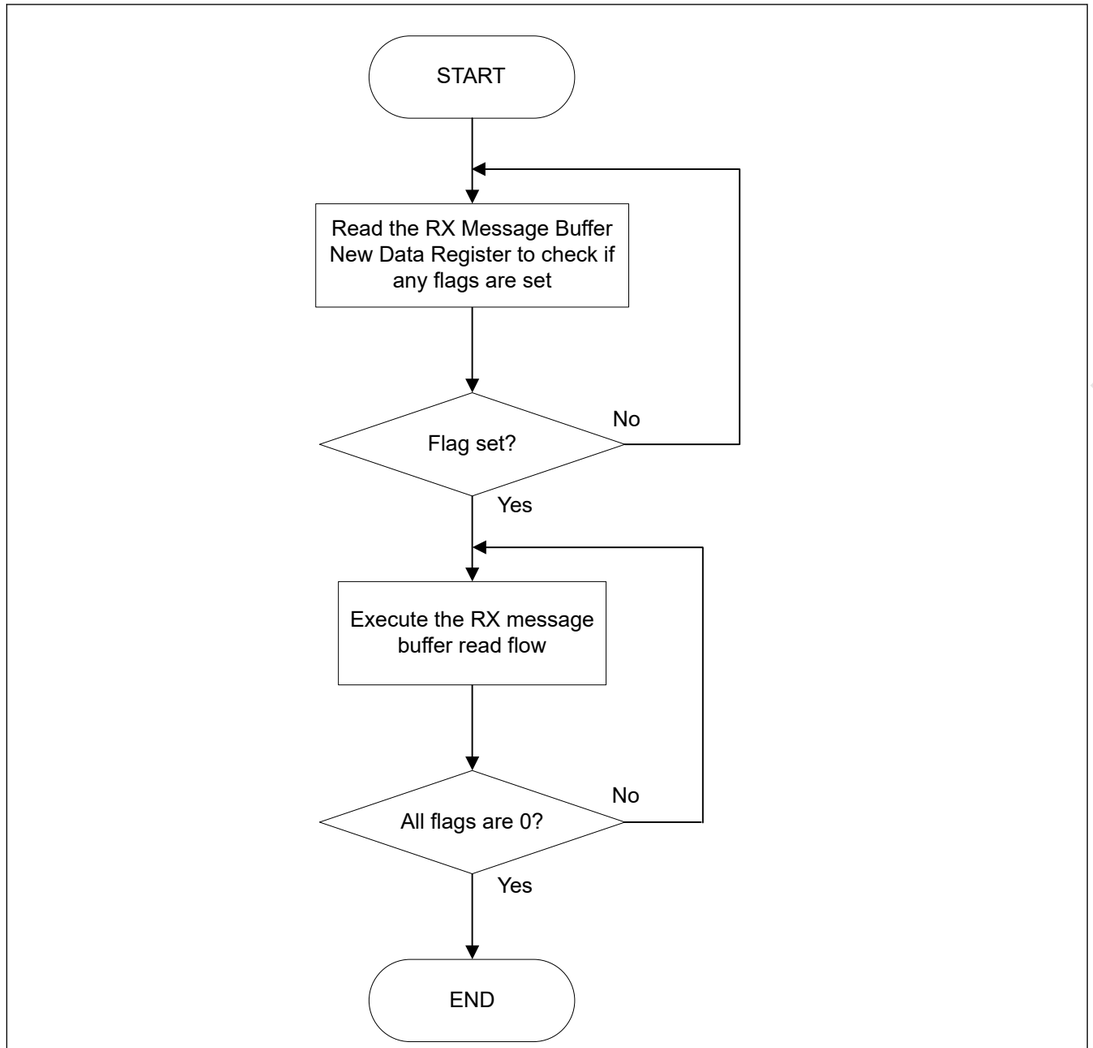


Figure 32.35 Access flow of RX message buffer

32.8.1.1 RX消息缓冲区中的消息存储

当消息被成功接收并存储在RX消息缓冲区中时，相应的NewData标志在RX消息缓冲区新数据寄存器。

CAN报文可以从相应的RX报文缓冲区中读取。

如果在可以读取此消息缓冲区中的前一个消息之前将新消息存储到RX消息缓冲区中，则原始消息将被覆盖。没有机制可以防止新消息覆盖RX消息缓冲区中的当前消息。如果这样的消息丢失是不可接受的，则应使用RXFIFO来存储相关消息。

Note: CAN-FD模块中的RX消息缓冲区没有提供中断，因此，RX消息应定期访问缓冲区新数据寄存器以检查新消息是否已存储在RX消息缓冲区中。

Note: 未使用的数据字节根据DLC值填充为0x00。

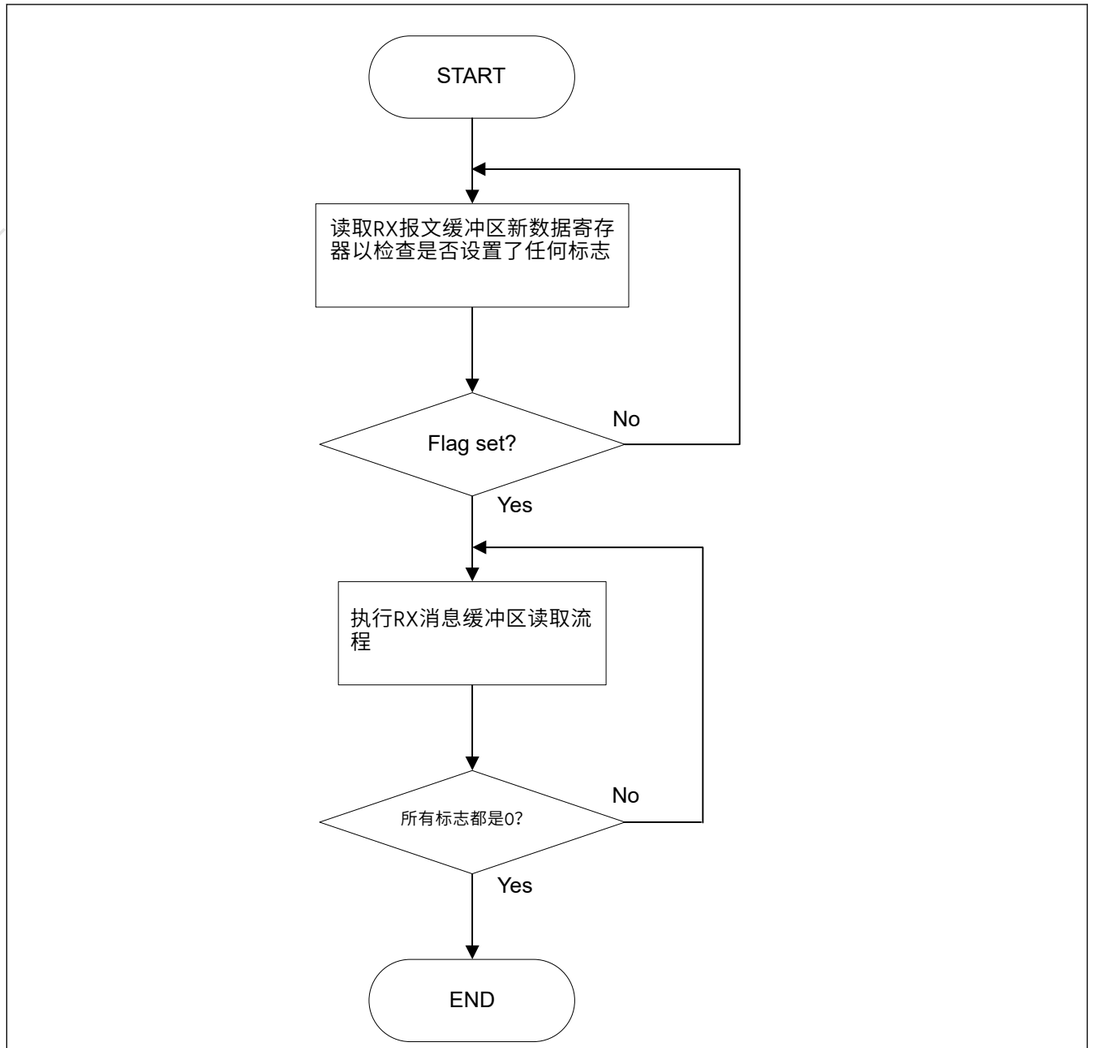


Figure 32.35 RX消息缓冲区的访问流程

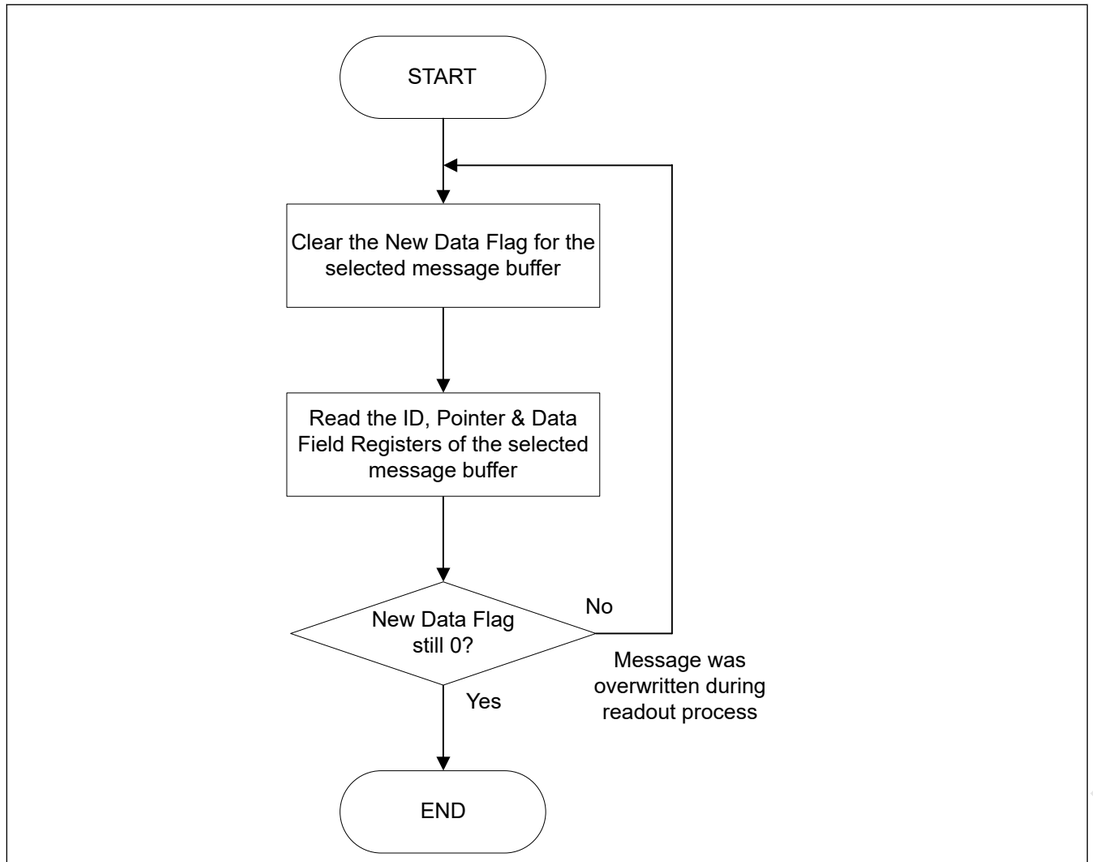


Figure 32.36 Read flow of RX message buffer

32.8.1.2 Message Storage in FIFO Buffers

The AFL entries for routing the received messages to RX FIFO buffers or Common FIFO buffers configured in RX or GW mode should be configured based on system requirements.

The CFDGAFLP1n.GAFLFDP[31:0] field in the matching AFL entry selects the FIFO buffers to which the related reception message is stored.

When the received message is stored in one or more RX FIFO buffers or Common FIFO buffers configured in RX mode or GW mode, the message counter value is incremented in the corresponding RX FIFO Status Registers or Common FIFO Status Registers.

Depending on the configuration of the FIFO buffers, an interrupt might also be generated.

The message can be read from the corresponding FIFO Access registers.

Note: Because many messages can be stored in the FIFO buffers, reading more than one message may be required to read the latest message stored in a FIFO buffer.

If the message count value matches the FIFO depth, the FIFO Full flag is set.

When the value 0xFF is written to the corresponding FIFO Pointer Control Register, the message count is decremented by 1.

Only write 0xFF to the FIFO Pointer Control register after reading the complete message from the FIFO Access registers of the corresponding FIFO.

When all the messages stored in the FIFO are read, the FIFO Empty flag is set.

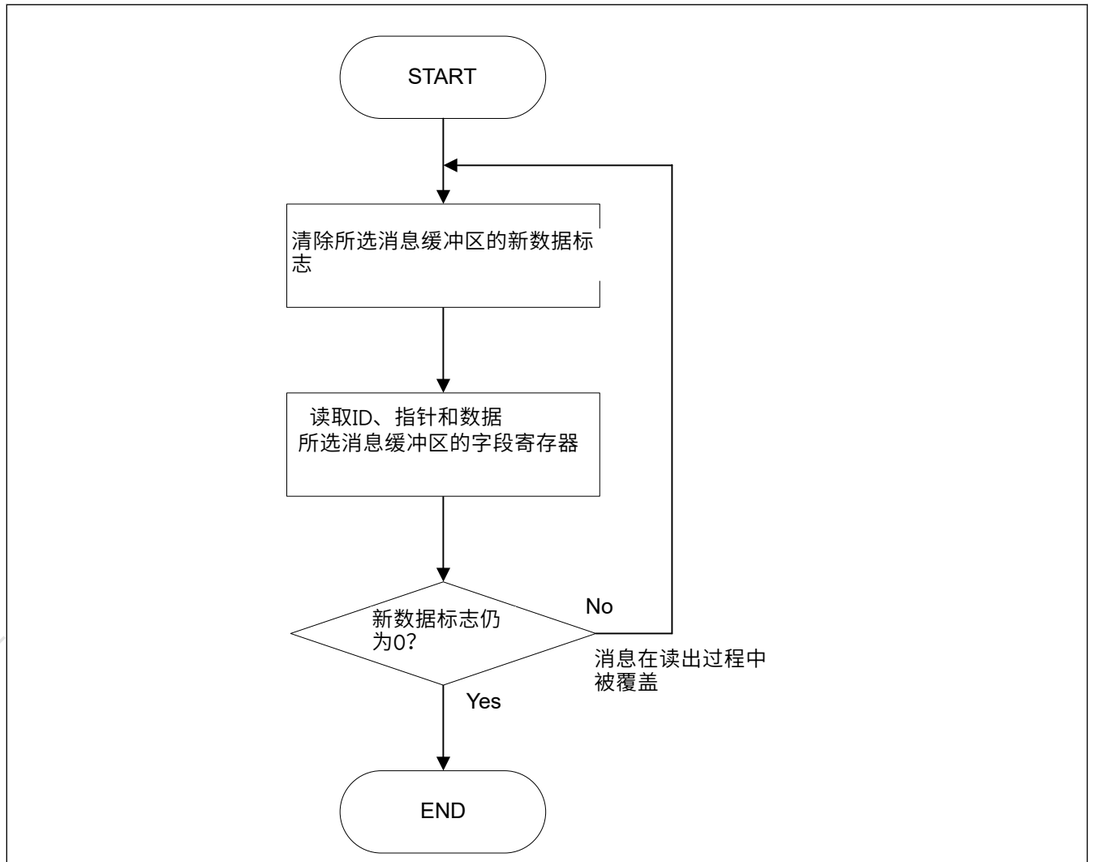


Figure 32.36 读取RX消息缓冲区的流程

32.8.1.2 FIFO缓冲区中的消息存储

用于将接收到的消息路由到RXFIFO缓冲区或配置为RX或GW模式的CommonFIFO缓冲区的AFL条目应根据系统要求进行配置。

匹配AFL条目中的CFDGAFLP1n.GAFLFDP[31:0]字段选择存储相关接收消息的FIFO缓冲区。

当接收到的报文存储在一个或多个RXFIFO缓冲区或配置为RX模式的CommonFIFO缓冲区时，或GW模式，消息计数器值在相应的RXFIFO状态寄存器或CommonFIFO中递增状态寄存器。

根据FIFO缓冲区的配置，也可能会产生中断。

该消息可以从相应的FIFO访问寄存器中读取。

Note: 因为许多消息可以存储在FIFO缓冲区中，所以可能需要读取多个消息才能读取存储在FIFO缓冲区中的最新消息。

如果消息计数值与FIFO深度匹配，则设置FIFO满标志。

当值0xFF写入相应的FIFO指针控制寄存器时，消息计数减1。

仅在从相应FIFO的FIFO访问寄存器中读取完整报文后，将0xFF写入FIFO指针控制寄存器。

当读取存储在FIFO中的所有消息时，设置FIFOEmpty标志。

If a new message is stored into the FIFO when the FIFO message count matches the FIFO depth (FIFO full condition), the FIFO Message Lost flag is set and the new message is lost (no overwrite of already stored messages takes place).

An appropriate value can be configured as warning level to generate an interrupt before the FIFO full condition occurs to avoid loss of a message due to an overrun condition.

In GW mode, when a transmit/receive FIFO buffer is receiving a new message while the transmit/receive FIFO buffer is already full of data, the oldest data of the buffer is overwritten with the message received or the message is discarded. The behavior is determined by setting CFDCFCCEn.CFMOWM bit.

- When CFDCFCCEn.CFMOWM = 0:
  When writing data is required due to reception of a new message while a transmit/receive FIFO buffer is full of data, the received message is discarded and the CFDCFSTSn.CFMLT bit is set to 1.

- When CFDCFCCEn.CFMOWM = 1:
  When writing data is required due to reception of a new message while a transmit/receive FIFO buffer is full of data, the oldest data in the buffer is overwritten with the received message.
  The read pointer of the transmit/receive FIFO buffer simultaneously moves to the next oldest message.
  The CFDCFSTSn.CFMOW bit is set to 1, which notifies that the oldest message has been overwritten with the received message.
  In addition, when a CAN bus error or arbitration-lost for the transmitting message occurs in the transmit/receive FIFO buffer full, the transmitting message is lost and retransmission for the message is not performed. The read point moves to the next message automatically.

Do not modify this bit when the CFDCFCCn.CFE bit is 1.

Common FIFO can set the interrupt when CAN frame reception is completed.

Common FIFO can set the interrupt when FIFO is in full status in RX mode or GW mode.

Note: The message lost can be set only in RX or GW mode by CAN, and the flag is not set when the CPU is overloading the FIFO buffers.

Note: When CFDGAFLP0n.GAFLSRD i (i = 0 to 2) is set and the CFDTXQCCin.TXQGWE (i = 0 to 2, n = 0 to 7) is also set, a receiving frame is stored in the target TXQ as send data by routing.

The RX FIFO buffers and the Common FIFO buffers configured in RX or GW mode can be disabled at any time by clearing the CFDRFCCn.RFE or CFDCFCCn.CFE bit in the RX FIFO Configuration/Control Registers and the Common FIFO Configuration/Control Registers.

When the CFDRFCCn.RFE or CFDCFCCn.CFE bit is cleared, the message read and write pointers of the FIFO are cleared and are no longer active. Therefore, all messages in the FIFO buffers are lost and no further messages can be stored into the FIFO.

When the RX FIFO buffers or Common FIFO buffers configured in RX mode is assigned as a DMA channel, software should not access the FIFO Access Register of this FIFO buffer or write 0xFF to the FIFO Pointer Control Register (CFDCFPCTRn.CFPC or CFDRFPCTRn.RFPC). This can lead to unintended FIFO message decrement. The DMA channel controls the FIFO decrement automatically.

Note: If the interrupt flag is set for a FIFO buffer and then the FIFO is disabled, the interrupt flag is not cleared automatically. The interrupt flag should be cleared before disabling the FIFO.

如果在FIFO消息计数与FIFO深度匹配（FIFO满状态）时将新消息存储到FIFO，则
FIFO消息丢失标志被设置，新消息丢失（不会覆盖已存储的消息）。

可以将适当的值配置为警告级别，以在FIFO满情况发生之前生成中断，以避免由于溢出情况而丢失消息。

在GW模式下，当发送接收FIFO缓冲区正在接收新消息而发送接收FIFO缓冲区已满数据时，缓冲区中最旧的数据将被接收到的消息覆盖或丢弃该消息。该行为由设置CFDCFCCEn.CFMOWM位决定。

- When CFDCFCCEn.CFMOWM = 0:
  当发送接收FIFO缓冲区已满数据而由于接收到新报文而需要写入数据时，将丢弃接收到的报文并将CFDCFSTSn.CFMLT位设置为1。

- When CFDCFCCEn.CFMOWM = 1:
  当发送接收FIFO缓冲区已满数据时，由于接收到新报文而需要写入数据时，缓冲区中最旧的数据将被接收到的报文覆盖。发送接收FIFO缓冲区的读指针同时移动到下一个最旧的消息。

  CFDCFSTSn.CFMOW位设置为1，表示最旧的消息已被接收的消息覆盖。此外，当发送接收FIFO缓冲区已满时发生CAN总线错误或发送报文仲裁丢失时，发送报文将丢失，并且不执行报文重传。阅读点自动移动到下一条消息。

当CFDCFCCn.CFE位为1时不要修改该位。

普通FIFO可以在CAN帧接收完成时设置中断。

CommonFIFO可以在RX模式或GW模式下FIFO处于满状态时设置中断。

Note: 消息丢失只能由CAN在RX或GW模式下设置，并且当CPU使FIFO缓冲区过载时不设置该标志。

Note: 当CFDGAFLP0n.GAFLSRDi(i=0to2)被设置并且CFDTXQCCin.TXQGWE(i=0to2 n=0to7)也被设置时，接收帧被存储在目标TXQ作为路由发送数据.

通过清除RXFIFO配置控制寄存器和通用FIFO配置控制寄存器中的CFDRFCCn.RFE或CFDCFCCn.CFE位，可以随时禁用在RX或GW模式下配置的RXFIFO缓冲区和通用FIFO缓冲区。

当CFDRFCCn.RFE或CFDCFCCn.CFE位被清零时，FIFO的报文读写指针被清零，不再处于活动状态。因此，FIFO缓冲区中的所有消息都将丢失，并且无法将更多消息存储到FIFO中。

当在RX模式下配置的RXFIFO缓冲区或通用FIFO缓冲区被分配为DMA通道时，软件不应访问该FIFO缓冲区的FIFO访问寄存器或将0xFF写入FIFO指针控制寄存器（CFDCFPCTRn.CFPC或CFDRFPCTRn.RFPC）.这可能导致意外的FIFO消息递减。DMA通道自动控制FIFO递减。

Note: 如果为FIFO缓冲区设置了中断标志，然后禁用了FIFO，则不会自动清除中断标志。在禁用FIFO之前应清除中断标志。

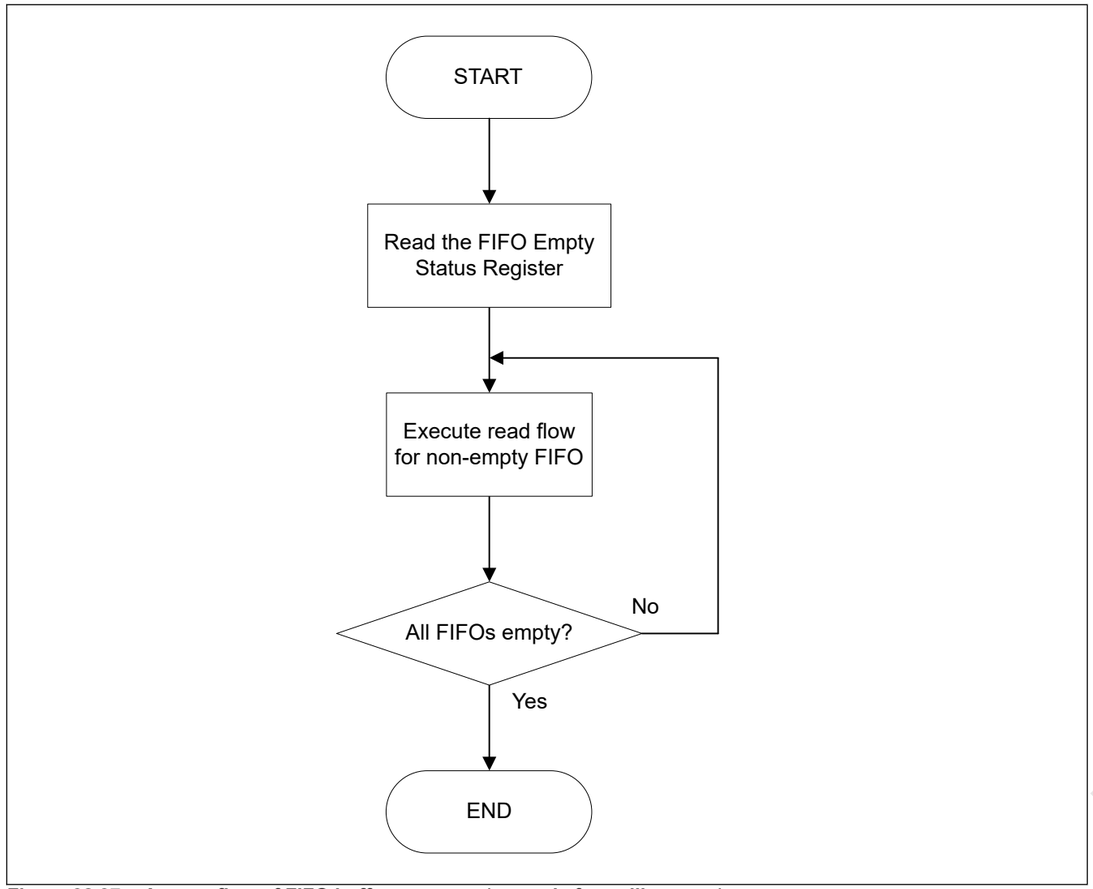


Figure 32.37 Access flow of FIFO buffer message (example for polling case)

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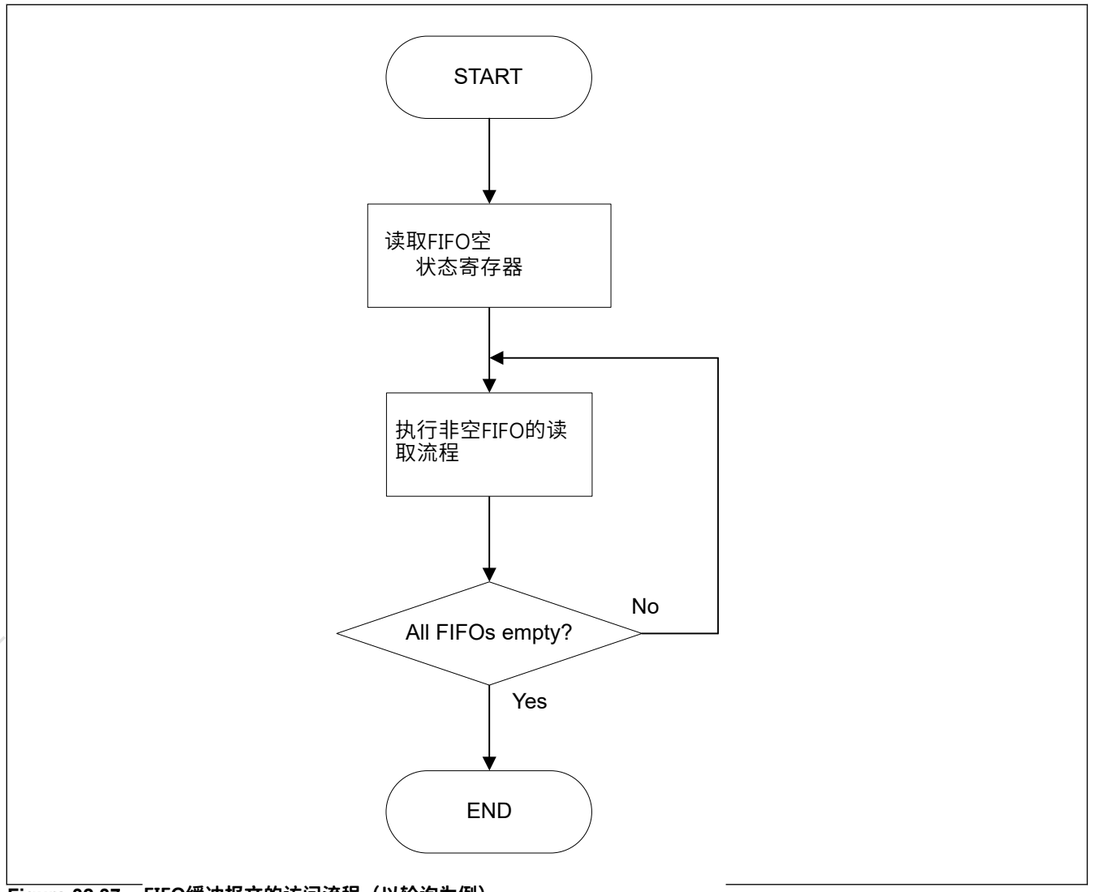

Figure 32.37 FIFO缓冲报文的访问流程（以轮询为例）

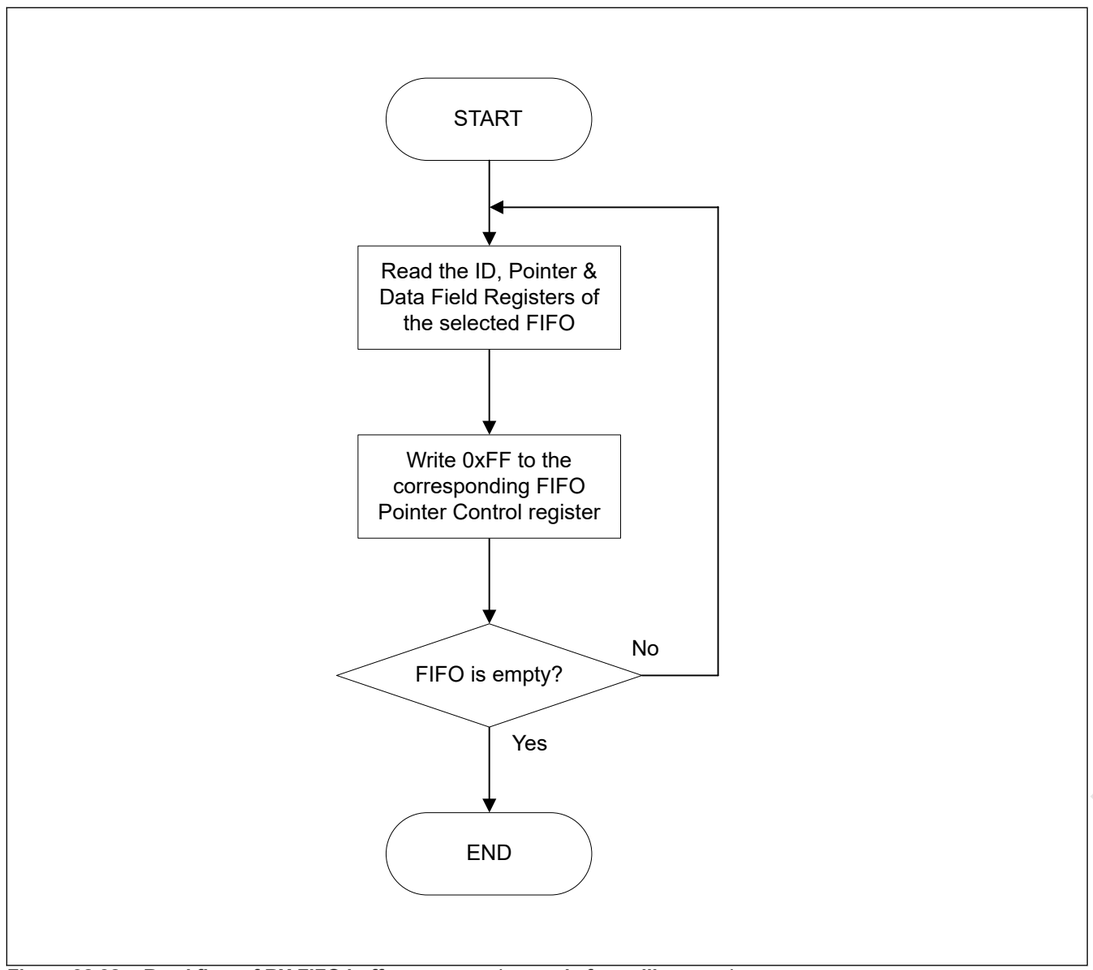

Figure 32.38 Read flow of RX FIFO buffer message (example for polling case)

Note: When the next frame is received before clearing the completion interrupt flag of reception, the completion interrupt of reception is not set again.

Even when an interruption flag is cleared after the completion processing of reception, the already received interrupt flag is not set.

It is necessary to perform the completion processing of reception even before the next completion of frame reception, and to clear an interruption flag.

When processing does not meet the condition, after checking that receiving data is empty, interrupt flag is cleared and it checks that receiving data is empty again.

32.8.1.3 Timestamp

The timestamp counter is a free-running counter that can be used to check reception time of an incoming message or transmission time of successful transmitted messages. The Timestamp counter value is captured based on the CFDGFDCFG.TSCCFG[1:0] configuration (at the sample point of start of frame, point in time when the frame is valid, or for CAN-FD frames also at the sample point of the RES bit). For reception, it is stored together with the message ID and data into the target RX message buffer or RX/GW FIFO.

For transmit message, the timestamp counter value is stored as part of the TX History List entry.

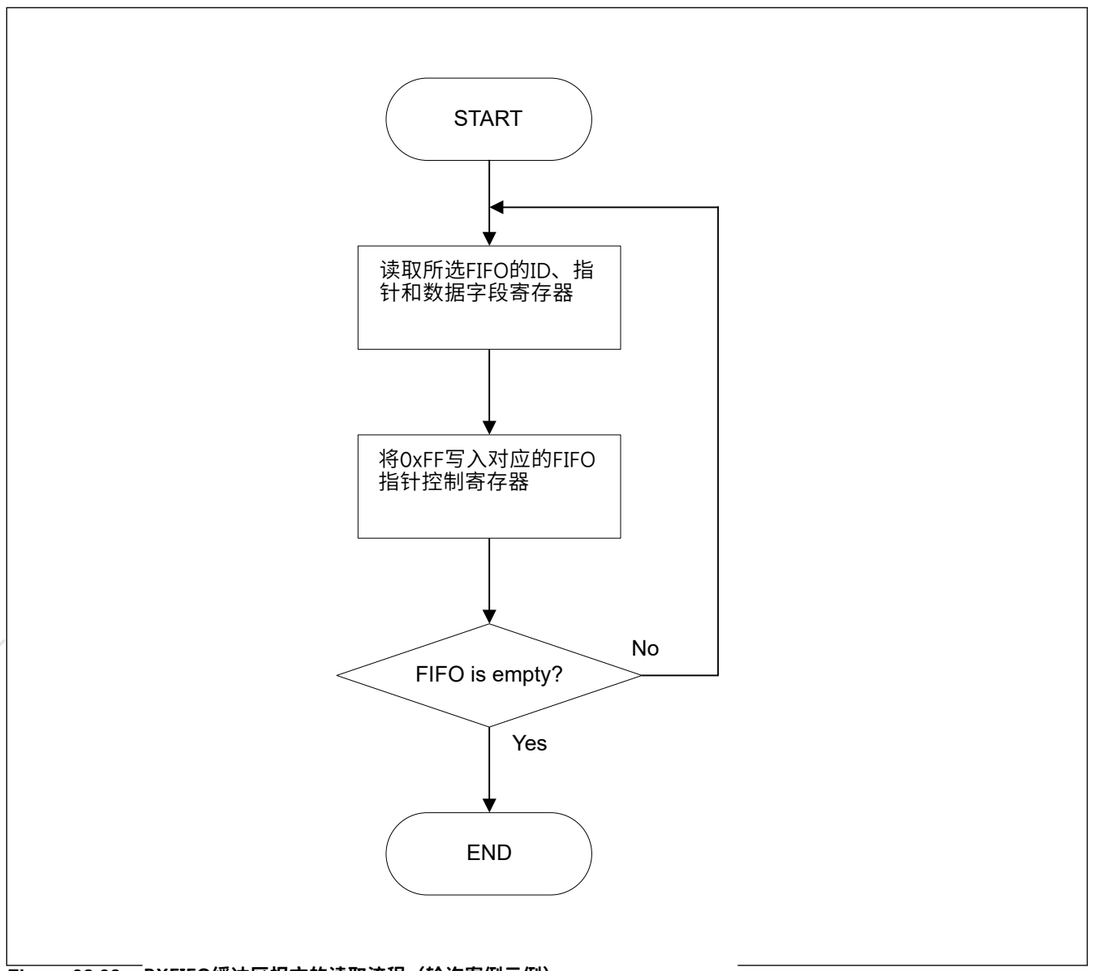

Figure 32.38 RXFIFO缓冲区报文的读取流程（轮询案例示例）

Note: 在清除接收完成中断标志之前接收到下一帧时，不再设置接收完成中断。

即使在接收完成处理后清除中断标志，已接收中断标志也不会置位。

甚至在下一次帧接收完成之前也需要执行接收完成处理，并清除中断标志。

当处理不满足条件时，检查接收数据为空后，清除中断标志，再次检查接收数据是否为空。

32.8.1.3 Timestamp

时间戳计数器是一个自由运行的计数器，可用于检查传入消息的接收时间或成功传输消息的传输时间。Timestamp计数器值基于CFDGFDCFG.TSCCFG[1:0]配置（在帧开始的采样点、帧有效的时间点或CAN-FD帧的采样点）捕获。RES位）。对于接收，它与消息ID和数据一起存储到目标RX消息缓冲区或RXGWFIFO中。

对于发送消息，时间戳计数器值存储为TX历史列表条目的一部分。

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The counter can be clocked with the peripheral clock or with the CAN channel bit timing clock. The counter source clock can be configured with the CFDGCFG.TSSS bit of the Global Configuration Register. If this bit is 0, the peripheral clock is used. If the bit is 1, the selected CAN channel bit time clock is used.

The channel selection is performed with the CFDGCFG.TSBTCS bit of the Global Configuration Register.

Care must be taken when using selected CAN channel bit time clock as the clock source. When entering Channel Halt mode or Channel Reset node, for this channel, the timestamp counter is stopped. For other CAN channels, the timestamp counter value is not updated.

If peripheral clock is selected as the timestamp counter clock source, Channel modes do not affect the timestamp counter function.

The source clock for the timestamp counter can be divided by a factor defined by the CFDGCFG.TSP bits (timestamp prescaler) in the Global Configuration Register.

The timestamp counter can be reset to 0x0000 with the CFDGCTR.TSRST bit (timestamp reset).

32.8.2 Transmission

There are several possible transmission configurations for each channel:

- Normal transmission
- FIFO transmission
- Gateway transmission
- TX Queue transmission
  A fixed number of transmission message buffers (16 TX message buffers) are dedicated for each channel. These message buffers are only used for transmission and cannot be configured for reception.
  Additionally transmission from TX Queue or Common FIFO in TX or GW mode can be configured in the following way (see Figure 32.39):
  – TX Queue: Up to eight transmission message buffers for one channel can be grouped to form a TX Queue with a common access window.
    Upper transmission message buffers are used to form the TXQ1 or TXQ3.
    Lower transmission message buffers are used to form the TXQ0 or TXQ2.
    Transmission Control and Status registers of these transmission message buffers should not be used.
    One channel has four TX Queues.
    Each TXQ has an access window.
    - TXQ0 is transmission Message Buffer 0 of each channel.
    - TXQ1 is transmission Message Buffer 7 of each channel.
    - TXQ2 is transmission Message Buffer 32 of each channel.
    - TXQ3 is transmission Message Buffer 39 of each channel.

    When using TXQ1 and TXQ0 simultaneously, the sum of the depths of TXQ1 and TXQ0 should not exceed 8.
    When using TXQ3 and TXQ2 simultaneously, the sum of the depths of TXQ3 and TXQ2 should not exceed 8.
- Common FIFO (TX/GW mode): each Common FIFO in TX or GW mode is linked to a dedicated channel.
  Each channel has a fixed number of three Common FIFOs assigned to it. Within the channel, a Common FIFO configured in TX or GW mode, can be freely linked (assigned) between 32 and 39 transmission message buffers (only one FIFO to one transmission message buffer).
  The Common FIFO buffer then replaces the transmission message buffer linked to it.
  Transmission Control and Status registers of these transmission message buffers should not be used.

See Figure 32.28 for information about Common FIFO buffer assignment to related channels.

Note: Common FIFO buffers should not be linked to TX message buffers that are already part of a TX Queue.

计数器可以使用外设时钟或CAN通道位定时时钟进行计时。计数器源时钟可以通过全局配置寄存器的CFDGCFG.TSSS位进行配置。如果该位为0，则使用外设时钟。如果该位为1，则使用选定的CAN通道位时钟。

通道选择通过全局配置寄存器的CFDGCFG.TSBTCS位执行。

使用选定的CAN通道位时钟作为时钟源时必须小心。当进入ChannelHalt模式或ChannelReset节点时，对于该通道，时间戳计数器停止。对于其他CAN通道，时间戳计数器值不会更新。

如果选择外设时钟作为时间戳计数器时钟源，通道模式不影响时间戳计数器功能。

时间戳计数器的源时钟可以除以全局配置寄存器中的CFDGCFG.TSP位（时间戳预分频器）定义的因子。

时间戳计数器可通过CFDGCTR.TSRST位（时间戳复位）复位为0x0000。

32.8.2 Transmission

每个通道有几种可能的传输配置：

●正常传输

- FIFO transmission

●网关传输

●TX队列传输
  固定数量的传输消息缓冲区（16个TX消息缓冲区）专用于每个通道。这些消息缓冲区仅用于传输，不能配置为接收。此外，在TX或GW模式下从TXQueue或CommonFIFO传输可以通过以下方式配置（参见图32.39）：
  TX队列：可以将一个通道的多达8个传输消息缓冲区分组，以形成具有公共访问窗口的TX队列。上部传输消息缓冲区用于形成TXQ1或TXQ3。较低的传输消息缓冲区用于形成TXQ0或TXQ2。

  不应使用这些传输消息缓冲区的传输控制和状态寄存器。
  一个通道有四个TX队列。每个
  TXQ都有一个访问窗口。
  - TXQ0是每个通道的传输消息缓冲区0。
  - TXQ1是每个通道的传输报文缓冲器7。
  - TXQ2是每个通道的传输消息缓冲器32。
  - TXQ3是每个通道的传输消息缓冲器39。

  当同时使用TXQ1和TXQ0时，TXQ1和TXQ0的深度之和不应超过8。当同时使用TXQ3和TXQ2时，TXQ3和TXQ2的深度之和不应超过8。

●CommonFIFO（TXGW模式）：TX或GW模式下的每个CommonFIFO都链接到一个专用通道。
  每个通道都分配有固定数量的三个通用FIFO。在通道内，配置为TX或GW模式的CommonFIFO可以在32和39个传输消息缓冲区之间自由链接（分配）（只有一个FIFO到一个传输消息缓冲区）。通用FIFO缓冲区然后替换链接到它的传输消息缓冲区。

  不应使用这些传输消息缓冲区的传输控制和状态寄存器。

有关分配给相关通道的通用FIFO缓冲区的信息，请参见图32.28。

Note: 公共FIFO缓冲区不应链接到已经是TX队列一部分的TX消息缓冲区。

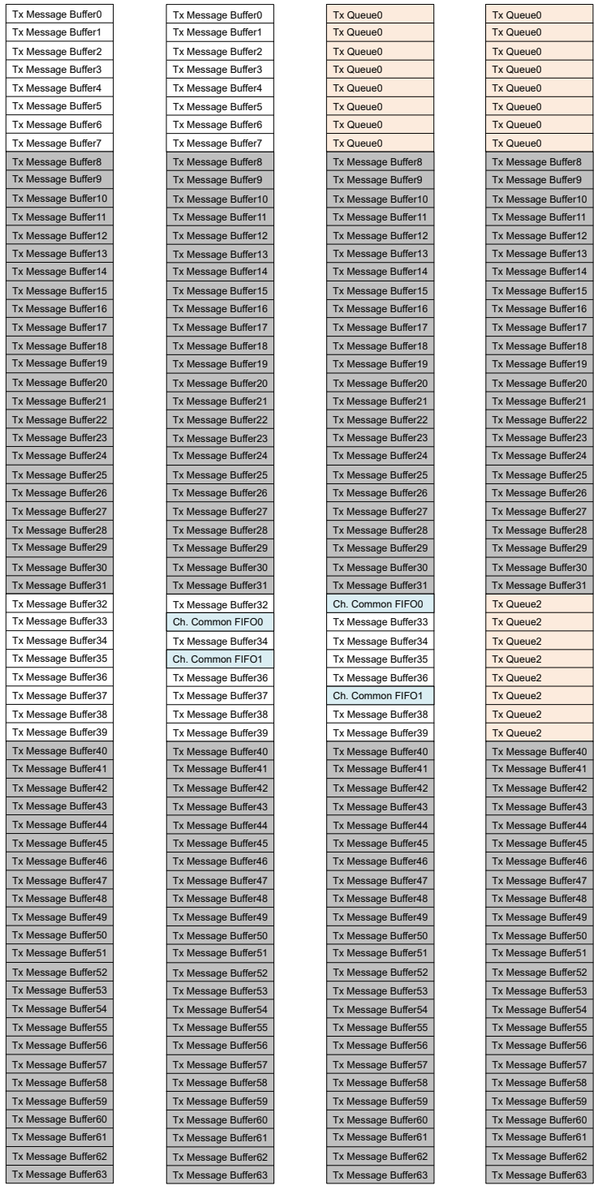

Figure 32.39 Configuration of channel transmission message buffer

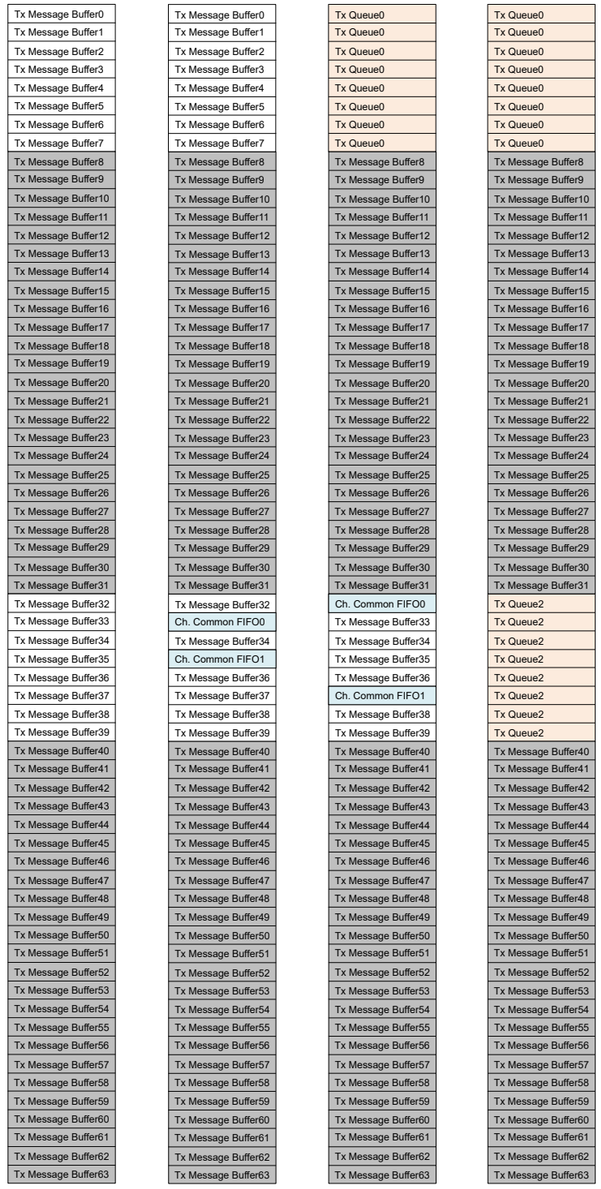

Figure 32.39 通道传输消息缓冲区的配置

32.8.2.1 Transmission Priority

If two or more transmission message buffers of a channel are configured for transmission, then the transmission priority in the CAN-FD module can be selected from the following two modes:

- CAN ID priority
- Message buffer number priority.

The transmission priority mode is common for all message buffers and all CAN channels. It can be configured with the CFDGCFG.TPRI bit in the Global Configuration Register.

For message buffer number priority transmission, the smallest message buffer number with transmission request has the highest priority for transmission. This also includes the TX message buffers linked to the Common FIFO buffers configured in TX mode or GW mode.

However, message buffer number priority should not be used if TX Queue is enabled.

For CAN ID priority transmission, ID priority complies with the CAN bus arbitration rule (as specified in ISO 11898-1 specification). All TX message buffers can enter the ID priority comparison for message buffers configured for transmission. This also includes the TX message buffers linked to the Common FIFO buffers configured in TX mode or GW mode and includes the TX Queue message buffers.

If the ID of two or more message buffers is the same, then the smaller message buffer number has higher priority for transmission.

Note: For Common FIFO buffers configured in TX mode or GW mode, only the message currently being pointed to by the FIFO read pointer can be included in the transmission arbitration.

If the message is being transmitted from the FIFO, then the next pending message within the same FIFO is considered in the transmission arbitration.

In contrast to this, all transmission message buffers of a TX Queue participate in internal transmission arbitration.

Figure 32.40 shows the transmission configuration flow.

32.8.2.1 传输优先级

如果配置了一个通道的两个或多个传输报文缓冲区进行传输，则CAN-FD模块中的传输优先级可以从以下两种模式中选择：

- CANID优先级
- 消息缓冲区编号优先级。

传输优先模式对于所有消息缓冲区和所有CAN通道都是通用的。它可以配置为全局配置寄存器中的CFDGCFG.TPRI位。

对于消息缓冲区号优先传输，具有传输请求的最小消息缓冲区号具有最高传输优先级。这还包括链接到在TX模式或GW模式下配置的CommonFIFO缓冲区的TX消息缓冲区。

但是，如果启用了TXQueue，则不应使用消息缓冲区编号优先级。

对于CANID优先级传输，ID优先级符合CAN总线仲裁规则（在ISO11898-1规范中指定）。所有TX报文缓冲区都可以进入配置为传输的报文缓冲区的ID优先级比较。这还包括链接到在TX模式或GW模式下配置的Common FIFO缓冲区的TX消息缓冲区，并包括TXQueue消息缓冲区。

如果两个或多个消息缓冲区的ID相同，则较小的消息缓冲区号具有较高的传输优先级。

Note: 对于配置为TX模式或GW模式的CommonFIFO缓冲区，只有当前由FIFO读指针可以包含在传输仲裁中。

如果消息是从FIFO传输的，则在传输仲裁中考虑同一FIFO中的下一个待处理消息。

与此相反，TXQueue的所有传输消息缓冲区都参与内部传输仲裁。

图32.40显示了传输配置流程。

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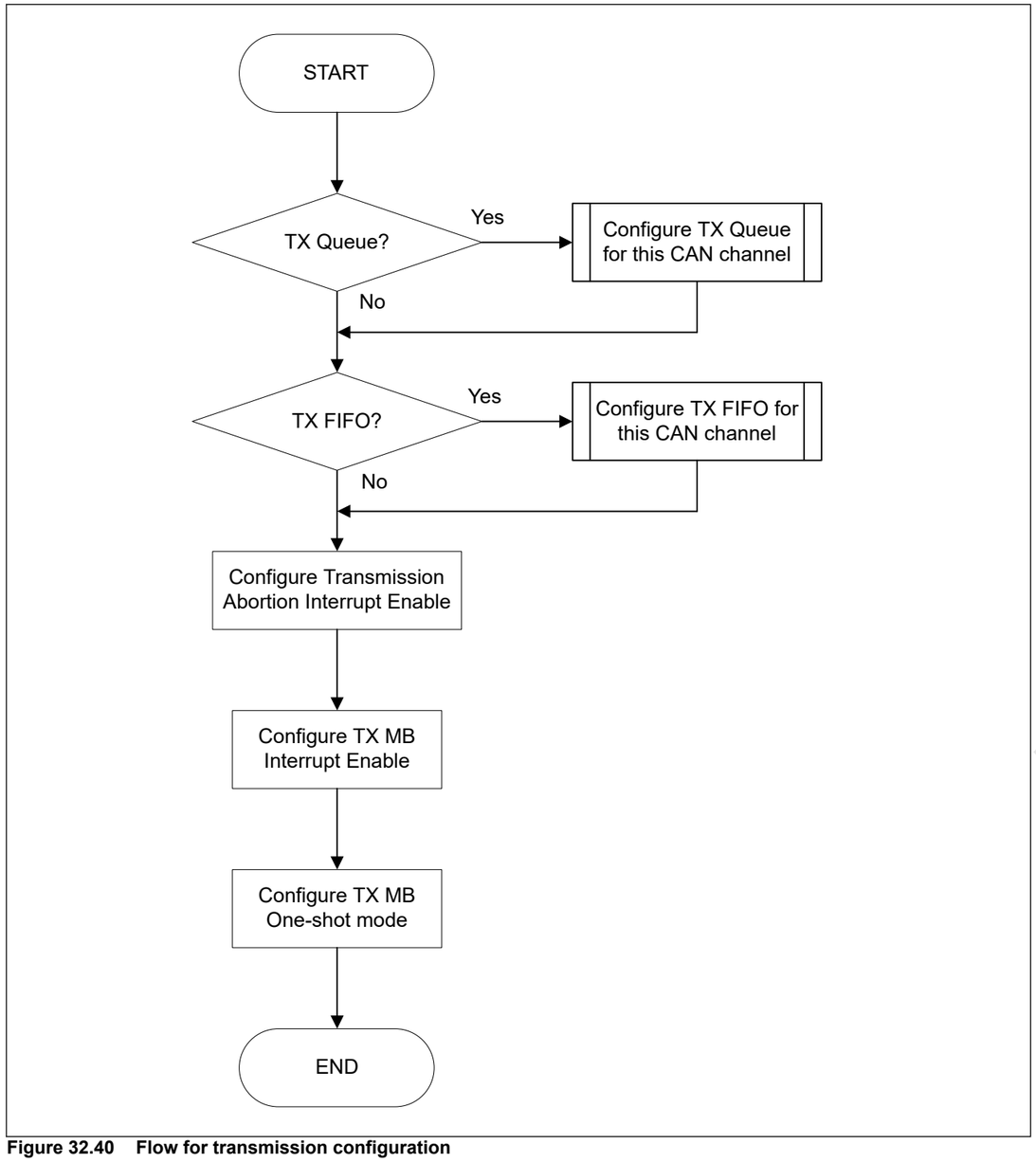

Figure 32.40 Flow for transmission configuration

32.8.2.2 Normal Transmission

Each transmission message buffer has two modes of message transmission:

1. Regular transmission mode
   If the message buffer is placed in regular transmission mode, the data frame or remote frame set in that message buffer can be transmitted.
   Completion of regular transmission can be checked through the related TX Message Buffer Transmission Result flag bits (CFDTMSTSn.TMTRF) in the TX Message Buffer Status Registers. These bits are set to 10b or 11b when the regular transmission is successful.

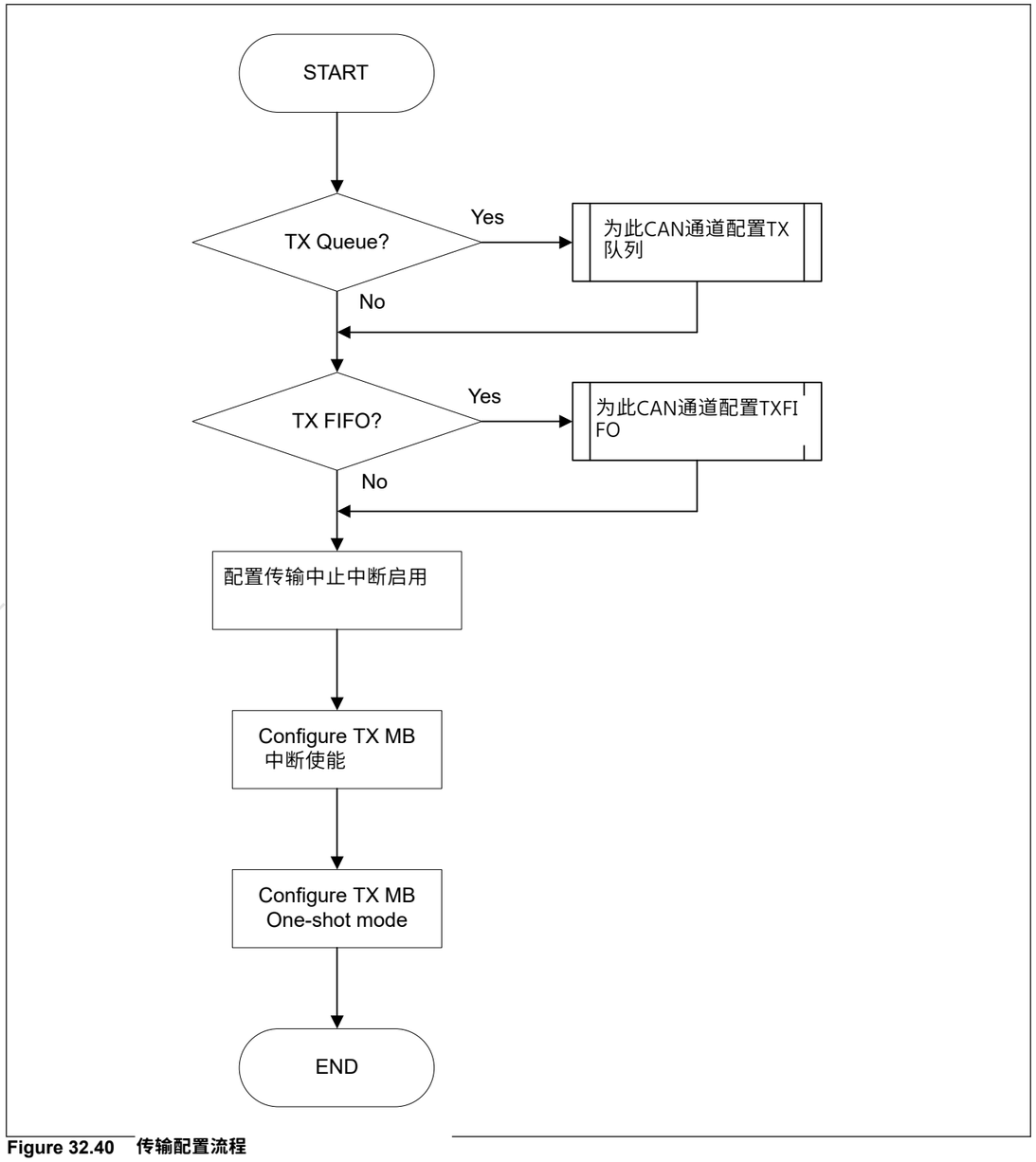

Figure 32.40 传输配置流程

32.8.2.2 正常传输

每个传输消息缓冲区有两种消息传输模式：

1.常规传输方式
   如果将消息缓冲区置于常规传输模式，则可以传输该消息缓冲区中设置的数据帧或远程帧。可以通过TX报文缓冲区状态寄存器中的相关TX报文缓冲区传输结果标志位(CFDTMSTSn.TMTRF)来检查是否完成了定期传输。当常规传输成功时，这些位设置为10b或11b。

When arbitration is lost or an error occurs, message transmission is further attempted if no transmission abort request is set for this transmission message buffer.
New internal transmission arbitration for this channel is performed for all message buffers with transmission request.

2. One-shot transmission mode

When the CFDTMCn.TMOM bit of the TX Message Buffer Control Registers is set for a transmission message buffer, the message buffer is placed in One-shot transmission mode and attempts to transmit a message only once.

Completion of One shot transmission can be checked through the related TX Message Buffer Transmission Result Flag bits (CFDTMSTSn.TMTRF) in the TX Message Buffer Status Registers. The CFDTMSTSn.TMTRF bits are set to 10b or 11b when One-shot transmission is successful.

The CFDTMSTSn.TMTRF bits are set to 01b when arbitration is lost or an error occurs during transmission of the related message buffer.

Additional message transmission is not attempted in this case.

The regular transmission request procedure after a configuration is shown in Figure 32.41.

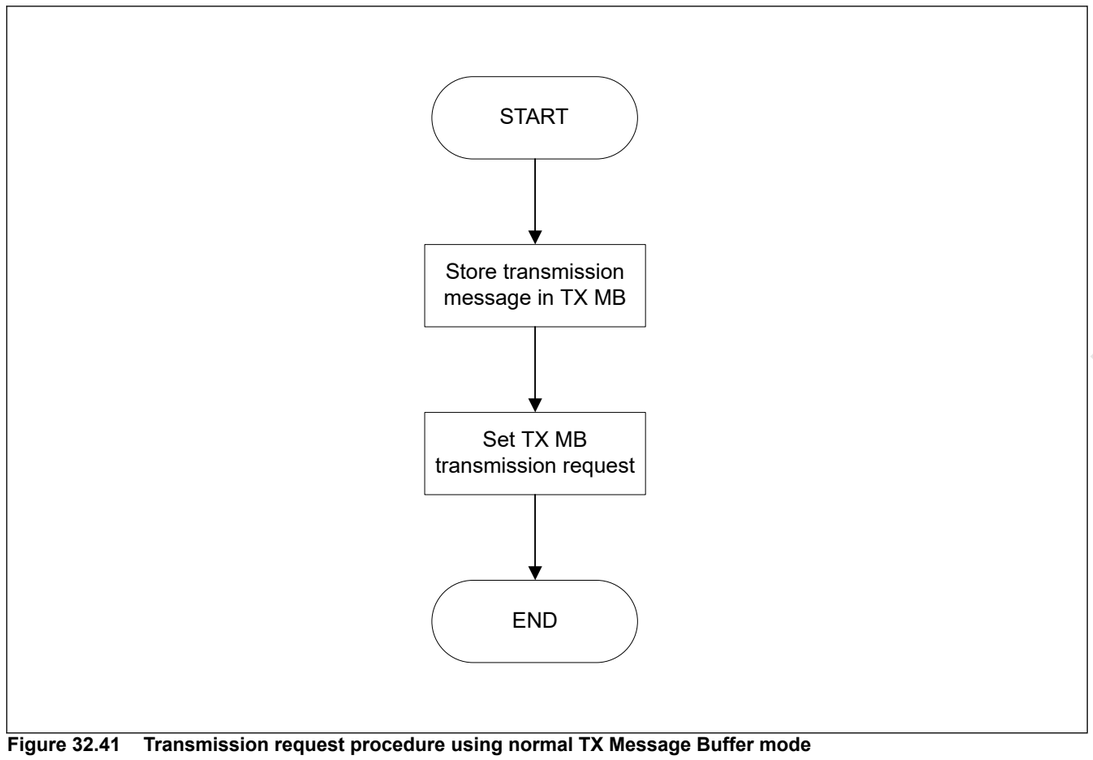

Figure 32.41 Transmission request procedure using normal TX Message Buffer mode

(1) Setting for TX Message Buffer Control Register

Table 32.21 shows configuration of a normal CAN transmission mode.

Table 32.21 Configuration of CAN transmission mode (1 of 2)

Transmission request CFDTMCn.TMTR	Transmission abort request CFDTMCn.TMTAR	One-shot enable CFDTMCn.TMOM	Communication activity
0	0	0	Message buffer disabled
0	0	1	Message buffer disabled

当仲裁丢失或发生错误时，如果没有为此发送消息缓冲区设置发送中止请求，则进一步尝试发送消息。该通道的新内部传输仲裁针对所有具有传输请求的消息缓冲区执行。

2.一键传输模式

当TX报文缓冲区控制寄存器的CFDTMCn.TMOM位为发送报文缓冲区设置时，报文缓冲区被置于一次性发送模式，并且只尝试发送一次报文。

可以通过TX报文缓冲区状态寄存器中的相关TX报文缓冲区传输结果标志位(CFDTMSTSn.TMTRF)来检查一次性传输是否完成。当One-shot传输成功时，CFDTMSTSn.TMTRF位设置为10b或11b。

当仲裁丢失或在相关消息缓冲区的传输过程中发生错误时，CFDTMSTSn.TMTRF位设置为01b。

在这种情况下，不会尝试额外的消息传输。

配置后的常规传输请求流程如图32.41所示。

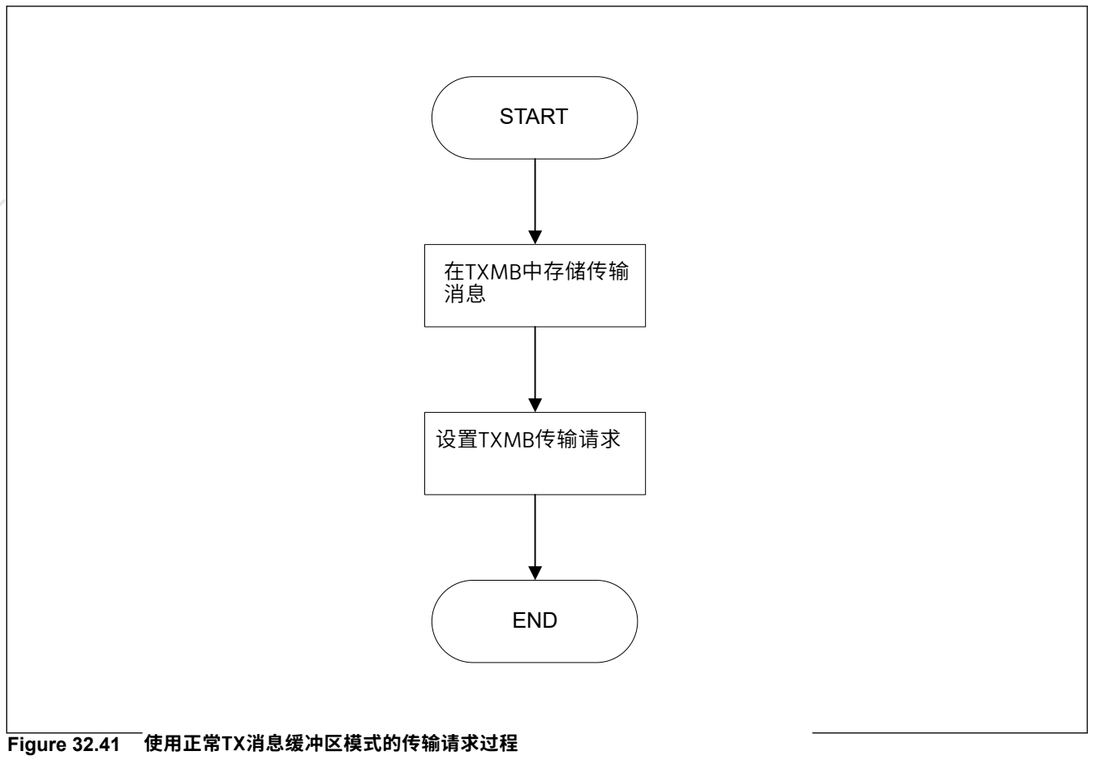

Figure 32.41 使用正常TX消息缓冲区模式的传输请求过程

(1) TX报文缓冲区控制寄存器的设置

表32.21显示了普通CAN传输模式的配置。

Table 32.21 CAN传输模式的配置（1of2）

传输请求 CFDTMCn.TMTR	传输中止请求 CFDTMCn.TMTAR	One-shot enable CFDTMCn.TMOM	通信活动
0	0	0	消息缓冲区已禁用
0	0	1	消息缓冲区已禁用

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Table 32.21 Configuration of CAN transmission mode (2 of 2)

Transmission request CFDTMCn.TMTR	Transmission abort request CFDTMCn.TMTAR	One-shot enable CFDTMCn.TMOM	Communication activity
1	0	0	Configured as a transmission message buffer for a data frame or a remote frame
1	0	1	Configured as a one-shot transmission message buffer for a data frame or a remote frame
1	1	0	Transmission abort requested
1	1	1	One-shot transmission abort requested

The configuration bits can be configured in the TX Message Buffer Control Registers.

Figure 32.42 shows timings for successful transmission for two message buffers of one channel.

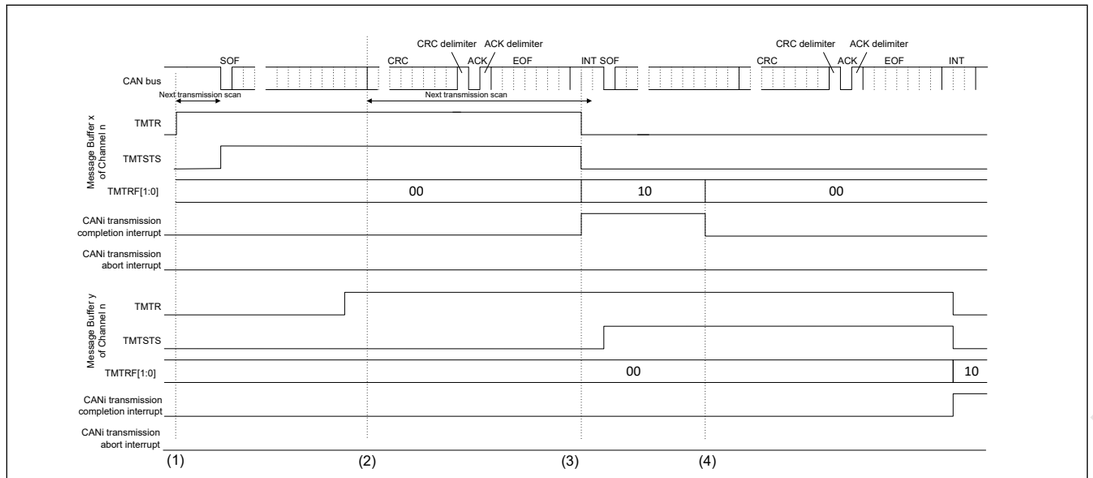

Figure 32.42 Timing of request and flag bits for successful transmission

1. If the CFDTMCn.TMTR bit in the TX Message Buffer Control Registers is set in the bus idle state, the message buffer scanning procedure determines the highest priority message buffer for transmission.
   When the transmission message buffer is determined, the CFDTMSTSn.TMTSTS bit in the related TX Message Buffer Status Registers is set (transmitting/transmitter), and CAN channel starts the transmission *1.
2. At the first bit of CRC, the transmission scanning procedure starts for the next possible transmission when pending transmission requests exist.
   The scan time can be delayed due to other transmission scan on other channels, but it finishes before intermission 3 to be able to continue transmission without any gaps.
3. If the message has been successfully transmitted, the CFDTMSTSn.TMTRF[1:0] bits in the corresponding TX Message Buffer Status Registers are set to 10b and CFDTMSTSn.TMTSTS and the CFDTMCn.TMTR bits are cleared.
   When the TMIE bit in the TX Message Buffer Interrupt Enable Configuration Registers is set (interrupt enabled), the CAN successful transmission interrupt request is generated.
   To clear the related interrupt line, clear the CFDTMSTSn.TMTRF flag bits.
4. Before starting the next transmission, clear the CFDTMSTSn.TMTRF bits. Load the next message in the transmission message buffer and set the CFDTMCn.TMTR bit again.
   CFDTMCn.TMTR bit cannot be set again before CFDTMSTSn.TMTRF[1:0] bits are cleared.

Note 1. If arbitration is lost after the CAN channel starts the transmission, the CFDTMSTSn.TMTSTS bit is cleared.
The transmission scanning procedure is performed again to search for the highest priority transmission message buffer from the beginning of the first CRC bit.

Table 32.21 CAN传输模式的配置（2of2）

传输请求 CFDTMCn.TMTR	传输中止请求 CFDTMCn.TMTAR	One-shot enable CFDTMCn.TMOM	通信活动
1	0	0	配置为数据帧或远程帧的传输消息缓冲区
1	0	1	配置为数据帧或远程帧的一次性传输消息缓冲区
1	1	0	请求传输中止
1	1	1	请求单发传输中止

配置位可以在TX报文缓冲区控制寄存器中进行配置。

图32.42显示了一个通道的两个消息缓冲区成功传输的时序。

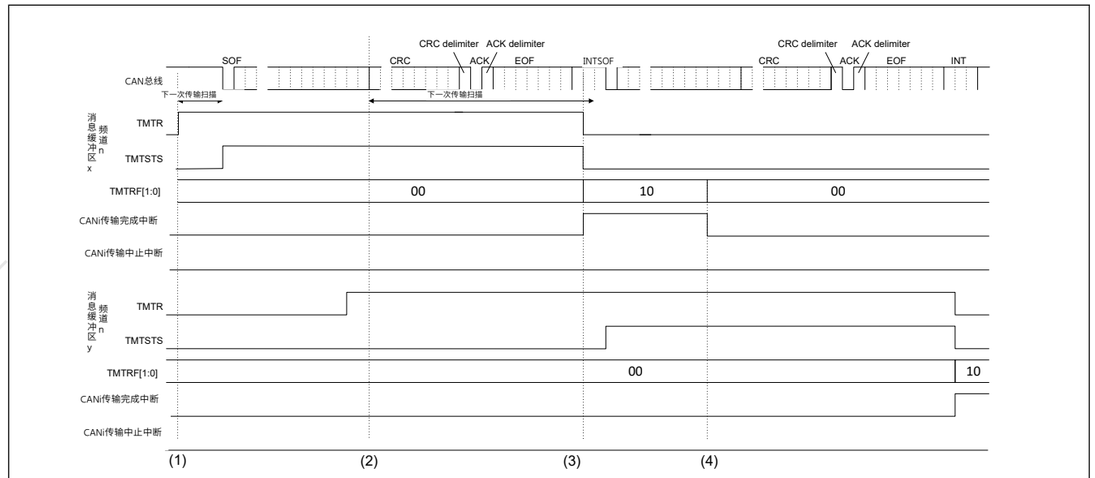

Figure 32.42 成功传输的请求和标志位的时序

1.如果TX报文缓冲区控制寄存器中的CFDTMCn.TMTR位在总线空闲状态下设置，则报文缓冲区扫描程序确定发送的最高优先级报文缓冲区。当确定发送消息缓冲区时，相关的TX消息缓冲区中的CFDTMSTSn.TMTSTS位

设置状态寄存器（发送发送器），CAN通道开始发送*1。

2.在CRC的第一位，当存在未决的传输请求时，传输扫描程序开始为下一个可能的传输。由于其他通道上的其他传输扫描，扫描时间可能会延迟，但它会在间歇3之前完成，以便能够继续传输而没有任何间隙。

3.如果报文已成功发送，则相应的TX报文缓冲区状态寄存器中的CFDTMSTSn.TMTRF[1:0]位设置为10b，CFDTMSTSn.TMTSTS和CFDTMCn.TMTR位清零。

当TX报文缓冲区中断允许配置寄存器中的TMIE位置位（允许中断）时，
CAN成功传输中断请求产生。
要清除相关中断线，请清除CFDTMSTSn.TMTRF标志位。

4.在开始下一次传输之前，清除CFDTMSTSn.TMTRF位。在发送消息缓冲区中加载下一条消息并再次设置CFDTMCn.TMTR位。在CFDTMSTSn.TMTRF[1:0]位清零之前，CFDTMCn.TMTR位不能再次置位。

注1.如果在CAN通道开始传输后仲裁丢失，CFDTMSTSn.TMTSTS位被清零。

再次执行传输扫描程序，以从第一个CRC位的开头搜索最高优先级的传输消息缓冲区。

If an error occurs either during transmission or following the loss of arbitration, then during the error frame, the transmission scanning procedure is performed again to search for the highest priority transmission message buffer.

Note: The setting point of CFDTMSTSn.TMTSTS is not always fixed at the start of the SOF. It may be delayed up to the start of the standard ID due to the synchronization logic implemented for the PLL bypass.

Figure 32.43 shows timings for transmission abort for two message buffers of one channel.

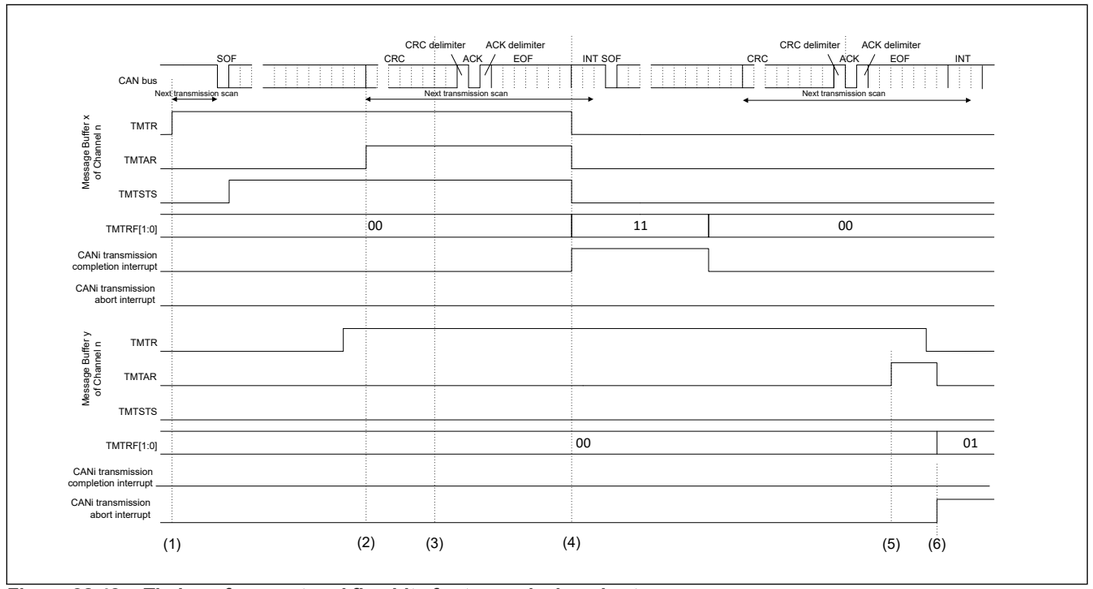

Figure 32.43 Timing of request and flag bits for transmission abort

1. If the CFDTMCn.TMTR bit in the TX Message Buffer Control Registers is set in the bus idle state, the message buffer scanning procedure determines the highest priority message buffer for transmission.
   When the transmission message buffer is determined, the CFDTMSTSn.TMTSTS bit in the TX Message Buffer Status Registers is set (transmitting/transmitter), and CAN channel starts the transmission*1.
2. If the CFDTMCn.TMTAR bit is set when the related message buffer is already selected for transmission or currently transmitting, the message is not aborted, if no error occurs or arbitration is lost.
3. At the first CRC bit, the transmission scanning procedure starts for the next transmission. In this example, timing chart message buffer y is not selected as the next transmission message buffer.
   The scan time can be delayed due to other transmission scan on other channels, but it finishes before intermission 3 to be able to continue transmission without any gaps.
4. If the message has been successfully transmitted, the CFDTMSTSn.TMTRF[1:0] bits in the corresponding TX Message Buffer Status Registers are set to 11b and the CFDTMSTSn.TMTSTS and CFDTMCn.TMTR bits are cleared.
   When the TMIE bit in the TX Message Buffer Interrupt Enable Configuration Registers is set (interrupt enabled), the CAN successful transmission interrupt request is generated.
   To clear the related interrupt line, clear the CFDTMSTSn.TMTRF[1:0] bits.
5. Another CAN node is transmitting on the CAN bus (CFDTMSTSn.TMTSTS is not set). If the CFDTMCn.TMTAR bit is set when the related channel is under transmission scan, the transmission request cannot be cleared.
6. After internal processing time, the transmission is aborted and the CFDTMSTSn.TMTRF[1:0] bits are set to 01b.
   If the message buffer is not transmitting or selected as the next transmission message buffer or under transmit scan, then the abort is immediately accepted and the corresponding CFDTMSTSn.TMTRF[1:0] bits in the TX Message Buffer Status Registers are set to 01b.
   In addition, CFDTMCn.TMTR, and CFDTMCn.TMTAR bits are cleared automatically.
   When the transmission abort interrupt enable TAIE bit of the related Channel Control Register is set then an interrupt is generated for successful transmission abort.
   To clear the related interrupt line the CFDTMSTSn.TMTRF[1:0] bits have to be cleared.

如果在传输过程中或仲裁失败后发生错误，则在错误帧期间，再次执行传输扫描程序以搜索最高优先级的传输消息缓冲区。

Note: CFDTMSTSn.TMTSTS的设定点并不总是固定在SOF的开始处。由于为PLL旁路实现的同步逻辑，它可能会延迟到标准ID的开始。

图32.43显示了一个通道的两个消息缓冲区的传输中止时序。

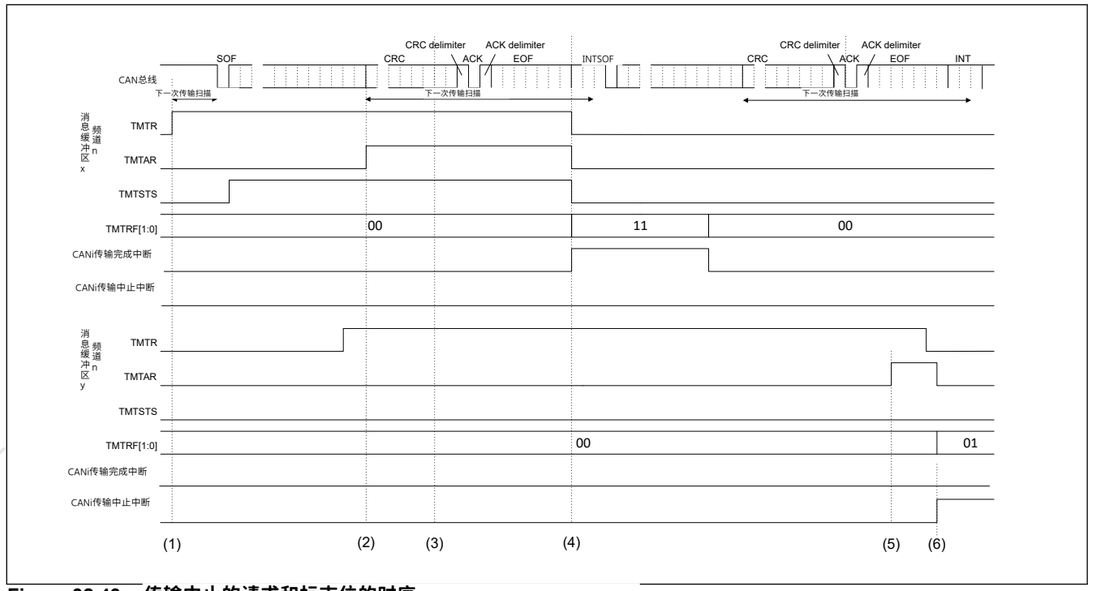

Figure 32.43 传输中止的请求和标志位的时序

1.如果TX报文缓冲区控制寄存器中的CFDTMCn.TMTR位在总线空闲状态下设置，则报文缓冲区扫描程序确定发送的最高优先级报文缓冲区。当确定发送报文缓冲区时，TX报文缓冲区状态中的CFDTMSTSn.TMTSTS位

设置寄存器（发送发送器），CAN通道开始发送*1。

2.如果CFDTMCn.TMTAR位在相关报文缓冲区已被选择发送或正在发送时被置位，如果没有错误发生或仲裁丢失，则不会中止报文。

3.在第一个CRC位，传输扫描程序开始下一次传输。在这个例子中，时序图消息缓冲区y没有被选为下一个传输消息缓冲区。由于其他通道上的其他传输扫描，扫描时间可能会延迟，但它会在间歇3之前完成，以便能够继续传输而没有任何间隙。

4.如果报文已成功发送，则相应的TX报文缓冲区状态寄存器中的CFDTMSTSn.TMTRF[1:0]位设置为11b，并且CFDTMSTSn.TMTSTS和CFDTMCn.TMTR位清零。
当TX报文缓冲区中断允许配置寄存器中的TMIE位置位（允许中断）时，
CAN成功传输中断请求产生。
要清除相关中断线，请清除CFDTMSTSn.TMTRF[1:0]位。

5.另一个CAN节点正在CAN总线上传输（CFDTMSTSn.TMTSTS未设置）。如果在相关通道正在发送扫描时设置CFDTMCn.TMTAR位，则不能清除发送请求。

6.内部处理时间过后，发送中止，CFDTMSTSn.TMTRF[1:0]位设置为01b。
如果报文缓冲区未发送或被选为下一个发送报文缓冲区或正在发送扫描，则立即接受中止并将TX报文缓冲区状态寄存器中的相应CFDTMSTSn.TMTRF[1:0]位设置为01b。

此外，CFDTMCn.TMTR和CFDTMCn.TMTAR位会自动清零。
当相关通道控制寄存器的发送中止中断使能位TAIE置位时，将产生中断以成功发送中止。要清除相关的中断线，必须清除CFDTMSTSn.TMTRF[1:0]位。

Note 1. If arbitration is lost after the CAN channel starts the transmission, the CFDTMSTSn.TMTSTS bit is cleared.

The transmission scanning procedure is performed again to search for the highest priority transmission message buffer from the beginning of the first CRC bit.

If an error occurs, either during transmission, or following the loss of arbitration, then during the error frame, the transmission scanning procedure is performed again to search for the highest priority transmission message buffer.

32.8.2.3 TX FIFO or GW FIFO Transmission

Three common FIFO buffers are assigned to each channel. The three FIFO buffers can be linked to any normal TX message buffer position for this channel with the CFDCFCCn.CFTML bits in the Common FIFO Configuration/Control Register if configured in TX or GW mode.

When the transmission scan starts and the FIFO buffer corresponding to this TX message buffer is enabled, the relevant message in the FIFO buffer participates in the transmission scan.

Configuration of a TX message buffer linked to a FIFO buffer configured in TX or GW mode should not be done.

(1) TX FIFO Operation

CAN messages can be written into the TX FIFO by writing to the corresponding FIFO Access registers.

When the value 0xFF is written into the corresponding FIFO Pointer Control Register, the message count of the related FIFO is incremented by 1.

Only write to the FIFO Pointer Control register after writing the complete message to the corresponding FIFO Access registers. If the message count matches the FIFO depth, the FIFO Full flag is set.

The oldest message in the TX FIFO is included in the scan for transmission by the corresponding CAN-FD module channel logic.

When a message is successfully transmitted from the TX FIFO, the message count value is decremented by 1. When all the messages from the FIFO are transmitted, the FIFO Empty flag is set.

The interrupt generation conditions for the TX FIFO buffers can be configured by configuring the CFDCFCCn.CFIM bit in the corresponding Common FIFO Configuration/Control Registers.

If CFDCFCCn.CFIM bit is 0, then interrupt is generated when the last message is successfully transmitted from the TX FIFO buffer.

If CFDCFCCn.CFIM bit is 1, then interrupt is generated for every successfully transmitted message from the TX FIFO buffer.

The Common FIFO can set interrupt when CAN frame transmission is complete.

The Common FIFO buffers configured in TX Mode can be disabled by clearing the CFDCFCCn.CFE bit in the Common FIFO Configuration/Control Registers. If this bit is cleared to 0, the FIFO Empty flag is set as follows:

- Immediately if the message from the TX FIFO is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the TX FIFO is already scheduled for transmission or already in transmission.

Note: The Common FIFO buffer is considered as disabled after clearing the CFDCFCCn.CFE bit only when the Empty flag is set for the corresponding Common FIFO buffer.

Other possible messages pending from the TX FIFO are lost and their transmission must be requested again. Before CFDCFCCn.CFE is set again, ensure that CFDCFSTSn.CFEMP bit is set and that there are no pending abort from the TX FIFO.

When the CFDCFCCn.CFE bit is cleared, the message read and write pointers of the FIFO are cleared and are no longer active. Therefore, all messages in the FIFO buffers are lost and no further message can be stored into the FIFO.

The FIFO transmission request procedure after configuration is shown in Figure 32.44.

注1.如果在CAN通道开始传输后仲裁丢失，CFDTMSTSn.TMTSTS位被清零。

再次执行传输扫描程序，以从第一个CRC位的开头搜索最高优先级的传输消息缓冲区。

如果在传输过程中或在仲裁失败之后发生错误，则在错误帧期间，再次执行传输扫描程序以搜索最高优先级的传输消息缓冲区。

32.8.2.3 TXFIFO或GWFIFO传输

为每个通道分配了三个通用FIFO缓冲区。如果配置为TX或GW模式，则三个FIFO缓冲区可以通过通用FIFO配置控制寄存器中的CFDCFCCn.CFTML位链接到该通道的任何正常TX消息缓冲区位置。

当发送扫描开始并且与该TX报文缓冲区对应的FIFO缓冲区使能时，FIFO缓冲区中的相关报文参与发送扫描。

不应配置链接到在TX或GW模式下配置的FIFO缓冲区的TX消息缓冲区。

(1) TX FIFO Operation

通过写入相应的FIFO访问寄存器，可以将CAN消息写入TXFIFO。

当值0xFF被写入对应的FIFO指针控制寄存器时，相关的报文计数
FIFO加1。

仅在将完整消息写入相应的FIFO访问寄存器后才写入FIFO指针控制寄存器。如果消息计数与FIFO深度匹配，则设置FIFO满标志。

TXFIFO中最旧的消息包含在相应CAN-FD模块通道逻辑的传输扫描中。

当一条消息从TXFIFO成功发送时，消息计数值减1。当FIFO中的所有消息都发送完毕时，FIFO空标志置位。

TXFIFO缓冲区的中断生成条件可以通过配置相应通用FIFO配置控制寄存器中的CFDCFCCn.CFIM位来配置。

如果CFDCFCCn.CFIM位为0，则当最后一条消息从TX成功发送时产生中断
FIFO buffer.

如果CFDCFCCn.CFIM位为1，则每次从TXFIFO缓冲区成功发送的消息都会产生中断。

当CAN帧传输完成时，CommonFIFO可以设置中断。

在TX模式下配置的通用FIFO缓冲区可以通过清除通用的CFDCFCCn.CFE位来禁用
FIFO配置控制寄存器。如果该位清0，FIFO空标志设置如下：

●如果来自TXFIFO的消息既没有安排下一次传输也没有在传输中，则立即执行

●传输完成后，检测到CAN总线错误、仲裁丢失或转换到
如果来自TXFIFO的传输已被安排传输或已在传输中，则为通道或全局暂停模式。

Note: 仅当为相应的CommonFIFO缓冲区设置Empty标志时，在清除CFDCFCCn.CFE位后，CommonFIFO缓冲区才被视为禁用。

来自TXFIFO的其他可能未决消息丢失，必须再次请求它们的传输。前
CFDCFCCn.CFE再次设置，确保CFDCFSTSn.CFEMP位已设置并且TX没有挂起的中止
FIFO.

当CFDCFCCn.CFE位清零时，FIFO的报文读写指针被清零，不再处于活动状态。因此，FIFO缓冲区中的所有消息都将丢失，并且无法将更多消息存储到FIFO中。

配置后的FIFO发送请求流程如图32.44所示。

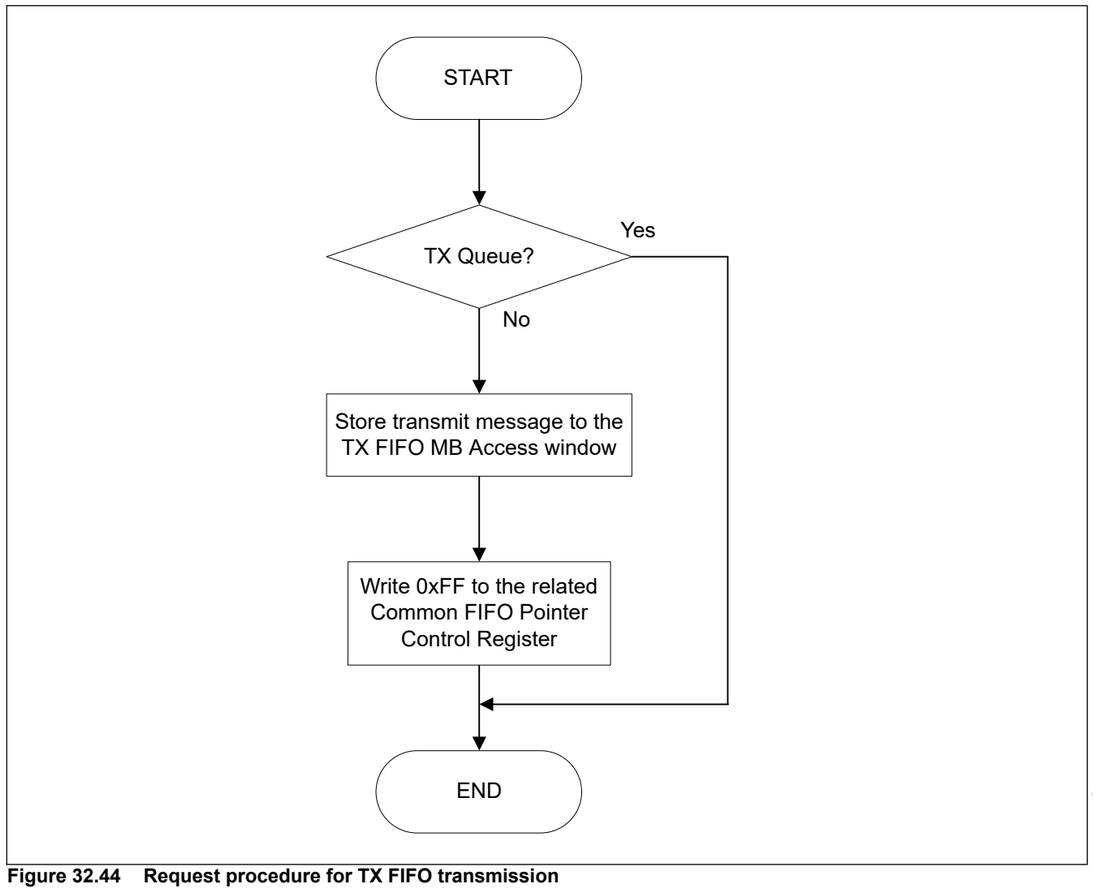

Figure 32.44 Request procedure for TX FIFO transmission

(2) GW FIFO Operation

The AFL entries for routing the received messages to GW FIFO buffers should be configured based on the system requirements. The matching AFL entry selects the GW FIFO buffer for storage of a received message on any of the CAN channels.

When a message is successfully received and stored in a GW FIFO buffer, the FIFO message count in the corresponding FIFO Status Register is incremented by 1. If the message count matches the FIFO depth, the FIFO Full flag is set.

The oldest message in the GW FIFO is included in the scan for transmission by the corresponding CAN-FD module channel logic.

When a message is successfully transmitted from the GW FIFO, the message count value is decremented by 1. When all messages from the GW FIFO are transmitted, the FIFO Empty flag is set.

If a new message is stored into the FIFO when the FIFO message count matches the FIFO depth (FIFO Full condition), the FIFO Message Lost flag is set and the new message is lost (no overwrite of already stored messages takes place).

In GW mode, when a transmit/receive FIFO buffer is receiving a new message while the transmit/receive FIFO buffer is already full of data, the oldest data of the buffer is overwritten with the message received or the message is discarded. The behavior is determined by setting the CFDCFCCEn.CFMOWM bit.

- When CFDCFCCEn.CFMOWM = 0:
  When writing of data is required due to reception of a new message while a transmit/receive FIFO buffer is full of data, the received message is discarded and the CFDCFSTSn.CFMLT bit is set to 1.

- When CFDCFCCEn.CFMOWM = 1:

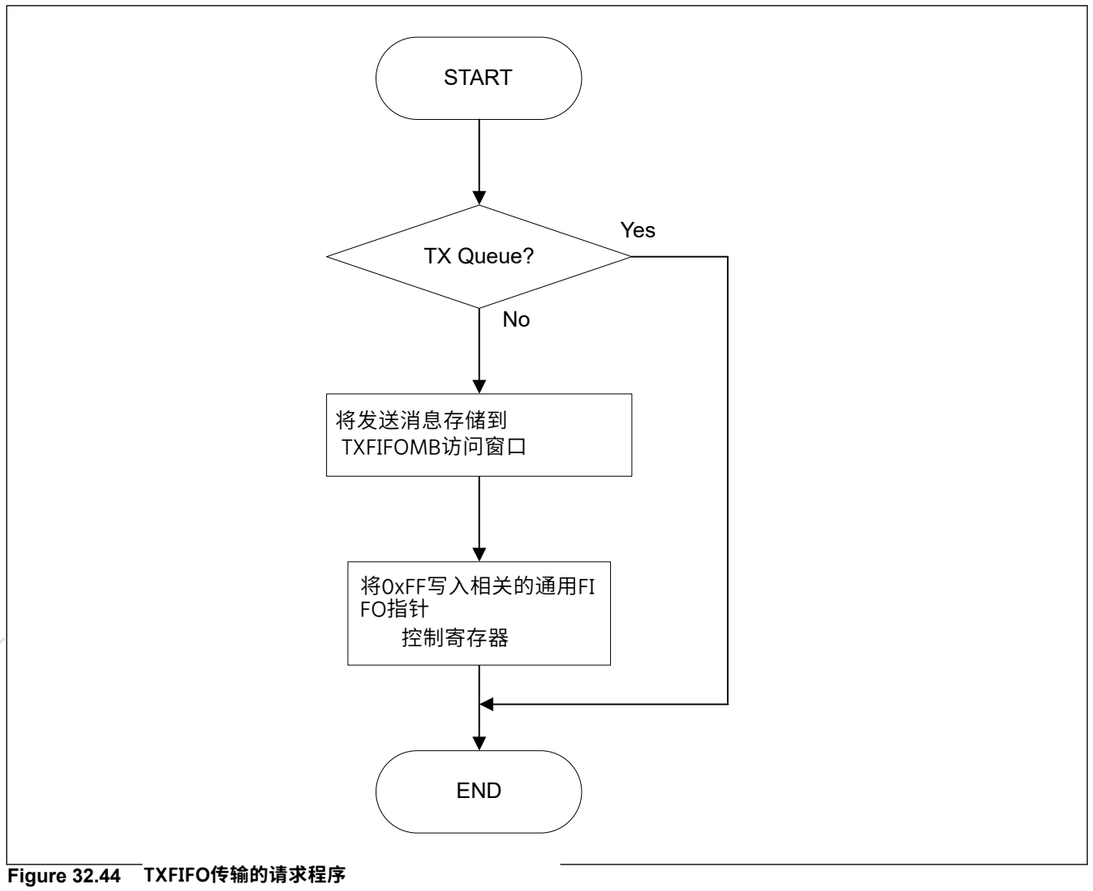

Figure 32.44 TXFIFO传输的请求程序

(2) GW FIFO Operation

应根据系统要求配置用于将接收到的消息路由到GWFIFO缓冲区的AFL条目。匹配的AFL条目选择GWFIFO缓冲区，用于在任何CAN通道上存储接收到的消息。

当消息被成功接收并存储在GWFIFO缓冲区中时，相应的FIFO消息计数
FIFO状态寄存器加1。如果报文计数与FIFO深度匹配，则设置FIFO满标志。

GWFIFO中最旧的消息包含在扫描中以供相应的CAN-FD模块通道逻辑进行传输。

当一条消息从GWFIFO成功传输时，消息计数值减1。当所有来自GWFIFO的消息都传输完毕时，设置FIFOEmpty标志。

如果在FIFO消息计数与FIFO深度匹配（FIFO满条件）时将新消息存储到FIFO，则
FIFO消息丢失标志被设置，新消息丢失（不会覆盖已存储的消息）。

在GW模式下，当发送接收FIFO缓冲区正在接收新消息而发送接收FIFO缓冲区已满数据时，缓冲区中最旧的数据将被接收到的消息覆盖或丢弃该消息。该行为是通过设置CFDCFCCEn.CFMOWM位来确定的。

- When CFDCFCCEn.CFMOWM = 0:
  当发送接收FIFO缓冲区已满数据而由于接收到新报文而需要写入数据时，将丢弃接收到的报文并将CFDCFSTSn.CFMLT位设置为1。

- When CFDCFCCEn.CFMOWM = 1:

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When writing of data is required due to reception of a new message while a transmit/receive FIFO buffer is full of data, the oldest data in the buffer is overwritten with the received message.
The read pointer of the transmit/receive FIFO buffer simultaneously moves to the next oldest message. The CFDCFSTSn.CFMOW bit is then set to 1, which notifies that the oldest message has been overwritten with the received message.
In addition, when a CAN bus error or arbitration-lost for the transmitting message occurs in transmit/receive FIFO buffer full, the transmitting message is lost and retransmission of the message is not performed. The read pointer moves to the next message automatically.

The interrupt generation conditions for the GW FIFO buffers can be configured by setting the CFDCFCCn.CFIM bit in the corresponding Common FIFO Configuration/Control Registers.

If CFDCFCCn.CFIM bit is 0, the RX Interrupt flag is set when the FIFO counter increments and reaches value configured by CFDCFCCn.CFIGCV and the TX Interrupt flag is set when FIFO transmits the last message successfully.

If CFDCFCCn.CFIM bit is 1, the RX Interrupt flag is set at the end of storage of every received message and the TX Interrupt flag is set if a message is successfully transmitted from the FIFO.

The Common FIFO can set interrupt when:

- CAN frame transmitted is complete
- CAN frame reception is complete
- FIFO is in full status in RX mode or GW mode.

When CFDCFCCEn.CFBME = 1, the mode is FIFO buffering, send data is stored in Common FIFO, and transmission is stopped. Transmission is started if it is set as CFDCFCCEn.CFBME = 0.

The Common FIFO buffers configured in GW mode can be disabled by clearing the CFDCFCCn.CFE bit in the Common FIFO Configuration/Control Register. If this bit is cleared, the GW FIFO becomes empty as follows:

- Immediately if the message from the GW FIFO is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the GW FIFO is already scheduled for transmission or already in transmission.

Other possible messages pending from the GW FIFO are lost.

Before CFDCFCCn.CFE is set again, ensure that the CFDCFSTSn.CFEMP bit is set and that there are no pending abort from the GW FIFO.

When the CFDCFCCn.CFE bit is cleared and the CFDCFSTSn.CFEMP bit is set, the read and write pointers of the message in GW FIFO are cleared and are no longer active. Therefore, all messages in the GW FIFO buffers are lost and no further message can be stored into the GW FIFO.

In applications intended to be used as CAN-to-CAN gateways, it is recommended that if the Error State Indication (ESI) information of the routing messages is not replaced by the sending node error state indication. For this, each channel has the Control Function register CFDCnFDCFG.ESIC to replace their own ESI information by the routing ESI information.

Note: If the sending node is error-passive, the ESI bit is sent anyway as error-passive (ESI = 1).

Note: This feature is not available in classical CAN function because CFDCnFDCFG is not in classical CAN.

(3) Interval Timer for FIFO Transmission

For each Common FIFO in TX or GW mode, it is possible to specify a delay between two consecutive messages that are configured for transmission from the same FIFO buffer. This delay is called interval time. This interval time starts after the first message has been successfully transmitted from the FIFO buffer after the CFDCFCCn.CFE bit is set.

When the Common FIFO in TX or GW mode is enabled, the first message is transmitted without considering this interval time.

The interval timer stops counting when:

- FIFO is disabled by clearing the CFDCFCCn.CFE bit.
- CAN channel is in CH_RESET mode.

当发送接收FIFO缓冲区已满数据时，由于接收到新报文而需要写入数据时，缓冲区中最旧的数据将被接收到的报文覆盖。发送接收FIFO缓冲区的读指针同时移动到下一个最旧的消息。这

CFDCFSTSn.CFMOW位然后设置为1，通知最旧的消息已被接收的消息覆盖。此外，当发送接收FIFO缓冲区已满时发生CAN总线错误或发送报文仲裁丢失时，发送报文丢失且不进行报文重传。读取指针自动移动到下一条消息。

GWFIFO缓冲区的中断生成条件可以通过设置相应的通用FIFO配置控制寄存器中的CFDCFCCn.CFIM位来配置。

如果CFDCFCCn.CFIM位为0，则当FIFO计数器递增并达到CFDCFCCn.CFIGCV配置的值时设置RX中断标志 ，并且当FIFO成功发送最后一条消息时设置TX中断标志 。

如果CFDCFCCn.CFIM位为1，则RX中断标志 在每个接收到的消息的存储结束时设置，并且TX
如果消息从FIFO成功发送，则设置中断标志。

CommonFIFO可以在以下情况下设置中断：

●CAN帧传输完成

●CAN帧接收完成

●在RX模式或GW模式下，FIFO处于满状态。

当CFDCFCCEn.CFBME=1时，模式为FIFO缓冲，发送数据存储在CommonFIFO中，停止发送。如果设置为CFDCFCCEn.CFBME=0，则开始传输。

配置为GW模式的CommonFIFO缓冲区可以通过清除Common中的CFDCFCCn.CFE位来禁用。
FIFO配置控制寄存器。如果该位清零，则GWFIFO变为空，如下所示：

●如果来自GWFIFO的消息既没有安排下一次传输也没有在传输中，则立即执行

●传输完成后，检测到CAN总线错误、仲裁丢失或转换到
如果来自GWFIFO的传输已被安排传输或已在传输中，则通道或全局暂停模式。

GWFIFO中未决的其他可能消息将丢失。

在再次设置CFDCFCCn.CFE之前，确保设置了CFDCFSTSn.CFEMP位并且没有来自GWFIFO的挂起的中止。

当CFDCFCCn.CFE位清零并设置CFDCFSTSn.CFEMP位时，GWFIFO中报文的读写指针被清零，不再处于活动状态。因此，GWFIFO缓冲区中的所有消息都将丢失，并且无法将更多消息存储到GWFIFO中。

在打算用作CAN到CAN网关的应用中，如果路由消息的错误状态指示(ESI)信息不被发送节点错误状态指示替换，则建议。为此，每个通道都有控制功能寄存器CFDCnFDCFG.ESIC来用路由ESI信息替换自己的ESI信息。

Note: 如果发送节点是错误被动的，ESI位无论如何都会作为错误被动（ESI=1）发送。

Note: 此功能在经典CAN功能中不可用，因为CFDCnFDCFG不在经典CAN中。

(3) FIFO传输间隔定时器

对于TX或GW模式下的每个CommonFIFO，可以指定配置为从同一FIFO缓冲区传输的两个连续消息之间的延迟。这种延迟称为间隔时间。在CFDCFCCn.CFE位置位后，从FIFO缓冲区成功发送第一条消息后，此间隔时间开始。

当TX或GW模式下的CommonFIFO被使能时，第一个报文在不考虑这个间隔时间的情况下被发送。

间隔计时器在以下情况下停止计数：

●通过清除CFDCFCCn.CFE位禁用FIFO。

●CAN通道处于CH_RESET模式。

The interval time is specified by the CFDCFCCn.CFITT value from 0 to 255 timer units in the Common FIFO Configuration/Control Register.

The timer unit can be defined based on two different source clocks for the interval timer. To disable the interval timer for FIFO transmission, select a value of 0.

The timer source can be selected with the configuration bit CFITSS in the Common FIFO Configuration/Control Register.

If CAN channel bit time clock is configured as the clock source, and the CAN channel enters CH_HALT, CH_RESET, or CH_SLEEP mode, the interval timer is stopped for that channel.

If peripheral clock is selected as the interval timer clock source, the interval timer is stopped only when the CAN channel is in CH_RESET or CH_SLEEP mode.

The reference clock can be used to configure the interval time in fixed time units. It is based on the peripheral clock. The reference clock prescaler value CFDGCFG.ITRCP in the Global Configuration Register defines the relation between the peripheral clock frequency/period and the reference clock period.

See Table 32.22 for CFDGCFG.ITRCP configuration values to achieve different reference clock periods based on the peripheral clock frequency and period.

Table 32.22 Configuration example for the reference clock of the FIFO interval timer

Reference clock/Peripheral clock	1 µs	100 µs	500 µs
16 MHz/62.5 ns	16	1600	8000
20 MHz/50 ns	20	2000	10000
32 MHz/31.25 ns	32	3200	16000
50 MHz/20 ns	50	5000	25000

The reference clock resolution can be specified by the interval timer reference clock resolution value CFDCFCCn.CFITR in the Common FIFO Configuration/Control Register.

The interval time is based on the reference clock period multiplied by the configured value (x1 or x10). The reference clock based interval timer can be used to satisfy the requirements of the ISO 15765-2 Separation Time. The whole range for the separation time from 100 µs to 127 µs can be covered.

The specified interval time starts after successful transmission event (after EOF7 state of the CAN protocol).

When the interval time has elapsed, the next transmission request is raised by the related TX/GW FIFO. Therefore, the interval time defines the minimum time between two messages transmitted from one FIFO.

The next message is sent at earliest after this interval time. Figure 32.45 shows an example timing of the internal processing.

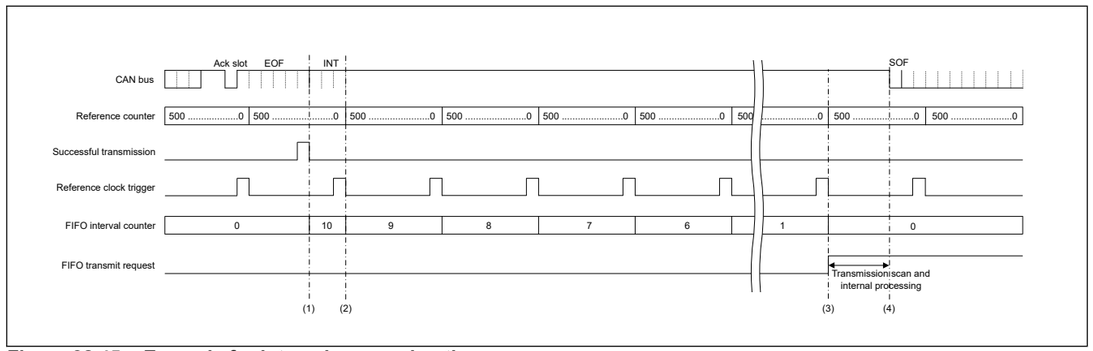


Figure 32.45 Example for interval processing time

The configuration for the timing in Figure 32.45 is as follows:

- Peripheral clock frequency = 50 MHz
- Interval timer reference clock (CFDGCFG.ITRCP) = 500 times
- Reference clock from the settings in Figure 32.45 = 10 µs

间隔时间由CommonFIFO中0到255个定时器单位的CFDCFCCn.CFITT值指定
Configuration/Control Register.

可以根据间隔定时器的两个不同源时钟来定义定时器单元。禁用间隔计时器
FIFO传输，选择值0。

定时器源可以通过通用FIFO配置控制寄存器中的配置位CFITSS来选择。

如果CAN通道位时间时钟配置为时钟源，并且CAN通道进入CH_HALT、CH_RESET或
CH_SLEEP模式，该通道的间隔定时器停止。

如果选择外设时钟作为间隔定时器时钟源，则间隔定时器只有在CAN通道处于CH_RESET或CH_SLEEP模式时才会停止。

参考时钟可用于以固定时间单位配置间隔时间。它基于外设时钟。全局配置寄存器中的参考时钟预分频器值CFDGCFG.ITRCP定义了外设时钟频率周期和参考时钟周期之间的关系。

有关CFDGCFG.ITRCP配置值，请参见表32.22，以根据外设时钟频率和周期实现不同的参考时钟周期。

Table 32.22 FIFO间隔定时器的参考时钟配置示例

参考时钟外设时钟	1 µs	100 µs	500 µs
16 MHz/62.5 ns	16	1600	8000
20 MHz/50 ns	20	2000	10000
32 MHz/31.25 ns	32	3200	16000
50 MHz/20 ns	50	5000	25000

参考时钟分辨率可以通过公共FIFO配置控制寄存器中的间隔定时器参考时钟分辨率值CFDCFCCn.CFITR来指定。

间隔时间基于参考时钟周期乘以配置值（x1或x10）。基于参考时钟的间隔定时器可用于满足ISO15765-2分离时间的要求。可以覆盖从100µs到127µs的整个分离时间范围。

指定的间隔时间在成功传输事件后（在CAN协议的EOF7状态后）开始。

当间隔时间过去时，下一个传输请求由相关的TXGWFIFO提出。因此，间隔时间定义了从一个FIFO传输的两条消息之间的最短时间。

下一条消息最早在此间隔时间之后发送。图32.45显示了内部处理的示例时序。

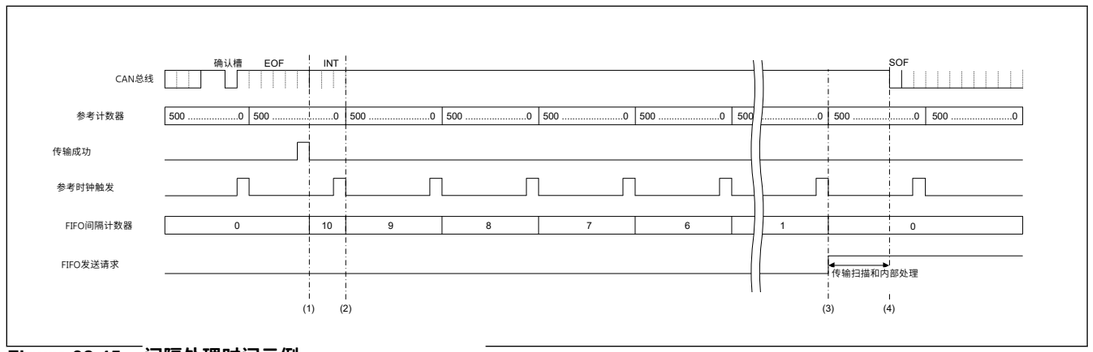


Figure 32.45 间隔处理时间示例

图32.45中的时序配置如下：

- 外设时钟频率=50MHz
- 间隔定时器参考时钟(CFDGCFG.ITRCP)=500次
- 图32.45中设置的参考时钟=10µs

- Common FIFO interval timer source selection (CFDCFCCn.CFITSS) = 0
- Common FIFO interval timer resolution (CFDCFCCn.CFITR) = 0
- Common FIFO interval transmission time (CFDCFCCn.CFITT) = 10 times
- Theoretical message separation interval = 100 µs

1. Internal FIFO interval timer is restarted with the occurrence of successful transmission result. This restart is not synchronized to the reference clock trigger. Therefore, the first interval is counting less or equal to 1 reference clock interval.
2. With the next reference clock trigger the FIFO interval timer is decremented.
3. When the FIFO interval timer reached the value 0, the FIFO transmit request is set.
4. When the FIFO is selected for transmission, the transmission starts. Due to internal processing, this usually takes less than 3 CAN bit time, between the internal FIFO transmit request set in step 3. and the actual transmission.

In the worst case when multiple events such as a reception scan, an internal message routing, a transmit scan on all channels occur, it can take up to 1152 peripheral clock cycles.

As shown in Figure 32.45, it is not guaranteed that the minimum interval is always equal to the configured value. If a minimum time must never be breached, configure CFDCFCCn.CFITT to the required minimum value plus 1.

If additional TX message buffers or TX/GW FIFOs are configured for transmission of the same channel, the real delay between two messages transmitted from a TX FIFO can be much longer than specified by the interval time. This is due to higher priority message transmission from these TX message buffers or TX/GW FIFOs.

Figure 32.46 shows a block diagram of the FIFO interval time generation circuit.

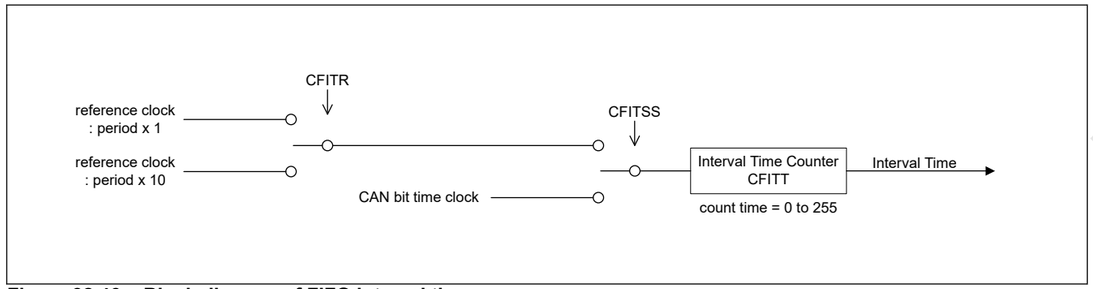


Figure 32.46 Block diagram of FIFO interval timer

32.8.2.4 TX Queue

Each enabled TX Queue for a specific channel consists of three to 16 TX message buffers, which are accessed through one access window. One channel has four TX Queues:

- The first TX Queue can be configured with a depth of three up to eight buffers and uses TX Message Buffer No. 0 as access window (referred to as TXQ0)
- The second TX Queue can be configured with a depth of three up to eight buffers and uses TX Message Buffer No. 7 as access window (referred to as TXQ1)
- The third TX Queue can be configured with a depth of three up to eight buffers and uses TX Message Buffer No. 32 as access window (referred to as TXQ2)
- The fourth TX Queue can be configured with a depth of three up to eight buffers and uses TX Message Buffer No. 39 as access window (referred to as TXQ3).

All the TXQ0, TXQ1, TXQ2 and TXQ3 messages enter the priority comparison for transmission, which should be only ID Priority (CFDGCFG.TPRI = 0).

The registers for TXQ0 are:

- CFDTXQCC0[n]
- CFDTXQSTS0[n]

●通用FIFO间隔定时器源选择(CFDCFCCn.CFITSS)=0
●通用FIFO间隔定时器分辨率(CFDCFCCn.CFITR)=0
●普通FIFO间隔传输时间（CFDCFCCn.CFITT）=10次
●理论消息分离间隔=100µs

1.内部FIFO间隔定时器随着成功传输结果的出现而重新启动。这次重启不同步到参考时钟触发。因此，第一个间隔计数小于或等于1个参考时钟间隔。

2.随着下一个参考时钟触发，FIFO间隔定时器递减。

3.当FIFO间隔定时器达到值0时，设置FIFO发送请求。

4.WhentheFIFOisselectedfortransmission thetransmissionstarts.由于内部处理，在步骤3中设置的内部FIFO发送请求和实际发送之间，这通常需要不到3个CAN位时间。

在最坏的情况下，当接收扫描、内部消息路由、所有通道上的发送扫描等多个事件发生时，可能需要多达1152个外设时钟周期。

如图32.45所示，不能保证最小间隔总是等于配置的值。如果决不能超过最短时间，请将CFDCFCCn.CFITT配置为所需的最小值加1。

如果额外的TX消息缓冲区或TXGWFIFO配置为传输同一通道，则从TXFIFO传输的两个消息之间的实际延迟可能比间隔时间指定的长得多。这是由于来自这些TX消息缓冲区或TXGWFIFO的更高优先级的消息传输。

图32.46显示了FIFO间隔时间生成电路的框图。

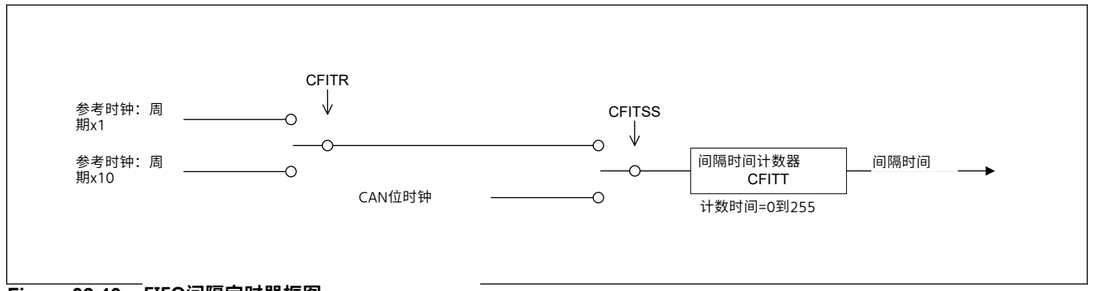


Figure 32.46 FIFO间隔定时器框图

32.8.2.4 TX Queue

特定通道的每个启用的TX队列由3到16个TX消息缓冲区组成，这些缓冲区通过一个访问窗口访问。一个通道有四个TX队列：

●第一个TXQueue可以配置深度为3到8个缓冲区，并使用0号TX消息缓冲区作为访问窗口（简称TXQ0）

●第二个TXQueue可配置深度为3到8个缓冲区，并使用7号TX消息缓冲区作为访问窗口（简称TXQ1）

●第三个TXQueue可配置深度为3到8个缓冲区，并使用32号TXMessageBuffer作为访问窗口（简称TXQ2）

●第四个TXQueue可配置深度为3到8个缓冲区，并使用39号TX消息缓冲区作为访问窗口（简称TXQ3）。

所有的TXQ0、TXQ1、TXQ2、TXQ3报文都进入优先级比较进行传输，应该只有ID Priority (CFDGCFG.TPRI = 0).

TXQ0的寄存器是：

- CFDTXQCC0[n]
- CFDTXQSTS0[n]

- CFDTXQPCTR0[n].

The registers for TXQ1 are:

- CFDTXQCC1[n]
- CFDTXQSTS1[n]
- CFDTXQPCTR1[n].

The registers for TXQ2 are:

- CFDTXQCC2 [n]
- CFDTXQSTS2[n]
- CFDTXQPCTR2[n].

The registers for TXQ3 are:

- CFDTXQCC3[n]
- CFDTXQSTS3[n]
- CFDTXQPCTR3[n].

See related access registers TX Message Buffer ID Registers (TMID[m]), TX Message Buffer Pointer Registers (TMPTR[m]), TX Message Buffer Data Field 0 Registers, and TX Message Buffer Data Field 1 Registers (TMDF[0:1][m]) when access window TXQ0, TXQ1, TXQ2, or TXQ3 is used.

The depth of each TXQ0 buffer can be configured by writing to the CFDTXQCC0n.TXQDC[12:8] bits of the TX Queue Configuration/Control Register. TXQ0 can be set from TXMB0 to TXMB7 as a queue buffer at the maximum.

The 15 available options for the depth configuration of TXQ0 buffer are:

- 0x00: TX Queue disabled
- 0x01: Reserved
- 0x02: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

The depth of each TXQ1 buffer can be configured by writing to the CFDTXQCC1n.TXQDC[12:8] bits of the TX Queue Configuration/Control Register. TXQ1 can be set from TXMB7 to TXMB0 as a queue buffer at the maximum.

The 15 available options for the depth configuration of TXQ1 buffer are:

- 0x00: TX Queue disabled
- 0x01: Reserved
- 0x02: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

The depth of each TXQ2 buffer can be configured by writing to the CFDTXQCC2n.TXQDC[12:8] bits of the TX Queue Configuration/Control Register. TXQ2 can be set from TXMB32 to TXMB39 as a queue buffer at the maximum.

The 15 available options for the depth configuration of TXQ2 buffer are:

- 0x00: TX Queue disabled
- 0x01: Reserved

- CFDTXQPCTR0[n].

TXQ1的寄存器是：

- CFDTXQCC1[n]
- CFDTXQSTS1[n]
- CFDTXQPCTR1[n].

TXQ2的寄存器是：

- CFDTXQCC2 [n]
- CFDTXQSTS2[n]
- CFDTXQPCTR2[n].

TXQ3的寄存器是：

- CFDTXQCC3[n]
- CFDTXQSTS3[n]
- CFDTXQPCTR3[n].

请参阅相关访问寄存器TX报文缓冲区ID寄存器(TMID[m])、TX报文缓冲区指针寄存器(TMPTR[m])、TX报文缓冲区数据字段0寄存器和TX报文缓冲区数据字段1寄存器(TMDF[0:1][m])当使用访问窗口TXQ0、TXQ1、TXQ2或TXQ3时。

每个TXQ0缓冲区的深度可以通过写入TX队列的CFDTXQCC0n.TXQDC[12:8]位来配　　置配置控制寄存器。TXQ0最大可以设置为TXMB0到TXMB7作为队列缓冲区。

TXQ0缓冲区深度配置的15个可用选项是：

- 0x00：TX队列禁用
- 0x01: Reserved
- 0x02: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

每个TXQ1缓冲区的深度可以通过写入TX队列的CFDTXQCC1n.TXQDC[12:8]位来配　　置配置控制寄存器。TXQ1最大可以设置为TXMB7到TXMB0作为队列缓冲区。

TXQ1缓冲器深度配置的15个可用选项是：

- 0x00：TX队列禁用
- 0x01: Reserved
- 0x02: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

每个TXQ2缓冲区的深度可以通过写入TX队列的CFDTXQCC2n.TXQDC[12:8]位来配　　置配置控制寄存器。TXQ2最大可以设置为TXMB32到TXMB39作为队列缓冲区。

TXQ2缓冲器深度配置的15个可用选项是：

- 0x00：TX队列禁用
- 0x01: Reserved

- 0x02: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

The depth of each TXQ3 buffer can be configured by writing to the CFDTXQCC3n.TXQDC[12:8] bits of the TX Queue Configuration/Control Register. TXQ3 can be set from TXMB39 to TXMB32 as a queue buffer at the maximum.

The 15 available options for the depth configuration of TXQ3 buffer are:

- 00000b: TX Queue disabled
- 00001b: Reserved
- 00010b: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

When using TXQ1 and TXQ0 simultaneously, the depth of TXQ is 8 or less in total.

When using TXQ3 and TXQ2 simultaneously, the depth of TXQ is 8 or less in total.

Do not access all the TX message buffers forming the TX Queue directly (except TX Message Buffer No. 39, TX Message Buffer No. 32, TX Message Buffer No. 7 and TX Message Buffer No. 0, which act as TX Queue access window).

When CFDGAFLP0n.GAFLSRD i (i = 0 to 2) is set and the CFDTXQCCin.TXQGWE (i = 0 to 2, n = 0 to 7) is also set, a receiving frame is stored in the target TXQ as send data by routing.

When CFDTXQCCn.TXQOWE bit is 1, the TX Queue is in TX Queue Overwrite mode. If the message of the same ID is stored in TX Queue when a frame is received and it is stored in TX Queue, an old message is overwritten by a new message. Therefore, an old message is not transmitted. When the old message of the same ID is transmitting and a CAN bus error and an arbitration-lost occur, the message of old ID is not resent.

When using the function in GW mode and TX Queue Overwrite mode, the depth of TXQ (CFDTXQCC0n.TXQDC) should be configured to a value that is the various number of ID used in the TX Queue plus 3. If it accesses by routing in GW mode when a TXQ buffer is full, CFDTXQSTS.TXQMLT is set and send data is thrown away. The function is valid for the standard ID frame and is invalid for the extended ID frame.

Operation of the TXQ same ID over-writing function in GW mode is shown in the following figure.

- 0x02: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

每个TXQ3缓冲区的深度可以通过写入TX队列的CFDTXQCC3n.TXQDC[12:8]位来配　　置
配置控制寄存器。TXQ3最大可以设置为TXMB39到TXMB32作为队列缓冲区。

TXQ3缓冲器深度配置的15个可用选项是：

●00000b：TX队列禁用

- 00001b: Reserved
- 00010b: 3 messages
- ⋮
- 0x0D: 14 messages
- 0x0E: 15 messages
- 0x0F: 16 messages

当同时使用TXQ1和TXQ0时，TXQ的深度总共为8或更少。

当同时使用TXQ3和TXQ2时，TXQ的深度总共为8或更少。

不要直接访问形成TXQueue的所有TX消息缓冲区（TX消息缓冲区No.39，TX消息除外）
BufferNo.32、TXMessageBufferNo.7和TXMessageBufferNo.0，作为TXQueue访问窗口）。

当CFDGAFLP0n.GAFLSRDi(i=0to2)被设置并且CFDTXQCCin.TXQGWE(i=0to2 n=0to7)也被设置时，接收帧被存储
在目标TXQ作为路由发送数据.

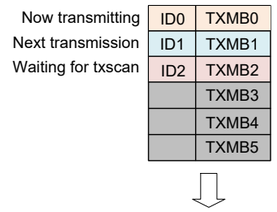
当CFDTXQCCn.TXQOWE位为1时，TXQueue处于TXQueueOverwrite模式。如果在接收到一帧时将相同ID的消息存储在TXQueue中，并将其存储在TXQueue中，则旧消息将被新消息覆盖。因此，不发送旧消息。当发送相同ID的旧报文时，出现CAN总线错误和仲裁丢失时，旧ID报文不再发送。

在GW模式和TXQueueOverwrite模式下使用该功能时，TXQ的深度（CFDTXQCC0n.TXQDC）应配置为TXQueue中使用的各种ID数加3的值。如果通过GW中的路由访问当TXQ缓冲区已满时，设置CFDTXQSTS.TXQMLT并丢弃发送数据。该功能对标准ID帧有效，对扩展ID帧无效。

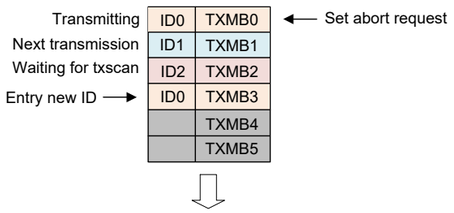
GW模式下TXQ同ID覆盖功能的操作如下图所示。

TXQ0 depth = 6 buffers, ID is 3, TXQ0 GW mode

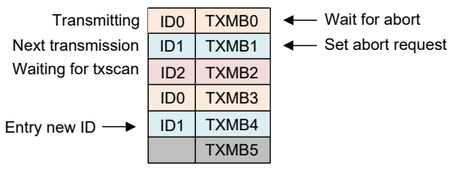
1. Three frames are stored.



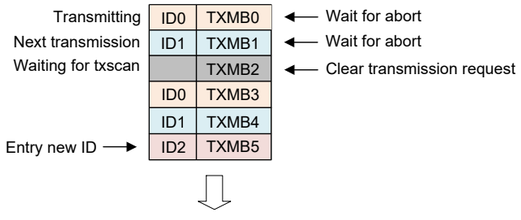
2. ID0 is stored in TXMB3 and abort is set as TXMB0.



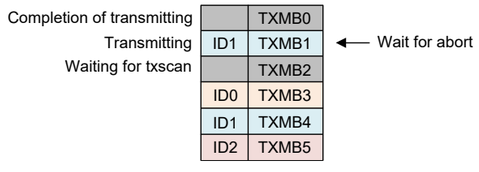
3. ID1 is stored in TXMB4 and abort is set as TXMB1.



4. ID2 is stored in TXMB5 and the transmit request of TXMB2 is cleared.



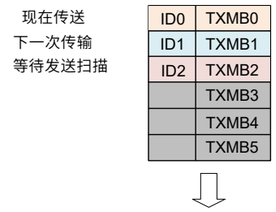
5. Transmission of TXMB0 is complete and transmission of ID1 of TXMB1 is started.



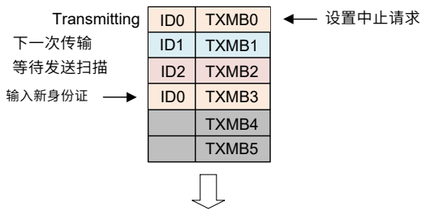
When a system writes in TXQ, it writes in send data, after checking the state of TXQ.

TXQ0深度=6个缓冲区，ID为3，TXQ0GW模式

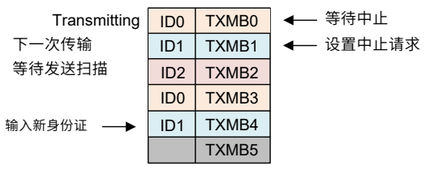
1.存储三帧。



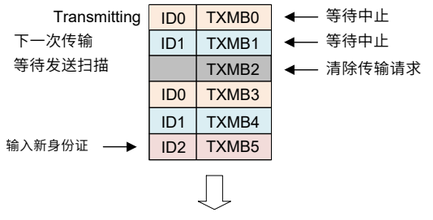
2.ID0存储在TXMB3中，abort设置为TXMB0。



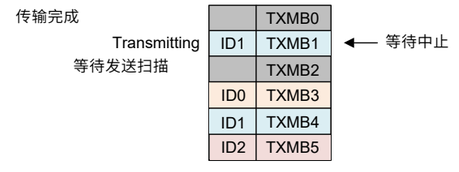
3.ID1存储在TXMB4中，abort设置为TXMB1。



4.ID2存储在TXMB5中，TXMB2的发送请求被清除。



5.TXMB0发送完成，开始发送TXMB1的ID1。



当系统写入TXQ时，它会在检查TXQ的状态后写入发送数据。

Do not access or configure the related TX Message Buffer Control Registers.

The messages stored to the TX Queue access window are internally stored to a free buffer of the TX Queue.

When the buffer is full, no further access should be done to the queue, until it is no longer full. If access is a software write when the buffer of TXQ is full, send data is overwritten.

The TX Queue can be disabled by clearing the TXQE bit in the TX Queue Configuration/Control Register. If this bit is cleared, the TX Queue Empty flag is set as follows:

- Immediately if the message from the TX Queue is neither scheduled for the next transmission nor in transmission
- Following the transmission completion, the detection of an error on the CAN bus, loss of arbitration or transition to Channel or Global Halt mode if the transmission from the TX Queue is already scheduled for transmission or already in transmission.

Note: The TX Queue is disabled only when the Empty flag is set after clearing the TXQE bit for the corresponding TX Queue.

Other possible messages pending from the TX Queue are lost and their transmission must be requested again.

Before TXQE is set again, ensure that the CFDTXQSTSn.TXQEMP bit is set and that there is no pending abort from the TX Queue.

When the TXQE bit is cleared, all messages in the TX Queue buffers are lost and no further message should be stored in the TX Queue.

When a message has been stored to the TX Queue, write 0xFF in the TX Queue Pointer Control Register. This sets the transmit request automatically and changes the internal message buffer pointer to the next free message buffer location of the TX Queue.

Note: If two messages with the same ID are stored in the TX Queue, the order of transmission of these messages can be different from the order in which they were stored in the TX Queue.

To avoid this condition, it is important to confirm that the previous message with the same ID was successfully transmitted before a new message with the same ID is stored in the TX Queue.

If TX Queue Overwrite mode is used, the frame of the same ID is rewritten on a new frame.

For the TX Queue, a dedicated interrupt can be enabled by setting the TXQIE bit of the TX Queue Configuration/Control Register.

The interrupt mode can be configured with the CFDTXQCCn.TXQIM bit of the same register either to generate an interrupt for every transmitted message or for the last transmitted message.

The TX Queue transmission request procedure after configuration is shown in Figure 32.48.

不要访问或配置相关的TX报文缓冲区控制寄存器。

存储到TXQueue访问窗口的消息在内部存储到TXQueue的空闲缓冲区中。

当缓冲区已满时，不应进一步访问队列，直到它不再满为止。如果在TXQ的缓冲区已满时访问是软件写入，则发送数据将被覆盖。

可以通过清除TX队列配置控制寄存器中的TXQE位来禁用TX队列。如果该位清零，则TXQueueEmpty标志设置如下：

- 如果来自TXQueue的消息既没有安排下一次传输也没有在传输中，则立即执行
- 传输完成后，检测到CAN总线错误、仲裁丢失或转换到
  如果来自TX队列的传输已被安排传输或已在传输中，则通道或全局暂停模式。

Note: 只有在清除相应TX的TXQE位后设置Empty标志时，才会禁用TX队列
Queue.

其他可能从TXQueue挂起的消息丢失，必须再次请求它们的传输。

在再次设置TXQE之前，确保CFDTXQSTSn.TXQEMP位已设置并且没有挂起的中止来自
TX Queue.

当TXQE位被清零时，TX队列缓冲区中的所有消息都将丢失，并且不应将更多消息存储在
TX Queue.

当消息已存储到TX队列时，在TX队列指针控制寄存器中写入0xFF。这会自动设置发送请求并将内部消息缓冲区指针更改为TX队列的下一个空闲消息缓冲区位置。

Note: 如果两个具有相同ID的消息存储在TXQueue中，则这些消息的传输顺序可能与它们存储在TXQueue中的顺序不同。

为避免这种情况，重要的是在将具有相同ID的新消息存储到TXQueue之前确认先前具有相同ID的消息已成功传输。

如果使用TXQueueOverwrite模式，相同ID的帧将被重写到新帧上。

对于TX队列，可以通过设置TX队列配置控制的TXQIE位来启用专用中断
Register.

可以使用同一寄存器的CFDTXQCCn.TXQIM位配置中断模式，以便为每个发送的消息或最后发送的消息产生中断。

配置后的TXQueue发送请求流程如图32.48所示。

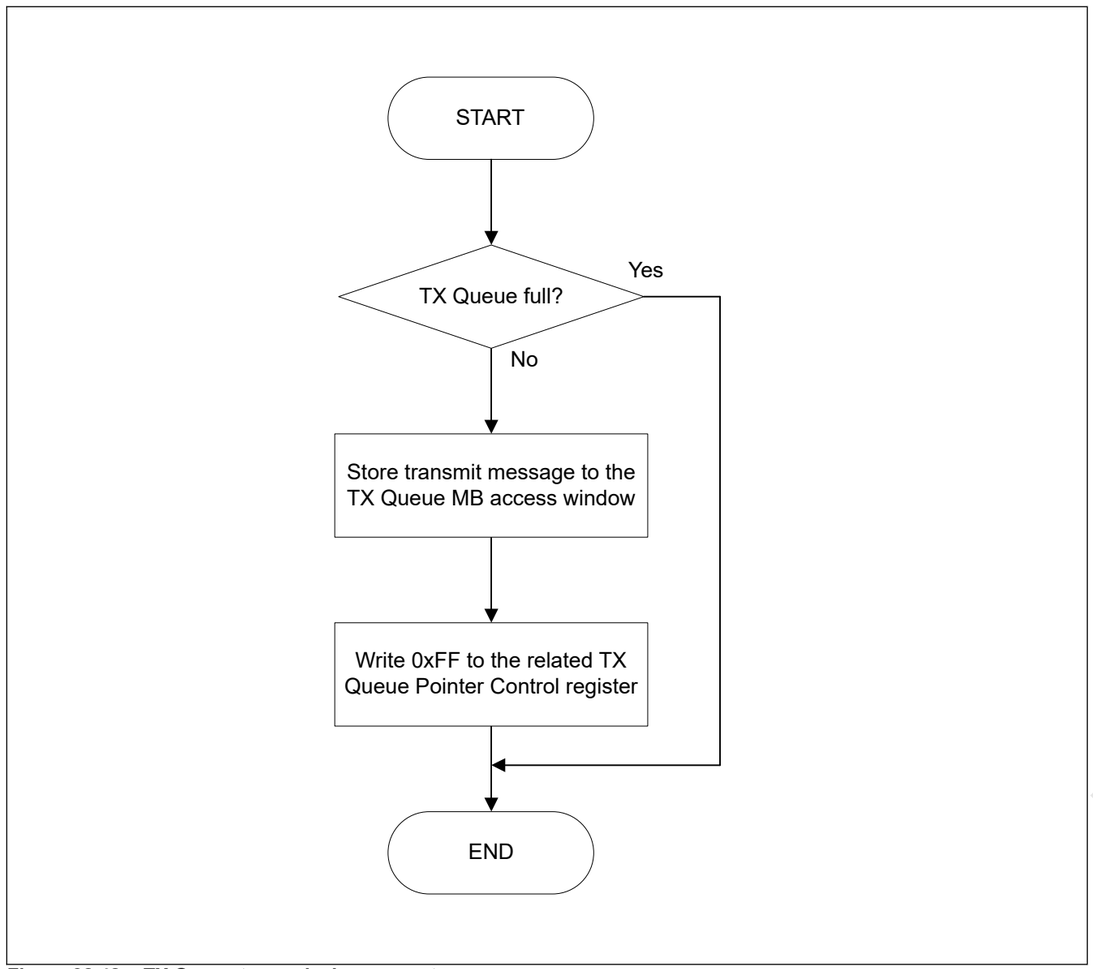


Figure 32.48 TX Queue transmission request

TXQ name	Access window	Range width	Direction	Hardware routing access point	CPU access point	DMA access point	Note
TXQ0	TXMB0	0, 3-16	TXMB0 → TXMB7	Yes	Yes	Yes	When using both TXQ0 and TXQ1, the total number of stages is 8 or less
TXQ1	TXMB7	0, 3-16	TXMB7 → TXMB0	Yes	No	No	
TXQ2	TXMB32	0, 3-16	TXMB32 → TXMB39	Yes	No	No	When using both TXQ2 and TXQ3, the total number of stages is 8 or less
TXQ3	TXMB39	0, 3-16	TXMB39 → TXMB32	No	Yes	Yes	

TXQ0 can use hardware routing access, CPU access, and DMA access. However, these access methods should not be used simultaneously. Only choose one access method.

32.8.2.5 TX History List

The TX History List function records the information of the successfully transmitted message in the TX History List Buffers for each CAN channel. Two TX History List buffers are provided for each CAN channel and each THL buffer can store up to 16 TX History List entries for a CAN channel.

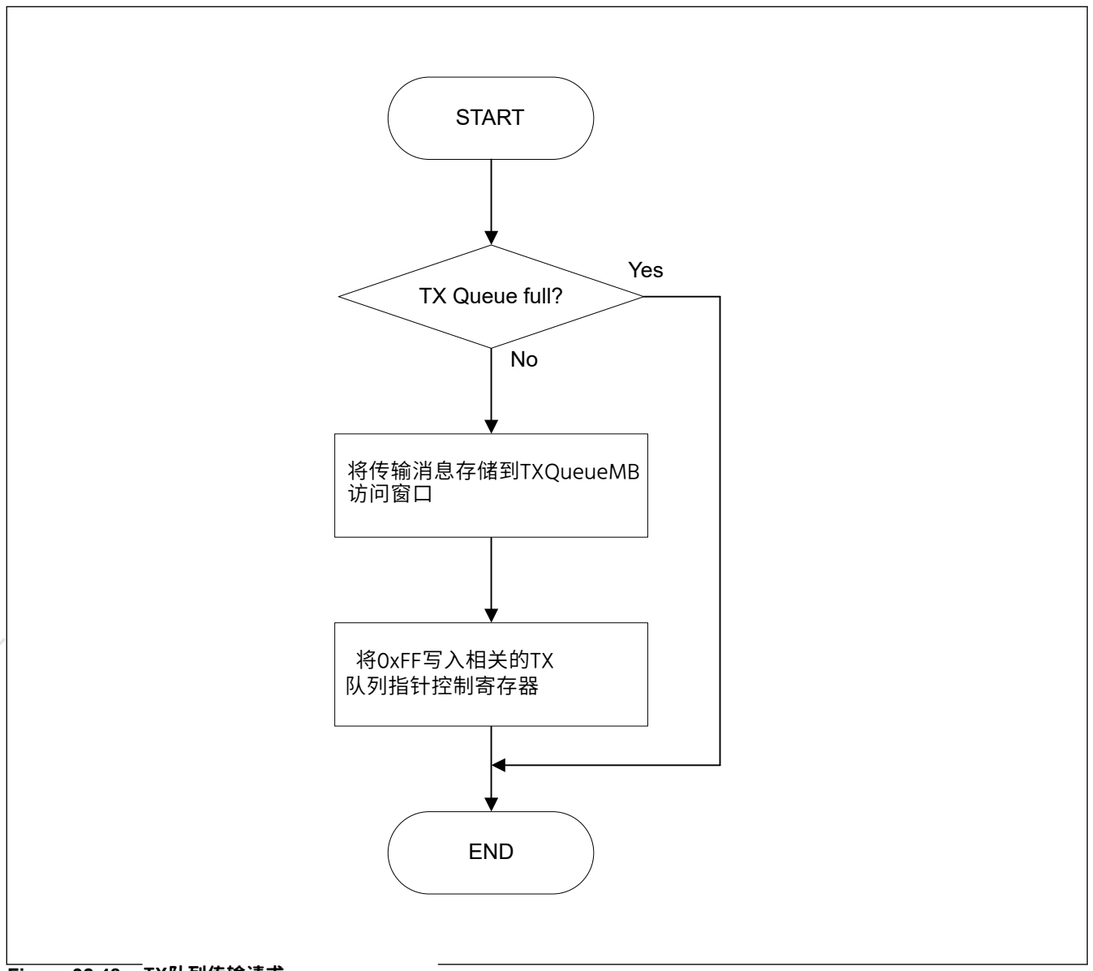


Figure 32.48 TX队列传输请求

TXQ name	访问窗口	范围宽度	Direction	硬件路由接入点	CPU访问点	DMA访问点	Note
TXQ0	TXMB0	0, 3-16	TXMB0 → TXMB7	Yes	Yes	Yes	当同时使用TXQ0和TXQ1，总级数为8或更少
TXQ1	TXMB7	0, 3-16	TXMB7 → TXMB0	Yes	No	No	
TXQ2	TXMB32	0, 3-16	TXMB32 → TXMB39	Yes	No	No	当同时使用TXQ2和TXQ3，总级数为8或更少
TXQ3	TXMB39	0, 3-16	TXMB39 → TXMB32	No	Yes	Yes	

TXQ0可以使用硬件路由访问、CPU访问和DMA访问。但是，这些访问方法不应同时使用。只选择一种访问方法。

32.8.2.5 交易历史列表

TXHistoryList功能将成功传输的报文信息记录在每个CAN通道的TXHistoryListBuffers中。为每个CAN通道提供两个TX历史列表缓冲区，每个THL缓冲区可以为一个CAN通道存储多达16个TX历史列表条目。

The CFDTHLCCn.THLDTE bit of the TX History List Configuration/Control Register can be used to configure if only message information from TX FIFOs or TX Queue is stored, or if all transmit message information from TX Queue, TX FIFO, or normal TX message buffers is stored in the TX History List for a CAN channel.

When a CFDTHLCCn.THLDGE bit is set, the information on all the frames transmitted in Gateway mode is stored in TX History List. Each transmit message can be individually configured for acceptance to the TX History List with the CFDCFID.THLEN bit in the Message Buffer Pointer Register.

The message information is stored to the TX History List Buffer of a CAN channel after the message is successfully transmitted on that CAN channel.

Storing to the list is not synchronized with the status of CFDTMSTSn.TMTRF[1:0] bits in the TX Message Buffer Status Register.

Due to internal processing, the storage to the list can happen with a delay after the successful transmission indication.

Storing the TX History List data can be recognized by the condition that the THLIF is set to 1 when the THLIE bit is configured to 1 or when the TX History List counter CFDTHLSTSn.THLMC[5:0] is increased.

The delay time is dependent on the number of channels due to internal processing.

- Maximum delay time from setting the CFDTMSTSn.TMTRF to store the TX History List data is 224 peripheral bus clock cycles.

The History list records the following information of a transmitted message:

- Buffer type:
  - 001: TX Message Buffer
  - 010: TX FIFO
  - 100: TX Queue
- Buffer number:
  TX message buffer, TX Queue message buffer or TX message buffer link for the Common FIFO buffer from which transmission occurred. The number depends on the buffer type. See Table 32.23.
- Transmission ID:
  Transmission pointer stored in the transmission message
- Transmit timestamp:
  Message timestamp captured at capture point as configured by CFDGFDCFG.TSCCFG.
- Transmission information label:
  Transmission information label stored in the transmission message.
- Transmit gateway buffer indication:
  When data is transmitted from gateway, CFDTHLACC0n.TGW bit is set to 1.

TX历史列表配置控制寄存器的CFDTHLCCn.THLDTE位可用于配置是否仅存储来自TXFIFO或TX队列的报文信息，或者是否存储了来自TXQueue、TXFIFO或正常TX报文缓冲区的所有发送报文信息存储在CAN通道的TX历史列表中。

当CFDTHLCCn.THLDGE位置位时，在网关模式下传输的所有帧的信息都存储在TX中
历史列表。每个发送消息都可以单独配置为接受到TX历史列表，其中
消息缓冲区指针寄存器中的CFDCFID.THLEN位。

在CAN通道上成功传输消息后，消息信息将存储到CAN通道的TX历史列表缓冲区。

存储到列表与TX消息缓冲区状态中CFDTMSTSn.TMTRF[1:0]位的状态不同步
Register.

由于内部处理，在成功传输指示后存储到列表可能会有延迟。

当THLIE位配置为1或TX历史列表计数器CFDTHLSTSn.THLMC[5:0]增加时，THLIF设置为1的条件可以识别存储TX历史列表数据。

由于内部处理，延迟时间取决于通道数。

●从设置CFDTMSTSn.TMTRF到存储TXHistoryList数据的最大延迟时间为224个外设总线时钟周期。

历史列表记录传输消息的以下信息：

- Buffer type:
  001：TX消息缓冲区
  - 010: TX FIFO
  - 100: TX Queue
- Buffer number:
  用于发生传输的通用FIFO缓冲区的TX消息缓冲区、TX队列消息缓冲区或TX消息缓冲区链接。数量取决于缓冲区类型。见表32.23。
- Transmission ID:
  传输消息中存储的传输指针
- Transmit timestamp:
  在CFDGFDCFG.TSCCFG配置的捕获点捕获的消息时间戳。

●传输信息标签：
传输信息标签存储在传输消息中。

●发送网关缓冲区指示：
从网关发送数据时，CFDTHLACC0n.TGW位设置为1。

Table 32.23 TX History List Buffer number entry

BT[2:0] Buffer Type		
001b	**101b**	**100b**
TX Message Buffer	**TX FIFO**	**TX Queue**
TXMB0	Number shown corresponds to the common FIFO. TX Message Buffer Link CFTML of the related Common FIFO configuration	Number shown corresponds to the message buffer belonging to the TX Queue for which the frame was transmitted
TXMB1		
TXMB2		
TXMB3		
TXMB4		
TXMB5		
TXMB6		
TXMB7		
TXMB32		
TXMB33		
TXMB34		
TXMB35		
TXMB36		
TXMB37		
TXMB38		
TXMB39		

The Transmission ID entry is used to identify which message of a TX FIFO or TX Queue has been successfully transmitted because the TX FIFO or TX Queue number alone is not sufficient.

Therefore, a unique number can be attached to each transmission message stored in a TX FIFO or TX Queue. This unique identification number should be written to the CFDCFFDCSTSn.CFPTR[15:0] part of the Common FIFO Access Pointer Register for a TX FIFO or to the CFDTMFDCTRn.TMPTR[15:0] part of the TX Message Buffer Pointer Register of the TX Queue access window message buffer.

When the message is successfully transmitted, this identification number is stored together with the other message related information to the TX History List and can be read using the Transmission ID (TID) of the TX History List Access Register.

Also, for normal TX message buffers, the CFDTMFDCTRn.TMPTR[15:0] part of the TX Message Buffer Pointer Register is stored in the Transmission History List and the information label is the same.

Figure 32.48 shows a transmission preparation flow when TX History List is used.

Read access to the TX History List Access Register is done for every single entry.

After reading one entry, 0xFF must be written to the corresponding TX History List Pointer Control Register to be able to access the next entry until TX History List is empty.

Figure 32.49 shows an example flow for processing the TX History List information.

The TX History Lists have dedicated interrupts, which can be configured with the CFDTHLCCn.THLIM bit of the corresponding TX History List Configuration/Control Registers and enabled with the CFDTHLCCn.THLIE bit of the same registers, either to generate an interrupt when the History List reached a filling level of 75% or for every new TX History List entry.

An entry lost indication is flagged by the CFDTHLSTSn.THLELT bit in the TX History List Status Register. The status of this bit is also shown by the THLES bit in the Global Error Flag Register.

Table 32.23 TX历史列表缓冲区编号条目

BT[2:0]缓冲器类型		
001b	**101b**	**100b**
TX消息缓冲区	**TX FIFO**	**TX Queue**
TXMB0	显示的数字对应于常见的FIFO。TXMessageBufferLinkCFTML的相关 通用FIFO配置	显示的数字对应于属于发送帧的TX队列的消息缓冲区
TXMB1		
TXMB2		
TXMB3		
TXMB4		
TXMB5		
TXMB6		
TXMB7		
TXMB32		
TXMB33		
TXMB34		
TXMB35		
TXMB36		
TXMB37		
TXMB38		
TXMB39		

传输ID条目用于识别TXFIFO或TXQueue的哪个消息已成功传输，因为仅TXFIFO或TXQueue编号是不够的。

因此，可以将唯一编号附加到存储在TXFIFO或TX队列中的每个传输消息。此唯一标识号应写入TXFIFO的通用FIFO访问指针寄存器的CFDCFFDCSTSn.CFPTR[15:0]部分，或写入TXFIFO的TX消息缓冲区指针寄存器的CFDTMFDCTRn.TMPTR[15:0]部分德克萨斯州

队列访问窗口消息缓冲区。

当报文成功发送时，该标识号与其他报文相关信息一起存储到TX历史列表中，并可使用TX历史列表访问寄存器的发送ID(TID)读取。

此外，对于普通的TX报文缓冲区，TX报文缓冲区指针寄存器的CFDTMFDCTRn.TMPTR[15:0]部分存储在传输历史列表中，并且信息标签相同。

图32.48显示了使用TXHistoryList时的传输准备流程。

对TX历史列表访问寄存器的读取访问针对每个条目进行。

读取一个条目后，必须将0xFF写入相应的TX历史列表指针控制寄存器，才能访问下一个条目，直到TX历史列表为空。

图32.49显示了处理TX历史列表信息的示例流程。

TX历史列表具有专用中断，可以使用相应的TX历史列表配置控制寄存器的CFDTHLCCn.THLIM位进行配置，并使用相同寄存器的CFDTHLCCn.THLIE位启用，以便在达到历史列表时生成中断75%的填充水平或每个新的TX历史列表条目。

条目丢失指示由TX历史列表状态寄存器中的CFDTHLSTSn.THLELT位标记。该位的状态也由全局错误标志寄存器中的THLES位显示。

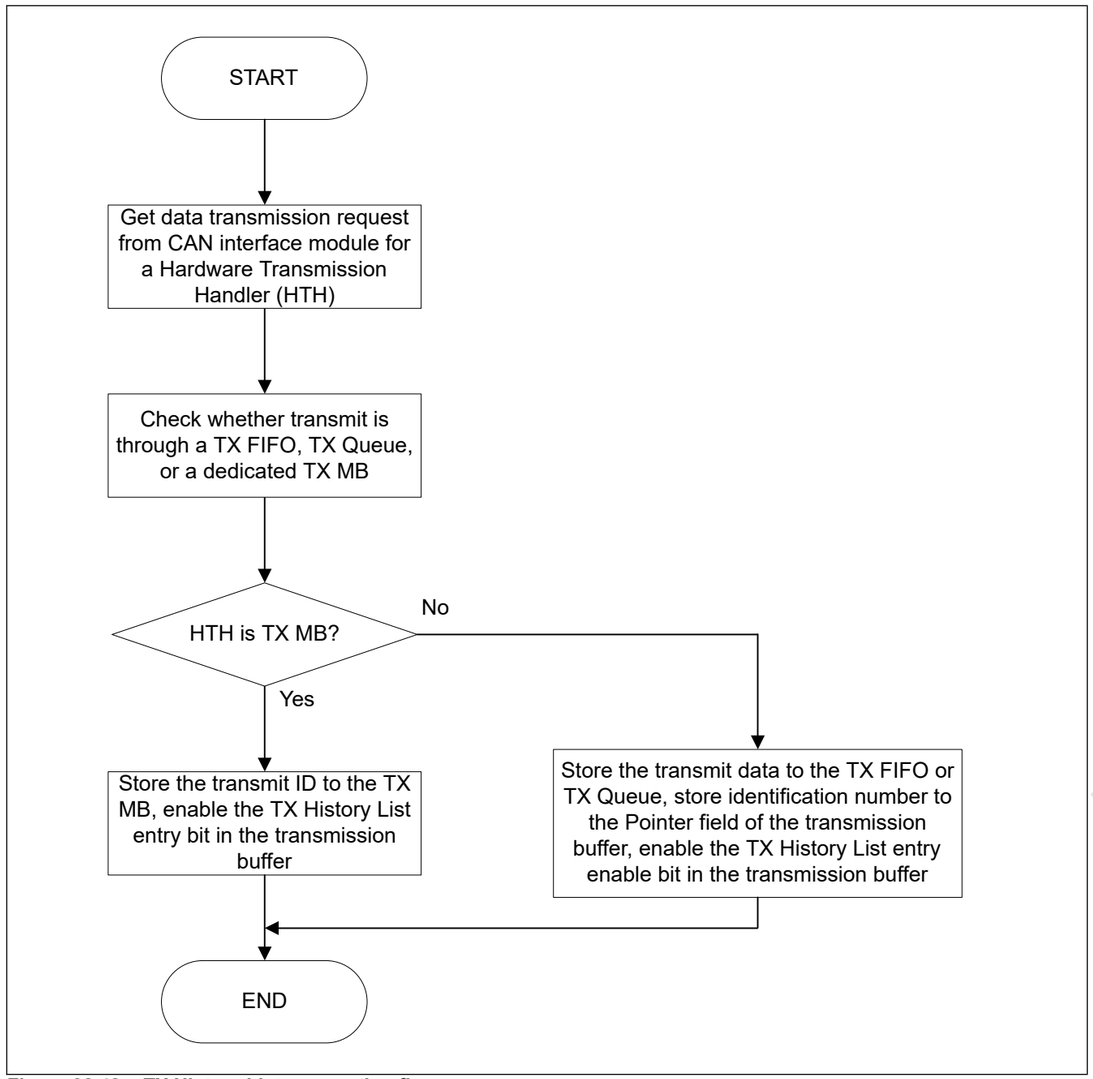


Figure 32.48 TX History List preparation flow

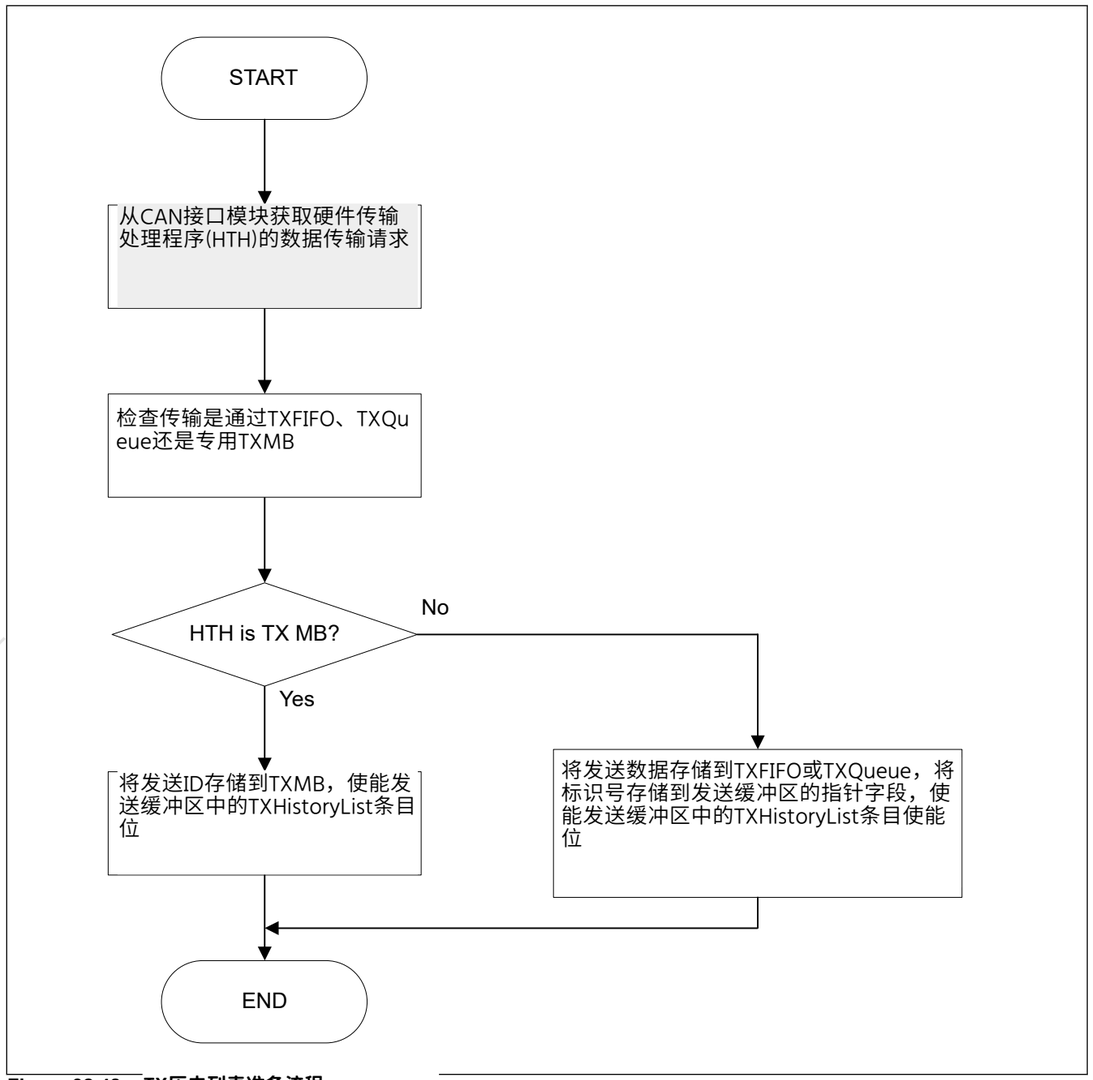


Figure 32.48 TX历史列表准备流程

RA生态工作室

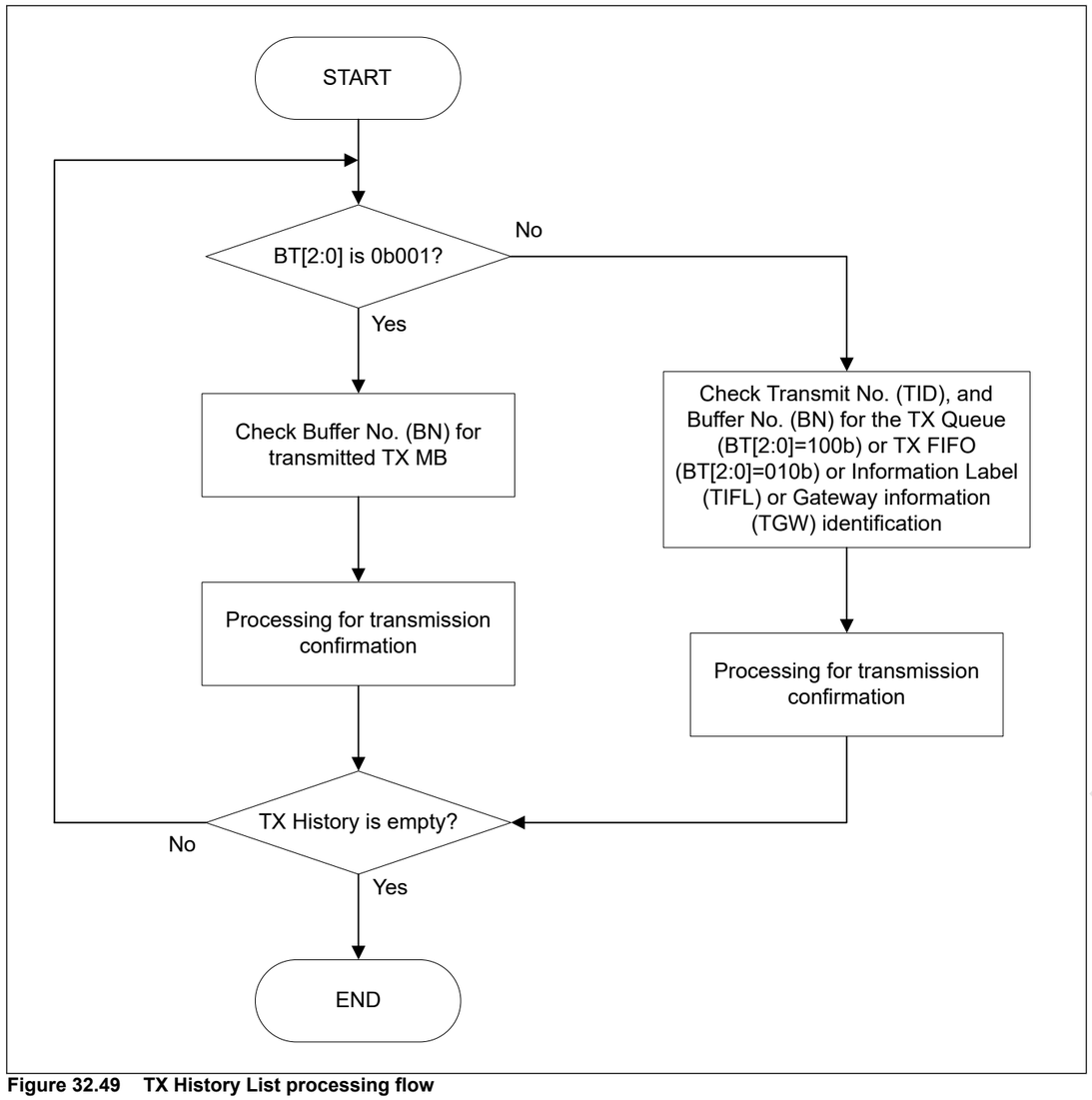


Figure 32.49 TX History List processing flow

32.8.2.6 TX Data Padding

This chapter is not valid for classical CAN.

If the data length code (DLC) of the transmitting message has a higher number of data bytes than the buffer size, the data bytes beyond the restricted range are replaced by bytes with the value of 0xCC.

This can happen for Common FIFOs configured as (TX or GW mode) when the transmit message DLC is higher than the CFDCFCCn.CFPLS.

This can also happen in FD only mode, if a Classical frame is configured with a DLC bigger than 8.

32.9 Test Mode

The CAN-FD module can be configured into test modes to allow testing of certain features. These features are provided only for special purposes and care must be taken when configuring the CAN-FD module in test modes.

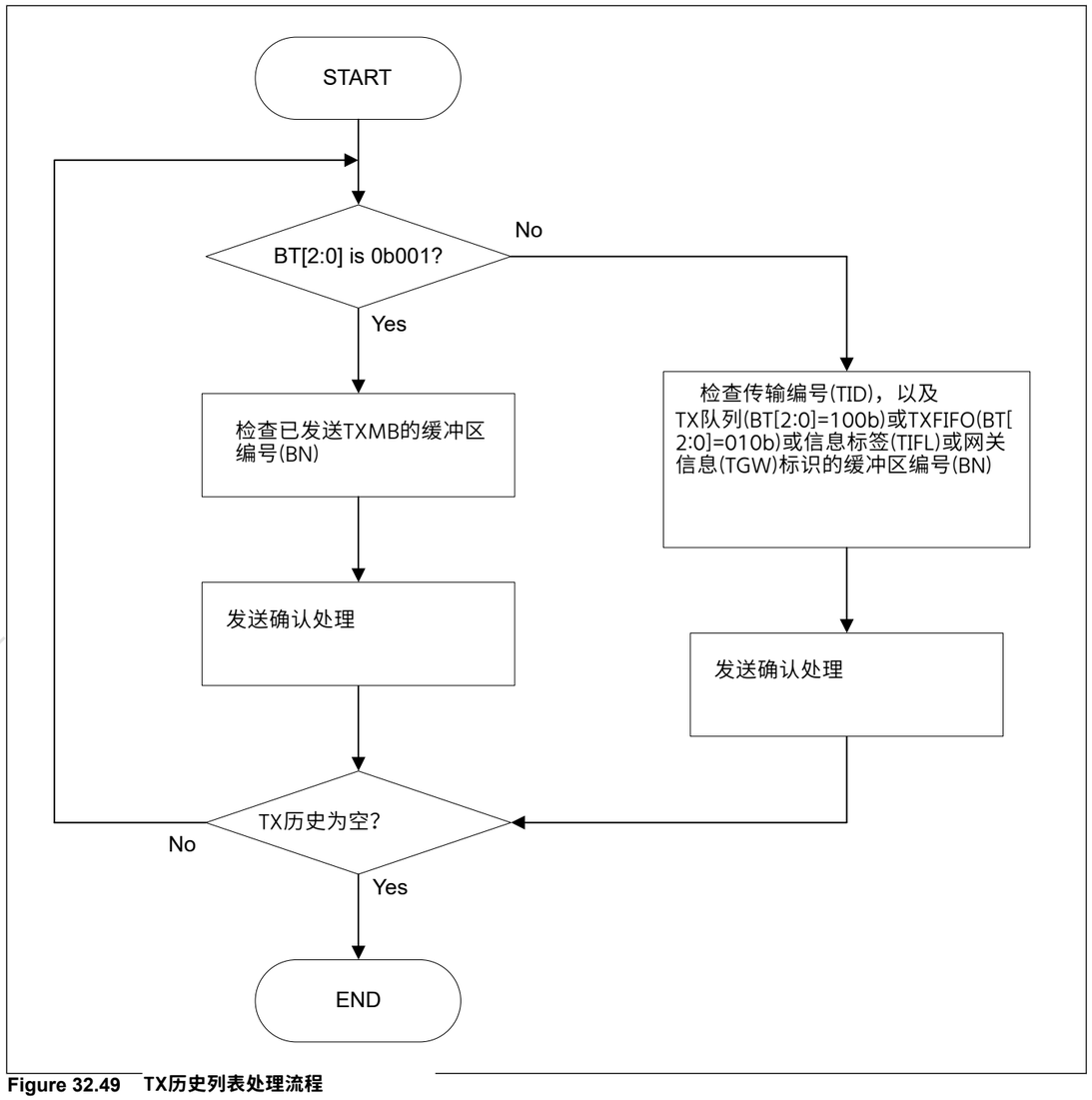


Figure 32.49 TX历史列表处理流程

32.8.2.6 TX数据填充

本章不适用于经典CAN。

如果发送报文的数据长度码(DLC)的数据字节数大于缓冲区大小，则超出限制范围的数据字节将替换为值为0xCC的字节。

当发送消息DLC高于
CFDCFCCn.CFPLS.

如果经典帧配置了大于8的DLC，这也可能发生在仅FD模式下。

32.9 测试模式

CAN-FD模块可以配置为测试模式以允许测试某些功能。这些功能仅用于特殊目的，在测试模式下配置CAN-FD模块时必须小心。

Note: All test modes are mutually exclusive unless it is explicitly stated that some functions can be enabled across other test modes.

Do not enable any combination of the various test modes specified in this section.

The test modes can be broadly split into 2 groups:

- Channel specific test modes
- Global test modes.

32.9.1 Channel Specific Test Modes

Each CAN channel can be configured into the following test modes:

- Basic test mode
- Listen-only mode
- Self-test mode 0 (External loop back mode)
- Self-test mode 1 (Internal loop back mode)
- Restricted operation mode.

32.9.1.1 Basic Test Mode

The basic test mode should be used when there is requirement for a particular test setting to be enabled other than when in Listen-only and Self-test modes.

32.9.1.2 Listen-only Mode

The ISO 11898-1 recommends an optional bus-monitoring mode. In this mode, the CAN channel is able to receive valid data frames and valid remote frames. However, it sends only recessive bits on the CAN bus and is not allowed to transmit. If the CAN engine is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is routed internally so that the CAN engine monitors this as dominant. The external TX pin remains in recessive state.

This mode can be used for baud rate detection. In this mode, an error interrupt is generated if a bus error occurs and the interrupt is enabled.

In this mode, it is not permitted to request transmission from any normal TX message buffer or TX/GW FIFO of this channel.

Note: If a message is stored in GW FIFO or routing TXQ, ensure that the transmitting channel is not in Listen-only mode so that transmission is not requested for this channel from the GW FIFO or routing TXQ.

Note: 所有测试模式都是互斥的，除非明确声明某些功能可以跨其他测试模式启用。

不要启用本节中指定的各种测试模式的任何组合。

测试模式可以大致分为两组：

●通道特定的测试模式

●全局测试模式。

32.9.1 通道特定测试模式

每个CAN通道都可以配置为以下测试模式：

●基本测试模式

- Listen-only mode

●自检模式0（外部环回模式）

●自检模式1（内部环回模式）

●受限操作模式。

32.9.1.1 基本测试模式

当需要启用特定测试设置时，应使用基本测试模式，而不是在只听和自测模式。

32.9.1.2 Listen-only Mode

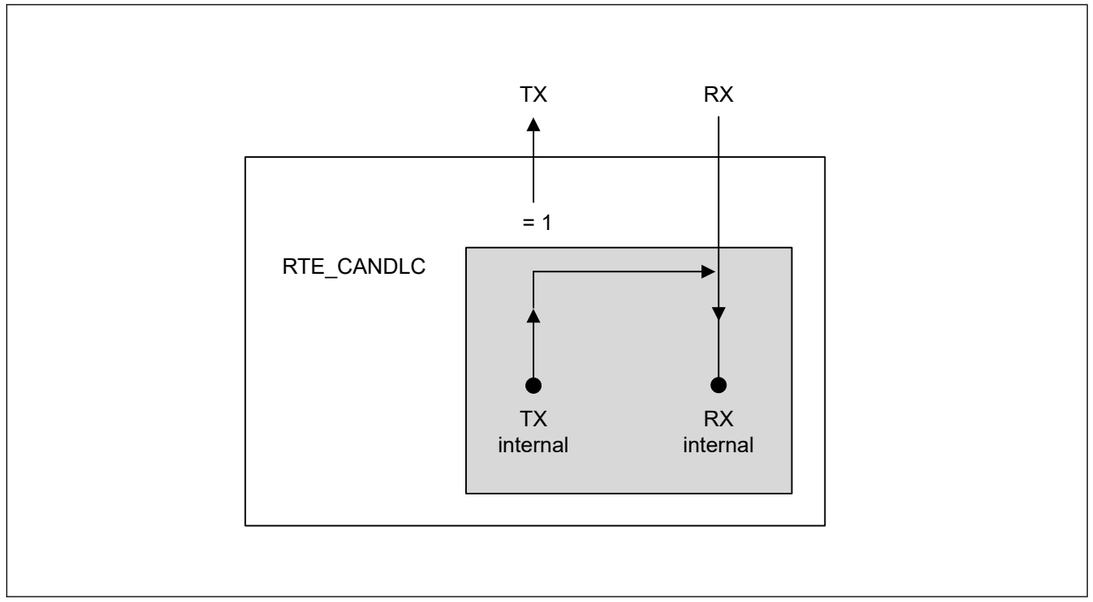
ISO11898-1推荐一种可选的总线监控模式。在此模式下，CAN通道能够接收有效的数据帧和有效的远程帧。但是，它只在CAN总线上发送隐性位，不允许发送。

如果CAN引擎需要发送显性位（ACK位、过载标志、活动错误标志），则该位在内部路由，以便CAN引擎将其监控为显性。外部TX引脚保持隐性状态。

该模式可用于波特率检测。在此模式下，如果发生总线错误并启用中断，则会产生错误中断。

在此模式下，不允许从该通道的任何正常TX消息缓冲区或TXGWFIFO请求传输。

Note: 如果消息存储在GWFIFO或路由TXQ中，请确保发送通道不处于Listen-only模式，以便不会从GWFIFO或路由TXQ请求此通道的传输。

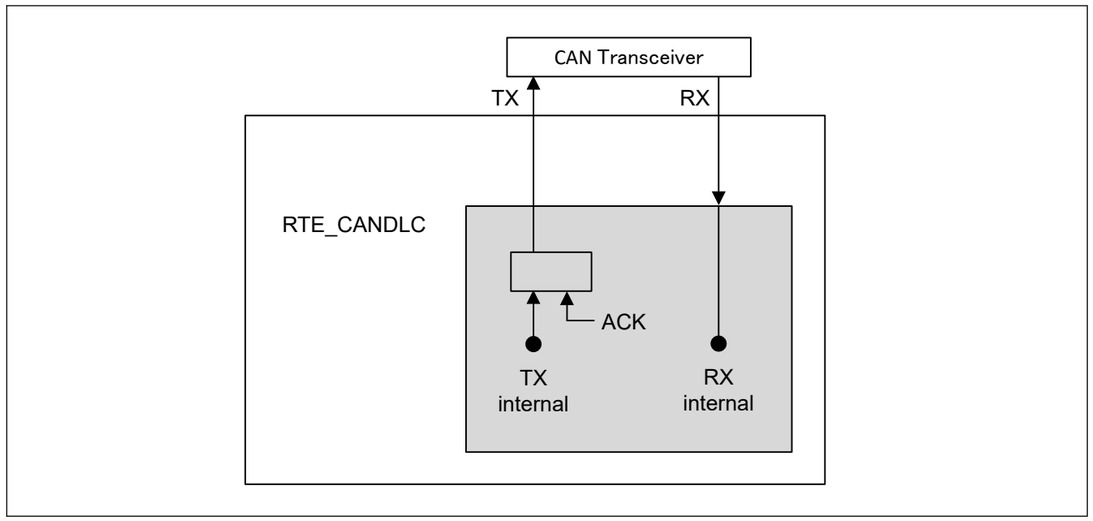


32.9.1.3 Self-test Mode 0 (External loopback mode)

In Self-test mode 0, the CAN engine treats its own transmitted messages as received messages through the CAN transceiver and stores them into its receive message buffers.

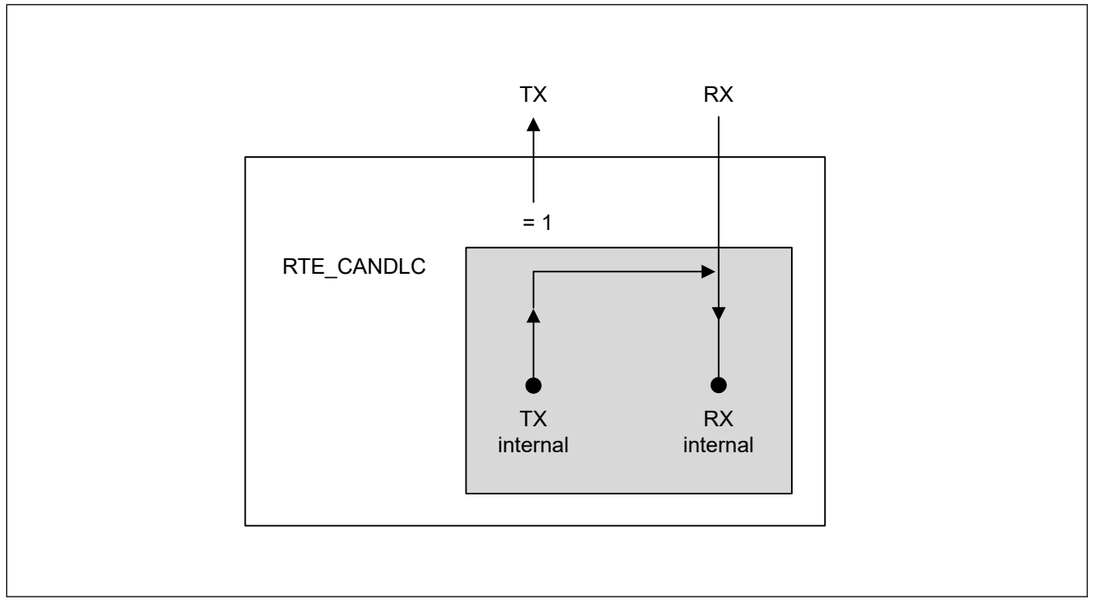
To be independent from external stimulation, the engine generates its own Acknowledge bit.

This test can be used for CAN transceiver tests and the RX/TX pins should be connected to the transceiver.



32.9.1.4 Self-test Mode 1 (Internal loopback mode)

In Self-test mode 1, the CAN engine treats its own transmitted messages as received messages and stores them into the receive buffer. This mode is provided for self-test functions. To be independent from external stimulation, the CAN engine generates its own Acknowledge bit. In this mode the CAN engine performs an internal feedback from TX internal to RX internal. The actual value of the external RX input is disregarded by the CAN engine.

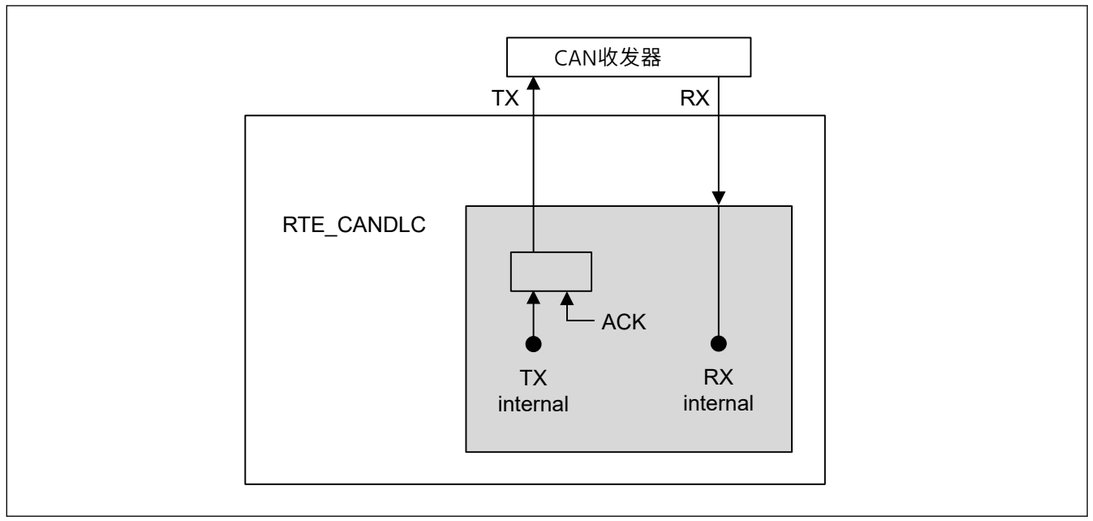


32.9.1.3 Self-test Mode 0 (External loopback mode)

在自检模式0中，CAN引擎将自己发送的消息视为通过CAN收发器接收到的消息，并将它们存储到其接收消息缓冲区中。

为了独立于外部刺激，引擎会生成自己的确认位。

此测试可用于CAN收发器测试，并且RXTX引脚应连接到收发器。

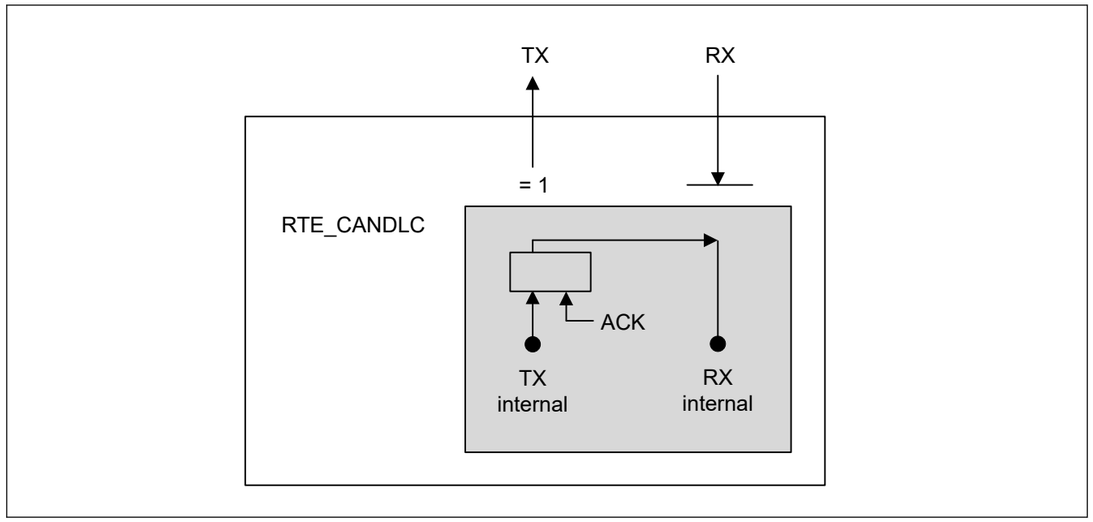


32.9.1.4 Self-test Mode 1 (Internal loopback mode)

在自检模式1中，CAN引擎将自己发送的消息视为接收的消息，并将它们存储到接收缓冲区中。此模式用于自检功能。为了独立于外部刺激，CAN引擎生成自己的确认位。在这种模式下，CAN引擎执行从TX内部到RX内部的内部反馈。CAN引擎忽略外部RX输入的实际值。

The external TX pin outputs only recessive bits. The RX/TX pins do not need to be connected to the CAN bus or any external device.

Note: The channel pins are also disconnected from the internal CAN bus communication line.



32.9.1.5 Restricted Operation Mode

This chapter is not valid for classical CAN.

In Restricted operation mode, the CAN node is able to receive valid data and remote frames generating the Acknowledge bit.

Active error or overload frames cannot be transmitted, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication after an error or overload condition occurs.

Additionally, the Receive and Transmit Error Counter (REC and TEC) are frozen independently from the occurrence of errors. The mode is specified in ISO 11898-1 and the setting of transmit request is permitted.

32.9.2 Global Test Modes

The CAN-FD module can be configured into the following test modes:

- RAM test mode
- Internal CAN bus communication mode
- CRC error test

The test modes in the following table are protected by a special software procedure to enable the mode. This software procedure enables write access to the test mode by a specific unlock key as shown in the table.

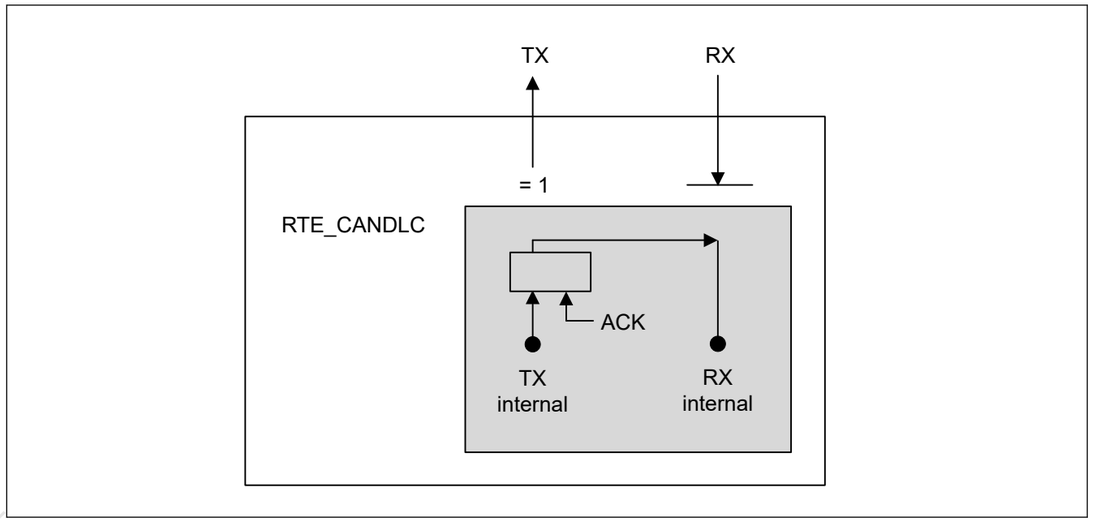
Test mode	Unlock key 1	Unlock key 2
RAM test mode	0x7575	0x8A8A

If the software sequence of the two consecutive unlock key write accesses (half-word or word access) is interrupted by any other write access to the register or if incorrect data is written to the Global Unlock Key Register, the corresponding test mode cannot be set and the sequence must be restarted.

After the two unlock key write accesses, the next write access should be to set the corresponding test mode enable bit. If this is not followed, the unlock mechanism reset and the test mode enable bit cannot be set and the unlock sequence must be restarted.

外部TX引脚仅输出隐性位。RXTX引脚不需要连接到CAN总线或任何外部设备。

Note: 通道引脚也与内部CAN总线通信线路断开。



32.9.1.5 受限操作模式

本章不适用于经典CAN。

在受限操作模式下，CAN节点能够接收有效数据和生成确认位的远程帧。

无法传输主动错误或过载帧，而是在发生错误或过载情况后等待总线空闲条件的出现以重新同步到CAN通信。

此外，接收和发送错误计数器（REC和TEC）独立于错误发生而被冻结。模式在ISO11898-1中指定，允许设置发送请求。

32.9.2 全局测试模式

CAN-FD模块可配置为以下测试模式：

- RAM测试模式
- 内部CAN总线通讯方式
- CRC错误测试

下表中的测试模式受特殊软件程序保护以启用该模式。该软件程序允许通过特定的解锁密钥对测试模式进行写访问，如表中所示。

测试模式	解锁钥匙1	解锁钥匙2
RAM测试模式	0x7575	0x8A8A

如果两次连续的解锁密钥写访问（半字或字访问）的软件序列被对寄存器的任何其他写访问中断，或者如果向全局解锁密钥寄存器写入不正确的数据，则无法设置相应的测试模式并且必须重新启动序列。

在两次解锁密钥写访问之后，下一次写访问应该是设置相应的测试模式使能位。如果不遵循，解锁机制复位和测试模式使能位不能设置，解锁序列必须重新启动。

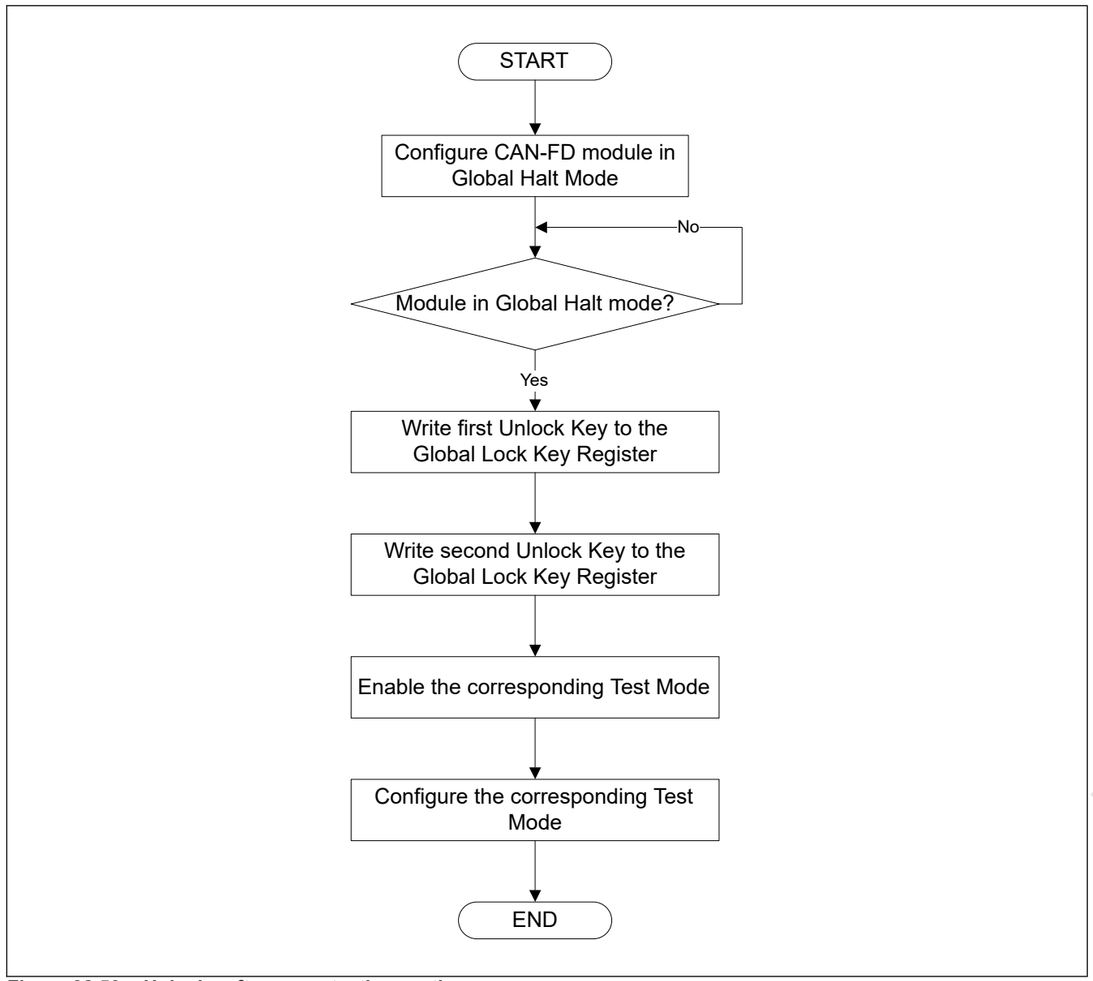


Figure 32.50 Unlock software protection routine

32.9.2.1 RAM Test Mode

The CAN-FD module can be configured in RAM test mode by setting the CFDGTSTCTR.RTME bit in the Global Test Control Register when the corresponding lock key is previously written. This is a special test mode, in which, the complete RAM area can be accessed.

Note: The actual RAM size is bigger than the RAM area initialized after a hardware reset. Therefore, ECC error flag (of the ECC macro) may be set if CPU reads data from this uninitialized RAM area while CAN-FD module is in RAM test mode.

In this mode, the RAM area is split into number of pages (pn) of 256 bytes, each which can be accessed with the CFDRPGACCn register.

The page should be selected for read/write access by writing to the CFDGTSTCFG.RTMPS[9:0] bits in the Global Test Control Register. Data can then be read from or written in to the RAM Test Page Access Registers.

Figure 32.51 shows the structure of the pages in the RAM when performing a RAM test mode.

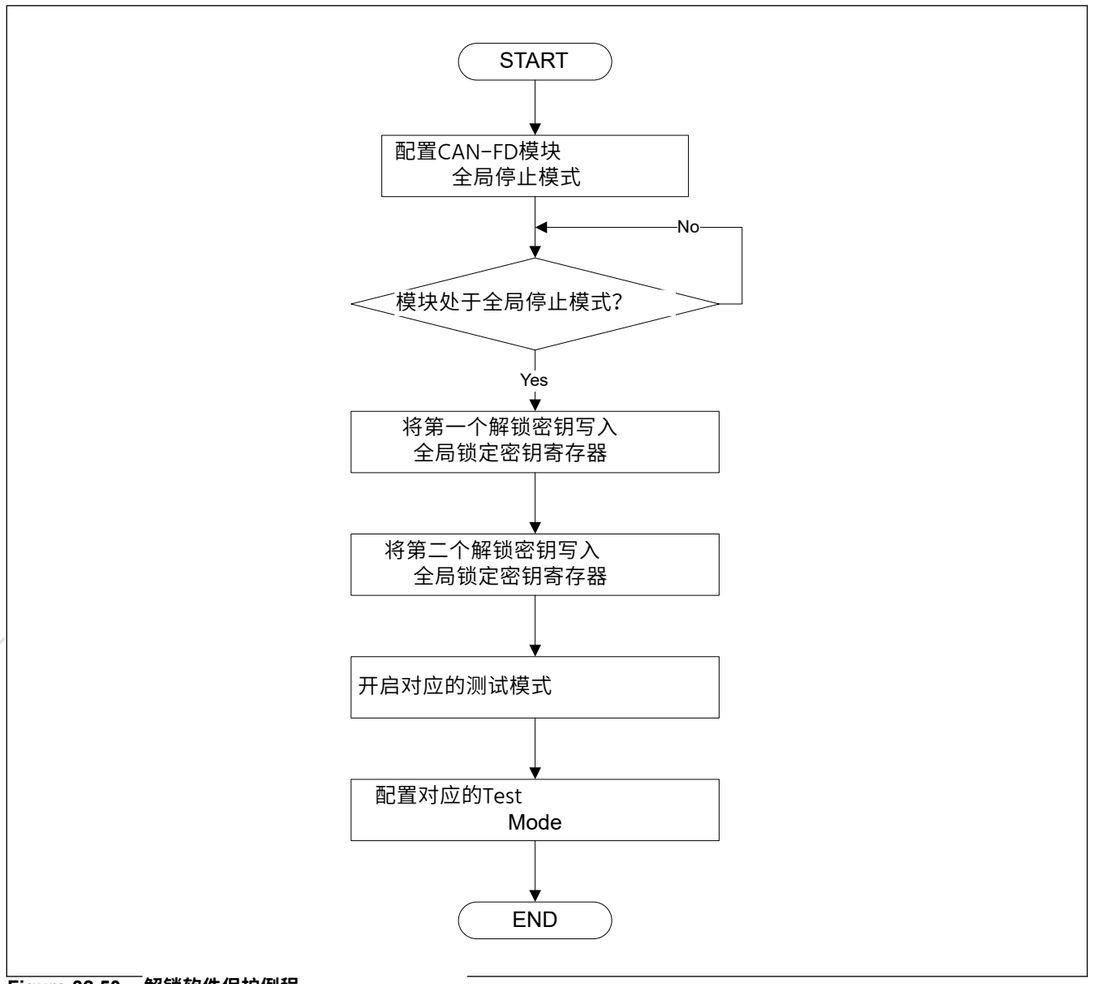


Figure 32.50 解锁软件保护例程

32.9.2.1 RAM测试模式

CAN-FD模块可通过设置GlobalTest中的CFDGTSTCTR.RTME位配置为RAM测试模式控制寄存器，当相应的锁定键先前被写入时。这是一种特殊的测试模式，其中，完整的可以访问RAM区域。

Note: 实际RAM大小大于硬件复位后初始化的RAM区域。因此，ECC错误标志（的如果在CAN-FD模块处于RAM测试模式时CPU从该未初始化的RAM区域读取数据，则可以设置ECC宏。

在这种模式下，RAM区域被分成256字节的页数(pn)，每个页都可以通过CFDRPGACCn register.

应通过写入全局测试中的CFDGTSTCFG.RTMPS[9:0]位来选择该页面进行读写访问控制寄存器。然后可以从RAM测试页访问寄存器读取或写入数据。

图32.51显示了执行RAM测试模式时RAM中的页面结构。

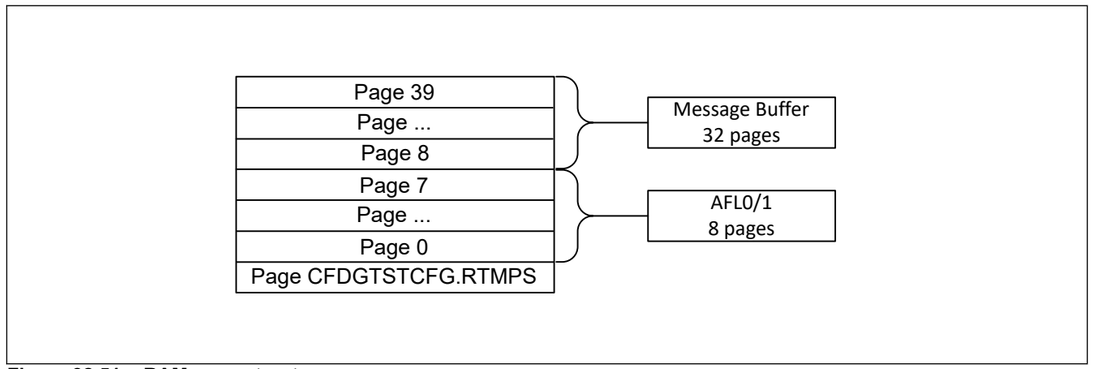


Figure 32.51 RAM page structure

The total available RAM size for a 2-CAN channel version is 2048 bytes for the AFL RAM and 8192 bytes for the Message Buffer RAM.

AFL RAM0/1 can treat RAM test mode as one RAM.

The pn and CFDGTSTCFG.RTMPS[9:0] values for the AFL and MB RAMs are calculated in the following way:

pn = ceil (total RAM size in bytes / number of bytes per page)

- AFL RAM:
  pn = ceil (2048 / 256) = 8 pages
  CFDGTSTCFG.RTMPS[9:0] = 0 to 7 (0x00F) inclusive
- MB RAM:
  pn = ceil (8192 / 256) = 32 pages
  CFDGTSTCFG.RTMPS[9:0] = 8 to 39 (0x27) inclusive

Figure 32.52 shows the software flow for RAM test mode.

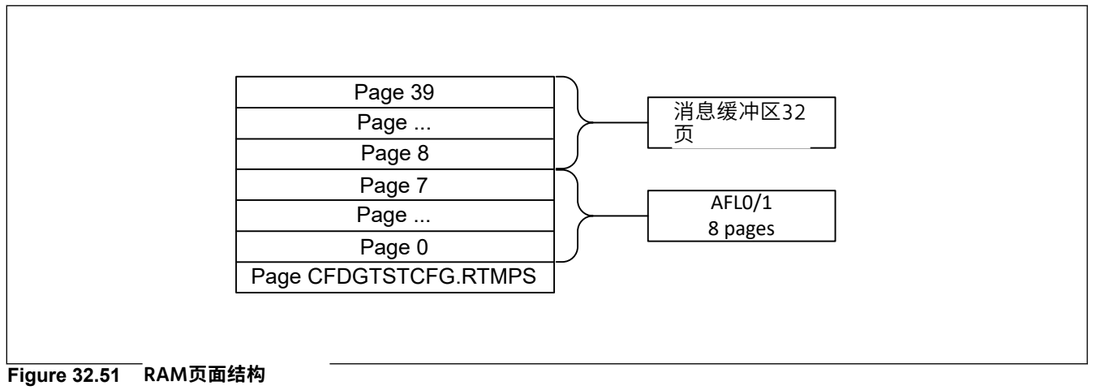


Figure 32.51 RAM页面结构

2-CAN通道版本的总可用RAM大小为AFLRAM为2048字节，消息为8192字节缓冲RAM。

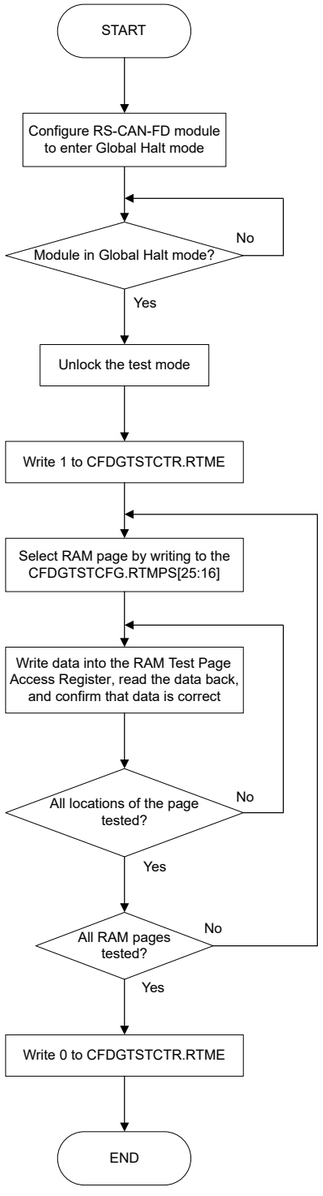
AFLRAM01可以将RAM测试模式视为一个RAM。

AFL和MBRAM的pn和CFDGTSTCFG.RTMPS[9:0]值按以下方式计算：

pn=ceil（以字节为单位的总RAM大小每页的字节数）

- AFL RAM:
  pn=ceil(2048256)=8页CFDGTSTCFG.RTMPS[9:0]=0到7(0x00F)（含）
- MB RAM:
  pn=ceil(8192256)=32页CFDGTSTCFG.RTMPS[9:0]=8到39(0x27)（含）

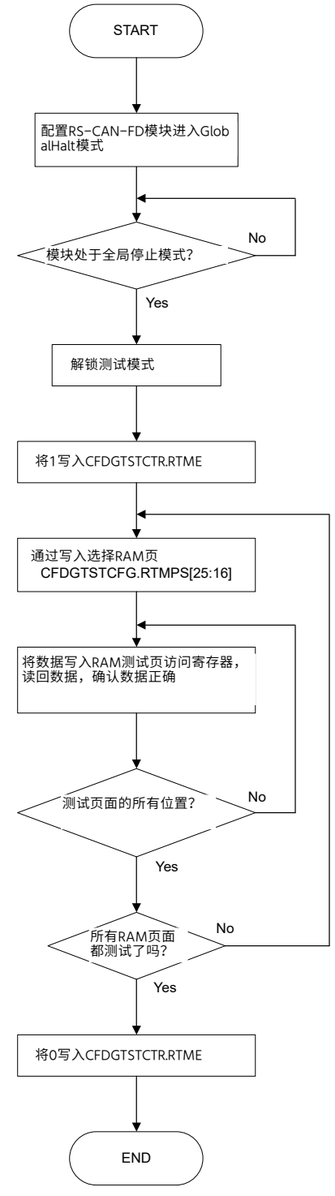
图32.52显示了RAM测试模式的软件流程。



Note 1. Change into the following status before changing to RAMTEST.
- Cancel of a request for transmission.
- Disable of all the FIFO and TXQ.
- Clear of the receiving flag for a receiving buffer.

Figure 32.52 Software flow for RAM test mode

To exit this test mode, the CFDGTSTCTR.RTME bit must be cleared. The CFDGTSTCTR.RTME bit is cleared by writing 0 to it.



注1.更改为RAMTEST之前，请更改为以下状态。
- 取消传输请求。
- 禁用所有FIFO和TXQ。
- 清除接收缓冲区的接收标志。

Figure 32.52 RAM测试模式的软件流程

要退出此测试模式，CFDGTSTCTR.RTME位必须清零。CFDGTSTCTR.RTME位通过向其写入0来清除。

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The CFDGTSTCTR.RTME bit is cleared automatically when the CAN-FD module enters Global Reset mode from the test mode.

32.9.2.2 Internal CAN Bus Communication Test Mode

The CAN-FD module can be configured in internal CAN bus communication test mode by setting the CFDGTSTCTR.ICBCTME bit in the Global Test Control Register. This is a special test mode, in which the CAN channels can be connected together internally to generate a CAN cluster within the CAN-FD module.

Only use the following sequence to enter internal CAN bus communication test mode:

1. Configure all channels in Halt mode and check that all channels have entered Halt mode (Global Halt mode).
2. Write data into the Global Test Configuration Register to select the channels participating in the internal CAN bus communication test.
3. Set the CFDGTSTCTR.ICBCTME bit of the Global Test Control Register.
4. Check that CFDGTSTCTR.ICBCTME bit is set in the Global Test Control Register.

In this mode, the TXD outputs of the channels participating (configured) in internal CAN bus communication mode are connected together using AND gate. The output of the AND gate is connected to the RXD inputs of all participating channels to create a CAN cluster within the CAN-FD module. The channels are isolated from the external CAN bus while the CAN-FD module is in this test mode.

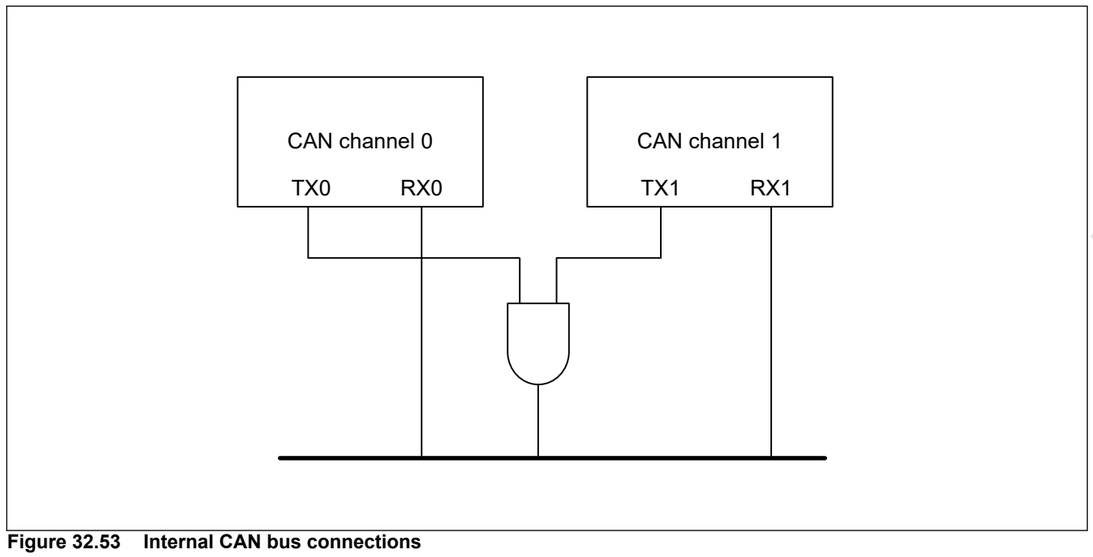


Figure 32.53 Internal CAN bus connections

The AFL, Flat RX message buffers, FIFO buffers, Flat TX message buffers and various registers can now be configured as normal to start communication between channels.

The channels not participating in internal CAN bus should only be configured in Halt mode.

(1) CRC Error Test

After the CAN-FD module has been configured in internal CAN bus communication test mode, use the following sequence to perform CRC Error testing. In this sequence, channel x is the reference transmitter CAN-FD module and channel y is the receiver CAN-FD module where (x,y = [0…n] and x ≠ y):

1. Configure channel x node to transmit 1 reference message.
2. Set the CFDCyCTR.CRCT bit to 1 to invert the first bit of the incoming bit stream from channel x.
3. Set the CFDTMCx.TMTR.
4. Read either the CFDCyERFL.CRCREG or the CFDCyCRC.CRCREG (depending on the received frame type: Classical or FD). The value should be different from the received CRC value of the reference message from channel x.

当CAN-FD模块从测试模式进入全局复位模式时，CFDGTSTCTR.RTME位会自动清零。

32.9.2.2 内部CAN总线通讯测试模式

CAN-FD模块可以通过设置内部CAN总线通信测试模式配置
全局测试控制寄存器中的CFDGTSTCTR.ICBCTME位。这是一种特殊的测试模式，其中CAN通道可以在内部连接在一起，以在CAN-FD模块内生成一个CAN集群。

只能使用以下顺序进入内部CAN总线通讯测试模式：

1.将所有通道配置为Halt模式，并检查所有通道是否已进入Halt模式（GlobalHalt模式）。

2.向全局测试配置寄存器写入数据，选择参与内部CAN总线通信测试的通道。

3.设置全局测试控制寄存器的CFDGTSTCTR.ICBCTME位。

4.检查CFDGTSTCTR.ICBCTME位是否在全局测试控制寄存器中设置。

在此模式下，参与（配置）内部CAN总线通信模式的通道的TXD输出使用与门连接在一起。与门的输出连接到所有参与通道的RXD输入，以在CAN-FD模块内创建一个CAN集群。当CAN-FD模块处于此测试模式时，通道与外部CAN总线隔离。

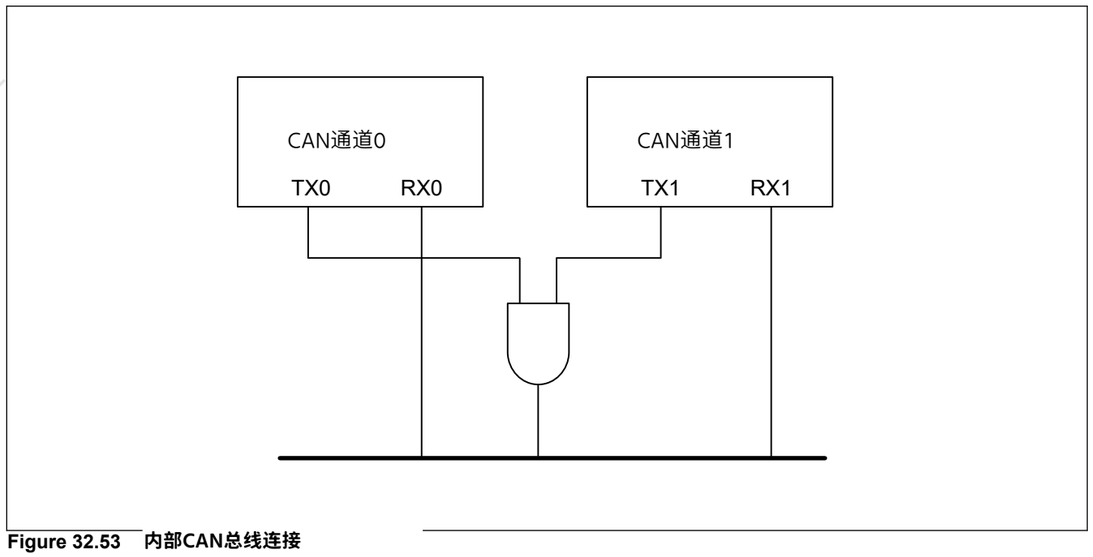


Figure 32.53 内部CAN总线连接

AFL、FlatRX消息缓冲区、FIFO缓冲区、FlatTX消息缓冲区和各种寄存器现在可以正常配置以开始通道之间的通信。

不参与内部CAN总线的通道只能配置为暂停模式。

(1) CRC错误测试

将CAN-FD模块配置为内部CAN总线通信测试模式后，按照以下顺序执行CRC错误测试。在此序列中，通道x是参考发送器CAN-FD模块，通道y是接收器CAN-FD模块，其中(x y=[0…n]且x≠y)：

1.配置通道x节点发送1条参考消息。

2.将CFDCyCTR.CRCT位设置为1，以反转来自通道x的输入比特流的第一位。

3.设置CFDTMCx.TMTR。

4.读取CFDCyERFL.CRCREG或CFDCyCRC.CRCREG（取决于接收到的帧类型：Classic或FD）。该值应不同于从通道x接收到的参考消息的CRC值。

5. Check that CFDCyERFL.CERR is 1

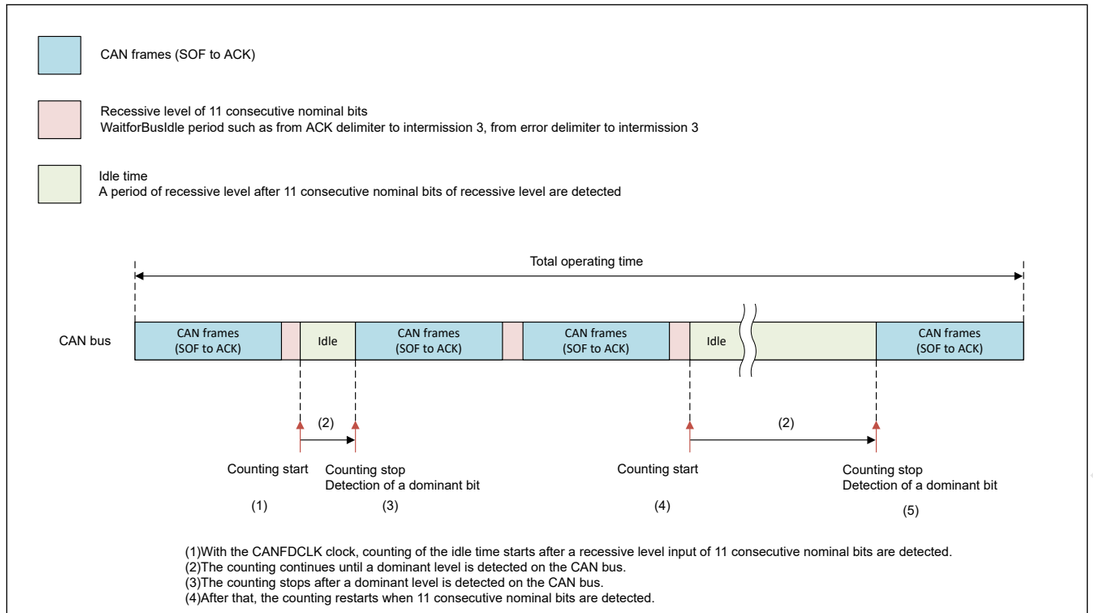
The CRC generator logic is shared between RX and TX so there is no need to create a separate TX CRC error test.

32.10 Bus Traffic Measurement

The idle time of the CAN bus can be measured using the CANFDCLK or CANMCLK. Bus traffic can be calculated based on the measurement results.

32.10.1 How to Count the CAN Bus Idle Time

The following figure shows the concept for measuring idle time of the CAN bus.



(1)With the CANFDCLK clock, counting of the idle time starts after a recessive level input of 11 consecutive nominal bits are detected.
(2)The counting continues until a dominant level is detected on the CAN bus.
(3)The counting stops after a dominant level is detected on the CAN bus.
(4)After that, the counting restarts when 11 consecutive nominal bits are detected.

32.10.2 Operations and Measurement Procedure

The following procedure shows the steps for measuring idle time of the CAN bus.

1. The channel to be measured exters operation mode.
2. Write 1 to CFDCnBLCT.BLCE bit to set the measuring counter to operating mode.
3. Write 1 to CFDCnBLCT.BLCLD bit to clear the counter register.
4. Detect a recessive level input of 11 consecutive nominal bits.
5. Start counting the bus idle time.
6. Detect a dominant level.
7. The counting stops.
8. Detect a recessive level input of 11 consecutive nominal bits.
9. The counting starts.
10. Write 1 to CFDCnBLCT.BLCLD bit to clear the counter register and simultaneously load the counter value to CFDCnBLSTS.
11. Read the value of CFDCnBLSTS.

5.检查CFDCyERFL.CERR是否为1

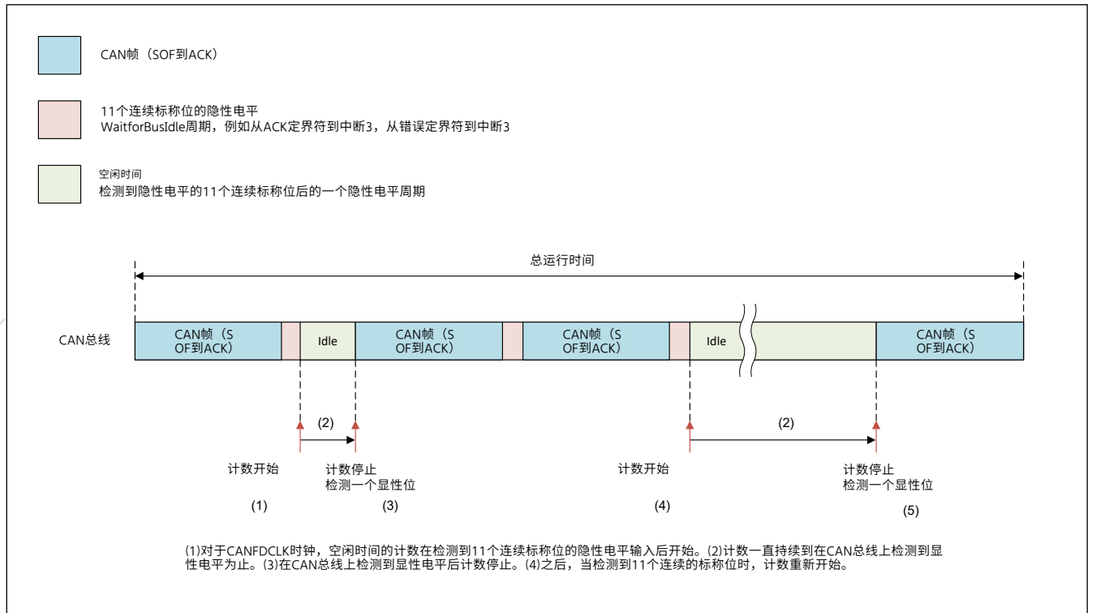
CRC生成器逻辑在RX和TX之间共享，因此无需创建单独的TXCRC错误测试。

32.10 公交车流量测量

CAN总线的空闲时间可以使用CANFDCLK或CANMCLK来测量。可以根据测量结果计算总线流量。

32.10.1 如何计算CAN总线空闲时间

下图显示了测量CAN总线空闲时间的概念。



(1)对于CANFDCLK时钟，空闲时间的计数在检测到11个连续标称位的隐性电平输入后开始。(2)计数一直持续到在CAN总线上检测到显性电平为止。(3)在CAN总线上检测到显性电平后计数停止。(4)之后，当检测到11个连续的标称位时，计数重新开始。

32.10.2 操作和测量程序

以下过程显示了测量CAN总线空闲时间的步骤。

1.被测通道采用工作模式。
2.将1写入CFDCnBLCT.BLCE位以将测量计数器设置为工作模式。
3.将1写入CFDCnBLCT.BLCLD位以清除计数器寄存器。
4.检测11个连续标称位的隐性电平输入。
5.开始计算总线空闲时间。
6.检测显性电平。
7.计数停止。
8.检测11个连续标称位的隐性电平输入。
9.计数开始。
10.将1写入CFDCnBLCT.BLCLD位以清除计数器寄存器，同时将计数器值加载到CFDCnBLSTS。

11.读取CFDCnBLSTS的值。

To stop the measurement counter, write 0 to CFDCnBLCT.BLCE bit.

To initialize the counter, write 1 to CFDCnBLCT.BLCLD bit.

This measurement is enabled when the channel to be measured is in operation mode.

When the relevant channels are in reset mode, the counter does not operate.

Also, accurate measurements are not available in test mode.

Write 1 to CFDCnBLCT.BLCLD bit to clear the counter register and simultaneously load the value of the counter to CFDCnBLSTS.

The lower three bits of CFDCnBLSTS are fixed to 0.

Based on the values of the counter, software can calculate the CAN bus traffic according to the following formulas.

$$\frac{(\text{total operating time} - \text{total idle time})}{\text{Total operating time}} = \frac{\text{bus operating time}}{\text{total operating time}} = \text{Bus usage ratio}$$

- Total idle time: a value read from CFDCnBLSTS × a clock cycle of CANFDCLK
- Total operating time: a setting interval of CFDCnBLCT.BLCLD bit

Example: Below is a calculation example under the following conditions.

- Conditions: nominal bit rate = 1 Mbps
- CANFDCLK clock = 40 MHz (= 25 ns)
- A setting interval of CFDCnBLCT.BLCLD bit = cycle of 1 ms
- A read value of CFDCnBLSTS register = 0x4E20

$$\frac{(\text{total operating time} - \text{total idle time})}{\text{Total operating time}} = \frac{(1000000\text{ns} - 20000 * 25\text{ns})}{1000000\text{ns}} = 50\,\%$$

要停止测量计数器，请将0写入CFDCnBLCT.BLCE位。

要初始化计数器，请将1写入CFDCnBLCT.BLCLD位。

当要测量的通道处于操作模式时，启用此测量。

当相关通道处于复位模式时，计数器不工作。

此外，在测试模式下无法进行精确测量。

将1写入CFDCnBLCT.BLCLD位以清除计数器寄存器并同时将计数器的值加载到CFDCnBLSTS.

CFDCnBLSTS的低三位固定为0。

根据计数器的值，软件可以根据以下公式计算CAN总线流量。

（总运行时间-总空闲时间）总运行时间 =巴总运行时间=公交使用率

●总空闲时间：从CFDCnBLSTS读取的一个值×CANFDCLK的一个时钟周期

●总运行时间：CFDCnBLCT.BLCLD位的设置间隔

示例：以下是以下条件下的计算示例。

●条件：标称比特率=1Mbps

- CANFDCLK clock = 40 MHz (= 25 ns)

●CFDCnBLCT.BLCLD位的设置间隔=1ms周期

●CFDCnBLSTS寄存器的读取值=0x4E20

（总运行时间-总空闲时间）总运行时间 $= \frac{(1000000\text{ns} - 20000 * 25\text{ns})}{1000000\text{ns}} = 50\,\%$

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33. CANFD ECC (CNECC)

33.1 Overview

AFLRAM0, AFLRAM1 and MBRAM have ECC function of 2-bit ECC error detection and 1-bit ECC error detection and correction*1. The ECC module adds 7 bits ECC data to 32 bits RAM data.

Note 1. The ECC module cannot detect 3 or more bits error. In this case, the ECC module detects 1-bit or 2-bit error, does not detect errors, or corrects the erroneous bit to erroneous data by setting. When all RAM data are fixed to 0 or 1, it is detected as 2-bit ECC error.

33.2 Register Descriptions

33.2.1 EC710CTL : ECC Control Register

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECDEDF0	ECSEDF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	—	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	ECEMF	ECC Error Message Flag 0: There is no bit error in present RAM output data 1: There is bit error in present RAM output data	R
1	ECER1F	ECC Error Detection and Correction Flag 0: After clearing this bit, 1-bit error correction has not occurred 1: 1-bit error has occurred	R
2	ECER2F	2-bit ECC Error Detection Flag 0: After clearing this bit, 2-bit error has not occurred 1: 2-bit error has occurred	R
3	EC1EDIC	ECC 1-bit Error Detection Interrupt Control 0: Disable 1-bit error detection interrupt request 1: Enable 1-bit error detection interrupt request	R/W
4	EC2EDIC	ECC 2-bit Error Detection Interrupt Control 0: Disable 2-bit error detection interrupt request 1: Enable 2-bit error detection interrupt request	R/W
5	EC1ECP	ECC 1-bit Error Correction Permission 0: At 1-bit error detection, the error correction is executed 1: At 1-bit error detection, the error correction is not executed	R/W
6	ECERVF	ECC Error Judgment Enable Flag 0: Error judgment disable 1: Error judgment enable	R/W
8:7	—	These bits are read as 0. The write value should be 0.	R/W
9	ECER1C	Accumulating ECC Error Detection and Correction Flag Clear 0: No effect 1: Clear accumulating ECC error detection and correction flag	R/W

33. CANFD ECC (CNECC)

33.1 Overview

AFLRAM0、AFLRAM1和MBRAM具有2位ECC错误检测和1位ECC错误检测和纠正的ECC功能*1。ECC模块将7位ECC数据添加到32位RAM数据中。

注1.ECC模块无法检测3位或更多位错误。在这种情况下，ECC模块检测1位或2位错误，不检测错误，或通过设置将错误位纠正为错误数据。当所有RAM数据固定为0或1时，将被检测为2位ECC错误。

33.2 注册说明

33.2.1 EC710CTL:ECC控制寄存器

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECDEDF0	ECSEDF0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	—	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	ECEMF	ECC错误消息标志 0：当前RAM输出数据无误码1：当前RAM输出数据有误码	R
1	ECER1F	ECC错误检测和纠正标志 0：清除该位后，未发生1位错误纠正1：发生1位错误	R
2	ECER2F	2位ECC错误检测标志 0：清除该位后，未发生2位错误1：发生2位错误	R
3	EC1EDIC	ECC1位错误检测中断控制 0：禁止1位错误检测中断请求1：允许1位错误检测中断请求	R/W
4	EC2EDIC	ECC2位错误检测中断控制 0：禁止2位错误检测中断请求1：允许2位错误检测中断请求	R/W
5	EC1ECP	ECC1位纠错权限 0：1位错误检测时执行纠错1：1位错误检测时不执行错误纠正	R/W
6	ECERVF	ECC错误判断使能标志 0：错误判断无效1：错误判断有效	R/W
8:7	—	这些位被读取为0。写入值应为0。	R/W
9	ECER1C	累积ECC错误检测和纠正标志清除 0：无效1：清除累积ECC错误检测和纠正标志	R/W

Bit	Symbol	Function	R/W
10	ECER2C	2-bit ECC Error Detection Flag Clear 0: No effect 1: Clear 2-bit ECC error detection flag	R/W
11	ECOVFF	ECC Overflow Detection Flag 0: No effect 1: ECC overflow detection flag	R
13:12	—	These bits are read as 0. The write value should be 0.	R/W
15:14	EMCA[1:0]	Access Control to ECC Mode Select bit These bits enable or disable write access to ECERVF bit.	R/W
16	ECSEDF0	ECC Single bit Error Address Detection Flag 0: There is no bit error in EC710EAD0 after reset or clearing ECER1F bit 1: Address captured in EC710EAD0 shows that 1-bit error occurred and captured	R
17	ECDEDF0	ECC Dual Bit Error Address Detection Flag 0: There is no bit error in EC710EAD0 after reset or clearing ECER2F bit 1: Address captured in EC710EAD0 shows that 2-bit error occurred and captured	R
31:18	—	These bits are read as 0. The write value should be 0.	R/W

ECEMF bit (ECC Error Message Flag)

The ECEMF bit shows that there is error in present read data bus. This bit is updated by every RAM output data.

When RAM output data is undefined and the ECERVF bit is set to 1, the value of this bit is undefined.

[Setting condition]

There is bit error in present RAM output data under the condition that error judgement is enabled.

[Clearing condition]

- Under the condition that there is no 1-bit error in input data to decode circuit
- When ECC error judgement is disabled (ECERVF = 0).

ECER1F bit (ECC Error Detection and Correction Flag)

The ECER1F bit shows that the bit errors are detected in the one part of RAM read data [38:0] at RAM read access when the error judgment is enabled.

When the 1-bit error interrupt output is enabled, error interrupt is generated by setting this flag.

This bit is read-only, so writing 1 or 0 has no effect.

At clearing, write 1 to the ECER1C bit.

When 1-bit error is detected again under the condition that this bit is set, the interrupt is not generated.

[Setting condition]

When the error judgment is enabled and there is 1-bit error to RAM output data (when not setting ECER1C = 1).

[Clearing condition]

- Writing ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

ECER2F bit (2-bit ECC Error Detection Flag)

The ECER2F bit shows that the bit errors are detected in the two parts of RAM read data [38:0] at RAM read access when the error judgment is enabled.

When the 2-bit error interrupt output is enabled, error interrupt is generated by setting this flag.

This bit is read-only, so writing 1 or 0 has no effect.

At clearing, write 1 to the ECER2C bit.

When 2-bit error is detected again under the condition that this bit is set, the interrupt is not generated.

[Setting condition]

Bit	Symbol	Function	R/W
10	ECER2C	2位ECC错误检测标志清除 0：无效1：清除2位ECC错误检测标志	R/W
11	ECOVFF	ECC溢出检测标志 0：无效1：ECC溢出检测标志	R
13:12	—	这些位被读取为0。写入值应为0。	R/W
15:14	EMCA[1:0]	ECC模式选择位的访问控制 这些位启用或禁用对ECERVF位的写访问。	R/W
16	ECSEDF0	ECC单位错误地址检测标志 0：复位或清除ECER1F后EC710EAD0中没有位错误位1：EC710EAD0中捕获的地址显示发生并捕获了1位错误	R
17	ECDEDF0	ECC双位错误地址检测标志 0：复位或清除ECER2F位后EC710EAD0中没有位错误1：EC710EAD0中捕获的地址显示发生并捕获了2位错误	R
31:18	—	这些位被读取为0。写入值应为0。	R/W

ECEMF位（ECC错误消息标志）

ECEMF位显示当前读数据总线有错误。该位由每个RAM输出数据更新。

当RAM输出数据未定义且ECERVF位设置为1时，该位的值未定义。

[Setting condition]

在启用错误判断的情况下，当前RAM输出数据存在位错误。

[Clearing condition]

●解码电路的输入数据无1位错误的情况下

●ECC错误判断无效时（ECERVF=0）。

ECER1F位（ECC错误检测和纠正标志）

ECER1F位表示当启用错误判断时，在RAM读取访问时，在RAM读取数据[38:0]的一部分中检测到位错误。

当1位错误中断输出使能时，通过设置该标志产生错误中断。

该位是只读的，因此写入1或0无效。

清零时，将1写入ECER1C位。

在该位置位的情况下再次检测到1位错误时，不会产生中断。

[Setting condition]

启用错误判断且RAM输出数据有1位错误时（未设置ECER1C=1时）。

[Clearing condition]

- Writing ECER1C = 1

●ECC错误判断无效时（ECERVF=0）。

ECER2F位（2位ECC错误检测标志）

ECER2F位表示当错误判断使能时，在RAM读取访问的两部分RAM读取数据[38:0]中检测到位错误。

当2位错误中断输出使能时，通过设置该标志产生错误中断。

该位是只读的，因此写入1或0无效。

清除时，将1写入ECER2C位。

在该位置位的情况下再次检测到2位错误时，不会产生中断。

[Setting condition]

When the error judgment is enabled and there is 2-bit error to RAM output data (when not setting ECER2C = 1).

[Clearing condition]

- Writing ECER2C = 1
- When ECC error judgement is disabled (ECERVF = 0).

EC1EDIC bit (ECC 1-bit Error Detection Interrupt Control)

The EC1EDIC controls the interrupt output at detecting 1-bit error. By setting 1 to this bit, the 1-bit error interrupt is outputted when 1-bit error detected.

EC2EDIC bit (ECC 2-bit Error Detection Interrupt Control)

The EC2EDIC controls the interrupt output at detecting 2-bit error. By setting 1 to this bit, the 2-bit error interrupt is outputted when 2-bit error detected.

EC1ECP bit (ECC 1-bit Error Correction Permission)

The EC1ECP sets enable or disable to correct the 1-bit error when ECC error detection and correction is valid. By setting 1 to this bit, the non-corrected data is outputted if 1-bit error is detected.

ECERVF bit (ECC Error Judgment Enable Flag)

Setting the ECERVF bit to 1 enables the judgment of error. The correction of output data and the interrupt output depend on setting of the EC1ECP bit, EC2EDIC bit, and EC1EDIC bit.

The write access to this bit is valid when the write value of the EMCA[1:0] is 01b. So only the 16 bits or 32 bits operation command is valid in the case of the write access to this bit.

ECER1C bit (Accumulating ECC Error Detection and Correction Flag Clear)

The ECER1C bit clears the status flag of the ECER1F bit.

The read value is always 0. By writing 0, the internal condition is not changed. When the competition between writing 1 to this bit and setting the ECER1F bit, the former has priority.

The ECER1F bit is cleared by writing 1 to this bit while the ECER1F bit is set. Additionally, the Overflow Detection flag (ECOVFF), ECC Dual Bit Error flag (ECDEDF0) and ECC Single Bit Error flag (ECSEDF0) are also cleared.

ECER2C bit (2-bit ECC Error Detection Flag Clear)

The ECER2C bit clears the status flag of the ECER2F bit.

The read value is always 0. By writing 0, the internal condition is not changed. When the competition between writing 1 to this bit and setting the ECER2F bit, the former has priority.

The ECER2F bit is cleared by writing 1 to this bit while the ECER2F bit is set. Additionally, the Overflow Detection flag (ECOVFF), ECC Dual Bit Error flag (ECDEDF0), and ECC Single Bit Error flag (ECSEDF0) are also cleared.

ECOVFF bit (ECC Overflow Detection Flag)

The ECOVFF bit is set and the overflow interruption is outputted by detecting the new error address under the condition that error address is already captured in the EC710EAD0 register. The overflow interrupt is outputted again when this bit is set and new error is detected.

This bit is read-only, so writing 1 or 0 has no effect.

To clear this bit, write 1 to the ECER2C bit and the ECER1C bit.

[Setting condition]

When new error address is captured under the condition that error address is already captured in the EC710EAD0 register (when not setting ECER2C = 1 or ECER1C = 1).

[Clearing condition]

- Writing ECER2C = 1 or ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

启用错误判断且RAM输出数据有2位错误时（未设置ECER2C=1时）。

[Clearing condition]

- Writing ECER2C = 1
- ●ECC错误判断无效时（ECERVF=0）。

EC1EDIC位（ECC1位错误检测中断控制）

EC1EDIC在检测到1位错误时控制中断输出。通过将该位设置为1，当检测到1位错误时输出1位错误中断。

EC2EDIC位（ECC2位错误检测中断控制）

EC2EDIC在检测到2位错误时控制中断输出。通过将此位设置为1，当检测到2位错误时输出2位错误中断。

EC1ECP位（ECC1位纠错权限）

当ECC错误检测和纠正有效时，EC1ECP设置启用或禁用以纠正1位错误。通过将此位设置为1，如果检测到1位错误，则输出未校正的数据。

ECERVF位（ECC错误判断使能标志）

将ECERVF位设置为1可以进行错误判断。输出数据的校正和中断输出取决于EC1ECP位、EC2EDIC位和EC1EDIC位的设置。

当EMCA[1:0]的写值为01b时，对该位的写访问有效。因此在对该位进行写访问的情况下，只有16位或32位操作命令有效。

ECER1C位（累积ECC错误检测和纠正标志清除）

ECER1C位清除ECER1F位的状态标志。

读取值始终为0。通过写入0，内部条件不会改变。当向该位写1与设置ECER1F位竞争时，前者具有优先权。

当ECER1F位置位时，通过向该位写入1来清除ECER1F位。此外，溢出检测标志(ECOVFF)、ECC双比特错误标志(ECDEDF0)和ECC单比特错误标志(ECSEDF0)也被清除。

ECER2C位（2位ECC错误检测标志清除）

ECER2C位清除ECER2F位的状态标志。

读取值始终为0。通过写入0，内部条件不会改变。当向该位写1与设置ECER2F位竞争时，前者具有优先权。

当ECER2F位置位时，通过向该位写入1来清除ECER2F位。此外，溢出检测标志(ECOVFF)、ECC双比特错误标志(ECDEDF0)和ECC单比特错误标志(ECSEDF0)也被清除。

ECOVFF位（ECC溢出检测标志）

在EC710EAD0寄存器中已经捕捉到错误地址的情况下，通过检测新的错误地址，设置ECOVFF位并输出溢出中断。当该位置位并检测到新错误时，溢出中断再次输出。

该位是只读的，因此写入1或0无效。

要清除该位，向ECER2C位和ECER1C位写入1。

[Setting condition]

在EC710EAD0寄存器中已捕获错误地址的情况下捕获新的错误地址时（未设置ECER2C=1或ECER1C=1时）。

[Clearing condition]

- ●写入ECER2C=1或ECER1C=1
- ●ECC错误判断无效时（ECERVF=0）。

EMCA[1:0] bit (Access Control to ECC Mode Select bit)

The EMCA[1:0] bits are the write trigger reserved bits to the ECERVF bit. The read value is always 0. When the value of these bits is 01b, it is possible to have write access to the ECERVF bit. If these bits are not 01b, write access to the ECERVF bit is ignored and the value is not written.

ECSEDF0 bit (ECC Single bit Error Address Detection Flag)

The ECSEDF0 bit shows that the error is captured in the error address register when error detection is valid. This bit is set by 1-bit error detection.

When 1-bit error is detected after the 2-bit error address is already captured in the EC710EAD0 register, this bit is not updated but the EC710EAD0 register is updated.

This bit is read-only, so writing 1 or 0 has no effect. To clear these bits, write 1 to the ECER1C bit.

[Setting condition]

When there is 1-bit error to RAM output data and error address is captured in EC710EAD0 under the condition that the error judgment is permitted (when not setting ECER1C = 1).

[Clearing condition]

- Writing ECER1C = 1
- When ECC error judgement is disabled (ECERVF = 0).

ECDEDF0 bit (ECC Dual Bit Error Address Detection Flag)

The ECDEDF0 bit shows that the error is captured in the error address register when error detection is valid. This bit is set by 2-bit error detection.

When 2-bit error is detected after the 1-bit error address is already captured in the EC710EAD0 register, this bit is not updated and the EC710EAD0 register is updated.

This bit is read-only, so writing 1 or 0 has no effect. To clear these bits, write 1 to the ECER2C bit.

[Setting condition]

When there is 2-bit error to RAM output data and error address is captured in EC710EAD0 under the condition that the error judgment is permitted (when not setting ECER2C = 1).

[Clearing condition]

- Writing ECER2C = 1
- When ECC error judgement is disabled (ECERVF = 0).

33.2.2 EC710TMC : ECC Test Mode Control Register

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ETMA[1:0]		—	—	—	—	—	—	ECTMCE	—	—	—	—	—	ECDCS	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	ECDCS	ECC Decode Input Select 0: Input lower 32 bits of RAM output data to data area of decode circuit 1: Input ECEDB31-0 in EC710TED register to data area of decode circuit	R/W
6:2	—	These bits are read as 0. The write value should be 0.	R/W

EMCA[1:0]位（ECC模式选择位的访问控制）

EMCA[1:0]位是ECERVF位的写触发保留位。读取值始终为0。当这些位的值为01b时，可以对ECERVF位进行写访问。如果这些位不是01b，则忽略对ECERVF位的写访问并且不写入该值。

ECSEDF0位（ECC单个位错误地址检测标志）

ECSEDF0位表示当错误检测有效时，错误被捕获到错误地址寄存器中。该位由1位错误检测设置。

当在EC710EAD0寄存器中已捕获2位错误地址后检测到1位错误时，该位不会更新，但EC710EAD0寄存器会更新。

该位是只读的，因此写入1或0无效。要清除这些位，请将1写入ECER1C位。

[Setting condition]

在允许错误判断的条件下（未设置ECER1C=1时），当RAM输出数据出现1位错误并在EC710EAD0中捕获错误地址时。

[Clearing condition]

- Writing ECER1C = 1
- ●ECC错误判断无效时（ECERVF=0）。

ECDEDF0位（ECC双位错误地址检测标志）

ECDEDF0位表示当错误检测有效时，错误被捕获在错误地址寄存器中。该位由2位错误检测设置。

当在EC710EAD0寄存器中已捕获1位错误地址后检测到2位错误时，该位不更新，EC710EAD0寄存器更新。

该位是只读的，因此写入1或0无效。要清除这些位，请将1写入ECER2C位。

[Setting condition]

在允许错误判断的条件下（未设置ECER2C=1时），当RAM输出数据有2位错误并且错误地址被捕获到EC710EAD0中时。

[Clearing condition]

- Writing ECER2C = 1
- ●ECC错误判断无效时（ECERVF=0）。

33.2.2 EC710TMC：ECC测试模式控制寄存器

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ETMA[1:0]		—	—	—	—	—	—	ECTMCE	—	—	—	—	—	ECDCS	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	ECDCS	ECC解码输入选择 0：将RAM输出数据的低32位输入到解码电路的数据区1：将EC710TED寄存器中的ECEDB31-0输入到解码电路的数据区	R/W
6:2	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
7	ECTMCE	ECC Test Mode Control Enable 0: The access to test mode register and bit is disabled 1: The access to test mode register and bit is enabled	R/W
13:8	—	These bits are read as 0. The write value should be 0.	R/W
15:14	ETMA[1:0]	ECC Test Mode Bit Access Control These bits enable or disable write access to ECTMCE bit.	R/W

ECDCS bit (ECC Decode Input Select)

The ECDCS bit selects either the lower 32 bits data value from RAM or value from the internal test register (EDEDB[31:0] in EC710TED) as input signal to decoder.

The write access to this bit is valid under the condition of ECTMCE = 1 (it is possible to set them at the same time.)

This bit is cleared by setting ECTMCE = 0.

ECTMCE bit (ECC Test Mode Control Enable)

The ECTMCE bit selects the access enable or disable to test register and test control bit.

The write access to this bit is valid under the condition that the value of the ETMA[1:0] bits is 10b.

ETMA[1:0] bits (ECC Test Mode Bit Access Control)

The ETMA[1:0] bits are the write trigger reserved bits to the ECTMCE bit. The read value is always 0. When the value of these bits is 10b, it is possible to have write access to the ECTMCE bit. If these bits are not 10b, the write access to the ECTMCE bit is ignored and the value is not written.

33.2.3 EC710TED : ECC Test Substitute Data Register

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x0C

Bit position:	31																												0
Bit field:	ECEDB[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ECEDB[31:0]	ECC Test Substitute Data Substitute data in ECC test mode.	R/W

This register is for the 32 bits data for ECC decode. It is possible to read and write using 32 bits operation command when ECTMCE = 1. When ECTMCE = 0, all bits are always 0.

ECEDB[31:0] bits (ECC Test Substitute Data)

When ECDCS in EC710TMC register is 1, the value of this register is bits [31:0] of the input data to the decode circuit.

Bit	Symbol	Function	R/W
7	ECTMCE	ECC测试模式控制启用 0：禁止访问测试模式寄存器和位1：允许访问测试模式寄存器和位	R/W
13:8	—	这些位被读取为0。写入值应为0。	R/W
15:14	ETMA[1:0]	ECC测试模式位访问控制 这些位启用或禁用对ECTMCE位的写访问。	R/W

ECDCS位（ECC解码输入选择）

ECDCS位选择来自RAM的低32位数据值或来自内部测试寄存器（EC710TED中的EDEDB[31:0]）的值作为解码器的输入信号。

对该位的写访问在ECTMCE=1的条件下有效（可以同时置位）。

该位通过设置ECTMCE=0清零。

ECTMCE位（ECC测试模式控制使能）

ECTMCE位选择对测试寄存器和测试控制位的访问启用或禁用。

在ETMA[1:0]位的值为10b的情况下，对该位的写访问是有效的。

ETMA[1:0]位（ECC测试模式位访问控制）

ETMA[1:0]位是ECTMCE位的写触发保留位。读取值始终为0。当这些位的值为10b时，可以对ECTMCE位进行写访问。如果这些位不是10b，则忽略对ECTMCE位的写访问并且不写入该值。

33.2.3 EC710TED:ECC测试替代数据寄存器

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x0C

Bit position:	31																												0
Bit field:	ECEDB[31:0]																												
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	ECEDB[31:0]	ECC测试替代数据 在ECC测试模式下替换数据。	R/W

该寄存器用于ECC解码的32位数据。可以使用32位操作命令读取和写入时ECTMCE=1。当ECTMCE=0时，所有位始终为0。

ECEDB[31:0]位（ECC测试替代数据）

当EC710TMC寄存器中的ECDCS为1时，该寄存器的值为解码电路输入数据的位[31:0]。

33.2.4 EC710EAD0 : ECC Error Address Register

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ECEAD[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	ECEAD[10:0]	ECC Error Address	R
31:11	—	These bits are read as 0. The write value should be 0.	R

This is a read-only register to hold the ECC error address.

ECEAD[10:0] bits (ECC Error Address)

When ECC error is detected for permitting ECC error judgment, RAM address is captured by the detected signal as a trigger and is hold as the error occurring address. The error address is not captured when the error occurred again to the one held by the same factor.

If 2-bit error occurred under the condition that 1-bit error address is already captured, the 2-bit error address is over-written and the ECDEDF0 bit is set to 1.

If 1-bit error occurred under the condition that 2-bit error address is already captured, the 1-bit error address is not overwritten and the ECSEDF0 bit is not set to 1.

33.3 Operation

33.3.1 ECC Function Setting

Figure 33.1 shows a procedure for ECC function setting.

33.2.4 EC710EAD0：ECC错误地址寄存器

Base address: ECCAFLn = 0x4012_F000 + 0x0100 × n (n = 0, 1)
ECCMB = 0x4012_F200

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	ECEAD[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	ECEAD[10:0]	ECC错误地址	R
31:11	—	这些位被读取为0。写入值应为0。	R

这是一个只读寄存器，用于保存ECC错误地址。

ECEAD[10:0]位（ECC错误地址）

当检测到ECC错误以允许ECC错误判断时，RAM地址被检测信号捕获作为触发，并作为错误发生地址保持。当错误再次发生到相同因素持有的地址时，错误地址不会被捕获。

如果在已捕获1位错误地址的情况下发生2位错误，则覆盖2位错误地址并将ECDEDF0位设置为1。

如果在已捕获2位错误地址的情况下发生1位错误，则不会覆盖1位错误地址且ECSEDF0位不会设置为1。

33.3 Operation

33.3.1 ECC功能设置

图33.1显示了ECC功能设置的过程。

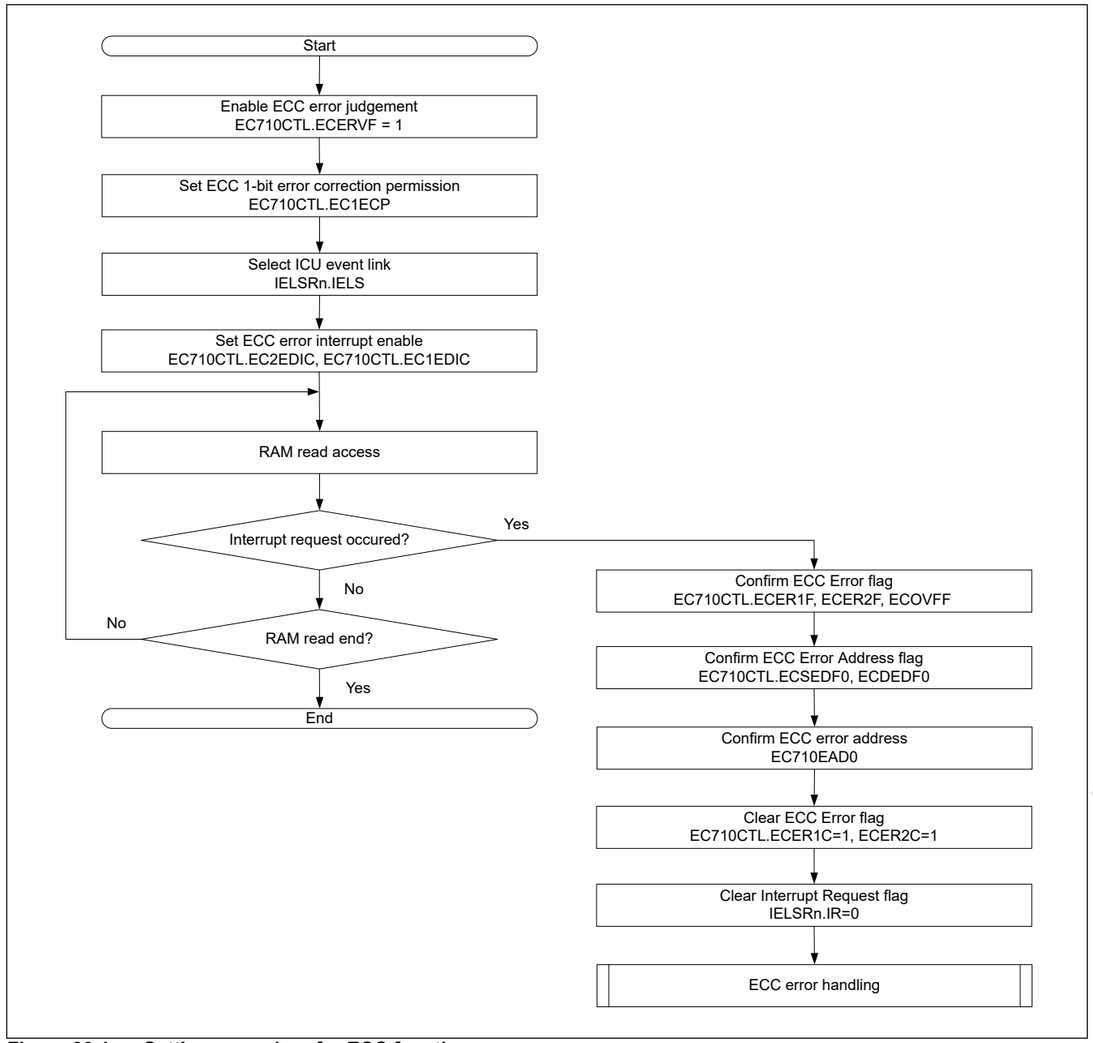

Figure 33.1 Setting procedure for ECC function

33.3.2 ECC Decoder Testing

ECC interrupts can be intentionally generated by ECC test mode. Figure 33.2 shows a procedure for ECC decoder testing.

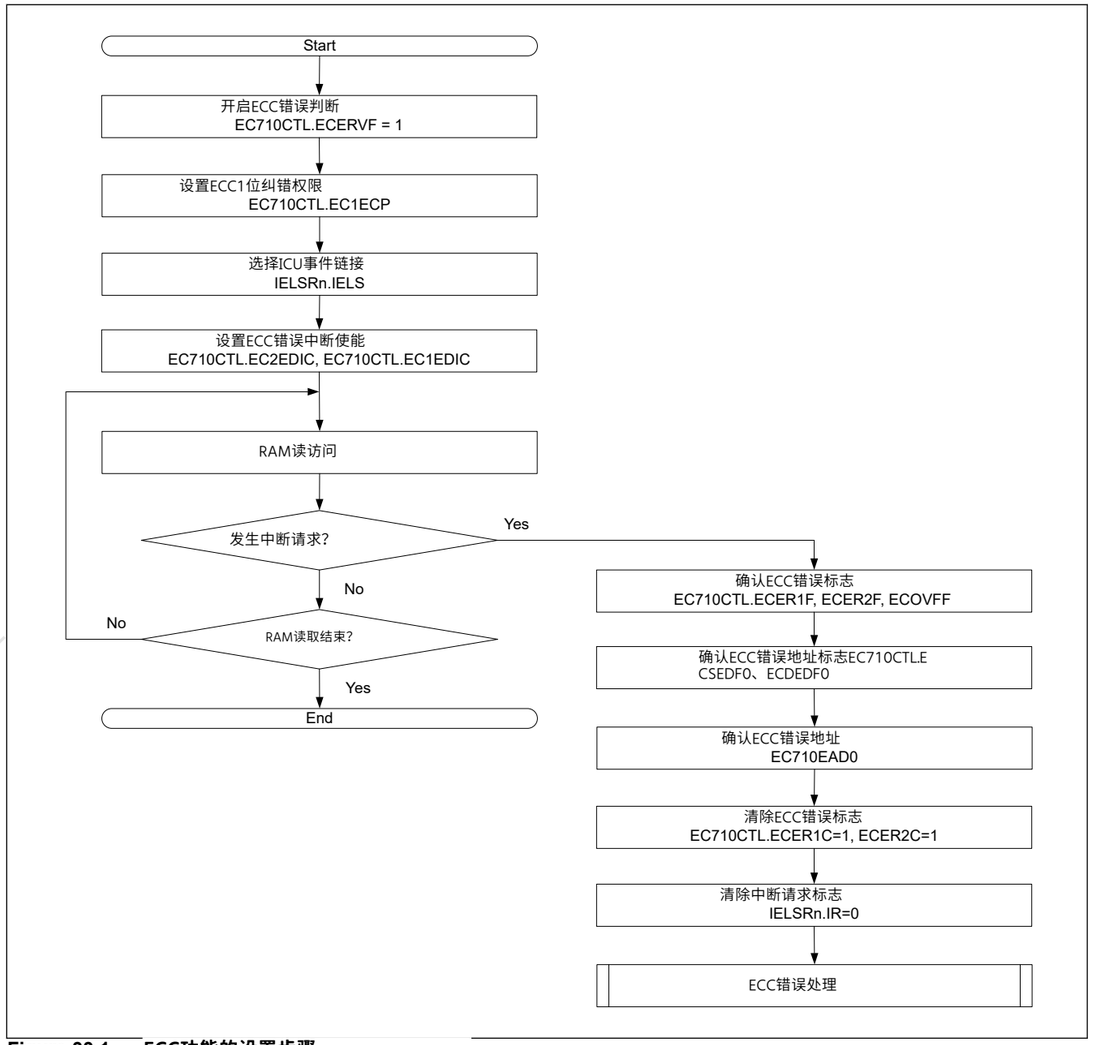

Figure 33.1 ECC功能的设置步骤

33.3.2 ECC解码器测试

ECC测试模式可以有意生成ECC中断。图33.2显示了ECC解码器测试的过程。

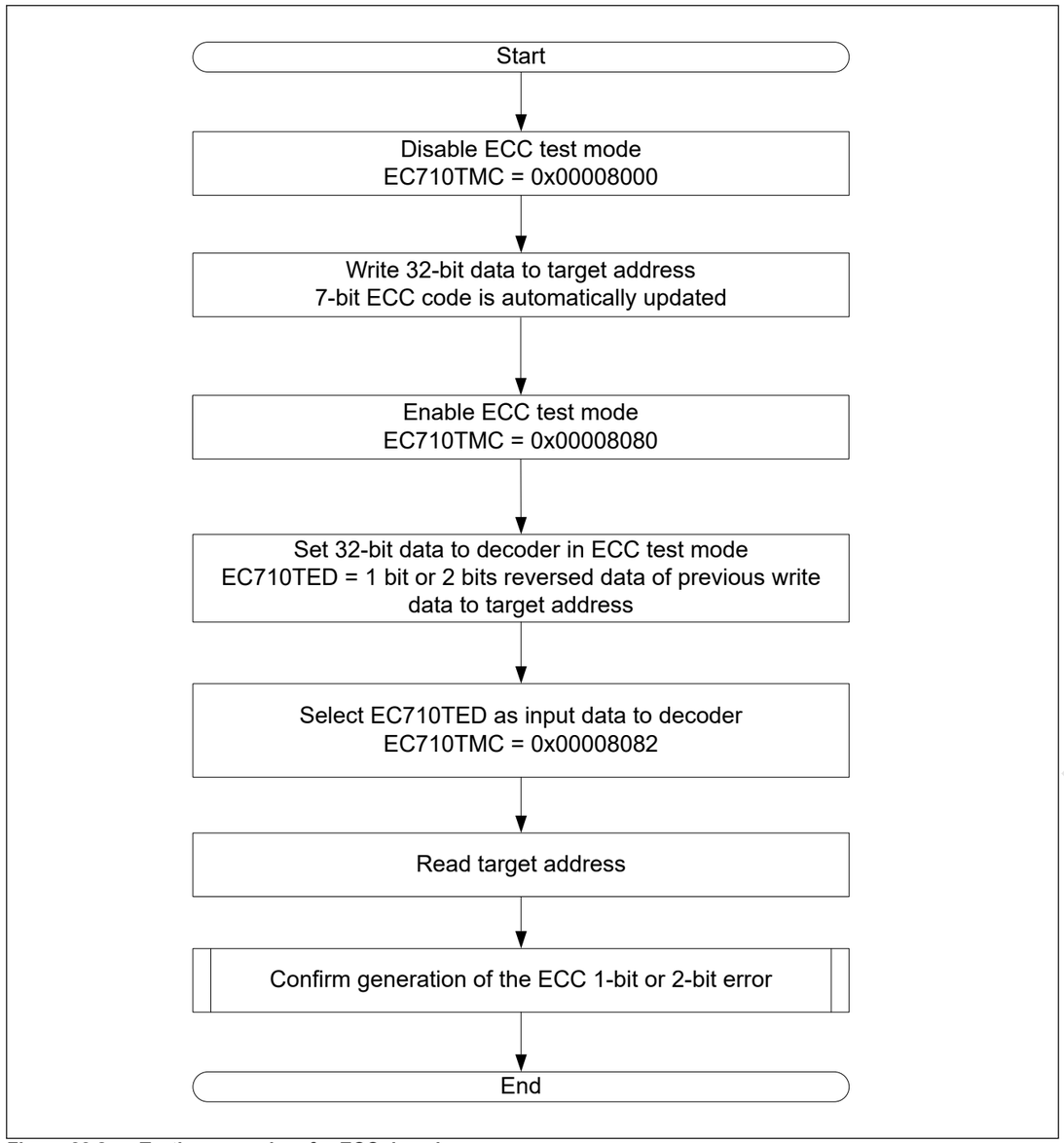

Figure 33.2 Testing procedure for ECC decoder

33.4 Interrupts

The ECC module issues three interrupt requests:

- CAN_AFLRAM0_ERI
- CAN_AFLRAM1_ERI
- CAN_MRAM_ERI.

Interrupt sources of each interrupt request include:

- 1-bit ECC error
- 2-bit ECC error

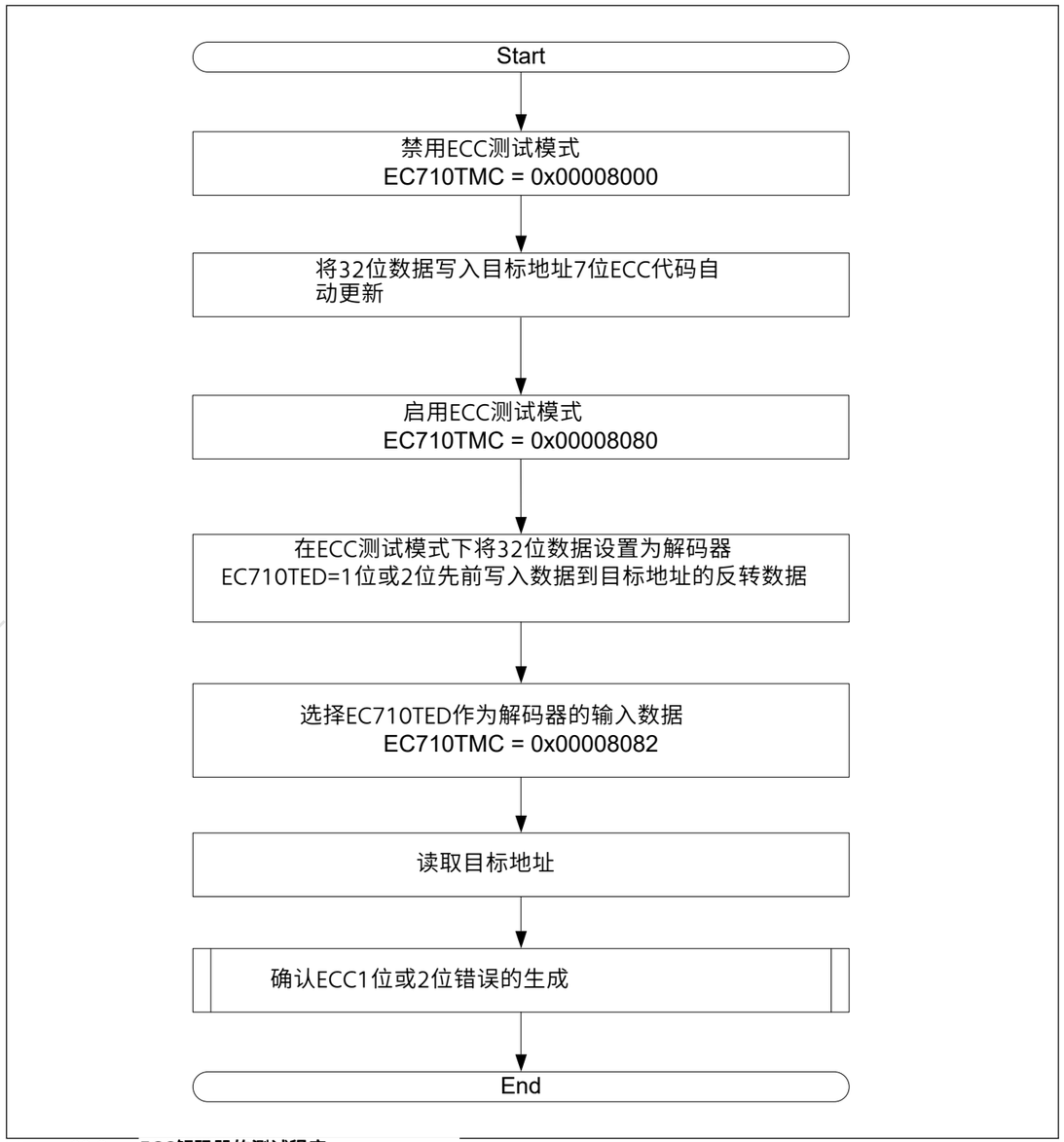

Figure 33.2 ECC解码器的测试程序

33.4 Interrupts

ECC模块发出三个中断请求：

- CAN_AFLRAM0_ERI
- CAN_AFLRAM1_ERI
- CAN_MRAM_ERI.

每个中断请求的中断源包括：

- 1-bit ECC error
- 2-bit ECC error

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- ECC error overflow.

●ECC错误溢出。

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34. Serial Peripheral Interface (SPI)

34.1 Overview

The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. Table 34.1 lists the SPI specifications, Figure 34.1 shows a block diagram, and Table 34.2 lists the I/O pins.

Table 34.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Receive-only operation is available (Slave mode only) • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 128-bit transmit and receive buffers • Up to four frames transferable in one round of transmission or reception (each frame consisting of up to 32 bits) • Byte swap operating function • Transmit/receive data can be inverted.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKA (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKA clock divided by 4 can be input as RSPCK (PCLKA divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKA cycles; width at low level: 2 PCLKA cycles
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection
SSL control function	• Four SSL pins (SSLni: SSLn0 to SSLn3) (n = A, B) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity • Delay between frames in burst transfer is settable
Control in master transfer	• Transfers of up to eight commands each can be executed sequentially in looped execution • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

34. 串行外设接口(SPI)

34.1 Overview

串行外围接口(SPI)提供与多个处理器和外围设备的高速全双工同步串行通信。表34.1列出了SPI规格，图34.1显示了框图，表34.2列出了IO引脚。

Table 34.1 SPI规格（2个中的1个）

Parameter	Specifications
通道数	两个通道
SPI传输函数	• 使用MOSI（主输出从输入）、MISO（主输入从输出）、SSL（从选择）和RSPCK（SPI时钟）信号允许通过SPI操作（4线方法）或时钟同步操作（3-线法） • 仅传输操作可用 • 仅接收操作可用（仅从模式） • 通信模式可选择全双工或仅传输 • RSPCK极性切换 • RSPCK相位切换
数据格式	• 可选择MSB优先或LSB优先 • 传输位长度可选择为8、9、10、11、12、13、14、15、16、20、24或32位 • 128位发送和接收缓冲器 • 在一轮发送或接收中最多可传输四帧（每帧最多包含32位） • 字节交换操作功能 • 发送接收数据可以反转。
比特率	• 在主机模式下，片内波特率发生器通过分频产生RSPCK PCLKA（分频比范围从2分频到4096分频） • 从机模式下，可以输入最小PCLKA时钟4分频作为RSPCK（PCLKA4分频为最大RSPCK频率）高电平宽度：2个PCLKA周期；低电平宽度：2个PCLKA周期
缓冲区配置	• 发送和接收缓冲区的双缓冲区配置 • 128位用于发送和接收缓冲区
错误检测	• 模式故障错误检测 • 欠载错误检测 • 溢出错误检测*1 • 奇偶校验错误检测
SSL控制功能	• 每个通道有四个SSL引脚（SSLni：SSLn0到SSLn3）（n=A、B） • 在单主模式下，输出SSLn0到SSLn3引脚 • 在多主模式下，SSLn0引脚用于输入，SSLn1至SSLn3引脚用于输出或未使用 • 在从机模式下，SSLn0引脚用于输入，SSLn1到SSLn3引脚未使用 • 从SSL输出断言到RSPCK操作的可控延迟（RSPCK延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 从RSPCK停止到SSL输出否定的可控延迟（SSL否定延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 下一次访问SSL输出断言的可控等待（下一次访问延迟） 范围：1到8个RSPCK循环（以RSPCK循环为单位设置） • 更改SSL极性的功能 • 突发传输中帧之间的延迟是可设置的
主传输中的控制	• 最多可传输8个命令，每个命令可以在循环执行中顺序执行 • 对于每个命令，可以设置以下内容： SSL信号值、比特率、RSPCK极性和相位、传输数据长度、MSBorLSB在前、突发、RSPCK延迟、SSL否定延迟和下一次访问延迟 • 可以通过写入发送缓冲区来启动传输 • 在SSL否定中可指定的MOSI信号值 • RSPCK auto-stop function

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Table 34.1 SPI specifications (2 of 2)

Parameter	Specifications
Interrupt sources	Interrupt sources: ● Receive buffer full interrupt ● Transmit buffer empty interrupt ● SPI error interrupt (mode fault error, overrun error, parity error) ● SPI idle interrupt (SPI idle) ● Transmission-complete interrupt
Event link function	The following events can be output to the Event Link Controller (ELC): ● Receive buffer full signal ● Transmit buffer empty signal ● Mode fault, underrun, overrun, or parity error signal ● SPI idle signal ● Communication end signal
Other functions	● Switching between CMOS output and open-drain output ● SPI initialization function ● Loopback mode
Module-stop function	Module-stop state can be set to reduce power consumption.
TrustZone Filter	Security attribution can be set

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.

Table 34.1 SPI规范（2个中的2个）

Parameter	Specifications
中断源	Interrupt sources: ● 接收缓冲区满中断 ● 发送缓冲区空中断 ● SPI错误中断（模式错误错误、溢出错误、奇偶校验错误） ● SPI空闲中断（SPI空闲） ● Transmission-complete interrupt
事件链接功能	以下事件可以输出到事件链接控制器(ELC)：● 接收缓冲区满信号 ● 发送缓冲器空信号 ● 模式故障、欠载、溢出或奇偶校验错误信号 ● SPI空闲信号 ● 通讯结束信号
其他功能	● 在CMOS输出和开漏输出之间切换 ● SPI初始化函数 ● Loopback mode
Module-stop function	可设置模块停止状态以降低功耗。
TrustZone Filter	可设置安全属性

注1.在主机接收和启用RSPCK自动停止功能时，不会发生溢出错误，因为在检测到溢出错误时会停止传输时钟。

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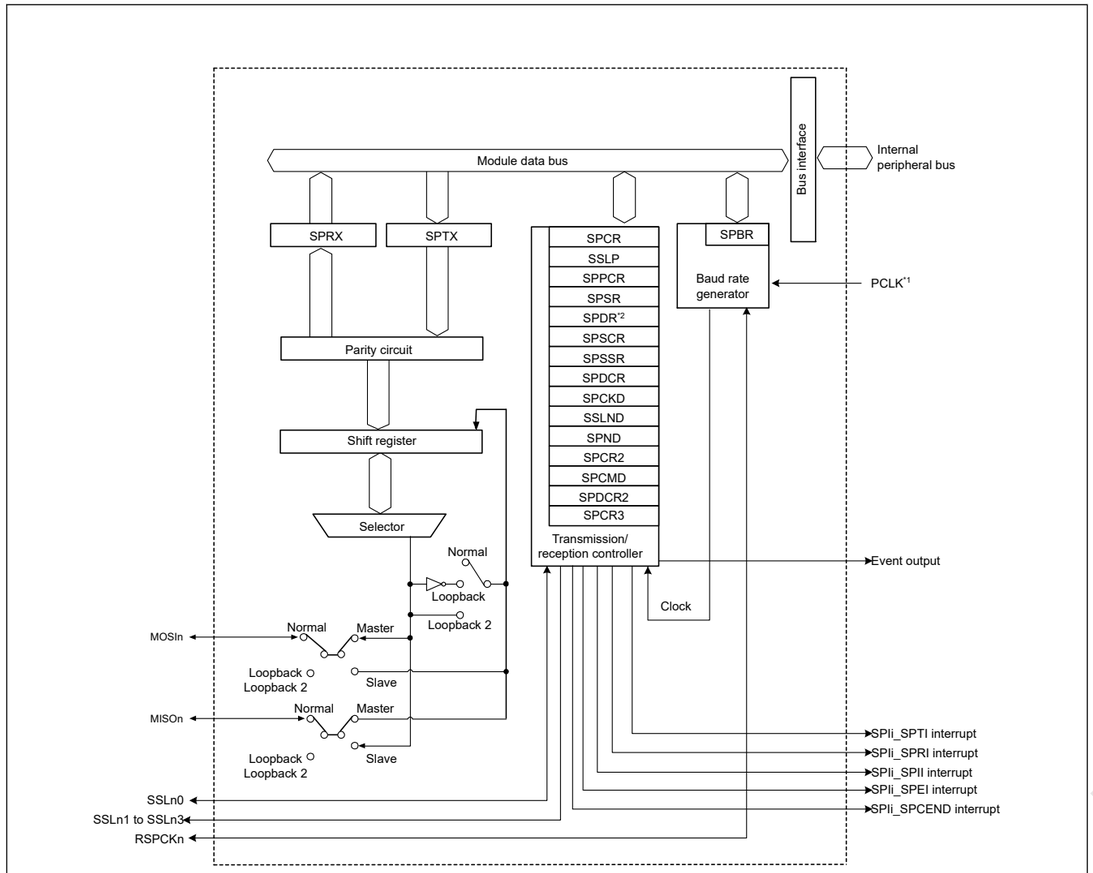


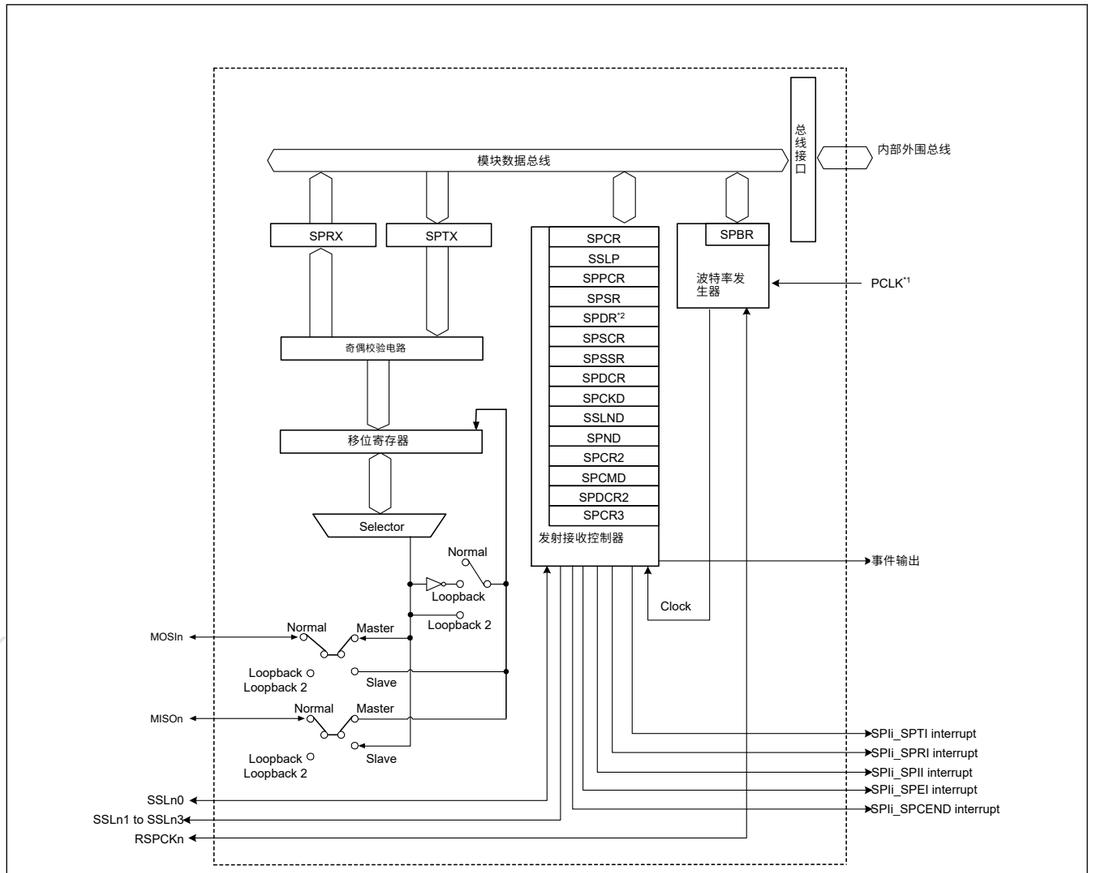
Note 1. PCLK = PCLKA
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
Note 3. m = 0 to 7

Figure 34.1 SPI block diagram

The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is set as an output when the SPI is a single master, and as an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 34.3.2. Controlling the SPI Pins.

Table 34.2 SPI I/O pins (1 of 2)

Channel	Pin name	I/O	Description
SPI0	RSPCKA	I/O	Clock input/output pin
	SSLA0	I/O	Slave selection input/output
	SSLA1 to SSLA3	Output	Slave selection output
	MOSIA	I/O	Master transmit data input/output
	MISOA	I/O	Slave transmit data input/output
SPI1	RSPCKB	I/O	Clock input/output pin
	MOSIB	I/O	Master transmit data input/output



Note 1. PCLK = PCLKA
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
注3.m=0到7

Figure 34.1 SPI框图

SPI自动切换SSLn0引脚的IO方向。当SPI为单主机时SSLn0设置为输出，当SPI为多主机或从机时设置为输入。RSPCKn、MOSIn和MISOn引脚会根据主机或从机设置以及SSLn0引脚上的电平输入自动设置为输入或输出。有关详细信息，请参阅第34.3.2节。控制SPI引脚。

Table 34.2 SPIIO引脚（2个中的1个）

Channel	引脚名称	I/O	Description
SPI0	RSPCKA	I/O	时钟输入输出引脚
	SSLA0	I/O	从机选择输入输出
	SSLA1 to SSLA3	Output	从机选择输出
	MOSIA	I/O	主机发送数据输入输出
	MISOA	I/O	从机发送数据输入输出
SPI1	RSPCKB	I/O	时钟输入输出引脚
	MOSIB	I/O	主机发送数据输入输出

Table 34.2 SPI I/O pins (2 of 2)

Channel	Pin name	I/O	Description
	MISOB	I/O	Slave transmit data input/output
	SSLB0	I/O	Slave selection input/output
	SSLB1 to SSLB3	Output	Slave selection output

Note: Pin names are indicated as "...A" or "...An" for SPI0, and "...B" or "...Bn" for SPI1 (n = 0, 1, 2, or 3).

34.2 Register Descriptions

34.2.1 SPCR : SPI Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPMS	SPI Mode Select 0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method)	R/W
1	TXMD	Communications Operating Mode Select 0: Select full-duplex synchronous serial communications 1: Select serial communications with transmit-only	R/W
2	MODFEN	Mode Fault Error Detection Enable 0: Disable detection of mode fault errors 1: Enable detection of mode fault errors	R/W
3	MSTR	SPI Master/Slave Mode Select 0: Select slave mode 1: Select master mode	R/W
4	SPEIE	SPI Error Interrupt Enable 0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests	R/W
5	SPTIE	Transmit Buffer Empty Interrupt Enable 0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests	R/W
6	SPE	SPI Function Enable 0: Disable SPI function 1: Enable SPI function	R/W
7	SPRIE	SPI Receive Buffer Full Interrupt Enable 0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests	R/W

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. For clock synchronous operation in master mode (MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. For clock synchronous operation in slave mode (MSTR = 0), always set the CPHA bit to 1. Do not perform operations if the CPHA bit is set to 0 for clock synchronous operation in slave mode (MSTR = 0).

Table 34.2 SPIIO引脚（2个中的2个）

Channel	引脚名称	I/O	Description
	MISOB	I/O	从机发送数据输入输出
	SSLB0	I/O	从机选择输入输出
	SSLB1 to SSLB3	Output	从机选择输出

Note: SPIO的引脚名称表示为"...A"或"...An"，SPI1的引脚名称表示为"...B"或"...Bn"（n=0、1、2或3）。

34.2 注册说明

34.2.1 SPCR:SPI控制寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPMS	SPI模式选择 0：选择SPI操作（4线方式）1：选择时钟同步操作（3线方式）	R/W
1	TXMD	通讯操作模式选择 0：选择全双工同步串行通信1：选择只发送串行通信	R/W
2	MODFEN	模式故障错误检测启用 0：禁用模式故障错误检测1：启用模式故障错误检测	R/W
3	MSTR	SPI主从模式选择 0：选择从模式1：选择主模式	R/W
4	SPEIE	SPI错误中断使能 0：禁用SPI错误中断请求1：启用SPI错误中断请求	R/W
5	SPTIE	发送缓冲区空中断使能 0：禁止发送缓冲区空中断请求1：允许发送缓冲区空中断请求	R/W
6	SPE	SPI功能使能 0：禁用SPI功能1：启用SPI功能	R/W
7	SPRIE	SPI接收缓冲器满中断使能 0：禁止SPI接收缓冲区满中断请求1：使能SPI接收缓冲区满中断请求	R/W

SPMS位（SPI模式选择）

SPMS位选择SPI操作（4线方法）或时钟同步操作（3线方法）。

SSLn0到SSLn3引脚不用于时钟同步操作。RSPCKn、MOSIn和MIOn引脚处理通信。对于主机模式下的时钟同步操作(MSTR=1)，SPCMDm.CPHA位可以设置为0或1。对于从机模式下的时钟同步操作(MSTR=0)，始终将CPHA位设置为1。不要如果CPHA位设置为0以在从机模式下进行时钟同步操作（MSTR=0），则执行操作。

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations. When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 34.3.6. Data Transfer Modes), and receive buffer full interrupt requests cannot be used.

TXMD setting is invalid in receive only slave mode.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault errors (see section 34.3.9. Error Detection). In addition, the SPI determines the I/O direction of the SSLni pins based on combination of the MODFEN and MSTR bits (see section 34.3.2. Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLni pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when one of the following occurs:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1

For details, see section 34.3.9. Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty. To generate a transmit buffer empty interrupt request when transmission starts, set the SPE and SPTIE bits to 1 at the same time or set the SPE bit to 1 after setting the SPTIE bit to 1.

When the SPTIE bit is 1, transmit buffer interrupts are generated even when the SPI function is disabled (when the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function. The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 34.3.9. Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 34.3.10. Initializing the SPI. In addition, a transmit buffer empty interrupt request is generated when the SPE bit is changed from 0 to 1 or from 1 to 0.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an SPI receive buffer full interrupt request when the SPI detects a receive buffer full write after completion of a serial transfer.

34.2.2 SSLP : SPI Slave Select Polarity Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

TXMD位（通信操作模式选择）

TXMD位选择全双工同步串行通信或仅发送操作。当该位设置为1时，SPI只执行发送操作而不执行接收操作（参见第34.3.6节。数据传输模式），并且无法使用接收缓冲区满中断请求。

TXMD设置在只接收从机模式下无效。

MODFEN位（模式故障错误检测使能）

MODFEN位启用或禁用模式故障错误检测（请参见第34.3.9节。错误检测）。此外，SPI根据MODFEN和MSTR位的组合确定SSLni引脚的IO方向（参见第34.3.2节。控制SPI引脚）。

MSTR位（SPI主从模式选择）

MSTR位选择SPI的主模式或从模式。根据MSTR位设置，SPI确定RSPCKn、MOSIn、MISOn和SSLni引脚的方向。

SPEIE位（SPI错误中断使能）

当发生以下情况之一时，SPEIE位启用或禁用SPI错误中断请求的生成：

- SPI检测到模式故障错误或欠载错误并将SPSR.MODF标志设置为1
- SPI检测到溢出错误并将SPSR.OVRF标志设置为1
- SPI检测到奇偶校验错误并将SPSR.PERF标志设置为1

有关详细信息，请参阅第34.3.9节。错误检测。

SPTIE位（发送缓冲区空中断允许）

当SPI检测到发送缓冲区为空时，SPTIE位使能或禁止生成发送缓冲区空中断请求。要在发送开始时产生发送缓冲区空中断请求，请将SPE和SPTIE位同时设置为1，或在将SPTIE位设置为1后将SPE位设置为1。

当SPTIE位为1时，即使禁用SPI功能（当SPE位变为0时）也会产生发送缓冲区中断。

SPE位（SPI功能使能）

SPE位启用或禁用SPI功能。当SPSR.MODF标志为1时，SPE位不能设置为1。详情请参见34.3.9节。错误检测。

将SPE位设置为0将禁用SPI功能并初始化部分模块功能。有关详细信息，请参阅第34.3.10节。初始化SPI。此外，当SPE位从0变为1或从1变为0时，会产生发送缓冲区空中断请求。

SPRIE位（SPI接收缓冲器满中断使能）

当SPI在串行传输完成后检测到接收缓冲区已满写入时，SPRIE位启用或禁用SPI接收缓冲区已满中断请求的生成。

34.2.2 SSLP：SPI从机选择极性寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SSL0P	SSLn0 Signal Polarity Setting 0: Set SSLn0 signal to active-low 1: Set SSLn0 signal to active-high	R/W
1	SSL1P	SSLn1 Signal Polarity Setting 0: Set SSLn1 signal to active-low 1: Set SSLn1 signal to active-high	R/W
2	SSL2P	SSLn2 Signal Polarity Setting 0: Set SSLn2 signal to active-low 1: Set SSLn2 signal to active-high	R/W
3	SSL3P	SSLn3 Signal Polarity Setting 0: Set SSLn3 signal to active-low 1: Set SSLn3 signal to active-high	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

34.2.3 SPPCR : SPI Pin Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPLP	SPI Loopback 0: Normal mode 1: Loopback mode (receive data = inverted transmit data)	R/W
1	SPLP2	SPI Loopback 2 0: Normal mode 1: Loopback mode (receive data = transmit data)	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	MOIFV	MOSI Idle Fixed Value 0: Set level output on MOSIn pin during MOSI idling to low 1: Set level output on MOSIn pin during MOSI idling to high	R/W
5	MOIFE	MOSI Idle Value Fixing Enable 0: Set MOSI output value to equal final data from previous transfer 1: Set MOSI output value to equal value set in the MOIFV bit	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then inverts the value of the input path for the shift register and connects it to the output path (loopback mode). For more information, see section 34.3.13. Loopback Mode.

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the value of the input path for the shift register to the output path (loopback mode) without inverting the value. For more information, see section 34.3.13. Loopback Mode.

Bit	Symbol	Function	R/W
0	SSL0P	SSLn0信号极性设置 0：将SSLn0信号设置为低电平有效 1：将SSLn0信号设置为高电平有效	R/W
1	SSL1P	SSLn1信号极性设置 0：将SSLn1信号设置为低电平有效 1：将SSLn1信号设置为高电平有效	R/W
2	SSL2P	SSLn2信号极性设置 0：将SSLn2信号设置为低电平有效 1：将SSLn2信号设置为高电平有效	R/W
3	SSL3P	SSLn3信号极性设置 0：设置SSLn3信号为低电平有效1 ：设置SSLn3信号为高电平有效	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

34.2.3 SPPCR:SPI引脚控制寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPLP	SPI Loopback 0：正常模式1：环回模式（接收数据=反转发送数据）	R/W
1	SPLP2	SPI Loopback 2 0：正常模式1：环回模式（接收数据=发送数据）	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	MOIFV	MOSI空闲固定值 0：在MOSI空闲期间将MOSIn引脚的电平输出设置为低1：在MOSI空闲期间将MOSIn引脚的电平输出设置为高	R/W
5	MOIFE	MOSI空闲值固定启用 0：设置MOSI输出值等于上次传输的最终数据1：设置MOSI输出值等于MOIFV位中设置的值	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

SPLP bit (SPI Loopback)

SPLP位选择SPI引脚的模式。当该位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MIOn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则关闭MOSIn引脚和移位寄存器之间的路径。SPI然后反转移位寄存器的输入路径的值并将其连接到输出路径（环回模式）。有关详细信息，请参阅第34.3.13节。环回模式。

SPLP2 bit (SPI Loopback 2)

SPLP2位选择SPI引脚的模式。当该位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MIOn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则关闭MOSIn引脚和移位寄存器之间的路径。然后SPI将移位寄存器的输入路径的值连接到输出路径（环回模式），而不反转该值。有关详细信息，请参阅第34.3.13节。环回模式。

MOIFV bit (MOSI Idle Fixed Value)

The MOIFV bit determines the MOSIn pin output value during the SSL negation period (including the SSL retention period during a burst transfer) when the MOIFE bit is 1 in master mode.

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI is in master mode and in an SSL negation period (including the SSL retention period during a burst transfer).When the MOIFE bit is 0, the SPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

34.2.4 SPSR : SPI Status Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRF	CENDF	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVRF	Overrun Error Flag 0: No overrun error occurred 1: Overrun error occurred	R/W*1
1	IDLNF	SPI Idle Flag 0: SPI is in the idle state 1: SPI is in the transfer state	R
2	MODF	Mode Fault Error Flag 0: No mode fault or underrun error occurred 1: Mode fault error or underrun error occurred	R/W*1
3	PERF	Parity Error Flag 0: No parity error occurred 1: Parity error occurred	R/W*1
4	UDRF	Underrun Error Flag The UDRF bit is valid when MODF flag is 1. 0: Mode fault error occurred (MODF = 1) 1: Underrun error occurred (MODF = 1)	R/W*1 *2
5	SPTEF	SPI Transmit Buffer Empty Flag 0: Data is in the transmit buffer 1: No data is in the transmit buffer	R/W*3
6	CENDF	Communication End Flag 0: Not communicating or communicating 1: Communication completed	R/W*1
7	SPRF	SPI Receive Buffer Full Flag 0: No valid data is in SPDR/SPDR_HA 1: Valid data is in SPDR/SPDR_HA	R/W*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. Clear the UDRF flag at the same time as the MODF flag.
Note 3. The write value should be 1.

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR bit = 1) and when the RSPCK clock auto-stop function is enabled (SPCR1.SCKASE bit = 1), overrun errors do not occur. This flag does not set to 1. For details, see section 34.3.9.1. Overrun errors.

[Setting condition]

When the next serial transfer ends and the receive buffer is full, and satisfy one of following.

MOIFV位（MOSI空闲固定值）

MOIFV位决定主模式下MOIFE位为1时SSL否定期间（包括突发传输期间的SSL保持期间）的MOSIn引脚输出值。

MOIFE位（MOSI空闲值固定启用）

MOIFE位固定SPI处于主机模式和SSL否定周期（包括突发传输期间的SSL保持周期）时的MOSIn输出值。当MOIFE位为0时，SPI输出上一个串行的最后一个数据在SSL否定期间传输到MOSIn引脚。当MOIFE位为1时，SPI将MOIFV位中设置的固定值输出到MOSIn引脚。

34.2.4 SPSR：SPI状态寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SPRF	CENDF	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
重置后的值：	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OVRF	溢出错误标志 0：未发生溢出错误1：发生溢出错误	R/W*1
1	IDLNF	SPI空闲标志 0：SPI处于空闲状态1：SPI处于传输状态	R
2	MODF	模式故障错误标志 0：未发生模式故障或欠载错误1：发生模式故障错误或欠载错误	R/W*1
3	PERF	奇偶校验错误标志 0：未发生奇偶校验错误1 ：发生奇偶校验错误	R/W*1
4	UDRF	欠载错误标志 当MODF标志为1时，UDRF位有效。 0：发生模式故障错误（MODF=1）1：发生欠载错误（MODF=1）	R/W*1 *2
5	SPTEF	SPI发送缓冲区空标志 0：发送缓冲区中有数据1：发送缓冲区中没有数据	R/W*3
6	CENDF	通讯结束标志 0：不通讯或通讯1：通讯完成	R/W*1
7	SPRF	SPI接收缓冲区满标志 0：SPDRSPDR_HA中没有有效数据1：SPDRSPDR_HA中有有效数据	R/W*3

注1.读1后只能写0清除标志。
注2.在清除MODF标志的同时清除UDRF标志。
注3.写入值应为1。

OVRF标志（溢出错误标志）

OVRF标志指示发生溢出错误。在主机模式（SPCR.MSTR位=1）和启用RSPCK时钟自动停止功能（SPCR1.SCKASE位=1）时，不会发生溢出错误。此标志不设置为1。有关详细信息，请参阅第34.3.9.1节。溢出错误。

[Setting condition]

当下一次串行传输结束且接收缓冲区已满时，满足以下条件之一。

RA生态工作室

- The SPCR.TXMD bit = 0. (transmit-receive master mode or transmit-receive slave mode or receive only slave mode)
- The SPCR.MSTR bit = 0, and the SPCR3.ETXMD bit = 1. (receive only slave mode)

[Clearing condition]

- When 0 is written to the OVRF flag after the OVRF flag is confirmed to be 1 by a read of SPSR.

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

[Setting conditions]

Master mode

- When none of the conditions in the master mode [Clearing condition] is met.

Slave mode

- When the SPE bit in SPCR is 1, enabling the SPI function.

[Clearing conditions]

Master mode

When condition 1 or all other conditions are satisfied.

Condition 1: The SPE bit in SPCR is 0, indicating that the SPI is initialized.

Condition 2: The transmit buffer (SPTX) is empty, indicating that data for the next transfer is not set.

Condition 3: The SPI internal sequencer is in the idle state, indicating that operation up to next-access delay is complete.

Condition 4: The SPCP[2:0] bits in SPSSR are 000 (at the beginning of sequence control)

Slave mode

- When condition 1 is satisfied.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. The UDRF flag indicates which error occurred.

[Setting conditions]

Multi-master mode

- When the input level of the SSLni pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Slave mode

- When condition 1 or 2 is satisfied.

Condition 1: The SSLni pin is negated before the RSPCK cycle required for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), triggering a mode fault error.

Condition 2: The serial transfer begins with the SPCR.MSTR bit is set to 0 (slave mode), the SPCR.SPE bit is set to 1, and the transmission data not prepared, triggering an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting).

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

When a serial transfer ends while the SPCR2.SPPE bit is 1, triggering a parity error, and satisfy one of following.

●SPCR.TXMD位=0。（发送-接收主模式或发送-接收从模式或仅接收从模式）

●SPCR.MSTR位=0，SPCR3.ETXMD位=1。（仅接收从机模式）

[Clearing condition]

●在通过读取SPSR确认OVRF标志为1后，向OVRF标志写入0时。

IDLNF标志（SPI空闲标志）

IDLNF标志指示SPI的传输状态。

[Setting conditions]

主模式

●当主模式[清除条件]中的条件均不满足时。

从机模式

●当SPCR的SPE位为1时，使能SPI功能。

[Clearing conditions]

主模式

当满足条件1或所有其他条件时。

条件1：SPCR中的SPE位为0，表示SPI已初始化。

条件2：发送缓冲区（SPTX）为空，表示未设置下一次传输的数据。

条件3：SPI内部定序器处于空闲状态，表示到next-accessdelay的操作已完成。

条件4：SPSSR中的SPCP[2:0]位为000（在序列控制开始时）

从机模式

●满足条件1时。

MODF标志（模式故障错误标志）

MODF标志指示发生模式故障错误或欠载错误。UDRF标志指示发生了哪个错误。

[Setting conditions]

Multi-master mode

●当SPCR.MSTR位为1（主模式）且SPCR.MODFEN位为1（使能模式故障错误检测）时，SSLni管脚的输入电平变为有效电平时，触发模式故障错误。

从机模式

●满足条件1或2时。

条件1：当SPCR.MSTR位为0（从模式）且SPCR.MODFEN位为1（启用模式故障错误检测）时，SSLni引脚在数据传输所需的RSPCK周期结束前被取反，触发模式故障错误。

条件2：串行传输开始时SPCR.MSTR位设置为0（从模式），SPCR.SPE位设置为1，传输数据未准备好，触发欠载错误。

SSLni信号的有效电平由SSLP.SSLiP位（SSLi信号极性设置）确定。

[Clearing condition]

●当此标志为1时读取SPSR，然后将0写入此标志。

PERF标志（奇偶校验错误标志）

PERF标志指示奇偶校验错误的发生。

[Setting condition]

当SPCR2.SPPE位为1时串行传输结束，触发奇偶校验错误，并满足以下之一。

- The SPCR.TXMD bit = 0. (transmit-receive master mode or transmit-receive slave mode or receive only slave mode)
- The SPCR.MSTR bit = 0, and the SPCR3.ETXMD bit = 1. (receive only slave mode)

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting condition]

- When the serial transfer begins with the SPCR.MSTR bit is set to 0 (slave mode), the SPCR3.ETXMD bit =0 (transmit-receive slave mode or transmit slave mode) the SPCR.SPE bit is set to 1, and the transmission data not prepared, triggering an underrun error.

[Clearing condition]

- When SPSR is read while this flag is 1, and then 0 is written to this flag.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- When condition 1. or 2. is satisfied.
  1. The SPCR.SPE bit is 0, indicating that the SPI is initialized.
  2. Transmit data (the frame size specified by the SPDCR.SPFC[1:0]) is transferred from the transmit buffer to the shift register.

[Clearing condition]

- When data is written to SPDR/SPDR_HA/SPDR_BY equals the number of frames set in the SPFC[1:0] bits in the SPI Data Control Register (SPDCR).

Data can only be written to SPDR/SPDR_HA/SPDR_BY when the SPTEF flag is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF flag is 0, data in the transmit buffer is not updated.

CENDF flag (Communication End Flag)

This flag indicates communication end status of RSPI. It turns 1 at communication end, and turns 0 at starting next communication.

[Setting condition]

Mastar mode

The following 3 conditions are met.

- The transmit buffer(SPTX) is empty. (There is no next transmission data.)
- The SPSSR.SPCP[2:0] are 000b. (It means the head of the sequential control.)
- The state of RSPI internal sequencer transferred to the idle state. (It means the next access delay has been completed.)

Transmit-receive / transmit only slave mode in SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

The following 3 conditions are met.

- The transmit buffer(SPTX) is empty. (There is no next transmission data.)
- The transmission shift register is empty. (It means RSPI does not do serial transfer.)
- SSL0 was negated.

Transmit-receive / transmit only slave mode in clock synchronous (3-wire: the SPCR.SPMS bit is 1)

The following 3 conditions are met.

- The transmit buffer(SPTX) is empty. (There is no next transmission data.)

●SPCR.TXMD位=0。（发送-接收主模式或发送-接收从模式或仅接收从模式）

●SPCR.MSTR位=0，SPCR3.ETXMD位=1。（仅接收从机模式）

[Clearing condition]

●当此标志为1时读取SPSR，然后将0写入此标志。

UDRF标志（欠载错误标志）

UDRF标志指示发生了欠载错误。

[Setting condition]

●当串行传输开始时SPCR.MSTR位设置为0（从机模式），SPCR3.ETXMD位=0（发送接收从机模式或发送从机模式）SPCR.SPE位设置为1，发送数据未准备好，触发欠载错误。

[Clearing condition]

●当此标志为1时读取SPSR，然后将0写入此标志。

SPTEF标志（SPI发送缓冲区空标志）

SPTEF标志指示SPI数据寄存器(SPDRSPDR_HA)的发送缓冲区的状态。

[Setting conditions]

●满足条件1.或2.时。

1.SPCR.SPE位为0，表示SPI初始化。

2.发送数据（由SPDCR.SPFC[1:0]指定的帧大小）从发送缓冲器传送到移位寄存器。

[Clearing condition]

●当数据写入SPDRSPDR_HASPDR_BY等于SPI数据控制寄存器(SPDCR)的SPFC[1:0]位中设置的帧数。

数据只能在SPTEF标志为1时写入SPDRSPDR_HASPDR_BY。如果在SPTEF标志为0时将数据写入SPDRSPDR_HA的发送缓冲区，则发送缓冲区中的数据不会更新。

CENDF标志（通信结束标志）

该标志指示RSPI的通信结束状态。通讯结束时变为1，开始下一次通讯时变为0。

[Setting condition]

Mastar mode

满足以下3个条件。

●发送缓冲区(SPTX)为空。（没有下一个传输数据。）

●SPSSR.SPCP[2:0]为000b。（表示顺序控制的头部。）

●RSPI内部定序器的状态转为空闲状态。（表示下一次访问延迟已经完成。）

SPI串行通信中的发送-接收仅发送从机模式（4线：SPCR.SPMS位为0）

满足以下3个条件。

●发送缓冲区(SPTX)为空。（没有下一个传输数据。）

●传输移位寄存器为空。（这意味着RSPI不进行串行传输。）

●SSL0被否定。

时钟同步中的发送-接收仅发送从模式（3线：SPCR.SPMS位为1）

满足以下3个条件。

●发送缓冲区(SPTX)为空。（没有下一个传输数据。）

- The transmission shift register is empty. (It means RSPI does not do serial transfer.)
- The last even edge of RSPCK of the last data was detected. (When the SPCMD.CPHA bit is “1”.)

Receive only slave mode in SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

The following condition is met.

- SSL0 was negated after the last data was written in the received buffer.

Receive only slave mode in clock synchronous (3-wire: the SPCR.SPMS bit is 1)

The following condition is met.

- The last even edge of RSPCK of the last data was detected. (When the SPCMD.CPHA bit is 1.)

[Clearing condition]

Master mode

Satisfy one of following.

- The next transmit data was written to the transmit buffer (SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1

Transmit-receive / transmit only slave mode

Satisfy one of following.

- The next transmit data was written to the transmit buffer(SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Receive only slave mode in SPI serial communication (4-wire: the SPCR.SPMS bit is 0)

Satisfy one of following.

- SSL0 assertion of next data was detected.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Receive only slave mode in clock synchronous (3-wire: the SPCR.SPMS bit is 1)

Satisfy one of following.

- The first edge of RSPCK of the next data was detected.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- Received data with the frame size specified by the SPDCR.SPFC[1:0] bits have been transferred to the SPDR from the shift register while the SPRF flag is 0. And satisfy one of following. However, the SPRF flag does not change from 0 to 1 while the OVRF flag = 1.
  - The SPCR.TXMD bit is 0 (transmit-receive master mode, transmit-receive slave mode, or receive only slave mode)
  - The SPCR.MSTR bit is 0 and the SPCR3.ETXMD bit is 1 (receive only slave mode)

[Clearing condition]

- When received data is read from the SPDR/SPDR_HA.

●传输移位寄存器为空。（这意味着RSPI不进行串行传输。）

●检测到最后一个数据的RSPCK的最后一个偶边沿。（当SPCMD.CPHA位为“1”时。）

SPI串行通信中仅接收从机模式（4线：SPCR.SPMS位为0）

满足以下条件。

●最后一个数据写入接收缓冲区后，SSL0被否定。

在时钟同步下仅接收从模式（3线：SPCR.SPMS位为1）

满足以下条件。

●检测到最后一个数据的RSPCK的最后一个偶边沿。（当SPCMD.CPHA位为1时。）

[Clearing condition]

主模式

满足以下之一。

●下一个发送数据被写入发送缓冲区(SPTX)。

●当CENDF标志为1时，读取SPSR后CENDF标志被写入0

发送-接收仅发送从模式

满足以下之一。

●下一个发送数据被写入发送缓冲区(SPTX)。

●当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

SPI串行通信中仅接收从机模式（4线：SPCR.SPMS位为0）

满足以下之一。

●检测到下一个数据的SSL0断言。

●当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

在时钟同步下仅接收从模式（3线：SPCR.SPMS位为1）

满足以下之一。

●检测到下一个数据的RSPCK的第一个边沿。

●当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

SPRF标志（SPI接收缓冲区满标志）

SPRF标志指示SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区的状态。

[Setting condition]

●在SPRF标志为0时，接收到的具有SPDCR.SPFC[1:0]位指定的帧大小的数据已从移位寄存器传送到SPDR。并且满足以下之一。但是，当OVRF标志=1时，SPRF标志不会从0变为1。

SPCR.TXMD位为0（发送-接收主机模式、发送-接收从机模式或仅接收从机模式）

SPCR.MSTR位为0，SPCR3.ETXMD位为1（仅接收从模式）

[Clearing condition]

●从SPDRSPDR_HA读取接收数据时。

34.2.5 SPDR/SPDR_HA/SPDR_BY : SPI Data Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

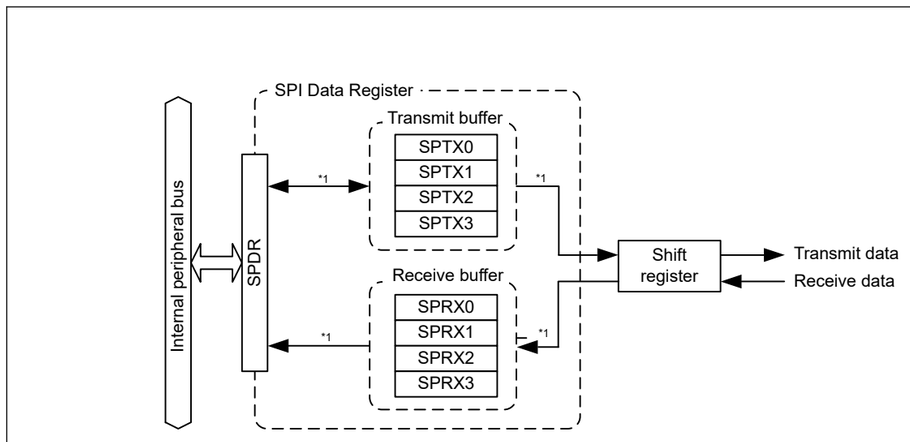
Offset address: 0x04

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	SPI Data	R/W

SPDR/SPDR_HA/SPDR_BY is the interface with the buffers that hold data for transmission and reception by the SPI. When accessing this register in words (the SPDCR.SPLW bit is 1), access SPDR. When accessing it in halfwords (the SPLW bit is 0), access SPDR_HA. When accessing it in byte (the SPDCR.SPBYT bit is 1), access SPDR_BY.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA. Figure 34.2 shows the configuration of the SPDR/SPDR_HA register.



Note: SPDR = SPDR/SPDR_HA/SPDR_BY
Note 1. The destination buffer and stage for access is automatically switched by the hardware.

Figure 34.2 Configuration of SPDR/SPDR_HA/SPDR_BY

The transmit and receive buffers each have one stages. The four stages of the buffer are all mapped to the single address of SPDR/SPDR_HA/SPDR_BY.

Data written to SPDR/SPDR_HA/SPDR_BY is written to a transmit-buffer stage (SPTXn) (n = 0 to 3), and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.

Additionally, if the data length is not 32 bits, bits not referred to in SPTXn (n = 0 to 3) are stored in the associated bits in SPRXn (n = 0 to 3). For example, if the data length is 9 bits, the received data is stored in the SPRXn[8:0] bits, and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus interface

SPDR/SPDR_HA/SPDR_BY is an interface with 32-bit wide transmit and receive buffers, each of which has one stages, for a total of 32 bytes. The 32 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA/SPDR_BY. Additionally, the unit of access for SPDR/SPDR_HA/SPDR_BY is selected by the SPI Word Access/Halfword Access Specification bit in the

34.2.5 SPDRSPDR_HASPDR_BY:SPI数据寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

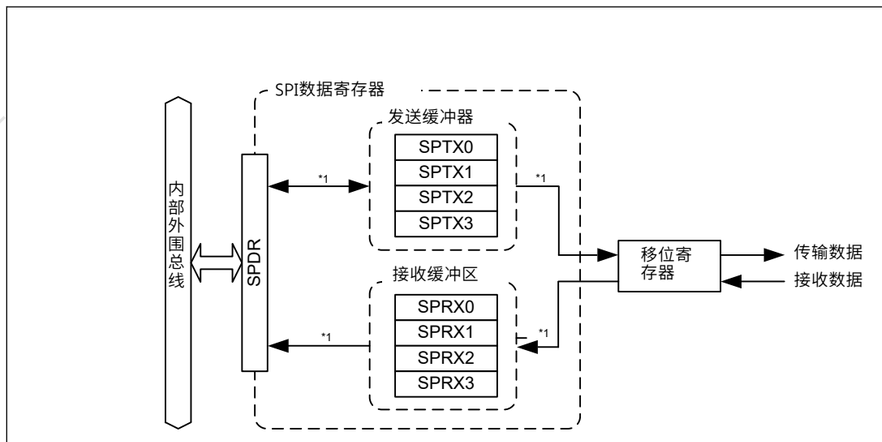
Offset address: 0x04

Bit position:	31																												0
Bit field:																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	SPI数据	R/W

SPDRSPDR_HASPDR_BY是与缓冲区的接口，缓冲区保存数据以供SPI发送和接收。以字访问该寄存器时（SPDCR.SPLW位为1），访问SPDR。当以半字访问它时（
SPLW位为0），访问SPDR_HA。当按字节访问时（SPDCR.SPBYT位为1），访问SPDR_BY。

发送缓冲区(SPTX)和接收缓冲区(SPRX)是独立的，但都映射到SPDRSPDR_HA。图34.2显示了SPDRSPDR_HA寄存器的配置。



Note: SPDR = SPDR/SPDR_HA/SPDR_BY
注1.访问的目标缓冲区和阶段由硬件自动切换。

Figure 34.2 SPDRSPDR_HASPDR_BY的配置

发送和接收缓冲器各有一级。缓冲区的四个阶段都映射到单个地址
SPDR/SPDR_HA/SPDR_BY.

写入SPDRSPDR_HASPDR_BY的数据被写入发送缓冲区级(SPTXn)(n=0到3)，然后从缓冲区发送。接收缓冲器在接收完成时保存接收到的数据。如果产生溢出，接收缓冲区不会更新。

此外，如果数据长度不是32位，SPTXn(n=0到3)中未提及的位将存储在
SPRXn（n=0到3）。例如，如果数据长度为9位，则接收到的数据存储在SPRXn[8:0]位中，而
SPTXn[31:9]位存储在SPRXn[31:9]位中。

(1) 总线接口

SPDRSPDR_HASPDR_BY是一个具有32位宽的发送和接收缓冲区的接口，每个缓冲区都有一个阶段，总共32个字节。32个字节映射到SPDRSPDR_HASPDR_BY的4字节地址空间。此外，SPDRSPDR_HASPDR_BY的访问单元由SPI字访问半字访问规范位选择

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SPI Data Control Register (SPDCR.SPLW). SPDR can also be accessed with the access size specified by the SPI Byte Access bit in the SPI Data Control Register (SPDCR.SPBYT).

Flush the transmission data at the LSB end of the register, and store the received data at the LSB end.

The following sections describe the operations involved in writing to and reading from SPDR/SPDR_HA/SPDR_BY.

Writing

Data written to SPDR/SPDR_HA/SPDR_BY is written to a transmit buffer (SPTXn). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA/SPDR_BY. The transmit buffer includes a transmit buffer write pointer that is automatically updated to reference the next stage each time data is written to SPDR/SPDR_HA/SPDR_BY.

Figure 34.3 shows the configuration of the bus interface with the transmit buffer when writing to SPDR/SPDR_HA/SPDR_BY.

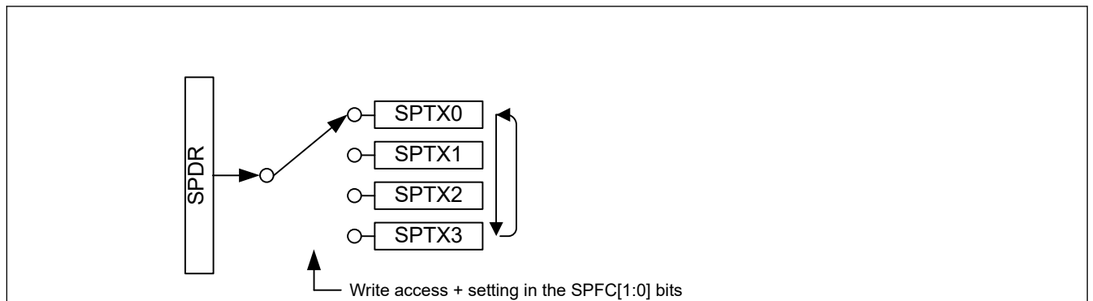


Figure 34.3 Configuration of SPDR/SPDR_HA/SPDR_BY for write access

The sequence for switching the transmit buffer write pointer differs with the setting of the number of frames specification bits in the SPI Data Control Register (SPDCR.SPFC[1:0]). The relationship of the SPFC[1:0] setting and the sequence of pointer switching from SPTX0 to SPTX3 is as follows:

- When SPFC[1:0] = 00b: SPTX0 → SPTX0 → SPTX0 → …
- When SPFC[1:0] = 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the SPI Function Enable bit in the SPI Control Register (SPCR.SPE) while the bit is 0, SPTX0 is the destination for the next write.

When writing to the transmit buffer (SPTXn) after generating the transmit buffer empty interrupt (when SPSR.SPTEF is 1), write the number of frames set in SPFC[1:0] in the SPI Data Control Register (SPDCR). Even when the specified number of frames is written to the transmit buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before generation of the next transmit buffer empty interrupt (when SPTEF is 0).

Reading

SPDR/SPDR_HA/SPDR_BY can be accessed to read the value of a receive buffer (SPRXn) or a transmit buffer (SPTXn). The setting in the SPI Receive/Transmit Data Select bit in the SPI Data Control Register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer. The sequence of reading the SPDR/SPDR_HA/SPDR_BY register is controlled by the independent receive buffer and transmit buffer read pointers.

Figure 34.4 shows the configuration of the bus interface with the receive and transmit buffers for reading from SPDR/SPDR_HA/SPDR_BY.

SPI数据控制寄存器(SPDCR.SPLW)。SPDR也可以通过SPI字节指定的访问大小进行访问
SPI数据控制寄存器(SPDCR.SPBYT)中的访问位。

在寄存器的LSB端刷新发送数据，在LSB端存储接收到的数据。

以下部分描述了写入和读取SPDRSPDR_HASPDR_BY所涉及的操作。

Writing

写入SPDRSPDR_HASPDR_BY的数据被写入发送缓冲区(SPTXn)。这不受价值的影响
SPDCR.SPRDTD位，与从SPDRSPDR_HASPDR_BY读取时不同。发送缓冲区包括一个发送缓冲区写指针，每次将数据写入SPDRSPDR_HASPDR_BY时，该指针会自动更新以引用下一阶段。

图34.3显示了写入SPDRSPDR_HA时带有发送缓冲区的总线接口的配置
SPDR_BY.

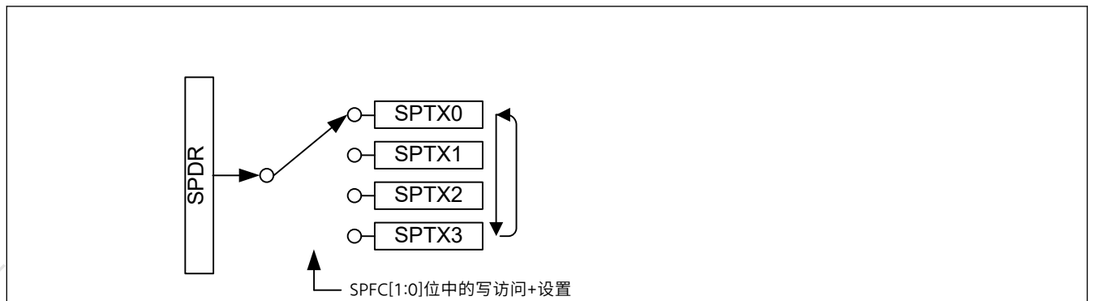


Figure 34.3 为写访问配置SPDRSPDR_HASPDR_BY

发送缓冲区写指针的切换顺序因SPI数据控制寄存器(SPDCR.SPFC[1:0])中帧数规范位的设置而异。SPFC[1:0]设置与指针从SPTX0切换到SPTX3的顺序关系如下：

- When SPFC[1:0] = 00b: SPTX0 → SPTX0 → SPTX0 → …
- When SPFC[1:0] = 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

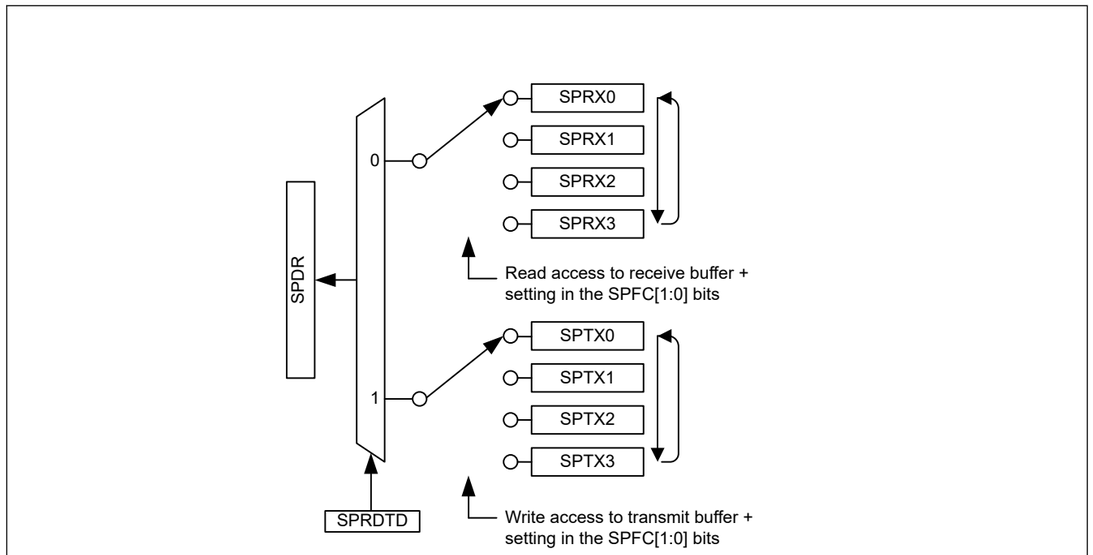
当1写入SPI控制寄存器(SPCR.SPE)中的SPI功能使能位且该位为0时，SPTX0是下一次写入的目标。

在产生发送缓冲区空中断后写入发送缓冲区(SPTXn)时（当SPSR.SPTEF为1时），将SPFC[1:0]中设置的帧数写入SPI数据控制寄存器(SPDCR)。即使指定的帧数被写入发送缓冲区(SPTXn)，缓冲区的值在写入完成后和下一个发送缓冲区空中断发生之前（SPTEF为0时）也不会更新。

Reading

SPDRSPDR_HA可以访问SPDR_BY以读取接收缓冲区(SPRXn)或发送缓冲区(SPTXn)的值。
SPI数据控制寄存器(SPDCR.SPRDTD)的SPI接收发送数据选择位中的设置选择读取接收缓冲区还是发送缓冲区。
读取SPDRSPDR_HASPDR_BY寄存器的顺序由独立的接收缓冲区和发送缓冲区读取指针控制。

图34.4显示了带有用于从SPDR读取的接收和发送缓冲区的总线接口配置
SPDR_HA/SPDR_BY.



Note: SPDR = SPDR/SPDR_HA/SPDR_BY

Figure 34.4 Configuration of SPDR/SPDR_HA/SPDR_BY for read access

Reading the receive buffer switches the receive buffer read pointer to the next buffer automatically. The switching sequence for the receive buffer read pointer is the same as that for the transmit buffer write pointer. However, when 1 is written to the SPI Function Enable bit in the SPI Control Register (SPCR.SPE) while the value of the bit is 1, SPRX0 is referenced by the buffer read pointer for the next read.

The transmit buffer read pointer is updated when writing to SPDR/SPDR_HA/SPDR_BY, but not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR/SPDR_HA/SPDR_BY is read.

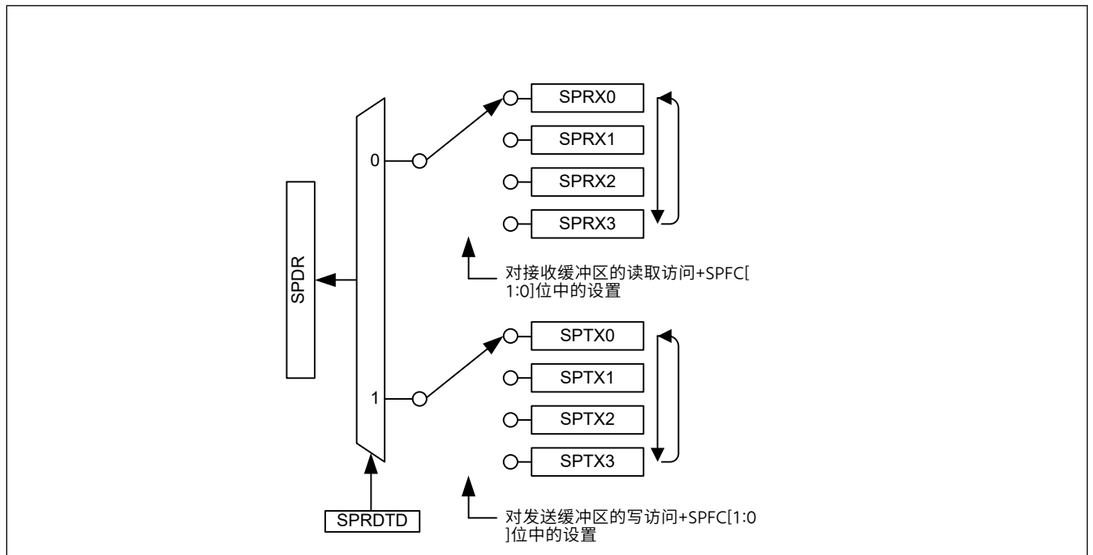
After a transmit buffer empty interrupt is generated, reading from the transmit buffer returns all 0s after the completion of writing the number of frames of data specified in the SPDCR.SPFC[1:0] bits, until the next buffer empty interrupt is generated (when SPTEF is 0).

34.2.6 SPSCR : SPI Sequence Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0



Note: SPDR = SPDR/SPDR_HA/SPDR_BY

Figure 34.4 为读取访问配置SPDRSPDR_HASPDR_BY

读取接收缓冲区会自动将接收缓冲区读取指针切换到下一个缓冲区。接收缓冲区读指针的切换顺序与发送缓冲区写指针的切换顺序相同。但是，当1写入SPI控制寄存器(SPCR.SPE)中的SPI功能使能位且该位的值为1时，缓冲区读取指针将引用SPRX0以进行下一次读取。

发送缓冲区读指针在写入SPDRSPDR_HASPDR_BY时更新，但在从发送缓冲区读取时不更新。从发送缓冲区读取时，会读取最近写入SPDRSPDR_HASPDR_BY的值。

产生发送缓冲区空中断后，在完成写入SPDCR.SPFC[1:0]位中指定的数据帧数后，从发送缓冲区读取返回全0，直到产生下一个缓冲区空中断（当SPTEF为0时）。

34.2.6 SPSCR:SPI序列控制寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPSLN[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPSLN[2:0]	SPI Sequence Length Specification The sequence length that is set in these bits determines the order in which the SPCMD0 to SPCMD07 registers are referenced. The setting defines the relationship between the sequence length and the SPCMD0 to SPCMD7 registers referenced by the SPI. In slave mode, the SPI references SPCMD0. 0 0 0: Sequence Length is 1 (Referenced SPCMDn, n = 0→0→…) 0 0 1: Sequence Length is 2 (Referenced SPCMDn, n = 0→1→0→…) 0 1 0: Sequence Length is 3 (Referenced SPCMDn, n = 0→1→2→0→…) 0 1 1: Sequence Length is 4 (Referenced SPCMDn, n = 0→1→2→3→0→…) 1 0 0: Sequence Length is 5 (Referenced SPCMDn, n = 0→1→2→3→4→0→…) 1 0 1: Sequence Length is 6 (Referenced SPCMDn, n = 0→1→2→3→4→5→0→…) 1 1 0: Sequence Length is 7 (Referenced SPCMDn, n = 0→1→2→3→4→5→6→0→…) 1 1 1: Sequence Length is 8 (Referenced SPCMDn, n = 0→1→2→3→4→5→6→7→0→…)	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPSCR specifies the sequence length when the SPI operates in master mode. Before changing the SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, check that the SPSR.IDLNF flag is 0.

SPSLN[2:0] bits (SPI Sequence Length Specification)

The SPSLN[2:0] bits specify the sequence length when the SPI in master mode performs sequential operations. The SPI in master mode changes the SPCMD0 to SPCMD7 registers to be referenced, and the order in which they are referenced is based on this sequence length setting. In slave mode, SPCMD0 is referenced.

34.2.7 SPSSR : SPI Sequence Status Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPCP[2:0]	SPI Command Pointer 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
3	—	This bit is read as 0.	R
6:4	SPECM[2:0]	SPI Error Command 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
7	—	This bit is read as 0.	R

SPSSR indicates the sequence control status when the SPI operates in master mode. Any writes to SPSSR are ignored.

Bit	Symbol	Function	R/W
2:0	SPSLN[2:0]	SPI序列长度规范 在这些位中设置的序列长度决定了SPCMD0到 引用了SPMD07寄存器。该设置定义了序列长度与SPI引用的SPCMD0到SPCMD7寄存器之间的关系。在从机模式下，SPI参考SPCMD0。 000：序列长度为1（参考SPCMDn，n=0→0→…）001：序列长度为2（参考SPCMDn，n=0→1→0→…）010：序列长度为3（参考SPCMDn，n=0→1→2→0→…）011：序列长度为4（参考SPCMDn，n=0→1→2→3→0→…）100：序列长度为5（参考SPCMDn，n=0→1→2→3→4→0→…）101：序列长度为6（参考SPCMDn，n=0→1→2→3→4→5→0→…）110：序列长度为7（参考SPCMDn，n=0→1→2→3→4→5→6→0→…）111：序列长度为8（参考SPCMDn，n=0→1→2→3→4→5→6→7→0→…）	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

SPSCR指定SPI在主模式下工作时的序列长度。在SPCR.MSTR和SPCR.SPE位均为1时更改SPSLN[2:0]位之前，请检查SPSR.IDLNF标志是否为0。

SPSLN[2:0]位（SPI序列长度规范）

SPSLN[2:0]位指定SPI在主模式下执行顺序操作时的序列长度。主机模式下的SPI将SPCMD0到SPCMD7寄存器更改为被引用，它们被引用的顺序基于此序列长度设置。在从模式下，以SPMD0为参考。

34.2.7 SPSSR：SPI序列状态寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x09

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SPECM[2:0]			—	SPCP[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPCP[2:0]	SPI命令指针 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
3	—	该位读为0。	R
6:4	SPECM[2:0]	SPI错误命令 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
7	—	该位读为0。	R

SPSSR指示SPI在主模式下工作时的序列控制状态。对SPSSR的任何写入都将被忽略。

SPCP[2:0] bits (SPI Command Pointer)

The SPCP[2:0] bits indicate the SPCMDm register that is referenced to by the pointer during sequence control by the SPI. For the SPI sequence control, see section 34.3.11.1. Master mode operation.

SPECM[2:0] bits (SPI Error Command)

The SPECM[2:0] bits indicate the SPCMDm register that is specified in the SPCP[2:0] bits when an error is detected during sequence control by the SPI. The SPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF flags are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning.

For the SPI error detection function, see section 34.3.9. Error Detection. For the SPI sequence control, see section 34.3.11.1. Master mode operation.

34.2.8 SPBR : SPI Bit Rate Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	Bit rate	R/W

SPBR sets the bit rate in master mode.

When the SPI is in slave mode, the bit rate depends on the bit rate of the input clock, regardless of the settings in SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting). Use bit rates that satisfy the electrical characteristics of the device.

The bit rate is determined by combinations of the SPBR and SPCMDm.BRDV[1:0] settings in the SPI Command Register. The equation for calculating the bit rate is given as follows:

$$\text{Bit rate} = \frac{f(\text{PCLK})}{2 \times (n+1) \times 2^N}$$

(PCLK = PCLKA)

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] setting (0, 1, 2, 3).

Table 34.3 lists examples of the relationship between the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 34.3 Relationship between SPBR settings, BRDV[1:0] settings, and bit rates

SPBR(n)	BRDV[1:0] bits (N)	Division ratio	Bit rate
			PCLKA = 32 MHz
0	0	2	16.0 Mbps
1	0	4	8.00 Mbps
2	0	6	5.33 Mbps
3	0	8	4.00 Mbps
4	0	10	3.20 Mbps
5	0	12	2.67 Mbps
5	1	24	1.33 Mbps
5	2	48	667 kbps
5	3	96	333 kbps
255	3	4096	7.81 kbps

SPCP[2:0]位（SPI命令指针）

SPCP[2:0]位指示在SPI序列控制期间指针所引用的SPCMDm寄存器。
有关SPI序列控制，请参见第34.3.11.1节。主模式操作。

SPECM[2:0]位（SPI错误命令）

SPECM[2:0]位指示在SPI序列控制期间检测到错误时在SPCP[2:0]位中指定的SPCMDm寄存器。SPI仅在检测到错误时更新SPECM[2:0]位。如果SPSR.OVRF和SPSR.MODF标志均为0且没有错误，则SPECM[2:0]位的值没有意义。

关于SPI错误检测功能，请参见第34.3.9节。错误检测。有关SPI序列控制，请参见第34.3.11.1节。
主模式操作。

34.2.8 SPBR:SPI比特率寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0A

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
7:0	n/a	比特率	R/W

SPBR在主模式下设置比特率。

当SPI处于从机模式时，比特率取决于输入时钟的比特率，与SPBR和SPMDm.BRDV[1:0]位（比特率分频设置）的设置无关。使用满足设备电气特性的比特率。

比特率由SPI命令寄存器中的SPBR和SPMDm.BRDV[1:0]设置的组合确定。
计算比特率的公式如下：

$$\text{比特率} = \frac{f(\text{PCLK})}{2 \times (n+1) \times 2^N}$$

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在等式中，n表示SPBR设置(0 1 2 … 255)，N表示BRDV[1:0]设置(0 1 2 3)。

表34.3列出了SPBR设置、BRDV[1:0]设置和比特率之间的关系示例。

Table 34.3 SPBR设置、BRDV[1:0]设置和比特率之间的关系

SPBR(n)	BRDV[1:0] bits (N)	分工比	比特率
			PCLKA = 32 MHz
0	0	2	16.0 Mbps
1	0	4	8.00 Mbps
2	0	6	5.33 Mbps
3	0	8	4.00 Mbps
4	0	10	3.20 Mbps
5	0	12	2.67 Mbps
5	1	24	1.33 Mbps
5	2	48	667 kbps
5	3	96	333 kbps
255	3	4096	7.81 kbps

34.2.9 SPDCR : SPI Data Control Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SPFC[1:0]	Number of Frames Specification 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SPRDTD	SPI Receive/Transmit Data Select 0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty	R/W
5	SPLW	SPI Word Access/Halfword Access Specification 0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access	R/W
6	SPBYT	SPI Byte Access Specification 0: SPDR/SPDR_HA is accessed in halfword or word (SPLW is valid) 1: SPDR_BY is accessed in byte (SPLW is invalid)	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

The SPI Data Control Register (SPDCR) is used to read the number of frames that can be stored in the SPDR register,read the SPDR register, and to set the access width for the SPDR register to word access, halfword access, or byte access. Up to four frames can be transmitted or received in one round of transmission or reception. The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPFC[1:0] bits.

When changing the SPFC[1:0] bits while the SPCR.SPE bit is 1, check that the SPSR.IDLNF flag is 0.

SPFC[1:0] bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR/SPDR_HA per transfer activation. Up to four frames can be transmitted or received in one round of transmission or reception.

When the number of transmission data frames specified in the SPFC[1:0] bits is written to the SPDR/SPDR_HA register, SPI clears the SPSR.SPTEF flag to 0 and begins transmitting. After that, when the number of transmission data frames specified in the SPFC[1:0] bits is transmitted to the shift register, the SPI generates the transmit buffer empty interrupt (SPSR.SPTEF sets to 1).

When the number of data frames specified in the SPFC[1:0] bits is received, the SPI generates the receive buffer full interrupt (SPSR.SPRF sets to 1).

Table 34.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits (1 of 2)

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or receive buffer is filled
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2

34.2.9 SPDCR:SPI数据控制寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SPFC[1:0]	帧数规格 00：1帧01： 2帧10：3帧1 1：4帧	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	SPRDTD	SPI接收发送数据选择 0：从接收缓冲区读取SPDRSPDR_HA值1：从发送缓冲区读取SPDRSPDR_HA值，但前提是发送缓冲区为空	R/W
5	SPLW	SPI字访问半字访问规范 0：将SPDR_HA设置为对半字访问有效1：将SPDR设置为对字访问有效	R/W
6	SPBYT	SPI字节访问规范 0：SPDRSPDR_HA以半字或字访问（SPLW有效）1：SPDR_BY以字节访问（SPLW无效）	R/W
7	—	该位读取为0。写入值应为0。	R/W

SPI数据控制寄存器(SPDCR)用于读取SPDR寄存器中可存储的帧数，读取SPDR寄存器，并将SPDR寄存器的访问宽度设置为字访问、半字访问或字节访问.在一轮发送或接收中最多可以发送或接收四帧。每次传输中的数据量由SPCMDm.SPB[3:0]位、SPSCR.SPSLN[2:0]位和SPFC[1:0]位的组合控制。

在SPCR.SPE位为1时更改SPFC[1:0]位时，检查SPSR.IDLNF标志是否为0。

SPFC[1:0]位（帧数规范）

SPFC[1:0]位指定每次传输激活时可以存储在SPDRSPDR_HA中的帧数。在一轮发送或接收中最多可以发送或接收四帧。

当SPFC[1:0]位中指定的传输数据帧数写入SPDRSPDR_HA寄存器时，SPI将SPSR.SPTEF标志清除为0并开始发送。之后，当SPFC[1:0]位中指定的发送数据帧数被发送到移位寄存器时，SPI产生发送缓冲区空中断（SPSR.SPTEF设置为1）。

当接收到SPFC[1:0]位中指定的数据帧数时，SPI产生接收缓冲区满中断（SPSR.SPRF设置为1）。

Table 34.4 SPSLN[2:0]和SPFC[1:0]位的可设置组合（2个中的1个）

Setting	SPSLN[2:0]	SPFC[1:0]	单个序列中的帧数	填充传输或接收缓冲区的帧数
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2

Table 34.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits (2 of 2)

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or receive buffer is filled
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the last value written to SPDR/SPDR_HA register is read. Read the transmit buffer after an SPI transmit buffer empty interrupt is generated until data of frames specified by SPFC[1:0] has been written (while the SPSR.SPTEF flag is 1).

For details, see section 34.2.5. SPDR/SPDR_HA/SPDR_BY : SPI Data Register.

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to SPDR in words is valid when the SPLW bit is 1. Also, when this bit is 0, set the SPI data length setting bits, SPCMDm.SPB[3:0], from 8 to 16 bits. Do not perform any operations when a data length of 20, 24, or 32 bits is specified.

SPBYT bit (SPI Byte Access Specification)

The SPBYT bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR/SPDR_HA. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR_BY.

When SPBYT = 1, set the SPI data length bits (SPB[3:0]) in the SPI Command Register m (SPCMDm) to 8 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bit, subsequent operation is not guaranteed.

34.2.10 SPCKD : SPI Clock Delay Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK Delay Setting 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPCKD specifies the RSPCK delay, the period from the beginning of SSLni signal assertion to RSPCK oscillation, when the SPCMDm.SCKDEN bit is 1.

Table 34.4 SPSLN[2:0]和SPFC[1:0]位的可设置组合（2个中的2个）

Setting	SPSLN[2:0]	SPFC[1:0]	单个序列中的帧数	填充传输或接收缓冲区的帧数
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD位（SPI接收发送数据选择）

SPRDTD位选择SPDRSPDR_HA是从接收缓冲区还是从发送缓冲区读取值。如果从发送缓冲区读取，则读取写入SPDRSPDR_HA寄存器的最后一个值。在产生SPI发送缓冲区空中断后读取发送缓冲区，直到SPFC[1:0]指定的帧数据被写入（此时SPSR.SPTEF标志为1）。

有关详细信息，请参阅第34.2.5节。SPDRSPDR_HASPDR_BY：SPI数据寄存器。

SPLW位（SPI字访问半字访问规范）

SPLW位指定SPDR的访问宽度。当SPLW位为0时，以半字访问SPDR_HA有效，当SPLW位为1时，以字访问SPDR有效。此外，当该位为0时，设置SPI数据长度设置位SPMDm.SPB[3：0]，从8到16位。当指定数据长度为20、24或32位时，请勿执行任何操作。

SPBYT位（SPI字节访问规范）

SPBYT位用于设置访问SPI数据寄存器(SPDR)的数据宽度。当SPBYT=0时，使用字或半字访问SPDRSPDR_HA。当SPBYT=1时（在这种情况下，SPLW无效），使用对SPDR_BY的字节访问。

当SPBYT=1时，将SPI命令寄存器m(SPCMDm)中的SPI数据长度位(SPB[3:0])设置为8位。如果SPB[3:0]设置为9至16、20、24或32位，不保证后续操作。

34.2.10 SPCKD:SPI时钟延迟寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SCKDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SCKDL[2:0]	RSPCK延迟设置 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

SPCKD指定RSPCK延迟，即从SSLni信号断言开始到RSPCK振荡的周期，当SPCMDm.SCKDEN位为1时。

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits specify an RSPCK delay value when the SPCMDm.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

34.2.11 SSLND : SPI Slave Select Negation Delay Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SLNDL[2:0]	SSL Negation Delay Setting 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SSLND specifies the SSL negation delay, the period from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits specify an SSL negation delay value when the SLNDEN bit in SPCMDn is 1 and the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

34.2.12 SPND : SPI Next-Access Delay Register

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPNDL[2:0]	SPI Next-Access Delay Setting 0 0 0: 1 RSPCK + 2 PCLKA 0 0 1: 2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1: 4 RSPCK + 2 PCLKA 1 0 0: 5 RSPCK + 2 PCLKA 1 0 1: 6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W

SPND specifies the next-access delay, the non-active period of the SSLni signal after termination of a serial transfer, when the SPCMDm.SPNDEN bit is 1.

SCKDL[2:0]位（RSPCK延迟设置）

当SPCMDm.SCKDEN位为1时，SCKDL[2:0]位指定RSPCK延迟值。在从机模式下使用SPI时，将SCKDL[2:0]位设置为000b。

34.2.11 SSLND:SPI从机选择否定延迟寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SLNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SLNDL[2:0]	SSL否定延迟设置 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

SSLND指定SSL否定延迟，从传输最终RSPCK边缘到否定SPI在主模式下进行串行传输期间的SSLni信号。如果SSLND的内容发生更改，而SPCR.MSTR和SPCR.SPE位为1，不执行后续操作。

SLNDL[2:0]位（SSL否定延迟设置）

当SPCMDn中的SLNDEN位为1且SPI处于主模式时，SLNDL[2:0]位指定SSL否定延迟值。在从机模式下使用SPI时，将SLNDL[2:0]位设置为000b。

34.2.12 SPND:SPI下一次访问延迟寄存器

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0E

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SPNDL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SPNDL[2:0]	SPI下一次访问延迟设置 0 0 0: 1 RSPCK + 2 PCLKA 0 0 1: 2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1: 4 RSPCK + 2 PCLKA 1 0 0: 5 RSPCK + 2 PCLKA 1 0 1: 6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W

当SPMDm.SPNDEN位为1时，SPND指定下一次访问延迟，即串行传输终止后SSLni信号的非活动期。

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits specify a next-access delay when the SPCMDm.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

34.2.13 SPCR2 : SPI Control Register 2

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPPE	Parity Enable 0: Do not add parity bit to transmit data and do not check parity bit of receive data 1: When SPCR.TXMD = 0: Add parity bit to transmit data and check parity bit of receive data When SPCR.TXMD = 1: Add parity bit to transmit data but do not check parity bit of receive data	R/W
1	SPOE	Parity Mode 0: Select even parity for transmission and reception 1: Select odd parity for transmission and reception	R/W
2	SPIIE	SPI Idle Interrupt Enable 0: Disable idle interrupt requests 1: Enable idle interrupt requests	R/W
3	PTE	Parity Self-Testing 0: Disable self-diagnosis function of the parity circuit 1: Enable self-diagnosis function of the parity circuit	R/W
4	SCKASE	RSPCK Auto-Stop Function Enable 0: Disable RSPCK auto-stop function 1: Enable RSPCK auto-stop function	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data.

When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of bits whose value is 1 in the transmit or receive character plus the parity bit is odd.

The SPOE bit is only valid when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an idle state is detected in the SPI and the SPSR.IDLNF flag clears is set to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables self-diagnosis of the parity circuit to check whether the parity function is operating correctly.

SPNDL[2:0]位（SPI下一次访问延迟设置）

当SPMDm.SPNDEN位为1时，SPNDL[2:0]位指定下一次访问延迟。在从机模式下使用SPI时，将SPNDL[2:0]位设置为000b。

34.2.13 SPCR2：SPI控制寄存器2

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x0F

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SPPE	奇偶校验使能 0：发送数据不添加奇偶校验位，接收数据不校验校验位1：当SPCR.TXMD=0：发送数据添加校验位，接收数据校验校验位当SPCR.TXMD=1：添加校验位位发送数据但不检查接收数据的奇偶校验位	R/W
1	SPOE	奇偶校验模式 0：发送和接收选择偶校验1：发送和接收选择奇校验	R/W
2	SPIIE	SPI空闲中断使能 0：禁用空闲中断请求1：启用空闲中断请求	R/W
3	PTE	Parity Self-Testing 0：禁用奇偶电路自诊断功能1：启用奇偶电路自诊断功能	R/W
4	SCKASE	RSPCK自动停止功能启用 0：禁用RSPCK自动停止功能1：启用RSPCK自动停止功能	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

SPPE bit (Parity Enable)

SPPE位启用或禁用奇偶校验功能。

当SPCR.TXMD位为0且该位为1时，发送数据添加奇偶校验位，接收数据执行奇偶校验。

当SPCR.TXMD位为1且该位为1时，发送数据添加奇偶校验位，但接收数据不执行奇偶校验。

SPOE bit (Parity Mode)

SPOE位指定奇校验或偶校验。

当设置了偶校验时，执行奇偶校验位相加，以使发送或接收字符中值为1的总位数加上奇偶校验位为偶数。类似地，当设置奇校验时，执行校验位相加，使得发送或接收字符中值为1的位加上奇偶校验位的总数为奇数。

SPOE位仅在SPPE位为1时有效。

SPIIE位（SPI空闲中断允许）

当在SPI中检测到空闲状态并且SPSR.IDLNF标志清除设置为0时，SPIIE位启用或禁用SPI空闲中断请求的生成。

PTE bit (Parity Self-Testing)

PTE位启用奇偶校验电路的自诊断，以检查奇偶校验功能是否正常运行。

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs, when data is received in master mode. For details, see section 34.3.9.1. Overrun errors.

34.2.14 SPCMDm : SPI Command Register m (m = 0 to 7)

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10 + 0x02 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	CPHA	RSPCK Phase Setting 0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge	R/W
1	CPOL	RSPCK Polarity Setting 0: Set RSPCK low during idle 1: Set RSPCK high during idle	R/W
3:2	BRDV[1:0]	Bit Rate Division Setting 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8	R/W
6:4	SSLA[2:0]	SSL Signal Assertion Setting 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 Others: Setting prohibited	R/W
7	SSLKP	SSL Signal Level Keeping 0: Negate all SSL signals on completion of transfer 1: Keep SSL signal level from the end of transfer until the beginning of the next access	R/W
11:8	SPB[3:0]	SPI Data Length Setting 0x0: 20 bits 0x1: 24 bits 0x2: 32 bits 0x3: 32 bits 0x8: 9 bits 0x9: 10 bits 0xA: 11 bits 0xB: 12 bits 0xC: 13 bits 0xD: 14 bits 0xE: 15 bits 0xF: 16 bits Others: 8 bits	R/W
12	LSBF	SPI LSB First 0: MSB-first 1: LSB-first	R/W
13	SPNDEN	SPI Next-Access Delay Enable 0: Select next-access delay of 1 RSPCK + 2 PCLKA 1: Select next-access delay equal to the setting in the SPI Next-Access Delay Register (SPND)	R/W

SCKASE位（RSPCK自动停止功能使能）

SCKASE位启用或禁用RSPCK自动停止功能。启用此功能后，在主机模式下接收数据时，RSPCK时钟会在发生溢出错误之前停止。有关详细信息，请参阅第34.3.9.1节。溢出错误。

34.2.14 SPCMDm：SPI命令寄存器m（m=0到7）

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x10 + 0x02 × m

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Function	R/W
0	CPHA	RSPCK相位设置 0：选择前沿数据采样，后沿数据变化1：选择前沿数据变化，后沿数据采样	R/W
1	CPOL	RSPCK极性设置 0：空闲时将RSPCK设置为低1 ：空闲时将RSPCK设置为高	R/W
3:2	BRDV[1:0]	比特率划分设置 00：基本比特率01：基本比特率除以210：基本比特率除以411：基本比特率除以8	R/W
6:4	SSLA[2:0]	SSL信号断言设置 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 其他：禁止设置	R/W
7	SSLKP	SSL信号电平保持 0：在传输完成时否定所有SSL信号1：从传输结束到下一次访问开始时保持SSL信号电平	R/W
11:8	SPB[3:0]	SPI数据长度设置 0x0: 20 bits 0x1: 24 bits 0x2: 32 bits 0x3: 32 bits 0x8: 9 bits 0x9: 10 bits 0xA: 11 bits 0xB: 12 bits 0xC: 13 bits 0xD: 14 bits 0xE: 15 bits 0xF: 16 bits Others: 8 bits	R/W
12	LSBF	SPILSB优先 0: MSB-first 1: LSB-first	R/W
13	SPNDEN	SPI下一次访问延迟使能 0：选择下一次访问延迟1RSPCK+2PCLKA1：选择下一次访问延迟等于SPI下一次访问延迟寄存器(SPND)中的设置	R/W

Bit	Symbol	Function	R/W
14	SLNDEN	SSL Negation Delay Setting Enable 0: Select SSL negation delay of 1 RSPCK 1: Select SSL negation delay equal to the setting in the SPI Slave Select Negation Delay Register (SSLND)	R/W
15	SCKDEN	RSPCK Delay Setting Enable 0: Select RSPCK delay of 1 RSPCK 1: Select RSPCK delay equal to the setting in the SPI Clock Delay Register (SPCKD)	R/W

The SPCMDm registers specify the transfer format for the SPI in master mode. Each channel has eight SPCMDm (m = 0 to 7). Some of the bits in the SPCMD0 registers are used to set the transfer mode for the SPI in slave mode. The SPI in master mode sequentially references the SPCMDm registers based on the settings in the SPSCR.SPSLN[2:0] bits and executes the serial transfer that is set in the referenced SPCMDm registers.

Set the SPCMDm registers while the transmit buffer is empty (SPSR.SPTEF is 1 and data for the next transfer is not set) and before the setting of the data to be transmitted when that SPCMDm registers is referenced.

The SPCMDm registers referenced by the SPI in master mode can be checked by means of the SPSSR.SPCP[2:0] bits.

CPHA bit (RSPCK Phase Setting)

The CPHA bit selects the RSPCK phase of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

CPOL bit (RSPCK Polarity Setting)

The CPOL bit selects the RSPCK polarity of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate in combination with the settings in the SPBR register. (see section 34.2.8. SPBR : SPI Bit Rate Register). The SPBR settings determine the base bit rate. The BRDV[1:0] setting selects the bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. Different BRDV[1:0] bit settings can be specified in the SPCMD0 register. This enables execution of serial transfers at different bit rates for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode. When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLn0 pin acts as input).

When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP bit (SSL Signal Level Keeping)

When the SPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLni signal level for the current command is to be kept or negated between the SSL negation associated with the current command and the SSL assertion associated with the next command. Setting the SSLKP bit to 1 enables a burst transfer. For details, see section 34.3.11.1. Master mode operation. When using the SPI in slave mode, set the SSLKP bit to 0.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits specify the transfer data length for the SPI in master or slave mode.

LSBF bit (SPI LSB First)

The LSBF bit specifies the data format of the SPI in master or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit specifies the next-access delay, the period from the time the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access. If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLKA. If the SPNDEN bit is 1, the SPI inserts a next-access delay according to the SPND setting.

Bit	Symbol	Function	R/W
14	SLNDEN	SSL否定延迟设置启用 0：选择SSL否定延迟1RSPCK1：选择SSL否定延迟等于SPI从选择否定延迟寄存器(SSLND)中的设置	R/W
15	SCKDEN	RSPCK延迟设置启用 0：选择RSPCK延迟为1RSPCK1：选择RSPCK延迟等于SPI时钟延迟寄存器(SPCKD)中的设置	R/W

SPCMDm寄存器指定主模式下SPI的传输格式。每个通道有8个SPCMDm（m=0到7）。SPCMD0寄存器中的一些位用于设置SPI在从机模式下的传输模式。主机模式下的SPI根据SPSCR.SPSLN[2:0]位中的设置顺序引用SPCMDm寄存器，并执行在引用的SPCMDm寄存器中设置的串行传输。

在发送缓冲区为空时（SPSR.SPTEF为1且未设置下一次传输的数据）和设置要发送的数据之前，当引用该SPCMDm寄存器时设置SPCMDm寄存器。

SPI在主模式下引用的SPCMDm寄存器可以通过SPSSR.SPCP[2:0]位进行检查。

CPHA位（RSPCK相位设置）

CPHA位在主模式或从模式下选择SPI的RSPCK相位。SPI模块之间的数据通信需要模块之间相同的RSPCK相位设置。

CPOL位（RSPCK极性设置）

CPOL位在主模式或从模式下选择SPI的RSPCK极性。SPI模块之间的数据通信要求模块之间的RSPCK极性设置相同。

BRDV[1:0]位（比特率划分设置）

BRDV[1:0]位结合SPBR寄存器中的设置确定比特率。（参见第34.2.8节。SPBR：SPI比特率寄存器）。SPBR设置决定了基本比特率。BRDV[1:0]设置选择通过将基本比特率除以1、2、4或8获得的比特率。可以在SPCMD0寄存器中指定不同的BRDV[1:0]位设置。这使得每个命令能够以不同的比特率执行串行传输。

SSLA[2:0]位（SSL信号断言设置）

当SPI在主模式下执行串行传输时，SSLA[2:0]位控制SSLni信号断言。当一个SSLni信号被置位，其极性由相关SSLP中设置的值确定。当SSLA[2:0]位在多主机模式下设置为000b时，串行传输在所有SSL信号处于否定状态时执行（因为SSLn0引脚用作输入）。

在从机模式下使用SPI时，将SSLA[2:0]位设置为000b。

SSLKP位（SSL信号电平保持）

当主模式的SPI执行串行传输时，SSLKP位指定当前命令的SSLni信号电平是在与当前命令关联的SSL否定和与下一个命令关联的SSL断言之间保持还是否定。将SSLKP位设置为1可启用突发传输。有关详细信息，请参阅第34.3.11.1节。主模式操作。在从机模式下使用SPI时，将SSLKP位设置为0。

SPB[3:0]位（SPI数据长度设置）

SPB[3:0]位指定SPI在主模式或从模式下的传输数据长度。

LSBF bit (SPI LSB First)

LSBF位指定SPI在主模式或从模式下的数据格式为MSB优先或LSB优先。

SPNDEN位（SPI下一次访问延迟使能）

SPNDEN位指定下一次访问延迟，即从主模式下的SPI终止串行传输并将SSLni信号设置为无效到SPI为下一次访问启用SSLni信号断言的时间段。如果SPNDEN位为0，则SPI将下一次访问延迟设置为1RSPCK+2PCLKA。如果SPNDEN位为1，则SPI根据SPND设置插入下一次访问延迟。

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit specifies the SSL negation delay, the period from the time the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal to inactive. If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal at the SSL negation delay according to the SSLND setting.

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit specifies the SPI clock delay, the period from the point when the SPI in master mode asserts the SSLni signal until the RSPCK starts oscillation. If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at an RSPCK delay according to the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

34.2.15 SPDCR2 : SPI Data Control Register 2

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SINV	BYSW
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BYSW	Byte Swap Operating Mode Select 0: Byte Swap OFF 1: Byte Swap ON	R/W
1	SINV	Serial Data Invert Bit 0: Not invert serial data 1: Invert serial data	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

SPI Data Control Register 2 (SPDCR2) is the setting register, that is to swap a transmit/receive data in byte units and to invert serial data. If these bits are modified while the SPI in slave mode is enabled (SPCR.SPE = 1), subsequent operation is not guaranteed.

BYSW bit (Byte Swap Operating Mode Select)

It is a setting bit, that is to swap a transmit/receive data in byte units. When byte access is valid (SPDCR.SPBYT = 1), byte swap is invalid. When byte swap is valid, parity function must be invalid (SPCR2.SPPE bit = 0). Setting change of BYSW bit must be SPCR.SPE bit = 0.

A data after byte swap is different by a data length (setting of SPCMD.SPB[3:0]).

When byte swap, A data length (setting of SPB[3:0]) must be set to 32 bit or 16bit. Other case of data length (that is 8 to 15, 20, 24 bit length), byte swap is not guaranteed. Before swap and after swap are shown below (length data (32 bit/16 bit)).

- Length data 32 bits (SPB[3:0] = 0010b or 0011b)

  Before swap: [31:24] [23:16] [15:8] [7:0]

  After swap: [7:0] [15:8] [23:16] [31:24]
- Length data 16 bit (SPB[3:0] = 1111b)

  Before swap: [31:24] [23:16]

  After swap: [23:16] [31:24]

When byte access mode (SPDCR.SPBT = 1), byte swap setting is invalid.

在从机模式下使用SPI时，将SPNDEN位设置为0。

SLNDEN位（SSL否定延迟设置启用）

SLNDEN位指定SSL否定延迟，即从主模式下的SPI停止RSPCK振荡到SPI将SSLni信号设置为无效的时间段。如果SLNDEN位为0，则SPI将SSL否定延迟设置为1RSPCK。如果SLNDEN位为1，则SPI根据SSLND设置在SSL否定延迟时否定SSL信号。

在从机模式下使用SPI时，将SLNDEN位设置为0。

SCKDEN位（RSPCK延迟设置使能）

SCKDEN位指定SPI时钟延迟，即从主模式下的SPI断言SSLni信号到RSPCK开始振荡的周期。如果SCKDEN位为0，则SPI将RSPCK延迟设置为1RSPCK。如果SCKDEN位为1，则SPI根据SPCKD设置以RSPCK延迟启动RSPCK的振荡。

在从机模式下使用SPI时，将SCKDEN位设置为0。

34.2.15 SPDCR2:SPI数据控制寄存器2

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x20

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SINV	BYSW
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BYSW	字节交换操作模式选择 0：字节交换关闭1 ：字节交换开启	R/W
1	SINV	串行数据反转位 0：不反转串行数据1： 反转串行数据	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

SPI数据控制寄存器2(SPDCR2)是设置寄存器，即以字节为单位交换发送接收数据和反转串行数据。如果在使能从模式下的SPI(SPCR.SPE=1)时修改这些位，则无法保证后续操作。

BYSW位（字节交换操作模式选择）

它是一个设置位，即以字节为单位交换一个发送接收数据。当字节访问有效时（SPDCR.SPBYT=1），字节交换无效。当字节交换有效时，奇偶校验功能必须无效（SPCR2.SPPE位=0）。BYSW位的设置更改必须是SPCR.SPE位=0。

字节交换后的数据因数据长度不同（SPCMD.SPB[3:0]的设置）。

字节交换时，A数据长度（SPB[3:0]的设置）必须设置为32位或16位。其他数据长度情况（即8到15、20、24位长度），不保证字节交换。交换前和交换后如下所示（长度数据（32位16位））。

●长度数据32位(SPB[3:0]=0010b或0011b)

Before swap: [31:24] [23:16] [15:8] [7:0]

After swap: [7:0] [15:8] [23:16] [31:24]

●长度数据16位(SPB[3:0]=1111b)

Before swap: [31:24] [23:16]

After swap: [23:16] [31:24]

当字节访问模式（SPDCR.SPBT=1）时，字节交换设置无效。

When byte swap is valid, set parity function to invalid (SPCR2.SPPE = 0). When the parity function set to valid, the behavior is not guaranteed.

SINV bit (Serial Data Invert Bit)

This bit is used to invert transmit data and receive data.

When the SINV bit is set to 1, transmit buffer (SPTX) data is inverted to invert transmit data and receive data, and then the inverted data is stored in the receive buffer (SPRX). The parity bit is the value corresponding to the inverted transmission/ reception data.

34.2.16 SPCR3 : SPI Control Register 3

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x21

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CENDIE	—	—	BFDS	ETXMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ETXMD	Extended Communication Mode Select 0: Full-duplex synchronous or transmit-only serial communications. [the SPCR.TXMD bit is enabled] 1: Receive-only serial communications in slave mode (SPCR.MSTR bit = 0). [the SPCR.TXMD bit is disabled] Setting is prohibited in master mode (SPCR.MSTR bit = 1).	R/W
1	BFDS	Between Burst Transfer Frames Delay Select 0: Delay (RSPCK delay, SSL negation delay and next-access delay) between frames is inserted in burst transfer. 1: Delay between frames is not inserted in burst transfer.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	CENDIE	RSPI Communication End Interrupt Enable 0: Communication end interrupt request is disabled. 1: Communication end interrupt request is enabled.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

SPI control register 3 (SPCR3) is control register for operation mode. If you change the value of ETXMD and BFDS when the SPCR.SPE bit is 1, the SPI operation does not guarantee.

ETXMD bit (Extended Communication Mode Select)

This bit is valid on slave mode only (the SPCR.MSTR bit is 0). This bit select receive only operation. When the ETXMD bit is 1 on slave mode, the communication is only received not transmit (see section 34.3.6. Data Transfer Modes). When the ETXMD is 1, transmit data empty interrupt can not be used.

The communication state by each mode (master mode, slave mode) is shown as below. It is controlled by the ETXMD bit, the SPCR.MSTR bit and the TXMD bit.

Table 34.5 RSPI communication state (master/slave mode)

SPCR.MSTR bit	SPCR3.ETXMD bit	SPCR.TXMD bit	Communication state
1	0	0	Transmit-receive master mode
1	0	1	Transmit master mode
0	0	0	Transmit-receive slave mode (default)
0	0	1	Transmit slave mode
0	1	—	Receive slave mode

当字节交换有效时，将奇偶校验功能设置为无效（SPCR2.SPPE=0）。当奇偶校验函数设置为有效时，行为不被保证。

SINV位（串行数据反转位）

该位用于反转发送数据和接收数据。

当SINV位设置为1时，发送缓冲器(SPTX)数据反转以反转发送数据和接收数据，然后将反转的数据存储在接收缓冲器(SPRX)中。奇偶校验位是对应于反转的发送接收数据的值。

34.2.16 SPCR3：SPI控制寄存器3

Base address: SPIn = 0x4011_A000 + 0x0100 × n (n = 0, 1)

Offset address: 0x21

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CENDIE	—	—	BFDS	ETXMD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ETXMD	扩展通信模式选择 0：全双工同步或仅传输串行通信。[启用SPCR.TXMD位] 1：从机模式下仅接收串行通信（SPCR.MSTR位=0）。[SPCR.TXMD位禁用]主机模式下禁止设置（SPCR.MSTR位=1）。	R/W
1	BFDS	突发传输帧之间延迟选择 0：在突发传输中插入帧之间的延迟（RSPCK延迟、SSL否定延迟和下一次访问延迟）。 1：突发传输中不插入帧间延迟。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	CENDIE	RSPI通信结束中断使能 0：禁止通讯结束中断请求。1：使能通信结束中断请求。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

SPI控制寄存器3(SPCR3)是操作模式的控制寄存器。如果在SPCR.SPE位为1时更改ETXMD和BFDS的值，则SPI操作不保证。

ETXMD位（扩展通信模式选择）

该位仅在从模式下有效（SPCR.MSTR位为0）。该位选择只接收操作。当ETXMD位在从机模式下为1时，通信只接收不发送（参见第34.3.6节。数据传输模式）。当ETXMD为1时，不能使用发送数据空中断。

各模式（主模式、从模式）的通信状态如下所示。它由ETXMD位、SPCR.MSTR位和TXMD位控制。

Table 34.5 RSPI通信状态（主从模式）

SPCR.MSTR bit	SPCR3.ETXMD bit	SPCR.TXMD bit	通讯状态
1	0	0	收发主模式
1	0	1	传输主模式
0	0	0	发送接收从模式（默认）
0	0	1	传输从模式
0	1	—	接收从机模式

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BFDS bit (Between Burst Transfer Frames Delay Select)

This bit controls whether insert the delay time between the burst transfer frames.

This bit is valid when the SPCMD.SSLKP bit is 1 in master mode (the SPCR.MSTR bit is 1).

This bit should be set to 0 in slave mode. The usage of SSL delay control between transfer frames is shown as below. See (4)Burst transfers in detail.

Table 34.6 Usage of SSL delay control between transfer frames (Master mode)

Transmit		SPCMD.SSLKP bit	SPCR3.BFDS bit	SSL delay control register*1 (RSPCK clock delay, SSL negation delay, next access delay)
Non-burst transmit		0	0	Any given value. You can control each delay value according to setting for RSPCK clock delay, SSL negation delay and next access delay.
Burst transmit with delay between frames	From the 1st frame to the last previous frame	1	0	
	The last frame	0	0	
Burst transmit with no delay between frames	From the 1st frame to the last previous frame	1	1	Any given value. But delay is inserted only below. ● RSPCK clock delay of the 1st frame ● SSL negation delay and next access delay of the last frame
	The last frame	0	1	

Note 1. Whether the setting value of following bits are valid or not depends on the setting value of the SPCMD.SPNDEN bit (see section 34.2.14. SPCMDm : SPI Command Register m (m = 0 to 7)).
The SPCKD.SCKDL[2:0] bits: RSPCK delay
The SSLND.SLNDL[2:0] bits: SSL negate delay
The SPND.SPNDL[2:0] bits: Next access delay

CENDIE bit (RSPI Communication End Interrupt Enable)

This bit controls generation of a communication end interrupt request.

34.3 Operation

In this section, the serial transfer period refers to the period from the beginning of driving valid data to the fetching of the final valid data.

34.3.1 Overview of SPI Operation

The SPI is capable of synchronous serial transfers in the following modes:

- Slave mode (SPI operation)
- Single master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation)

The SPI mode can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 34.7 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 34.7 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1

BFDS位（突发传输帧之间延迟选择）

该位控制是否在突发传输帧之间插入延迟时间。

当SPCMD.SSLKP位在主机模式下为1（SPCR.MSTR位为1）时，该位有效。

在从机模式下，该位应设置为0。传输帧之间的SSL延迟控制的使用如下所示。详见(4)突发传输。

Table 34.6 传输帧之间使用SSL延迟控制（主模式）

Transmit		SPCMD.SSLKP bit	SPCR3.BFDS bit	SSL延迟控制寄存器*1 （RSPCK时钟延迟、SSL否定延迟、下一次访问延迟）
Non-burst transmit		0	0	任何给定的值。您可以根据对RSPCK时钟延迟、SSL否定延迟和下一次访问延迟的设置来控制每个延迟值。
帧之间有延迟的突发传输	从第一帧到最后一帧	1	0	
	最后一帧	0	0	
帧间无延迟的突发传输	从第一帧到最后一帧	1	1	任何给定的值。但是延迟只在下面插入。● 第一帧的RSPCK时钟延迟 ● 最后一帧的SSL否定延迟和下一次访问延迟
	最后一帧	0	1	

注1.以下位的设置值是否有效取决于SPCMD.SPNDEN位的设置值（参见第34.2.14节。SPCMDm：SPI命令寄存器m（m=0至7））。SPCKD.SCDL[2:0]位：RSPCK延迟

SSLND.SLNDL[2:0]位：SSL否定延迟SPND.SPNDL[2:0]位：下一次访问延迟

CENDIE位（RSPI通信结束中断使能）

该位控制通信结束中断请求的产生。

34.3 Operation

在本节中，串行传输周期是指从开始驱动有效数据到获取最终有效数据的周期。

34.3.1 SPI操作概述

SPI能够在以下模式下进行同步串行传输：

●从机模式（SPI操作）

●单主模式（SPI操作）

- Multi-master mode (SPI operation)

●从机模式（时钟同步操作）

●主模式（时钟同步操作）

可以使用SPCR中的MSTR、MODFEN和SPMS位选择SPI模式。表34.7列出了SPI模式和SPCR设置之间的关系，以及每种模式的说明。

Table 34.7 SPCR设置和SPI模式之间的关系(1of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
MSTR位设置	0	1	1	0	1
MODFEN位设置	0 or 1	0	1	0	0
SPMS位设置	0	0	0	1	1

Table 34.7 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 pins	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	—	—
Max transfer rate	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0, 1)	Possible (CPHA = 0, 1)	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer trigger	SSL input active or RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported*5				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2*4	Supported*2*4	Supported*2	Supported*2
Parity error detection	Supported*3*2				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported
Underrun error detection	Supported*5	Not supported	Not supported	Supported*5	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, detection of receiver buffer full, overrun error, and parity error are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.
Note 5. When SPI is receive only slave mode, none of transmit buffer empty and underrun error is detected.

34.3.2 Controlling the SPI Pins

Based on the settings of the MSTR, MODFEN, and SPMS bits in SPCR and the PmnPFS.NCODR bit for I/O Ports, the SPI can switch pin states. Table 34.8 lists the relationship between pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects the CMOS output. Setting it to 1 selects the open-drain output. The I/O port settings must follow this relationship.

Table 34.7 SPCR设置和SPI模式之间的关系(2of2)

Mode	Slave (SPI operation)	Single-master (SPI operation)	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
RSPCKn pins	Input	Output	Output/Hi-Z	Input	Output
MOSIn pin	Input	Output	Output/Hi-Z	Input	Output
MISOn pin	Output/Hi-Z	Input	Input	Output	Input
SSLn0 pins	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1到SSLn3引脚	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL极性改变功能	Supported	Supported	Supported	—	—
最大传输率	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
时钟源	RSPCK input	片上波特率发生器	片上波特率发生器	RSPCK input	片上波特率发生器
时钟极性	Two				
时钟相位	Two	Two	Two	One (CPHA = 1)	Two
第一个传输位	MSB/LSB				
传输数据长度	8至16、20、24、32位				
突发传输	Possible (CPHA = 1)	Possible (CPHA = 0, 1)	Possible (CPHA = 0, 1)	—	—
RSPCK延迟控制	不支持	Supported	Supported	不支持	Supported
SSL否定延迟控制	不支持	Supported	Supported	不支持	Supported
下一次访问延迟控制	不支持	Supported	Supported	不支持	Supported
转移触发	SSL输入有效或RSPCK振荡	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	RSPCK oscillation	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)
顺序控制	不支持	Supported	Supported	不支持	Supported
发送缓冲区空检测	Supported*5				
接收缓冲区满检测	Supported*2				
溢出错误检测	Supported*2	Supported*2*4	Supported*2*4	Supported*2	Supported*2
奇偶校验错误检测	Supported*3*2				
模式故障错误检测	Supported (MODFEN = 1)	不支持	Supported	不支持	不支持
欠载错误检测	Supported*5	不支持	不支持	Supported*5	不支持

注1.此模式不支持此功能。
注2.当SPCR.TXMD位为1时，不执行接收缓冲区满、溢出错误和奇偶校验错误的检测。
注3.当SPCR2.SPPE位为0时，不执行奇偶校验错误检测。
注4.当SPCR2.SCKASE位为1时，不进行溢出错误检测。
注5.当SPI为仅接收从机模式时，不会检测到发送缓冲区为空和欠载错误。

34.3.2 控制SPI引脚

根据SPCR中的MSTR、MODFEN和SPMS位以及IO端口的PmnPFS.NCODR位的设置，SPI可以切换引脚状态。表34.8列出了引脚状态和位设置之间的关系。将IO端口的PmnPFS.NCODR位设置为0可选择CMOS输出。将其设置为1选择开漏输出。IO端口设置必须遵循这种关系。

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Table 34.8 Relationship between pin states and bit settings

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SSLP.SSL0P bit.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z. Whether or not the input signal is at the active level determines the setting of the SSLP.SSL0P bit.
Note 5. These pins are available for use as I/O port pins.

The SPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) based on the MOIFE and MOIFV bit settings in SPPCR, as listed in Table 34.9.

Table 34.9 MOSI signal value determination during SSL negation

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

Table 34.8 引脚状态和位设置之间的关系

Mode	Pin	引脚状态*2	
		IO端口的PmnPFS.NCODR位=0	IO端口的PmnPFS.NCODR位=1
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
从机模式（SPI操作）（MSTR=0，SPMS=0）	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
主模式（时钟同步操作）（MSTR=1，MODFEN=0，SPMS=1）	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
从机模式（时钟同步操作）（MSTR=0，SPMS=1）	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

注1.此模式不支持此功能。
注2.SPI设置不反映在未选择SPI功能的复用引脚中。
注3.当SSLn0处于有效电平时，引脚状态为Hi-Z。输入信号是否处于活动电平决定SSLP.SSL0P位的设置。

注4.当SSLn0处于无效电平或SPCR.SPE位为0时，引脚状态为Hi-Z。输入信号是否处于活动电平决定SSLP.SSL0P位的设置。

注5.这些引脚可用作IO端口引脚。

单主机模式（SPI操作）或多主机模式（SPI操作）下的SPI根据中的MOIFE和MOIFV位设置确定SSL否定期间（包括突发传输期间的SSL保留期间）的MOSI信号值SPPCR，如表34.9中所列。

Table 34.9 SSL否定期间的MOSI信号值确定

MOIFE bit	MOIFV bit	SSL否定期间的MOSIn信号值
0	0, 1	上次传输的最终数据
1	0	Low
1	1	High

34.3.3 SPI System Configuration Examples

34.3.3.1 Single-master/single-slave with the MCU as a master

Figure 34.5 shows a single-master/single-slave SPI system configuration example where the MCU is used as a master. In the single-master/single-slave configuration, the SSLni outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is maintained in the selected state.*1

Note 1. In the transfer format configured when the SPCMDm.CPHA bit is 0, the SSL signal for some slave devices cannot be fixed to an active level. In this case, always connect the SSLni output of the MCU to the SSL input of the slave device.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

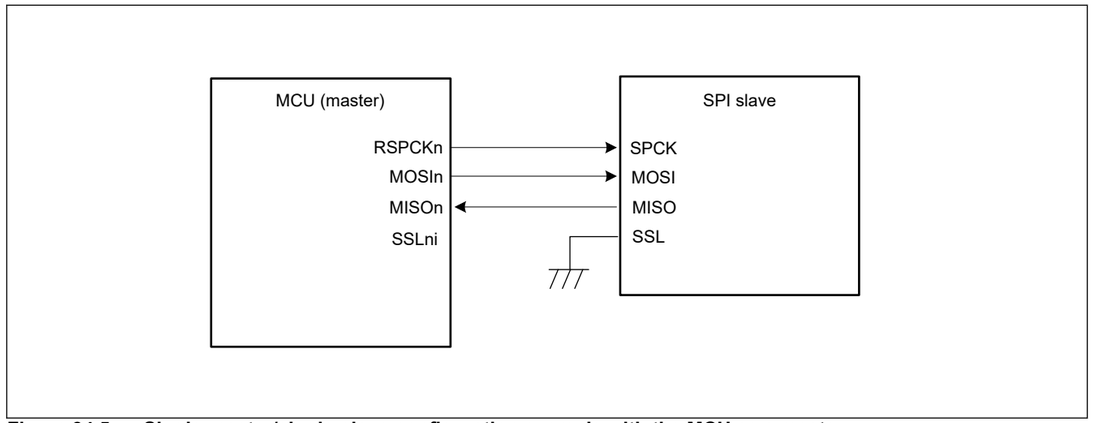

Figure 34.5 Single-master/single-slave configuration example with the MCU as a master

34.3.3.2 Single-master/single-slave with the MCU as a slave

Figure 34.6 shows a single-master/single-slave SPI system configuration example where the MCU is used as a slave. When the MCU operates as a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

Note 1. When SSLn0 is at a non-active level, the pin state is Hi-Z.

In the single-slave configuration when the SPCMDm.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level and the MCU (slave) is maintained in the selected state. This enables serial transfer execution (Figure 34.7). However, the communication end interrupt does not output when SSL0 input is fixed as Figure 34.7.

34.3.3 SPI系统配置示例

34.3.3.1 单主单从单片机为主

图34.5显示了单主单从SPI系统配置示例，其中MCU用作主机。在单主单从配置中，不使用MCU（主）的SSLni输出。SPI从机的SSL输入固定为低电平，SPI从机保持在选中状态。*1

注1.在SPCMDm.CPHA位为0时配置的传输格式中，某些从设备的SSL信号不能固定为有效电平。在这种情况下，请始终将MCU的SSLni输出连接到从设备的SSL输入。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

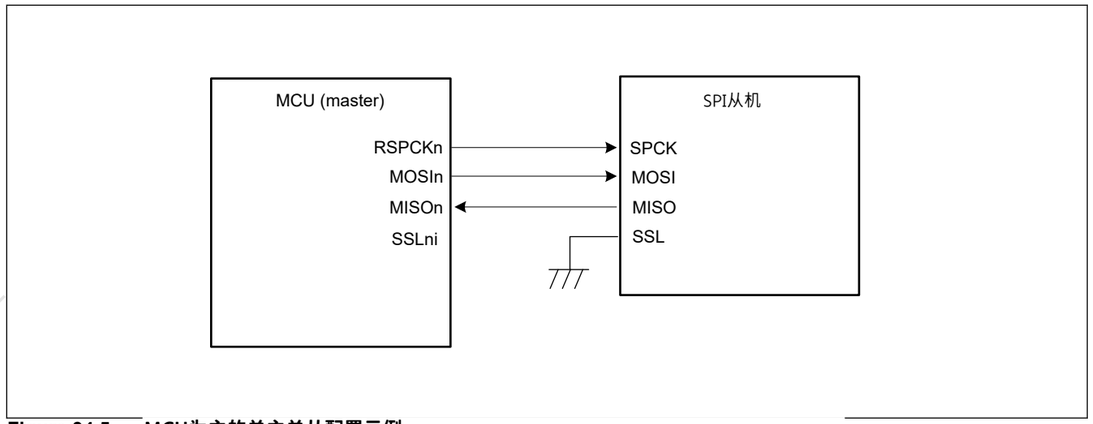

Figure 34.5 MCU为主的单主单从配置示例

34.3.3.2 单主单从单片机作为从机

图34.6显示了单主单从SPI系统配置示例，其中MCU用作从机。当MCU作为从机运行时，SSLn0引脚用作SSL输入。SPI主机驱动RSPCK和MOSI信号。MCU（从机）驱动MIOn信号。*1

注1.当SSLn0处于非活动电平时，引脚状态为Hi-Z。

在单从机配置中，当SPCMDm.CPHA位设置为1时，MCU（从机）的SSLn0输入固定为低电平，MCU（从机）保持在选择状态。这将启用串行传输执行（图34.7）。但是，如图34.7那样固定SSL0输入时，不输出通信结束中断。

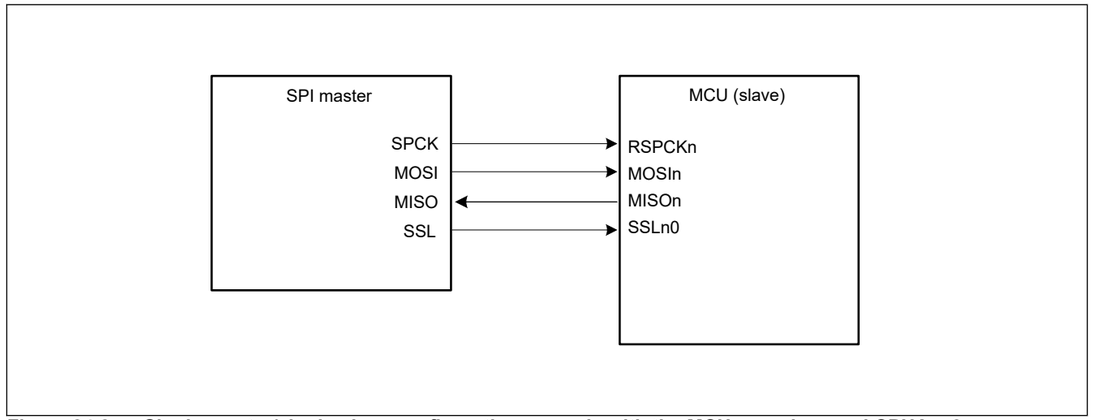

Figure 34.6 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 0

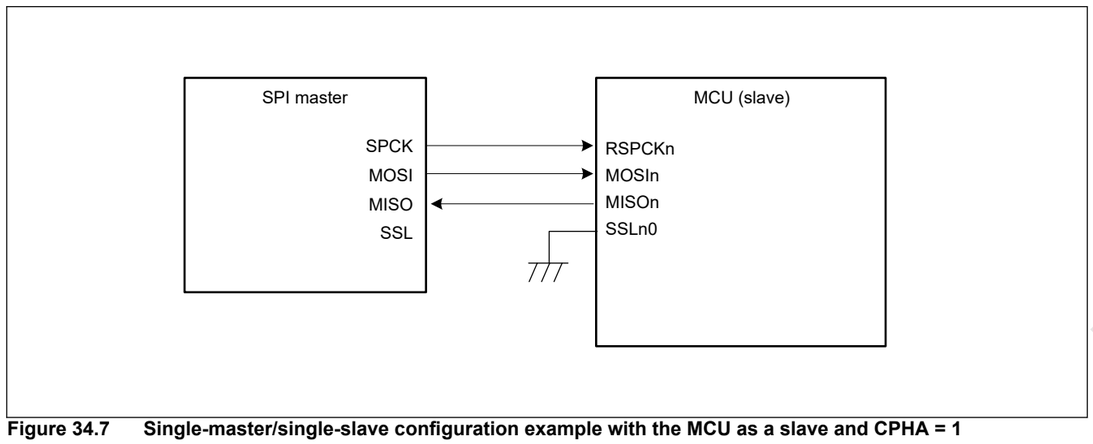

Figure 34.7 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 1

34.3.3.3 Single-master/multi-slave with the MCU as a master

Figure 34.8 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slaves 0 to 3. The MISO outputs of SPI slaves 0 to 3 are all connected to the MISOn input of the MCU (master). The SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slaves 0 to 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn, and SSLn0 to SSLn3 signals. Of the SPI slaves 0 to 3, the slave that receives low-level input into the SSL input drives the MISO signal.

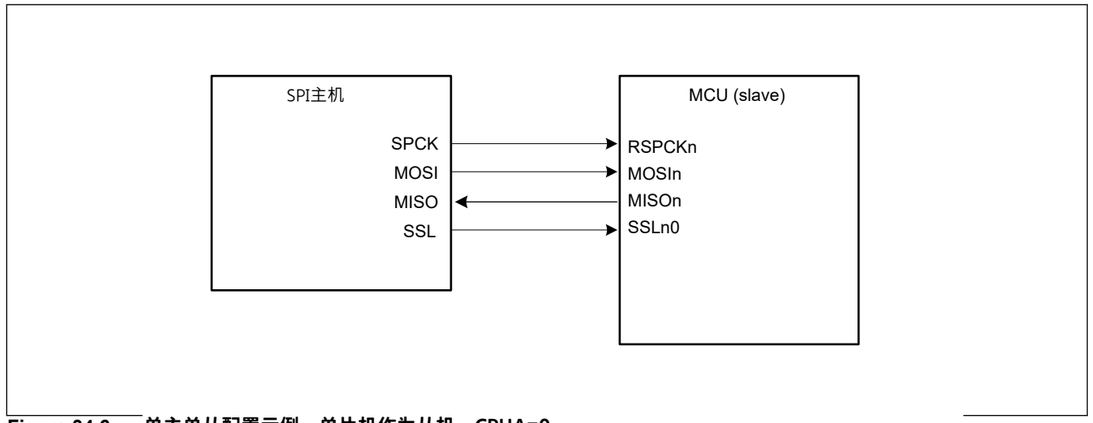

Figure 34.6 单主单从配置示例，单片机作为从机，CPHA=0

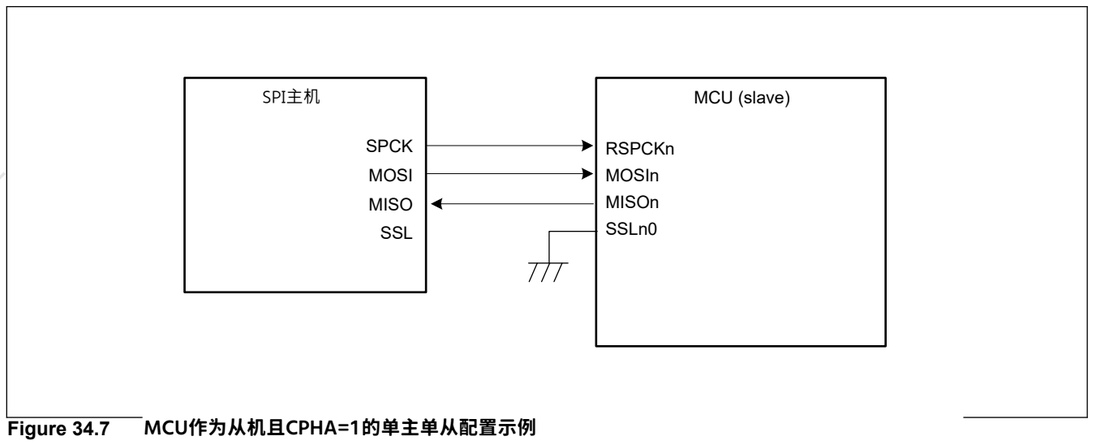

Figure 34.7 MCU作为从机且CPHA=1的单主单从配置示例

34.3.3.3 单主多从，单片机为主

图34.8显示了单主多从SPI系统配置示例，其中MCU用作主控。在本例中，SPI系统包括MCU（主机）和四个从机（SPI从机0到SPI从机3）。

MCU（主机）的RSPCKn和MOSIn输出连接到SPI从机0到3的RSPCK和MOSI输入。
SPI从机0到3的MISO输出都连接到MCU（主机）的MISOn输入。MCU（主机）的SSLn0到SSLn3输出分别连接到SPI从机0到3的SSL输入。

MCU（主控）驱动RSPCKn、MOSIn和SSLn0到SSLn3信号。在SPI从机0到3中，接收到SSL输入的低电平输入的从机驱动MISO信号。

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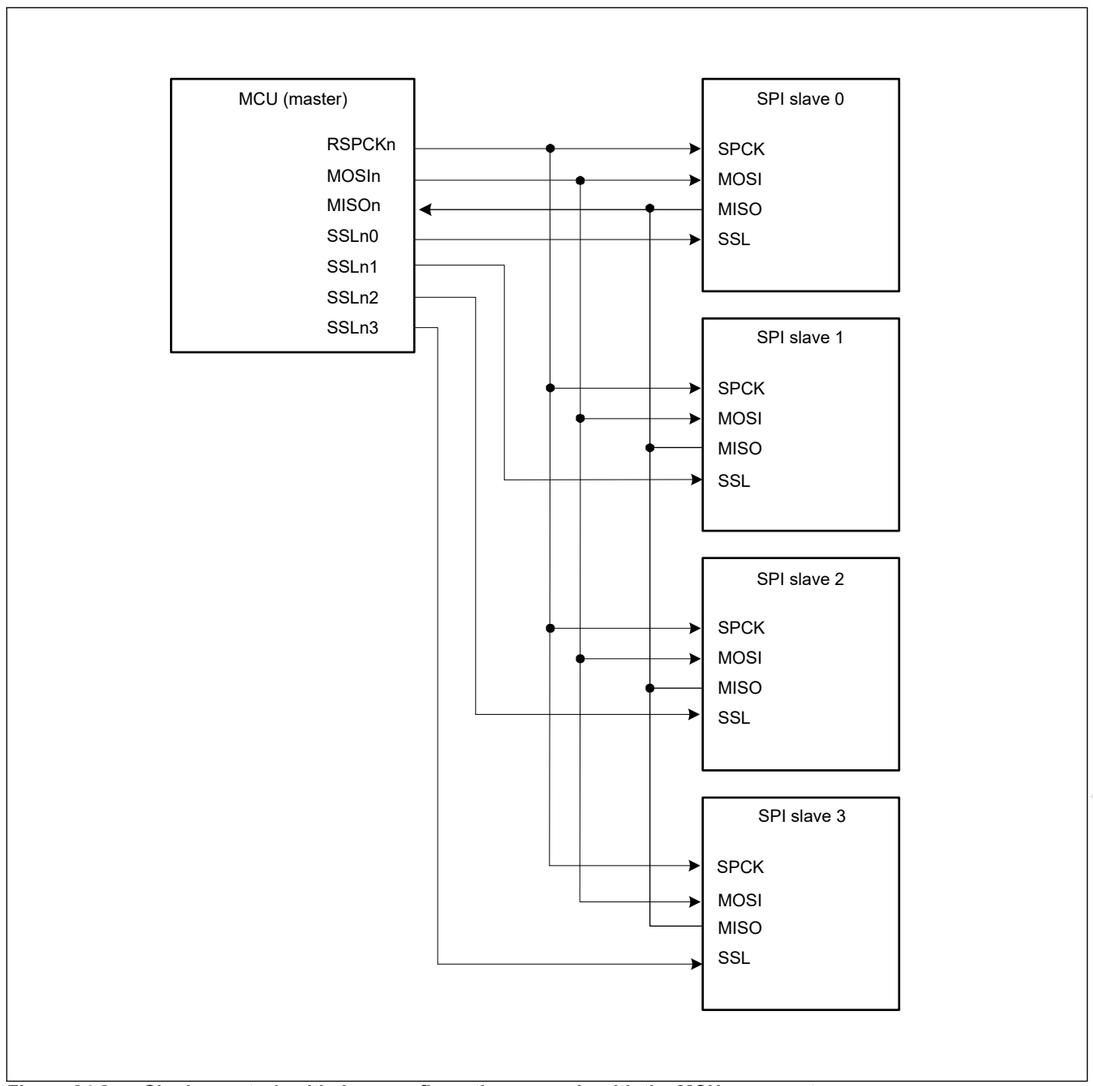

Figure 34.8 Single-master/multi-slave configuration example with the MCU as a master

34.3.3.4 Single-master/mult-slave with the MCU as a slave

Figure 34.9 shows a single-master/multi-slave SPI system configuration example where the MCU is used as a slave. In this example, the SPI system includes an SPI master and two MCUs (slaves X and Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slaves X and Y). The MISOn outputs of the MCUs (slaves X and Y) are all connected to the MISO input of the SPI master. The SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slaves X and Y, respectively).

The SPI master drives the SPCK, MOSI, SSLX, and SSLY signals. Of the MCUs (slaves X and Y), the slave that receives low-level input into the SSLn0 input drives the MISOn signal.

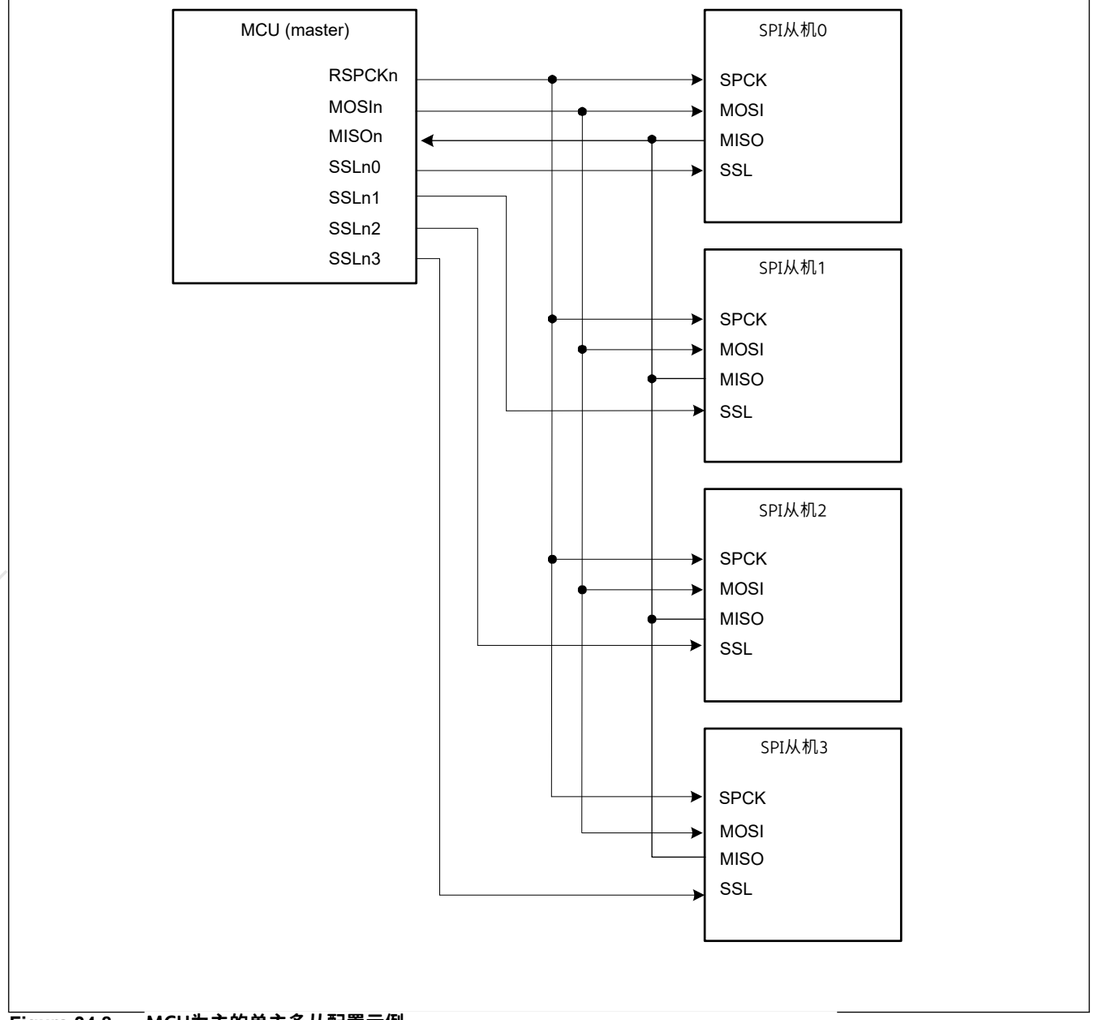

Figure 34.8 MCU为主的单主多从配置示例

34.3.3.4 单主多从，单片机作为从机

图34.9显示了单主多从SPI系统配置示例，其中MCU用作从设备。在本例中，SPI系统包括一个SPI主控和两个MCU（从属X和Y）。

SPI主机的SPCK和MOSI输出连接到MCU（从机X和Y）的RSPCKn和MOSIn输入。MCU（从机X和Y）的MISOn输出都连接到SPI主机的MISO输入。SPI主机的SSLX和SSLY输出连接到MCU的SSLn0输入（分别为从机X和Y）。

SPI主机驱动SPCK、MOSI、SSLX和SSLY信号。在MCU（从机X和Y）中，接收到SSLn0输入的低电平输入的从机驱动MISOn信号。

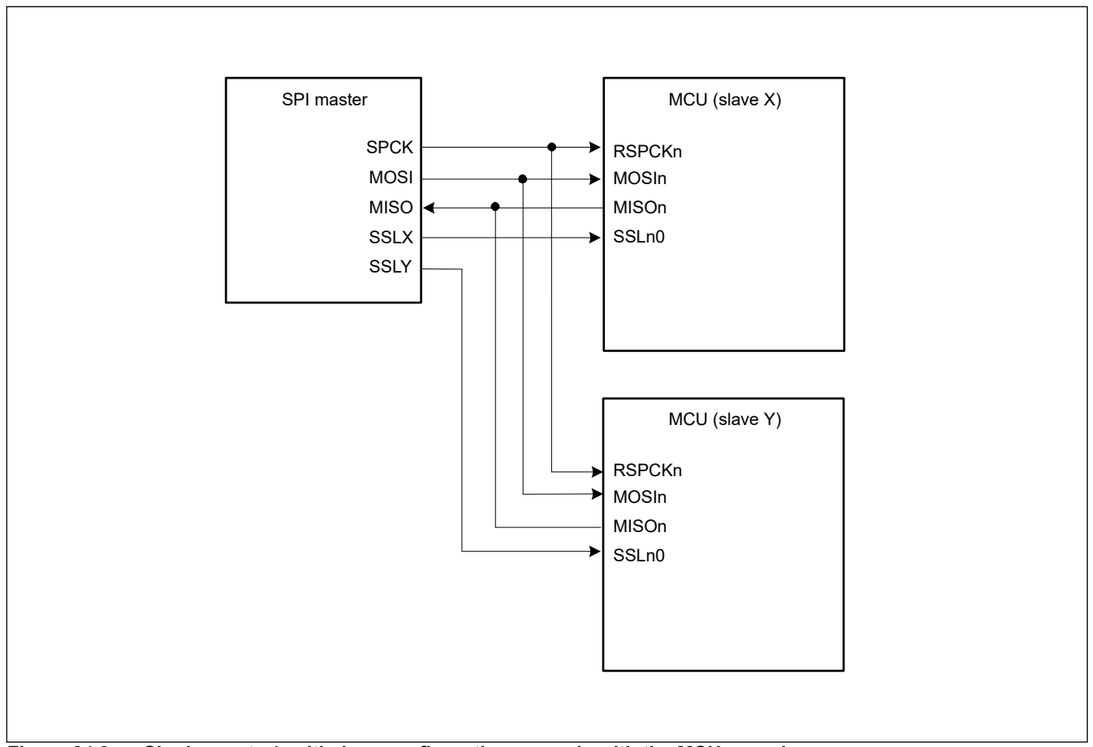

Figure 34.9 Single-master/multi-slave configuration example with the MCU as a slave

34.3.3.5 Multi-master/multi-slave with the MCU as a master

Figure 34.10 shows a multi-master/multi-slave SPI system configuration example where the MCU is used as a master. In this example, the SPI system includes two MCUs (masters X and Y) and two SPI slaves (SPI slaves 1 and 2).

The RSPCKn and MOSIn outputs of the MCUs (masters X and Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (masters X and Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (masters X and Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives the RSPCKn, MOSIn, SSLn1, and SSLn2 signals when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

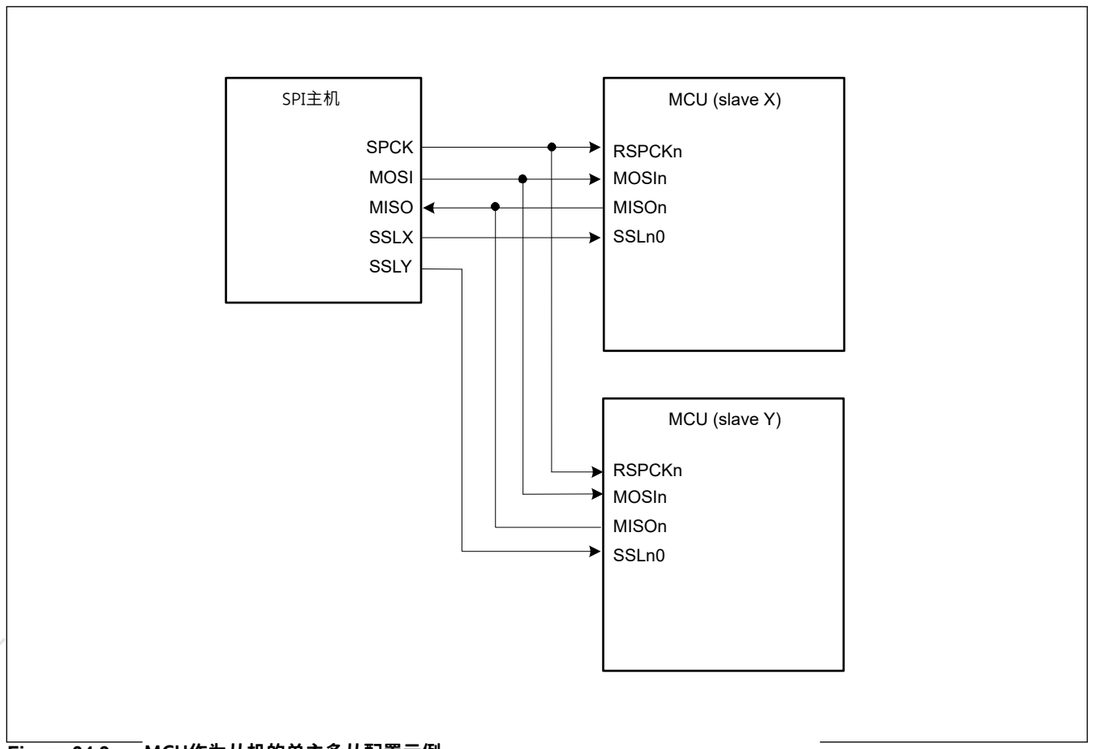

Figure 34.9 MCU作为从机的单主多从配置示例

34.3.3.5 以单片机为主的多主多从

图34.10显示了一个多主机多从机SPI系统配置示例，其中MCU用作主机。在此示例中，SPI系统包括两个MCU（主X和Y）和两个SPI从机（SPI从机1和2）。

MCU（主机X和Y）的RSPCKn和MOSIn输出连接到SPI从机1和2的RSPCK和MOSI输入。SPI从机1和2的MISO输出连接到MCU（主机X）的MISOn输入和Y)。来自MCU（主X）的任何通用端口Y输出都连接到MCU（主Y）的SSLn0输入。MCU（主设备Y）的任何通用端口X输出都连接到MCU（主设备X）的SSLn0输入。MCU（主机X和Y）的SSLn1和SSLn2输出连接到SPI从机1和2的SSL输入。在此配置示例中，因为系统可以仅由SSLn0输入和SSLn1和SSLn2输出组成从连接，不需要MCU的SSLn3输出。

当SSLn0输入电平为高电平时，MCU驱动RSPCKn、MOSIn、SSLn1和SSLn2信号。当SSLn0输入电平为低时，MCU检测到模式故障错误，将RSPCKn、MOSIn、SSLn1和SSLn2设置为Hi-Z，并将SPI总线直接释放到另一个主控。在SPI从机1和2中，接收到SSL输入的低电平输入的从机驱动MISO信号。

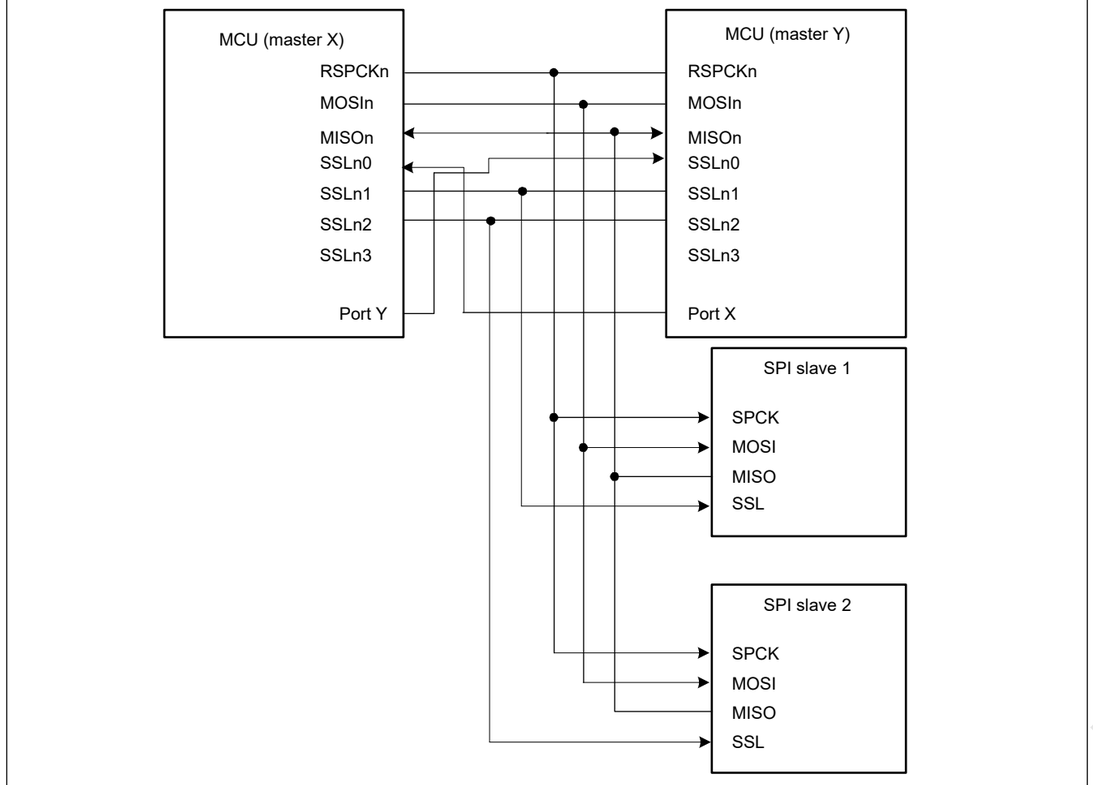

Figure 34.10 Multi-master/multi-slave configuration example with the MCU as a master

34.3.3.6 Master and slave in clock synchronous mode with the MCU configured as a master

Figure 34.11 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a master. In this configuration, SSLni of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

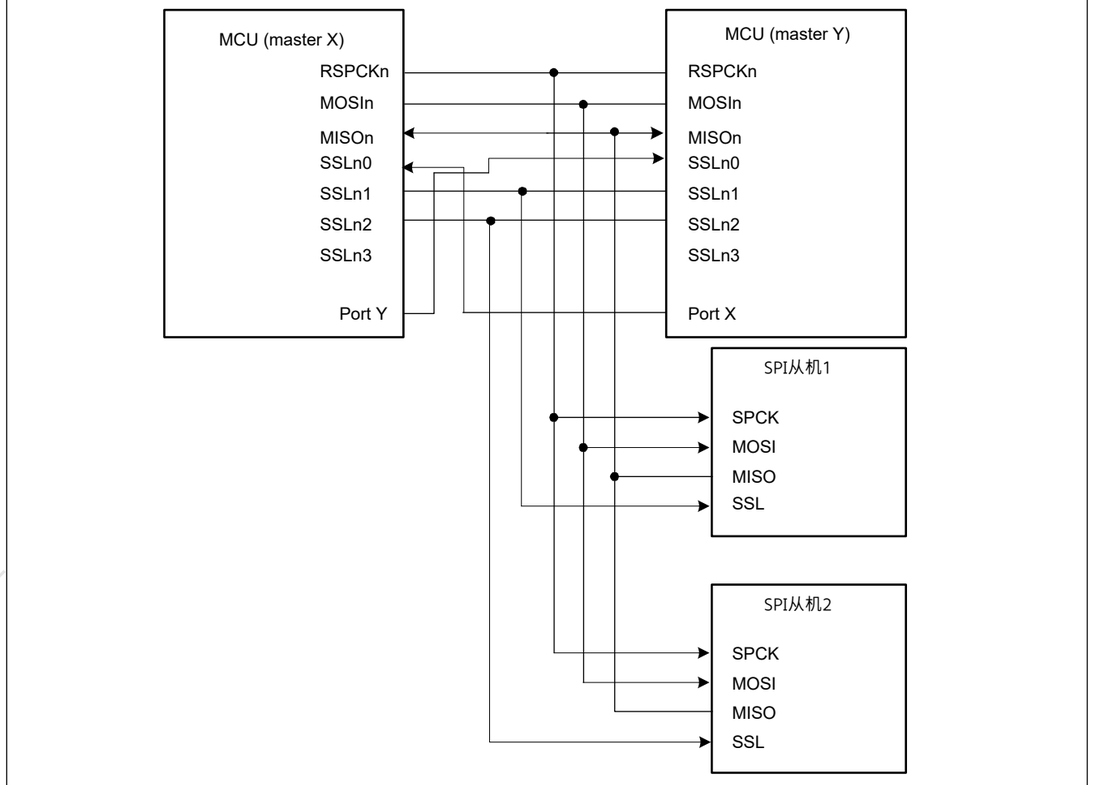

Figure 34.10 MCU为主的多主多从配置示例

34.3.3.6 主从时钟同步模式，MCU配置为主

图34.11显示了时钟同步模式下的主机和从机配置示例，其中MCU用作主机。在此配置中，不使用MCU（主）的SSLni。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

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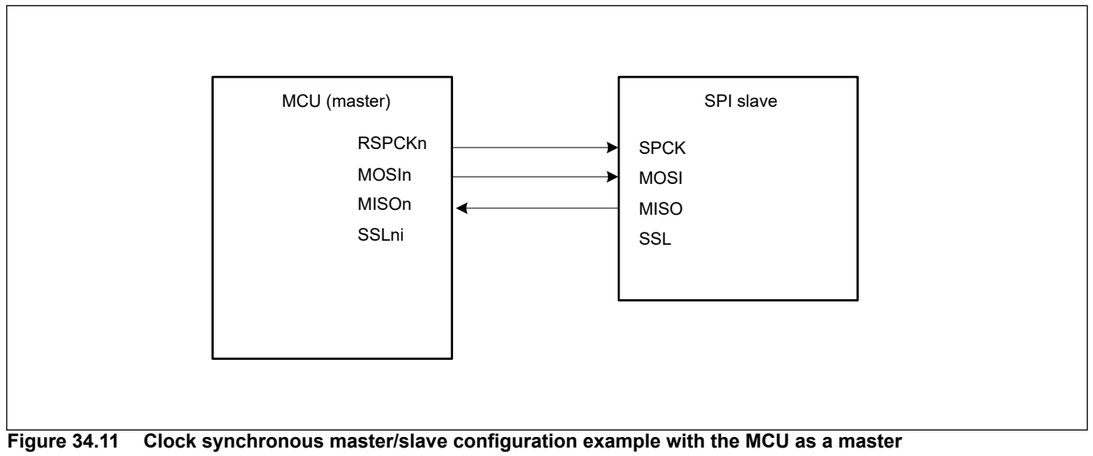


Figure 34.11 Clock synchronous master/slave configuration example with the MCU as a master

34.3.3.7 Master and slave in clock synchronous mode with the MCU as a slave

Figure 34.12 shows a master and slave in clock synchronous mode configuration example where the MCU is used as a slave. When the MCU operates as a slave (clock synchronous operation), the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. In addition, SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfers in the single-slave configuration when the SPCMDm.CPHA bit is set to 1.

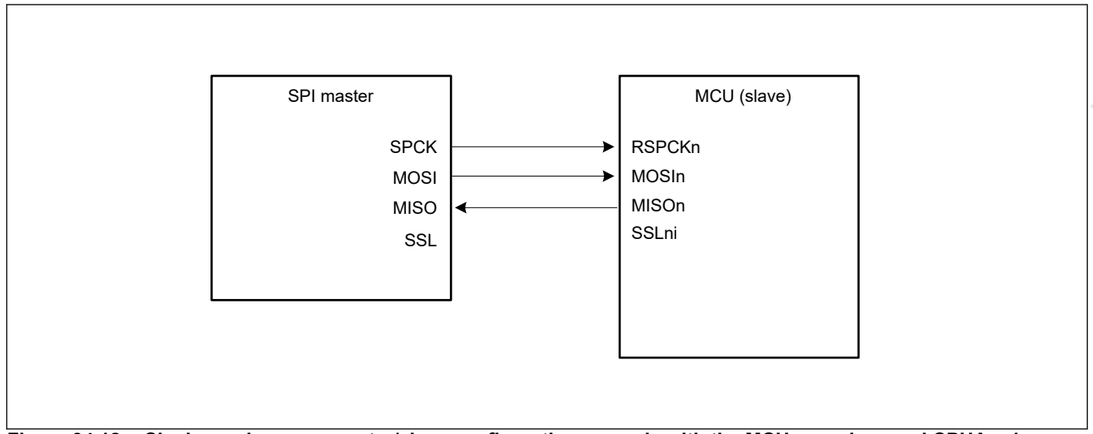


Figure 34.12 Clock synchronous master/slave configuration example with the MCU as a slave and CPHA = 1

34.3.4 Data Formats

The data format of the SPI depends on the settings in SPI Command Register m (SPCMDm) and the parity enable bit in SPI Control Register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit associated with the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[3:0]).

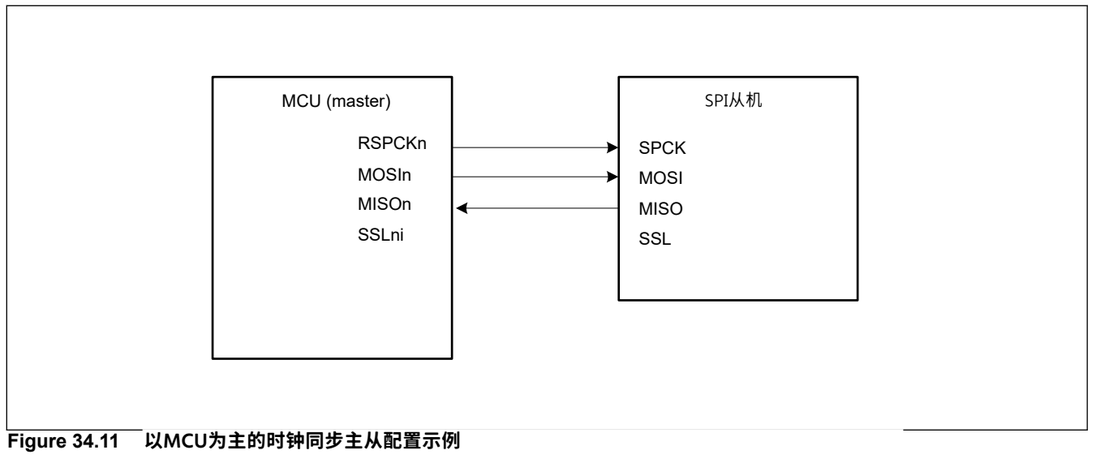


Figure 34.11 以MCU为主的时钟同步主从配置示例

34.3.3.7 主从时钟同步模式，单片机作为从机

图34.12显示了时钟同步模式下的主机和从机配置示例，其中MCU用作从机。当MCU作为从机运行时（时钟同步操作），MCU（从机）驱动MIOn信号，SPI主机驱动SPCK和MOSI信号。此外，不使用MCU（从机）的SSLn0到SSLn3。

当SPCMDm.CPHA位设置为1时，MCU（从机）只能在单从机配置中执行串行传输。

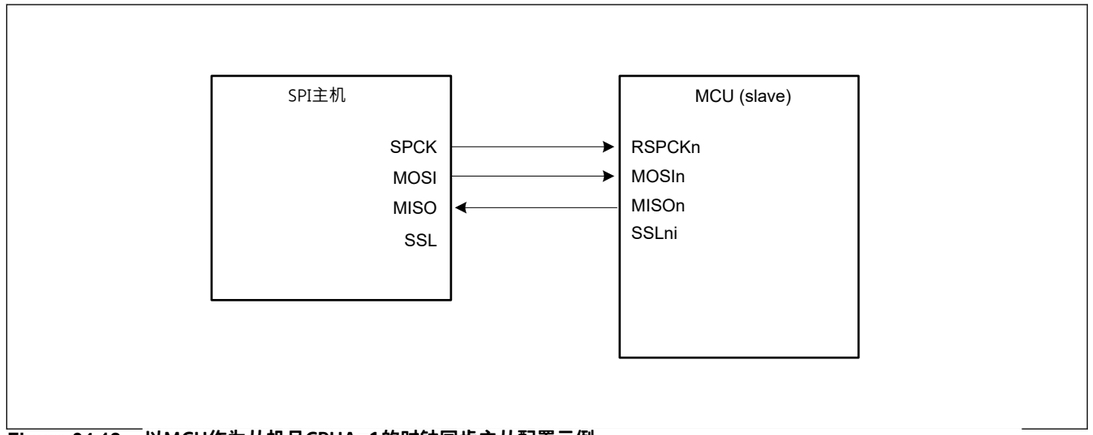


Figure 34.12 以MCU作为从机且CPHA=1的时钟同步主从配置示例

34.3.4 数据格式

SPI的数据格式取决于SPI命令寄存器m(SPCMDm)中的设置和SPI控制寄存器2(SPCR2.SPPE)中的奇偶校验使能位。无论MSB还是LSB在前，SPI都会将SPI数据寄存器(SPDRSPDR_HA)中的LSB位到与所选数据长度相关的位的范围视为传输数据。

本节显示传输前后一帧数据的格式。

禁用奇偶校验的数据格式

当奇偶校验被禁用时，数据的发送或接收将按照在SPI命令寄存器m(SPCMDm.SPB[3:0])的SPI数据长度设置中选择的位长度进行。

Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[3:0]). In this case, however, the last bit is a parity bit.

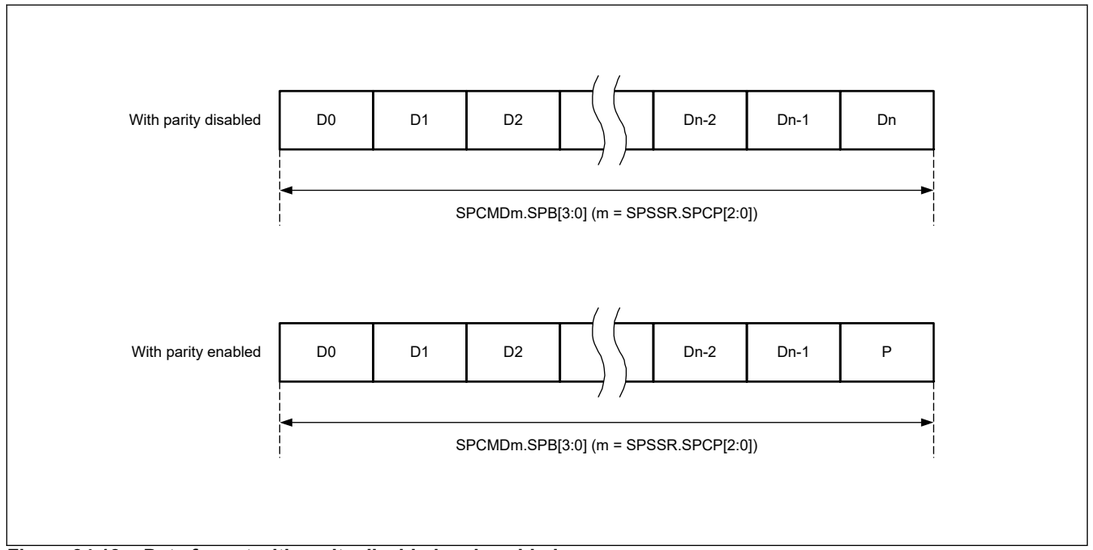


Figure 34.13 Data format with parity disabled and enabled

34.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no pre-processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 34.14 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, a SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

启用奇偶校验的数据格式

当奇偶校验使能时，数据的发送或接收按照在SPI命令寄存器m(SPCMDm.SPB[3:0])的SPI数据长度设置中选择的位长度进行。然而，在这种情况下，最后一位是奇偶校验位。

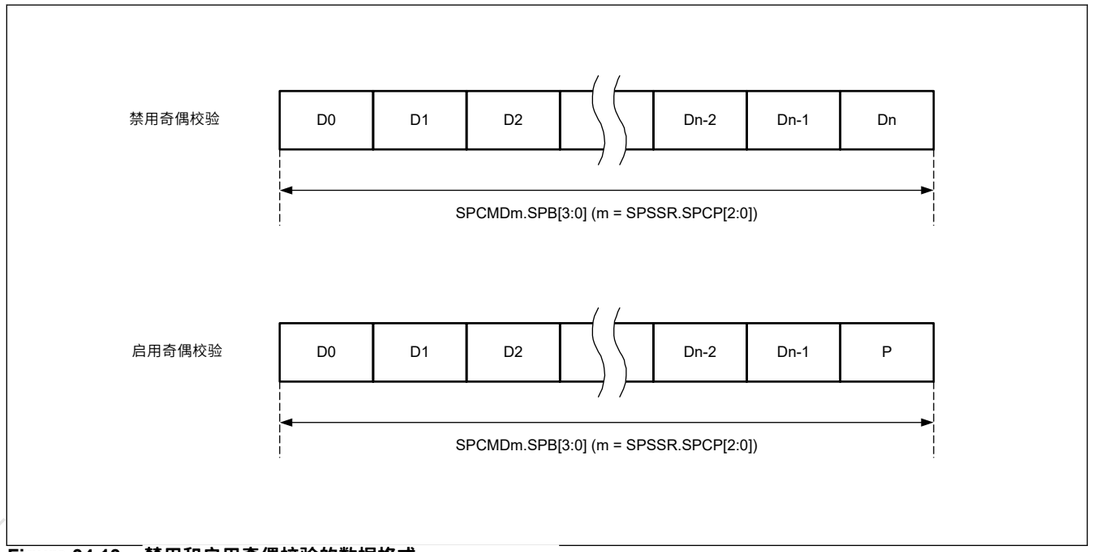


Figure 34.13 禁用和启用奇偶校验的数据格式

34.3.4.1 禁用奇偶校验时的操作(SPCR2.SPPE=0)

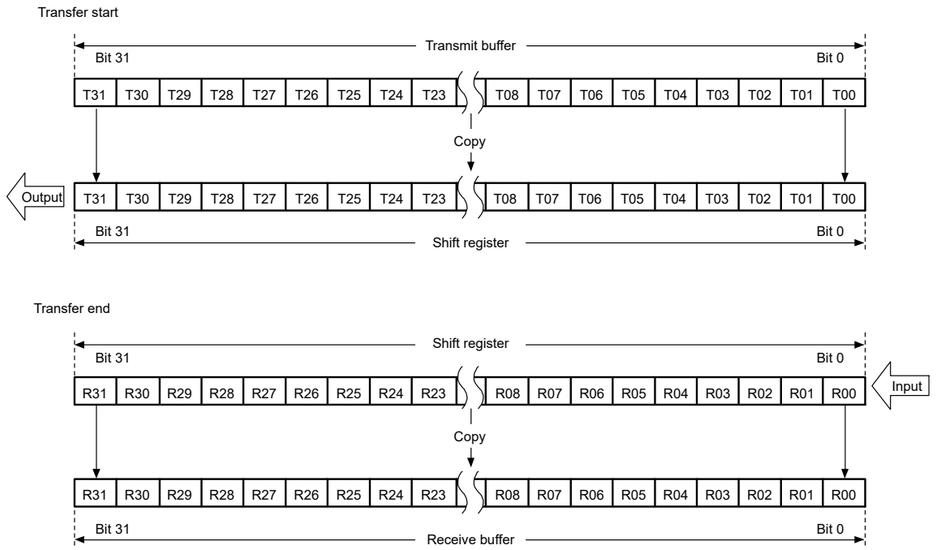
当奇偶校验被禁用时，用于传输的数据被复制到移位寄存器而不进行预处理。本节从MSB或LSB-firstorder和数据长度的组合来描述SPI数据寄存器(SPDRSPDR_HA)和移位寄存器之间的连接。

(1) 32位数据的MSB优先传输

图34.14显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，a SPI数据长度为32位，且MSB优先选择。

在发送过程中，发送缓冲器当前级的T31到T00位被复制到移位寄存器。发送数据从移位寄存器从T31移出到T30，并继续到T00。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需的RSPCK周期数后收集R31至R00位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

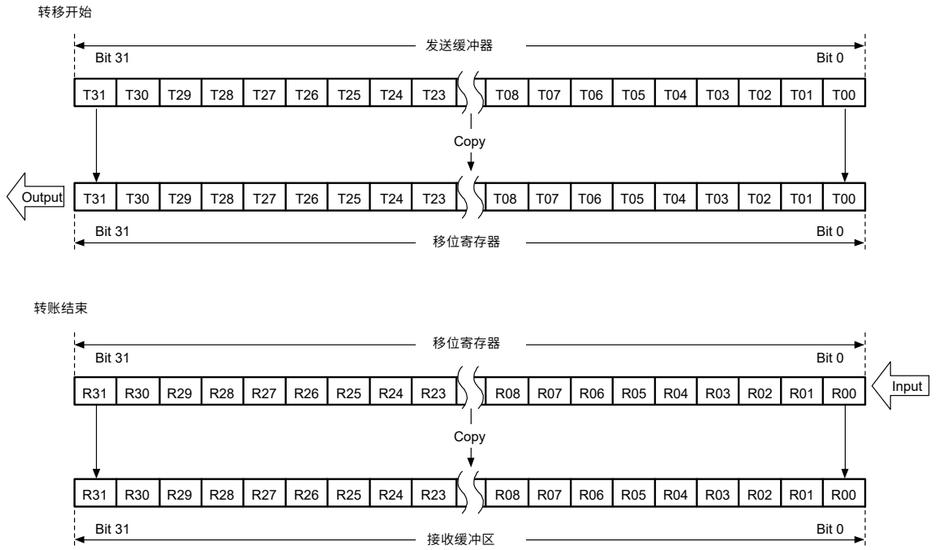
Figure 34.14 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 34.15 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 24 bits for an example that is not 32 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to bits T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

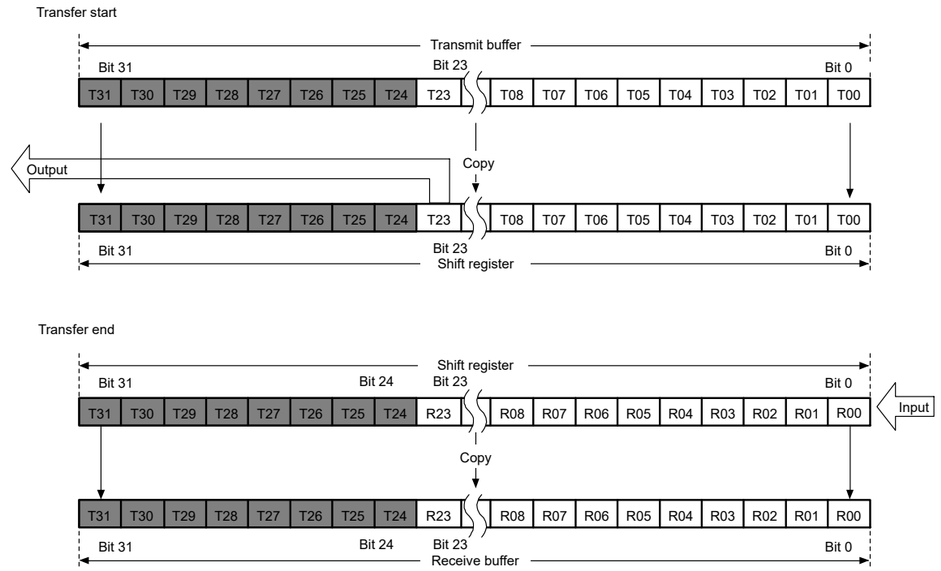
Figure 34.14 禁用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图34.15显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，
以24位SPI数据长度为例，即不是32位，并且选择MSB优先。

在发送过程中，来自发送缓冲器当前阶段的低24位（T23到T00）被复制到移位寄存器。
发送的数据从移位寄存器从T23移出到T22，并继续到T00。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后，当R23到R00位被收集时，移位寄存器中的值被复制到接收缓冲区。在发送-接收操作的情况下，发送缓冲区的高8位存储在接收缓冲区的高8位中。在传输过程中将0写入位T31到T24会导致将0插入接收缓冲区的高8位。另一方面，在只接收操作的情况下，接收缓冲区的高8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

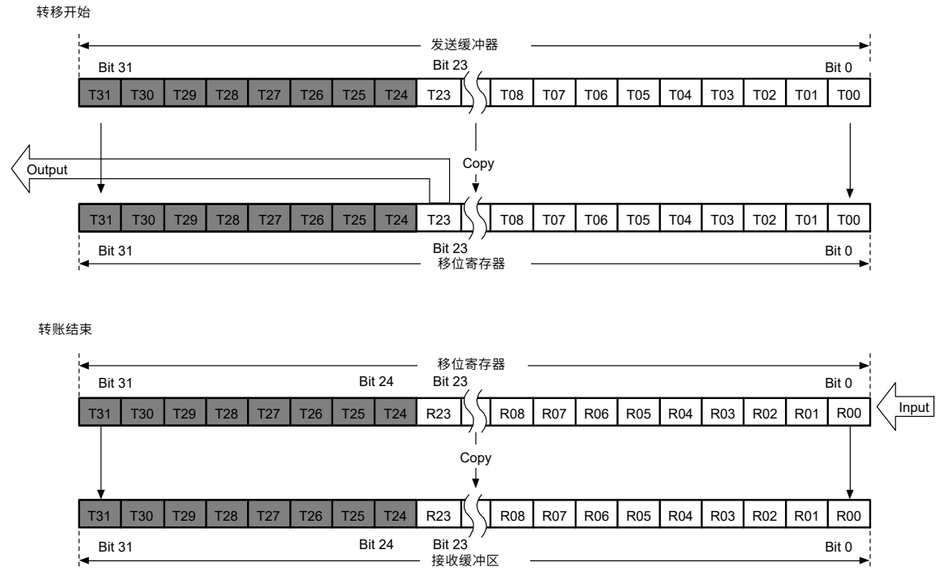
Figure 34.15 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 34.16 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register in order from T00 to T01, and continuing to T31.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to R31 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

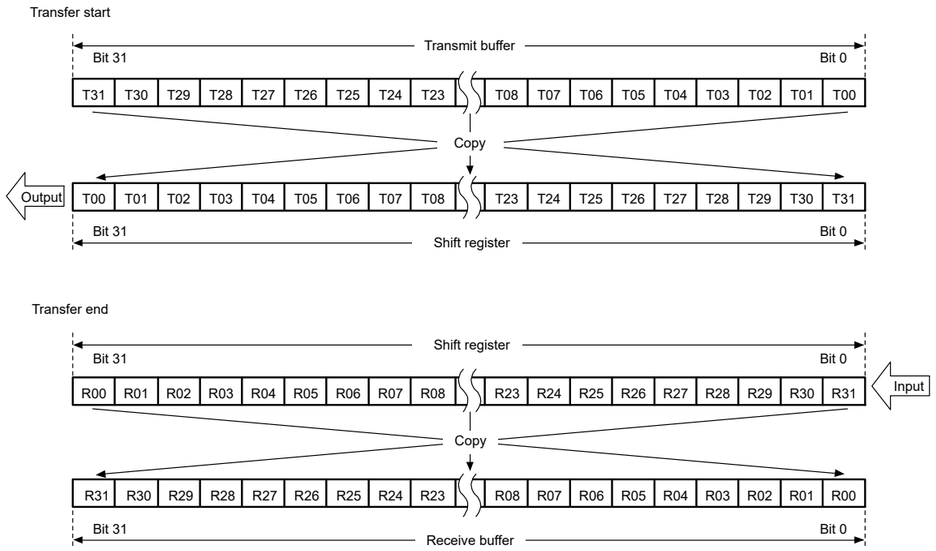
Figure 34.15 禁用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图34.16显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，
SPI数据长度为32位，并选择LSB-first。

在传输过程中，传输缓冲器当前级的位T31到T00被逐位重新排序，以获得用于复制到移位寄存器的顺序T00到T31。传输的数据从移位寄存器中按顺序从T00移出到T01，并继续到T31。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至R31位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 34.16 LSB-first transfer with 32-bit data and parity disabled

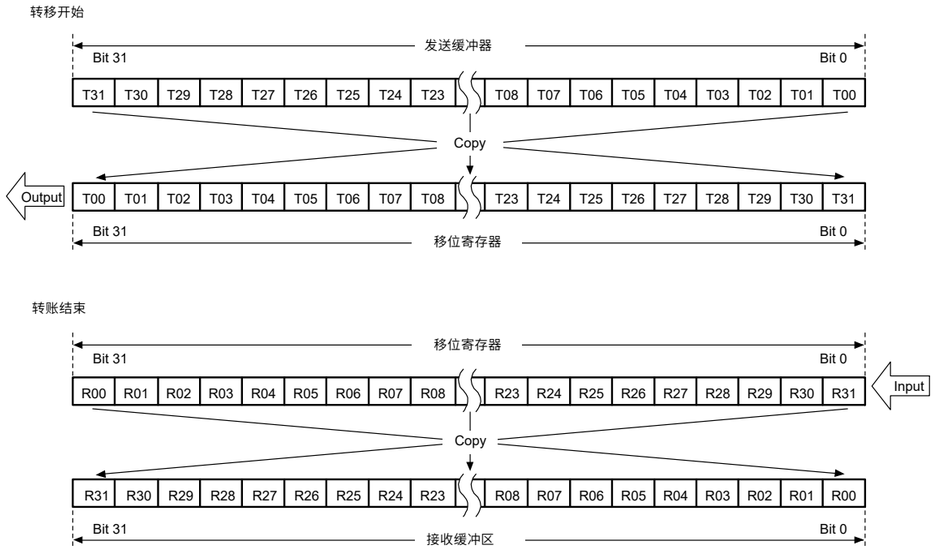
(4) LSB-first transfer with 24-bit data

Figure 34.17 shows the operation of the SPI Data Register (SPDR) and the shift register in transfers with parity disabled, an SPI data length of 24 bits for an example that is not 32, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 34.16 LSB优先传输，32位数据和奇偶校验禁用

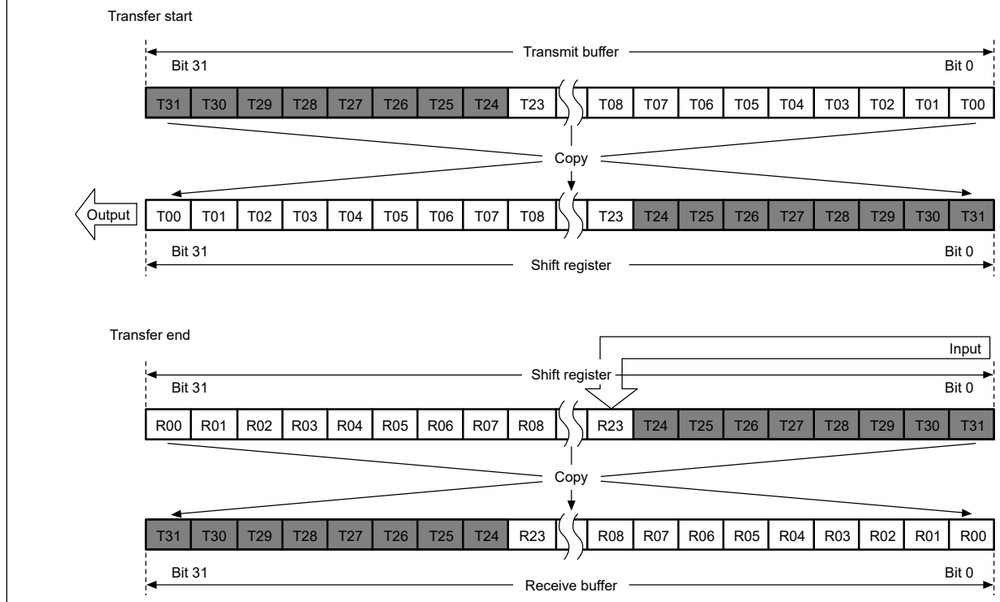
(4) 24位数据的LSB优先传输

图34.17显示了SPI数据寄存器(SPDR)和移位寄存器在奇偶校验禁用的传输中的操作，一个SPI数据长度为24位，例如不是32位，并且选择LSB优先。

发送时，将发送缓冲器当前级的低24位（T23到T00）逐位重新排序，得到T00到T23的顺序，用于复制到移位寄存器。发送的数据从移位寄存器从T00移出到T01，并继续到T23。

在接收中，接收到的数据通过移位寄存器的bit[8]逐位移位。在输入所需的RSPCK周期数后收集R00至R23位时，将移位寄存器中的值复制到接收缓冲区。

在发送-接收操作的情况下，发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送过程中将0写入T31到T24会导致将0插入接收缓冲区的高8位。另一方面，在只接收操作的情况下，接收缓冲区的高8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 34.17 LSB-first transfer with 24-bit data and parity disabled

34.3.4.2 Operation when parity is enabled (SPCR2.SPPE = 1)

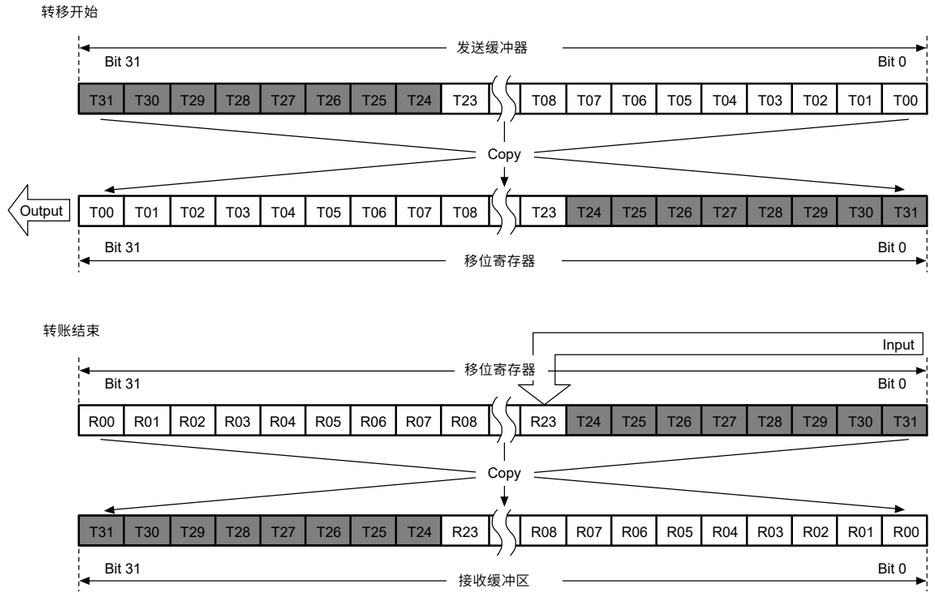
When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 34.18 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T31, T30, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R31 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R31 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 34.17 LSB优先传输，24位数据和奇偶校验禁用

34.3.4.2 启用奇偶校验时的操作(SPCR2.SPPE=1)

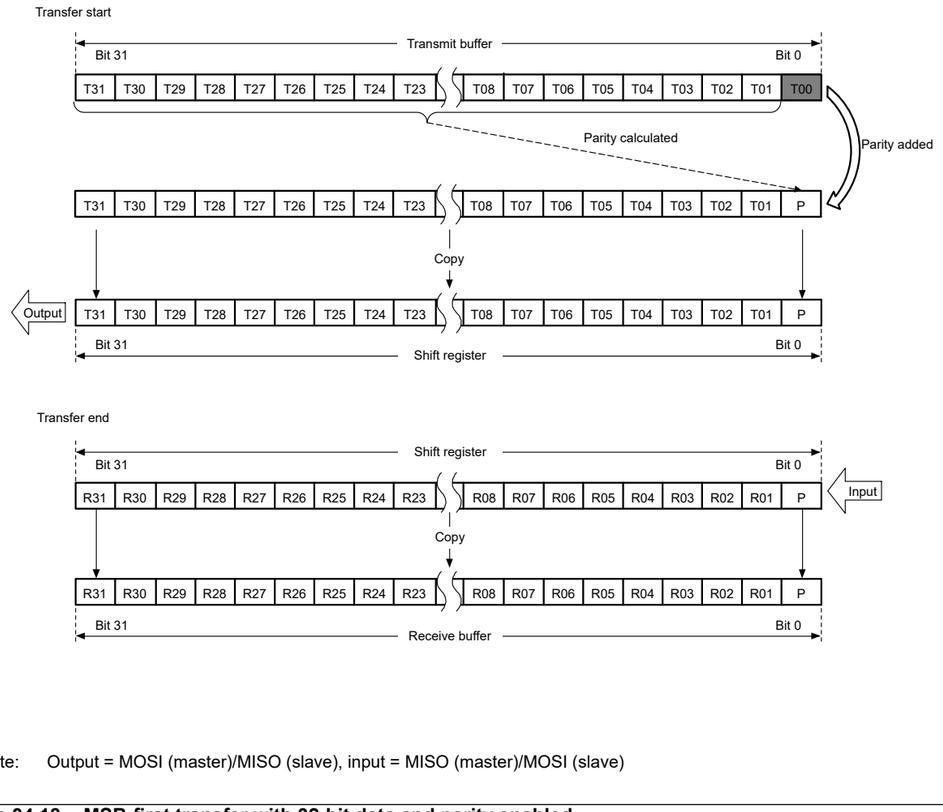
启用奇偶校验时，传输数据的最低位变为奇偶校验位。硬件计算奇偶校验位的值。

(1) 32位数据的MSB优先传输

图34.18显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，
SPI数据长度为32位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T31到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据按T31、T30、……、T01和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R31至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R31到P的数据的奇偶性。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

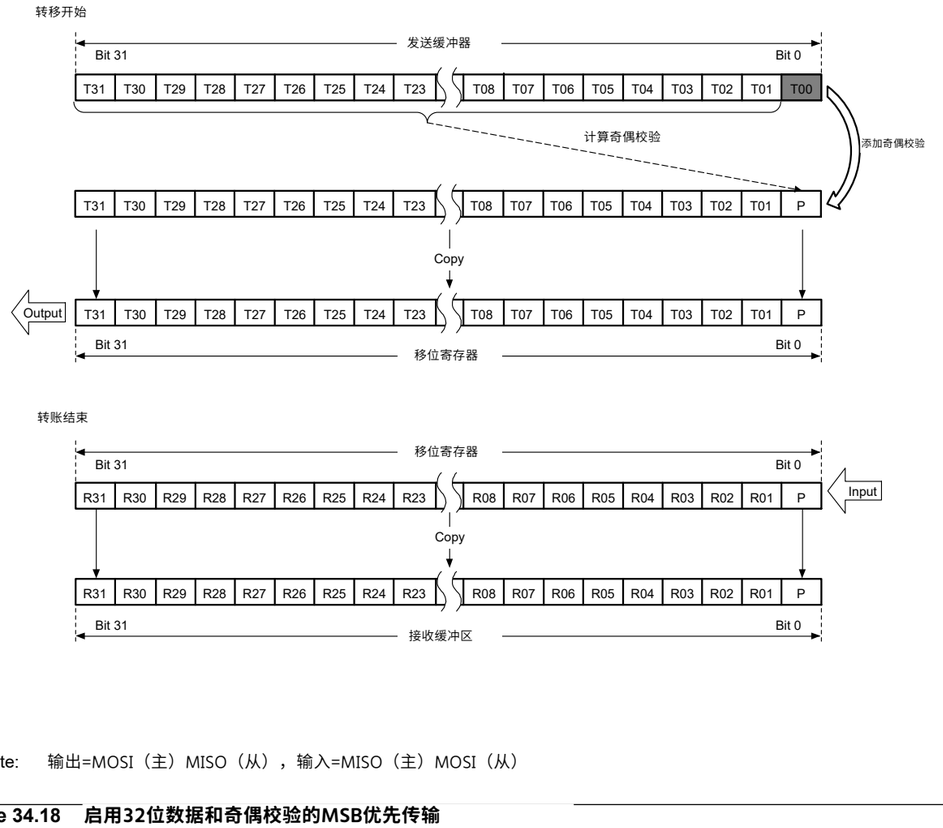
Figure 34.18 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 34.19 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole value is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R23 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer is stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

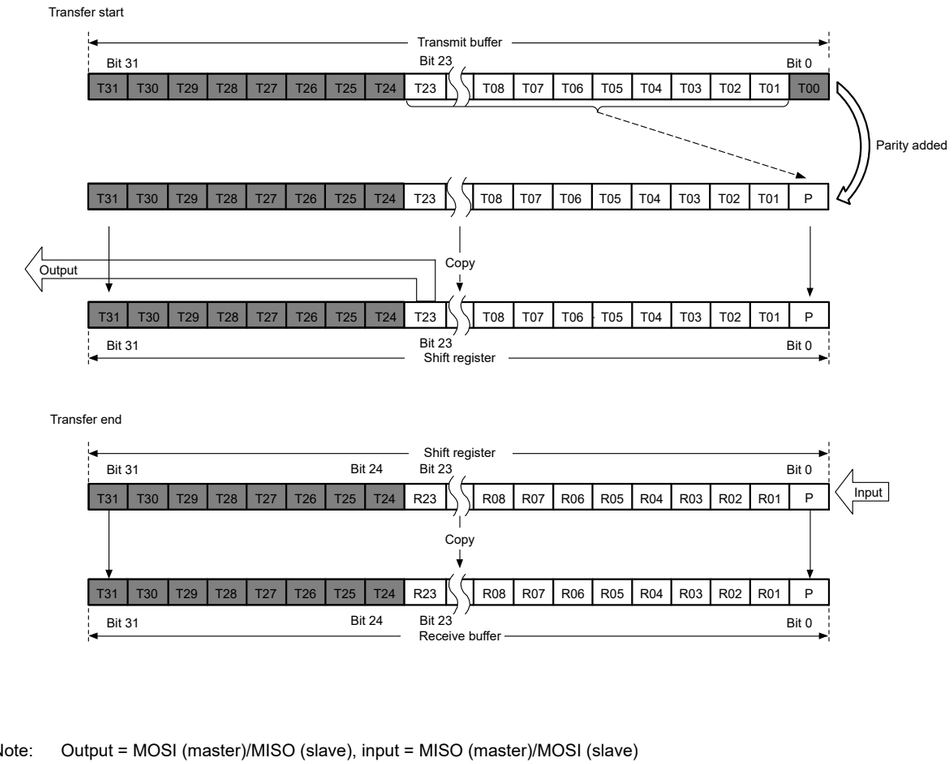
Figure 34.18 启用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图34.19显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，a SPI数据长度为24位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T23到T01计算的。这将替换最后一位T00，并将整个值复制到移位寄存器。数据按T23、T22、……、T01和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R23至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R23到P的数据的奇偶性。在发送-接收操作的情况下，发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送过程中将0写入T31到T24会导致将0插入接收缓冲区的高8位。另一方面，在只接收操作的情况下，接收缓冲区的高8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

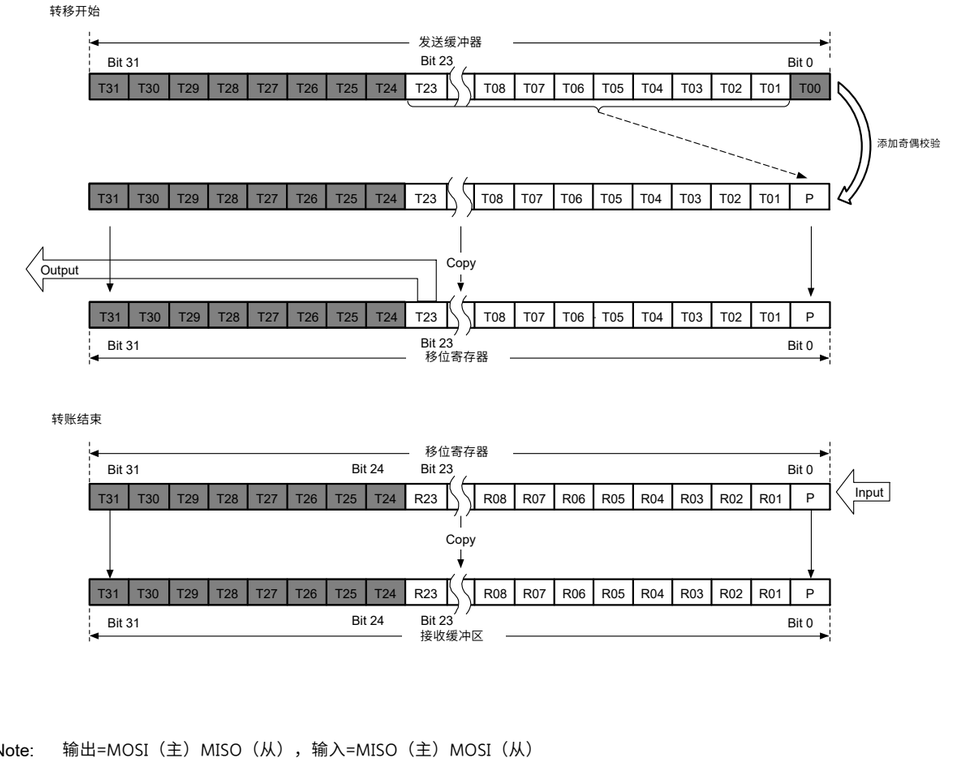
Figure 34.19 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 34.20 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit-by-bit through bit[0] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 34.19 启用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图34.20显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，
SPI数据长度为32位，并选择LSB-first。

在传输中，奇偶校验位(P)的值是从位T30到T00计算的。这将替换最后一位T31，并将整个值复制到移位寄存器。数据按T00、T01、……、T30和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R00到P的数据的奇偶性。

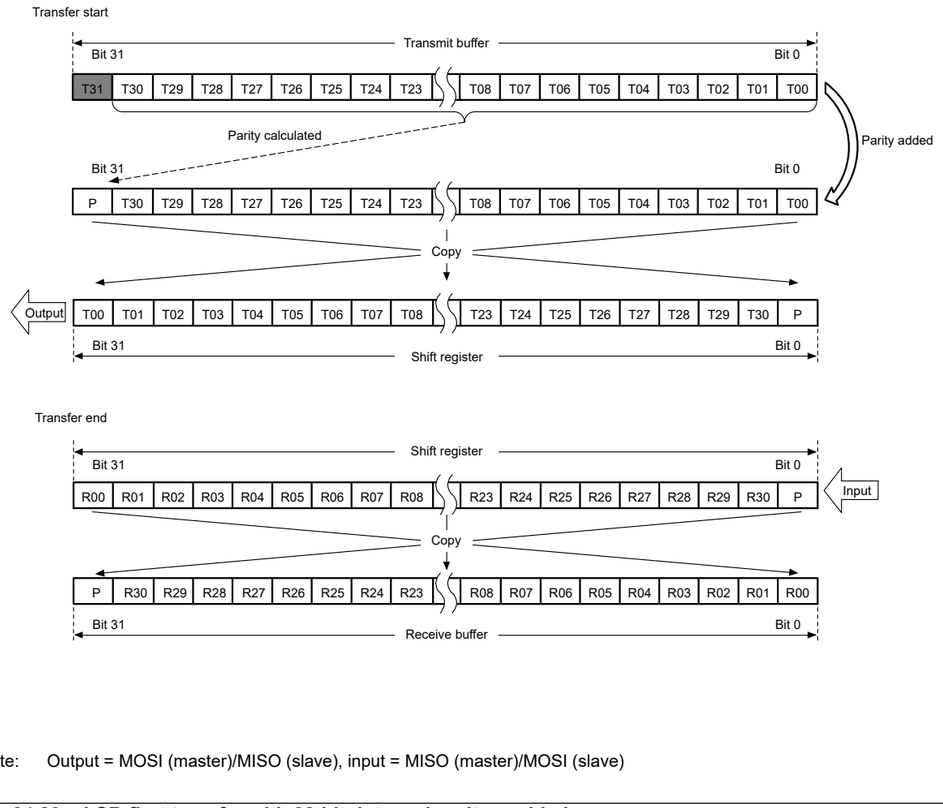


Figure 34.20 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 34.21 shows the operation of the SPI Data Register (SPDR) and the shift register in a transfer with parity enabled, a SPI data length of 24 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole value is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit-by-bit through bit[8] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, the data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer is stored in the upper 8 bits of the receive buffer in case of transmit-receive operation. Writing 0 to T31 to T24 during transmission leads to 0 being inserted in the upper 8 bits of the receive buffer. On the other hand, the upper 8-bits of the receive buffer is written 0 in case of receive only operation.

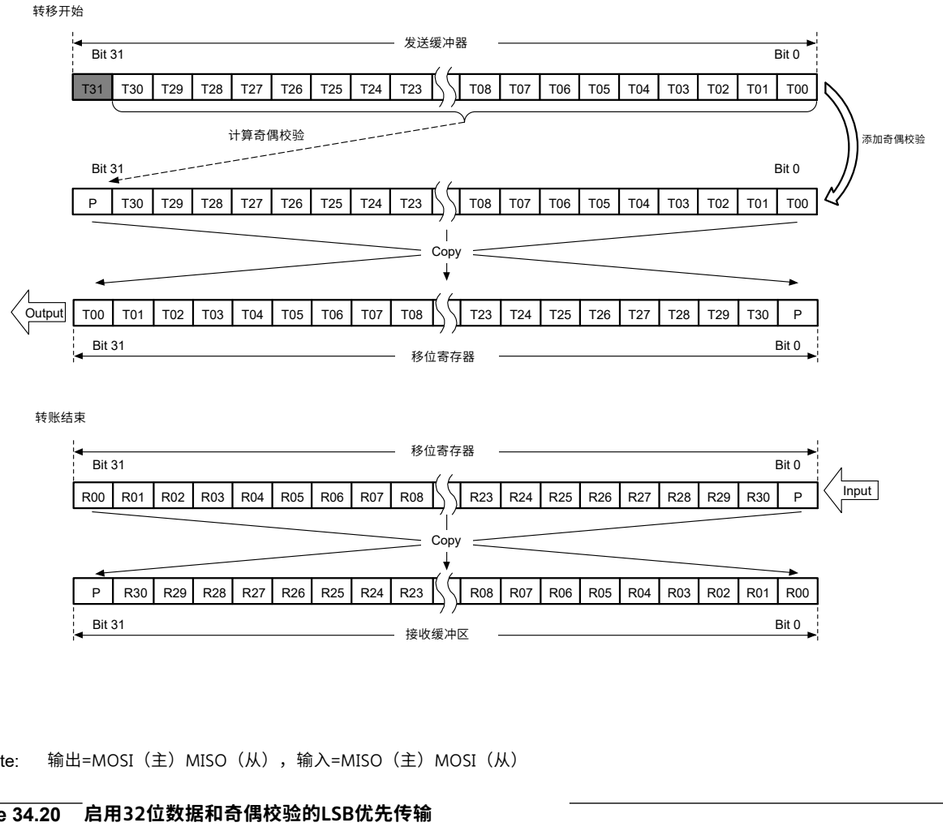


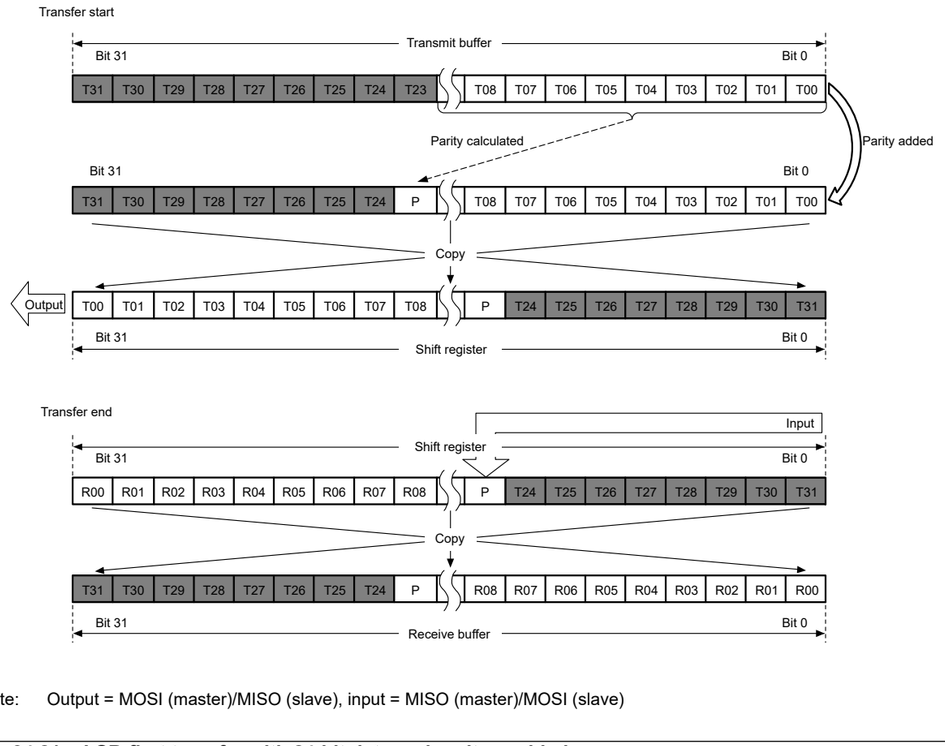
Figure 34.20 启用32位数据和奇偶校验的LSB优先传输

(4) 24位数据的LSB优先传输

图34.21显示了SPI数据寄存器(SPDR)和移位寄存器在启用奇偶校验的传输中的操作，a SPI数据长度为24位，并选择LSB优先。

在传输中，奇偶校验位(P)的值是从位T22到T00计算的。这将替换最后一位T23，并将整个值复制到移位寄存器。数据按T00、T01、……、T22和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的bit[8]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R00到P的数据的奇偶性。在发送-接收操作的情况下，发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送过程中将0写入T31到T24会导致将0插入接收缓冲区的高8位。另一方面，在只接收操作的情况下，接收缓冲区的高8位被写入0。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 34.21 LSB-first transfer with 24-bit data and parity enabled

34.3.4.3 Byte Swap Transmission

(1) MSB-first transfer. (When the byte swap is disabled.)

Data (Byte0 [T31 to T24] to Byte3 [T07 to T00]) in the transmit buffer are copied to the shift register.

Bit values in the shift register are shifted and transmitted in the order of T31 → T30 → … → T00 as transmit data.

(2) MSB-first transfer. (When the byte swap is enabled.)

Byte values of the transmit buffer (Byte0 [T31 to T24] to Byte3 [T07 to T00]) are reversed in byte units and are copied to the shift register in the order of Byte3 [T07 to T00] to Byte0 [T31 to T24].

Bit values in the shift register are shifted and transmitted in the order of T07 → T06 → … → T00 → T15 → T14 → … → T08 → T23 → T22 → … → T16 → T31 → T30 → … → T24 as transmit data.

(3) LSB-first transfer. (When the byte swap is disabled.)

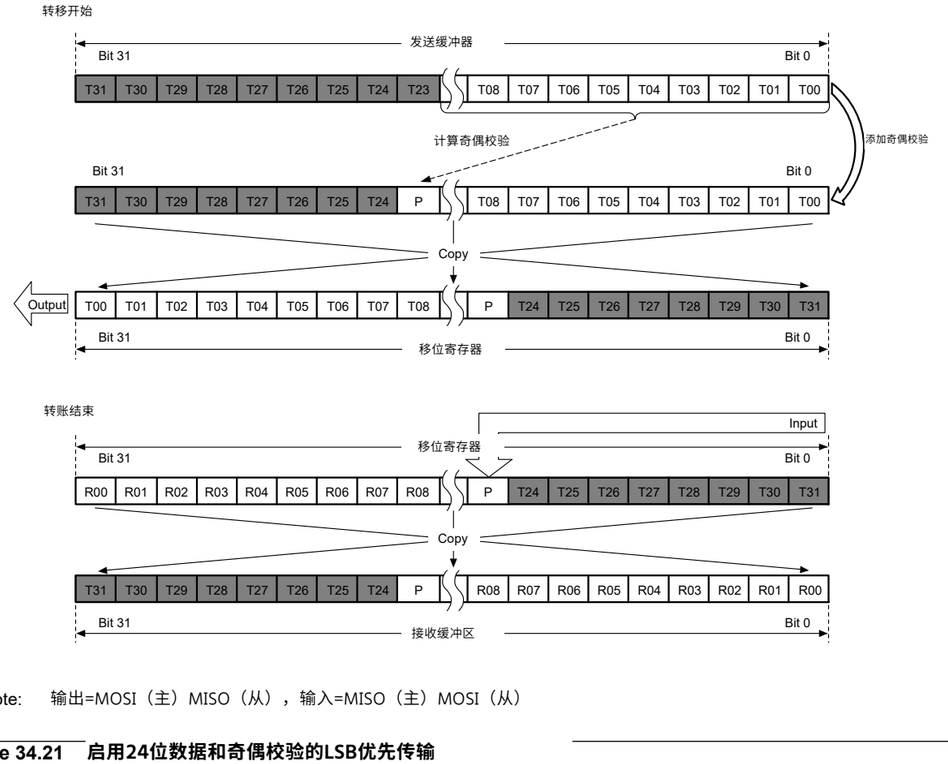
Bit values of the transmit buffer (Byte0 [T31 to T24] to Byte3 [T07 to T00]) are reversed in bit units and are copied to the shift register in the order of Byte3 [T00 to T07] to Byte0 [T24 to T31].

Bit values in the shift register are shifted and transmitted in the order of T00 → T01 → … → T31 as transmit data.

(4) LSB-first transfer. (When the byte swap is enabled.)

Bit values of each byte of the transmit buffer (Byte0 [T31 to T24] to Byte3 [T07 to T00]) are reversed in bit units and are copied to the shift register in the order of Byte0 [T24 to T31] to Byte3 [T00 to T07].

Bit values in the shift register are shifted and transmitted in the order of T24 → T25 → … → T31 → T16 → T17 → … → T23 → T08 → T09 → … → T15 → T00 → T01 → … → T07 as transmit data.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 34.21 启用24位数据和奇偶校验的LSB优先传输

34.3.4.3 字节交换传输

(1) MSB优先传输。（禁用字节交换时。）

发送缓冲器中的数据（Byte0[T31到T24]到Byte3[T07到T00]）被复制到移位寄存器。

移位寄存器中的位值按照T31→T30→…→T00的顺序移位和传输，作为传输数据。

(2) MSB优先传输。（启用字节交换时。）

发送缓冲区的字节值（Byte0[T31到T24]到Byte3[T07到T00]）以字节为单位反转，并按照Byte3[T07到T00]到Byte0[T31到T24]的顺序复制到移位寄存器.

移位寄存器中的位值按照T07→T06→…→T00→T15→T14→…→的顺序移位传输
T08→T23→T22→…→T16→T31→T30→…→T24作为传输数据。

(3) LSB优先传输。（禁用字节交换时。）

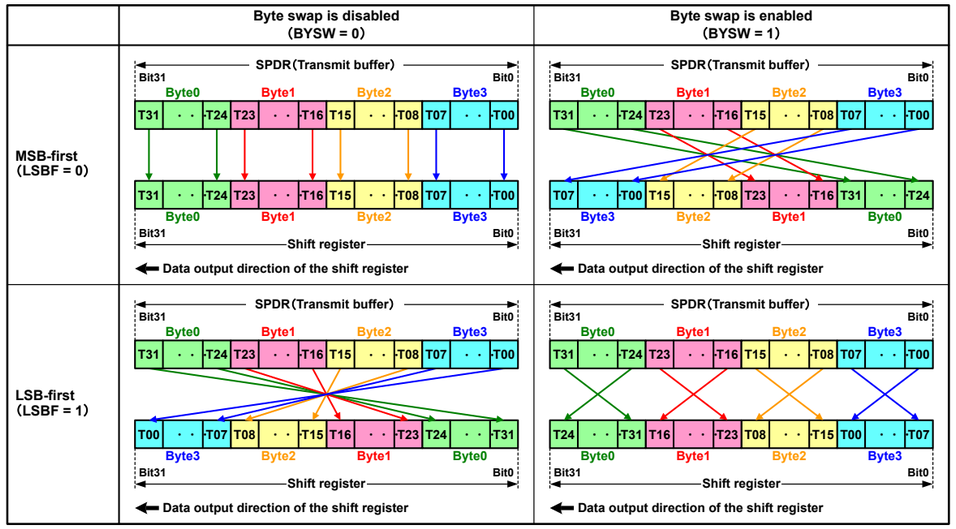
发送缓冲区的位值（Byte0[T31到T24]到Byte3[T07到T00]）以位为单位反转，并按照Byte3[T00到T07]到Byte0[T24到T31]的顺序复制到移位寄存器.

移位寄存器中的位值按照T00→T01→…→T31的顺序移位和发送，作为发送数据。

(4) LSB优先传输。（启用字节交换时。）

发送缓冲区（Byte0[T31到T24]到Byte3[T07到T00]）的每个字节的位值以位为单位反转，并按照Byte0[T24到T31]到Byte3[T00]的顺序复制到移位寄存器到T07]。

移位寄存器中的位值按照T24→T25→…→T31→T16→T17→…→的顺序进行移位和传输
T23→T08→T09→…→T15→T00→T01→…→T07作为传输数据。



Note: 1. When using the byte swap, set 16 bits or 32 bits to the data length (SPCMD.SPB[3:0] setting). If setting the other length (8 to 15, 20, 24 bits), the behavior is not guaranteed.
2. When the byte swap is valid, set the parity function as invalid (SPCR2.SPPE bit = 0). If setting the parity function as valid (SPPE bit = 1), the behavior is not guaranteed.
3. Set SPDCR2.BYSW bit, when SPCR.SPE bit is 0. If rewriting BYSW bit, when SPE bit is 1, the behavior after it is not guaranteed.

Figure 34.22 Byte swap with MSB/LSB transfer

34.3.4.4 Byte Swap Reception

(1) MSB-first transfer. (When the byte swap is disabled.)

The first received data (R31) is stored in bit 0 of the shift register, and received data is shifted in the order of R31 → R30 → … → R00.

When necessary RSPCK cycles are input and data is stored from Byte0 [R31 to R24] to Byte3 [R07 to R00], the shift register value is copied to the receive buffer.

(2) MSB-first transfer. (When the byte swap is enabled.)

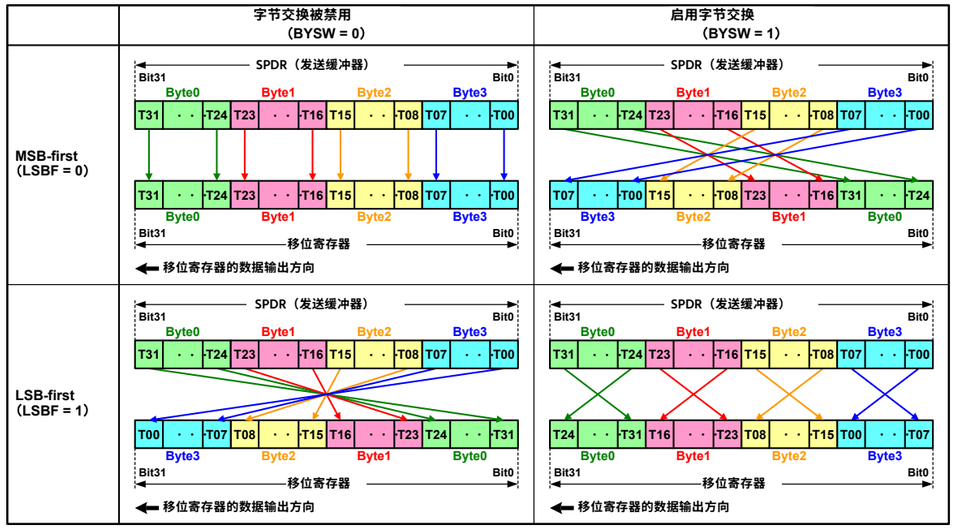
The first received data (R07) is stored in bit 0 of the shift register, and received data is shifted in the order of R07 → R06 → … → R00 → R15 → R14 → … → R08 → R23 → R22 → … → R16 → R31 → R30 → … → R24.

When necessary RSPCK cycles are input and data is stored from Byte3 [R07 to R00] to Byte0 [R31 to R24], byte values in the shift register are reversed in byte units and are copied to the receive buffer in the order of Byte0 [R31 to R24] to Byte3 [R07 to R00].

(3) LSB-first transfer. (When the byte swap is disabled.)

The first received data (R00) is stored in bit 0 of the shift register, and received data is shifted in the order of R00 → R01 → … → R31.

When necessary RSPCK cycles are input and data is stored from Byte3 [R00 to R07] to Byte0 [R24 to R31], bit values in the shift register are reversed in bit units and are copied to the receive buffer in the order of Byte0 [R31 to R24] to Byte3 [R07 to R00].



Note: 1.使用字节交换时，将数据长度设置为16位或32位（SPCMD.SPB[3:0]设置）。如果设置其他长度（8到15、20、24位），则无法保证行为。2.当字节交换有效时，将奇偶校验功能设置为无效（SPCR2.SPPE位=0）。如果将奇偶校验功能设置为有效（SPPE位=1），则无法保证行为。3.当SPCR.SPE位为0时，设置SPDCR2.BYSW位。如果重写BYSW位，当SPE位为1时，不保证之后的行为。

Figure 34.22 带MSBLSB传输的字节交换

34.3.4.4 字节交换接收

(1) MSB优先传输。（禁用字节交换时。）

第一个接收到的数据（R31）存储在移位寄存器的第0位，接收到的数据按照R31→R30→…→R00的顺序进行移位。

当输入必要的RSPCK周期并将数据从Byte0[R31到R24]存储到Byte3[R07到R00]时，移位寄存器值被复制到接收缓冲区。

(2) MSB优先传输。（启用字节交换时。）

第一个接收到的数据（R07）存放在移位寄存器的第0位，接收到的数据按照R07→R06→…→R00→R15→R14→…→R08→R23→R22→…→R16→的顺序移位R31→R30→…→R24。

当输入必要的RSPCK周期并将数据从Byte3[R07到R00]存储到Byte0[R31到R24]时，移位寄存器中的字节值以字节为单位进行反转，并按Byte0[R31的顺序复制到接收缓冲区到R24]到字节3[R07到R00]。

(3) LSB优先传输。（禁用字节交换时。）

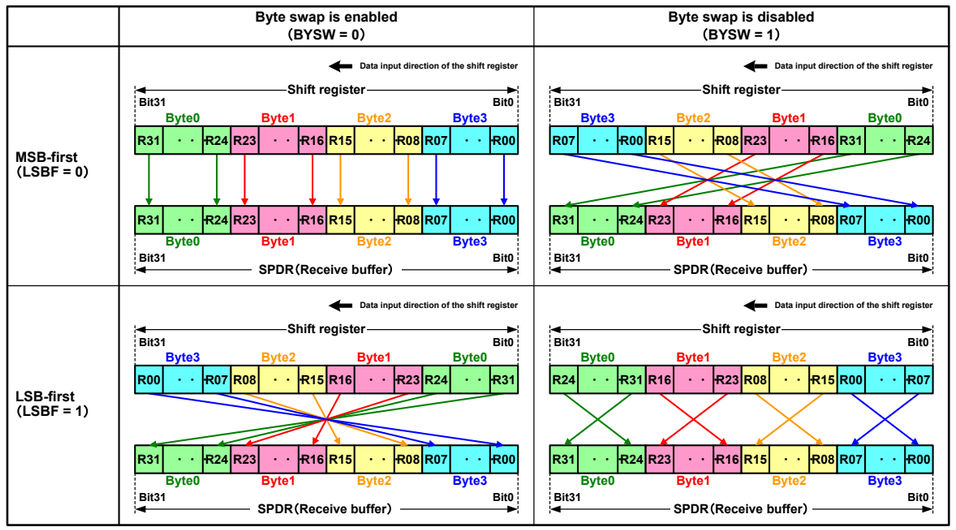
第一个接收到的数据（R00）存放在移位寄存器的第0位，接收到的数据按照R00→R01→…→R31的顺序移位。

当输入必要的RSPCK周期并将数据从Byte3[R00到R07]存储到Byte0[R24到R31]时，移位寄存器中的位值以位为单位反转，并按Byte0[R31的顺序复制到接收缓冲区到R24]到字节3[R07到R00]。

(4) LSB-first transfer. (When the byte swap is enabled.)

The first received data (R24) is stored in bit 0 of the shift register, and received data is shifted in the order of R24 → R25 → … → R31 → R16 → R17 → … → R23 → R08 → R09 → … → R15 → R00 → R01 → … → R07.

When necessary RSPCK cycles are input and data is stored from Byte0 [R24 to R31] to Byte3 [R00 to R07], bit values of each byte in the shift register are reversed in bit units and are copied to the receive buffer in the order of Byte0 [R31 to R24] to Byte3 [R07 to R00].



Note: 1. When using the byte swap, set 16 bits or 32 bits to the data length (SPCMD.SPB[3:0] setting). If setting the other length (8 to 15, 20, 24 bits), the behavior is not guaranteed.
2. When the byte swap is valid, set the parity function as invalid (SPCR2.SPPE bit = 0). If setting the parity function as valid (SPPE bit = 1), the behavior is not guaranteed.
3. Set SPDCR2.BYSW bit, when SPCR.SPE bit is 0. If rewriting BYSW bit, when SPE bit is 1, the behavior after it is not guaranteed.

Figure 34.23 Byte swap with MSB/LSB transfer

34.3.5 Transfer Formats

34.3.5.1 When CPHA = 0

Figure 34.24 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 34.24, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0, and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 34.3.2. Controlling the SPI Pins.

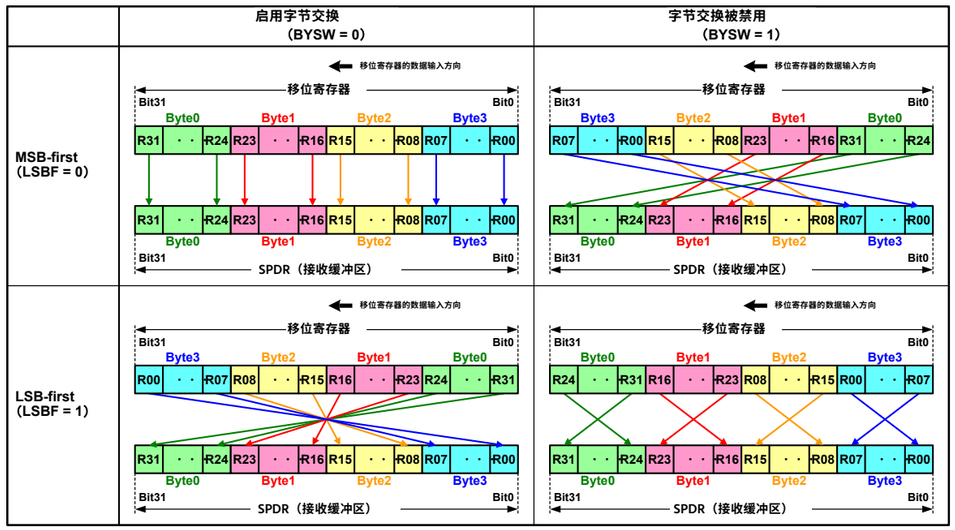
When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals begins at an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCK cycle. The change timing for MOSIn and MISOn signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing as it only affects the signal polarity.

t1 denotes the RSPCK delay, the period from an SSLni signal assertion to RSPCKn oscillation. t2 denotes the SSL negation delay, the period from the termination of RSPCKn oscillation to an SSLni signal negation. t3 denotes the next-access delay,

(4) LSB优先传输。（启用字节交换时。）

第一个接收到的数据（R24）存放在移位寄存器的第0位，接收到的数据按R24→R25→…→R31→R16→R17→…→R23→R08→R09→…→R15→的顺序移位R00→R01→…→R07。

当输入必要的RSPCK周期并将数据从Byte0[R24到R31]到Byte3[R00到R07]存储时，移位寄存器中每个字节的位值以位为单位反转，并按顺序复制到接收缓冲区Byte0[R31到R24]到Byte3[R07到R00]。



Note: 1.使用字节交换时，将数据长度设置为16位或32位（SPCMD.SPB[3:0]设置）。如果设置其他长度（8到15、20、24位），则无法保证行为。2.当字节交换有效时，将奇偶校验功能设置为无效（SPCR2.SPPE位=0）。如果将奇偶校验功能设置为有效（SPPE位=1），则无法保证行为。3.当SPCR.SPE位为0时，设置SPDCR2.BYSW位。如果重写BYSW位，当SPE位为1时，不保证之后的行为。

Figure 34.23 带MSBLSB传输的字节交换

34.3.5 传输格式

34.3.5.1 When CPHA = 0

图34.24显示了当SPCMDm.CPHA位为0时串行传输8位数据的示例传输格式。当SPI在从机模式下运行时（SPCR.MSTR=0)且CPHA位为0。在图34.24中，RSPCKn(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形，RSPCKn(CPOL=1)表示CPOL位为0时的RSPCKn信号波形1.采样时序表示SPI将串行传输数据取入移位寄存器的时序。信号的IO方向取决于SPI设置。有关详细信息，请参阅第34.3.2节。控制SPI引脚。

当SPCMDm.CPHA位为0时，将有效数据驱动到MOSIn和MISOn信号开始于SSLni信号断言。在SSLni信号断言之后发生的第一个RSPCKn信号变化成为第一次传输数据获取。此后，每1个RSPCK周期对数据进行采样。MOSIn和MISOn信号的变化时序是传输数据获取时序之后的12RSPCK周期。CPOL位设置不影响RSPCK信号操作时序，因为它只影响信号极性。

t1表示RSPCK延迟，即从SSLni信号断言到RSPCKn振荡的周期。t2表示SSL否定延迟，即从RSPCKn振荡终止到SSLni信号否定的周期。t3表示下一次访问延迟，

the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer. t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI is in master mode, see section 34.3.11.1. Master mode operation.

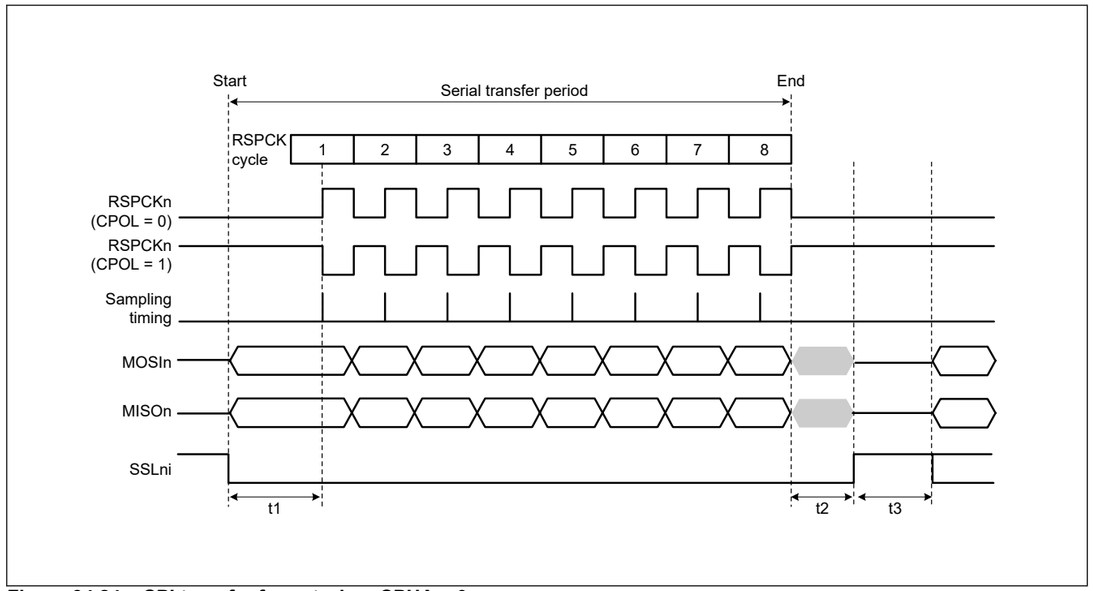


Figure 34.24 SPI transfer format when CPHA = 0

34.3.5.2 When CPHA = 1

Figure 34.25 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 34.25, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0 and RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave mode). For details, see section 34.3.2. Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal begins at an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals begins at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing. It only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 34.3.11.1. Master mode operation.

在串行传输结束后，为下一次传输抑制SSLni信号断言的时间段。t1、t2和t3由在SPI系统上运行的主设备控制。有关SPI处于主机模式时的t1、t2和t3的说明，请参见第34.3.11.1节。主模式操作。

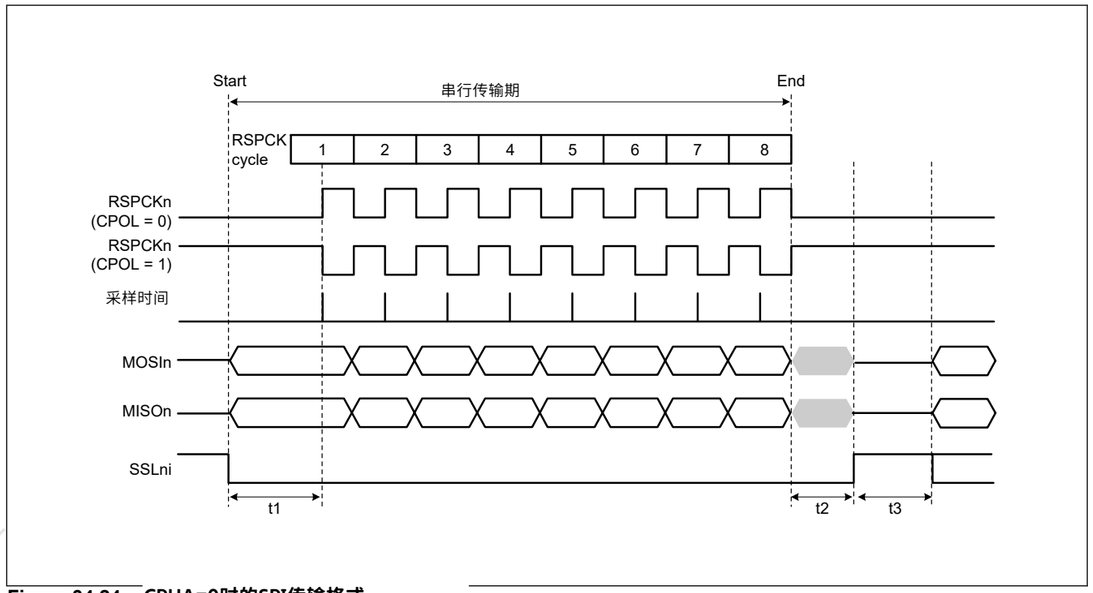


Figure 34.24 CPHA=0时的SPI传输格式

34.3.5.2 When CPHA = 1

图34.25显示了当SPMDm.CPHA位为1时串行传输8位数据的示例传输格式。
但是，当SPCR.SPMS位为1时，不使用SSLni信号，只有RSPCKn、MOSIn和MISON处理通信。在图34.25中，RSPCK(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形，RSPCK(CPOL=1)表示CPOL位为1时的RSPCKn信号波形。SPI将串行传输数据提取到移位寄存器中。信号的IO方向取决于SPI模式（主模式或从模式）。有关详细信息，请参阅第34.3.2节。控制SPI引脚。

当SPCMDm.CPHA位为1时，将无效数据驱动到MIOn信号开始于SSLni信号断言。在SSLni信号置位后发生的第一个RSPCKn信号变化时，开始向MOSIn和MISOn信号输出有效数据。此后，每1个RSPCK周期更新一次数据。传输数据获取时序是数据更新时序之后的12个RSPCK周期。SPCMDm.CPOL位设置不影响RSPCKn信号操作时序。它只影响信号极性。

t1、t2、t3与CPHA=0时相同。MCU的SPI为主机模式时t1、t2、t3的说明见34.3.11.1节。主模式操作。

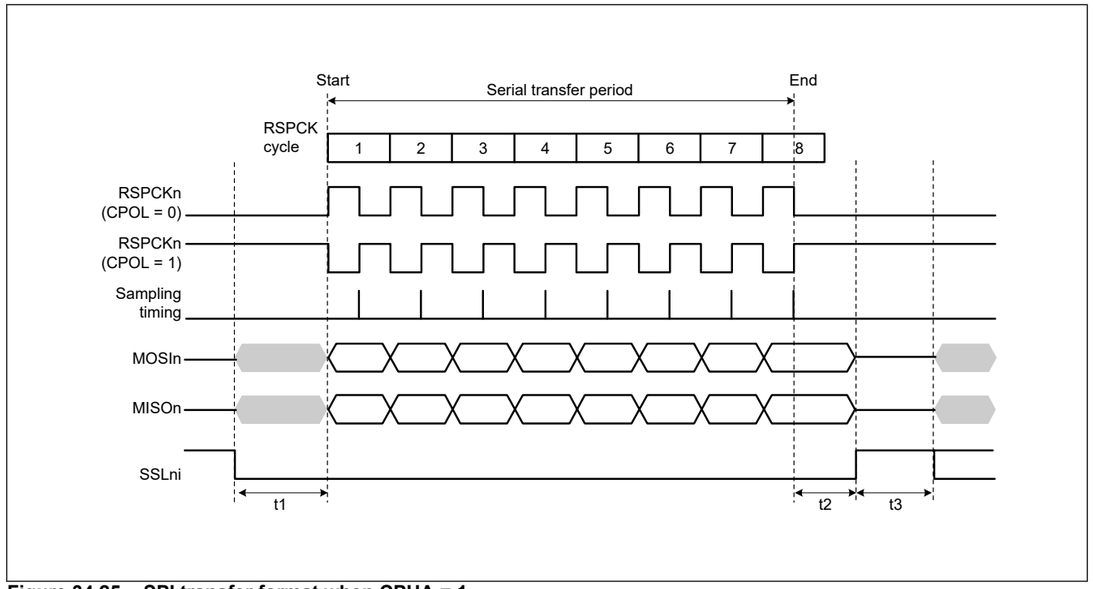


Figure 34.25 SPI transfer format when CPHA = 1

34.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected in the Communications Operating Mode Select bit (SPCR.TXMD) when the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is 0. The SPI operation is receive only in slave mode (SPCR.MSTR = 0) when the SPCR3.ETXMD bit is 1, because SPCR.TXMD bit does not affect the SPI operation. The register accesses shown in Figure 34.26, Figure 34.27, and Figure 34.28 indicate the condition of access to the SPDR/SPDR_HA register, where W denotes a write cycle.

34.3.6.1 Full-duplex synchronous serial communications (SPCR3.ETXMD = 0, SPCR.TXMD = 0)

Figure 34.26 shows an example of operation when the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is set to 0 and the Communications Operating Mode Select bit (SPCR.TXMD) is set to 0. In this example, the SPI performs an 8-bit serial transfer when SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

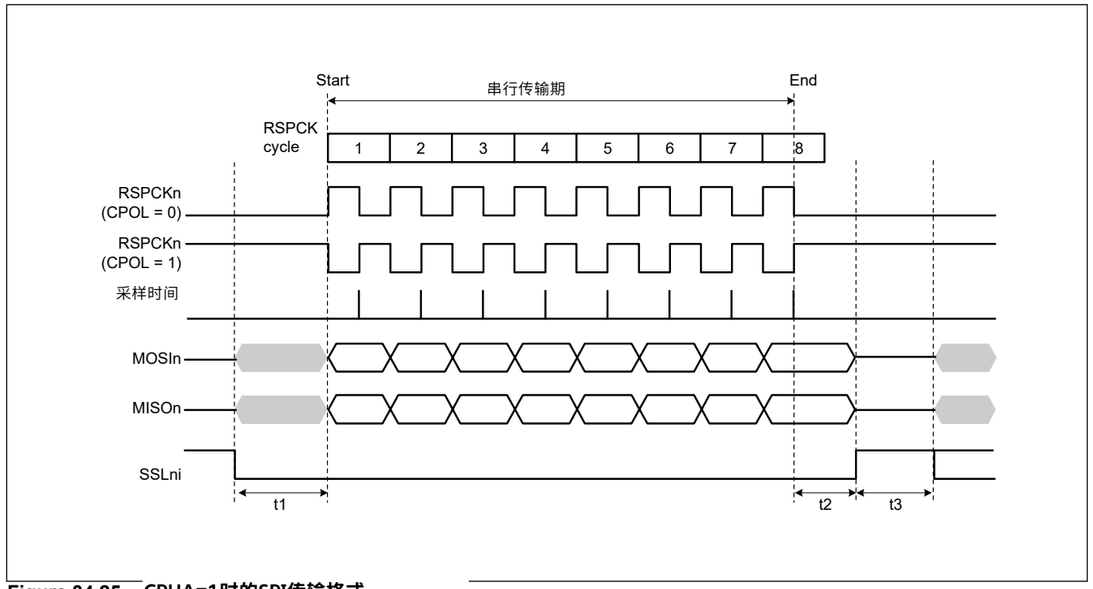


Figure 34.25 CPHA=1时的SPI传输格式

34.3.6 数据传输模式

全双工同步串行通信或传输操作只能在通信中选择当SPI控制寄存器3(SPCR3)中的扩展通信模式选择位(ETXMD)为0时，工作模式选择位(SPCR.TXMD)。当SPCR3.ETXMD位为1，因为SPCR.TXMD位不影响SPI操作。图34.26、图34.27和图34.28所示的寄存器访问表示访问SPDRSPDR_HA寄存器的条件，其中W表示写周期。

34.3.6.1 全双工同步串行通信（SPCR3.ETXMD=0，SPCR.TXMD = 0)

图34.26显示了当SPI控制寄存器3(SPCR3)中的扩展通信模式选择位(ETXMD)设置为0并且通信操作模式选择位(SPCR.TXMD)设置为0时的操作示例。在此示例中，当SPDCR.SPFC[1:0]位为00b、SPCMDm.CPHA位为1、SPCMDm.CPOL位为0时，SPI执行8位串行传输。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

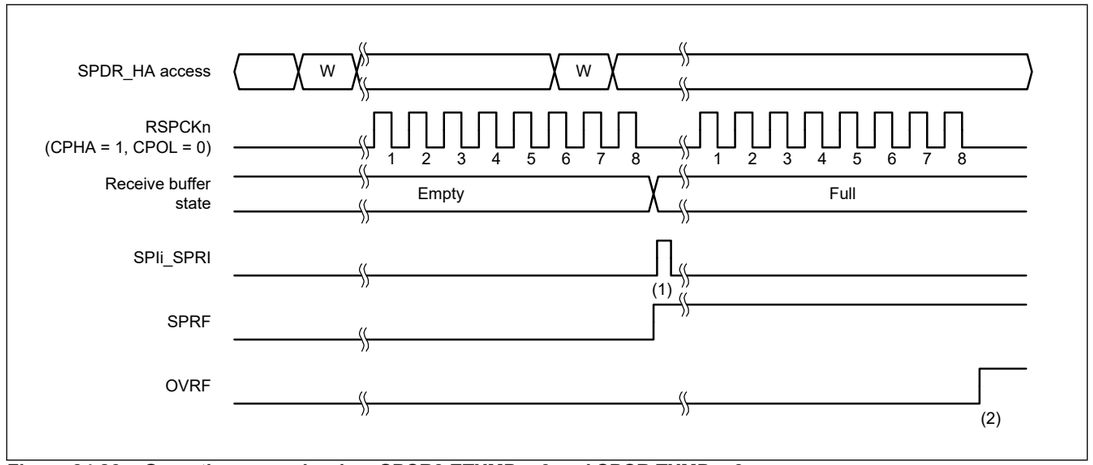


Figure 34.26 Operation example when SPCR3.ETXMD = 0 and SPCR.TXMD = 0

The operation of the flags at timings (1) and (2) in Figure 34.26 is as follows:

1. When a serial transfer ends with the receive buffer of SPDR_HA empty, the SPI generates a receive buffer full interrupt request (SPIi_SPRI), the SPI sets the SPSR.SPRF flag to 1, and copies the received data in the shift register to the receive buffer.
2. When a serial transfer ends with the receive buffer of SPDR_HA holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1, and discards the received data in the shift register. For details about the operation of the SPSR.OVRF flag, see section 34.3.9.1. Overrun errors.

34.3.6.2 Transmit-Only Serial Communications (SPCR3.ETXMD = 0, SPCR.TXMD = 1)

Figure 34.27 shows an example of operation when the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is set to 0 and the Communications Operating Mode Select bit (SPCR.TXMD) is set to 1. In this example, the SPI performs an 8-bit serial transfer when SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

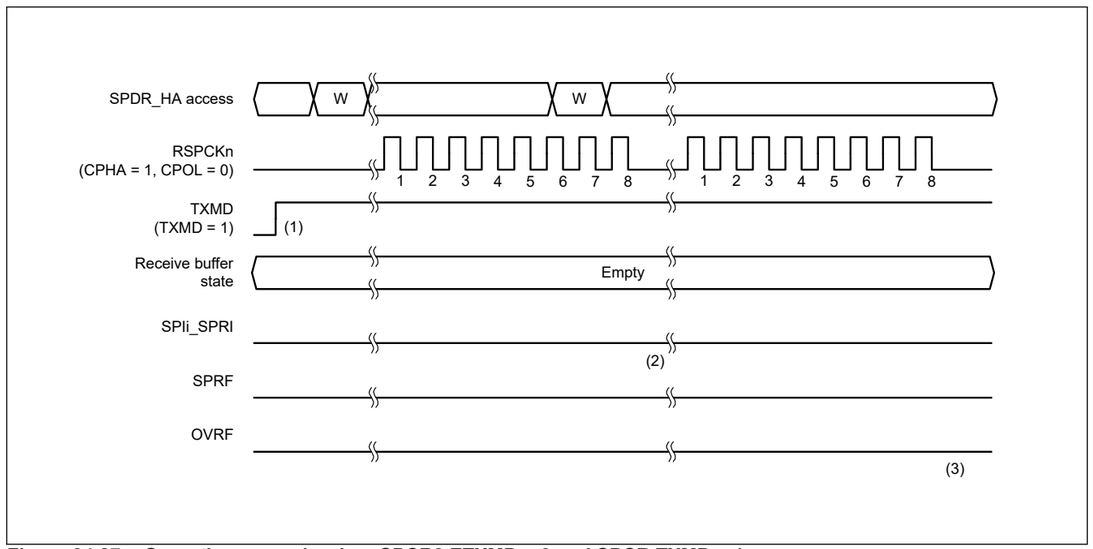


Figure 34.27 Operation example when SPCR3.ETXMD = 0 and SPCR.TXMD = 1

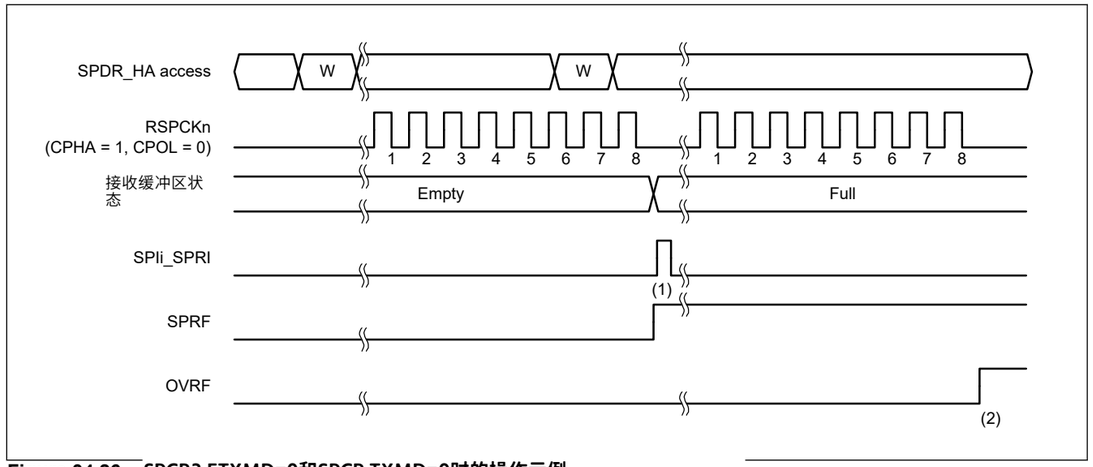


Figure 34.26 SPCR3.ETXMD=0和SPCR.TXMD=0时的操作示例

图34.26中时间(1)和(2)的标志操作如下：

1.当串行传输结束且SPDR_HA的接收缓冲区为空时，SPI产生接收缓冲区满中断请求（SPIi_SPRI），SPI将SPSR.SPRF标志设置为1，并将接收到的移位寄存器中的数据复制到接收缓冲区。

2.当串行传输结束时，SPDR_HA的接收缓冲区保存了前一次串行传输中接收到的数据，SPI将SPSR.OVRF标志设置为1，并丢弃移位寄存器中接收到的数据。有关SPSR.OVRF标志操作的详细信息，请参见第34.3.9.1节。溢出错误。

34.3.6.2 仅发送串行通信（SPCR3.ETXMD=0，SPCR.TXMD=1）

图34.27显示了当SPI控制寄存器3(SPCR3)中的扩展通信模式选择位(ETXMD)设置为0并且通信操作模式选择位(SPCR.TXMD)设置为1时的操作示例。在此示例中，当SPDCR.SPFC[1:0]位为00b、SPCMDm.CPHA位为1、SPCMDm.CPOL位为0时，SPI执行8位串行传输。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的位数。

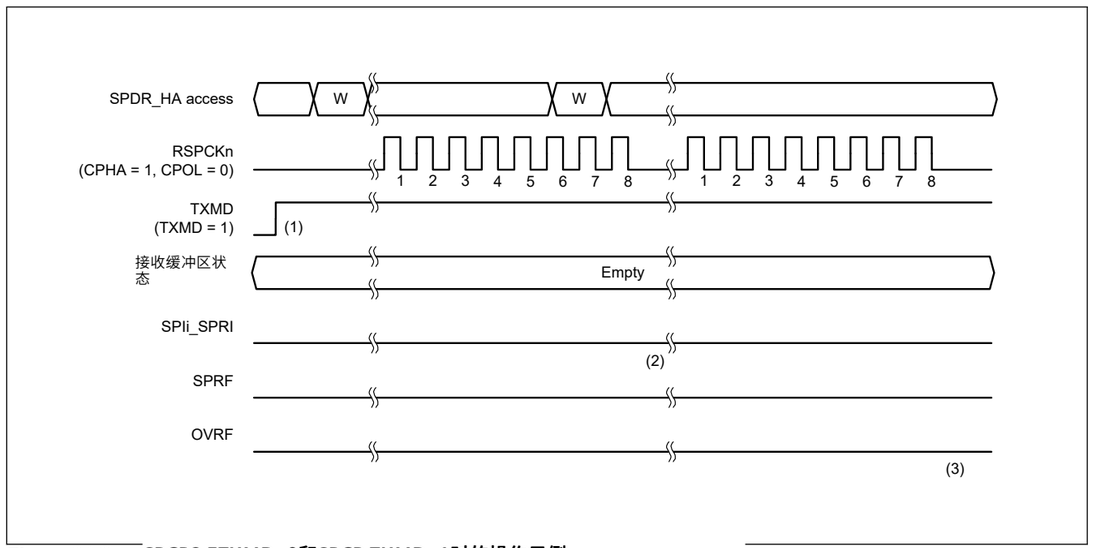


Figure 34.27 SPCR3.ETXMD=0和SPCR.TXMD=1时的操作示例

The operation of the flags at timings (1) to (3) in Figure 34.27 is as follows:

1. Make sure there is no data left in the receive buffer (the SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering transmit-only mode (SPCR3.ETXMD = 0, SPCR.TXMD = 1).
2. When a serial transfer ends with the receive buffer of SPDR_HA empty, if the transmit-only mode is selected (SPCR3.ETXMD = 0, SPCR.TXMD = 1), the SPSR.SPRF flag retains the value of 0, and the SPI does not copy the data in the shift register to the receive buffer.
3. Because the receive buffer of SPDR_HA does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

In transmit-only mode (SPCR3.ETXMD = 0, SPCR.TXMD = 1), the SPI transmits data but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at timings (1) to (3).

34.3.6.3 Receive-Only Serial Communication (MSTR = 0, ETXMD = 1)

Figure 34.28 shows an example of operation when the SPI master/slave mode select bit (MSTR) in the SPI control register (SPCR) is set to 0 and the extended communication mode select bit (ETXMD) in the SPI control register 3 (SPCR3) is set to 1. In the example in Figure 34.28, the SPI performs 8-bit data serial transfer with the settings of SPFC[1:0] in the SPI data control register (SPDCR) = 00b, CPHA in the SPI command register (SPCMD) = 1, and CPOL in SPCMD = 0. Numbers under the RSPCK waveform show the number of RSPCK cycles (number of transfer bits).

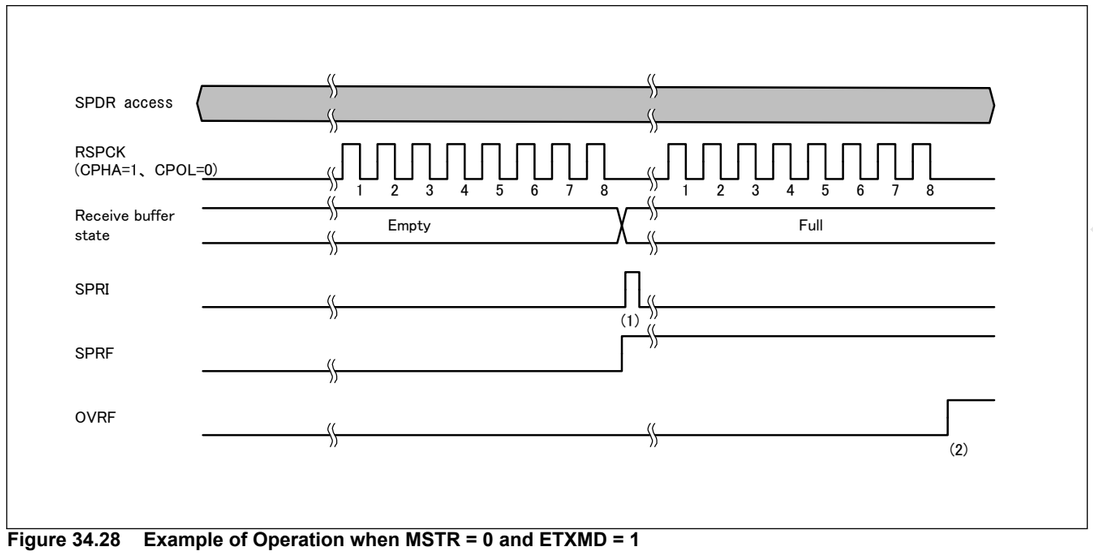


Figure 34.28 Example of Operation when MSTR = 0 and ETXMD = 1

The following describes operation of flags at timings (1) and (2) in the figure above.

(1) When serial transfer ends while the SPDR's receive buffer is empty, the SPI generates a receive buffer full interrupt request SPRI (setting the SPSR.SPRF flag to 1) and copies the received data in the shift register to the receive buffer

(2) When serial transfer ends while previously received data is remaining in the SPDR's receive buffer, the SPI sets the OVRF flag in the SPI status register (SPSR) to 1 and discards the received data in the shift register.

34.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 34.29 and Figure 34.30 show examples of operation of the transmit buffer empty interrupt (SPIi_SPTI) and the receive buffer full interrupt (SPIi_SPRI). The SPDR_HA register accesses shown in these figures indicate the conditions of access to the register, where W denotes a write cycle and R a read cycle. In Figure 34.29, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 0, and the SPCMDm.CPOL bit is 0. In Figure 34.30, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the

图34.27中时间(1)到(3)的标志操作如下：

1.在进入仅发送模式（SPCR3.ETXMD=0，SPCR.TXMD=1）之前，确保接收缓冲区中没有剩余数据（SPSR.SPRF标志为0）且SPSR.OVRF标志为0。

2.当串行传输结束且SPDR_HA的接收缓冲区为空时，如果选择了仅传输模式（SPCR3.ETXMD=0 SPCR.TXMD=1），SPSR.SPRF标志保持0的值，SPI不将移位寄存器中的数据复制到接收缓冲区。

3、因为SPDR_HA的接收缓冲区中没有保存上一次串行传输接收到的数据，所以即使一次串行传输结束，SPSR.OVRF标志保持值0，移位寄存器中的数据不会被复制到接收缓冲区。

在仅发送模式下（SPCR3.ETXMD=0，SPCR.TXMD=1），SPI发送数据但不接收数据。
因此，SPSR.SPRF和SPSR.OVRF标志在时间(1)到(3)保持0。

34.3.6.3 仅接收串行通信（MSTR=0，ETXMD=1）

图34.28显示了当SPI控制寄存器(SPCR)中的SPI主从模式选择位(MSTR)设置为0并且SPI控制寄存器3(SPCR3)中的扩展通信模式选择位(ETXMD)为设置为1。在图34.28的示例中，SPI执行8位数据串行传输，设置SPI数据控制寄存器（SPDCR）中的SPFC[1:0]=00b，SPI命令寄存器中的CPHA（SPCMD)=1，SPCMD中的CPOL=0。RSPCK波形下的数字表示RSPCK周期数（传输位数）。

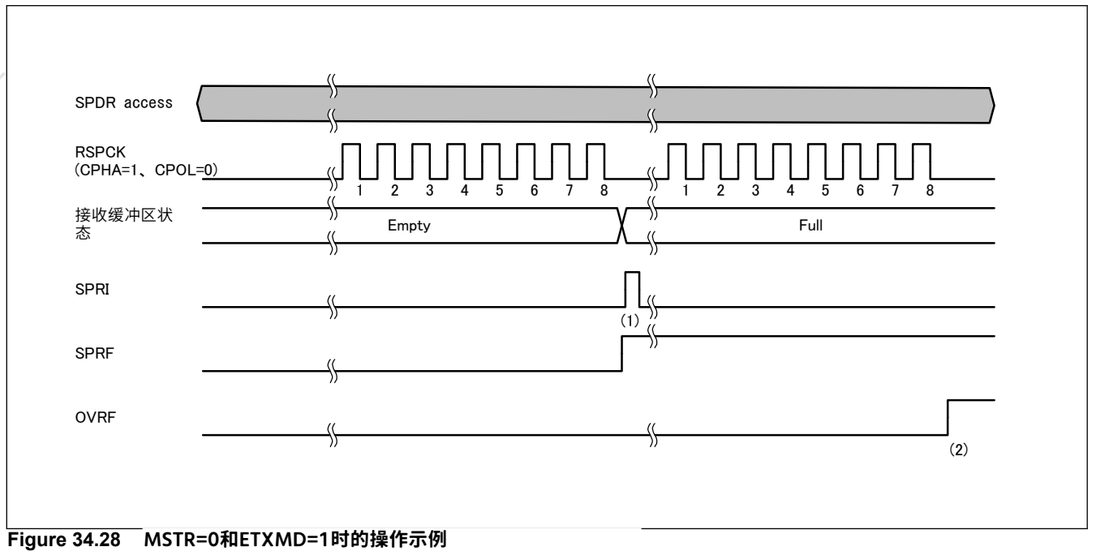


Figure 34.28 MSTR=0和ETXMD=1时的操作示例

下面描述在上图中的时间(1)和(2)的标志的操作。

(1)当串行传输结束而SPDR的接收缓冲区为空时，SPI产生接收缓冲区满中断请求SPRI（将SPSR.SPRF标志设置为1）并将接收到的移位寄存器中的数据复制到接收缓冲区

(2)当串行传输结束而先前接收的数据仍留在SPDR的接收缓冲区中时，SPI将SPI状态寄存器(SPSR)中的OVRF标志设置为1，并丢弃移位寄存器中的接收数据。

34.3.7 发送缓冲区空和接收缓冲区满中断

图34.29和图34.30显示了发送缓冲区空中断(SPIi_SPTI)和接收缓冲区满中断(SPIi_SPRI)的操作示例。这些图中显示的SPDR_HA寄存器访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在图34.29中，当SPCR.TXMD位为0、SPDCR.SPFC[1:0]位为00b、SPCMDm.CPHA位为0、SPCMDm.CPOL位为0时，SPI执行8位串行传输.在图34.30中，当SPCR.TXMD位为0时，SPI执行8位串行传输，

SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

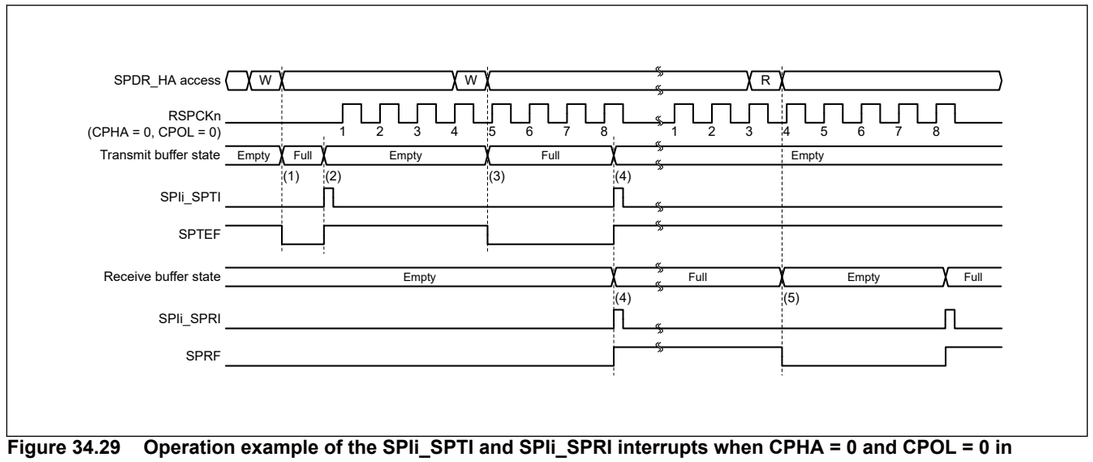


Figure 34.29 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 0 and CPOL = 0 in master mode

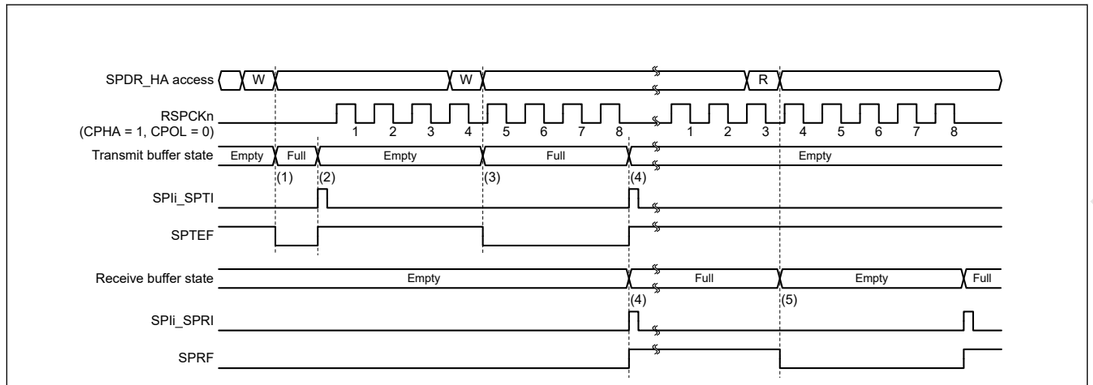


Figure 34.30 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 1 and CPOL = 0 in master mode

The operation of the SPI at timings (1) to (5) in Figure 34.29 and Figure 34.30 is as follows:

1. When transmit data is written to SPDR_HA with the transmit buffer of SPDR_HA is empty and data for the next transfer is not set, the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.
2. If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIi_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the SPI mode. For details, see section 34.3. Operation, and section 34.3.12. Clock Synchronous Operation.
3. When transmit data is written to SPDR_HA either by the transmit buffer empty interrupt routine, or by the processing of the transmit buffer empty using the SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the data being transferred serially is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends with the receive buffer of SPDR_HA empty, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIi_SPRI), and sets the SPRF flag to 1. Because the shift register becomes empty on completion of the serial transfer, if the transmit buffer is full before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies data in the transmit buffer to the shift register. Even

SPDCR.SPFC[1:0]位为00b，SPCMDm.CPHA位为1，SPCMDm.CPOL位为0。
波形中的RSPCKn表示RSPCK周期数，例如传输的位数。

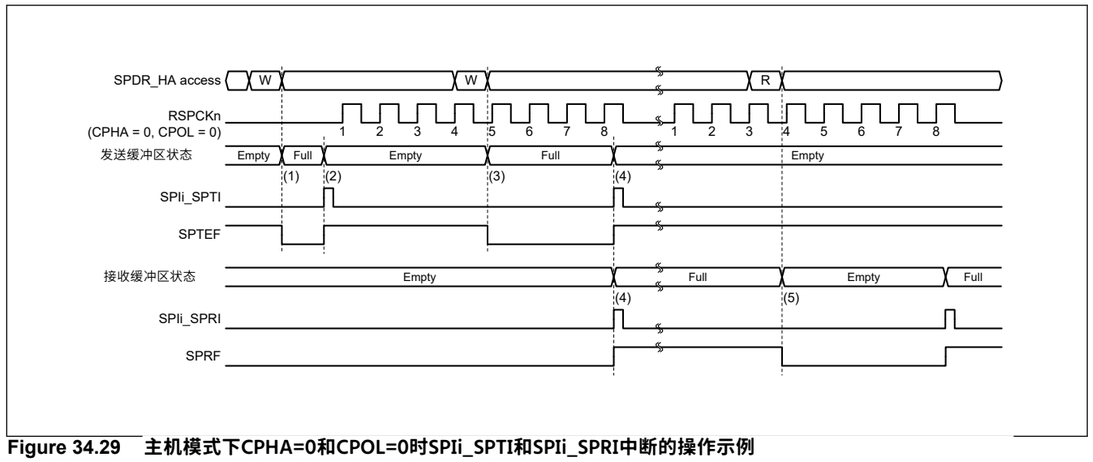


Figure 34.29 主机模式下CPHA=0和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

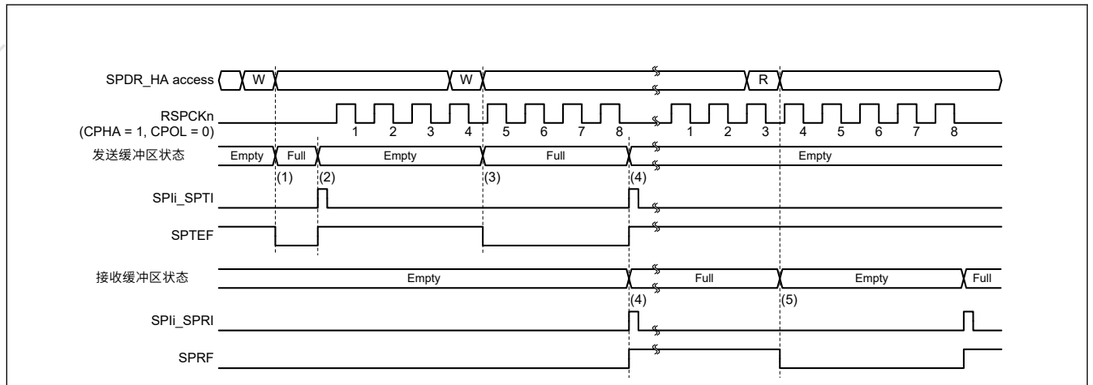


Figure 34.30 主机模式下CPHA=1和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

SPI在图34.29和图34.30中时序（1）到（5）的操作如下：

1.当发送数据写入SPDR_HA且SPDR_HA的发送缓冲区为空且未设置下一次传输的数据时，SPI将数据写入发送缓冲区并将SPSR.SPTEF标志清除为0。

2.如果移位寄存器为空，SPI将发送缓冲区中的数据复制到移位寄存器，产生发送缓冲区空中断请求（SPIi_SPTI），并将SPSR.SPTEF标志设置为1。如何启动串行传输取决于SPI模式。有关详细信息，请参阅第34.3节。操作和第34.3.12节。时钟同步操作。

3.当发送数据被发送缓冲区空中断程序写入SPDR_HA时，或者通过使用SPTEF标志处理发送缓冲区空时，SPI将数据写入发送缓冲区并将SPTEF标志清除为0。因为串行传输的数据存储在移位寄存器中，SPI不会将发送缓冲区中的数据复制到移位寄存器中。

4.当串行传输结束且SPDR_HA的接收缓冲区为空时，SPI将移位寄存器中的接收数据复制到接收缓冲区，产生接收缓冲区满中断请求（SPIi_SPRI），并将SPRF标志设置为1。因为串行传输完成后移位寄存器变为空，如果在串行传输结束前发送缓冲区已满，SPI将SPTEF标志设置为1，并将发送缓冲区中的数据复制到移位寄存器。甚至

when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.

5. When SPDR_HA is read either by the receive buffer full interrupt routine or processing of the receive buffer full interrupt using the SPRF flag, the receive data can be read.

If SPDR_HA is written to when the transmit buffer holds data that is not yet transmitted (the SPTEF flag is 0), the SPI does not update data in the transmit buffer. When writing to SPDR_HA, always use either a transmit buffer empty interrupt request or processing of the transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (the SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends and the receive buffer is full (the SPRF flag is 1), the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 34.3.9. Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRn.IR flags (where n is the interrupt vector number) in the ICU can be used to confirm the states of the transmit and receive buffers.

Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 13, Interrupt Controller Unit (ICU) for the interrupt vector numbers.

34.3.8 Communication End Interrupt

34.3.8.1 Transmit-Receive/Transmit in Master Mode

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1, when following conditions are satisfied in transmit-receive master mode and transmit master mode. The set timing of the CENDF flag is same as IDLNF flag. The communication end interrupt (SPCI) is one PCLKUSCIx width and low active.

- When the value of the SPSSR.SPCP[2:0] bits are same as the SPSCR.SPSLN[2:0] bits.
- When there is no next transmission data.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- When the next transmission data is written to the transmit buffer (SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 34.31 shows an example of communication end interrupt operation during transmit-receive/transmit master mode.

当接收到的数据在溢出错误状态下没有从移位寄存器复制到接收缓冲区时，在串行传输完成时，SPI确定移位寄存器为空，因此从发送缓冲区到移位寄存器的数据传输被启用.

5.当接收缓冲区满中断程序或使用SPRF标志处理接收缓冲区满中断读取SPDR_HA时，可以读取接收数据。

如果在发送缓冲区保存尚未发送的数据时写入SPDR_HA（SPTEF标志为0），则SPI不会更新发送缓冲区中的数据。写入SPDR_HA时，始终使用发送缓冲区空中断请求或使用SPTEF标志处理发送缓冲区空中断。要使用发送缓冲区空中断，请将SPCR中的SPTIE位设置为1。如果禁用SPI功能（SPCR.SPE位为0），请将SPTIE位设置为0。

当串行传输结束并且接收缓冲区已满（SPRF标志为1）时，SPI不会将数据从移位寄存器复制到接收缓冲区，它会检测到溢出错误（参见第34.3.9节。错误检测）。为防止接收数据溢出错误，请在下一次串行传输结束前使用接收缓冲区满中断请求读取接收数据。要使用SPI接收缓冲区满中断，请将SPCR.SPRIE位设置为1。

ICU中的发送和接收中断或相关的IELSRn.IR标志（其中n是中断向量号）可用于确认发送和接收缓冲区的状态。

类似地，SPTEF和SPRF标志可用于确认发送和接收缓冲区的状态。见第13节，用于中断向量编号的中断控制器单元(ICU)。

34.3.8 通讯结束中断

34.3.8.1 主控模式下的发送-接收发送

在发送-接收主机模式和发送主机模式下满足以下条件时，将产生通信结束中断(SPCI)并将CENDF标志设置为1。CENDF标志的设置时序与IDLNF标志相同。通信结束中断(SPCI)是一个PCLKUSCIx宽度和低电平有效。

- ●当SPSSR.SPCP[2:0]位的值与SPSCR.SPSLN[2:0]位的值相同时。
- ●当没有下一个传输数据时。

即使在CENDF=1后清除SPCR.SPE位，CENDF标志也不会被清除。CENDF标志将在以下两种情况之一被清除。

- ●下一个发送数据写入发送缓冲区（SPTX）时。
- ●当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

图34.31显示了发送-接收发送主机模式期间的通信结束中断操作示例。

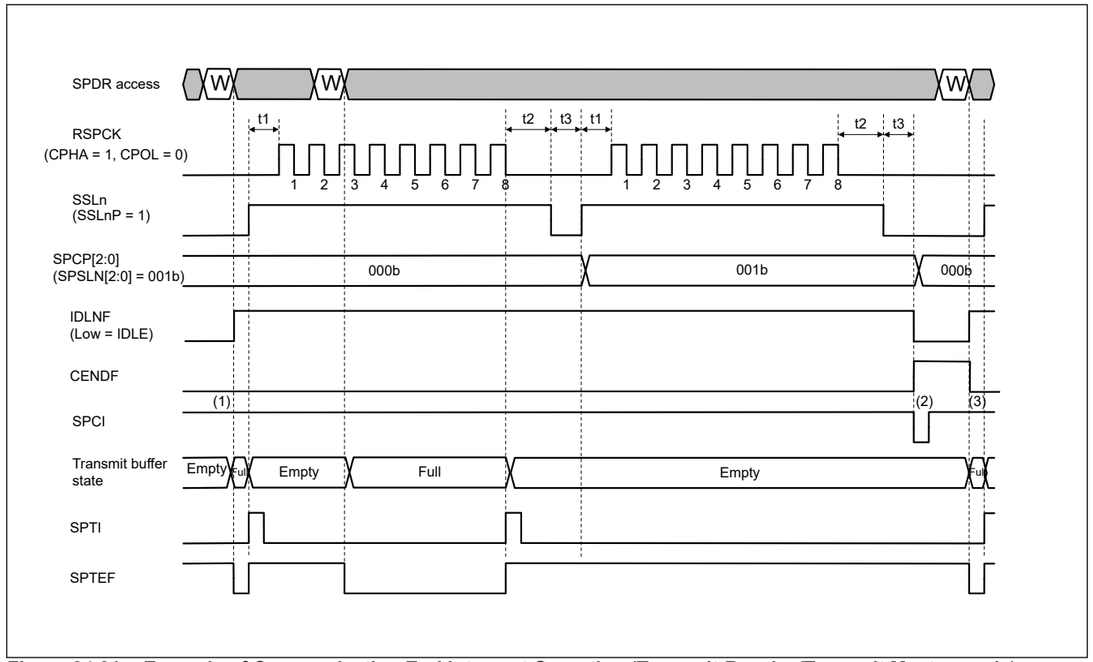


Figure 34.31 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Master mode)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the end of t3 cycle, because the next command is 000b and there is no next transmit data, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

In slave mode operation, the output timing of the communication end interrupt is deferent due to the value of the SPCR.SPMS bit (RSPI mode select bit), and the clear timing of the communication end interrupt is deferent due to the communication mode (transmit-receive or transmit-only or receive-only).

34.3.8.2 Transmit-Receive/Transmit in Slave Mode on SPI Operation (4-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1, when both SPTX buffer and transmit shift buffer are empty in transmit-receive/transmit slave mode on SPI Operation (4-wire). The set timing of the CENDF flag is same as SSL0 negate timing. The communication end interrupt (SPCI) is one PCLKUSCIx width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- When the next transmission data is written to the transmit buffer (SPTX).
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 34.32 shows an example of communication end interrupt operation during transmit-receive/transmit slave mode on SPI operation.

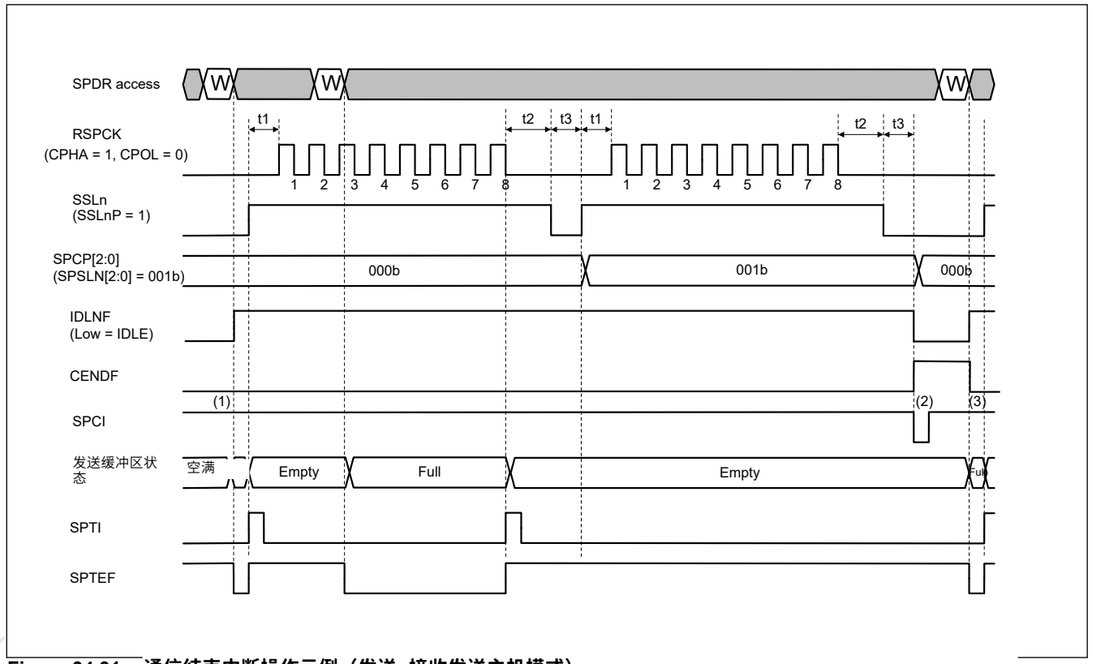


Figure 34.31 通信结束中断操作示例（发送-接收发送主机模式）

1、通信开始前CNEDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.CENDF标志在t3周期结束时为1（通讯结束），因为下一条指令为000b，没有下一条发送数据，当CENDIE位为1时SPCI中断输出。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者，当CENDF标志为1时，如果在读取SPCR后将CENDF标志写入0，则清除CENDF标志。

在从模式操作中，通信结束中断的输出时序是不同的，因为SPCR.SPMS位（RSPI模式选择位），通信结束中断的清除时序因通信模式（发送-接收或仅发送或仅接收）而异。

34.3.8.2 SPI操作（4线）从模式下的发送-接收发送

在SPI操作（4线）的发送-接收发送从模式下，当SPTX缓冲区和发送移位缓冲区都为空时，将产生通信结束中断(SPCI)并将CENDF标志设置为1。CENDF标志的设置时序与SSL0否定时序相同。通信结束中断(SPCI)是一个PCLKUSCIx宽度和低电平有效。

即使在CENDF=1后清除SPCR.SPE位，CENDF标志也不会被清除。CENDF标志将在以下两种情况之一被清除。

- ●下一个发送数据写入发送缓冲区（SPTX）时。
- ●当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

图34.32显示了在发送-接收发送从模式开启期间的通信结束中断操作示例SPI操作。

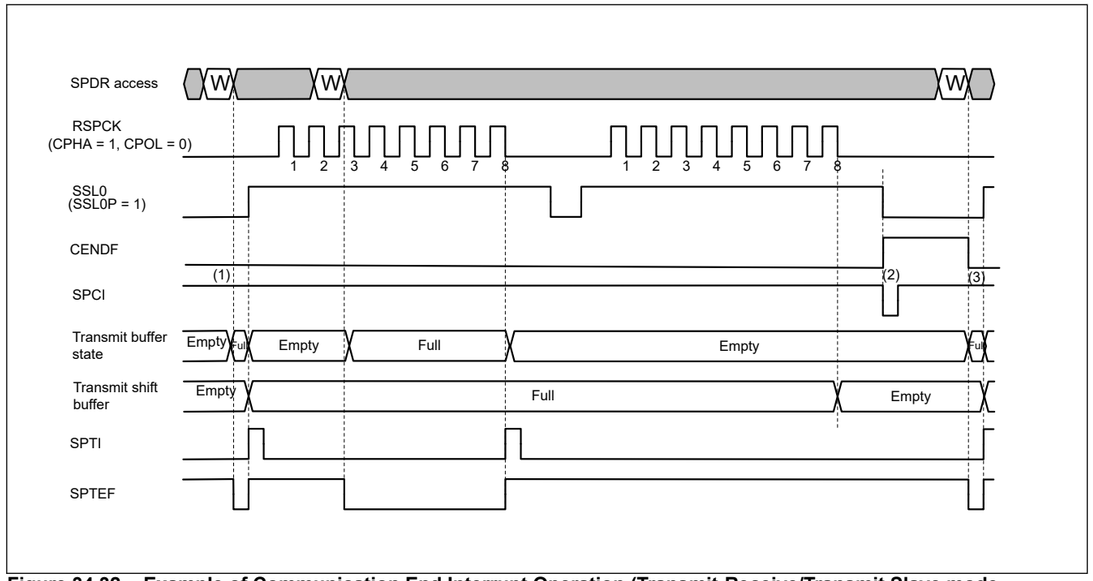


Figure 34.32 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Slave mode on SPI Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the timing of SSL0 negate, when both SPTX buffer and transmit shift buffer are empty, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

34.3.8.3 Receive Only in Slave Mode on SPI Operation (4-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1 at the SSL0 negate timing in receive only slave mode on SPI operation (4-wire). The number of transmission frame is set by the SPDCR.SPFC[1:0]. Then the SSL0 is negated at the last frame transmission end. The communication end interrupt (SPCI) is one PCLKUSCIx width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- The SSL0 assert timing of next transmission.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 34.33 shows an example of communication end interrupt operation during receive only slave mode on SPI operation (4-wire).

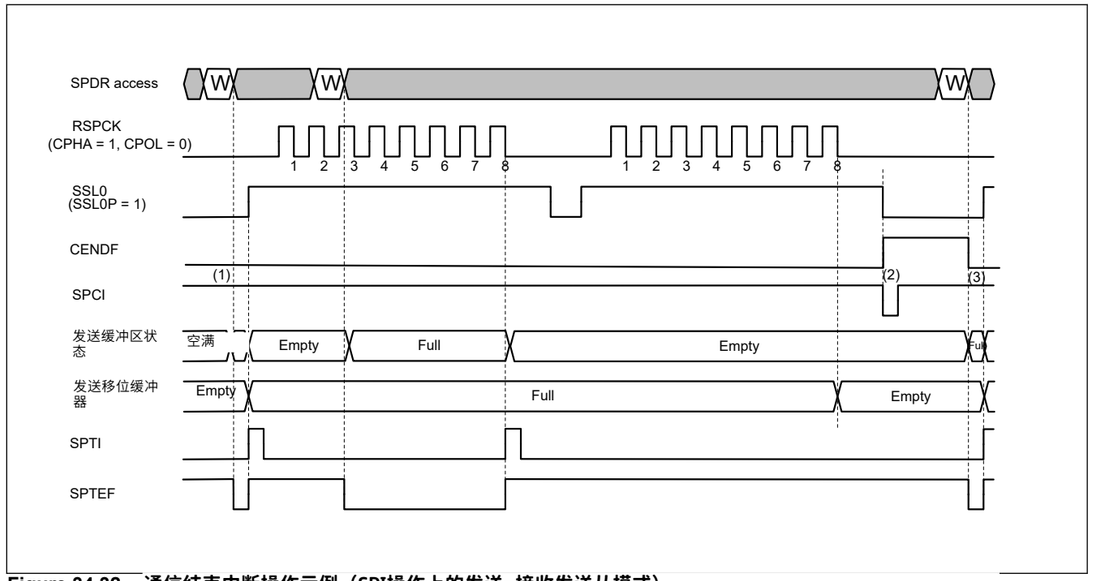


Figure 34.32 通信结束中断操作示例（SPI操作上的发送-接收发送从模式）

1、通信开始前CNEDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.在SSL0否定的时刻，当SPTX缓冲区和发送移位缓冲区都为空时，CENDF标志将为1（通信结束），然后当CENDIE位为1时输出SPCI中断。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者，当CENDF标志为1时，如果在读取SPCR后将CENDF标志写入0，则清除CENDF标志。

34.3.8.3 SPI操作时仅在从模式下接收（4线）

在SPI操作（4线）上仅接收从机模式下，在SSL0否定时序产生通信结束中断(SPCI)并将CENDF标志设置为1。传输帧数由SPDCR.SPFC[1:0]设置。然后在最后一帧传输结束时对SSL0取反。通信结束中断(SPCI)是一个PCLKUSCIx宽度和低电平有效。

即使在CENDF=1后清除SPCR.SPE位，CENDF标志也不会被清除。CENDF标志将在以下两种情况之一被清除。

- SSL0断言下一次传输的时序。
- 当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

图34.33显示了SPI操作（4线）上仅接收从机模式期间的通信结束中断操作示例。

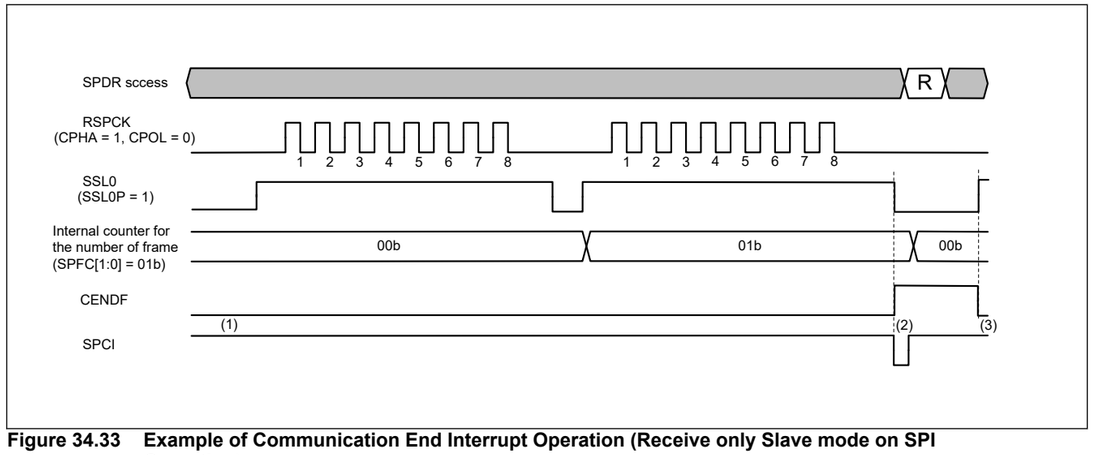


Figure 34.33 Example of Communication End Interrupt Operation (Receive only Slave mode on SPI Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the timing of SSL0 negate, when the last frame transmission ends, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared at the SSL0 assert when the next transmission start. Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

34.3.8.4 Transmit-Receive/Transmit in Slave Mode on Clock Synchronous Operation (3-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1 when both SPTX buffer and transmit shift register are empty in transmit-receive/transmit slave mode on clock synchronous operation (3-wire). The set timing of CENDF flag is same as the last data sampling of the RSPCK (the last odd edge of RSPCK when the SPCMD0.CPHA bit is 0, the last even edge of RSPCK when the SPCMD0.CPHA bit is 1). The communication end interrupt (SPCI) is one PCLKUSCIx width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- The SSL0 assert timing of next transmission.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 34.34 shows an example of communication end interrupt operation during transmig-receive/transmit slave mode on clock synchronous operation (3-wire).

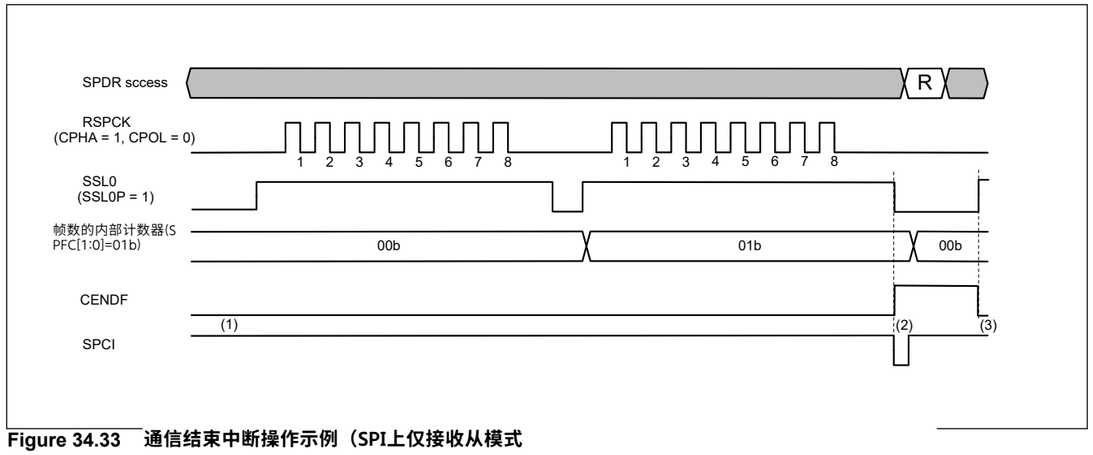


Figure 34.33 通信结束中断操作示例（SPI上仅接收从模式 Operation)

1、通信开始前CNEDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.CENDF标志位在SSL0否定的时刻，即最后一帧传输结束时为1（通信结束），然后当CENDIE位为1时输出SPCI中断。

3.CENDF标志在下一次传输开始时在SSL0断言处被清除。或者，当CENDF标志为1时，如果在读取SPCR后将CENDF标志写入0，则清除CENDF标志。

34.3.8.4 在时钟同步操作（3线）的从模式下发送-接收发送

在时钟同步操作（3线）的发送-接收发送从模式下，当SPTX缓冲器和发送移位寄存器都为空时，产生通信结束中断(SPCI)并将CENDF标志设置为1。CENDF标志的设置时序与RSPCK的最后一次数据采样相同（SPCMD0.CPHA位为0时RSPCK的最后一个奇边沿，SPCMD0.CPHA位为1时RSPCK的最后一个偶边沿）。通信结束中断(SPCI)是一个PCLKUSCIx宽度和低电平有效。

即使在CENDF=1后清除SPCR.SPE位，CENDF标志也不会被清除。CENDF标志将在以下两种情况之一被清除。

- SSL0断言下一次传输的时序。
- 当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

图34.34显示了在时钟同步操作（3线）下发送接收发送从模式期间的通信结束中断操作示例。

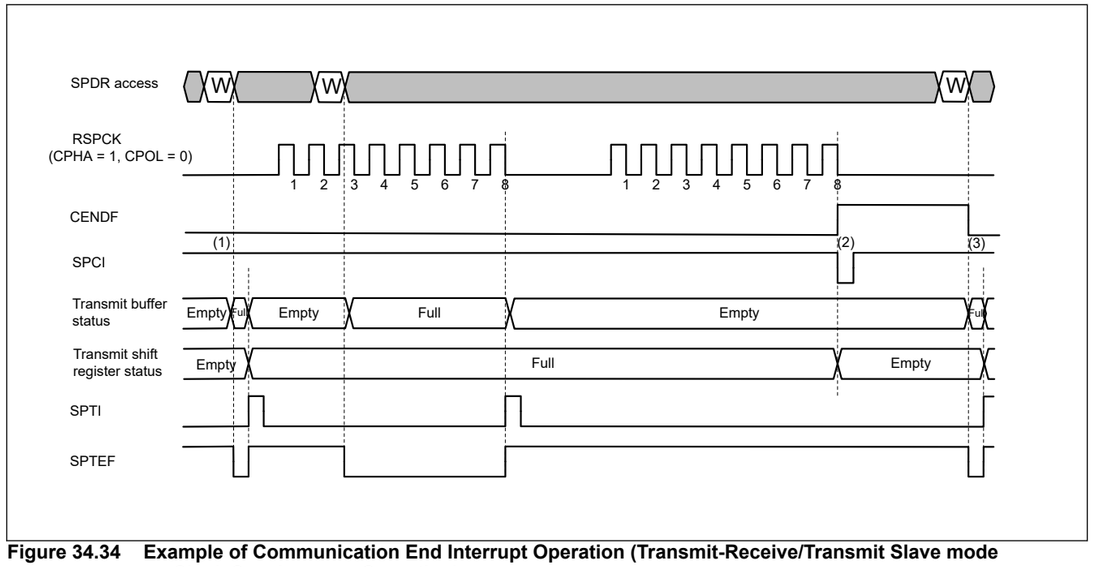


Figure 34.34 Example of Communication End Interrupt Operation (Transmit-Receive/Transmit Slave mode on Clock Synchronous Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the last data sampling timing of RSPCK, when both SPTX buffer and transmit shift buffer are empty, and then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared when the next transmission data is written to the transmit buffer (SPTX). Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

34.3.8.5 Receive Only in Slave Mode on Clock Synchronous Operation (3-wire)

The communication end interrupt (SPCI) is made and the CENDF flag is set to 1 at the last data sampling of the last transmission frame in receive only slave mode on clock synchronous operation (3-wire). The sampling timing is the last odd edge of RSPCK when the SPCMD0.CPHA bit is 0, the last even edge of RSPCK when the SPCMD0.CPHA bit is 1. The number of transmission frame is set by the SPDCR.SPFC[1:0]. The communication end interrupt (SPCI) is one PCLKUSCIx width and low active.

The CENDF flag will not be cleared even if the SPCR.SPE bit is cleared after CENDF = 1. The CENDF flag will be cleared in one of following tow conditions.

- The first edge of RSPCK for next transmission.
- The CENDF flag was written 0 after reading the SPSR when the CENDF flag was 1.

Figure 34.35 shows an example of communication end interrupt operation during receive only slave mode on clock synchronous operation.

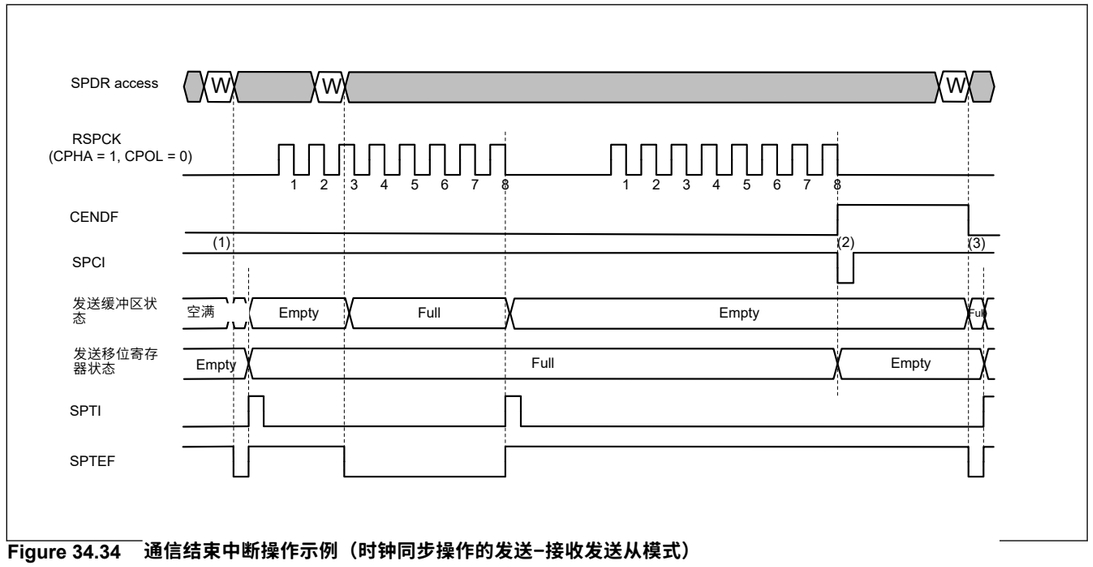


Figure 34.34 通信结束中断操作示例（时钟同步操作的发送–接收发送从模式）

1、通信开始前CNEDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.在RSPCK的最后一个数据采样时序，当SPTX缓冲区和发送移位缓冲区都为空时，CENDF标志为1（通信结束），然后当CENDIE位为1时输出SPCI中断。

3.CENDF标志在下一个发送数据写入发送缓冲区（SPTX）时被清除。或者，当CENDF标志为1时，如果在读取SPCR后将CENDF标志写入0，则清除CENDF标志。

34.3.8.5 在时钟同步操作（3线）上仅在从模式下接收

在时钟同步操作（3线）仅接收从机模式下，在最后一个传输帧的最后一个数据采样时产生通信结束中断(SPCI)并将CENDF标志设置为1。采样时序在SPCMD0.CPHA位为0时为RSPCK的最后一个奇边沿，当SPCMD0.CPHA位为1时为RSPCK的最后一个偶边沿。发送帧数由SPDCR.SPFC[1:0设置]。通信结束中断(SPCI)是一个PCLKUSCIx宽度和低电平有效。

即使在CENDF=1后清除SPCR.SPE位，CENDF标志也不会被清除。CENDF标志将在以下两种情况之一被清除。

- ●RSPCK的第一个边沿用于下一次传输。
- ●当CENDF标志为1时，读取SPSR后CENDF标志被写入0。

图34.35显示了在时钟同步操作下仅接收从机模式期间的通信结束中断操作示例。

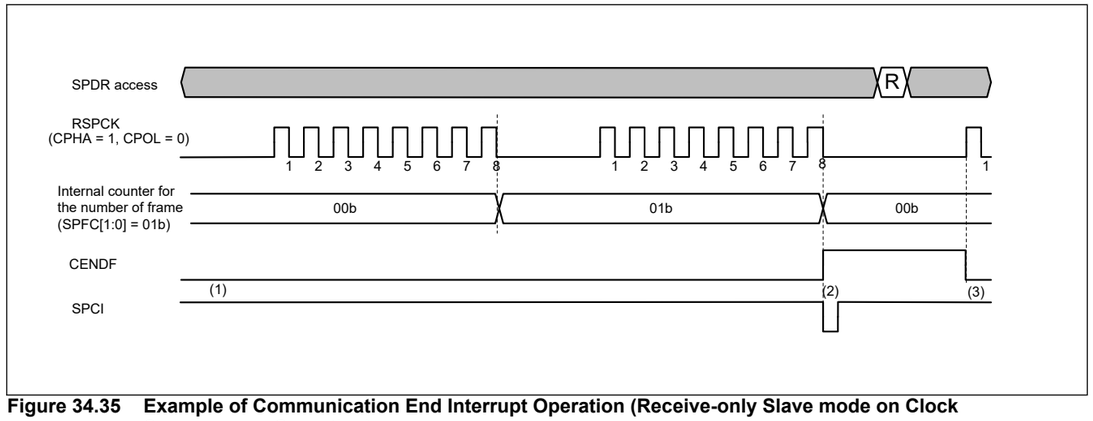


Figure 34.35 Example of Communication End Interrupt Operation (Receive-only Slave mode on Clock Synchronous Operation)

1. The CNEDF flag is 0 and the level of SPCI is 1 before communication start, and these have kept during communication.
2. The CENDF flag will be 1 (Communication End) at the last data sampling timing of RSPCK, when the last frame transmission end. The number of transmission frame is set by the SPDCR.SPFC[1:0]. And then the SPCI interrupt output when the CENDIE bit is 1.
3. The CENDF flag is cleared at the first edge of RSPCK for the next transmission. Or the CENDF flag is cleared if the CENDF flag was written 0 after reading the SPCR when the CENDF flag was 1.

34.3.8.6 Common Operation

In this chapter, the operation common to each mode / area option communication in section 34.3.8.1. Transmit-Receive/ Transmit in Master Mode to section 34.3.8.5. Receive Only in Slave Mode on Clock Synchronous Operation (3-wire) is explained. When the enable of RSPI communication end interrupt (CENDIE) is 0, at the time of communication completion, a flag of communication end (CENDF) is set and an event of communication end (sp_elccend) is output, but no interrupt is output. However, if the enable of communication end interrupt (CENDIE) is set to 1 before clearing the flag of communication end (CENDF) while the enable of RSPI function (SPE) is 1, the communication end interrupt is output.

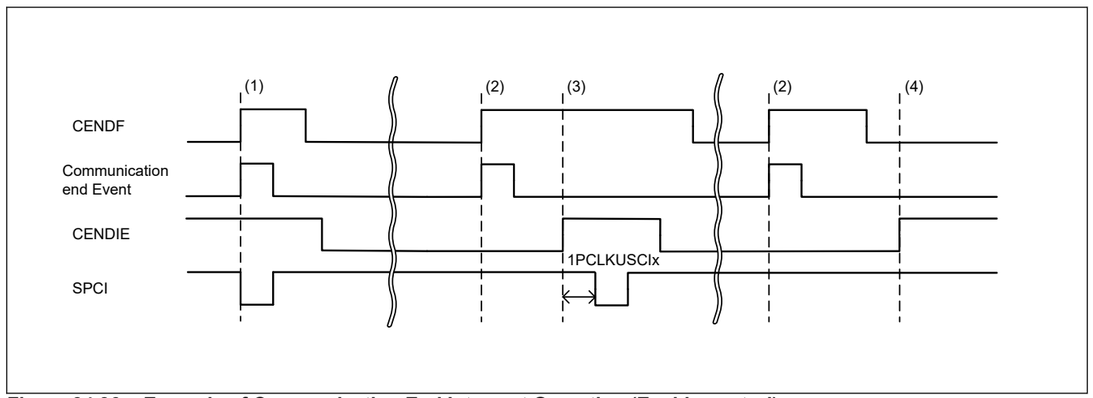


Figure 34.36 Example of Communication End Interrupt Operation (Enable control)

1. When the enable of RSPI communication end interrupt (CENDIE) is 1, at the time of communication completion, the following three are the same timing.
   - A flag of communication end (CENDF)
   - An event of communication end (sp_elccend)
   - The communication end interrupt

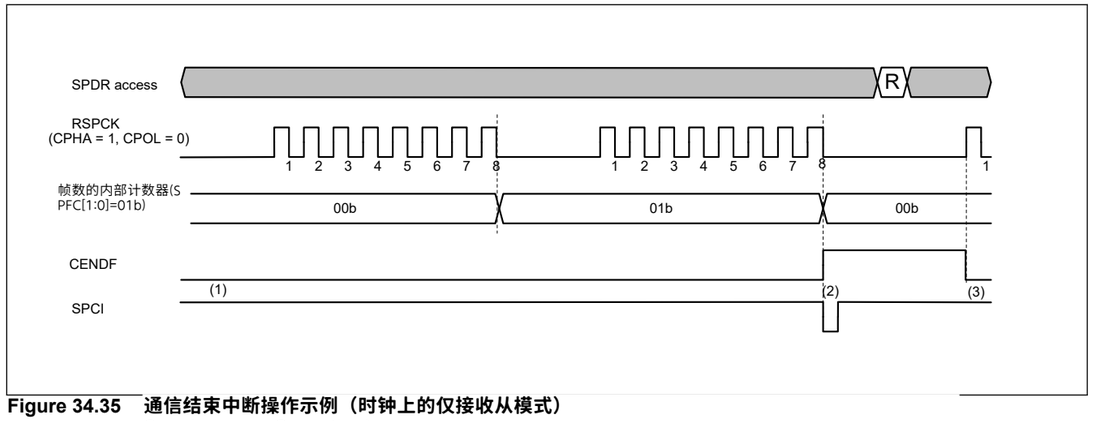


Figure 34.35 通信结束中断操作示例（时钟上的仅接收从模式）

1、通信开始前CNEDF标志为0，SPCI的电平为1，在通信过程中一直保持。

2.CENDF标志位在RSPCK的最后一个数据采样定时为1（通信结束），即最后一帧传输结束。传输帧数由SPDCR.SPFC[1:0]设置。然后在CENDIE位为1时输出SPCI中断。

3.CENDF标志在RSPCK的第一个边沿被清除以进行下一次传输。或者，当CENDF标志为1时，如果在读取SPCR后将CENDF标志写入0，则清除CENDF标志。

34.3.8.6 常用操作

在本章中，34.3.8.1节中的每个模式区域选项通信的通用操作。发送-接收在主模式下发送到第34.3.8.5节。解释了时钟同步操作（3线）时仅在从模式下接收。当RSPI通信结束中断（CENDIE）使能为0时，通信完成时，设置通信结束标志（CENDF）并输出通信结束事件（sp_elccend），但不输出中断。但是，如果在清除通信结束标志（CENDF）之前将通信结束中断（CENDIE）的使能设置为1，而RSPI功能（SPE）的使能为1，则输出通信结束中断。

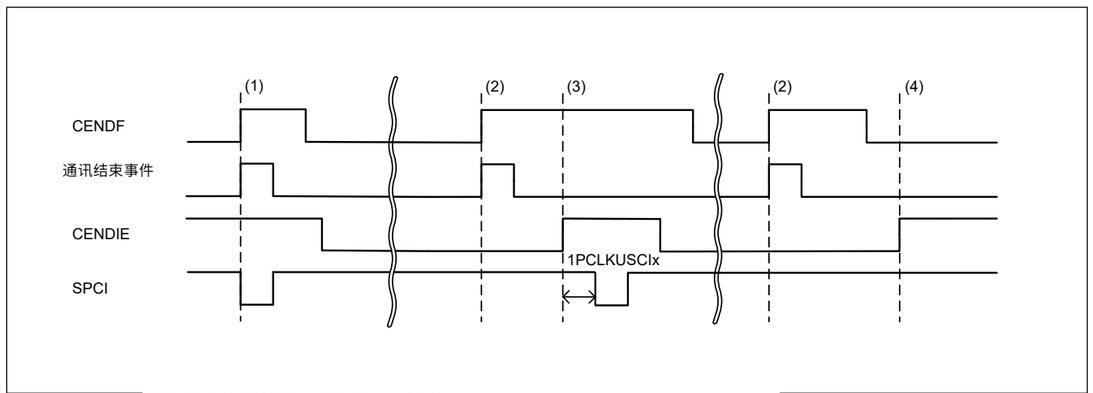


Figure 34.36 通信结束中断操作示例（启用控制）

1、当RSPI通讯结束中断（CENDIE）使能为1时，通讯完成时，以下三个是相同的时序。

- ●通讯结束标志（CENDF）
- ●通信结束事件（sp_elccend）
- ●通讯结束中断

2. When the enable of RSPI communication end interrupt (CENDIE) is 0, at the time of communication completion, the following two are the same timing, but no interrupt.
   - A flag of communication end (CENDF)
   - An event of communication end (sp_elccend)
3. After (2), if the enable of communication end interrupt (CENDIE) is set when the enable of RSPI function (SPE) and the flag of communication end (CENDF) are 1, the communication end interrupt is output after 1 PCLKUSCIx.
4. After (2), even if the enable of communication end interrupt (CENDIE) is set when the enable of RSPI function (SPE) or the flag of communication end (CENDF) is 0, the communication end interrupt is not output.

34.3.9 Error Detection

In normal SPI serial transfers, data written to the transmit buffer of SPDR/SPDR_HA is transmitted, and received data can be read from the receive buffer of SPDR/SPDR_HA. If access is made to SPDR/SPDR_HA, an abnormal transfer might occur, depending on the status of the transmit or receive buffer or the status of the SPI at the beginning or end of serial transfer.

If an abnormal transfer occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 34.10 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 34.10 Relationship between non-normal transfer operations and SPI error detection

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full.	• The contents of the transmit buffer are kept • Write data is missing	None
2	SPDR/SPDR_HA is read when the receive buffer is empty.	The contents of the receive buffer and previously received data are output.	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Underrun error
4	Serial transfer terminates when the receive buffer is full.	• Keeps the contents of the receive buffer • Missing receive data	Overrun error
5	An incorrect parity bit is received during full-duplex synchronous serial communication with the parity function enabled in following mode: • Transmit-receive master mode • Transmit-receive slave mode • Receive-only slave mode	The parity error flag is asserted	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals is stopped • SPI function is disabled	Mode fault error
8	The SSLn0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended • Transmit or receive data is missing • Driving of the MISOn output signal is stopped • SPI function is disabled	Mode fault error

In operation 1 described in Table 34.10, the SPI does not detect an error. To prevent data omission during writes to SPDR/SPDR_HA, the writes to SPDR/SPDR_HA must be executed using a transmit buffer empty interrupt request (when the SPSR.SPTEF flag is 1).

Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR/SPDR_HA read must be executed with an SPI receive buffer full interrupt request (when the SPSR.SPRF flag is 1).

For information on the other errors, see the following sections:

2、当RSPI通讯结束中断（CENDIE）使能为0时，通讯完成时，以下两者时序相同，但无中断。

●通讯结束标志（CENDF）
●通信结束事件（sp_elccend）

3.（2）之后，如果在RSPI功能（SPE）使能和通信结束标志（CENDF）为1的情况下设置通信结束中断（CENDIE）使能，则在1个PCLKUSCIx后输出通信结束中断。

4.(2)后，即使在RSPI功能(SPE)使能或通信结束标志(CENDF)为0时设置通信结束中断(CENDIE)使能，也不输出通信结束中断。

34.3.9 错误检测

在正常的SPI串行传输中，写入到SPDRSPDR_HA的发送缓冲区的数据被发送，接收到的数据可以从SPDRSPDR_HA的接收缓冲区中读取。如果访问SPDRSPDR_HA，可能会发生异常传输，具体取决于发送或接收缓冲区的状态或串行传输开始或结束时SPI的状态。

如果发生异常传输，SPI会将事件检测为欠载错误、溢出错误、奇偶校验错误或模式故障错误。
表34.10列出了非正常传输操作和SPI错误检测功能之间的关系。

Table 34.10 非正常传输操作与SPI错误检测的关系

Operation	发生条件	SPI操作	错误检测
1	SPDRSPDR_HA在发送缓冲区已满时写入。	• 发送缓冲区的内容被保留 • 写入数据丢失	None
2	SPDRSPDR_HA在接收缓冲区为空时读取。	输出接收缓冲区的内容和先前接收的数据。	None
3	当SPI无法传输数据时，串行传输在从模式下启动。	• 串行传输被暂停 • 发送或接收数据丢失 • MIOn输出信号的驱动停止 • SPI功能被禁用	Underrun error
4	当接收缓冲区已满时，串行传输终止。	• 保留接收缓冲区的内容 • 缺少接收数据	溢出错误
5	全双工同步串行通信时接收到错误的奇偶校验位，并在以下模式下启用奇偶校验功能：● 收发主模式 • 收发从模式 • 只接收从模式	奇偶错误标志被置位	奇偶校验错误
6	当串行传输在多主模式下空闲时，SSLn0输入信号被置位。	• 将RSPCKn、MOSIn、SSLn1驱动到SSLn3输出信号停止 • SPI功能被禁用	模式故障错误
7	SSLn0输入信号在多主机模式下的串行传输期间被置位。	• 串行传输被暂停 • 发送或接收数据丢失 • 将RSPCKn、MOSIn、SSLn1驱动到SSLn3输出信号停止 • SPI功能被禁用	模式故障错误
8	SSLn0输入信号在从模式下的串行传输期间被否定。	• 串行传输被暂停 • 发送或接收数据丢失 • MIOn输出信号的驱动停止 • SPI功能被禁用	模式故障错误

在表34.10中描述的操作1中，SPI未检测到错误。防止写入SPDR期间的数据遗漏SPDR_HA，对SPDRSPDR_HA的写入必须使用发送缓冲区空中断请求（当SPSR.SPTEF标志为1)。

同样，SPI不会检测到操作2中的错误。为防止读取无关数据，必须使用SPI接收缓冲区满中断请求（当SPSR.SPRF标志为1时）执行SPDRSPDR_HA读取。

有关其他错误的信息，请参阅以下部分：

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- Underrun error, indicated in operation 3, see section 34.3.9.4. Underrun errors
- Overrun error, indicated in operation 4, see section 34.3.9.1. Overrun errors
- Parity error, indicated in operation 5, see section 34.3.9.2. Parity errors
- Mode fault error, indicated in operations 6 to 8, see section 34.3.9.3. Mode fault errors
- For the transmit and receive interrupts, see section 34.3.7. Transmit Buffer Empty and Receive Buffer Full Interrupts.

34.3.9.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data prior to the error occurrence is retained in the receive buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU reads SPSR with the OVRF flag set to 1.

Figure 34.37 shows an example of operation of the OVRF and SPRF flags. The SPSR and SPDR_HA accesses shown in Figure 34.37 indicate the condition of accesses to the SPSR and SPDR_HA register, where W denotes a write cycle, and R a read cycle. In this example, the SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

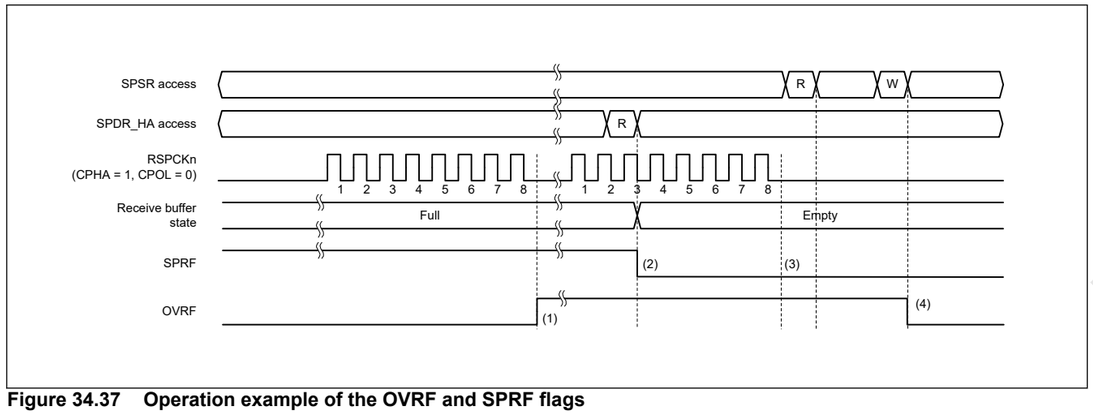

Figure 34.37 Operation example of the OVRF and SPRF flags

The operation of the flags at timings (1) to (4) in Figure 34.37 is as follows:

1. If a serial transfer terminates with the SPRF flag set to 1 (receive buffer full), the SPI detects an overrun error, and sets the OVRF flag to 1. The SPI does not copy the data in the shift register to the receive buffer. Even when the SPPE bit is 1, parity errors are not detected.
2. When SPDR/SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The receive buffer becoming empty does not set the OVRF flag to 0.
3. If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag does not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In an overrun error state when the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.
4. If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag clears is set to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, you must ensure that overrun errors are detected early, for example by reading SPSR immediately after SPDR/SPDR_HA/SPDR_BY is read.

If an overrun error occurs and the OVRF flag sets to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

●欠载错误，在操作3中指示，请参阅第34.3.9.4节。欠载错误

●超限错误，在操作4中显示，参见第34.3.9.1节。溢出错误

●奇偶校验错误，在操作5中指示，参见第34.3.9.2节。奇偶校验错误

●模式故障错误，在操作6到8中指示，参见第34.3.9.3节。模式故障错误

●关于发送和接收中断，请参见第34.3.7节。发送缓冲区空和接收缓冲区满中断。

34.3.9.1 溢出错误

如果在SPDRSPDR_HA的接收缓冲区已满时串行传输结束，则SPI检测到溢出错误并设置SPSR.OVRF标志为1。当OVRF标志为1时，SPI不会将数据从移位寄存器复制到接收缓冲区，因此错误发生之前的数据会保留在接收缓冲区中。要将OVRF标志设置为0，请在CPU读取OVRF标志设置为1的SPSR后将0写入OVRF标志。

图34.37显示了OVRF和SPRF标志的操作示例。SPSR和SPDR_HA访问显示在图34.37表示访问SPSR和SPDR_HA寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCMDm.CPHA位为1且SPCMDm.CPOL位为0时，SPI执行8位串行传输。波形中为RSPCKn给出的数字表示RSPCK周期数，例如传输的次数位。

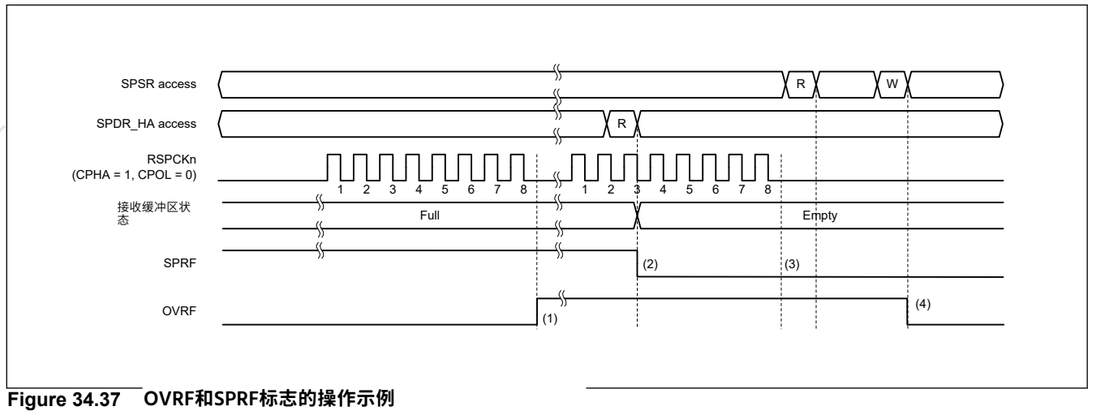

Figure 34.37 OVRF和SPRF标志的操作示例

图34.37中时间(1)到(4)的标志操作如下：

1.如果串行传输终止且SPRF标志设置为1（接收缓冲区已满），则SPI检测到溢出错误，并将OVRF标志设置为1。SPI不会将移位寄存器中的数据复制到接收缓冲区.即使SPPE位为1，也不会检测到奇偶校验错误。

2.读取SPDRSPDR_HA时，SPI输出接收缓冲区中的数据。然后SPRF标志设置为0。接收缓冲区变空不会将OVRF标志设置为0。

3.如果串行传输结束时OVRF标志设置为1（发生溢出错误），则SPI不会将移位寄存器中的数据复制到接收缓冲区（SPRF标志不设置为1）。不产生接收缓冲区满中断。即使SPPE位为1，也不会检测到奇偶校验错误。在SPI未将接收到的数据从移位寄存器复制到接收缓冲区的溢出错误状态下，在串行传输终止时，SPI确定移位寄存器为空。这使数据能够从发送缓冲器传输到移位寄存器。

4.如果在OVRF标志为1时读取SPSR后向OVRF标志写入0，则OVRF标志清除设置为0。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查溢出的发生。
执行串行传输时，必须确保及早检测到溢出错误，例如在读取SPDRSPDR_HASPDR_BY后立即读取SPSR。

如果发生溢出错误并且OVRF标志设置为1，则在OVRF标志设置为0之前无法执行正常接收操作。

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When the RSPCK auto-stop function is enabled (SPCR2.SCKASE = 1) in master mode, an overrun error does not occur. Figure 34.38 and Figure 34.39 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

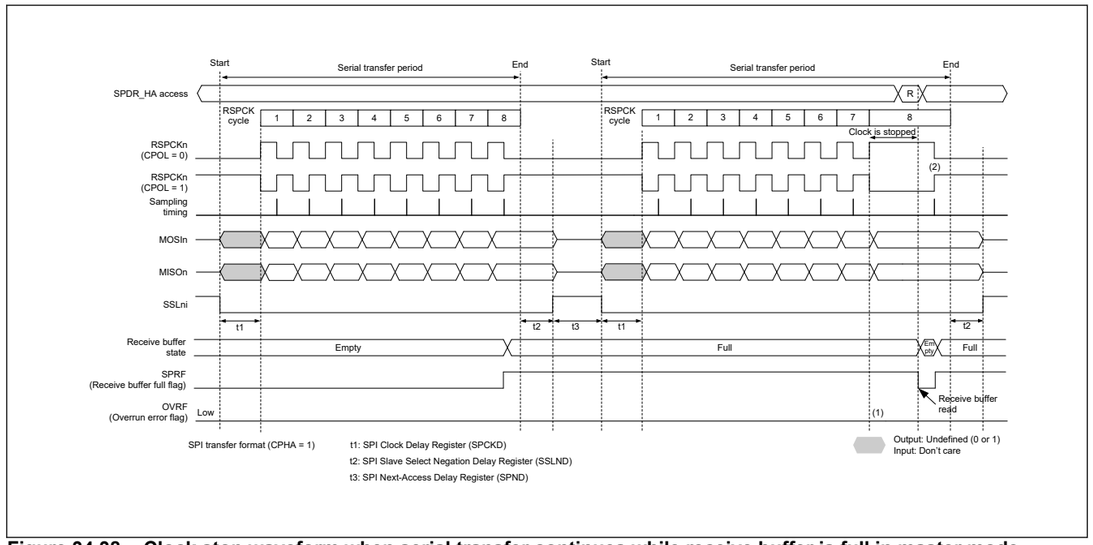

Figure 34.38 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 1)

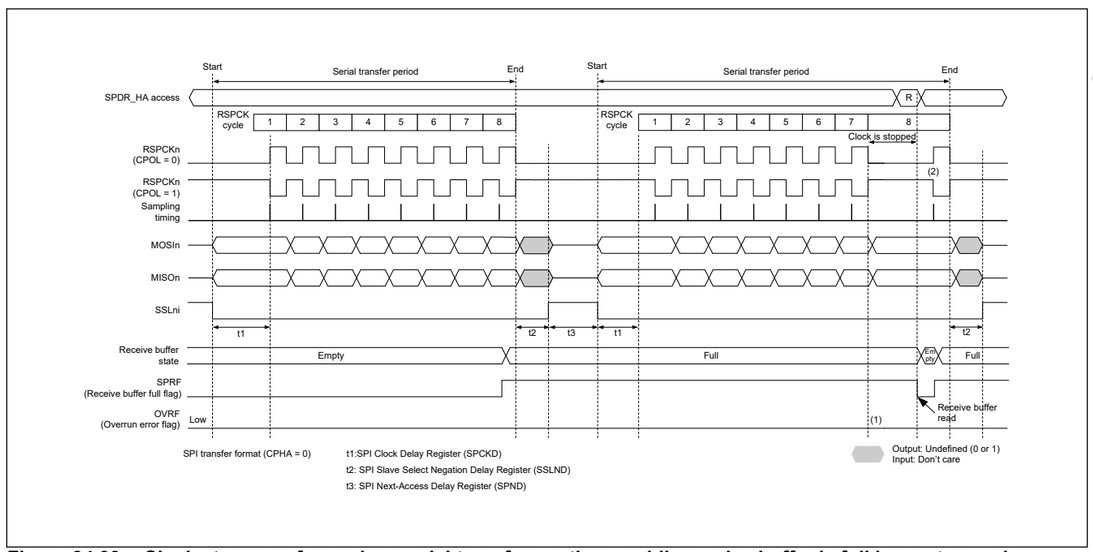

Figure 34.39 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 0)

The operation of the flags at timings (1) and (2) in Figure 34.38 and Figure 34.39 is as follows:

1. When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.
2. If SPDR/SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after the SPSR.SPRF flag is set to 0).

在主机模式下启用RSPCK自动停止功能（SPCR2.SCKASE=1）时，不会发生溢出错误。
图34.38和图34.39显示了在主机模式下接收缓冲器已满时串行传输继续时的时钟停止波形。

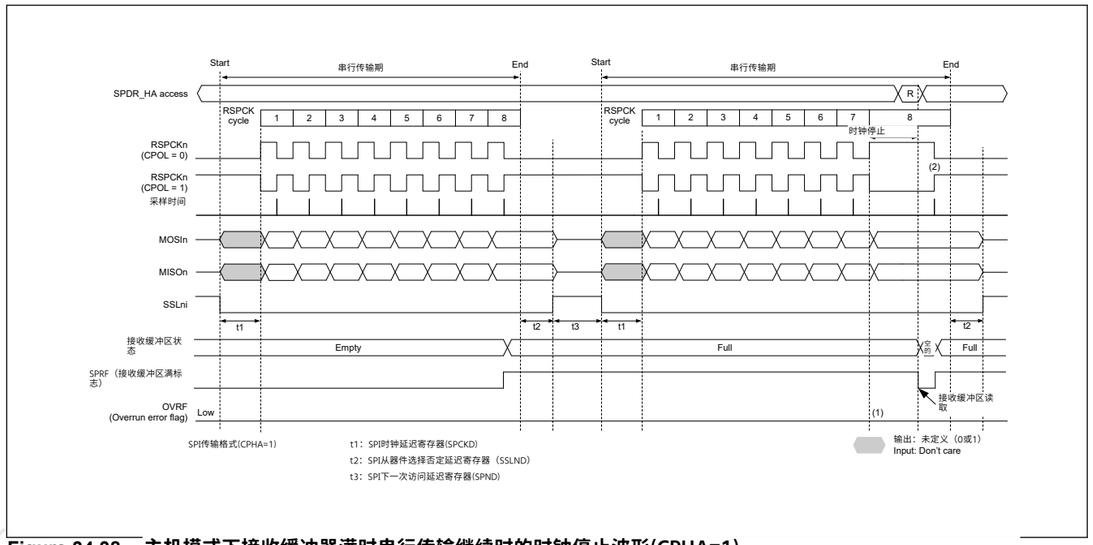

Figure 34.38 主机模式下接收缓冲器满时串行传输继续时的时钟停止波形(CPHA=1)

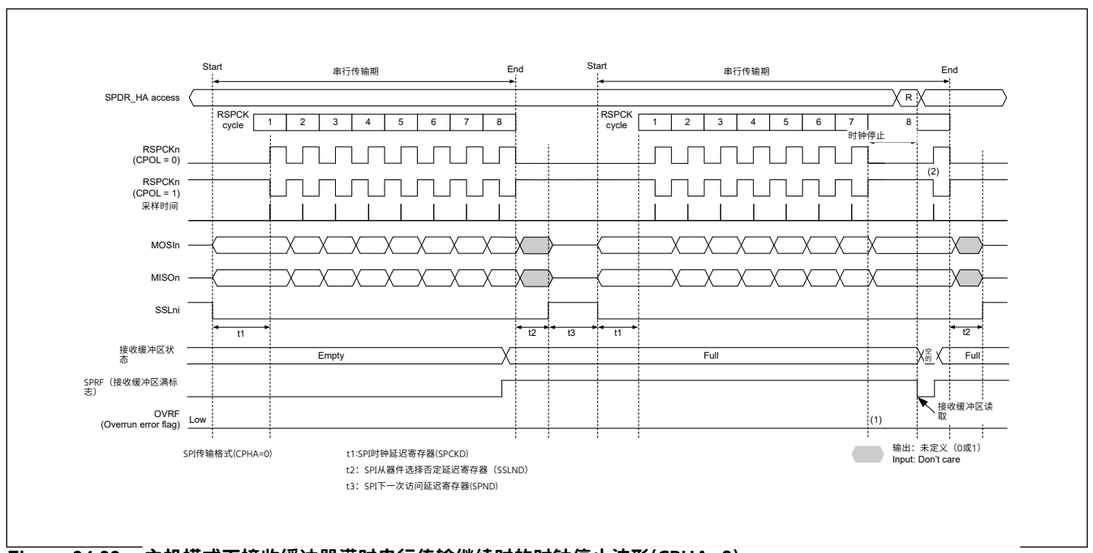

Figure 34.39 主机模式下接收缓冲器满时串行传输继续时的时钟停止波形(CPHA=0)

图34.38和图34.39中时序（1）和（2）的标志操作如下：

1.当接收缓冲区已满时，不会发生溢出错误，因为RSPCK时钟已停止。

2.如果在时钟停止时读取SPDRSPDR_HA，则可以读取接收缓冲区中的数据。RSPCK时钟在读取接收缓冲区后重新启动（在SPSR.SPRF标志设置为0后）。

Overrun error does not occur when RSPCK automatic stop function is enabled for transfer with no delay of between frames during burst transfer in master mode. Figure 34.40 and Figure 34.41 show the clock stop waveform, when there is no delay between frames at burst transfer and the serial transfer continues in the reception buffer full state.

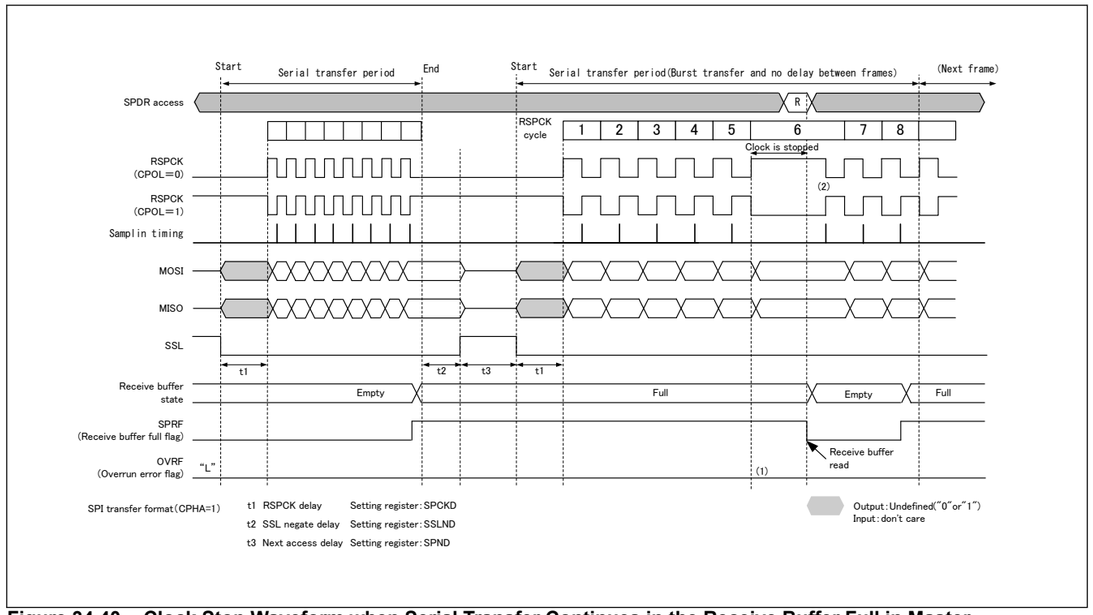

Figure 34.40 Clock Stop Waveform when Serial Transfer Continues in the Receive Buffer Full in Master Mode (at burst transfer and no delay between frames CPHA = 1)

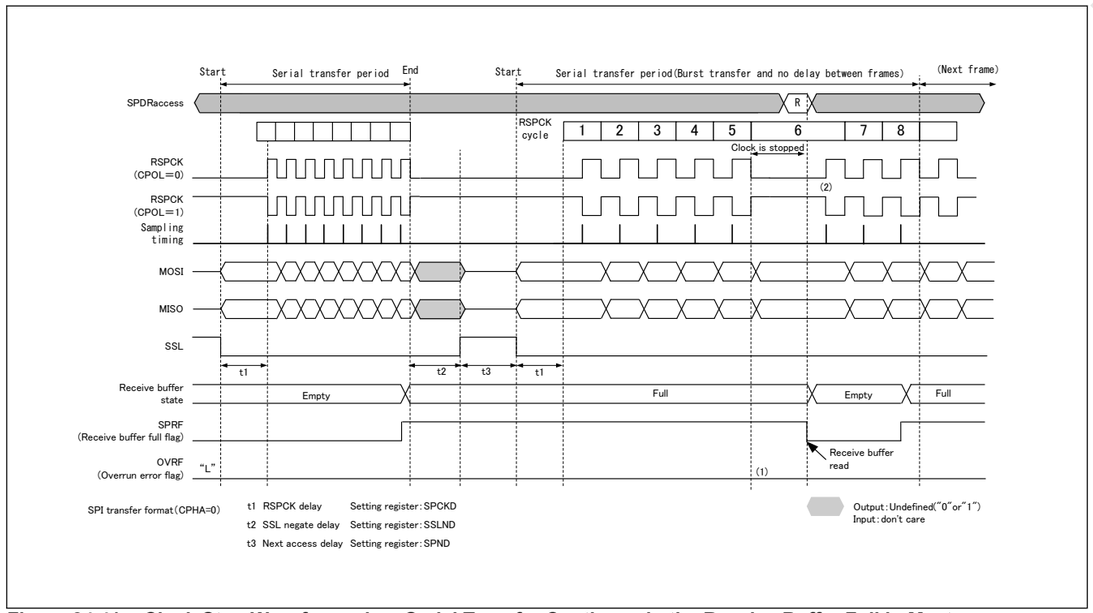

Figure 34.41 Clock Stop Waveform when Serial Transfer Continues in the Receive Buffer Full in Master Mode (at burst transfer and no delay between frames CPHA = 0)

The following describes operation of flags at timings (1) and (2) in the figure above.

在主模式下的突发传输期间，如果传输启用RSPCK自动停止功能且帧之间没有延迟，则不会发生溢出错误。图34.40和图34.41显示了时钟停止波形，当突发传输的帧之间没有延迟并且串行传输在接收缓冲器满状态下继续时。

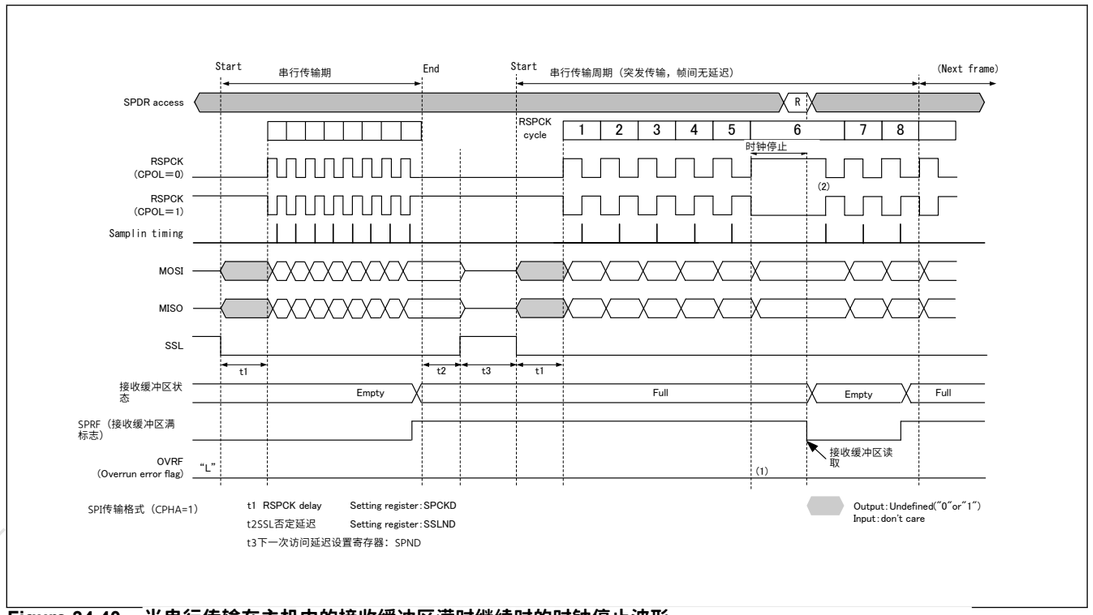

Figure 34.40 当串行传输在主机中的接收缓冲区满时继续时的时钟停止波形模式（突发传输且帧之间无延迟CPHA=1）

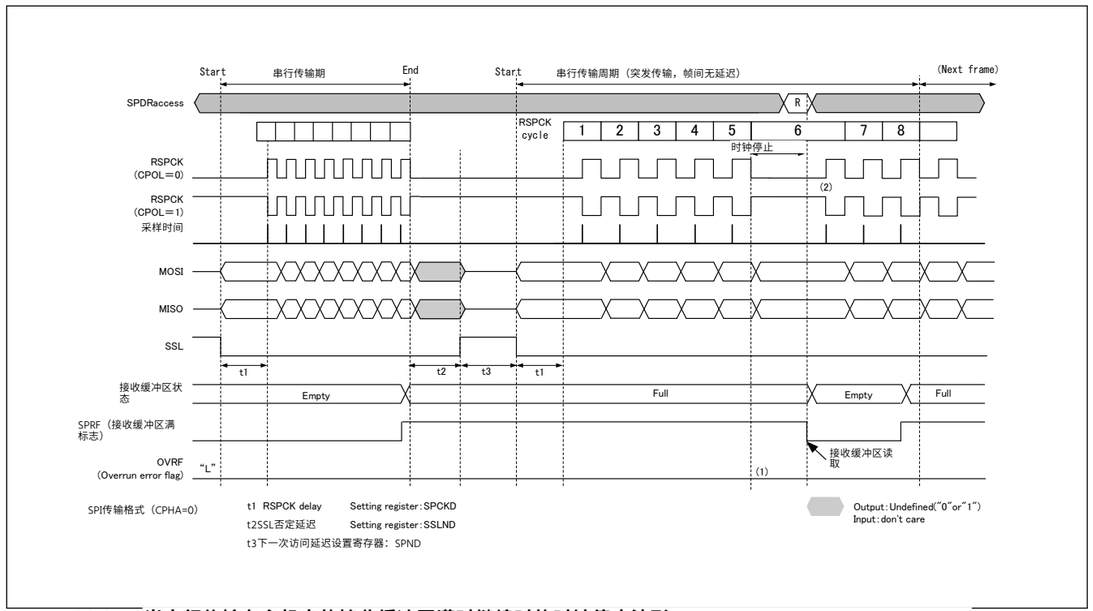

Figure 34.41 当串行传输在主机中的接收缓冲区满时继续时的时钟停止波形模式（突发传输且帧之间无延迟CPHA=0）

下面描述在上图中的时间(1)和(2)的标志的操作。

1. While the receive buffer is full, the RSPCK clock is deactivated and no overrun error occurs.
2. Receive buffer data can be read by reading SPDR during clock stop. After the receive buffer data has been read (after the SPSR.SPRF flag has been cleared to 0), the RSPCK clock restarts.

34.3.9.2 Parity errors

When full-duplex synchronous serial communications is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, when serial transfer ends, the SPI checks whether there are parity errors. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 34.42 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 34.42 indicates the condition of access to the register, where W denotes a write cycle, and R a read cycle. In this example, full-duplex serial communication is performed while the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, such as the number of transferred bits.

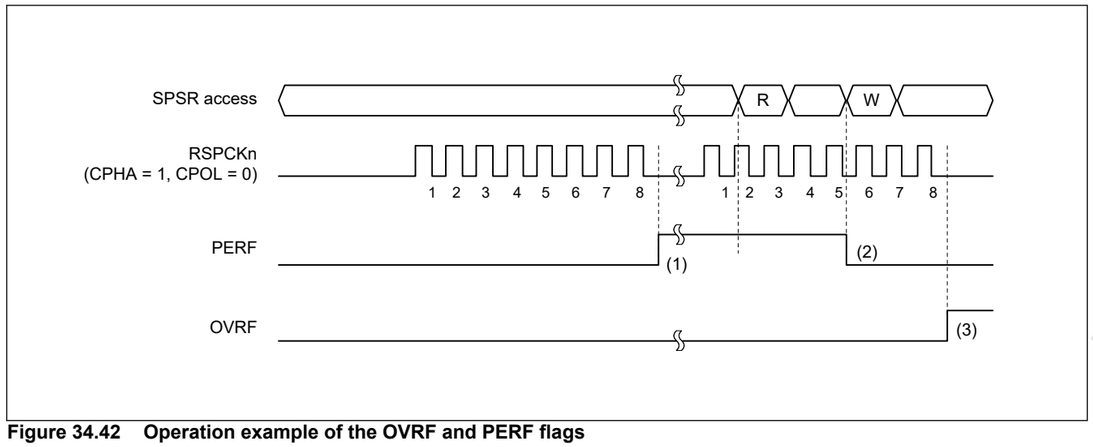

Figure 34.42 Operation example of the OVRF and PERF flags

The operation of the flags at timings (1) to (3) in Figure 34.42 is as follows:

1. If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies the data in the shift register to the receive buffer. The SPI checks the received data at this time and sets the PERF flag to 1 if a parity error is detected.
2. If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.
3. When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

Parity errors can be checked for by either reading the SPSR register or using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, such checks are required to ensure early detection of parity errors. When the SPI is used in master mode, the pointer value to the SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits (Only SPI0).

34.3.9.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1. On detecting the mode fault error, the SPI copies the value of the pointer to SPCMDm to the SPDCR.SPFC[1:0] bits. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

1.当接收缓冲器已满时，RSPCK时钟被停用，不会发生溢出错误。

2.在时钟停止时，可以通过读取SPDR来读取接收缓冲数据。读取接收缓冲区数据后（在SPSR.SPRF标志被清除为0后），RSPCK时钟重新启动。

34.3.9.2 奇偶校验错误

当SPCR.TXMD位设置为0且SPCR2.SPPE位设置为1进行全双工同步串行通信时，串行传输结束时，SPI会检查是否有奇偶校验错误。在检测到接收数据中的奇偶校验错误时，SPI将SPSR.PERF标志设置为1。因为当SPSR.OVRF标志设置为1时，SPI不会将移位寄存器中的数据复制到接收缓冲区，所以奇偶校验错误检测不针对接收到的数据执行。要将PERF标志设置为0，请在读取SPSR寄存器并将PERF标志设置为1后将0写入PERF标志。

图34.42显示了OVRF和PERF标志的操作示例。图34.42所示的SPSR访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCR2.SPPE位为1时执行全双工串行通信。当SPCMDm.CPHA位为1且SPCMDm.CPOL位为0时，SPI执行8位串行传输。波形表示RSPCK周期数，例如传输的位数。

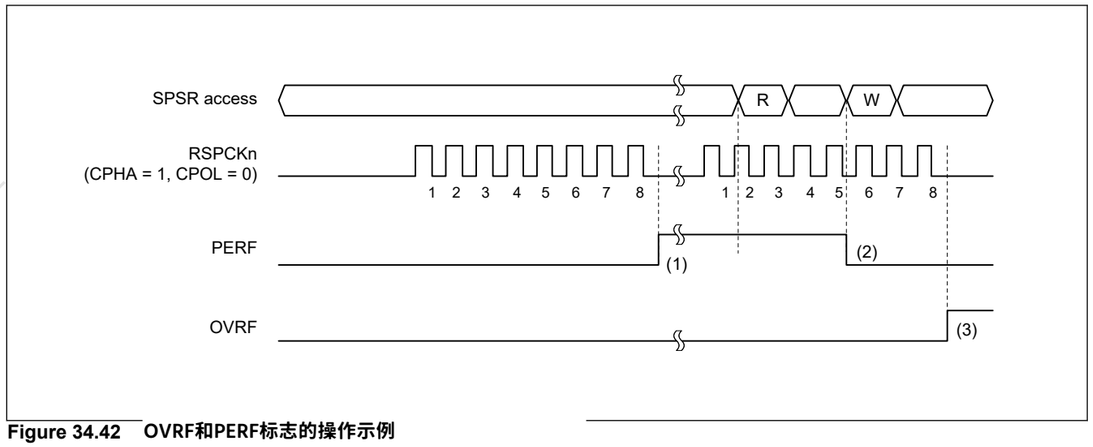

Figure 34.42 OVRF和PERF标志的操作示例

图34.42中时间(1)到(3)的标志操作如下：

1.如果串行传输终止且SPI未检测到溢出错误，则SPI将移位寄存器中的数据复制到接收缓冲区。此时SPI会检查接收到的数据，如果检测到奇偶校验错误，则将PERF标志设置为1。

2.如果在PERF标志为1时读取SPSR寄存器后将0写入PERF标志，则将PERF标志设置为0。

3.当SPI检测到溢出错误并终止串行传输时，移位寄存器中的数据不会复制到接收缓冲区。此时SPI不执行奇偶校验错误检测。

可以通过读取SPSR寄存器或使用SPI错误中断并读取SPSR寄存器来检查奇偶校验错误。在执行串行传输时，需要进行此类检查以确保及早发现奇偶校验错误。当SPI用于主机模式时，可以通过读取SPSSR.SPECM[2:0]位（仅SPI0）来检查发生错误时指向SPCMDm寄存器的指针值。

34.3.9.3 模式故障错误

当SPCR.MSTR位为1、SPCR.SPMS位为0、SPCR.MODFEN位为1时，SPI工作在多主机模式。如果在多主机模式下SPI的SSLn0输入信号输入有效电平-主模式，无论串行传输的状态如何，SPI都会检测到模式故障错误，并将SPSR.MODF标志设置为1。在检测到模式故障错误时，SPI将指向SPCMDm的指针的值复制到SPDCR.SPFC[1:0]位。SSLn0信号的有效电平由SSLP.SSL0P位决定。

当MSTR位为0时，SPI工作在从机模式。如果从机模式下SPI的MODFEN位为1，SPMS位为0，并且在串行传输期间（从驱动有效数据开始开始到获取最终有效数据的时间）。

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On detecting a mode fault error, the SPI stops the driving of the output signals and clears the SPCR.SPE bit to 0 (see section 34.3.10. Initializing the SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting mode-fault errors without using the SPI error interrupt requires polling of SPSR. When using the SPI in master mode, the value of the pointer to the SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

34.3.9.4 Underrun errors

While the SPI is operating in slave mode (SPCR.MSTR bit = 0) and the Extended Communication Mode Select bit (ETXMD) in the SPI Control Register 3 (SPCR3) is set to 0, if serial transfer is started before transmit data output is ready with the SPCR.SPE bit set to 1 (SPI function enabled), the SPI detects an underrun error and sets the SPSR.MODF and SPSR.UDRF flags to 1.

On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 34.3.10. Initializing the SPI).

The occurrence of underrun errors can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. Detecting underrun errors without using the SPI error interrupt requires polling of SPSR.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be set to 0.

34.3.10 Initializing the SPI

If 0 is written to the SPCR.SPE bit or if the SPI sets the SPE bit to 0 because it detected a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset is generated, the SPI initializes all of the module functions. This section describes initialization by clearing of the SPCR.SPE bit and by a system reset.

34.3.10.1 Initialization by clearing of the SPCR.SPE bit

When the SPCR.SPE bit is set to 0, the SPI initializes by:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the SPI
- Initializing the transmit buffer of the SPI (the SPSR.STEF flag sets to 1)

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use prior to initialization when the SPE bit is set to 1 again.

The SPSR.CENDF, SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized, and the value of the SPI Sequence Status Register (SPSSR) is not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the communication completion status and the error status during an SPI transfer.

The transmit buffer is initialized to an empty state (the SPSR.SPTEF flag sets to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit simultaneously while writing 0 to the SPE bit.

34.3.10.2 Initialization by system reset

A system reset completely initializes the SPI by initializing all SPI control bits, status bits, and data registers, in addition to meeting the requirements described in section 34.3.10.1. Initialization by clearing of the SPCR.SPE bit.

在检测到模式故障错误时，SPI停止驱动输出信号并将SPCR.SPE位清零（参见第34.3.10节。初始化SPI）。对于多主机配置，检测到模式故障错误用于停止驱动输出信号和SPI功能，从而释放主机。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查模式故障错误的发生。在不使用SPI错误中断的情况下检测模式错误需要轮询SPSR。在主模式下使用SPI时，可以通过读取SPSSR.SPECM[2:0]位来检查发生错误时指向SPCMDm寄存器的指针的值。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到模式故障错误后启用SPI功能，MODF标志必须设置为0。

34.3.9.4 Underrun errors

当SPI工作在从机模式（SPCR.MSTR位=0）并且SPI控制寄存器3（SPCR3）中的扩展通信模式选择位（ETXMD）设置为0时，如果串行传输在发送数据输出之前开始准备好将SPCR.SPE位设置为1（启用SPI功能），SPI检测到欠载错误并将SPSR.MODF和SPSR.UDRF标志设置为1。

检测到欠载错误时，SPI停止驱动输出信号并将SPCR.SPE位清零（参见第34.3.10节。初始化SPI）。

可以通过读取SPSR或使用SPI错误中断并读取
SPSR。在不使用SPI错误中断的情况下检测欠载错误需要轮询SPSR。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到欠载错误后启用SPI功能，MODF标志必须设置为0。

34.3.10 初始化SPI

如果将0写入SPCR.SPE位，或者如果SPI由于检测到模式故障错误或欠载错误而将SPE位设置为0，则SPI将禁用SPI功能并初始化一些模块功能。当产生系统复位时，SPI初始化所有模块功能。本节介绍通过清除SPCR.SPE位和系统复位进行的初始化。

34.3.10.1 通过清除SPCR.SPE位进行初始化

当SPCR.SPE位设置为0时，SPI通过以下方式初始化：

●暂停任何正在执行的串行传输

●从机模式下停止驱动输出信号（Hi-Z）

●初始化SPI的内部状态

●初始化SPI的发送缓冲区（SPSR.STEF标志设置为1）

通过清除SPE位进行的初始化不会初始化SPI的控制位。因此，当SPE位再次设置为1时，SPI可以在初始化之前以相同的传输模式启动。

SPSR.CENDF、SPSR.SPRF、SPSR.OVRF、SPSR.MODF、SPSR.PERF和SPSR.UDRF标志未初始化，SPI序列状态寄存器(SPSSR)的值未初始化。因此，即使在SPI初始化之后，也可以从接收缓冲区读取数据，以检查SPI传输期间的通信完成状态和错误状态。

发送缓冲区初始化为空状态（SPSR.SPTEF标志设置为1）。因此，如果SPCR.SPTIE位在SPI初始化后设置为1，则会产生发送缓冲区空中断。要在SPI初始化时禁用任何发送缓冲区空中断，请同时将0写入SPTIE位，同时将0写入SPE位。

34.3.10.2 通过系统复位初始化

除了满足第34.3.10.1节中描述的要求外，系统复位还通过初始化所有SPI控制位、状态位和数据寄存器来完全初始化SPI。通过清除SPCR.SPE位进行初始化。

34.3.11 SPI Operation

34.3.11.1 Master mode operation

The only difference between single- and multi-master mode operation is the use of mode fault error detection (see section 34.3.9. Error Detection). In single-master mode, the SPI does not detect mode fault errors whereas in multi-master mode, it does. This section explains operations that are common to both modes.

(1) Starting a serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) with the SPI transmit buffer empty, data for the next transfer is not set, and the SPSR.STEF flag is 0. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA/SPDR_BY, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full. On termination of the serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SSLP register settings. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

(2) Terminating a serial transfer

Regardless of the SPCMDm.CPHA bit setting, the SPI terminates the serial transfer after transmitting an RSPCKn edge associated with the final sampling timing. If free space is available in the receive buffer (SPRX) (the SPSR.SPRF flag is 0), on termination of the serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit settings. The polarity of the SSLni output pin depends on the SSLP register settings. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following items are set in the SPCMDm register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced

SPBR holds some of the bit rate settings, including SPCKD (SPI clock delay), SSLND (SSL negation delay), and SPND (next-access delay).

Based on the sequence length assigned in SPSCR, the SPI makes up a sequence comprised of a part or all of the SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command in the sequence, the SPI sets the pointer to SPCMD0, and in this way the sequence is executed repeatedly.

34.3.11 SPI操作

34.3.11.1 主模式操作

单主机模式和多主机模式操作之间的唯一区别是使用模式故障错误检测（请参阅第34.3.9节。错误检测）。在单主机模式下，SPI不检测模式故障错误，而在多主机模式下，它可以。本节介绍两种模式共有的操作。

(1) 开始串行传输

当数据写入SPI数据寄存器(SPDRSPDR_HA)且SPI发送缓冲区为空、未设置下一次传输的数据且SPSR.STEF标志为0时，SPI更新发送缓冲区(SPTX)中的数据。当SPDCR.SPFC[1:0]位设置的帧数写入SPDRSPDR_HASPDR_BY后移位寄存器为空时，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。在将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为已满。在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(2) 终止串行传输

无论SPMDm.CPHA位设置如何，SPI在发送与最终采样时序相关的RSPCKn边沿后终止串行传输。如果接收缓冲区(SPRX)中有可用空间（SPSR.SPRF标志为0），则在串行传输终止时，SPI将数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主模式下，SPI数据长度取决于SPMDm.SPB[3:0]位设置。SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(3) 顺序控制

主机模式中使用的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器确定。

SPSCR寄存器确定由SPI在主模式下执行的串行传输的序列配置。
在SPCMDm寄存器中设置以下项目：

●SSLni管脚输出信号值

- MSB- or LSB-first

●数据长度

●一些比特率设置

●RSPCK极性和相位

●是否引用SPCKD

●是否引用SSLND

●是否引用SPND

SPBR保存一些比特率设置，包括SPCKD（SPI时钟延迟）、SSLND（SSL否定延迟）和SPND（下一次访问延迟）。

根据在SPSCR中分配的序列长度，SPI组成一个由部分或全部SPMDm寄存器组成的序列。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPSSR.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI加载指向SPCMD0中命令的指针，并在串行传输开始时将SPCMD0设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于序列中最终命令的串行传输后，SPI将指针设置为

SPCMD0，并以这种方式重复执行序列。

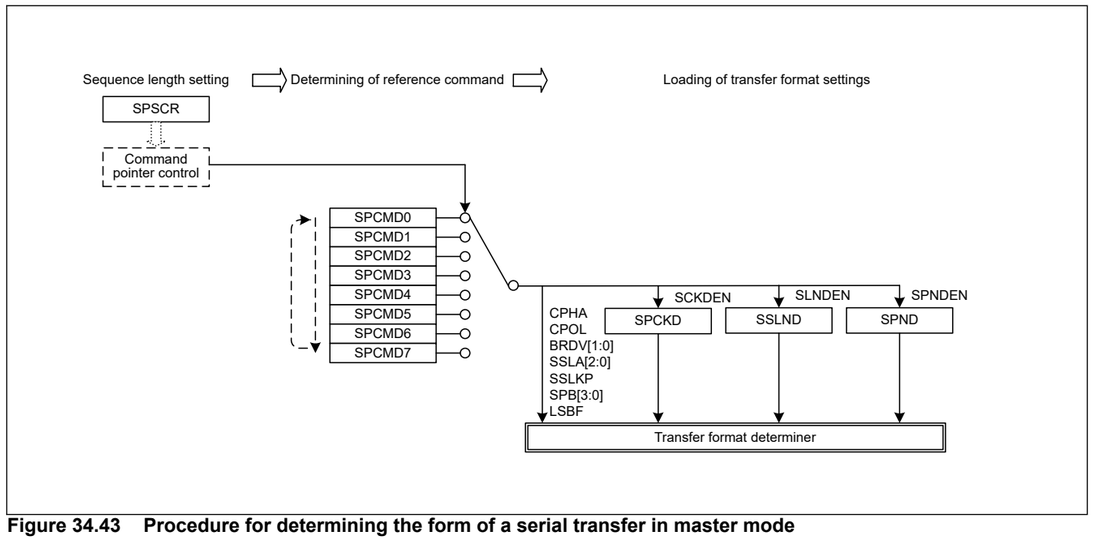

Figure 34.43 Procedure for determining the form of a serial transfer in master mode

In this section, a frame is the combination of the data in SPDR/SPDR_HA and the settings in SPCMDm.

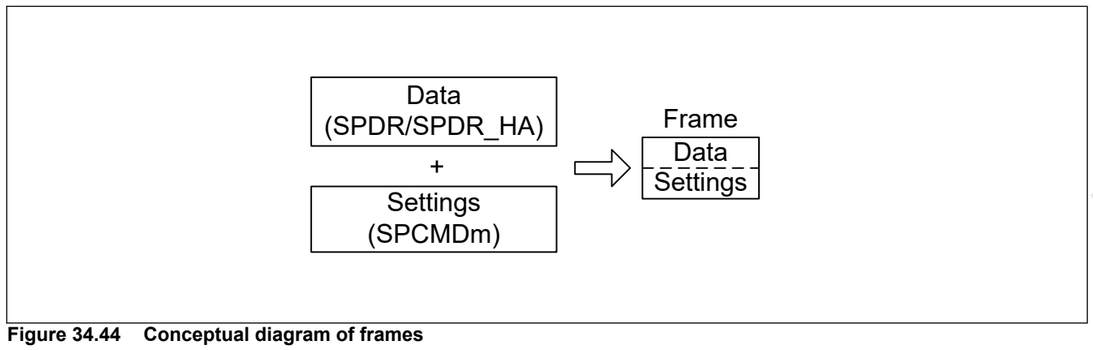

Figure 34.44 Conceptual diagram of frames

Figure 34.45 shows the correspondence between the commands and the transmit and receive buffers in the sequence of operations specified by the settings in Table 34.4.

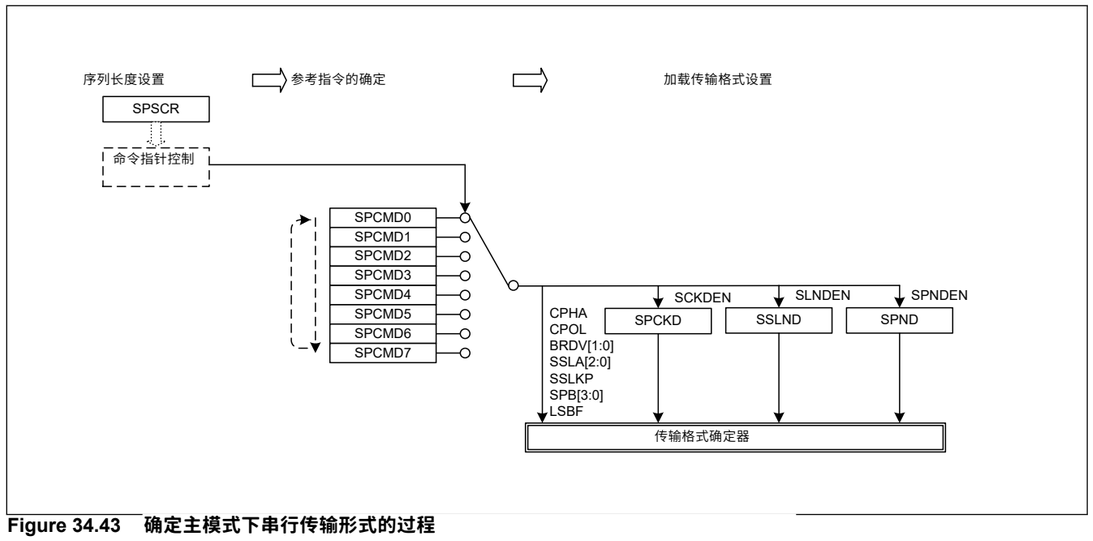

Figure 34.43 确定主模式下串行传输形式的过程

在本节中，帧是SPDRSPDR_HA中的数据和SPMDm中的设置的组合。

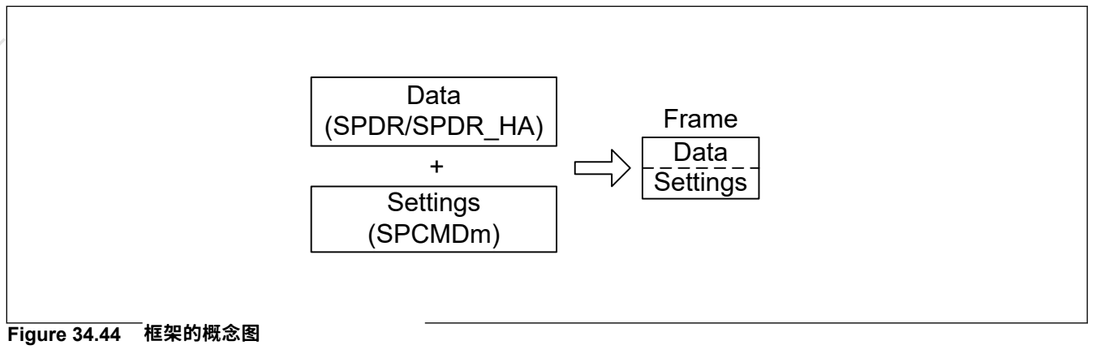

Figure 34.44 框架的概念图

图34.45显示了在表34.4中的设置指定的操作序列中命令与发送和接收缓冲区之间的对应关系。

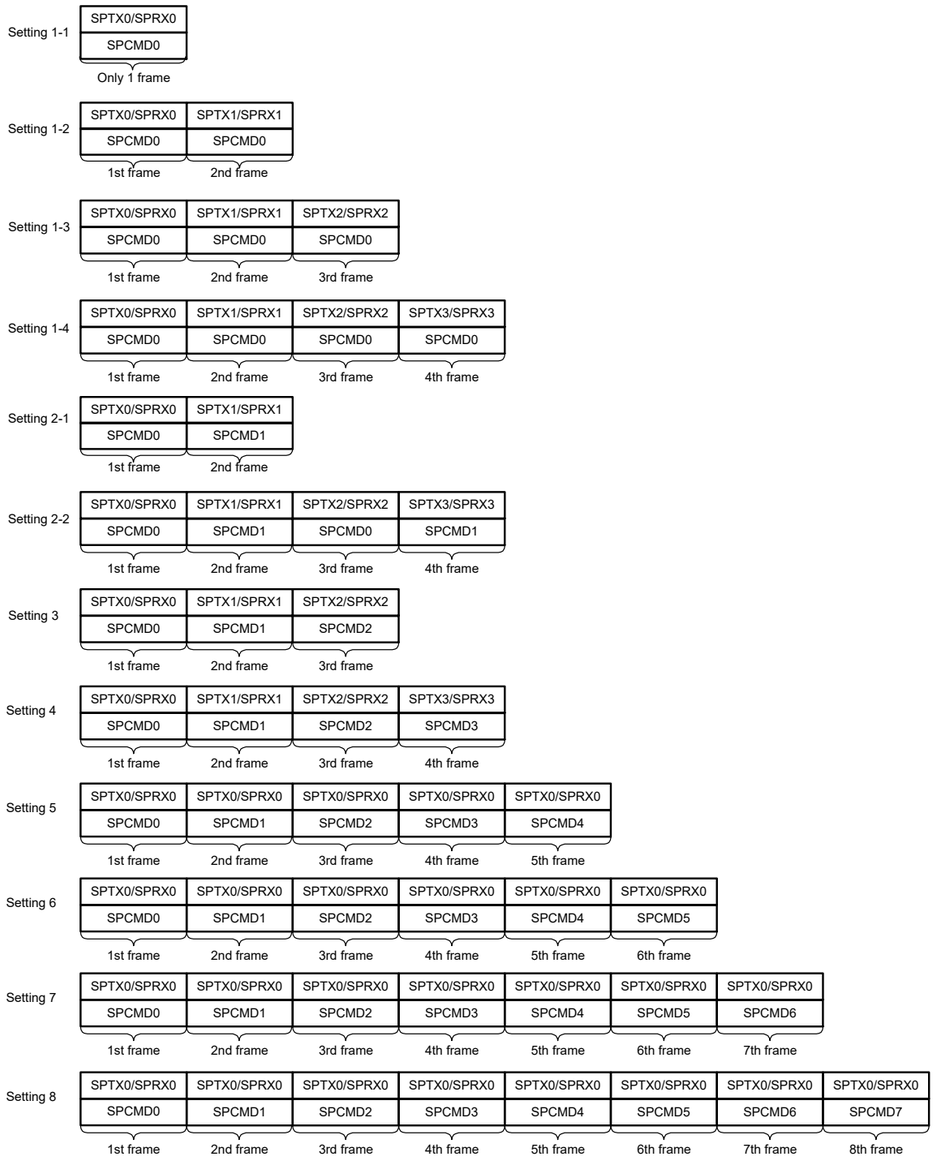

Figure 34.45 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Burst transfers

If the SPCMDm.SSLKP bit that the SPI references during the current serial transfer is 1, the SPI maintains the SSLni signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni

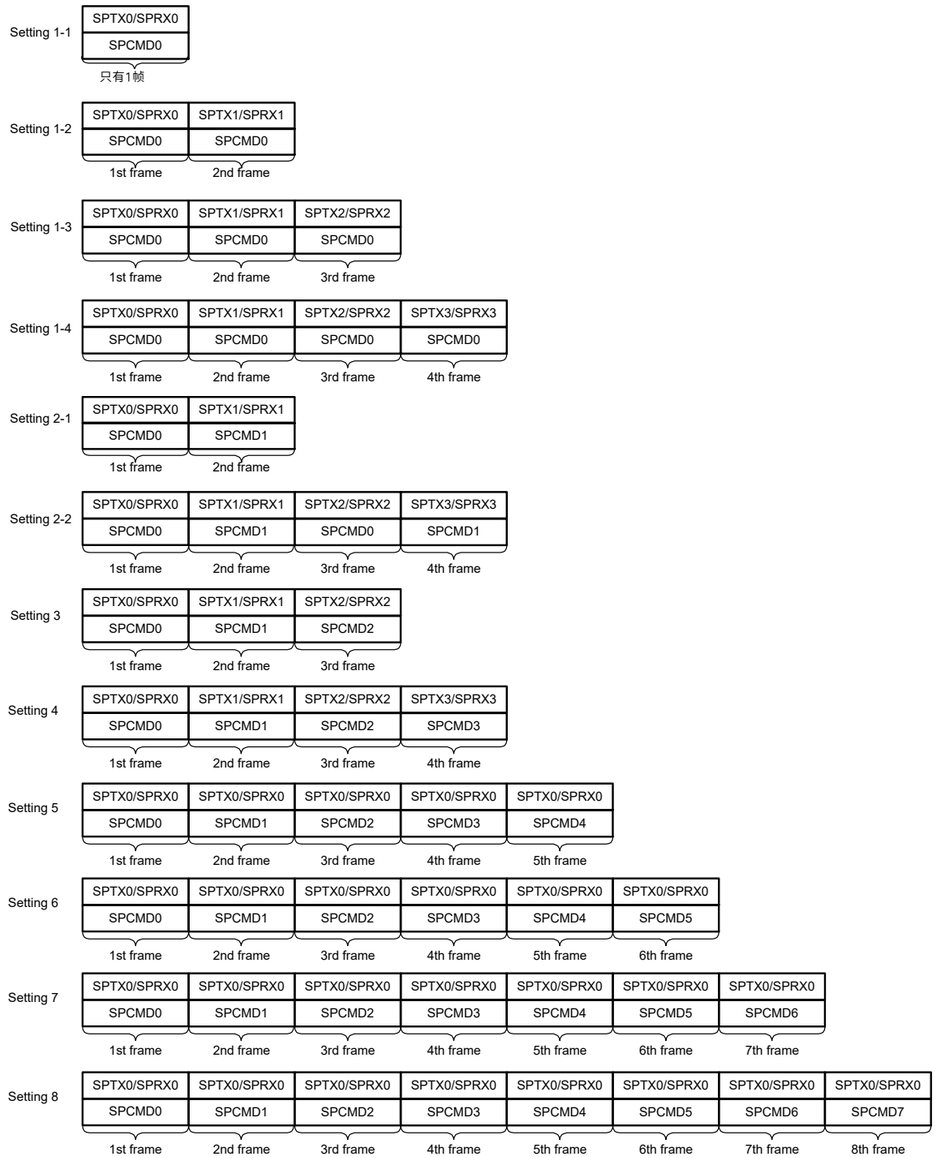

Figure 34.45 顺序操作中SPI命令寄存器与发送接收缓冲区的对应关系

(4) 突发传输

如果SPI在当前串行传输期间引用的SPCMDm.SSLKP位为1，则SPI在串行传输期间保持SSLni信号电平，直到下一次串行传输的SSLni信号断言开始。如果SSLni

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signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the SPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

- When Between Burst Transfer Frames Delay Select bit (BFDS) of SPI control register 3 (SPCR3) is 0.

Figure 34.46 shows an example of an SSLni signal operation for a burst transfer that is implemented using the SPCMD0 and SPCMD1 register settings. This section describes SPI operations (1) to (8) shown in Figure 34.46.

Note: The polarity of the SSLni output signal depends on the SSLP register settings.

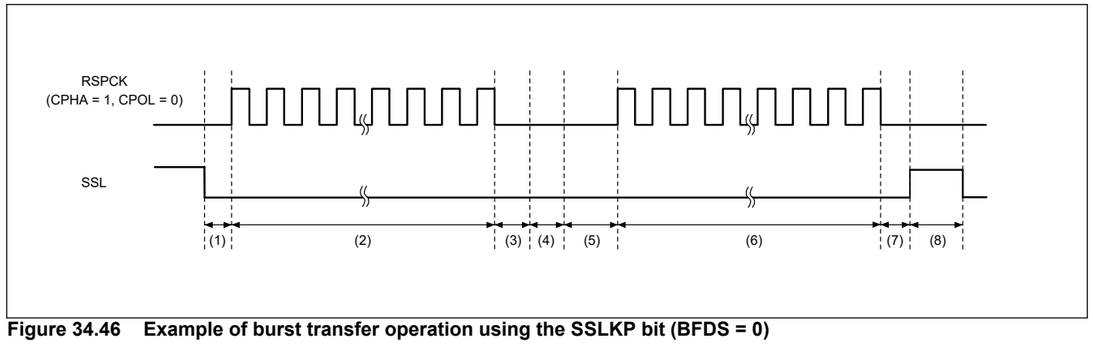


Figure 34.46 Example of burst transfer operation using the SSLKP bit (BFDS = 0)

The SPI operation at times (1) to (8) in the figure is as follows:

1. Based on the SPCMD0 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
2. The SPI executes serial transfers in accordance with the SPCMD0 settings.
3. The SPI inserts an SSL negation delay.
4. Because the SPCMD0.SSLKP bit is 1, the SPI keeps the SSLni signal value specified in SPCMD0. This period is sustained at a minimum for a period equal to the next-access delay in SPCMD0. If the shift register is empty after the passage of the minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
5. Based on the SPCMD1 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
6. The SPI executes serial transfers in accordance with the SPCMD1 settings.
7. Insert SSL negate delay.
8. Because the SPCMD1.SSLKP bit is 0, the SPI negates the SSLni signal. In addition, a next-access delay is inserted in accordance with SPCMD1.

If the SSLni signal output settings in the SPCMDm register where 1 is assigned to the SSLKP bit are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the SPI switches the SSLni signal status to SSLni signal assertion as shown in (5) in Figure 34.46. This corresponds to the command for the next transfer.

Note: If such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and collision of signal levels might occur.

The SPI in master mode references the SSLni signal operation within the module when the SSLKP bit is not used. When the SPCMDm.CPHA bit is 0, the SPI can accurately start serial transfers by using the SSLni signal assertion for the next transfer that is detected internally.

- When Between Burst Transfer Frames Delay Select bit (BFDS) of SPI control register 3 (SPCR3) is 1.

Figure 34.47 shows an example of SSL signal operation when burst transfer is achieved by using the settings of SPCMD0 and SPCMD1. The following describes SPI operations of (1) to (6) shown in Figure 34.47. The SSL output signal polarity depends on the set SPI slave select polarity register (SSLP) value.

下一次串行传输的信号电平与当前串行传输的SSLni信号电平相同，SPI可以在保持SSLni信号断言状态（突发传输）的同时执行连续串行传输。

●当SPI控制寄存器3(SPCR3)的突发传输帧之间延迟选择位(BFDS)为0时。

图34.46显示了使用SPCMD0和SPCMD1寄存器设置实现的突发传输的SSLni信号操作示例。本节介绍图34.46所示的SPI操作(1)至(8)。

Note: SSLni输出信号的极性取决于SSLP寄存器设置。

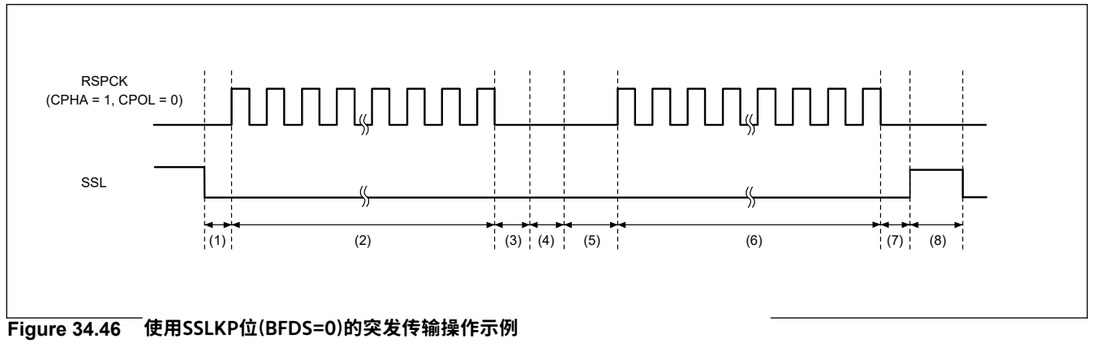


Figure 34.46 使用SSLKP位(BFDS=0)的突发传输操作示例

图中（1）到（8）时刻的SPI操作如下：

1.基于SPCMD0设置，SPI断言SSLni信号并插入RSPCK延迟。

2.SPI根据SPMD0设置执行串行传输。

3.SPI插入SSL否定延迟。

4.由于SPCMD0.SSLKP位为1，SPI保持SPCMD0中指定的SSLni信号值。这个时期是至少持续一段时间等于SPMD0中的下一次访问延迟。如果在经过最小周期后移位寄存器为空，则该周期一直持续到发送数据存储在移位寄存器中以供下一次传输。

5.基于SPCMD1设置，SPI断言SSLni信号并插入RSPCK延迟。

6.SPI根据SPMD1设置执行串行传输。

7.插入SSL否定延迟。

8.由于SPCMD1.SSLKP位为0，SPI否定SSLni信号。此外，根据SPMD1插入下一个访问延迟。

如果SPCMDm寄存器中SSLKP位为1的SSLni信号输出设置与下次传输使用的SPCMDm寄存器中的SSLni信号输出设置不同，则SPI将SSLni信号状态切换为SSLni信号断言，如下所示如图34.46(5)所示。这对应于下一次传输的命令。

Note: 如果发生这种SSLni信号切换，驱动MISon信号的从机竞争，可能会发生信号电平冲突。

当不使用SSLKP位时，主模式下的SPI参考模块内的SSLni信号操作。当。。。的时候SPCMDm.CPHA位为0，SPI可以通过使用SSLni信号断言来准确启动串行传输，以进行内部检测到的下一次传输。

●当SPI控制寄存器3(SPCR3)的突发传输帧之间延迟选择位(BFDS)为1时。

图34.47显示了使用SPCMD0和SPCMD1的设置实现突发传输时SSL信号操作的示例。下面描述图34.47所示的(1)到(6)的SPI操作。SSL输出信号极性取决于设置的SPI从机选择极性寄存器(SSLP)值。

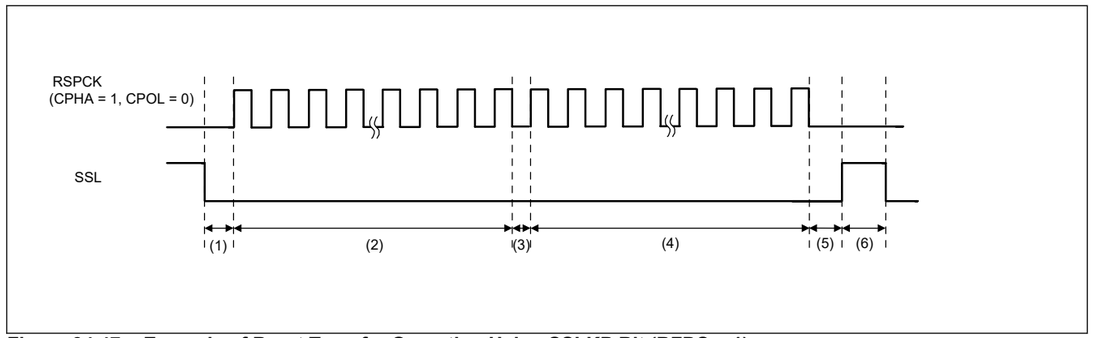


Figure 34.47 Example of Burst Transfer Operation Using SSLKP Bit (BFDS = 1)

1. Assert the SSL signal and insert an RSPCK delay according to SPCMD0. The RSPCK delay is inserted only the first frame of burst transmission.
2. Perform serial transfer according to SPCMD0. Wait last clock until the next transmit data is stored in the shift register, if the shift register is empty during RSPCK negate period between frames.
3. The value of SSL signal according to SPCMD0 was hold, because the SPCMD0.SSLKP bit is 1. RSPCK negate period between frames is 0.5RSPCK, if the shift register is not empty.
4. Perform serial transfer according to SPCMD1.
5. Insert SSL negate delay for the last frame.
6. The SSL signal is negated because the SSLKP bit in SPCMD1 is 0. Furthermore, the next-access delay is inserted according to SPCMD1.

(5) RSPCK delay (t1)

The RSPCK delay value of the SPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD.SCKDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced during a serial transfer by pointer control, and determines an RSPCK delay using the SPCMDm.SCKDEN bit and SPCKD.SCKDL[2:0] bits, as listed in Table 34.11. For a definition of RSPCK delay, see section 34.3.5. Transfer Formats.

RSPCK delay insert to only the first frame of burst transmission, when transmit without “Between Burst Transfer Frames Delay”. (The SPCMD.SSLKP bit is 1 and the SPCR3.BFDS bit is 1.)

Table 34.11 Relationship between the SPCMDm.SCKDEN bit, SPCKD.SCKDL[2:0] bits, and RSPCK delay

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL negation delay (t2)

The SSL negation delay value of the SPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND.SLNDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced by pointer control during a serial transfer, and determines an SSL negation delay using the SPCMDm.SLNDEN bit and SSLND.SLNDL[2:0] bits, as listed in Table 34.12. For a definition of SSL negation delay, see section 34.3.5. Transfer Formats.

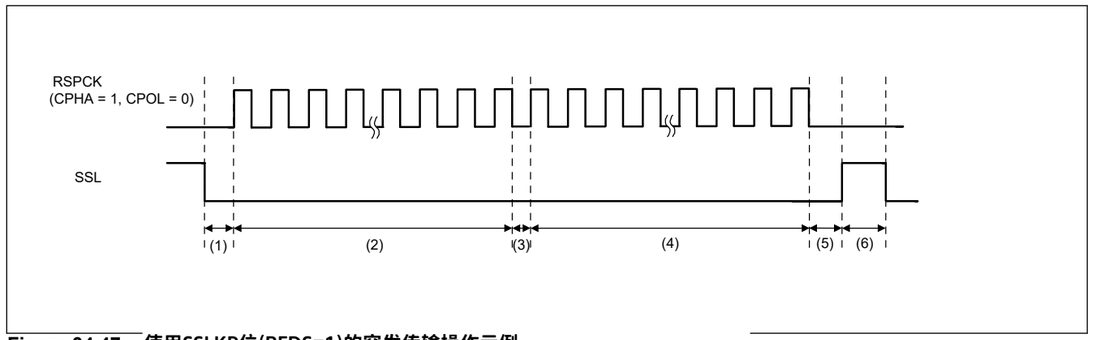


Figure 34.47 使用SSLKP位(BFDS=1)的突发传输操作示例

1.置位SSL信号并根据SPMD0插入一个RSPCK延迟。RSPCK延迟仅插入突发传输的第一帧。

2.根据SPMD0进行串行传输。如果在帧之间的RSPCK否定周期内移位寄存器为空，则等待最后一个时钟，直到下一个发送数据存储在移位寄存器中。

3.SPCMD0的SSL信号值被保持，因为SPCMD0.SSLKP位为1。如果移位寄存器不为空，则帧之间的RSPCK否定周期为0.5RSPCK。

4.根据SPMD1进行串行传输。

5.为最后一帧插入SSL否定延迟。

6.SSL信号被取反，因为SPCMD1中的SSLKP位为0。另外，根据SPCMD1插入下一个访问延迟。

(5) RSPCK delay (t1)

主机模式下SPI的RSPCK延迟值取决于SPMDm.SCKDEN位设置和SPCKD.SCKDL[2:0]位设置。SPI通过指针控制确定串行传输期间要参考的SPCMDm寄存器，并使用SPCMDm.SCKDEN位和SPCKD.SCKDL[2:0]位确定RSPCK延迟，如表34.11中所列。有关RSPCK延迟的定义，请参见第34.3.5节。传输格式。

当没有“BetweenBurstTransferFrames”传输时，RSPCK延迟仅插入到突发传输的第一帧延迟”。（SPCMD.SSLKP位为1，SPCR3.BFDS位为1。）

Table 34.11 SPCMDm.SCKDEN位、SPCKD.SCKDL[2:0]位和RSPCK延迟之间的关系

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL否定延迟(t2)

主模式下SPI的SSL否定延迟值取决于SPMDm.SLNDEN位设置和SSLND.SLNDL[2:0]位设置。SPI确定串行传输期间指针控制要引用的SPCMDm寄存器，并使用SPCMDm.SLNDEN位和SSLND.SLNDL[2:0]位确定SSL否定延迟，如表34.12中所列。有关SSL否定延迟的定义，请参阅第34.3.5节。传输格式。

An SSL negation delay is inserted to only the last frame of the burst transmission, that is, transmit without “between burst transfer frames delay”. (SPCMD.SSLKP bit is 1 and SPCR3.BFDS bit is 1).

Table 34.12 Relationship between the SPCMDm.SLNDEN bit, SSLND.SLNDL[2:0] bits, and SSL negation delay

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

The next-access delay value of the SPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND.SPNDL[2:0] bits setting. The SPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and then determines a next-access delay during serial transfer using the SPCMDm.SPNDEN bit and SPND.SPNDL[2:0] bits, as listed in Table 34.13. For a definition of next-access delay, see section 34.3.5. Transfer Formats.

A next-Access delay is inserted to only the last frame of the burst transmission, that is, transmit without “between burst transfer frames delay”. (SPCMD.SSLKP bit is 1 and SPCR3.BFDS bit is 1).

Table 34.13 Relationship between the SPCMDm.SPNDEN bit, SPND.SPNDL[2:0] bits, and next-access delay

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8) Initialization flow

Figure 34.48 shows an example of SPI initialization flow when the SPI is in master mode. For information on how to set up the Interrupt Controller Unit (ICU), DMAC and I/O ports, see the descriptions given in the individual blocks.

SSL否定延迟仅插入到突发传输的最后一帧，即没有“突发传输帧之间延迟”的传输。（SPCMD.SSLKP位为1，SPCR3.BFDS位为1）。

Table 34.12 SPCMDm.SLNDEN位、SSLND.SLNDL[2:0]位和SSL否定延迟之间的关系

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL否定延迟
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

主机模式下SPI的下一次访问延迟值取决于SPMDm.SPNDEN位设置和SPND.SPNDL[2:0]位设置。SPI通过指针控制确定串行传输期间要引用的SPCMDm寄存器，然后使用SPCMDm.SPNDEN位和SPND.SPNDL[2:0]位确定串行传输期间的下一次访问延迟，如表34.13中所列。有关下一次访问延迟的定义，请参见第34.3.5节。传输格式。

仅在突发传输的最后一帧中插入下一个访问延迟，即，在没有“突发传输帧之间延迟”的情况下进行传输。（SPCMD.SSLKP位为1，SPCR3.BFDS位为1）。

Table 34.13 SPMDm.SPNDEN位、SPND.SPNDL[2:0]位和下一次访问延迟之间的关系

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8) 初始化流程

图34.48显示了SPI处于主机模式时的SPI初始化流程示例。有关如何设置中断控制器单元(ICU)、DMAC和IO端口的信息，请参见各个块中给出的说明。

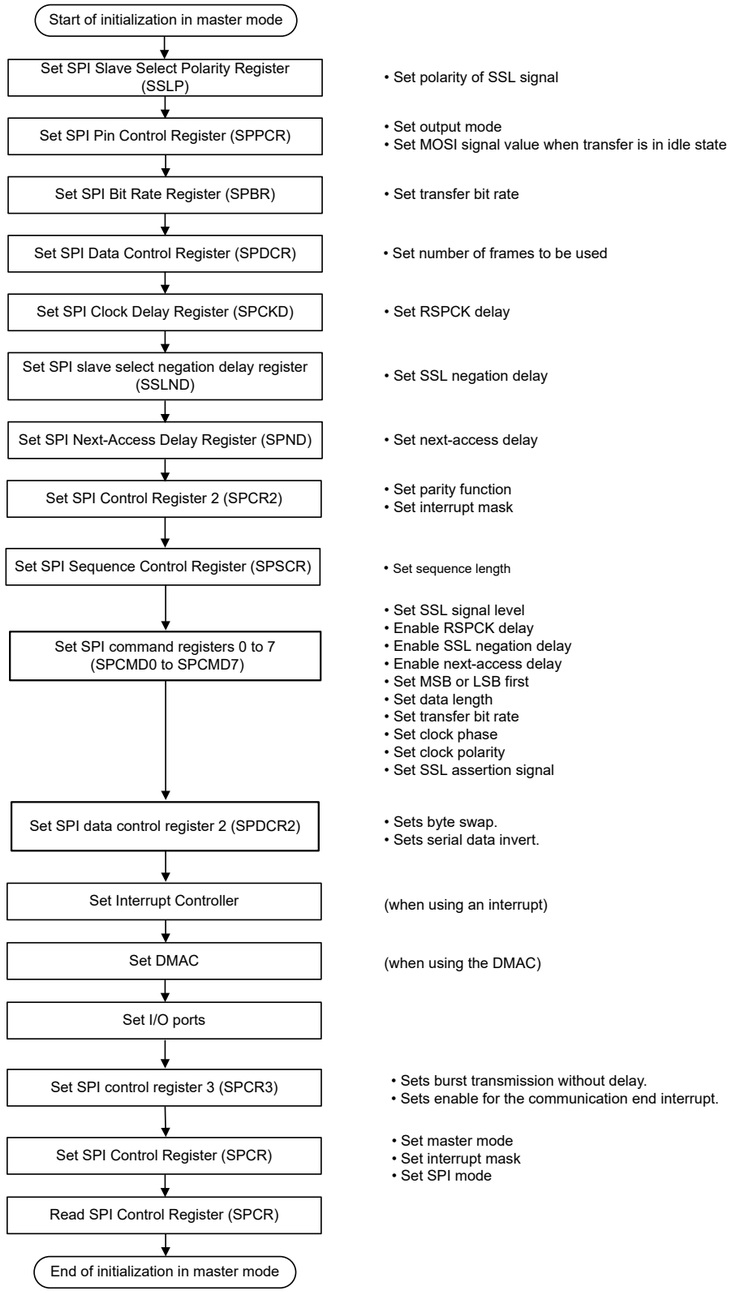


Figure 34.48 Example of initialization flow in master mode for SPI operation

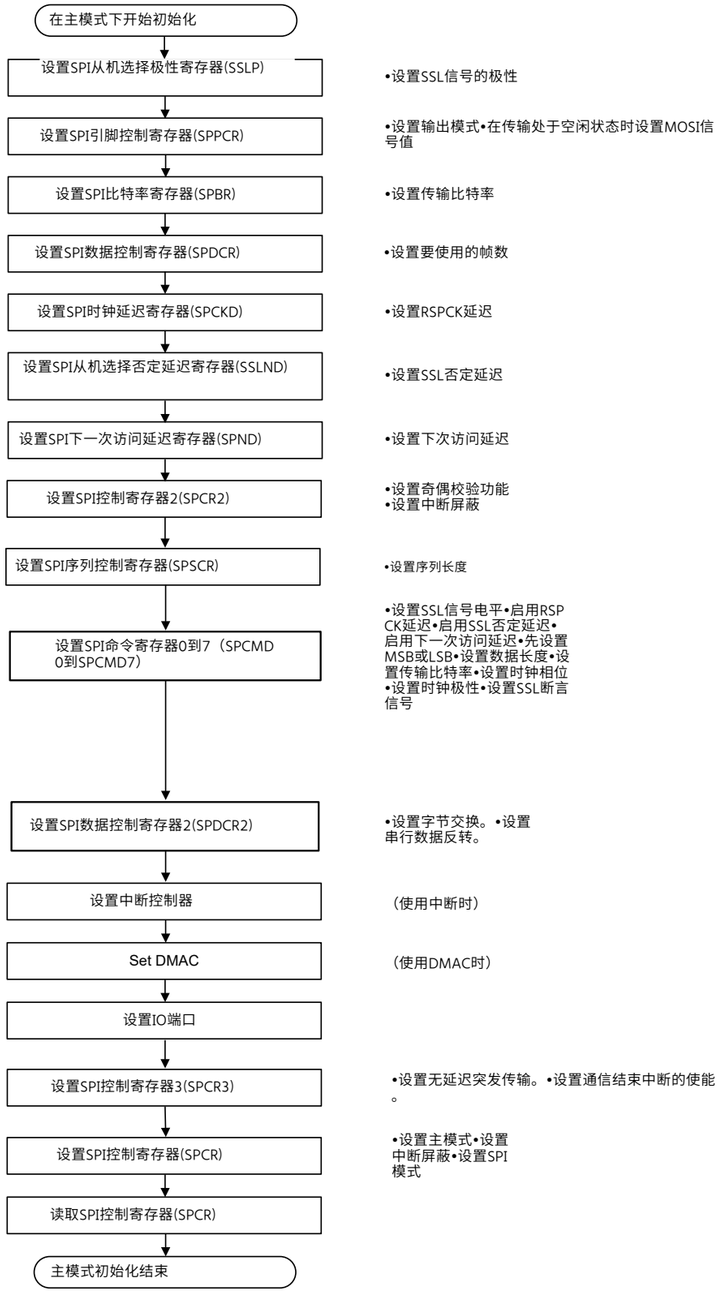


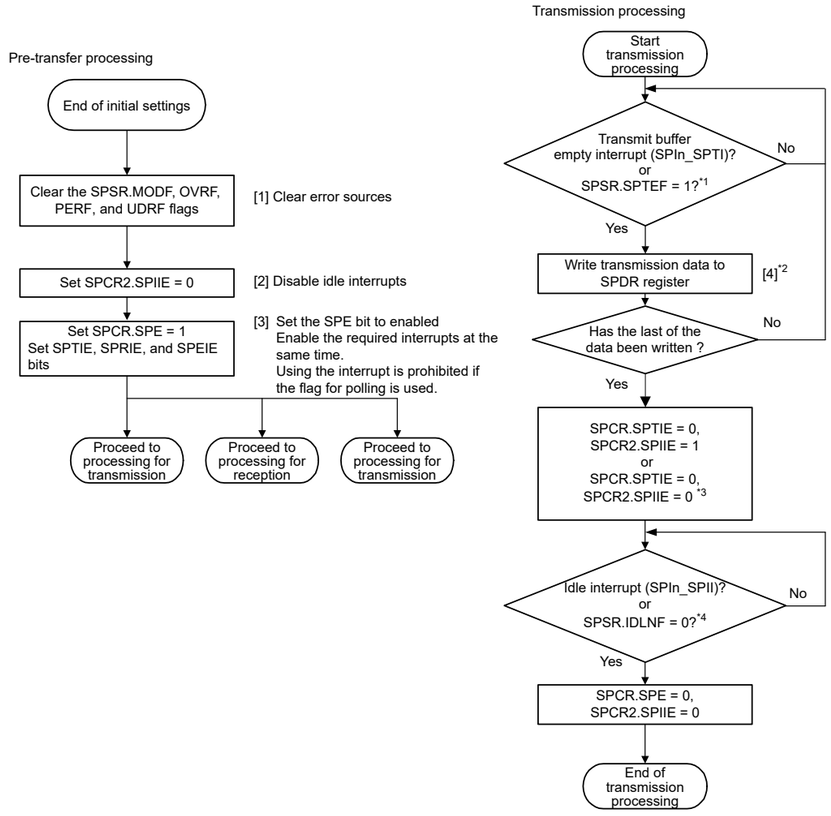
Figure 34.48 SPI操作的主模式初始化流程示例

(9) Software processing flow

Figure 34.49 to Figure 34.51 show examples of the software processing flow.

Transmit processing flow

When transmitting data, with the SPIi_SPII interrupt enabled, the CPU is notified of the completion of data transmission after the last data write for transmission.



Note 1. Before writing data for transmission to SPDR/SPDR_HA/SPDR_BY, check that the transmit buffer is empty by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. Setting SPCR2.SPIIE and SPCR3.CENDIE to 0 is prohibited if the flag for polling is used.
Note 3. Wait more than 1 PCLKA, after writing data for transmission to SPDR register, and before starting to poll SPSR.IDLNF flag or SPSR.CENDF, if the flag for polling is used.
Note 4. SPDR = SPDR/SPDR_HA/SPDR_BY
Access when interrupt handling routine is executed once to the number of frames set in SPDCR.SPFC[1:0]

Figure 34.49 Transmission flow in master mode

Receive processing flow

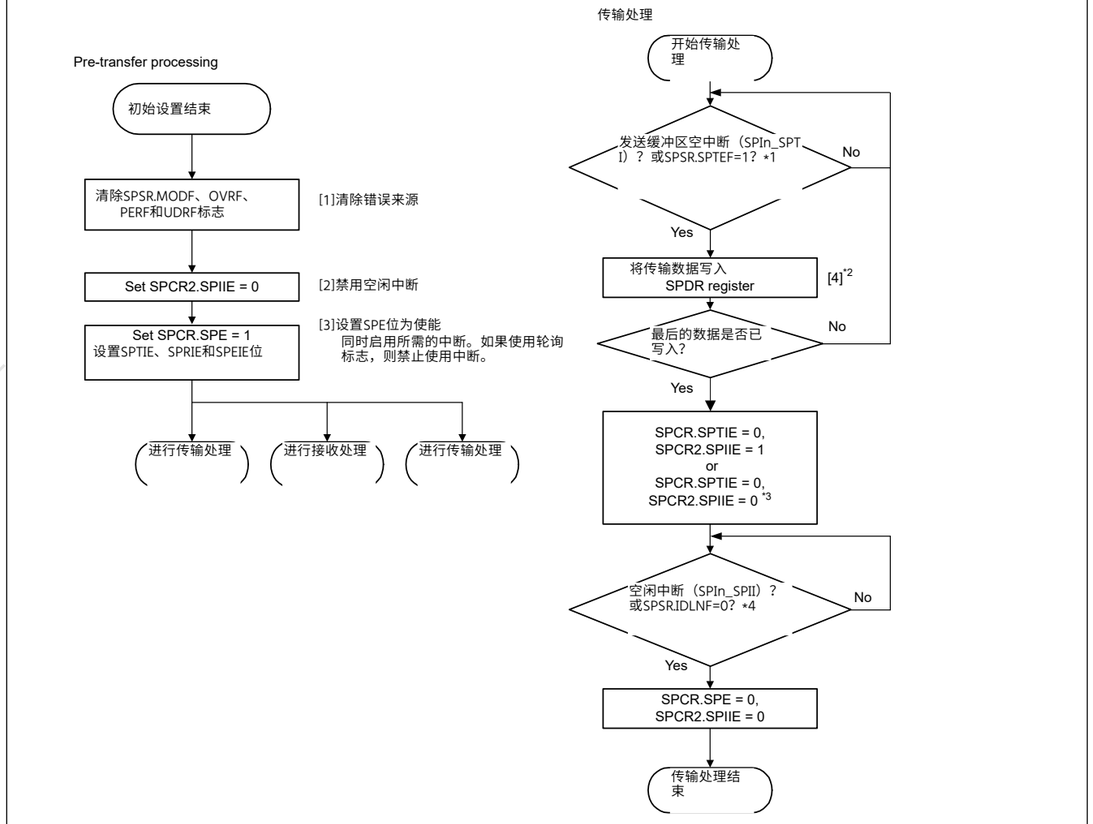
The SPI has receive only operation in slave mode.

(9) 软件处理流程

图34.49至图34.51显示了软件处理流程的示例。

传输处理流程

发送数据时，SPIi_SPII中断使能，在最后一次数据写入发送后通知CPU数据发送完成。



注1.在将数据写入SPDRSPDR_HASPDR_BY之前，如果使用轮询标志，请通过读取SPSR.SPTEF标志检查发送缓冲区是否为空。

注2.如果使用轮询标志，则禁止将SPCR2.SPIIE和SPCR3.CENDIE设置为0。
注3.等待超过1个PCLKA，在将数据写入SPDR寄存器后，如果使用轮询标志，则在开始轮询SPSR.IDLNF标志或SPSR.CENDF之前。

Note 4. SPDR = SPDR/SPDR_HA/SPDR_BY
当中断处理例程执行一次到SPDCR.SPFC[1:0]中设置的帧数时访问

Figure 34.49 主模式下的传输流

接收处理流程

SPI在从机模式下仅接收操作。

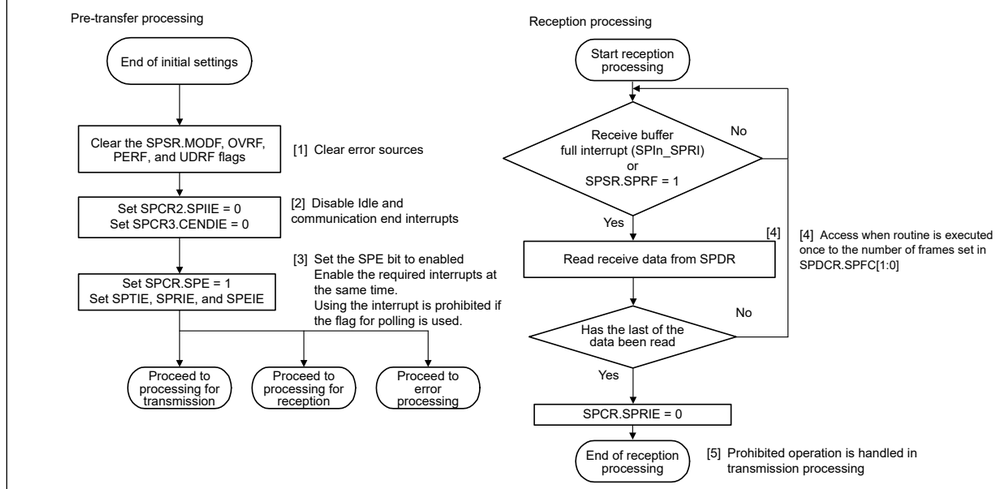


Figure 34.50 Reception flow in master mode

Error processing flow

The SPI detects the following errors:

- Mode fault error
- Underrun error
- Overrun error
- Parity error

When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Therefore, Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors. Not doing so leads to updating of the SPSSR.SPECM[2:0] bits.

When an error is detected using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

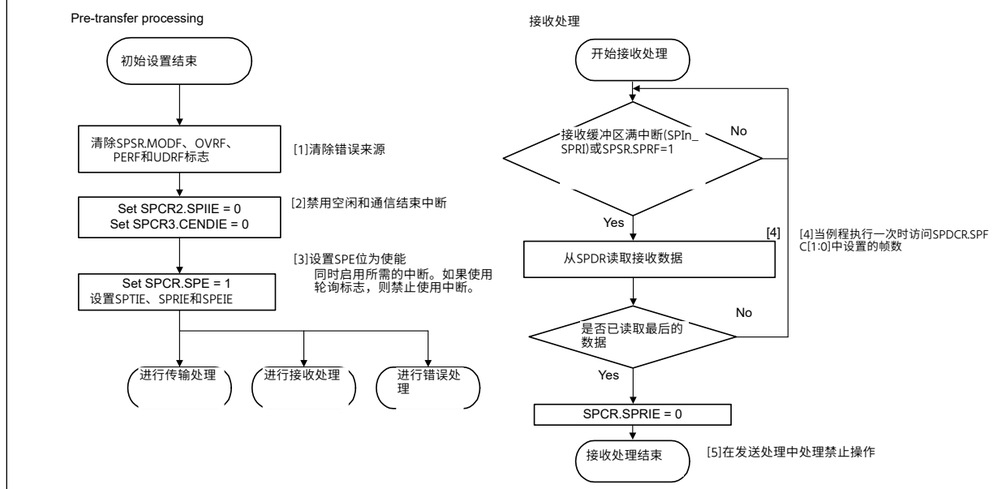


Figure 34.50 主模式下的接收流程

错误处理流程

SPI检测到以下错误：

●模式故障错误

- Underrun error

●超限错误

●奇偶校验错误

当产生模式故障错误时，SPCR.SPE位自动清零，停止发送和接收操作。对于其他来源的错误，SPCR.SPE位不会被清除，发送和接收操作会继续。因此，瑞萨建议清除SPCR.SPE位以停止除模式故障错误以外的错误操作。不这样做会导致更新SPSSR.SPECM[2:0]位。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

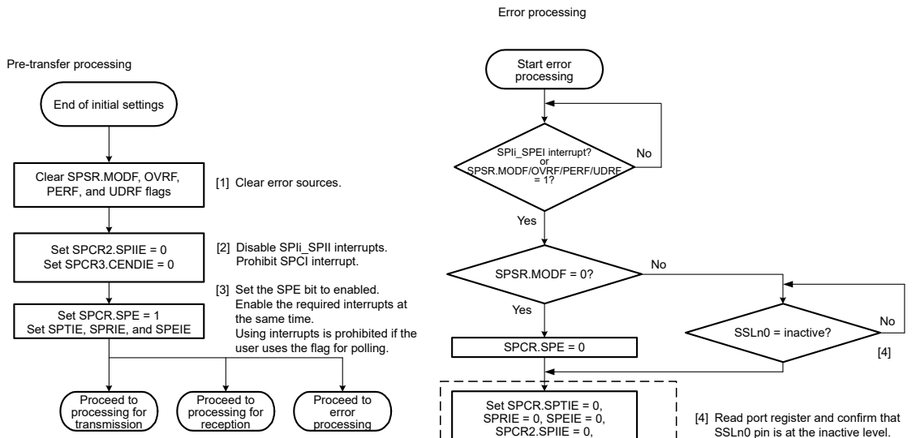


Figure 34.51 Error processing flow in master mode

34.3.11.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

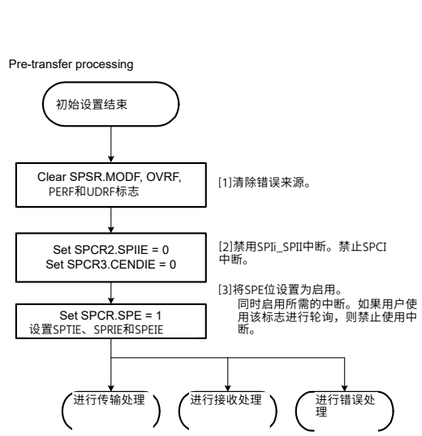
When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

For details on the SPI transfer format, see section 34.3.5. Transfer Formats. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P setting.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 34.3.9. Error Detection).



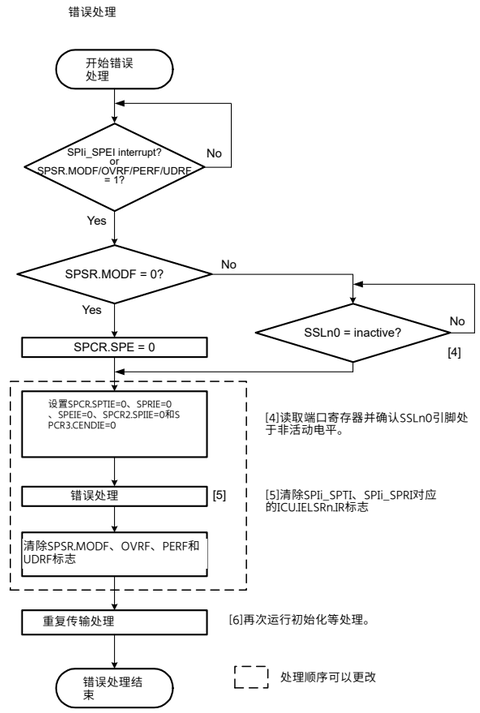


Figure 34.51 主模式下的错误处理流程

34.3.11.2 从模式操作

(1) 开始串行传输

当SPCMD0.CPHA位为0时，如果SPI检测到SSLn0输入信号断言，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为0时，SSLn0输入信号的断言触发串行传输的开始。

当CPHA位为1时，如果SPI在SSLn0信号置位条件下检测到第一个RSPCKn边沿，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为1时，SSLn0信号断言条件中的第一个RSPCKn边沿触发串行传输的开始。

无论CPHA位设置如何，SPI都会在SSLn0信号置位时驱动MIOn输出信号。SPI输出的数据是有效还是无效，取决于CPHA位设置。

有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。SSLn0输入信号的极性取决于SSLP.SSL0P设置。

(2) 终止串行传输

无论SPCMD0.CPHA位设置如何，SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间时（SPSR.SPRF标志为0），在串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区状态无关。如果SPI从串行传输开始到串行传输结束检测到SSLn0输入信号否定，则会发生模式故障错误（请参阅第34.3.9节。错误检测）。

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[3:0] bits setting. The polarity of the SSLn0 input signal is determined by the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

(3) Notes on single-slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the configuration shown in Figure 34.7, if the SPI is used in single-slave mode, the SSLn0 signal is fixed at an active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. For the SPI to correctly execute transmit and receive operations in slave mode when the SSLn0 input signal is fixed at an active state, the CPHA bit must be set to 1. Do not fix the SSLn0 input signal if there is a requirement for setting the CPHA bit to 0.

(4) Burst transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. When the CPHA bit is 1, the serial transfer period is the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state. Even when the SSLn0 input signal remains at the active level, the SPI can accommodate burst transfers, because it can detect the start of an access.

When the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization flow

Figure 34.52 shows an example of initialization flow for SPI operation when the SPI is in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度由SPCMD0.SPB[3:0]位设置决定。SSLn0输入信号的极性由SSLP.SSL0P位设置决定。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(3) 单从操作注意事项

如果SPCMD0.CPHA位为0，则SPI在检测到SSLn0输入信号的断言边沿时开始串行传输。在图34.7所示的配置中，如果SPI用于单从模式，则SSLn0信号固定在激活状态。因此，当CPHA位设置为0时，SPI无法正确启动串行传输。为使SPI在SSLn0输入信号固定为活动状态时正确执行从模式下的发送和接收操作，CPHA位必须设置为1。如果需要设置CPHA，请不要固定SSLn0输入信号位为0。

(4) 突发传输

如果SPCMD0.CPHA位为1，则可以执行连续串行传输（突发传输），同时保持SSLn0输入信号的断言状态。当CPHA位为1时，串行传输周期是从第一个RSPCKn边沿到SSLn0信号有效状态下接收最后一个位的采样时序的周期。即使SSLn0输入信号保持在有效电平，SPI也可以适应突发传输，因为它可以检测访问的开始。

当CPHA位为0时，突发传输期间的第二次和后续串行传输无法正确执行。

(5) 初始化流程

图34.52显示了SPI处于从机模式时SPI操作的初始化流程示例。有关如何设置ICU、DTC和IO端口的说明，请参见各个块中给出的说明。

RA生态工作室

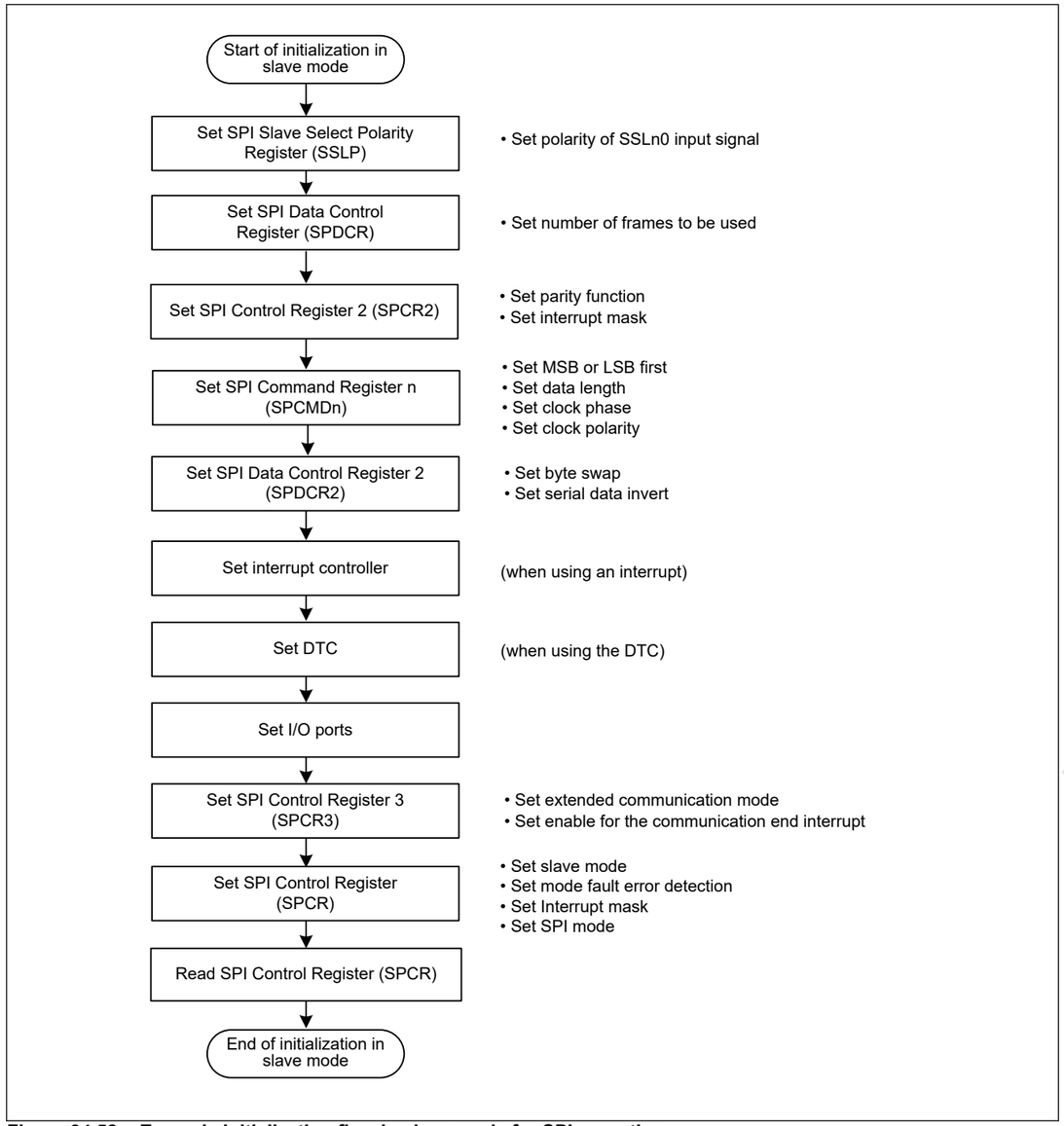


Figure 34.52 Example initialization flow in slave mode for SPI operation

(6) Software processing flow

Figure 34.53 to Figure 34.55 show examples of the flow of software processing.

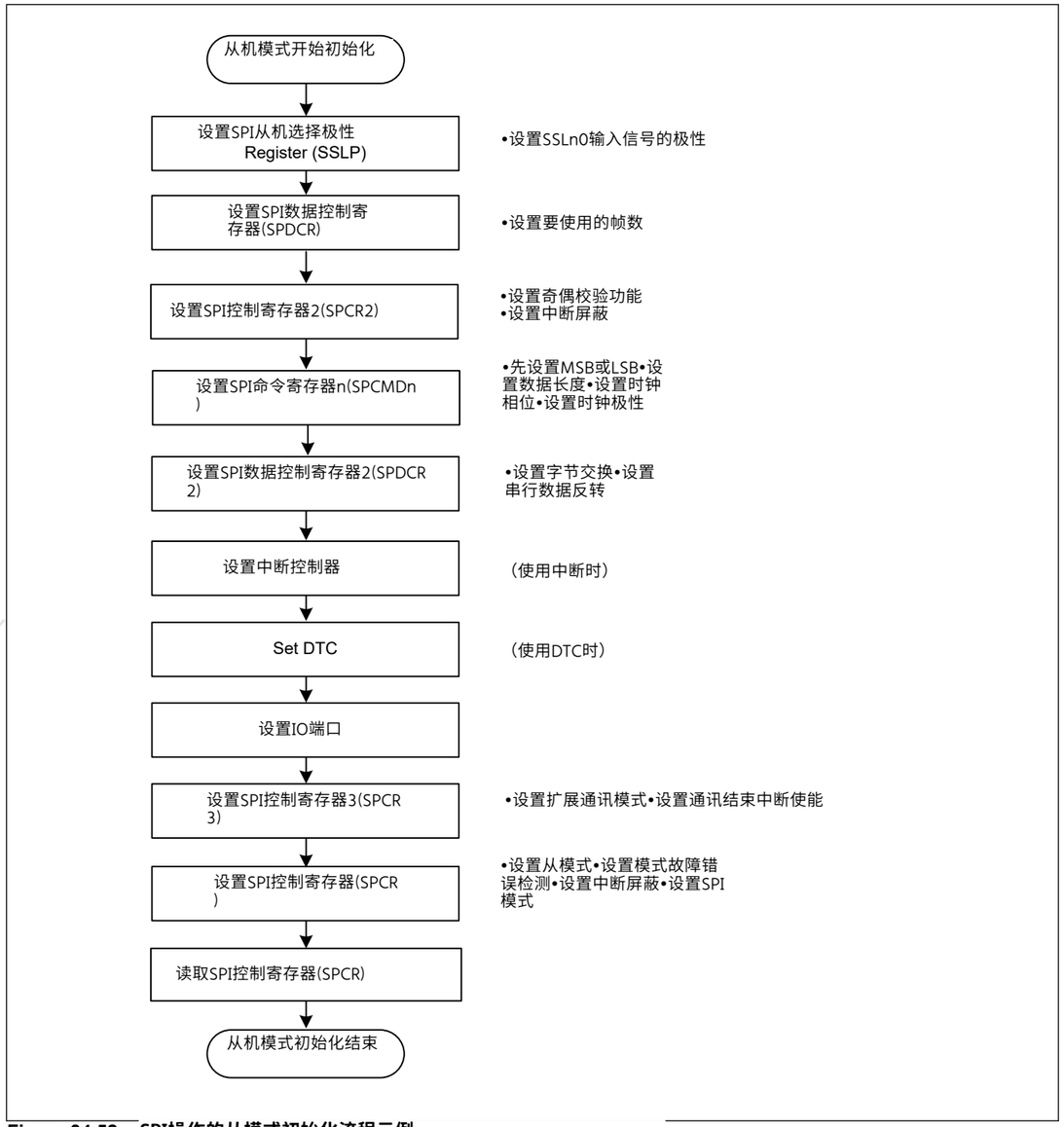
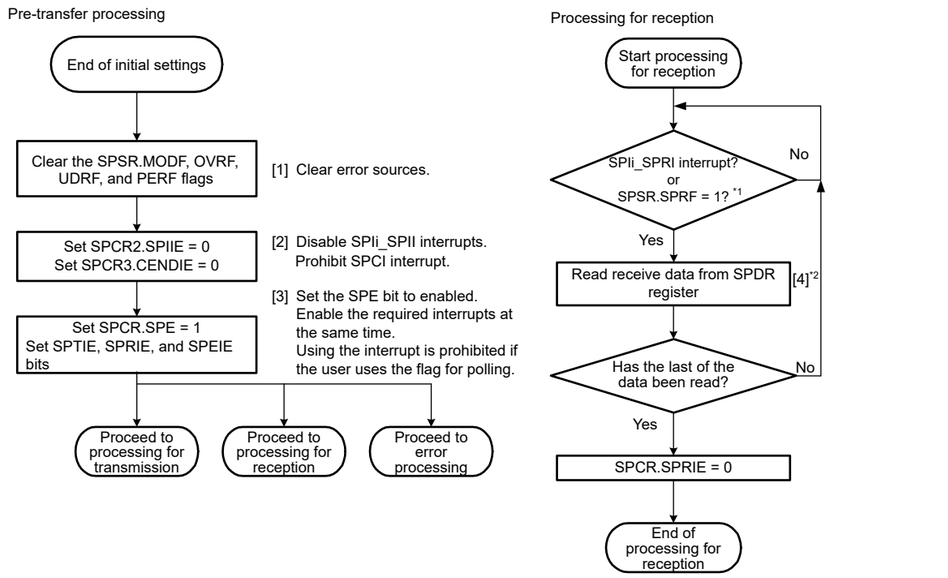


Figure 34.52 SPI操作的从模式初始化流程示例

(6) 软件处理流程

图34.53至图34.55显示了软件处理流程的示例。

Transmit processing flow



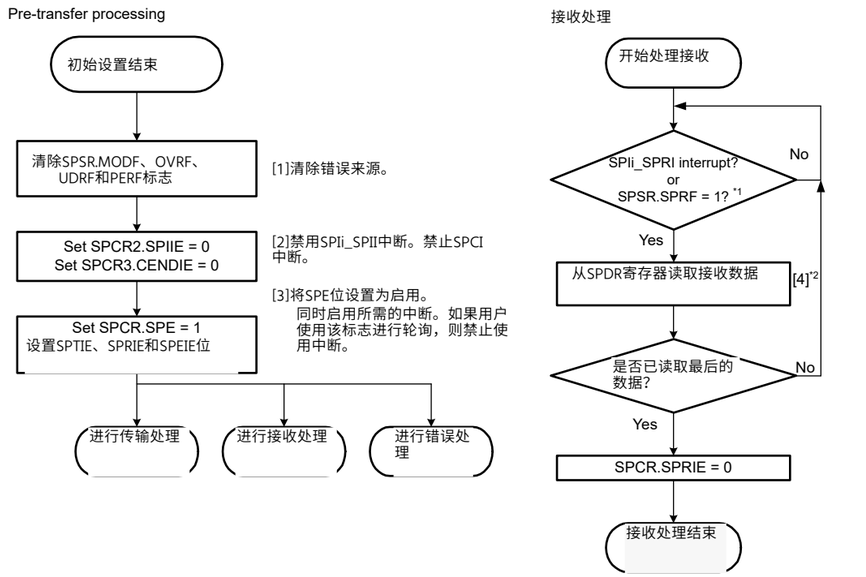
Note 1. Before writing data for transmission to SPDR register, check the transmit buffer empty interrupt by reading SPSR.SPTEF flag, if the flag for polling is used.
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
Access when interrupt handling routine is executed once to the number of frames set in SPDCR.SPFC[1:0] bits

Figure 34.53 Transmission flow in slave mode

Receive processing flow

The SPI does not handle receive-only operation, so processing for transmission is required.

传输处理流程



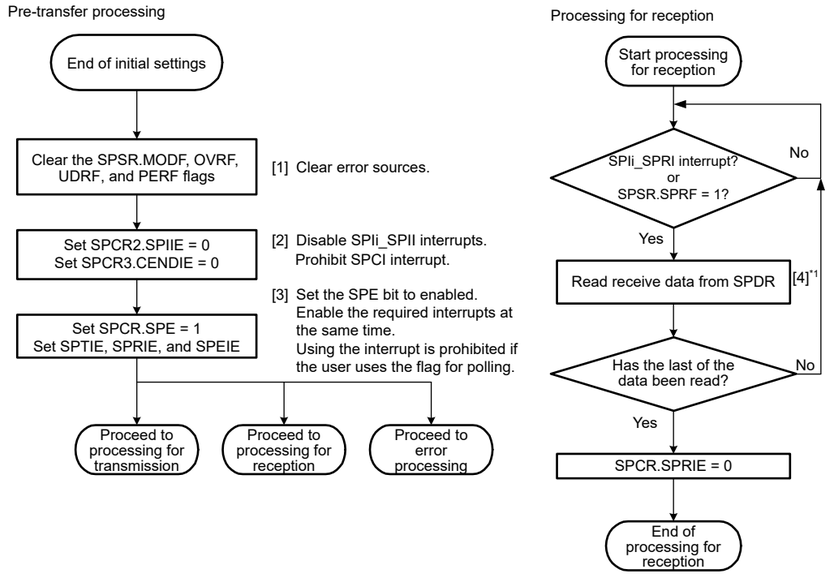
注1.在将数据写入SPDR寄存器之前，如果使用轮询标志，请通过读取SPSR.SPTEF标志检查发送缓冲区空中断。

Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
当中断处理例程执行一次到SPDCR.SPFC[1:0]位中设置的帧数时访问

Figure 34.53 从模式下的传输流

接收处理流程

SPI不处理只接收操作，因此需要处理传输。



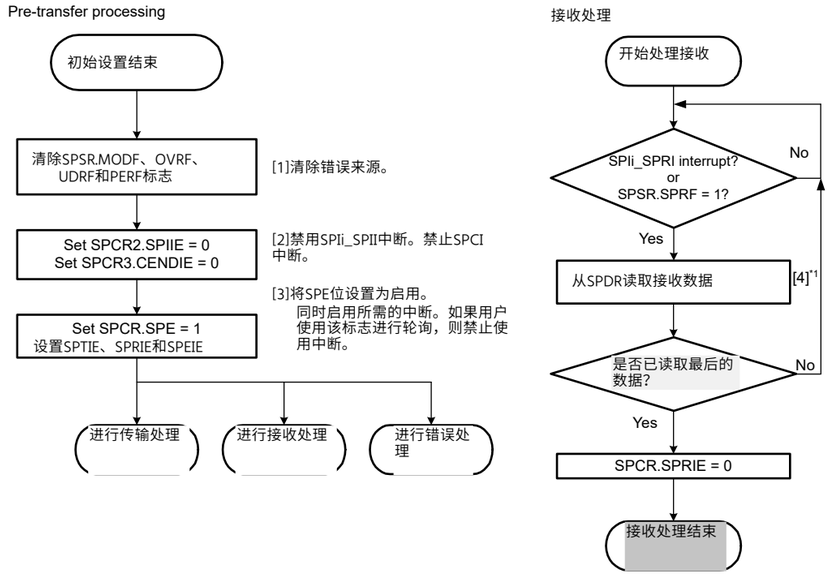
Note 1. Before writing data for transmission to the SPDR register, check that the transmit buffer is empty by reading the SPSR.SPTEF flag, if the flag for polling is used.
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
Access when interrupt handling routine is executed once to the number of frames set in SPDCR.SPFC[1:0] bits

Figure 34.54 Reception flow in slave mode

Error processing flow

In slave mode operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.



注1.在将要发送的数据写入SPDR寄存器之前，请通过读取SPSR.SPTEF标志，如果使用了轮询标志。
Note 2. SPDR = SPDR/SPDR_HA/SPDR_BY
当中断处理例程执行一次到SPDCR.SPFC[1:0]位中设置的帧数时访问

Figure 34.54 从机模式下的接收流程

错误处理流程

在从模式操作中，即使产生了模式故障错误，SPSR.MODF标志也可以被清除，而与SSLn0引脚的状态无关。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

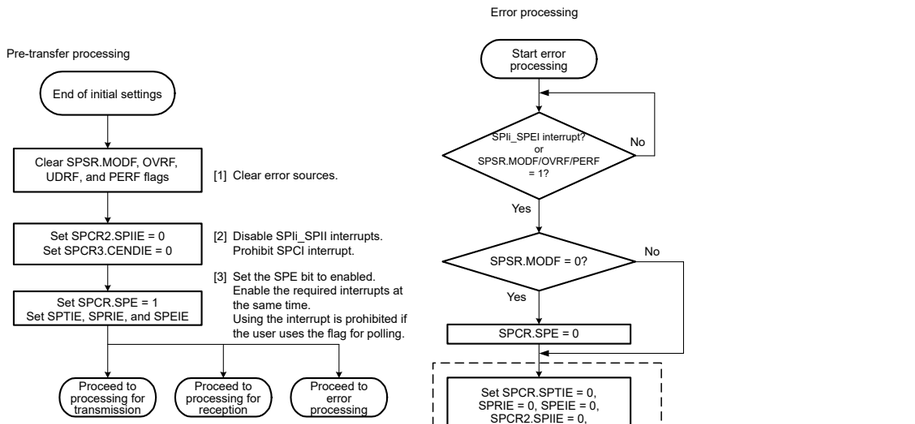


Figure 34.55 Error processing flow for slave mode

34.3.12 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master mode and slave mode operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected, because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation is enabled when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

34.3.12.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/SPDR_HA register with the transmit buffer empty, the data for the next transfer not set and the SPSR.SPTEF flag is 1. When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA, the SPI copies data from the transmit buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

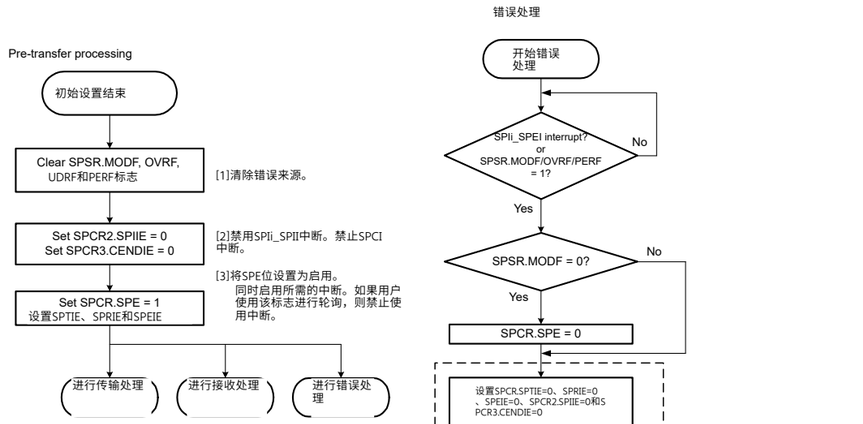


Figure 34.55 从机模式的错误处理流程

34.3.12 时钟同步操作

将SPCR.SPMS位设置为1可选择SPI的时钟同步操作。在时钟同步操作中，不使用SSLni引脚，而RSPCKn、MOSIn和MISOn引脚处理通信。所有SSLni引脚都可用作IO端口引脚。

虽然时钟同步操作不需要使用SSLni引脚，但模块的操作与SPI操作相同。在主模式和从模式操作中，可以使用与在相同的流程中执行通信

SPI操作。但是，未检测到模式故障错误，因为未使用SSLni引脚。

此外，如果在从模式(SPCR.MSTR=0)下SPCMDm.CPHA位设置为0时使能时钟同步操作，则不要执行操作。

34.3.12.1 主模式操作

(1) 开始串行传输

当数据写入SPDRSPDR_HA寄存器且发送缓冲区为空、未设置下一次传输的数据且SPSR.SPTEF标志为1时，SPI更新SPDRSPDR_HA的发送缓冲区(SPTX)中的数据。将SPDCR.SPFC[1:0]位中设置的帧数写入SPDRSPDR_HA后，寄存器为空，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为满，而在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bits setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following parameters are specified in the SPCMDm register:

- SSLni output signal value
- MSB or LSB first
- Data length
- Some of the bit rate settings
- RSPCKn polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced

SPBR holds some of the bit rate settings such as SPCKD, an SPI clock delay value, SSLND, an SSL negation delay, and SPND, a next-access delay value.

Based on the sequence length that is assigned to SPSCR, the SPI makes up a sequence comprised of a part or all of SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command comprising the sequence, the SPI sets the pointer to the SPCMD0 register, and in this manner the sequence is executed repeatedly.

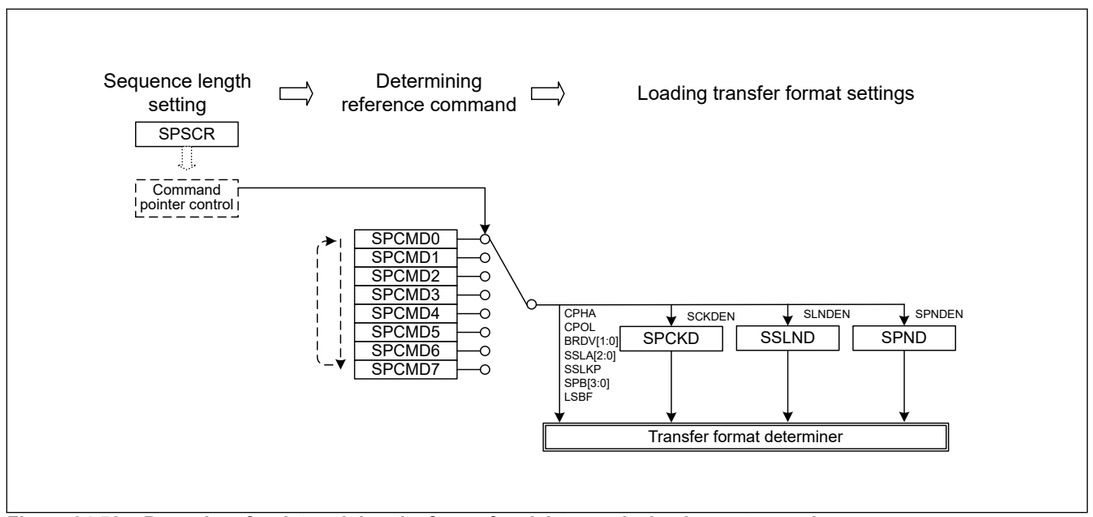


Figure 34.56 Procedure for determining the form of serial transmission in master mode

(2) 终止串行传输

SPI在发送对应于采样时序的RSPCKn边沿后终止串行传输。如果接收缓冲区中有可用空间（SPSR.SPRF标志为0），则在串行传输终止时，SPI将数据从移位寄存器复制到SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPMDm.SPB[3:0]位设置。在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(3) 顺序控制

主机模式中使用的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器确定。虽然在时钟同步操作中不输出SSLni信号，但这些设置是有效的。

SPSCR寄存器确定由SPI在主模式下执行的串行传输的序列配置。
SPCMDm寄存器中指定了以下参数：

- SSLni输出信号值
- MSB或LSB在前
- 数据长度
- 一些比特率设置
- RSPCKn极性和相位
- 是否引用SPCKD
- 是否引用SSLND
- 是否引用SPND

SPBR保存一些比特率设置，例如SPCKD、SPI时钟延迟值、SSLND、SSL否定延迟和SPND，下一次访问延迟值。

根据分配给SPSCR的序列长度，SPI组成一个序列，该序列由部分或全部SPMDm寄存器。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPSSR.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI将指针加载到SPCMD0寄存器中的命令，并在串行传输开始时将SPCMD0寄存器设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于包含序列的最终命令的串行传输后，SPI将指针设置为SPMD0寄存器，并以这种方式重复执行序列。

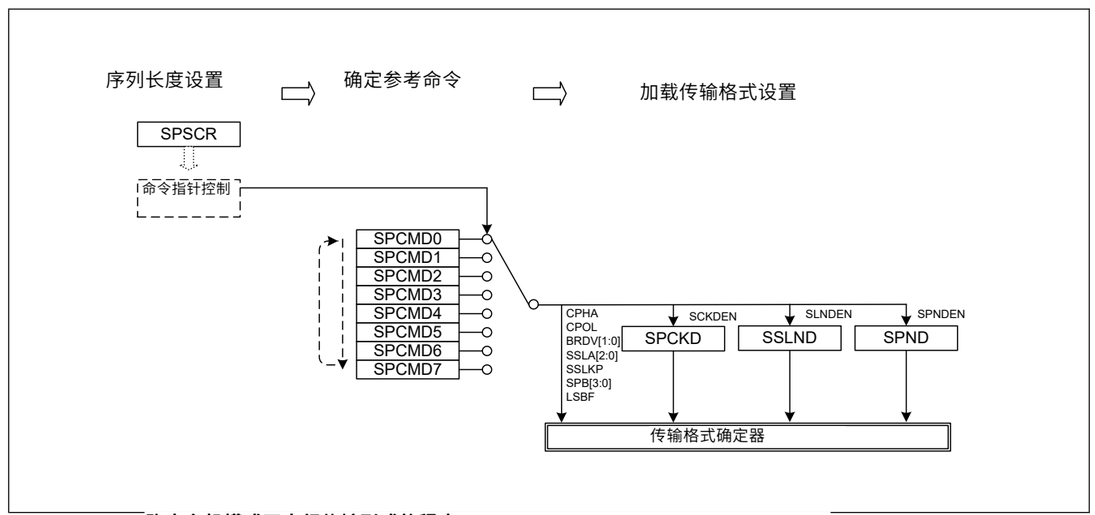


Figure 34.56 确定主机模式下串行传输形式的程序

In this section, a frame is the combination of the data (SPDR/SPDR_HA) and the settings (SPCMDm).

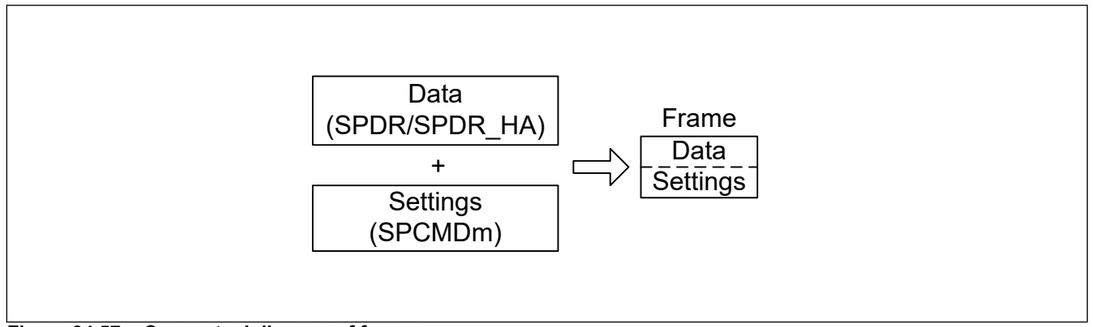


Figure 34.57 Conceptual diagram of frames

Figure 34.58 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 34.4.

在本节中，帧是数据(SPDRSPDR_HA)和设置(SPCMDm)的组合。

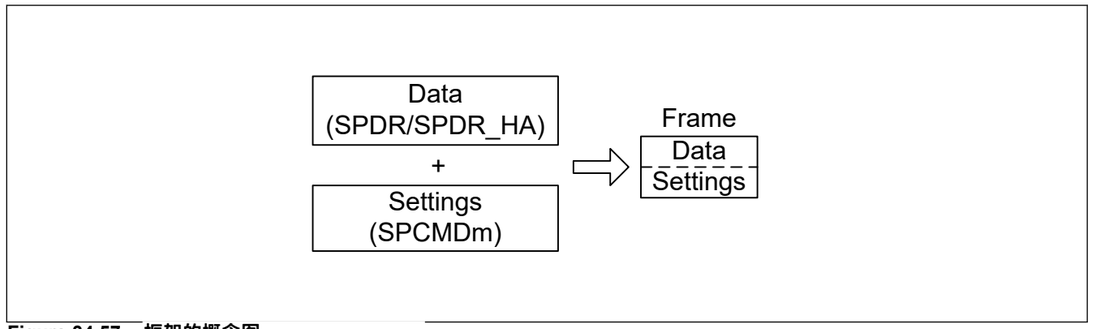


Figure 34.57 框架的概念图

图34.58显示了在表34.4中的设置指定的操作序列中命令与发送和接收缓冲区之间的关系。

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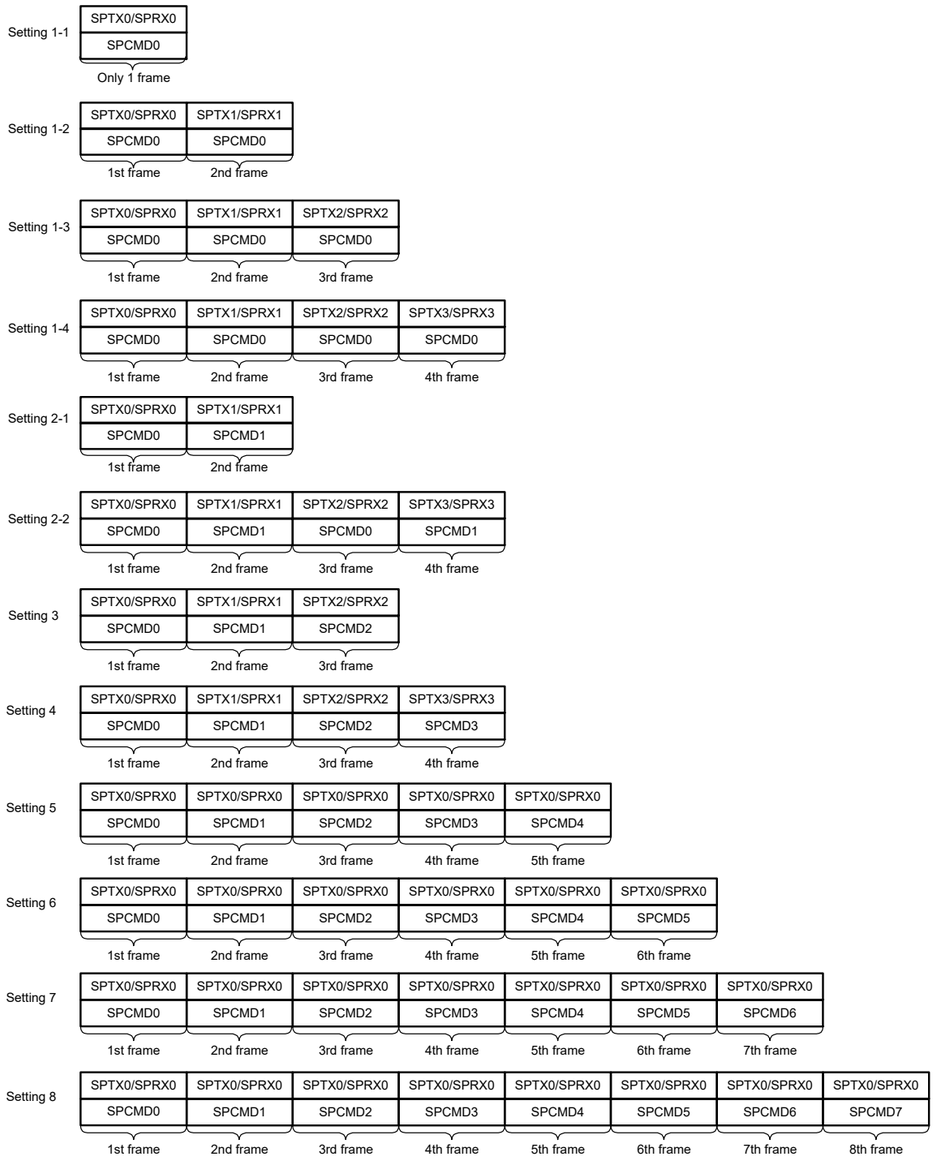

Figure 34.58 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Initialization flow

Figure 34.59 shows an example of initialization flow for clock synchronous operation when the SPI is used in master mode. For information on how to set up the ICU, DMAC or DTC, and I/O ports, see the descriptions given in the individual blocks.

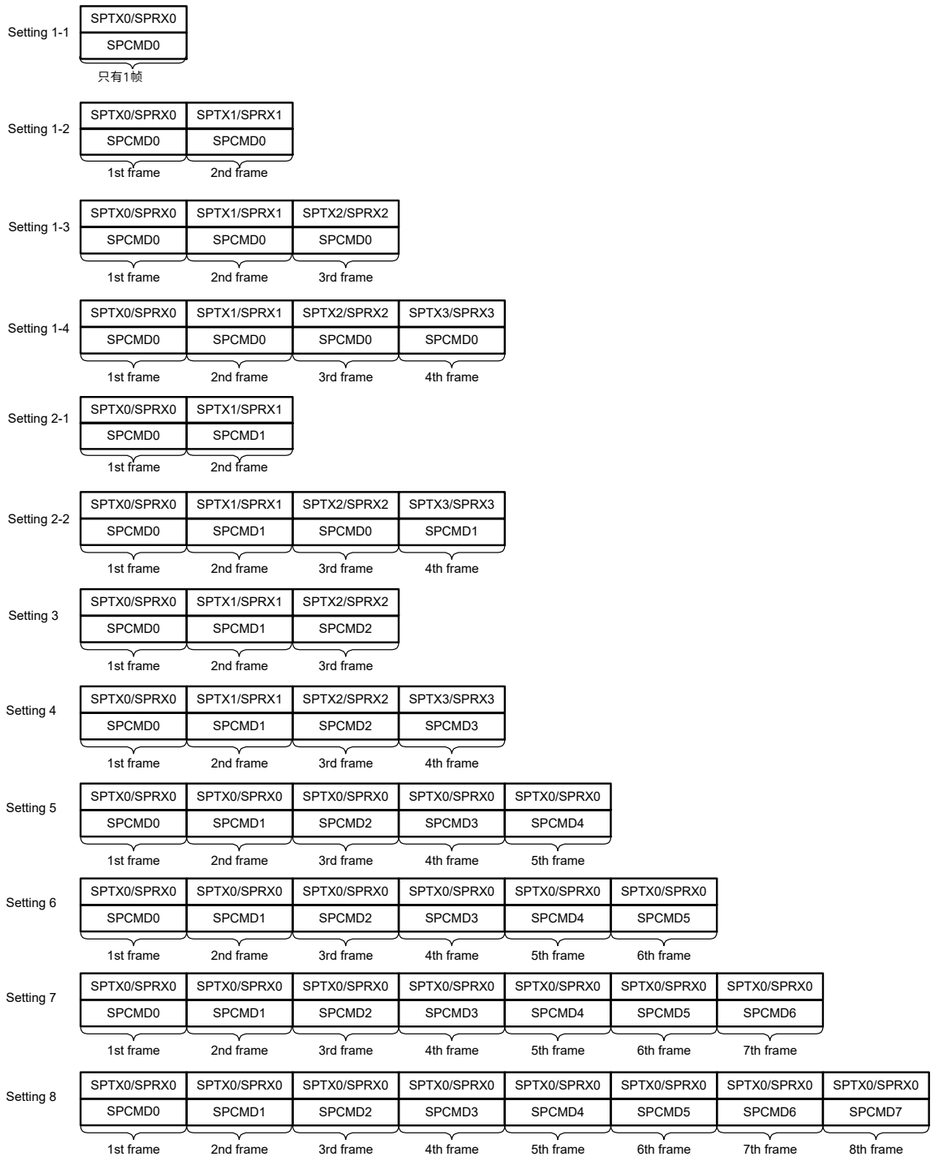

Figure 34.58 顺序操作中SPI命令寄存器与发送接收缓冲区的对应关系

(4) 初始化流程

图34.59显示了在主模式下使用SPI时时钟同步操作的初始化流程示例。
有关如何设置ICU、DMAC或DTC以及IO端口的信息，请参阅各个块中给出的说明。

RA生态工作室

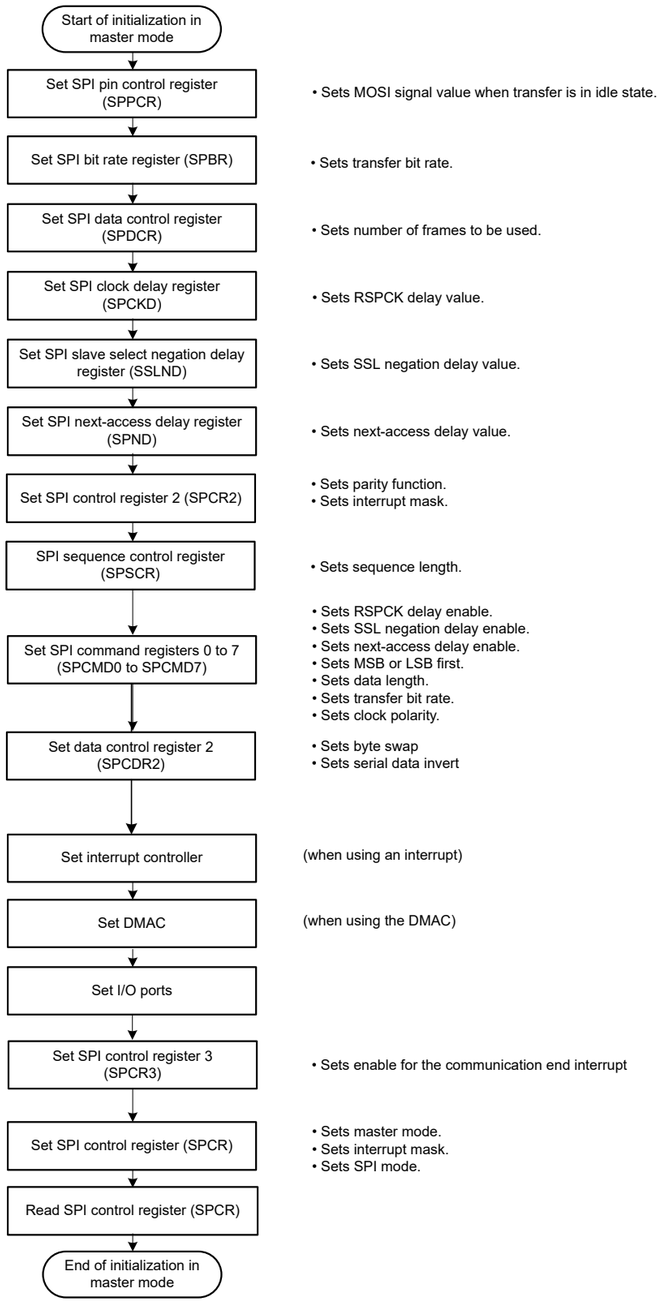

Figure 34.59 Example of initialization flow in master mode for clock synchronous operation

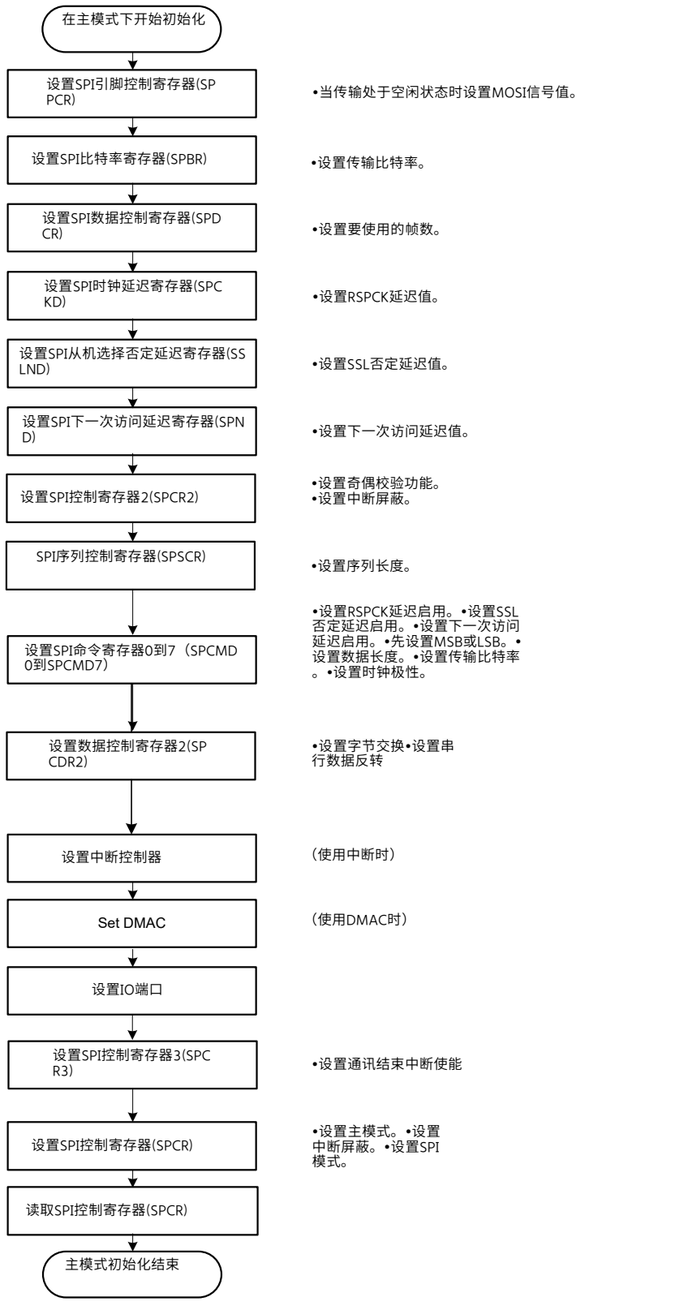

Figure 34.59 时钟同步操作的主模式初始化流程示例

(5) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see (9) Software processing flow in section 34.3.11.1. Master mode operation. Mode fault errors do not occur in clock synchronous operation.

34.3.12.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal. The SSL0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty regardless of the receive buffer.

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bits setting. For details on the SPI transfer format, see section 34.3.5. Transfer Formats.

(3) Initialization flow

Figure 34.60 shows an example of initialization flow for clock synchronous operation when the SPI is used in slave mode. For a description of how to set up the ICU, DTC, and I/O ports, see the descriptions given in the individual blocks.

(5) 软件处理流程

时钟同步主机操作期间的软件处理与SPI主机操作相同。详见34.3.11.1节（9）软件处理流程。主模式操作。时钟同步操作中不会发生模式故障错误。

34.3.12.2 从模式操作

(1) 开始串行传输

当SPCR.SPMS位为1时，第一个RSPCKn边沿触发SPI中串行传输的开始，并且SPI驱动MISon输出信号。SSL0输入信号不用于时钟同步操作。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(2) 终止串行传输

SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间（SPSR.SPRF标志为0）时，串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区无关。

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。有关SPI传输格式的详细信息，请参见第34.3.5节。传输格式。

(3) 初始化流程

图34.60显示了在从模式下使用SPI时时钟同步操作的初始化流程示例。
有关如何设置ICU、DTC和IO端口的说明，请参见各个块中给出的说明。

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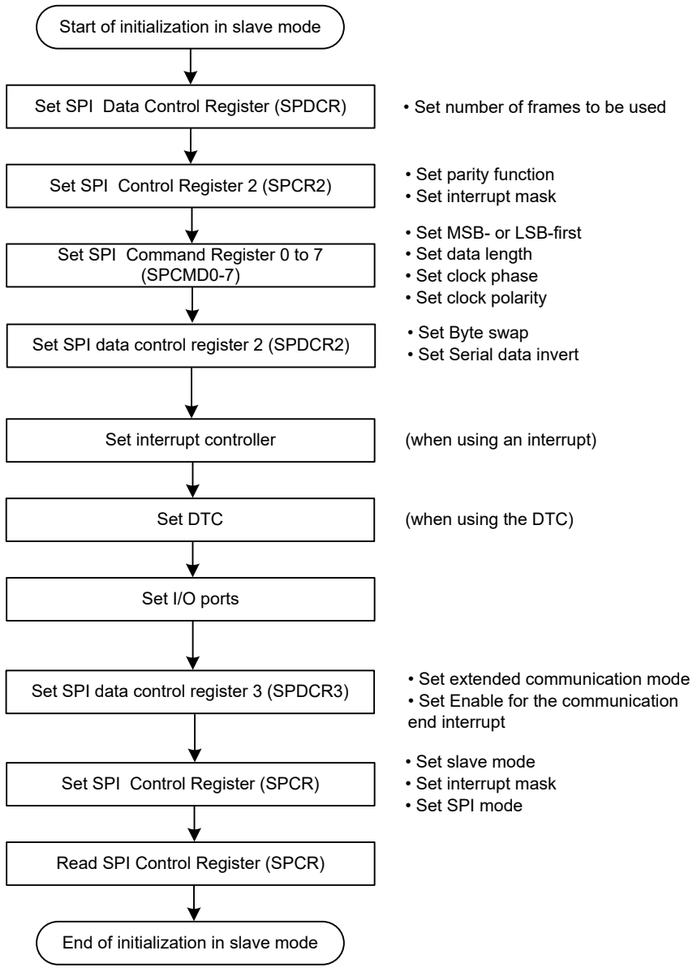

Figure 34.60 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see (6)Software processing flow. Mode fault errors do not occur in clock synchronous mode.

34.3.13 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input and output paths of the shift register, establishing a loopback mode. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

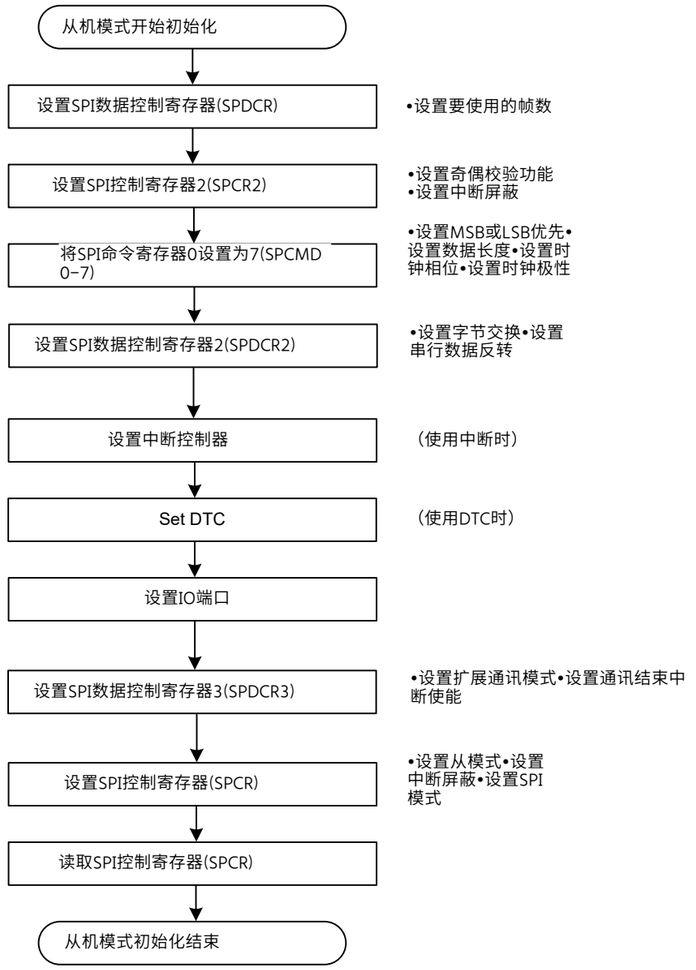

Figure 34.60 时钟同步操作的从模式初始化流程示例

(4) 软件处理流程

时钟同步从机操作期间的软件处理与SPI从机操作相同。详见（6）软件处理流程。时钟同步模式下不会发生模式故障错误。

34.3.13 Loopback Mode

当向SPPCR.SPLP2位或SPPCR.SPLP位写入1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，或者如果SPCR.MSTR位为0，连接移位寄存器的输入和输出路径，建立环回模式。如果SPCR.MSTR位为1，SPI不关闭MOSIn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则SPI不关闭MISOn引脚和移位寄存器之间的路径。这称为环回模式。当在环回模式下执行串行传输时，SPI的发送数据或反向发送数据将成为SPI的接收数据。

Table 34.14 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 34.61 shows the configuration of the shift register I/O paths when the SPI in master mode is set to loopback mode (SPPCR.SPLP2 = 0, SPPCR.SPLP = 1).

Table 34.14 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

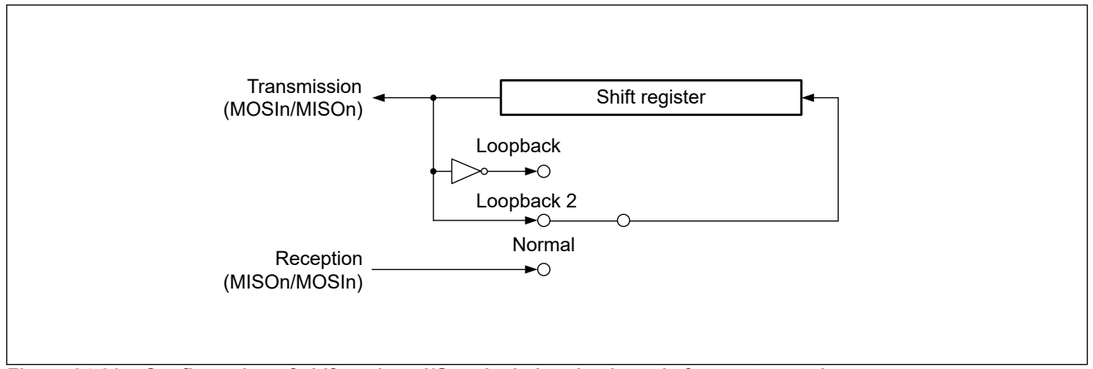

Figure 34.61 Configuration of shift register I/O paths in loopback mode for master mode

34.3.14 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. To detect defects in the parity bit adding unit and error detecting unit, the parity circuit performs self-diagnosis as shown in Figure 34.62.

表34.14列出了SPLP2和SPLP位与接收数据之间的关系。图34.61显示了当主模式下的SPI设置为环回模式（SPPCR.SPLP2=0，SPPCR.SPLP=1）时移位寄存器IO路径的配置。

Table 34.14 SPLP2和SPLP位设置和接收数据

SPPCR.SPLP2 bit	SPPCR.SPLP bit	接收数据
0	0	从MOSIn引脚或MIOn引脚输入数据
0	1	反相传输数据
1	0	传输数据
1	1	传输数据

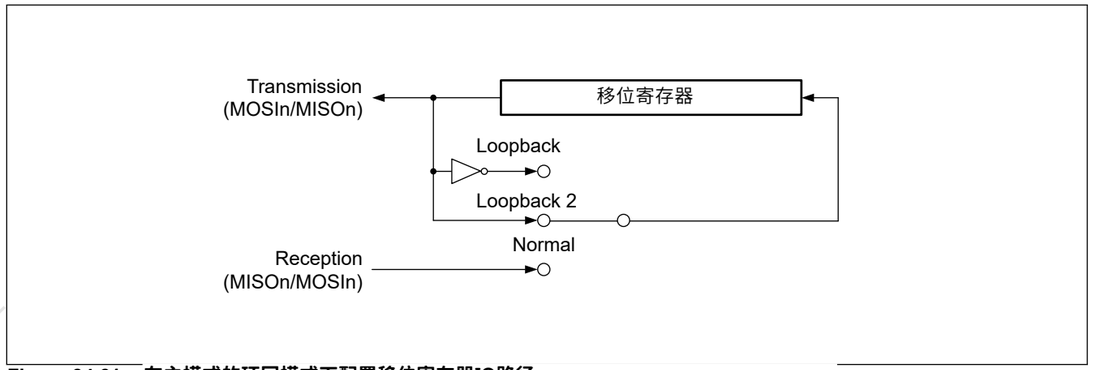

Figure 34.61 在主模式的环回模式下配置移位寄存器IO路径

34.3.14 奇偶校验位功能自诊断

奇偶校验电路由用于发送数据的奇偶校验位添加单元和用于接收数据的错误检测单元组成。为了检测奇偶校验位添加单元和错误检测单元中的缺陷，奇偶校验电路执行自诊断，如图所示Figure 34.62.

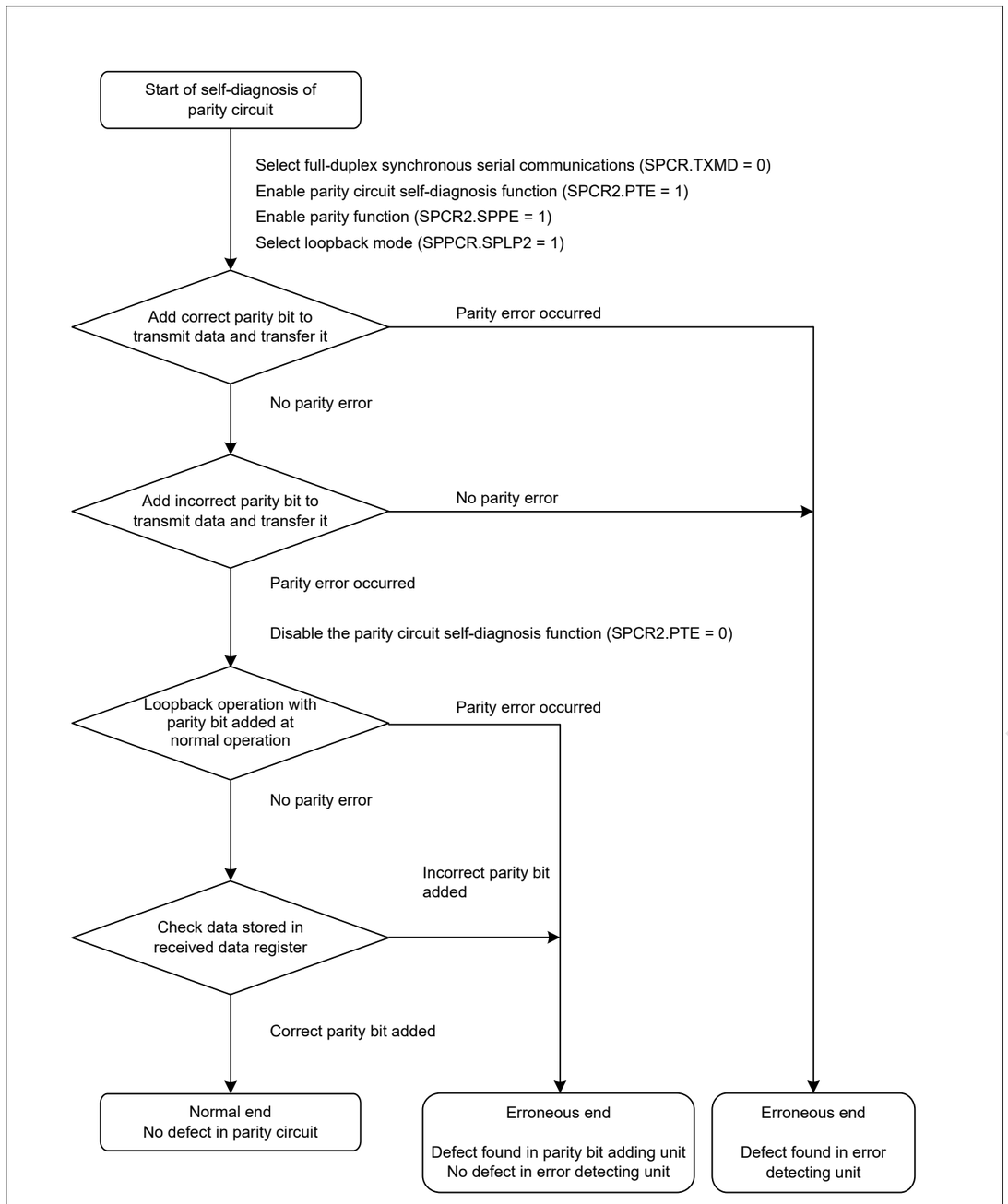

Figure 34.62 Self-diagnosis flow for parity circuit

34.3.15 Interrupt Sources

The SPI has the following interrupt sources:

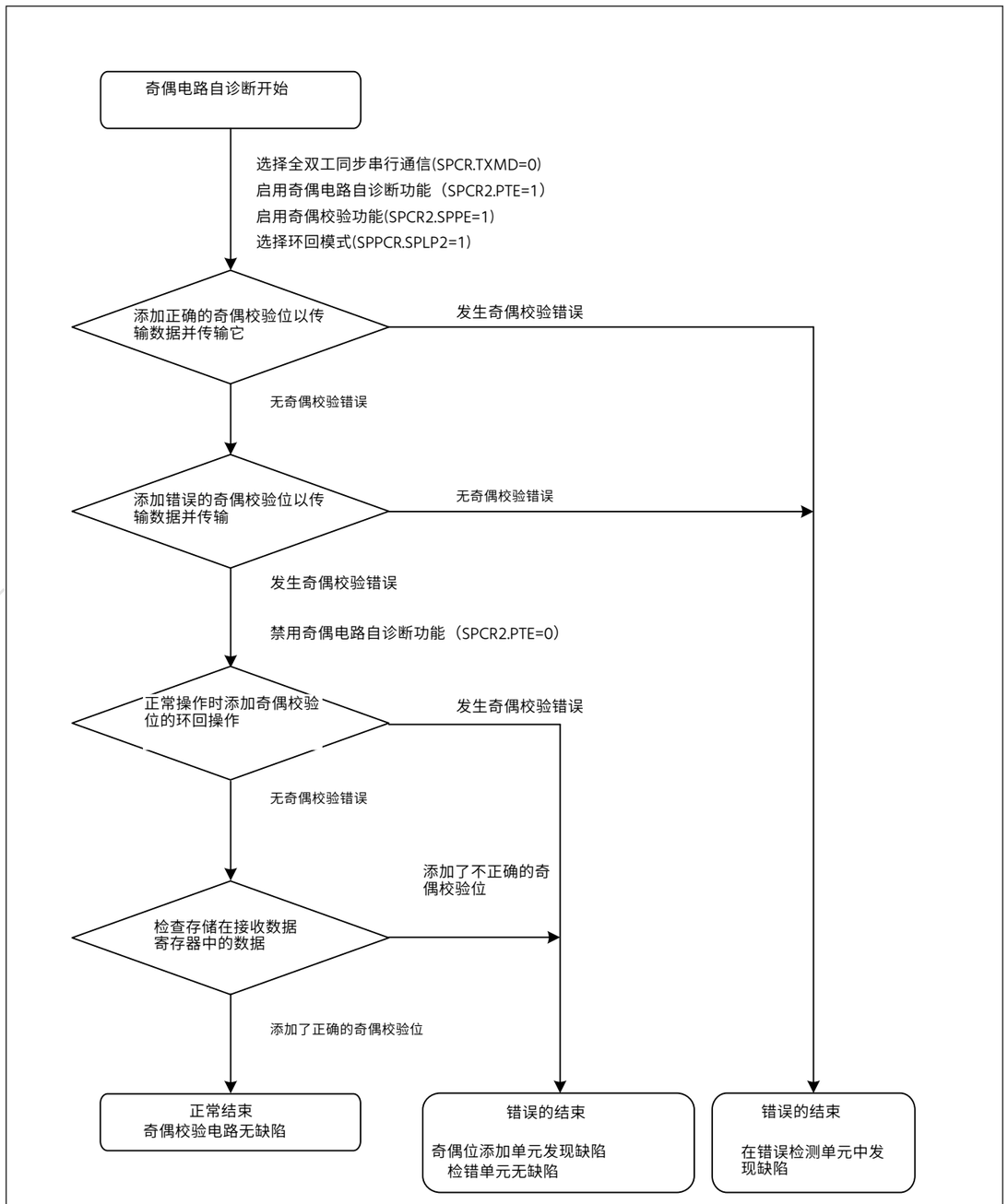

Figure 34.62 奇偶校验电路的自诊断流程

34.3.15 中断源

SPI有以下中断源：

- Receive buffer full
- Transmit buffer empty
- SPI error (mode-fault, underrun, overrun, or parity error)
- SPI idle
- Communication-end

The DMAC or DTC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for the SPIi_SPEI (SPI error interrupt) is allocated to interrupt requests on mode-fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the SPI are listed in Table 34.15. An interrupt is generated on satisfaction of one of the interrupt conditions in Table 34.15. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DMAC or DTC to perform data transmission and reception, you must first set up the DMAC or DTC to be in a transfer-enabled status before setting the SPI. For information on setting up the DMAC or DTC, see section 16, DMA Controller (DMAC) and section 17, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRn.IR flag is 1, the interrupt is not output as a request for the ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request is output when the ICU.IELSRn.IR flag becomes 0. A retained interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be set to 0.

Table 34.15 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DTC/DMAC activation
Receive buffer full	SPIi_SPRI	The receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1	Possible
Transmit buffer empty	SPIi_SPTI	The transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1	Possible
SPI error (mode-fault, underrun, overrun, or parity error)	SPIi_SPEI	The SPSR.MODF, OVRF, UDRF or PERF flag sets to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIi_SPII	The SPSR.IDLNF flag sets to 0 while the SPCR2.SPIIE bit is 1	Impossible
Communication-end	SPIi_SPCI	CENDIE = 1 and CENDF = 1	Impossible

34.4 Event Link Controller Event Output

The Event Link Controller (ELC) can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode-fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output

The event link output signal is output regardless of the interrupt enable bit setting.

34.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of serial transfer.

34.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmit buffer to the shift register and when the value of the SPE bit changes from 0 to 1.

●接收缓冲区已满

●发送缓冲区空

●SPI错误（模式故障、欠载、溢出或奇偶校验错误）

●SPI空闲

- Communication-end

DMAC或DTC可由接收缓冲区满或发送缓冲区空中断激活以执行数据传输。

由于SPIi_SPEI（SPI错误中断）的向量地址分配给模式错误、欠载、溢出和奇偶校验错误的中断请求，因此必须根据标志确定实际中断源。SPI的中断源在表34.15中列出。满足表34.15中的中断条件之一时会产生中断。通过数据传输清除接收缓冲区满和发送缓冲区空源。

使用DMAC或DTC进行数据收发时，必须先将DMAC或DTC设置为传输使能状态，然后再设置SPI。有关设置DMAC或DTC的信息，请参阅第16节，DMA控制器(DMAC)和第17节，数据传输控制器(DTC)。

如果在ICU.IELSRn.IR标志为1时发生发送缓冲区空或接收缓冲区满中断的条件，则该中断不会作为对ICU的请求输出，而是在内部保留（保留容量为每个请求一个请求）资源）。当ICU.IELSRn.IR标志变为0时，输出保留中断请求。当作为实际中断请求输出时，自动丢弃保留中断请求。内部保留中断请求的中断使能位（SPCR.SPTIE或SPCR.SPRIE位）也可以设置为0。

Table 34.15 SPI中断源

中断源	Symbol	中断条件	DTC/DMAC activation
接收缓冲区已满	SPIi_SPRI	当SPCR.SPRIE位为1时，接收缓冲区变满（SPSR.SPRF标志为1）	Possible
发送缓冲区为空	SPIi_SPTI	当SPCR.SPTIE位为1时，发送缓冲区变为空（SPSR.SPTEF标志为1）	Possible
SPI错误（模式错误、欠载、溢出或奇偶校验错误）	SPIi_SPEI	SPSR.MODF、OVRF、UDRF或PERF标志设置为1，而SPCR.SPEIE位为1	Impossible
SPI空闲	SPIi_SPII	SPSR.IDLNF标志设置为0，而SPCR2.SPIIE位为1	Impossible
Communication-end	SPIi_SPCI	CENDIE = 1 and CENDF = 1	Impossible

34.4 事件链接控制器事件输出

事件链接控制器(ELC)可以产生以下事件输出信号：

●接收缓冲区满事件输出

●发送缓冲区空事件输出

●模式故障、欠载、溢出或奇偶校验错误事件输出

●SPI空闲事件输出

●传输完成事件输出

无论中断允许位设置如何，都会输出事件链接输出信号。

34.4.1 接收缓冲区满事件输出

串行传输完成后，当接收到的数据从移位寄存器传输到SPDRSPDR_HA时，输出此事件信号。

34.4.2 发送缓冲区空事件输出

当要发送的数据从发送缓冲器传送到移位寄存器时，以及SPE位的值从0变为1时，输出该事件信号。

34.4.3 Mode-Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode-fault, underrun, overrun, or parity error is detected. See section 34.5.4. Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode-fault

Table 34.16 lists the conditions for occurrence of a mode-fault event.

Table 34.16 Conditions for mode-fault occurrence

SPI mode	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI operation (SPMS = 0) Slave (SPCR.MSTR = 0)	1	Not active	Event is output only when the SSLn0 pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags are set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the receive buffer contains unread data and the value of the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag is set to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

34.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

34.4.5 Communication End Event Output

In master mode, an event is output when the IDLNF flag (RSPI idle flag) changes from 1 to 0. In slave mode, an event occurs with conditions shown in Table 34.17 and Table 34.18

Table 34.17 Communication End Event Generating Conditions (transmit-receive/transmit slave mode)

	Transmit Buffer Status	Shift Register Status	Others
SPI operation (SPMS = 0)	Empty	Empty	SSL0 input is negated
Clock synchronous operation (SPMS = 1)	Empty	Empty	The last even edge of RSPCK of last data was detected (CPHA = 1)

Table 34.18 Communication End Event Generating Conditions (receive only slave mode)

	Others
SPI operation (SPMS = 0)	SSL0 input is negated
Clock synchronous operation (SPMS = 1)	The last even edge of RSPCK of last data was detected (CPHA = 1)

Regardless of master mode or slave mode, no event is output when 0 is written to the SPCR.SPE bit during transmission or when the SPCR.SPE bit is cleared due to a mode fault error or an underrun error.

34.4.3 模式故障、欠载、溢出或奇偶校验错误事件输出

当检测到模式故障、欠载、溢出或奇偶校验错误时，输出此事件信号。请参见第34.5.4节。如果使用此事件信号，则对模式故障、欠载、溢出或奇偶校验错误事件输出的约束。

(1) Mode-fault

表34.16列出了模式故障事件发生的条件。

Table 34.16 模式故障发生的条件

SPI模式	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI操作(SPMS=0)从机(SPCR.MSTR=0)	1	不活跃	只有在传输过程中禁用SSLn0引脚时才会输出事件

(2) Underrun

当串行传输开始而传输数据尚未准备好，并且SPCR.MSTR位的值为0且SPCR.SPE位为1时，输出此事件信号以响应欠载。在这些条件下，MODF和UDRF标志设置为1。

(3) Overrun

当串行传输完成而接收缓冲区包含未读数据且SPCR.TXMD位的值为0时，输出此事件信号以响应溢出。在这些情况下，OVRF标志设置为1。

(4) 奇偶校验错误

该事件信号是响应在串行传输完成时检测到的奇偶校验错误而输出的，而SPCR中的TXMD位为0，SPCR2中的SPPE位的值为1。

34.4.4 SPI空闲事件输出

(1) 在主模式

在主机模式下，当将IDLNF标志（SPI空闲标志）设置为0的条件成立时输出事件。

(2) 在从模式

在从机模式下，当SPCR.SPE位设置为0（SPI初始化）时，会输出一个事件。

34.4.5 通讯结束事件输出

在主机模式下，当IDLNF标志（RSPI空闲标志）从1变为0时输出事件。在从机模式下，事件发生的条件如表34.17和表34.18所示

Table 34.17 通信结束事件发生条件（发送-接收发送从模式）

	发送缓冲区状态	移位寄存器状态	Others
SPI操作(SPMS=0)	Empty	Empty	SSL0输入被否定
时钟同步操作(SPMS=1)	Empty	Empty	检测到最后一个数据的RSPCK的最后一个偶边沿(CPHA=1)

Table 34.18 通信结束事件发生条件（仅接收从模式）

	Others
SPI操作(SPMS=0)	SSL0输入被否定
时钟同步操作(SPMS=1)	检测到最后一个数据的RSPCK的最后一个偶边沿(CPHA=1)

无论主模式还是从模式，在传输过程中向SPCR.SPE位写入0或由于模式故障错误或欠载错误而清除SPCR.SPE位时，不输出任何事件。

A communication end event is output at the following timing. The communication end event output timing in master operation is omitted because it is output at the same timing as an idle event.

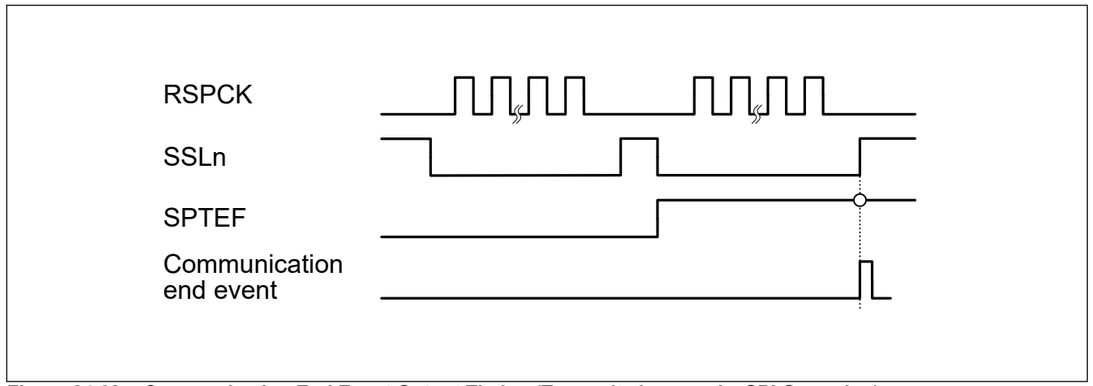

Figure 34.63 Communication End Event Output Timing (Transmit slave mode, SPI Operation)

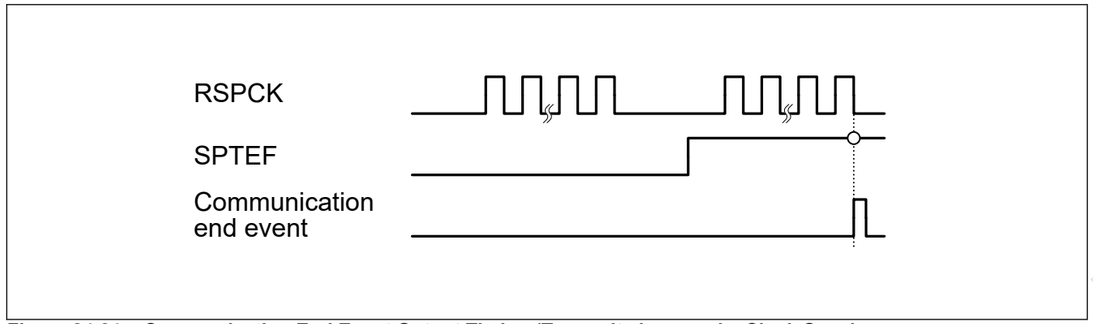

Figure 34.64 Communication End Event Output Timing (Transmit slave mode, Clock Synchronous Operation)

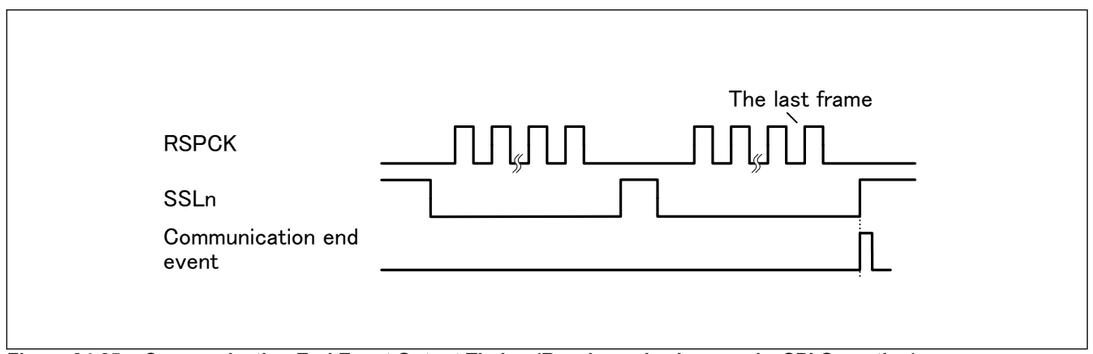

Figure 34.65 Communication End Event Output Timing (Receive only slave mode, SPI Operation)

在以下定时输出通信结束事件。主操作中的通信结束事件输出时序被省略，因为它与空闲事件在相同的时序输出。

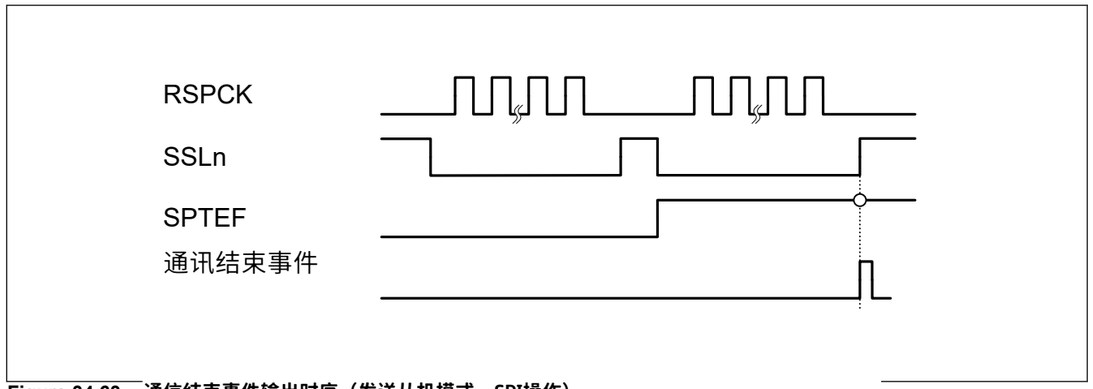

Figure 34.63 通信结束事件输出时序（发送从机模式，SPI操作）

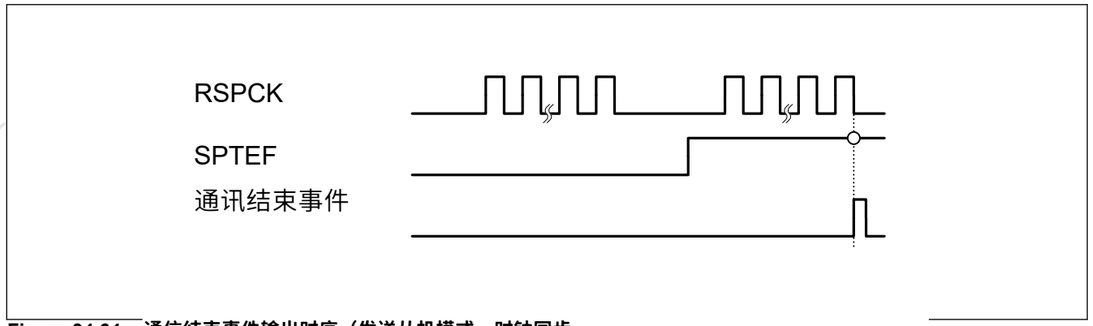

Figure 34.64 通信结束事件输出时序（发送从机模式，时钟同步 Operation)

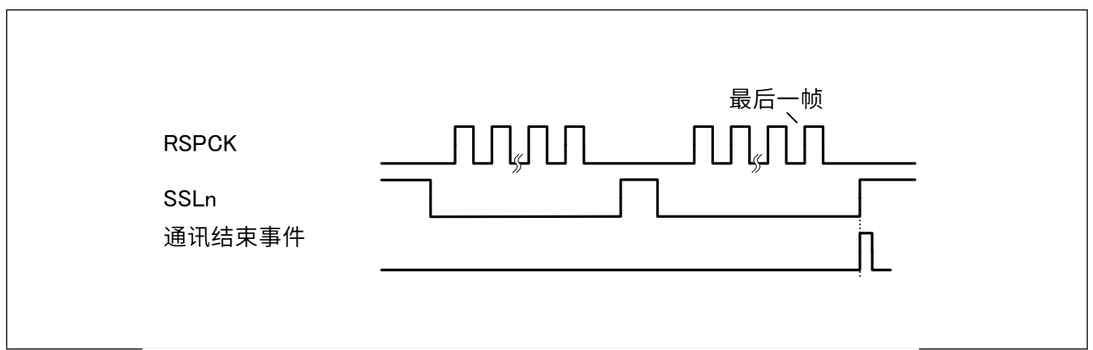

Figure 34.65 通信结束事件输出时序（仅接收从机模式，SPI操作）

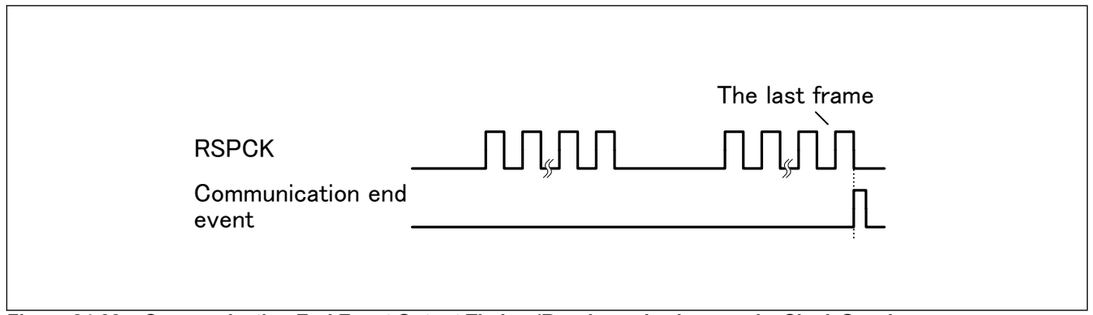

Figure 34.66 Communication End Event Output Timing (Receive only slave mode, Clock Synchronous Operation)

34.5 Usage Notes

34.5.1 Settings for the Module-Stop State

The Module Stop Control Register B (MSTPCRB) can enable or disable the SPI operation. The SPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details on the Module Stop Control Register B, see section 10, Low Power Modes.

34.5.2 Constraint on Low-Power Functions

When using the module-stop function and entering a low-power mode other than Sleep mode, set the SPCR.SPE bit to 0 before completing communication.

34.5.3 Constraints on Starting Transfer

If the ICU.IELSRn.IR flag is 1 when transfer starts, the interrupt request is internally retained, which can lead to unanticipated behavior of the ICU.IELSRn.IR flag.

To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1):

1. Confirm that transfer stopped (the SPCR.SPE bit is 0).
2. Set the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) to 0.
3. Read the associated interrupt enable bit (SPCR.SPTIE bit or SPCR.SPRIE bit) and confirm that its value is 0.
4. Set the ICU.IELSRn.IR flag to 0.

34.5.4 Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode-fault, underrun, overrun, or parity error event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

34.5.5 Constraints on the SPSR.SPRF and SPSR.SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, using the interrupts is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

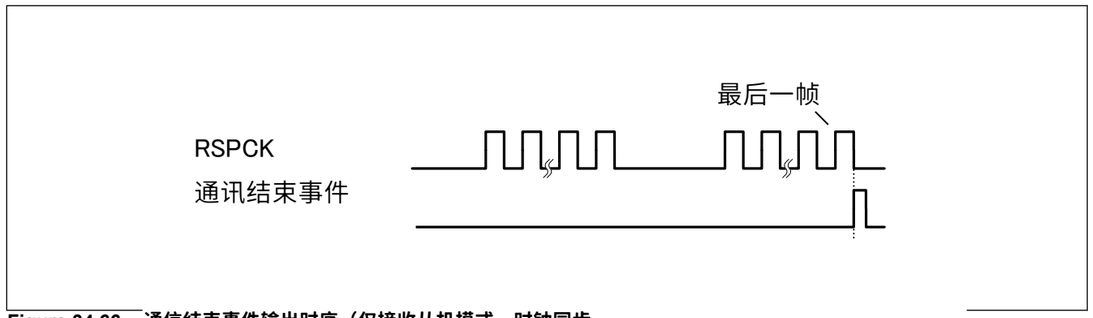

Figure 34.66 通信结束事件输出时序（仅接收从机模式，时钟同步 Operation)

34.5 使用说明

34.5.1 模块停止状态的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SPI操作。SPI在复位后最初停止。释放模块停止状态可以访问寄存器。有关模块停止控制寄存器B的详细信息，请参见第10节，低功耗模式。

34.5.2 对低功耗功能的约束

当使用模块停止功能并进入除睡眠模式以外的低功耗模式时，在完成通信之前将SPCR.SPE位设置为0。

34.5.3 开始传输的限制

如果ICU.IELSRn.IR标志在传输开始时为1，则内部保留中断请求，这可能导致ICU.IELSRn.IR标志的意外行为。

为防止这种情况发生，请使用以下程序在使能操作之前清除中断请求（通过将SPCR.SPE位设置为1）：

1.确认传输停止（SPCR.SPE位为0）。
2.将相关的中断使能位（SPCR.SPTIE位或SPCR.SPRIE位）设置为0。
3.读取相关的中断使能位（SPCR.SPTIE位或SPCR.SPRIE位）并确认其值为0。
4.将ICU.IELSRn.IR标志设置为0。

34.5.4 模式故障、欠载、溢出或奇偶校验错误事件输出的约束

如果SPI处于多主模式（当
SPCR.SPMS位为0，SPCR.MSTR位为1，SPCR.MODFEN位为1)。

34.5.5 SPSR.SPRF和SPSR.SPTEF标志的约束

如果使用轮询标志SPRF和SPTEF，则禁止使用中断，您必须设置SPCR.SPRIE和SPCR.SPTIE位为0。可以使用中断或标志，但不能同时使用。

35. Quad Serial Peripheral Interface (QSPI)

35.1 Overview

The QSPI is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface.

Table 35.1 lists the QSPI specifications, Figure 35.1 shows a block diagram, and Table 35.2 lists the I/O pins.

Table 35.1 QSPI specifications

Parameter	Specifications
Number of channels	1 channel
SPI protocols	• Single SPI protocol, extended SPI protocol to achieve full-duplex communications Note: Standard or fast reading can only be used in single SPI operation. Four-wire communications with the serial flash memory by using the QSSL, QSPCLK, QIO0, and QIO1 pins (QIO0, QSSL, and QSPCLK for output, and QIO1 for input) • Dual SPI protocol to achieve half-duplex communications Four-wire communications with the serial flash memory by using the QSSL, QSPCLK, QIO0, and QIO1 pins (QSSL and QSPCLK for output, and QIO0 and QIO1 for input and output) • Quad SPI protocol to achieve half-duplex communications Six-wire communications with the serial flash memory by using the QSSL, QSPCLK, and QIO0 to QIO3 pins (QSSL and QSPCLK for output, and QIO0 to QIO3 for input and output)
SPI mode	• SPI mode 0: The QSPCLK signal is driven low when the SPI bus is not active. • SPI mode 3: The QSPCLK signal is driven high when the SPI bus is not active.
SPI timing adjustment function	The following settings are possible to suit various types of serial flash memory device: • SPI bus reference cycle (SFMSKC.SFMDV[4:0]) • Duty cycle correction (SFMSKC.SFMDTY) • Adjustment of the number of dummy cycles (SFMSDC.SFMDN[3:0]) • Minimum width at high level for the QSSL signal (SFMSSC.SFMSW[3:0]) • QSSL signal setup time (SFMSSC.SFMSLD) • QSSL signal hold time (SFMSSC.SFMSHD) • Serial data output enable hold time (SFMSMD.SFMOEX)
ROM access mode	• Support for Standard Read, Fast Read, Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, and Fast Read Quad I/O instructions • Substitutable instruction code • Prefetch function (data are sequentially stored in a buffer after one request without waiting for further requests to read the serial flash memory) • Polling processing • SPI bus cycle extension function • XIP mode (allowing skipping of the reception of an instruction code to read the serial flash memory) Note: ROM access mode is only possible with reading .
Direct communication mode	Flexible support for a wide variety of serial flash memory instructions and functions through software control, including erase, ID read, and power-down control
Interrupt source	Error interrupts
Module-stop function	Module-stop state can be set to reduce power consumption.
TrustZone Filter	Security attribution is always non-secure

35. 四路串行外设接口(QSPI)

35.1 Overview

QSPI是一种存储器控制器，用于连接串行ROM（非易失性存储器，例如串行闪存、串行具有SPI兼容接口的EEPROM或串行FeRAM）。

表35.1列出了QSPI规范，图35.1显示了框图，表35.2列出了IO引脚。

Table 35.1 QSPI specifications

Parameter	Specifications
通道数	1 channel
SPI协议	• 单SPI协议，扩展SPI协议实现全双工通信 Note: 标准或快速读取只能在单个SPI操作中使用。 使用QSSL、QSPCLK、QIO0和串行闪存进行四线通信 QIO1引脚（QIO0、QSSL和QSPCLK用于输出，QIO1用于输入） • 双SPI协议实现半双工通信 使用QSSL、QSPCLK、QIO0和串行闪存进行四线通信 QIO1引脚（QSSL和QSPCLK用于输出，QIO0和QIO1用于输入和输出） • QuadSPI协议实现半双工通信 通过使用QSSL、QSPCLK和QIO0与串行闪存进行六线通信 QIO3引脚（QSSL和QSPCLK用于输出，QIO0到QIO3用于输入和输出）
SPI模式	• SPI模式0：当SPI总线处于非活动状态时，QSPCLK信号被驱动为低电平。 • SPI模式3：当SPI总线不活动时，QSPCLK信号被驱动为高电平。
SPI时序调整功能	可以进行以下设置以适应各种类型的串行闪存设备：● SPI总线参考周期(SFMSKC.SFMDV[4:0]) • 占空比校正(SFMSKC.SFMDTY) • 调整虚拟周期数(SFMSDC.SFDMN[3:0]) • QSSL信号的高电平最小宽度(SFMSSC.SFMSW[3:0]) • QSSL信号建立时间(SFMSSC.SFMSLD) • QSSL信号保持时间(SFMSSC.SFMSHD) • 串行数据输出使能保持时间(SFMSMD.SFMOEX)
ROM访问模式	• 支持标准读取、快速读取、快速读取双输出、快速读取双IO、快速读取四路输出和快速读取四路IO指令 • 可替换指令代码 • 预取功能（数据在一个请求后顺序存储在缓冲区中，无需等待进一步的请求来读取串行闪存） • 轮询处理 • SPI总线周期扩展功能 ●XIP模式（允许跳过接收指令码来读取串行闪存）注意： ROM访问模式仅适用于读取。
直接通讯方式	通过软件控制灵活支持各种串行闪存指令和功能，包括擦除、ID读取和断电控制
中断源	错误中断
Module-stop function	可设置模块停止状态以降低功耗。
TrustZone Filter	安全归因始终是不安全的

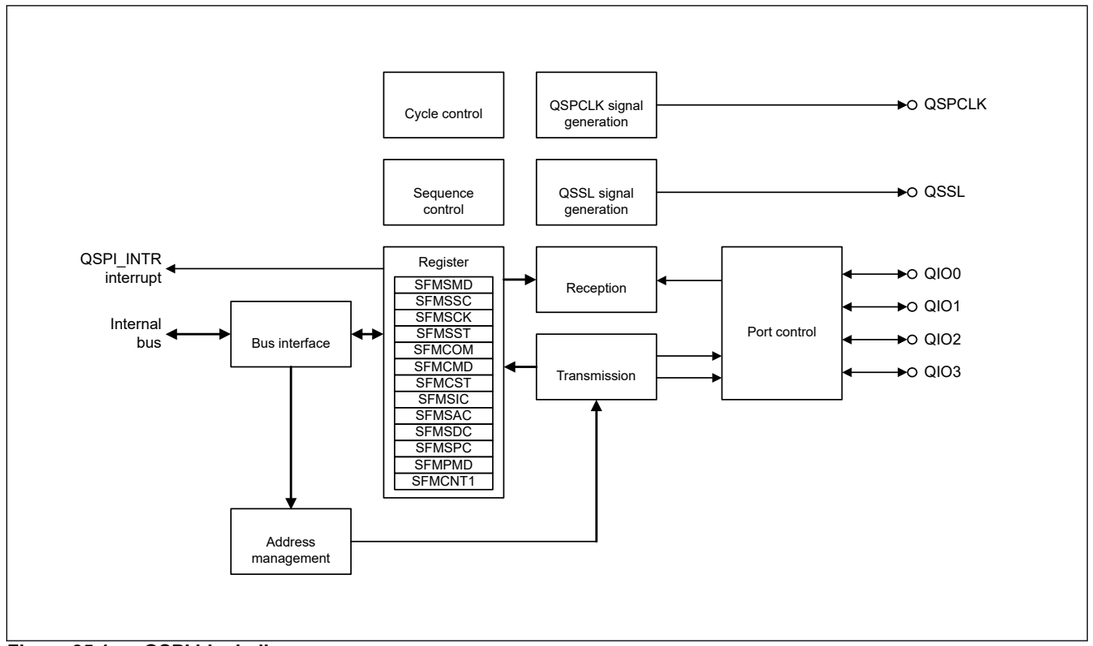

Figure 35.1 QSPI block diagram

Table 35.2 QSPI I/O pins

Function	Pin name	I/O	Description
QSPI	QSPCLK	Output	QSPI clock output pin.
	QSSL	Output	QSPI slave output pin.
	QIO0 to QIO3	I/O	Data0 to Data3

35.2 Register Descriptions

35.2.1 SFMSMD : Transfer Mode Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SFMCCE	—	—	—	SFMOSW	SFMOHW	SFMOEX	SFMMD3	SFMPAE	SFMPFE	SFMSE[1:0]		—	SFMRM[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

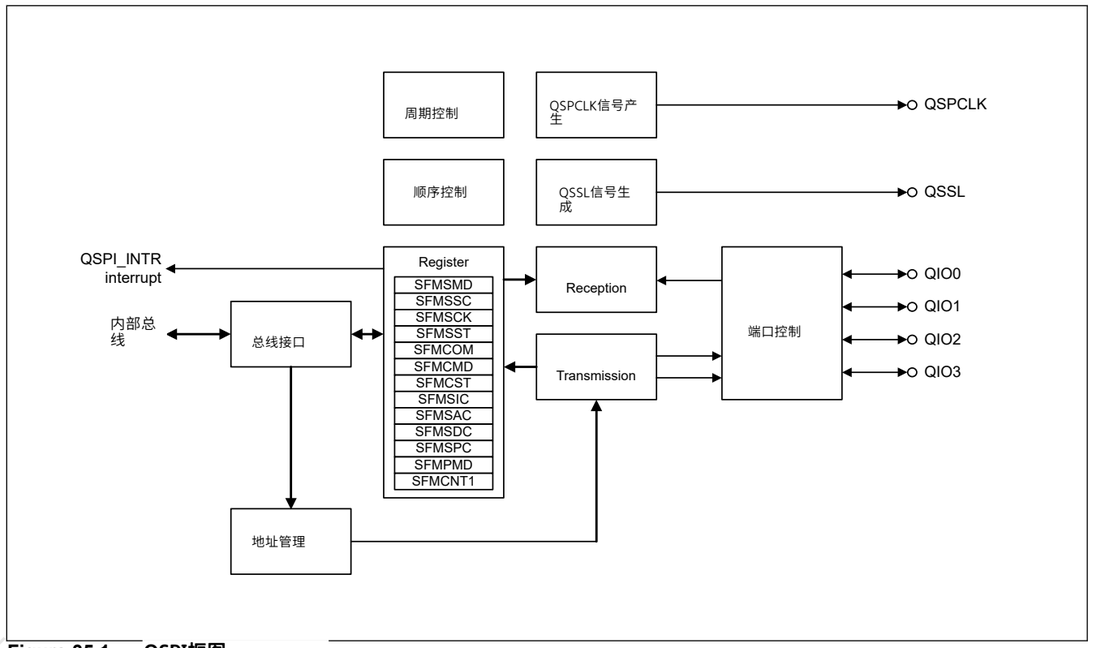

Figure 35.1 QSPI框图

Table 35.2 QSPI I/O pins

Function	引脚名称	I/O	Description
QSPI	QSPCLK	Output	QSPI时钟输出引脚。
	QSSL	Output	QSPI从机输出引脚。
	QIO0 to QIO3	I/O	Data0 to Data3

35.2 注册说明

35.2.1 SFMSMD:传输模式控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SFMCCE	—	—	—	SFMOSW	SFMOHW	SFMOEX	SFMMD3	SFMPAE	SFMPFE	SFMSE[1:0]		—	SFMRM[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	SFMRM[2:0]	Serial interface read mode select 0 0 0: Standard Read 0 0 1: Fast Read 0 1 0: Fast Read Dual Output 0 1 1: Fast Read Dual I/O 1 0 0: Fast Read Quad Output 1 0 1: Fast Read Quad I/O Others: Setting prohibited	R/W
3	—	This bit is read as 0. The write value should be 0.	R/W
5:4	SFMSE[1:0]	QSSL extension function select after SPI bus access 0 0: Do not extend QSSL 0 1: Extend QSSL by 33 QSPCLK 1 0: Extend QSSL by 129 QSPCLK 1 1: Extend QSSL infinitely	R/W
6	SFMPFE	Prefetch function select 0: Disable function 1: Enable function	R/W
7	SFMPAE	Function select for stopping prefetch at locations other than on byte boundaries*1 0: Disable function 1: Enable function	R/W
8	SFMMD3	SPI mode select. 0: SPI mode 0 1: SPI mode 3	R/W
9	SFMOEX	Extension select for the I/O buffer output enable signal for the serial interface 0: Do not extend 1: Extend by 1 QSPCLK	R/W
10	SFMOHW	Hold time adjustment for serial transmission 0: Do not extend high-level width of QSPCLK during transmission 1: Extend high-level width of QSPCLK by 1 PCLKA during transmission	R/W
11	SFMOSW	Setup time adjustment for serial transmission 0: Do not extend low-level width of QSPCLK during transmission 1: Extend low-level width of QSPCLK by 1 PCLKA during transmission	R/W
14:12	—	These bits are read as 0. The write value should be 0.	R/W
15	SFMCCE	Read instruction code select 0: Uses automatically generated SPI instruction code*2 1: Use instruction code in the SFMSIC register	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The QSPI outputs additional one clock without accompanying data reception. For details, see section 35.5.9. Serial Data Receiving Latency.

Note 2. When QSPI accesses serial flash memory, the instruction code is based on the SFMSAC register and SFMSMD register settings. See section 35.6.1. SPI Instructions That Are Automatically Generated.

35.2.2 SFMSSC : Chip Selection Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	SFMSLD	SFMSHD	SFMSW[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

Bit	Symbol	Function	R/W
2:0	SFMRM[2:0]	串行接口读取模式选择 000：标准读取001：快速读取 010：快速读取双路输出011： 快速读取双路IO100：快速读取 四路输出101：快速读取四路IO 其他：禁止设置	R/W
3	—	该位读取为0。写入值应为0。	R/W
5:4	SFMSE[1:0]	SPI总线访问后QSSL扩展功能选择 00：不扩展QSSL01：将QSSL扩展3 3个QSPCLK10：将QSSL扩展129个Q SPCLK11：无限扩展QSSL	R/W
6	SFMPFE	预取功能选择 0：禁用功能1：启 用功能	R/W
7	SFMPAE	用于在字节边界以外的位置停止预取的功能选择*1 0：禁用功能1：启 用功能	R/W
8	SFMMD3	SPI模式选择。 0：SPI模式01 ：SPI模式3	R/W
9	SFMOEX	串行接口的IO缓冲器输出使能信号的扩展选择 0：不扩展1：扩展1个QS PCLK	R/W
10	SFMOHW	串行传输的保持时间调整 0：在传输过程中不扩展QSPCLK的高电平宽度1：在传输过程中将QSPCL K的高电平宽度扩展1PCLKA	R/W
11	SFMOSW	串行传输的建立时间调整 0：在传输过程中不扩展QSPCLK的低电平宽度1：在传输过程中将QSPC LK的低电平宽度扩展1PCLKA	R/W
14:12	—	这些位被读取为0。写入值应为0。	R/W
15	SFMCCE	读取指令代码选择 0：使用自动生成的SPI指令代码*2 1：使用SFMSIC寄存器中的指令码	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.QSPI输出额外的1个时钟而不伴随数据接收。有关详细信息，请参阅第35.5.9节。串行数据接收Latency.

注2.QSPI访问串行闪存时，指令代码基于SFMSAC寄存器和SFMSMD寄存器设置。请参阅第35.6.1节。自动生成的SPI指令。

35.2.2 SFMSSC:芯片选择控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x004

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	SFMSLD	SFMSHD	SFMSW[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

Bit	Symbol	Function	R/W
3:0	SFMSW[3:0]	Minimum high-level width select for QSSL signal 0x0: 1 QSPCLK 0x1: 2 QSPCLK 0x2: 3 QSPCLK 0x3: 4 QSPCLK 0x4: 5 QSPCLK 0x5: 6 QSPCLK 0x6: 7 QSPCLK 0x7: 8 QSPCLK 0x8: 9 QSPCLK 0x9: 10 QSPCLK 0xA: 11 QSPCLK 0xB: 12 QSPCLK 0xC: 13 QSPCLK 0xD: 14 QSPCLK 0xE: 15 QSPCLK 0xF: 16 QSPCLK	R/W
4	SFMSHD	QSSL Signal Hold Time 0: QSSL outputs high after 0.5 QSPCLK cycles from the last rising edge of QSPCLK. 1: QSSL outputs high after 1.5 QSPCLK cycles from the last rising edge of QSPCLK.	R/W
5	SFMSLD	QSSL Signal Setup Time 0: QSSL outputs low before 0.5 QSPCLK cycles from the first rising edge of QSPCLK. 1: QSSL outputs low before 1.5 QSPCLK cycles from the first rising edge of QSPCLK.	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

35.2.3 SFMSKC : Clock Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	SFMDTY	SFMDV[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
3:0	SFMSW[3:0]	QSSL信号的最小高电平宽度选择 0x0: 1 QSPCLK 0x1: 2 QSPCLK 0x2: 3 QSPCLK 0x3: 4 QSPCLK 0x4: 5 QSPCLK 0x5: 6 QSPCLK 0x6: 7 QSPCLK 0x7: 8 QSPCLK 0x8: 9 QSPCLK 0x9: 10 QSPCLK 0xA: 11 QSPCLK 0xB: 12 QSPCLK 0xC: 13 QSPCLK 0xD: 14 QSPCLK 0xE: 15 QSPCLK 0xF: 16 QSPCLK	R/W
4	SFMSHD	QSSL信号保持时间 0：从QSPCLK的最后一个上升沿起0.5个QSPCLK周期后QSSL输出高电平。1：从QSPCLK的最后一个上升沿开始1.5个QSPCLK周期后QSSL输出高电平。	R/W
5	SFMSLD	QSSL信号建立时间 0：QSSL在QSPCLK的第一个上升沿起0.5个QSPCLK周期之前输出低电平。 1：QSSL在QSPCLK的第一个上升沿起1.5个QSPCLK周期之前输出低电平。	R/W
31:6	—	这些位被读取为0。写入值应为0。	R/W

35.2.3 SFMSKC:时钟控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	SFMDTY	SFMDV[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Function	R/W
4:0	SFMDV[4:0]	Serial interface reference cycle select. (Pay attention to irregularities.) 0x00: 2 PCLKA 0x01: 3 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x02: 4 PCLKA 0x03: 5 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x04: 6 PCLKA 0x05: 7 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x06: 8 PCLKA 0x07: 9 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x08: 10 PCLKA 0x09: 11 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x0A: 12 PCLKA 0x0B: 13 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x0C: 14 PCLKA 0x0D: 15 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x0E: 16 PCLKA 0x0F: 17 PCLKA (divided by an odd number)*1section 35.2.3. SFMSKC : Clock Control Register 0x10: 18 PCLKA 0x11: 20 PCLKA 0x12: 22 PCLKA 0x13: 24 PCLKA 0x14: 26 PCLKA 0x15: 28 PCLKA 0x16: 30 PCLKA 0x17: 32 PCLKA 0x18: 34 PCLKA 0x19: 36 PCLKA 0x1A: 38 PCLKA 0x1B: 40 PCLKA 0x1C: 42 PCLKA 0x1D: 44 PCLKA 0x1E: 46 PCLKA 0x1F: 48 PCLKA	R/W
5	SFMDTYsection 35.2.3. SFMSKC : Clock Control Register	Duty ratio correction function select for the QSPCLK signal when devided by an odd number 0: Make no correction 1: Make correction	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Set the SFMDTY bit to 1 when PCLKA is to be divided by an odd number.

Bit	Symbol	Function	R/W
4:0	SFMDV[4:0]	串行接口参考周期选择。（注意违规行为。） 0x00：2PCLKA0x01：3PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x02：4PCLKA0x03：5PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x04：6PCLKA0x05：7PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x06：8PCLKA0x07：9PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x08：10PCLKA0x09：11PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x0A：12PCLKA0x0B：13PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x0C：14PCLKA0x0D：15PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x0E：16PCLKA0x0F：17PCLKA（除以奇数）*135.2.3节。SFMSKC:时钟控制寄存器 0x10: 18 PCLKA 0x11: 20 PCLKA 0x12: 22 PCLKA 0x13: 24 PCLKA 0x14: 26 PCLKA 0x15: 28 PCLKA 0x16: 30 PCLKA 0x17: 32 PCLKA 0x18: 34 PCLKA 0x19: 36 PCLKA 0x1A: 38 PCLKA 0x1B: 40 PCLKA 0x1C: 42 PCLKA 0x1D: 44 PCLKA 0x1E: 46 PCLKA 0x1F: 48 PCLKA	R/W
5	SFMDTY第35.2.3节。SFMSKC:时钟控制Register	QSPCLK信号除以奇数时的占空比校正功能选择 0：不修正1：修正	R/W
31:6	—	这些位被读取为0。写入值应为0。	R/W

注1.当PCLKA除以奇数时，将SFMDTY位设置为1。

35.2.4 SFMSST : Status Register

Base address: QSPI = 0x6400_0000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	PFOFF	PFFUL	—	PFCNT[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	PFCNT[4:0]	Number of bytes of prefetched data 0x00: 0 byte 0x01: 1 byte 0x02: 2 bytes 0x03: 3 bytes 0x04: 4 bytes 0x05: 5 bytes 0x06: 6 bytes 0x07: 7 bytes 0x08: 8 bytes 0x09: 9 bytes 0x0A: 10 bytes 0x0B: 11 bytes 0x0C: 12 bytes 0x0D: 13 bytes 0x0E: 14 bytes 0x0F: 15 bytes 0x10: 16 bytes 0x11: 17 bytes 0x12: 18 bytes Others: Reserved	R
5	—	This bit is read as 0.	R
6	PFFUL	Prefetch buffer state 0: Prefetch buffer has free space 1: Prefetch buffer is full	R
7	PFOFF	Prefetch function operating state 0: Prefetch function operating 1: Prefetch function not enabled or not operating	R
31:8	—	These bits are read as 0.	R

35.2.4 SFMSST:状态寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	PFOFF	PFFUL	—	PFCNT[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	PFCNT[4:0]	预取数据的字节数 0x00：0字节0x01：1字节0x02：2字节0x03：3字节0x04：4字节0x05：5字节0x06：6字节0x07：7字节0x08：8字节0x09：9字节0x0A：10字节0x0B：11字节0x0C：12字节0x0D：13字节0x0E：14字节0x0F：15字节0x10：16字节0x11：17字节0x12：18字节 Others: Reserved	R
5	—	该位读为0。	R
6	PFFUL	预取缓冲区状态 0：预取缓冲区有空闲空间1：预取缓冲区已满	R
7	PFOFF	预取功能运行状态 0：预取功能运行1：预取功能未使能或未运行	R
31:8	—	这些位读为0。	R

35.2.5 SFMCOM : Communication Port Register

Base address: QSPI = 0x6400_0000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SFMD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	SFMD[7:0]	Port for direct communication with the SPI bus Input and output from this port are converted to an SPI bus cycle in direct communications mode (DCOM = 1). Access to this port is ignored in ROM access mode.	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

35.2.6 SFMCMD : Communication Mode Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DCOM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCOM	Mode select for communication with the SPI bus 0: ROM access mode 1: Direct communication mode*1	R/W
31:1	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. SFMCMD.DCOM = 1 must be written when the transaction ends. For details, see section 35.10. Direct Communication Mode.

35.2.5 SFMCOM:通讯端口寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SFMD[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
7:0	SFMD[7:0]	与SPI总线直接通信的端口 此端口的输入和输出在直接通信模式(DCOM=1)下转换为SPI总线周期。在ROM访问模式下，对该端口的访问被忽略。	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

35.2.6 SFMCMD:通信模式控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DCOM
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	DCOM	与SPI总线通信的模式选择 0：ROM访问模式1：直接通信模式*1	R/W
31:1	—	这些位被读取为0。写入值应为0。	R/W

注1.SFMCMD.DCOM=1必须在事务结束时写入。有关详细信息，请参阅第35.10节。直接通信模式。

35.2.7 SFMCST : Communication Status Register

Base address: QSPI = 0x6400_0000

Offset address: 0x018

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	EROMR	—	—	—	—	—	—	COMBSY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	COMBSY	SPI bus cycle completion state in direct communication 0: No serial transfer being processed 1: Serial transfer being processed	R
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	EROMR	ROM access detection status in direct communication mode 0: ROM access not detected 1: ROM access detected	R/(W)*1
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit.

35.2.8 SFMSIC : Instruction Code Register

Base address: QSPI = 0x6400_0000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SFMCIC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SFMCIC[7:0]	Serial flash instruction code to substitute	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

35.2.7 SFMCST:通讯状态寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x018

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	EROMR	—	—	—	—	—	—	COMBSY
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	COMBSY	直接通信中的SPI总线周期完成状态 0：未处理串行传输1：正在处理串行传输	R
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	EROMR	直接通信模式下的ROM访问检测状态 0：未检测到ROM访问1：检测到ROM访问	R/(W)*1
31:8	—	这些位被读取为0。写入值应为0。	R/W

注1.该位只能写入0。

35.2.8 SMSIC:指令代码寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x020

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SFMCIC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SFMCIC[7:0]	替代的串行闪存指令代码	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

35.2.9 SFMSAC : Address Mode Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SFM4BC	—	—	SFMAS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	SFMAS[1:0]	Number of address bytes select for the serial interface 0 0: 1 byte 0 1: 2 bytes 1 0: 3 bytes 1 1: 4 bytes	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SFM4BC	Selection of instruction code automatically generated when the serial interface address width is 4 bytes 0: Do not use 4-byte address read instruction code 1: Use 4-byte address read instruction code	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

35.2.10 SFMSDC : Dummy Cycle Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SFMXD[7:0]								SFMXEN	SFMXST	—	—	SFMDN[3:0]			
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

35.2.9 SFMSAC:地址模式控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x024

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SFM4BC	—	—	SFMAS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	SFMAS[1:0]	为串行接口选择的地址字节数 00：1个字节0 1：2个字节10 ：3个字节11 ：4个字节	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	SFM4BC	串行接口地址宽度为4字节时自动生成的指令代码选择 0：不使用4字节地址读取指令码1：使用4字节地址读取指令码	R/W
31:5	—	这些位被读取为0。写入值应为0。	R/W

35.2.10 SFMSDC:虚拟周期控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x028

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SFMXD[7:0]								SFMXEN	SFMXST	—	—	SFMDN[3:0]			
重置后的值:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	SFMDN[3:0]	Number of dummy cycles select for Fast Read instructions 0x0: Default dummy cycles for each instruction: - Fast Read Quad I/O: 6 QSPCLK - Fast Read Quad Output: 8 QSPCLK - Fast Read Dual I/O: 4 QSPCLK - Fast Read Dual Output: 8 QSPCLK - Fast Read: 8 QSPCLK 0x1: 3 QSPCLK*1 0x2: 4 QSPCLK 0x3: 5 QSPCLK 0x4: 6 QSPCLK 0x5: 7 QSPCLK 0x6: 8 QSPCLK 0x7: 9 QSPCLK 0x8: 10 QSPCLK 0x9: 11 QSPCLK 0xA: 12 QSPCLK 0xB: 13 QSPCLK 0xC: 14 QSPCLK 0xD: 15 QSPCLK 0xE: 16 QSPCLK 0xF: 17 QSPCLK	R/W
5:4	—	These bits are read as 0. The write value should be 0.	R/W
6	SFMXST	XIP mode status 0: Normal (non-XIP) mode 1: XIP mode	R
7	SFMXEN	XIP mode permission 0: Prohibit XIP mode 1: Permit XIP mode	R/W
15:8	SFMXD[7:0]	Mode data for serial flash (Controls XIP mode.)*2	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. To avoid a conflict with the input/output switch of the serial flash memory pin connected to QIO0 pin, select more than four cycles of QSPCLK as the number of dummy cycles for the fast read instruction when the output enable signal is extended by setting the SFMOEX bit in the SFMSMD register to 1.
Note 2. As the mode data for serial flash memory, specify the XIP mode setting data set in actual serial flash memory.

35.2.11 SFMSPC : SPI Protocol Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SFMSDE	—	—	SFMSPI[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SFMSPI[1:0]	SPI protocol select*1 0 0: Single SPI Protocol, Extended SPI protocol 0 1: Dual SPI protocol 1 0: Quad SPI protocol 1 1: Setting prohibited	R/W

Bit	Symbol	Function	R/W
3:0	SFMDN[3:0]	为快速读取指令选择的虚拟周期数 0x0：每条指令的默认虚拟周期：快速读取四路IO：6QSPCLK快速读取四路输出：8QSPCLK快速读取双路IO：4QSPCLK快速读取双路输出：8QSPCLK快速读取：8QSPCLK 0x1: 3 QSPCLK*1 0x2: 4 QSPCLK 0x3: 5 QSPCLK 0x4: 6 QSPCLK 0x5: 7 QSPCLK 0x6: 8 QSPCLK 0x7: 9 QSPCLK 0x8: 10 QSPCLK 0x9: 11 QSPCLK 0xA: 12 QSPCLK 0xB: 13 QSPCLK 0xC: 14 QSPCLK 0xD: 15 QSPCLK 0xE: 16 QSPCLK 0xF: 17 QSPCLK	R/W
5:4	—	这些位被读取为0。写入值应为0。	R/W
6	SFMXST	XIP模式状态 0：正常（非XIP）模式1：XIP模式	R
7	SFMXEN	XIP模式权限 0：禁止XIP模式1：允许XIP模式	R/W
15:8	SFMXD[7:0]	串行闪存的模式数据（控制XIP模式。）*2	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.为避免与连接到QIO0引脚的串行闪存引脚的输入输出开关冲突，请选择4个以上的周期QSPCLK作为快速读取指令的虚拟周期数，当输出使能信号通过设置SFMSMD寄存器中的SFMOEX位为1。
注2.作为串行闪存的模式数据，指定实际串行闪存中设置的XIP模式设置数据。

35.2.11 SFMSPC:SPI协议控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SFMSDE	—	—	SFMSPI[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SFMSPI[1:0]	SPI协议选择*1 00：单SPI协议，扩展SPI协议01：双SPI协议10：四线SPI协议11：禁止设置	R/W

Bit	Symbol	Function	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	SFMSDE	QSPCLK extended selection bit when switching I/O of QIOn pin 0: No QSPCLK extension 1: QSPCLK expansion when switching I/O direction of QIOn pin	R/W
31:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The states of the QIO2 and QIO3 pins change depending on the settings of the SFMSMD.SFMRM[2:0] and SFMSPI[1:0] bits. For details, see section 35.9. QIO2 and QIO3 Pin States.

35.2.12 SFMPMD : Port Control Register

Base address: QSPI = 0x6400_0000

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SFMWPL	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	These bits are read as 0. The write value should be 0.	R/W
2	SFMWPL	WP pin level specification 0: Low level 1: High level	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

35.2.13 SFMCNT1 : External QSPI Address Register

Base address: QSPI = 0x6400_0000

Offset address: 0x804

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	QSPI_EXT[5:0]						—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
25:0	—	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	SFMSDE	QSPCLK扩展选择位在切换QIOn引脚的IO时 0：无QSPCLK扩展1：切换QIOn引脚IO方向时QSPCLK扩展	R/W
31:5	—	这些位被读取为0。写入值应为0。	R/W

注1.QIO2和QIO3引脚的状态根据SFMSMD.SFMRM[2:0]和SFMSPI[1:0]位的设置而变化。有关详细信息，请参阅第35.9节。QIO2和QIO3引脚状态。

35.2.12 SFMPMD:端口控制寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SFMWPL	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	—	这些位被读取为0。写入值应为0。	R/W
2	SFMWPL	WP引脚电平规范 0：低电平1 ：高电平	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

35.2.13 SFMCNT1：外部QSPI地址寄存器

Base address: QSPI = 0x6400_0000

Offset address: 0x804

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	QSPI_EXT[5:0]						—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
25:0	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
31:26	QSPI_EXT[5:0]	Bank switching address When accessing from 0x60000000 to 0x63FFFFFF, the address bus is set from QSPI_EXT[5:0] to the upper 6 bits of the internal bus address for the address bus. 0x00: QSPI bank 00 0x01: QSPI bank 01 0x02: QSPI bank 02 ⋮ ⋮ 0x3C: QSPI bank 60 0x3D: QSPI bank 61 0x3E: QSPI bank 62 0x3F: Setting prohibited	R/W

35.3 Memory Map

35.3.1 External Bus Space

The locations of a serial flash memory and control register on the address space are determined by the address range of the area set in the configuration.

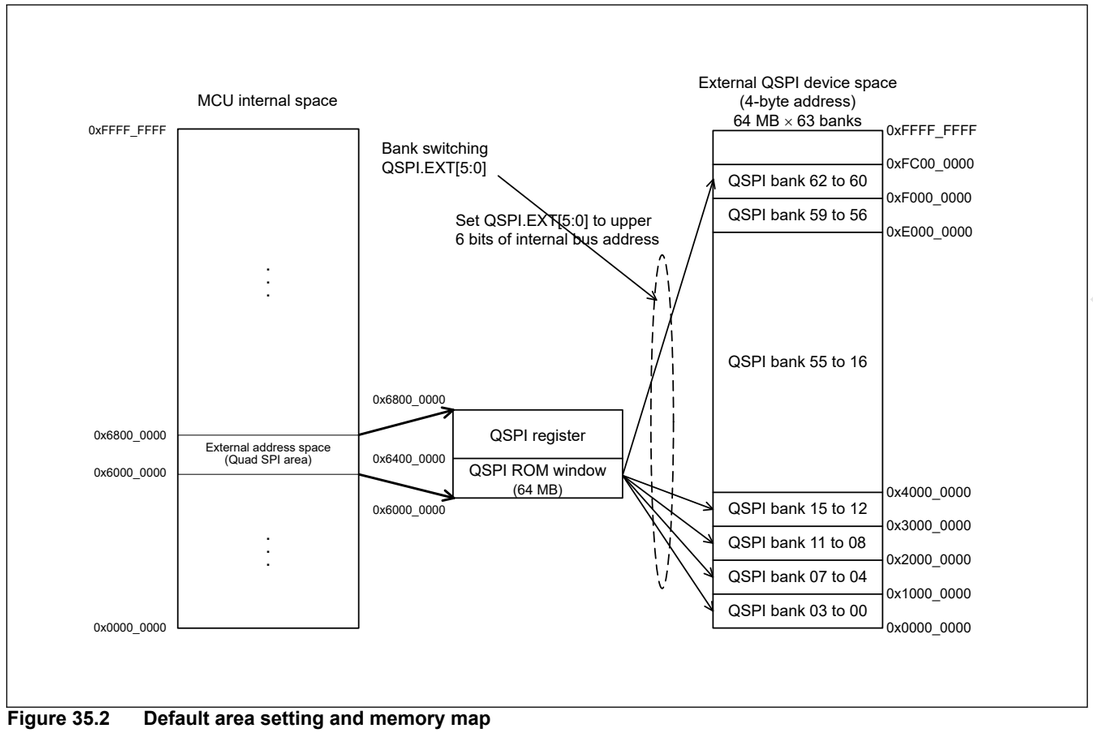

Figure 35.2 Default area setting and memory map

35.3.2 Address Width of the SPI Space and SPI Bus

The SPI space has a 32-bit address width for referencing the serial flash memory. When the SPI space is accessed for a read, an SPI bus cycle starts automatically, and data read from the serial flash is returned.

The address width of the SPI space is fixed at 32 bits. However, the address width of the SPI bus is selectable to 8, 16, 24, or 32 bits in the SFMAS[1:0] bits in the Address Mode Control Register (SFMSAC) register. If 8, 16, or 24 bits is selected as the address width of the SPI bus, only the lower part of the address used to access the SPI space is posted to the serial flash memory through the SPI bus. As a result, the mirror image of the serial flash corresponding to the address width of the SPI bus repeatedly appears in the SPI space.

Bit	Symbol	Function	R/W
31:26	QSPI_EXT[5:0]	银行转换地址 从0x60000000到0x63FFFFFF访问时，地址总线设置为QSPI_EXT[5:0]到地址总线的内部总线地址的高6位。 0x00: QSPI bank 00 0x01: QSPI bank 01 0x02: QSPI bank 02 ⋮ ⋮ 0x3C：QSPIbank600x3D：QSPIbank610x3E：QSPIbank620x3F：禁止设置	R/W

35.3 内存映射

35.3.1 外部总线空间

串行闪存和控制寄存器在地址空间上的位置由配置中设置的区域的地址范围决定。

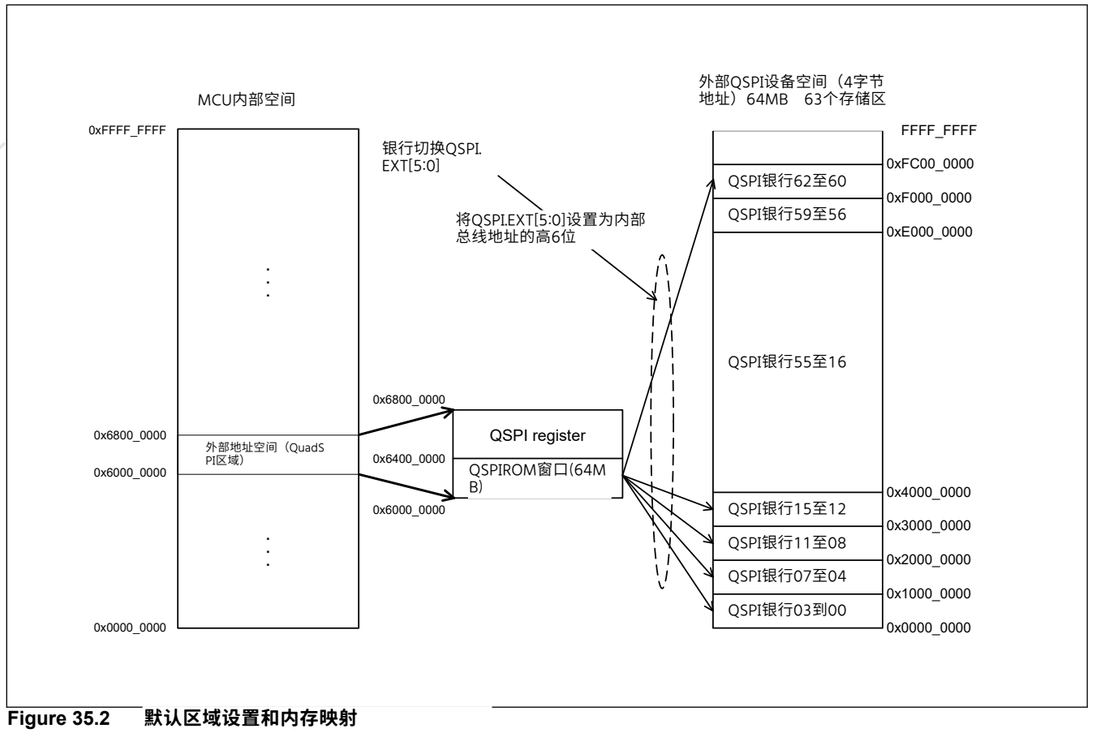

Figure 35.2 默认区域设置和内存映射

35.3.2 SPI空间和SPI总线的地址宽度

SPI空间具有32位地址宽度，用于引用串行闪存。当访问SPI空间进行读取时，会自动启动一个SPI总线周期，并返回从串行闪存读取的数据。

SPI空间的地址宽度固定为32位。但是，SPI总线的地址宽度可选择为地址模式控制寄存器(SFMSAC)寄存器中的SFMAS[1:0]位中的8、16、24或32位。如果选择8位、16位或24位作为SPI总线的地址宽度，则只有用于访问SPI空间的地址的低部分通过SPI总线发布到串行闪存中。结果，对应于SPI总线地址宽度的串行闪存的镜像在SPI空间中反复出现。

RA生态工作室

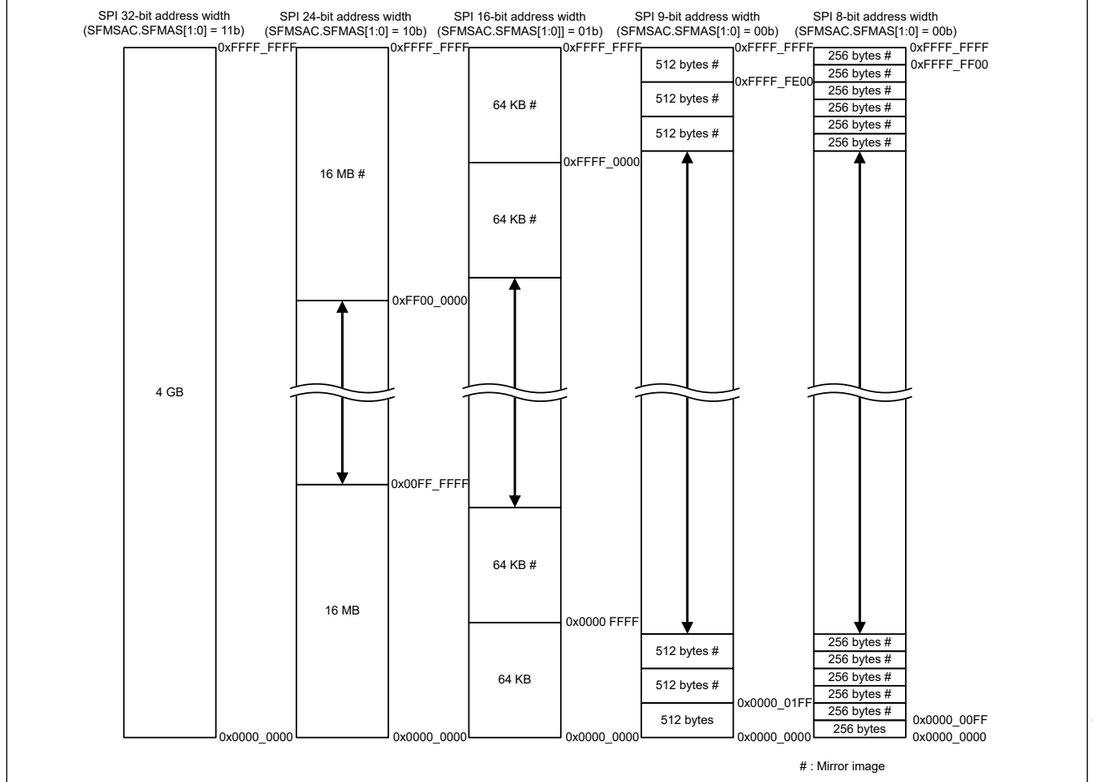

Figure 35.3 Memory map of SPI space

Note: The SPI bus address width is selectable to 8, 16, 24, or 32 bits in the SFMAS[1:0] bits in the SFMSAC register (cases 1 to 3 and 5 in the figure correspond to the respective address widths). When an 8-bit address width is selected, the address information of the ninth bit can be embedded in the Read instruction code. The memory map in case 4 in the figure is for the 9-bit address width. For details on the Read instruction, see section 35.6.2. Standard Read Instruction.

35.4 SPI Bus

35.4.1 SPI Protocol

Single SPI, extended SPI, dual SPI, and quad SPI are supported in addition to the SPI protocol used for serial flash memory connection.

The initial state of the SPI protocol is Single SPI, extended SPI and can be changed with the SFMSPI[1:0] bits in the SPI Protocol Control Register (SFMSPC) register.

The address and data pins used in the Single SPI, extended SPI protocol change depending on the setting of the serial interface read mode select bits SFMRM[2:0] in Transfer Mode Control Register (SFMSMD). Table 35.3 and Table 35.4 list the pins used for instruction code, addresses, and data in each of the SPI protocols.

Note: In read operation, the QSPI outputs additional one clock without accompanying data reception per one SPI bus cycle. For details, see section 35.5.9. Serial Data Receiving Latency.

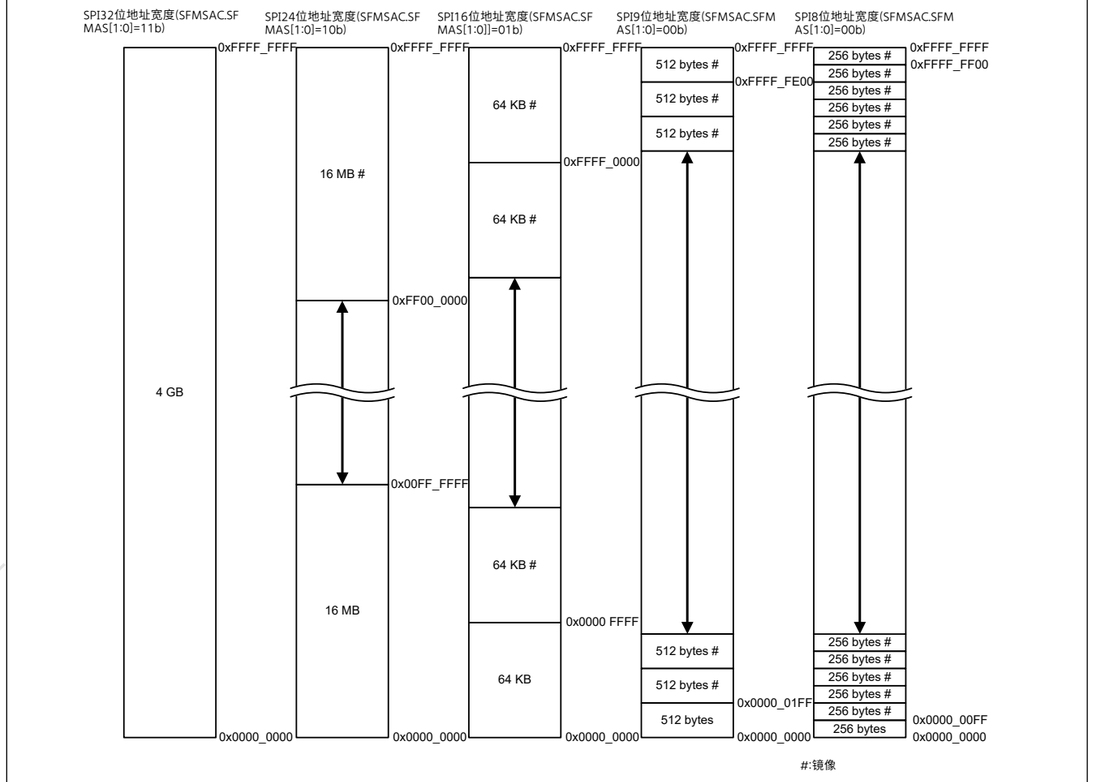

Figure 35.3 SPI空间的内存映射

Note: SPI总线地址宽度在SFMSAC寄存器的SFMAS[1:0]位中可选择为8、16、24或32位（图中的情况1到3和5对应于各自的地址宽度）。Whenan8-bitaddresswidthisselected theaddressinformationoftheninthbitcanbeembeddedintheReadinstructioncode.图中案例4中的内存映射是针对9位地址宽度的。有关Read指令的详细信息，请参阅第35.6.2节。标准阅读说明。

35.4 SPI总线

35.4.1 SPI协议

除了用于串行闪存连接的SPI协议外，还支持单SPI、扩展SPI、双SPI和四SPI。

SPI协议的初始状态是SingleSPI，扩展SPI，可以通过SPI中的SFMSPI[1:0]位改变协议控制寄存器(SFMSPC)寄存器。

单SPI、扩展SPI协议中使用的地址和数据引脚根据传输模式控制寄存器(SFMSMD)中串行接口读取模式选择位SFMRM[2:0]的设置而变化。表35.3和表35.4列出了每个SPI协议中用于指令代码、地址和数据的引脚。

Note: 在读操作中，QSPI会在每个SPI总线周期输出额外的一个时钟，而不会伴随数据接收。有关详细信息，请参阅第35.5.9节。串行数据接收延迟。

Table 35.3 List of SPI Protocols (1)

SPI Protocol (SFMSPC.SFMSPI[1:0])	Single SPI Protocol, Extended SPI Protocol					
Serial interface read mode select (SFMSMD.SFMRM[2:0])	Standard read	Fast read	Fast read dual output	Fast read dual I/O	Fast read quad output	Fast read quad I/O
All pins used	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3
Pins used for instruction code	QIO0	QIO0	QIO0	QIO0	QIO0	QIO0
Pins used for addresses	QIO0	QIO0	QIO0	QIO0, QIO1	QIO0	QIO0, QIO1, QIO2, QIO3
Pins used for data	QIO0/QIO1	QIO0/QIO1	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3

Note: Single SPI protocol operation is for standard read and fast read. Extended SPI protocol operation is fast read dual output, fast read dual I/O, fast read quad output, and fast read quad I/O.

Table 35.4 List of SPI Protocols (2)

SPI Protocol (SFMSPC.SFMSPI[1:0])	Dual-SPI Protocol		Quad-SPI Protocol	
Serial interface read mode select (SFMSMD.SFMRM[2:0])	Fast read dual output	Fast read dual I/O	Fast read quad output	Fast read quad I/O
All pins used	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3
Pins used for instruction code	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3
Pins used for addresses	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3
Pins used for data	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3

In single SPI protocol and extended SPI protocol, the instruction code is always output from the QIO0 pin. Address and data input/output operations are performed according to the settings in SFMSMD.SFMRM[2:0].

Table 35.3 SPI协议列表(1)

SPI协议(SFMSPC.SFMSPI[1:0])	单SPI协议，扩展SPI协议					
串行接口读取模式选择(SFMSMD.SFMRM[2:0])	标准阅读	快速阅读	快速读取双输出	快速读取双IO	快速读取四路输出	快速读取四路IO
使用的所有引脚	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3
用于指令代码的引脚	QIO0	QIO0	QIO0	QIO0	QIO0	QIO0
用于地址的引脚	QIO0	QIO0	QIO0	QIO0, QIO1	QIO0	QIO0, QIO1, QIO2, QIO3
用于数据的引脚	QIO0/QIO1	QIO0/QIO1	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3

Note: 单SPI协议操作用于标准读取和快速读取。扩展的SPI协议操作是快速读取双输出、快速读取双IO、快速读取四输出和快速读取四IO。

Table 35.4 SPI协议列表(2)

SPI协议(SFMSPC.SFMSPI[1:0])	Dual-SPI Protocol		Quad-SPI Protocol	
串行接口读取模式选择(SFMSMD.SFMRM[2:0])	快速读取双输出	快速读取双IO	快速读取四路输出	快速读取四边形I/O
使用的所有引脚	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3	QSPCLK, QSSL, QIO0, QIO1, QIO2, QIO3
用于指令代码的引脚	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3
用于地址的引脚	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3
用于数据的引脚	QIO0, QIO1	QIO0, QIO1	QIO0, QIO1, QIO2, QIO3	QIO0, QIO1, QIO2, QIO3

在单SPI协议和扩展SPI协议中，指令代码总是从QIO0引脚输出。地址和数据输入输出操作根据SFMSMD.SFMRM[2:0]中的设置执行。

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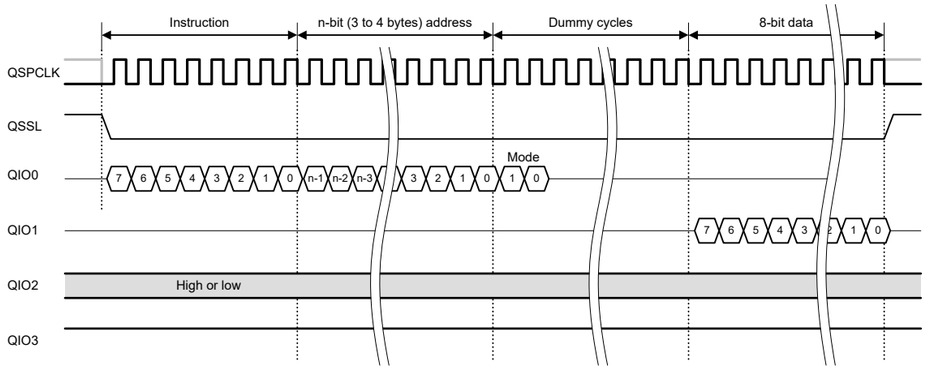

Figure 35.4 Single SPI Protocol example for Fast Read

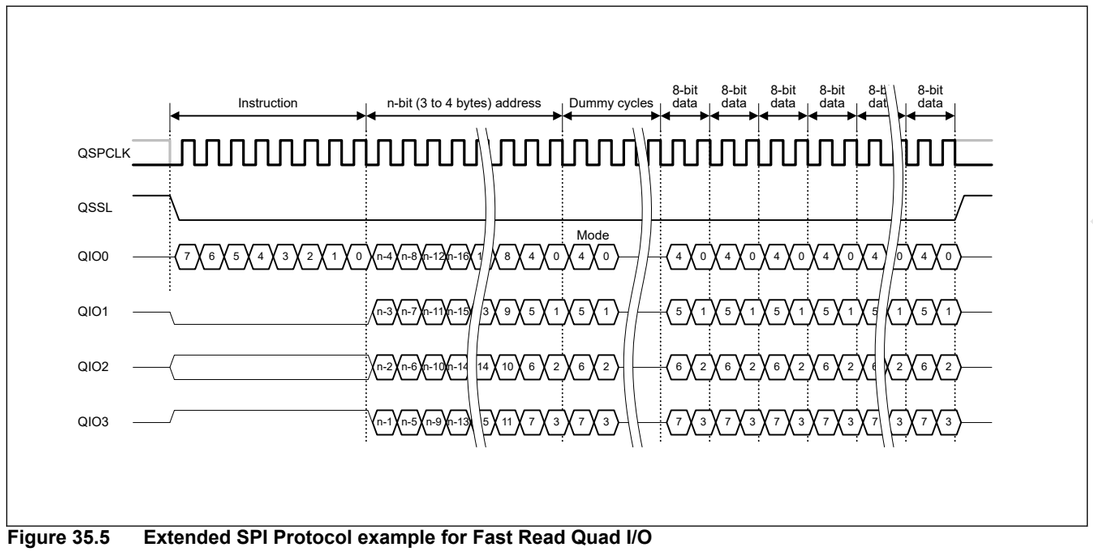

Figure 35.5 Extended SPI Protocol example for Fast Read Quad I/O

The Dual SPI protocol performs I/O operation of all signals such as instruction codes, addresses, and data using two pins, QIO0 and QIO1.

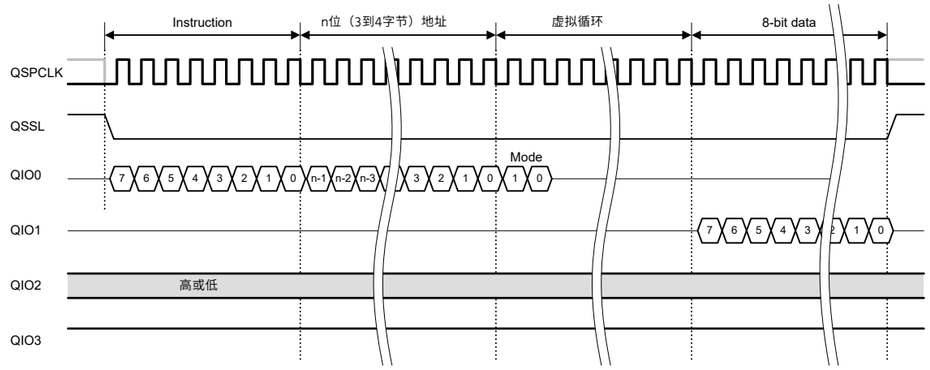

Figure 35.4 用于快速读取的单SPI协议示例

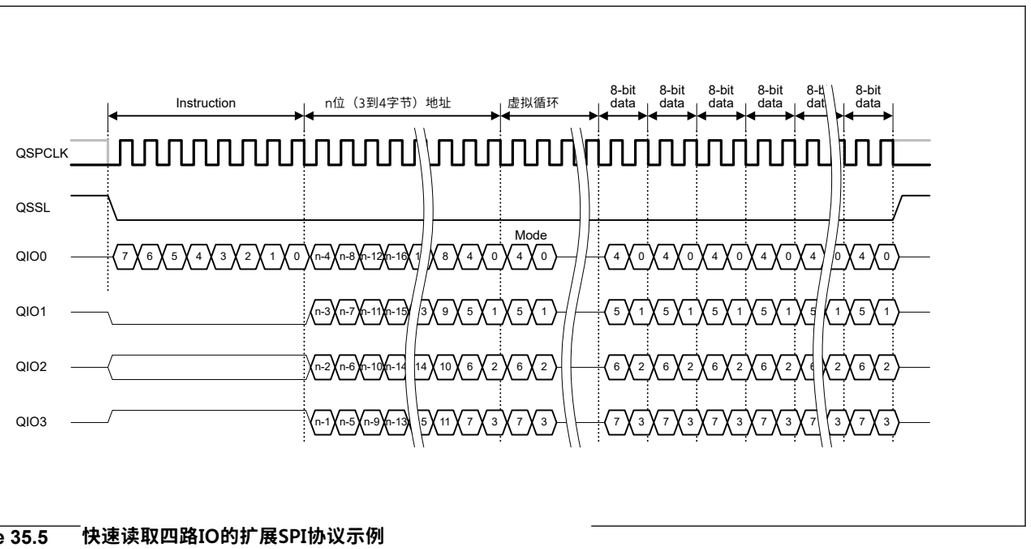

Figure 35.5 快速读取四路IO的扩展SPI协议示例

DualSPI协议使用两个引脚执行指令代码、地址和数据等所有信号的IO操作，
QIO0 and QIO1.

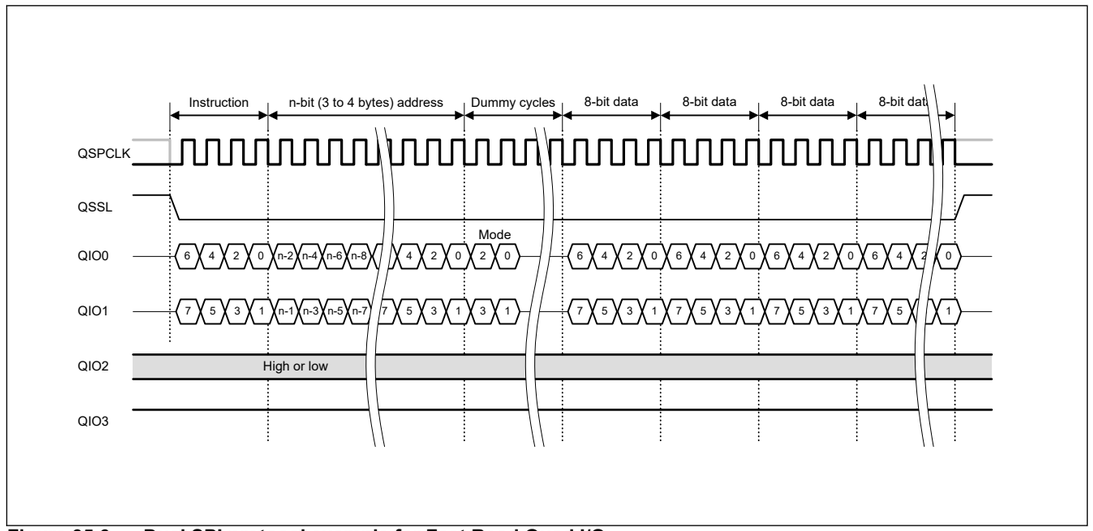

Figure 35.6 Dual SPI protocol example for Fast Read Quad I/O

The Quad SPI protocol performs I/O operation of all signals such as instruction codes, addresses, and data using four pins, QIO0, QIO1, QIO2, and QIO3.

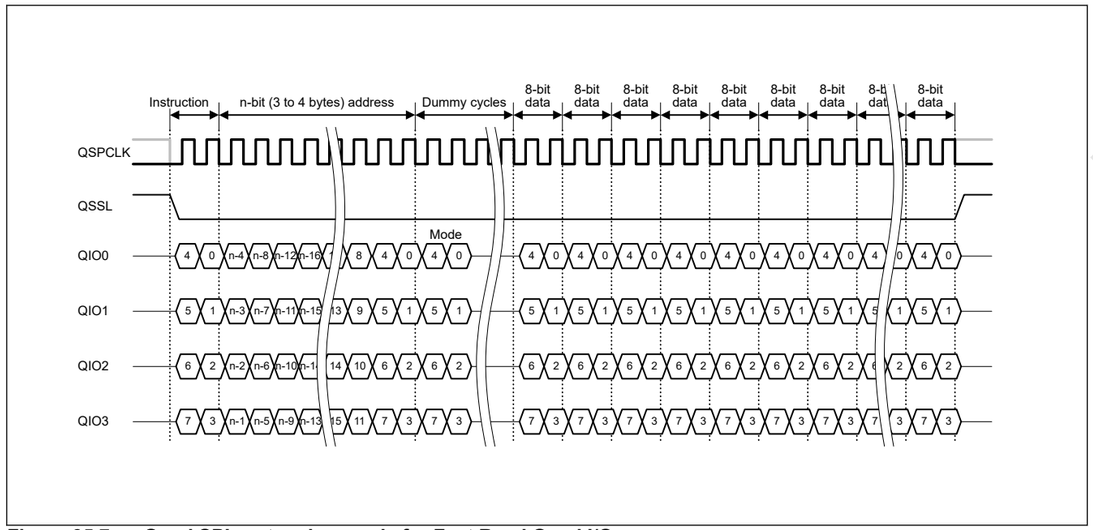

Figure 35.7 Quad SPI protocol example for Fast Read Quad I/O

35.4.2 SPI Mode

Either SPI mode 0 or SPI mode 3 can be selected as the SPI mode by the SFMSMD.SFMMD3 bit. This can be switched by changing the register setting during operation. The difference between SPI modes 0 and 3 is the state of the QSPCLK signal when it is inactive. The standby level of the QSPCLK signal in SPI mode 0 is low, and high in SPI mode 3.

Serial data is output from the QSPI on a falling edge of the serial clock and is read into the serial flash memory on a rising edge of the serial clock. Serial data is output from the serial flash memory on a falling edge of the serial clock and is read into the QSPI on the next falling edge of the serial clock.

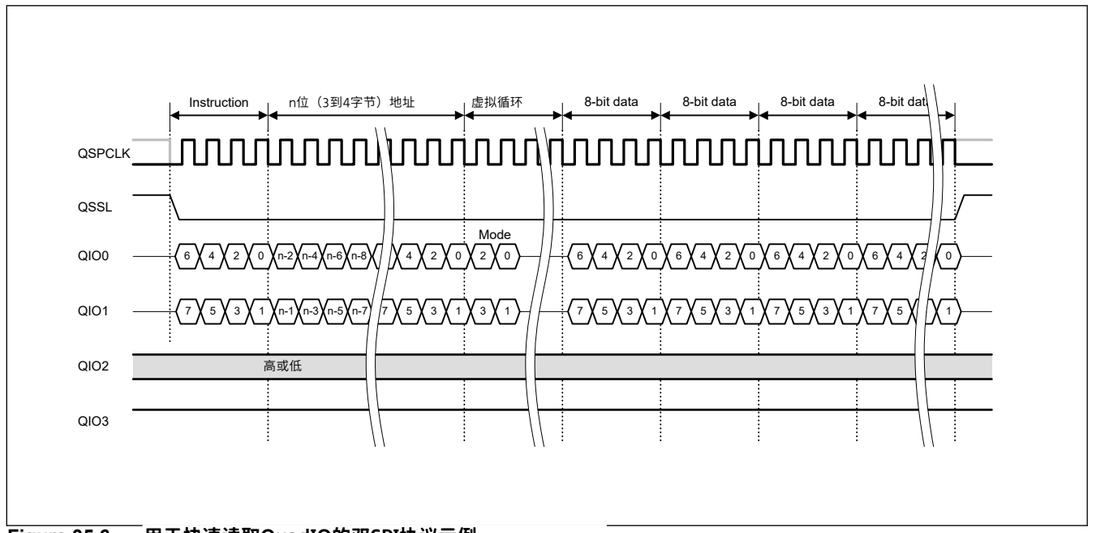

Figure 35.6 用于快速读取QuadIO的双SPI协议示例

QuadSPI协议使用四个引脚执行指令代码、地址和数据等所有信号的IO操作，
QIO0, QIO1, QIO2, and QIO3.

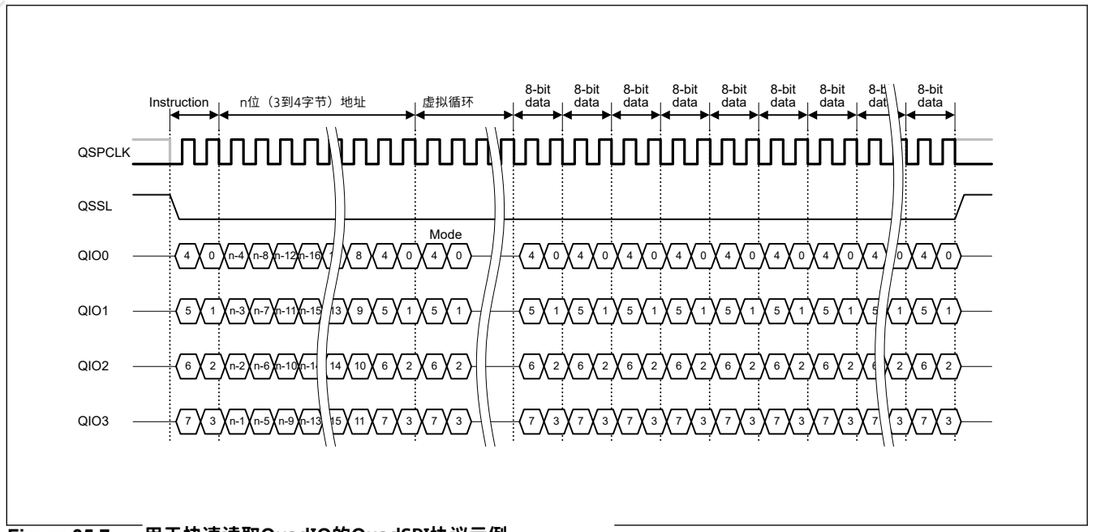

Figure 35.7 用于快速读取QuadIO的QuadSPI协议示例

35.4.2 SPI模式

可以通过SFMSMD.SFMMD3位选择SPI模式0或SPI模式3作为SPI模式。这可以通过在操作期间更改寄存器设置来切换。SPI模式0和3之间的区别在于QSPCLK信号处于非活动状态时的状态。QSPCLK信号在SPI模式0中的待机电平为低，在SPI模式3中为高。

串行数据在串行时钟的下降沿从QSPI输出，并在串行时钟的上升沿读入串行闪存。串行数据在串行时钟的下降沿从串行闪存输出，并在串行时钟的下一个下降沿读入QSPI。

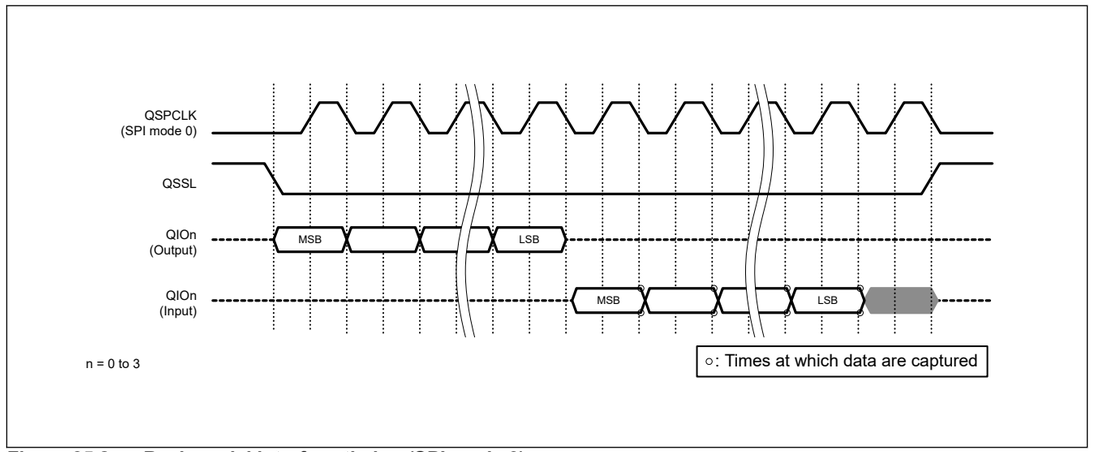

Figure 35.8 Basic serial interface timing (SPI mode 0)

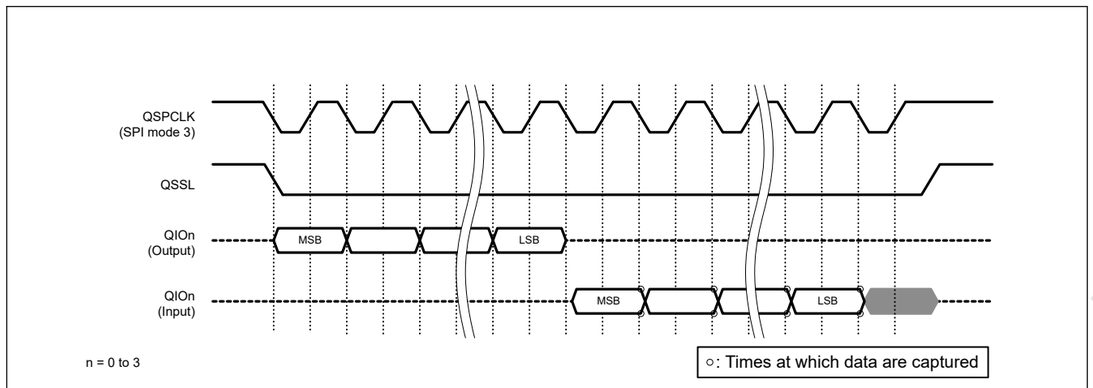

Figure 35.9 Basic serial interface timing (SPI mode 3)

35.5 SPI Bus Timing Adjustment

The timing of the SPI bus signal can be adjusted in the registers. The configured timing is applied to all SPI bus accesses, for both ROM access and direct communication.

35.5.1 SPI Bus Reference Cycles

The SPI bus operates on reference cycles obtained by multiplying PCLKA by an integer. The reference cycles are selectable within the range of PCLKA multiplied by 2 to 48 in the SFMDV[4:0] bits in the Transfer Mode Control Register (SFMSKC) register.

Table 35.5 Relationship among SFMDV[4:0] bits, cycle multiplier, and serial clock frequencies (1 of 2)

SFMDV[4:0]	Cycle multiplier	PCLKA = 100 [MHz]
11111b	48	2.08
11110b	46	2.17
11101b	44	2.27
11100b	42	2.38
11011b	40	2.50

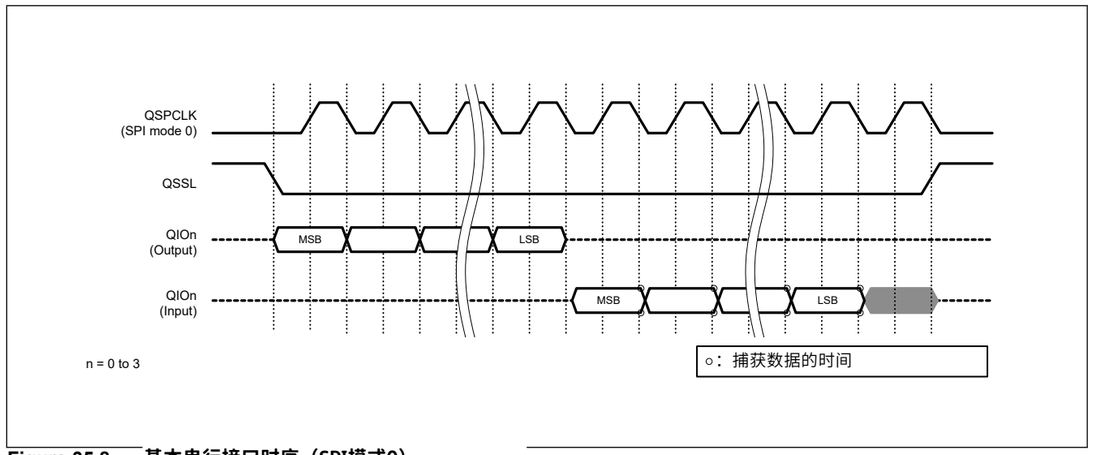

Figure 35.8 基本串行接口时序（SPI模式0）

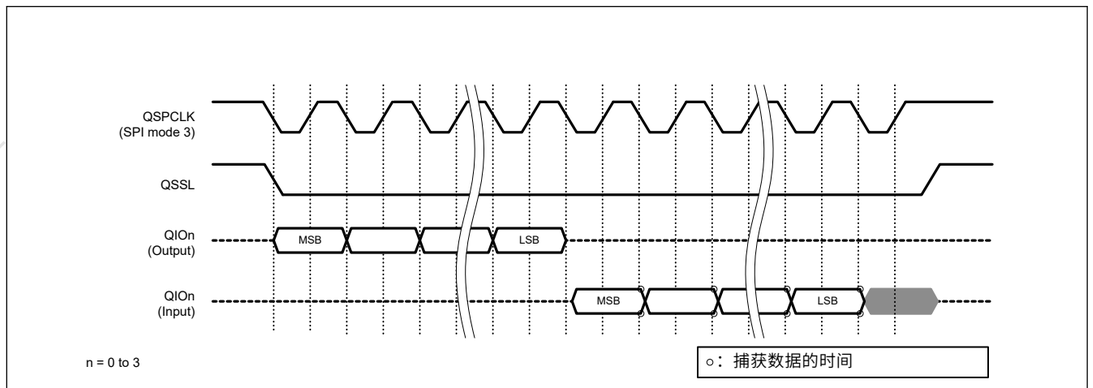

Figure 35.9 基本串行接口时序（SPI模式3）

35.5 SPI总线时序调整

SPI总线信号的时序可以在寄存器中调整。配置的时序适用于所有SPI总线访问，包括ROM访问和直接通信。

35.5.1 SPI总线参考周期

SPI总线在通过将PCLKA乘以一个整数获得的参考周期上运行。参考周期可在传输模式控制寄存器(SFMSKC)寄存器的SFMDV[4:0]位中的PCLKA乘以2到48的范围内选择。

Table 35.5 SFMDV[4:0]位、周期乘数和串行时钟频率之间的关系（1of2）

SFMDV[4:0]	循环乘数	PCLKA = 100 [MHz]
11111b	48	2.08
11110b	46	2.17
11101b	44	2.27
11100b	42	2.38
11011b	40	2.50

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Table 35.5 Relationship among SFMDV[4:0] bits, cycle multiplier, and serial clock frequencies (2 of 2)

SFMDV[4:0]	Cycle multiplier	PCLKA = 100 [MHz]
11010b	38	2.63
11001b	36	2.78
11000b	34	2.94
10111b	32	3.13
10110b	30	3.33
10101b	28	3.57
10100b	26	3.85
10011b	24	4.17
10010b	22	4.55
10001b	20	5.00
10000b	18	5.56
01111b	17	5.88
01110b	16	6.25
01101b	15	6.67
01100b	14	7.14
01011b	13	7.69
01010b	12	8.33
01001b	11	9.09
01000b	10	10.00
00111b	9	11.11
00110b	8	12.50
00101b	7	14.29
00100b	6	16.67
00011b	5	20.00
00010b	4	25.00
00001b	3	33.33
00000b	2	50.00

35.5.2 QSPCLK Signal Duty Ratio

When the reference clock is configured as PCLKA divided by an odd number without duty ratio correction, the duty ratio of the QSPCLK signal will not be 50%. When the reference clock is PCLKA divided by an odd number, be sure to enable the duty ratio correction function (SFMSKC.SFMDTY = 1).

When the reference clock is PCLKA divided by an even number, the SFMDTY setting in the SFMSKC register is ignored.

Table 35.5 SFMDV[4:0]位、周期乘数和串行时钟频率之间的关系(2of2)

SFMDV[4:0]	循环乘数	PCLKA = 100 [MHz]
11010b	38	2.63
11001b	36	2.78
11000b	34	2.94
10111b	32	3.13
10110b	30	3.33
10101b	28	3.57
10100b	26	3.85
10011b	24	4.17
10010b	22	4.55
10001b	20	5.00
10000b	18	5.56
01111b	17	5.88
01110b	16	6.25
01101b	15	6.67
01100b	14	7.14
01011b	13	7.69
01010b	12	8.33
01001b	11	9.09
01000b	10	10.00
00111b	9	11.11
00110b	8	12.50
00101b	7	14.29
00100b	6	16.67
00011b	5	20.00
00010b	4	25.00
00001b	3	33.33
00000b	2	50.00

35.5.2 QSPCLK信号占空比

当参考时钟配置为PCLKA除以奇数而不进行占空比校正时，QSPCLK信号的占空比不会为50%。当参考时钟为PCLKA除以奇数时，请务必启用占空比校正功能（SFMSKC.SFMDTY=1）。

当参考时钟为PCLKA除以偶数时，SFMSKC寄存器中的SFMDTY设置被忽略。

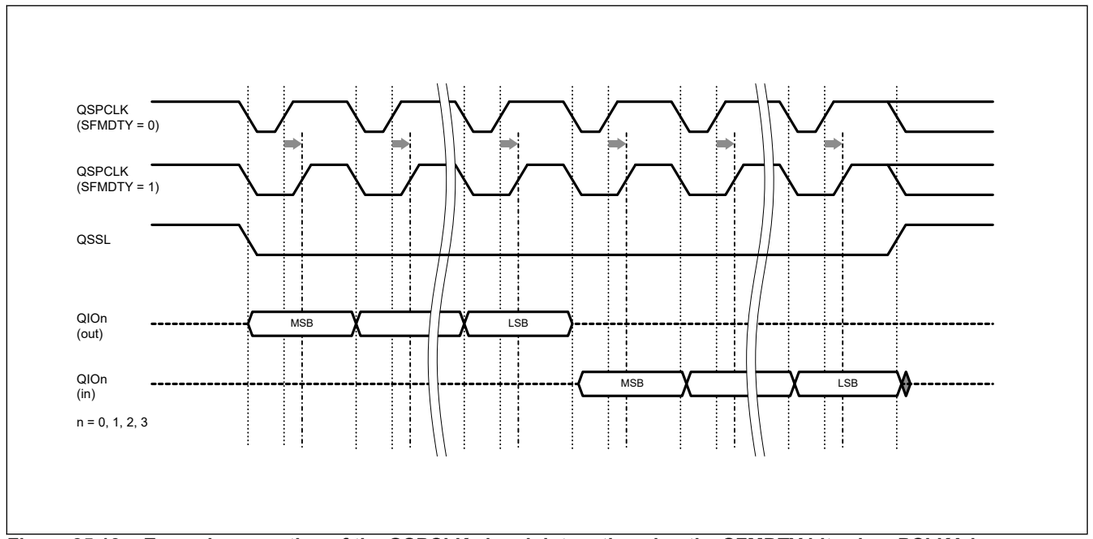

Figure 35.10 Example correction of the QSPCLK signal duty ratio using the SFMDTY bit, when PCLKA is multiplied by 3

35.5.3 Minimum High-Level Width for the QSSL Signal

Between adjacent SPI bus cycles, the QSSL signal must be held high (inactive) for a sufficient time to satisfy the deselect time required by the serial flash memory. The minimum high-level width of the QSSL output signal is selectable as the reference cycle multiplied by an integer from 1 to 16 in the SFMSW[3:0] bits in the Instruction Code Register (SFMSSC) register.

35.5.4 QSSL Signal Setup Time

The QSSL signal setup time that the serial flash memory requires after the QSSL signal is driven active low until the first rising edge of the QSPCLK signal can be configured. The setup time can be selected as 0.5 or 1.5 cycles of QSPCLK in the SFMSLD bit of the SFMSSC register.

Set a value that meets the most constrained timing condition for your application.

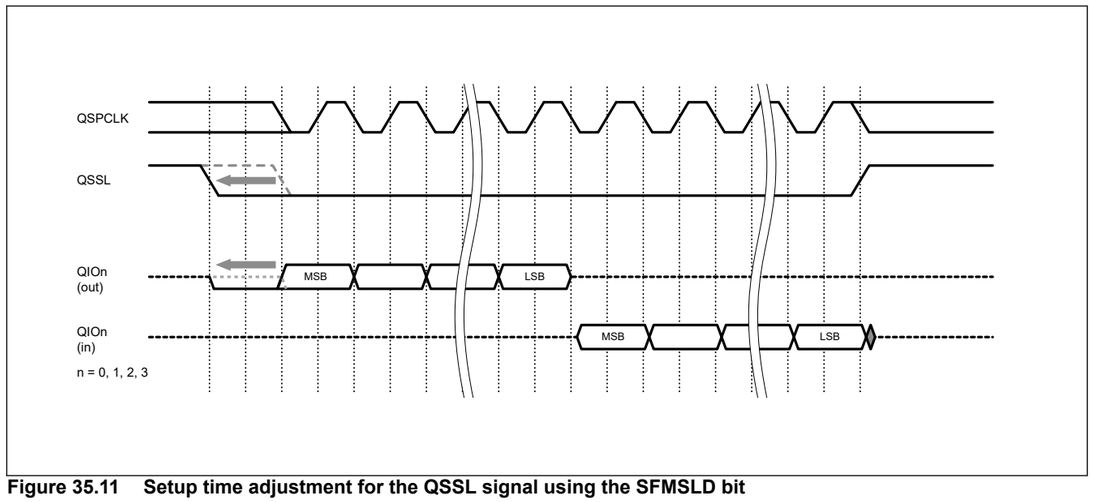

Figure 35.11 Setup time adjustment for the QSSL signal using the SFMSLD bit

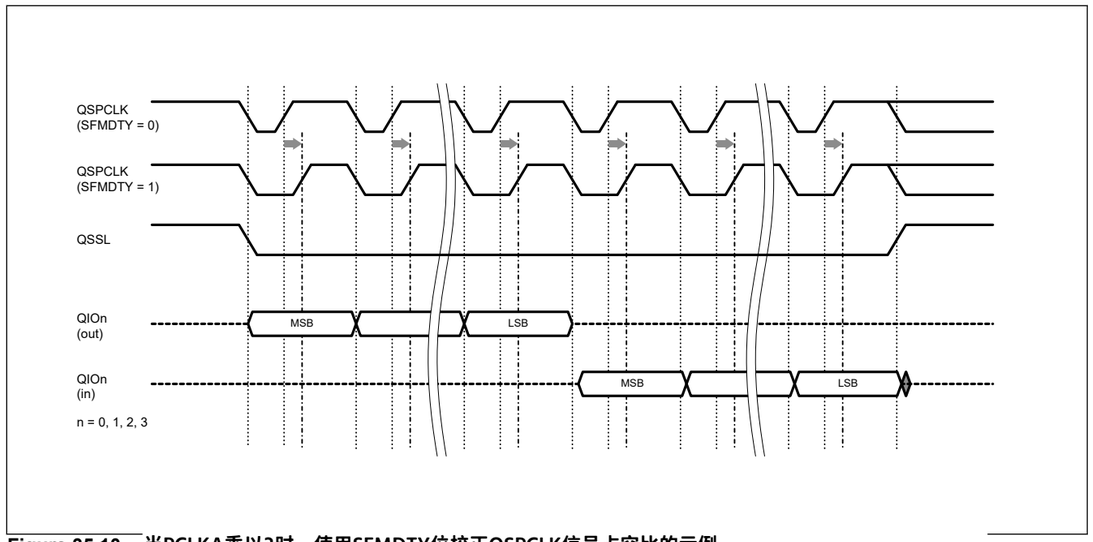

Figure 35.10 当PCLKA乘以3时，使用SFMDTY位校正QSPCLK信号占空比的示例

35.5.3 QSSL信号的最小高电平宽度

在相邻的SPI总线周期之间，QSSL信号必须保持高电平（无效）足够长的时间，以满足串行闪存所需的取消选择时间。QSSL输出信号的最小高电平宽度可选择为参考周期乘以指令代码寄存器(SFMSSC)寄存器中SFMSW[3:0]位中的1到16的整数。

35.5.4 QSSL信号建立时间

从QSSL信号被驱动为低电平有效到QSPCLK信号的第一个上升沿可以配置，串行闪存所需的QSSL信号建立时间。设置时间可以在SFMSSC寄存器的SFMSLD位中选择为0.5或1.5个QSPCLK周期。

为您的应用设置一个满足最受约束的时序条件的值。

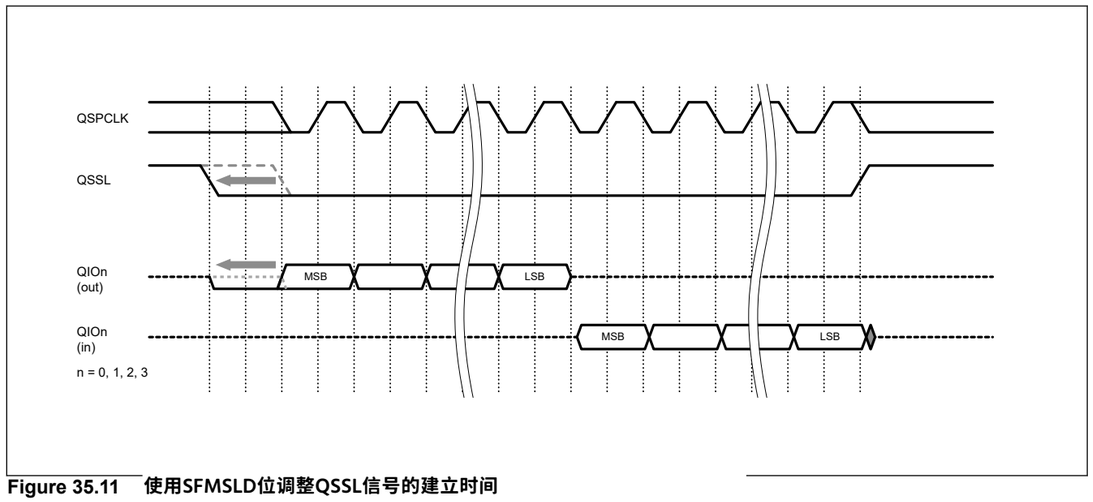

Figure 35.11 使用SFMSLD位调整QSSL信号的建立时间

35.5.5 QSSL Signal Hold Time

The QSSL signal hold time that the serial flash memory requires until the QSSL signal is driven high after the last rising edge of the QSPCLK signal can be configured. The hold time can be selected as 0.5 or 1.5 cycles of QSPCLK in the SFMSHD bit of the SFMSSC register.

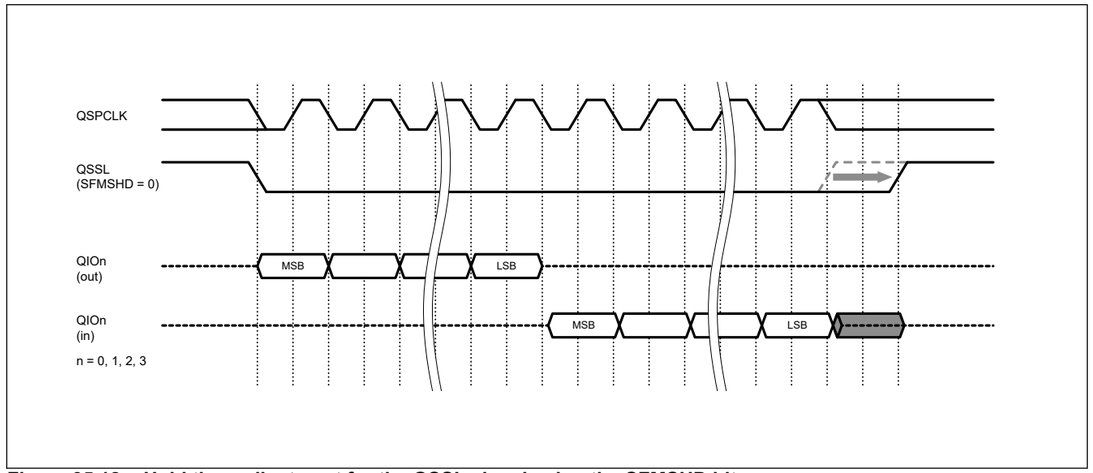

Figure 35.12 Hold time adjustment for the QSSL signal using the SFMSHD bit

35.5.6 Hold Time of the Serial Data Output Enable

The buffer output enable of the QIO0, QIO1, QIO2, or QIO3 pin can be extended by 1 QSPCLK using the SFMOEX bit in the SFMSMD register.

For a standard read instruction, it is extended immediately after an address code. For other read instructions, it is extended after two cycles of mode data (XIP mode control) of the serial flash memory in dummy cycles.

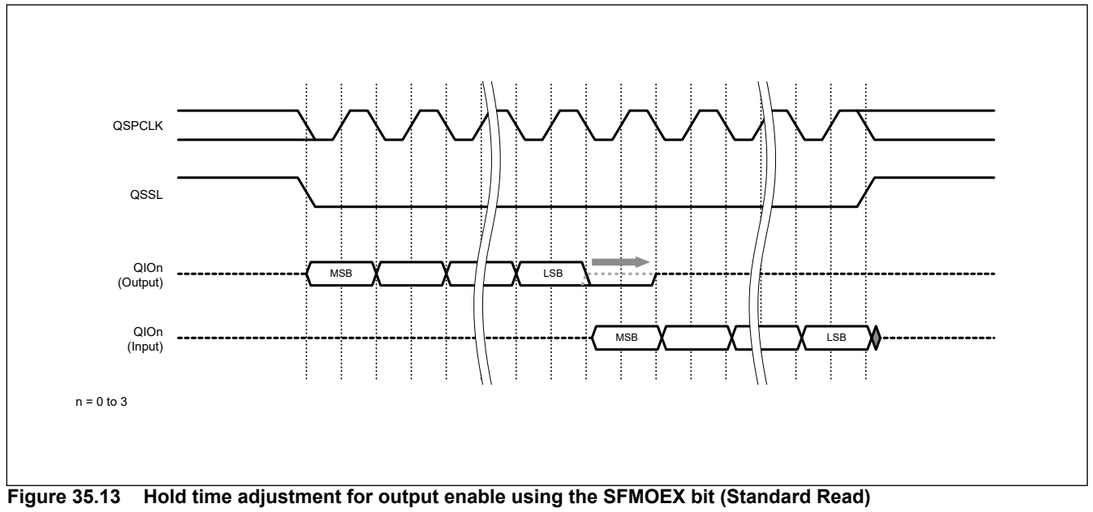

Figure 35.13 Hold time adjustment for output enable using the SFMOEX bit (Standard Read)

35.5.5 QSSL信号保持时间

可以配置在QSPCLK信号的最后一个上升沿之后，直到QSSL信号被驱动为高电平之前，串行闪存所需的QSSL信号保持时间。保持时间可以在SFMSSC寄存器的SFMSHD位中选择为0.5或1.5个QSPCLK周期。

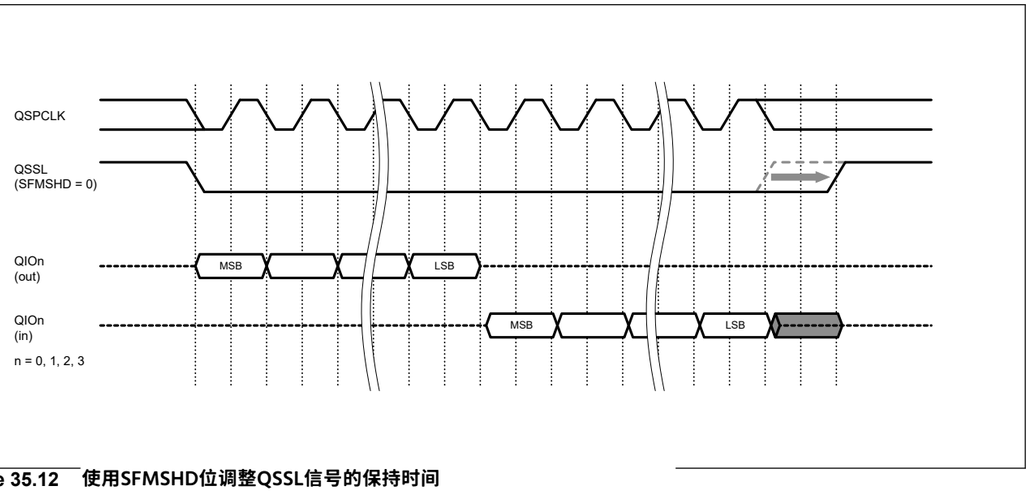

Figure 35.12 使用SFMSHD位调整QSSL信号的保持时间

35.5.6 串行数据输出使能的保持时间

可以使用SFMSMD寄存器中的SFMOEX位将QIO0、QIO1、QIO2或QIO3引脚的缓冲器输出使能扩展1个QSPCLK。

对于标准读指令，它在地址码之后立即扩展。对于其他读指令，它在串行闪存的两个模式数据（XIP模式控制）周期后以虚拟周期进行扩展。

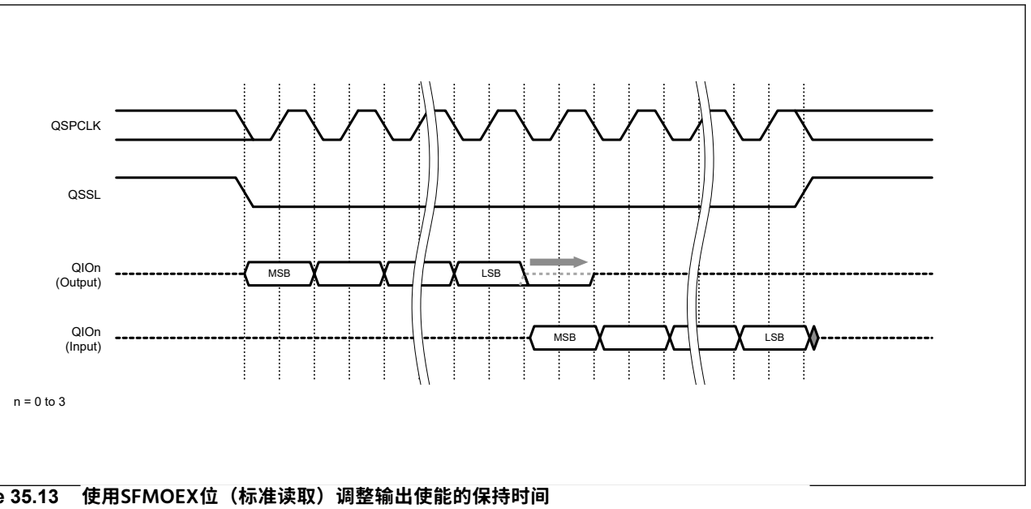

Figure 35.13 使用SFMOEX位（标准读取）调整输出使能的保持时间

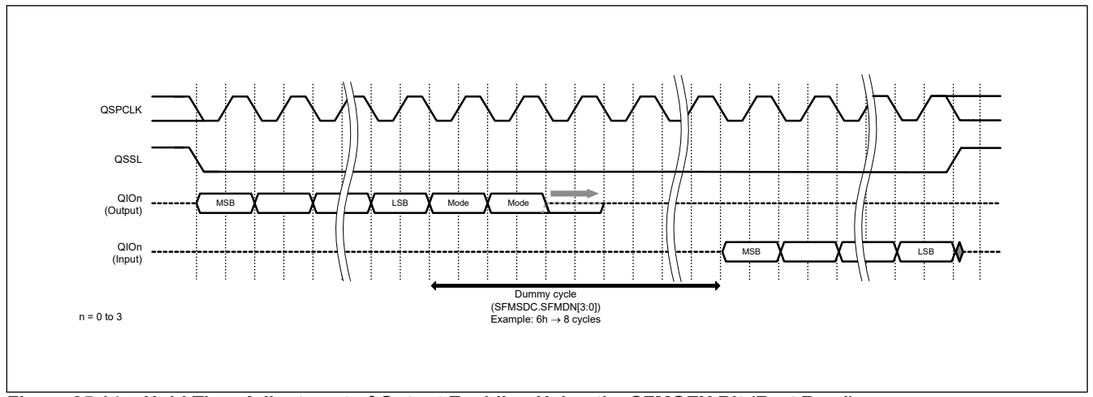

Figure 35.14 Hold Time Adjustment of Output Enabling Using the SFMOEX Bit (Fast Read)

35.5.7 Setup Time for Serial Data Output

When a command or address is transmitted to the serial flash memory, the setup time begins on serial data output and ends when the QSPCLK signal rises. If this setup time is insufficient, it can be extended by 1 PCLKA using the SFMOSW bit in the SFMSMD register. When SFMOSW is 1, the low-level width of QSPCLK during serial data transmission is extended by 1 PCLKA while data is being output from the QSPI. This function has no effect on serial data reception.

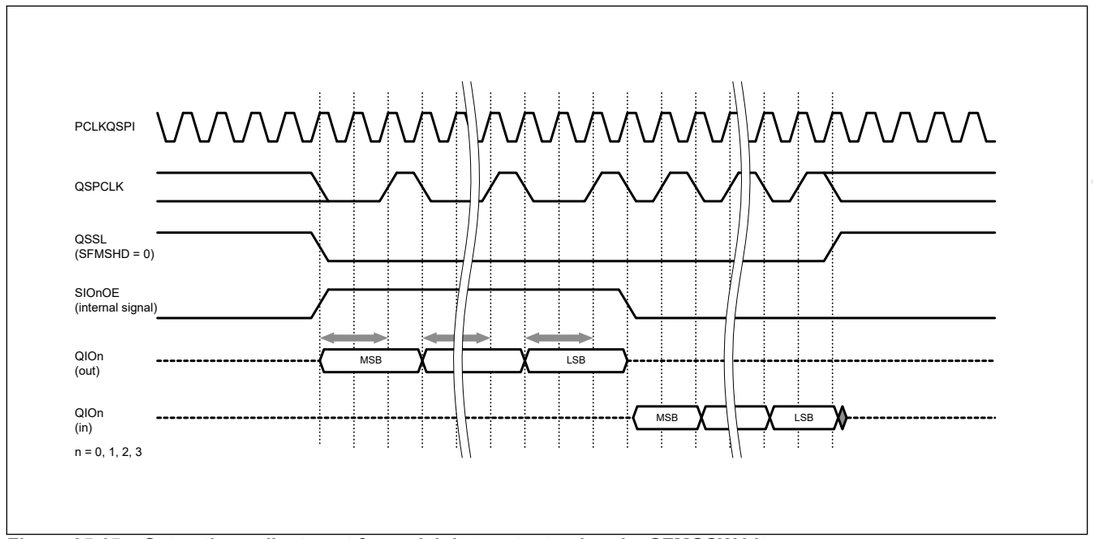

Figure 35.15 Setup time adjustment for serial data output using the SFMOSW bit

35.5.8 Hold Time for Serial Data Output

When a command or address is transmitted to the serial flash memory, the hold time begins on the rising edge of QSPCLK and ends when the serial data makes another transmission. If this hold time is insufficient, it can be extended by 1 PCLKA using the SFMOHW bit in the SFMSMD register. When SFMOSW is 1, the high-level width of QSPCLK during serial data transmission is extended by 1 PCLKA while data is being output from the QSPI. This function has no effect on serial data reception.

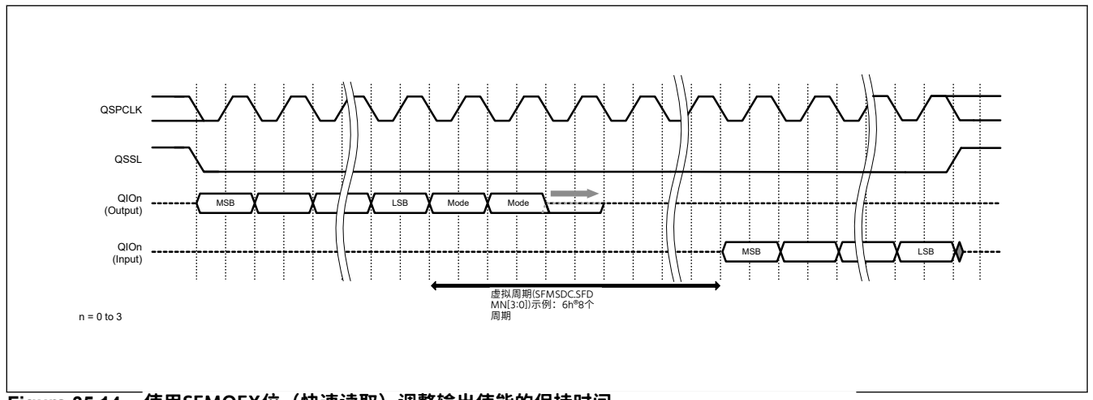

Figure 35.14 使用SFMOEX位（快速读取）调整输出使能的保持时间

35.5.7 串行数据输出的建立时间

当命令或地址传输到串行闪存时，设置时间从串行数据输出开始，到QSPCLK信号上升时结束。如果此建立时间不足，可以使用SFMSMD寄存器中的SFMOSW位将其延长1个PCLKA。当SFMOSW为1时，在从QSPI输出数据时，串行数据传输期间QSPCLK的低电平宽度扩展1PCLKA。该功能对串行数据接收没有影响。

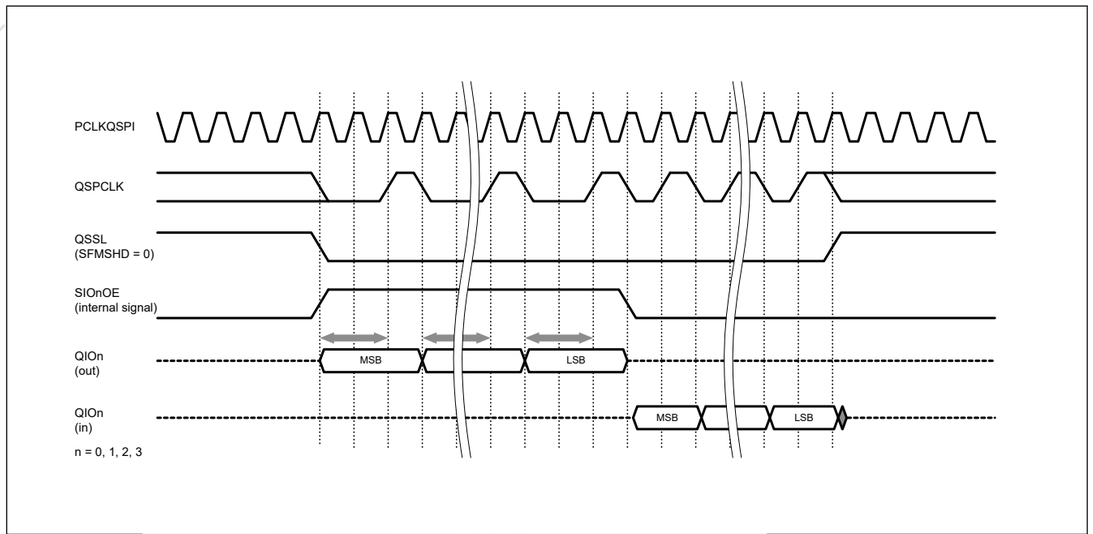

Figure 35.15 使用SFMOSW位调整串行数据输出的建立时间

35.5.8 串行数据输出的保持时间

当命令或地址传输到串行闪存时，保持时间从QSPCLK的上升沿开始，并在串行数据进行另一次传输时结束。如果该保持时间不足，可以使用SFMSMD寄存器中的SFMOHW位将其延长1个PCLKA。当SFMOSW为1时，在从QSPI输出数据时，串行数据传输期间QSPCLK的高电平宽度扩展1PCLKA。该功能对串行数据接收没有影响。

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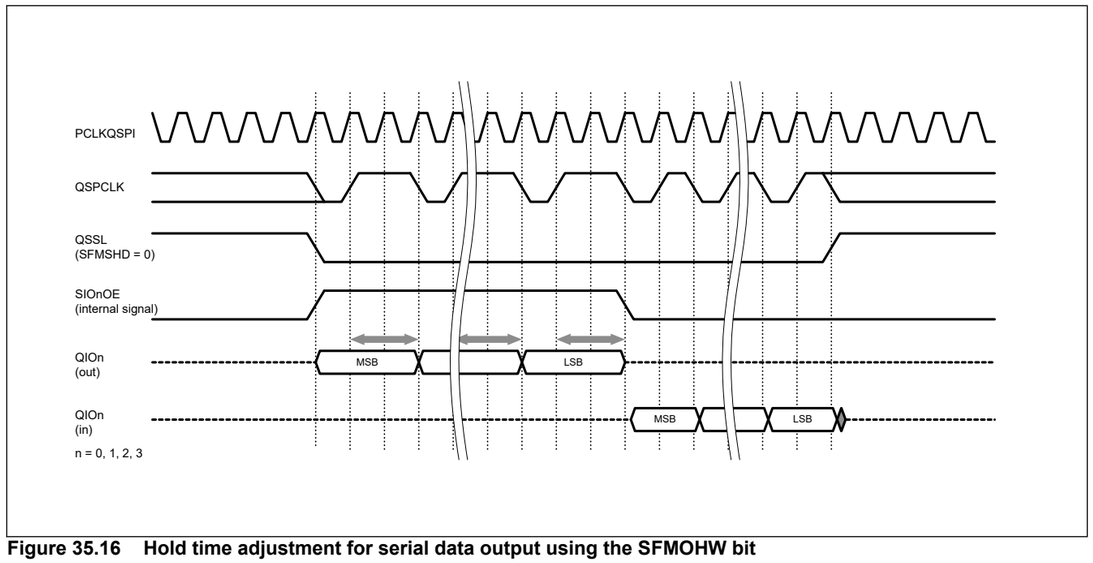

Figure 35.16 Hold time adjustment for serial data output using the SFMOHW bit

35.5.9 Serial Data Receiving Latency

The serial flash outputs data in synchronization with the falling edge of the QSPCLK signal. The QSPI receives that data in synchronization with the falling edge of the subsequent QSPCLK signal. The delay from when the serial flash starts outputting data until the QSPI receives that data is called the receiving latency. The QSPI adds a latency adjustment cycle immediately before the first data reception cycle in the SPI bus cycle. From the serial flash side, this is seen as an increase in the number of data reception cycles. This added latency adjustment cycle is not generated in the SPI bus cycle without accompanying data reception.

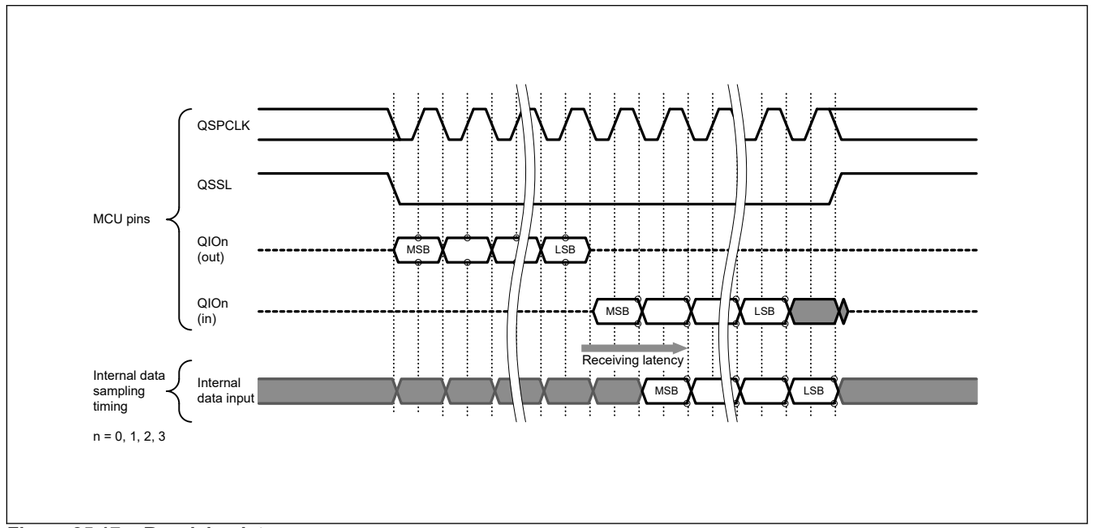

Figure 35.17 Receiving latency

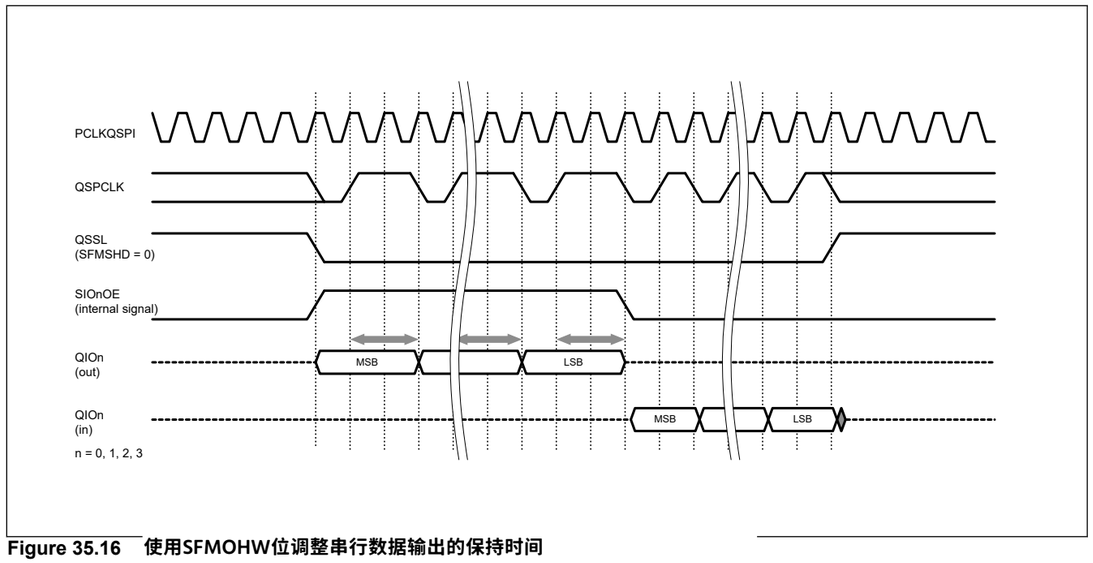

Figure 35.16 使用SFMOHW位调整串行数据输出的保持时间

35.5.9 串行数据接收延迟

串行闪存与QSPCLK信号的下降沿同步输出数据。QSPI与随后的QSPCLK信号的下降沿同步接收该数据。从串行闪存开始输出数据到QSPI接收到该数据的延迟称为接收延迟。QSPI在SPI总线周期的第一个数据接收周期之前添加一个延迟调整周期。从串行闪存方面来看，这被视为数据接收周期数的增加。如果没有伴随的数据接收，则不会在SPI总线周期中生成这个增加的延迟调整周期。

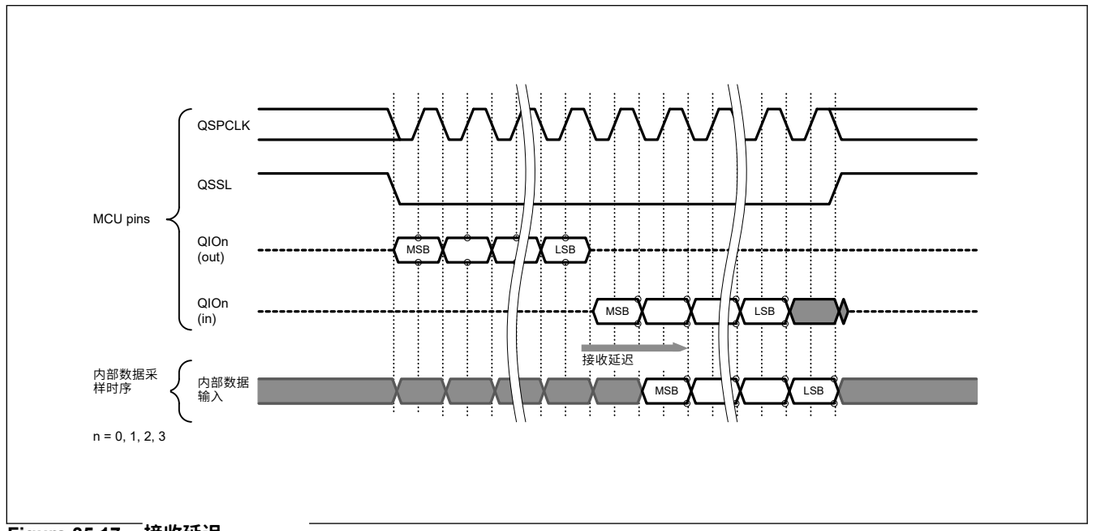

Figure 35.17 接收延迟

35.6 SPI Instruction Set Used for Serial Flash Memory Access

35.6.1 SPI Instructions That Are Automatically Generated

When the serial flash memory is accessed, an SPI bus cycle using the instructions described in Table 35.6 to Table 35.10 is automatically generated based on the settings in the SFMSAC register and in the SFMSMD register.

Table 35.6 SPI instructions automatically generated when SFMAS[1:0] = 00b

SPI instruction	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Standard Read	0x03*1	1	—	1 to ∞	SFMRM[2:0] = 000b, A8 = 0
	0x0B*1	1	—	1 to ∞	SFMRM[2:0] = 000b, A8 = 1

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMCIC[7:0] bits in the Instruction Code Register (SFMSIC) setting is used as an instruction code.

Table 35.7 SPI instructions automatically generated when SFMAS[1:0] = 01b

SPI instruction	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Standard Read	0x03*1	2	—	1 to ∞	SFMRM[2:0] = 000b

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.

Table 35.8 SPI instructions automatically generated when SFMAS[1:0] = 10b

SPI instruction	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Standard Read	0x03*1	3	—	1 to ∞	SFMRM[2:0] = 000b
Fast Read	0x0B*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001b
Fast Read Dual Output	0x3B*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010b
Fast Read Dual I/O	0xBB*1	3	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011b
Fast Read Quad Output	0x6B*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100b
Fast Read Quad I/O	0xEB*1	3	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101b

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.
Note 2. The number of dummy cycles is configurable by using SFMDN[3:0] bits in the Dummy Cycle Control Register (SFMSDC).

Table 35.9 SPI instructions automatically generated when SFMAS[1:0] = 11b and SFM4BC = 0

SPI instruction	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Standard Read	0x03*1	4	—	1 to ∞	SFMRM[2:0] = 000b
Fast Read	0x0B*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001b
Fast Read Dual Output	0x3B*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010b
Fast Read Dual I/O	0xBB*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011b
Fast Read Quad Output	0x6B*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100b
Fast Read Quad I/O	0xEB*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101b

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.
Note 2. The number of dummy cycles is configurable by using the SFMSDC.SFMDN[3:0] bits.

Table 35.10 SPI instructions automatically generated when SFMAS[1:0] = 11b and SFM4BC = 1 (1 of 2)

SPI instruction	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Standard Read	0x13*1	4	—	1 to ∞	SFMRM[2:0] = 000b

35.6 用于串行闪存访问的SPI指令集

35.6.1 自动生成的SPI指令

访问串行闪存时，会根据SFMSAC寄存器和SFMSMD寄存器中的设置自动生成使用表35.6至表35.10中描述的指令的SPI总线周期。

Table 35.6 SFMAS[1:0]=00b时自动生成SPI指令

SPI指令	指令码	地址字节	虚拟循环	数据字节	Remarks
标准阅读	0x03*1	1	—	1 to ∞	SFMRM[2:0] = 000b, A8 = 0
	0x0B*1	1	—	1 to ∞	SFMRM[2:0] = 000b, A8 = 1

注1.如果SFMSMD.SFMCCE位设置为1，则指令代码寄存器(SFMSIC)设置中的SFMCIC[7:0]位用作指令代码。

Table 35.7 SFMAS[1:0]=01b时自动生成SPI指令

SPI指令	指令码	地址字节	虚拟循环	数据字节	Remarks
标准阅读	0x03*1	2	—	1 to ∞	SFMRM[2:0] = 000b

注1.如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。

Table 35.8 SFMAS[1:0]=10b时自动生成SPI指令

SPI指令	指令码	地址字节	虚拟循环	数据字节	Remarks
标准阅读	0x03*1	3	—	1 to ∞	SFMRM[2:0] = 000b
快速阅读	0x0B*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001b
快速读取双输出	0x3B*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010b
快速读取双IO	0xBB*1	3	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011b
快速读取四路输出	0x6B*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100b
快速读取四路IO	0xEB*1	3	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101b

注1.如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。
注2.虚拟周期数可通过使用虚拟周期控制寄存器(SFMSDC)中的SFMDN[3:0]位进行配置。

Table 35.9 当SFMAS[1:0]=11b和SFM4BC=0时自动生成SPI指令

SPI指令	指令码	地址字节	虚拟循环	数据字节	Remarks
标准阅读	0x03*1	4	—	1 to ∞	SFMRM[2:0] = 000b
快速阅读	0x0B*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001b
快速读取双输出	0x3B*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010b
快速读取双IO	0xBB*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011b
快速读取四路输出	0x6B*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100b
快速读取四路IO	0xEB*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101b

注1.如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。
注2.虚拟周期数可通过使用SFMSDC.SFMDN[3:0]位进行配置。

Table 35.10 当SFMAS[1:0]=11b和SFM4BC=1时自动生成SPI指令（1of2）

SPI指令	指令码	地址字节	虚拟循环	数据字节	Remarks
标准阅读	0x13*1	4	—	1 to ∞	SFMRM[2:0] = 000b

Table 35.10 SPI instructions automatically generated when SFMAS[1:0] = 11b and SFM4BC = 1 (2 of 2)

SPI instruction	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Fast Read	0x0C*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001b
Fast Read Dual Output	0x3C*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010b
Fast Read Dual I/O	0xBC*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011b
Fast Read Quad Output	0x6C*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100b
Fast Read Quad I/O	0xEC*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101b

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.
Note 2. The number of dummy cycles is configurable by using the SFMSDC.SFMDN[3:0] bits..

35.6.2 Standard Read Instruction

The standard Read instruction is a common read instruction supported by most serial flash memory. When an SPI bus cycle starts, the QSSL signal (serial flash memory select) is asserted, and the instruction code (0x03 or 0x13)*1 is output. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted. Data is then received.

This standard Read instruction is selected in the initial QSPI settings.

Note 1. Many 4-KB serial flash memory devices have an address field not larger than 1 byte (A7-A0) to minimize the overhead and to receive A8 information from bit 3 of the Read instruction code. To support these devices, the QSPI only outputs A8 (address bit 8) to bit [3] of the standard Read instruction code when an address width of 1 byte is specified (SFMAS[1:0] = 00). This means that 0x0B might be output instead of 0x03 as the standard Read instruction code. This code duplicates the Fast Read instruction code. However, for most of the 2-KB or smaller serial flash memory, with an address width of 1 byte, bit 3 of a command is designed to be excluded from decoding as a don't-care bit, so such a Read instruction code is recognized correctly as the standard Read instruction code. In rare cases, some serial flash memory allow bit 3 to be decoded. When such a serial flash memory is connected, configure your application to avoid access resulting in A8 = 1.

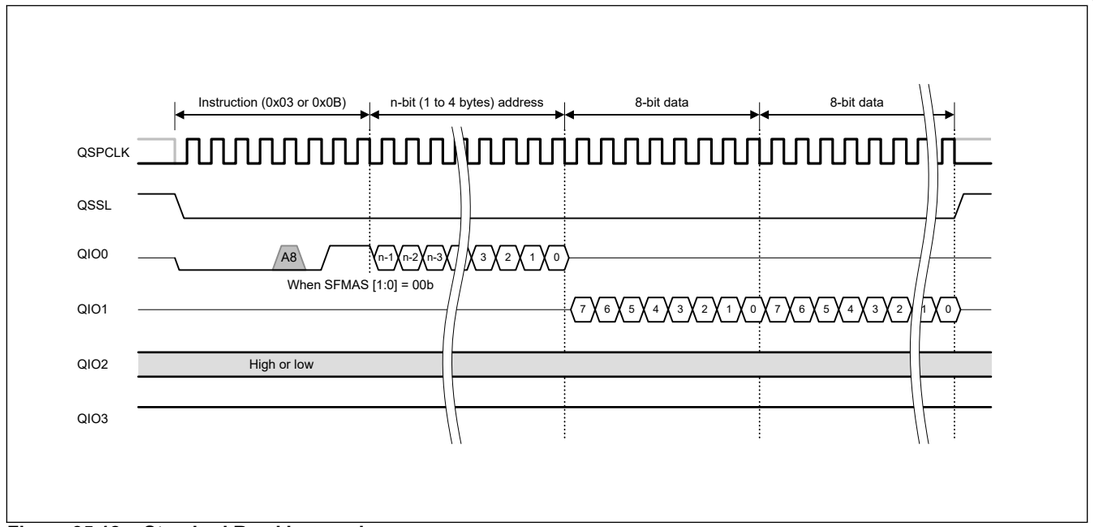

Figure 35.18 Standard Read bus cycle

35.6.3 Fast Read Instruction

The Fast Read instruction is a read instruction that supports a higher communication clock speed than the standard Read instruction. When an SPI bus cycle starts, the QSSL signal is asserted, and the instruction code (0x0B or 0x0C) is output.

Table 35.10 当SFMAS[1:0]=11b和SFM4BC=1(2of2)时自动生成SPI指令

SPI指令	指令码	地址字节	虚拟循环	数据字节	Remarks
快速阅读	0x0C*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001b
快速读取双输出	0x3C*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010b
快速读取双IO	0xBC*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011b
快速读取四路输出	0x6C*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100b
快速读取四路IO	0xEC*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101b

注1.如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。
注2.虚拟周期数可通过使用SFMSDC.SFMDN[3:0]位进行配置。

35.6.2 标准阅读说明

标准读指令是大多数串行闪存支持的常见读指令。当SPI总线周期开始时，QSSL信号（串行闪存选择）被置位，并输出指令代码（0x03或0x13）*1。接下来，发送宽度为1到4字节的地址，在SFMSAC寄存器的SFMAS[1:0]位中指定。然后接收数据。

在初始QSPI设置中选择此标准读取指令。

注1.许多4KB串行闪存器件的地址字段不大于1字节(A7-A0)，以尽量减少
开销并从读取指令代码的第3位接收A8信息。为了支持这些器件，当指定地址宽度为1字节（SFMAS[1:0]=00）时，QSPI仅将A8（地址位8）输出到标准读指令代码的位[3]。这意味着可能会输出0x0B而不是0x03作为标准读取指令代码。此代码复制了快速读取指令代码。然而，对于大多数2-KB或更小的串行闪存，地址宽度为1字节，命令的第3位被设计为作为无关位从解码中排除，因此这样的读取指令代码被正确识别为标准读取指令代码。在极少数情况下，某些串行闪存允许对第3位进行解码。连接此类串行闪存时，配置您的应用程序以避免访问导致A8=1。

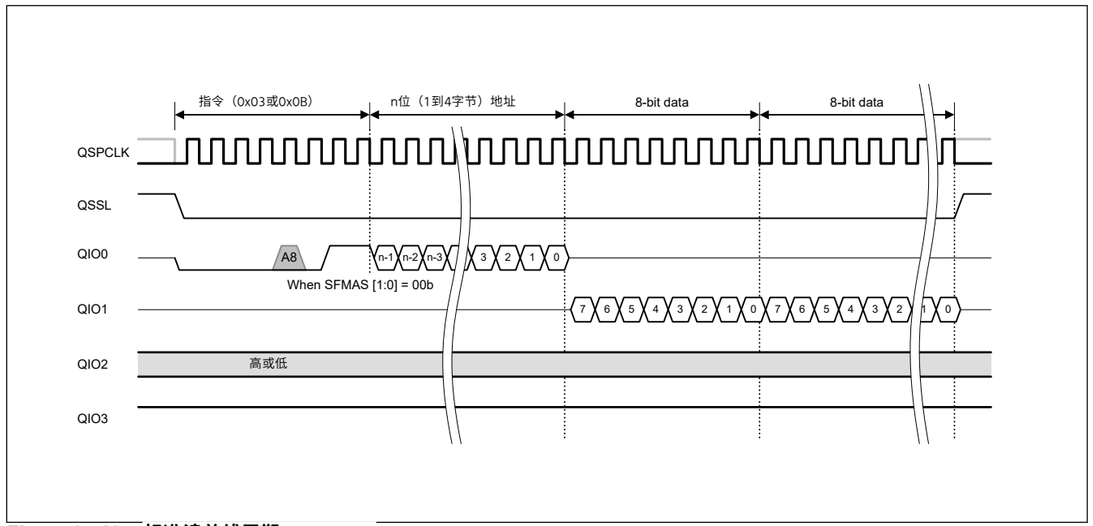

Figure 35.18 标准读总线周期

35.6.3 快速阅读说明

快速读取指令是一种读取指令，它支持比标准读取指令更高的通信时钟速度。当一个SPI总线周期开始时，QSSL信号被置位，并输出指令代码（0x0B或0x0C）。

Next, an address with a width of 1 to 4 bytes specified by the SFMSAC.SFMAS [1: 0] bits is transmitted, a dummy cycle specified by the SFMSDC register is generated, then the data is received.

The first two dummy cycles are used to select the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 35.8. XIP Control.

Switching to the Fast Read instruction is controlled in the SFMSMD register.

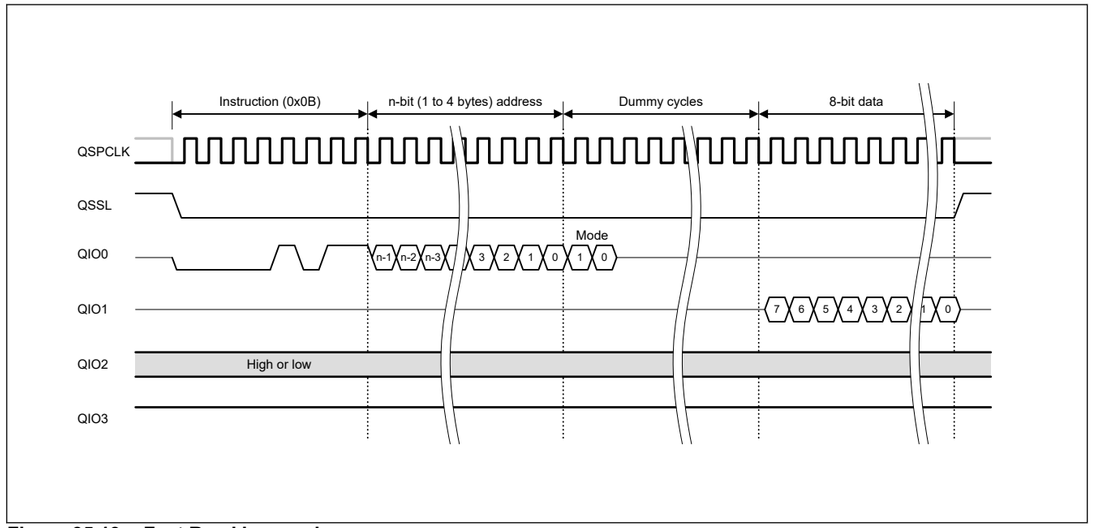

Figure 35.19 Fast Read bus cycle

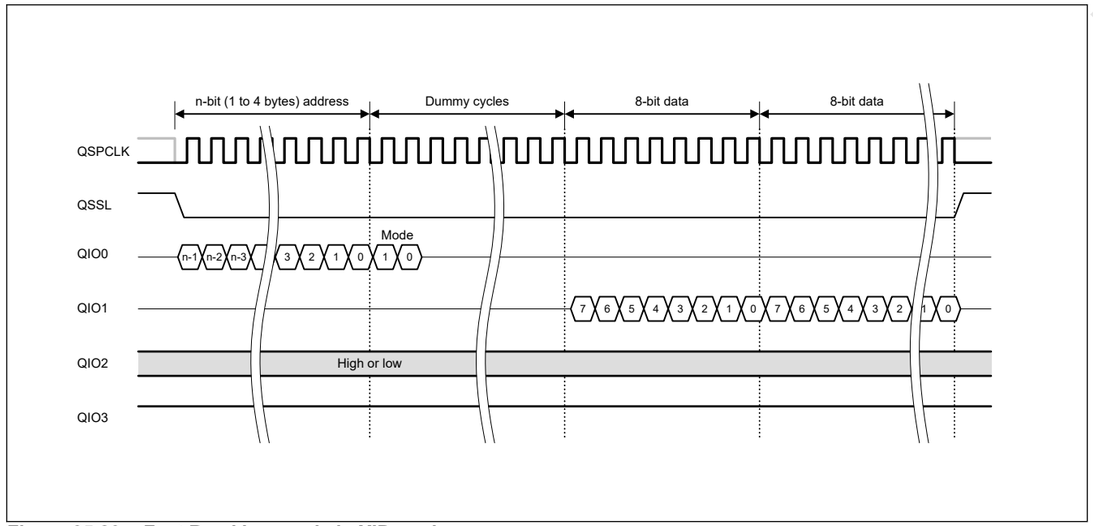

Figure 35.20 Fast Read bus cycle in XIP mode

Note: To use the Fast Read instruction, a serial flash memory that supports Fast Read transfers is required.

35.6.4 Fast Read Dual Output Instruction

The Fast Read Dual Output instruction is a read instruction that uses two signal lines to receive data. When the SPI bus cycle starts, the QSSL signal is asserted. The instruction code (0x3B or 0x3C) and an address with a width of 1 to 4 bytes,

接下来，发送由SFMSAC.SFMAS[1:0]位指定的1到4字节宽度的地址，生成由SFMSDC寄存器指定的虚拟周期，然后接收数据。

前两个虚拟周期用于选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPI总线周期。有关XIP模式的详细信息，请参阅第35.8节。XIP控制。

切换到快速读取指令在SFMSMD寄存器中进行控制。

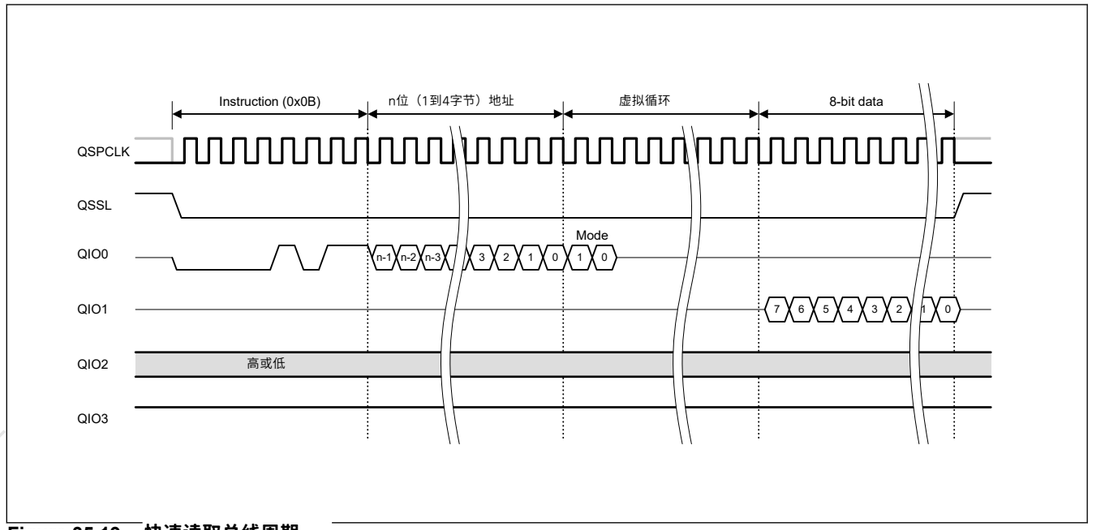

Figure 35.19 快速读取总线周期

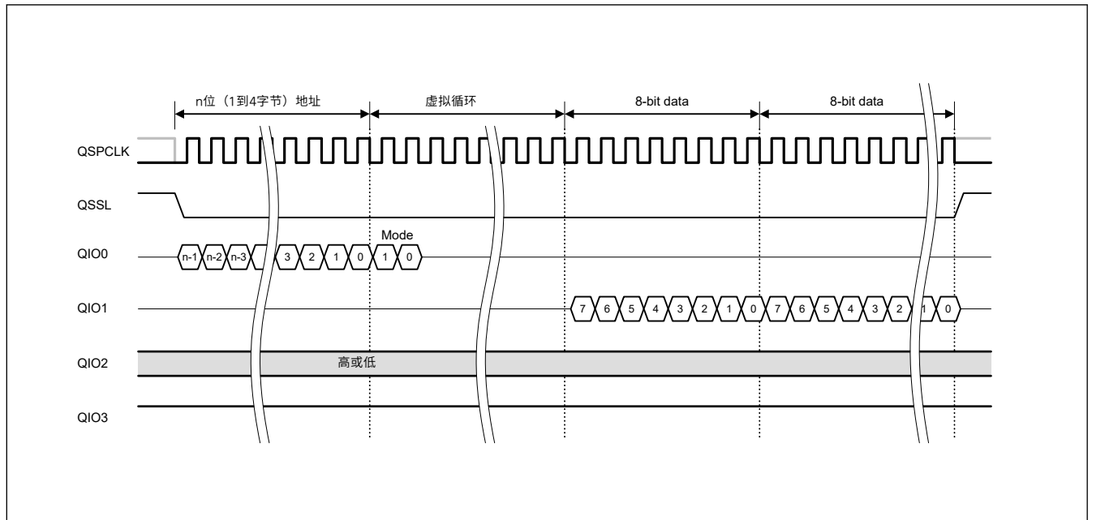

Figure 35.20 XIP模式下的快速读取总线周期

Note: 要使用快速读取指令，需要支持快速读取传输的串行闪存。

35.6.4 快速读取双输出指令

快速读取双输出指令是使用两条信号线接收数据的读取指令。当SPI总线周期开始时，QSSL信号被置位。指令代码（0x3B或0x3C）和一个宽度为1到4个字节的地址，

specified by the SFMSAC.SFMAS [1: 0] bits are transmitted from the QIO0 pin in the extended SPI protocol, and transmitted from the QIO0 and QIO1 pins in the Dual-SPI protocol. Next, a certain number of dummy cycles, specified in the SFMSDC register, is generated. Data is then received through the QIO0 and QIO1 pins. Even bit data is received from the QIO0 pin and odd bit data is received from the QIO1 pin.

The first two dummy cycles are used to select the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 35.8. XIP Control.

Switching to Fast Read Dual Output is controlled in the SFMSMD register.

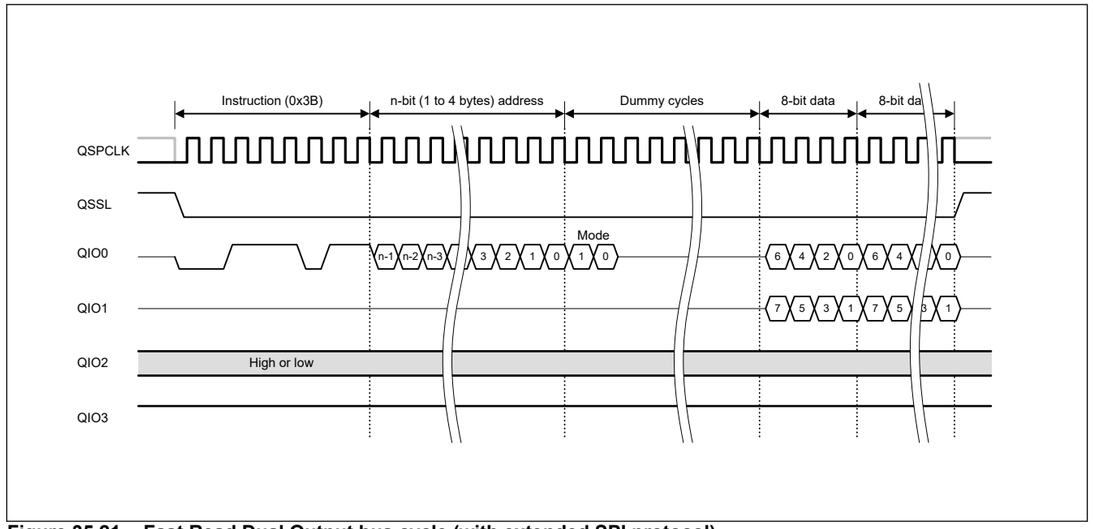

Figure 35.21 Fast Read Dual Output bus cycle (with extended SPI protocol)

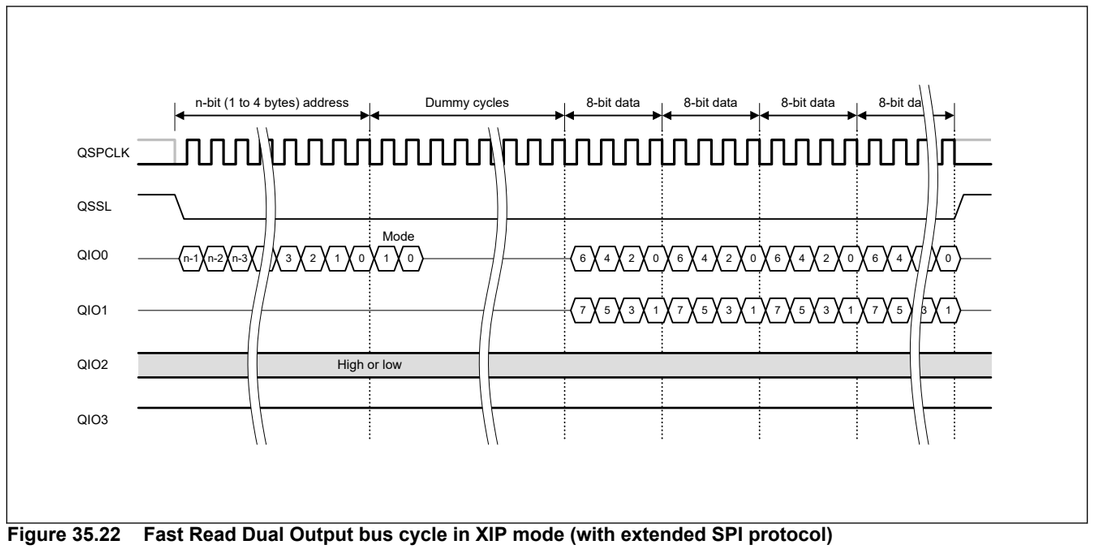

Figure 35.22 Fast Read Dual Output bus cycle in XIP mode (with extended SPI protocol)

Note: To use the Fast Read Dual Output instruction, a serial flash memory that supports Fast Read Dual Output transfers is required.

由SFMSAC.SFMAS[1:0]位指定在扩展SPI协议中从QIO0引脚传输，在Dual-SPI协议中从QIO0和QIO1引脚传输。接下来，生成在SFMSDC寄存器中指定的一定数量的虚拟周期。然后通过QIO0和QIO1引脚接收数据。从QIO0引脚接收偶数位数据，从QIO1引脚接收奇数位数据。

前两个虚拟周期用于选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPI总线周期。有关XIP模式的详细信息，请参阅第35.8节。XIP控制。

切换到快速读取双路输出由SFMSMD寄存器控制。

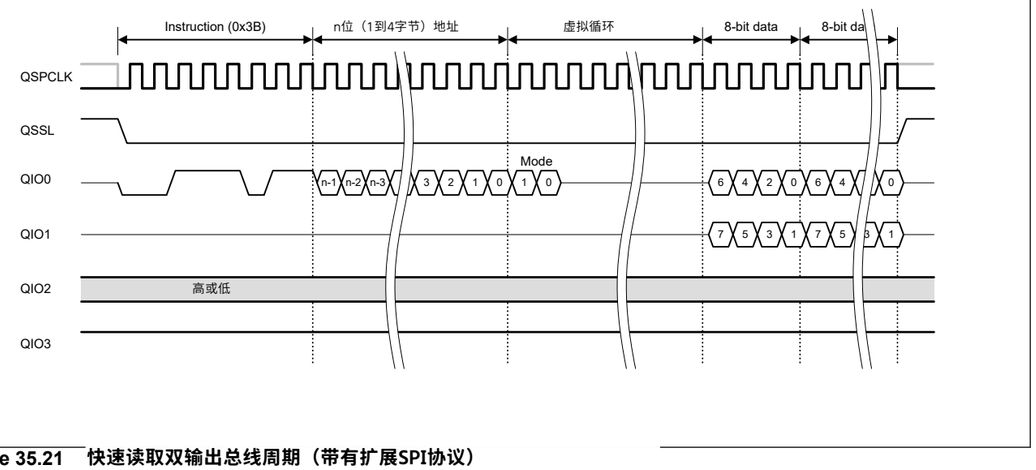

Figure 35.21 快速读取双输出总线周期（带有扩展SPI协议）

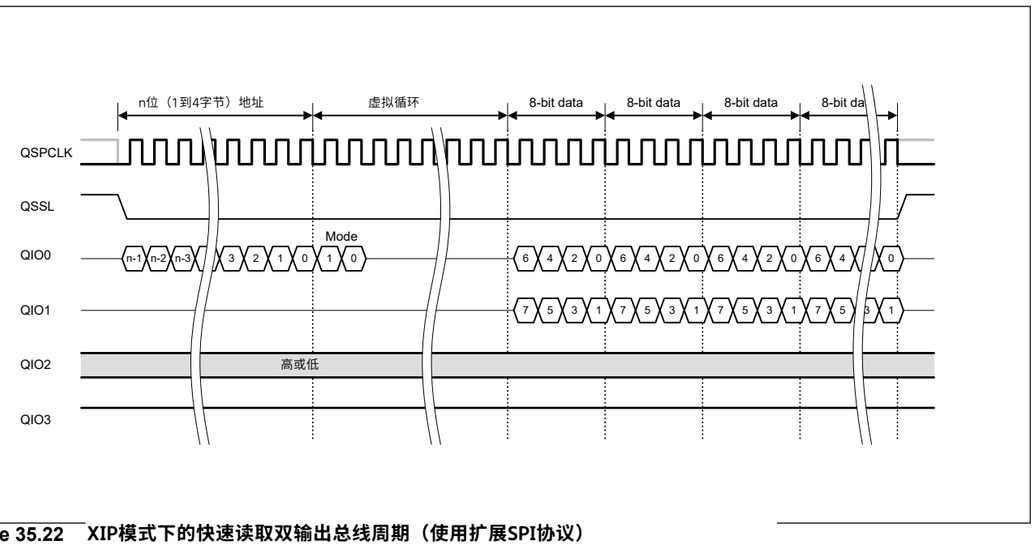

Figure 35.22 XIP模式下的快速读取双输出总线周期（使用扩展SPI协议）

Note: 要使用快速读取双输出指令，需要支持快速读取双输出传输的串行闪存。

35.6.5 Fast Read Dual I/O Instruction

The Fast Read Dual I/O instruction is a read instruction that uses two signal lines to transmit an address and receive data. When the SPI bus cycle starts, the QSSL signal is asserted, and the instruction code (0xBB / 0xBC) is transmitted from QIO0 pin in the extended SPI protocol and from QIO0, and QIO1 pins in the Dual SPI protocol. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted through the QIO0 and QIO1 pins, and a certain number of dummy cycles, specified in the SFMSDC register, is generated. Data is then is received through the QIO0 and QIO1 pins. Address and dummy cycle transmission and data reception are performed through the QIO0 pin for even bits and through the QIO1 pin for odd bits.

The first two dummy cycles are used to select the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 35.8. XIP Control.

Switching to Fast Read Dual I/O is controlled in the SFMSMD register.

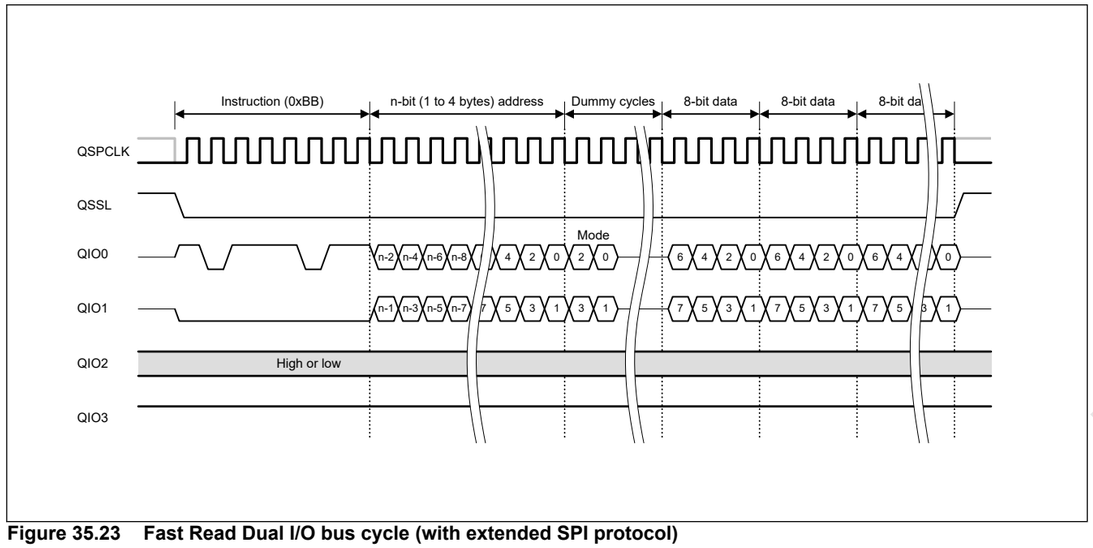

Figure 35.23 Fast Read Dual I/O bus cycle (with extended SPI protocol)

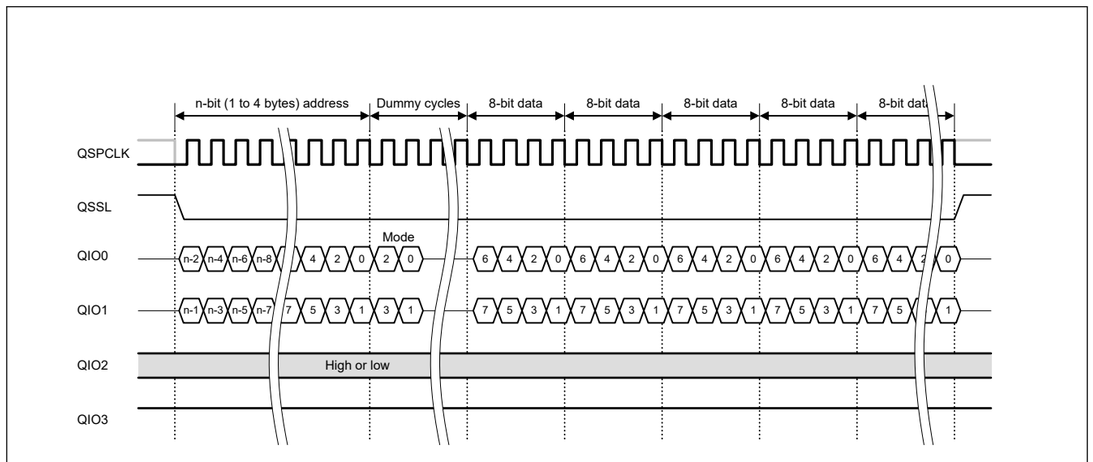

Figure 35.24 Fast Read Dual I/O bus cycle in XIP mode

35.6.5 快速读取双IO指令

FastReadDualIO指令是使用两条信号线传输地址和接收数据的读取指令。当SPI总线周期开始时，QSSL信号被置位，指令代码（0xBB0xBC）从扩展SPI协议中的QIO0引脚和双SPI协议中的QIO0和QIO1引脚传输。接下来，在SFMSAC寄存器的SFMAS[1:0]位中指定的1到4字节宽度的地址通过QIO0和QIO1引脚以及在SFMSDC寄存器中指定的一定数量的空周期发送 生成。然后通过QIO0和QIO1引脚接收数据。地址和虚拟周期的发送和数据接收通过QIO0引脚（偶数位）和QIO1引脚（奇数位）执行。

前两个虚拟周期用于选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPI总线周期。有关XIP模式的详细信息，请参阅第35.8节。XIP控制。

切换到快速读取双IO由SFMSMD寄存器控制。

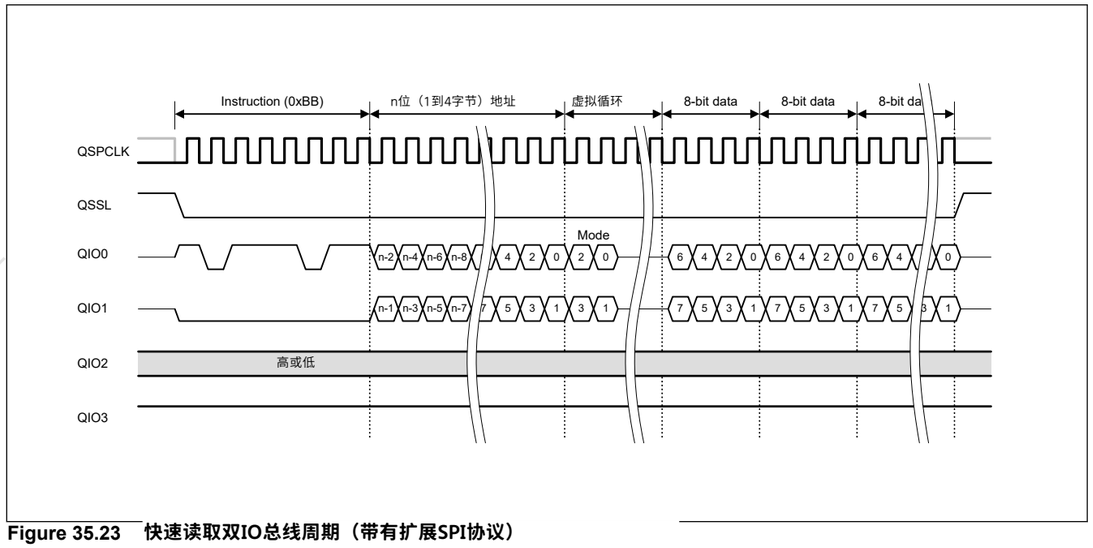

Figure 35.23 快速读取双IO总线周期（带有扩展SPI协议）

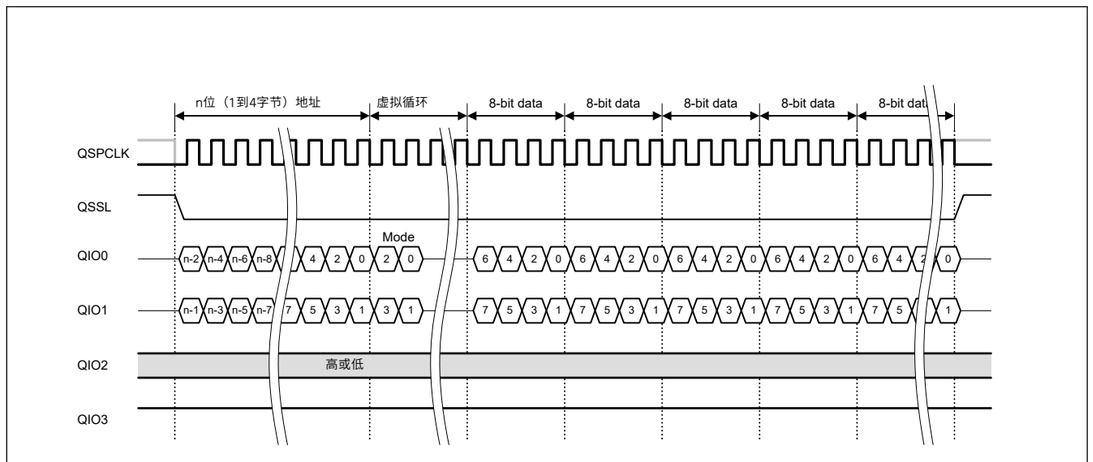

Figure 35.24 XIP模式下的快速读取双IO总线周期

Note: To use the Fast Read Dual I/O instruction, a serial flash memory that supports Fast Read Dual I/O transfers is required.

35.6.6 Fast Read Quad Output Instruction

The Fast Read Quad Output instruction is a read instruction that uses four signal lines to receive data. When the SPI bus cycle starts, the QSSL signal is asserted. The instruction code (0x6B or 0x6C) and an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, are output from the QIO0 pin. Next, a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSMD register, are generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

The first two dummy cycles are used to select the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 35.8. XIP Control.

Switching to Fast Read Quad Output is controlled in the SFMSMD register.

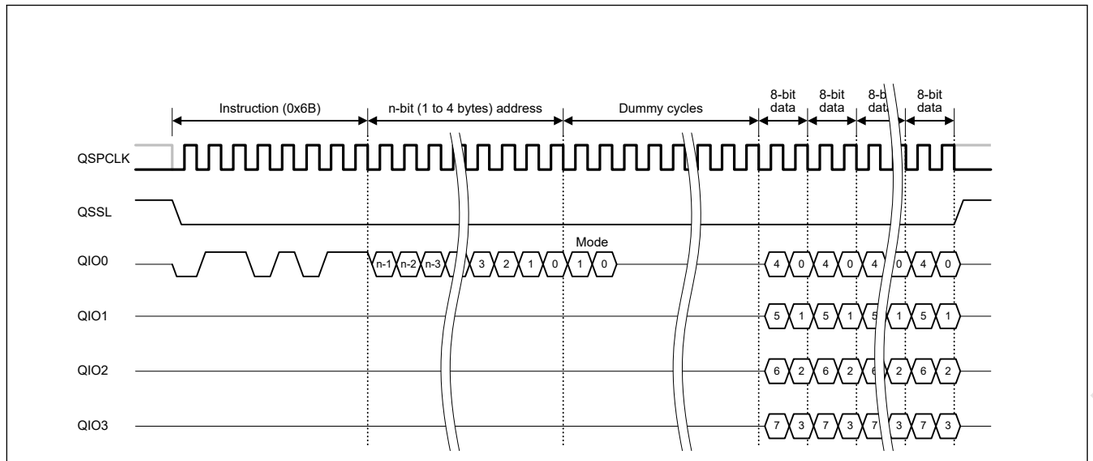

Figure 35.25 Fast Read Quad Output bus cycle (with extended SPI protocol)

Note: 要使用快速读取双IO指令，需要支持快速读取双IO传输的串行闪存。

35.6.6 快速读取四路输出指令

快速读取四路输出指令是使用四根信号线接收数据的读取指令。当SPI总线周期开始时，QSSL信号被置位。在SFMSAC寄存器的SFMAS[1:0]位中指定的指令代码（0x6B或0x6C）和宽度为1到4字节的地址从QIO0引脚输出。接下来，生成一定数量的空周期，在SFMSMD寄存器的SFMDN[3:0]位中指定。然后通过QIO0、QIO1、QIO2和QIO3引脚接收数据。

前两个虚拟周期用于选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPI总线周期。有关XIP模式的详细信息，请参阅第35.8节。XIP控制。

切换到快速读取四路输出由SFMSMD寄存器控制。

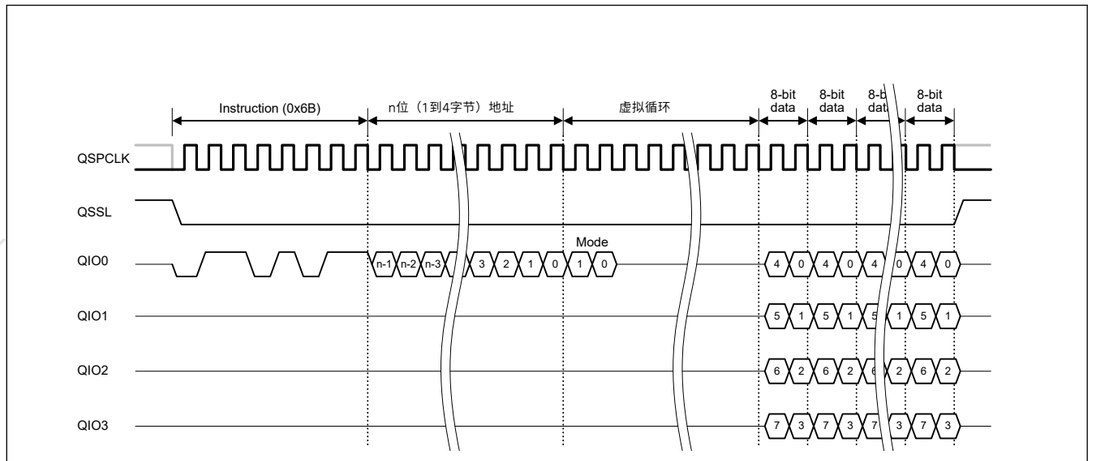

Figure 35.25 快速读取四路输出总线周期（使用扩展SPI协议）

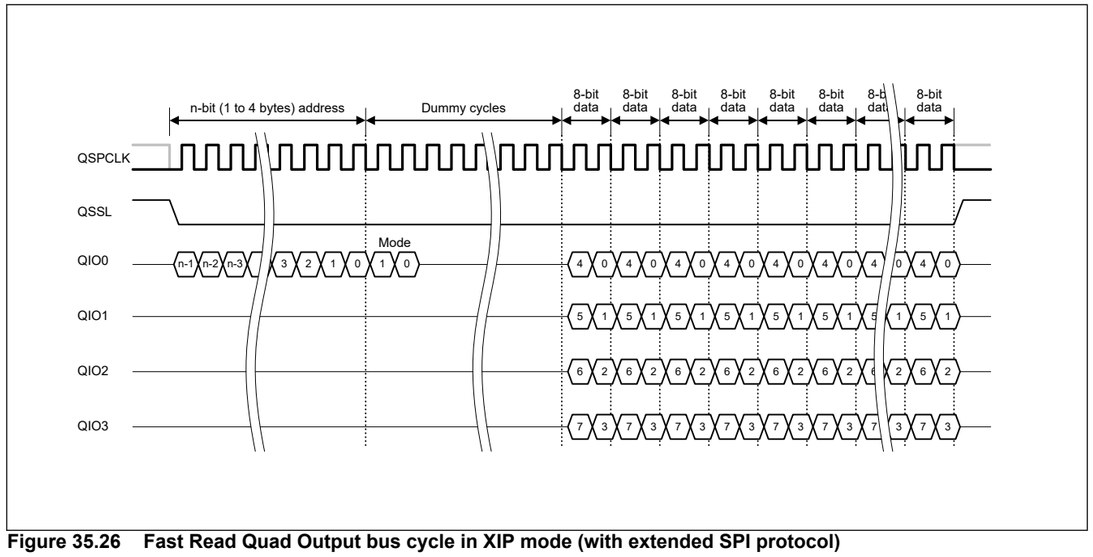

Figure 35.26 Fast Read Quad Output bus cycle in XIP mode (with extended SPI protocol)

Note: To use Fast Read Quad Output, a serial flash memory that supports Fast Read Quad Output transfer is required.

35.6.7 Fast Read Quad I/O Instruction

The Fast Read Quad I/O instruction is a read instruction that uses four signal lines to transmit an address and receive data. When the SPI bus cycle starts, the QSSL signal is asserted, and the instruction code (0xEB / 0xEC) is transmitted from QIO0 pin in the extended SPI protocol and from QIO0, QIO1, QIO2, and QIO3 pins in the Quad-SPI protocol. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted through the QIO0, QIO1, QIO2, and QIO3 pins, and a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSMD register, is generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

The first two dummy cycles are used to select the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 35.8. XIP Control.

Switching to Fast Read Quad I/O is controlled in the SFMSMD register.

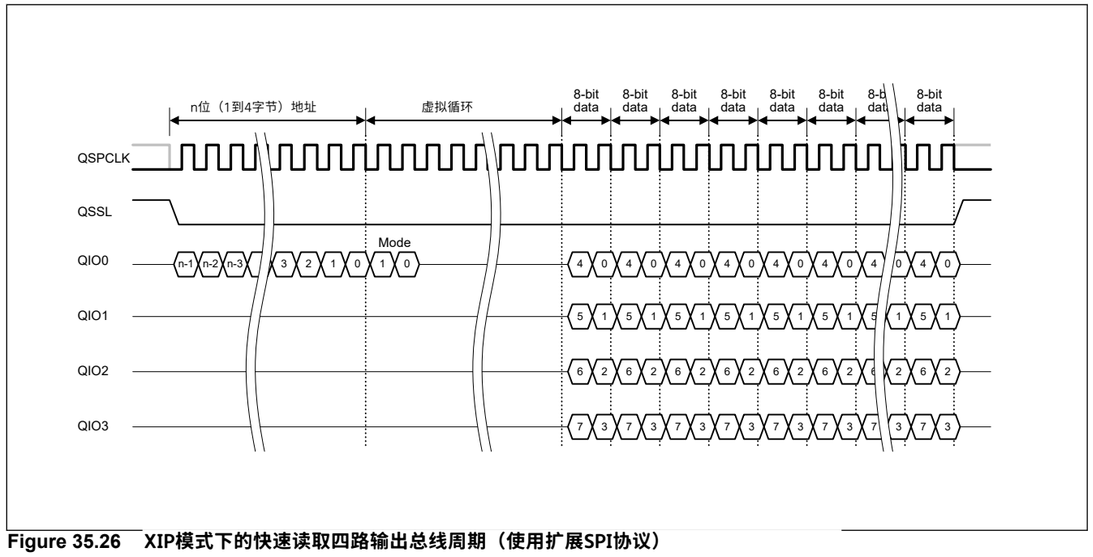

Figure 35.26 XIP模式下的快速读取四路输出总线周期（使用扩展SPI协议）

Note: 要使用快速读取四路输出，需要支持快速读取四路输出传输的串行闪存。

35.6.7 快速读取QuadIO指令

FastReadQuadIO指令是使用四根信号线传输地址和接收数据的读取指令。

当SPI总线周期开始时，QSSL信号被置位，指令代码（0xEB0xEC）从扩展SPI协议的QIO0引脚和Quad-SPI协议的QIO0、QIO1、QIO2和QIO3引脚传输。接下来，在SFMSAC寄存器的SFMAS[1:0]位中指定的1到4字节宽度的地址通过QIO0、QIO1、QIO2和QIO3引脚和一定数量的空周期传输，在SFMDN[3:0]位中指定

SFMSMD寄存器，生成。然后通过QIO0、QIO1、QIO2和QIO3引脚接收数据。

前两个虚拟周期用于选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPI总线周期。有关XIP模式的详细信息，请参阅第35.8节。XIP控制。

切换到快速读取四线IO由SFMSMD寄存器控制。

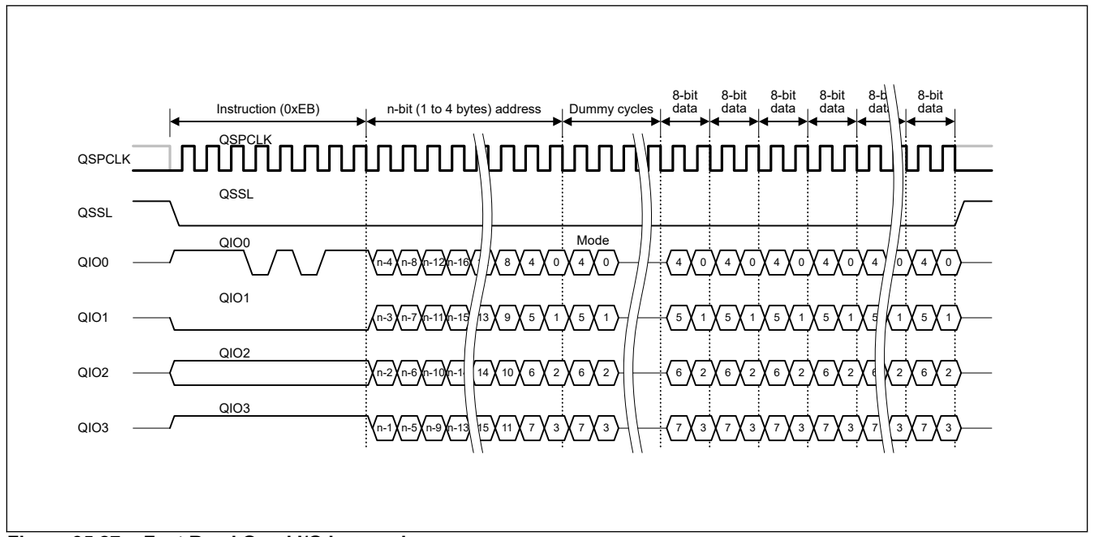

Figure 35.27 Fast Read Quad I/O bus cycle

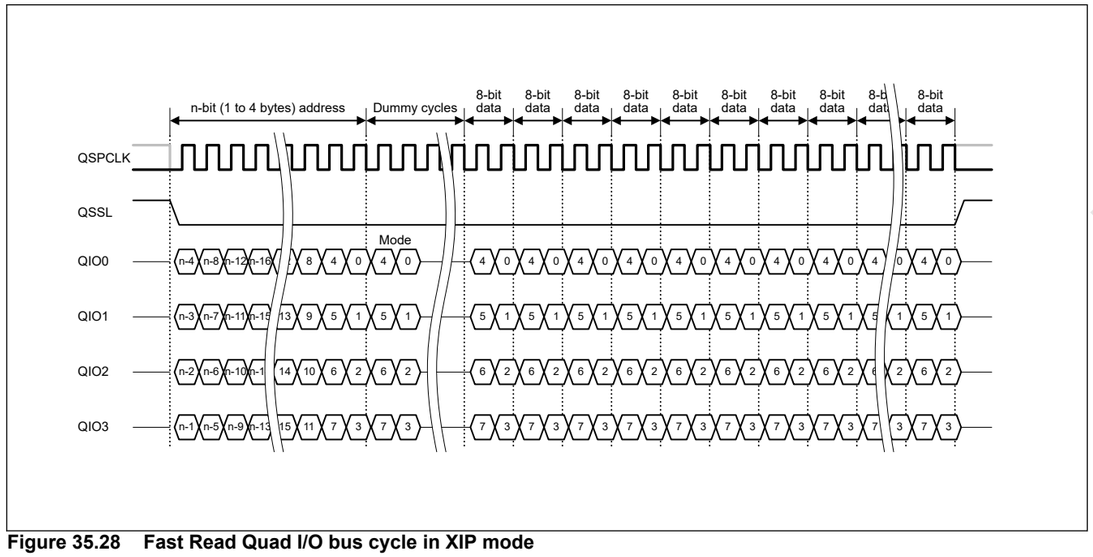

Figure 35.28 Fast Read Quad I/O bus cycle in XIP mode

Note: To use the Fast Read Quad I/O instruction, a serial flash memory that supports Fast Read Quad I/O transfers is required.

35.6.8 Enter 4-Byte Mode Instruction

The Enter 4-Byte Mode instruction sets the serial flash address width to 4 bytes. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (0xB7) is output.

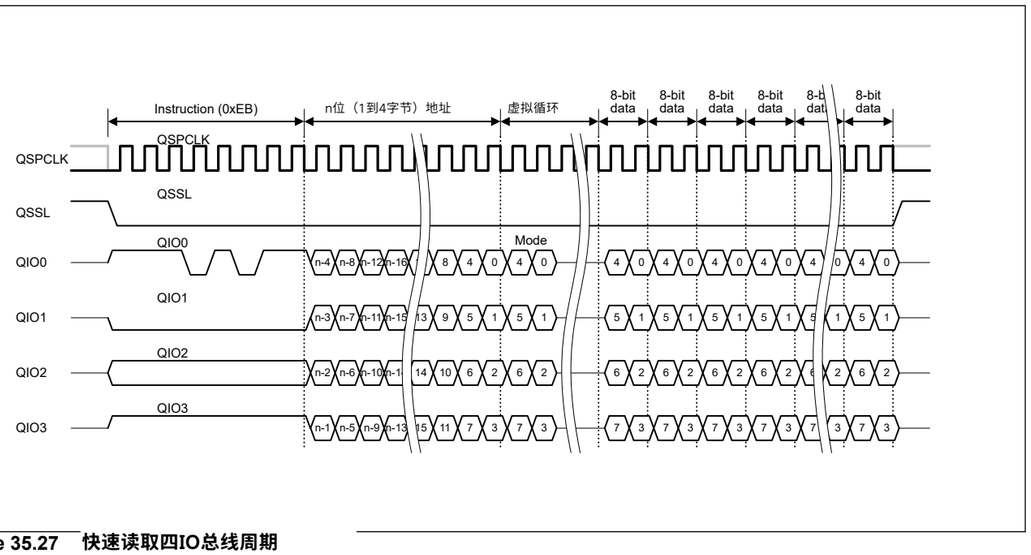

Figure 35.27 快速读取四IO总线周期

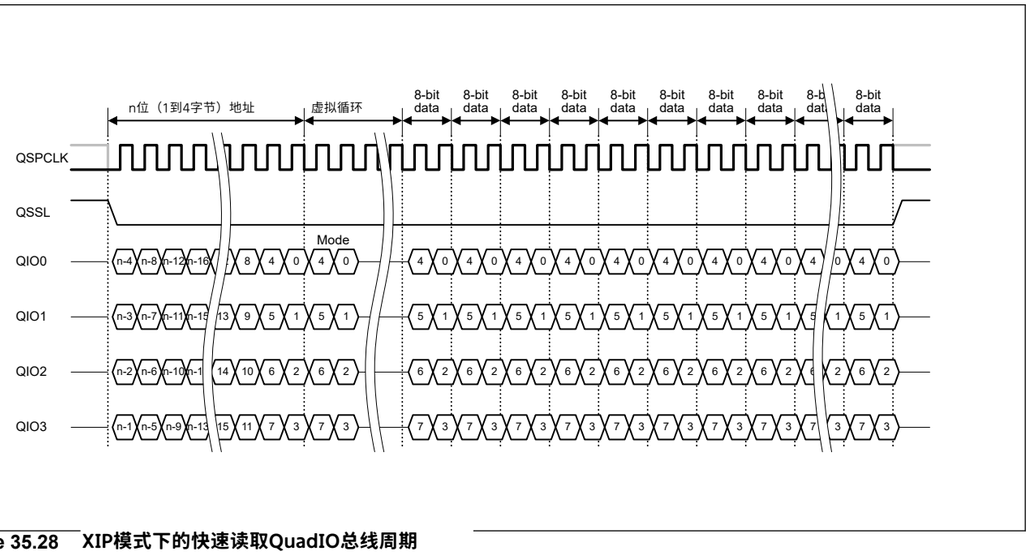

Figure 35.28 XIP模式下的快速读取QuadIO总线周期

Note: 要使用FastReadQuadIO指令，需要支持FastReadQuadIO传输的串行闪存。

35.6.8 进入4字节模式指令

进入4字节模式指令将串行闪存地址宽度设置为4字节。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（0xB7）。

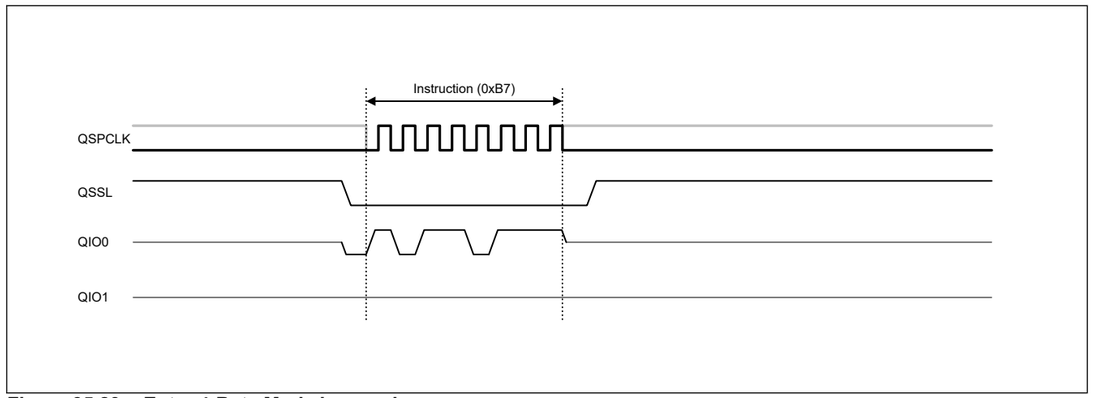

Figure 35.29 Enter 4-Byte Mode bus cycle

Note: The Enter 4-Byte Mode instruction is issued regardless of whether the serial flash is in 3- or 4-byte mode.

35.6.9 Exit 4-Byte Mode Instruction

The Exit 4-Byte Mode instruction sets the serial flash address width to 3 bytes. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (0xE9) is output.

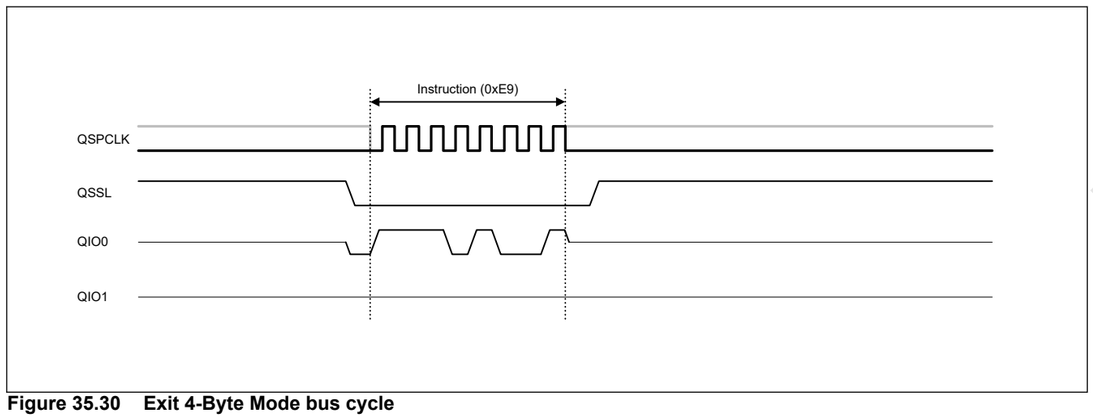

Figure 35.30 Exit 4-Byte Mode bus cycle

Note: The Exit 4-Byte Mode instruction is issued regardless of whether the serial flash is in 3- or 4-byte mode.

35.6.10 Write Enable Instruction

The Write Enable instruction enables changing of the serial flash address width. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (0x06) is output.

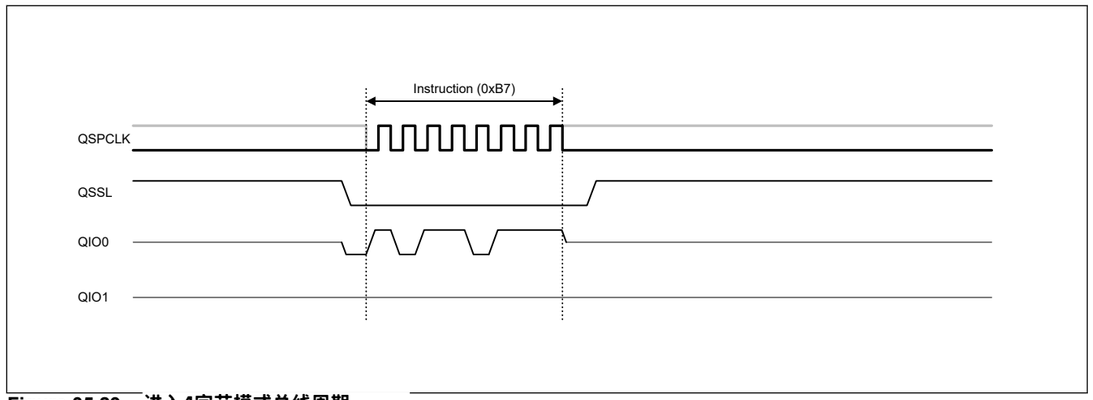

Figure 35.29 进入4字节模式总线周期

Note: 无论串行闪存是处于3字节模式还是4字节模式，都会发出进入4字节模式指令。

35.6.9 退出4字节模式指令

退出4字节模式指令将串行闪存地址宽度设置为3字节。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（0xE9）。

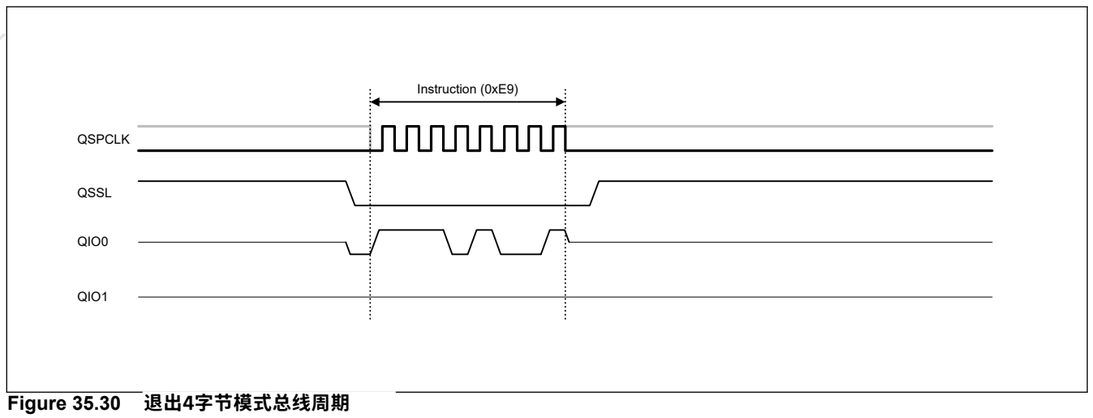

Figure 35.30 退出4字节模式总线周期

Note: 无论串行闪存是处于3字节模式还是4字节模式，都会发出退出4字节模式指令。

35.6.10 写使能指令

写使能指令可以改变串行闪存地址宽度。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（0x06）。

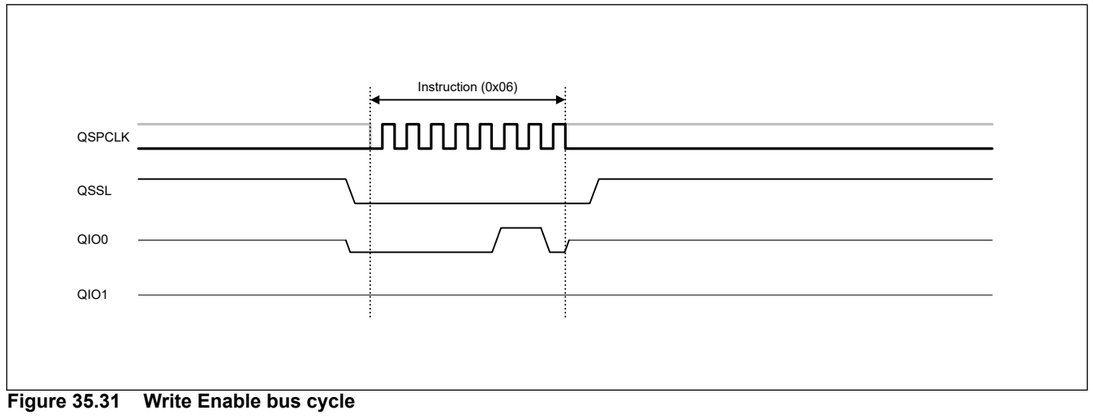

Figure 35.31 Write Enable bus cycle

35.7 SPI Bus Cycle Arrangement

35.7.1 Serial Flash Memory Read Based on Individual Conversion

ROM read bus cycles are individually converted to SPI bus cycles on a one-to-one basis. When a ROM read bus cycle is detected, the QSSL signal is asserted, and an SPI bus cycle starts. When the data receiving is finished from the serial flash memory, the QSSL signal is negated and the SPI bus cycle is complete.

When the next ROM read bus cycle is detected, the QSSL signal set by the SFMSSC.SFMSW[3: 0] bits is asserted again, then the next SPI bus cycle starts.

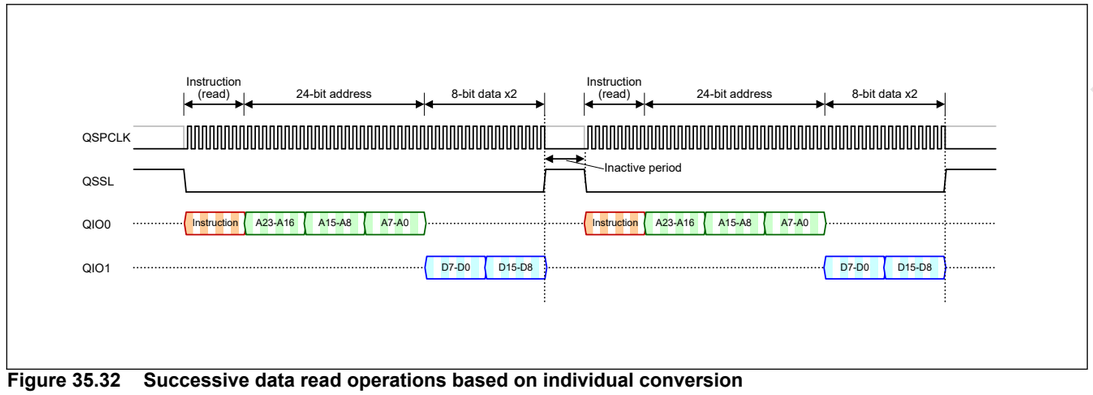

Figure 35.32 Successive data read operations based on individual conversion

35.7.2 Serial Flash Memory Read Using the Prefetch Function

In operations such as CPU instruction execution and block data transfer, data is often read in ascending order from contiguous addresses. Serial flash memory provides the ability to repeat data reception without reissuing an instruction code and address. To work with this function, the QSPI has a prefetch function for continuous data reception. However, if the CPU issues a flash read request for discontinuous flash addresses, SPI bus cycles are separated from each other, disabling the prefetch function.

To enable the prefetch function of the QSPI, set the SFMPFE bit in the SFMSMD register to 1. When the prefetch function is enabled, data is received continuously and stored in the prefetch buffer of the QSPI, without waiting for another flash read request. When the CPU issues a flash read request, an address check is made. If an address match is confirmed, the data in the buffer is passed to the CPU. If an address mismatch is detected, the data in the buffer is discarded and a new SPI bus cycle is issued.

The buffer for prefetching is 18 bytes long. When this buffer is full, the SPI bus cycle is ended. When the buffer data is read to create free space, a new SPI bus cycle is automatically started to resume prefetching.

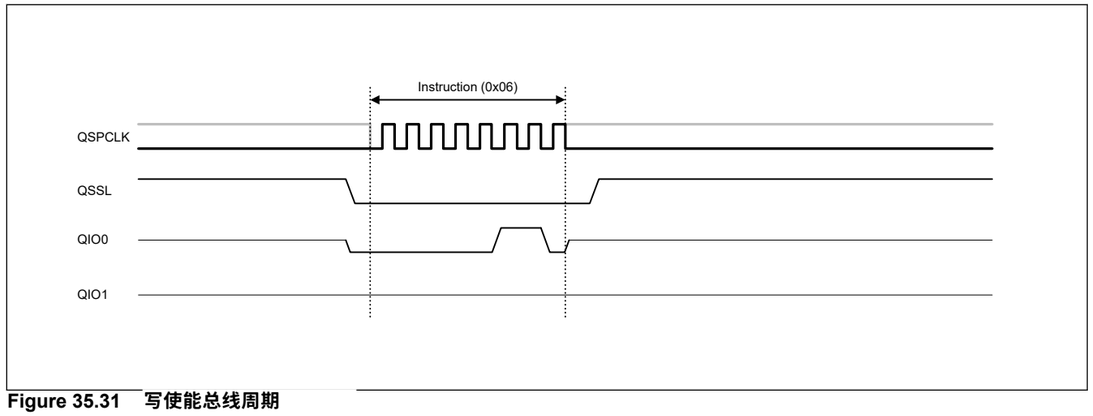

Figure 35.31 写使能总线周期

35.7 SPI总线周期安排

35.7.1 基于单独转换的串行闪存读取

ROM读取总线周期以一对一的方式单独转换为SPI总线周期。当检测到ROM读取总线周期时，QSSL信号被置位，并且SPI总线周期开始。当从串行闪存完成数据接收时，QSSL信号被取反，SPI总线周期完成。

当检测到下一个ROM读取总线周期时，由SFMSSC.SFMSW[3:0]位设置的QSSL信号再次置位，然后下一个SPI总线周期开始。

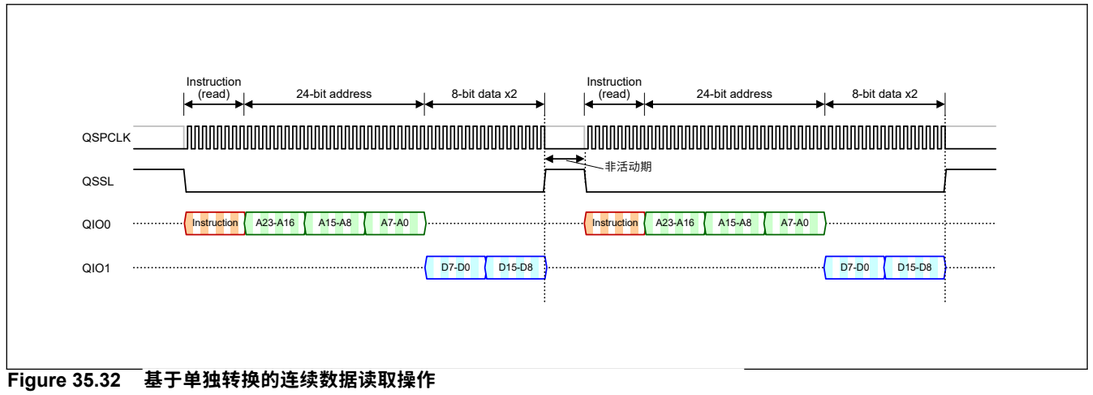

Figure 35.32 基于单独转换的连续数据读取操作

35.7.2 使用预取功能读取串行闪存

在CPU指令执行和块数据传输等操作中，数据通常是从连续地址按升序读取的。串行闪存提供了重复数据接收的能力，而无需重新发出指令代码和地址。为了使用此功能，QSPI具有用于连续数据接收的预取功能。但是，如果CPU对不连续的闪存地址发出闪存读取请求，则SPI总线周期会相互分离，从而禁用预取功能。

要使能QSPI的预取功能，请将SFMSMD寄存器中的SFMPFE位设置为1。当使能预取功能时，会连续接收数据并存储在QSPI的预取缓冲区中，而无需等待另一个闪存读取请求。当CPU发出闪存读取请求时，会进行地址检查。如果确认地址匹配，则将缓冲区中的数据传递给CPU。如果检测到地址不匹配，则丢弃缓冲区中的数据并发出新的SPI总线周期。

用于预取的缓冲区为18字节长。当此缓冲区满时，SPI总线周期结束。当缓冲区数据被读取以创建空闲空间时，会自动启动一个新的SPI总线周期以恢复预取。

The prefetch function allows for efficient transfer operations when data is read in ascending order from contiguous addresses, as in instruction fetch and block data transfer.

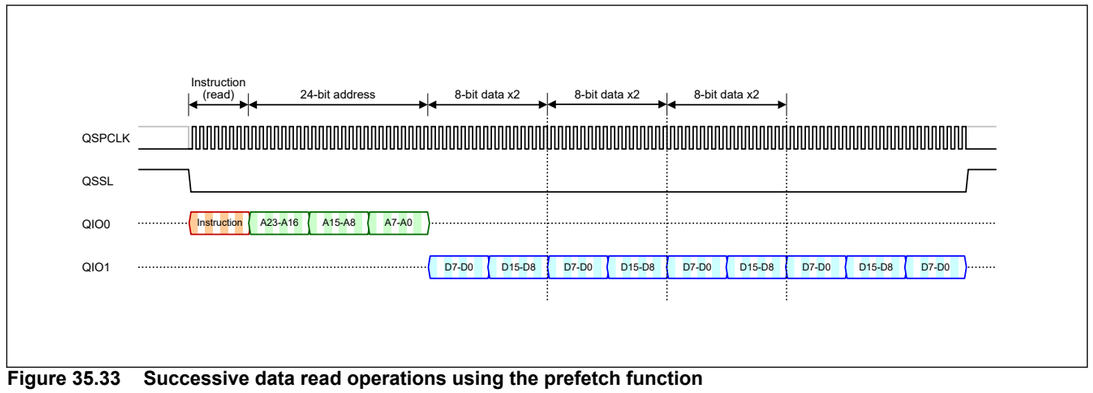

Figure 35.33 Successive data read operations using the prefetch function

35.7.3 Halt of Prefetching

If a serial flash memory read request for discontinuous addresses is issued when continuous data is being received by the prefetch function, the transfer of continuous data being made is halted and a new SPI bus cycle is started. Usually, such a halt of serial transfer occurs on data reception byte boundaries. However, if the SFMPAE bit in the SFMSMD register is set to 1, the halt can occur on locations other than byte boundaries.

35.7.4 Direct Specification of Prefetch Destination

When the prefetch function is enabled (SFMSMD.SFMPFE = 1), when writing to the QSPI window area occurs, after the writing is completed, prefetching starts from the write start address. Writes to serial flash memory cannot be performed.

Combining this function with described in section 35.7.5. Prefetch State Polling, can reduce the load on the internal bus when data is read from a low-speed serial flash memory.

Note: Writing to the QSPI window area with a data size of 2 bytes or more causes a hardfault.

35.7.5 Prefetch State Polling

A read by CPU from a low-speed serial flash memory causes the CPU system bus to be occupied until completion of the SPI reception bus cycle. The prefetch state polling function is provided to reduce this load.

The PFOFF bit in the Status Register (SFMSST) register indicates the state of the prefetch function, and the PFCNT[4:0] bits in the SFMSST register indicate the number of data bytes already prefetched. Place the polling program in the SRAM of this device.

```
//
// copy 1K byte (32bit x 256 word) data from serial flash to internal SRAM
//
unsigned long *sptr; // pointer for the serial flash
unsigned long *dptr; // pointer for the destination
int i;

SFMSMD |= 0x0040; // set SFMPFE bit to enable prefetch
*( (volatile unsigned char *) sptr ) = 0; // make the TAG valid to start prefetch

for ( i = 0 ; i < 256 ; i++ ){
while ( ( SFMSST & 0x00FF ) < 0x04 ){}; // waiting for 4-byte data to be received
*(dptr++) = *(sptr++);
}
```

Note: When executing a polling program, place the program outside of the serial flash memory. If the polling program is executed when the program is placed on the serial flash memory, the prefetch target frequently switches to an instruction code. This eliminates the effect of polling, and an infinite loop can result because the prefetch buffer is not filled.

当从连续地址以升序读取数据时，预取功能允许有效的传输操作，如在指令取指和块数据传输中。

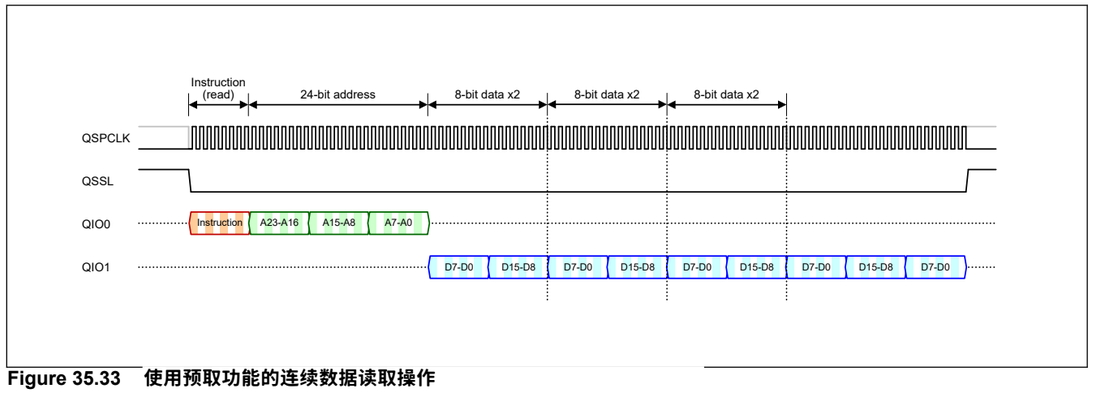

Figure 35.33 使用预取功能的连续数据读取操作

35.7.3 停止预取

如果在预取功能正在接收连续数据时发出对不连续地址的串行闪存读取请求，则正在进行的连续数据的传输将停止并开始新的SPI总线周期。通常，这种串行传输的停止发生在数据接收字节边界上。但是，如果SFMSMD寄存器中的SFMPAE位设置为1，则停止可能发生在字节边界以外的位置。

35.7.4 直接指定预取目的地

当预取功能使能时（SFMSMD.SFMPFE=1），当写入QSPI窗口区域时，写入完成后，从写入起始地址开始预取。无法执行对串行闪存的写入。

将此功能与第35.7.5节中的描述相结合。PrefetchStatePolling，可以减少从低速串行闪存读取数据时内部总线的负载。

Note: 写入数据大小为2字节或更大的QSPI窗口区域会导致硬故障。

35.7.5 预取状态轮询

CPU从低速串行闪存中读取会导致CPU系统总线被占用，直到完成
SPI接收总线周期。提供了预取状态轮询功能来减少这种负载。

状态寄存器(SFMSST)寄存器中的PFOFF位指示预取功能的状态，SFMSST寄存器中的PFCNT[4:0]位指示已经预取的数据字节数。将轮询程序放在本设备的SRAM中。

```
将1K字节（32位x256字）数据从      串行闪存复制到内部SRAM无符号长*sptr；串行闪存指针un
signedlong*dptr;目标inti的指针；




SFMSMD=0x0040；设置SFMPFE位以启用预取*((volatileunsignedchar*)sptr)=0;使TAG有效以开始预
取

for(i=0;i<256;i++){而((SFMSST&0x00FF)<0x04){ ;等待接收4字节数据*(dptr++)=*(sptr++);
```

Note: 执行轮询程序时，请将程序置于串行闪存之外。如果轮询程序在程序放在串行闪存上时执行，则预取目标频繁切换到指令代码。这消除了轮询的影响，并且由于未填充预取缓冲区可能导致无限循环。

35.7.6 SPI Bus Cycle Extension Function

If the SFMSE[1:0] bits in the SFMSMD register are set to a value other than 00b, the QSPI waits for the next flash read. At this time, the QSPCLK signal stops, the QSSL signal is kept active low even after data is obtained from the serial flash memory, and the SPI bus cycle is suspended.

If the address of the next flash read is contiguous in ascending order, the toggling of the QSPCLK signal is restarted to continue reception of subsequent data. If the address of the next flash read is not contiguous in ascending order, the QSSL signal is driven high once to end the SPI bus cycle being suspended. A new SPI bus cycle is then started.

When data is read intermittently from ascending order contiguous addresses, this function enables an efficient transfer operation to be performed by reducing the overhead for instruction code and address transmission.

The SPI bus cycle extension time is selectable in the SFMSE[1:0] bits in the SFMSMD register. When the specified extension time elapses, the QSSL signal returns to the high level to automatically end the SPI bus cycle being suspended. If the SFMSE[1:0] bits are set to 11b, QSSL is extended infinitely. This increases the power consumption of the serial flash memory.

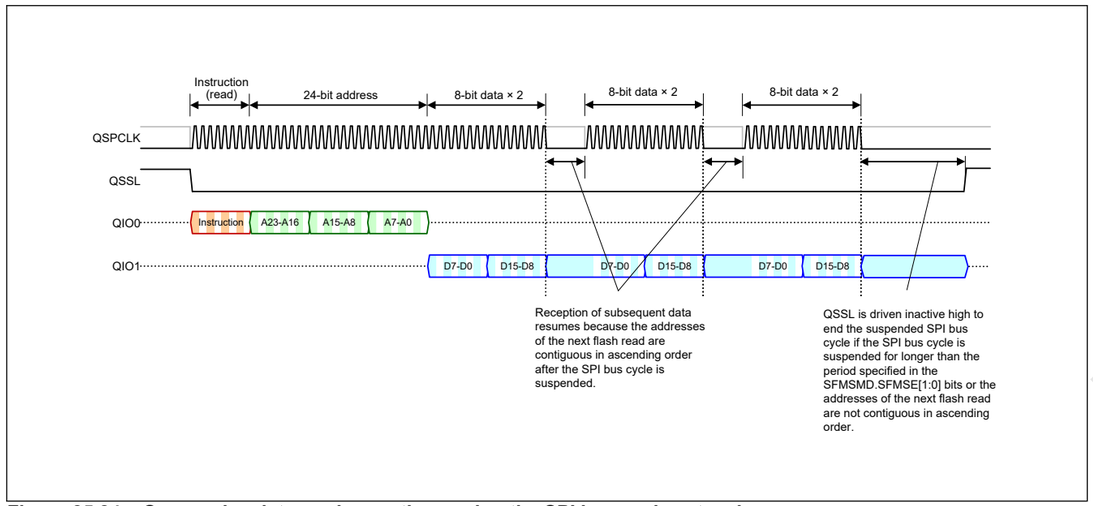

Figure 35.34 Successive data read operations using the SPI bus cycle extension

35.8 XIP Control

Some serial flash memory devices allow latencies to be reduced by skipping instruction code reception for flash reads. This instruction code skip function is selected in mode data received during the dummy cycle period of the previous serial bus cycle.

In the dummy cycle of the Fast Read instructions, the QSPI controls the XIP mode of the serial flash memory by using the serial data signal to send the mode data set in the SFMXD[7:0] bits in the SFMSDC register during the first 2 cycles, as shown in Figure 35.35.

The mode data to enable the XIP mode differs for each serial flash memory. Accordingly, set the appropriate mode data in the SFMXD[7:0] bits.

35.7.6 SPI总线周期扩展功能

如果SFMSMD寄存器中的SFMSE[1:0]位设置为00b以外的值，则QSPI等待下一次闪存读取。此时，QSPCLK信号停止，即使从串行闪存中获取数据后，QSSL信号也保持低电平有效，并且暂停SPI总线周期。

如果下一次闪存读取的地址按升序连续，则重新启动QSPCLK信号的翻转以继续接收后续数据。如果下一次flash读取的地址升序不连续，则QSSL信号被驱动一次高电平以结束暂停的SPI总线周期。然后开始一个新的SPI总线周期。

当从升序连续地址间歇性地读取数据时，该功能通过减少指令代码和地址传输的开销来实现高效的传输操作。

SPI总线周期延长时间可在SFMSMD寄存器的SFMSE[1:0]位中选择。当指定的延长时间过去后，QSSL信号返回高电平，自动结束暂停的SPI总线周期。如果SFMSE[1:0]位设置为11b，QSSL将无限扩展。这增加了串行闪存的功耗。

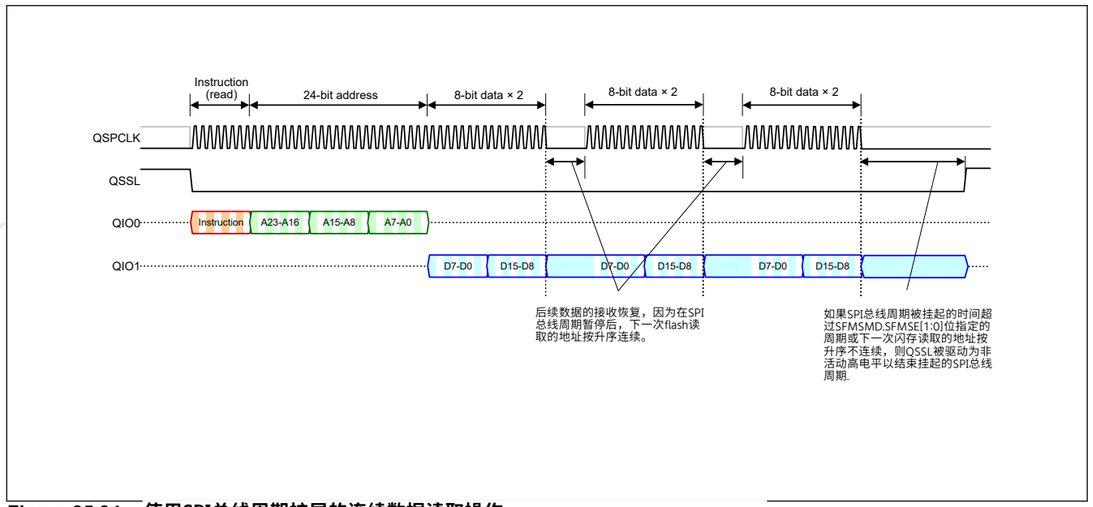

Figure 35.34 使用SPI总线周期扩展的连续数据读取操作

35.8 XIP Control

一些串行闪存设备允许通过跳过用于闪存读取的指令代码接收来减少延迟。在前一个串行总线周期的虚拟周期期间接收到的模式数据中选择此指令代码跳过功能。

在快速读取指令的空周期中，QSPI控制串行闪存的XIP模式，在前2循环，如图35.35所示。

启用XIP模式的模式数据因串行闪存而异。因此，在SFMXD[7:0]位中设置适当的模式数据。

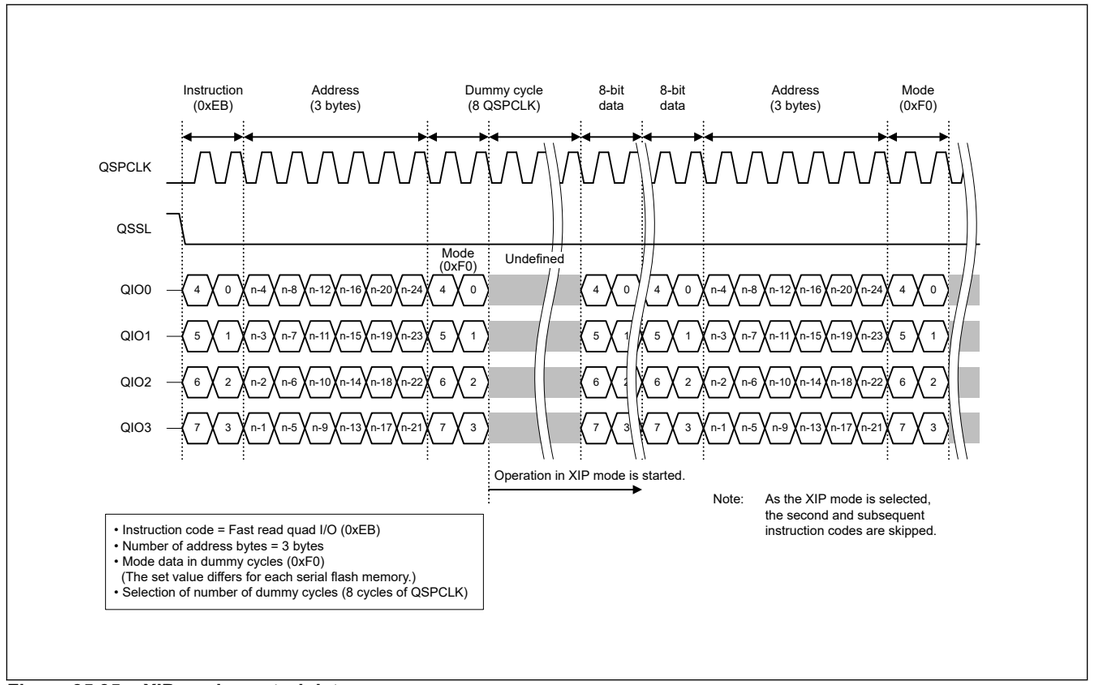

Figure 35.35 XIP mode control data

35.8.1 Setting XIP Mode

To start XIP mode in serial flash memory, perform the following register settings:

- Set a mode data value in the SFMXD[7:0] bits in the SFMSDC register.*1
- Set the SFMXEN bit in the SFMSDC register to 1.

In the dummy cycle of the first fast read cycle after these registers are set, the mode data value set in the register is transferred. From that point, XIP mode is enabled in the serial flash memory. To confirm the current XIP mode status, read the SFMXST flag in the SFMSDC register.

Note 1. In the SFMXD[7:0] bits in the SFMSDC register, set the mode data that follows the specifications for the actual serial flash memory.

The following figure shows an example of the XIP mode setting procedure.

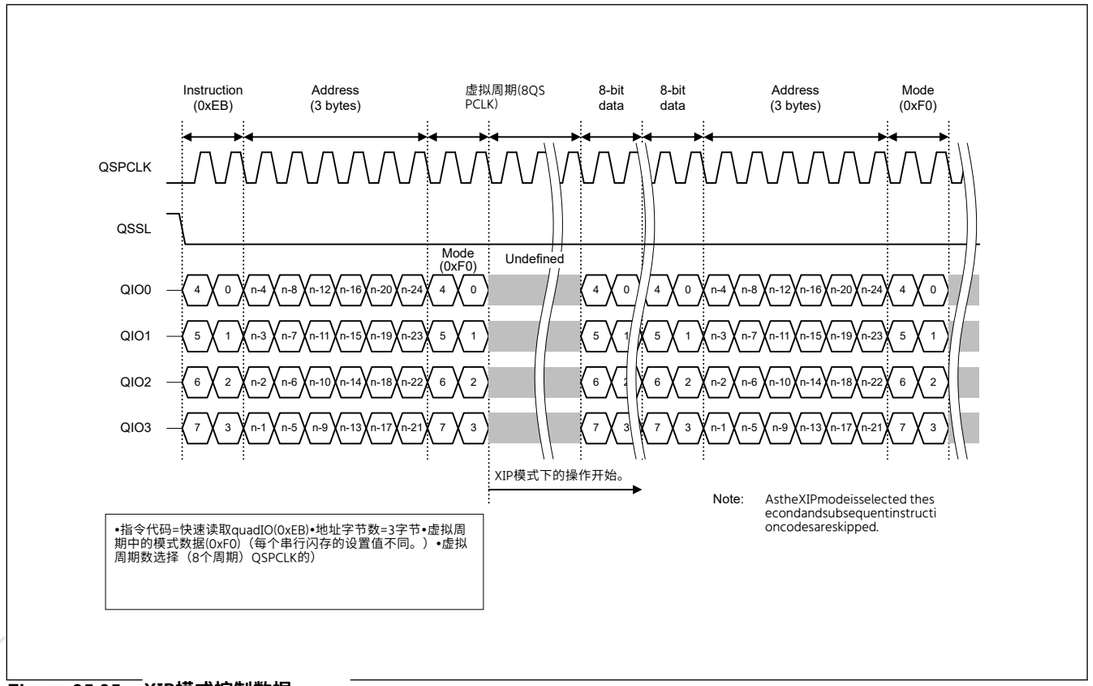

Figure 35.35 XIP模式控制数据

35.8.1 设置XIP模式

要在串行闪存中启动XIP模式，请执行以下寄存器设置：

●在SFMSDC寄存器的SFMXD[7:0]位中设置模式数据值。*1

●将SFMSDC寄存器中的SFMXEN位设置为1。

在设置这些寄存器后的第一个快速读取周期的空周期中，传输寄存器中设置的模式数据值。从那时起，串行闪存中的XIP模式被启用。要确认当前XIP模式状态，请读取SFMSDC寄存器中的SFMXST标志。

注1.在SFMSDC寄存器的SFMXD[7:0]位中，设置符合实际串行闪存规范的模式数据。

下图显示了XIP模式设置过程的示例。

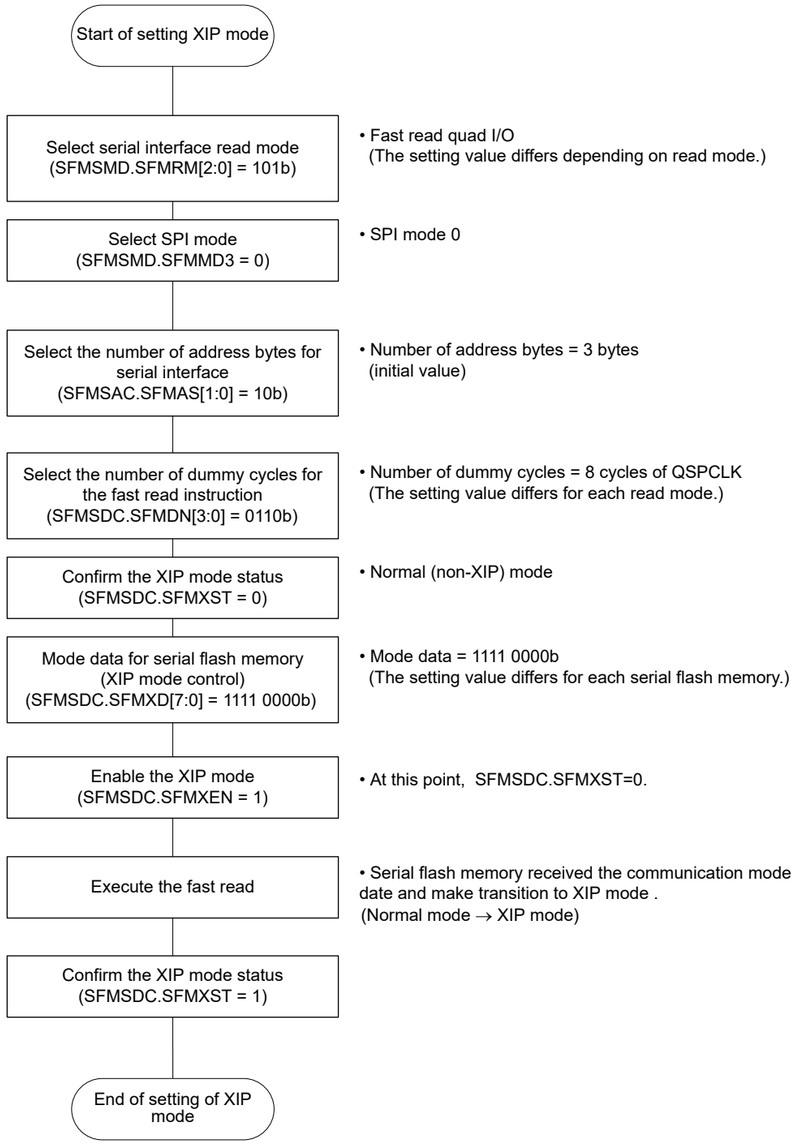

Figure 35.36 Flowchart of XIP Mode

35.8.2 Releasing the XIP Mode

To release XIP mode in serial flash memory, perform the following register setting:

- Set the mode data value to disable XIP mode in SFMSDC.SFMXD [7: 0] bits*1
- Set the SFMXEN bit in the SFMSDC register to 0.

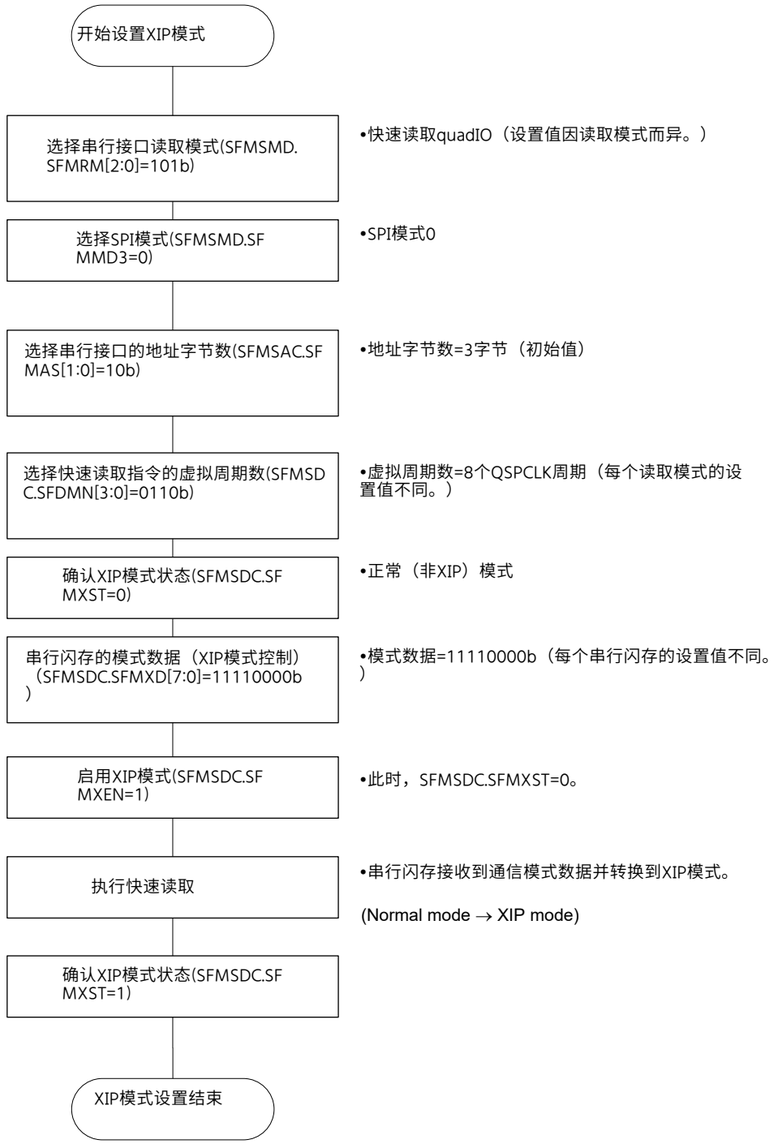

Figure 35.36 XIP模式流程图

35.8.2 释放XIP模式

要在串行闪存中释放XIP模式，请执行以下寄存器设置：

●在SFMSDC.SFMXD[7:0]位中设置模式数据值以禁用XIP模式*1

●将SFMSDC寄存器中的SFMXEN位设置为0。

In the dummy cycle of the first fast read cycle after this register is set, The mode data value that disables the XIP mode set in the register is transferred. From that point, XIP mode is disabled in the serial flash memory. To confirm the current XIP mode status, read the SFMXST flag in the SFMSDC register.

Note 1. Set the mode data in the SFMSDC.SFMXD [7: 0] bits according to the specifications of the serial flash memory.

Figure 35.37 shows an example of the procedure for releasing XIP mode.

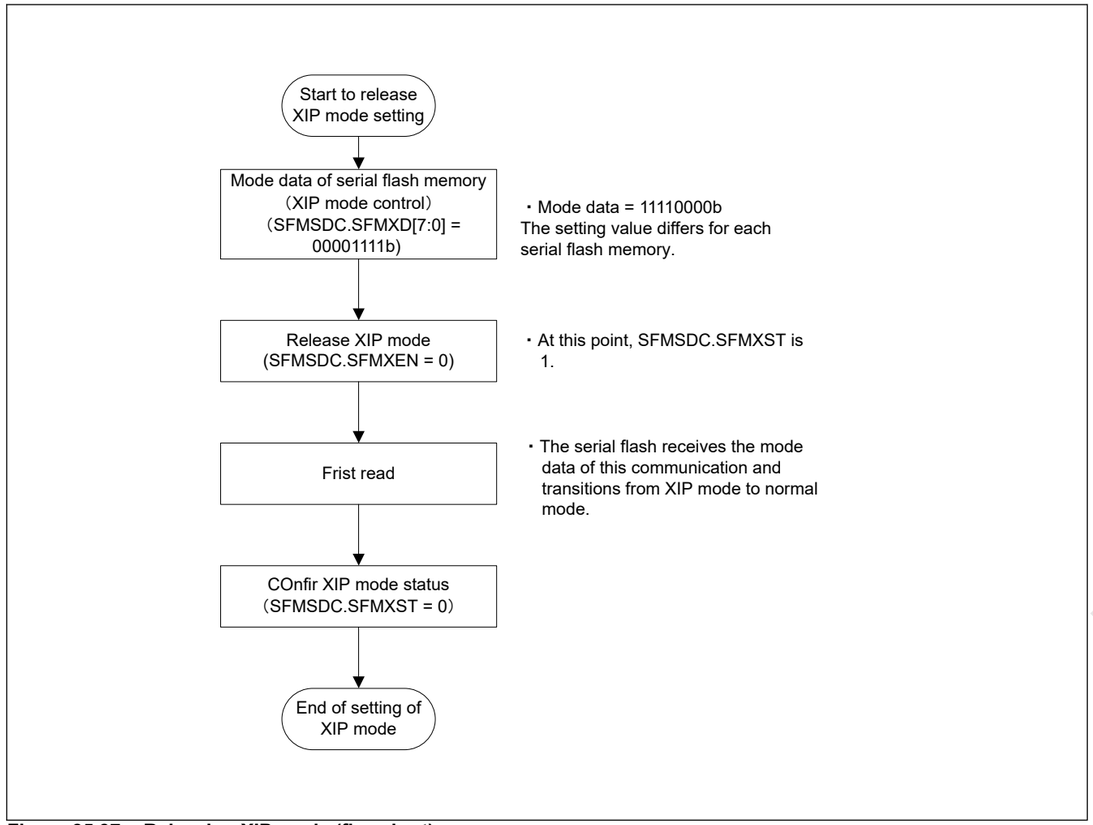

Figure 35.37 Releasing XIP mode (flowchart)

35.9 QIO2 and QIO3 Pin States

The QIO2 and QIO3 pin states depend on the serial interface read mode specified in the SFMRM[2:0] bits in the SFMSMD register.

Table 35.11 QIO2 and QIO3 pin states (1 of 2)

SFMSMD.SFMRM[2:0] bits	QIO2 pin state*1	QIO3 pin state*2	Remarks
111	Setting prohibited		
110			
101	Input or output as serial data signal (The pin is in the Hi-Z state when it is inactive.)	Input or output as serial data signal (The pin is in the Hi-Z state when it is inactive.)	Fast Read Quad I/O
100			Fast Read Quad Output

在设置该寄存器后的第一个快速读取周期的空周期中，传输寄存器中设置的禁用XIP模式的模式数据值。从那时起，串行闪存中的XIP模式被禁用。要确认当前XIP模式状态，请读取SFMSDC寄存器中的SFMXST标志。

注1.根据串行闪存的规格设置SFMSDC.SFMXD[7:0]位中的模式数据。

图35.37显示了释放XIP模式的过程示例。

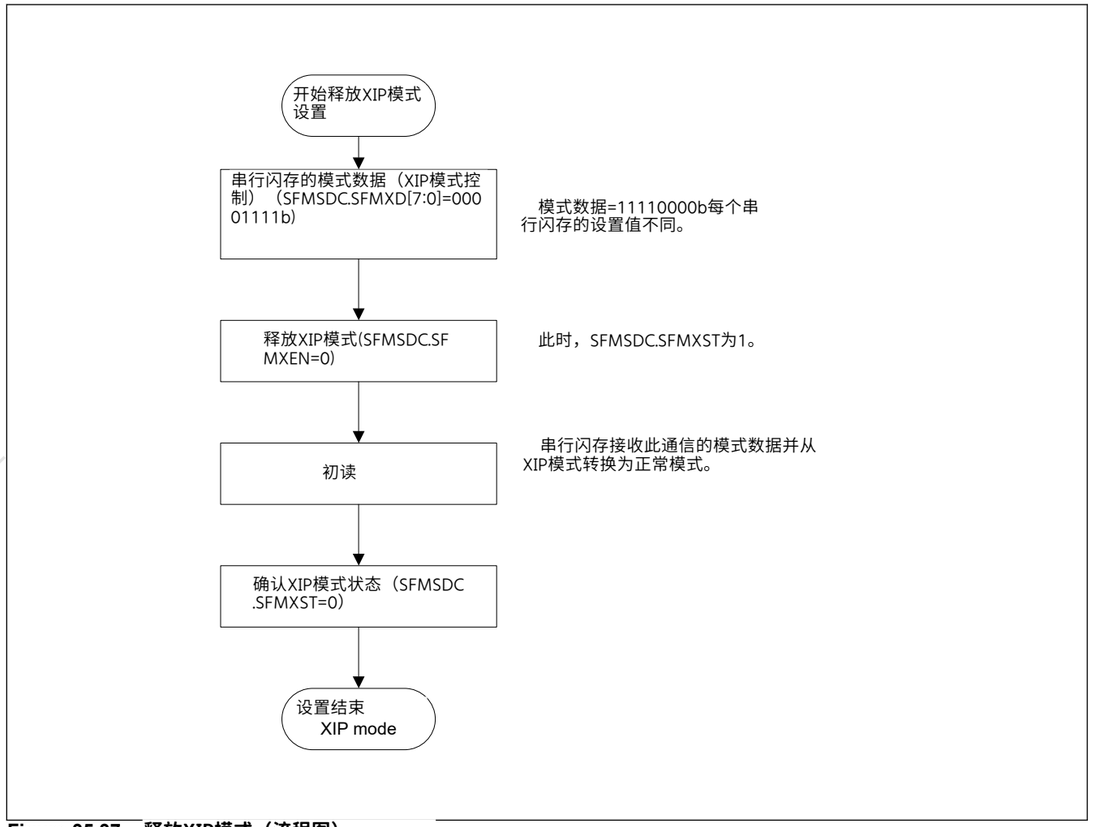

Figure 35.37 释放XIP模式（流程图）

35.9 QIO2和QIO3引脚状态

QIO2和QIO3引脚状态取决于SFMSMD寄存器的SFMRM[2:0]位中指定的串行接口读取模式。

Table 35.11 QIO2和QIO3引脚状态（1of2）

SFMSMD.SFMRM[2:0] bits	QIO2引脚状态*1	QIO3引脚状态*2	Remarks
111	禁止设定		
110			
101	作为串行数据信号的输入或输出（引脚处于非活动状态时处于Hi-Z状态。）	作为串行数据信号的输入或输出（引脚处于非活动状态时处于Hi-Z状态。）	快速读取四路IO
100			快速读取四路输出

Table 35.11 QIO2 and QIO3 pin states (2 of 2)

SFMSMD.SFMRM[2:0] bits	QIO2 pin state*1	QIO3 pin state*2	Remarks
011	Output SFMWPL bit variable of the Port Control Register (SFMPMD) (initial value is low level)	Output high level	Fast Read Dual I/O
010			Fast Read Dual Output
001			Fast Read
000			Standard Read (Initial State)

Note 1. The serial flash memory can also use the QIO2 pin for the write protect (WP) function. The WP function prohibits writes to the status registers. (The function is available in mode other than Quad-SPI mode.)
Note 2. The serial flash memory can also use the QIO3 pin for the HOLD or RESET function.
The hold function places the I/O pin in an inactive state without deselecting the chip. (The function is available in mode other than Quad-SPI mode.)
The reset function resets the serial flash memory. (The function is available when the QSSL pin function is disabled or in a mode in which the QIO3 pin is not used.)

35.10 Direct Communication Mode

35.10.1 About Direct Communication

The QSPI can read the serial flash memory contents by automatically converting from reading the QSPI window area to SPI bus cycles. However, serial flash memory have many different functions in addition to memory data read, including ID information read, erase, programming, and status information read. There is no standardized instruction set for using these functions, and more functions are being added rapidly by different vendors to different devices. Therefore, to support these functions, the software can create any required SPI bus cycle by communicating directly with serial flash memory.

35.10.2 Using Direct Communication Mode

To communicate directly with serial flash memory, transition to direct communication mode by setting the DCOM bit in the Communication Mode Control Register (SFMCMD) register to 1. While direct communications mode is selected, the read operation to the serial flash memory by the QSPI window is invalid.

Note: If the QSPI is set to the XIP mode, you must terminate the XIP mode before starting direct communication mode.

35.10.3 Generating the SPI Bus Cycle during Direct Communication

The SPI bus cycle in direct communications starts on the first access to the SFMCOM register, and after a series of input / output operations are executed via the SFMCOM register, the bus cycle ends when 1 is written to the SFMCMD register. At that point, a write to the SFMCOM port is converted to a one-byte transmission to the SPI bus, and a read from the SFMCOM register is converted to a one-byte reception from the SPI bus.

During the period from the first access to the SFMCOM register to the last write operation to the SFMCMD register, the QSSL signal is held active to notify the serial flash memory that a series of SPI bus cycles is in progress.

Note: In direct communication mode, all writes to registers other than SFMCMD and SFMCOM (including SFMSMD, SFMSSC, SFMSKC, SFMSST, SFMCST, SFMSIC, SFMSAC, SFMSDC, SFMSPC, and SFMPMD) are disabled.

Figure 35.38 to Figure 35.40 show direct communication program examples, and Figure 35.41 shows ID read direct communication timing examples.

Table 35.11 QIO2和QIO3引脚状态（2个中的2个）

SFMSMD.SFMRM[2:0] bits	QIO2引脚状态*1	QIO3引脚状态*2	Remarks
011	输出端口控制寄存器（SFMPMD）的SFMWPL位变量（初始值为低电平）	输出高电平	快速读取双IO
010			快速读取双输出
001			快速阅读
000			标准读取（初始状态）

注1.串行闪存也可以将QIO2引脚用于写保护(WP)功能。WP功能禁止写入状态寄存器。（该功能在Quad-SPI模式以外的模式下可用。）

注2.串行闪存也可以将QIO3引脚用于HOLD或RESET功能。
保持功能将IO引脚置于非活动状态，而无需取消选择芯片。（该功能在除Quad-SPI mode.)
复位功能复位串行闪存。（当QSSL引脚功能被禁用或处于未使用QIO3引脚的模式时，该功能可用。）

35.10 直接通讯方式

35.10.1 关于直接沟通

QSPI可以通过从读取QSPI窗口区域自动转换为SPI总线周期来读取串行闪存内容。然而，串行闪存除了读取存储器数据外，还有许多不同的功能，包括ID信息读取、擦除、编程和状态信息读取。使用这些功能没有标准化的指令集，更多的功能正在由不同的供应商迅速添加到不同的设备中。因此，为了支持这些功能，软件可以通过直接与串行闪存通信来创建任何所需的SPI总线周期。

35.10.2 使用直接通信模式

要直接与串行闪存通信，通过设置DCOM位转换到直接通信模式CommunicationModeControlRegister(SFMCMD)registerto1.Whiledirectcommunicationsmodeisselected thereadoperationtotheserialflashmemorybytheQSPIwindowisinvalid.

Note: 如果QSPI设置为XIP模式，则必须在启动直接通信模式之前终止XIP模式。

35.10.3 在直接通信期间生成SPI总线周期

直接通信中的SPI总线周期从第一次访问SFMCOM寄存器开始，通过SFMCOM寄存器执行一系列输入输出操作后，总线周期在SFMCMD寄存器写入1时结束。此时，对SFMCOM端口的写入转换为向SPI总线发送一个字节，从SFMCOM寄存器读取转换为从SPI总线接收一个字节。

在从第一次访问SFMCOM寄存器到最后一次写入SFMCMD寄存器期间，
QSSL信号保持有效，以通知串行闪存一系列SPI总线周期正在进行中。

Note: 在直接通信模式下，所有写入除SFMCMD和SFMCOM以外的寄存器（包括SFMSMD、SFMSSC、SFMSKC、SFMSST、SFMCST、SFMSIC、SFMSAC、SFMSDC、SFMSPC和SFMPMD）被禁用。

图35.38至图35.40为直接通信程序示例，图35.41为ID读取直接通信时序示例。

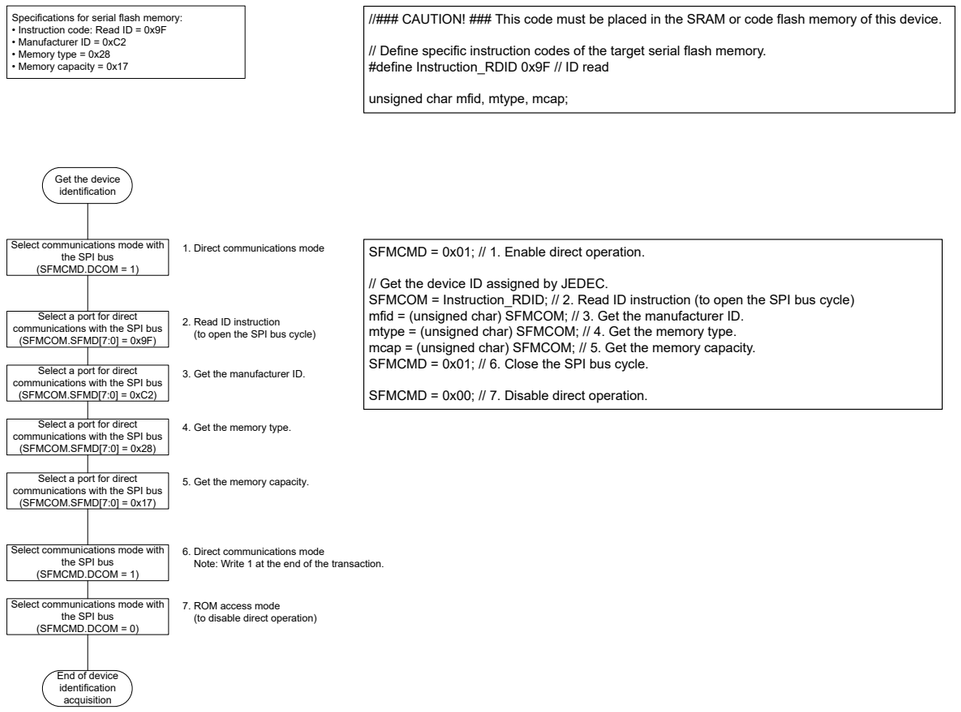

Figure 35.38 Flowchart of Device ID Acquisition

Figure 35.38 设备ID获取流程图

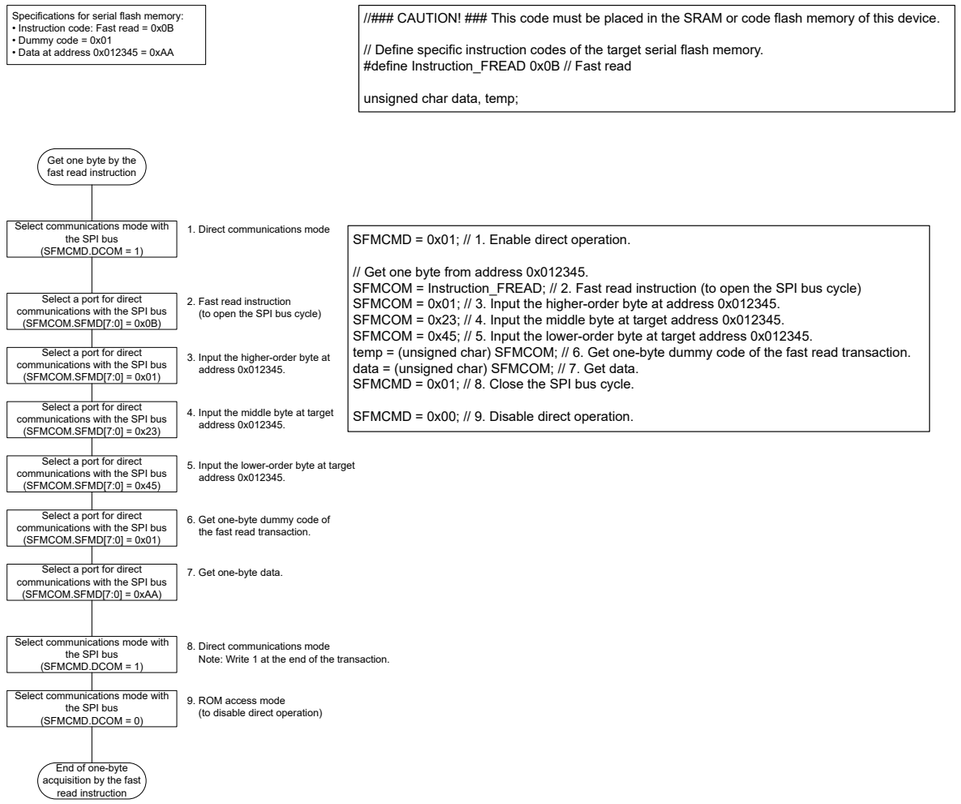

Figure 35.39 Flowchart of One-byte Acquisition by the Fast Read Instruction

Figure 35.39 快速读取指令获取一字节的流程图

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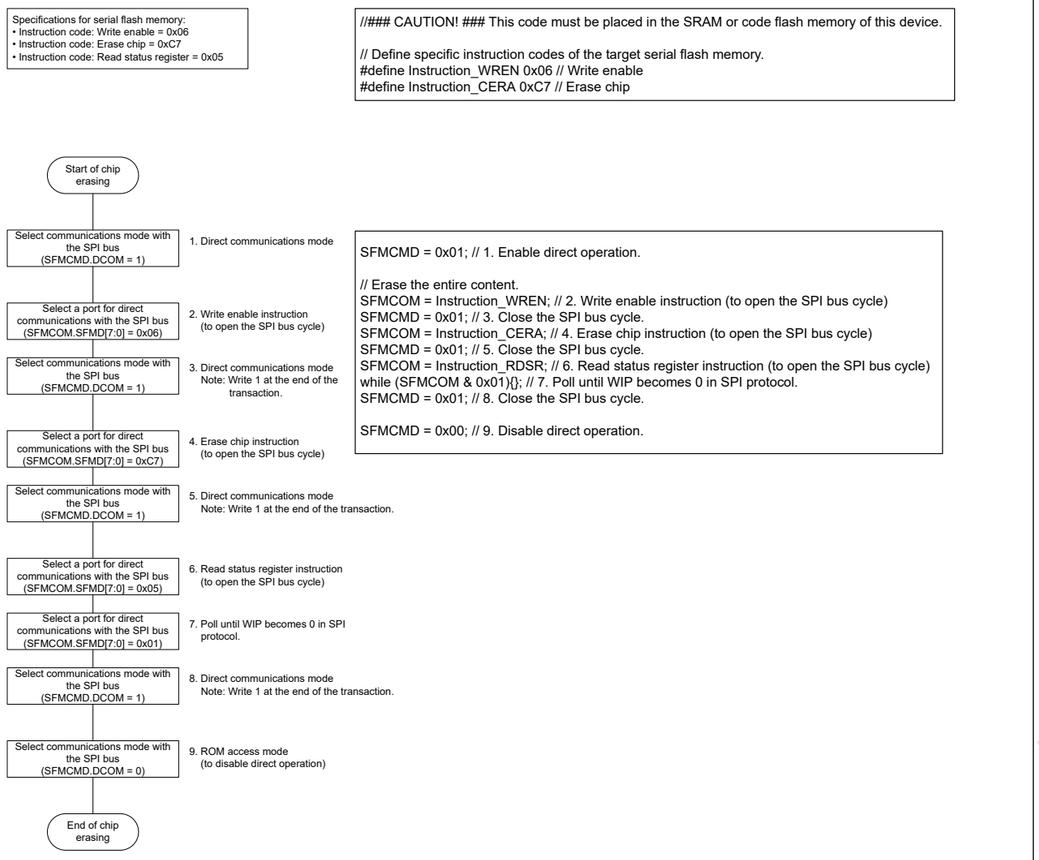


Figure 35.40 Flowchart of Chip Erasing

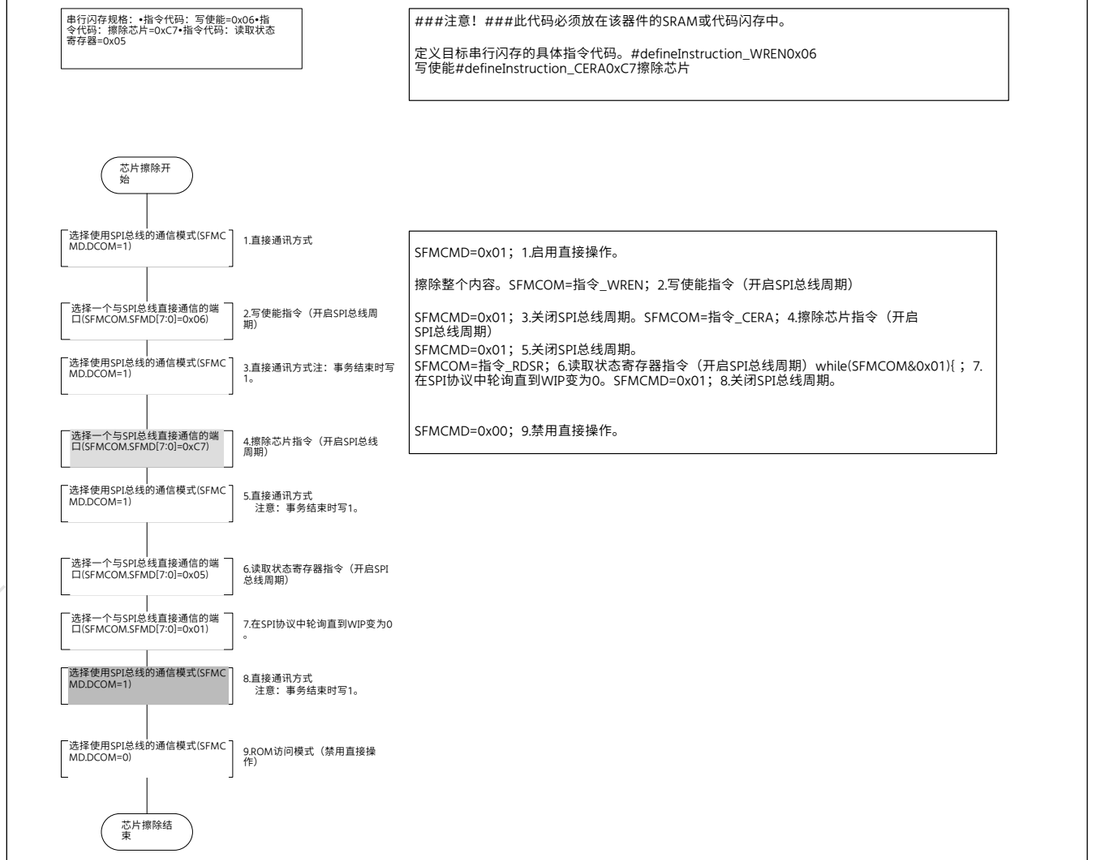
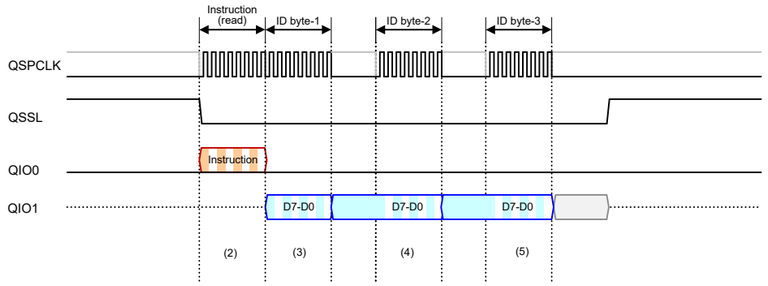


Figure 35.40 芯片擦除流程图



Note: (1) SFMCMD = 0x01; // Enable direct operation. Get the device ID assigned by JEDEC.
(2) SFMCOM = Instruction_RDID; // Read ID instruction (to open the transaction)
(3) mfid = (unsigned char) SFMCOM; // Get the manufacturer ID from ID byte 1.
(4) mtype = (unsigned char) SFMCOM; // Get the memory type from ID byte 2.
(5) mcap = (unsigned char) SFMCOM; // Get the memory capacity from ID byte 3.
(6) SFMCMD = 0x01; // Close the transaction.
(7) SFMCMD = 0x00; // Disable direct operation.

The timings (1), (6) and (7) for enabling or disabling direct communications mode are omitted in the figure.

Figure 35.41 Example of direct communication timing for ID read

Note: When the Single SPI Protocol, Extended SPI Protocol is used in direct communication mode, the standard Read or Fast Read instruction must be used to reference the contents of the serial flash memory. The QSPI does not support Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, or Fast Read Quad I/O transfers in this configuration. When these Fast Read operations are required, use ROM access memory.

35.11 Interrupts

When ROM read access is detected in direct communication mode, the SFMCST.EROMR flag is set to 1 and QSPI generates an interrupt request. Interrupt requests are retained until the EROMR flag is cleared by a 0 write. For details, see section 13, Interrupt Controller Unit (ICU).

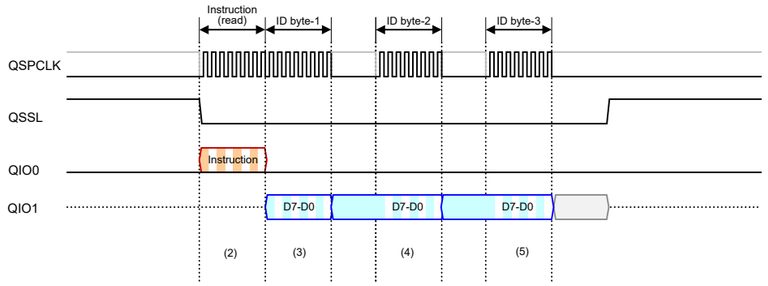
35.12 Usage Note

35.12.1 Settings for the Module-Stop Function

QSPI operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The QSPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

35.12.2 Procedure for Changing Settings in Multiple Control Registers

The settings of the QSPI control registers can be modified dynamically during system operation. However, when the settings of multiple control registers are changed sequentially, an SPI bus cycle might occur before all of the registers are updated. The register setting sequence must be designed so that the SPI bus timing specifications are satisfied at all stages of register setting modification.



Note: (1)SFMCMD=0x01；启用直接操作。获取JEDEC分配的设备ID。(2)SFMCOM=指令_RDID；读取ID指令（开启交易）(3)mfid=(unsignedchar)SFMCOM;从ID字节1获取制造商ID。(4)mtype=(unsignedchar)SFMCOM;从ID字节2获取内存类型。(5)mcap=(unsignedchar)SFMCOM;从ID字节3获取内存容量。(6)SFMCMD=0x01;关闭交易。(7)SFMCMD=0x00；禁用直接操作。

图中省略了启用或禁用直接通信模式的时序(1)、(6)和(7)。

Figure 35.41 ID读取的直接通信时序示例

Note: 当单SPI协议、扩展SPI协议用于直接通信模式时，标准的Read或必须使用快速读取指令来引用串行闪存的内容。QSPI不支持此配置中的快速读取双输出、快速读取双IO、快速读取四输出或快速读取四IO传输。当需要这些快速读取操作时，请使用ROM存取存储器。

35.11 Interrupts

当在直接通信模式下检测到ROM读访问时，SFMCST.EROMR标志设置为1，并且QSPI产生中断请求。中断请求被保留，直到EROMR标志被0写入清除。有关详细信息，请参阅第13节，中断控制器单元(ICU)。

35.12 使用说明

35.12.1 模块停止功能的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用QSPI操作。QSPI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

35.12.2 更改多个控制寄存器中的设置的步骤

QSPI控制寄存器的设置可以在系统运行期间动态修改。但是，当多个控制寄存器的设置依次更改时，可能会在所有寄存器更新之前发生一个SPI总线周期。必须设计寄存器设置序列，以便在寄存器设置修改的所有阶段都满足SPI总线时序规范。

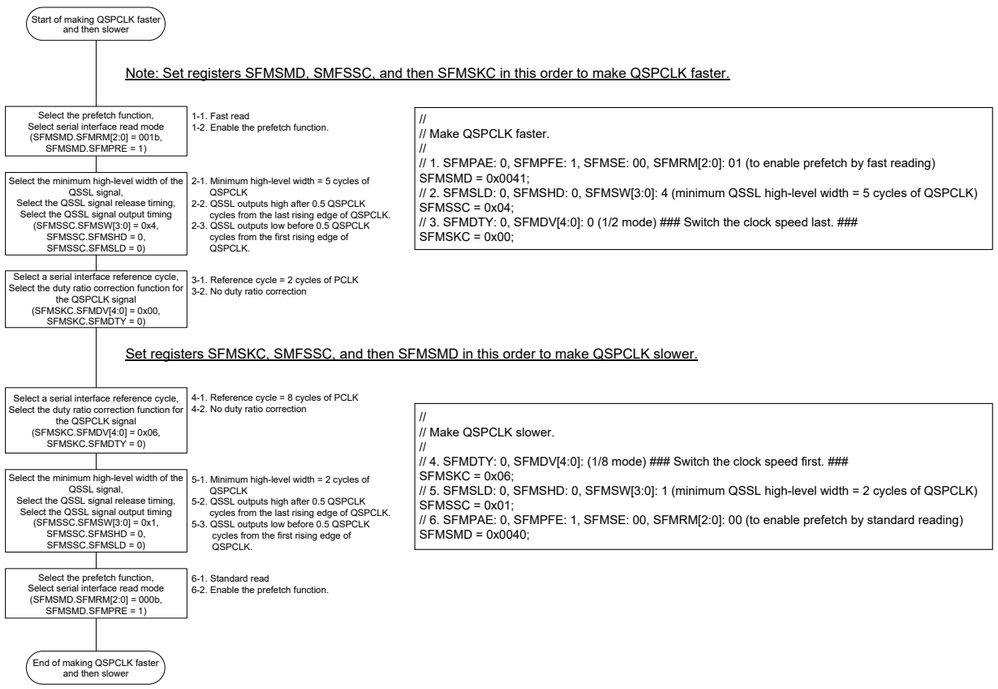


Figure 35.42 Flowchart of Making QSPCLK Faster and Slower

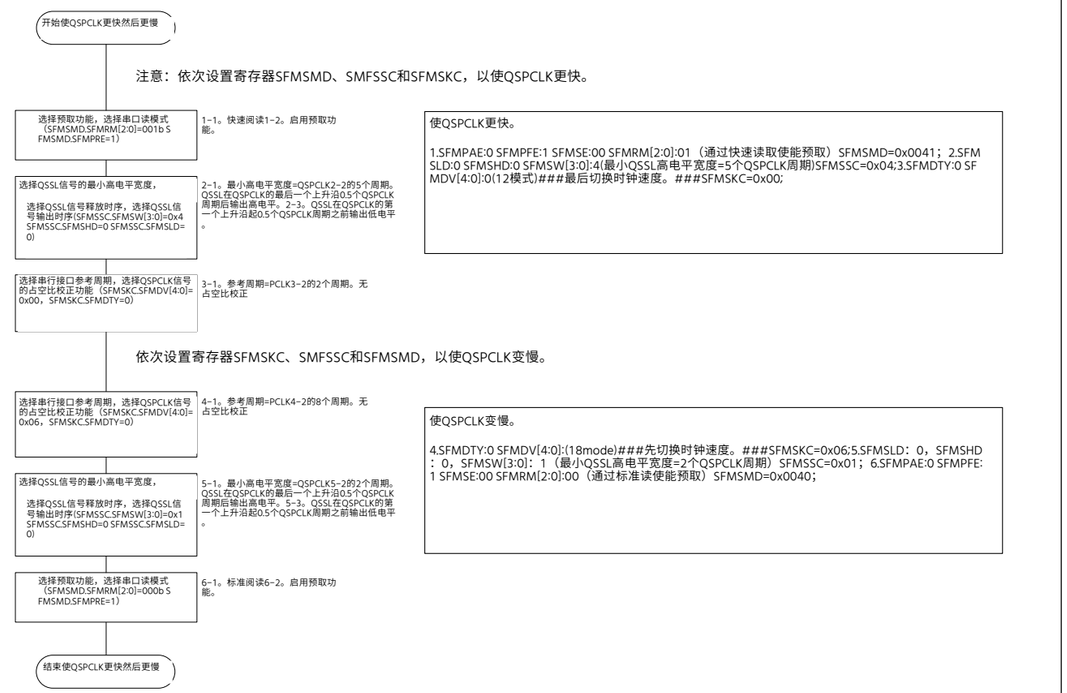


Figure 35.42 使QSPCLK更快和更慢的流程图

36. Octa Serial Peripheral Interface (OSPI)

The Octa Serial Peripheral Interface (OSPI) module is a memory controller for connecting OctaFlash™ and OctaRAM™.

The OSPI is compliant with JEDEC standard JESD251, Profile 1.0.

Note: OctaFlash™ and OctaRAM™ are trademarks of Macronix International Co., Ltd.

36.1 Overview

36.1.1 Features

- Macronix Serial Multi I/O (MXSMIO®) Octa Peripheral Interface (OPI) for high-end consumer applications is supported.
- Flash device compliant with JEDEC standard JESD251, Profile 1.0 is supported.
- One each of an OctaFlash device and an OctaRAM device compliant with the OPI specifications are connectable.
- A chip select signal is assigned to each memory device (OM_CS0: OctaRAM; OM_CS1: OctaFlash).*1
- Supported device interfaces
  - SPI: Serial peripheral interface (OctaFlash, SPI mode)
  - SOPI: Single Octa I/O (8 bits) (OctaFlash, single data rate)
  - DOPI: Double Octa I/O (8 bits) (OctaFlash and OctaRAM, double data rate)
- 3-byte and 4-byte OctaFlash address commands are supported.
- 4-byte OctaRAM address commands are supported.
- The read-while-write (RWW) operation is supported.
- 1LC and 2LC (latency count) OctaRAM devices are supported.
- The error corrected signal (ECS) is available, and ECC errors can be detected (for OctaFlash only).
- Interrupt source: Error interrupts.
- Fastboot mode is not supported.
- Direct access (memory-mapped reading and writing) to memory devices in separate flash and RAM address spaces is supported.

Note 1. Only one of the memory devices can operate (be read or written to) at a time.

36. Octa串行外设接口(OSPI)

Octa串行外设接口(OSPI)模块是用于连接OctaFlash 和OctaRAM 的内存控制器。

OSPI符合JEDEC标准JESD251，Profile1.0。

Note: OctaFlash 和OctaRAM 是MacronixInternationalCo. Ltd.的商标。

36.1 Overview

36.1.1 Features

●支持用于高端消费应用的Macronix串行多IO(MXSMIO®)八角外设接口(OPI)。

●闪存器件符合JEDEC标准JESD251，支持Profile1.0。

●可连接符合OPI规格的OctaFlash设备和OctaRAM设备各一个。

●为每个存储设备分配一个片选信号（OM_CS0：OctaRAM；OM_CS1：OctaFlash）。*1

●支持的设备接口

SPI：串行外设接口（OctaFlash，SPI模式）

SOPI：单OctaIO（8位）（OctaFlash，单数据速率）

DOPI：双OctaIO（8位）（OctaFlash和OctaRAM，双倍数据速率）

●支持3字节和4字节OctaFlash地址命令。

●支持4字节OctaRAM地址命令。

●支持边写边读（RWW）操作。

●支持1LC和2LC（延迟计数）OctaRAM设备。

●纠错信号（ECS）可用，可检测ECC 错误（仅适用于OctaFlash）。

●中断源：错误中断。

●不支持快速启动模式。

●支持在单独的闪存和RAM地址空间中直接访问（内存映射读取和写入）存储设备。

注1.一次只能操作（读取或写入）其中一个存储设备。

36.1.2 Block diagram

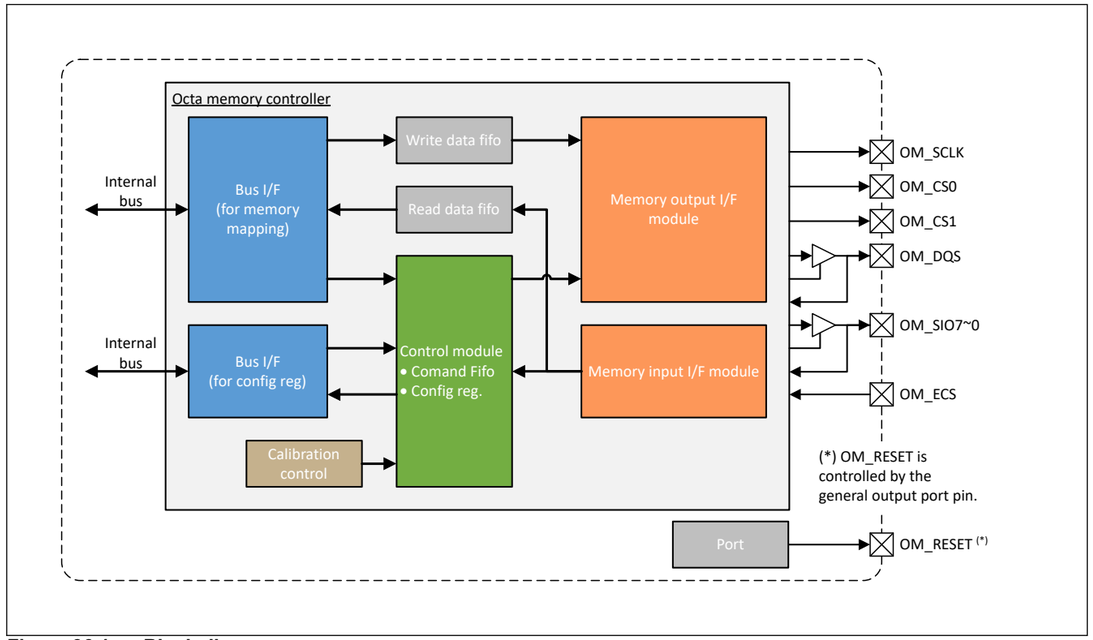


Figure 36.1 Block diagram

36.1.3 Input/Output Pins

Table 36.1 shows the pin configuration to connect chip pins.

Table 36.1 Configuration of Memory Controller Pins to connect Chip pins

Pin name	I/O	Function
OM_SCLK	Output	Clock output (OCTACLK divided by 2)
OM_CS0	Output	Chip select signal for an OctaRAM device
OM_CS1	Output	Chip select signal for an OctaFlash device
OM_DQS	I/O	Read data strobe/write data mask signal
OM_SIO7 to OM_SIO0	I/O	Data input/output
OM_RESET	Output	Reset signal for both OctaFlash and OctaRAM devices
OM_ECS	Input	ECC error detection signal from the external memory

36.1.4 Device Interface

The device interface is compatible with OctaFlash/OctaRAM interface.

When reading data from memory or programming data to memory, the bit order is changed in accordance with the I/O mode. The bit order is shown below:

Table 36.2 Bit order in accordance with I/O mode (1 of 2)

I/O mode	Bit order (MSB)
Read data from device	
1 I/O (SPI)	OM_SIO1 input
8 I/O (SOPI)	OM_SIO7 to OM_SIO0 input

36.1.2 框图

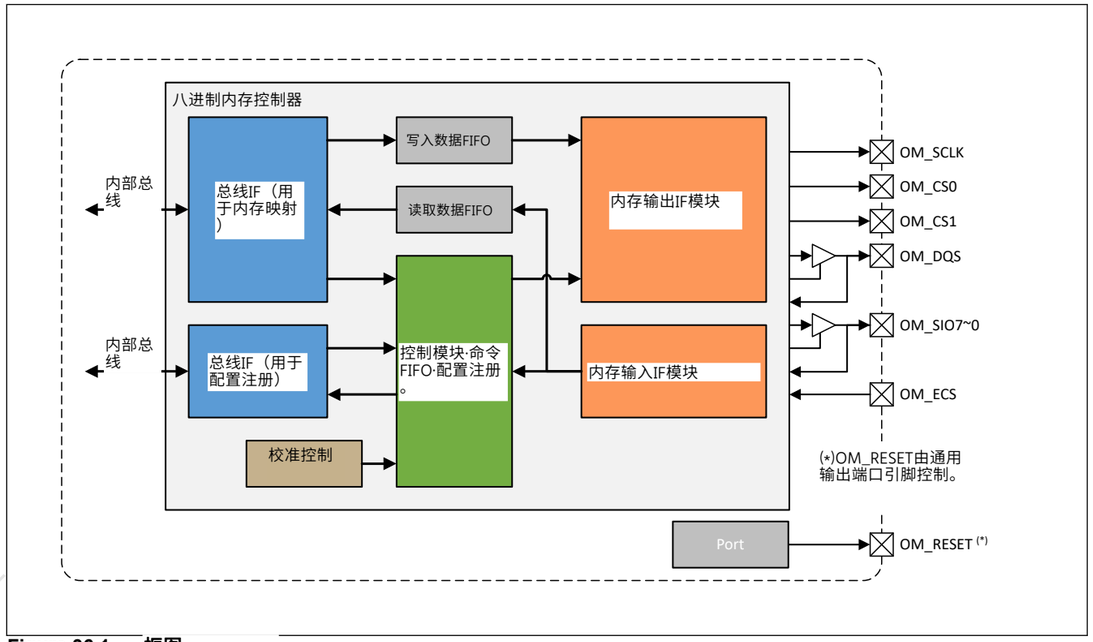


Figure 36.1 框图

36.1.3 Input/Output Pins

表36.1显示了连接芯片引脚的引脚配置。

Table 36.1 内存控制器引脚配置以连接芯片引脚

引脚名称	I/O	Function
OM_SCLK	Output	时钟输出（OCTACLK除以2）
OM_CS0	Output	OctaRAM器件的片选信号
OM_CS1	Output	OctaFlash器件的片选信号
OM_DQS	I/O	读数据选通写数据屏蔽信号
OM_SIO7 to OM_SIO0	I/O	Data input/output
OM_RESET	Output	OctaFlash和OctaRAM器件的复位信号
OM_ECS	Input	来自外部存储器的ECC错误检测信号

36.1.4 设备接口

设备接口与OctaFlashOctaRAM接口兼容。

当从内存读取数据或将数据编程到内存时，位顺序会根据IO模式而改变。位顺序如下所示：

Table 36.2 符合IO模式的位顺序(1of2)

I/O mode	位序(MSB)
从设备读取数据	
1 I/O (SPI)	OM_SIO1 input
8 I/O (SOPI)	OM_SIO7至OM_SIO0输入

Table 36.2 Bit order in accordance with I/O mode (2 of 2)

I/O mode	Bit order (MSB)
8 I/O (DOPI)	OM_SIO7 to OM_SIO0 input. Order of data {D1, D0}, {D3, D2}, … or {D0, D1}, {D2, D3}, …, according to setting for memory to be connected.
Program/Write data to device	
1 I/O (SPI)	OM_SIO0 output
8 I/O (SOPI)	OM_SIO7 to OM_SIO0 output
8 I/O (DOPI)	OM_SIO7 to OM_SIO0 output. Order of data {D1, D0}, {D3, D2}, …or {D0, D1}, {D2, D3}, …, according to setting for memory to be connected.

36.2 Register Descriptions

Table 36.3 shows the register configuration.

There are memory-map and configuration modes for accessing the OctaFlash/RAM memory.

In the memory-map mode, the OSPI automatically sends the command for read or write. In the configuration mode, the controller sends commands and data.

Table 36.3 OSPI register configuration

Register Name	Symbol	R/W	Initial Value	Address	Access Size
Device command register	DCR	R/W	0x00000000	0x400A_6000	32
Device address register	DAR	R/W	0x00000000	0x400A_6004	32
Device command setting register	DCSR	R/W	0x00000000	0x400A_6008	32
Device size register 0	DSR0	R/W	0x00000000	0x400A_600C	32
Device size register 1	DSR1	R/W	0x00000000	0x400A_6010	32
Memory delay trim register	MDTR	R/W	0x06009400	0x400A_6014	32
Auto-calibration timer register	ACTR	R/W	0x10000000	0x400A_6018	32
Auto-Calibration Address Register 0	ACAR0	R/W	0x00000000	0x400A_601C	32
Auto-Calibration Address Register 1	ACAR1	R/W	0x00000000	0x400A_6020	32
Device Memory Map Read chip select timing setting register	DRCSTR	R/W	0x00000000	0x400A_6034	32
Device Memory Map Write chip select timing setting register	DWCSTR	R/W	0x00000000	0x400A_6038	32
Device chip select timing setting register	DCSTR	R/W	0x00000000	0x400A_603C	32
Controller and device setting register	CDSR	R/W	0x00000000	0x400A_6040	32
Memory Map dummy length register	MDLR	R/W	0x00000000	0x400A_6044	32
Memory Map read/write command register 0	MRWCR0	R/W	0x00000000	0x400A_6048	32
Memory Map read/write command register 1	MRWCR1	R/W	0x00000000	0x400A_604C	32
Memory Map read/write setting register	MRWCSR	R/W	0x00000000	0x400A_6050	32
Error status register	ESR	R/W	0x00000000	0x400A_6054	32
Configure Write without Data Register	CWNDR	W	0x00000000	0x400A_6058	32
Configure Write Data Register	CWDR	W	0x00000000	0x400A_605C	32
Configure Read Register	CRR	R	0x00000000	0x400A_6060	32
Auto-calibration status register	ACSR	R/W	0x00000000	0x400A_6064	32
Device chip select maximum period register	DCSMXR	R/W	0x00000000	0x400A_607C	32
Device Memory Map Write single continuous translating size Register	DWSCTSR	R/W	0x00000000	0x400A_6080	32

Table 36.2 符合IO模式的位顺序(2of2)

I/O mode	位序(MSB)
8 I/O (DOPI)	OM_SIO7到OM_SIO0输入。 数据顺序为{D1 D0 {D3 D2 …或{D0 D1 {D2 D3 …，根据要连接的存储器的设置。
程序写入数据到设备	
1 I/O (SPI)	OM_SIO0 output
8 I/O (SOPI)	OM_SIO7至OM_SIO0输出
8 I/O (DOPI)	OM_SIO7到OM_SIO0输出。 数据顺序为{D1 D0 {D3 D2 …或{D0 D1 {D2 D3 …，根据要连接的内存的设置。

36.2 注册说明

表36.3显示了寄存器配置。

有用于访问OctaFlashRAM存储器的存储器映射和配置模式。

在内存映射模式下，OSPI自动发送读取或写入命令。在配置模式下，控制器发送命令和数据。

Table 36.3 OSPI寄存器配置

注册名称	Symbol	R/W	初始值	Address	访问大小
设备命令寄存器	DCR	R/W	0x00000000	0x400A_6000	32
设备地址寄存器	DAR	R/W	0x00000000	0x400A_6004	32
设备命令设置寄存器	DCSR	R/W	0x00000000	0x400A_6008	32
设备大小寄存器0	DSR0	R/W	0x00000000	0x400A_600C	32
设备大小寄存器1	DSR1	R/W	0x00000000	0x400A_6010	32
内存延迟调整寄存器	MDTR	R/W	0x06009400	0x400A_6014	32
自动校准定时器寄存器	ACTR	R/W	0x10000000	0x400A_6018	32
自动校准地址寄存器0	ACAR0	R/W	0x00000000	0x400A_601C	32
自动校准地址寄存器1	ACAR1	R/W	0x00000000	0x400A_6020	32
DeviceMemoryMap读取片选时序设置寄存器	DRCSTR	R/W	0x00000000	0x400A_6034	32
DeviceMemoryMap写片选时序设置寄存器	DWCSTR	R/W	0x00000000	0x400A_6038	32
设备片选时序设置寄存器	DCSTR	R/W	0x00000000	0x400A_603C	32
控制器和设备设置寄存器	CDSR	R/W	0x00000000	0x400A_6040	32
内存映射虚拟长度寄存器	MDLR	R/W	0x00000000	0x400A_6044	32
内存映射读写命令寄存器0	MRWCR0	R/W	0x00000000	0x400A_6048	32
内存映射读写命令寄存器1	MRWCR1	R/W	0x00000000	0x400A_604C	32
内存映射读写设置寄存器	MRWCSR	R/W	0x00000000	0x400A_6050	32
错误状态寄存器	ESR	R/W	0x00000000	0x400A_6054	32
配置无数据寄存器写入	CWNDR	W	0x00000000	0x400A_6058	32
配置写数据寄存器	CWDR	W	0x00000000	0x400A_605C	32
配置读取寄存器	CRR	R	0x00000000	0x400A_6060	32
自动校准状态寄存器	ACSR	R/W	0x00000000	0x400A_6064	32
设备片选最大周期寄存器	DCSMXR	R/W	0x00000000	0x400A_607C	32
设备内存映射写入单个连续翻译大小寄存器	DWSCTSR	R/W	0x00000000	0x400A_6080	32

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36.2.1 DCR : Device Command Register

Base address: OSPI = 0x400A_6000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DVCMD1[7:0]								DVCMD0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DVCMD0[7:0]	Device Command data Sets the data to be transferred as a command to the device. If DCSR.CMDLEN[2:0] = 1, the controller will send DCR[7:0] as the 1st byte to memory. If DCSR.CMDLEN[2:0] = 2, the controller will send DCR[7:0] as the 2nd byte to memory.	R/W
15:8	DVCMD1[7:0]	Device Command data Sets the data to be transferred as a command to the device. If DCSR.CMDLEN[2:0] = 2, the controller will send DCR[15:8] as the 1st byte to memory	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

DCR sets the device commands for controller operation.

36.2.2 DAR : Device Address Register

Base address: OSPI = 0x400A_6000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVAD3[7:0]								DVAD2[7:0]								DVAD1[7:0]								DVAD0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DVAD0[7:0]	Device Address data 0 Set the device address data. When DCSR.ADLEN[2:0] = 3, set as the third byte. When DCSR.ADLEN[2:0] = 4, set as the fourth byte.	R/W
15:8	DVAD1[7:0]	Device Address data 1 Set the device address data. When DCSR.ADLEN[2:0] = 3, set as the second byte. When DCSR.ADLEN[2:0] = 4, set as the third byte.	R/W
23:16	DVAD2[7:0]	Device Address data 2 Set the device address data. When DCSR.ADLEN[2:0] = 3, set as the first byte. When DCSR.ADLEN[2:0] = 4, set as the second byte.	R/W
31:24	DVAD3[7:0]	Device Address data 3 Set the device address data. When DCSR.ADLEN[2:0] = 4 only, set as the first byte.	R/W

DAR sets the device address for controller operation.

36.2.1 DCR:设备命令寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DVCMD1[7:0]								DVCMD0[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DVCMD0[7:0]	设备命令数据 设置要作为命令传输到设备的数据。 如果DCSR.CMDLEN[2:0]=1，控制器会将DCR[7:0]作为第一个字节发送到内存。如果DCSR.CMDLEN[2:0]=2，控制器会将DCR[7:0]作为第2个字节发送到内存。	R/W
15:8	DVCMD1[7:0]	设备命令数据 设置要作为命令传输到设备的数据。 如果DCSR.CMDLEN[2:0]=2，控制器会将DCR[15:8]作为第一个字节发送到内存	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

DCR为控制器操作设置设备命令。

36.2.2 DAR:设备地址寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVAD3[7:0]								DVAD2[7:0]								DVAD1[7:0]								DVAD0[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DVAD0[7:0]	设备地址数据0 设置设备地址数据。 当DCSR.ADLEN[2:0]=3时，设置为第三个字节。当DCSR.ADLEN[2:0]=4时，设置为第四个字节。	R/W
15:8	DVAD1[7:0]	设备地址数据1 设置设备地址数据。 当DCSR.ADLEN[2:0]=3时，设置为第二个字节。 当DCSR.ADLEN[2:0]=4时，设置为第三个字节。	R/W
23:16	DVAD2[7:0]	设备地址数据2 设置设备地址数据。 当DCSR.ADLEN[2:0]=3时，设置为第一个字节。 当DCSR.ADLEN[2:0]=4时，设置为第二个字节。	R/W
31:24	DVAD3[7:0]	设备地址数据3 设置设备地址数据。 仅当DCSR.ADLEN[2:0]=4时，设置为第一个字节。	R/W

DAR设置控制器操作的设备地址。

36.2.3 DCSR : Device Command Setting Register

Base address: OSPI = 0x400A_6000

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	PREN	ACDA	DOPI	ADLEN[2:0]			DAOR	CMDLEN[2:0]			ACDV	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMLEN[7:0]								DALEN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DALEN[7:0]	Transfer data length setting Sets the length of data to be transferred in bytes. Set a value less than 0x5. When [7:0] is 0, there are no transmission data to memory and reception data from memory.	R/W
15:8	DMLEN[7:0]	Dummy cycle setting Sets the length of dummy cycle in OM_SCLK units.	R/W
18:16	—	These bits are read as 0. The write value should be 0.	R
19	ACDV	Access Device setting Sets the device to be accessed. 0: Send commands to device 0. 1: Send commands to device 1.	R/W
22:20	CMDLEN[2:0]	Transfer command length setting Sets the length of the command to be transferred in bytes.	R/W
23	DAOR	Data order setting Sets the byte order of data during read and write operations. 0: byte0, byte1, byte2, byte3 1: byte1, byte0, byte3, byte2	R/W
26:24	ADLEN[2:0]	Transfer address length setting Sets the length of the address to be transferred in bytes.	R/W
27	DOPI	DOPI single byte setting Sets the amount of data transfer per one clock cycle in DOPI mode. 0: Each cycle has two bytes data. (normal DOPI mode) 1: Each cycle has one byte data. (The byte data changes at the rising edge of the clock and does not change at the falling edge of the clock.)	R/W
28	ACDA	Data Access Control Set data access or register access 1. the address bit0 will be forced to 0 in DOPI mode. 2. If DAR[0] of the lead type command is 1, byte 0 from the device will be dropped in DOPI mode. 3. The AXI read data will be arranged according to the DAR. For example: When DAR[1:0] = 1, the first valid data is stored in RDATA[15:8]. 4. The AXI write data is used according to the DAR in DOPI mode. For example: If the target device is Flash Memory and DAR[1:0] = 1, the first byte sent to the flash memory is forced to 0xff. If the target device is RAM and DAR[1: 0] = 1, the first byte sent to RAM is masked by DQSM. 5. When the target device is RAM, the address sent to the memory changes according to RAM specification. 0: Register access Do not arrange the transfer data. 1: Data access	R/W
29	PREN	Preamble bit enable for OctaRAM 0: No check preamble bit from OctaRAM 1: Check preamble bit from OctaRAM	R/W

36.2.3 DCSR：设备命令设置寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	PREN	ACDA	DOPI	ADLEN[2:0]			DAOR	CMDLEN[2:0]			ACDV	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DMLEN[7:0]								DALEN[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DALEN[7:0]	传输数据长度设置 以字节为单位设置要传输的数据长度。 设置一个小于0x5的值。 当[7:0]为0时，没有向内存发送数据和从内存接收数据。	R/W
15:8	DMLEN[7:0]	虚拟循环设置 以OM_SCLK为单位设置虚拟周期的长度。	R/W
18:16	—	这些位被读取为0。写入值应为0。	R
19	ACDV	访问设备设置 设置要访问的设备。 0：向设备0发送命令。1：向设备1发送命令。	R/W
22:20	CMDLEN[2:0]	传送指令长度设定 设置要传输的命令的长度（以字节为单位）。	R/W
23	DAOR	数据顺序设置 在读取和写入操作期间设置数据的字节顺序。 0: byte0, byte1, byte2, byte3 1: byte1, byte0, byte3, byte2	R/W
26:24	ADLEN[2:0]	传输地址长度设置 设置要传输的地址的长度（以字节为单位）。	R/W
27	DOPI	DOPI单字节设置 设置DOPI模式下每个时钟周期的数据传输量。 0：每个周期有两个字节数据。（正常DOPI模式）1：每个周期有一个字节数据。（字节数据在时钟的上升沿变化，在时钟的下降沿不变。）	R/W
28	ACDA	数据访问控制 设置数据访问或寄存器访问1.在DOPI模式下地址bit0将被强制为0。2.如果导联类型命令的DAR[0]为1，则来自设备的字节0将在DOPI模式下被丢弃。3.AXI读取的数据会根据DAR进行排列。 例如：当DAR[1:0]=1时，第一个有效数据存储在RDATA[15:8]中。4、AXI写入数据根据DOPI模式下的DAR使用。 例如：如果目标设备是FlashMemory并且DAR[1:0]=1，则发送到flash存储器的第一个字节被强制为0xff。如果目标设备是RAM并且DAR[1:0]=1，则发送到RAM的第一个字节被DQSM屏蔽。5.当目标设备为RAM时，发送到内存的地址会根据RAM规范而变化。 0：注册访问 不要安排传输数据。 1：数据访问	R/W
29	PREN	OctaRAM的前导位启用 0：没有来自OctaRAM的检查前导位1：检查来自OctaRAM的前导位	R/W

Bit	Symbol	Function	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R

DCSR sets device commands.

36.2.4 DSR0 : Device Size Register 0

Base address: OSPI = 0x400A_6000

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DV0TYP[1:0]		DV0SZ[29:16]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DV0SZ[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
29:0	DV0SZ[29:0]	Device 0 size setting Set a 30-bit value for the size of memory connected as device 0. Examples: 0x08000000: 128-Mbyte memory 0x01000000: 16-Mbyte memory 0x00800000: 8-Mbyte memory	R/W
31:30	DV0TYP[1:0]	Device 0 type setting 0 0: flash on device 0 0 1: RAM on device 0 1 0: no connection on device 0 1 1: forbidden	R/W

DSR0 specifies the type of memory to be accessed as device 0 and the size of the RAM.

36.2.5 DSR1 : Device Size Register 1

Base address: OSPI = 0x400A_6000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DV1TYP[1:0]		DV1SZ[29:16]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DV1SZ[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
29:0	DV1SZ[29:0]	Device 1 size setting Set a 30-bit value for the size of memory connected as device 1. Examples: 0x10000000: 256-Mbyte memory 0x08000000: 128-Mbyte memory 0x01000000: 16-Mbyte memory 0x00800000: 8-Mbyte memory	R/W

Bit	Symbol	Function	R/W
31:30	—	这些位被读取为0。写入值应为0。	R

DCSR设置设备命令。

36.2.4 DSR0：设备大小寄存器0

Base address: OSPI = 0x400A_6000

Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DV0TYP[1:0]		DV0SZ[29:16]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DV0SZ[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
29:0	DV0SZ[29:0]	设备0大小设置 为设备0连接的内存大小设置30位值。 Examples: 0x08000000: 128-Mbyte memory 0x01000000: 16-Mbyte memory 0x00800000: 8-Mbyte memory	R/W
31:30	DV0TYP[1:0]	设备0类型设置 00：设备0上的闪存01：设备0上的RAM10：设备上无连接01 1：禁止	R/W

DSR0指定要访问的内存类型为设备0和RAM的大小。

36.2.5 DSR1：设备大小寄存器1

Base address: OSPI = 0x400A_6000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DV1TYP[1:0]		DV1SZ[29:16]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DV1SZ[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
29:0	DV1SZ[29:0]	设备1尺寸设置 设置作为设备1连接的内存大小的30位值。 Examples: 0x10000000: 256-Mbyte memory 0x08000000: 128-Mbyte memory 0x01000000: 16-Mbyte memory 0x00800000: 8-Mbyte memory	R/W

RA生态工作室

Bit	Symbol	Function	R/W
31:30	DV1TYP[1:0]	Device 1 type setting 0 0: flash on device 1 0 1: RAM on device 1 1 0: no connection on device 1 1 1: forbidden	R/W

DSR1 specifies the type of memory to be accessed as device 1 and the size of the flash memory.

36.2.6 MDTR : Memory Delay Trim Register

Base address: OSPI = 0x400A_6000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	DQSEDOPI[3:0]				DV1DEL[7:0]							
Value after reset:	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DQSESOPI[3:0]				DQSERAM[3:0]				DV0DEL[7:0]							
Value after reset:	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DV0DEL[7:0]	Device 0 delay setting These bits specify the delay cycles to be inserted on the input strobe signal (OM_DQS) to adjust the timing for latching data during read access to device 0 in the SOPI or DOPI mode.	R/W
11:8	DQSERAM[3:0]	OM_DQS enable counter Setting for DOPI mode [RAM].	R/W
15:12	DQSESOPI[3:0]	OM_DQS enable counter Setting for SOPI mode [Flash].	R/W
23:16	DV1DEL[7:0]	Device 1 delay setting These bits specify the delay cycles to be inserted on the input strobe signal (OM_DQS) to adjust the timing for latching data during read access to device 1 in the SOPI or DOPI mode.	R/W
27:24	DQSEDOPI[3:0]	OM_DQS enable counter Setting for DOPI mode [Flash].	R/W
31:28	—	These bits are read as 0. The write value should be 0.	R/W

MDTR sets the timing adjustment of memory access.

For the information about the auto-calibration, see section 36.3. Operation.

During a read operation with the OM_DQS clock input (in the SOPI or DOPI mode), the OM_DQS clock transitions from the high-impedance state to the input state (for receiving a value of 0 from the external device) after the command and address phases are completed. To obtain valid data, adjust the DQS enable counter and delay cycles.

OM_DQS enable counter setting (OM_SCLK units)

0000: 1 clock cycle

0001: 2 clock cycles

0010: 3 clock cycles

0011: 4 clock cycles

⋮

1111: 16 clock cycles

OM_DQS enable counter setting examples

Bit	Symbol	Function	R/W
31:30	DV1TYP[1:0]	设备1类型设置 00：设备1上的闪存01：设备1上的RAM10：设备1上无连接1 1：禁止	R/W

DSR1指定要作为设备1访问的内存类型和闪存的大小。

36.2.6 MDTR:内存延迟调整寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	DQSEDOPI[3:0]				DV1DEL[7:0]							
重置后的值：	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DQSESOPI[3:0]				DQSERAM[3:0]				DV0DEL[7:0]							
重置后的值：	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DV0DEL[7:0]	设备0延迟设置 这些位指定要在输入选通信号(OM_DQS)上插入的延迟周期，以调整在SOPI或DOPI模式下对器件0进行读取访问期间锁存数据的时序。	R/W
11:8	DQSERAM[3:0]	OM_DQS启用计数器 DOPI模式[RAM]的设置。	R/W
15:12	DQSESOPI[3:0]	OM_DQS启用计数器 SOPI模式[闪光灯]的设置。	R/W
23:16	DV1DEL[7:0]	设备1延迟设置 这些位指定要在输入选通信号(OM_DQS)上插入的延迟周期，以调整在SOPI或DOPI模式下对器件1进行读取访问期间锁存数据的时序。	R/W
27:24	DQSEDOPI[3:0]	OM_DQS启用计数器 DOPI模式[闪光灯]的设置。	R/W
31:28	—	这些位被读取为0。写入值应为0。	R/W

MDTR设置内存访问的时序调整。

有关自动校准的信息，请参见第36.3节。手术。

在使用OM_DQS时钟输入的读取操作期间（在SOPI或DOPI模式下），在命令和地址阶段之后，OM_DQS时钟从高阻抗状态转换为输入状态（用于从外部设备接收值0）完成。要获得有效数据，请调整DQS启用计数器和延迟周期。

OM_DQS启用计数器设置（OM_SCLK单位）

0000：1个时钟周期

0001：2个时钟周期

0010：3个时钟周期

0011：4个时钟周期

⋮

1111：16个时钟周期

OM_DQS启用计数器设置示例

Table 36.4 OctaRAM

Number of dummy cycles	DOPI Pre-cycle On	DOPI Pre-cycle Off
3	3 to 4	3 to 5
4	3 to 5	3 to 6
5	3 to 6	3 to 7
6	3 to 7	3 to 8
7	3 to 8	3 to 9
8	3 to 9	3 to 10

Table 36.5 OctaFlash

Number of dummy cycles*1	SOPI Pre-cycle On	DOPI Pre-cycle On	DOPI Pre-cycle Off
4	9	6	6 to 7
6	9 to 11	6 to 8	6 to 9
8	9 to 13	6 to 10	6 to 11
10	9 to 15	6 to 12	6 to 13
12	9 to 15	6 to 14	6 to 15
14	9 to 15	6 to 15	6 to 15
16	9 to 15	6 to 15	6 to 15
18	9 to 15	6 to 15	6 to 15
20	9 to 15	6 to 15	6 to 15

Note 1. Some read register commands of OctaFlash is always 4 cycles regardless of dummy cycle setting of configuration register.

These two tables list cases of DQS delay.

If DQS delay cycle is not within this range, see section 36.6. OM_DQS Enable Counter, and recalculate the correct range.

36.2.7 ACTR : Auto-Calibration Timer Register

Base address: OSPI = 0x400A_6000

Offset address: 0x18

Bit position:	31																													0
Bit field:	CTP[31:0]																													
Value after reset:	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CTP[31:0]	Automatic calibration cycle time setting Sets performing cycle for the automatic calibration with 32 bits. Automatic calibration cycle time (ns) = CTP[31:0] × OM_SCLK / 2 When automatic calibration is enabled (CDSR.ACMODE[1:0] = 0x1) and the value of the internal timer is equal to that of this register, automatic calibration will start.	R/W

The ACTR register is a register that sets the cycle at which automatic calibration is executed.

Table 36.4 OctaRAM

虚拟周期数	DOPI Pre-cycle On	DOPI Pre-cycle Off
3	3 to 4	3 to 5
4	3 to 5	3 to 6
5	3 to 6	3 to 7
6	3 to 7	3 to 8
7	3 to 8	3 to 9
8	3 to 9	3 to 10

Table 36.5 OctaFlash

虚拟周期数*1	SOPI Pre-cycle On	DOPI Pre-cycle On	DOPI Pre-cycle Off
4	9	6	6 to 7
6	9 to 11	6 to 8	6 to 9
8	9 to 13	6 to 10	6 to 11
10	9 to 15	6 to 12	6 to 13
12	9 to 15	6 to 14	6 to 15
14	9 to 15	6 to 15	6 to 15
16	9 to 15	6 to 15	6 to 15
18	9 to 15	6 to 15	6 to 15
20	9 to 15	6 to 15	6 to 15

注1.OctaFlash的某些读取寄存器命令始终为4个周期，与配置寄存器的虚拟周期设置无关。

这两个表列出了DQS延迟的情况。

如果DQS延迟周期不在此范围内，请参阅第36.6节。OM_DQS启用计数器，并重新计算正确的范围。

36.2.7 ACTR:自动校准定时器寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x18

Bit position:	31																													0
Bit field:	CTP[31:0]																													
重置后的值:	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CTP[31:0]	自动校准周期时间设置 使用32位设置自动校准的执行周期。 自动校准周期时间(ns)=CTP[31:0]×OM_SCLK2 当自动校准使能（CDSR.ACMODE[1:0]=0x1）并且内部定时器的值等于该寄存器的值时，自动校准将开始。	R/W

ACTR寄存器是设置执行自动校准的周期的寄存器。

36.2.8 ACAR0 : Auto-Calibration Address Register 0

Base address: OSPI = 0x400A_6000

Offset address: 0x1C

Bit position:	31																													0
Bit field:	CAD0[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CAD0[31:0]	Automatic calibration address Sets the address of the write and read destination to perform the automatic calibration of device 0.	R/W

ACAR0 sets the address of the write/read destination to be performed the automatic calibration of device 0.

36.2.9 ACAR1 : Auto-Calibration Address Register 1

Base address: OSPI = 0x400A_6000

Offset address: 0x20

Bit position:	31																													0
Bit field:	CAD1[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CAD1[31:0]	Automatic calibration address Sets the address of the write and read destination to perform the automatic calibration of device 1.	R/W

ACAR1 sets the address of the write/read destination to be performed the automatic calibration of device 1.

36.2.10 DRCSTR : Device Memory Map Read Chip Select Timing Setting Register

Base address: OSPI = 0x400A_6000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DVRDLO1[1:0]		DVRDHI1[2:0]			DVRDCMD1[2:0]			CTR1	CTRW1[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVRDLO0[1:0]		DVRDHI0[2:0]			DVRDCMD0[2:0]			CTR0	CTRW0[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	CTRW0[6:0]	Device 0 single continuous read waiting cycle setting in PCLKA units When single continuous read mode of Device 0 is enabled, OM_CS0 is fixed to Low for the clock cycle to be set by CTRW0 from the previous read operation. If the number of clock cycles exceeds the value to be set in these bits before the next read operation is performed, OM_CS0 is returned to High, and the single continuous read will finish.	R/W

36.2.8 ACAR0：自动校准地址寄存器0

Base address: OSPI = 0x400A_6000

Offset address: 0x1C

Bit position:	31																													0
Bit field:	CAD0[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CAD0[31:0]	自动校准地址 设置写入和读取目标的地址以执行设备0的自动校准。	R/W

ACAR0设置写入读取目标的地址以执行设备0的自动校准。

36.2.9 ACAR1：自动校准地址寄存器1

Base address: OSPI = 0x400A_6000

Offset address: 0x20

Bit position:	31																													0
Bit field:	CAD1[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	CAD1[31:0]	自动校准地址 设置写入和读取目标的地址以执行设备1的自动校准。	R/W

ACAR1设置写入读取目标的地址以执行设备1的自动校准。

36.2.10 DRCSTR:器件存储器映射读取片选时序设置寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x34

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DVRDLO1[1:0]		DVRDHI1[2:0]			DVRDCMD1[2:0]			CTR1	CTRW1[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVRDLO0[1:0]		DVRDHI0[2:0]			DVRDCMD0[2:0]			CTR0	CTRW0[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	CTRW0[6:0]	以PCLKA为单位的设备0单个连续读取等待周期设置 当设备0的单次连续读取模式启用时，OM_CS0固定为低电平，时钟周期由CTRW0从上一次读取操作设置。如果在执行下一次读取操作之前时钟周期数超过了这些位中设置的值，则OM_CS0返回高电平，单次连续读取将完成。	R/W

Bit	Symbol	Function	R/W
7	CTR0	Device 0 single continuous read mode setting When the OSPI receives single read with increment address, multiple single read is executed in one CS asserted period (refer to section 36.5.2. Single continuous read operation). This bit must be 0 in SPI mode. 0: Single continuous read mode is disabled for device 0. 1: Single continuous read mode is enabled for device 0.	R/W
10:8	DVRDCMD0[2:0]	Device 0 Command execution interval setting*1 Indicates the timing between command to command for the device 0. Timing definition from OM_CS0 high to the next OM_CS0 low 0 0 0: 2 clock cycles 0 0 1: 5 clock cycles 0 1 0: 7 clock cycles 0 1 1: 9 clock cycles 1 0 0: 11 clock cycles 1 0 1: 13 clock cycles 1 1 0: 15 clock cycles 1 1 1: 17 clock cycles	R/W
13:11	DVRDHI0[2:0]	Device 0 select signal pull-up timing setting*1 Indicates the timing, from the end of read operation to the select signal is pulled up. Timing definition from the last OM_SCLK low to OM_CS0 high 0 0 0: Setting prohibit 0 0 1: Setting prohibit 0 1 0: Setting prohibit 0 1 1: Setting prohibit (DOPI mode) 5 clock cycles (Other mode) 1 0 0: Setting prohibit (DOPI mode) 6 clock cycles (Other mode) 1 0 1: 6.5 clock cycles (DOPI mode) 7 clock cycles (Other mode) 1 1 0: 7.5 clock cycles (DOPI mode) 8 clock cycles (Other mode) 1 1 1: 8.5 clock cycles (DOPI mode) 9 clock cycles (Other mode)	R/W
15:14	DVRDLO0[1:0]	Device 0 select signal pull-down timing setting*1 Indicates the timing between the select signal pull-down to the read operation for the device 0. Timing definition from OM_CS0 low to the first OM_SCLK high 0 0: Setting prohibit 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode)	R/W
22:16	CTRW1[6:0]	Device 1 single continuous read waiting cycle setting in PCLKA units When single continuous read mode of Device 1 is enabled, OM_CS1 is fixed to Low for the clock cycle to be set by CTRW1 from the previous read operation. If the number of clock cycles exceeds the value to be set in these bits before the next read operation is performed, OM_CS1 is returned to High, and the single continuous read will finish.	R/W
23	CTR1	Device 1 single continuous read mode setting When the OSPI receives single read with increment address, multiple single read is executed in one CS asserted period (refer to section 36.5.2. Single continuous read operation). This bit must be 0 in SPI mode. 0: Single continuous read mode is disabled for device 1. 1: Single continuous read mode is enabled for device 1.	R/W

Bit	Symbol	Function	R/W
7	CTR0	Device0单次连续读取模式设置 当OSPI接收到带有递增地址的单次读取时，会在一个CS断言周期内执行多次单次读取（请参阅第36.5.2节。单次连续读取操作）。该位在SPI模式下必须为0。 0：禁用设备0的单次连续读取模式。1：启用设备0的单次连续读取模式。	R/W
10:8	DVRDCMD0[2:0]	软元件0命令执行间隔设置*1 指示设备0的命令与命令之间的时间。 从OM_CS0高电平到下一个OM_CS0低电平的时序定义 000：2个时钟周期00 1：5个时钟周期010： 7个时钟周期011：9个 时钟周期100：11个时 钟周期101：13个时钟 周期110：15个时钟周 期111:17个时钟周期	R/W
13:11	DVRDHI0[2:0]	设备0选择信号上拉时序设置*1 表示从读操作结束到选择信号上拉的时序。 从最后一个OM_SCLK低到OM_CS0高的时序定义 000：设置禁止001：设置禁止010 ：设置禁止011：设置禁止（DOPI模式）5个时钟周期（其他模式） 100：设置禁止（DOPI模式）6个时钟周期（其他模式） 101：6.5个时钟周期（DOPI模式）7个时钟周期（其他模式） 110：7.5个时钟周期（DOPI模式）8个时钟周期（其他模式） 111：8.5个时钟周期（DOPI模式）9个时钟周期（其他模式）	R/W
15:14	DVRDLO0[1:0]	设备0选择信号下拉时序设置*1 指示从选择信号下拉到器件0的读取操作之间的时序。从OM_CS0低到第一个OM_SCLK高的时序定义 00：设置禁止01：2.5个时钟周期（DOPI模式）3个时钟周期（其他模式） 10：3.5个时钟周期（DOPI模式）4个时钟周期（其他模式） 11：4.5个时钟周期（DOPI模式）5个时钟周期（其他模式）	R/W
22:16	CTRW1[6:0]	以PCLKA为单位的设备1单次连续读取等待周期设置 当设备1的单次连续读取模式启用时，OM_CS1固定为低电平，时钟周期由CTRW1从上一次读取操作设置。如果在执行下一次读取操作之前时钟周期数超过了这些位中设置的值，则OM_CS1返回高电平，单次连续读取将完成。	R/W
23	CTR1	设备1单次连续读取模式设置 当OSPI接收到带有递增地址的单次读取时，会在一个CS断言周期内执行多次单次读取（请参阅第36.5.2节。单次连续读取操作）。该位在SPI模式下必须为0。 0：禁用设备1的单次连续读取模式。1：启用设备1的单次连续读取模式。	R/W

Bit	Symbol	Function	R/W
26:24	DVRDCMD1[2:0]	Device 1 Command execution interval*1 Indicates the timing, between command and command for device 1. Timing, until the OM_CS1 signal goes from High to the next Low 0 0 0: 2 clock cycles 0 0 1: 5 clock cycles 0 1 0: 7 clock cycles 0 1 1: 9 clock cycles 1 0 0: 11 clock cycles 1 0 1: 13 clock cycles 1 1 0: 15 clock cycles 1 1 1: 17 clock cycles	R/W
29:27	DVRDHI1[2:0]	Device 1 select signal High timing setting*1 Indicates the timing, from the end of read operation to the select signal is pulled up. Timing definition from the last OM_SCLK low to OM_CS1 high 0 0 0: Setting prohibit 0 0 1: Setting prohibit 0 1 0: Setting prohibit 0 1 1: Setting prohibit (DOPI mode) 5 clock cycles (Other mode) 1 0 0: Setting prohibit (DOPI mode) 6 clock cycles (Other mode) 1 0 1: 6.5 clock cycles (DOPI mode) 7 clock cycles (Other mode) 1 1 0: 7.5 clock cycles (DOPI mode) 8 clock cycles (Other mode) 1 1 1: 8.5 clock cycles (DOPI mode) 9 clock cycles (Other mode)	R/W
31:30	DVRDLO1[1:0]	Device 1 select signal pull-down timing setting*1 Indicates the timing between the select signal pull-down to the read operation for the device 1. Timing definition from OM_CS1 low to the first OM_SCLK high 0 0: Setting prohibited 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode)	R/W

Note 1. These clock cycles are values in OCTACLK units. In OM_SCLK units, the clock cycle is 1/2 of the above table.

DRCSTR sets the timing of memory-mapped reading for each device.

36.2.11 DWCSTR : Device Memory Map Write Chip Select Timing Setting Register

Base address: OSPI = 0x400A_6000

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DVWLO1[1:0]		DVWHI1[2:0]			DVWCMD1[2:0]			CTW1	CTWW1[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVWLO0[1:0]		DVWHI0[2:0]			DVWCMD0[2:0]			CTW0	CTWW0[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
26:24	DVRDCMD1[2:0]	软元件1命令执行间隔*1 指示设备1的命令和命令之间的时序。 时序，直到OM_CS1信号从高电平变为下一个低电平 000：2个时钟周期00 1：5个时钟周期010： 7个时钟周期011：9个 时钟周期100：11个时 钟周期101：13个时钟 周期110：15个时钟周 期111:17个时钟周期	R/W
29:27	DVRDHI1[2:0]	设备1选择信号高时序设置*1 表示从读操作结束到选择信号上拉的时序。 从最后一个OM_SCLK低到OM_CS1高的时序定义 000：设置禁止001：设置禁止010 ：设置禁止011：设置禁止（DOPI模 式）5个时钟周期（其他模式） 100：设置禁止（DOPI模式）6个时 钟周期（其他模式） 101：6.5个时钟周期（DOPI模式）7 个时钟周期（其他模式） 110：7.5个时钟周期（DOPI模式）8 个时钟周期（其他模式） 111：8.5个时钟周期（DOPI模式）9 个时钟周期（其他模式）	R/W
31:30	DVRDLO1[1:0]	设备1选择信号下拉时序设置*1 指示从选择信号下拉到器件读操作之间的时序1.从OM_CS1低到第一个OM_SCLK高的时序定义 00：禁止设置01：2.5个时钟周期 （DOPI模式）3个时钟周期（其他 模式） 10：3.5个时钟周期（DOPI模式）4 个时钟周期（其他模式） 11：4.5个时钟周期（DOPI模式）5 个时钟周期（其他模式）	R/W

注1.这些时钟周期是以OCTACLK为单位的值。以OM_SCLK为单位，时钟周期为上表的12。

DRCSTR设置每个设备的内存映射读取时间。

36.2.11 DWCSTR:器件存储器映射写入片选时序设置寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x38

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DVWLO1[1:0]		DVWHI1[2:0]			DVWCMD1[2:0]			CTW1	CTWW1[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVWLO0[1:0]		DVWHI0[2:0]			DVWCMD0[2:0]			CTW0	CTWW0[6:0]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	CTWW0[6:0]	Device 0 single continuous write waiting cycle setting in PCLKA units When single continuous write mode of Device 0 is enabled, OM_CS0 is fixed to Low for the clock cycle to be set by CTWW0 from the previous single write operation. If the number of clock cycles exceeds the value to be set in these bits before the next single write operation is performed, OM_CS0 is returned to High, and the single continuous write will finish.	R/W
7	CTW0	Device 0 single continuous write mode setting When the OSPI receives single write with increment address, multiple single write is executed in one CS asserted period. See section 36.3.3.1. Write Operation about the operation of the single continuous write. 0: Single continuous write mode is disabled for device 0 1: Single continuous write mode is enabled for device 0	R/W
10:8	DVWCMD0[2:0]	Device 0 Command execution interval setting*1 Indicates the timing between command to command for the device 0. Timing definition from OM_CS0 high to the next OM_CS0 low 0 0 0: 2 clock cycles 0 0 1: 5 clock cycles 0 1 0: 7 clock cycles 0 1 1: 9 clock cycles 1 0 0: 11 clock cycles 1 0 1: 13 clock cycles 1 1 0: 15 clock cycles 1 1 1: 17 clock cycles	R/W
13:11	DVWHI0[2:0]	Device 0 select signal pull-up timing setting*1 Indicates the timing, from the end of write operation to the select signal is pulled up. Timing definition from the last OM_SCLK low to OM_CS0 high 0 0 0: 1.5 clock cycles (DOPI mode) 2 clock cycles (Other mode) 0 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 0 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 0 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode) 1 0 0: 5.5 clock cycles (DOPI mode) 6 clock cycles (Other mode) 1 0 1: 6.5 clock cycles (DOPI mode) 7 clock cycles (Other mode) 1 1 0: 7.5 clock cycles (DOPI mode) 8 clock cycles (Other mode) 1 1 1: 8.5 clock cycles (DOPI mode) 9 clock cycles (Other mode)	R/W
15:14	DVWLO0[1:0]	Device 0 select signal pull-down timing setting*1 Indicates the timing between the select signal pull-down to the write operation for the device 0. Timing definition from OM_CS0 low to the first OM_SCLK high 0 0: Setting prohibit 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode)	R/W
22:16	CTWW1[6:0]	Device 1 single continuous write waiting cycle setting in PCLKA units When single continuous write mode of Device 1 is enabled, OM_CS1 is fixed to Low for the clock cycle to be set by CTWW1 from the previous single write operation. If the number of clock cycles exceeds the value to be set in these bits before the next single write operation is performed, OM_CS1 is returned to High, and the single continuous write will finish.	R/W
23	CTW1	Device 1 single continuous write mode setting When the OSPI receives single write with increment address, multiple single write is executed in one CS asserted period. See section 36.3.3.1. Write Operation about the operation of the single continuous write. 0: Single continuous write mode is disabled for device 1 1: Single continuous write mode is enabled for device 1	R/W

Bit	Symbol	Function	R/W
6:0	CTWW0[6:0]	以PCLKA为单位的设备0单个连续写入等待周期设置 当设备0的单次连续写入模式启用时，OM_CS0固定为低电平，时钟周期由CTWW0从上一次单次写入操作设置。如果在执行下一次单次写操作之前时钟周期数超过了这些位中设置的值，则OM_CS0返回高电平，单次连续写将完成。	R/W
7	CTW0	Device0单次连续写入模式设置 当OSPI接收到带有递增地址的单次写入时，会在一个CS置位周期内执行多次单次写入。请参阅第36.3.3.1节。WriteOperation关于单次连续写入的操作。 0：禁用设备0的单次连续写入模式1：启用设备0的单次连续写入模式	R/W
10:8	DVWCMD0[2:0]	软元件0命令执行间隔设置*1 指示设备0的命令与命令之间的时间。 从OM_CS0高电平到下一个OM_CS0低电平的时序定义 000：2个时钟周期00 1：5个时钟周期010： 7个时钟周期011：9个 时钟周期100：11个时 钟周期101：13个时钟 周期110：15个时钟周 期111:17个时钟周期	R/W
13:11	DVWHI0[2:0]	设备0选择信号上拉时序设置*1 指示时序，从写操作结束到选择信号被上拉。 从最后一个OM_SCLK低到OM_CS0高的时序定义 000：1.5个时钟周期（DOPI模式）2 个时钟周期（其他模式） 001：2.5个时钟周期（DOPI模式）3 个时钟周期（其他模式） 010：3.5个时钟周期（DOPI模式）4 个时钟周期（其他模式） 011：4.5个时钟周期（DOPI模式）5 个时钟周期（其他模式） 100：5.5个时钟周期（DOPI模式）6 个时钟周期（其他模式） 101：6.5个时钟周期（DOPI模式）7 个时钟周期（其他模式） 110：7.5个时钟周期（DOPI模式）8 个时钟周期（其他模式） 111：8.5个时钟周期（DOPI模式）9 个时钟周期（其他模式）	R/W
15:14	DVWLO0[1:0]	设备0选择信号下拉时序设置*1 指示从选择信号下拉到器件0的写操作之间的时序。时序定义从OM_CS0低到第一个OM_SCLK高 00：设置禁止01：2.5个时钟周期（DOPI模式）3个时钟周期（其他模式） 10：3.5个时钟周期（DOPI模式）4 个时钟周期（其他模式） 11：4.5个时钟周期（DOPI模式）5 个时钟周期（其他模式）	R/W
22:16	CTWW1[6:0]	以PCLKA为单位的设备1单个连续写入等待周期设置 当设备1的单次连续写入模式启用时，OM_CS1固定为低电平，时钟周期由CTWW1从上一次单次写入操作设置。如果在执行下一次单次写操作之前时钟周期数超过了这些位中设置的值，则OM_CS1返回高电平，单次连续写将完成。	R/W
23	CTW1	设备1单次连续写入模式设置 当OSPI接收到带有递增地址的单次写入时，会在一个CS置位周期内执行多次单次写入。请参阅第36.3.3.1节。WriteOperation关于单次连续写入的操作。 0：禁用设备1的单次连续写入模式1：启用设备1的单次连续写入模式	R/W

Bit	Symbol	Function	R/W
26:24	DVWCMD1[2:0]	Device 1 Command execution interval setting*1 Indicates the timing between command to command for the device 1. Timing definition from OM_CS1 high to the next OM_CS1 low 0 0 0: setting prohibited 0 0 1: 5 clock cycles 0 1 0: 7 clock cycles 0 1 1: 9 clock cycles 1 0 0: 11 clock cycles 1 0 1: 13 clock cycles 1 1 0: 15 clock cycles 1 1 1: 17 clock cycles	R/W
29:27	DVWHI1[2:0]	Device 1 select signal pull-up timing setting*1 Indicates the timing, from the end of write operation to the select signal is pulled up. Timing definition from the last OM_SCLK low to OM_CS1 high 0 0 0: 1.5 clock cycles (DOPI mode) 2 clock cycles (Other mode) 0 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 0 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 0 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode) 1 0 0: 5.5 clock cycles (DOPI mode) 6 clock cycles (Other mode) 1 0 1: 6.5 clock cycles (DOPI mode) 7 clock cycles (Other mode) 1 1 0: 7.5 clock cycles (DOPI mode) 8 clock cycles (Other mode) 1 1 1: 8.5 clock cycles (DOPI mode) 9 clock cycles (Other mode)	R/W
31:30	DVWLO1[1:0]	Device 1 select signal pull-down timing setting*1 Indicates the timing between the device 1 select signal pull-down to the write operation. Timing definition from OM_CS1 low to the first OM_SCLK high 0 0: Setting prohibit 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode)	R/W

Note 1. These clock cycles are values in internal clock units. In OM_SCLK units, the clock cycle is 1/2 of the above table.

DWCSTR sets the timing of memory-mapped writing for each device.

36.2.12 DCSTR : Device Chip Select Timing Setting Register

Base address: OSPI = 0x400A_6000

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVSELLO[1:0]		DVSELHI[2:0]			DVSELCMD[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
26:24	DVWCMD1[2:0]	软元件1命令执行间隔设置*1 指示设备1的命令与命令之间的时间。 从OM_CS1高电平到下一个OM_CS1低电平的时序定义 000：设置禁止001：5 个时钟周期010：7个时 钟周期011：9个时钟周 期100：11个时钟周期1 01：13个时钟周期110 ：15个时钟周期111：1 7个时钟周期	R/W
29:27	DVWHI1[2:0]	设备1选择信号上拉时序设置*1 指示时序，从写操作结束到选择信号被上拉。 从最后一个OM_SCLK低到OM_CS1高的时序定义 000：1.5个时钟周期（DOPI模式）2 个时钟周期（其他模式） 001：2.5个时钟周期（DOPI模式）3 个时钟周期（其他模式） 010：3.5个时钟周期（DOPI模式）4 个时钟周期（其他模式） 011：4.5个时钟周期（DOPI模式）5 个时钟周期（其他模式） 100：5.5个时钟周期（DOPI模式）6 个时钟周期（其他模式） 101：6.5个时钟周期（DOPI模式）7 个时钟周期（其他模式） 110：7.5个时钟周期（DOPI模式）8 个时钟周期（其他模式） 111：8.5个时钟周期（DOPI模式）9 个时钟周期（其他模式）	R/W
31:30	DVWLO1[1:0]	设备1选择信号下拉时序设置*1 指示设备1选择信号下拉到写操作之间的时序。 从OM_CS1低到第一个OM_SCLK高的时序定义 00：设置禁止01：2.5个时钟周期 （DOPI模式）3个时钟周期（其他 模式） 10：3.5个时钟周期（DOPI模式）4 个时钟周期（其他模式） 11：4.5个时钟周期（DOPI模式）5 个时钟周期（其他模式）	R/W

注1.这些时钟周期是以内部时钟为单位的值。以OM_SCLK为单位，时钟周期为上表的12。

DWCSTR设置每个设备的内存映射写入时间。

36.2.12 DCSTR:器件片选时序设置寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x3C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DVSELLO[1:0]		DVSELHI[2:0]			DVSELCMD[2:0]			—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R
10:8	DVSELCMD[2:0]	Device Command execution interval setting*1 Indicates the timing between command to command. Timing definition from OM_CS high to the next OM_CS low 0 0 0: 2 clock cycles 0 0 1: 5 clock cycles 0 1 0: 7 clock cycles 0 1 1: 9 clock cycles 1 0 0: 11 clock cycles 1 0 1: 13 clock cycles 1 1 0: 15 clock cycles 1 1 1: 17 clock cycles	R/W
13:11	DVSELHI[2:0]	Device select signal pull-up timing setting*1 Indicates the timing when the select signal is pulled up from the end of the command execution. Timing definition from the last OM_SCLK low to OM_CS high 0 0 0: Setting prohibited 0 0 1: Setting prohibited 0 1 0: Setting prohibited 0 1 1: Setting prohibited (DOPI mode) 5 clock cycles (Other mode) 1 0 0: Setting prohibited (DOPI mode) 6 clock cycles (Other mode) 1 0 1: 6.5 clock cycles (DOPI mode) 7 clock cycles (Other mode) 1 1 0: 7.5 clock cycles (DOPI mode) 8 clock cycles (Other mode) 1 1 1: 8.5 clock cycles (DOPI mode) 9 clock cycles (Other mode)	R/W
15:14	DVSELLO[1:0]	Device select signal pull-down timing setting*1 Indicates the timing, from the device selection signal is pulled-down to the command execution. Timing definition from OM_CS low to the first OM_SCLK high 0 0: Setting prohibit 0 1: 2.5 clock cycles (DOPI mode) 3 clock cycles (Other mode) 1 0: 3.5 clock cycles (DOPI mode) 4 clock cycles (Other mode) 1 1: 4.5 clock cycles (DOPI mode) 5 clock cycles (Other mode)	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R

Note 1. These clock cycles are values in OCTACLK units. In OM_SCLK units, the clock cycle is 1/2 of the above table.

DCSTR sets the operation timings of each device other than memory-mapped reading and writing.

36.2.13 CDSR : Controller and Device Setting Register

Base address: OSPI = 0x400A_6000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DLFT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	ACMODE[1:0]		ACME ME1	ACME ME0	—	—	—	—	DV1PC	DV0PC	DV1TTYP[1:0]		DV0TTYP[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R
10:8	DVSELCMD[2:0]	软元件命令执行间隔设置*1 指示命令到命令之间的时间。 从OM_CS高电平到下一个OM_CS低电平的时序定义 000：2个时钟周期00 1：5个时钟周期010： 7个时钟周期011：9个 时钟周期100：11个时 钟周期101：13个时钟 周期110：15个时钟周 期111:17个时钟周期	R/W
13:11	DVSELHI[2:0]	器件选择信号上拉时序设置*1 表示从命令执行结束拉高选择信号的时间。从最后一个OM_SCLK低到OM_CS高的时序定义 000：禁止设置001：禁止设置010： 禁止设置011：禁止设置（DOPI模式） 5个时钟周期（其他模式） 100：禁止设置（DOPI模式）6个时钟 周期（其他模式） 101：6.5个时钟周期（DOPI模式）7 个时钟周期（其他模式） 110：7.5个时钟周期（DOPI模式）8 个时钟周期（其他模式） 111：8.5个时钟周期（DOPI模式）9 个时钟周期（其他模式）	R/W
15:14	DVSELLO[1:0]	器件选择信号下拉时序设置*1 表示从器件选择信号被下拉到命令执行的时序。从OM_CS低到第一个OM_SCLK高的时序定义 00：设置禁止01：2.5个时钟周期 （DOPI模式）3个时钟周期（其他 模式） 10：3.5个时钟周期（DOPI模式）4 个时钟周期（其他模式） 11：4.5个时钟周期（DOPI模式）5 个时钟周期（其他模式）	R/W
31:16	—	这些位被读取为0。写入值应为0。	R

注1.这些时钟周期是以OCTACLK为单位的值。以OM_SCLK为单位，时钟周期为上表的12。

DCSTR设置每个设备的操作时序，而不是内存映射读取和写入。

36.2.13 CDSR：控制器和设备设置寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x40

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	DLFT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	ACMODE[1:0]		ACME ME1	ACME ME0	—	—	—	—	DV1PC	DV0PC	DV1TTYP[1:0]		DV0TTYP[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	DV0TTYP[1:0]	Device0_transfer_type setting 0 0: SPI mode 0 1: SOPI mode 1 0: DOPI mode 1 1: Setting prohibited	R/W
3:2	DV1TTYP[1:0]	Device1_transfer_type setting 0 0: SPI mode 0 1: SOPI mode 1 0: DOPI mode 1 1: Setting prohibited	R/W
4	DV0PC	Device0_memory precycle setting 0: Disable 1: Enable	R/W
5	DV1PC	Device1_memory precycle setting*1 0: Disable 1: Enable	R/W
9:6	—	These bits are read as 0. The write value should be 0.	R/W
10	ACMEME0	Automatic calibration memory enable setting for device 0 Automatic calibration supports DOPI and SOPI mode. To end DOPI/SOPI mode, disable automatic calibration. 0: Disable 1: Enable	R/W
11	ACMEME1	Automatic calibration memory enable setting for device 1 Automatic calibration supports DOPI and SOPI mode. To end DOPI/SOPI mode, disable automatic calibration. 0: Disable 1: Enable	R/W
13:12	ACMODE[1:0]	Automatic calibration mode The ACMODE bits should be set to disabled, before program/erase access to the OctaFlash device. Automatic calibration is available in the DOPI and SOPI mode. 0 0: Automatic calibration is disabled*2 0 1: Automatic calibration is enabled and modify MDTR 1 0: Automatic calibration immediately is executed for all trim code, but it will not modify MDTR 1 1: Setting prohibited	R/W
30:14	—	These bits are read as 0. The write value should be 0.	R/W
31	DLFT	Deadlock Free Timer Enable*3 Enable the timer to prevent the occurrence of controller deadlock. The timeout status is reset only by a system reset. 0: Enable timer 1: Disable timer	R/W

Note 1. This bit should be set 1 in SOPI mode.
Note 2. When automatic calibration is disabled, the device 0 delay and device 1 delay should be manually specified in the memory delay trim register (MDTR) (see section 36.2.6. MDTR : Memory Delay Trim Register).
To determine the device 0 delay and device 1 delay values to be specified in the register, perform automatic calibration in advance and obtain valid delay values from the results.
Note 3. This function is available only when OM_SCLK is 100 MHz. Otherwise, disable the timer.

CDSR controls the automatic calibration, output byte order, precycle setting, and device transfer type of the controller and each device.

Bit	Symbol	Function	R/W
1:0	DV0TTYP[1:0]	Device0_transfer_type setting 00：SPI模式01：SOPI 模式10：DOPI模式11 ：禁止设置	R/W
3:2	DV1TTYP[1:0]	Device1_transfer_type setting 00：SPI模式01：SOPI 模式10：DOPI模式11 ：禁止设置	R/W
4	DV0PC	Device0_memory precycle setting 0：禁用1 ：启用	R/W
5	DV1PC	Device1_memory precycle setting*1 0：禁用1 ：启用	R/W
9:6	—	这些位被读取为0。写入值应为0。	R/W
10	ACMEME0	设备0的自动校准内存启用设置 自动校准支持DOPI和SOPI模式。要结束DOPISOPI模式，请禁用自动校准。 0：禁用1 ：启用	R/W
11	ACMEME1	设备1的自动校准内存启用设置 自动校准支持DOPI和SOPI模式。要结束DOPISOPI模式，请禁用自动校准。 0：禁用1 ：启用	R/W
13:12	ACMODE[1:0]	自动校准模式 在程序擦除访问之前，应将ACMODE位设置为禁用 OctaFlash device. 在DOPI和SOPI模式下可以使用自动校准。 00：禁用自动校准*2 01：启用自动校准并修改MDTR10：立即对所有修整代码执行自动校准，但不会修改MDTR 11：禁止设定	R/W
30:14	—	这些位被读取为0。写入值应为0。	R/W
31	DLFT	无死锁定时器启用*3 启用定时器以防止控制器死锁的发生。 超时状态只能通过系统复位来复位。 0：启用定时器1 ：禁用定时器	R/W

注1.在SOPI模式下，该位应设置为1。
注2.禁用自动校准时，应在内存延迟调整寄存器(MDTR)中手动指定设备0延迟和设备1延迟（参见第36.2.6节。MDTR：内存延迟调整寄存器）。要确定寄存器中要指定的设备0延迟和设备1延迟值，请提前执行自动校准，并从结果中获取有效的延迟值。

注3.此功能仅在OM_SCLK为100MHz时可用。否则，禁用计时器。

CDSR控制控制器和每个设备的自动校准、输出字节顺序、预循环设置和设备传输类型。

36.2.14 MDLR : Memory Map Dummy Length Register

Base address: OSPI = 0x400A_6000

Offset address: 0x44

Bit position:	31							24	23							16	15							8	7							0
Bit field:	DV1WDL[7:0]								DV1RDL[7:0]								DV0WDL[7:0]								DV0RDL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DV0RDL[7:0]	Device 0 Read dummy length setting Set the dummy length when reading to device 0 in OM_SCLK cycles unit.	R/W
15:8	DV0WDL[7:0]	Device 0 Write dummy length setting Set the dummy length when writing to device 0 in OM_SCLK cycles unit.	R/W
23:16	DV1RDL[7:0]	Device 1 Read dummy length setting Set the dummy length when reading to device 1 in OM_SCLK cycles unit.	R/W
31:24	DV1WDL[7:0]	Device 1 Write dummy length setting Set the dummy length when writing to device 1 in OM_SCLK cycles unit.	R/W

MDLR sets the dummy length for memory map write/read.

Note: When changing the dummy length for the OctaFlash device, modify the setting on the memory and then modify the setting in the DMLEN[7:0] bits in the device command setting register (DCSR) so that the dummy length becomes the same between the memory and OSPI. After that, execute the status read command to confirm the memory status.

36.2.15 MRWCR0 : Memory Map Read/Write Command Register 0

Base address: OSPI = 0x400A_6000

Offset address: 0x48

Bit position:	31							24	23							16	15							8	7							0
Bit field:	D0MWCMD1[7:0]								D0MWCMD0[7:0]								D0MRCMD1[7:0]								D0MRCMD0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	D0MRCMD0[7:0]	Memory map read command 0 setting Set the memory map read command. According to the memory spec to connect the device 0 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will send only command 0. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 0 is specified by CDSR.DV0TTYP[1:0].	R/W
15:8	D0MRCMD1[7:0]	Memory map read command 1 setting Set the memory map read command. According to the memory spec to connect the device 0 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will not send command 1. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 0 is specified by CDSR.DV0TTYP[1:0].	R/W

36.2.14 MDLR:内存映射虚拟长度寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x44

Bit position:	31							24	23							16	15							8	7							0
Bit field:	DV1WDL[7:0]								DV1RDL[7:0]								DV0WDL[7:0]								DV0RDL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	DV0RDL[7:0]	设备0读取虚拟长度设置 以OM_SCLK周期为单位设置读取到设备0时的虚拟长度。	R/W
15:8	DV0WDL[7:0]	设备0写入虚拟长度设置 以OM_SCLK周期为单位设置写入设备0时的虚拟长度。	R/W
23:16	DV1RDL[7:0]	设备1读取虚拟长度设置 以OM_SCLK周期为单位设置读取到设备1时的虚拟长度。	R/W
31:24	DV1WDL[7:0]	设备1写入虚拟长度设置 以OM_SCLK周期为单位设置写入设备1时的虚拟长度。	R/W

MDLR设置内存映射写入读取的虚拟长度。

Note: 更改OctaFlash器件的虚拟长度时，修改存储器上的设置，然后修改器件命令设置寄存器(DCSR)中DMLEN[7:0]位的设置，使存储器之间的虚拟长度相同和OSPI。之后，执行状态读取命令确认内存状态。

36.2.15 MRWCR0:内存映射读写命令寄存器0

Base address: OSPI = 0x400A_6000

Offset address: 0x48

Bit position:	31							24	23							16	15							8	7							0
Bit field:	D0MWCMD1[7:0]								D0MWCMD0[7:0]								D0MRCMD1[7:0]								D0MRCMD0[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	D0MRCMD0[7:0]	内存映射读取命令0设置设置内存映射 读取命令。 根据内存规范连接设备0和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器将只发送命令0。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备0的模式由CDSR.DV0TTYP[1:0]指定。	R/W
15:8	D0MRCMD1[7:0]	内存映射读取命令1设置设置内存映射 读取命令。 根据内存规范连接设备0和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器不会发送命令1。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备0的模式由CDSR.DV0TTYP[1:0]指定。	R/W

Bit	Symbol	Function	R/W
23:16	D0MWCMD0[7:0]	Memory map write command 0 setting Set the memory map write command. According to the memory spec to connect the device 0 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will send only command 0. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 0 is specified by CDSR.DV0TTYP[1:0].	R/W
31:24	D0MWCMD1[7:0]	Memory map write command 1 setting Set the memory map write command. According to the memory spec to connect the device 0 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will not send command 1. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 0 is specified by CDSR.DV0TTYP[1:0].	R/W

MRWCR0 sets the read/write commands for the device 0.

36.2.16 MRWCR1 : Memory Map Read/Write Command Register 1

Base address: OSPI = 0x400A_6000

Offset address: 0x4C

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	D1MWCMD1[7:0]	D1MWCMD0[7:0]	D1MRCMD1[7:0]	D1MRCMD0[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	D1MRCMD0[7:0]	Memory map read command 0 setting Set the memory map read command. According to the memory spec to connect the device 1 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will send only command 0. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 1 is specified by CDSR.DV1TTYP[1:0].	R/W
15:8	D1MRCMD1[7:0]	Memory map read command 1 setting Set the memory map read command. According to the memory spec to connect the device 1 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will not send command 1. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 1 is specified by CDSR.DV1TTYP[1:0].	R/W
23:16	D1MWCMD0[7:0]	Memory map write command 0 setting Set the memory map write command. According to the memory spec to connect the device 1 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will send only command 0. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 1 is specified by CDSR.DV1TTYP[1:0].	R/W
31:24	D1MWCMD1[7:0]	Memory map write command 1 setting Set the memory map write command. According to the memory spec to connect the device 1 and transfer type (SPI, SOPI, or DOPI mode), select the write command In SPI mode, the controller will not send command 1. In SOPI and DOPI mode, the controller will send command 1 first and then send command 0. The mode of device 1 is specified by CDSR.DV1TTYP[1:0].	R/W

Bit	Symbol	Function	R/W
23:16	D0MWCMD0[7:0]	内存映射写入命令0设置设置内存映射 写入命令。 根据内存规范连接设备0和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器将只发送命令0。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备0的模式由CDSR.DV0TTYP[1:0]指定。	R/W
31:24	D0MWCMD1[7:0]	内存映射写入命令1设置设置内存映射 写入命令。 根据内存规范连接设备0和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器不会发送命令1。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备0的模式由CDSR.DV0TTYP[1:0]指定。	R/W

MRWCR0设置设备0的读写命令。

36.2.16 MRWCR1:内存映射读写命令寄存器1

Base address: OSPI = 0x400A_6000

Offset address: 0x4C

Bit position:	31 … 24	23 … 16	15 … 8	7 … 0
Bit field:	D1MWCMD1[7:0]	D1MWCMD0[7:0]	D1MRCMD1[7:0]	D1MRCMD0[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	D1MRCMD0[7:0]	内存映射读取命令0设置设置内存映射 读取命令。 根据内存规格连接设备1和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器将只发送命令0。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备1的模式由CDSR.DV1TTYP[1:0]指定。	R/W
15:8	D1MRCMD1[7:0]	内存映射读取命令1设置设置内存映射 读取命令。 根据内存规格连接设备1和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器不会发送命令1。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备1的模式由CDSR.DV1TTYP[1:0]指定。	R/W
23:16	D1MWCMD0[7:0]	内存映射写入命令0设置设置内存映射 写入命令。 根据内存规格连接设备1和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器将只发送命令0。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备1的模式由CDSR.DV1TTYP[1:0]指定。	R/W
31:24	D1MWCMD1[7:0]	内存映射写入命令1设置设置内存映射 写入命令。 根据内存规格连接设备1和传输类型（SPI、SOPI或DOPI模式），选择写入命令 在SPI模式下，控制器不会发送命令1。 在SOPI和DOPI模式下，控制器会先发送命令1，然后发送命令0。设备1的模式由CDSR.DV1TTYP[1:0]指定。	R/W

MRWCR1 sets the read/write commands for the device 1.

36.2.17 MRWCSR : Memory Map Read/Write Setting Register

Base address: OSPI = 0x400A_6000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	MWO1	MWCL1[2:0]			MWAL1[2:0]			PREN1	MRO1	MRCL1[2:0]			MRAL1[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MWO0	MWCL0[2:0]			MWAL0[2:0]			PREN0	MRO0	MRCL0[2:0]			MRAL0[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	MRAL0[2:0]	Device 0 read address length setting Set the memory map read address byte length for device 0.	R/W
5:3	MRCL0[2:0]	Device 0 read command length setting Set the write command byte length for device 0.	R/W
6	MRO0	Device 0 read order setting*1 0: Read order is byte0, byte1, byte2, byte3. 1: Read order is byte1, byte0, byte3, byte2.	R/W
7	PREN0	Preamble bit enable for mem0 memory-map read*2 0: No check preamble bit 1: Check preamble bit from OctaFlash (if OctaFlash is connected to device 0)	R/W
10:8	MWAL0[2:0]	Device 0 write address length setting Set the memory map write address byte length for device 0.	R/W
13:11	MWCL0[2:0]	Device 0 write command length setting Set the write command byte length for device 0.	R/W
14	MWO0	Device 0 write order setting*1 0: Write order is byte0, byte1, byte2, byte3. 1: Write order is byte1, byte0, byte3, byte2.	R/W
15	—	This bit is read as 0. The write value should be 0.	R
18:16	MRAL1[2:0]	Device 1 read address length setting Set the memory map read address byte length for device 1.	R/W
21:19	MRCL1[2:0]	Device 1 read command length setting Set the read command byte length for device 1.	R/W
22	MRO1	Device 1 read order setting*1 0: Read order is byte0, byte1, byte2, byte3. 1: Read order is byte1, byte0, byte3, byte2.	R/W
23	PREN1	Preamble bit enable for mem1 memory-map read*2 0: No check preamble bit 1: Check preamble bit from OctaFlash (if OctaFlash is connected to device 1)	R/W
26:24	MWAL1[2:0]	Device 1 write address length setting Set the memory map write address byte length for device 1.	R/W
29:27	MWCL1[2:0]	Device 1 write command length setting Set the number of bytes in the write command for device 1.	R/W
30	MWO1	Device 1 write order setting*1 0: Write order is byte0, byte1, byte2, byte3. 1: Write order is byte1, byte0, byte3, byte2.	R/W
31	—	This bit is read as 0. The write value should be 0.	R

Note 1. This setting is only valid in the DOPI mode. It has no effect in the SOPI or SPI mode.

MRWCR1设置设备1的读写命令。

36.2.17 MRWCSR：内存映射读写设置寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x50

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	MWO1	MWCL1[2:0]			MWAL1[2:0]			PREN1	MRO1	MRCL1[2:0]			MRAL1[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MWO0	MWCL0[2:0]			MWAL0[2:0]			PREN0	MRO0	MRCL0[2:0]			MRAL0[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	MRAL0[2:0]	Device0读地址长度设置 设置设备0的内存映射读取地址字节长度。	R/W
5:3	MRCL0[2:0]	设备0读取命令长度设置 设置设备0的写命令字节长度。	R/W
6	MRO0	设备0读取顺序设置*1 0：读取顺序为byte0、byte1、byte2、byte3。1 ：读取顺序为byte1、byte0、byte3、byte2。	R/W
7	PREN0	mem0内存映射读取的前导位启用*2 0：无检查前导位1：检查OctaFlash的前导位（如果OctaFlash连接到设备0）	R/W
10:8	MWAL0[2:0]	Device0写地址长度设置 设置设备0的内存映射写地址字节长度。	R/W
13:11	MWCL0[2:0]	设备0写命令长度设置 设置设备0的写命令字节长度。	R/W
14	MWO0	设备0写入顺序设置*1 0：写入顺序为byte0、byte1、byte2、byte3。1 ：写入顺序为byte1、byte0、byte3、byte2。	R/W
15	—	该位读取为0。写入值应为0。	R
18:16	MRAL1[2:0]	设备1读地址长度设置 设置设备1的内存映射读取地址字节长度。	R/W
21:19	MRCL1[2:0]	设备1读取命令长度设置 设置设备1的读取命令字节长度。	R/W
22	MRO1	设备1读取顺序设置*1 0：读取顺序为byte0、byte1、byte2、byte3。1 ：读取顺序为byte1、byte0、byte3、byte2。	R/W
23	PREN1	mem1内存映射读取的前导位启用*2 0：无检查前导位1：检查OctaFlash的前导位（如果OctaFlash连接到设备1）	R/W
26:24	MWAL1[2:0]	设备1写地址长度设置 设置设备1的内存映射写地址字节长度。	R/W
29:27	MWCL1[2:0]	设备1写入命令长度设置 在设备1的写入命令中设置字节数。	R/W
30	MWO1	设备1写入顺序设置*1 0：写入顺序为byte0、byte1、byte2、byte3。1 ：写入顺序为byte1、byte0、byte3、byte2。	R/W
31	—	该位读取为0。写入值应为0。	R

注1.此设置仅在DOPI模式下有效。它在SOPI或SPI模式下无效。

Note 2. Setting this bit to 1 is prohibited, when SPI and SOPI mode.

MRWCSR sets the memory map read/write operations.

36.2.18 ESR : Error Status Register

Base address: OSPI = 0x400A_6000

Offset address: 0x54

Bit position:	31																15							8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MWESR[7:0]								MRESR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MRESR[7:0]	Memory map read error status 0x01: ECC error 0x02: Preamble error 0x03: Wait OM_DQS timeout 0x80: Invalid command Others: Reserved	R/W
15:8	MWESR[7:0]	Memory map write error status 0x80: Invalid command Others: Reserved	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

ESR indicates the error status when performing memory map read and write commands.

Note: When ESR register is read by CPU, ESR register is cleared, and the interrupt signal is cleared (if asserted).

36.2.19 CWNDR : Configure Write without Data Register

Base address: OSPI = 0x400A_6000

Offset address: 0x58

Bit position:	31																															0
Bit field:	WND[31:0]																															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	WND[31:0]	The write value should be 0.	W

CWNDR is used for write access to configure register of memory. When this register is written to, this module issues a write command without data to memory.

Specify an address in the DAR register, a command in the DCSR register, and command data in the DCR register.

36.2.20 CWDR : Configure Write Data Register

Base address: OSPI = 0x400A_6000

Offset address: 0x5C

Bit position:	31								24	23							16	15							8	7							0
Bit field:	WD3[7:0]									WD2[7:0]								WD1[7:0]								WD0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

注2.当SPI和SOPI模式时，禁止将该位设置为1。

MRWCSR设置内存映射读写操作。

36.2.18 ESR：错误状态寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x54

Bit position:	31																15							8	7							0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MWESR[7:0]								MRESR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	MRESR[7:0]	内存映射读取错误状态 0x01：ECC错误0x02：前导错误0x03：等待OM_DQS超时0 x80：无效命令 Others: Reserved	R/W
15:8	MWESR[7:0]	内存映射写入错误状态 0x80：无效命令 Others: Reserved	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

ESR指示执行内存映射读取和写入命令时的错误状态。

Note: 当CPU读取ESR寄存器时，ESR寄存器被清除，并且中断信号被清除（如果被断言）。

36.2.19 CWNDR：配置无数据寄存器写入

Base address: OSPI = 0x400A_6000

Offset address: 0x58

Bit position:	31																															0
Bit field:	WND[31:0]																															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	WND[31:0]	写入值应为0。	W

CWNDR用于对内存的配置寄存器进行写访问。当该寄存器被写入时，该模块向存储器发出一个没有数据的写入命令。

在DAR寄存器中指定地址，在DCSR寄存器中指定命令，在DCR寄存器中指定命令数据。

36.2.20 CWDR：配置写数据寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x5C

Bit position:	31								24	23							16	15							8	7							0
Bit field:	WD3[7:0]									WD2[7:0]								WD1[7:0]								WD0[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	WD0[7:0]	Write data 0 Set the zeroth byte of the write data.	W
15:8	WD1[7:0]	Write data 1 Set the first byte of the write data.	W
23:16	WD2[7:0]	Write data 2 Set the second byte of the write data.	W
31:24	WD3[7:0]	Write data 3 Set the third byte of the write data.	W

CWDR is used in writing to configure register of memory device. After this register has been written to, it holds the written value, and a write command for that value is issued to the memory device.

Specify the byte order in CDSR, a command in DCSR, an address in DAR, and command data in DCR.

36.2.21 CRR : Configure Read Register

Base address: OSPI = 0x400A_6000

Offset address: 0x60

Bit position:	31–24	23–16	15–8	7–0
Bit field:	RD3[7:0]	RD2[7:0]	RD1[7:0]	RD0[7:0]
Value after reset:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RD0[7:0]	Read data 0 Store the zeroth byte of the read data.	R
15:8	RD1[7:0]	Read data 1 Store the first byte of the read data.	R
23:16	RD2[7:0]	Read data 2 Store the second byte of the read data.	R
31:24	RD3[7:0]	Read data 3 Store the third byte of the read data.	R

CRR is used in reading from configure register of memory device.When this register is read, a read command is issued to the device and the value read from the device is stored in this register.

Change the byte order with CDSR. Specify a command in DCSR, an address in DAR, and command data in DCR.

36.2.22 ACSR : Auto-Calibration Status Register

Base address: OSPI = 0x400A_6000

Offset address: 0x64

Bit position:	31–5	4–3	2–0
Bit field:	—	ACSR1[2:0]	ACSR0[2:0]
Value after reset:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0

Bit	Symbol	Function	R/W
2:0	ACSR0[2:0]	Auto-calibration status of device 0 0 0 0: Initial state 0 0 1: Reserved 0 1 0: Reserved 0 1 1: Normal end 1 0 0: Error end*1	R/W

Bit	Symbol	Function	R/W
7:0	WD0[7:0]	写入数据0 设置写入数据的第0个字节。	W
15:8	WD1[7:0]	写入数据1 设置写入数据的第一个字节。	W
23:16	WD2[7:0]	写入数据2 设置写入数据的第二个字节。	W
31:24	WD3[7:0]	写入数据3 设置写入数据的第三个字节。	W

CWDR用于写入配置存储设备的寄存器。写入该寄存器后，它会保存写入的值，并将该值的写入命令发送到存储设备。

在CDSR中指定字节顺序，在DCSR中指定命令，在DAR中指定地址，在DCR中指定命令数据。

36.2.21 CRR：配置读取寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x60

Bit position:	31–24	23–16	15–8	7–0
Bit field:	RD3[7:0]	RD2[7:0]	RD1[7:0]	RD0[7:0]
重置后的值:	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

Bit	Symbol	Function	R/W
7:0	RD0[7:0]	读取数据0 存储读取数据的第0个字节。	R
15:8	RD1[7:0]	读取数据1 存储读取数据的第一个字节。	R
23:16	RD2[7:0]	读取数据2 存储读取数据的第二个字节。	R
31:24	RD3[7:0]	读取数据3 存储读取数据的第三个字节。	R

CRR用于从存储设备的配置寄存器中读取。读取该寄存器时，会向设备发出读取命令，并且从设备中读取的值存储在该寄存器中。

使用CDSR更改字节顺序。在DCSR中指定命令，在DAR中指定地址，在DCR中指定命令数据。

36.2.22 ACSR：自动校准状态寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x64

Bit position:	31–5	4–3	2–0
Bit field:	—	ACSR1[2:0]	ACSR0[2:0]
重置后的值:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0	0 0 0

Bit	Symbol	Function	R/W
2:0	ACSR0[2:0]	设备0的自动校准状态 000：初始状态00 1：保留010：保留 011：正常结束10 0：错误结束*1	R/W

Bit	Symbol	Function	R/W
5:3	ACSR1[2:0]	Auto-calibration status of device 1 0 0 0: Initial state 0 0 1: Reserved 0 1 0: Reserved 0 1 1: Normal end 1 0 0: Error end*1	R/W
31:6	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Read data in auto-calibration does not match with the preamble pattern.

ACSR provides the auto-calibration status until next auto-calibration.

36.2.23 DCSMXR : Device Chip Select Maximum Period Register

Base address: OSPI = 0x400A_6000

Offset address: 0x7C

Bit position:	31							24								16								8								0
Bit field:	—	—	—	—	—	—	—	CTWMX1[8:0]								—	—	—	—	—	—	—	CTWMX0[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CTWMX0[8:0]	Indicates the maximum period that OM_CS0 and OM_CS1 are Low in single continuous write of OctaRAM. Period of CTWMX0 cycle + 16 cycles in PCLKA unit to be less than t_{CSM}. For example, CTWMX0 is 0x180, when PCLKA is 100 MHz and t_{CSM} is 4.0 µs. These bits are ignored in OctaFlash.	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W
24:16	CTWMX1[8:0]	Indicates the maximum period that OM_CS0 and OM_CS1 are Low in single continuous read of OctaRAM. Period of CTWMX1 cycle + 16 cycles in PCLKA unit to be less than t_{CSM}. For example, CTWMX1 is 0x180, when PCLKA is 100 MHz and t_{CSM} is 4.0 µs. These bits are ignored in OctaFlash.	R/W
31:25	—	These bits are read as 0. The write value should be 0.	R/W

Note: Refer to OctaRAM data sheet about t_{CSM}.

DCSMXR provides the maximum period that OM_CS is Low in single continuous write/read mode of OctaRAM.

36.2.24 DWSCTSR : Device Memory Map Write single continuous translating size Register

Base address: OSPI = 0x400A_6000

Offset address: 0x80

Bit position:	31															26																16										10									0
Bit field:	—	—	—	—	—	CTSN1[10:0]																						—	—	—	—	—	CTSN0[10:0]																	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	CTSN0[10:0]	Indicates the number of bytes to translate in single continuous write of device 0. If these bits are set all 0, the translating length is undefined, the single continuous write is finished, when the period of idle is over the period to be specified by DWCSTR.CTWW0. CTSN0 must be set from 1 to 256, when PCLKA > OCTACLK/2	R/W

Bit	Symbol	Function	R/W
5:3	ACSR1[2:0]	设备1的自动校准状态 000：初始状态00 1：保留010：保留 011：正常结束10 0：错误结束*1	R/W
31:6	—	这些位被读取为0。写入值应为0。	R/W

注1.自动校准中读取的数据与前导码模式不匹配。

ACSR提供 自动校准状态，直到下一次自动校准。

36.2.23 DCSMXR:器件片选最大周期寄存器

Base address: OSPI = 0x400A_6000

Offset address: 0x7C

Bit position:	31							24								16								8								0
Bit field:	—	—	—	—	—	—	—	CTWMX1[8:0]								—	—	—	—	—	—	—	CTWMX0[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	CTWMX0[8:0]	指示在OctaRAM的单次连续写入中OM_CS0和OM_CS1为低电平的最大周期。CTWMX0周期+PCLKA单元中的16个周期的周期小于tCSM。例如， 当PCLKA为100MHz且tCSM为4.0µs时，CTWMX0为0x180。 这些位在OctaFlash中被忽略。	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W
24:16	CTWMX1[8:0]	指示OM_CS0和OM_CS1在OctaRAM的单次连续读取中为低的最大周期。CTWMX1周期+PCLKA单元中的16个周期的周期小于tCSM。例如， 当PCLKA为100MHz且tCSM为4.0µs时，CTWMX1为0x180。 这些位在OctaFlash中被忽略。	R/W
31:25	—	这些位被读取为0。写入值应为0。	R/W

Note: 请参阅有关tCSM的OctaRAM数据表。

DCSMXR提供了在OctaRAM的单次连续写入读取模式下OM_CS为低的最大周期。

36.2.24 DWSCTSR:设备内存映射写入单个连续翻译大小 Register

Base address: OSPI = 0x400A_6000

Offset address: 0x80

Bit position:	31															26																16										10									0
Bit field:	—	—	—	—	—	CTSN1[10:0]																						—	—	—	—	—	CTSN0[10:0]																	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
10:0	CTSN0[10:0]	指示在设备0的单次连续写入中要转换的字节数。 如果这些位都设置为0，则翻译长度未定义，当空闲时间超过DWCSTR.CTWW0指定的时间时，完成单次连续写入。当PCLKA>OCTACLK2时，CTSN0必须设置为1到256	R/W

Bit	Symbol	Function	R/W
15:11	—	These bits are read as 0. The write value should be 0.	R/W
26:16	CTSN1[10:0]	Indicates the number of bytes to translate in single continuous write of device 1. If these bits are set all 0, the translating length is undefined, the single continuous write is finished, when the period of idle is over the period to be specified by DWCSTR.CTWW1. CTSN1 must be set from 1 to 256, when PCLKA > OCTACLK/2	R/W
31:27	—	These bits are read as 0. The write value should be 0.	R/W

DWSCTSR provides the translating size of the single continuous write in byte. When the number of single write operations is the value to be set by DWSCTSR, the single continuous write will be finished.

36.3 Operation

36.3.1 Octa Serial Peripheral Interface System Configuration

Figure 36.2 shows an example of connections between OSPI and OctaFlash/OctaRAM.

OM_CS0 should be connected to the OctaRAM device and OM_CS1 should be connected to the OctaFlash device.

Bit	Symbol	Function	R/W
15:11	—	这些位被读取为0。写入值应为0。	R/W
26:16	CTSN1[10:0]	指示在设备1的单次连续写入中要转换的字节数。 如果这些位都设置为0，则翻译长度未定义，当空闲时间超过DWCSTR.CTWW1指定的时间时，完成单次连续写入。当PCLKA>OCTACLK2时，CTSN1必须 设置为1到256	R/W
31:27	—	这些位被读取为0。写入值应为0。	R/W

DWSCTSR以字节为单位提供单个连续写入的转换大小。当单次写操作的次数是DWSCTSR设置的值时，单次连续写就结束了。

36.3 Operation

36.3.1 Octa串行外设接口系统配置

图36.2显示了OSPI和OctaFlashOctaRAM之间的连接示例。

OM_CS0应该连接到OctaRAM设备，OM_CS1应该连接到OctaFlash设备。

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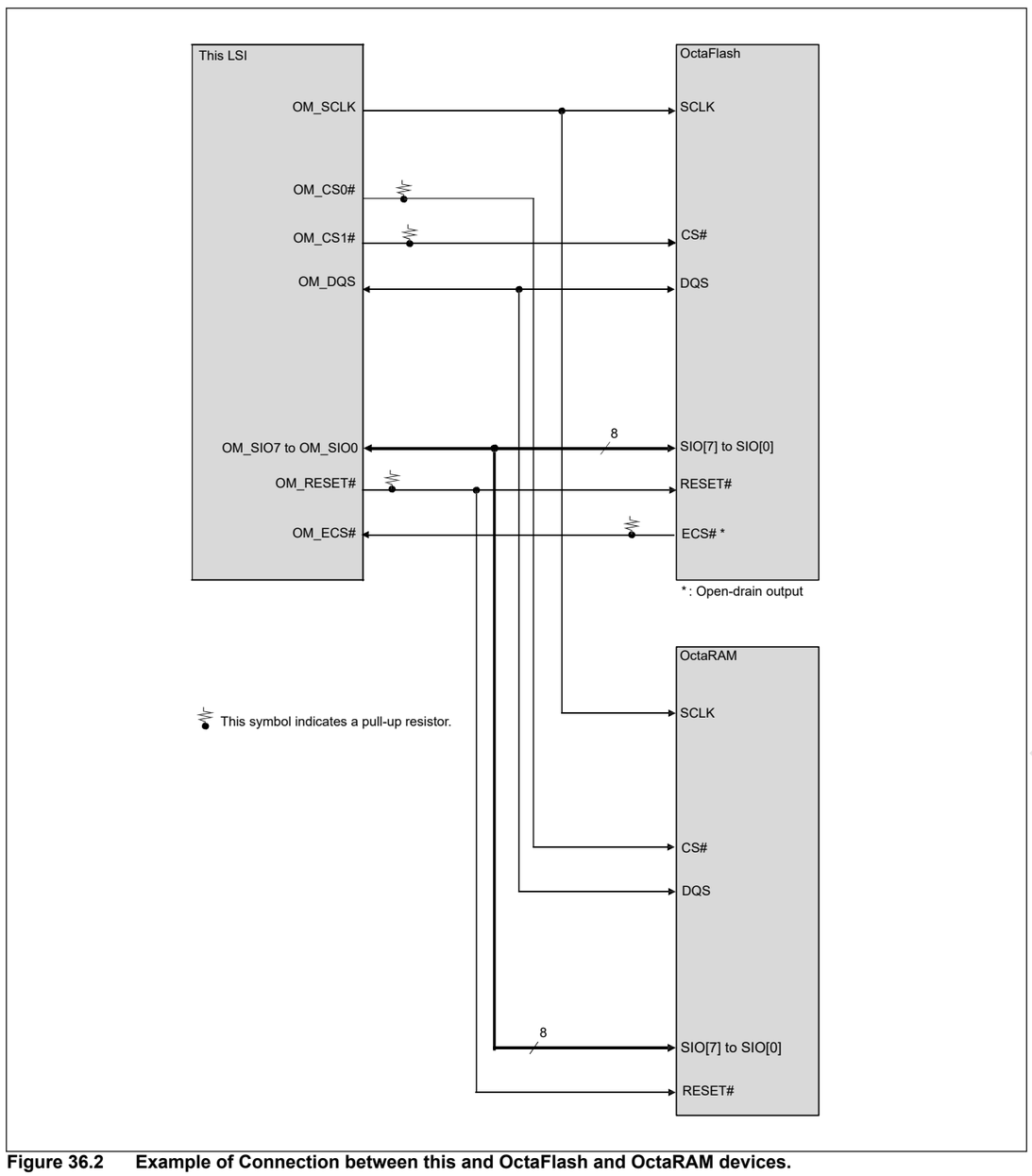


Figure 36.2 Example of Connection between this and OctaFlash and OctaRAM devices.

36.3.2 Address Map

In the memory-map read/write mode, OctaFlash is allocated to the OctaFlash space (0x7000_0000 to 0x7FFF_FFFF), and OctaRAM is allocated to the OctaRAM space (0x6800_0000 to 0x6FFF_FFFF).

One OctaFlash device and one OctaRAM device can be connected to this LSI, and up to 256 Mbytes can be accessed in OctaFlash device, and up to 128 Mbytes can be accessed in OctaRAM device.

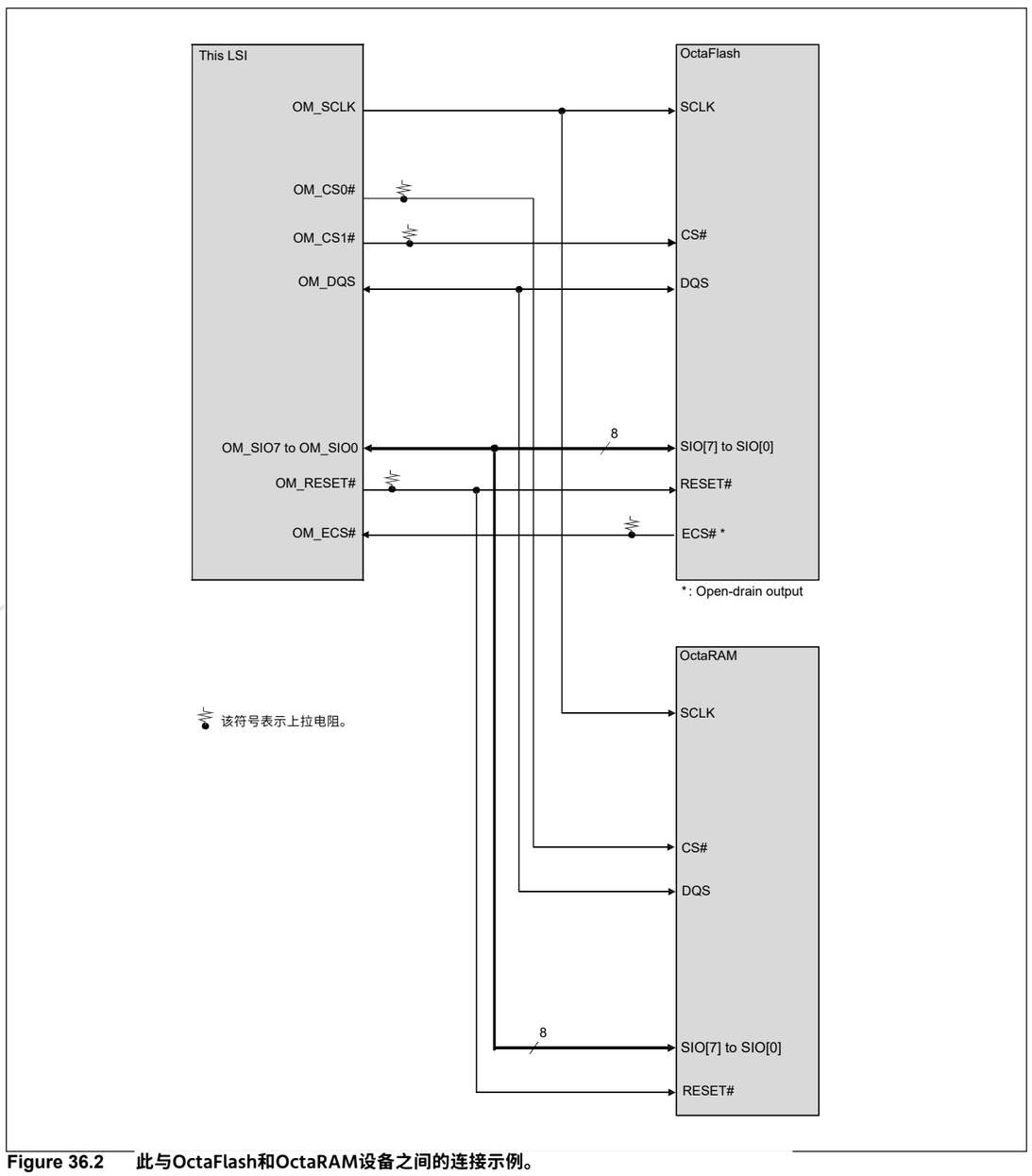


Figure 36.2 此与OctaFlash和OctaRAM设备之间的连接示例。

36.3.2 地址图

在内存映射读写模式下，OctaFlash被分配到OctaFlash空间（0x7000_0000到0x7FFF_FFFF），并且OctaRAM被分配到OctaRAM空间（0x6800_0000到0x6FFF_FFFF）。

本LSI可连接1个OctaFlash设备和1个OctaRAM设备，最多可访问256MB OctaFlash设备，最多可在OctaRAM设备中访问128MB。

RA生态工作室

	Internal Address	Maximum Accessible Area
OctaFlash	0x7000_0000 to 0x7FFF_FFFF	Up to 256 Mbytes
OctaRAM	0x6800_0000 to 0x6FFF_FFFF	Up to 128 Mbytes

36.3.3 Octa Memory Interface

This section describes the Octa memory interface.

36.3.3.1 Write Operation

The OSPI outputs a command and an address and writes one or more data bytes by using lines OM_CS0 /OM_CS1, OM_SCLK, and OM_SIO7 to OM_SIO0.

The write operation for OctaRAM has latency cycles before data is written to memory.

Figure 36.3 to Figure 36.5 show waveforms of the write operation in the OctaFlash interface, and Figure 36.6 shows a waveform of the write operation in the OctaRAM interface.

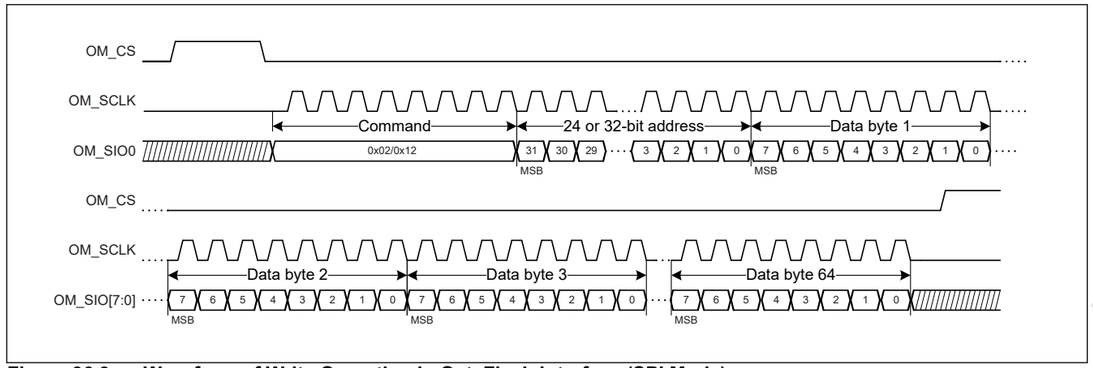


Figure 36.3 Waveform of Write Operation in OctaFlash interface (SPI Mode)

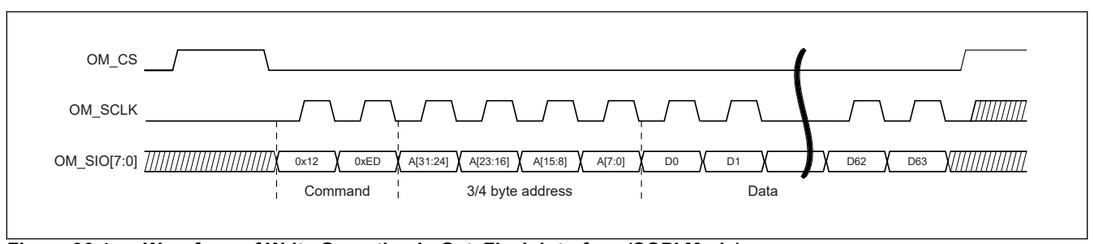


Figure 36.4 Waveform of Write Operation in OctaFlash interface (SOPI Mode)

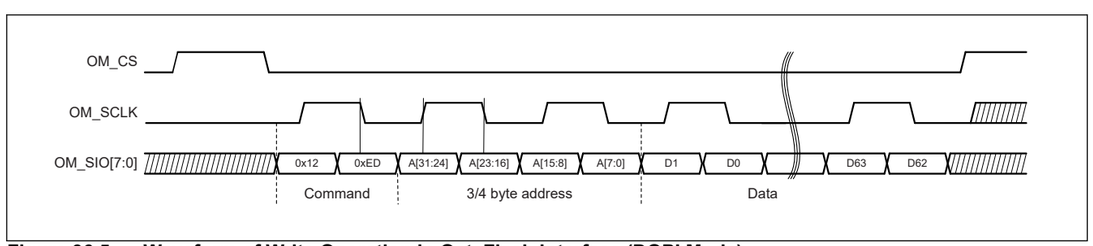


Figure 36.5 Waveform of Write Operation in OctaFlash interface (DOPI Mode)

	内部地址	最大可达面积
OctaFlash	0x7000_0000 to 0x7FFF_FFFF	高达256MB
OctaRAM	0x6800_0000 to 0x6FFF_FFFF	高达128MB

36.3.3 八进制存储器接口

本节介绍Octa存储器接口。

36.3.3.1 写操作

OSPI通过使用线OM_CS0OM_CS1输出命令和地址并写入一个或多个数据字节，
OM_SCLK和OM_SIO7到OM_SIO0。

OctaRAM的写操作在数据写入内存之前有延迟周期。

图36.3至图36.5为OctaFlash接口的写操作波形，图36.6为OctaRAM接口的写操作波形。

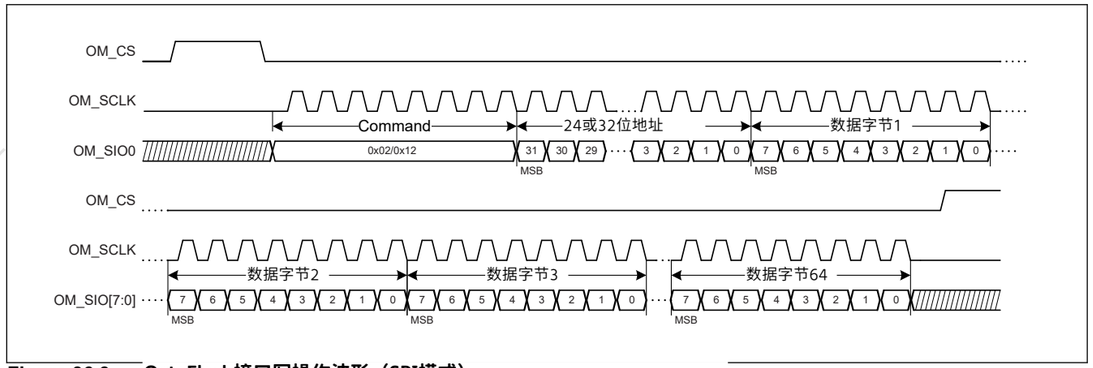


Figure 36.3 OctaFlash接口写操作波形（SPI模式）

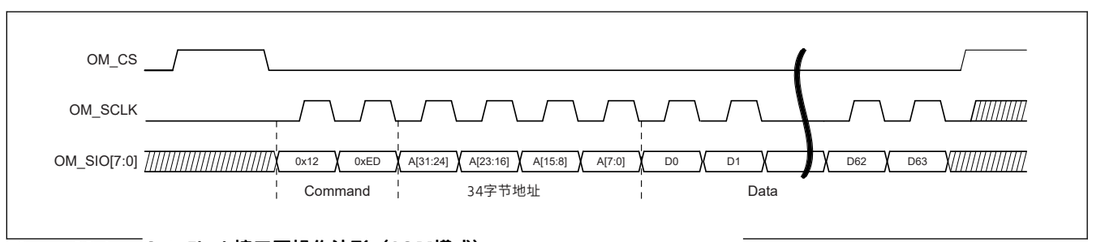


Figure 36.4 OctaFlash接口写操作波形（SOPI模式）

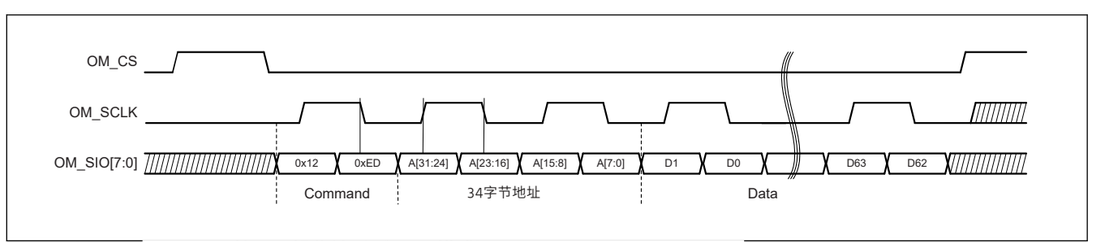


Figure 36.5 OctaFlash接口写操作波形（DOPI模式）

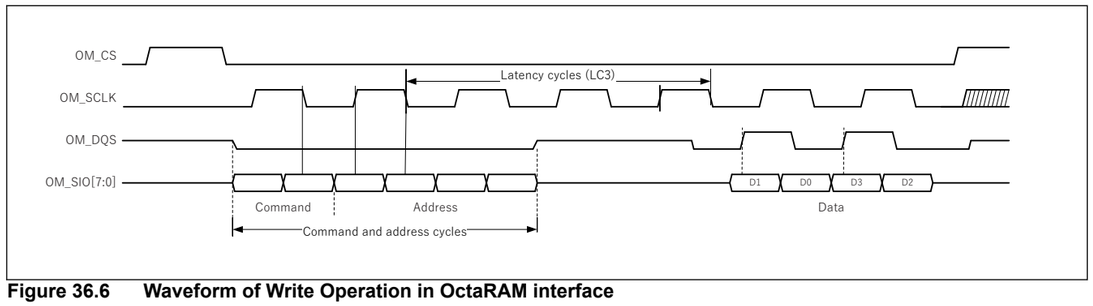


Figure 36.6 Waveform of Write Operation in OctaRAM interface

36.3.3.2 Read Operation

The OSPI outputs a command and an address and reads one or more data bytes by using lines OM_CS0 /OM_CS1, OM_SCLK, and OM_SIO7 to OM_SIO0.

The read operation for OctaFlash and OctaRAM has latency cycles before data is read from memory.

The number of latency cycles should be specified in the memory map dummy length setting register (MDLR) (See section 36.2.14. MDLR : Memory Map Dummy Length Register) in accordance with the setting in the memory device.

In SOPI or DOPI mode, OM_DQS is used. Automatic calibration should be executed before first read OctaFlash or OctaRAM in SOPI or DOPI mode.

Figure 36.7 to Figure 36.9 show waveforms of the read operation in the OctaFlash interface, and Figure 36.10 shows a waveform of the read operation in the OctaRAM interface.

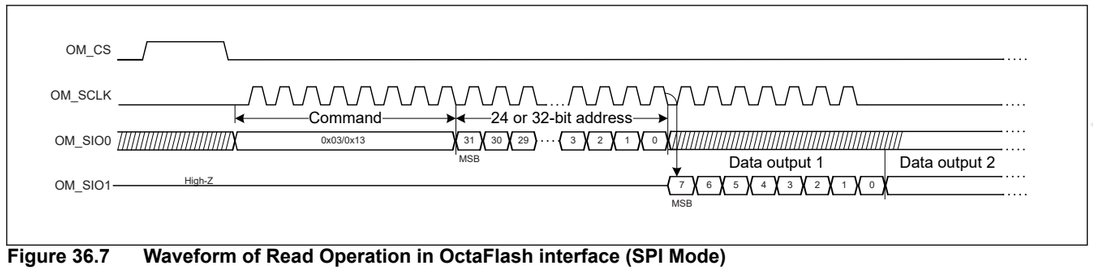


Figure 36.7 Waveform of Read Operation in OctaFlash interface (SPI Mode)

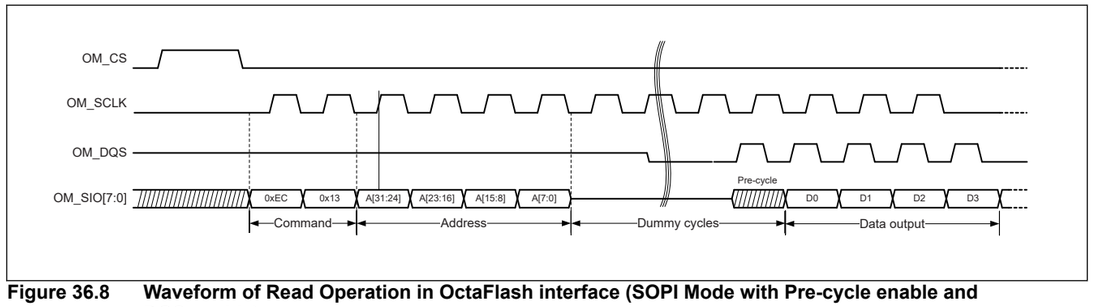


Figure 36.8 Waveform of Read Operation in OctaFlash interface (SOPI Mode with Pre-cycle enable and DQS enable)

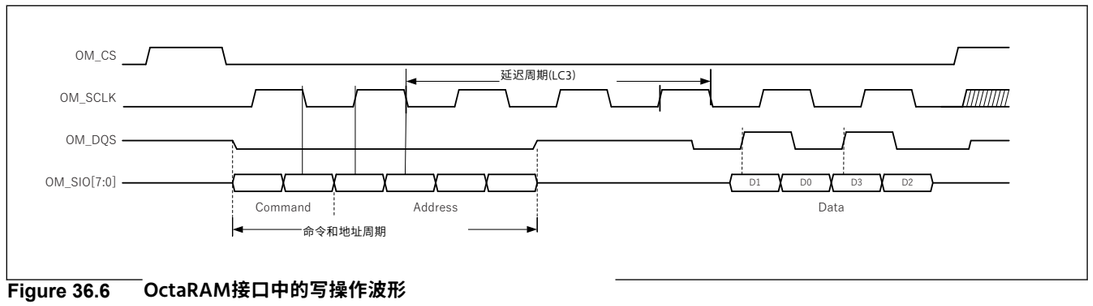


Figure 36.6 OctaRAM接口中的写操作波形

36.3.3.2 读操作

OSPI输出命令和地址，并通过使用线OM_CS0OM_CS1读取一个或多个数据字节，
OM_SCLK和OM_SIO7到OM_SIO0。

OctaFlash和OctaRAM的读取操作在从内存读取数据之前有延迟周期。

延迟周期数应根据存储器设备中的设置在存储器映射虚拟长度设置寄存器(MDLR)中指定（参见第36.2.14节。MDLR：存储器映射虚拟长度寄存器）。

在SOPI或DOPI模式下，使用OM_DQS。自动校准应在首次读取OctaFlash或
在SOPI或DOPI模式下的OctaRAM。

OctaFlash接口的读操作波形如图36.7至图36.9所示，OctaRAM接口的读操作波形如图36.10所示。

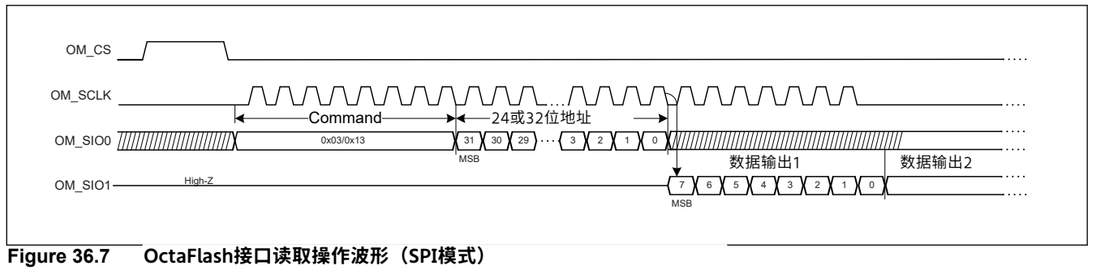


Figure 36.7 OctaFlash接口读取操作波形（SPI模式）

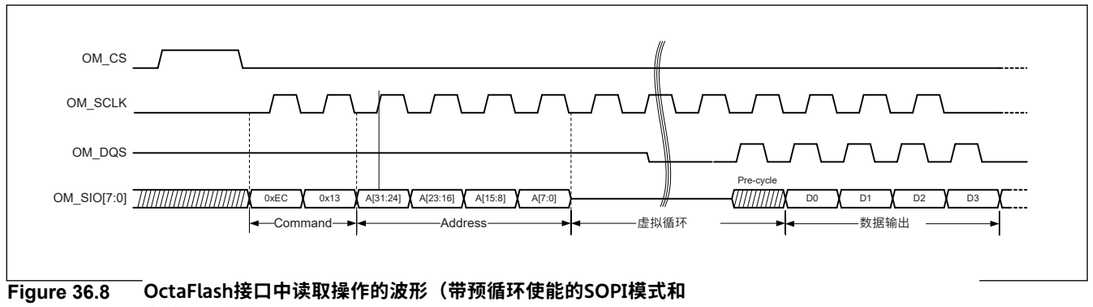


Figure 36.8 OctaFlash接口中读取操作的波形（带预循环使能的SOPI模式和DQS enable）

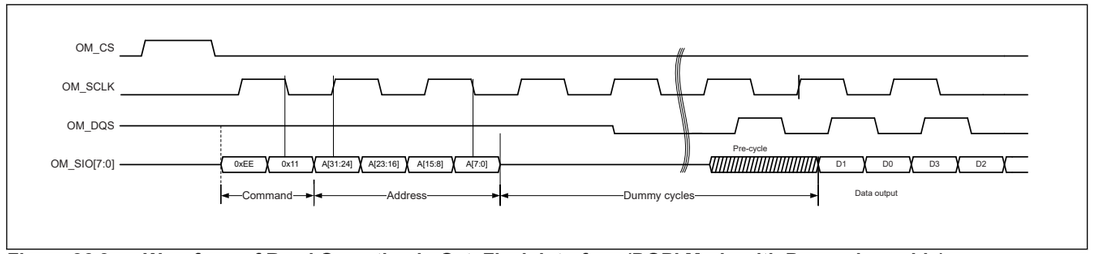


Figure 36.9 Waveform of Read Operation in OctaFlash interface (DOPI Mode with Pre-cycle enable)

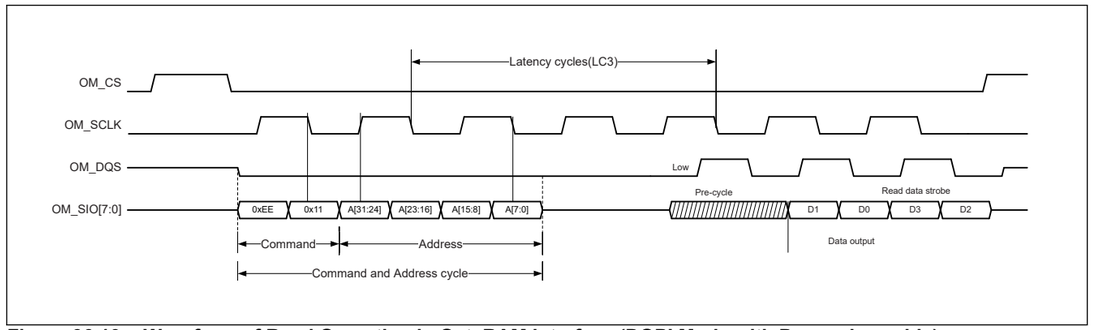


Figure 36.10 Waveform of Read Operation in OctaRAM interface (DOPI Mode with Pre-cycle enable)

36.3.4 Data Alignment in the OctaFlash and OctaRAMSpaces

Figure 36.11 shows the memory data alignment in the OctaFlash and OctaRAM spaces.

Figure 36.12 shows the data alignment when the configuration register in OctaFlash or OctaRAM is accessed.

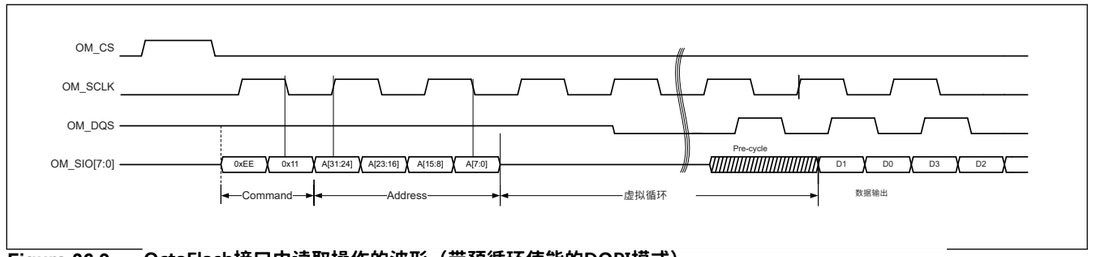


Figure 36.9 OctaFlash接口中读取操作的波形（带预循环使能的DOPI模式）

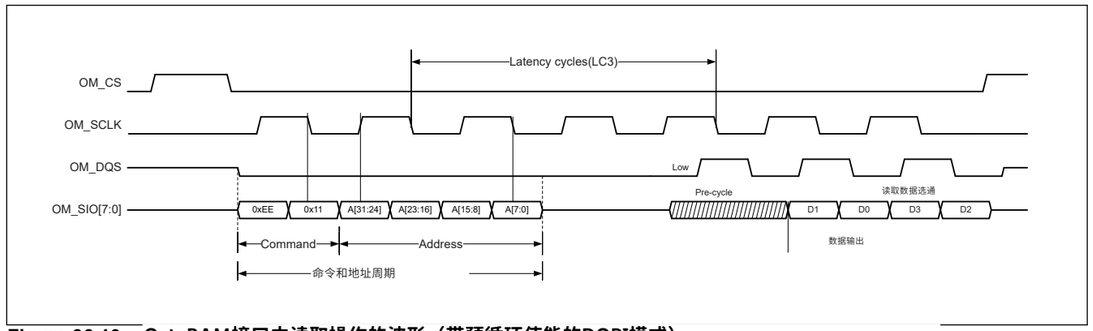


Figure 36.10 OctaRAM接口中读取操作的波形（带预循环使能的DOPI模式）

36.3.4 OctaFlash和OctaRAMSpaces中的数据对齐

图36.11显示了OctaFlash和OctaRAM空间中的存储器数据对齐。

图36.12显示了访问OctaFlash或OctaRAM中的配置寄存器时的数据对齐方式。

When OctaFlash is connected (MRWCSR.MWO0 = 0, MRWCSR.MRO0 = 0) or OctaRAM is connected (MRWCSR.MWO1 = 0, MRWCSR.MRO1 = 0)

Flash/RAM 8-bit DDR	Access width	Address	Internal bus 63 56 55 48 47 40 39 32 31 24 23 16 15 8 7 0
0 D0[7:0]	1 byte	b'000	X X X X X X X D0
1 D1[7:0]		b'001	X X X X X X D1 X
2 D2[7:0]		b'010	X X X X X D2 X X
3 D3[7:0]		b'011	X X X X D3 X X X
4 D4[7:0]		b'100	X X X D4 X X X X
5 D5[7:0]		b'101	X X D5 X X X X X
6 D6[7:0]		b'110	X D6 X X X X X X
7 D7[7:0]		b'111	D7 X X X X X X X
OM_SIO[7:0]	2 bytes	b'000	X X X X X X D1 D0
		b'010	X X X X D3 D2 X X
		b'100	X X D5 D4 X X X X
		b'110	D7 D6 X X X X X X
	4 bytes	b'000	X X X X D3 D2 D1 D0
		b'100	D7 D6 D5 D4 X X X X
	8 bytes	b'000	D7 D6 D5 D4 D3 D2 D1 D0

When OctaFlash is connected (MRWCSR.MWO0 = 1, MRWCSR.MRO0 = 1) or OctaRAM is connected (MRWCSR.MWO1 = 1, MRWCSR.MRO1 = 1)

Flash/RAM 8bit DDR	Access width	Address	Internal bus 63 56 55 48 47 40 39 32 31 24 23 16 15 8 7 0
0 D0[7:0]	1 byte	b'000	X X X X X X X D1
1 D1[7:0]		b'001	X X X X X X D0 X
2 D2[7:0]		b'010	X X X X X D3 X X
3 D3[7:0]		b'011	X X X X D2 X X X
4 D4[7:0]		b'100	X X X D5 X X X X
5 D5[7:0]		b'101	X X D4 X X X X X
6 D6[7:0]		b'110	X D7 X X X X X X
7 D7[7:0]		b'111	D6 X X X X X X X
OM_SIO[7:0]	2 bytes	b'000	X X X X X X D0 D1
		b'010	X X X X D2 D3 X X
		b'100	X X D4 D5 X X X X
		b'110	D6 D7 X X X X X X
	4 bytes	b'000	X X X X D2 D3 D0 D1
		b'100	D6 D7 D4 D5 X X X X
	8 bytes	b'000	D6 D7 D4 D5 D2 D3 D0 D1

Figure 36.11 Memory Data Alignment in the OctaFlash and OctaRAM Spaces

当OctaFlash连接时(MRWCSR.MWO0=0 MRWCSR.MRO0=0)或OctaRAM已连接（MRWCSR.MWO1=0，MRWCSR.MRO1=0）

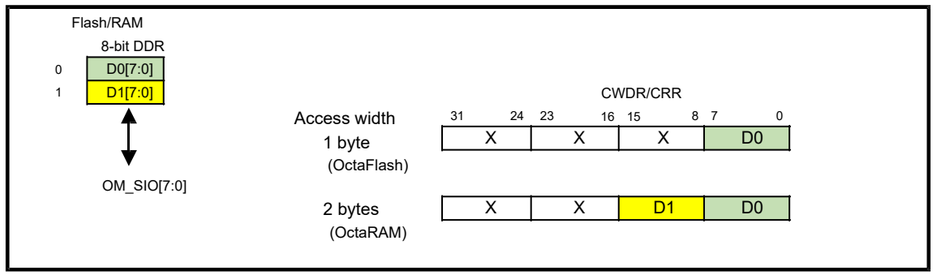
Flash/RAM 8-bit DDR	存取宽度	Address	内部总线 63 56 55 48 47 40 39 32 31 24 23 16 15 8 7 0
0 D0[7:0]	1 byte	b'000	X X X X X X X D0
1 D1[7:0]		b'001	X X X X X X D1 X
2 D2[7:0]		b'010	X X X X X D2 X X
3 D3[7:0]		b'011	X X X X D3 X X X
4 D4[7:0]		b'100	X X X D4 X X X X
5 D5[7:0]		b'101	X X D5 X X X X X
6 D6[7:0]		b'110	X D6 X X X X X X
7 D7[7:0]		b'111	D7 X X X X X X X
OM_SIO[7:0]	2 bytes	b'000	X X X X X X D1 D0
		b'010	X X X X D3 D2 X X
		b'100	X X D5 D4 X X X X
		b'110	D7 D6 X X X X X X
	4 bytes	b'000	X X X X D3 D2 D1 D0
		b'100	D7 D6 D5 D4 X X X X
	8 bytes	b'000	D7 D6 D5 D4 D3 D2 D1 D0

当OctaFlash连接时(MRWCSR.MWO0=1 MRWCSR.MRO0=1)或OctaRAM已连接（MRWCSR.MWO1=1，MRWCSR.MRO1=1）

Flash/RAM 8bit DDR	存取宽度	Address	内部总线 63 56 55 48 47 40 39 32 31 24 23 16 15 8 7 0
0 D0[7:0]	1 byte	b'000	X X X X X X X D1
1 D1[7:0]		b'001	X X X X X X D0 X
2 D2[7:0]		b'010	X X X X X D3 X X
3 D3[7:0]		b'011	X X X X D2 X X X
4 D4[7:0]		b'100	X X X D5 X X X X
5 D5[7:0]		b'101	X X D4 X X X X X
6 D6[7:0]		b'110	X D7 X X X X X X
7 D7[7:0]		b'111	D6 X X X X X X X
OM_SIO[7:0]	2 bytes	b'000	X X X X X X D0 D1
		b'010	X X X X D2 D3 X X
		b'100	X X D4 D5 X X X X
		b'110	D6 D7 X X X X X X
	4 bytes	b'000	X X X X D2 D3 D0 D1
		b'100	D6 D7 D4 D5 X X X X
	8 bytes	b'000	D6 D7 D4 D5 D2 D3 D0 D1

Figure 36.11 OctaFlash和OctaRAM空间中的内存数据对齐

When OctaFlash is connected (DCSR.DAOR = 0),
OctaRAM is connected (DCSR.DAOR = 0), or
OctaFlash/OctaRAM is connected



When OctaFlash is connected (DCSR.DAOR = 1),
OctaRAM is connected (DCSR.DAOR = 1), or
OctaFlash/OctaRAM is connected

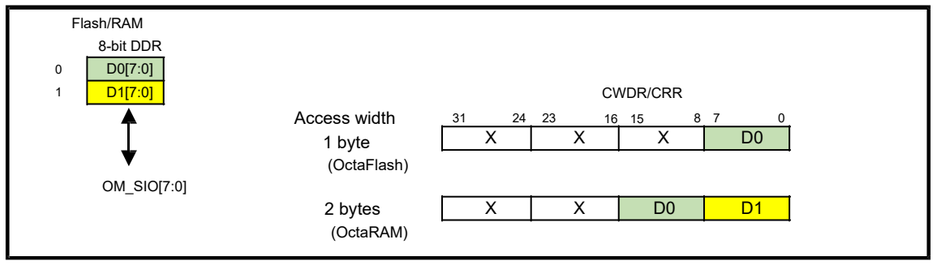


Figure 36.12 Configuration Register Data Alignment in the OctaFlash and OctaRAM Spaces

36.3.5 Byte Mask

This section describes the byte mask function. This function is only available for OctaRAM devices. The OSPI outputs the OM_DQS signal as a write data mask signal during write operation. Write data is masked with the OM_DQS signal driven high. Figure 36.13 shows a waveform of the write operation with the byte mask function enabled.

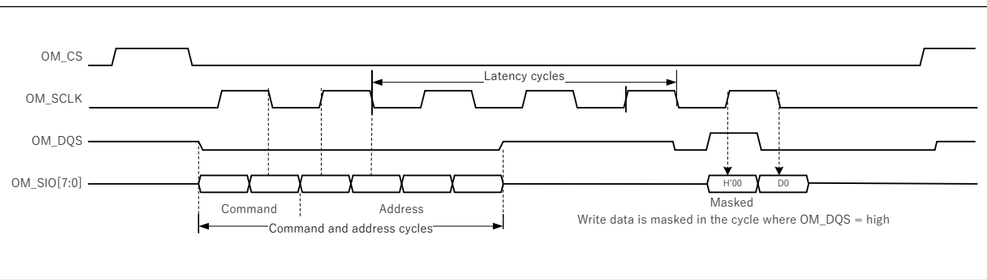


Figure 36.13 Waveform of Write Operation with Byte Mask Enabled

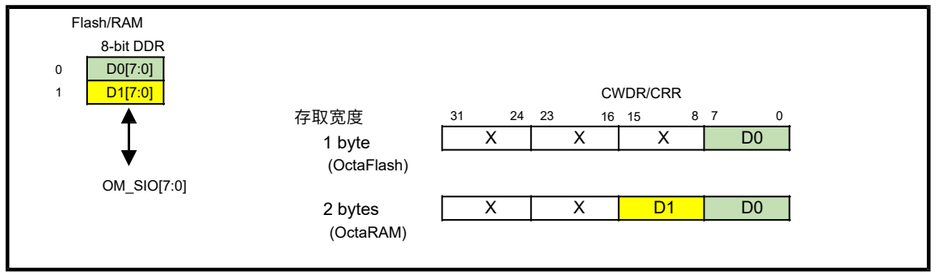
36.3.6 Operation Flows

This section describes the flows of OSPI operations for various purposes.

The following only shows sample settings, and appropriate commands and data should be specified in accordance with the specifications of the target memory device.

The sample settings assume the following environment:

当OctaFlash连接时（DCSR.DAOR=0），
OctaRAM已连接(DCSR.DAOR=0)，或
OctaFlashOctaRAM已连接



当OctaFlash连接时（DCSR.DAOR=1），
OctaRAM已连接(DCSR.DAOR=1)，或
OctaFlashOctaRAM已连接

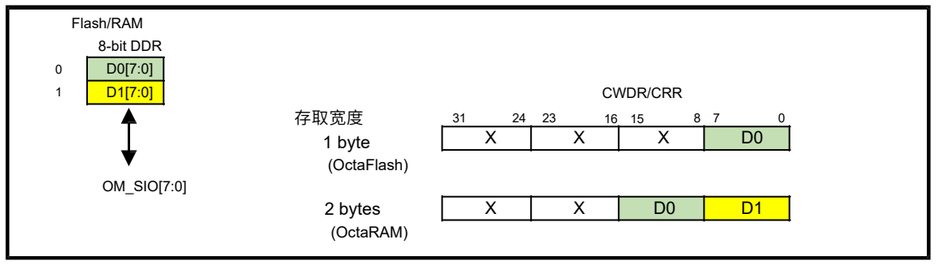


Figure 36.12 OctaFlash和OctaRAM空间中的配置寄存器数据对齐

36.3.5 字节掩码

本节介绍字节掩码功能。此功能仅适用于OctaRAM设备。OSPI在写操作期间输出OM_DQS信号作为写数据屏蔽信号。写入数据被OM_DQS信号驱动为高电平屏蔽。图36.13显示了启用字节掩码功能的写操作波形。

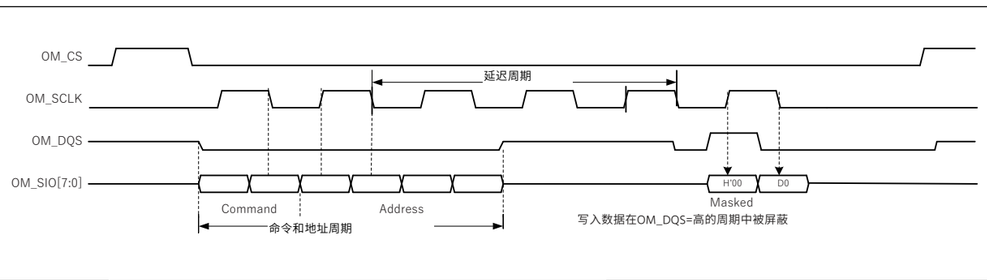


Figure 36.13 启用字节掩码的写操作波形

36.3.6 操作流程

本节描述了用于各种目的的OSPI操作流程。

以下仅显示示例设置，应根据目标存储设备的规格指定适当的命令和数据。

示例设置假定以下环境：

1. Memory connections: OM_CS0 (device 0) to OctaRAM and OM_CS1 (device 1) to OctaFlash
2. OM_SCLK (Octa memory clock) frequency: 100 MHz

36.3.6.1 Initial Settings

Table 36.6 shows an example of initial settings of the OSPI registers.

Table 36.6 Example of initial settings of the OSPI registers

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	DSR0	0x40800000	4	Specifies the type and size of device 0 The device 0 connects 128 Mbit OctaRAM
2	Write	DSR1	0x08000000	4	Specifies the type and size of device 1 The device 1 connects 1 Gbit OctaFlash
3	Write	MDTR	0x0640A440	4	Adjusts the memory access timing
4	Write	DRCSTR	0x69206920	4	Specifies the read timing for each device
5	Write	DWCSTR	0x41204120	4	Specifies the write timing for each device
6	Write	DCSTR	0x00006A00	4	Specifies the timing of the chip select signals
7	Write	CDSR	0x80000002	4	Sets up the controller functions 1. Auto-calibration is disabled 2. Memory pre-cycle is disabled 3. Transfer type set SPI mode for OctaFlash (devide 1) and DOPI mode for OctaRAM (device 0)
8	Write	MDLR	0x000E0505	4	Specifies the dummy length
9	Write	MRWCR0	0x2000A000	4	Specifies the read and write commands for device 0 Write command: WRCONT of OctaRAM Read command: RDCONT of OctaRAM
10	Write	MRWCR1	0x12EDEE11	4	Specifies the read and write commands for device 1 Write command: PP of OctaFlash Read command: 8DTRD of OctaFlash
11	Write	MRWCSR	0x54545454	4	Sets up the memory-mapped reading and writing 1. The length (bytes) of a command is specified 2. The length (bytes) of an address is specified 3. The order of bytes to be written is specified

36.3.6.2 Basic Operation Settings

This section describes the basic operations of OctaFlash and OctaRAM.

The following only shows sample settings, and appropriate commands and data should be specified in accordance with the specifications of the target memory device.

(1) OctaFlash Operation Settings

Table 36.7 1. Write Enable Settings

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	Any value	4	Any value	4	—

Table 36.8 2. Read Status Register (1 of 2)

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	0x00000005	4	0x000005FA	4	—

1.内存连接：OM_CS0（设备0）到OctaRAM和OM_CS1（设备1）到OctaFlash
2. OM_SCLK (Octa memory clock) frequency: 100 MHz

36.3.6.1 初始设置

表36.6显示了OSPI寄存器的初始设置示例。

Table 36.6 OSPI寄存器的初始设置示例

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	DSR0	0x40800000	4	指定设备0的类型和大小 设备0连接128MbitOctaRAM
2	Write	DSR1	0x08000000	4	指定设备1的类型和大小 设备1连接1GbitOctaFlash
3	Write	MDTR	0x0640A440	4	调整内存访问时间
4	Write	DRCSTR	0x69206920	4	指定每个设备的读取时序
5	Write	DWCSTR	0x41204120	4	指定每个设备的写入时序
6	Write	DCSTR	0x00006A00	4	指定片选信号的时序
7	Write	CDSR	0x80000002	4	设置控制器功能1.禁用自动校准2.禁用内存预循环3.传输类型设置OctaFlash（设备1）的SPI模式和OctaRAM（设备0）的DOPI模式
8	Write	MDLR	0x000E0505	4	指定虚拟长度
9	Write	MRWCR0	0x2000A000	4	指定设备0的读取和写入命令 写命令：OctaRAM的WRCONT读命令： OctaRAM的RDCONT
10	Write	MRWCR1	0x12EDEE11	4	指定设备1的读取和写入命令 写指令：OctaFlash的PP 读取指令：OctaFlash的8DTRD
11	Write	MRWCSR	0x54545454	4	设置内存映射读写1.指定命令的长度（字节）2.指定地址的长度（字节）3.指定要写入的字节顺序

36.3.6.2 基本操作设置

本节介绍OctaFlash和OctaRAM的基本操作。

以下仅显示示例设置，应根据目标存储设备的规格指定适当的命令和数据。

(1) OctaFlash操作设置

Table 36.7 1.写使能设置

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	任何值	4	任何值	4	—

Table 36.8 2.读取状态寄存器(1of2)

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	0x00000005	4	0x000005FA	4	—

Table 36.8 2. Read Status Register (2 of 2)

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
2	Write	DAR	—	—	0x00000000	4	—
3	Write	DCSR	0x00180001	4	0x0C280401	4	—
4	Read	CRR	0x000000xx	4	0x000000xx	1	The high-order 24 bits are all set to 0s, and the read data is stored in the low-order eight bits.

Table 36.9 3. Read Configuration Register

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	0x00000015	4	0x000015EA	4	—
2	Write	DAR	—	—	0x00000001	4	—
3	Write	DCSR	0x00180001	4	0x0C280401	4	—
4	Read	CRR	0x000000xx	1	0x000000xx	1	The high-order 24 bits are all set to 0s, and the read data is stored in the low-order eight bits.

Table 36.10 4. Write Configuration Register

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	—	—	0x000001FE	4	—
2	Write	DAR	—	—	0x00000001	4	—
3	Write	DCSR	—	—	0x04280001	4	—
4	Write	CWDR	—	—	0x000000xx	1	Set all the high-order 24 bits to 0 and specify the write data in the low-order eight bits.

Note: It is necessary to execute Write Enable instruction before modifying Write Configuration Register and then Write Configuration Register will be set after tW (tW is Write Status/Configuration Register Cycle Time, refer to OctaFlash data sheet).

Table 36.11 5. Read Configuration Register 2

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	0x00000071	4	0x0000718E	4	—
2	Write	DAR	Address	4	Address	4	—
3	Write	DCSR	0x04180001	4	0x0C280401	4	—
4	Read	CRR	0x000000xx	1	0x000000xx	1	The high-order 24 bits are all set to 0s, and the read data is stored in the low-order eight bits.

Table 36.12 6. Write Configuration Register 2

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	0x00000072	4	0x0000728D	4	—
2	Write	DAR	Address	4	Address	4	—
3	Write	DCSR	0x04180001	4	0x04280001	4	—
4	Write	CWDR	0x000000xx	1	0x000000xx	1	Set all the high-order 24 bits to 0s, and specify the write data in the low-order eight bits

Note: It is necessary to execute Write Enable instruction before modifying Write Configuration Register2.

Table 36.8 2.读取状态寄存器(2of2)

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
2	Write	DAR	—	—	0x00000000	4	—
3	Write	DCSR	0x00180001	4	0x0C280401	4	—
4	Read	CRR	0x000000xx	4	0x000000xx	1	高24位全部置0，读取的数据存放在低8位。

Table 36.9 3.读取配置寄存器

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	0x00000015	4	0x000015EA	4	—
2	Write	DAR	—	—	0x00000001	4	—
3	Write	DCSR	0x00180001	4	0x0C280401	4	—
4	Read	CRR	0x000000xx	1	0x000000xx	1	高24位全部置0，读取的数据存放在低8位。

Table 36.10 4.写配置寄存器

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	—	—	0x000001FE	4	—
2	Write	DAR	—	—	0x00000001	4	—
3	Write	DCSR	—	—	0x04280001	4	—
4	Write	CWDR	—	—	0x000000xx	1	将所有高24位设置为0，并在低8位中指定写入数据。

Note: 在修改WriteConfigurationRegister和WriteConfiguration之前需要执行WriteEnable指令寄存器将在tW之后设置（tW是写状态配置寄存器周期时间，请参阅OctaFlash数据手册）。

Table 36.11 5.读取配置寄存器2

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	0x00000071	4	0x0000718E	4	—
2	Write	DAR	Address	4	Address	4	—
3	Write	DCSR	0x04180001	4	0x0C280401	4	—
4	Read	CRR	0x000000xx	1	0x000000xx	1	高24位全部置0，读取的数据存放在低8位。

Table 36.12 6.写配置寄存器2

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	0x00000072	4	0x0000728D	4	—
2	Write	DAR	Address	4	Address	4	—
3	Write	DCSR	0x04180001	4	0x04280001	4	—
4	Write	CWDR	0x000000xx	1	0x000000xx	1	将高24位全部置0，低8位指定写入数据

Note: 在修改写配置寄存器2之前需要执行写使能指令。

RA生态工作室

Table 36.13 7. Erase Sector

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
1	Write	DCR	0x00000021	4	0x000021DE	4	—
2	Write	DAR	Address to be erased	4	Address to be erased	4	—
3	Write	DCSR	0x04180000	4	0x04280000	4	—
4	Write	CWNDR	Any value	4	Any value	4	—

Note: Refer to section 36.3.6.5. Program/Erase of OctaFlash Setting about the sequence of erase.

(2) OctaRAM Operation Settings

Table 36.14 1. Read Configuration Register

Step	Read/ Write	Register	Data	Data Length (Bytes)	Description
1	Write	DCR	0x0000C000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00502	4	—
4	Read	CRR	0x0000xxxx	2	The high-order 16 bits are all set to 0s, and the read data is stored in the low-order 16 bits.

Table 36.15 2. Write Configuration Register

Step	Read/ Write	Register	Data	Data Length (Bytes)	Description
1	Write	DCR	0x00004000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00002	4	—
4	Write	CWDR	0x0000xxxx	2	Set all the high-order 16 bits to 0 and specify the write data in the low-order 16 bits.

36.3.6.3 Modify Settings

If OctaFlash/RAM is operating in the different condition (not default condition), the Config Registers of OctaFlash/RAM and the memory controller must be modified after the initial setting.

(1) Set translate mode

When the translating mode uses whether DOPI, SOPI, or SPI mode in OctaFlash, it is necessary to modify the setting of the Config Register of OctaFlash and memory-controller. Refer to the data sheet of OctaFlash about how to set transfer type. For example, show the sequence to change transfer type in OctaFlash to Table 36.16. When the transfer type is changed from current transfer type, users issue WREN (Write Enable) instruction, successively issue WRCR2 instruction to modify the values of Configuration Register 2 in OctaFlash to change translating mode.

Table 36.16 Example of translating mode setting of OctaFlash (1 of 2)

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
Write Enable (WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	Any value	4	Any value	4	—

Table 36.13 7.擦除扇区

Step	Read/ Write	Register	SPI模式数据	数据长度（字节）	OPI模式数据	数据长度（字节）	Description
1	Write	DCR	0x00000021	4	0x000021DE	4	—
2	Write	DAR	要删除的地址	4	要删除的地址	4	—
3	Write	DCSR	0x04180000	4	0x04280000	4	—
4	Write	CWNDR	任何值	4	任何值	4	—

Note: 请参阅第36.3.6.5节。ProgramEraseofOctaFlash设置擦除的顺序。

(2) OctaRAM操作设置

Table 36.14 1.读取配置寄存器

Step	Read/ Write	Register	Data	Data Length (Bytes)	Description
1	Write	DCR	0x0000C000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00502	4	—
4	Read	CRR	0x0000xxxx	2	高16位全部置0，读取的数据存放在低16位。

Table 36.15 2.写配置寄存器

Step	Read/ Write	Register	Data	Data Length (Bytes)	Description
1	Write	DCR	0x00004000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00002	4	—
4	Write	CWDR	0x0000xxxx	2	将所有高16位设置为0，并在低16位中指定写入数据。

36.3.6.3 修改设置

如果OctaFlashRAM在不同的条件下运行（不是默认条件），则必须在初始设置后修改OctaFlashRAM和内存控制器的配置寄存器。

(1) 设置翻译模式

在OctaFlash中翻译模式使用DOPI、SOPI或SPI模式时，需要修改OctaFlash和内存控制器的配置寄存器。关于如何设置传输类型，请参考OctaFlash的数据手册。
例如，将OctaFlash中的传输类型更改为表36.16的顺序。当传输类型从当前传输类型改变时，用户发出WREN（WriteEnable）指令，依次发出WRCR2指令修改OctaFlash中配置寄存器2的值来改变翻译模式。

Table 36.16 OctaFlash翻译模式设置示例(1of2)

Step	Read/ Write	Register	SPI模式数据	Data Length (Bytes)	OPI模式数据	Data Length (Bytes)	Description
写使能(WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	任何值	4	任何值	4	—

Table 36.16 Example of translating mode setting of OctaFlash (2 of 2)

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
Write Configuration Register2 (WRCR2)							
4	Write	DCR	0x00000072	4	0x0000728D	4	—
5	Write	DAR	0x00000000	4	0x00000000	4	—
6	Write	DCSR	0x04180001	4	0x04280001	4	—
7	Write	CWDR	0x00000001	1	0x00000001	1	in the case of SOPI mode
7	Write	CWDR	0x00000002	1	0x00000002	1	in the case of DOPI mode

The Config Register setting of the memory-controller in DOPI mode specifies to Table 36.17, the setting of SOPI mode specifies to Table 36.18, and the setting of SPI mode specifies to Table 36.19.

Table 36.17 Example of translating mode setting (DOPI mode)

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	CDSR	0x80001C0A	4	Sets up the controller functions Auto-calibration is enabled Memory pre-cycle is disabled Transfer type of OctaFlash and OctaRAM set DOPI mode
2	Write	MRWCR1	0x12EDEE11	4	Specifies the read and write commands for OctaFlash Write command: PP of OctaFlash Read command: 8DTRD of OctaFlash

Table 36.18 Example of translating mode setting (SOPI mode)

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	CDSR	0x80001C06	4	Sets up the controller functions Auto-calibration is enabled Memory pre-cycle is disabled Transfer type of OctaFlash set SOPI mode, and OctaRAM set DOPI mode
2	Write	MRWCR1	0x12EDEC13	4	Specifies the read and write commands for OctaFlash Write command: PP of OctaFlash Read command: 8READ of OctaFlash

Table 36.19 Example of translating mode setting (SPI mode)

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	CDSR	0x80000004	4	Sets up the controller functions Auto-calibration is disabled Memory pre-cycle is disabled Transfer type of OctaFlash set SPI mode, and OctaRAM set DOPI mode
2	Write	MRWCR1	0x00120013	4	Specifies the read and write commands for OctaFlash Write command: PP of OctaFlash Read command: 8READ of OctaFlash

Note: OctaFlash connects the device 1, and OctaRAM connects the device 0.

(2) Set pre-cycle is enabled

When pre-cycle is enabled in OctaFlash/RAM, it is necessary to modify the setting of the Config Register of OctaFlash/RAM and memory-controller. Refer to the data sheet of OctaFlash/RAM about how to be enabled pre-cycle. For

Table 36.16 OctaFlash翻译模式设置示例(2of2)

Step	Read/ Write	Register	SPI模式数据	Data Length (Bytes)	OPI模式数据	Data Length (Bytes)	Description
写配置寄存器2(WRCR2)							
4	Write	DCR	0x00000072	4	0x0000728D	4	—
5	Write	DAR	0x00000000	4	0x00000000	4	—
6	Write	DCSR	0x04180001	4	0x04280001	4	—
7	Write	CWDR	0x00000001	1	0x00000001	1	在SOPI模式的情况下
7	Write	CWDR	0x00000002	1	0x00000002	1	在DOPI模式的情况下

DOPI模式下内存控制器的配置寄存器设置见表36.17，SOPI模式设置见表36.18，SPI模式设置见表36.19。

Table 36.17 翻译模式设置示例（DOPI模式）

Step	Read/ Write	Address (Register)	Data	数据长度（字节）	Description
1	Write	CDSR	0x80001C0A	4	设置控制器功能 启用自动校准 内存预循环被禁用 OctaFlash和OctaRAM组的传输类型 DOPI mode
2	Write	MRWCR1	0x12EDEE11	4	指定读取和写入命令 OctaFlash 写指令：OctaFlash的PP 读取指令：OctaFlash的8DTRD

Table 36.18 翻译模式设置示例（SOPI模式）

Step	Read/ Write	Address (Register)	Data	数据长度（字节）	Description
1	Write	CDSR	0x80001C06	4	设置控制器功能 启用自动校准 内存预循环被禁用 OctaFlash的传输类型设置SOPI模式，以及 OctaRAM设置DOPI模式
2	Write	MRWCR1	0x12EDEC13	4	指定读取和写入命令 OctaFlash 写指令：OctaFlash的PP 读取指令：OctaFlash的8READ

Table 36.19 翻译模式设置示例（SPI模式）

Step	Read/ Write	Address (Register)	Data	数据长度（字节）	Description
1	Write	CDSR	0x80000004	4	设置控制器功能 自动校准被禁用 内存预循环被禁用 OctaFlash的传输类型设置为SPI模式，以及 OctaRAM设置DOPI模式
2	Write	MRWCR1	0x00120013	4	指定读取和写入命令 OctaFlash 写指令：OctaFlash的PP 读取指令：OctaFlash的8READ

Note: OctaFlash连接设备1，OctaRAM连接设备0。

(2) 设置预循环已启用

在OctaFlashRAM中启用预循环时，需要修改ConfigRegister的设置
OctaFlashRAM和内存控制器。请参阅OctaFlashRAM的数据手册了解如何启用预循环。为了

example, show the sequence to be enabled pre-cycle in OctaFlash to Table 36.20. When pre-cycle is enabled in OctaFlash, users issue WREN (Write Enable) instruction, and then issue WRCR2 instruction to modify the values of Configuration Register 2 in OctaFlash to be enabled pre-cycle. For example, show the sequence to be enabled pre-cycle in OctaRAM to Table 36.21 When pre-cycle is enabled in OctaRAM, users write the Configuration Register in OctaRAM.

Table 36.20 Example of setting pre-cycle in OctaFlash

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
Write Enable (WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	Any value	4	Any value	4	—
Write Configuration Register2 (WRCR2)							
4	Write	DCR	0x00000072	4	0x0000728D	4	—
5	Write	DAR	0x00000200	4	0x00000200	4	—
6	Write	DCSR	0x04180001	4	0x04280001	4	—
7	Write	CWDR	0x00000001	1	0x00000001	1	—

Table 36.21 Example of setting pre-cycle in OctaRAM

Step	Read/ Write	Register	Data	Data Length (Bytes)	Description
1	Write	DCR	0x00004000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00002	4	—
4	Write	CWDR	0x0000F152	2	pre-cycle is enabled latency counter is 8 clocks (default)

The configuration register of memory controller in DOPI mode specifies Table 36.22 and in SOPI mode specifies Table 36.23.

Table 36.22 Example of setting pre-cycle when OctaFlash is DOPI mode

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	CDSR	0x80001C3A	4	Sets up the controller functions Auto-calibration is enabled Memory pre-cycle is enabled Transfer type of OctaFlash and OctaRAM set DOPI mode

Table 36.23 Example of setting pre-cycle when OctaFlash is SOPI mode

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	CDSR	0x80001C36	4	Sets up the controller functions Auto-calibration is enabled Memory pre-cycle is enabled Transfer type of OctaFlash set SOPI mode and OctaRAM set DOPI mode

(3) Set the number of dummy cycle

In the case of operating in 100MHz, the dummy cycle of OctaFlash/RAM should be modified. Following the data-sheet of OctaFlash/RAM, the dummy cycle of OctaFlash is 10 and the dummy cycle (Latency counter) of OctaRAM is 4. For example, show the sequence to change the dummy cycle in OctaFlash to Table 36.24. When the dummy cycle is changed, users issue WREN (Write Enable) instruction, and successively issue WRCR2 instruction to change the dummy cycle in

例如，在表36.20中显示要在OctaFlash中预循环启用的序列。当在OctaFlash中启用预循环时，用户发出WREN（WriteEnable）指令，然后发出WRCR2指令来修改OctaFlash中配置寄存器2的值以启用预循环。例如，在OctaRAM中显示要在循环前启用的序列以

表36.21当在OctaRAM中启用预循环时，用户将配置寄存器写入OctaRAM。

Table 36.20 在OctaFlash中设置预循环的示例

Step	Read/ Write	Register	SPI模式数据	Data Length (Bytes)	OPI模式数据	Data Length (Bytes)	Description
写使能(WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	任何值	4	任何值	4	—
写配置寄存器2(WRCR2)							
4	Write	DCR	0x00000072	4	0x0000728D	4	—
5	Write	DAR	0x00000200	4	0x00000200	4	—
6	Write	DCSR	0x04180001	4	0x04280001	4	—
7	Write	CWDR	0x00000001	1	0x00000001	1	—

Table 36.21 在OctaRAM中设置预循环的示例

Step	Read/ Write	Register	Data	数据长度（字节）	Description
1	Write	DCR	0x00004000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00002	4	—
4	Write	CWDR	0x0000F152	2	启用预循环延迟计数器为8个时钟（默认）

DOPI模式下内存控制器的配置寄存器指定表36.22，SOPI模式下指定表36.23。

Table 36.22 OctaFlash为DOPI模式时设置预循环示例

Step	Read/ Write	Address (Register)	Data	数据长度（字节）	Description
1	Write	CDSR	0x80001C3A	4	设置控制器功能 启用自动校准 内存预循环已启用 OctaFlash和OctaRAM组的传输类型 DOPI mode

Table 36.23 OctaFlash为SOPI模式时设置预循环的示例

Step	Read/ Write	Address (Register)	Data	数据长度（字节）	Description
1	Write	CDSR	0x80001C36	4	设置控制器功能 启用自动校准 内存预循环已启用 OctaFlash的传输类型设置SOPI模式和OctaRAM设置DOPI模式

(3) 设置虚拟周期数

在工作在100MHz的情况下，需要修改OctaFlashRAM的虚拟周期。根据OctaFlashRAM的数据表，OctaFlash的虚拟周期为10，OctaRAM的虚拟周期（延迟计数器）为4。例如，将OctaFlash中的虚拟周期更改为表36.24的顺序。当虚拟周期改变时，用户发出WREN（WriteEnable）指令，并依次发出WRCR2指令来改变虚拟周期

OctaFlash. For example, show the sequence to change the latency counter in OctaRAM to Table 36.25. When the latency counter is changed, users write the Configuration Register in OctaRAM. The Config Register of the memory-controller specifies Table 36.26.

Table 36.24 Example of changing the dummy cycle in OctaFlash

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
Write Enable (WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	Any value	4	Any value	4	—
Write Configuration Register2 (WRCR2)							
4	Write	DCR	0x00000072	4	0x0000728D	4	—
5	Write	DAR	0x00000300	4	0x00000300	4	—
6	Write	DCSR	0x04180001	4	0x04280001	4	—
7	Write	CWDR	0x00000005	1	0x00000005	1	—

Table 36.25 Example of changing the latency counter in OctaRAM

Step	Read/ Write	Register	Data	Data Length (Bytes)	Description
1	Write	DCR	0x00004000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00002	4	—
4	Write	CWDR	0x0000F112	2	pre-cycle is enabled latency counter is 4 clocks

Table 36.26 Example of dummy cycle setting

Step	Read/ Write	Address (Register)	Data	Data Length (Bytes)	Description
1	Write	MDLR	0x000A0404	4	Specifies the dummy length Dummy cycle of OctaFlash is 10 in reading Dummy cycle of OctaRAM is 4 in writing/reading

(4) Set preamble mode is enable

When users use the preamble of OctaFlash, it is necessary to modify the setting of the Config Register of OctaFlash and memory controller. Refer to the data sheet of OctaFlash about how to be enabled preamble. For example, show the sequence to set preamble mode in OctaFlash to Table 36.27. When users set preamble mode, users issue WREN (Write Enable) instruction, and then issue WRCR instruction to set preamble mode. Users need to check out bit0 (WIP) of Status Register in OctaFlash, until this bit (WIP) set 0.

Table 36.27 Example of setting preamble mode in OctaFlash (1 of 2)

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
Write Enable (WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	Any value	4	Any value	4	—
Write Configuration Register (WRCR)							
4	Write	DCR	—	—	0x000001FE	4	—

八闪。例如，将OctaRAM中的延迟计数器更改为表36.25的顺序。当延迟计数器改变时，用户将配置寄存器写入OctaRAM。内存控制器的配置寄存器指定表36.26。

Table 36.24 在OctaFlash中更改虚拟周期的示例

Step	Read/ Write	Register	SPI模式数据	Data Length (Bytes)	OPI模式数据	Data Length (Bytes)	Description
写使能(WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	任何值	4	任何值	4	—
写配置寄存器2(WRCR2)							
4	Write	DCR	0x00000072	4	0x0000728D	4	—
5	Write	DAR	0x00000300	4	0x00000300	4	—
6	Write	DCSR	0x04180001	4	0x04280001	4	—
7	Write	CWDR	0x00000005	1	0x00000005	1	—

Table 36.25 在OctaRAM中更改延迟计数器的示例

Step	Read/ Write	Register	Data	数据长度（字节）	Description
1	Write	DCR	0x00004000	4	—
2	Write	DAR	0x00040000	4	—
3	Write	DCSR	0x04A00002	4	—
4	Write	CWDR	0x0000F112	2	启用预循环延迟计数器为4 个时钟

Table 36.26 虚拟循环设置示例

Step	Read/ Write	Address (Register)	Data	数据长度（字节）	Description
1	Write	MDLR	0x000A0404	4	指定虚拟长度 OctaFlash的虚拟循环读取为10 OctaRAM的空周期为4写读

(4) 设置前导码模式启用

当用户使用OctaFlash的前导码时，需要修改OctaFlash的ConfigRegister和内存控制器的设置。有关如何启用前导码，请参阅OctaFlash的数据手册。例如，在表36.27中显示在OctaFlash中设置前导码模式的序列。当用户设置前导模式时，用户发出WREN（WriteEnable）指令，然后发出WRCR指令来设置前导模式。用户需要检查OctaFlash中状态寄存器的bit0(WIP)，直到该位(WIP)设置为0。

Table 36.27 在OctaFlash中设置前导码模式的示例（1of2）

Step	Read/ Write	Register	SPI模式数据	Data Length (Bytes)	OPI模式数据	Data Length (Bytes)	Description
写使能(WREN)							
1	Write	DCR	0x00000006	4	0x000006F9	4	—
2	Write	DCSR	0x00180000	4	0x00280000	4	—
3	Write	CWNDR	任何值	4	任何值	4	—
写配置寄存器(WRCR)							
4	Write	DCR	—	—	0x000001FE	4	—

Table 36.27 Example of setting preamble mode in OctaFlash (2 of 2)

Step	Read/ Write	Register	SPI Mode Data	Data Length (Bytes)	OPI Mode Data	Data Length (Bytes)	Description
5	Write	DAR	—	—	0x00000001	4	—
6	Write	DCSR	—	—	0x04200001	4	—
7	Write	CWDR	—	—	0x00000017	1	—
Read Status Register (RDSR)							
8	Write	DCR	0x00000005	4	0x000005FA	4	—
9	Write	DAR	—	—	0x00000000	4	—
10	Write	DCSR	0x00180001	4	0x0C280401	4	—
11	Read	CRR	0x000000xx	4	0x000000xx	4	Users must repeat to read Status Register, until the bit0 (WIP) of data to read from Status Register will be 0.

36.3.6.4 Automatic Calibration Setting

The OSPI has an automatic calibration function to prevent acquisition of wrong data due to the variation of voltage and temperature.

Figure 36.14 shows the automatic calibration setting flow for the OctaFlash and OctaRAM devices.

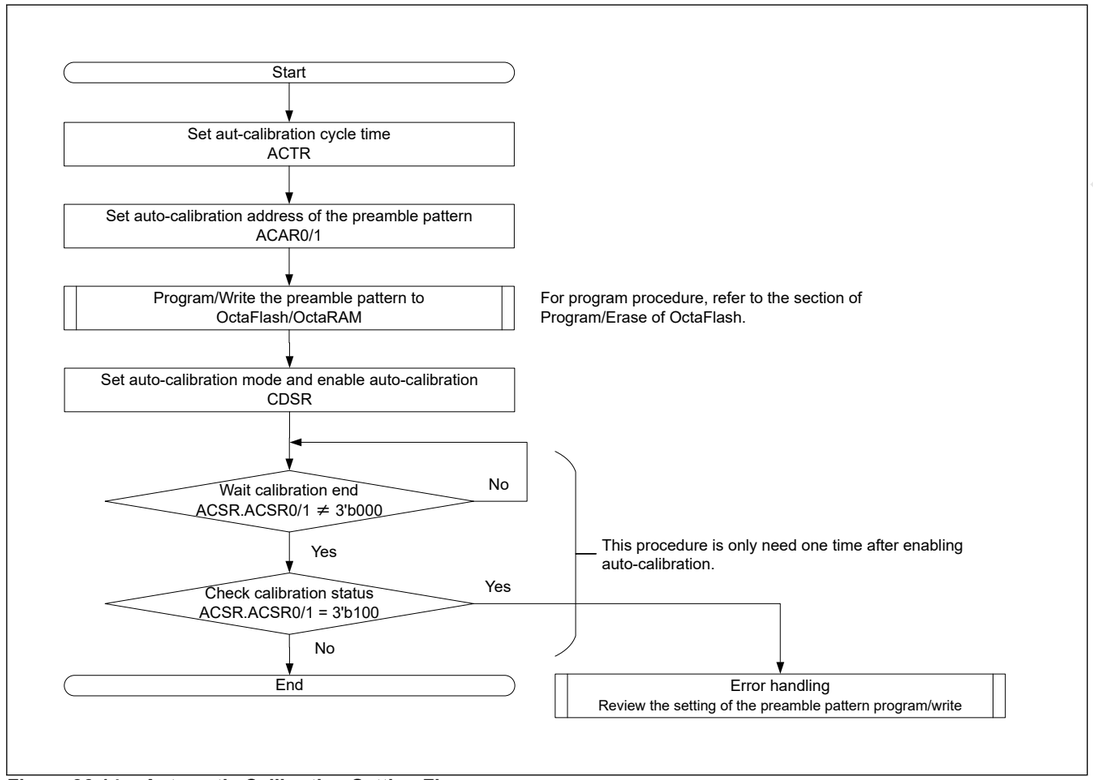


Figure 36.14 Automatic Calibration Setting Flow

For details, see section 36.3.6.2. Basic Operation Settings.

The following preamble pattern should be stored in the setting address of ACAR0 and ACAR1.

Table 36.27 在OctaFlash中设置前导码模式的示例(2of2)

Step	Read/ Write	Register	SPI模式数据	Data Length (Bytes)	OPI模式数据	Data Length (Bytes)	Description
5	Write	DAR	—	—	0x00000001	4	—
6	Write	DCSR	—	—	0x04200001	4	—
7	Write	CWDR	—	—	0x00000017	1	—
读取状态寄存器(RDSR)							
8	Write	DCR	0x00000005	4	0x000005FA	4	—
9	Write	DAR	—	—	0x00000000	4	—
10	Write	DCSR	0x00180001	4	0x0C280401	4	—
11	Read	CRR	0x000000xx	4	0x000000xx	4	用户必须重复阅读状态寄存器，直到从状态寄存器中读取的数据的第0位（WIP）为0。

36.3.6.4 自动校准设置

OSPI具有自动校准功能，可防止由于电压和温度的变化而采集错误数据。

图36.14显示了OctaFlash和OctaRAM设备的自动校准设置流程。

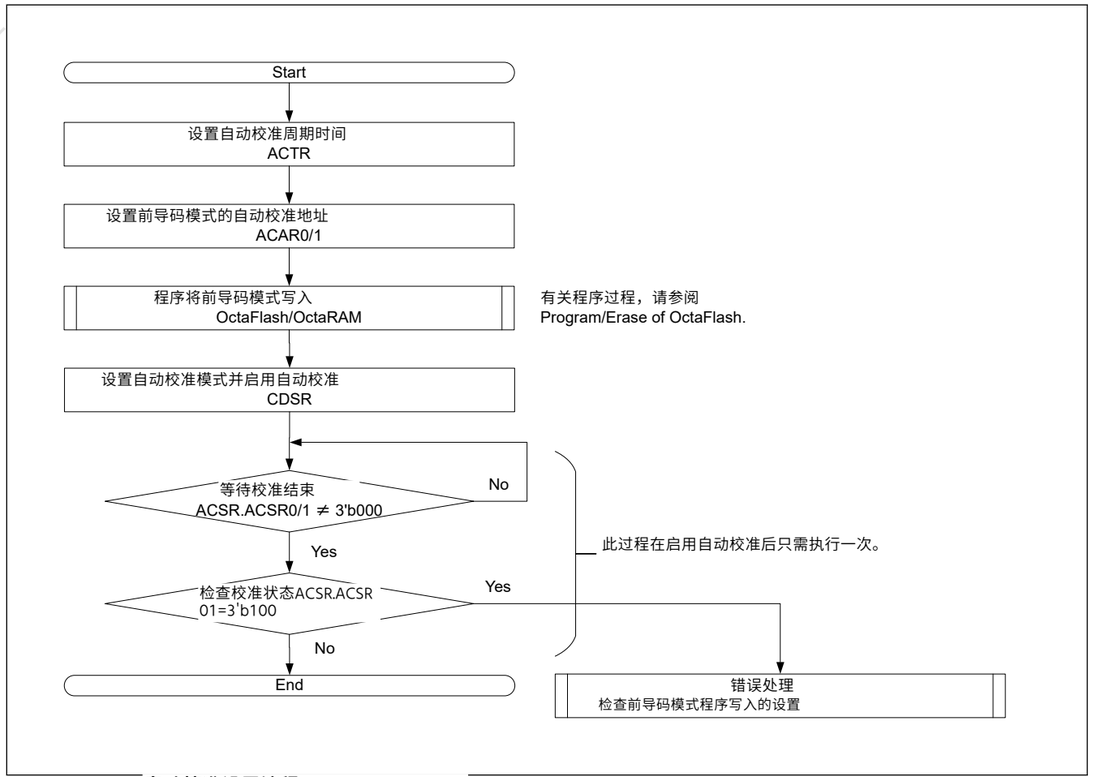


Figure 36.14 自动校准设置流程

有关详细信息，请参阅第36.3.6.2节。基本操作设置。

ACAR0和ACAR1的设置地址中应存储以下前导码模式。

RA生态工作室

- DOPI mode when MRWCSR.MWOn = 0 (n = 0, 1) : 0x00F708F7_FF0000F7_0800FF00_FFFF0000
- DOPI mode when MRWCSR.MWOn = 1 (n = 0, 1) : 0xF700F708_00FFF700_000800FF_FFFF0000
- SOPI mode : 0xF7F700F7_0000FF00

36.3.6.5 Program/Erase of OctaFlash Setting

Figure 36.15 and Figure 36.16 show the procedure for program (write) and erase of OctaFlash. There is a restriction on partial program or double program in OctaFlash, so it should be programmed with a proper size according to the usage of OctaFlash. For details, see OctaFlash datasheet. The program size in one CS asserted period can be specified by enabling single continuous write mode.

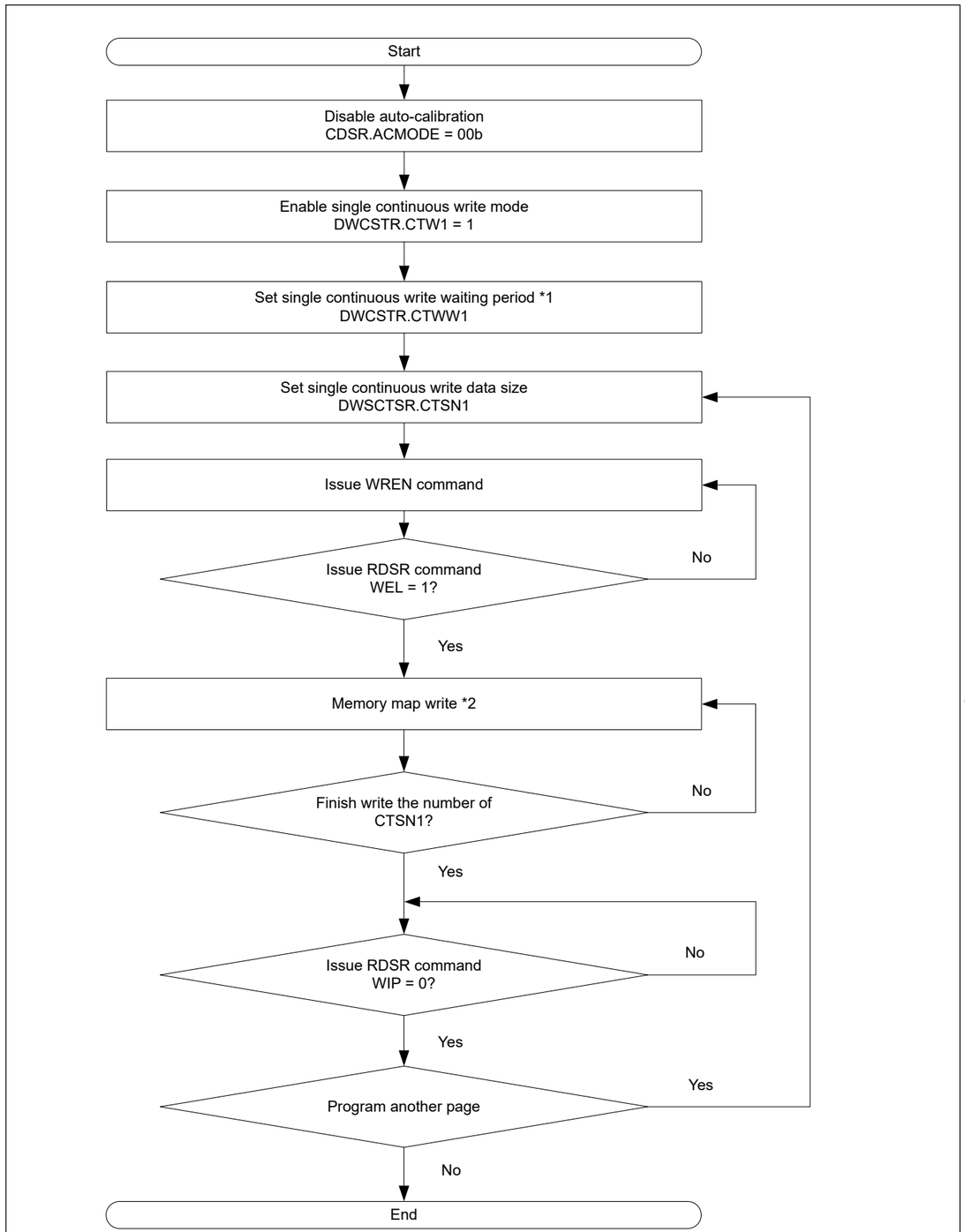
●MRWCSR.MWOn=0(n=0 1)时的DOPI模式：0x00F708F7_FF0000F7_0800FF00_FFFF0000
●MRWCSR.MWOn=1(n=0 1)时的DOPI模式：0xF700F708_00FFF700_000800FF_FFFF0000

- SOPI mode : 0xF7F700F7_0000FF00

36.3.6.5 OctaFlash设置的程序擦除

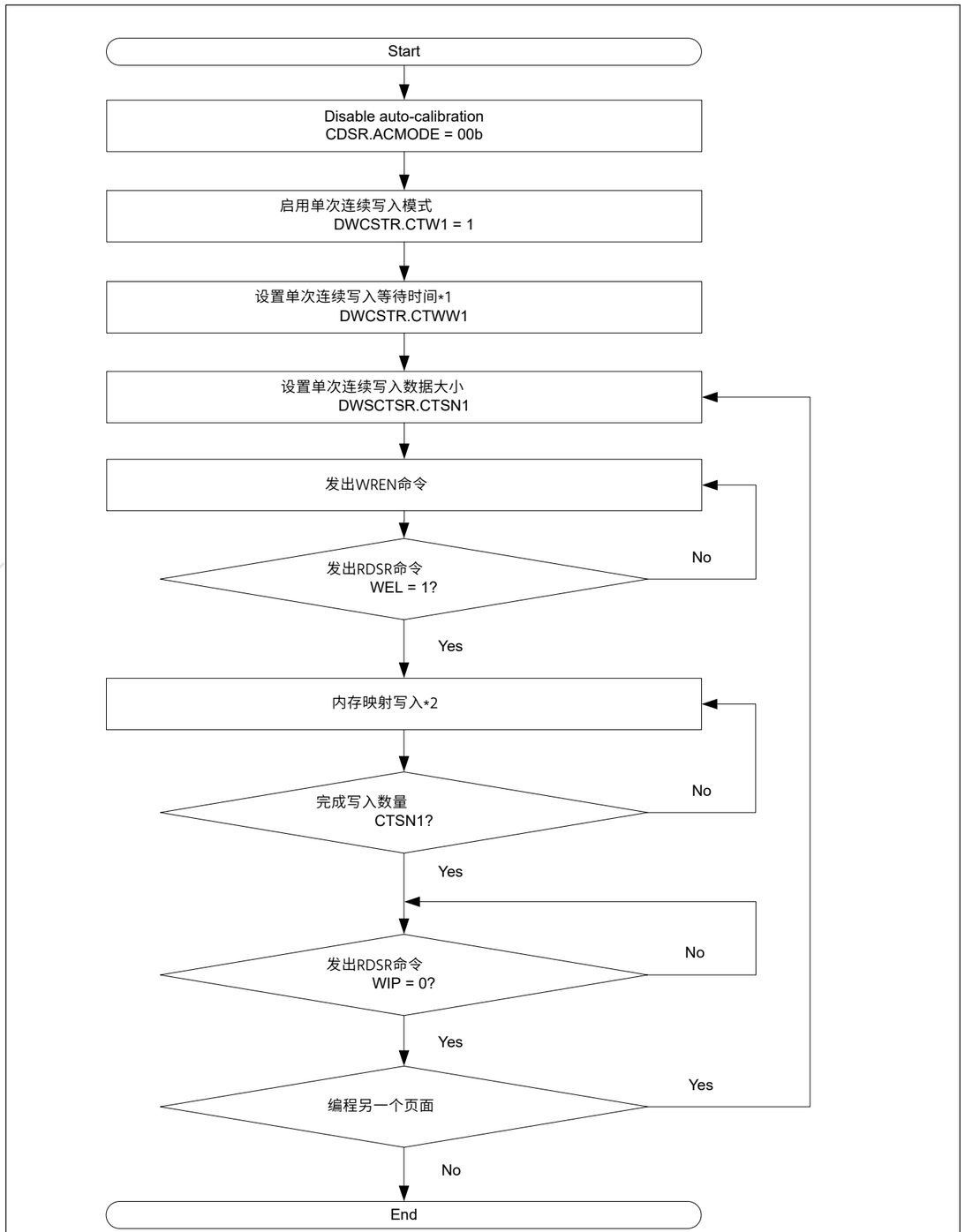
图36.15和图36.16显示了OctaFlash的编程（写入）和擦除过程。OctaFlash对部分烧写或重复烧写是有限制的，所以要根据OctaFlash的使用情况，烧写合适的大小。有关详细信息，请参阅OctaFlash数据表。一个CS断言周期内的程序大小可以通过启用单次连续写入模式来指定。

RA生态工作室



Note 1. Set long enough period to ensure the one program size defined by the CTSN1 bits.
Note 2. Not change write access size 8/16/32 bit in one page program.

Figure 36.15 Procedure for program of OctaFlash



注1.设置足够长的周期以确保由CTSN1位定义的一个程序大小。
注2.在一页程序中不改变写访问大小81632位。

Figure 36.15 OctaFlash程序的程序

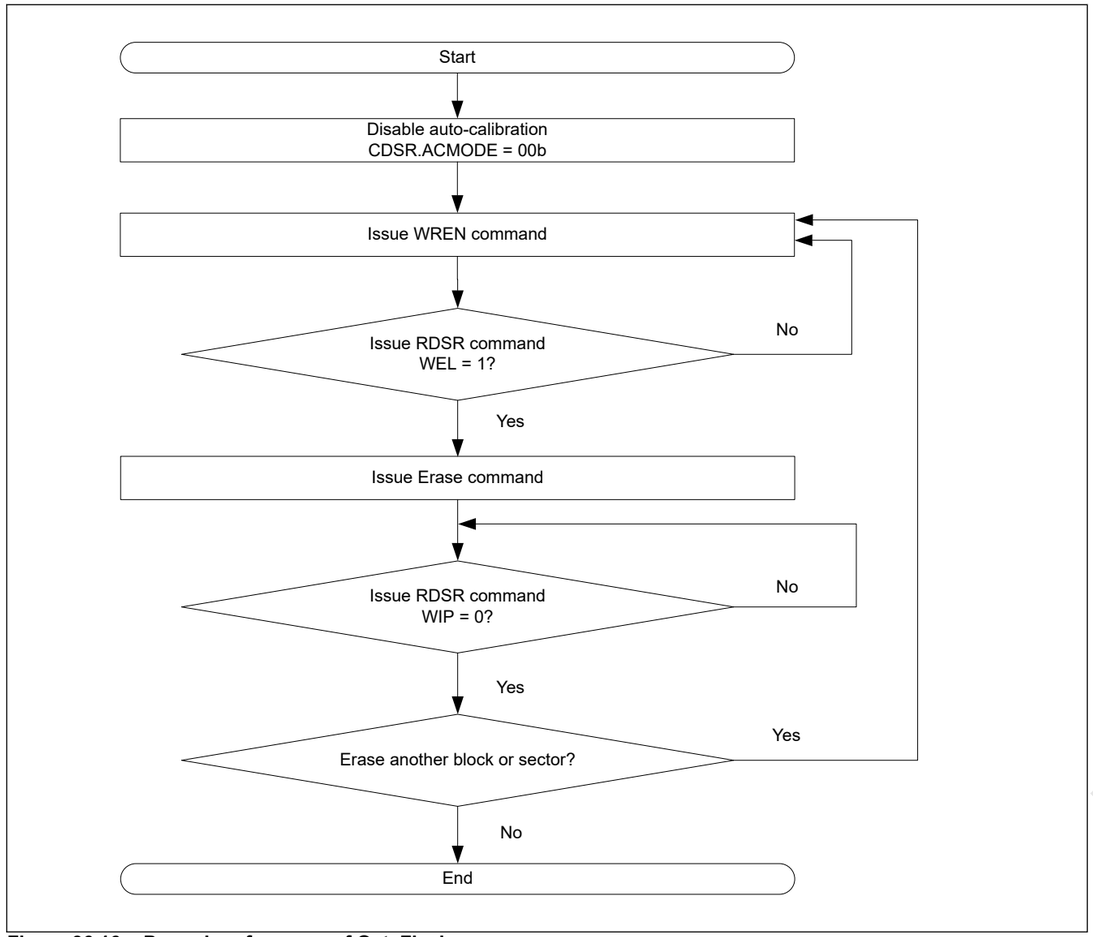


Figure 36.16 Procedure for erase of OctaFlash

36.4 SOPI/DOPI mode, Delay Line Adjustment and OM_DQS Auto-Calibration

36.4.1 SOPI/DOPI mode and OM_DQS

Depending on the characteristic of SOPI/DOPI mode, controller cannot latch data on the rising edge / falling edge of the OM_DQS clock, the delayed OM_DQS is needed to capture data with sufficiency setup/hold time margin.

Figure 36.17 shows delayed OM_DQS (OM_DQS strobe) has good latch position to latch data.

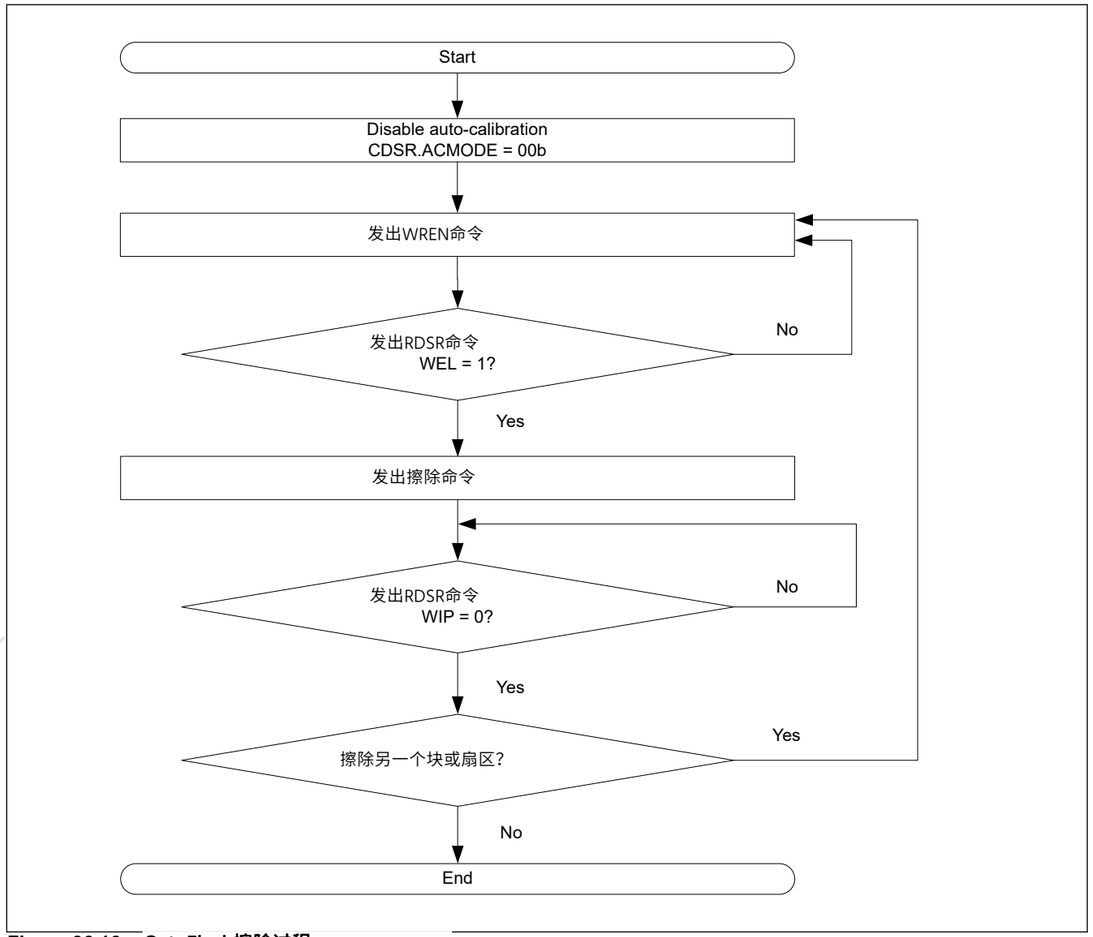


Figure 36.16 OctaFlash擦除过程

36.4 SOPIDOPI模式、延迟线调整和OM_DQS自动校准

36.4.1 SOPIDOPI模式和OM_DQS

根据SOPIDOPI模式的特性，控制器不能在信号的上升沿下降沿锁存数据OM_DQS时钟，需要延迟的OM_DQS来捕获具有足够设置保持时间余量的数据。

图36.17显示延迟的OM_DQS（OM_DQS选通）具有良好的锁存位置来锁存数据。

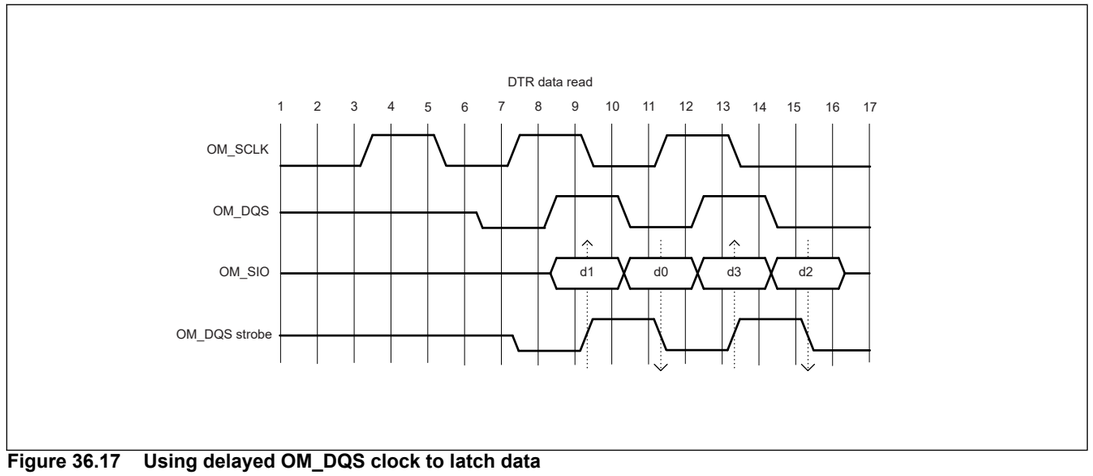


Figure 36.17 Using delayed OM_DQS clock to latch data

36.5 Single continuous write/read mode

Single continuous write/read is a mode to optimize a performance of single access with increment address. When the address is continuous, the OSPI skips to re-send command, address, and dummy cycles to memory device again by keeping OM_CS0/1 low.

Whether single continuous mode effectively optimize a performance depends on master. When master issue single access (not burst) with increment address, single continuous mode effectively optimize a performance. For recommended setting, see Table 36.28.

Table 36.28 Recommended single continuous mode setting when access address is increment

Master	Write/Read	Single continuous mode
CPU	Write	Enable
	Read with S Cache off*1	Enable
	Read with S Cache on*1	Disable
DMAC/DTC	Write	Enable
	Read	Enable
EDMAC	Write	Disable
	Read	Disable

Note 1. For details, see section 14.8. Cache.

36.5.1 Single continuous write operation

Figure 36.18 shows the procedure of single continuous write of OctaRAM. For the procedure of OctaFlash, see the Figure 36.15.

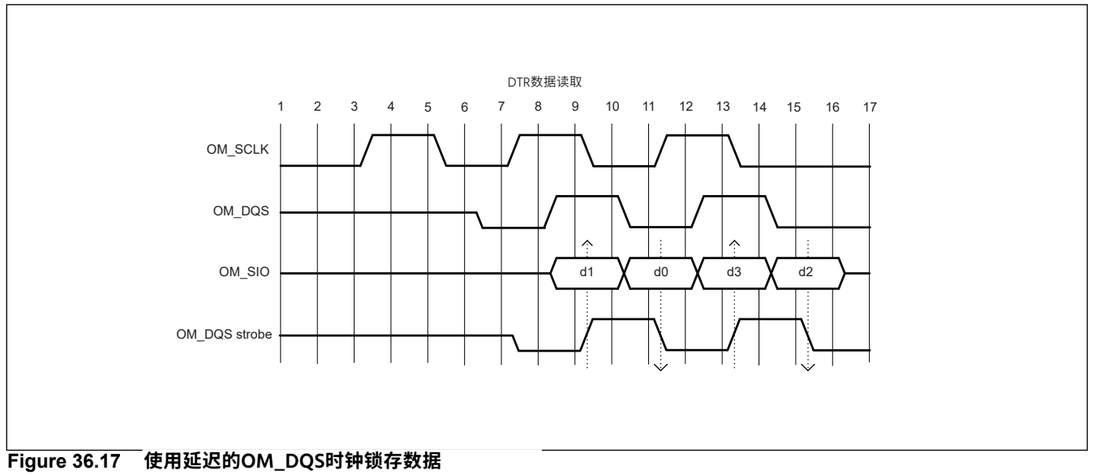


Figure 36.17 使用延迟的OM_DQS时钟锁存数据

36.5 单次连续写读模式

单次连续写读是一种以递增地址优化单次访问性能的模式。当地址连续时，OSPI通过保持OM_CS01为低，跳过重新发送命令、地址和虚拟周期到存储设备。

单一连续模式能否有效优化性能取决于master。当主机发出带有递增地址的单次访问（非突发）时，单次连续模式有效地优化了性能。推荐设置见表36.28。

Table 36.28 访问地址递增时推荐的单连续模式设置

Master	Write/Read	单次连续模式
CPU	Write	Enable
	在SCache关闭的情况下读取*1	Enable
	在*1上使用SCache读取	Disable
DMAC/DTC	Write	Enable
	Read	Enable
EDMAC	Write	Disable
	Read	Disable

注1.详见14.8节。缓存。

36.5.1 单次连续写操作

图36.18显示了OctaRAM的单次连续写入过程。OctaFlash的流程见图36.15。

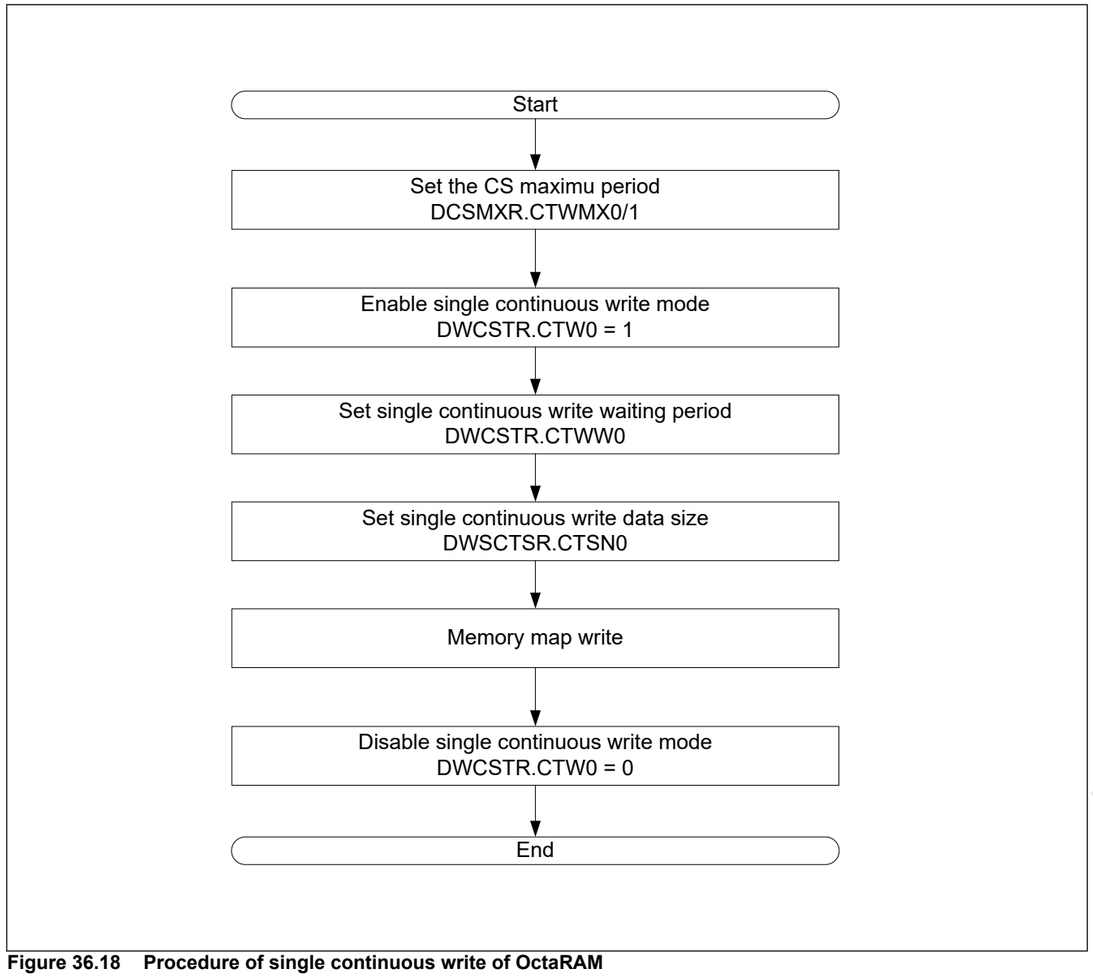


Figure 36.18 Procedure of single continuous write of OctaRAM

When DWCSTR.CTW0/1 is 1 and the OSPI receives a single write, write command will be issued and CS pin will be kept asserted.

When one of the following conditions is satisfied, the current single continuous write will finish and CS pin will be negated.

1. Current access address is not increment.
   The definition of increment address is:
   Current address = Previous address + Previous length
2. Current access attribution is burst (not single).
3. Current access size is different from previous access.*1
4. The OSPI has not received any access for the period specified by DWCSTR.CTWW0/1 bits.
5. Current access is read (not write).
6. CS asserted period has been elapsed the period specified by DCSMXR.CTWMX0/1 bits.*1 *2
7. The number of bytes specified by DWSCTSR.CTSN0/1 bits has been transferred.*3

Note 1. Although once CS pin is negated, next single continuous write will be issued automatically.
Note 2. This condition is for a restriction on CS asserted period in OctaRAM.
This condition is not applied to OctaFlash.
Note 3. When DWSCTSR.CTSN0/1 is set to 0, this condition is never satisfied.

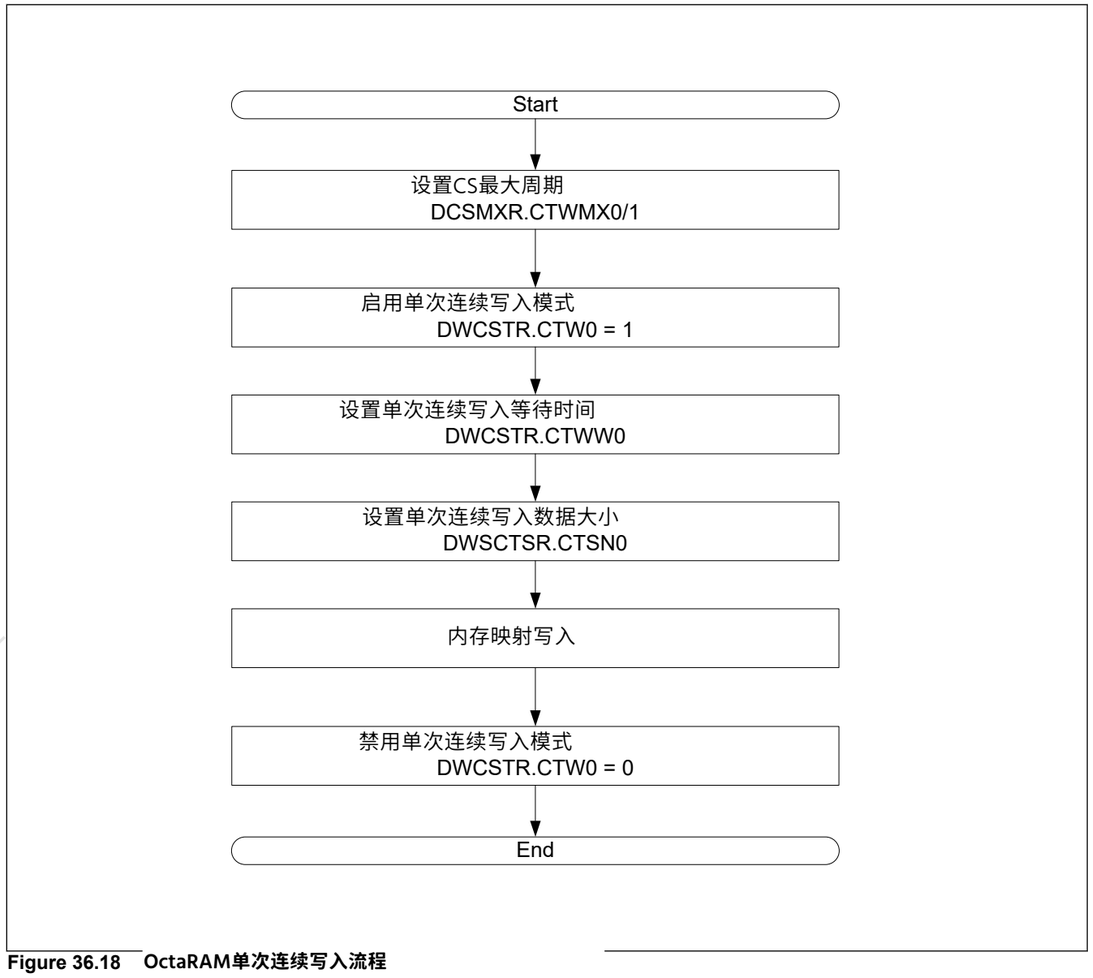


Figure 36.18 OctaRAM单次连续写入流程

当DWCSTR.CTW01为1且OSPI接收到单次写入时，将发出写入命令且CS引脚将保持有效。

当满足以下条件之一时，当前单次连续写入将完成，CS引脚将被取反。

1.当前访问地址不递增。增量地址的定义是：
当前地址=前一个地址+前一个长度

2.当前访问属性是突发的（不是单一的）。

3.当前访问大小与以前访问不同。*1

4.OSPI在DWCSTR.CTWW01位指定的时间段内没有收到任何访问。

5.当前访问是读（不是写）。

6.CS断言周期已经过DCSMXR.CTWMX01位指定的周期。*1*2

7.DWSCTSR.CTSN01位指定的字节数已被传输。*3

注1.虽然一旦CS引脚被取反，下一次连续写入将自动发出。
注2.此条件用于限制OctaRAM中的CS断言周期。
此条件不适用于OctaFlash。
注3.当DWSCTSR.CTSN01设置为0时，此条件永远不会满足。

36.5.2 Single continuous read operation

Figure 36.19 shows procedure for single continuous read of OctaRAM and OctaFlash.

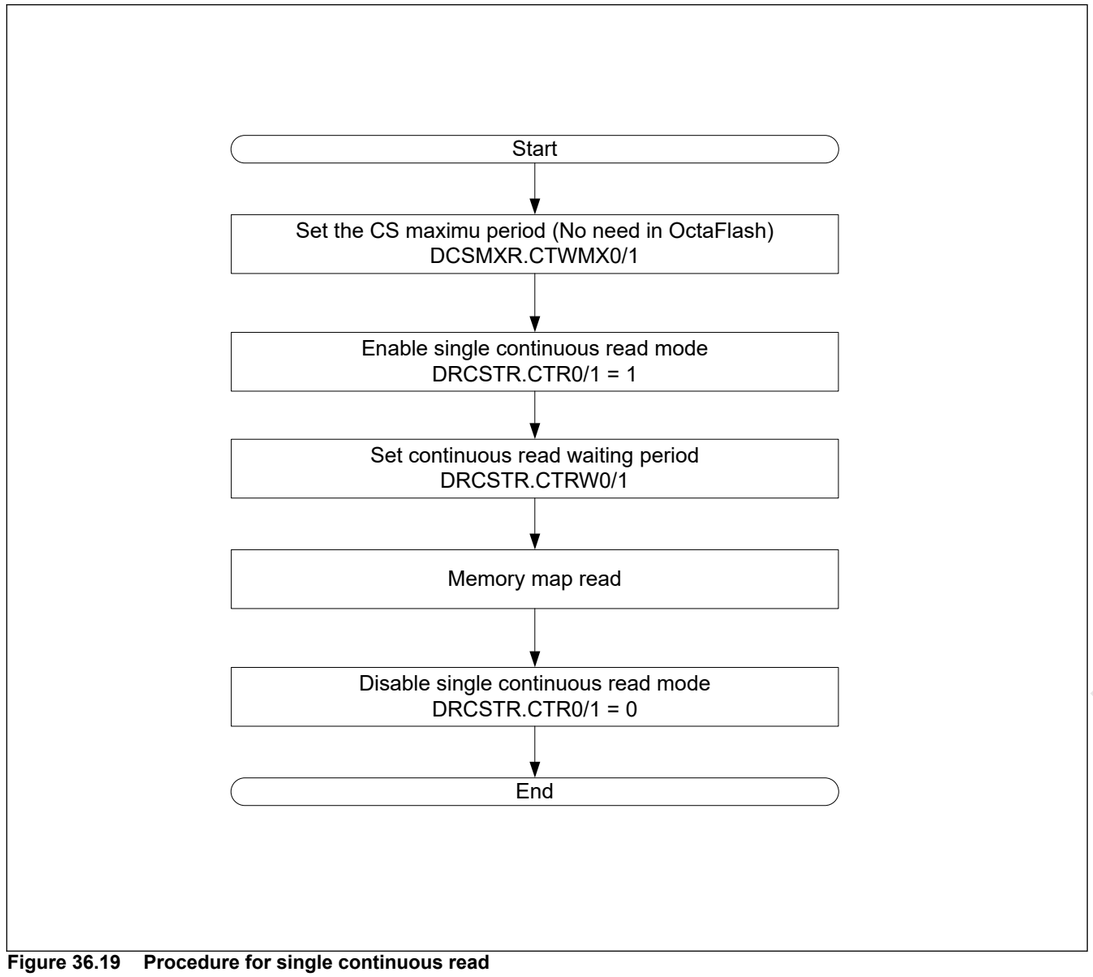


Figure 36.19 Procedure for single continuous read

When DRCSTR.CTR0/1 is 1 and the OSPI receives a single write, read command will be issued and CS pin will be kept asserted.

When one of the following conditions is satisfied, the current single continuous read will finish and CS pin will be negated.

1. Current access address is not increment.
   The definition of increment address is:
   Current address = Previous address + Previous length
2. Current access attribution is burst (not single).
3. Current access size is different from previous access.*1
4. The OSPI has not received any access for the period specified by DRCSTR.CTRW0/1 bits.
5. Current access is write (not read).
6. CS asserted period has been elapsed the period specified by DCSMXR.CTWMX0/1 bits.*1 *2

Note 1. Although once CS pin is negated, next single continuous read will be issued automatically.

36.5.2 单次连续读取操作

图36.19显示了对OctaRAM和OctaFlash进行单次连续读取的过程。

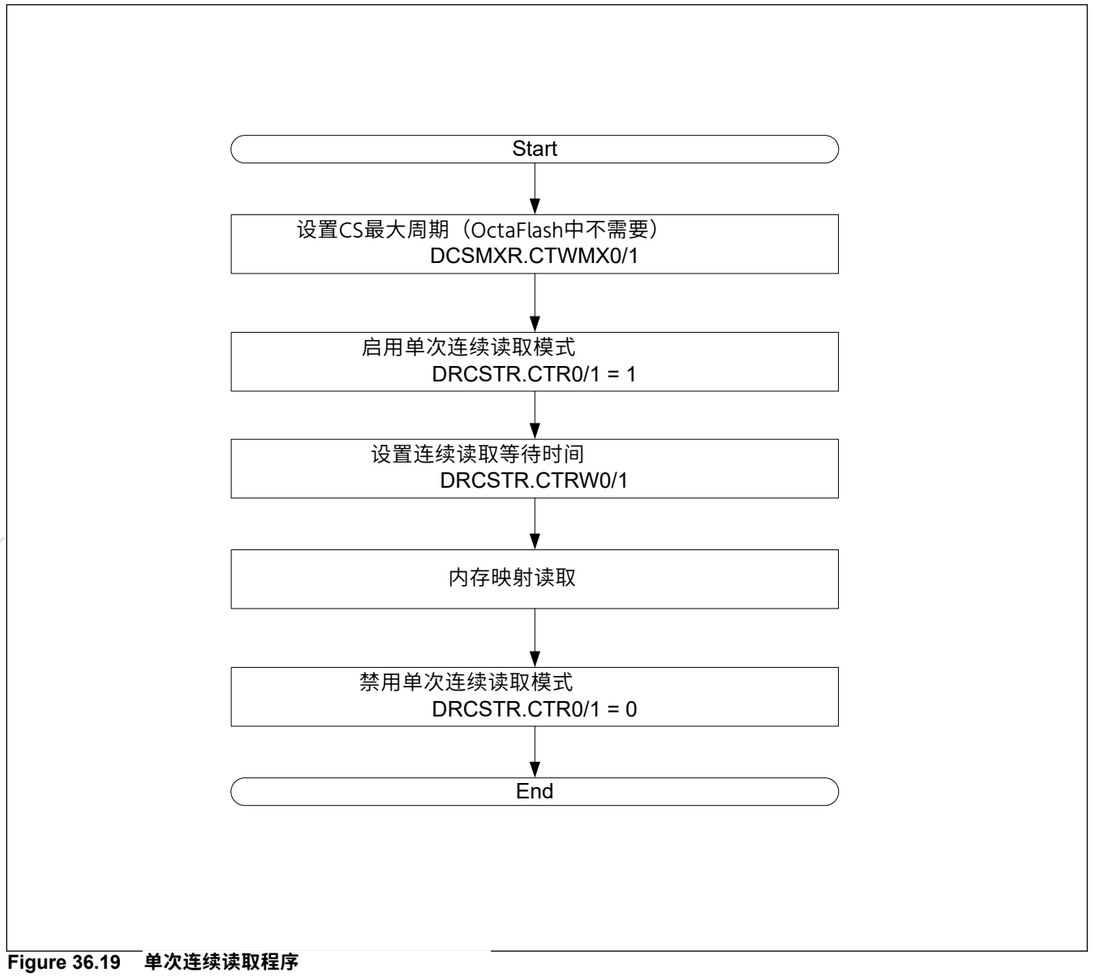


Figure 36.19 单次连续读取程序

当DRCSTR.CTR01为1且OSPI接收到单次写入时，将发出读取命令且CS引脚将保持有效。

当满足以下条件之一时，当前单次连续读取将完成，CS引脚将被取反。

1.当前访问地址不递增。
增量地址的定义是：
当前地址=前一个地址+前一个长度

2.当前访问属性是突发的（不是单一的）。

3.当前访问大小与以前访问不同。*1

4.OSPI在DRCSTR.CTRW01位指定的时间段内没有收到任何访问。

5.当前访问是写（不是读）。

6.CS断言周期已经过DCSMXR.CTWMX01位指定的周期。*1*2

注1.虽然一旦CS引脚被取反，下一次连续读取将自动发出。

Note 2. This condition is for a restriction on CS asserted period in OctaRAM.
This condition is not applied to OctaFlash.

36.6 OM_DQS Enable Counter

During read command operation, the OM_DQS signal is used as the data latch clock by the controller. When the memory device is in the idle state, OM_DQS maintains a high impedance (Hi-Z) state, and asserts low before data is output. This Hi-Z to Low transition may latch wrong data by driving the OM_DQS data latch logic of thecontroller.

Figure 36.20 shows the waveform when OM_DQS maintains a high-impedance (Hi-Z) state and asserts low before data is output.

Avoiding such Hi-Z to Low transitions, this controller can bypass wrong data with Memory delay trim register (MDTR). (MDTR.DQSEDOPI[3:0] for Flash DOPI mode, MDTR.DQSESOPI[3:0] for Flash SOPI mode, and MDTR.DQSERAM[3:0] for RAM mode)

Each configuration can be set from 0 to 15 for each case.

[OctaFlash]

OM_DQS Enable counter (MDTR) minimum value ≥ Command cycle number + Address cycle number*1 + OM_DQS Stable cycle number*2 + 1 (OM_DQS Delay cycle number)

OM_DQS Enable counter (MDTR) maximum value ≤ Command cycle number + Address cycle number*1 + Memory dummy cycle number*3 + Pre-cycle setting*4

[OctaRAM]

OM_DQS Enable counter (MDTR) minimum value ≥ Command cycle number + Address cycle number

OM_DQS Enable counter (MDTR) maximum value ≤ Command cycle number + Address cycle number*1 + Memory dummy cycle number + Pre-cycle setting*4

Note 1. Flash SOPI: Command cycle number + address cycle number = 2 + 4 = 6
Flash DOPI: Command cycle number + address cycle number = 1 + 2 = 3
RAM DOPI: number of command cycles + number of address cycles = 1 + 2 - 1 = 2 (start dummy calculation from the second cycle)
Note 2. OM_DQS Stable cycle number: Maximum value is 2 OM_SCLK (Reference specification of OctaFlash)
Note 3. Refer to OctaFlash minimum dummy cycle number in each command.
For example, dummy cycles of read configuration register is always 4 cycles regardless of dummy cycle setting of Configuration register 2.
Note 4. Pre-cycle setting: OM_DQSpre-cycle on/off
OM_DQS pre-cycle off: Pre-cycle setting = 0
OM_DQS pre-cycle on: Pre-cycle setting = -1

Setting example: Flash DOPI mode, dummy cycle = 4, pre-cycle is off

Minimum value of OM_DQS enable counter (MDTR) ≥ 1 + 2 + 2 + 1 = 6

Maximum value of OM_DQS enable counter (MDTR) ≤ 1 + 2 + 4 + 0 = 7

From the above, setting MDTR .DQSEDOPI[3:0] from 6 to 7 can latch the correct data. If MDTR is too small, wrong data may be latched due to a transition from Hi-Z to Low. If MDTR is too large, no data is latched.

注2.此条件用于限制OctaRAM中的CS断言周期。
此条件不适用于OctaFlash。

36.6 OM_DQS启用计数器

在读命令操作期间，OM_DQS信号被控制器用作数据锁存时钟。当存储设备处于空闲状态时，OM_DQS保持高阻抗(Hi-Z)状态，并在数据输出前置低。这种HiZ到Low的转换可能会通过驱动控制器的OM_DQS数据锁存逻辑来锁存错误的数据。

图36.20显示了当OM_DQS保持高阻抗(Hi-Z)状态并在数据输出之前断言为低电平时的波形。

为了避免这种Hi-Z到低电平的转换，该控制器可以使用内存延迟调整寄存器(MDTR)绕过错误数据。（MDTR.DQSEDOPI[3:0]用于FlashDOPI模式，MDTR.DQSESOPI[3:0]用于FlashSOPI模式，MDTR.DQSERA[3:0]用于RAM模式）

对于每种情况，每个配置都可以设置为0到15。

[OctaFlash]

OM_DQS启用计数器(MDTR)最小值≥命令周期数+地址周期数*1+OM_DQS稳定周期数*2+1（OM_DQS延迟周期数）

OM_DQS启用计数器(MDTR)最大值≤命令周期数+地址周期数*1+内存虚拟周期数*3+预周期设置*4

[OctaRAM]

OM_DQS启用计数器(MDTR)最小值≥命令周期数+地址周期数

OM_DQS启用计数器(MDTR)最大值≤命令周期数+地址周期数*1+内存虚拟周期数+预周期设置*4

注1.FlashSOPI：命令周期数+地址周期数=2+4=6
FlashDOPI：命令周期数+地址周期数=1+2=3
RAMDOPI：命令周期数+地址周期数=1+21=2（从第二个周期开始虚拟计算）

注2.OM_DQS稳定周期数：最大值为2OM_SCLK（OctaFlash参考规范）
注3.请参阅每个命令中的OctaFlash最小虚拟周期数。
例如，读取配置寄存器的虚拟周期始终为4个周期，而与配置寄存器2。
Note 4. Pre-cycle setting: OM_DQSpre-cycle on/off
OM_DQS pre-cycle off: Pre-cycle setting = 0
OM_DQS pre-cycle on: Pre-cycle setting = -1

设置示例：FlashDOPI模式，dummycycle=4，pre-cycle关闭

OM_DQS启用计数器(MDTR)的最小值≥1+2+2+1=6

OM_DQS启用计数器(MDTR)的最大值≤1+2+4+0=7

综上所述，将MDTR.DQSEDOPI[3:0]从6设置为7可以锁存正确的数据。如果MDTR太小，由于从Hi-Z到Low的转换，可能会锁存错误的数据。如果MDTR太大，则不会锁存任何数据。

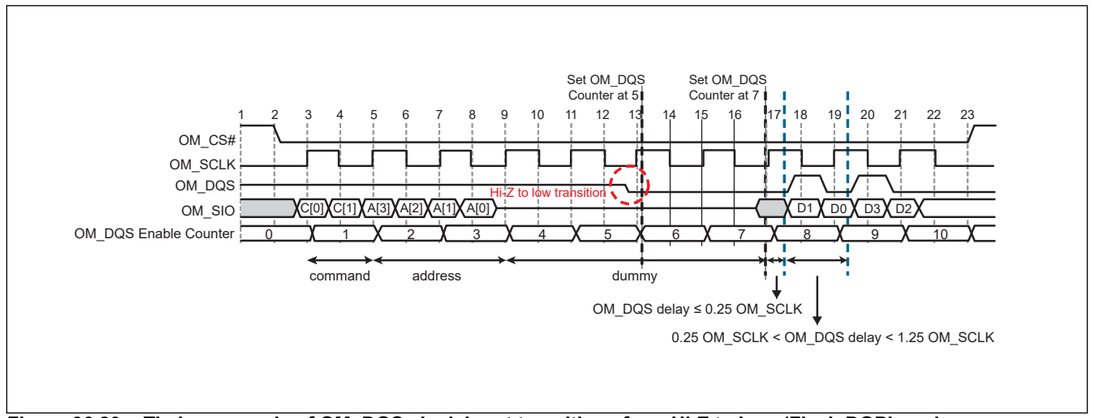


Figure 36.20 Timing example of OM_DQS clock input transitions from Hi-Z to Low (Flash DOPI mode, dummy cycle number = 4, OM_DQS pre-cycle on)

36.7 Interrupt and bus error

The OSPI output the interrupt request and bus error to the CPU in the following conditions.

Table 36.29 Interrupt and bus error sources

Access	Interrupt and bus error sources	Status flag	Interrupt	Bus error
memory-mapped write	Illegal address access	ESR.MWESR = 0x80	✓	✓
	Access during the OSPI is module stop state	—	×	✓
memory-mapped read	Illegal address access or DQS timeout detection in single continuous mode*1	ESR.MRESR = 0x80	✓	✓
	OctaFlash ECC error detection	ESR.MRESR = 0x01	✓	✓
	Preamble error detection	ESR.MRESR = 0x02	✓	✓
	DQS timeout detection*1	ESR.MRESR = 0x03	✓	✓
	Access during the OSPI is module stop state	—	×	✓
Register write	Illegal address access	—	×	✓
Register read	Illegal address access	—	×	✓
CRR register read	DQS timeout detection	—	×	✓

Note 1. After DQS timeout detection, the ESR.MRESR is set to 0x08 only under the condition that first memory map read after reset is executed in single continuous mode. The ESR.MRESR is set to 0x03 under other conditions.

36.8 Usage Note

36.8.1 Setting for the Module-Stop Function

Do not set the MSTP bit of the OSPI to 1 while the OSPI is accessing to the memory devices.

36.8.2 CPU write access attribution

CPU write access attribution to OSPI I/O registers area is recommended to be non-bufferable. Write access attribution is specified by the MPU registers in CPU. For details, see the *ARMv8-M Architecture Reference Manual* (ARM DDI 0553A).

When CPU write access attribution is bufferable, after writing register in memory device or OSPI, confirm that its value has actually changed before memory map read/write.

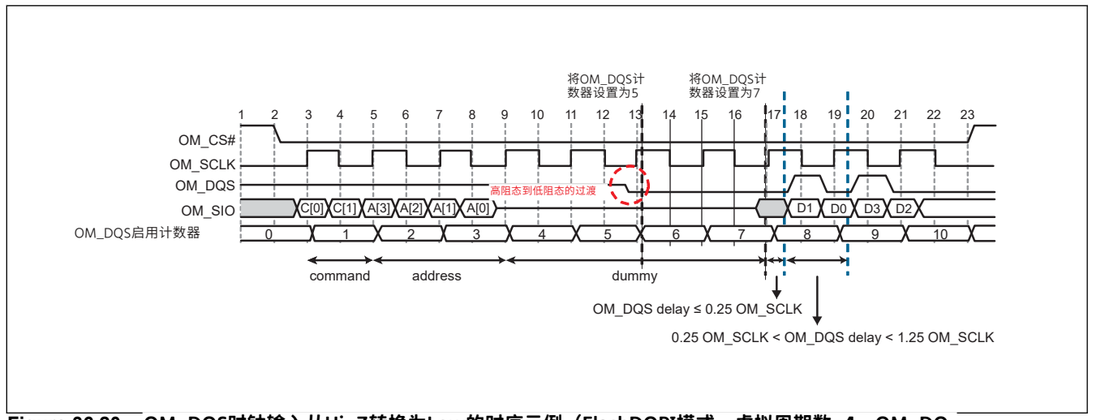


Figure 36.20 OM_DQS时钟输入从Hi-Z转换为Low的时序示例（FlashDOPI模式，虚拟周期数=4，OM_DQS预周期开启）

36.7 中断和总线错误

OSPI在以下情况下向CPU输出中断请求和总线错误。

Table 36.29 中断和总线错误源

Access	中断和总线错误源	状态标志	Interrupt	总线错误
memory-mapped write	非法地址访问	ESR.MWESR = 0x80	✓	✓
	OSPI期间的访问是模块停止状态	—	×	✓
memory-mapped read	单次连续模式下非法地址访问或DQS超时检测*1	ESR.MRESR = 0x80	✓	✓
	OctaFlashECC错误检测	ESR.MRESR = 0x01	✓	✓
	前导错误检测	ESR.MRESR = 0x02	✓	✓
	DQS超时检测*1	ESR.MRESR = 0x03	✓	✓
	OSPI期间的访问是模块停止状态	—	×	✓
寄存器写入	非法地址访问	—	×	✓
注册读取	非法地址访问	—	×	✓
CRR寄存器读取	DQS超时检测	—	×	✓

注1.在DQS超时检测后，ESR.MRESR仅在复位后的第一个存储器映射读取以单次连续模式执行的条件下设置为0x08。ESR.MRESR在其他条件下设置为0x03。

36.8 使用说明

36.8.1 模块停止功能的设置

当OSPI访问存储设备时，不要将OSPI的MSTP位设置为1。

36.8.2 CPU写访问属性

建议将CPU对OSPIIO寄存器区域的写访问属性设置为不可缓冲。写访问属性由CPU中的MPU寄存器指定。有关详细信息，请参阅ARMv8-M架构参考手册(ARMDDI0553A)。

当CPU写访问属性为可缓冲时，在内存设备或OSPI中写入寄存器后，确认其值在内存映射读写之前确实发生了变化。

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36.8.3 DQS in SOPI mode

OctaFlash support SOPI mode. In SOPI mode, set DQS enable by the configuration register2 of OctaFlash. The OSPI only support SOPI mode with enabling DQS.

36.8.3 SOPI模式下的DQS

OctaFlash支持SOPI模式。在SOPI模式下，通过OctaFlash的配置寄存器2设置DQS使能。OSPI仅支持启用DQS的SOPI模式。

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37. CEC Transmission/Reception Circuit (CEC)

37.1 Overview

The CEC transmission/reception circuit can generate and receive CEC signals conforming to the Consumer Electronics Control (CEC) standard, and automatically detect communication statuses by the CEC. CEC transmission/reception can be easily controlled by using these functions.

Table 37.1 lists the CEC specifications and Figure 37.1 shows a block diagram.

Table 37.1 CEC specifications

Parameter	Description
Communication method	Serial communication can be performed that conforms to the Consumer Electronics Control (CEC) standard in the High-Definition Multimedia Interface (HDMI) Ver. 1.4b.
CEC operation clock (f_{CEC})	Selectable from PCLKB/2^5, PCLKB/2^6, PCLKB/2^7, PCLKB/2^8, PCLKB/2^9, PCLKB/2^{10}, CECCLK, and CECCLK/2^8
Interrupt sources	• Data interrupt (INTDA) • Communication complete interrupt (INTCE) • Error interrupt (INTERR) (transmit, ACK, arbitration, timing, underrun, overrun, and bus lock errors)
Other functions	• Communication bit width adjustment function Can be used to set the low-level width and bit width of the start bit and data bit that configure the CEC data frame during transmission. • Count function during signal-free time Can be used to count during the signal-free time (transmission disable period) specified in the CEC standard and set the count period. • Error handling function Can be used to output an error handling pulse by detecting a timing error of the data bit. • Function that restarts reception by detecting the start bit during reception

37. CEC Transmission/Reception Circuit (CEC)

37.1 Overview

CEC发射接收电路可以产生和接收符合消费电子的CEC信号
控制（CEC）标准，并通过CEC自动检测通信状态。使用这些功能可以轻松控制CEC发送接收。

表37.1列出了CEC规范，图37.1显示了框图。

Table 37.1 CEC specifications

Parameter	Description
通讯方式	可以执行符合高清多媒体接口(HDMI)版本中的消费电子控制(CEC)标准的串行通信。1.4b。
CEC操作时钟(fCEC)	可选择PCLKB25、PCLKB26、PCLKB27、PCLKB28、PCLKB29、PCLKB210、CECCLK, and CECCLK/2^8
中断源	• 数据中断(INTDA) • 通信完成中断(INTCE) • 错误中断(INTERR)（发送、ACK、仲裁、计时、欠载、溢出和总线锁定错误 ）
其他功能	• 通讯位宽调整功能 可用于设置在传输过程中配置CEC数据帧的起始位和数据位的低电平宽度和位宽。 • 无信号时间计数功能 可用于在CEC标准中规定的无信号时间（传输禁用时间段）内进行计数并设置计数时间段 。 • 错误处理功能 可用于通过检测数据位的时序错误来输出错误处理脉冲。 • 通过在接收期间检测起始位来重新开始接收的功能

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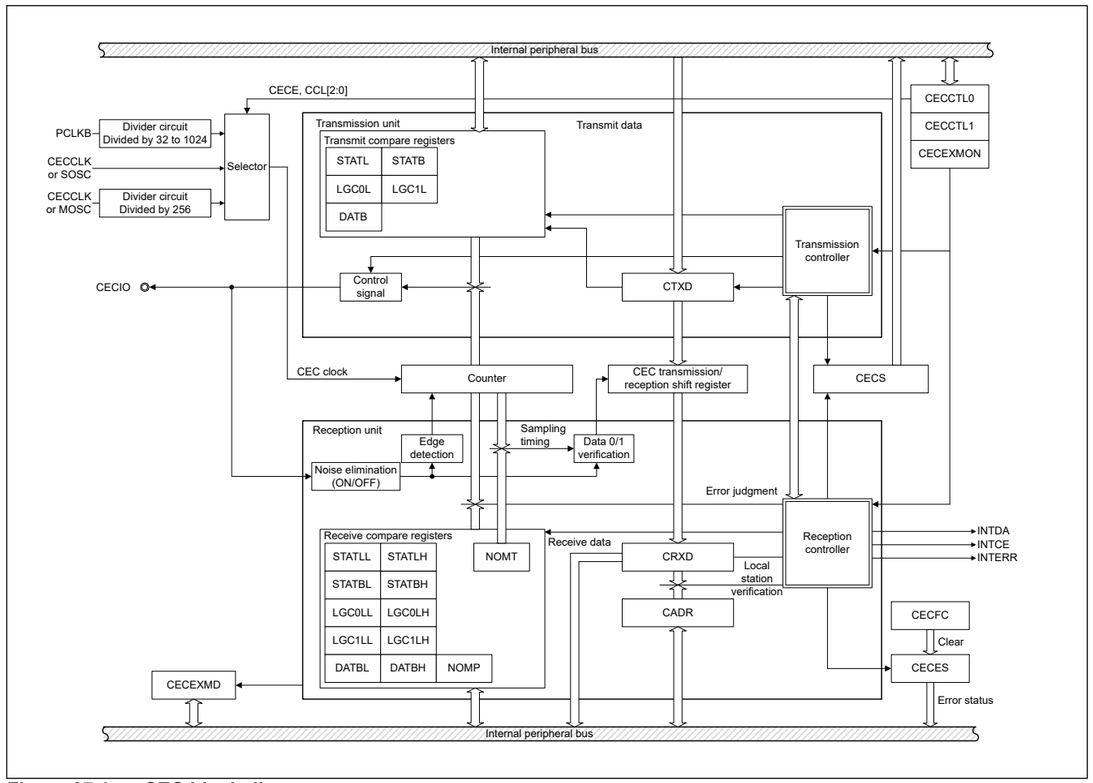
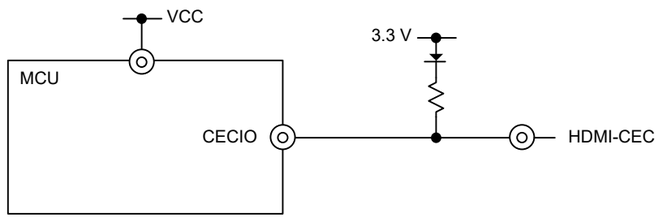


Figure 37.1 CEC block diagram

Figure 37.2 shows an example of I/O pin connection to the external circuit. Table 37.2 lists an I/O pin used for the CEC.



Note: When using the CEC transmission/reception function at a value other than VCC = 3.3 V ± 10%, an external circuit is required to meet the CEC standard value.

Figure 37.2 Example of I/O pin connection to external circuit (When using with Vcc = 3.3 ± 10%)

Table 37.2 CEC pin configuration

Pin name	I/O	Function
CECIO	I/O	CEC data communication

37.1.1 Term Description

- Initiator: Device that transmits or is transmitting CEC messages
- Follower: Device that receives or is receiving CEC messages

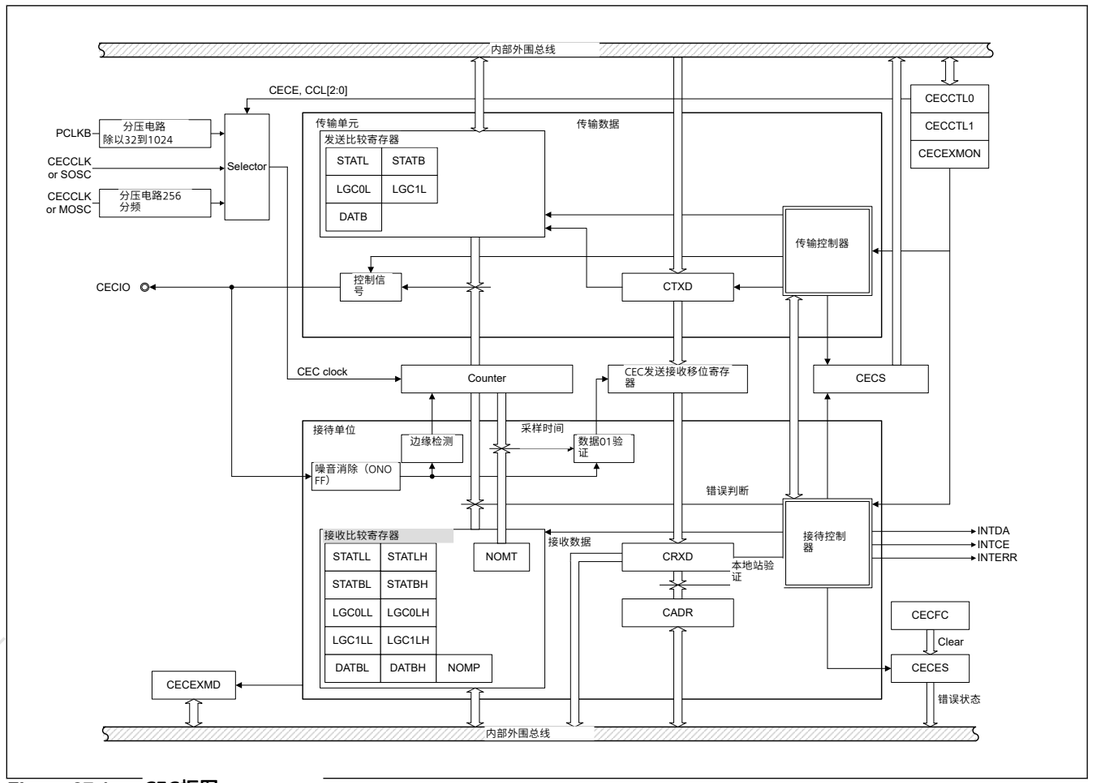
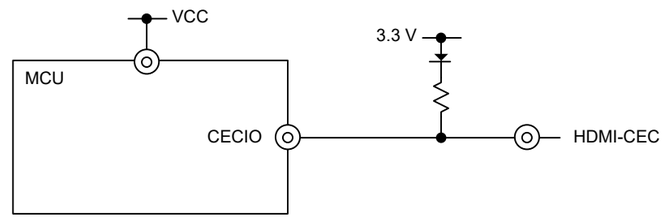


Figure 37.1 CEC框图

图37.2显示了IO引脚连接到外部电路的示例。表37.2列出了用于CEC的IO引脚。



Note: 在VCC=3.3V±10%以外的值使用CEC发送接收功能时，需要外部电路以满足CEC标准值。

Figure 37.2 IO引脚与外部电路的连接示例（使用Vcc=3.3±10%时）

Table 37.2 CEC引脚配置

引脚名称	I/O	Function
CECIO	I/O	CEC数据通信

37.1.1 术语描述

- Initiator：发送或正在发送CEC消息的设备
- Follower：接收或正在接收CEC消息的设备

- Message: All data from the start bit to the operand
- Initiator address: Source address
- Destination address: Destination address
- Direct address communication (direct address message): Communication with one follower
- Broadcast communication (broadcast message): Communication with multiple followers
- Arbitration: Prioritizing devices that output a low level to the CEC line when multiple initiators exist
- Arbitration loss: State in which competing devices are prioritized. At this time, the local station stops transmitting
- Bus free: State in which no communication is performed but transmission can be performed
- Bus busy: During communication
- Error handling: Outputting an error handling pulse (low level with a width of the bit width × 1.5) and transitioning to the communication standby state when a received bit width is shorter than the setting bit width of the data
- ACK/NACK: The logic levels received at the ACK bit timing are as follows:
  ACK: Outputs logical 0
  NACK: Outputs logical 1

(Example) If the initiator outputs logical 1 and the follower outputs logical 0 during an ACK bit period:
Initiator: Transmits a NACK
Follower: Transmits an ACK

Figure 37.3 shows an example of outputting the ACK bit.

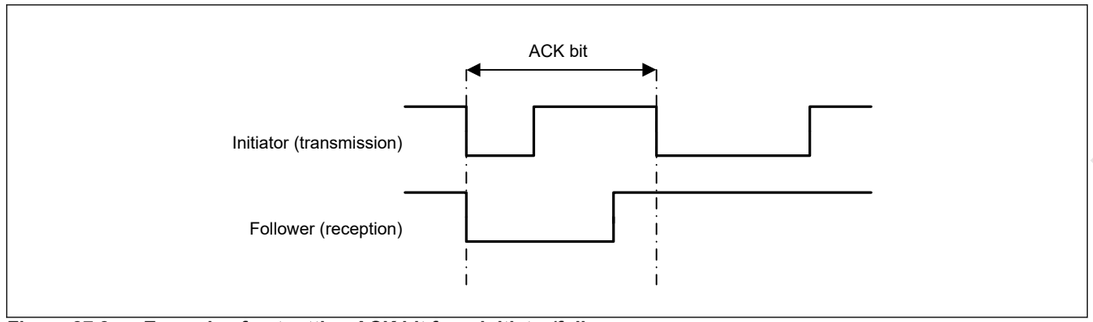


Figure 37.3 Example of outputting ACK bit from initiator/follower

37.2 Register Descriptions

37.2.1 CADR : CEC Local Address Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADR14	ADR13	ADR12	ADR11	ADR10	ADR09	ADR08	ADR07	ADR06	ADR05	ADR04	ADR03	ADR02	ADR01	ADR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADR00	Local Address at Address 0 (TV) 0: Does not set as local address. 1: Sets as local address.	R/W

●Message：从起始位到操作数的所有数据

●发起者地址：源地址

●目的地址：目的地址

●直接地址通讯（directaddressmessage）：与一个跟随者通讯

●广播通信（broadcastmessage）：与多个follower的通信

●仲裁：当存在多个发起方时，优先向CEC线路输出低电平的设备

●仲裁丢失：竞争设备优先的状态。此时本地站停止发射

●Busfree：不进行通信但可以进行传输的状态

●总线忙：通讯中

●错误处理：当接收到的位宽小于数据的设置位宽时，输出一个错误处理脉冲（位宽×1.5的低电平）并转移到通信待机状态

●ACKNACK：在ACK位时序接收到的逻辑电平如下：ACK：输出逻辑0

NACK：输出逻辑1

（示例）如果在ACK位周期内，发起方输出逻辑1，跟随方输出逻辑0：发起方：发送NACK跟随方：发送ACK

图37.3显示了输出ACK位的示例。

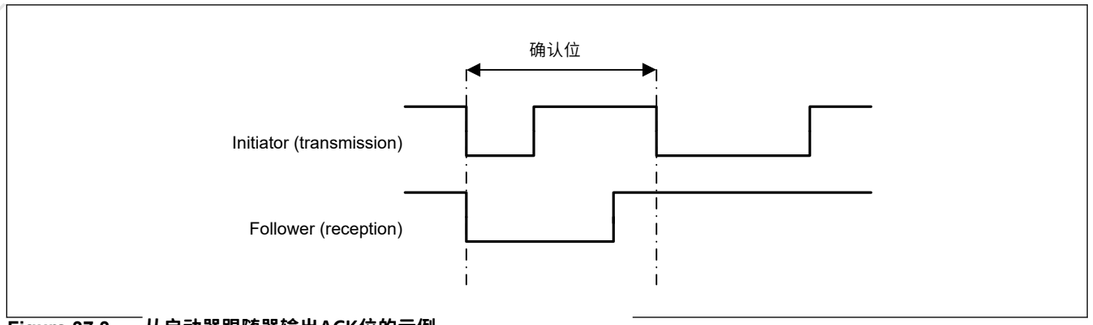


Figure 37.3 从启动器跟随器输出ACK位的示例

37.2 注册说明

37.2.1 CADR:CEC本地地址设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	ADR14	ADR13	ADR12	ADR11	ADR10	ADR09	ADR08	ADR07	ADR06	ADR05	ADR04	ADR03	ADR02	ADR01	ADR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADR00	地址0的本地地址(TV) 0：不设置为本地地址。1：设置为本地地址。	R/W

Bit	Symbol	Function	R/W
1	ADR01	Local Address Setting at Address 1 (recording device 1) 0: Does not set as local address. 1: Sets as local address.	R/W
2	ADR02	Local Address Setting at Address 2 (recording device 2) 0: Does not set as local address. 1: Sets as local address.	R/W
3	ADR03	Local Address Setting at Address 3 (tuner 1) 0: Does not set as local address. 1: Sets as local address.	R/W
4	ADR04	Local Address Setting at Address 4 (playback device 1) 0: Does not set as local address. 1: Sets as local address.	R/W
5	ADR05	Local Address Setting at Address 5 (audio system) 0: Does not set as local address. 1: Sets as local address.	R/W
6	ADR06	Local Address Setting at Address 6 (tuner 2) 0: Does not set as local address. 1: Sets as local address.	R/W
7	ADR07	Local Address Setting at Address 7 (tuner 3) 0: Does not set as local address. 1: Sets as local address.	R/W
8	ADR08	Local Address Setting at Address 8 (playback device 2) 0: Does not set as local address. 1: Sets as local address.	R/W
9	ADR09	Local Address Setting at Address 9 (recording device 3) 0: Does not set as local address. 1: Sets as local address.	R/W
10	ADR10	Local Address Setting at Address 10 (tuner 4) 0: Does not set as local address. 1: Sets as local address.	R/W
11	ADR11	Local Address Setting at Address 11 (playback device 3) 0: Does not set as local address. 1: Sets as local address.	R/W
12	ADR12	Local Address Setting at Address 12 (reserved) 0: Does not set as local address. 1: Sets as local address.	R/W
13	ADR13	Local Address Setting at Address 13 (reserved) 0: Does not set as local address. 1: Sets as local address.	R/W
14	ADR14	Local Address Setting at Address 14 (specific use) 0: Does not set as local address. 1: Sets as local address.	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W

Note: To specify address 15 (unregistered) as the CEC local address, clear the ADR00 to ADR14 bits to 0.
Note: Do not rewrite the set value during communication (CECS.BUSST = 1).

The CADR register is a 16-bit register that sets local addresses. This register is valid only during a reception, the ADR00 to ADR14 bits correspond to CEC logical addresses 0 to 14, and up to 15 local addresses can be set. To specify address 15 as the CEC local address, clear the ADR00 to ADR14 bits to 0. A broadcast address always operates as a local address.

For example, when using addresses 0 as local addresses, set the ADR00 bit to 1.

Bit	Symbol	Function	R/W
1	ADR01	地址1的本地地址设置（记录设备1） 0：不设置为本地地址。1：设置为本地地址。	R/W
2	ADR02	地址2的本地地址设置（记录设备2） 0：不设置为本地地址。1：设置为本地地址。	R/W
3	ADR03	地址3的本地地址设置（调谐器1） 0：不设置为本地地址。1：设置为本地地址。	R/W
4	ADR04	地址4的本地地址设置（播放设备1） 0：不设置为本地地址。1：设置为本地地址。	R/W
5	ADR05	地址5的本地地址设置（音频系统） 0：不设置为本地地址。1：设置为本地地址。	R/W
6	ADR06	地址6的本地地址设置（调谐器2） 0：不设置为本地地址。1：设置为本地地址。	R/W
7	ADR07	地址7的本地地址设置（调谐器3） 0：不设置为本地地址。1：设置为本地地址。	R/W
8	ADR08	地址8的本地地址设置（播放设备2） 0：不设置为本地地址。1：设置为本地地址。	R/W
9	ADR09	地址9的本地地址设置（记录设备3） 0：不设置为本地地址。1：设置为本地地址。	R/W
10	ADR10	地址10的本地地址设置（调谐器4） 0：不设置为本地地址。1：设置为本地地址。	R/W
11	ADR11	地址11的本地地址设置（播放设备3） 0：不设置为本地地址。1：设置为本地地址。	R/W
12	ADR12	地址12的本地地址设置（保留） 0：不设置为本地地址。1：设置为本地地址。	R/W
13	ADR13	地址13的本地地址设置（保留） 0：不设置为本地地址。1：设置为本地地址。	R/W
14	ADR14	地址14的本地地址设置（具体使用） 0：不设置为本地地址。1：设置为本地地址。	R/W
15	—	该位读取为0。写入值应为0。	R/W

Note: 要将地址15（未注册）指定为CEC本地地址，请将ADR00至ADR14位清零。
Note: 通信期间不要改写设定值（CECS.BUSST=1）。

CADR寄存器是一个16位寄存器，用于设置本地地址。该寄存器仅在接收期间有效，ADR00至ADR14位对应CEC逻辑地址0至14，最多可设置15个本地地址。要将地址15指定为CEC本地地址，请将ADR00至ADR14位清除为0。广播地址始终作为本地地址运行。

例如，当使用地址0作为本地地址时，将ADR00位设置为1。

37.2.2 CTXD : CEC Transmission Buffer Register

Base address: CEC = 0x400A_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

The CTXD sequentially transmits 8 bits of data, starting from bit 7 with MSB first. A transmission/reception interrupt request signal (INTDA) is generated at the start timing of the header block and data block. Successive transmission can be performed by writing the next data to the CTXD register before the transmission ends after INTDA is generated.

If an underrun error occurs (UERR = 1), transmission does not continue. An error interrupt is generated and the transmission wait state is entered.

If transmit data is written to this register after a data interrupt (INTDA) is generated during transmission of the last block, the data is invalid.

37.2.3 CRXD : CEC Reception Buffer Register

Base address: CEC = 0x400A_C000

Offset address: 0x41

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	0	0	0	0	0	0	0	0

The CRXD retains receive data that can be read by reading this register. For every byte of data received, new data is transferred from the CEC Reception Shift register.

If an overrun error occurs (CECES.OERR = 1), the data of the reception buffer register will be overwritten.

37.2.4 CECCTL0 : CEC Control Register 0

Base address: CEC = 0x400A_C000

Offset address: 0x45

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CECE	ACKTEN	CCL[2:0]			TXTRG	CECRXEN	EOM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOM	EOM Setting 0: Continues transmission. 1: Last frame	R/W
1	CECRXEN	Reception Enable Control 0: Disables continuing reception or reports abnormal reception. 1: Enables continuing reception or reports normal reception. Table 37.3 lists the reception status and ACK/NACK timing output.	R/W
2	TXTRG	Transmission Start Trigger 0: No effect 1: Starts CEC transmission.	W

37.2.2 CTXD:CEC传输缓冲寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

CTXD依次发送8位数据，从第7位开始，MSB在前。发送接收中断请求信号(INTDA)在标题块和数据块的开始定时产生。在产生INTDA后，在发送结束前将下一个数据写入CTXD寄存器，可以进行连续发送。

如果发生欠载错误(UERR=1)，则传输不会继续。产生错误中断并进入传输等待状态。

如果在最后一个块的传输过程中产生数据中断（INTDA）后将传输数据写入该寄存器，则数据无效。

37.2.3 CRXD:CEC接收缓冲寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x41

Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值:	0	0	0	0	0	0	0	0

CRXD保留可通过读取该寄存器读取的接收数据。对于接收到的每个数据字节，都会从CEC接收移位寄存器传输新数据。

如果发生溢出错误（CECES.OERR=1），接收缓冲寄存器的数据将被覆盖。

37.2.4 CECCTL0:CEC控制寄存器0

Base address: CEC = 0x400A_C000

Offset address: 0x45

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CECE	ACKTEN	CCL[2:0]			TXTRG	CECRXEN	EOM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	EOM	EOM Setting 0：继续发送。1：最后一帧	R/W
1	CECRXEN	接收启用控制 0：禁止继续接收或报告接收异常。1：启用继续接收或报告正常接收。 表37.3列出了接收状态和ACKNACK时序输出。	R/W
2	TXTRG	传输开始触发 0：无效1：开始CEC传输。	W

Bit	Symbol	Function	R/W
5:3	CCL[2:0]	CEC Clock Select*1 0 0 0: PCLKB/2^5 0 0 1: PCLKB/2^6 0 1 0: PCLKB/2^7 0 1 1: PCLKB/2^8 1 0 0: PCLKB/2^9 1 0 1: PCLKB/2^10 1 1 0: CECCLK (when using SOSC) 1 1 1: CECCLK/2^8 (when using MOSC)	R/W
6	ACKTEN	ACK Bit Timing Error (Bit Width) Check Enable*1 0: Does not detect ACK bit timing errors. 1: Detects ACK bit timing errors.	R/W
7	CECE	CEC Operation Enable Flag 0: Disables CEC operation. 1: Enables CEC operation.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

CECCTL0 selects enabling operation, starting transmission, and the operating clock.

EOM bit (EOM Setting)

The next frame after 1 is written to this bit is the last frame.

Set the EOM bit before writing transmit data to the transmission buffer register (CTXD).

Writing to the EOM bit and the transmission buffer register (CTXD) should be set after a data interrupt (INTDA) is generated and before the next data interrupt (INTDA) is generated (timing at which the EOM bit transmission is complete). However, this setting is not required when the data interrupt (INTDA) for the last block is generated.

CECRXEN bit (Reception Enable Control)

Setting the CECRXEN bit to 1 enables reception. Set this bit to 1 after determining the local address (setting the CADR register). Do not rewrite the set value during communication (CECS.BUSST = 1).

Table 37.3 Reception status and ACK/NACK timing output from the status of Reception Enable Control Bit

CECRXEN	Reception Enable Control Bit		
1	Reception status		ACK/NACK timing output
	During direct address reception (to local station)	Normal reception	ACK
		Timing error occurrence	NACK
	During broadcast reception	Normal reception	NACK
		Timing error occurrence	ACK
	During direct address reception (to another station)	Not participating in communication (high-impedance)	
0	Reception status		ACK/NACK timing output
	During direct address reception (to local station)	Normal reception	NACK
		Timing error occurrence	NACK
	During broadcast reception	Normal reception	ACK
		Timing error occurrence	ACK
	During direct address reception (to another station)	Not participating in communication (high-impedance)	

TXTRG bit (Transmission Start Trigger)

Setting TXTRG to 1 starts transmission.

This bit is a trigger bit and the read value is 0.

Bit	Symbol	Function	R/W
5:3	CCL[2:0]	CEC时钟选择*1 0 0 0: PCLKB/2^5 0 0 1: PCLKB/2^6 0 1 0: PCLKB/2^7 0 1 1: PCLKB/2^8 1 0 0: PCLKB/2^9 1 0 1: PCLKB/2^10 1 1 0: CECCLK (when using SOSC) 1 1 1: CECCLK/2^8 (when using MOSC)	R/W
6	ACKTEN	ACKBitTimingError(BitWidth)CheckEnable*1 0：不检测ACK位时序错误。1：检测ACK位时序错误。	R/W
7	CECE	CEC操作启用标志 0：禁用CEC操作。1：启用CEC操作。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

CECCTL0选择使能操作、开始传输和操作时钟。

EOM bit (EOM Setting)

向该位写入1之后的下一帧是最后一帧。

在将发送数据写入发送缓冲寄存器(CTXD)之前设置EOM位。

写入EOM位和发送缓冲寄存器(CTXD)应在数据中断(INTDA)产生之后和下一个数据中断(INTDA)产生之前（EOM位发送完成的时间）置位。但是，当产生最后一个块的数据中断(INTDA)时，不需要此设置。

CECRXEN位（接收使能控制）

将CECRXEN位设置为1使能接收。在确定本地地址（设置CADR寄存器）后将该位设置为1。通信期间不要改写设定值（CECS.BUSST=1）。

Table 37.3 从接收使能控制位的状态输出接收状态和ACKNACK时序

CECRXEN	接收使能控制位		
1	接收状态		ACKNACK定时输出
	直接地址接收期间（本地站）	正常接收	ACK
		发生时序错误	NACK
	广播接收期间	正常接收	NACK
		发生时序错误	ACK
	直接地址接收期间（到另一个站）	不参与通讯（高阻）	
0	接收状态		ACKNACK定时输出
	直接地址接收期间（本地站）	正常接收	NACK
		发生时序错误	NACK
	广播接收期间	正常接收	ACK
		发生时序错误	ACK
	直接地址接收期间（到另一个站）	不参与通讯（高阻）	

TXTRG位（发送开始触发）

将TXTRG设置为1开始传输。

该位为触发位，读取值为0。

Set CECCTL0.TXTRG to 1 only when CEC operation is enabled (CECCTL0.CECE = 1) and the bus is free (CECS.BUSST = 0). Transmission starts no more than three CEC clock cycles after CECCTL0.TXTRG is set to 1.

CCL[2:0] bit (CEC Clock Select)

The CCL[2:0] bits select the CEC clock. Set the frequency of the CEC clock in the range of 23.4375 to 78.125 kHz. Table 37.4 and Table 37.5 show examples of CEC clock settings.

Table 37.4 Examples of CEC clock settings (1)

CEC clock selected	CEC operation clock (f_{CEC})					
	When PCLKB = 50 MHz	When PCLKB = 40 MHz	When PCLKB = 30 MHz	When PCLKB = 20 MHz	When PCLKB = 10 MHz	When PCLKB = 1 MHz
PCLKB/2^5	set prohibited	set prohibited	set prohibited	set prohibited	set prohibited	31.250 kHz
PCLKB/2^6	set prohibited	set prohibited	set prohibited	set prohibited	set prohibited	set prohibited
PCLKB/2^7	set prohibited	set prohibited	set prohibited	set prohibited	78.125 kHz	set prohibited
PCLKB/2^8	set prohibited	set prohibited	set prohibited	78.125 kHz	39.062 kHz	set prohibited
PCLKB/2^9	set prohibited	78.125 kHz	58.593 kHz	39.062 kHz	set prohibited	set prohibited
PCLKB/2^{10}	48.828 kHz	39.062 kHz	29.296 kHz	set prohibited	set prohibited	set prohibited

Table 37.5 Examples of CEC clock settings (2)

CEC clock selected	CEC operation clock (f_{CEC})
CECCLK	32.768 kHz (SOSC selected)
CECCLK/2^8	31.250 kHz to 78.125 kHz (MOSC selected)

ACKTEN bit (ACK Bit Timing Error (Bit Width) Check Enable)

When ACKTEN is set to 1, timing errors are detected for the bit width (the values specified for DATBL and DATBH), in addition to the low-level width of the ACK bit (the values specified for LGC0LL, LGC0LH, LGC1LL, and LGC1LH). However, the maximum bit width (DATBH) is not checked for the ACK bit of the last frame (EOM = 1) even if ACKTEN is 1.

CECE flag (CEC Operation Enable Flag)

Setting CECE to 1 enables CEC operation. Setting this flag to 0 resets the internal block but does not reset control registers.

37.2.5 CECCTL1 : CEC Control Register 1

Base address: CEC = 0x400A_C000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CDFC	CINTMK	BLERRD	STERRD	CESEL[1:0]		SFT[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SFT[1:0]	Signal-Free Time Data Bit Width Select 0 0: 3-data bit width 0 1: 5-data bit width 1 0: 7-data bit width 1 1: Does not detect signal-free time.	R/W

仅当CEC操作使能(CECCTL0.CECE=1)且总线空闲(CECS.BUSST=0)时，才将CECCTL0.TXTRG设置为1。在CECCTL0.TXTRG设置为1后，传输开始不超过三个CEC时钟周期。

CCL[2:0]位（CEC时钟选择）

CCL[2:0]位选择CEC时钟。将CEC时钟的频率设置在23.4375到78.125kHz的范围内。表37.4和表37.5显示了CEC时钟设置的示例。

Table 37.4 CEC时钟设置示例(1)

选择CEC时钟	CEC操作时钟（fCEC）					
	When PCLKB = 50 MHz	When PCLKB = 40 MHz	When PCLKB = 30 MHz	When PCLKB = 20 MHz	When PCLKB = 10 MHz	When PCLKB = 1 MHz
PCLKB/2^5	设置禁止	设置禁止	设置禁止	设置禁止	设置禁止	31.250 kHz
PCLKB/2^6	设置禁止	设置禁止	设置禁止	设置禁止	设置禁止	设置禁止
PCLKB/2^7	设置禁止	设置禁止	设置禁止	设置禁止	78.125 kHz	设置禁止
PCLKB/2^8	设置禁止	设置禁止	设置禁止	78.125 kHz	39.062 kHz	设置禁止
PCLKB/2^9	设置禁止	78.125 kHz	58.593 kHz	39.062 kHz	设置禁止	设置禁止
PCLKB/2^{10}	48.828 kHz	39.062 kHz	29.296 kHz	设置禁止	设置禁止	设置禁止

Table 37.5 CEC时钟设置示例(2)

选择CEC时钟	CEC操作时钟（fCEC）
CECCLK	32.768 kHz (SOSC selected)
CECCLK/2^8	31.250 kHz to 78.125 kHz (MOSC selected)

ACKTEN位（ACK位时序错误（位宽）检查使能）

当ACKTEN设置为1时，除了ACK位的低电平宽度（为LGC0LL、LGC0LH、LGC1LL和LGC1LH指定的值）外，还会检测位宽度（为DATBL和DATBH指定的值）的时序错误）。但是，即使ACKTEN为1，也不检查最后一帧(EOM=1)的ACK位的最大位宽(DATBH)。

CECE标志（CEC操作启用标志）

将CECE设置为1可启用CEC操作。将此标志设置为0会重置内部模块，但不会重置控制寄存器。

37.2.5 CECCTL1:CEC控制寄存器1

Base address: CEC = 0x400A_C000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CDFC	CINTMK	BLERRD	STERRD	CESEL[1:0]		SFT[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SFT[1:0]	无信号时间数据位宽选择 00：3个数据位宽01：5个数据位宽10：7个数据位宽11：不检测无信号时间。	R/W

Bit	Symbol	Function	R/W
3:2	CESEL[1:0]	Communication Complete Interrupt (INTCE) Generation Timing Select*1 0 0: Generates communication complete interrupt once after ACK transmission (reception) of the last frame (EOM = 1) is complete and another time after signal-free time is detected. 0 1: Generates communication complete interrupt after ACK transmission (reception) of the last frame (EOM = 1) is completed. 1 0: Generates communication complete interrupt after signal-free time is detected. 1 1: Setting prohibited	R/W
4	STERRD	Start Bit Error Detection Select*1 0: Does not detect timing errors during start bit reception. 1: Detects timing errors during start bit reception.	R/W
5	BLERRD	Bus Lock Detection Select*1 0: Does not detect sticking of receive data to high or low 1: Detects sticking of receive data to high or low.	R/W
6	CINTMK	CEC Data Interrupt (INTDA) Generation Select*1 0: Does not generate an interrupt when the addresses do not match. 1: Generates an interrupt when the addresses do not match.	R/W
7	CDFC	Digital Filter Select*1 0: Does not use a digital filter. 1: Uses a digital filter.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

The CECCTL1 register selects a digital filter, data interrupt generation, a start bit error interrupt, and whether to generate a communication complete interrupt and when to generate it.

SFT[1:0] bits (Signal-Free Time Data Bit Width Select)

The bit width of the signal-free time is selected by setting the SFT[1:0] bits in the NOMP register. Rewrite these bits only after confirming that the Signal-Free Time Rewrite Disable Report Flag (CECS.SFTST) is 0.

CESEL[1:0] bits (Communication Complete Interrupt (INTCE) Generation Timing Select)

The timing at which a communication complete interrupt (INTCE) is generated, is selected by setting the CESEL[1:0] bits.

STERRD bit (Start Bit Error Detection Select)

The STERRD bit detects timing errors during start bit reception according to the set value of the STATLL, STATLH, STATBL, or STATBH register by setting this bit to 1.

If a timing error occurred, the start bit for which the error occurred is determined to be disabled and communication standby state is entered.

If the STERRD bit is 0, no timing error is detected. All pulses are determined to be start bits.

BLERRD bit (Bus Lock Detection Select)

The bus lock status of the CEC line can be detected by setting the BLERRD bit to 1. If the next falling edge is not input for a period 2.5 times the 1-data bit width set with the NOMP register in a state where the falling edge of the CEC line is awaited (excluding the communication standby state), an error interrupt (INTERR) is generated the Bus Lock Error Detection Flag (BLERR) is set. Afterward, communication standby state is entered.

CINTMK bit (CEC Data Interrupt (INTDA) Generation Select)

The CINTMK bit selects whether to generate INTDA of the header block when the destination address and local address do not match during a reception or to generate INTCE when communication is complete.

CDFC bit (Digital Filter Select)

The CDFC bit eliminates noise from one CEC clock cycle using a digital filter.

Bit	Symbol	Function	R/W
3:2	CESEL[1:0]	通信完成中断(INTCE)发生时序选择*1 00：ACK发送后产生一次通信完成中断 最后一帧（EOM=1）的（接收）完成，并且在检测到信号空闲时间之后的另一个时间。 01：在最后一帧（EOM=1）的ACK发送（接收）完成后产生通信完成中断。 10：检测到无信号时间后产生通信完成中断。11：禁止设定	R/W
4	STERRD	开始位错误检测选择*1 0：在起始位接收期间不检测时序错误。1：在起始位接收期间检测时序错误。	R/W
5	BLERRD	总线锁定检测选择*1 0：不检测接收数据保持高位或低位1：检测接收数据保持高位或低位。	R/W
6	CINTMK	CEC数据中断(INTDA)生成选择*1 0：地址不匹配时不产生中断。1：地址不匹配时产生中断。	R/W
7	CDFC	数字滤波器选择*1 0：不使用数字滤波器。1：使用数字滤波器。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

CECCTL1寄存器选择数字滤波器、数据中断产生、起始位错误中断、是否产生通信完成中断以及何时产生。

SFT[1:0]位（无信号时间数据位宽选择）

通过设置NOMP寄存器中的SFT[1:0]位来选择无信号时间的位宽。只有在确认无信号时间重写禁用报告标志(CECS.SFTST)为0后才重写这些位。

CESEL[1:0]位（通信完成中断（INTCE）产生时序选择）

通过设置CESEL[1:0]位来选择产生通信完成中断(INTCE)的时序。

STERRD位（起始位错误检测选择）

STERRD位根据STATLL、STATLH、
STATBL或STATBH寄存器通过将该位设置为1。

如果发生时序错误，则将发生错误的起始位确定为无效，并进入通信待机状态。

如果STERRD位为0，则未检测到时序错误。所有脉冲都被确定为起始位。

BLRRD位（总线锁定检测选择）

通过将BLRRD位设置为1，可以检测CEC线的总线锁定状态。如果在NOMP寄存器设置的1个数据位宽度的2.5倍期间内没有输入下一个下降沿，则在下降沿状态下等待CEC线的状态（不包括通信待机状态），产生错误中断(INTERR)总线锁定错误检测标志(BLERR)置位。之后，进入通信待机状态。

CINTMK位（CEC数据中断(INTDA)生成选择）

CINTMK位选择是在接收过程中目标地址和本地地址不匹配时生成头块的INTDA，还是在通信完成时生成INTCE。

CDFC位（数字滤波器选择）

CDFC位使用数字滤波器消除一个CEC时钟周期的噪声。

37.2.6 CECS : CEC Communication Status Register

Base address: CEC = 0x400A_C000

Offset address: 0x43

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SFTST	—	—	ITCEF	EOMF	TXST	BUSST	ADRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADRF	Address Match Detection Flag 0: During communication between other stations, while communication is stopped, or while the local station is transmitting 1: During local reception	R
1	BUSST	Bus Busy Detection Flag 0: Bus-free state 1: Bus-busy state	R
2	TXST	Transmission Status Flag 0: During communication standby state or reception (a follower is operating.) 1: During transmission (an initiator is operating.)	R
3	EOMF	EOM Flag 0: The EOM flag received immediately before is logically 0. 1: The EOM flag received immediately before is logically 1.	R
4	ITCEF	INTCE Generation Source Flag 0: Generates a communication complete interrupt (INTCE) if the signal-free time is counted. 1: Generates INTCE if communication is complete or an error is detected.	R
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	SFTST	Signal-Free Time Rewrite Disable Report Flag 0: Enables rewriting CECCTL1.SFT[1:0]. 1: Disables rewriting CECCTL1.SFT[1:0].	R

The CECS register indicates the CEC communication status.

ADRF flag (Address Match Detection Flag)

The ADRF flag checks whether communication is addressed to the local station.

[Setting conditions]

- When the local address and reception destination address match
- When a broadcast address is received

[Clearing conditions]

- When CEC operation is stopped (CECCTL0.CECE = 0)
- When reception is completed

BUSST flag (Bus Busy Detection Flag)

The BUSST flag checks the CEC bus state.

[Setting conditions]

- When a fall of the CEC line is detected
- When the status CEC operation is stopped changes to CEC operation is enabled (CECCTL0.CECE is changed from 0 to 1)

[Clearing conditions]

- When CEC operation is stopped (CECCTL0.CECE = 0)

37.2.6 CECS:CEC通信状态寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x43

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SFTST	—	—	ITCEF	EOMF	TXST	BUSST	ADRF
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ADRF	地址匹配检测标志 0：其他站通信中、通信停止中、本站发送中 1：在本地接收期间	R
1	BUSST	总线忙检测标志 0: Bus-free state 1: Bus-busy state	R
2	TXST	传输状态标志 0：通信待机或接收中（追随者动作中）1：发送中（发起者动作中）	R
3	EOMF	EOM Flag 0：之前接收到的EOM标志在逻辑上为0。1：之前接收到的EOM标志在逻辑上为1。	R
4	ITCEF	INTCE生成源标志 0：如果对无信号时间进行计数，则生成通信完成中断(INTCE)。 1：如果通信完成或检测到错误，则生成INTCE。	R
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	SFTST	无信号时间重写禁用报告标志 0：启用重写CECCTL1.SFT[1:0]。1：禁止重写CECCTL1.SFT[1:0]。	R

CECS寄存器指示CEC通信状态。

ADRF标志（地址匹配检测标志）

ADRF标志检查通信是否寻址到本地站。

[Setting conditions]

●当本地地址和接收目的地地址匹配时

●收到广播地址时

[Clearing conditions]

●CEC操作停止时(CECCTL0.CECE=0)

●接收完成时

BUSST标志（总线忙检测标志）

BUSST标志检查CEC总线状态。

[Setting conditions]

●当检测到CEC线路下降时

●当状态CEC操作停止时变为CEC操作启用（CECCTL0.CECE从0变为1）

[Clearing conditions]

●CEC操作停止时(CECCTL0.CECE=0)

RA生态工作室

- When the signal-free time has elapsed after communication has ended

TXST flag (Transmission Status Flag)

The TXST flag checks whether transmission is in progress.

EOMF flag (EOM Flag)

The EOMF flag checks the value of the bit received immediately before. The value is updated each time a data interrupt (INTDA) is generated.

ITCEF flag (INTCE Generation Source Flag)

By checking the ITCEF flag after INTCE is generated, it can be determined which case is the interrupt generation source that the signal-free time is counted, communication ends, or an error is detected. This setting is enabled only if CECCTL1.CESEL[1:0] are cleared to 0.

SFTST flag (Signal-Free Time Rewrite Disable Report Flag)

The SFTST flag checks whether rewriting CECCTL1.SFT[1:0] is enabled or disabled.

[Setting condition]

- When a write access to CECCTL1 is performed

[Clearing conditions]

- When CEC operation is stopped (CECCTL0.CECE = 0)
- When the CECCTL1.SFT[1:0] rewrite disable period has elapsed

37.2.7 CECES : CEC Communication Error Status Register

Base address: CEC = 0x400A C000

Offset address: 0x42

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	BLERR	AERR	TXERR	TERR	ACKERR	UERR	OERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OERR	Overrun Error Detection Flag 0: No overrun error has occurred. 1: An overrun error has occurred.	R
1	UERR	Underrun Error Detection Flag 0: No underrun error has occurred. 1: An underrun error has occurred.	R
2	ACKERR	ACK Error Detection Flag 0: No ACK error has occurred. 1: An ACK error has occurred.	R
3	TERR	Timing Error Detection Flag 0: No timing error has occurred. 1: A timing error has occurred.	R
4	TXERR	Transmission Error Detection Flag*1 0: No transmission error has occurred. 1: A transmission error has occurred.	R
5	AERR	Arbitration Loss Detection Flag 0: No arbitration loss has occurred. 1: An arbitration loss has occurred.	R

●通信结束后经过无信号时间时

TXST标志（传输状态标志）

TXST标志检查传输是否正在进行。

EOMF flag (EOM Flag)

EOMF标志检查之前收到的位的值。每次产生数据中断(INTDA)时都会更新该值。

ITCEF标志（INTCE生成源标志）

通过在INTCE产生后检查ITCEF标志位，可以判断是中断产生源是计数无信号时间、通信结束还是检测到错误。仅当CECCTL1.CESEL[1:0]被清除为0时才启用此设置。

SFTST标志（无信号时间重写禁用报告标志）

SFTST标志检查重写CECCTL1.SFT[1:0]是启用还是禁用。

[Setting condition]

●对CECCTL1进行写访问时

[Clearing conditions]

●CEC操作停止时(CECCTL0.CECE=0)

●当CECCTL1.SFT[1:0]重写禁止周期已过时

37.2.7 CECES:CEC通信错误状态寄存器

Base address: CEC = 0x400A C000

Offset address: 0x42

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	BLERR	AERR	TXERR	TERR	ACKERR	UERR	OERR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OERR	溢出错误检测标志 0：未发生溢出错误。1：发生溢出错误。	R
1	UERR	欠载错误检测标志 0：未发生欠载错误。1：发生欠载错误。	R
2	ACKERR	ACK错误检测标志 0：未发生ACK错误。1：发生ACK错误。	R
3	TERR	定时错误检测标志 0：未发生时序错误。1：发生时序错误。	R
4	TXERR	传输错误检测标志*1 0：未发生传输错误。1：发生传输错误。	R
5	AERR	仲裁丢失检测标志 0：未发生仲裁丢失。1：仲裁失败。	R

Bit	Symbol	Function	R/W
6	BLERR	Bus Lock Error Detection Flag 0: No bus lock error has occurred. 1: A bus lock error has occurred.	R
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Transmission errors are not detected while transmitting the start bit and ACK bit.

CECES indicates whether a bus lock error, arbitration loss, transmission error, timing error, ACK error, underrun error, or overrun error is detected.

OERR flag (Overrun Error Detection Flag)

The OERR flag checks whether an overrun has occurred.

[Setting condition]

- When the next receive operation completes before the receive data stored in the reception buffer register (CRXD) is read

[Clearing condition]

- When 1 is written to CECFC.OCTRG

UERR flag (Underrun Error Detection Flag)

The UERR flag checks whether an underrun has occurred.

[Setting condition]

- When transmit data is not written to the transmission buffer register (CTXD) after a data interrupt (INTDA) is generated and before the next interrupt (INTDA) is generated

[Clearing condition]

- When 1 is written to CECFC.UCTRG

ACKERR flag (ACK Error Detection Flag)

The ACKERR flag checks whether an ACK error has occurred.

[Setting conditions]

- When logical 1 is received at the ACK bit timing during a direct address communication
- When logical 0 is received at the ACK bit timing during a broadcast communication
- When logical 1 is received at the ACK bit timing during a logical address allocation transmission

[Clearing condition]

- When 1 is written to CECFC.ACKCTRG

TERR flag (Timing Error Detection Flag)

The TERR flag checks whether a timing error has occurred.

[Setting condition]

- When a violation is detected in the timing check of the received data

[Clearing condition]

- When 1 is written to CECFC.TCTRG

TXERR flag (Transmission Error Detection Flag)

The TXERR flag checks whether a transmission error has occurred.

[Setting condition]

- When the logic of the transmit and receive data are compared and do not match when the initiator is operating

Bit	Symbol	Function	R/W
6	BLERR	总线锁定错误检测标志 0：未发生总线锁定错误。1：发生总线锁定错误。	R
7	—	该位读取为0。写入值应为0。	R/W

注1.发送起始位和ACK位时不会检测到发送错误。

CECES指示是否检测到总线锁定错误、仲裁丢失、传输错误、定时错误、ACK错误、欠载错误或溢出错误。

OERR标志（溢出错误检测标志）

OERR标志检查是否发生了溢出。

[Setting condition]

●在接收缓冲寄存器（CRXD）中存储的接收数据被读取之前下一个接收操作完成时

[Clearing condition]

●CECFC.OCTRG写入1时

UERR标志（欠载错误检测标志）

UERR标志检查是否发生了欠载。

[Setting condition]

●发生数据中断（INTDA）后和下一个中断（INTDA）发生前，未将发送数据写入发送缓冲寄存器（CTXD）时

[Clearing condition]

●CECFC.UCTRG写入1时

ACKERR标志（ACK错误检测标志）

ACKERR标志检查是否发生了ACK错误。

[Setting conditions]

●在直接地址通信期间，在ACK位定时接收到逻辑1时

●在广播通信中，在ACK位定时接收到逻辑0时

●在逻辑地址分配传输过程中，在ACK位定时接收到逻辑1时

[Clearing condition]

●CECFC.ACKCTRG写入1时

TERR标志（定时错误检测标志）

TERR标志检查是否发生了计时错误。

[Setting condition]

●在接收数据的时序检查中检测到违规时

[Clearing condition]

●CECFC.TCTRG写入1时

TXERR标志（传输错误检测标志）

TXERR标志检查是否发生了传输错误。

[Setting condition]

●当发起方运行时，比较发送和接收数据的逻辑不匹配时

[Clearing condition]

- When 1 is written to CECFC.TXCTRG

AERR flag (Arbitration Loss Detection Flag)

The AERR flag checks whether arbitration is lost.

[Setting condition]

- When arbitration loss occurs between start bit transmission and initiator address transmission

[Clearing condition]

- When 1 is written to CECFC.ACTRG

BLERR flag (Bus Lock Error Detection Flag)

The BLERR flag checks whether a bus lock error has occurred.

[Setting condition]

- When the next falling edge is not input for a period of 2.5 times the 1-data bit width set by the NOMP register after the falling edge of the CEC reception signal and while the CEC reception signal is fixed to low or high midway through a frame

[Clearing condition]

- When 1 is written to CECFC.BLCTRG

37.2.8 CECFC : CEC Communication Error Flag Clear Trigger Register

Base address: CEC = 0x400A_C000

Offset address: 0x44

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	BLCTRG	ACTRG	TXCTRG	TCTRG	ACKCTRG	UCTRG	OCTRG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OCTRG	Overrun Error Detection Flag Clear Trigger*1 0: Does not clear overrun error detection flag. 1: Clears overrun error detection flag.	W
1	UCTRG	Underrun Error Detection Flag Clear Trigger*1 0: Does not clear underrun error detection flag. 1: Clears underrun error detection flag.	W
2	ACKCTRG	ACK Error Detection Flag Clear Trigger*1 0: Does not clear ACK error detection flag. 1: Clears ACK error detection flag.	W
3	TCTRG	Timing Error Detection Flag Clear Trigger*1 0: Does not clear timing error detection flag. 1: Clears timing error detection flag.	W
4	TXCTRG	Transmission Error Detection Flag Clear Trigger*1 0: Does not clear transmission error detection flag. 1: Clears transmission error detection flag.	W
5	ACTRG	Arbitration Loss Detection Flag Clear Trigger*1 0: Does not clear arbitration loss detection flag. 1: Clears arbitration loss detection flag.	W
6	BLCTRG	Bus Lock Error Detection Flag Clear Trigger*1 0: Does not clear bus lock error detection flag. 1: Clears bus lock error detection flag.	W

[Clearing condition]

●CECFC.TXCTRG写入1时

AERR标志（仲裁丢失检测标志）

AERR标志检查仲裁是否丢失。

[Setting condition]

●当起始位传输和发起地址传输之间发生仲裁丢失时

[Clearing condition]

●CECFC.ACTRG写入1时

BLERR标志（总线锁定错误检测标志）

BLERR标志检查是否发生了总线锁定错误。

[Setting condition]

●在CEC接收信号的下降沿之后，在NOMP寄存器设置的1个数据位宽度的2.5倍的时间内没有输入下一个下降沿，并且CEC接收信号在中途固定为低电平或高电平时框架

[Clearing condition]

●CECFC.BLCTRG写入1时

37.2.8 CECFC:CEC通信错误标志清除触发寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x44

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	BLCTRG	ACTRG	TXCTRG	TCTRG	ACKCTRG	UCTRG	OCTRG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OCTRG	溢出错误检测标志清除触发*1 0：不清除溢出错误检测标志。1：清除溢出错误检测标志。	W
1	UCTRG	欠载错误检测标志清除触发*1 0：不清除欠载错误检测标志。1：清除欠载错误检测标志。	W
2	ACKCTRG	ACK错误检测标志清除触发*1 0：不清除ACK错误检测标志。1：清除ACK错误检测标志。	W
3	TCTRG	定时错误检测标志清除触发*1 0：不清除定时错误检测标志。1：清除时序错误检测标志。	W
4	TXCTRG	传送错误检测标志清除触发*1 0：不清除传输错误检测标志。1：清除传输错误检测标志。	W
5	ACTRG	仲裁丢失检测标志清除触发*1 0：不清除仲裁丢失检测标志。1：清除仲裁丢失检测标志。	W
6	BLCTRG	总线锁定错误检测标志清除触发*1 0：不清除总线锁定错误检测标志。1：清除总线锁定错误检测标志。	W

Bit	Symbol	Function	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. The read value is 0.

The CECFC register clears error detection flags written to the communication error status register (CECES). Only the set bits can be cleared by setting 1 to each flag.

37.2.9 STATL : CEC Transmission Start Bit Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x06

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATL[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATL[8:0]	CEC Transmission Start Bit Low Width Setting*1 Low-level width of the start bit during a transmission Low-level width = (set value of STATL[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.10 STATB : CEC Transmission Start Bit Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATB[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATB[8:0]	CEC Transmission Start Bit Width Setting*1 Bit width of the start bit during a transmission Bit width = (set value of STATB[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.11 LGC0L : CEC Transmission Logical 0 Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x08

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC0L[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7	—	该位读取为0。写入值应为0。	R/W

注1.读取值为0。

CECFC寄存器清除写入通信错误状态寄存器(CECES)的错误检测标志。通过将每个标志设置为1，只能清除设置的位。

37.2.9 STATL:CEC传输起始位低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x06

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATL[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATL[8:0]	CEC发送起始位低宽度设置*1 传输期间起始位的低电平宽度 低电平宽度=(STATL[8:0]位的设置值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.10 STATB:CEC发送起始位宽设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATB[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATB[8:0]	CEC发送起始位宽设置*1 传输期间起始位的位宽 位宽=(STATB[8:0]位的设置值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.11 LGC0L:CEC传输逻辑0低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x08

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC0L[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC0L[8:0]	CEC Transmission Logical 0 Low Width Setting*1 Low-level width of logical 0 during a transmission Low-level width = (set value of LGC0L[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.12 LGC1L : CEC Transmission Logical 1 Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x0A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC1L[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC1L[8:0]	CEC Transmission Logical 1 Low Width Setting*1 Low-level width of logical 1 during a transmission Low-level width = (set value of LGC1L[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.13 DATB : CEC Transmission Data Bit Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x0C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DATB[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DATB[8:0]	CEC Transmission Data Bit Width Setting*1 Bit width of the data bit during a transmission 1-data bit width = (set value of DATB[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.14 STATLL : CEC Reception Start Bit Minimum Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATLL[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC0L[8:0]	CEC传输逻辑0低宽度设置*1 传输过程中逻辑0的低电平宽度 低电平宽度=(LGC0L[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.12 LGC1L:CEC传输逻辑1低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x0A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC1L[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC1L[8:0]	CEC传输逻辑1低宽度设置*1 传输过程中逻辑1的低电平宽度 低电平宽度=(LGC1L[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.13 DATB:CEC传输数据位宽设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x0C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DATB[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DATB[8:0]	CEC传输数据位宽设置*1 传输期间数据位的位宽1-数据位宽=(DATB[8:0]位的设置值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.14 STATLL:CEC接收起始位最小低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x10

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATLL[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATLL[8:0]	CEC Reception Start Bit Minimum Low Width Setting*1 Minimum value of the low-level width of the start bit during a reception Low-level width = (set value of STATLL[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: The value of this register is not used when the timing of the start bit is not checked (CECCTL1.STERRD = 0) and restarting reception on start detection is not enabled (CECEXMOD.RERCVEN = 0). The set value is invalid.
Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.15 STATLH : CEC Reception Start Bit Maximum Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x12

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATLH[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATLH[8:0]	CEC Reception Start Bit Maximum Bit Width Setting*1 Maximum value of the low-level width of the start bit during R/W a reception Low-level width = (set value of STATLH[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: The value of this register is not used when the timing of the start bit is not checked (CECCTL1.STERRD = 0) and restarting reception on start detection is not enabled (CECEXMOD.RERCVEN = 0). The set value is invalid.
Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.16 STATBL : CEC Reception Start Bit Minimum Bit Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATBL[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATBL[8:0]	CEC Reception Start Bit Minimum Bit Width Setting*1 Minimum value of the bit width of the start bit during a reception Bit width = (set value of STATBL[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: The value of this register is not used when the timing of the start bit is not checked (CECCTL1.STERRD = 0) and restarting reception on start detection is not enabled (CECEXMOD.RERCVEN = 0). The set value is invalid.
Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

Bit	Symbol	Function	R/W
8:0	STATLL[8:0]	CEC接收起始位最小低宽度设置*1 接收时起始位低电平宽度的最小值低电平宽度=(STATLL[8:0]位的设置值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 当未检查启动位的时序(CECCTL1.STERRD=0)并且未启用启动检测时重新启动接收(CECEXMOD.RERCVEN=0)时，不使用该寄存器的值。设定值无效。
注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.15 STATLH：CEC接收起始位最大低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x12

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATLH[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATLH[8:0]	CEC接收起始位最大位宽设置*1 RWa接收时起始位低电平宽度的最大值 低电平宽度=(STATLH[8:0]位的设置值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 当未检查启动位的时序(CECCTL1.STERRD=0)并且未启用启动检测时重新启动接收(CECEXMOD.RERCVEN=0)时，不使用该寄存器的值。设定值无效。
注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.16 STATBL:CEC接收起始位最小位宽设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATBL[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATBL[8:0]	CEC接收起始位最小位宽设置*1 接收期间起始位的位宽最小值位宽=(STATBL[8:0]位的设置值+1)× CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 当未检查启动位的时序(CECCTL1.STERRD=0)并且未启用启动检测时重新启动接收(CECEXMOD.RERCVEN=0)时，不使用该寄存器的值。设定值无效。
注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.17 STATBH : CEC Reception Start Bit Maximum Bit Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATBH[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATBH[8:0]	CEC Reception Start Bit Maximum Bit Width Setting*1 Maximum value of the bit width of the start bit during a reception reception Bit width = (set value of STATBH[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note: The value of this register is not used when the timing of the start bit is not checked (CECCTL1.STERRD = 0) and restarting reception on start detection is not enabled (CECEXMOD.RERCVEN = 0). The set value is invalid.

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.18 LGC0LL : CEC Reception Logical 0 Minimum Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC0LL[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC0LL[8:0]	CEC Reception Logical 0 Minimum Low Width Setting*1 Minimum value of the low-level width of logical 0 during a reception Low-level width = (set value of LGC0LL[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.19 LGC0LH : CEC Reception Logical 0 Maximum Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC0LH[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC0LH[8:0]	CEC Reception Logical 0 Minimum Low Width Setting*1 Maximum value of the low-level width of logical 0 during a reception Low-level width = (set value of LGC0LH[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.17 STATBH:CEC接收起始位最大位宽设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	STATBH[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	STATBH[8:0]	CEC接收起始位最大位宽设置*1 接收时起始位的位宽最大值位宽=(STATBH[8:0]位的设置值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

Note: 当未检查启动位的时序(CECCTL1.STERRD=0)并且未启用启动检测时重新启动接收(CECEXMOD.RERCVEN=0)时，不使用该寄存器的值。设定值无效。

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.18 LGC0LL:CEC接收逻辑0最小低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC0LL[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC0LL[8:0]	CEC接收逻辑0最小低宽度设置*1 接收期间逻辑0低电平宽度的最小值 低电平宽度=(LGC0LL[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.19 LGC0LH:CEC接收逻辑0最大低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC0LH[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC0LH[8:0]	CEC接收逻辑0最小低宽度设置*1 接收过程中逻辑0的低电平宽度最大值 低电平宽度=(LGC0LH[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.20 LGC1LL : CEC Reception Logical 1 Minimum Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC1LL[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC1LL[8:0]	CEC Reception Logical 1 Minimum Low Width Setting*1 Minimum value of the low-level width of logical 1 during a reception Low-level width = (set value of LGC1LL[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.21 LGC1LH : CEC Reception Logical 1 Maximum Low Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x1E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC1LH[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC1LH[8:0]	CEC Reception Logical 1 Maximum Low Width Setting*1 Maximum value of the low-level width of logical 1 during a reception Low-level width = (set value of LGC1LH[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.22 DATBL : CEC Reception Data Bit Minimum Bit Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x20

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DATBL[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DATBL[8:0]	CEC Reception Data Bit Minimum Bit Width Setting*1 Minimum value of the bit width of the data bit during a reception Bit width = (set value of DATBL[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.20 LGC1LL:CEC接收逻辑1最小低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC1LL[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC1LL[8:0]	CEC接收逻辑1最小低宽度设置*1 接收期间逻辑1的低电平宽度的最小值 低电平宽度=(LGC1LL[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.21 LGC1LH:CEC接收逻辑1最大低宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x1E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	LGC1LH[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	LGC1LH[8:0]	CEC接收逻辑1最大低宽度设置*1 接收过程中逻辑1的低电平宽度最大值 低电平宽度=(LGC1LH[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.22 DATBL:CEC接收数据位最小位宽设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x20

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DATBL[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DATBL[8:0]	CEC接收数据位最小位宽设置*1 接收期间数据位的位宽最小值位宽=(DATBL[8:0]位的设置值+1)× CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.23 DATBH : CEC Reception Data Bit Maximum Bit Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x22

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DATBH[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DATBH[8:0]	CEC Reception Data Bit Maximum Bit Width Setting*1 Maximum value of the bit width of the data bit during a reception Bit width = (set value of DATBH[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

37.2.24 NOMT : CEC Reception Data Sampling Time Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NOMT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	NOMT[8:0]	CEC Reception Data Sampling Time Setting*1, *2 Sampling time of received data Sampling time = (set value of NOMT[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).
Note 2. Set this register within a period of LGC1LH < NOMT < LGC0LL.

37.2.25 NOMP : CEC Data Bit Reference Width Setting Register

Base address: CEC = 0x400A_C000

Offset address: 0x24

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NOMP[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	NOMP[8:0]	CEC Data Bit Reference Width Setting*1 1-data bit width Bit width = (set value of NOMP[8:0] bits + 1) × CEC clock cycle	R/W
15:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

This 1-data bit width is used when counting the number of bits for errors handling, signal-free time, and bus locking detection.

37.2.23 DATBH:CEC接收数据位最大位宽设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x22

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	DATBH[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	DATBH[8:0]	CEC接收数据位最大位宽设置*1 接收期间数据位的位宽最大值位宽=(DATBH[8:0]位的设置值+1)× CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

37.2.24 NOMT:CEC接收数据采样时间设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x0E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NOMT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	NOMT[8:0]	CEC接收数据采样时间设置*1 *2 接收数据的采样时间 采样时间=(NOMT[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。
注2.在LGC1LH<NOMT<LGC0LL期间设置该寄存器。

37.2.25 NOMP:CEC数据位参考宽度设置寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x24

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NOMP[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
8:0	NOMP[8:0]	CEC数据位参考宽度设置*1 1-数据位宽位宽=(NOMP[8:0]位的设定值+1)×CEC时钟周期	R/W
15:9	—	这些位被读取为0。写入值应为0。	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

在计算错误处理、无信号时间和总线锁定检测的位数时，使用该1数据位宽度。

37.2.26 CECEXMD : CEC Extension Mode Register

Base address: CEC = 0x400A_C000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RCVINTDSEL	—	RERCVEN	LERPLEN	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	LERPLEN	Pulse Output Function Enable by Long Bit Width Error*1 0: Detects only a long bit width error. 1: Detects a long bit width error and outputs an error handling pulse.	R/W
5	RERCVEN	Start Detection Reception Restart Enable*1 0: Does not restart reception when the start bit is detected during reception. 1: Restarts reception when the start bit is detected during reception.	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	RCVINTDSEL	INTDA Reception Interrupt Timing Change*1 0: EOM timing (9th bit of data) 1: ACK timing (10th bit of data)	R/W

Note 1. Rewritable only when CEC operation is stopped (CECCTL0.CECE = 0).

This register is used to control enabling of error handling when a long bit error is detected, restarting of reception by detecting a start bit, and selecting of the timing for generating reception interrupts.

37.2.27 CECEXMON : CEC Extension Monitor Register

Base address: CEC = 0x400A_C000

Offset address: 0x2A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ACKF	CECLNMON
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	CECLNMON	CEC Line Monitor*1 0: Low level 1: High level	R
1	ACKF	ACK Flag*2 The value of the received ACK bit can be read. The value is updated at the timing of ACK reception regardless of transmission/reception or address match/mismatch during reception. However, the value is not updated if an error is detected before an ACK is received. The value is updated when an ACK is received at the next communication.	R
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When using the value of the CECEXMON.CECLNMON bit, determine the value after matching two or three times.
Note 2. When using the CECEXMON.ACKF bit, the relationship between the read timing and the read value changes depending on the value of the CECEXMD.RCVINTDSEL bit.

This register can be used to read the CEC line and the ACK flag.

37.2.26 CECEXMD:CEC扩展模式寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x28

Bit position:	7	6	5	4	3	2	1	0
Bit field:	RCVINTDSEL	—	RERCVEN	LERPLEN	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	LERPLEN	通过长位宽错误启用脉冲输出功能*1 0：仅检测长位宽错误。1：检测长位宽错误并输出错误处理脉冲。	R/W
5	RERCVEN	启动检测接收重启启用*1 0：在接收过程中检测到起始位时不重新开始接收。1：在接收过程中检测到起始位时重新开始接收。	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	RCVINTDSEL	INTDA接收中断时序改变*1 0：EOM时序（第9位数据）1：ACK时序（第10位数据）	R/W

注1.仅当CEC操作停止时可重写(CECCTL0.CECE=0)。

该寄存器用于控制检测到长位错误时的错误处理启用、通过检测起始位重新启动接收以及选择产生接收中断的时序。

37.2.27 CECEXMON:CEC扩展监控寄存器

Base address: CEC = 0x400A_C000

Offset address: 0x2A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ACKF	CECLNMON
重置后的值:	0	0	0	0	0	0	0	x

Bit	Symbol	Function	R/W
0	CECLNMON	CEC线路监视器*1 0：低电平1 ：高电平	R
1	ACKF	确认标志*2 可以读取接收到的ACK位的值。 无论发送接收或接收期间的地址匹配不匹配如何，都会在ACK接收定时更新该值。但是，如果在收到ACK之前检测到错误，则不会更新该值。在下一次通信中收到ACK时更新该值。	R
7:2	—	这些位被读取为0。写入值应为0。	R/W

注1.使用CECEXMON.CECLNMON位的值时，匹配2次或3次后确定值。
注2.使用CECEXMON.ACKF位时，读取时序和读取值之间的关系会根据CECEXMD.RCVINTDSEL位的值而变化。

该寄存器可用于读取CEC线和ACK标志。

CECLNMON bit (CEC Line Monitor)

The CEC pin state can be read by reading this bit. When using the value of this bit, determine the value after a match of two or three times.

ACKF flag (ACK Flag)

The value of the received ACK bit can be read by reading this bit. When using this bit, the relationship between the read timing and the read value changes depending on the value of the CECEXMD.RCVINTDSEL bit.

Figure 37.4 shows the ACKF flag update timing and reception interrupt generation timing.

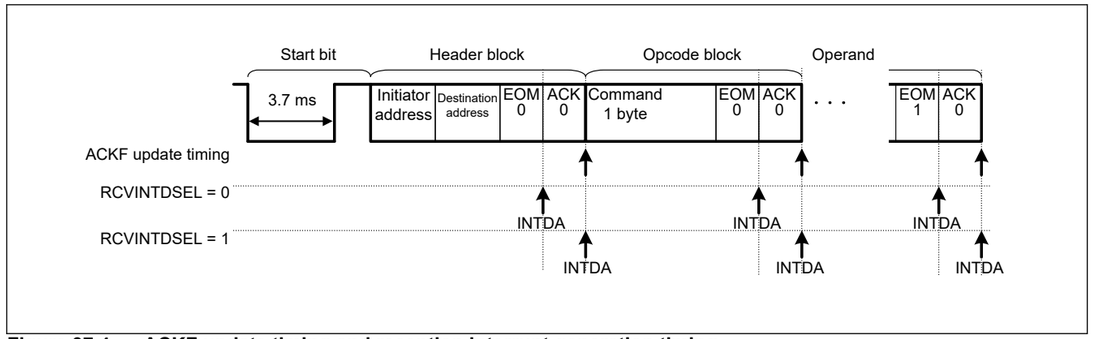


Figure 37.4 ACKF update timing and reception interrupt generation timing

When reading the ACKF bit while RCVINTDSEL = 0, the received ACK state can be read by reading this bit when a 1-bit wait time has elapsed after a reception interrupt is generated. If this bit is read after a reception interrupt is generated, the ACK of the previously received data is read.

When reading the ACKF bit while RCVINTDSEL = 1, read this bit after a reception interrupt is generated. The ACK of the newest received data can be read.

37.3 Operation

37.3.1 Operation of CEC Transmission/Reception Circuit

37.3.1.1 CEC Transmission/Reception Data Format

Figure 37.5 shows the basic CEC communication format. A CEC data frame consists of a start bit, a header block, data block 1 (opcode), and data block 2 (operand). The three blocks other than the start bit consist of 10 bits.

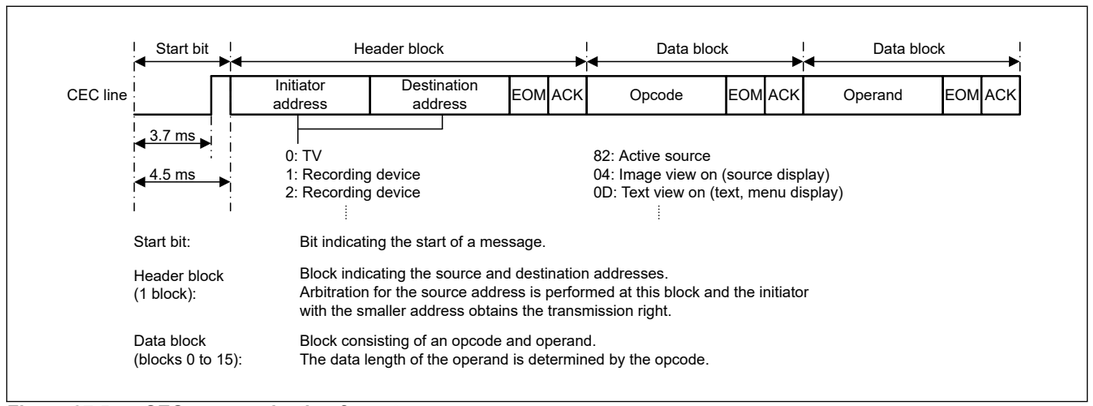


Figure 37.5 CEC communication format

CECLNMON位（CEC线路监视器）

通过读取该位可以读取CEC引脚状态。使用该位的值时，匹配两三次后确定值。

ACKF flag (ACK Flag)

通过读取该位可以读取接收到的ACK位的值。使用该位时，读取时序和读取值之间的关系会根据CECEXMD.RCVINTDSEL位的值而变化。

图37.4显示了ACKF标志更新时序和接收中断产生时序。

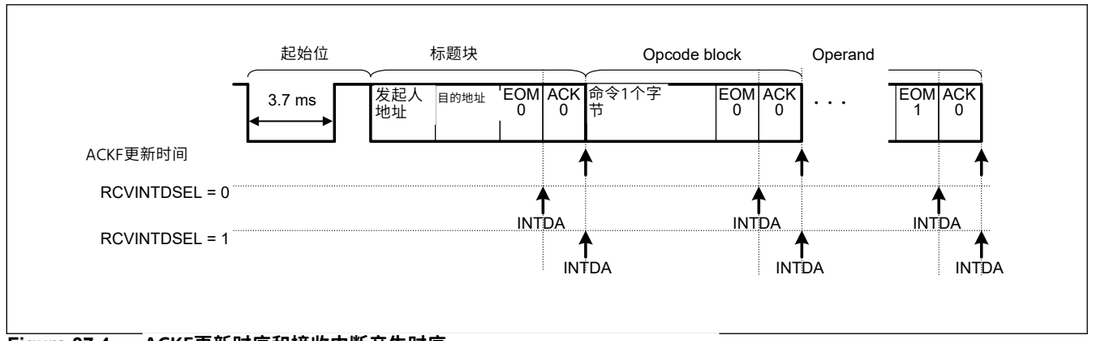


Figure 37.4 ACKF更新时序和接收中断产生时序

在RCVINTDSEL=0时读取ACKF位时，在产生接收中断后经过1位等待时间后，可以通过读取该位读取接收到的ACK状态。如果在产生接收中断后读取该位，则读取先前接收数据的ACK。

在RCVINTDSEL=1时读取ACKF位时，在产生接收中断后读取该位。可以读取最新接收数据的ACK。

37.3 Operation

37.3.1 CEC发送接收电路的操作

37.3.1.1 CEC发送接收数据格式

图37.5显示了基本的CEC通信格式。一个CEC数据帧由一个起始位、一个头块、数据块1（操作码）和数据块2（操作数）组成。除了起始位之外的三个块由10位组成。

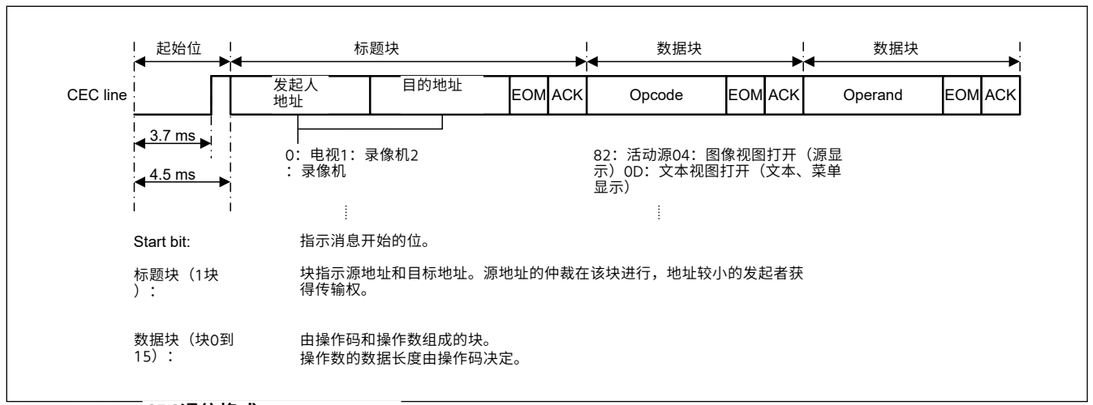


Figure 37.5 CEC通信格式

37.3.1.2 Communication Types

CEC transmission/reception takes place in the state of a direct address message or broadcast message. In a CEC communication, the transmitting side transmits a start bit and message (data) and the receiving side receives the message and returns a desired acknowledge signal to the transmitting side. CEC transmission/reception consist of a start bit and data and performs all transmissions/receptions of CEC.

37.3.1.3 Bit Timing

Figure 37.6 shows an example of the pulse format of a start bit. Whether the start bit is valid is determined at the low-level period (a) and bit period (b).

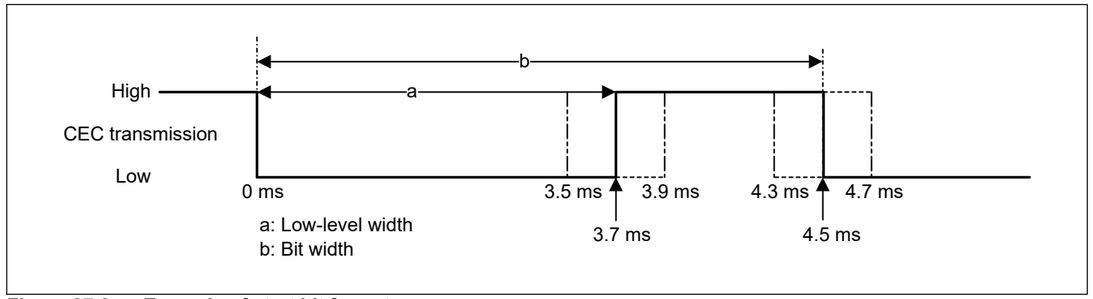


Figure 37.6 Example of start bit format

Figure 37.7 shows an example of the pulse format of a data bit timing. A data bit is sampled at a sampling timing set with the CEC reception data sampling time setting register (NOMT). If the result of sampling is low, the pulse format is logical 0. If the result of sampling is high, the pulse format is logical 1. The last change from high to low of a data bit is the start of the next data bit. Consequently, the last data bit remains high.

37.3.1.2 通讯类型

CEC发送接收在直接地址消息或广播消息的状态下进行。在CEC通信中，发送方发送起始位和消息（数据），接收方接收该消息并向发送方返回所需的确认信号。CEC发送接收由起始位和数据组成，执行CEC的所有发送接收。

37.3.1.3 位时序

图37.6显示了一个起始位的脉冲格式示例。在低电平周期（a）和位周期（b）确定起始位是否有效。

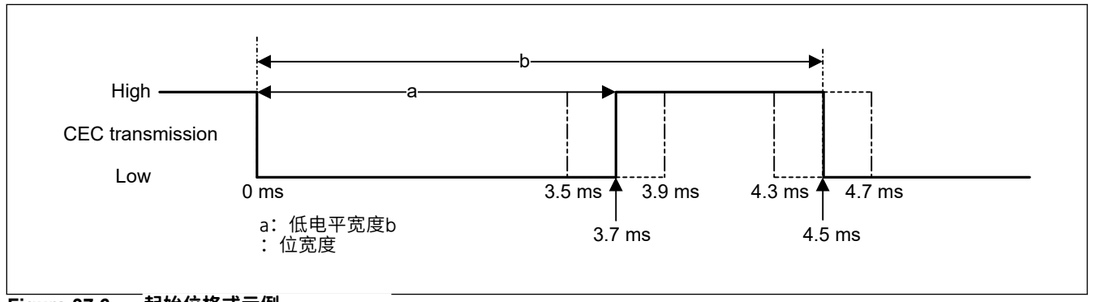
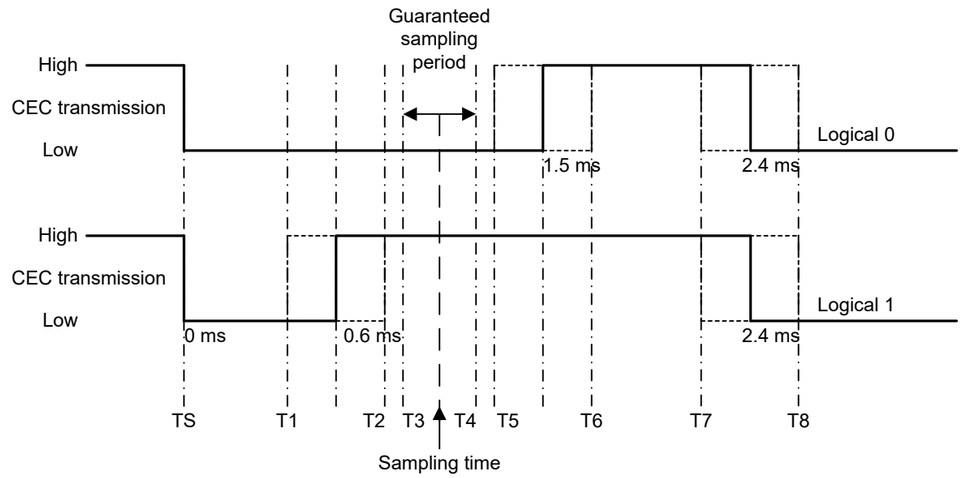


Figure 37.6 起始位格式示例

图37.7显示了数据位时序的脉冲格式示例。数据位以CEC接收数据采样时间设置寄存器(NOMT)设置的采样时间进行采样。如果采样结果为低电平，则脉冲格式为逻辑0。如果采样结果为高电平，则脉冲格式为逻辑1。最后一个数据位由高变低是下一个数据位的开始。因此，最后一个数据位保持高电平。



Ts	0 ms	The bit start event
T1	0.4 ms	The earliest time for a low/high transition when indicated by a logical 1
T2	0.8 ms	The latest time for a low/high transition when indicated by a logical 1
T3	0.85 ms	The earliest time for safely sampling the signal line to determine its state
T4	1.25 ms	The latest time for safely sampling the signal line to determine its state
T5	1.3 ms	The earliest time at which a device is permitted to return to a high impedance state (logical 0)
T6	1.7 ms	The latest time at which a device is permitted to return to a high impedance state (logical 0)
T7	2.05 ms	The earliest time for the start of a following bit
	2.4 ms	The nominal data bit period
T8	2.75 ms	The latest time for the start of a following bit

Figure 37.7 Example of data bit format

37.3.1.4 Header Block and Data Block

All data blocks consists of 10 bits and have the same structure. Figure 37.8 shows the format of header and data blocks. An information bit has different meaning for a header block and data block, and indicates the data, opcode, and address. EOM (End of Message) and ACK (Acknowledge) are control bits and have the same meanings for header block and data block.

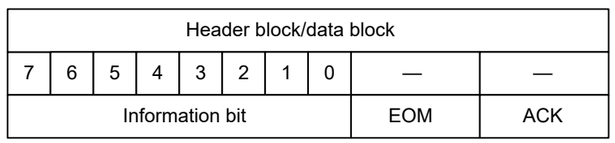
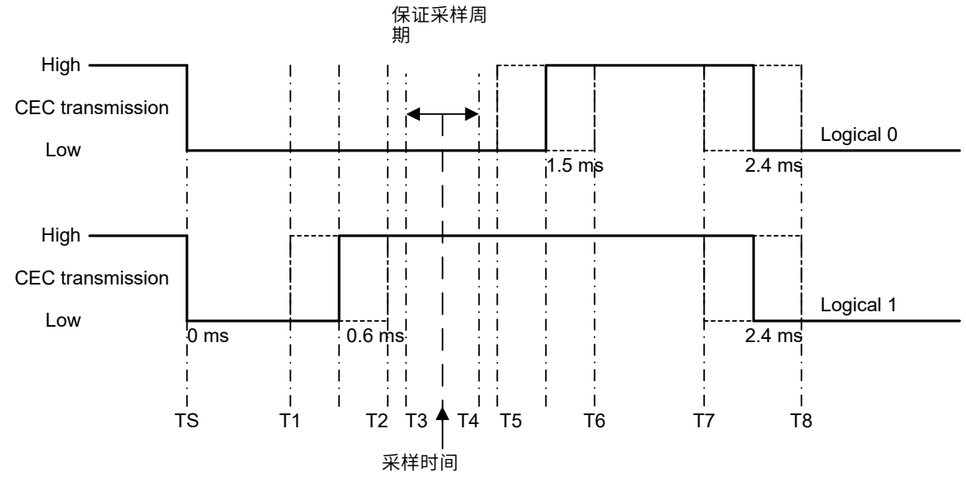


Figure 37.8 Format of header block and data block

A header block consists of an initiator logical address, destination logical address, EOM (End of Message), and ACK (Acknowledge). Information bits 7 to 4 indicate initiator logical addresses and bits 3 to 0 indicate destination logical addresses. The EOM of a header block is used for “ping” with another device (checking whether the power of another device is turned on). “ping” can be checked by setting EOM = 1 and transmitting only the header block (transmitting a



Ts	0 ms	位启动事件
T1	0.4 ms	由逻辑1指示的低高电平转换的最早时间
T2	0.8 ms	由逻辑1指示的低高转换的最晚时间
T3	0.85 ms	安全采样信号线以确定其状态的最早时间
T4	1.25 ms	安全采样信号线以确定其状态的最晚时间
T5	1.3 ms	允许设备返回高阻抗状态的最早时间（逻辑0）
T6	1.7 ms	允许设备返回高阻抗状态的最晚时间（逻辑0）
T7	2.05 ms	下一位开始的最早时间
	2.4 ms	标称数据位周期
T8	2.75 ms	下一位开始的最晚时间

Figure 37.7 数据位格式示例

37.3.1.4 头块和数据块

所有数据块均由10位组成并具有相同的结构。图37.8显示了标题和数据块的格式。信息位对于头块和数据块具有不同的含义，并指示数据、操作码和地址。EOM（EndofMessage）和ACK（Acknowledge）是控制位，对于头块和数据块具有相同的含义。

Figure 37.8 头块和数据块的格式

标头块由启动器逻辑地址、目标逻辑地址、EOM（消息结束）和ACK（确认）组成。信息位7到4表示启动器逻辑地址，位3到0表示目标逻辑地址。头块的EOM用于与另一个设备“ping”（检查另一个设备的电源是否打开）。“ping”可以通过设置EOM=1并仅传输头块（传输一个

message without data blocks). For direct address transmission, the power of the device to which the header block is transmitted is turned on if an ACK is returned.

37.3.1.5 EOM (End of Message)

An EOM indicates whether the transmitted block is the last block of a message. It is added to an information bit and output.

EOM bit = 0: When more blocks follow.

EOM bit = 1: When the transmitted block is the last block.

37.3.1.6 ACK (Acknowledge)

The meaning of an ACK depends on whether the receiving party of a transmission is a direct address message or broadcast message. The result of comparing the received data and CEC line data is transmitted to the transmitting side as an ACK or NACK.

The initiator outputs logical 1 at the ACK bit timing. Consequently, a follower determines the logic level of the ACK bit.

- An ACK (ACK = logical 0) is the normal value for a direct address message:
  1. If no error exists in the header block and the local address is used, the ACK bit is logical 0.
  2. If no error exists in the data blocks, the ACK bit is logical 0.
  3. If an error exists in the header block or another address is used, the ACK bit is logical 1.
  4. If an error exists in the data blocks, the ACK bit is logical 1.
- An NACK (ACK = logical 1) is the normal value for a broadcast message:
  1. If one or more followers have abandoned the message, the ACK bit is logical 0.
  2. If no followers have abandoned the message, the ACK bit is logical 1.

37.3.2 Operating Clocks

The CEC can use one of the following clocks as its operating clock: the divided clock of the peripheral module clock (PCLKB), or the directly clock of the CECCLK supplied from the main clock or sub clock oscillator. When using the CECCLOCK as the CEC operating clock, take note of the respective procedures for supplying these clocks. The following describes how to supply these clocks.

CEC clock can be selected from PCLKB/2^5, PCLKB/2^6, PCLKB/2^7, PCLKB/2^8, PCLKB/2^9, PCLKB/2^{10}, CECCLK (When using SOSC), and CECCLK/2^8 (When using MOSC).

37.3.3 CEC Communication Functions

37.3.3.1 Communication Bit Width Adjustment Function

This function can be used to set the low-level width and bit width of the start bit and data bit during a transmission. The values of some registers must be set according to the specified relationships. Set the following registers to ensure the relationships are kept:

- STATL < STATB
- LGC1L < LGC0L < DATB

The relationships between the various width setting registers (see section 37.2.9. STATL : CEC Transmission Start Bit Low Width Setting Register to section 37.2.13. DATB : CEC Transmission Data Bit Width Setting Register) and the bit timing are shown in (1) to (3).

(1) Start bit

The STATL register is used to set the low-level width and the STATB register is used to set the bit width of the start bit. Figure 37.9 shows the output waveform of the start bit.

没有数据块的消息）。对于直接地址传输，如果返回ACK，则打开头块被传输到的设备的电源。

37.3.1.5 EOM (End of Message)

EOM指示传输的块是否是消息的最后一个块。它被添加到信息位并输出。

EOM位=0：当后面有更多块时。

EOM位=1：当发送块是最后一个块时。

37.3.1.6 ACK (Acknowledge)

ACK的含义取决于传输的接收方是直接地址消息还是广播消息。接收数据和CEC线路数据的比较结果作为ACK或NACK被发送到发送方。

发起方在ACK位定时输出逻辑1。因此，跟随器确定ACK位的逻辑电平。

●ACK（ACK=逻辑0）是直接地址消息的正常值：

1.如果头块中没有错误并且使用本地地址，则ACK位为逻辑0。

2.如果数据块没有错误，则ACK位为逻辑0。

3.如果头块中存在错误或使用了其他地址，则ACK位为逻辑1。

4.如果数据块中存在错误，则ACK位为逻辑1。

●NACK（ACK=逻辑1）是广播消息的正常值：

1.如果有一个或多个追随者放弃了该消息，则ACK位为逻辑0。

2.如果没有跟随者放弃该消息，则ACK位为逻辑1。

37.3.2 工作时钟

CEC可以使用以下时钟之一作为其工作时钟：外围模块时钟(PCLKB)的分频时钟，或由主时钟或副时钟振荡器提供的CECCLK的直接时钟。当使用CECCLOCK作为CEC操作时钟时，请注意提供这些时钟的相应程序。下面介绍如何提供这些时钟。

CEC时钟可以从PCLKB25、PCLKB26、PCLKB27、PCLKB28、PCLKB29、PCLKB210、CECCLK（使用SOSC时）和CECCLK28（使用MOSC时）中选择。

37.3.3 CEC通讯功能

37.3.3.1 通讯位宽调整功能

该函数可用于设置传输过程中起始位和数据位的低电平宽度和位宽。有些寄存器的值必须按照指定的关系来设置。设置以下寄存器以确保保持关系：

- STATL < STATB
- LGC1L < LGC0L < DATB

各种宽度设置寄存器之间的关系（参见第37.2.9节。STATL：CEC传输起始位低宽度设置寄存器到第37.2.13节。DATB:CEC传输数据位宽设置寄存器)和位时序如(1)至(3)所示。

(1) 起始位

STATL寄存器用于设置低电平宽度，STATB寄存器用于设置起始位的位宽。
图37.9显示了起始位的输出波形。

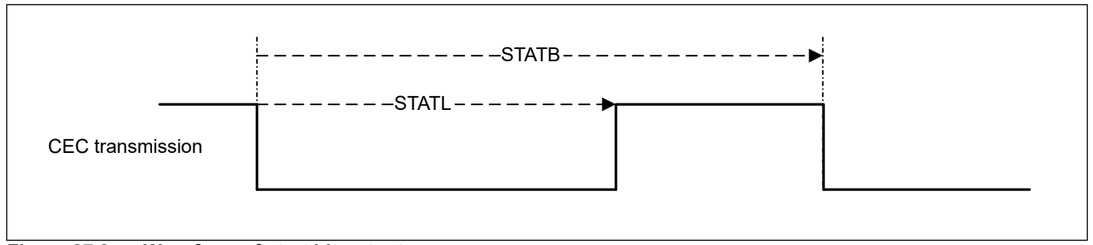


Figure 37.9 Waveform of start bit output

(2) Data bit (logical 0)

The LGC0L register is used to set the low-level width and the DATB register is used to set the bit width of the data bit of logical 0. Figure 37.10 shows the output waveform of the data bit (logical 0).

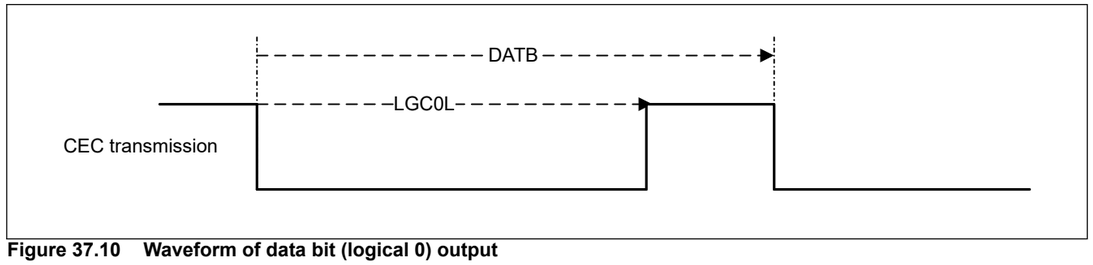


Figure 37.10 Waveform of data bit (logical 0) output

(3) Data bit (logical 1)

The LGC1L register is used to set the low-level width and the DATB register is used to set the bit width of the data bit of logical 1. Figure 37.11 shows the output waveform of the data bit (logical 1).

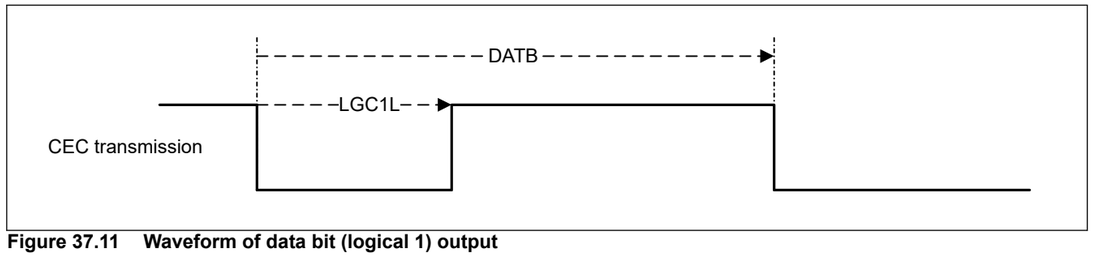


Figure 37.11 Waveform of data bit (logical 1) output

37.3.3.2 Receive Bit Timing Check Function

The CEC transmission/reception circuit has a timing check function that determines whether the low-level width and bit width of the start bit and data bit during reception are within the set range. The timing check period can be set using the various timing determination registers (see section 37.2.14. STATLL : CEC Reception Start Bit Minimum Low Width Setting Register to section section 37.2.23. DATBH : CEC Reception Data Bit Maximum Bit Width Setting Register).

The values of some registers must be set according to the specified relationships. Set the following registers to ensure the relationships are kept:

- STATLL < STATLH
- STATBL < STATBH
- LGC0LL < LGC0LH
- LGC1LL < LGC1LH
- DATBL < DATBH

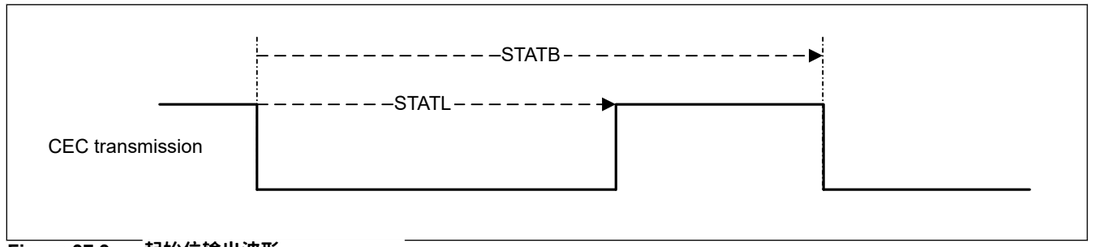


Figure 37.9 起始位输出波形

(2) 数据位（逻辑0）

LGC0L寄存器用于设置低电平宽度，DATB寄存器用于设置逻辑0的数据位的位宽。图37.10显示了数据位（逻辑0）的输出波形。

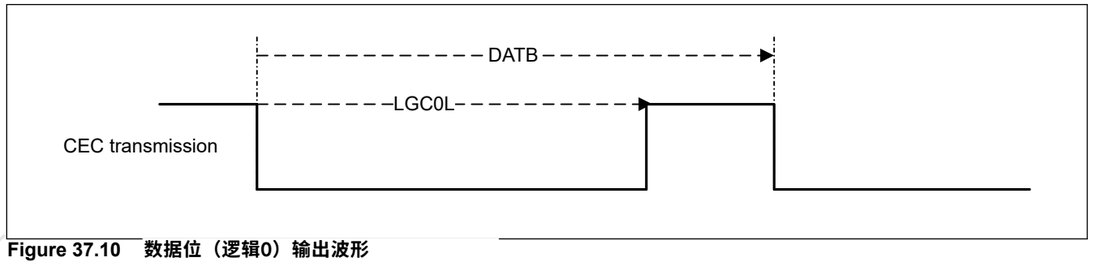


Figure 37.10 数据位（逻辑0）输出波形

(3) 数据位（逻辑1）

LGC1L寄存器用于设置低电平宽度，DATB寄存器用于设置逻辑1的数据位的位宽。图37.11显示了数据位（逻辑1）的输出波形。

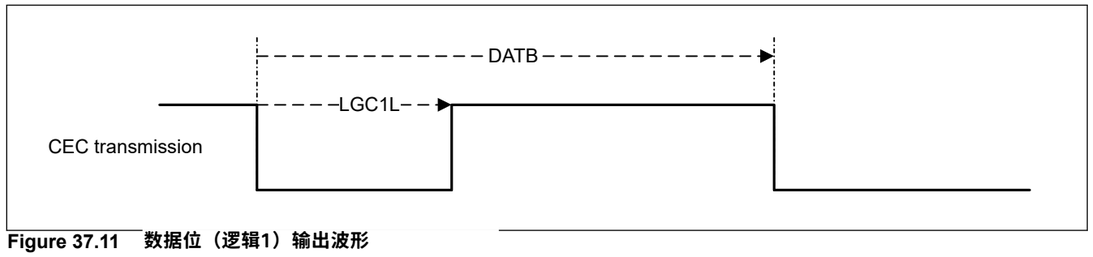


Figure 37.11 数据位（逻辑1）输出波形

37.3.3.2 接收位时序校验功能

CEC发送接收电路具有定时检查功能，判断接收时起始位和数据位的低电平宽度和位宽是否在设定范围内。可以使用各种时序确定寄存器设置时序检查周期（参见第37.2.14节。STATLL：CEC接收起始位最小低位宽度设置寄存器到第37.2.23节。DATBH：CEC接收数据位最大位宽度设置寄存器）.

有些寄存器的值必须按照指定的关系来设置。设置以下寄存器以确保保持关系：

- STATLL < STATLH
- STATBL < STATBH
- LGC0LL < LGC0LH
- LGC1LL < LGC1LH
- DATBL < DATBH

The relationships between the timing determination registers and bit timing are shown in (1) to (3).

(1) Start bit

The STATLL register is used to set the minimum low-level width and the STATLH register is used to set the maximum low-level width of the start bit. The STATBL register is used to set the minimum value of the start bit and the STATBH register is used to set the maximum value of the start bit width. Figure 37.12 shows the timing at which the start bit is received.

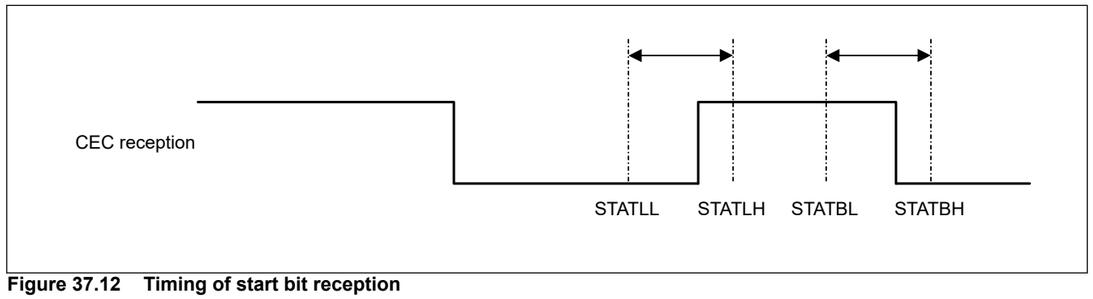


Figure 37.12 Timing of start bit reception

(2) Data bit (logical 0)

The LGC0LL register is used to set the minimum low-level width and the LGC0LH register is used to set the maximum low-level width of the data bit (logical 0). The DATBL register is used to set the minimum value the data bit and the DATBH register is used to set the maximum value of the data bit width. Figure 37.13 shows the timing at which the data bit (logical 0) is received.

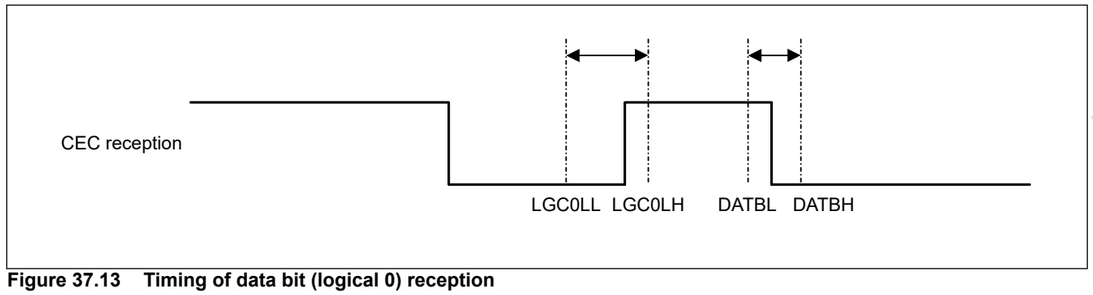


Figure 37.13 Timing of data bit (logical 0) reception

(3) Data bit (logical 1)

The LGC1LL register is used to set the minimum low-level width and the LGC1LH register is used to set the maximum low-level width of the data bit (logical 1). The DATBL register is used to set the minimum value data bit width and the DATBH register is used to set the maximum value of the data bit width. Figure 37.14 shows the timing at which the data bit (logical 1) is received.

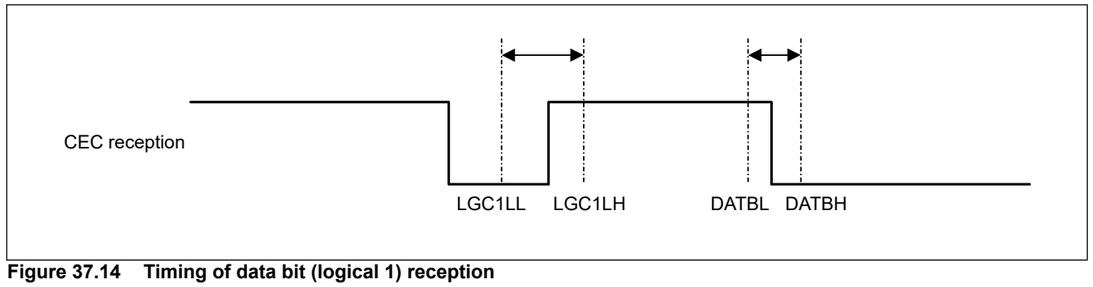


Figure 37.14 Timing of data bit (logical 1) reception

时序确定寄存器和位时序之间的关系如（1）至（3）所示。

(1) 起始位

STATLL寄存器用于设置最小低电平宽度，而STATLH寄存器用于设置起始位的最大低电平宽度。STATBL寄存器用于设置起始位的最小值，STATBH寄存器用于设置起始位宽度的最大值。图37.12显示了接收起始位的时序。

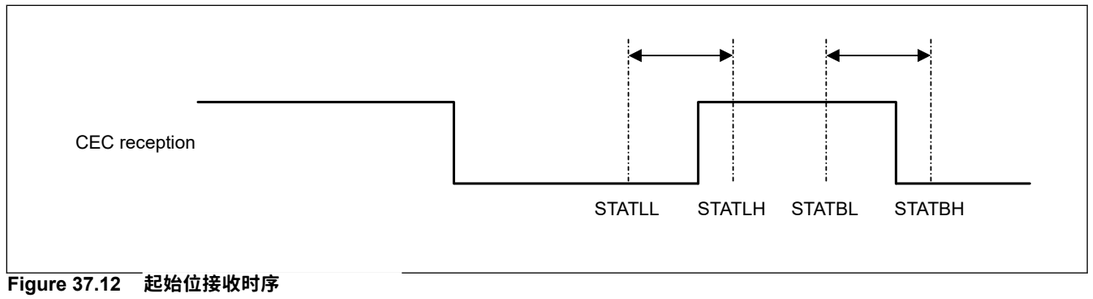


Figure 37.12 起始位接收时序

(2) 数据位（逻辑0）

LGC0LL寄存器用于设置最小低电平宽度，LGC0LH寄存器用于设置数据位（逻辑0）的最大低电平宽度。DATBL寄存器用于设置数据位的最小值，DATBH寄存器用于设置数据位宽的最大值。图37.13显示了接收数据位（逻辑0）的时序。

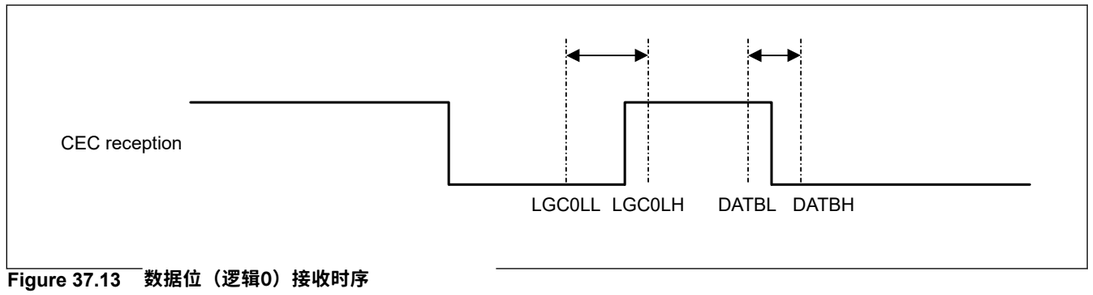


Figure 37.13 数据位（逻辑0）接收时序

(3) 数据位（逻辑1）

LGC1LL寄存器用于设置最小低电平宽度，而LGC1LH寄存器用于设置数据位（逻辑1）的最大低电平宽度。DATBL寄存器用于设置最小值数据位宽，DATBH寄存器用于设置数据位宽的最大值。图37.14显示了接收数据位（逻辑1）的时序。

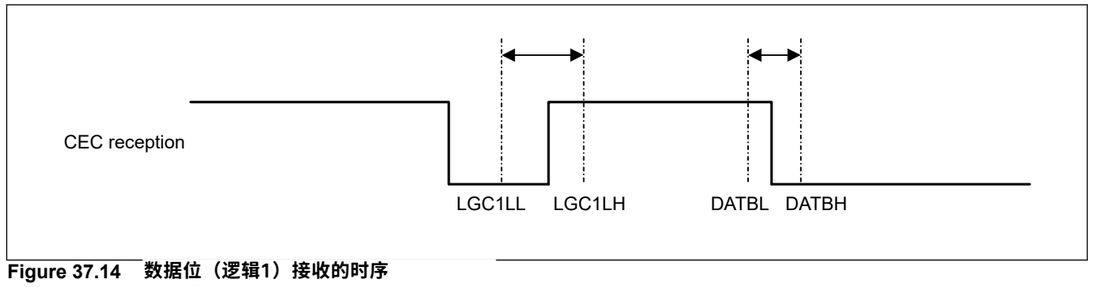


Figure 37.14 数据位（逻辑1）接收的时序

37.3.3.3 Initial CEC Communication Settings

The initial CEC communication setting flow is explained below. The logical address acquisition flow is executed by setting the various control registers and using direct address transmission after a reset. In a logical address acquisition transmission, EOM = 1 is set because the same address is set for the source and destination addresses and only the header block is transmitted. Additionally, to prevent a false address match from occurring before the local address is determined, CECRXEN = 0 must be set before the CADR register setting. Figure 37.15 shows the logical allocation timing diagram and Table 37.6 lists the operation procedure and an explanation of the operation.

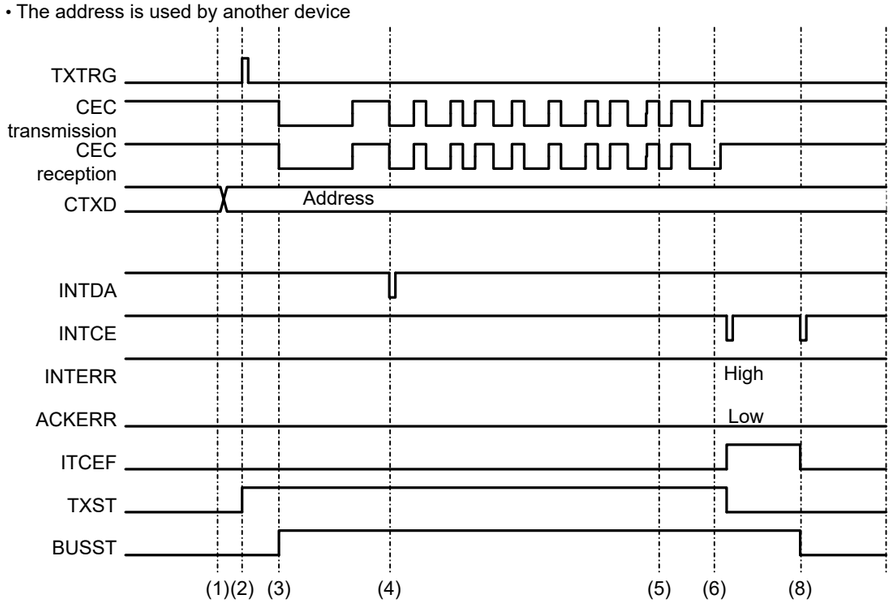
37.3.3.3 初始CEC通信设置

下面说明初始CEC通信设置流程。通过设置各种控制寄存器并在复位后使用直接地址传输来执行逻辑地址获取流程。在逻辑地址获取传输中，设置EOM=1，因为为源地址和目标地址设置了相同的地址，并且只传输了头块。此外，为防止在确定本地地址之前发生错误的地址匹配，必须在设置CADR寄存器之前设置CECRXEN=0。图37.15显示了逻辑分配时序图和

表37.6列出了操作过程和操作说明。

RA生态工作室

• The address is used by another device



• The address is not used by another device

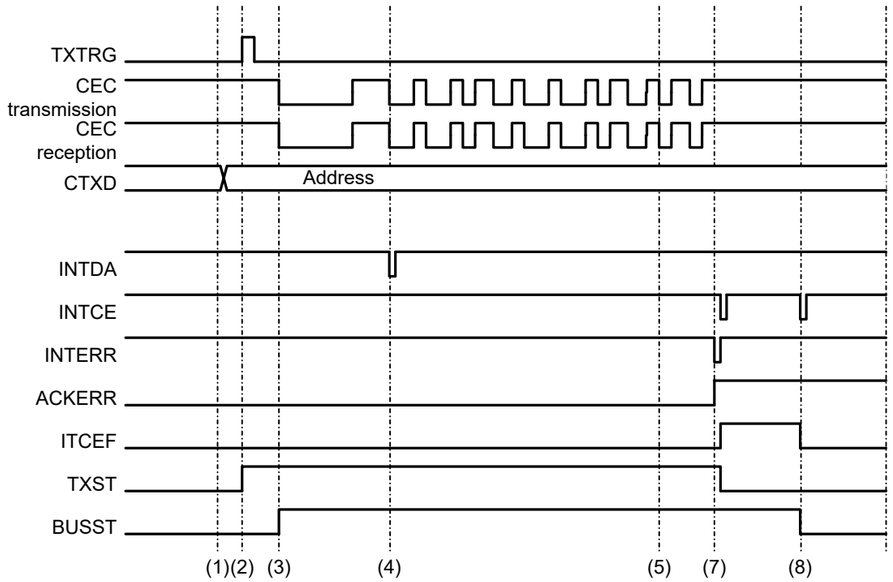
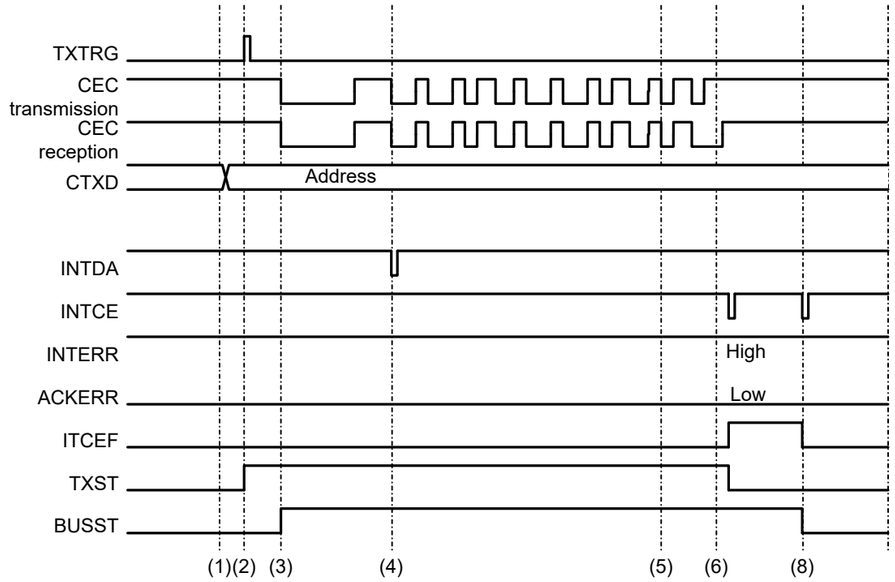


Figure 37.15 Logical allocation (CECCTL1.CESEL[1:0] = 00b)

•该地址被其他设备使用



•该地址未被其他设备使用

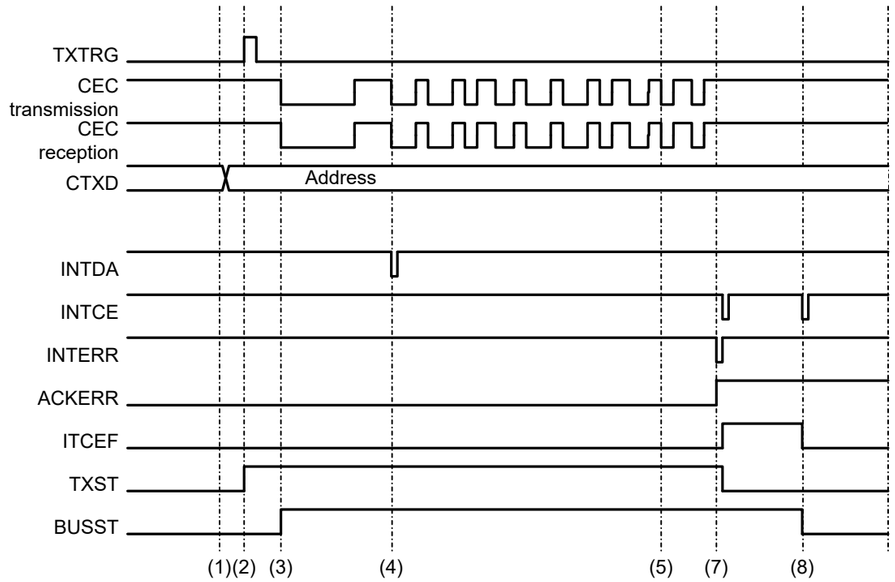


Figure 37.15 逻辑分配(CECCTL1.CESEL[1:0]=00b)

Table 37.6 Initial CEC communication setting procedure (1 of 2)

Stage	Step	Software manipulation	CEC state
Initial CEC setting	1	[IO initial setting] Select CECIO function for P206 or P706 Set to NMOS open drain output [CEC clock setting] Set the CCL[2:0] bits. [Reception rejection control setting] Set CECRXEN to 0. [Setting for reporting address mismatch] Set CINTMK. [Noise elimination selection] Set CDFC (Specify whether to use the noise filter). [Start bit low-level/bit width setting] Set the low/bit width to STATL/STATB. [Logical 0/1 low-level/bit width setting] Set the low/bit width to LGC0L/LGC1L/DATB. [Sampling time setting] Specify the time to sample the received data for NOMT. [Bit width setting] Specify the bit width for NOMP. [Register settings for timing check] Set the low-level width timing check period of the start bit to STATLL/STATLH. Set the bit width timing check period of the start bit to STATBL/STATBH. Set the low-level width timing check period of the data bit (logical 0) to LGC0LL/LGC0LH. Set the low-level width timing check period of the data bit (logical 1) to LGC1LL/LGC1LH. Set the bit width timing check period of the data bit to DATBL/DATBH. [Bus lock detection setting] Set up BLERRD (select whether to detect bus locking). [Start bit timing error detection setting] Set STERRD (select whether to detect timing errors of the start bit). [Communication complete interrupt setting] Set the CESEL[1:0]. [Signal-free time setting] Set the SFT[1:0] bits (set the signal-free time detection time). [CEC clock supply] Set CECE to 1.	The CEC clock is stopped.
	2	—	The CEC clock is supplied. Transmission can be performed. The signal-free time is started. BUSST becomes 1. BUSST becomes 0 and the communication standby state is entered after counting up to the set values of the SFT[1:0] bits.

Table 37.6 初始CEC通信设置程序(1of2)

Stage	Step	软件操作	CEC state
初始CEC设置	1	[IO初始设置]选择P206或P706的CECIO功能 设置为NMOS开漏输出[CEC时钟设置] 设置CCL[2:0]位。[接收拒绝控制设置]将CECRXEN设置为0。[用于报告地址不匹配的设置]设置CINTMK。【降噪选择】 设置CDFC（指定是否使用噪声过滤器）。【起始位低位位宽设置】 将低位宽度设置为STATLSTATB。【逻辑01低电平位宽设置】 将低位宽度设置为LGC0LLGC1LDATB。[采样时间设置] 指定对NOMT接收数据进行采样的时间。[位宽设置] 指定NOMP的位宽。[用于定时检查的注册设置] 设置起始位的低电平宽度时序检查周期为停止停止。设置起始位的位宽时序检查周期为 STATBL/STATBH. 将数据位（逻辑0）的低电平宽度时序检查周期设置为LGC0LLLGC0LH。将数据位（逻辑1）的低电平宽度时序检查周期设置为LGC1LLLGC1LH。设置数据位的位宽时序检查周期为 DATBLDATBH。[总线锁定检测设置] 设置BLERRD（选择是否检测总线锁定）。[起始位时序错误检测设置] 设置STERRD（选择是否检测起始位的时序错误）。[通信完成中断设置]设置CESEL[1:0]。[无信号时间设置] 设置SFT[1:0]位（设置无信号时间检测时间）。[CEC时钟供应]将CECE设置为1。	CEC时钟停止。
	2	—	提供CEC时钟。 可以进行传输。无信号时间开始。BUSST变为1。BUSST变为0，并在计数到SFT[1:0]位的设置值后进入通信待机状态。

Table 37.6 Initial CEC communication setting procedure (2 of 2)

Stage	Step	Software manipulation	CEC state
Logical address allocation	3	[EOM setting] Set EOM to 1. [Transmit data setting] (1) Set the transmit data (logical address) to CTXD. [Bus-free state check] Check that BUSST is 0. [Starting transmit operation] (2) Set TXTRG to 1.	—
	4	—	Transmission is started. The start bit is output (3).
	5	—	The values set in the CTXD register are sequentially output at the same time as INTDA is output when the header block output is started (4).
	6	Do not write the next data, because only the header block is transmitted.	—
	7	—	1 is output from the EOM bit (5).
	8	[Local address setting]	The ACK bit is received.
	8-1	ACK: Change the transmitted address and then retransmit the address, because it is used by another station.	When logical 0 is received, INTERR is not output and the ACKERR flag is not set (6).
	8-2	NACK: Use the transmitted address as the local address, because the transmitted address is not used by another station (CADR setting).	When logical 1 is received, INTERR is output and the ACKERR flag is set (7).
	9	—	INTCE is output according to the CESEL[1:0] and SFT[1:0] bit settings (8).
Reception rejection	10	[Reception rejection control setting] Set CECRXEN to 1.	—
	11	—	The communication standby state is entered.

37.3.3.4 CEC Transmission

A CEC transmission performs a receive operation even during transmission and performs an arbitration check, a data check, and a timing check.

The value of the reception buffer register (CRXD) during a transmit operation, however, is not guaranteed.

A new start bit detected during transmission (the time from when a start bit is detected until the EOM of the last frame is received) is ignored and detected as a timing error. Communication is not restarted. Figure 37.16 shows the basic timing of transmission, and Table 37.7 shows the procedure for manipulating CEC transmission.

Table 37.6 初始CEC通信设置过程(2of2)

Stage	Step	软件操作	CEC state
逻辑地址分配	3	[EOM setting] 将EOM设置为1。[传输数据设置](1) 将发送数据（逻辑地址）设置为CTXD。[公共汽车状态检查] 检查BUSST是否为0。[开始发送操作](2)将TXTRG设置为1。	—
	4	—	传输开始。起始位是输出(3)。
	5	—	CTXD寄存器中设置的值在开始头块输出时在输出INTDA的同时顺序输出(4)。
	6	不要写下一个数据，因为只传输头块。	—
	7	—	EOM位(5)输出1。
	8	[Local address setting]	接收到ACK位。
	8-1	ACK：改变发送地址，然后重新发送地址，因为它被另一个站使用。	当接收到逻辑0时，不输出INTERR并且不设置ACKERR标志(6)。
	8-2	NACK：使用传输的地址作为本地地址，因为传送的地址没有被其他站使用（CADR设置）。	当接收到逻辑1时，输出INTERR并设置ACKERR标志(7)。
	9	—	INTCE是根据输出CESEL[1:0]和SFT[1:0]位设置(8)。
接收拒绝	10	[接收拒绝控制设置]将CECRXEN设置为1。	—
	11	—	进入通信待机状态。

37.3.3.4 CEC Transmission

CEC传输即使在传输期间也执行接收操作并执行仲裁检查、数据检查和定时检查。

但是，不能保证发送操作期间的接收缓冲寄存器(CRXD)的值。

在传输过程中检测到的新起始位（从检测到起始位到接收到最后一帧的EOM的时间）将被忽略并检测为定时错误。通信未重新启动。图37.16显示了传输的基本时序，表37.7显示了操纵CEC传输的过程。

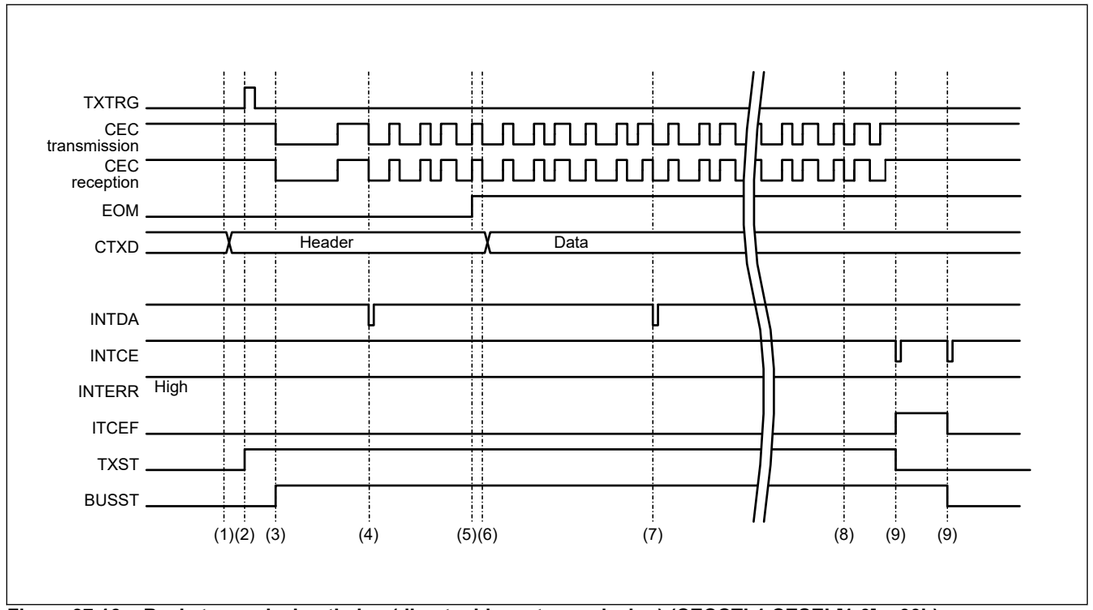


Figure 37.16 Basic transmission timing (direct address transmission) (CECCTL1.CESEL[1:0] = 00b)

(1) CEC transmission manipulation procedure

Table 37.7 CEC transmission manipulation procedure

Stage	Step	Software manipulation	CEC state
Initial CEC setting	1	See Table 37.6.	—
CEC transmit operation	2	[Signal-free time setting] Set the SFT[1:0] bits. (set the signal-free time detection time.) [EOM setting] (1) Set EOM (EOM = 0). [Transmit data setting] (1) Set the transmit data to CTXD. [Bus-free state check] Check that BUSST is 0. [Starting transmit operation] (2) Set TXTRG to 1.	—
	3	—	Transmission is started. The start bit is output (3).
	4	—	The values set in the CTXD register are sequentially output at the same time as INTDA is output when the header block output is started (4).
	5	[EOM setting] (5) Set the EOM of the next frame (EOM = 1) before the next frame starts (7). [Transmit data setting] (6) Set the transmit data to CTXD.	—
	6	—	Outputting the data of the second frame is started (7). 1 is output at the EOM bit position because the last frame is reached (8). INTCE is output according to the CESEL[1:0] and SFT[1:0] bit settings (9). The communication standby state is entered.

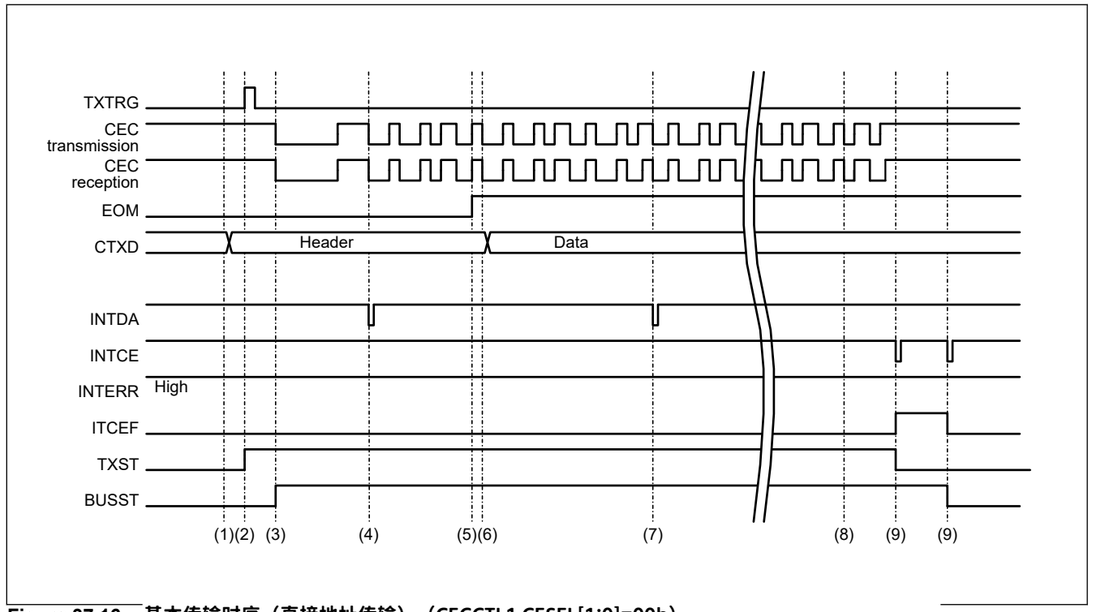


Figure 37.16 基本传输时序（直接地址传输）（CECCTL1.CESEL[1:0]=00b）

(1) CEC传输操作程序

Table 37.7 CEC传输操作程序

Stage	Step	软件操作	CEC state
初始CEC设置	1	见表37.6。	—
CEC发送操作	2	[无信号时间设置]设置SFT[1:0]位。（设置无信号时间检测时间。）[EOM设置](1) 设置EOM(EOM=0)。[传输数据设置](1) 将发送数据设置为CTXD。[公共汽车状态检查] 检查BUSST是否为0。[开始发送操作](2)将TXTRG设置为1。	—
	3	—	传输开始。起始位是输出(3)。
	4	—	CTXD寄存器中设置的值在开始头块输出时在输出INTDA的同时顺序输出(4)。
	5	[EOM setting] (5) 在下一帧开始之前设置下一帧的EOM(EOM=1)(7)。[发送数据设置](6) 将发送数据设置为CTXD。	—
	6	—	开始输出第二帧的数据(7)。因为到达最后一帧，所以在EOM位位置输出1(8)。INTCE是根据输出 CESEL[1:0]和SFT[1:0]位设置(9)。 进入通信待机状态。

(2) Broadcast transmission

When 0xF is set to the destination address of the header block transmit data (CTXD), the CEC recognizes the current transmission as a broadcast transmission and operates. Normally, the communication is determined as a successful operation when logical 0 is received at the ACK bit timing. However, in broadcast communication, the communication is a successful operation when logical 1 is received at the ACK bit timing.

The CEC determines whether the communication is a direct communication or broadcast communication by looking at the transmit data of the header block, and automatically determines whether the reception of logical 0 or logical 1 has been successfully performed.

(3) CEC transmission interrupt

The CEC has three interrupt functions, namely a data interrupt (INTDA), a communication complete interrupt (INTCE), and an error interrupt (INTERR). Figure 37.17 shows the timing for generating interrupts during transmission.

A data interrupt (INTDA) occurs at the start of each block.

A communication complete interrupt (INTCE) can be generated if ACK reception for a data block for which EOM is set to 1 ends, if the signal-free time specified using the CECCTL1.SFT[1:0] bits elapses, or if both conditions occur, depending on the settings of the CECCTL1.CESEL[1:0] bits.

An error interrupt (INTERR) is generated if any of the following errors is detected during any period of communication:

- Timing
- ACK
- Underrun
- Transmission.

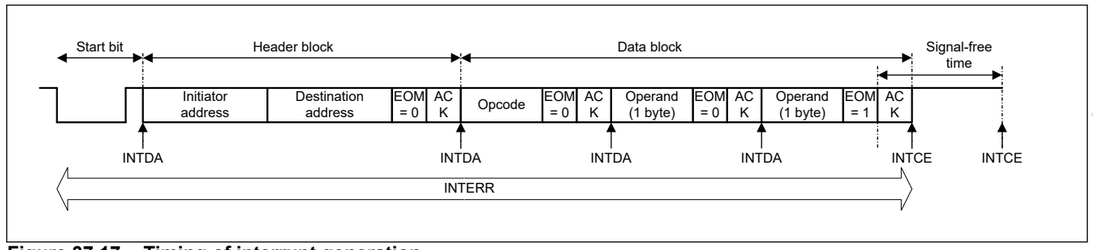


Figure 37.17 Timing of interrupt generation

If the falling edge of the CEC line is detected when receiving the ACK bit by setting EOM to 1 (before receiving the ACK bit ends), an irregular operation is performed as shown in Table 37.8 according to that timing.

Table 37.8 Operation if falling edge of CEC line is detected before receiving ACK bit ends

CEC line falling timing	CECCTL1.CESEL[1:0] bit setting	INTCE generation	Handling of ACK bit	Operation after CEC line falls
After the minimum data bit value (DATBL ≤ counter)	CESEL[1:0] = 00b or CESEL[1:0] = 01b	INTCE is generated once when the CEC line falls	Handling the ACK bit is enabled because it has the correct width. (ACK or NACK is correctly determined.)	The start of the next communication is recognized and then determines whether to receive the start bit starts.
	CESEL[1:0] = 10b	INTCE is not generated		
Before the minimum data bit value (counter < DATBL)	CESEL[1:0] = 00b or CESEL[1:0] = 01b	INTCE is generated once when the CEC line falls	ACK cannot be correctly determined because it has the incorrect width. (if ACKTEN is set to 1, a timing error occurs.)	
	CESEL[1:0] = 10b	INTCE is not generated		

(4) Receiving error handling pulse

During initiator operation, if the received data is at low level when the maximum low-level width of logical 0 is reached, an error handling pulse is received, a timing error occurs, transmission stops, and communication standby state is entered as shown in Figure 37.18.

(2) 广播传输

当0xF设置为标头块传输数据(CTXD)的目标地址时，CEC将当前传输识别为广播传输并进行操作。通常，当在ACK位定时接收到逻辑0时，通信被确定为成功操作。然而，在广播通信中，当在ACK位定时接收到逻辑1时，通信是成功的操作。

CEC通过查看头块的发送数据来判断通信是直接通信还是广播通信，并自动判断逻辑0或逻辑1的接收是否成功。

(3) CEC传输中断

CEC具有三个中断功能，即数据中断（INTDA）、通信完成中断（INTCE）和错误中断（INTERR）。图37.17显示了在传输过程中产生中断的时序。

数据中断（INTDA）发生在每个块的开始。

如果EOM设置为1的数据块的ACK接收结束，如果使用CECCTL1.SFT[1:0]位指定的无信号时间过去，或者如果这两种情况都可以生成通信完成中断(INTCE)发生，具体取决于CECCTL1.CESEL[1:0]位的设置。

如果在任何通信期间检测到以下任何错误，则会生成错误中断(INTERR)：

- Timing
- ACK
- Underrun
- Transmission.

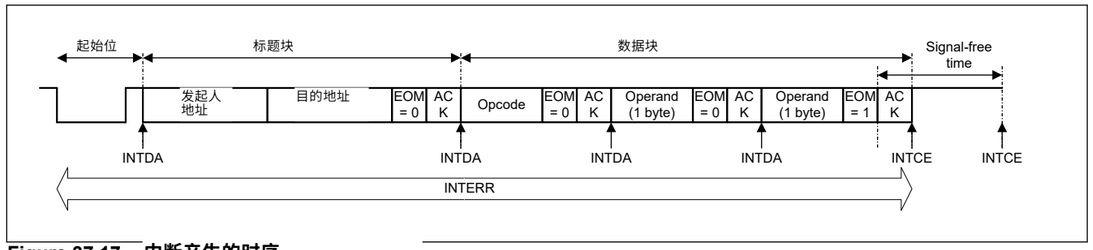


Figure 37.17 中断产生的时序

如果通过将EOM设置为1接收ACK位时（在接收ACK位结束之前）检测到CEC线的下降沿，则根据该时序执行如表37.8所示的不规则操作。

Table 37.8 在接收ACK位结束之前检测到CEC线的下降沿时的操作

CEC线下降时序	CECCTL1.CESEL[1:0]位设置	INTCE generation	ACK位的处理	CEC线下降后的操作
最小数据位值后（DATBL≤计数器）	CESEL[1:0] = 00b or CESEL[1:0] = 01b	CEC线下降时产生一次INTCE	启用处理ACK位，因为它具有正确的宽度。（ACK或NACK已正确确定。）	识别下一次通信的开始，然后确定是否开始接收开始位。
	CESEL[1:0] = 10b	未生成INTCE		
最小数据位值之前（计数器<DATBL）	CESEL[1:0] = 00b or CESEL[1:0] = 01b	CEC线下降时产生一次INTCE	ACK无法正确确定，因为它的宽度不正确。（如果ACKTEN设置为1，则会发生时序错误。）	
	CESEL[1:0] = 10b	未生成INTCE		

(4) 接收错误处理脉冲

在启动器操作过程中，如果在达到逻辑0的最大低电平宽度时接收到的数据为低电平，则接收到错误处理脉冲，发生时序错误，停止传输，进入通信待机状态，如图37.18.

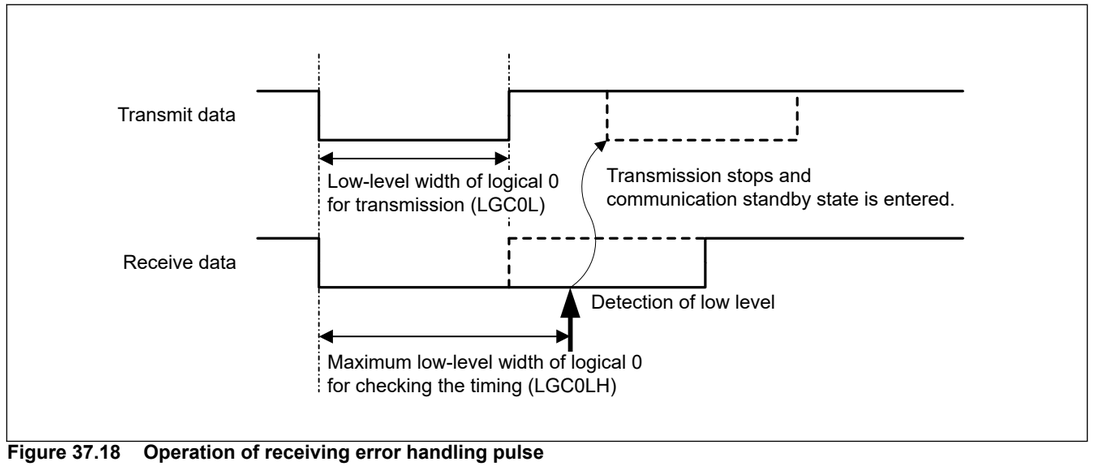


Figure 37.18 Operation of receiving error handling pulse

37.3.3.5 CEC Reception

During reception, the data is received at the sampling timing set by the CEC reception data sampling time setting register (NOMT) and stored in the reception buffer register (CRXD).

The receive operation differs depending on the CECCTL0.CECRXEN bit setting value, CECCTL1.CINTMK bit setting value, communication type (direct address communication or broadcast communication), and whether the reception address and local address match.

The correspondences between various conditions and the operations are shown in Table 37.9.

A new start bit detected during transmission (the time from when a start bit is detected until the EOM of the last frame is received) is ignored and detected as a timing error. However, when the restart reception function is used (CECEXMOD.RERCVEN = 1), a timing error is detected and determined as the start of new reception, so reception operation is performed again.

Table 37.9 Operation during CEC reception (1 of 2)

CEC RXEN	0	1							
Communication type	—	Start bit	Header			Direct data			Broadcast data
Address match/ mismatch	—	—	Mismatch		Match	Mismatch		Match	—
CINTMK bit	—	—	0	1	—	0	1	—	—
BUSST operation	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
INTDA output	Not supported	Not supported	Not supported	Supported	Supported	Not supported	Supported	Supported	Supported
INTCE output	Not supported	Supported*3	Supported*3	Supported	Supported	Not supported	Supported	Supported	Supported
INTERR output	Not supported	Not supported	Supported	Supported	Supported	Not supported	Supported	Supported	Supported
Error flag operation	Not supported	Not supported	Supported	Supported	Supported	Not supported	Supported	Supported	Supported
Error detection (other than short bit width detection)	Not supported	Supported*4	Supported	Supported	Supported	Not supported	Supported	Supported	Supported

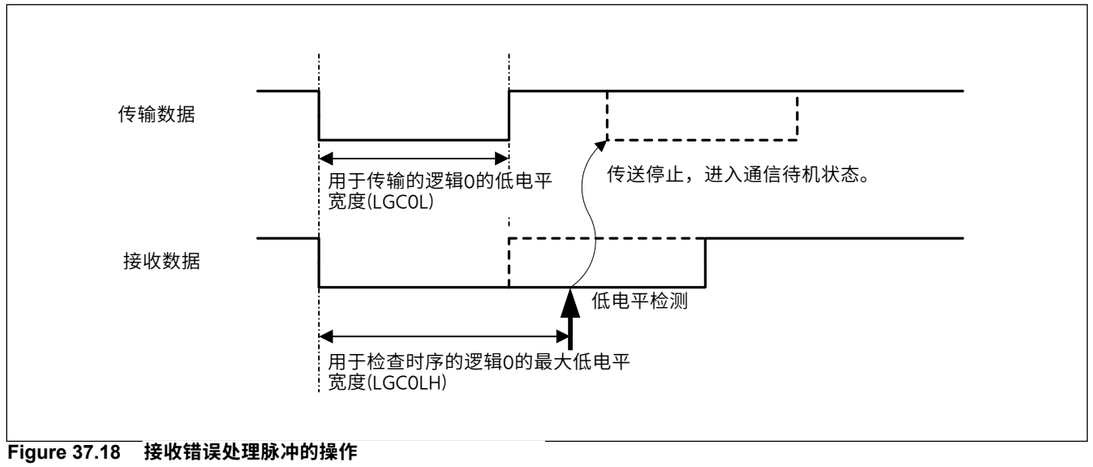


Figure 37.18 接收错误处理脉冲的操作

37.3.3.5 CEC Reception

在接收过程中，按照CEC接收数据采样时间设置寄存器(NOMT)设置的采样时间接收数据，并存储在接收缓冲寄存器(CRXD)中。

接收操作因CECCTL0.CECRXEN位设置值、CECCTL1.CINTMK位设置值、通信类型（直接地址通信或广播通信）以及接收地址和本地地址是否匹配而异。

各种条件与操作的对应关系如表37.9所示。

在传输过程中检测到的新起始位（从检测到起始位到接收到最后一帧的EOM的时间）将被忽略并检测为定时错误。但是，当使用重启接收功能时（CECEXMOD.RERCVEN=1），检测到定时错误并确定为新接收的开始，因此再次执行接收操作。

Table 37.9 CEC接收期间的操作(1of2)

CEC RXEN	0	1							
通讯类型	—	起始位	Header			直接数据			广播数据
地址匹配不匹配	—	—	Mismatch		Match	Mismatch		Match	—
CINTMK bit	—	—	0	1	—	0	1	—	—
BUSST operation	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
INTDA output	不支持	不支持	不支持	Supported	Supported	不支持	Supported	Supported	Supported
INTCE output	不支持	Supported*3	Supported*3	Supported	Supported	不支持	Supported	Supported	Supported
INTERR output	不支持	不支持	Supported	Supported	Supported	不支持	Supported	Supported	Supported
错误标志操作	不支持	不支持	Supported	Supported	Supported	不支持	Supported	Supported	Supported
错误检测（短位宽检测除外）	不支持	Supported*4	Supported	Supported	Supported	不支持	Supported	Supported	Supported

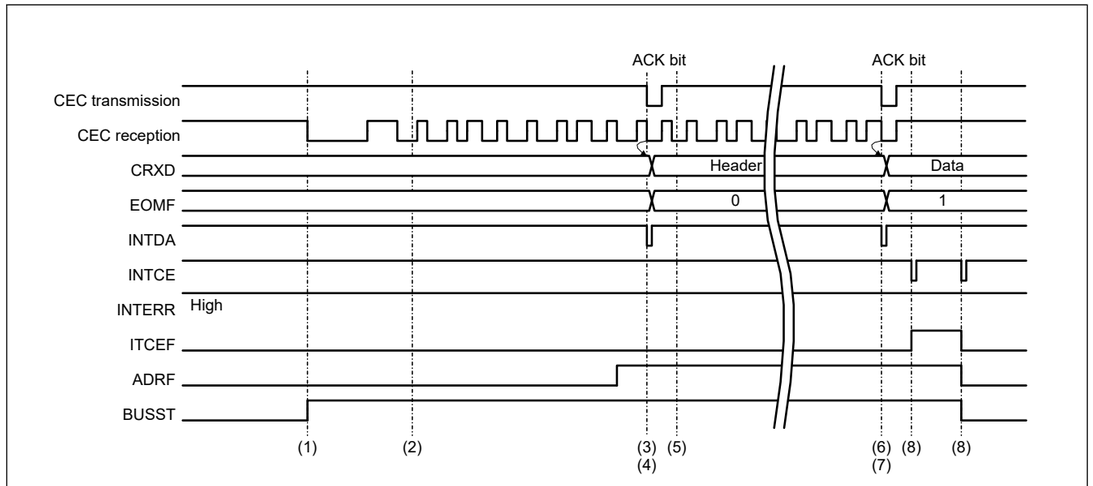
Table 37.9 Operation during CEC reception (2 of 2)

CEC RXEN	0	1							
Communication type	—	Start bit	Header			Direct data			Broadcast data
Address match/ mismatch	—	—	Mismatch		Match	Mismatch		Match	—
CINTMK bit	—	—	0	1	—	0	1	—	—
Error detection (short bit width detection)	Not supported	Supported*4	Supported	Supported	Supported	Supported	Supported	Supported	Supported
Error handling output	Not supported	Not supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
Bus lock detection*1	Supported*2	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
ACK/NACK output	Not supported	Not supported	Supported	Supported	Supported	Not supported	Not supported	Supported	Supported
Signal-free time count	Not supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported

Note 1. Bus lock errors are detected by setting CECCTL1.BLERRD.
Note 2. A bus lock error is detected but a flag is not set.
Note 3. Only if an error is detected.
Note 4. This is supported only if detecting timing errors for the start bit (CECCTL1.STERRD = 1). An error is detected but a flag is not set.

(1) CEC reception manipulation procedure

For the receiving operation of a direct address message, Figure 37.19 and Table 37.10 show operation when the addresses match, and Figure 37.20 and Table 37.11 show operation when the addresses do not match.



Note: (1) to (8) in Figure 37.19 correspond to (1) to (8) in Table 37.10.

Figure 37.19 Basic reception timing (1) (direct address reception, CECCTL1.CESEL[1:0] = 00b)

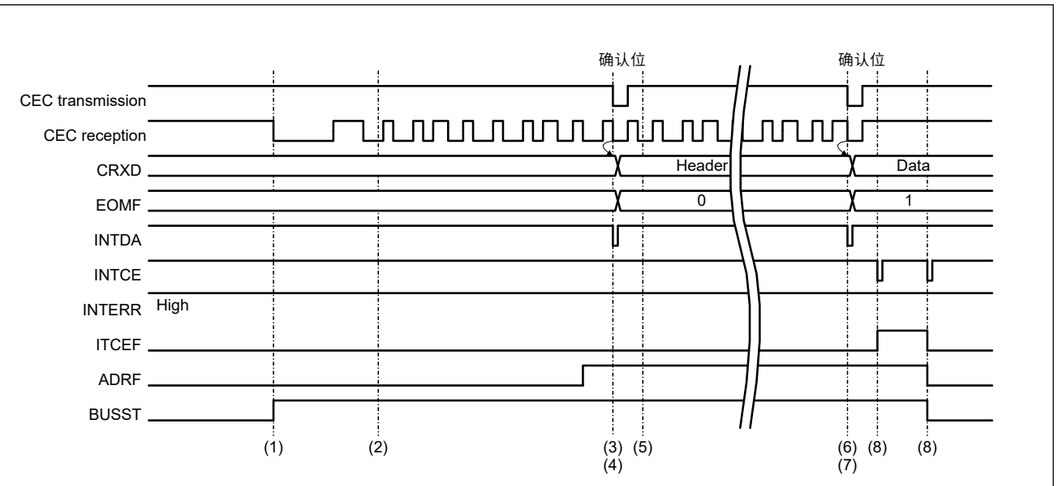
Table 37.9 CEC接收期间的操作(2of2)

CEC RXEN	0	1							
通讯类型	—	起始位	Header			直接数据			广播数据
地址匹配不匹配	—	—	Mismatch		Match	Mismatch		Match	—
CINTMK bit	—	—	0	1	—	0	1	—	—
错误检测（短位宽检测）	不支持	Supported*4	Supported	Supported	Supported	Supported	Supported	Supported	Supported
错误处理输出	不支持	不支持	Supported	Supported	Supported	Supported	Supported	Supported	Supported
总线锁定检测*1	Supported*2	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported
ACK/NACK output	不支持	不支持	Supported	Supported	Supported	不支持	不支持	Supported	Supported
无信号时间计数	不支持	Supported	Supported	Supported	Supported	Supported	Supported	Supported	Supported

注1.通过设置CECCTL1.BLERRD检测总线锁定错误。
注2.检测到总线锁定错误但未设置标志。
注3.仅当检测到错误时。
注4.仅当检测到起始位的时序错误(CECCTL1.STERRD=1)时才支持此功能。检测到错误但未设置标志。

(1) CEC接收操作程序

对于直接地址报文的接收操作，地址匹配时的操作如图37.19和表37.10所示，地址不匹配时的操作如图37.20和表37.11所示。



Note: 图37.19中的(1)至(8)对应于表37.10中的(1)至(8)。

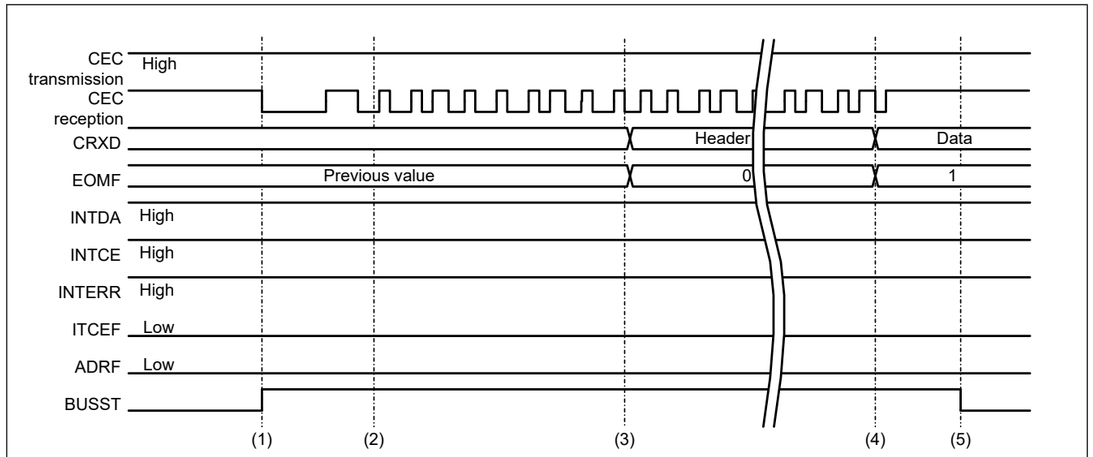
Figure 37.19 基本接收时序（1）（直接地址接收，CECCTL1.CESEL[1:0]=00b）

Table 37.10 CEC reception manipulation procedure (1)

Stage	Step	Software manipulation	CEC state
Initial CEC setting	1	See Table 37.6.	—
CEC receive operation	2	—	[Start bit detection] The falling edge of the CEC reception signal is detected and a receive operation is started (1). [Sampling] The data is sampled at the NOMT setting time and sequentially stored in the shift register (2). [Address match interrupt] INTDA is generated because the address received at the header block matched with the local address (3).
	3	Prepare for receiving data by returning from low power consumption mode or the like in response to INTDA generation. Use EOMF to check whether to continue transmission or whether it is the last frame.	—
	4	—	[ACK bit transmission] Logical 0 is transmitted at the ACK bit timing because the reception was successful (4).
	5	—	[Continuing reception] The data of the second frame is continuously received (5). [Receive data interrupt] When receiving 8-bit data is complete, the data is transferred to CRXD and INTDA is generated (6).
	6	Read the receive data from CRXD in response to INTDA generation. Use EOMF to check whether to continue transmission or whether it is the last frame.	
	7	—	[ACK bit transmission] Logical 0 is transmitted at the ACK bit timing because the reception was successful (7). [Reception completion] The reception is judged to be completed because EOM = 1 is received and INTCE is output according to the CECCTL1.CESEL[1:0] and CECCTL1.SFT[1:0] bit settings (8).

Table 37.10 CEC接收操作流程（一）

Stage	Step	软件操作	CEC state
初始CEC设置	1	见表37.6。	—
CEC接收操作	2	—	[Start bit detection] 检测到CEC接收信号的下降沿并开始接收操作(1)。[采样] 数据在NOMT设置时间被采样并顺序存储在移位寄存器(2)中。[地址匹配中断] INTDA的生成是因为在头块中接收到的地址与本地地址(3)匹配。
	3	响应INTDA生成，通过从低功耗模式等返回来准备接收数据。使用EOMF检查是否继续传输或是否是最后一帧。	—
	4	—	[ACK bit transmission] 因为接收成功(4)，所以在ACK位定时发送逻辑0。
	5	—	[Continuing reception] 连续接收第二帧的数据（5）。【接收数据中断】 接收完8位数据后，将数据传送到CRXD并生成INTDA(6)。
	6	从CRXD读取接收数据以响应INTDA一代。使用EOMF检查是否继续传输或是否是最后一帧。	
	7	—	[ACK bit transmission] 因为接收成功(7)，所以在ACK位定时发送逻辑0。[接收完成] 由于接收到EOM=1并根据CECCTL1.CESEL[1:0]和INTCE输出，因此判断接收完成 CECCTL1.SFT[1:0]位设置(8)。



Note: (1) to (5) in Figure 37.20 correspond to (1) to (5) in Table 37.11.

Figure 37.20 Basic reception timing (2) (CECCTL0.CECRXEN = 1, direct address, address mismatch, CECCTL1.CINTMK = 0)

Table 37.11 CEC reception manipulation procedure (2)

Stage	Step	Software manipulation	CEC state
CEC receive operation	1	—	[Start bit detection] The falling edge of the CEC reception signal is detected and a receive operation is started. Set BUSST flag (1). [Sampling] The data is sampled at the NOMT setting time and sequentially stored in the shift register (2). [Address match interrupt] INTDA is not generated and neither ACK nor NACK is returned because the address received at the header block does not match the local address and CINTMK is 0 (3). However, monitoring of the CEC line continues in order to check the bit length and detect completion of communication. [ACK bit transmission] Neither ACK nor NACK is returned because communication is performed between other stations (4). [Reception completion] Communication between other stations is complete because EOM = 1 is received, the signal-free time is counted according to the SFT[1:0] bit settings, and BUSST is cleared to 0 (5).

(2) Broadcast reception

The reception flow and timing check period are the same as those of direct address reception. If the destination address transmitted by the initiator is 0xF, the communication operates as a broadcast reception.

The differences from direct address reception are as follows:

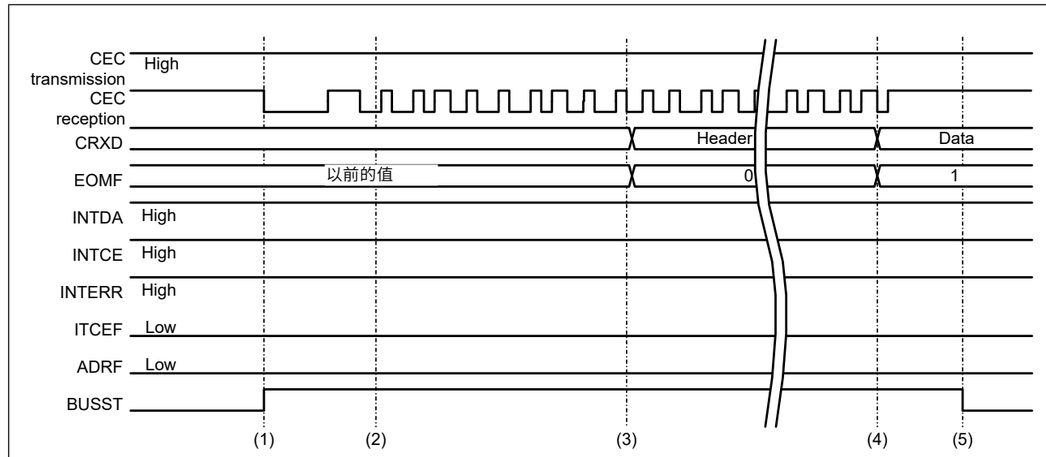
- Logical 1 is transmitted at the ACK bit timing in a normal operation.
- If reception failed or CECRXEN = 0 is set, logical 0 is transmitted at the ACK bit timing.

(3) CEC reception interrupt

Three interrupt functions, namely a data interrupt (INTDA), communication complete interrupt (INTCE), and error interrupt (INTERR) are provided. Figure 37.21 shows the timing for generating interrupts during CEC reception.

A data interrupt (INTDA) is output at the following timings during reception (follower):

- When the address received at the header block of a direct address communication matched the local address



Note: 图37.20中的(1)至(5)对应于表37.11中的(1)至(5)。

Figure 37.20 基本接收时序（2）（CECCTL0.CECRXEN=1，直接地址，地址不匹配，CECCTL1.CINTMK = 0)

Table 37.11 CEC接收操作程序（二）

Stage	Step	软件操作	CEC state
CEC接收操作	1	—	[Start bit detection] 检测到CEC接收信号的下降沿并开始接收操作。设置BUSST标志(1)。[采样] 数据在NOMT设置时间被采样并顺序存储在移位寄存器(2)中。[地址匹配中断] 不生成INTDA，也不返回ACK和NACK，因为在头块接收到的地址与本地地址不匹配并且CINTMK为0(3)。但是，为了检查位长和检测通信完成，继续监视CEC线路。【ACK位传输】 ACK和NACK均不返回，因为在其他站(4)之间执行通信。[接收完成] 其他站之间的通信是完整的，因为 接收到EOM=1，根据SFT[1:0]位设置计算无信号时间，并将BUSST清除为0(5)。

(2) 广播接收

接收流程和定时检查周期与直接地址接收相同。如果发起方发送的目的地址是0xF，则通信操作为广播接收。

与直接地址接收的区别如下：

- ●在正常操作中，在ACK位时序发送逻辑1。
- ●如果接收失败或设置CECRXEN=0，则在ACK位定时发送逻辑0。

(3) CEC接收中断

提供了三种中断功能，即数据中断（INTDA）、通信完成中断（INTCE）和错误中断（INTERR）。图37.21显示了在CEC接收期间产生中断的时序。

接收期间（跟随器）在以下时序输出数据中断（INTDA）：

- ●直接地址通信的报头块接收到的地址与本地地址匹配时

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- When address reception is complete at the header block of a direct address communication when CECCTL1.CINTMK = 1 is set
- When address reception of a broadcast communication is complete at the header block
- When data reception is complete at the data block and the receive data is stored in the CRXD register

Communication complete interrupt INTCE is output at the following timings during reception (follower):

- CECCTL1.CESEL[1:0] = 00b
  INTCE is output if receiving the ACK bit of the last frame (EOM = 1) ends, if the signal-free time is counted, if the falling edge of the CEC line is detected in the high-level period of the ACK bit of the last frame, or while the signal-free time is counted.
- CECCTL1.CESEL[1:0] = 01b
  INTCE is output if receiving the ACK bit of the last frame (EOM = 1) ends, if the falling edge of the CEC line is detected in the high-level period of the ACK bit of the last frame, or while the signal-free time is counted.
- CECCTL1.CESEL[1:0] = 10b
  INTCE is output if the signal-free time is counted.

An error interrupt (INTERR) is output at the following timings during reception (follower):

- When a timing error is detected
- When an overrun error is detected
- When a bus lock error is detected while CECCTL1.BLERRD = 1 is set

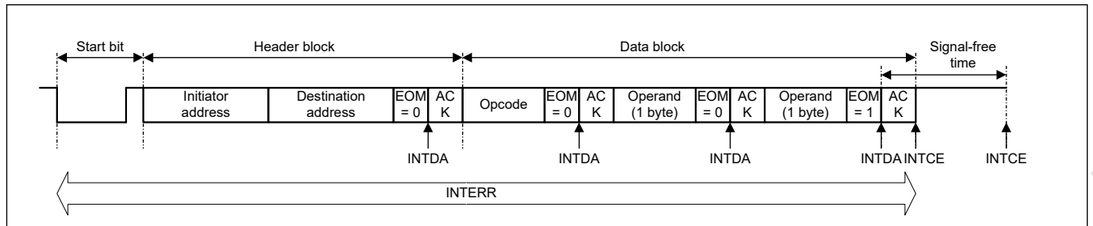

Figure 37.21 Basic reception interrupt timing

37.3.3.6 Status Flag Functions

Table 37.12 lists status flags.

Table 37.12 Status flags

No.	Status flag	Register.Bit symbol
1	Address match detection flag	CECS.ADRF
2	Bus busy detection flag	CECS.BUSST
3	Transmission status flag	CECS.TXST
4	EOM flag	CECS.EOMF
5	INTCE generation source flag	CECS.ITCEF
6	Signal-free time rewrite disable report flag	CECS.SFTST
7	CEC line monitor	CECEXMON.CECLNMON
8	ACK flag	CECEXMON.ACKF

(1) Address match detection flag

As shown in Figure 37.22, during follower operation, if the destination address of the header block received during direct address communication matches the address set by the CEC local address setting register (CADR) or during broadcast communication, the address match flag (CECS.ADRF) is set to 1 at the same time when a data interrupt (INTDA) of the header block is generated.

●设置CECCTL1.CINTMK=1时，在直接地址通信的报头块中完成地址接收时

●在报头块完成广播通信的地址接收时

●当数据块的数据接收完成并且接收数据存储在CRXD寄存器中时

通信完成中断INTCE在接收期间（跟随器）按以下时序输出：

- CECCTL1.CESEL[1:0] = 00b
  如果接收到最后一帧的ACK位（EOM=1）结束，如果计算无信号时间，如果在ACK位的高电平期间检测到CEC线的下降沿，则输出INTCE最后一帧，或在计算无信号时间时。
- CECCTL1.CESEL[1:0] = 01b
  如果接收到最后一帧的ACK位（EOM=1）结束，如果在最后一帧的ACK位的高电平期间检测到CEC线的下降沿，或者在无信号时，输出INTCE时间被计算。
- CECCTL1.CESEL[1:0] = 10b
  如果计算了无信号时间，则输出INTCE。

接收期间（跟随器）在以下时序输出错误中断（INTERR）：

●检测到定时错误时

●检测到溢出错误时

●CECCTL1.BLERRD=1时检测到总线锁定错误时

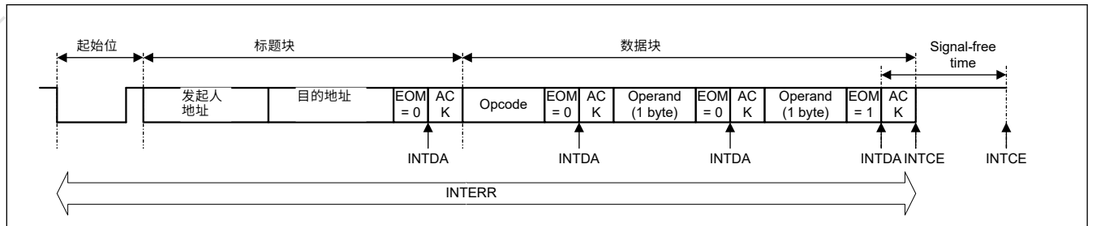

Figure 37.21 基本接收中断时序

37.3.3.6 状态标志功能

表37.12列出了状态标志。

Table 37.12 状态标志

No.	状态标志	Register.Bit symbol
1	地址匹配检测标志	CECS.ADRF
2	总线繁忙检测标志	CECS.BUSST
3	传输状态标志	CECS.TXST
4	EOM flag	CECS.EOMF
5	INTCE生成源标志	CECS.ITCEF
6	无信号时间重写禁用报告标志	CECS.SFTST
7	CEC线路监视器	CECEXMON.CECLNMON
8	确认标志	CECEXMON.ACKF

(1) 地址匹配检测标志

如图37.22所示，在跟随器操作期间，如果在直接地址通信期间接收到的头块的目标地址与CEC本地地址设置寄存器(CADR)或广播通信期间设置的地址匹配，则地址匹配标志(CECS.ADRF)在产生头块的数据中断(INTDA)的同时设置为1。

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The address match flag is cleared at the timing of the communication completion interrupt (INTCE) that is generated on completion of the signal-free time counting after the last frame (EOM = 1) is received.

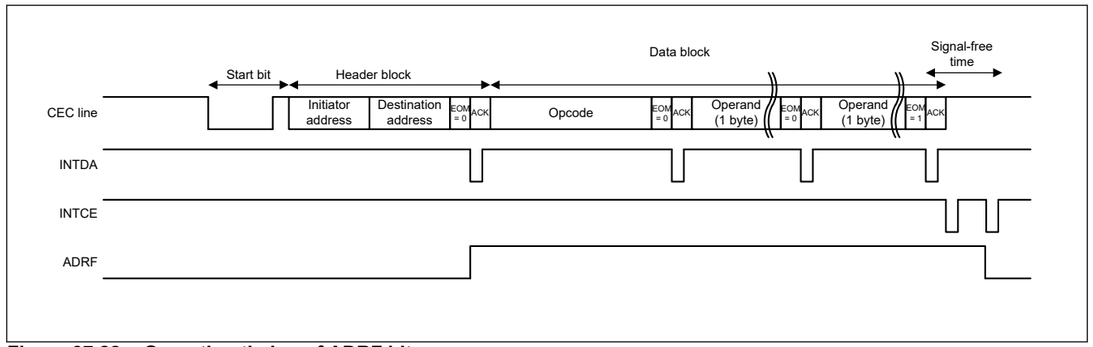
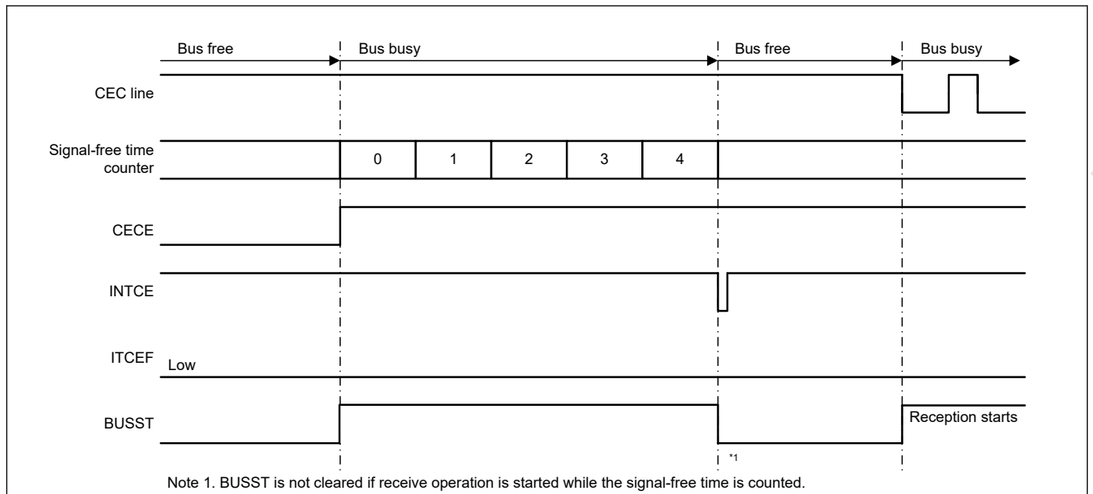


Figure 37.22 Operation timing of ADRF bit

(2) Bus busy detection flag

Figure 37.23 to Figure 37.25 show the timing operation of the Bus Busy Flag (CECS.BUSST). When CEC operation is enabled (CECCTL0.CECE = 0→1) or operation of the CEC line is detected, the Bus Busy Flag (CECS.BUSST) is set. After communication completes and the signal-free time has elapsed, the Bus Busy Flag is then cleared.



Note 1. BUSST is not cleared if receive operation is started while the signal-free time is counted.

Figure 37.23 Timing at the start of reception when CECE = 1

地址匹配标志在接收到最后一帧(EOM=1)后的无信号时间计数完成时产生的通信完成中断(INTCE)时被清除。

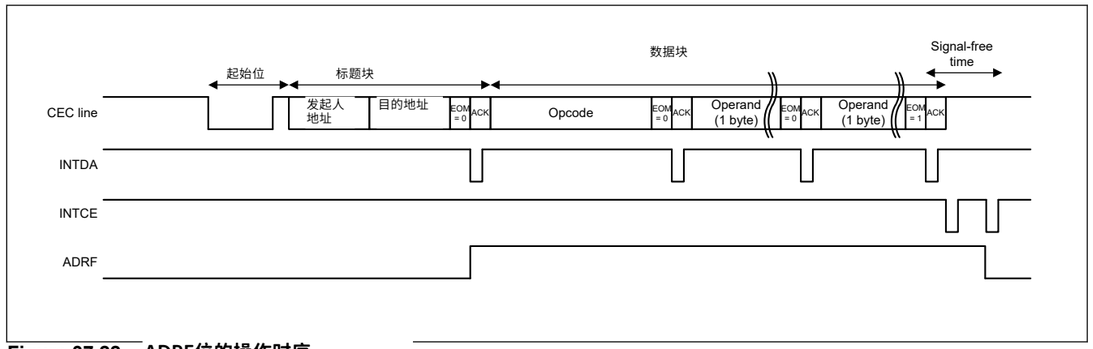
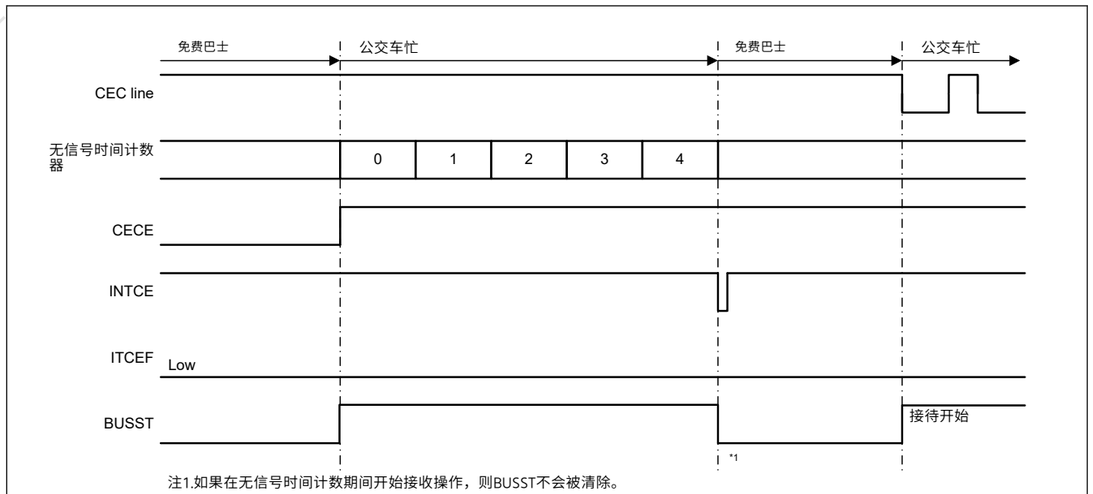


Figure 37.22 ADRF位的操作时序

(2) 总线繁忙检测标志

图37.23至图37.25显示了总线忙标志(CECS.BUSST)的时序操作。CEC运行时使能（CECCTL0.CECE=0→1）或检测到CEC线路的操作，则设置总线忙标志（CECS.BUSST）。通信完成且无信号时间过去后，总线忙标志将被清除。



注1.如果在无信号时间计数期间开始接收操作，则BUSST不会被清除。

Figure 37.23 CECE=1时开始接收的时间

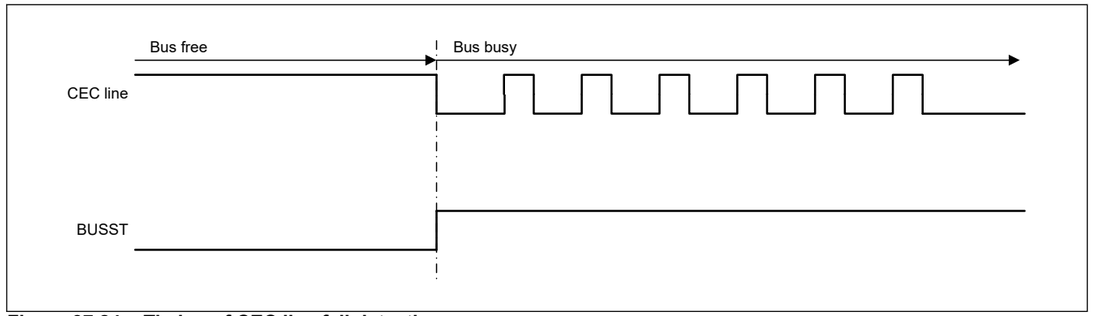


Figure 37.24 Timing of CEC line fall detection

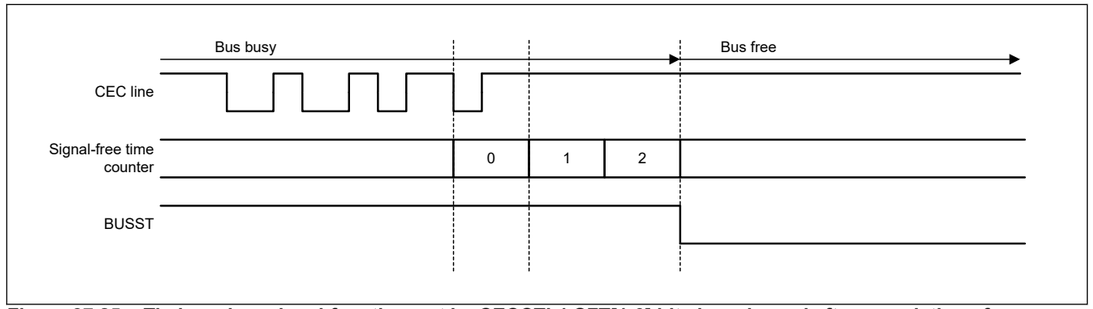


Figure 37.25 Timing when signal-free time set by CECCTL1.SFT[1:0] bits has elapsed after completion of communication

(3) Transmission status flag

As shown in Figure 37.26, when 1 is written to the Transmission Start Trigger Bit (CECCTL0.TXTRG) during initiator operation, the transmission status flag (CECS.TXST) is set.

The transmission status flag is cleared when the communication complete interrupt (INTCE) that is generated on completion of ACK reception for the data block with EOM = 1. However, as shown in Figure 37.27, if arbitration is lost, the transmission status flag is cleared at the same time when an error interrupt (INTERR) is generated and the Arbitration Loss Detection Flag (CECES.AERR) is set.

Likewise, if an underrun error occurs, the Transmission Status Flag is cleared as the same time when an error interrupt is generated.

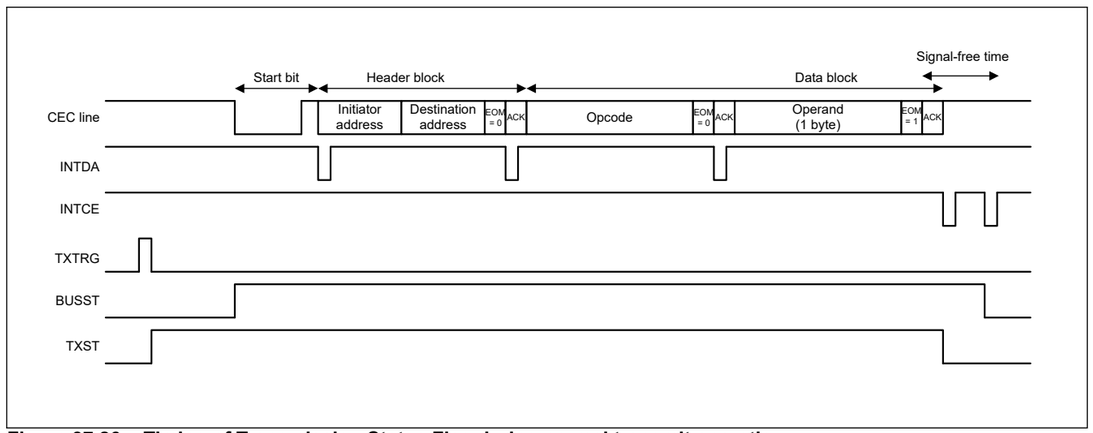


Figure 37.26 Timing of Transmission Status Flag during normal transmit operation

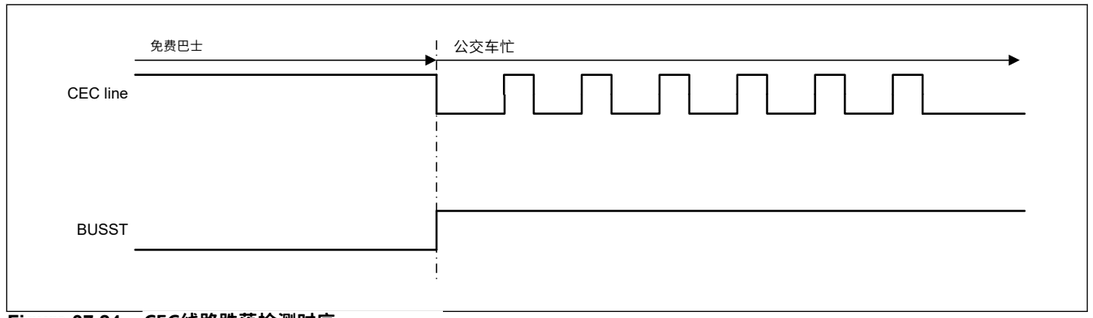


Figure 37.24 CEC线路跌落检测时序

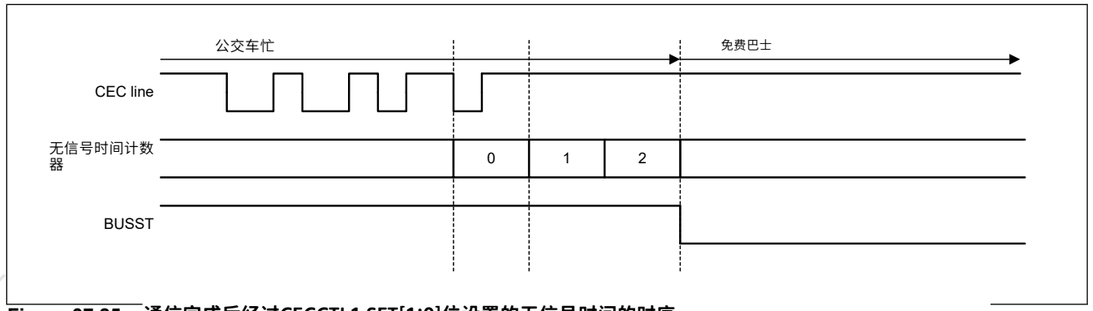


Figure 37.25 通信完成后经过CECCTL1.SFT[1:0]位设置的无信号时间的时序

(3) 传输状态标志

如图37.26所示，当在启动器操作期间向发送开始触发位(CECCTL0.TXTRG)写入1时，发送状态标志(CECS.TXST)被置位。

当EOM=1的数据块的ACK接收完成时产生的通信完成中断(INTCE)时，发送状态标志被清除。但是，如图37.27所示，如果仲裁失败，则发送状态标志被清除同时产生错误中断(INTERR)并设置仲裁丢失检测标志(CECES.AERR)。

同样，如果发生欠载错误，则在产生错误中断的同时清除传输状态标志。

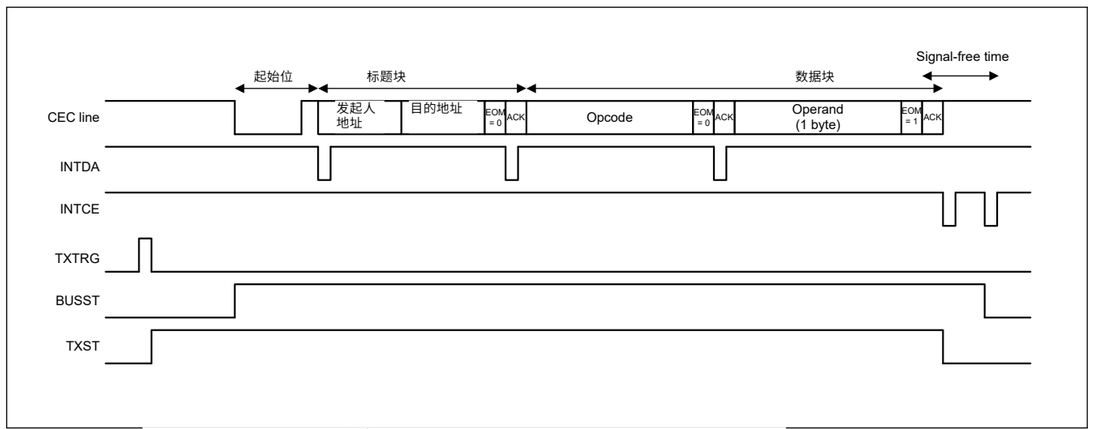


Figure 37.26 正常发送操作期间发送状态标志的时序

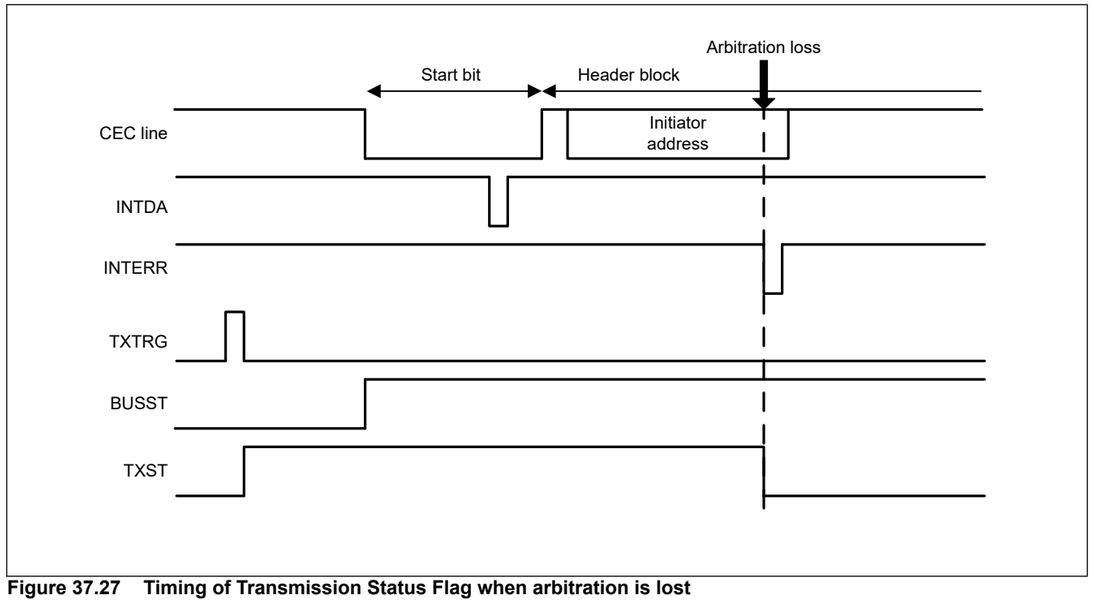


Figure 37.27 Timing of Transmission Status Flag when arbitration is lost

(4) EOM flag

As shown in Figure 37.28, during follower operation, the EOM flag (CECS.EOMF) is updated at the same time when a data interrupt (INTDA) is generated.

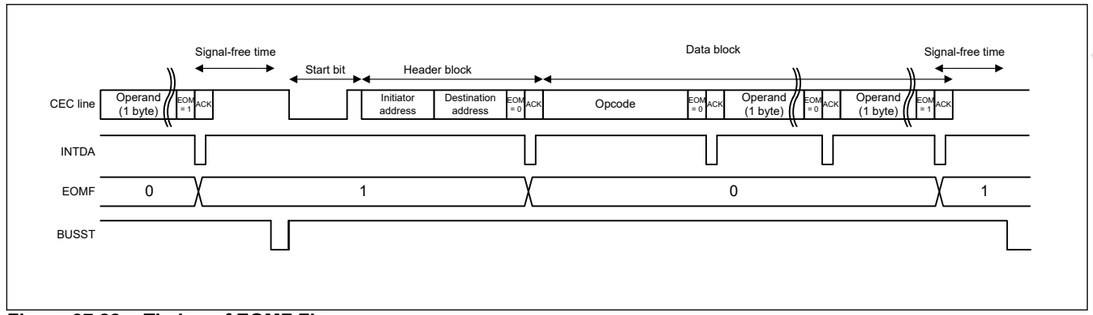


Figure 37.28 Timing of EOMF Flag

(5) INTCE generation source flag

This flag indicates which source was the generation source when a communication complete interrupt (INTCE) is generated. The INTCE Generation Source Flag (CECS.ITCEF) is set at the same time as the communication complete interrupt (INTCE) at the timing of ACK reception of the last block or when an error occurs.

After communication is complete, the INTCE Generation Source Flag is cleared when the signal-free time has elapsed. However, if receive operation is started during the signal-free time, the INTCE Generation Source Flag is not cleared and remains 1. Figure 37.29 shows an example of using the INTCE Generation Source Flag (CECS.ITCEF) to check the INTCE generation source.

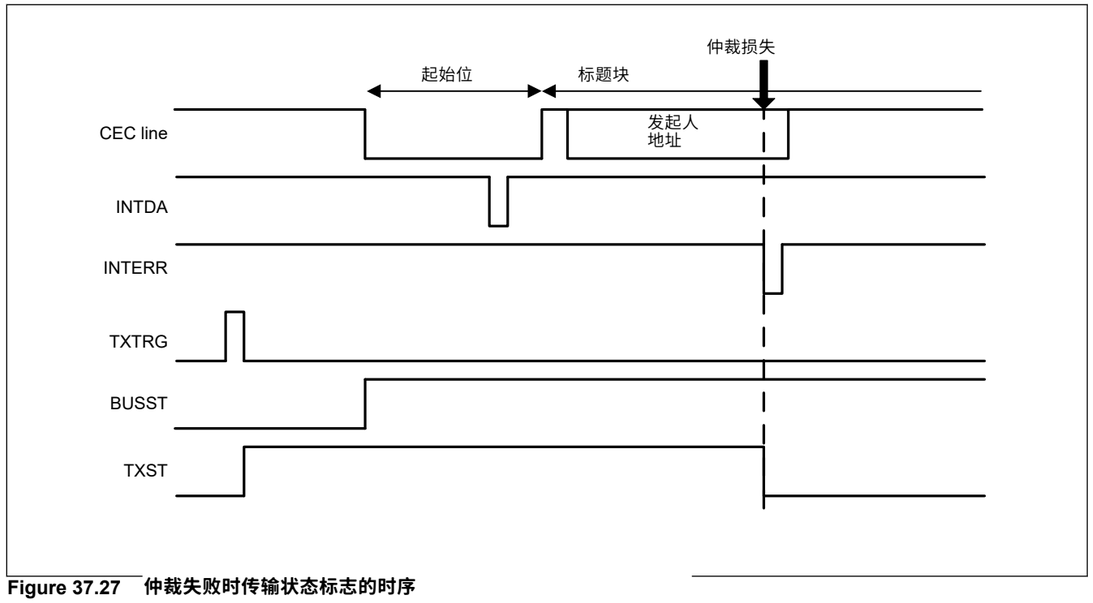


Figure 37.27 仲裁失败时传输状态标志的时序

(4) EOM flag

如图37.28所示，在跟随器操作期间，EOM标志(CECS.EOMF)会在产生数据中断(INTDA)的同时更新。

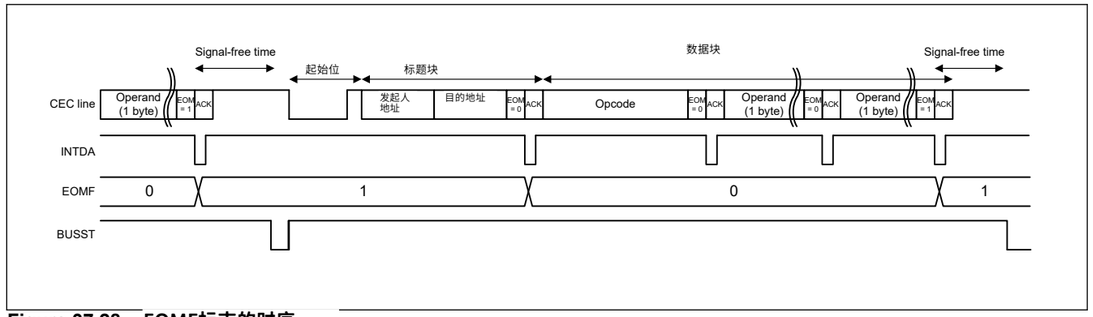


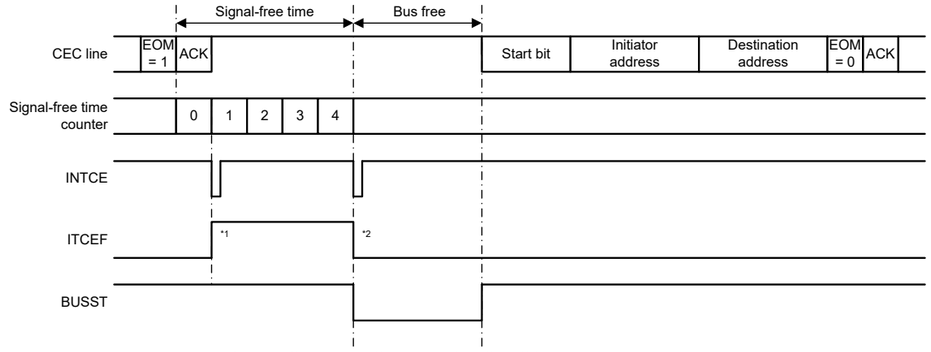
Figure 37.28 EOMF标志的时序

(5) INTCE生成源标志

该标志指示在产生通信完成中断(INTCE)时哪个源是产生源。INTCE发生源标志(CECS.ITCEF)在收到最后一个块的ACK时或发生错误时与通信完成中断(INTCE)同时设置。

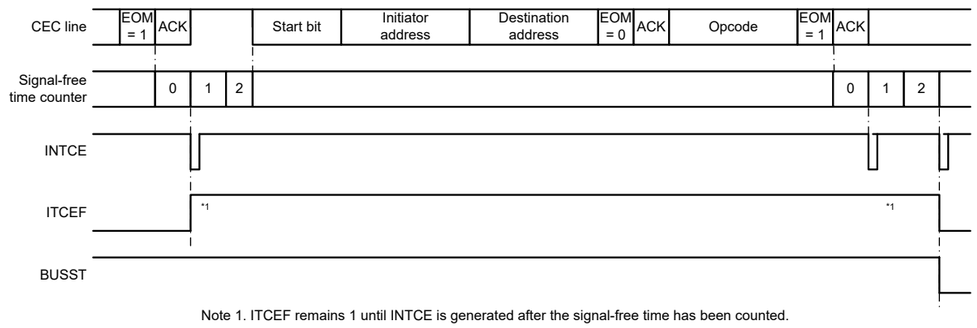
通信完成后，INTCE生成源标志在无信号时间过后被清除。
但是，如果在无信号时间内开始接收操作，则INTCE生成源标志不会被清除并保持为1。图37.29显示了使用INTCE生成源标志(CECS.ITCEF)检查INTCE生成源的示例。

(1) Reception is started after the signal-free time has been counted



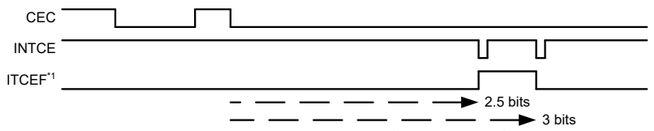
Note 1. If ITCEF is 1, INTCE is generated after ACK has been received.
Note 2. If ITCEF is 0, INTCE is generated after the signal-free time has been counted.

(2) Reception is started during the signal-free time



Note 1. ITCEF remains 1 until INTCE is generated after the signal-free time has been counted.

(3) When a bus lock error is detected



Note 1. This bit is set to 1 when INTCE is generated if a bus lock error is detected, and cleared to 0 when INTCE is generated after the signal-free time is counted.

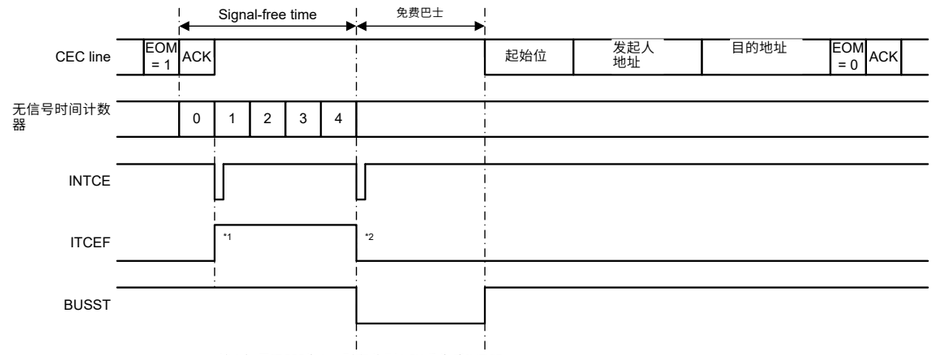
Figure 37.29 Using ITCEF to check INTCE generation source when CECCTL1.CESEL[1:0] = 00b

(6) Signal-free time rewrite disable report flag

This flag indicates the rewrite disable period of the signal-free time data width select bits (CECCTL1.SFT[1:0]). As shown in Figure 37.30, when the CECCTL1.SFT[1:0] bits are accessed, the Signal-free Time Rewrite Disable Report Flag (CECS.SFTST) is set.

This flag is cleared after the CECCTL1.SFT[1:0] bit setting is applied to the CEC internal control circuit.

(1)计算无信号时间后开始接收

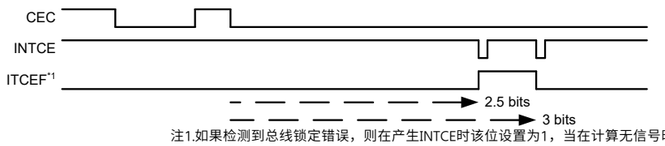


注1.如果ITCEF为1，则在收到ACK后生成INTCE。
注2.如果ITCEF为0，则在计算无信号时间后生成INTCE。

(2)在无信号时间内开始接收

注1.ITCEF保持为1，直到在计算无信号时间后生成INTCE。

(3)检测到总线锁定错误时



注1.如果检测到总线锁定错误，则在产生INTCE时该位设置为1，当在计算无信号时间后产生INTCE时，该位清零。

Figure 37.29 CECCTL1.CESEL[1:0]=00b时使用ITCEF检查INTCE生成源

(6) 无信号时间重写禁用报告标志

该标志指示无信号时间数据宽度选择位(CECCTL1.SFT[1:0])的重写禁用周期。如图37.30所示，当访问CECCTL1.SFT[1:0]位时，将设置无信号时间重写禁用报告标志(CECS.SFTST)。

在CECCTL1.SFT[1:0]位设置应用于CEC内部控制电路后，该标志被清除。

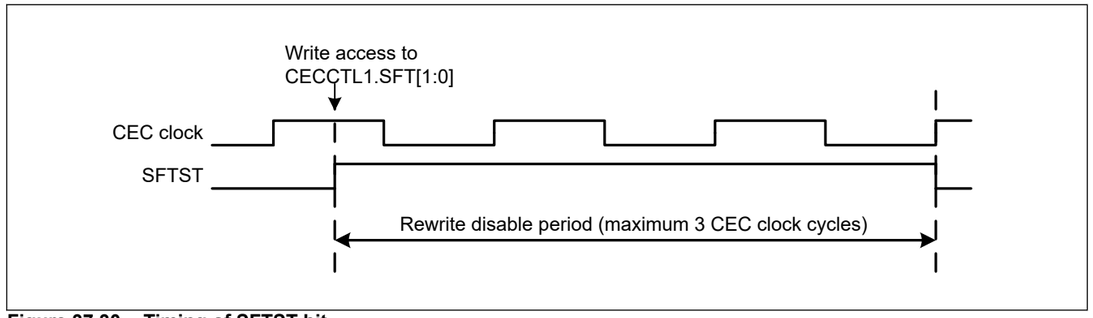


Figure 37.30 Timing of SFTST bit

(7) CEC line monitor

Figure 37.31 shows the timing operation of the CECEXMON.CECLNMON bit.

The state of the CEC pin can be read by reading the CECEXMON.CECLNMON bit.

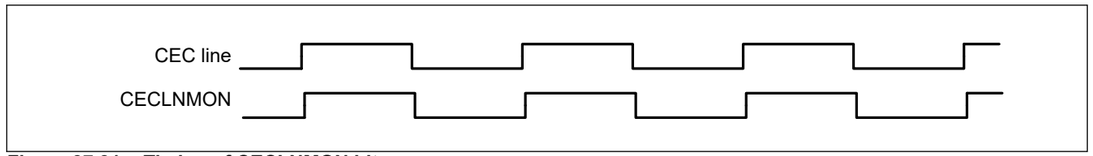


Figure 37.31 Timing of CECLNMON bit

(8) ACK flag

During follower operation, the ACK flag (CECEXMON.ACKF) is updated at the timing of ACK bit reception.

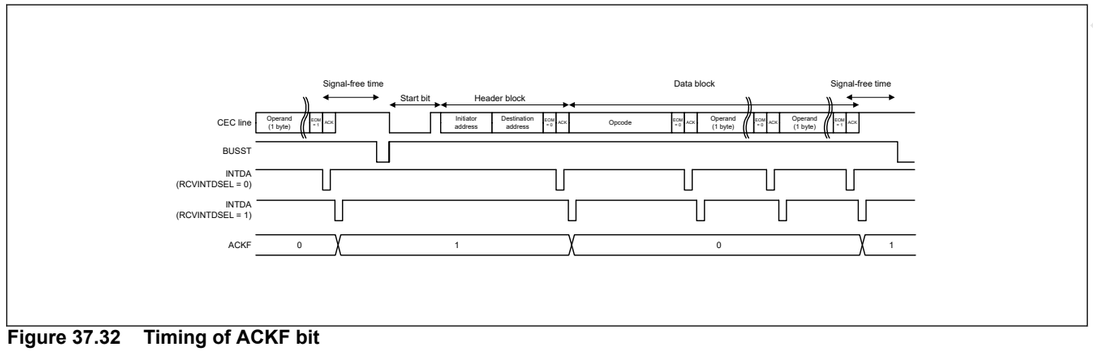


Figure 37.32 Timing of ACKF bit

As shown in Figure 37.32, when reading the ACKF bit while CECEXMD.RCVINTDSEL = 0, the received ACK state can be read by reading this bit when a 1-bit wait time has elapsed after a data interrupt (INTDA) is generated. (if this bit is read after a data interrupt is generated, the ACK of the previously received data is read).

When reading the ACKF bit while CECEXMD.RCVINTDSEL = 1, read this bit after a data interrupt (INTDA) is generated. The ACK of the newest received data can be read.

37.3.3.7 CEC Interrupts

The CEC transmission/reception circuit generates three interrupt requests.

- Data interrupt (INTDA)
  During transmission, this interrupt is generated at the timing when transmission of each block is started. During reception, this interrupt is generated at the timing of each completion of EOM bit reception if CECEXMD.RCVINTDSEL is 0, and each completion of ACK bit transmission if CECEXMD.RCVINTDSEL = 1, depending on the value of the Reception Interrupt Timing Change bit.

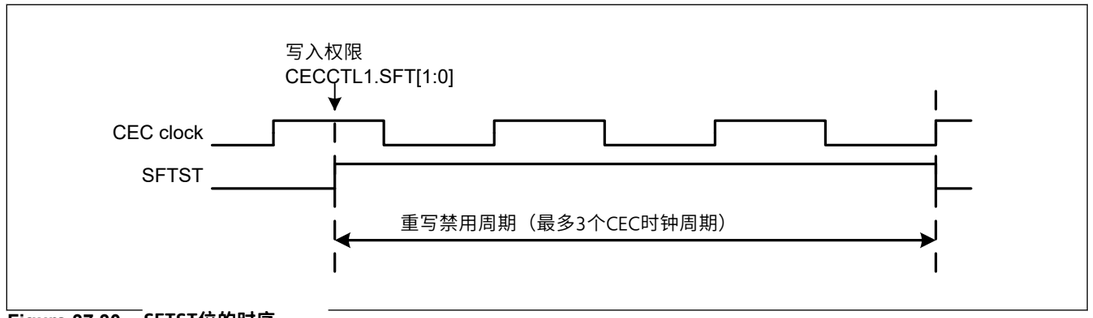


Figure 37.30 SFTST位的时序

(7) CEC线路监视器

图37.31显示了CECEXMON.CECLNMON位的时序操作。

通过读取CECEXMON.CECLNMON位可以读取CEC引脚的状态。

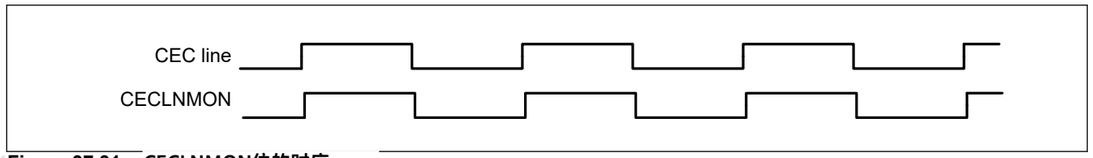


Figure 37.31 CECLNMON位的时序

(8) 确认标志

在跟随器操作期间，ACK标志(CECEXMON.ACKF)在ACK位接收时更新。

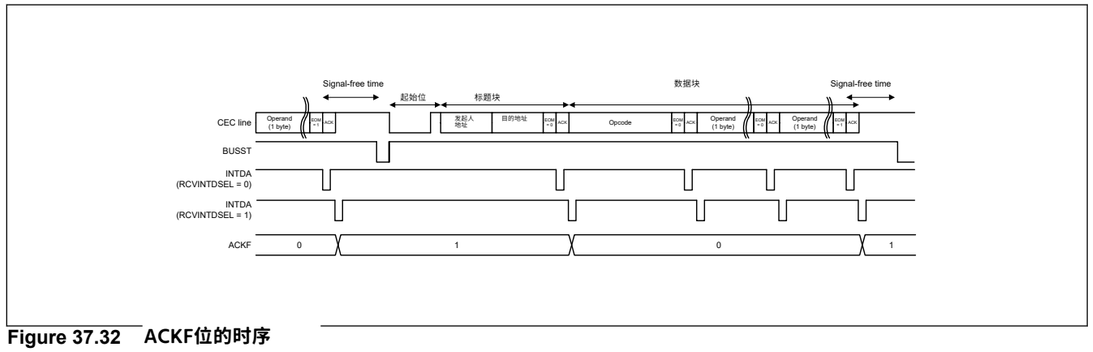


Figure 37.32 ACKF位的时序

如图37.32所示，当CECEXMD.RCVINTDSEL=0时读取ACKF位时，在产生数据中断(INTDA)后经过1位等待时间后，可以通过读取该位读取接收到的ACK状态。（如果在产生数据中断后读取该位，则读取之前接收到的数据的ACK）。

在CECEXMD.RCVINTDSEL=1时读取ACKF位时，在产生数据中断(INTDA)后读取该位。可以读取最新接收数据的ACK。

37.3.3.7 CEC Interrupts

CEC发送接收电路产生三个中断请求。

- 数据中断（INTDA）
  在传输过程中，该中断在每个块的传输开始时产生。在接收期间，如果CECEXMD.RCVINTDSEL为0，则在每次EOM位接收完成时产生此中断；如果CECEXMD.RCVINTDSEL=1，则在每次完成ACK位发送时产生此中断，具体取决于接收中断时序更改位的值。

- Communication complete interrupt (INTCE)
  During both transmission and reception, this interrupt is generated on completion of the message or signal-free time is complete. It is also possible to select only one of the two (completion of the message or signal-free time) by setting the communication complete Interrupt Generation Timing Change Bits (CECCTL1.CESEL[1:0]).
- Error interrupt (INTERR)
  This interrupt is generated when an error is generated.

Figure 37.33 shows the timing for generating each interrupt.

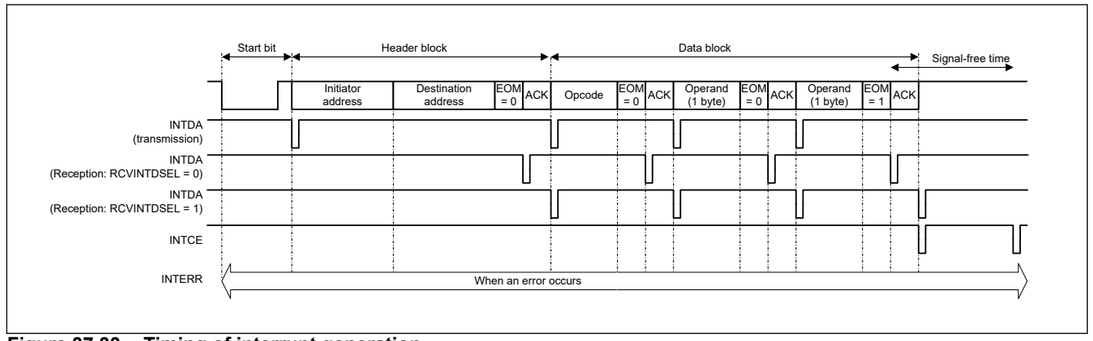


Figure 37.33 Timing of interrupt generation

Each of three interrupt requests can be used to output two types of interrupt requests. Use the two types exclusively depending on the application of the interrupt request. See Table 37.13 for details on the application corresponding to each CEC interrupt request.

Table 37.13 CEC interrupt sources

Name	Corresponding source				
	CPU interrupt	DTC activation	DMAC activation	Return from Software Standby mode	Return from All-Module Clock Stop mode
INTDA	Possible	Possible	Possible	Not possible	Not possible
INTCE	Possible	Possible	Possible	Not possible	Not possible
INTERR	Possible	Not possible	Not possible	Not possible	Not possible

37.3.3.7.1 Error Interrupt Sources

Table 37.14 lists the seven errors that CEC can detect for the initiator and follower, and Figure 37.34 shows the error detection period.

Table 37.14 Errors that can be detected for the initiator and follower

Error	Initiator	Follower
(1) Transmission error	Detected	Not detected
(2) ACK error	Detected	Not detected
(3) Underrun error	Detected	Not detected
(4) Arbitration error	Detected	Not detected
(5-1) Timing error (low-level width)	Detected	Detected
(5-2) Timing error (bit width)	Detected	Detected
(6) Overrun error	Not detected	Detected
(7) Bus lock error	Not detected	Detected

●通讯完成中断（INTCE）
在发送和接收期间，该中断在消息完成或无信号时间结束时产生。也可以通过设置通信完成中断生成时序更改位(CECCTL1.CESEL[1:0])仅选择两者之一（消息完成或无信号时间）。

●错误中断（INTERR）
产生错误时会产生此中断。

图37.33显示了产生每个中断的时序。

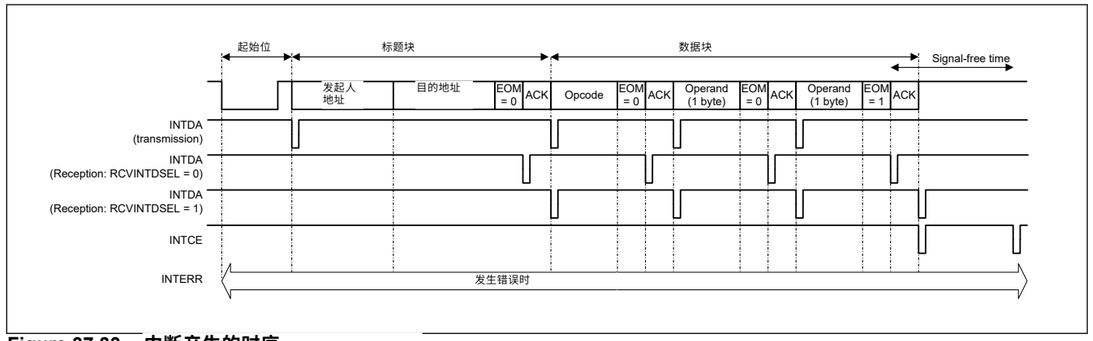


Figure 37.33 中断产生的时序

三个中断请求中的每一个都可用于输出两种类型的中断请求。根据中断请求的应用，专门使用这两种类型。有关每个CEC中断请求对应的应用程序的详细信息，请参见表37.13。

Table 37.13 CEC中断源

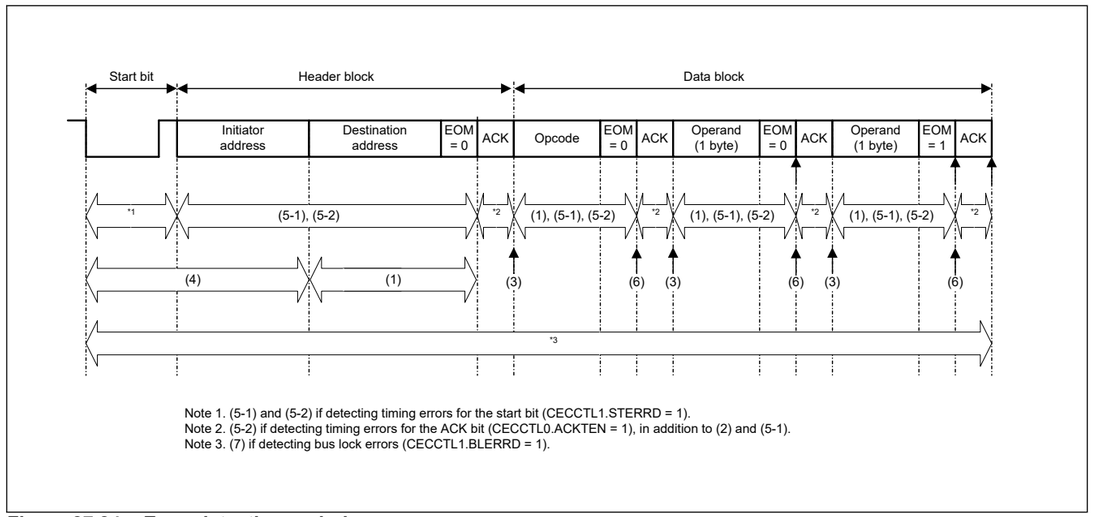
Name	对应来源				
	CPU中断	DTC activation	DMAC activation	从返回 软件待机模式	从所有返回 模块时钟停止模式
INTDA	Possible	Possible	Possible	不可能	不可能
INTCE	Possible	Possible	Possible	不可能	不可能
INTERR	Possible	不可能	不可能	不可能	不可能

37.3.3.7.1 错误中断源

表37.14列出了CEC可以为发起者和跟随者检测到的七个错误，图37.34显示了错误检测周期。

Table 37.14 可以为发起者和跟随者检测到的错误

Error	Initiator	Follower
(1)传输错误	Detected	没有检测到
(2)ACK错误	Detected	没有检测到
(3) Underrun error	Detected	没有检测到
(4)仲裁错误	Detected	没有检测到
(5-1)时序误差（低电平宽度）	Detected	Detected
(5-2)时序误差（位宽）	Detected	Detected
(6)超限错误	没有检测到	Detected
(7)总线锁定错误	没有检测到	Detected



Note 1. (5-1) and (5-2) if detecting timing errors for the start bit (CECCTL1.STERRD = 1).
Note 2. (5-2) if detecting timing errors for the ACK bit (CECCTL0.ACKTEN = 1), in addition to (2) and (5-1).
Note 3. (7) if detecting bus lock errors (CECCTL1.BLERRD = 1).

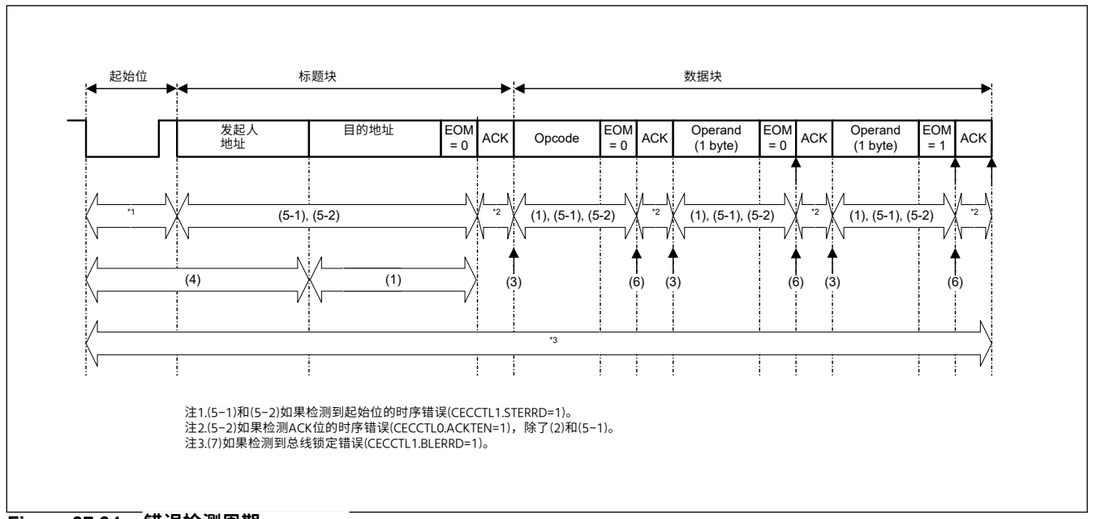
Figure 37.34 Error detection period

The details of each error are explained in the sections that follow.

(1) Transmission error

As shown in Figure 37.35, during initiator operation, the logic of the data the initiator transmitted is compared with that of the CEC line receive data and a transmission error occurs when they differ. Errors are determined at the timing specified by the value set to the CEC Reception Data Sampling Time Setting Register (NOMT). Errors are determined during the data bit period of the frame that includes the EOM bit. An error interrupt (INTERR) is generated after error detection, the Transmission Error Detection Flag (CECES.TXERR) is set, and transmission is stopped according to the value of the flag.

A communication complete interrupt INTCE is generated at the end of the bit at which transmission stopped and after the signal-free time is counted, according to the values specified for CECCTL1.CESEL[1:0].



注1.(5-1)和(5-2)如果检测到起始位的时序错误(CECCTL1.STERRD=1)。
注2.(5-2)如果检测ACK位的时序错误(CECCTL0.ACKTEN=1)，除了(2)和(5-1)。
注3.(7)如果检测到总线锁定错误(CECCTL1.BLERRD=1)。

Figure 37.34 错误检测周期

每个错误的详细信息将在以下部分中进行说明。

(1) 传输错误

如图37.35所示，在发起者操作过程中，发起者发送数据的逻辑与CEC线路接收数据的逻辑进行比较，当两者不同时会发生传输错误。在CEC接收数据采样时间设置寄存器(NOMT)中设置的值指定的时间确定错误。错误是在包含EOM位的帧的数据位周期内确定的。错误检测后产生错误中断（INTERR），发送错误检测标志（CECES.TXERR）置位，根据标志值停止发送。

根据为CECCTL1.CESEL[1:0]指定的值，在传输停止位的末尾和对无信号时间进行计数后，将产生一个通信完成中断INTCE。

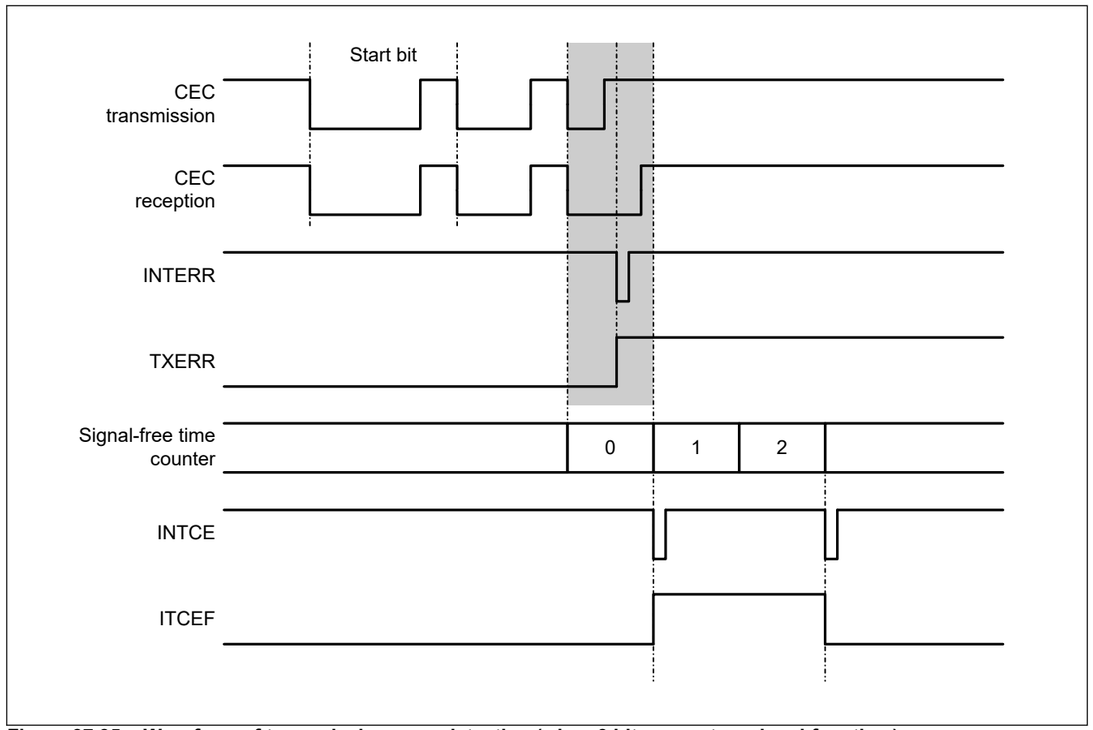


Figure 37.35 Waveform of transmission error detection (when 3 bits are set as signal-free time)

When a transmission error is detected, the transmit operation is stopped at the bit where the error was detected, regardless of the set value of the CECCTL0.EOM bit.

When EOM = 0 is received even though the initiator is transmitting EOM = 1, the transmission is a transmission error and therefore, stopped. Because EOM = 0, the follower determines that transmission should continue and so it waits for data reception. If CECCTL1.BLERRD is set to 1, whether the received data is at a high or low level can be detected.

(2) ACK error

During direct address transmission, an ACK error occurs when the initiator receives logical 1 at the ACK bit timing. During broadcast transmission, an ACK error occurs when the initiator receives logical 0 at the ACK bit timing. Figure 37.36 shows the timing of ACK error detection.

Errors are determined at the timing of the value set in the CEC Reception Data Sampling Time Setting Register (NOMT). After an error is detected, an error interrupt (INTERR) is generated and the ACK Error Detection Flag (CECES.ACKERR) is set. At the end of the ACK bit, communication standby state is entered and the signal-free time is counted. A communication complete interrupt (INTCE) occurs once or twice depending on the set values of the CECCTL1.CESEL[1:0] bits.

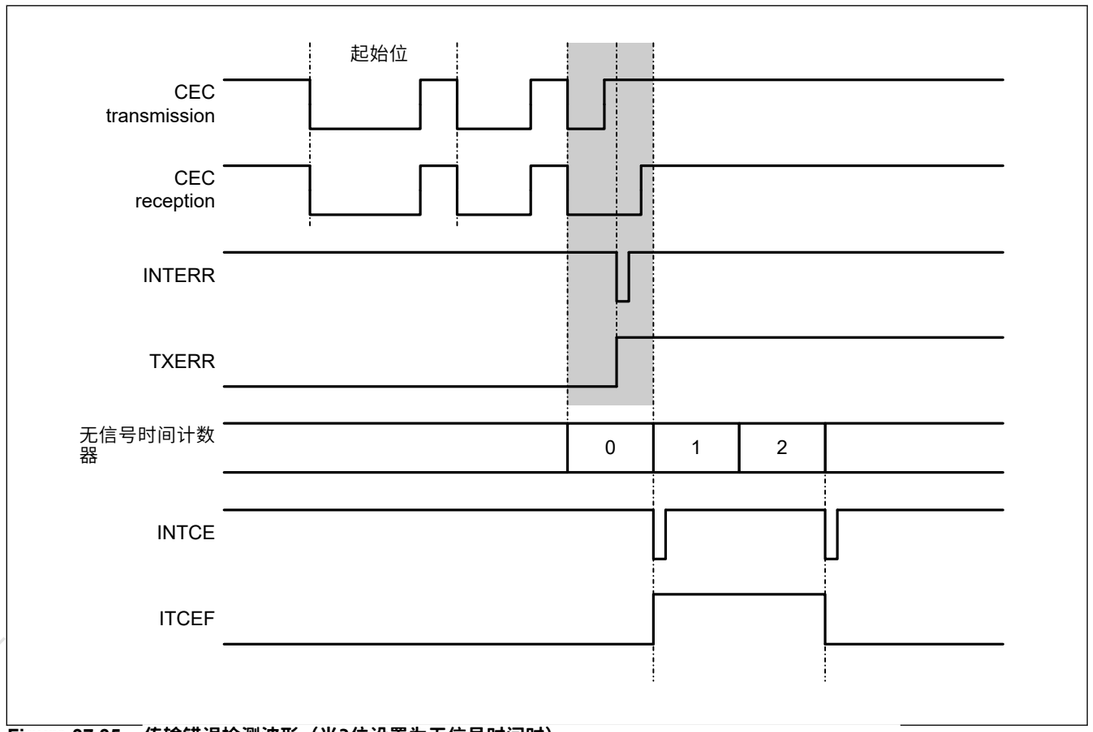


Figure 37.35 传输错误检测波形（当3位设置为无信号时间时）

当检测到传输错误时，无论CECCTL0.EOM位的设置值如何，发送操作都会在检测到错误的位停止。

即使发起方正在发送EOM=1，当接收到EOM=0时，传输是传输错误并因此停止。因为EOM=0，从机确定传输应该继续，因此它等待数据接收。如果CECCTL1.BLERRD设置为1，则可以检测接收到的数据是高电平还是低电平。

(2) 确认错误

在直接地址传输过程中，当发起方在ACK位时序接收到逻辑1时，会发生ACK错误。在广播传输过程中，当发起方在ACK位定时收到逻辑0时，会发生ACK错误。图37.36显示了ACK错误检测的时序。

在CEC接收数据采样时间设置寄存器(NOMT)中设置的值的时序确定错误。
检测到错误后，会产生错误中断(INTERR)并设置ACK错误检测标志(CECES.ACKERR)。在ACK位结束时，进入通信待机状态并计算无信号时间。根据CECCTL1.CESEL[1:0]位的设置值，会发生一次或两次通信完成中断(INTCE)。

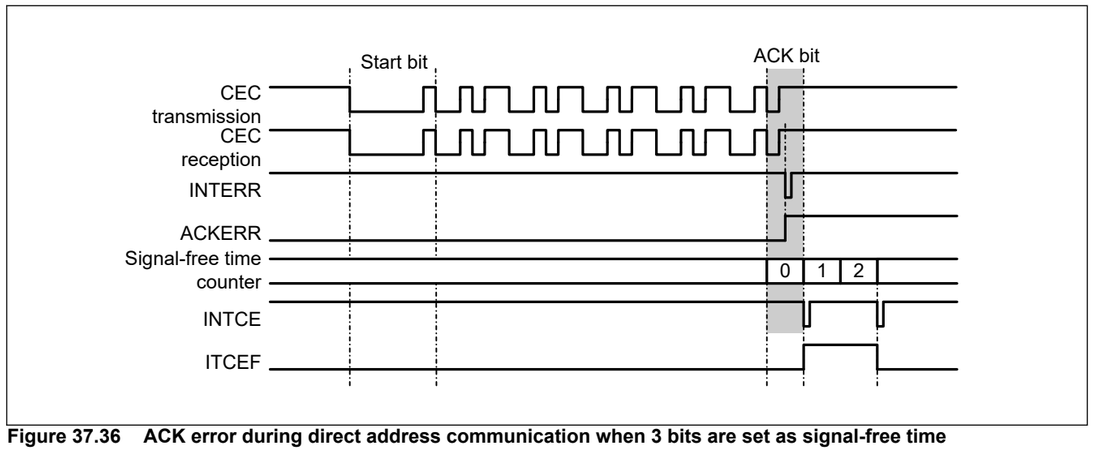


Figure 37.36 ACK error during direct address communication when 3 bits are set as signal-free time

(3) Underrun error

An underrun error occurs when no data is set to the transmission buffer when transmitting the next data is started. When an underrun is detected as shown in Figure 37.37, an error interrupt (INTERR) is generated, the Underrun Error Detection Flag (CECES.UERR) is set, the transmission is aborted, and communication standby state is entered. A communication complete interrupt (INTCE) occurs once or twice depending on the set values of the CECCTL1.CESEL[1:0] bits.

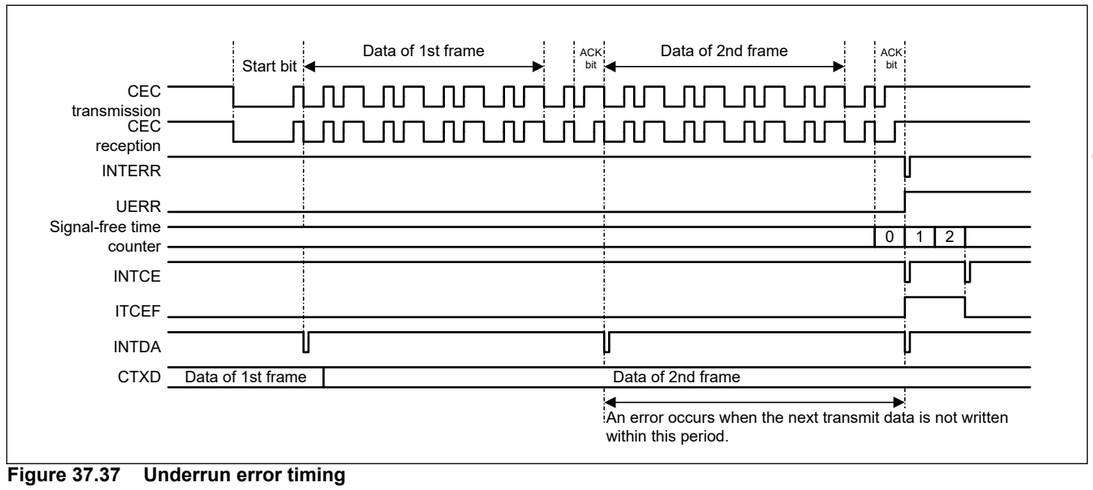


Figure 37.37 Underrun error timing

(4) Arbitration error

As shown in Figure 37.38, if logical 0 is received in response to logical 1 transmission during the period from the transmission start trigger (CECCTL0.TXTRG) being set to the source address being transmitted, an arbitration error occurs. Errors between setting the transmission start trigger and outputting the start bit are determined when low level is output to the CEC transmission signal. While the source address is being transmitted, errors are determined at the timing of the value set to the CEC Reception Data Sampling Time Setting Register (NOMT). After an error is detected, an error interrupt (INTERR) is generated and the Arbitration Loss Detection Flag (CECES.AERR) is set. At this time, the transmission is aborted, but the receive operation continues. Multiple error flags may be detected, as shown in Figure 37.39, until the source address detection period is entered.

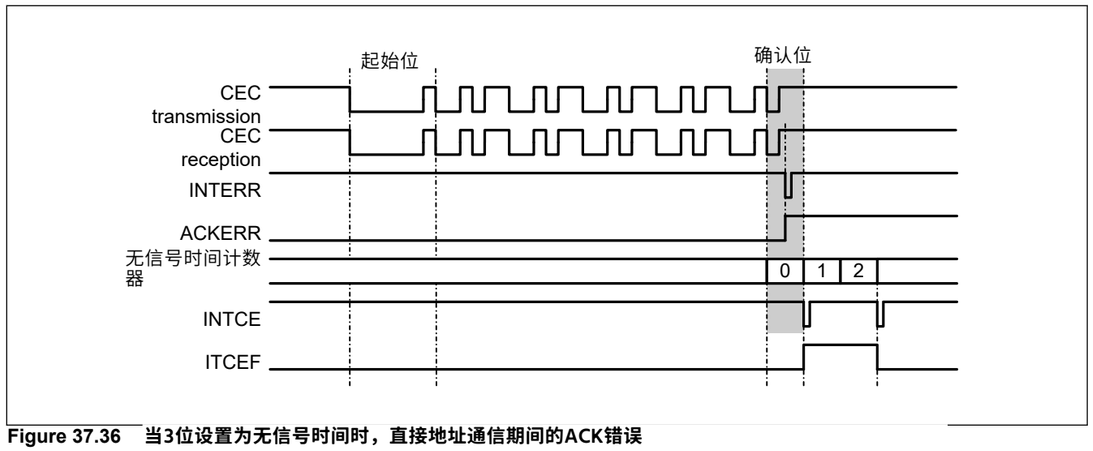


Figure 37.36 当3位设置为无信号时间时，直接地址通信期间的ACK错误

(3) Underrun error

开始发送下一个数据时，如果没有将数据设置到发送缓冲区，则会发生欠载错误。如图37.37所示，当检测到欠载时，会产生错误中断(INTERR)，设置欠载错误检测标志(CECES.UERR)，中止传输，进入通信待机状态。根据CECCTL1.CESEL[1:0]位的设置值，会发生一次或两次通信完成中断(INTCE)。

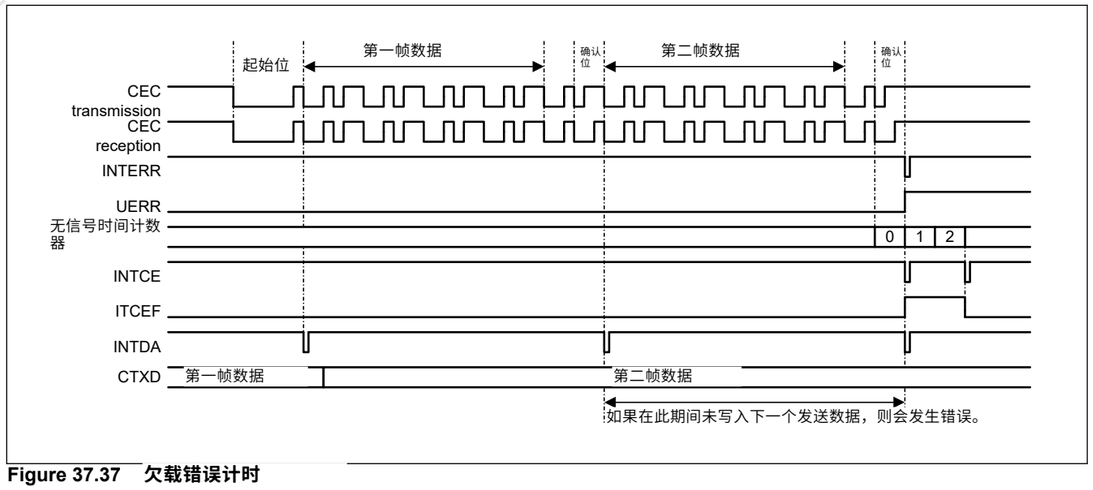


Figure 37.37 欠载错误计时

(4) 仲裁错误

如图37.38所示，如果在从设置发送开始触发(CECCTL0.TXTRG)到正在发送的源地址期间接收到逻辑0以响应逻辑1的发送，则会发生仲裁错误。当向CEC传输信号输出低电平时，确定设置传输启动触发和输出启动位之间的错误。在发送源地址时，在CEC接收数据采样时间设置寄存器(NOMT)中设置的值的时序确定错误。检测到错误后，会产生错误中断(INTERR)并设置仲裁丢失检测标志(CECES.AERR)。此时，发送被中止，但接收操作继续。可能会检测到多个错误标志，如图37.39所示，直到进入源地址检测周期。

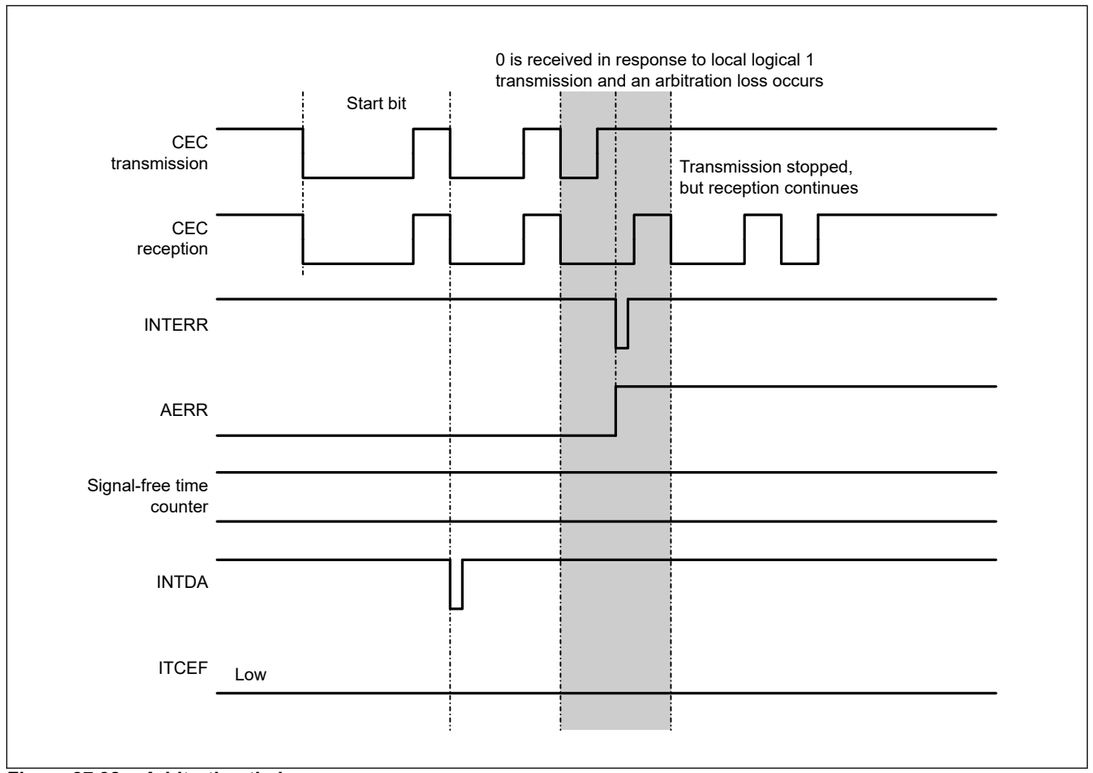


Figure 37.38 Arbitration timing

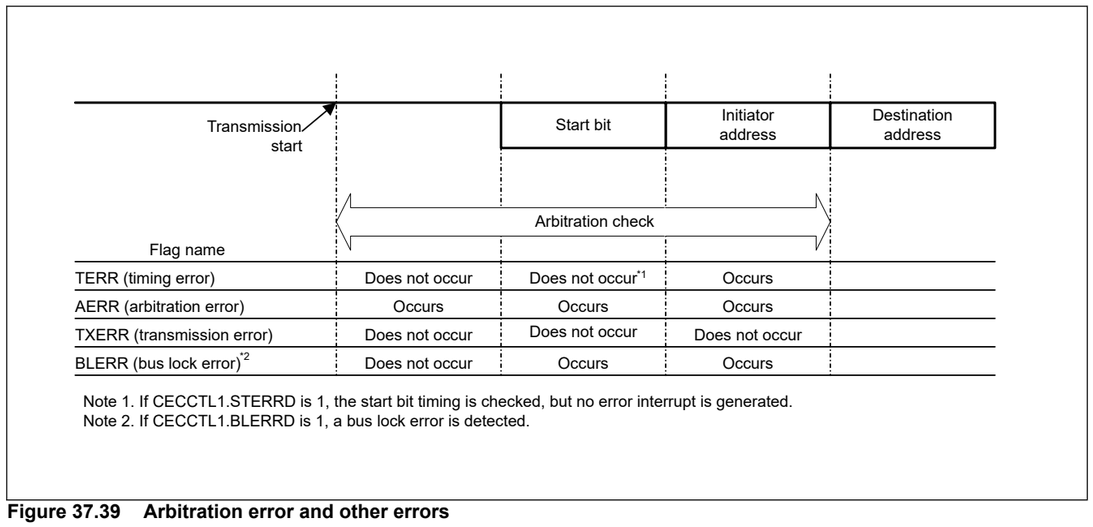


Figure 37.39 Arbitration error and other errors

Detailed description of arbitration error

Details about the arbitration check performed from the time when the transmission start trigger (CECCTL0.TXTRG) is set until the initiator address output period are provided in the sections that follow.

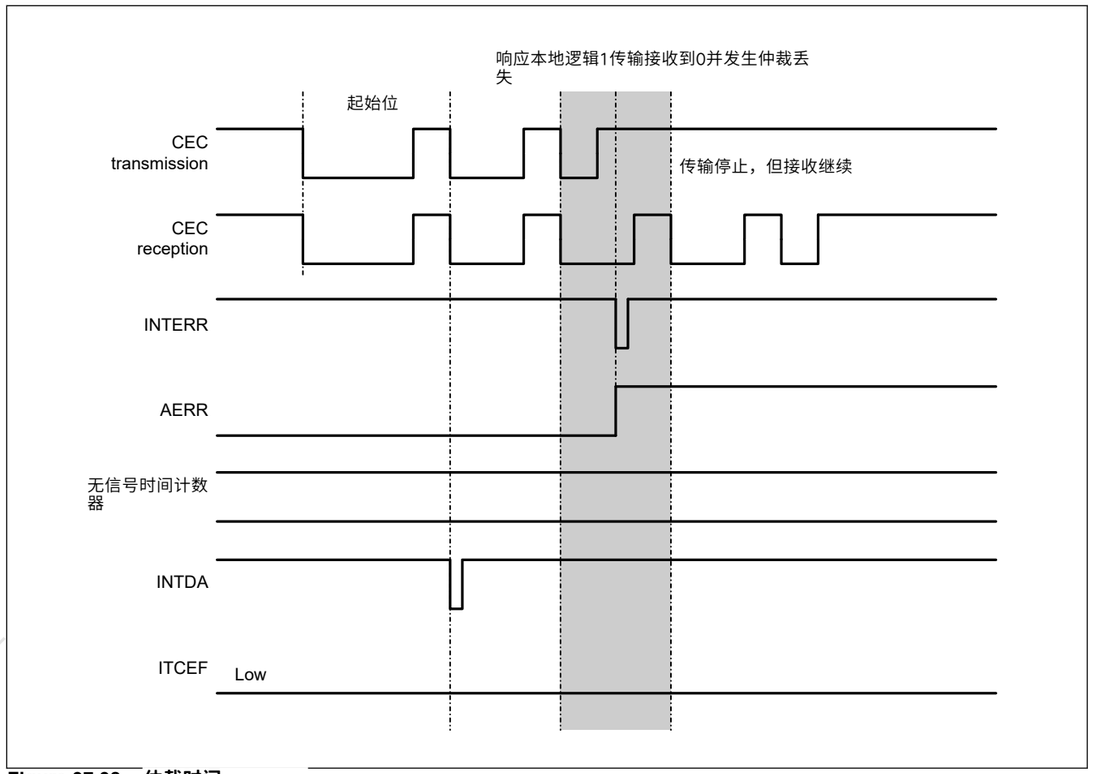


Figure 37.38 仲裁时间

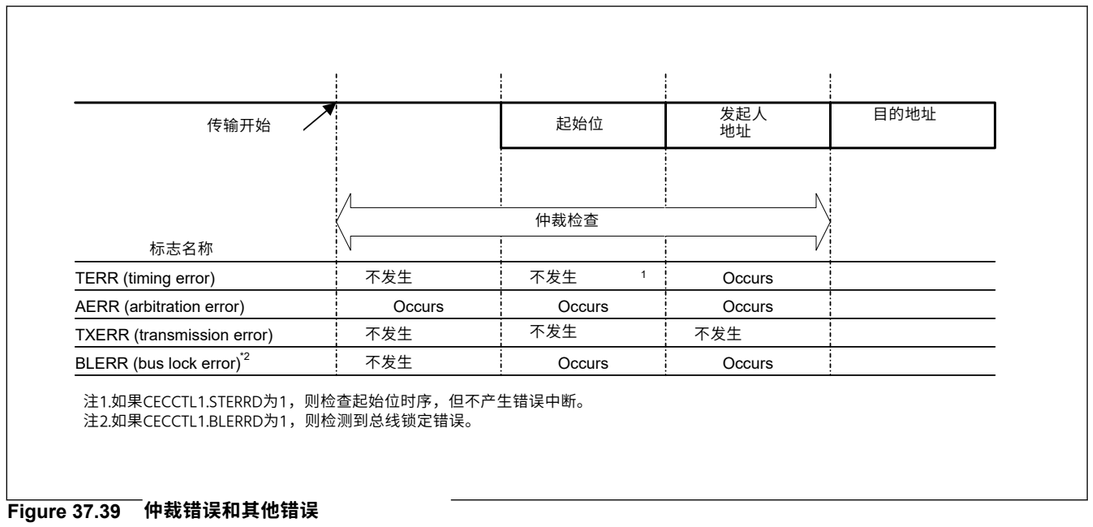


Figure 37.39 仲裁错误和其他错误

仲裁错误的详细描述

有关从设置发送开始触发(CECCTL0.TXTRG)到启动器地址输出周期执行的仲裁检查的详细信息将在以下部分中提供。

Arbitration check by setting transmission start trigger (CECCTL0.TXTRG)

The arbitration check is performed when two CEC clock cycles have elapsed after the transmission start trigger (CECCTL0.TXTRG) is set. If an arbitration loss is determined, an error interrupt (INTERR) is generated, the Arbitration Loss Detection Flag (CECES.AERR) is set, and the mode is switched to reception mode.

Start bit output period

If low level is detected at the reception line when the transmission start trigger (CECCTL0.TXTRG) is set and the start bit is actually output, the Arbitration Loss Detection Flag (CECES.AERR) is set and the mode is switched to reception mode. If the rising edge of the reception line is detected beyond the maximum low-level width of the start bit set by STATLH, the Arbitration Loss Detection Flag (CECES.AERR) is set and the mode is switched to reception mode.

Initiator address output period

After transmission of the start bit is complete, a logic check is performed at the same time as the transmission start of the initiator address. If an address earlier than the local address is detected, an error interrupt (INTERR) is generated, the Arbitration Loss Detection Flag (CECES.AERR) is set, and the mode is switched to reception mode.

(5) Timing error

Timing errors of the CEC reception signal are checked during initiator or follower operation. A timing error occurs if the CEC reception signal is outside the range of the compare register set. As shown in Figure 37.40, low-level width timing errors are detected when the rising edge is detected. Timing errors for the minimum bit width are detected when the falling edge is detected, and timing errors for the maximum bit width are detected if there is no falling edge even though the maximum bit width has exceeded. Whether to check the ACK bit timing can be selected using the CECCTL0.ACKTEN bit. However, even if CECCTL0.ACKTEN is set to 1, the maximum bit width is not checked only for the ACK bit of the last data block (when CECCTL0.EOM = 1). The minimum bit width is checked. As shown in Figure 37.41, if a timing error with a short bit width is detected during follower operation, a low-level pulse (error handling pulse) that has a bit width 1.5 times the bit width specified using the NOMP register is transmitted.

An error handling pulse is not transmitted if a start bit timing error is detected.

If a timing error other than one that has a short bit width is detected during initiator operation, transmission immediately stops. During follower operation, reception continues as shown in Figure 37.42, and logical 1 is transmitted during direct address communication and logical 0 is transmitted during broadcast communication at the ACK bit timing. The generation of a communication complete interrupt (INTCE) depends on the set values of CECCTL1.CESEL[1:0]. If a timing error for the minimum bit width of the last ACK bit is detected, a communication complete interrupt (INTCE) is output at the same time as an error interrupt (INTERR).

通过设置发送开始触发(CECCTL0.TXTRG)进行仲裁检查

在设置发送开始触发(CECCTL0.TXTRG)后经过两个CEC时钟周期后执行仲裁检查。如果确定仲裁丢失，则产生错误中断(INTERR)，设置仲裁丢失检测标志(CECES.AERR)，并将模式切换到接收模式。

起始位输出周期

如果在设置发送开始触发(CECCTL0.TXTRG)并且实际输出开始位时在接收线检测到低电平，则设置仲裁丢失检测标志(CECES.AERR)并且模式切换到接收模式。如果检测到接收线的上升沿超过了STATLH设置的起始位的最大低电平宽度，则设置仲裁丢失检测标志(CECES.AERR)并且模式切换到接收模式。

发起者地址输出周期

发送完起始位后，在发送起始地址的同时进行逻辑校验。如果检测到比本地地址更早的地址，则会产生错误中断(INTERR)，设置仲裁丢失检测标志(CECES.AERR)，并将模式切换到接收模式。

(5) 时间错误

在发起者或从者操作期间检查CEC接收信号的定时错误。如果CEC接收信号超出比较寄存器组的范围，则会发生时序错误。如图37.40所示，检测到上升沿时检测到低电平宽度时序错误。当检测到下降沿时，检测到最小位宽的时序错误，如果没有下降沿，即使超过了最大位宽，也会检测到最大位宽的时序错误。可以使用CECCTL0.ACKTEN位选择是否检查ACK位时序。但是，即使CECCTL0.ACKTEN设置为1，也不会仅检查最后一个数据块的ACK位的最大位宽（当CECCTL0.EOM=1时）。检查最小位宽。如图37.41所示，如果在跟随器操作期间检测到位宽较短的时序错误，则会发送位宽为使用NOMP寄存器指定的位宽的1.5倍的低电平脉冲（错误处理脉冲）。

如果检测到起始位定时错误，则不发送错误处理脉冲。

如果在启动器操作期间检测到除具有短位宽度的定时错误之外的定时错误，则传输立即停止。在跟随器操作期间，接收继续如图37.42所示，在直接地址通信期间发送逻辑1，在ACK位定时在广播通信期间发送逻辑0。通信完成中断(INTCE)的产生取决于CECCTL1.CESEL[1:0]的设置值。如果检测到最后一个ACK 位的最小位宽度的时序错误，则在错误中断(INTERR)的同时输出通信完成中断(INTCE)。

RA生态工作室

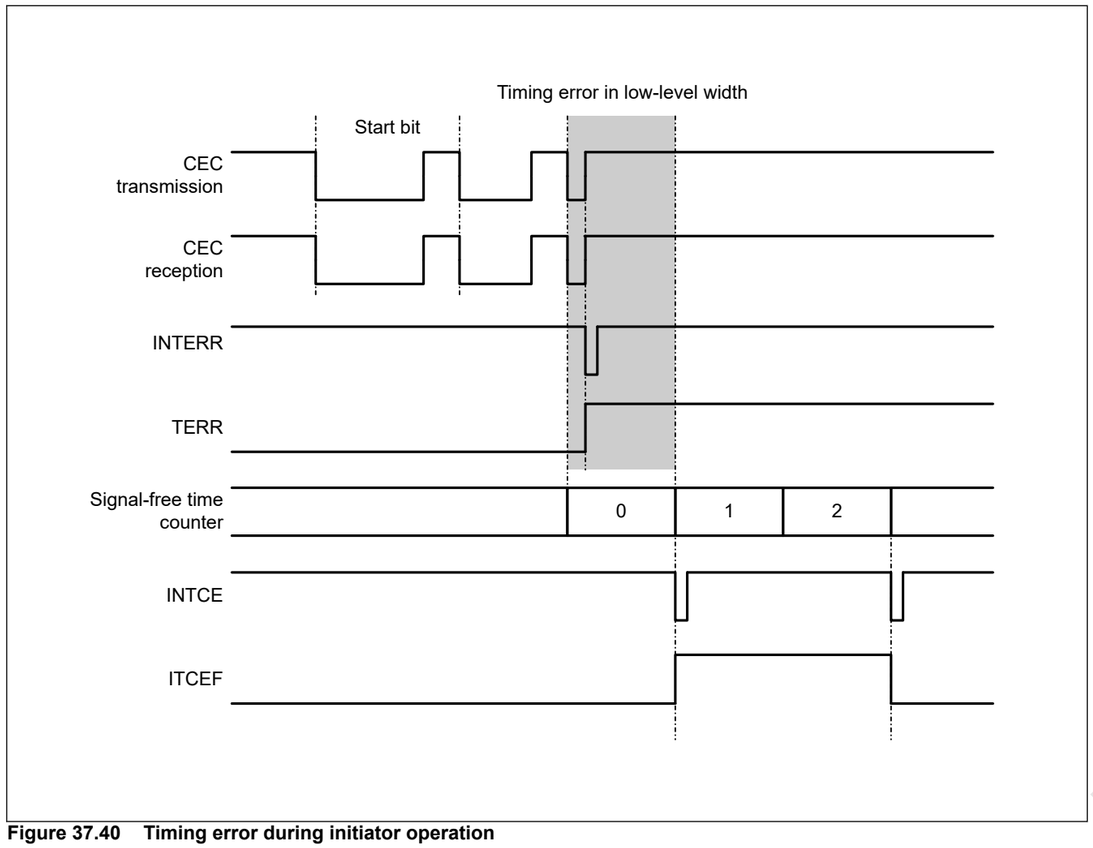


Figure 37.40 Timing error during initiator operation

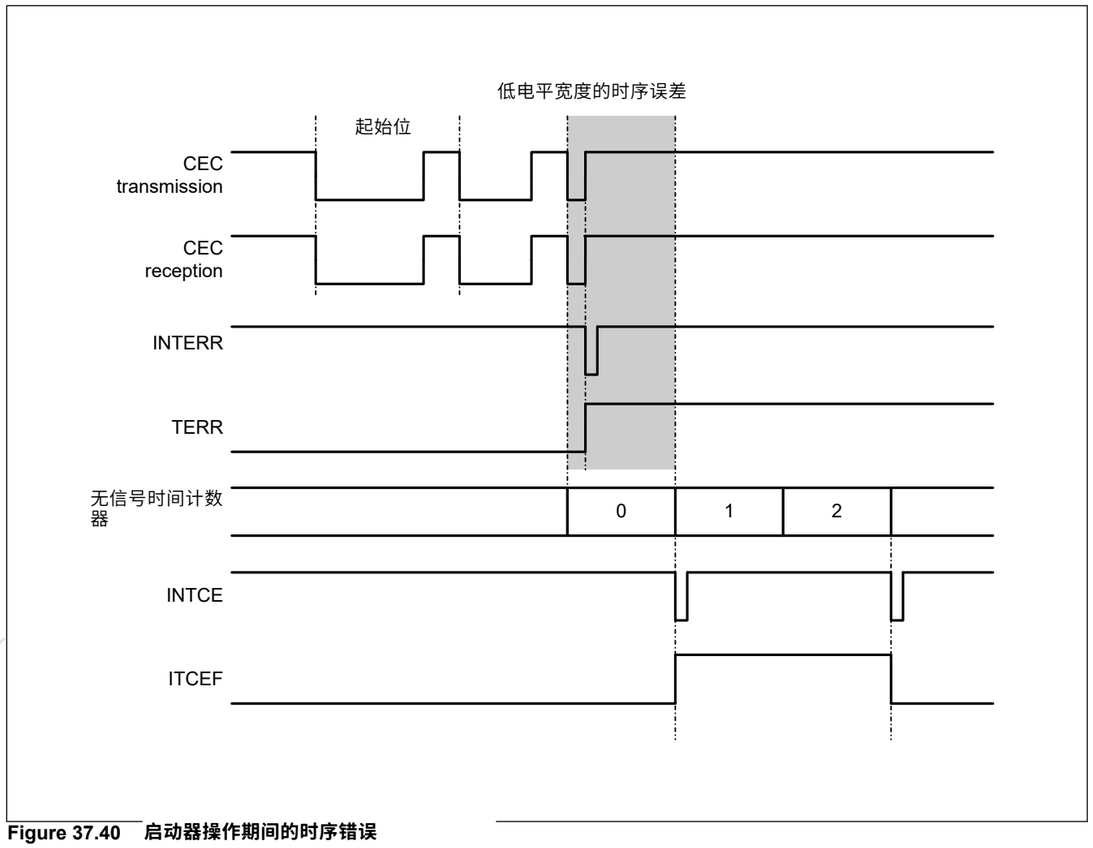


Figure 37.40 启动器操作期间的时序错误

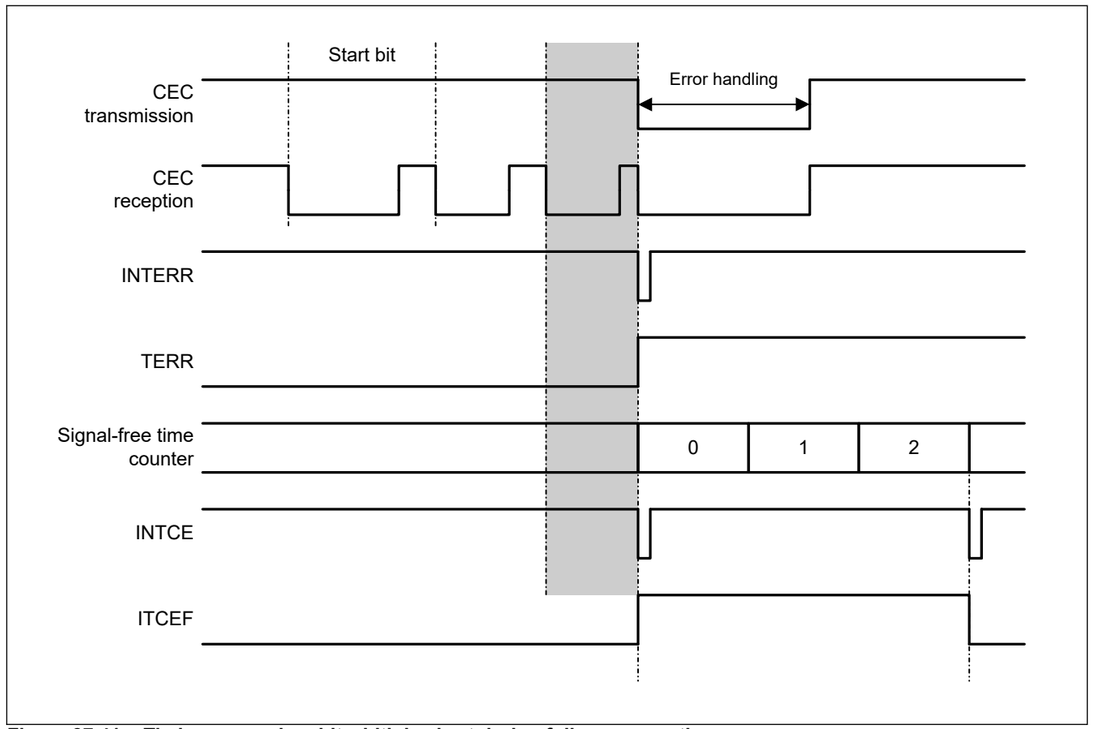


Figure 37.41 Timing error when bit width is short during follower operation

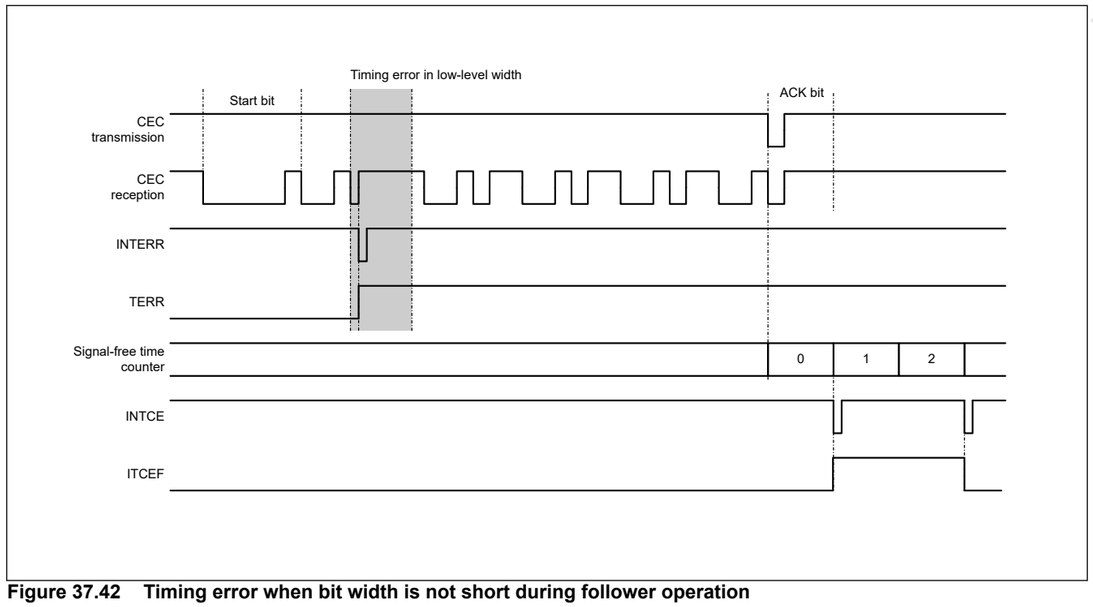


Figure 37.42 Timing error when bit width is not short during follower operation

(6) Overrun error

If receiving the next data is complete before reading data from the Reception Buffer Register (CRXD) during follower operation, an overrun error occurs. As shown in Figure 37.43, an error interrupt (INTERR) is generated, and the Overrun

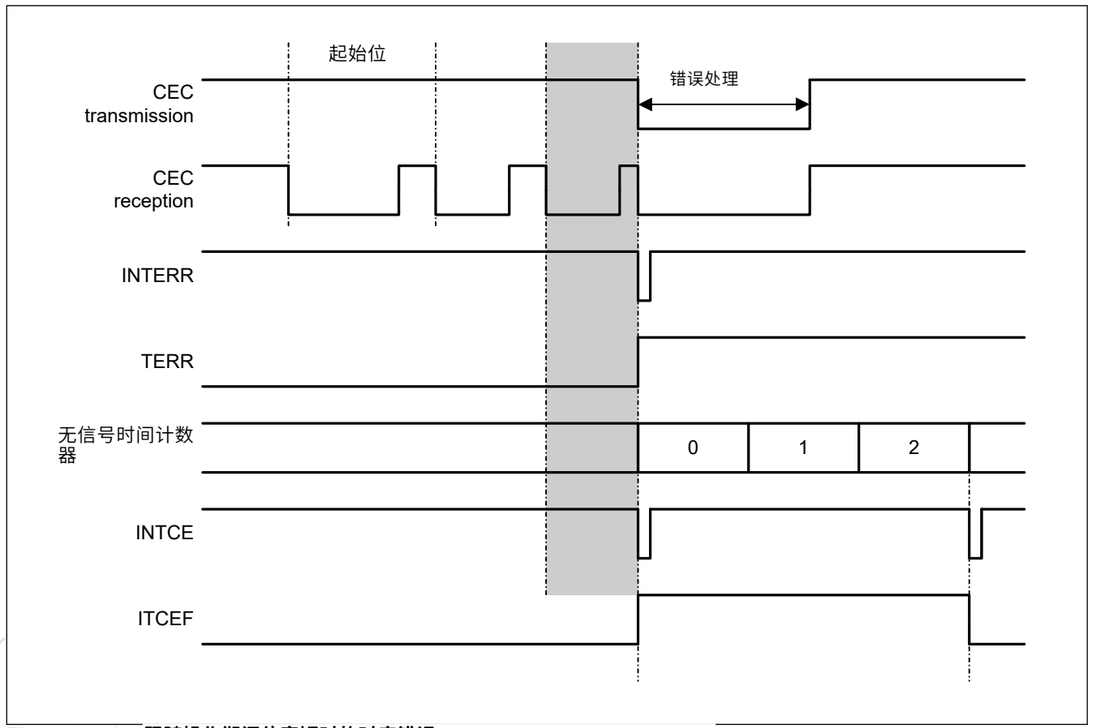


Figure 37.41 跟随操作期间位宽短时的时序错误

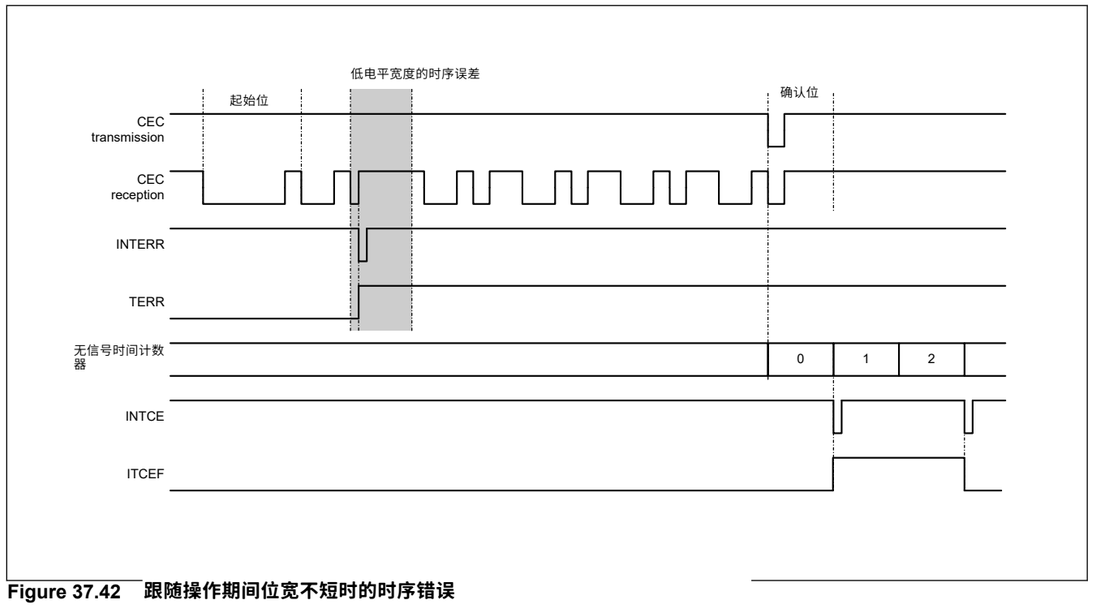


Figure 37.42 跟随操作期间位宽不短时的时序错误

(6) 溢出错误

如果在跟随器操作期间从接收缓冲寄存器(CRXD)读取数据之前完成接收下一个数据，则会发生溢出错误。如图37.43所示，产生错误中断（INTERR），Overrun

Error Detection Flag (CECES.OERR) is set. Afterward, logical 1 is returned during direct address communication and logical 0 is returned during broadcast communication at the ACK transmission timing of the block in which an overrun error occurred. The failure of reception is reported to the initiator, and reception standby state is entered. A communication complete interrupt (INTCE) operates according to the setting of the CECCTL1.CESEL[1:0] bits.

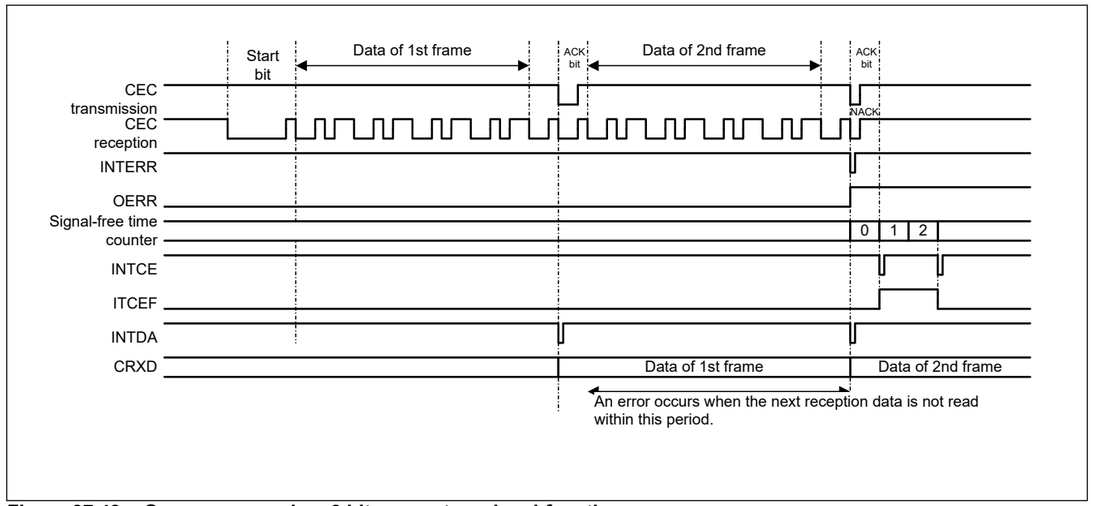


Figure 37.43 Overrun error when 3 bits are set as signal-free time

(7) Bus lock error

When bus lock errors are set to be detected (CECCTL1.BLERRD = 1), a bus lock error occurs if the bus is in the communication status (CECS.BUSST = 1) and the CEC reception signal stays high or low for a period corresponding to 2.5 times the data bit width specified by using the NOMP register. Figure 37.44 shows the timing of bus lock error detection.

If an error is detected, an error interrupt (INTERR) is generated, the Bus Lock Error Detection Flag (CECES.BLERR) is set, communication standby state is entered, and the signal-free time is counted. A communication complete interrupt (INTCE) operates according to the setting of the CECCTL1.CESEL[1:0] bits. Bus lock errors are detected only for the follower.

When bus lock errors are not set to be detected (CECCTL1.BLERRD = 0), no bus lock error is detected. To determine whether the bus is locked, monitor the CECEXMON.CECLNMON bit, and use software to determine and handle bus locking.

错误检测标志(CECES.OERR)被设置。之后，在发生溢出错误的块的ACK发送定时，在直接地址通信期间返回逻辑1，在广播通信期间返回逻辑0。接收失败上报给发起方，进入接收待机状态。通信完成中断(INTCE)根据CECCTL1.CESEL[1:0]位的设置进行操作。

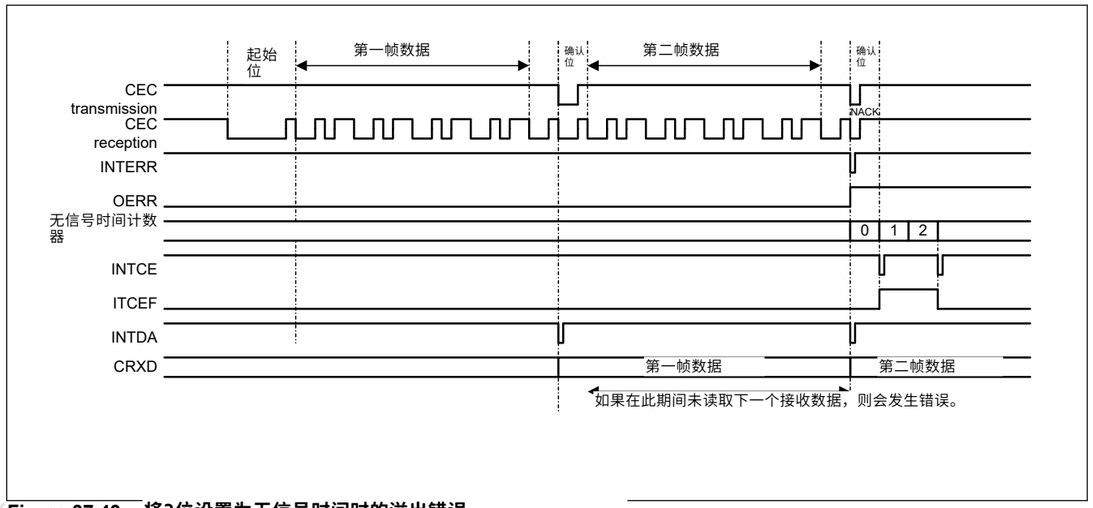


Figure 37.43 将3位设置为无信号时间时的溢出错误

(7) 总线锁定错误

当总线锁定错误设置为检测时（CECCTL1.BLERRD=1），如果总线处于通信状态（CECS.BUSST=1）并且CEC接收信号保持高电平或低电平相应的周期，则发生总线锁定错误到使用NOMP寄存器指定的数据位宽度的2.5倍。图37.44显示了总线锁定错误检测的时序。

如果检测到错误，则产生错误中断(INTERR)，设置总线锁定错误检测标志(CECES.BLERR)，进入通信待机状态，并计算无信号时间。通信完成中断(INTCE)根据CECCTL1.CESEL[1:0]位的设置进行操作。仅对从站检测总线锁定错误。

当未设置检测总线锁定错误时（CECCTL1.BLERRD=0），不会检测到总线锁定错误。要确定总线是否被锁定，请监视CECEXMON.CECLNMON位，并使用软件来确定和处理总线锁定。

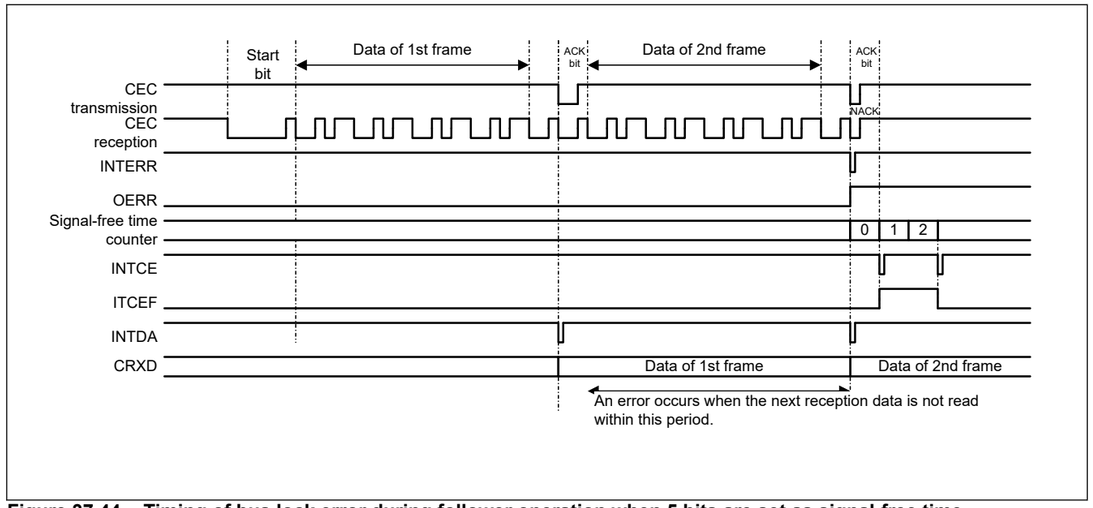


Figure 37.44 Timing of bus lock error during follower operation when 5 bits are set as signal-free time

37.3.3.7.2 Clearing Error Flag

An error flag set to the CEC Communication Error Status Register (CECES) can be cleared by setting 1 to the corresponding bit in the CEC Communication Error Flag Clear Trigger Register (CECFC). Figure 37.45 shows an example when an arbitration error occurs. An Arbitration Loss Detection Flag can be cleared by setting 0x20 to the CECFC register.

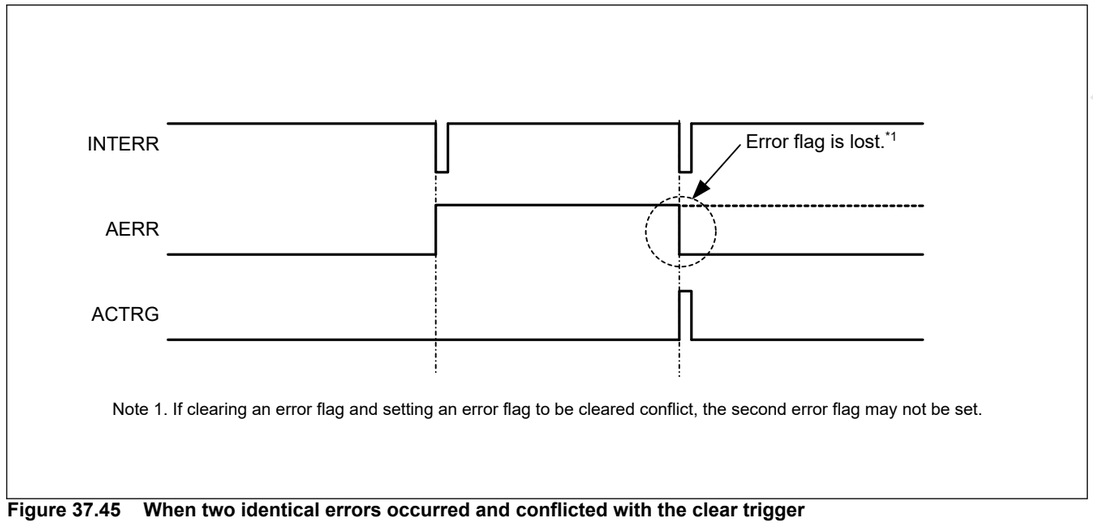


Figure 37.45 When two identical errors occurred and conflicted with the clear trigger

37.3.3.8 Signal-Free Time

The end of the signal-free time is reported by generating a communication complete interrupt by detecting a match with the specified time (3, 5, or 7 bits of the bit width specified using the NOMP register). The number of bits of the signal-free time is specified using the CECCTL1.SFT[1:0] bits. A communication complete interrupt is generated by setting up the CECCTL1.CESEL[1:0] bits. Counting the signal-free time always starts when the falling edge of the received data is detected. During normal communication, counting the signal-free time starts after the falling edge of the ACK bit is detected, if CECCTL0.EOM = 1.

Even if an error occurs, counting the signal-free time is started after communication is stopped.

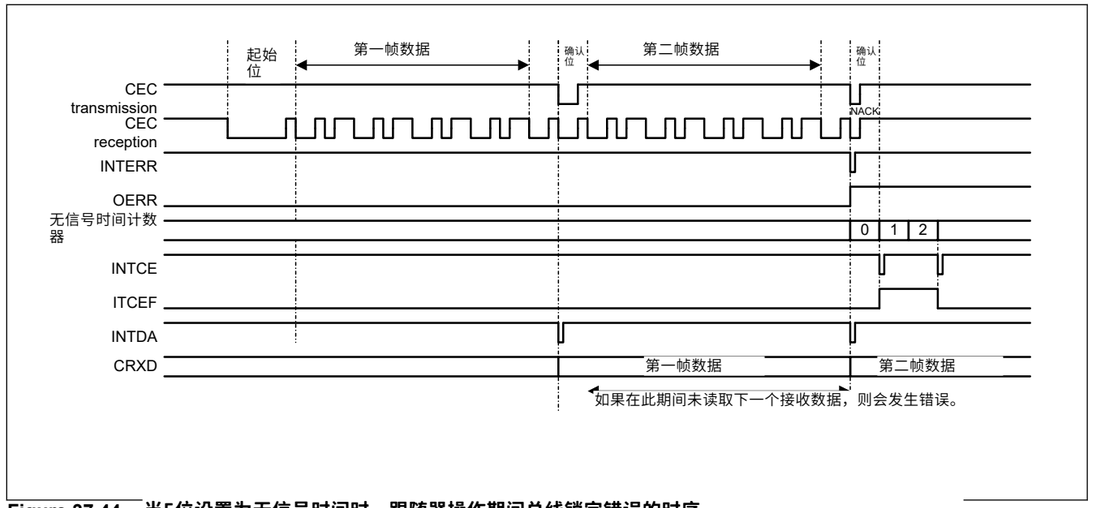


Figure 37.44 当5位设置为无信号时间时，跟随器操作期间总线锁定错误的时序

37.3.3.7.2 清除错误标志

通过将CEC通信错误标志清除触发寄存器(CECFC)中的相应位设置为1，可以清除设置到CEC通信错误状态寄存器(CECES)的错误标志。图37.45显示了发生仲裁错误时的示例。可以通过将CECFC寄存器设置为0x20来清除仲裁丢失检测标志。

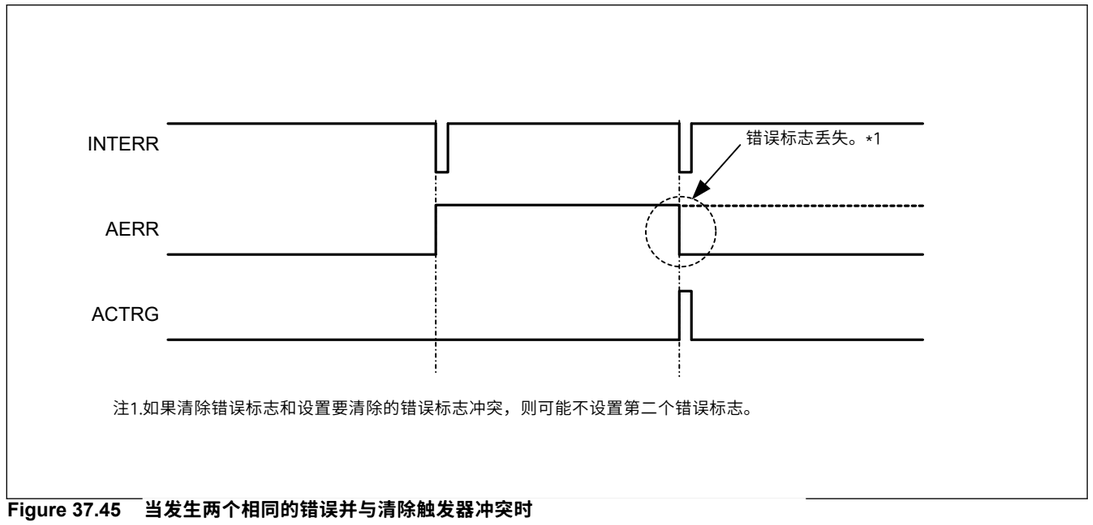


Figure 37.45 当发生两个相同的错误并与清除触发器冲突时

37.3.3.8 Signal-Free Time

通过检测与指定时间（使用NOMP寄存器指定的位宽的3、5或7位）匹配产生通信完成中断来报告无信号时间的结束。无信号时间的位数由CECCTL1.SFT[1:0]位指定。通过设置CECCTL1.CESEL[1:0]位产生通信完成中断。始终在检测到接收数据的下降沿时开始计算无信号时间。在正常通信期间，如果CECCTL0.EOM=1，则在检测到ACK位的下降沿后开始计算无信号时间。

即使发生错误，也会在通信停止后开始计算无信号时间。

If an error handling pulse (a low-level pulse that has a bit width of 1.5 times the bit width) is acknowledged, the signal-free time is counted starting at the falling edge of the error handling pulse signal. Figure 37.46 shows an operation example in which the detection of a 7-data bit width signal-free time when CECCTL1.CESEL[1:0] = 00b and CECCTL1.SFT[1:0] = 10b.

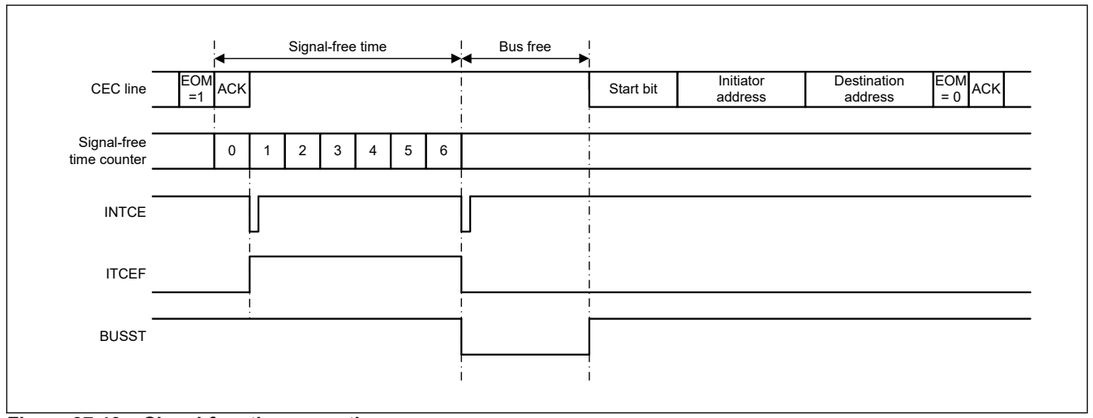


Figure 37.46 Signal-free time operation

Rewriting the values of the CECCTL1.SFT[1:0] bits to the number of bits smaller than the current number of bits while counting the signal-free time must be completed until the rewritten bit count values match. If rewriting is not performed in time, the counter overflows and the signal-free time period continues until the number of bits match again. Figure 37.47 shows an example when the data bit width is changed from 5 to 3 bits.

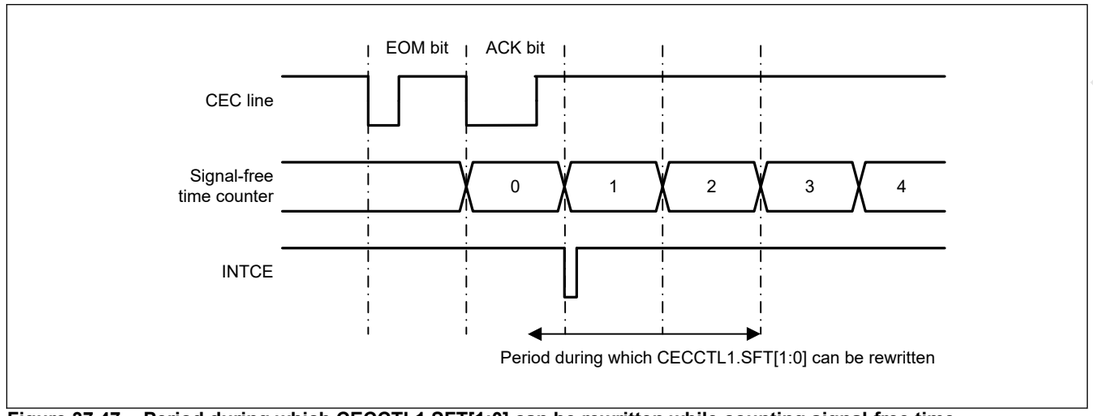


Figure 37.47 Period during which CECCTL1.SFT[1:0] can be rewritten while counting signal-free time

Starting receive operation during signal-free time

If a falling edge of the CEC reception signal is detected while counting the signal-free time, a receive operation is started as shown in Figure 37.48. A communication complete interrupt (INTCE) is not output even if the output of INTCE after counting the signal-free time is set, because the count operation of the signal-free time counter is stopped at this time.

如果确认了错误处理脉冲（位宽为位宽1.5倍的低电平脉冲），则从错误处理脉冲信号的下降沿开始计算无信号时间。图37.46显示了一个操作示例，其中当CECCTL1.CESEL[1:0]=00b和CECCTL1.SFT[1:0]=10b时，检测7个数据位宽的无信号时间。

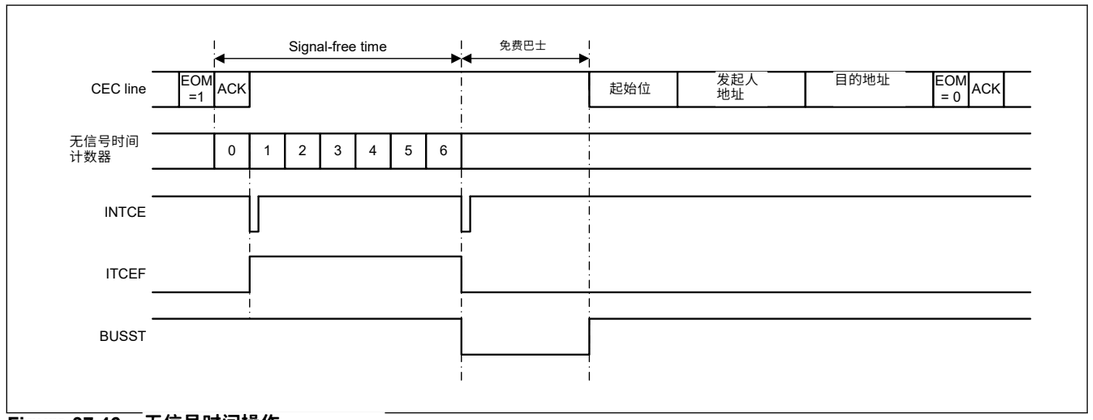


Figure 37.46 无信号时间操作

必须在计算无信号时间的同时将CECCTL1.SFT[1:0]位的值重写为小于当前位数的位数，直到重写的位计数值匹配为止。如果没有及时改写，计数器溢出，无信号时间周期一直持续，直到位数再次匹配。图37.47显示了数据位宽从5位更改为3位时的示例。

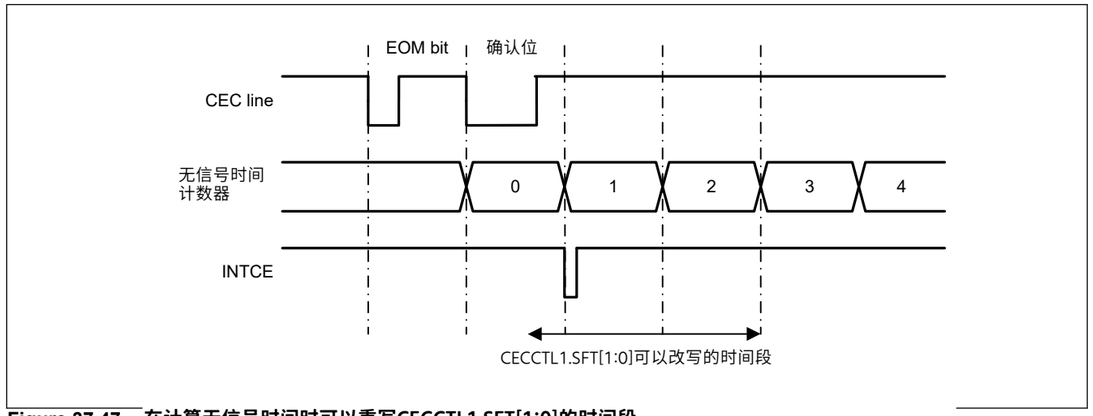


Figure 37.47 在计算无信号时间时可以重写CECCTL1.SFT[1:0]的时间段

在无信号时间开始接收操作

如果在计算无信号时间时检测到CEC接收信号的下降沿，则开始接收操作，如图37.48所示。即使在无信号时间计数后设置了INTCE的输出，也不会输出通信完成中断(INTCE)，因为此时无信号时间计数器的计数操作已停止。

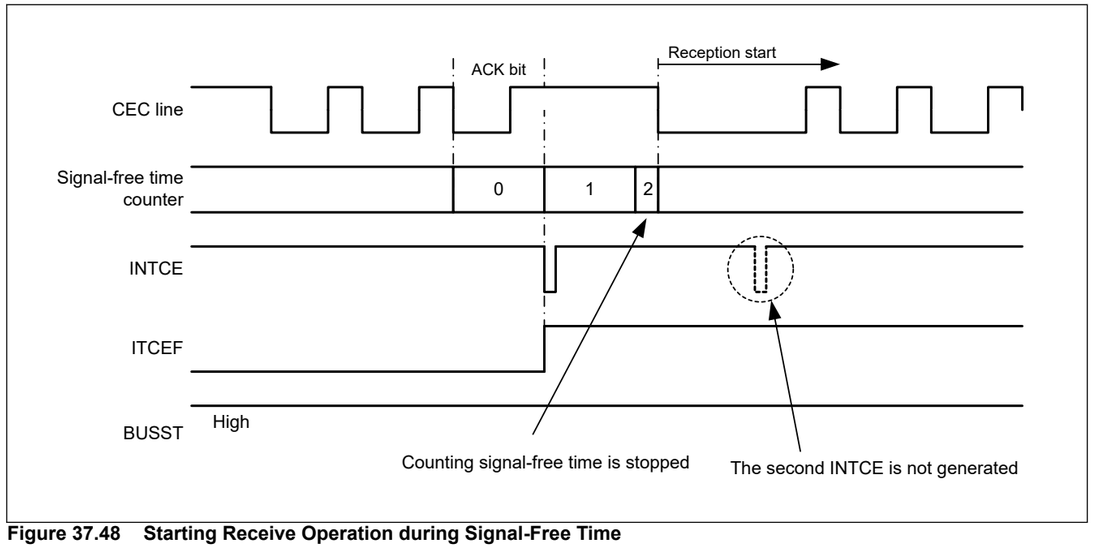


Figure 37.48 Starting Receive Operation during Signal-Free Time

37.3.3.9 Function that Restarts Reception by Detecting Start Bit during Reception

This function is used to restart reception starting from the detected start bit if a new start bit is detected during receive operation (follower operation), as shown in Figure 37.49. This function is enabled by enabling the Start Detection Restart Reception Enable Bit (CECEXMD.RERCVEN = 1).

A start bit is determined when received data matches the set value of the registers (STATLL, STATLH, STATBL, or STATBH) of the received start bit width, and reception is restarted.

Since the start bit is received during reception, a timing error occurs. An error occurs on the falling edge at the beginning of the start bit or at the header block.

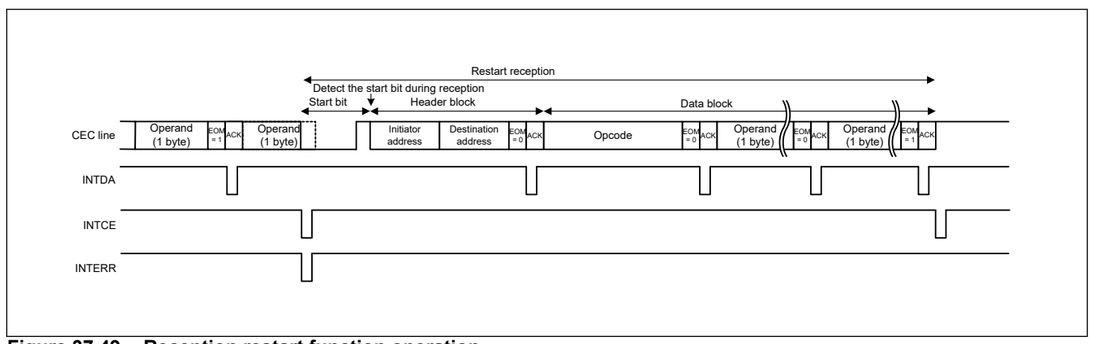


Figure 37.49 Reception restart function operation

37.4 Usage Notes

37.4.1 Recovery from low power consumption state

The CECIO terminal can be used as an IRQ input terminal. For the corresponding IRQ interrupt, if the interrupt request is enabled and the ICU IRQCRi.IRQMD[1:0] bits are set to 01b (falling edge) and the power consumption is changed to the low power consumption state, it recovers from the low power consumption state at the falling edge. Since the CEC operating clock is stopped in software standby mode, disable the start bit timing check. If MOSC is selected as the CEC

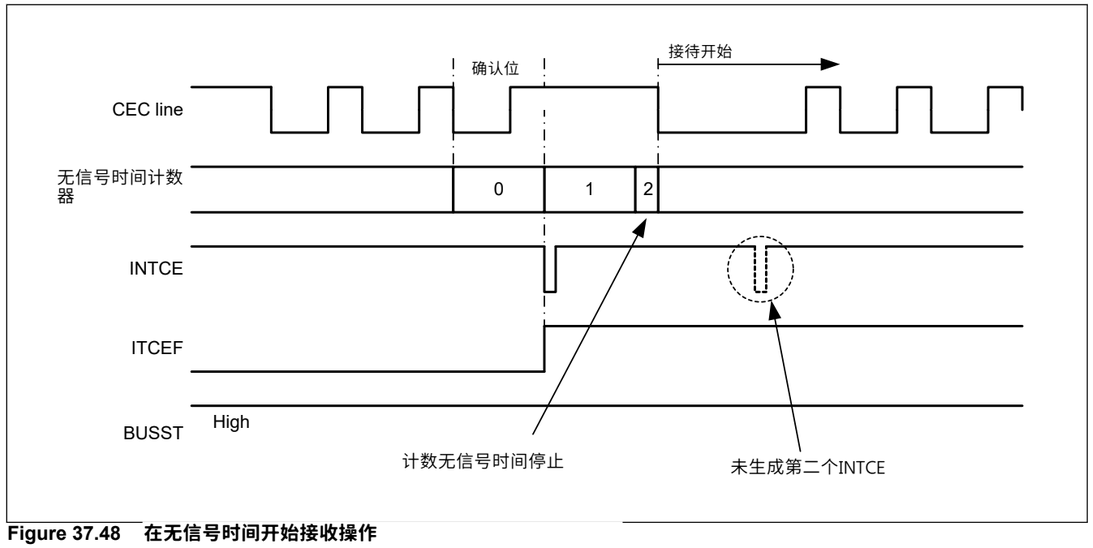


Figure 37.48 在无信号时间开始接收操作

37.3.3.9 通过在接收期间检测起始位来重新开始接收的功能

如果在接收操作（跟随操作）期间检测到新的起始位，则该功能用于从检测到的起始位重新开始接收，如图37.49所示。该功能通过启用启动检测重启接收使能位(CECEXMD.RERCVEN=1)来启用。

当接收到的数据与寄存器（STATLL、STATLH、STATBL或STATBH)的接收起始位宽度，并重新开始接收。

由于在接收过程中接收到起始位，因此会发生时序错误。错误发生在起始位开头或标题块的下降沿。

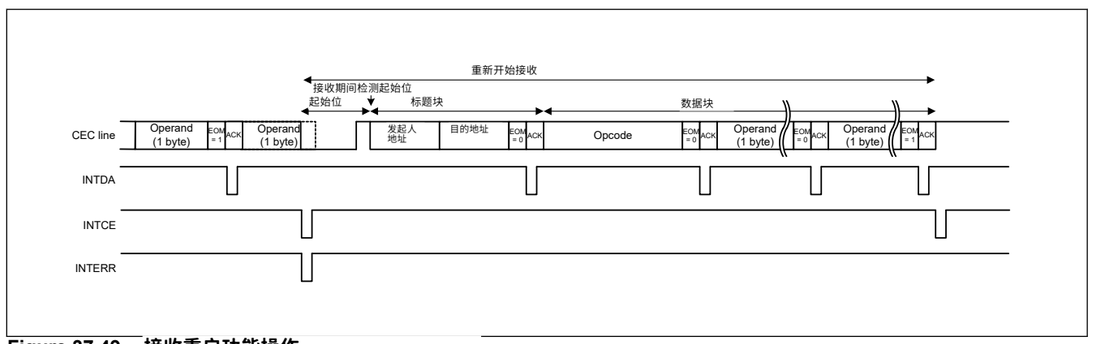


Figure 37.49 接收重启功能操作

37.4 使用说明

37.4.1 从低功耗状态恢复

CECIO终端可用作IRQ输入终端。对于相应的IRQ中断，如果中断请求使能，ICUIRQCRi.IRQMD[1:0]位设置为01b（下降沿）且功耗变为低功耗状态，则从低功耗状态恢复在下降沿的功耗状态。由于CEC工作时钟在软件待机模式下停止，因此禁用起始位时序检查。如果选择MOSC作为CEC

operating clock, adjust the setting value of the MOSCWTCR.MSTS bit so that the MOSC supply is restarted during the start bit L period.

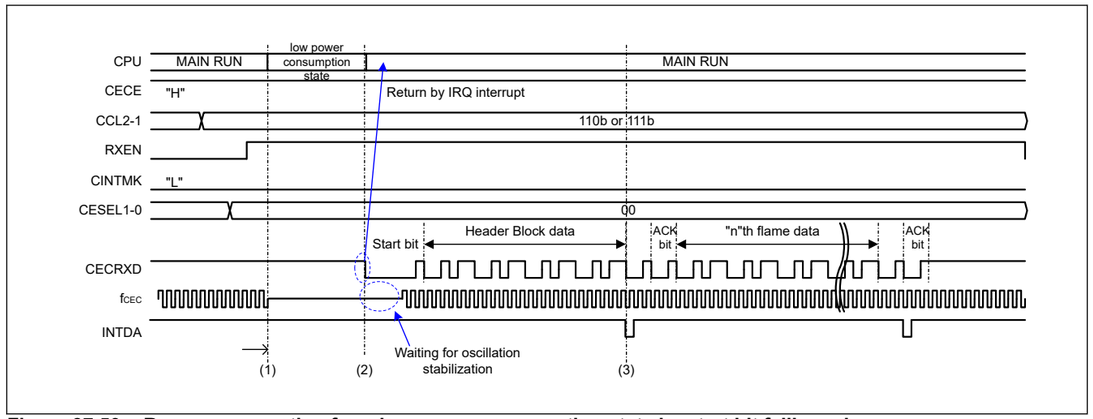


Figure 37.50 Recovery operation from low power consumption state by start bit falling edge

In the recovery operation from the low power consumption state by the start bit falling edge, even if data other than the own station address is received by direct address reception, it recovers from the low power consumption state.

When the CINTMK bit of CECCTL1 is set to 1, a CEC interrupt can be generated even when data other than the own station address is received. By checking the ADRF bit of CECS during data reception interrupt processing, it is possible to check whether the data was received to the local station address.

操作时钟，调整MOSCWTCR.MSTS位的设置值，使MOSC电源在起始位L期间重新启动。

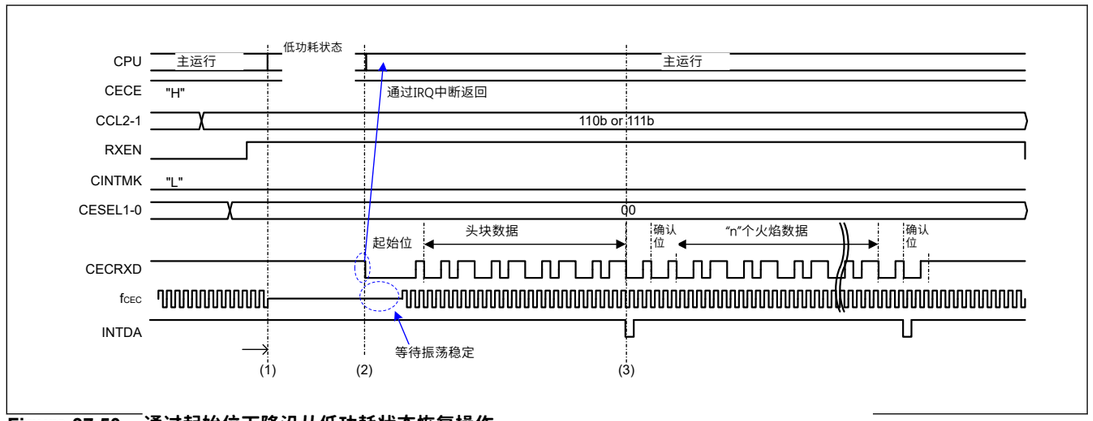


Figure 37.50 通过起始位下降沿从低功耗状态恢复操作

在起始位下降沿从低功耗状态恢复操作中，即使通过直接地址接收接收到本站地址以外的数据，它也会从低功耗状态恢复。

当CECCTL1的CINTMK位设置为1时，即使接收到本站地址以外的数据，也可以产生CEC中断。通过在数据接收中断处理期间检查CECS的ADRF位，可以检查数据是否接收到本地站地址。

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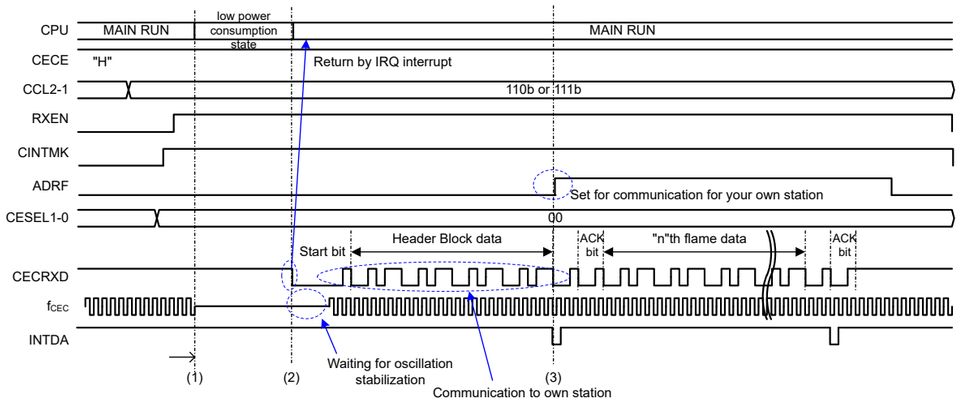
(1) When communication to own station



(2) When communication to other than own station

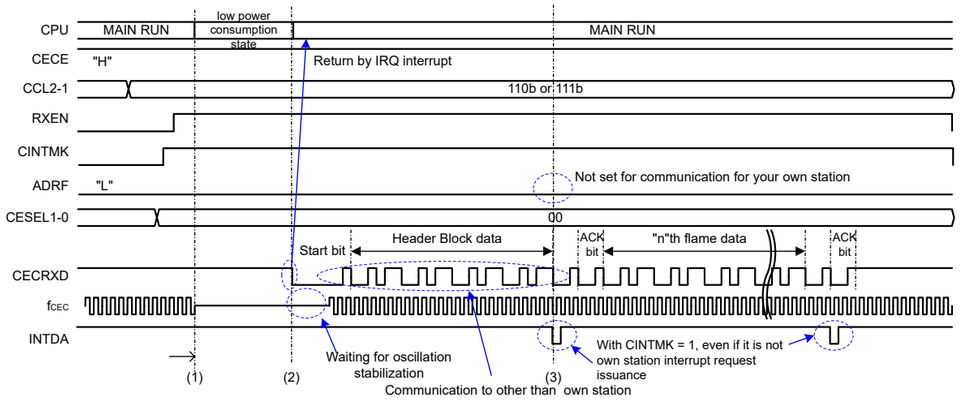


Figure 37.51 Recovery operation from low power consumption state by start bit falling edge (own station judgment)

37.4.2 Settings for Module-Stop Function

The Module Stop Control Register (MSTPCR) can enable or disable CEC operation. The CEC module is initially stopped after reset.

Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

37.4.3 Settings for Clock Division Ratio

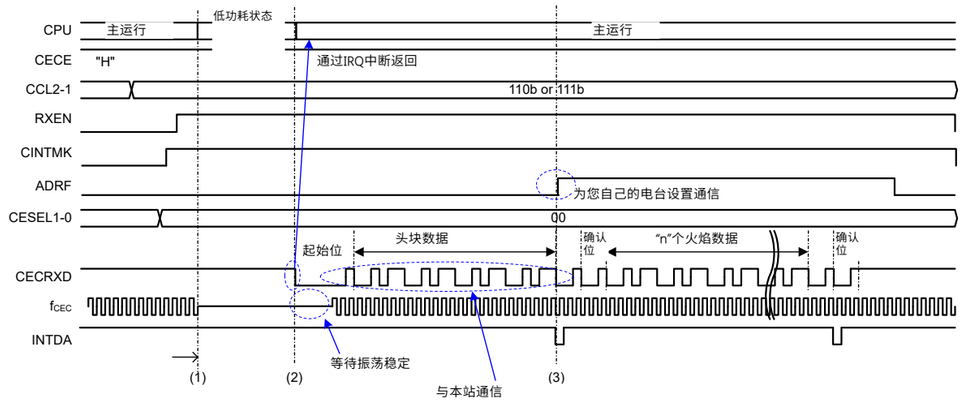
Set the peripheral module clock (PCLKB) frequency to higher than the CEC operating clock frequency.

37.4.4 Notes on re-reception function by detection of start bit during reception

37.4.4.1 Precautions for re-receive function by detecting start bit during reception

If a new start bit is detected during reception operation (follower operation), the CEC line may be fixed at Low, so please note the following notes.

(1)与本站通信时



(2)与本站以外的通信时

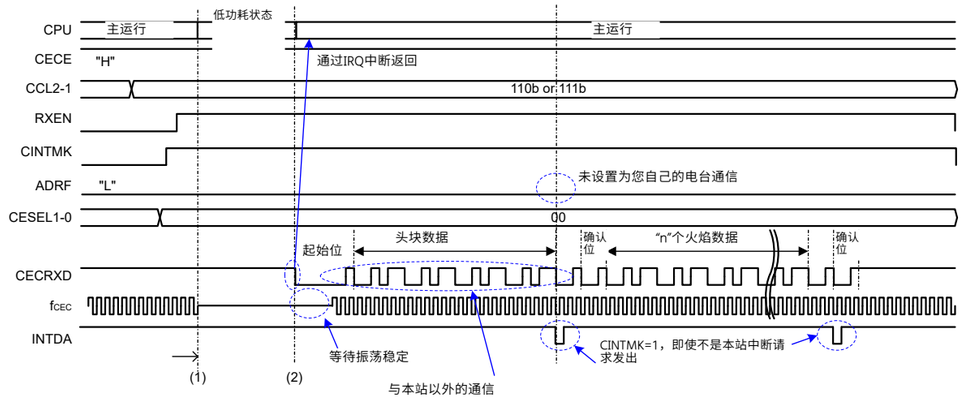


Figure 37.51 通过起始位下降沿从低功耗状态恢复操作（本站判断）

37.4.2 模块停止功能的设置

模块停止控制寄存器(MSTPCR)可以启用或禁用CEC操作。CEC模块在复位后最初停止。

释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

37.4.3 时钟分频比设置

将外围模块时钟(PCLKB)频率设置为高于CEC工作时钟频率。

37.4.4 接收期间通过检测起始位进行重新接收功能的注意事项

37.4.4.1 通过在接收期间检测起始位来重新接收功能的注意事项

如果在接收操作（跟随操作）期间检测到新的起始位，CEC线可能会固定为低电平，因此请注意以下注意事项。

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- To detect the high or low fixed (bus lock) state of the CEC line, set CECCTL1.BLERRD to 1 and enable the bus lock detection function.
- If the cause of the INTERR interrupt is a bus lock error (CECES.BLERR = 1), clear CECCTL0.CECE to 0 once in the INTERR interrupt processing, and initialize the internal sequencer of the CEC transmission/reception circuit. After that, set CECCTL0.CECE to 1 again. Even if CECCTL0.CECE is cleared to 0, the CEC register will not be reset. See Figure 37.52 for an example of the INTERR interrupt processing flow when a bus lock error occurs.

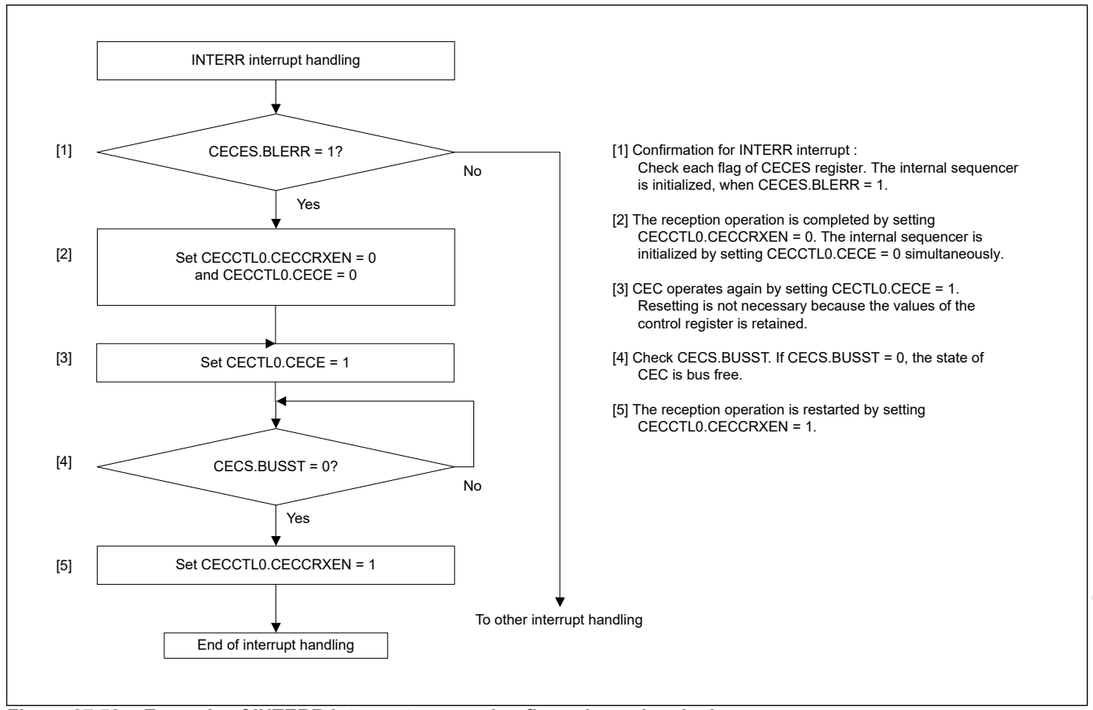

Figure 37.52 Example of INTERR interrupt processing flow when a bus lock error occurs

●要检测CEC线的高电平或低电平固定（总线锁定）状态，请将CECCTL1.BLERRD设置为1并启用总线锁定检测功能。

●如果INTERR中断的原因是总线锁定错误（CECES.BLERR=1），在INTERR中断处理中将CECCTL0.CECE清零一次，并初始化CEC发送接收电路的内部定序器。之后，再次将CECCTL0.CECE设置为1。即使CECCTL0.CECE被清零，CEC寄存器也不会被复位。发生总线锁定错误时的INTERR中断处理流程示例，请参见图37.52。

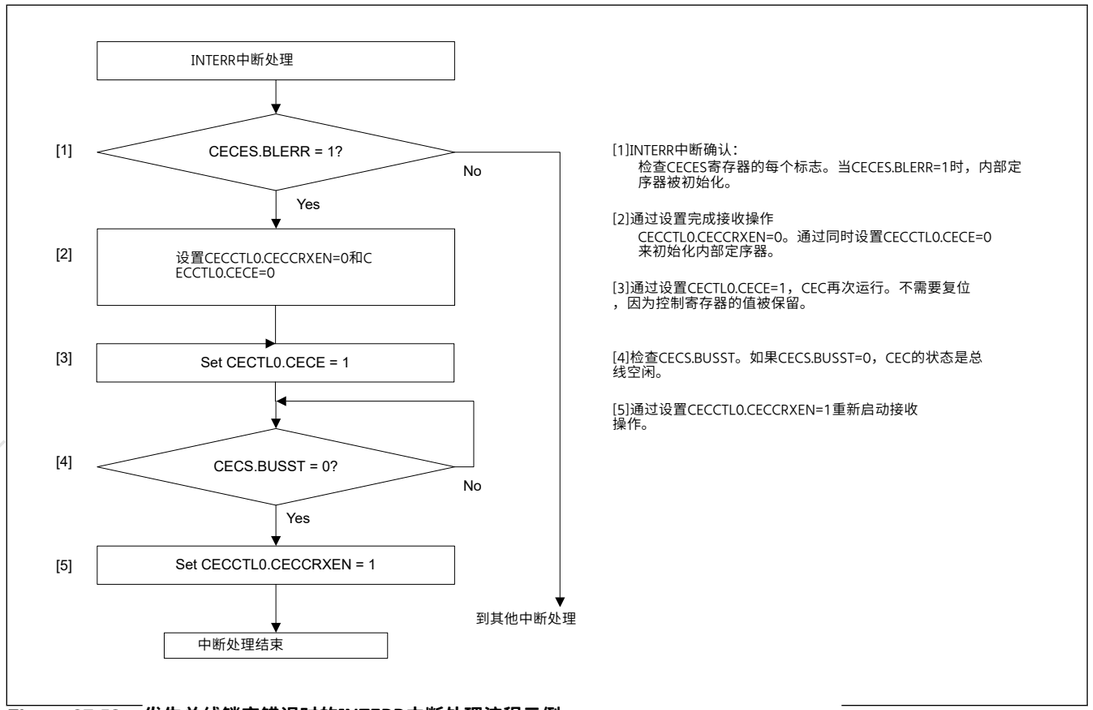

Figure 37.52 发生总线锁定错误时的INTERR中断处理流程示例

38. Serial Sound Interface Enhanced (SSIE)

38.1 Overview

The Serial Sound Interface Enhanced (SSIE) can transmit and receive audio data to and from various devices that support any of audio data formats, such as I^2S, monaural, and TDM.

38.2 Features

Table 38.1 Features of SSIE

Item		Description
Number of channels		One channel, SSIE0
Communication mode		• Master/slave • Transmission/reception (SSIE0 full duplex communication or half-duplex communication)
Communication format		• I^2S format • Monaural format • TDM format
Serial data		• MSB first • Data can be left-justified or right-justified. • Data delay (1 clock cycle) or no delay selectable for the period from SSILRCK/SSIFS to SSITXD0/SSIRXD0/SSIDATA0 • System word length: 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: 8, 16, 18, 20, 22, 24, or 32 bits • Padding polarity: Low or high
Bit clock (SSIBCK)	In master mode	• Two clock sources available (AUDIO_CLK/GPT output (GTIOC2A)) • Clock source division ratio: 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, and 1/128. • Supply/stop is selectable while communication is halted.
	In master/slave mode	• Polarity (rising edge or falling edge) selectable
LR clock/frame synchronization (SSILRCK/ SSIFS)	In master mode	• Polarity (low level or high level) selectable • Supply/stop is selectable while communication is halted.
Transmit data (SSITXD0/ SSIDATA0) and receive data (SSIRXD0/ SSIDATA0)	Transmission	• Muting method (transmission of transmit FIFO data or transmission of data fixed to 0) selectable
FIFO	Capacity	• Transmit FIFO/receive FIFO: 4 bytes × 32 stages
	Data alignment	• Data alignment method (left-justification or right-justification) selectable for the data transfer between FIFO and shift register
Interrupt	Interrupt output	• Communication error/idle mode • Receive data full • Transmit data empty
Low power consumption function		• Whether to supply the audio clock selectable in master mode
Module stop function	• Module stop state can be set to reduce power consumption.	
TrustZone Filter	• Security attribution can be set.	

The following table lists and defines the terms used for the communication formats SSIE can use:

Table 38.2 Definition of terms (1 of 2)

Term	Definition
Start trigger	First edge of the signal on the SSILRCK/SSIFS pin when the signal is set to the value specified in LRCKP to enable communication

38. 串行声音接口增强(SSIE)

38.1 Overview

增强型串行声音接口(SSIE)可以向各种支持任何音频数据格式（例如I2S、单声道和TDM）的设备发送和接收音频数据。

38.2 Features

Table 38.1 SSIE的特点

Item		Description
通道数		一个通道，SSIE0
通讯方式		• Master/slave • 发送接收（SSIE0全双工通信或半双工通信）
通讯格式		• I^2S format • Monaural format • TDM format
串行数据		• MSB first • 数据可以左对齐或右对齐。 • 从SSILRCKSSIFS到SSITXD0SSIRXD0SSIDATA0期间可选择数据延迟（1个时钟周期）或无延迟 • 系统字长：8、16、24、32、48、64、128或256位 • 数据字长：8、16、18、20、22、24或32位 • 填充极性：低或高
位时钟(SSIBCK)	在主模式	• 提供两个时钟源（AUDIO_CLKGPT输出(GTIOC2A)） • 时钟源分频比：11、12、14、16、18、112、116、124、132、148、164、196和1128。 • 通信停止时可选择停止供电。
	在主从模式	• 极性（上升沿或下降沿）可选
LR clock/frame synchronization (SSILRCK/ SSIFS)	在主模式	• 极性（低电平或高电平）可选 • 通信停止时可选择停止供电。
发送数据(SSITXD0SSIDATA0)和接收数据(SSIRXD0SSIDATA0)	Transmission	• 可选择静音方式（传送传送FIFO数据或传送固定为0的数据）
FIFO	Capacity	• 发送FIFO接收FIFO：4字节×32级
	数据对齐	• FIFO和移位寄存器之间的数据传输可选择数据对齐方式（左对齐或右对齐）
Interrupt	中断输出	• 通信错误空闲模式 • 接收数据已满 • 传输数据为空
低功耗功能		• 是否提供主模式下可选择的音频时钟
模块停止功能	• 可设置模块停止状态以降低功耗。	
TrustZone Filter	• 可以设置安全属性。	

下表列出并定义了用于SSIE可以使用的通信格式的术语：

Table 38.2 术语定义(1of2)

Term	Definition
启动触发器	当信号设置为LRCKP中指定的值以启用通信时，SSILRCKSSIFS引脚上的信号的第一个边沿

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Table 38.2 Definition of terms (2 of 2)

Term	Definition
Frame boundary	Point where SSIE starts transferring the first data of a frame or the point where SSIE ends transferring the last data of the frame
Frame word number	Number of sound channels per frame
System word length	Number of bits per channel
Data word length	Number of significant bits per channel
Control bits for communication formats	• SSICR register: FRM, DWL, SWL, LRCKP, SPDP, SDTA, PDTA, and DEL bits • SSIFCR register: BSW bit • SSIOFR register: OMOD bit • SSISCR register: TDES[4:0] and RDFS[4:0] bits

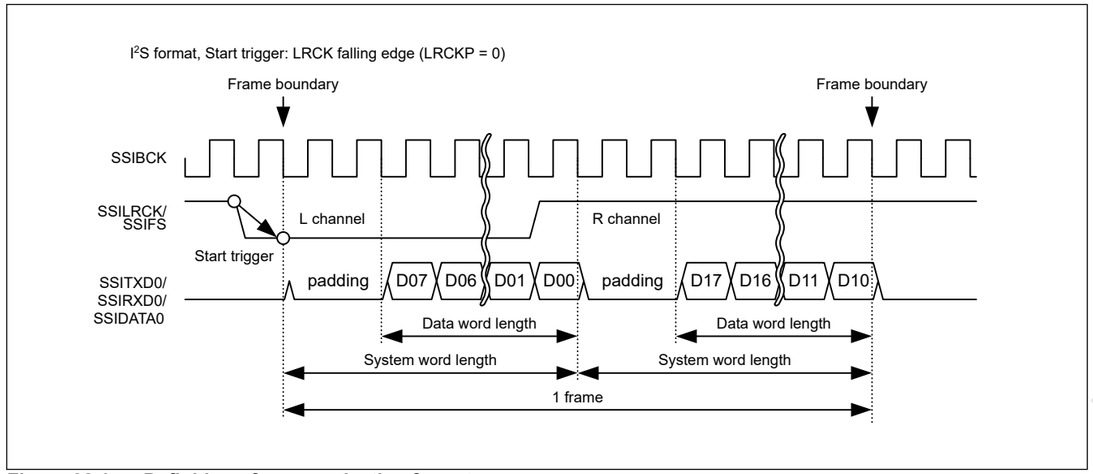


Figure 38.1 Definition of communication format

38.3 Block Diagram

Figure 38.2 shows a block diagram of SSIE.

Table 38.2 术语定义(2of2)

Term	Definition
框架边界	SSIE开始传输帧的第一个数据的点或SSIE结束传输帧的最后一个数据的点
帧字数	每帧声道数
系统字长	每个通道的位数
数据字长	每个通道的有效位数
通信格式的控制位	• SSICR寄存器：FRM、DWL、SWL、LRCKP、SPDP、SDTA、PDTA和DEL位 • SSIFCR register: BSW bit • SSIOFR register: OMOD bit • SISSCR寄存器：TDES[4:0]和RDFS[4:0]位

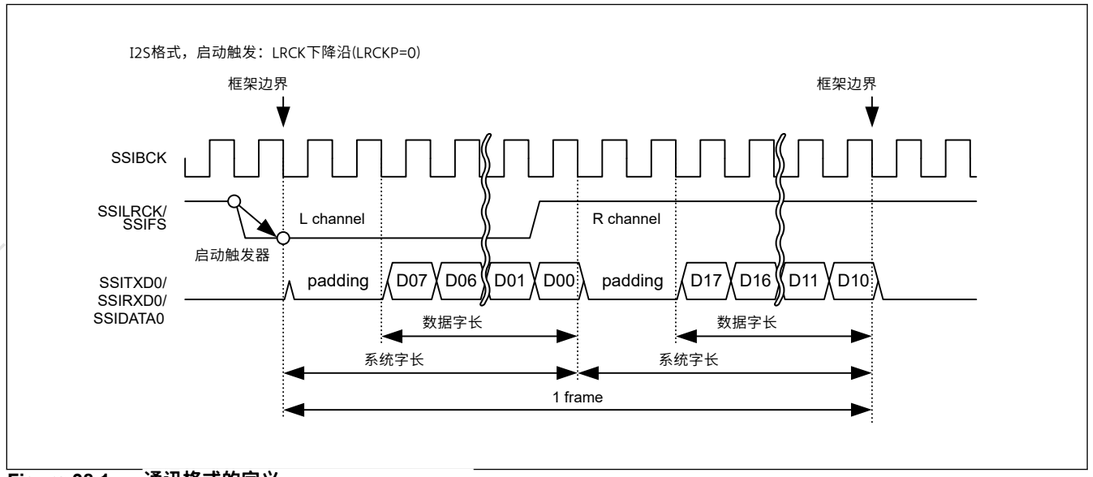
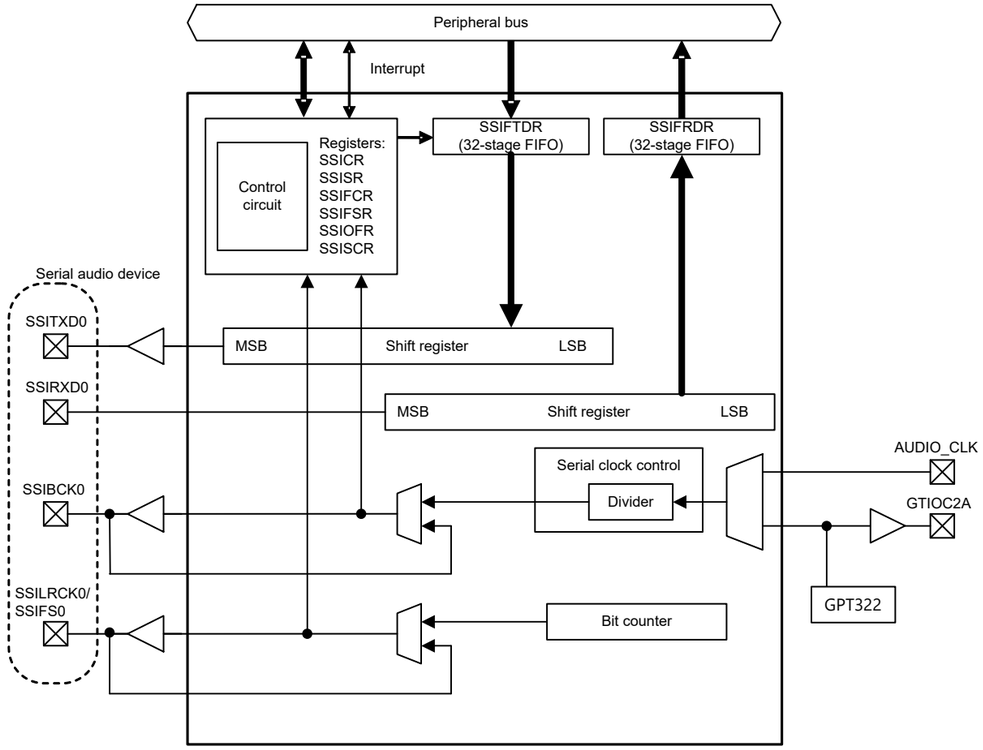


Figure 38.1 通讯格式的定义

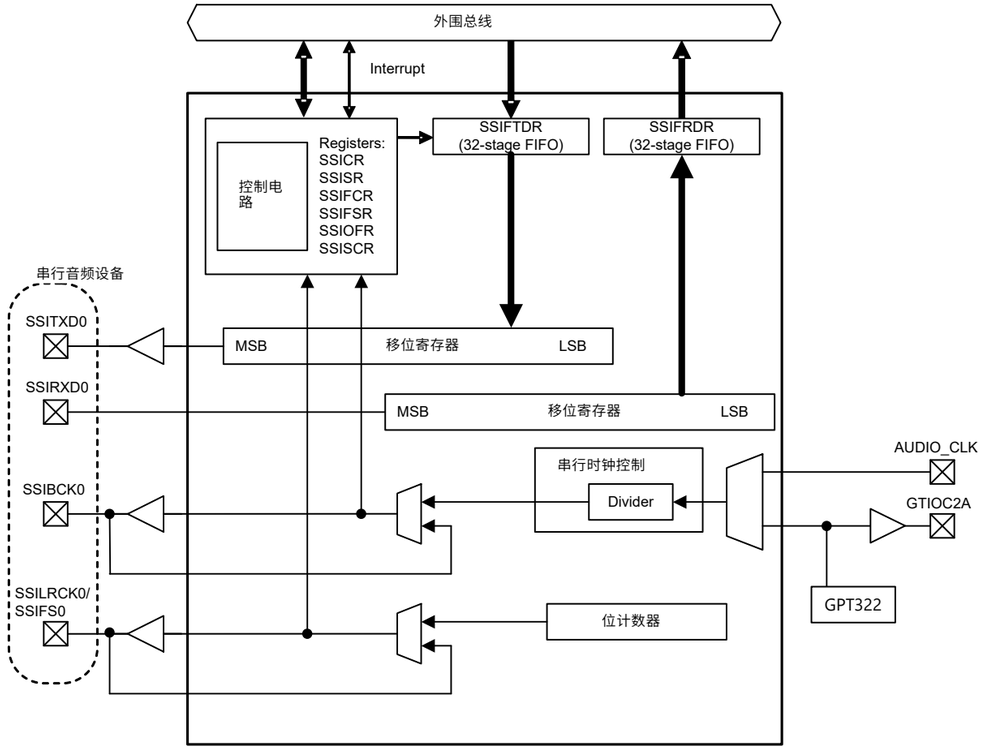
38.3 框图

图38.2显示了SSIE的框图。



[Legend]
SSICR: Control register
SSISR: Status register
SSIFCR: FIFO control register
SSIFSR: FIFO status register
SSIOFR: Audio format register
SSIFTDR: Transmit FIFO data register
SSIFRDR: Receive FIFO data register
SSISCR: Status control register

Figure 38.2 SSIE block diagram for full-duplex communication



[Legend]
SSICR: 控制寄存器
SSISR: 状态寄存器
SSIFCR: 先进先出控制寄存器
SSIFSR: 先进先出状态寄存器
SSIOFR: 音频格式寄存器
SSIFTDR：发送FIFO数据寄存器SSIFRDR
：接收FIFO数据寄存器
SSISCR: 状态控制寄存器

Figure 38.2 全双工通信的SSIE框图

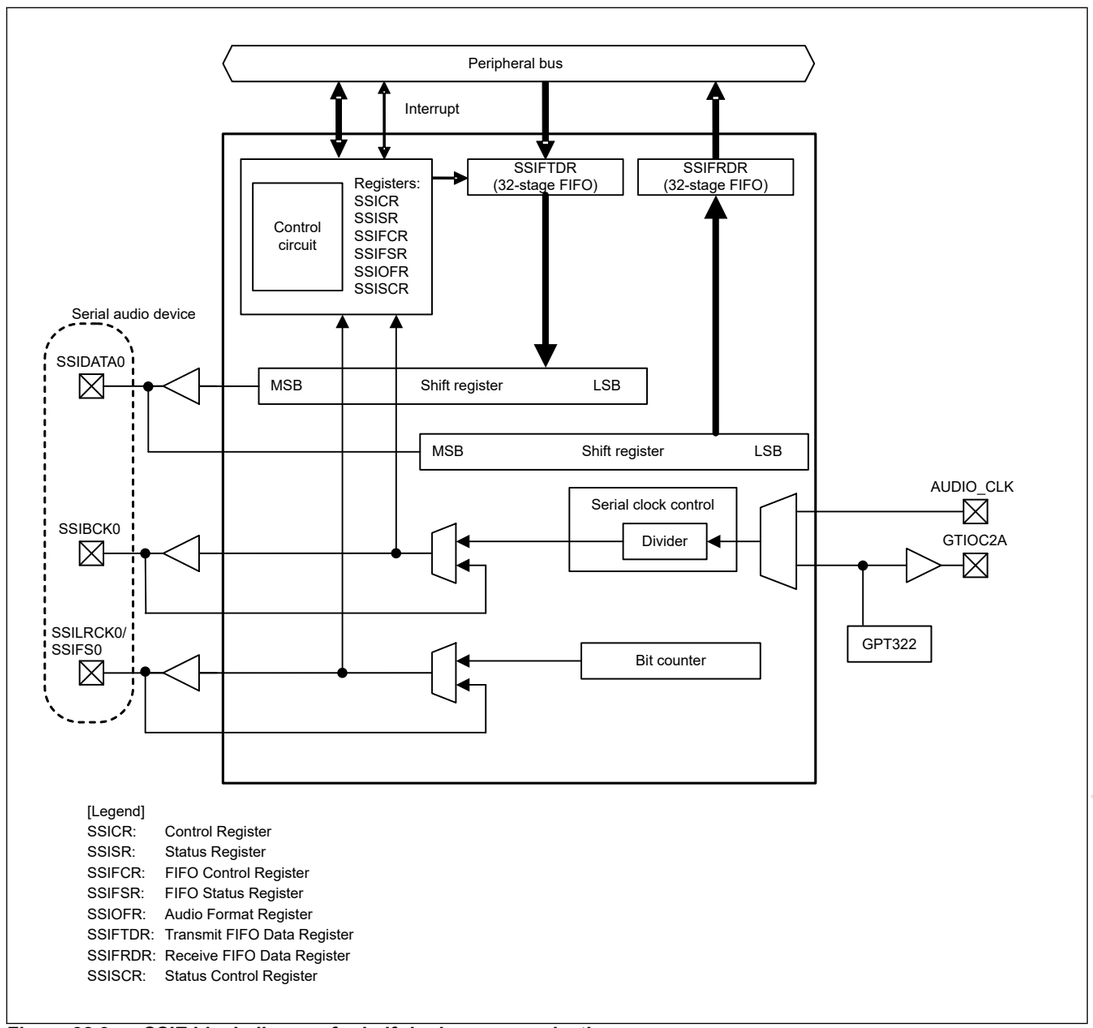


Figure 38.3 SSIE block diagram for half-duplex communication

Figure 38.4 shows the clock configuration of SSIE.

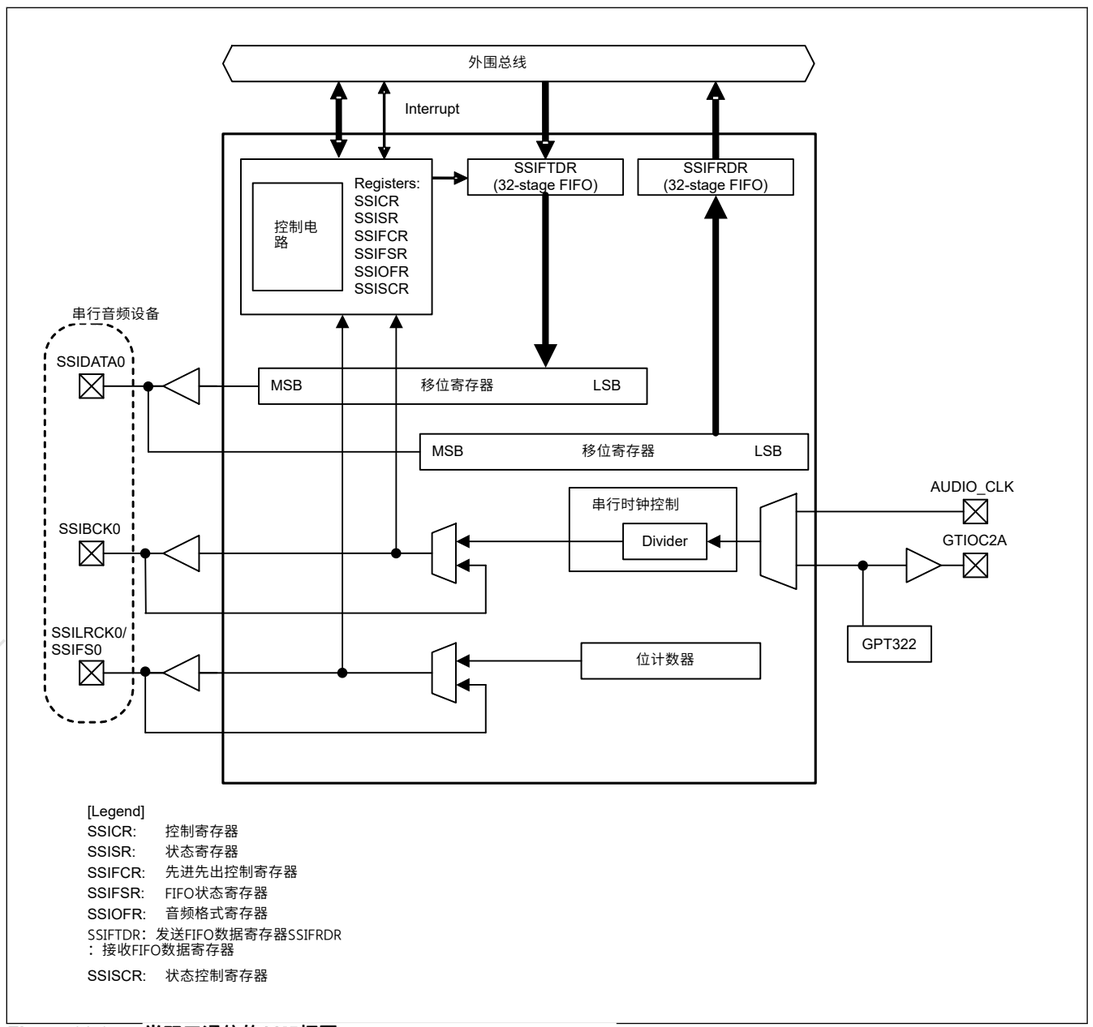


Figure 38.3 半双工通信的SSIE框图

图38.4显示了SSIE的时钟配置。

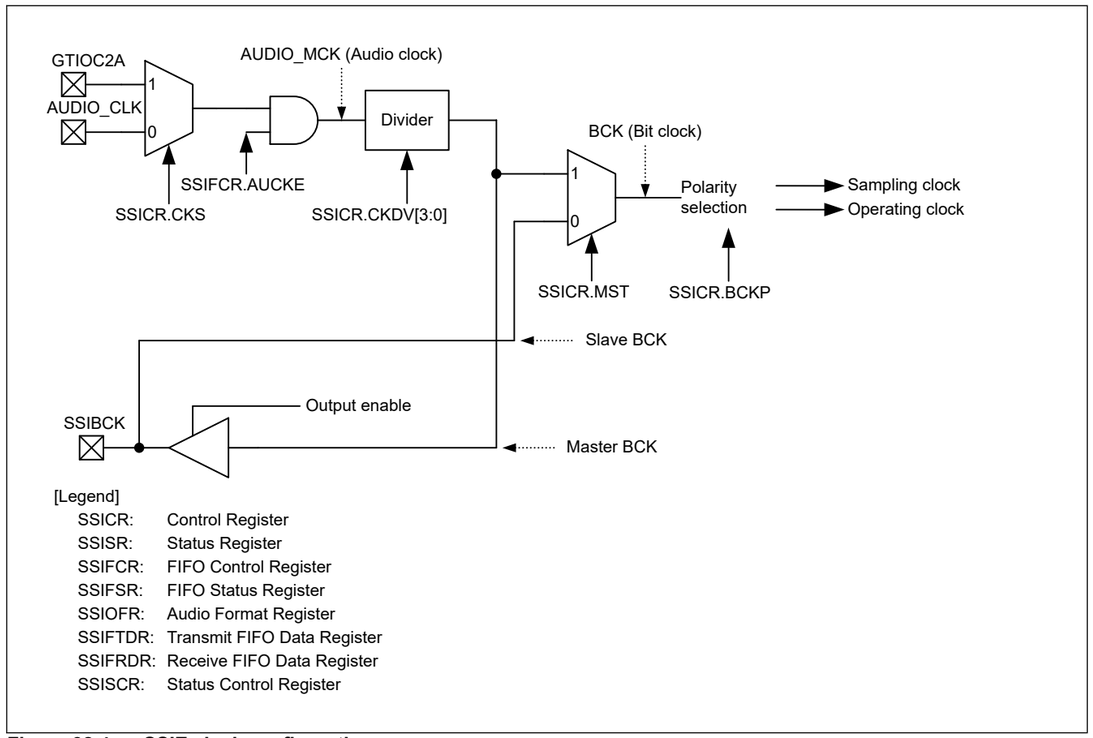


Figure 38.4 SSIE clock configuration

38.4 Register Descriptions

38.4.1 SSICR : Control Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	REN	Reception Enable*2 0: Disables reception 1: Enables reception (starts reception)	R/W
1	TEN	Transmission Enable*2 0: Disables transmission 1: Enables transmission (starts transmission)	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W

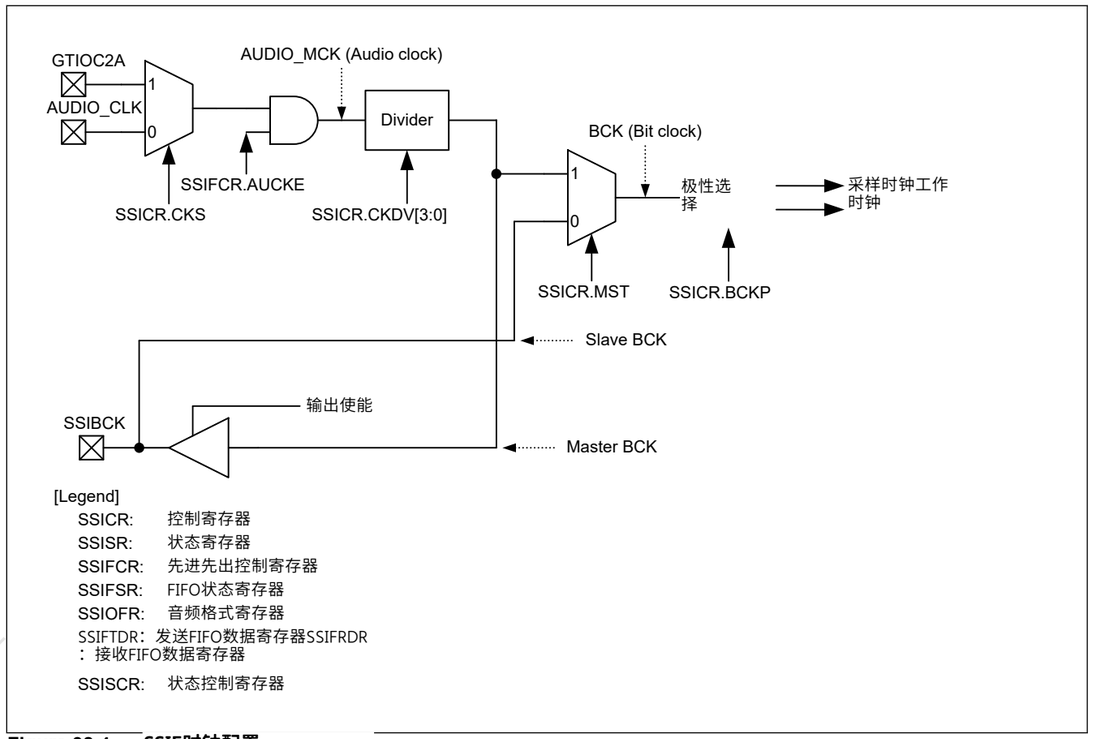


Figure 38.4 SSIE时钟配置

38.4 注册说明

38.4.1 SSICR:控制寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x00

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	REN	接收启用*2 0：禁止接收1：允许接收（开始接收）	R/W
1	TEN	传输启用*2 0：禁止发送1：允许发送（开始发送）	R/W
2	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
3	MUEN	Mute Enable 0: Disables muting on the next frame boundary 1: Enables muting on the next frame boundary	R/W
7:4	CKDV[3:0]	Selects Bit Clock Division Ratio*1 0x0: AUDIO_MCK 0x1: AUDIO_MCK/2 0x2: AUDIO_MCK/4 0x3: AUDIO_MCK/8 0x4: AUDIO_MCK/16 0x5: AUDIO_MCK/32 0x6: AUDIO_MCK/64 0x7: AUDIO_MCK/128 0x8: AUDIO_MCK/6 0x9: AUDIO_MCK/12 0xA: AUDIO_MCK/24 0xB: AUDIO_MCK/48 0xC: AUDIO_MCK/96 Others: Setting prohibited	R/W
8	DEL	Selects Serial Data Delay*1 In the monaural format, this bit controls the waveform of SSILRCK/SSIFS. For details, see section 38.5.2. Monaural Format. 0: Delay of 1 cycle of SSIBCK between SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA0 1: No delay between SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA0	R/W
9	PDTA	Selects Placement Data Alignment*1 0: Left-justifies placement data (SSIFTDR, SSIFRDR) 1: Right-justifies placement data (SSIFTDR, SSIFRDR)	R/W
10	SDTA	Selects Serial Data Alignment*1 0: Transmits and receives serial data first and then padding bits 1: Transmit and receives padding bits first and then serial data	R/W
11	SPDP	Selects Serial Padding Polarity*1 0: Padding data is at a low level 1: Padding data is at a high level	R/W
12	LRCKP	Selects the Initial Value and Polarity of LR Clock/Frame Synchronization Signal*1 0: The initial value is at a high level. The start trigger for a frame is synchronized with a falling edge of SSILRCK/SSIFS. 1: The initial value is at a low level. The start trigger for a frame is synchronized with a rising edge of SSILRCK/SSIFS.	R/W
13	BCKP	Selects Bit Clock Polarity*1 0: SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA0 change at a falling edge (SSILRCK/SSIFS and SSIRXD0/SSIDATA0 are sampled at a rising edge of SSIBCK). 1: SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA0 change at a rising edge (SSILRCK/SSIFS and SSIRXD0/SSIDATA0 are sampled at a falling edge of SSIBCK).	R/W
14	MST	Master Enable*1 0: Slave-mode communication 1: Master-mode communication	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Function	R/W
3	MUEN	静音启用 0：在下一帧边界禁用静音1：在下一帧边界启用静音	R/W
7:4	CKDV[3:0]	选择位时钟分频比*1 0x0: AUDIO_MCK 0x1: AUDIO_MCK/2 0x2: AUDIO_MCK/4 0x3: AUDIO_MCK/8 0x4: AUDIO_MCK/16 0x5: AUDIO_MCK/32 0x6: AUDIO_MCK/64 0x7: AUDIO_MCK/128 0x8: AUDIO_MCK/6 0x9: AUDIO_MCK/12 0xA: AUDIO_MCK/24 0xB: AUDIO_MCK/48 0xC: AUDIO_MCK/96 其他：禁止设置	R/W
8	DEL	选择串行数据延迟*1 在单声道格式中，该位控制SSILRCKSSIFS的波形。 有关详细信息，请参阅第38.5.2节。单声道格式。 0：在SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA0之间延迟1个SSIBCK周期 1：SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA0之间无延迟	R/W
9	PDTA	选择放置数据对齐*1 0：左对齐放置数据（SSIFTDR、SSIFRDR）1：右对齐放置数据（SSIFTDR、SSIFRDR）	R/W
10	SDTA	选择串行数据对齐*1 0：先发送和接收串行数据，然后是填充位1：先发送和接收填充位，然后是串行数据	R/W
11	SPDP	选择串行填充极性*1 0：填充数据为低电平1：填充数据为高电平	R/W
12	LRCKP	选择LR时钟帧同步信号的初始值和极性*1 0：初始值为高电平。 帧的开始触发与SSILRCK的下降沿同步SSIFS. 1：初始值为低电平。 帧的开始触发与SSILRCK的上升沿同步SSIFS.	R/W
13	BCKP	选择位时钟极性*1 0：SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA0在下降沿变化（SSILRCKSSIFS和SSIRXD0SSIDATA0在SSIBCK的上升沿采样）。 1：SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA0在上升沿变化（SSILRCKSSIFS和SSIRXD0SSIDATA0在SSIBCK的下降沿采样）。	R/W
14	MST	主使能*1 0: Slave-mode communication 1: Master-mode communication	R/W
15	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
18:16	SWL[2:0]	Selects System Word Length*1 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 24 bits 0 1 1: 32 bits 1 0 0: 48 bits 1 0 1: 64 bits 1 1 0: 128 bits 1 1 1: 256 bits	R/W
21:19	DWL[2:0]	Selects Data Word Length*1 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 18 bits 0 1 1: 20 bits 1 0 0: 22 bits 1 0 1: 24 bits 1 1 0: 32 bits 1 1 1: Setting prohibited	R/W
23:22	FRM[1:0]	Selects Frame Word Number*1	R/W
24	—	This bit is read as 0. The write value should be 0.	R/W
25	IIEN	Idle Mode Interrupt Output Enable 0: Disables idle mode interrupt output 1: Enables idle mode interrupt output	R/W
26	ROIEN	Receive Overflow Interrupt Output Enable 0: Disables receive overflow interrupt output 1: Enables receive overflow interrupt output	R/W
27	RUIEN	Receive Underflow Interrupt Output Enable 0: Disables receive underflow interrupt output 1: Enables receive underflow interrupt output	R/W
28	TOIEN	Transmit Overflow Interrupt Output Enable 0: Disables transmit overflow interrupt output 1: Enables transmit overflow interrupt output	R/W
29	TUIEN	Transmit Underflow Interrupt Output Enable 0: Disables transmit underflow interrupt output 1: Enables transmit underflow interrupt output	R/W
30	CKS	Selects an Audio Clock for Master-mode Communication*1 0: Selects the AUDIO_CLK input 1: Selects the GTIOC2A (GPT output)	R/W
31	—	This bit is read as 0. The write value should be 0.	R/W

	Communication format (SSIOFR.OMOD[1:0])		
FRM[1:0]	I²S (00b)	Monaural (10b)	TDM (01b)
00b	2	1	Setting prohibited
01b	Setting prohibited	Setting prohibited	4
10b			5
11b			6

Note 1. Writing to these bits while SSIE is in a communication state (SSISR.IIRQ = 0) is prohibited. If the value of these bits is changed by rewriting, subsequent operation is unpredictable.

Note 2. If the TEN bit or REN bit is rewritten, make sure that the SSISR.IIRQ bit is in the desired status. If the value of the TEN or REN bit is changed by rewriting, subsequent operation is unpredictable. For example, when transmission or reception is enabled, check that SSISR.IIRQ is 0; when transmission or reception is disabled, check that SSISR.IIRQ is 1.

With this register, select an audio clock, control interrupt requests, select data formats, and set an operation mode.

Bit	Symbol	Function	R/W
18:16	SWL[2:0]	选择系统字长*1 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 24 bits 0 1 1: 32 bits 1 0 0: 48 bits 1 0 1: 64 bits 1 1 0: 128 bits 1 1 1: 256 bits	R/W
21:19	DWL[2:0]	选择数据字长*1 000：8位001：16位010：18位011：20位100：22位101：24位110：32位111：禁止设置	R/W
23:22	FRM[1:0]	选择帧字号*1	R/W
24	—	该位读取为0。写入值应为0。	R/W
25	IIEN	空闲模式中断输出使能 0：禁用空闲模式中断输出1：启用空闲模式中断输出	R/W
26	ROIEN	接收溢出中断输出使能 0：禁止接收溢出中断输出1：使能接收溢出中断输出	R/W
27	RUIEN	接收下溢中断输出使能 0：禁止接收下溢中断输出1：使能接收下溢中断输出	R/W
28	TOIEN	发送溢出中断输出使能 0：禁止发送溢出中断输出1：使能发送溢出中断输出	R/W
29	TUIEN	发送下溢中断输出使能 0：禁止发送下溢中断输出1：使能发送下溢中断输出	R/W
30	CKS	选择主模式通信的音频时钟*1 0：选择AUDIO_CLK输入1：选择GTIOC2A（GPT输出）	R/W
31	—	该位读取为0。写入值应为0。	R/W

	通讯格式（SSIOFR.OMOD[1:0]）		
FRM[1:0]	I²S (00b)	Monaural (10b)	TDM (01b)
00b	2	1	禁止设定
01b	禁止设定	禁止设定	4
10b			5
11b			6

注1.禁止在SSIE处于通信状态(SSISR.IIRQ=0)时写入这些位。如果这些位的值通过重写而改变，后续的操作是不可预知的。

注2.如果TEN位或REN位被重写，请确保SSISR.IIRQ位处于所需状态。如果TEN或REN位的值因重写而改变，后续操作将无法预测。例如，启用发送或接收时，检查SSISR.IIRQ是否为0；当发送或接收被禁用时，检查SSISR.IIRQ是否为1。

使用该寄存器，选择音频时钟、控制中断请求、选择数据格式和设置操作模式。

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TEN and REN bits (Transmission and Reception Enable)

The TEN and REN bits enable/disable transmission and reception. When 1 is written to one of these bits, the corresponding communication operation starts in synchronization with a start trigger by the SSILRCK/SSIFS signal. For details, see section 38.8.2. Transmission to section 38.8.4. Transmission and Reception. When 0 is written to this bit, the current communication operation stops at the next frame boundary. To use SSIE for both transmission and reception, always write 1 to these bits together. When stopping the communication using SSIE, always disable both transmission and reception (write 0 to the TEN and REN bits).

If you want to stop SSIE before a frame boundary is reached, perform a software reset procedure.

MUEN bit (Mute Enable)

The MUEN bit sets/clears the mute function for the data output from the SSITXD0/SSIDATA0 pin. When this bit is set to 1 in the middle of a frame, the SSITXD0/SSIDATA0 output changes to 0 at the next frame boundary. When this bit is set to 0 in the middle of a frame, the SSITXD0/SSIDATA0 output changes to the data of transmit FIFO data register at the next frame boundary. Note that this bit controls data only. Status flags and interrupt signals are normally generated.

Changing the value of this bit must be performed only after setting the communication format to be used.

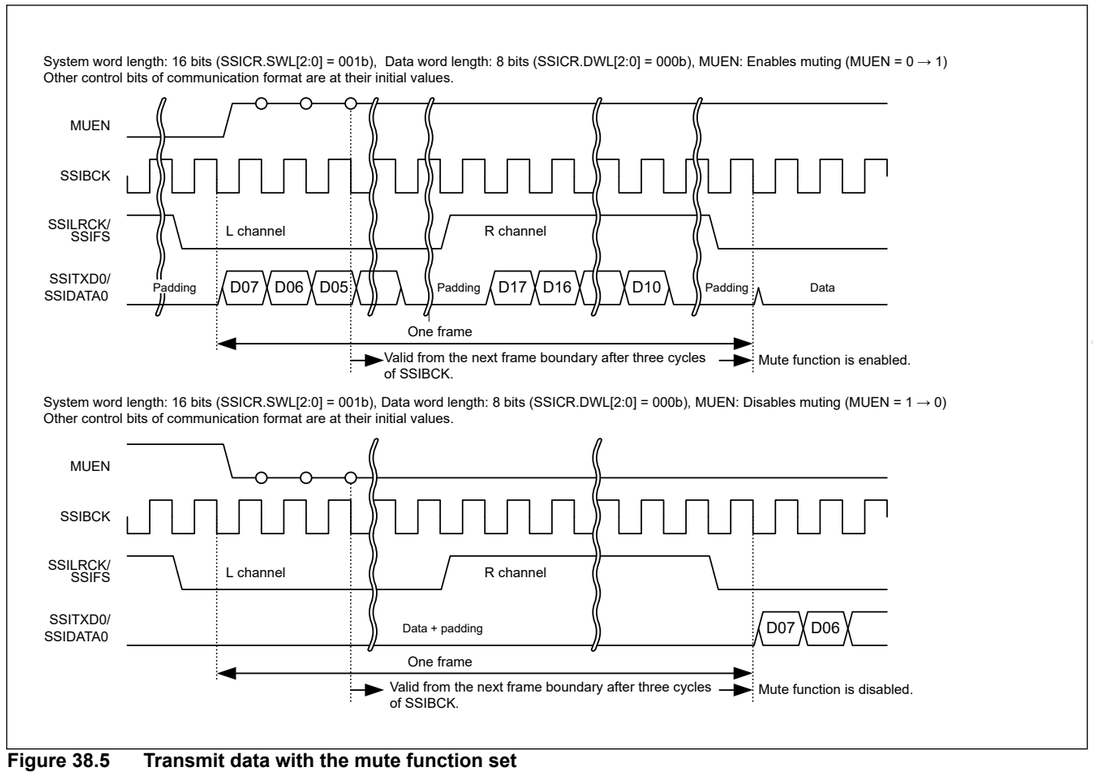

Figure 38.5 Transmit data with the mute function set

CKDV[3:0] bits (Selects Bit Clock Division Ratio)

The CKDV[3:0] bits set the division ratio of the bit clock based on AUDIO_MCK in master-mode communication (MST= 1). In slave-mode communication (MST = 0), setting of these bits are invalid.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in section 38.4.3. SSIFCR : FIFO Control Register.

TEN和REN位（发送和接收使能）

TEN和REN位使能禁用发送和接收。当这些位之一写入1时，相应的通信操作与SSILRCKSSIFS信号的开始触发同步开始。有关详细信息，请参阅第38.8.2节。传输到第38.8.4节。传输和接收。当向该位写入0时，当前通信操作在下一帧边界处停止。要同时使用SSIE进行发送和接收，请始终将1一起写入这些位。使用SSIE停止通信时，始终禁用发送和接收（将0写入TEN和REN位）。

如果要在达到帧边界之前停止SSIE，请执行软件复位程序。

MUEN bit (Mute Enable)

MUEN位设置清除SSITXD0SSIDATA0引脚数据输出的静音功能。当该位在帧中间设置为1时，SSITXD0SSIDATA0输出在下一帧边界变为0。当该位在帧中间设置为0时，SSITXD0SSIDATA0输出在下一帧边界变为发送FIFO数据寄存器的数据。请注意，该位仅控制数据。通常会产生状态标志和中断信号。

只有在设置要使用的通信格式后才能更改该位的值。

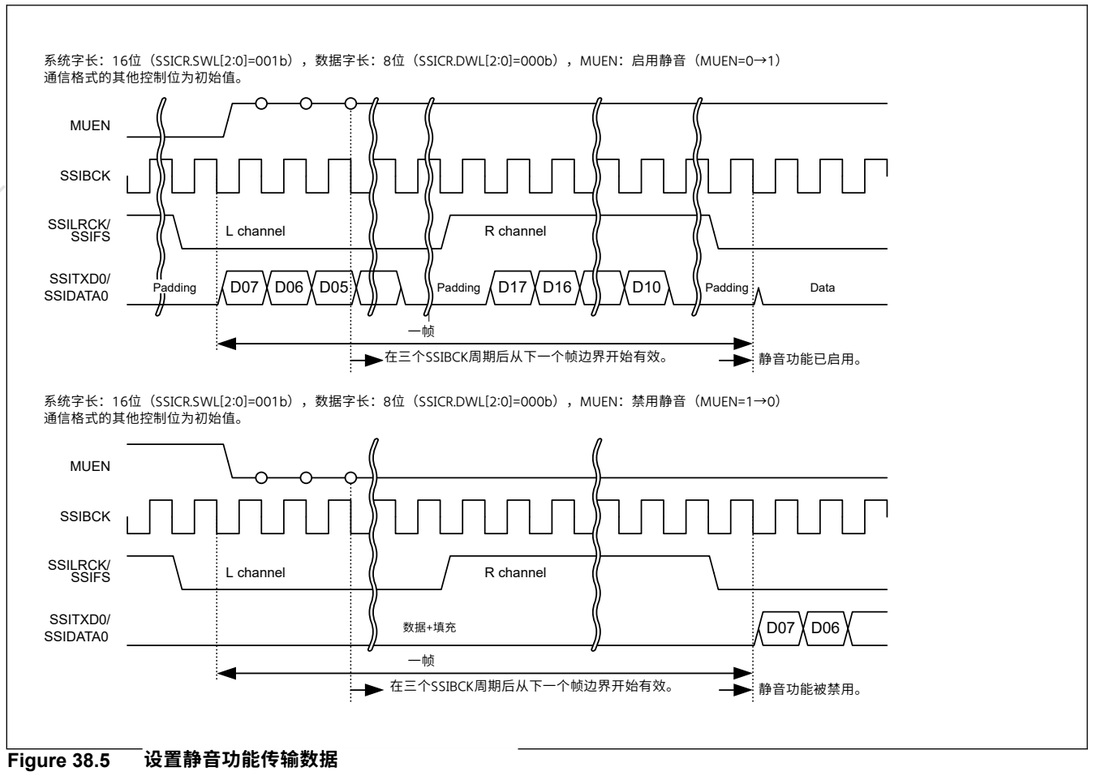

Figure 38.5 设置静音功能传输数据

CKDV[3:0]位（选择位时钟分频比）

CKDV[3:0]位在主模式通信(MST=1)中根据AUDIO_MCK设置位时钟的分频比。在从机模式通信(MST=0)中，这些位的设置无效。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见第38.4.3节中AUCKE位的详细说明。SSIFCR：FIFO控制寄存器。

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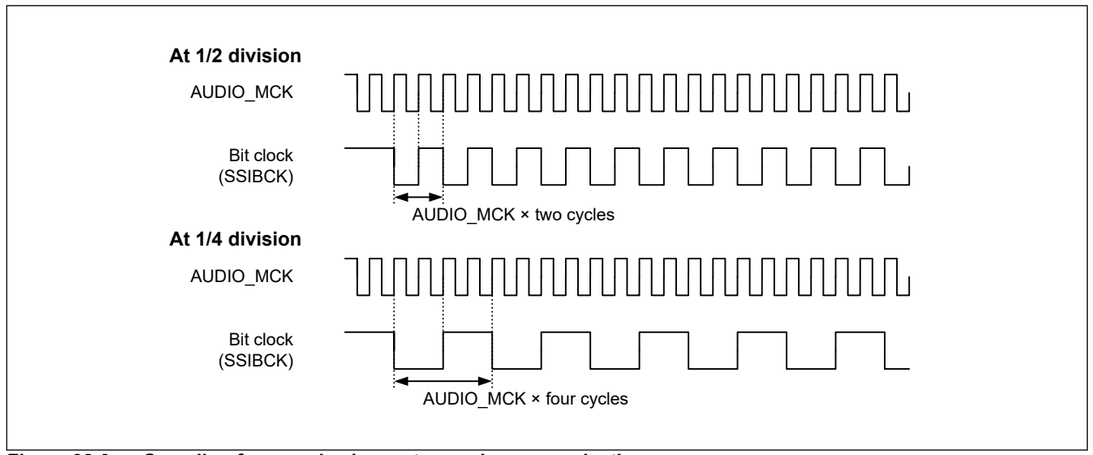


Figure 38.6 Sampling frequencies in master-mode communication

DEL bit (Selects Serial Data Delay)

The DEL bit sets whether or not there will be a delay between SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA0.

For the I^{2}S or TDM format, set the DEL bit to 0. When the monaural format is used, setting of this bit changes the high period width of SSILRCK/SSIFS. For details, see section 38.5.2. Monaural Format. When using a compatible communication format, specify a setting of this bit that enables communication.

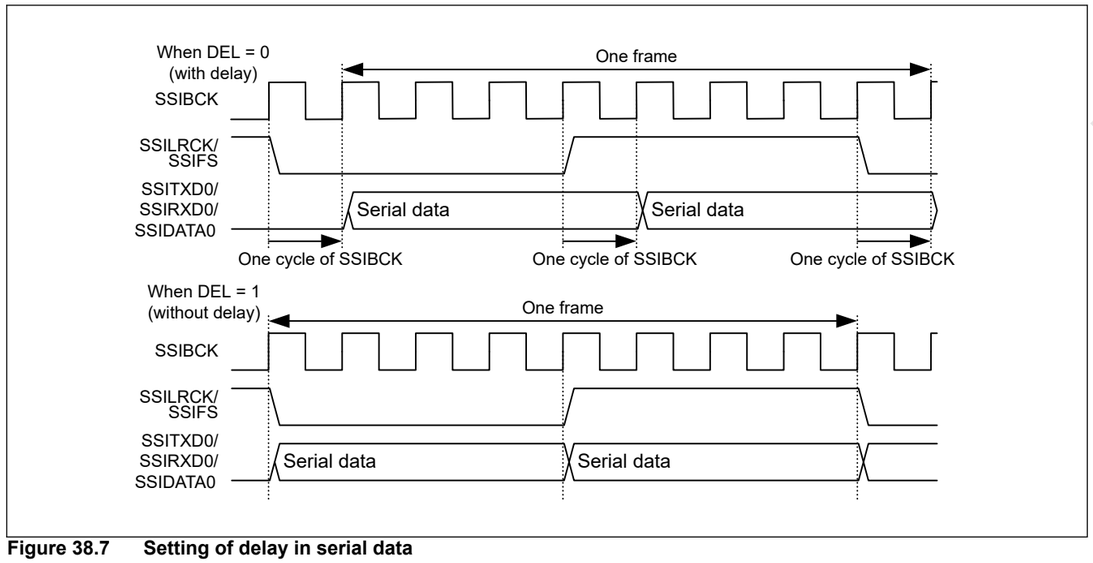


Figure 38.7 Setting of delay in serial data

PDTA bit (Selects Placement Data Alignment)

The PDTA bit sets how to align placement data. With the setting of data word length as 32 bits (SSICR.DWL[2:0] = 110b), this bit is invalid.

At transmission, see Figure 38.8.

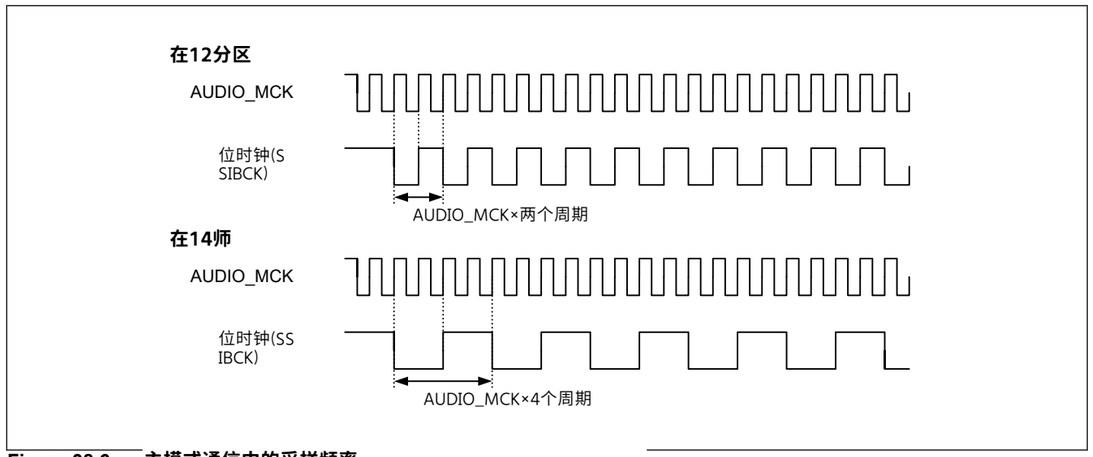


Figure 38.6 主模式通信中的采样频率

DEL位（选择串行数据延迟）

DEL位设置SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA0之间是否会有延迟。

对于I2S或TDM格式，将DEL位设置为0。当使用单声道格式时，该位的设置会改变SSILRCKSSIFS的高周期宽度。有关详细信息，请参阅第38.5.2节。单声道格式。使用兼容的通信格式时，指定该位的设置以启用通信。

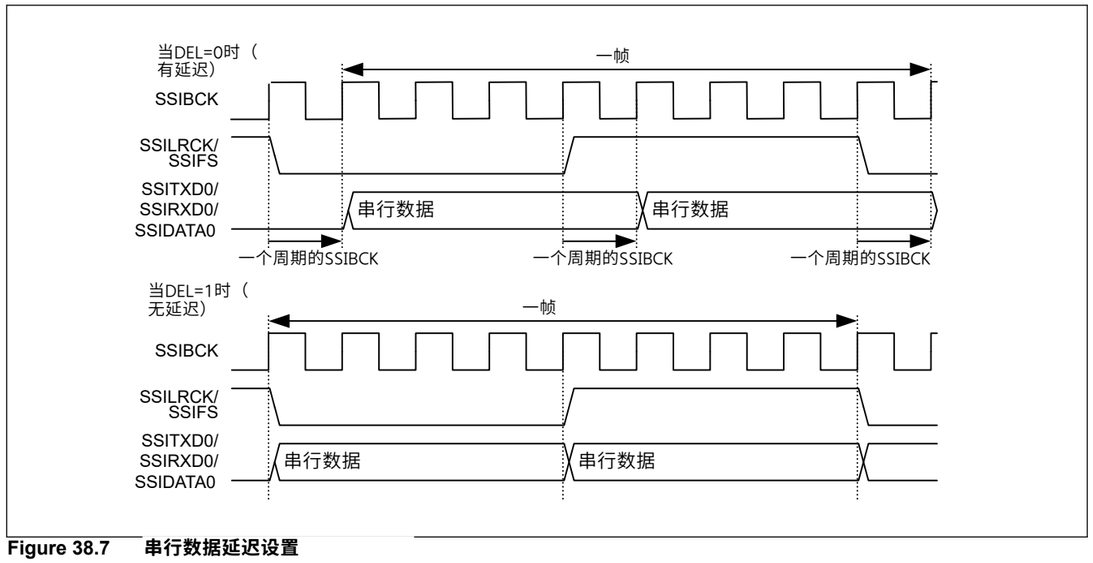


Figure 38.7 串行数据延迟设置

PDTA位（选择布局数据对齐）

PDTA位设置如何对齐布局数据。数据字长设置为32位（SSICR.DWL[2:0]=110b）时，该位无效。

传输时，见图38.8。

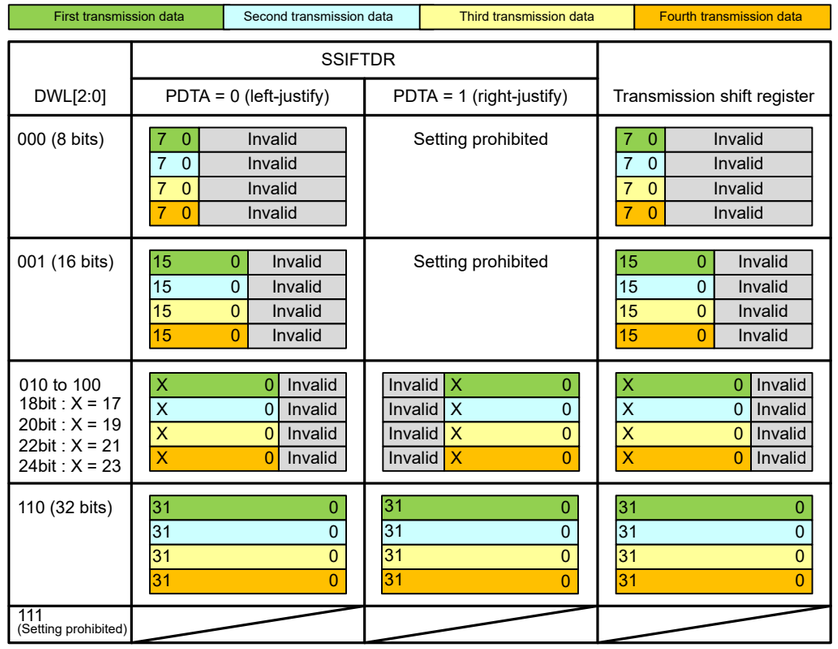


Figure 38.8 Alignment of placement data at transmission

At reception, see Figure 38.9.

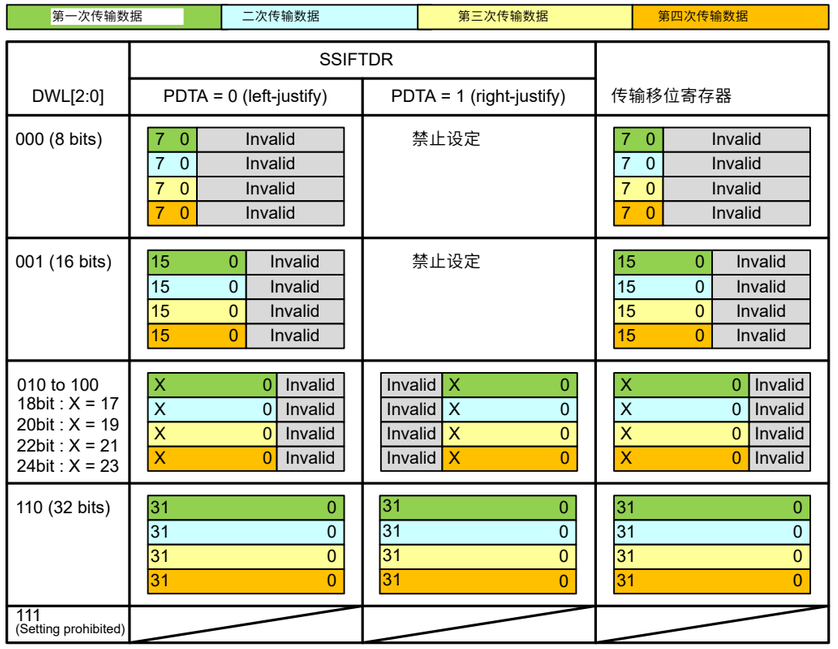


Figure 38.8 在传输时对齐放置数据

在接待处，见图38.9。

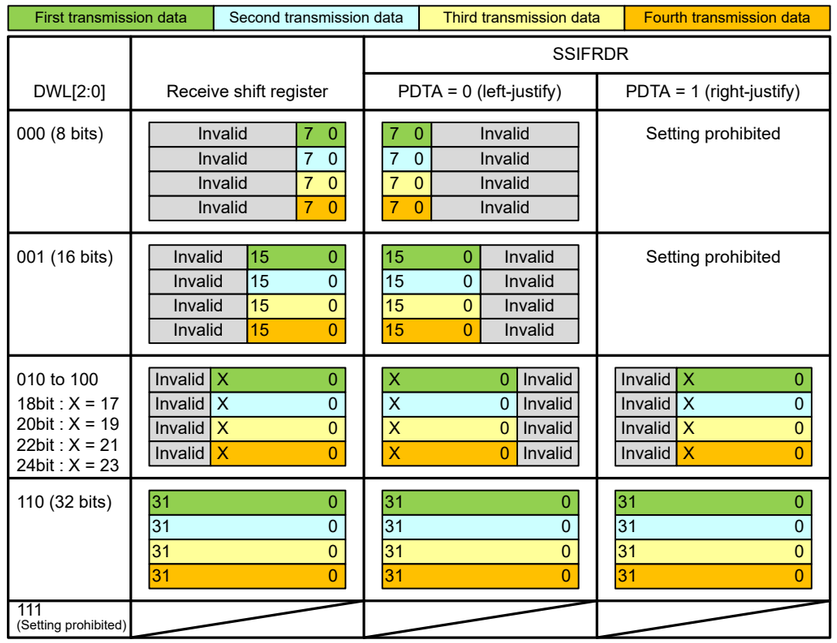


Figure 38.9 Alignment of placement data at reception

SDTA bit (Selects Serial Data Delay)

The SDTA bit sets how to align serial data and padding bits. For communication without padding bits, this bit is invalid.

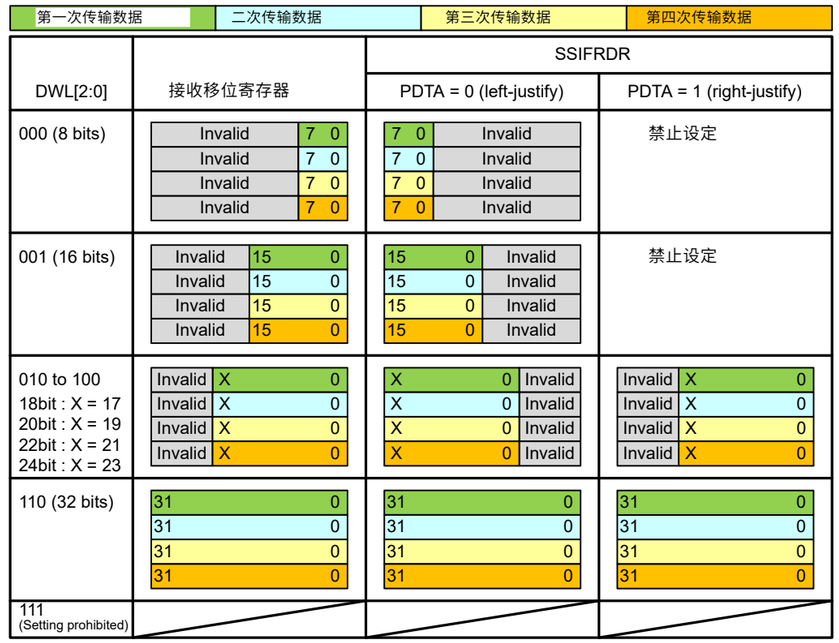


Figure 38.9 在接收时对齐放置数据

SDTA位（选择串行数据延迟）

SDTA位设置如何对齐串行数据和填充位。对于没有填充位的通信，该位无效。

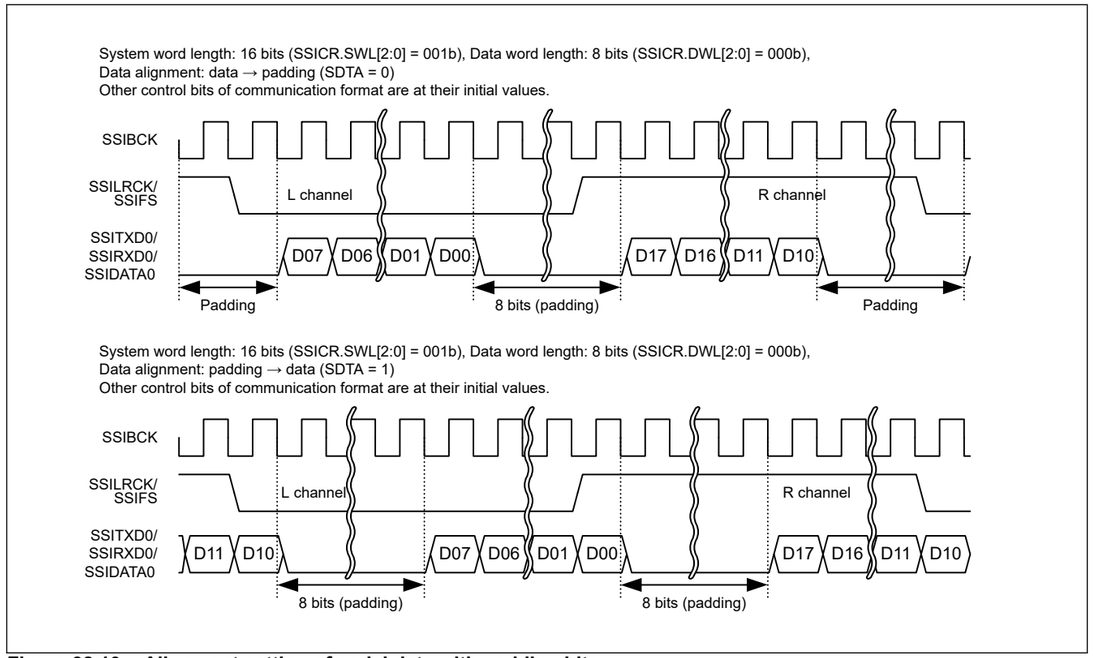


Figure 38.10 Alignment setting of serial data with padding bits

SPDP bit (Selects Serial Padding Polarity)

The SPDP bit sets polarity of padding bits.

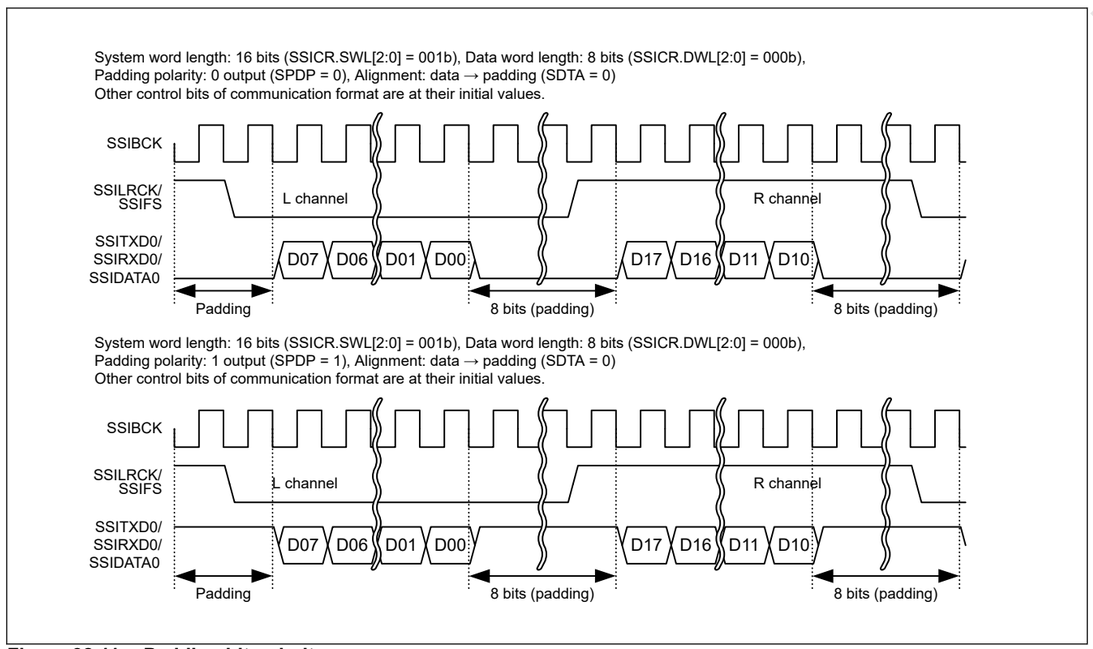


Figure 38.11 Padding bit polarity

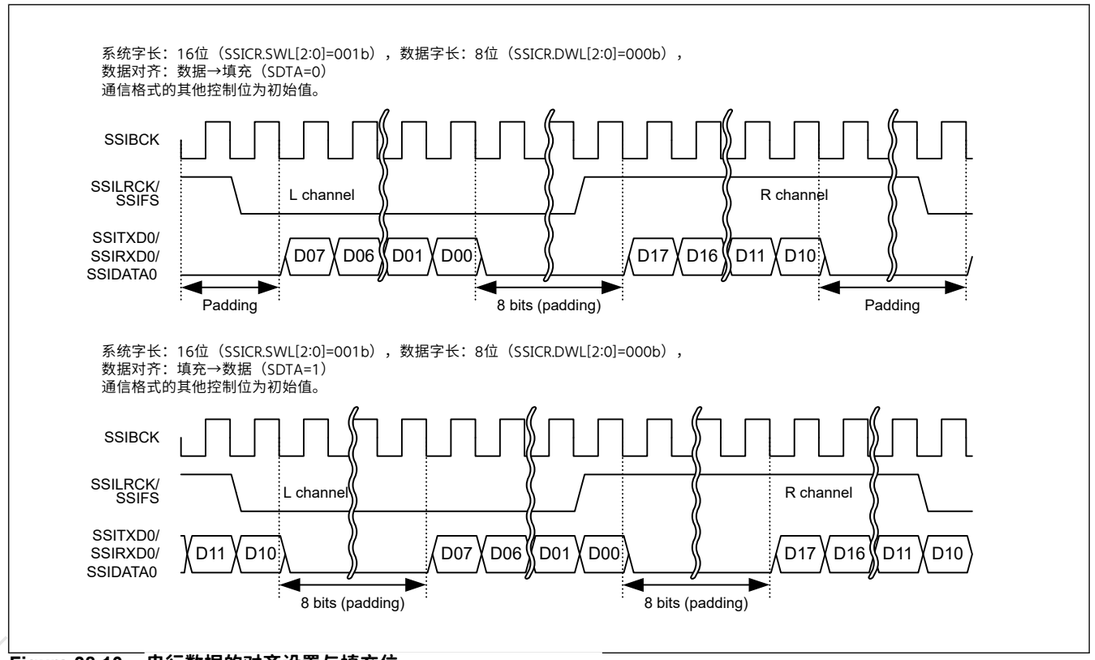


Figure 38.10 串行数据的对齐设置与填充位

SPDP位（选择串行填充极性）

SPDP位设置填充位的极性。

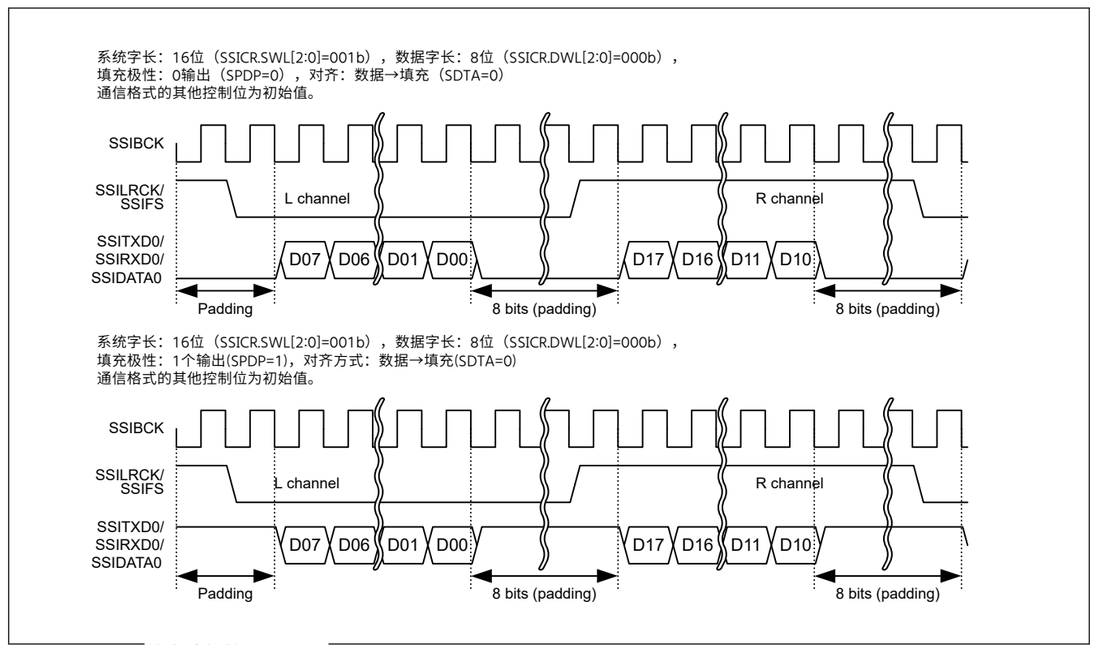


Figure 38.11 填充位极性

LRCKP bit (Selects the Initial Value and Polarity of LR Clock/Frame Synchronization Signal)

The LRCKP bit sets the initial value and polarity of SSILRCK/SSIFS. Set this bit according to the communication format to be used in SSIE. See Table 38.3 Initial output value and polarity of SSILRCK/SSIFS pin. For the slave-mode communication (MST = 0), only the start trigger is used.

Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in section 38.4.7. SSIOFR : Audio Format Register.

Table 38.3 Initial output value and polarity of SSILRCK/SSIFS pin

Communication Format	Expected Initial State	Setting Value of LRCKP
I²S	High	0
Monaural	Low	1
TDM	Low	1

Note: When the format to be used is compatible with the I²S, monaural, or TDM format, specify settings to enable communication with the respective formats.

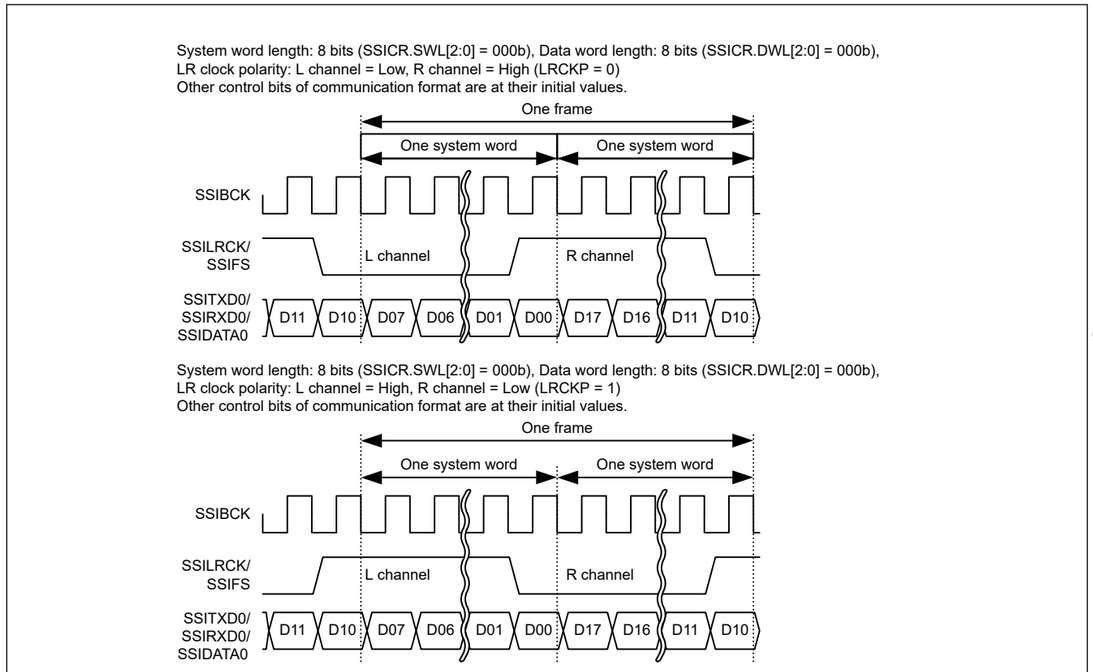


Figure 38.12 LR clock/frame synchronization polarity setting

BCKP bit (Selects Bit Clock Polarity)

The BCKP bit sets the bit clock polarity.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in section 38.4.3. SSIFCR : FIFO Control Register.

Table 38.4 Bit clock polarity (1 of 2)

Communication	Master/Slave	Timing	BCKP = 0	BCKP = 1
Reception	Slave	At SSILRCK/SSIFS sampling	SSIBCK rising edge	SSIBCK falling edge
	Master/slave	At SSIRXD0/SSIDATA0 sampling	SSIBCK rising edge	SSIBCK falling edge

LRCKP位（选择LR时钟帧同步信号的初始值和极性）

LRCKP位设置SSILRCKSSIFS的初始值和极性。根据要在SSIE中使用的通信格式设置该位。请参见表38.3SSILRCKSSIFS引脚的初始输出值和极性。对于从模式通信(MST=0)，仅使用启动触发器。

当向SSILRCKSSIFS引脚提供LR时钟停止时，必须执行写入这些位。LR时钟的输出详见38.4.7节LRCONT位的详细说明。SSIOFR：音频格式寄存器。

Table 38.3 SSILRCKSSIFS管脚的初始输出值和极性

通讯格式	预期的初始状态	LRCKP设定值
I²S	High	0
Monaural	Low	1
TDM	Low	1

Note: 当要使用的格式与I2S、单声道或TDM格式兼容时，指定设置以启用与相应格式的通信。

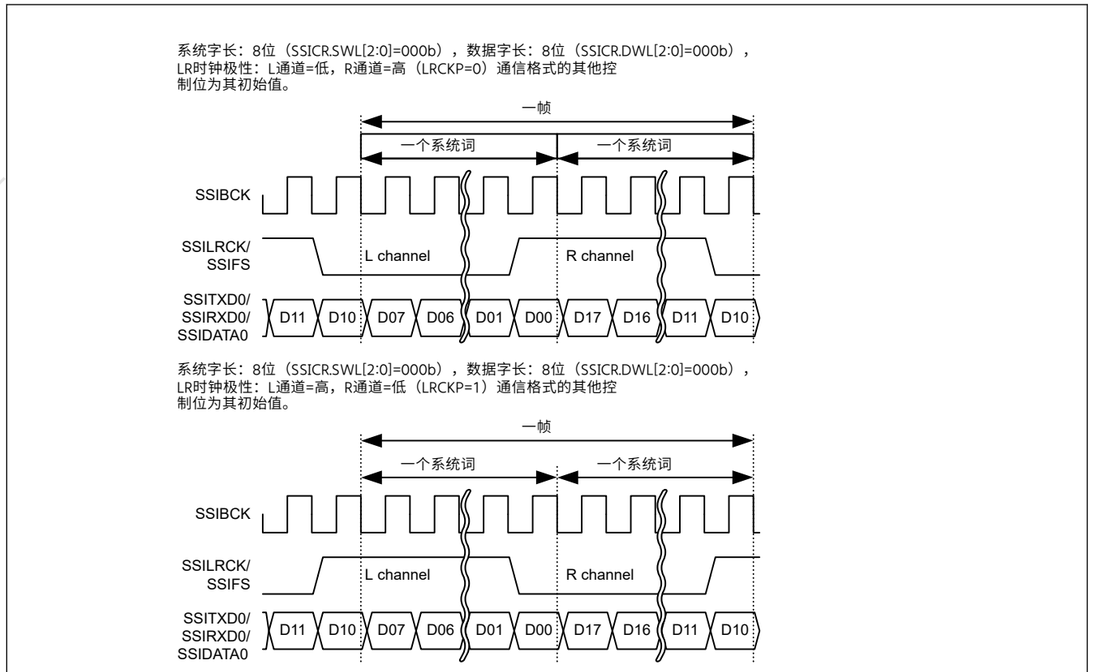


Figure 38.12 LR时钟帧同步极性设置

BCKP位（选择位时钟极性）

BCKP位设置位时钟极性。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见第38.4.3节中AUCKE位的详细说明。SSIFCR：FIFO控制寄存器。

Table 38.4 位时钟极性（1of2）

Communication	Master/Slave	Timing	BCKP = 0	BCKP = 1
Reception	Slave	在SSILRCKSSIFS采样	SSIBCK上升沿	SSIBCK下降沿
	Master/slave	在SSIRXD0SSIDATA0采样	SSIBCK上升沿	SSIBCK下降沿

Table 38.4 Bit clock polarity (2 of 2)

Communication	Master/Slave	Timing	BCKP = 0	BCKP = 1
Transmission	Master	At change of SSILRCK/SSIFS output	SSIBCK falling edge	SSIBCK rising edge
	Master/slave	At change of SSITXD0/SSIDATA0 output	SSIBCK falling edge	SSIBCK rising edge

MST bit (Master Enable)

The MST bit sets master-/slave-mode communication.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in section 38.4.3. SSIFCR : FIFO Control Register.

SWL[2:0] bits (Selects System Word Length)

The SWL[2:0] bits set the number of bits in one system word. Padding bits are sent and received in relation with one data word set with DWL[2:0]. See Table 38.11 for details.

Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in section 38.4.7. SSIOFR : Audio Format Register.

DWL[2:0] bits (Selects Data Word Length)

The DWL[2:0] bits set the number of bits in one data word. The data word length (number of bits per data word) must not exceed the system word length (number of bits per system word). For details, see Table 38.11.

FRM[1:0] bits (Selects Frame Word Number)

The FRM[1:0] bits set the frame word number in individual communication formats.

Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in section 38.4.7. SSIOFR : Audio Format Register.

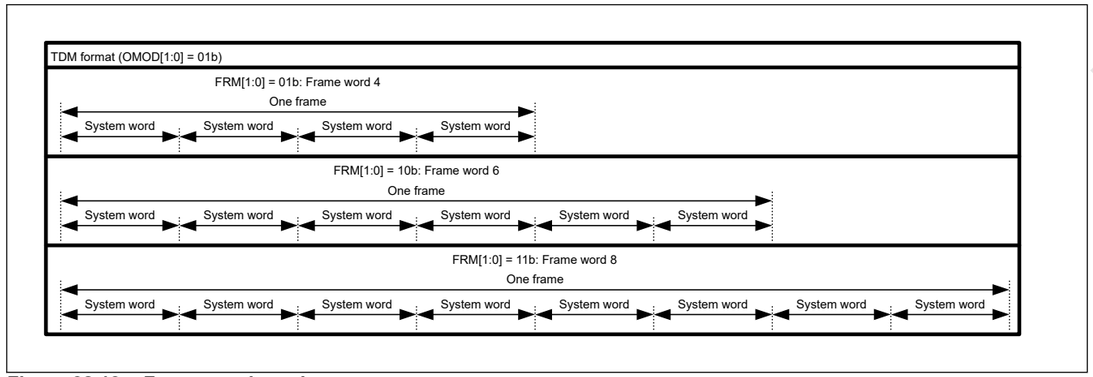


Figure 38.13 Frame word number

IIEN bit (Idle Mode Interrupt Output Enable)

The IIEN bit enables/disables output of idle mode interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.IIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.IIRQ = 1.

ROIEN bit (Receive Overflow Interrupt Output Enable)

The ROIEN bit enables/disables output of receive overflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.ROIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.ROIRQ = 1.

RUIEN bit (Receive Underflow Interrupt Output Enable)

The RUIEN bit enables/disables output of receive underflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.RUIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.RUIRQ = 1.

Table 38.4 位时钟极性（2之2）

Communication	Master/Slave	Timing	BCKP = 0	BCKP = 1
Transmission	Master	在改变SSILRCKSSIFS输出时	SSIBCK下降沿	SSIBCK上升沿
	Master/slave	在SSITXD0SSIDATA0输出变化时	SSIBCK下降沿	SSIBCK上升沿

MST bit (Master Enable)

MST位设置主从模式通信。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见第38.4.3节中AUCKE位的详细说明。SSIFCR：FIFO控制寄存器。

SWL[2:0]位（选择系统字长）

SWL[2:0]位设置一个系统字中的位数。填充位的发送和接收与使用DWL[2:0]设置的一个数据字相关。详见表38.11。

当向SSILRCKSSIFS引脚提供LR时钟停止时，必须执行写入这些位。LR时钟的输出详见38.4.7节LRCONT位的详细说明。SSIOFR：音频格式寄存器。

DWL[2:0]位（选择数据字长）

DWL[2:0]位设置一个数据字中的位数。数据字长（每个数据字的位数）不得超过系统字长（每个系统字的位数）。详见表38.11。

FRM[1:0]位（选择帧字号）

FRM[1:0]位设置各个通信格式中的帧字号。

当向SSILRCKSSIFS引脚提供LR时钟停止时，必须执行写入这些位。LR时钟的输出详见38.4.7节LRCONT位的详细说明。SSIOFR：音频格式寄存器。

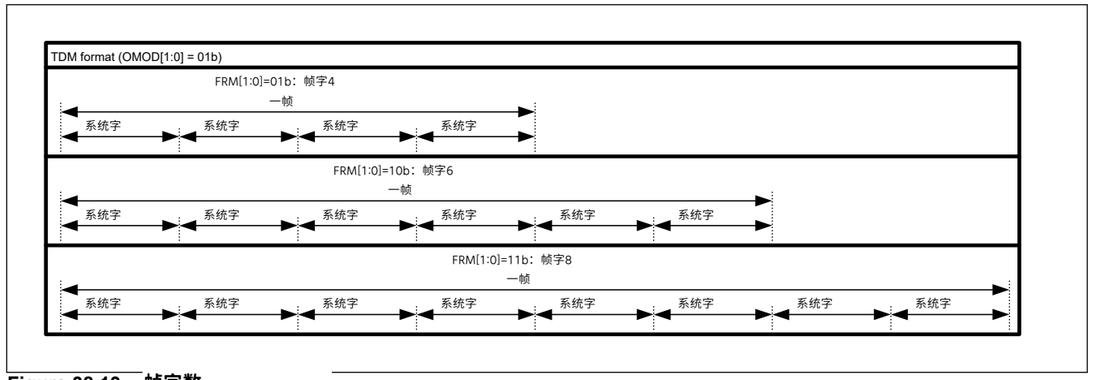


Figure 38.13 帧字数

IIEN位（空闲模式中断输出使能）

IIEN位启用禁用空闲模式中断的输出。通过启用该位（将其设置为1），在SSISR.IIRQ=1的上升沿输出中断。当SSISR.IIRQ=1时该位从0变为1时也会输出中断。

ROIEN位（接收溢出中断输出使能）

ROIEN位使能禁止接收溢出中断的输出。通过启用该位（将其设置为1），在SSISR.ROIRQ=1的上升沿输出中断。当SSISR.ROIRQ=1时该位从0变为1时也会输出中断。

RUIEN位（接收下溢中断输出使能）

RUIEN位启用禁用接收下溢中断的输出。通过启用该位（将其设置为1），在SSISR.RUIRQ=1的上升沿输出中断。当SSISR.RUIRQ=1时该位从0变为1时也会输出中断。

TOIEN bit (Transmit Overflow Interrupt Output Enable)

The TOIEN bit enables/disables output of transmit overflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.TOIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.TOIRQ = 1.

TUIEN bit (Transmit Underflow Interrupt Output Enable)

The TUIEN bit enables/disables output of transmit underflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.TUIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.TUIRQ = 1.

CKS bit (Selects an Audio Clock for Master-mode Communication)

The CKS bit sets the audio clock in master-mode communication (MST = 1). In slave-mode communication (MST = 0), setting of this bit is invalid.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in section 38.4.3. SSIFCR : FIFO Control Register.

38.4.2 SSISR : Status Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
24:0	—	These bits are read as 0. The write value should be 0.	R/W
25	IIRQ	Idle Mode Status Flag 0: In the communication state 1: In the idle state	R
26	ROIRQ	Receive Overflow Error Status Flag 0: No receive overflow error is generated. 1: A receive overflow error is generated.	R/W
27	RUIRQ	Receive Underflow Error Status Flag 0: No receive underflow error is generated. 1: A receive underflow error is generated.	R/W
28	TOIRQ	Transmit Overflow Error Status Flag 0: No transmit overflow error is generated. 1: A transmit overflow error is generated.	R/W
29	TUIRQ	Transmit Underflow Error Status flag 0: No transmit underflow error is generated. 1: A transmit underflow error is generated.	R/W
31:30	—	These bits are read as 0. The write value should be 0.	R/W

This register is configured with status flags that indicate SSIE operational state.

IIRQ flag (Idle Mode Status Flag)

The IIRQ flag is a status flag that indicates the idle state. It indicates whether SSIE is in the idle state or communication state.

For details, see Figure 38.14 and Figure 38.15.

TOIEN位（发送溢出中断输出使能）

TOIEN位使能禁用发送溢出中断的输出。通过启用该位（将其设置为1），在SSISR.TOIRQ=1的上升沿输出中断。当SSISR.TOIRQ=1时该位从0变为1时也会输出中断。

TUIEN位（发送下溢中断输出使能）

TUIEN位使能禁用发送下溢中断的输出。通过启用该位（将其设置为1），在SSISR.TUIRQ=1的上升沿输出中断。当SSISR.TUIRQ=1时该位从0变为1时也会输出中断。

CKS位（选择主模式通信的音频时钟）

CKS位设置主模式通信中的音频时钟(MST=1)。在从机模式通信(MST=0)中，该位的设置无效。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见第38.4.3节中AUCKE位的详细说明。SSIFCR：FIFO控制寄存器。

38.4.2 SSISR：状态寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

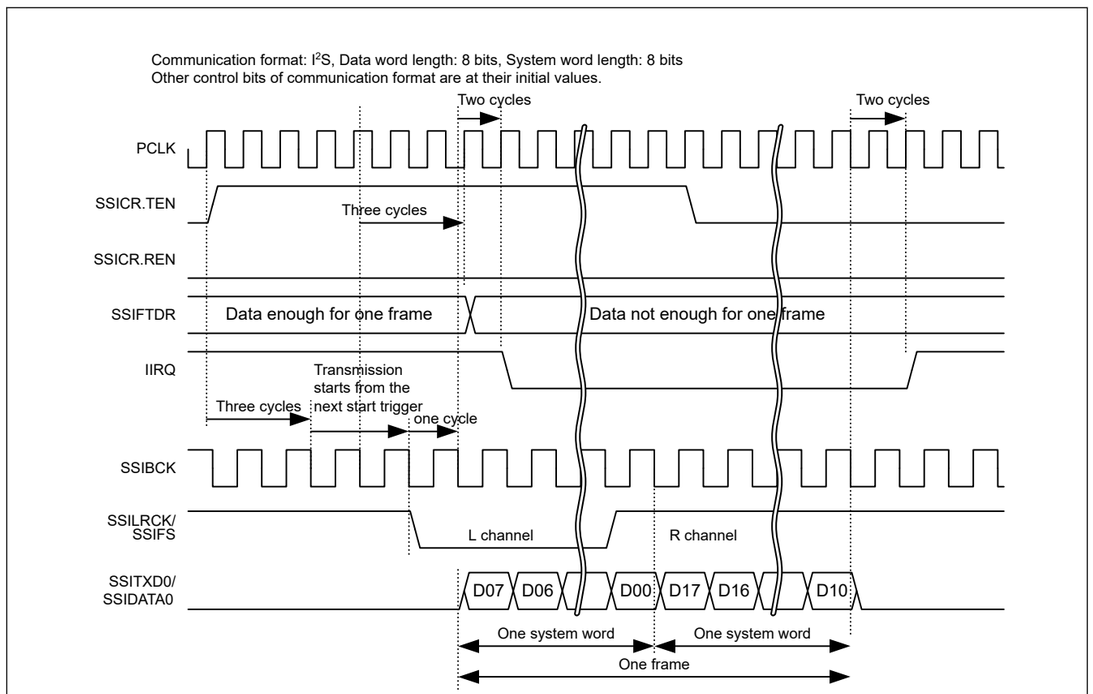
Bit	Symbol	Function	R/W
24:0	—	这些位被读取为0。写入值应为0。	R/W
25	IIRQ	空闲模式状态标志 0：处于通信状态1：处于空闲状态	R
26	ROIRQ	接收溢出错误状态标志 0：不产生接收溢出错误。1：产生接收溢出错误。	R/W
27	RUIRQ	接收下溢错误状态标志 0：不产生接收下溢错误。1：产生接收下溢错误。	R/W
28	TOIRQ	发送溢出错误状态标志 0：不产生发送溢出错误。1：产生发送溢出错误。	R/W
29	TUIRQ	发送下溢错误状态标志 0：不产生发送下溢错误。1：产生发送下溢错误。	R/W
31:30	—	这些位被读取为0。写入值应为0。	R/W

该寄存器配置有指示SSIE操作状态的状态标志。

IIRQ标志（空闲模式状态标志）

IIRQ标志是指示空闲状态的状态标志。它指示SSIE是处于空闲状态还是通信状态。

详见图38.14和图38.15。



Note: PCLK = PCLKB

Figure 38.14 IIRQ setting timing (transmission)

- Transmitter (dedicated to transmission)

[Clearing condition]

While transmission was enabled (SSICR.TEN = 1 and SSICR.REN = 0), the transmit data for a transmission frame was written to the SSIFTDR register, and a start trigger was generated by the SSILRCK/SSIFS signal.

[Clearing timing]

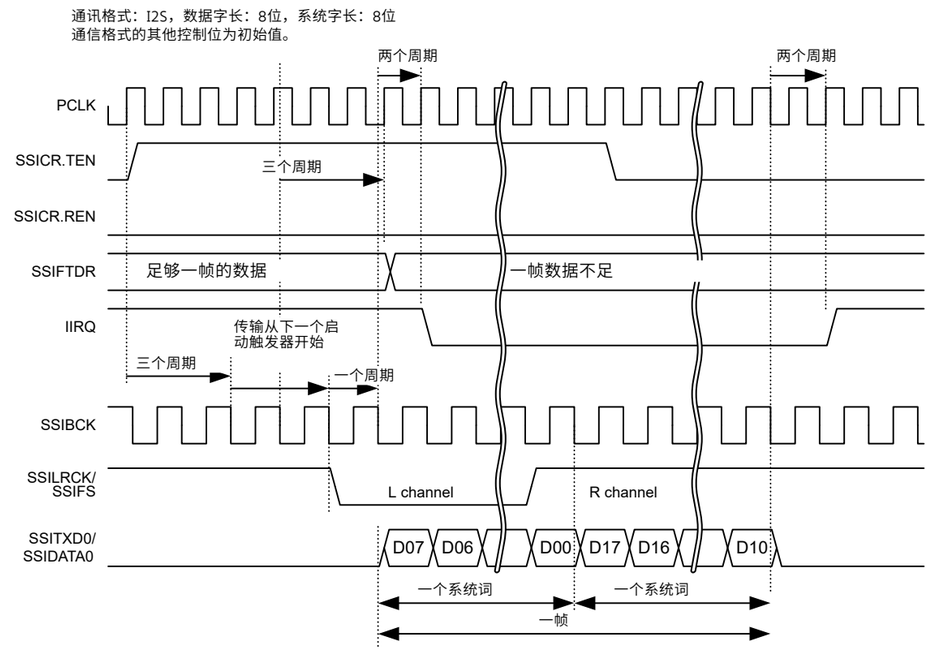
1 SSIBCK cycle + 2 PCLKB cycles after generation of the start trigger that is the clearing condition.

[Setting condition]

While transmission and reception were disabled (SSICR.TEN = 0 and SSICR.REN = 0), transmission of one frame was complete.

[Setting timing]

2 PCLKB cycles after the end of transmission (at a frame boundary) that is the setting condition.



Note: PCLK = PCLKB

Figure 38.14 IIRQ设置时序（传输）

●发射器（传输专用）

[Clearing condition]

启用传输时（SSICR.TEN=1和SSICR.REN=0），传输帧的传输数据被写入SSIFTDR寄存器，并由SSILRCKSSIFS信号生成启动触发。

[Clearing timing]

1个SSIBCK周期+2个PCLKB周期在产生作为清除条件的启动触发之后。

[Setting condition]

当发送和接收被禁用时（SSICR.TEN=0和SSICR.REN=0），一帧的发送完成。

[Setting timing]

在作为设置条件的传输结束后（在帧边界处）的2个PCLKB周期。

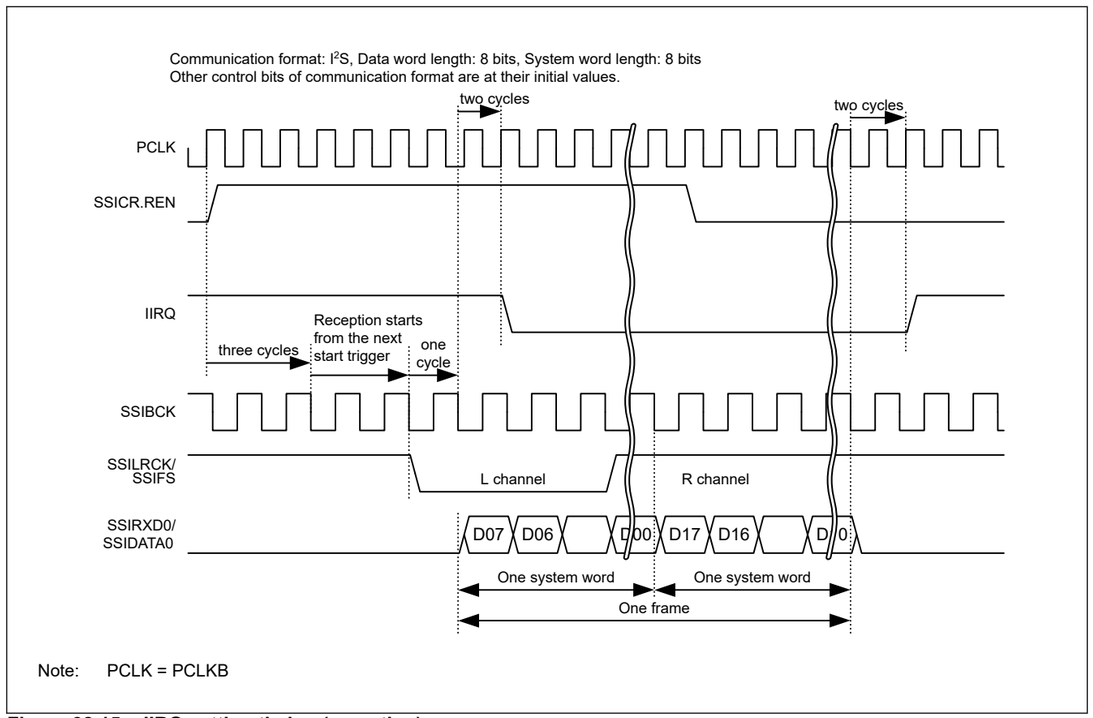


Figure 38.15 IIRQ setting timing (reception)

- Receiver (dedicated to reception)

[Clearing condition]

While reception was enabled (SSICR.TEN = 0 and SSICR.REN = 01, a start trigger was generated by the SSILRCK/SSIFS signal.

[Clearing timing]

1 SSIBCK cycle + 2 PCLKB cycles after generation of the start trigger that is the clearing condition.

[Setting condition]

While transmission and reception were disabled (SSICR.TEN = 0 and SSICR.REN = 0), reception of one frame was complete.

[Setting timing]

2 PCLKB cycles after the end of reception (at a frame boundary) that is the setting condition.

- Transceiver (transmission and reception)

[Clearing condition]

While transmission and reception were enabled (SSICR.TEN = 1 and SSICR.REN = 1), the transmit data for a transmission frame was written to the SSIFTDR register, and a start trigger is generated by the SSILRCK/SSIFS signal.

[Clearing timing]

1 SSIBCK cycle + 2 PCLKB cycles after generation of the start trigger that is the clearing condition.

[Setting condition]

While transmission and reception were disabled (SSICR.TEN = 0 and SSICR.REN = 0), transmission of one frame was complete.

[Setting timing]

2 PCLKB cycles after the end of transmission (at a frame boundary) that is the setting condition.

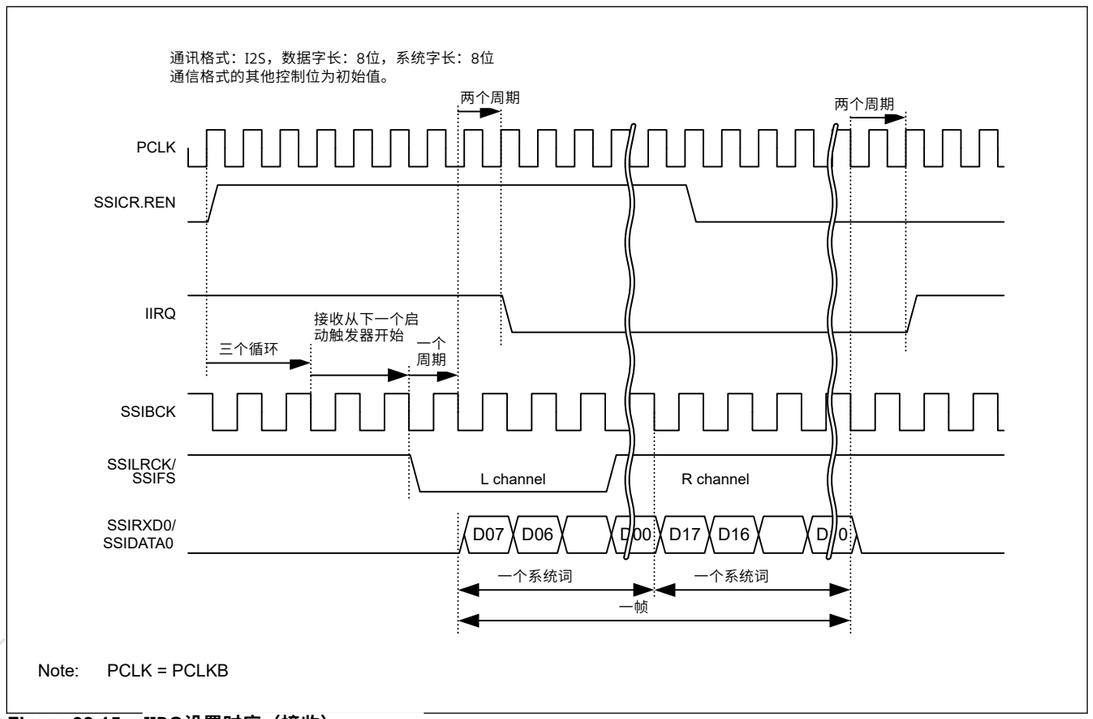


Figure 38.15 IIRQ设置时序（接收）

●接收器（接收专用）

[Clearing condition]

在启用接收时（SSICR.TEN=0和SSICR.REN=01，由SSILRCKSSIFS信号生成启动触发信号。

[Clearing timing]

1个SSIBCK周期+2个PCLKB周期在产生作为清除条件的启动触发之后。

[Setting condition]

当发送和接收被禁用时（SSICR.TEN=0和SSICR.REN=0），一帧的接收完成。

[Setting timing]

在作为设置条件的接收结束（在帧边界）之后的2个PCLKB周期。

●收发器（发送和接收）

[Clearing condition]

在使能发送和接收时（SSICR.TEN=1和SSICR.REN=1），发送帧的发送数据被写入SSIFTDR寄存器，并由SSILRCKSSIFS信号生成开始触发。

[Clearing timing]

1个SSIBCK周期+2个PCLKB周期在产生作为清除条件的启动触发之后。

[Setting condition]

当发送和接收被禁用时（SSICR.TEN=0和SSICR.REN=0），一帧的发送完成。

[Setting timing]

在作为设置条件的传输结束后（在帧边界处）的2个PCLKB周期。

ROIRQ flag (Receive Overflow Error Status Flag)

The ROIRQ flag is a status flag that indicates a receive overflow error. This flags is set by automatic determination but it must be cleared by register access. This flag indicates that received data is supplied at a higher rate than requested. Data is not transferred from the receive shift register to SSIFRDR where a receive overflow error is generated. For the procedure to recover from the overflow error, see section 38.8.6. Error Handling. This flag is not cleared by a receive FIFO data register reset (SSIFCR.RFRST).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.REN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition:

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 38.19)
2. 1 PCLKB cycle after writing 1 to SSICR.REN.*3

[Setting condition]
At completion of receiving new data while SSIFRDR is full.

[Setting timing]
3 cycles of PCLKB after reception is completed.

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.REN.

Note 3. After communication is enabled (by changing the value of SSICR.REN bit from 0 to 1), the reception error flags (RUIRQ and ROIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the reception error flags might be unable to be read.

ROIRQ标志（接收溢出错误状态标志）

ROIRQ标志是指示接收溢出错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。该标志表示接收到的数据以高于请求的速率提供。数据不会从接收移位寄存器传送到产生接收溢出错误的SSIFRDR。有关从溢出错误中恢复的过程，请参阅第38.8.6节。错误处理。该标志不会被接收FIFO数据寄存器复位(SSIFCR.RFRST)清除。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

1.从该位读取1后向该位写入0*2

2.启用通信（将SSICR.REN从0更改为1）。

[Clearing timing]

与上述清零条件对应的清零时机：

1.当从该位读取1后向该位写入0时（与图38.19中的时序相同）

2.向SSICR.REN写入1后的1个PCLKB周期。*3

[设置条件]在SSIFRDR已满时完成接收新数据时。

[设置时序]接收完成后的3个PCLKB周期。

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。

注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：●软件复位(SSIFCR.SSIRST=1)完成。●读1后，写0完成。●在向SSICR.REN写入1之后经过1个PCLKB周期。

注3.使能通信后（通过将SSICR.REN位的值从0更改为1），接收错误标志（SSISR寄存器中的RUIRQ和ROIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取接收错误标志的清除状态。

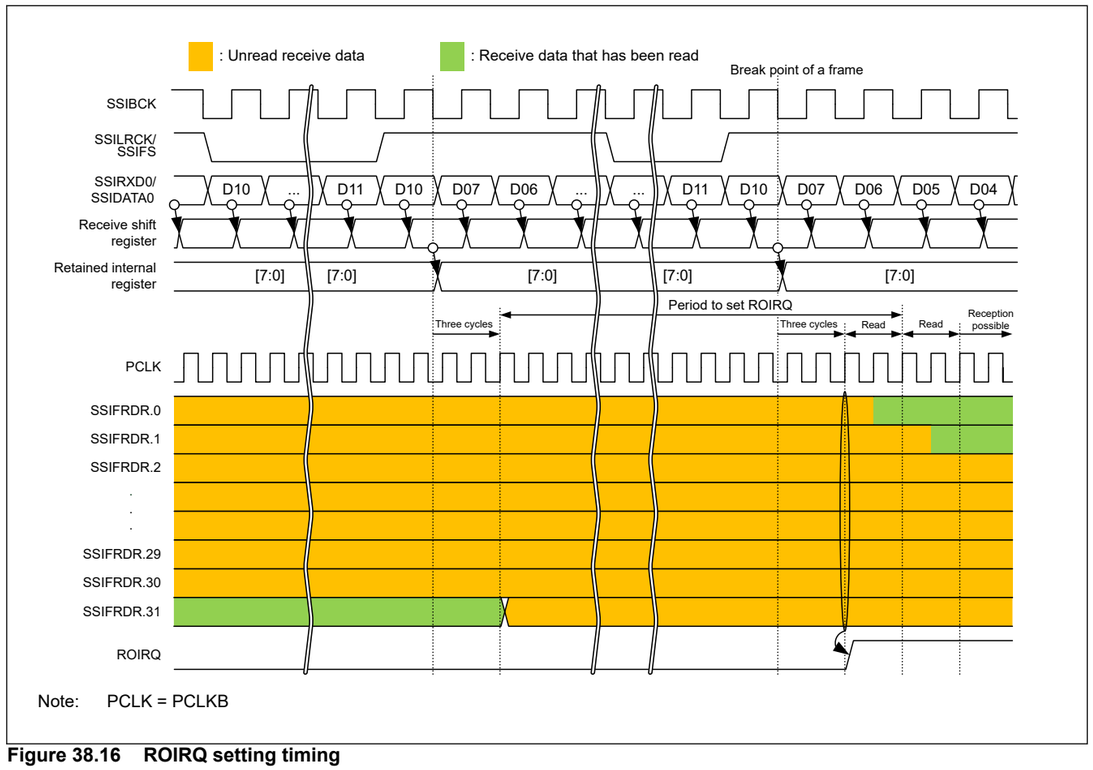


Figure 38.16 ROIRQ setting timing

RUIRQ flag (Receive Underflow Error Status Flag)

The RUIRQ flag is a status flag that indicates a receive underflow error. This flags is set by automatic determination but it must be cleared by register access. This flag indicates that SSIFRDR is read while it is empty. Data read from SSIFRDR where a receive underflow error is generated is invalid. See section 38.8.6. Error Handling for the error recovery procedure. This flag is not cleared by a receive FIFO data register reset (SSIFCR.RFRST). Note, however, that this flag is not set even if the SSIFRDR register is read while the receive FIFO data register is reset (by setting SSIFCR.RFRST to 1).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.REN from 0 to 1).

[Clearing timing]
Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 38.19)
2. 1 PCLKB cycle after writing 1 to SSICR.REN.*3

[Setting condition]

Reading from SSIFRDR while it is empty.

[Setting timing]

At completion of reading from SSIFRDR. See Figure 38.17.

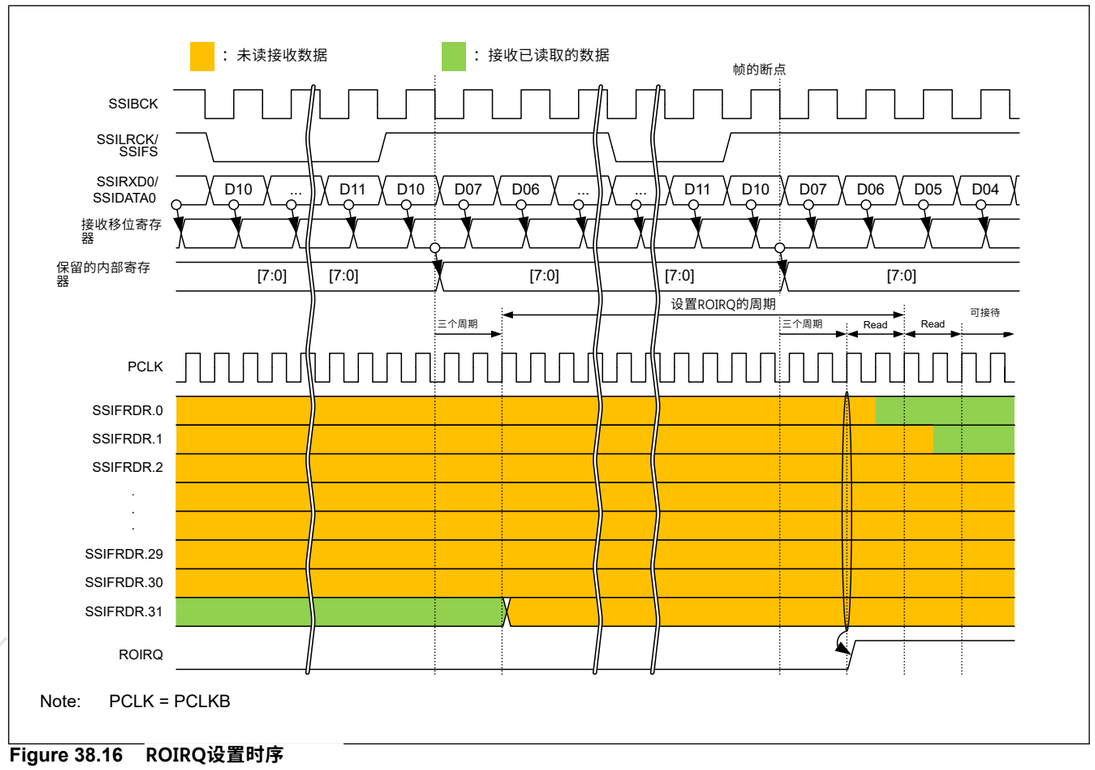


Figure 38.16 ROIRQ设置时序

RUIRQ标志（接收下溢错误状态标志）

RUIRQ标志是指示接收下溢错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。此标志指示SSIFRDR在为空时被读取。从产生接收下溢错误的SSIFRDR读取的数据无效。请参阅第38.8.6节。错误恢复过程的错误处理。该标志不会被接收FIFO数据寄存器复位(SSIFCR.RFRST)清除。但是请注意，即使在接收FIFO数据寄存器复位（通过将SSIFCR.RFRST设置为1）时读取SSIFRDR寄存器，该标志也不会设置。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

1.从该位读取1后向该位写入0*2

2.启用通信（将SSICR.REN从0更改为1）。

【清零时机】与上述清零条件对应的清零时机

1.当从该位读取1后向该位写入0时（与图38.19中的时序相同）

2.向SSICR.REN写入1后的1个PCLKB周期。*3

[Setting condition]

在SSIFRDR为空时读取。

[Setting timing]

从SSIFRDR读取完成时。请参见图38.17。

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.REN.

Note 3. After communication is enabled (by changing the value of SSICR.REN bit from 0 to 1), the reception error flags (RUIRQ and ROIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the reception error flags might be unable to be read.

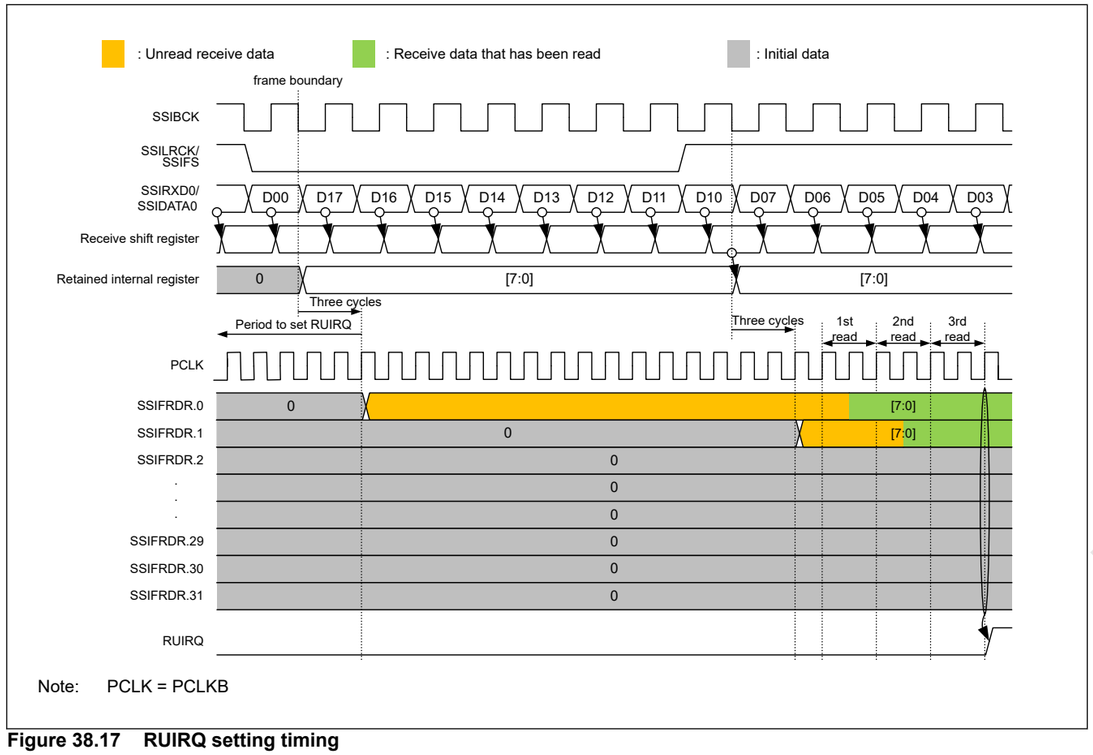


Figure 38.17 RUIRQ setting timing

TOIRQ flag (Transmit Overflow Error Status Flag)

The TOIRQ flag is a status flag that indicates a transmit overflow error. This flag is set by automatic determination but it must be cleared by register access. This flag indicates that an attempt has been made to write data to the SSIFTDR register when the register is full of data. The data writing that causes a transmit overflow is ignored. For the procedure to recover from the overflow error, see section 38.8.6. Error Handling. This flag is not cleared by a transmit FIFO data register reset (SSIFCR.TFRST).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.TEN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。

注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：●
完成软件复位(SSIFCR.SSIRST=1)。
- 读取1后，写入0完成。
- 在将1写入SSICR.REN后经过1个PCLKB周期。

注3.使能通信后（通过将SSICR.REN位的值从0更改为1），接收错误标志（SSISR寄存器中的RUIRQ和ROIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取接收错误标志的清除状态。

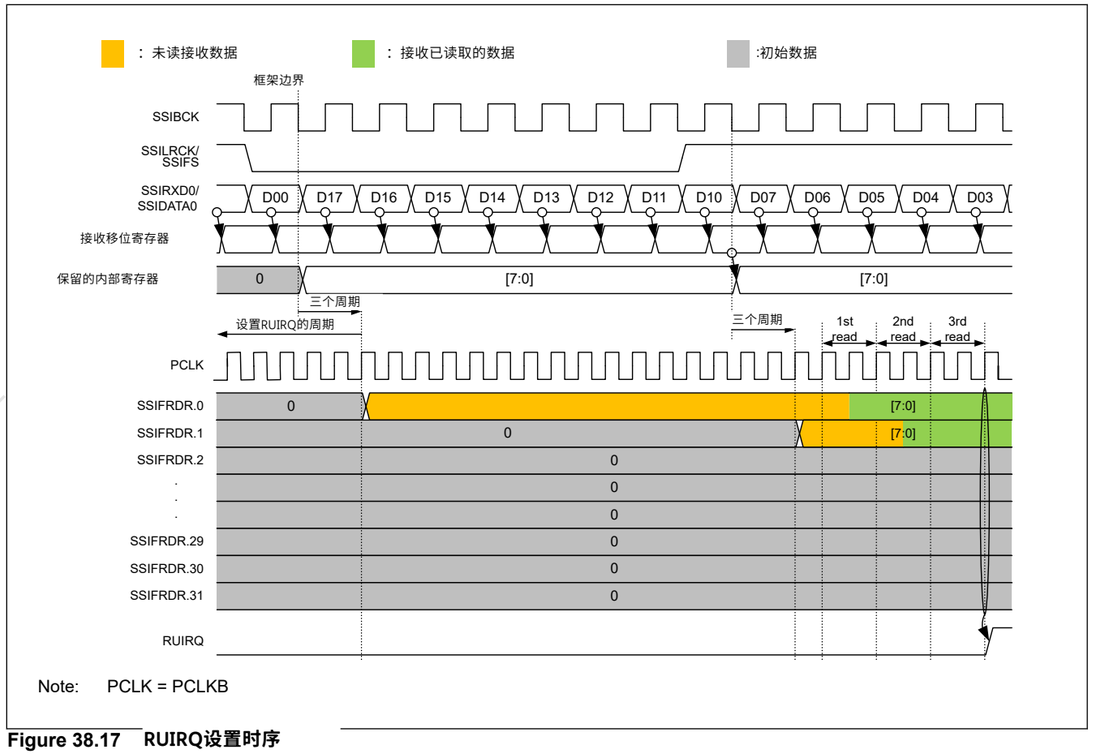


Figure 38.17 RUIRQ设置时序

TOIRQ标志（发送溢出错误状态标志）

TOIRQ标志是指示发送溢出错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。该标志表明当寄存器已满时尝试将数据写入SSIFTDR寄存器。导致发送溢出的数据写入将被忽略。有关从溢出错误中恢复的过程，请参阅第38.8.6节。错误处理。该标志不会被发送FIFO数据寄存器复位(SSIFCR.TFRST)清除。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

1.从该位读取1后向该位写入0*2

2.启用通信（将SSICR.TEN从0更改为1）。

[Clearing timing]

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1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 38.19)
2. 1 PCLKB cycle after writing 1 to SSICR.TEN.*3

[Setting condition]

An attempt was made to write data to the SSIFTDR register when the register is full of data.

[Setting timing]

At completion of writing to SSIFTDR. For details, see Figure 38.18.

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.TEN.

Note 3. After communication is enabled (by changing the value of SSICR.TEN bit from 0 to 1), the transmission error flags (TOIRQ and TUIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the transmission error flags might be unable to be read.

1.当从该位读取1后向该位写入0时（与图38.19中的时序相同）

2.向SSICR.TEN写入1后的1个PCLKB周期。*3

[Setting condition]

当寄存器已满时，尝试将数据写入SSIFTDR寄存器。

[Setting timing]

完成对SSIFTDR的写入。详见图38.18。

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。

注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：●软件复位(SSIFCR.SSIRST=1)完成。●读1后，写0完成。●在向SSICR.TEN写入1后经过1个PCLKB周期。

注3.使能通信后（通过将SSICR.TEN位的值从0更改为1），传输错误标志（SSISR寄存器中的TOIRQ和TUIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取传输错误标志的清除状态。

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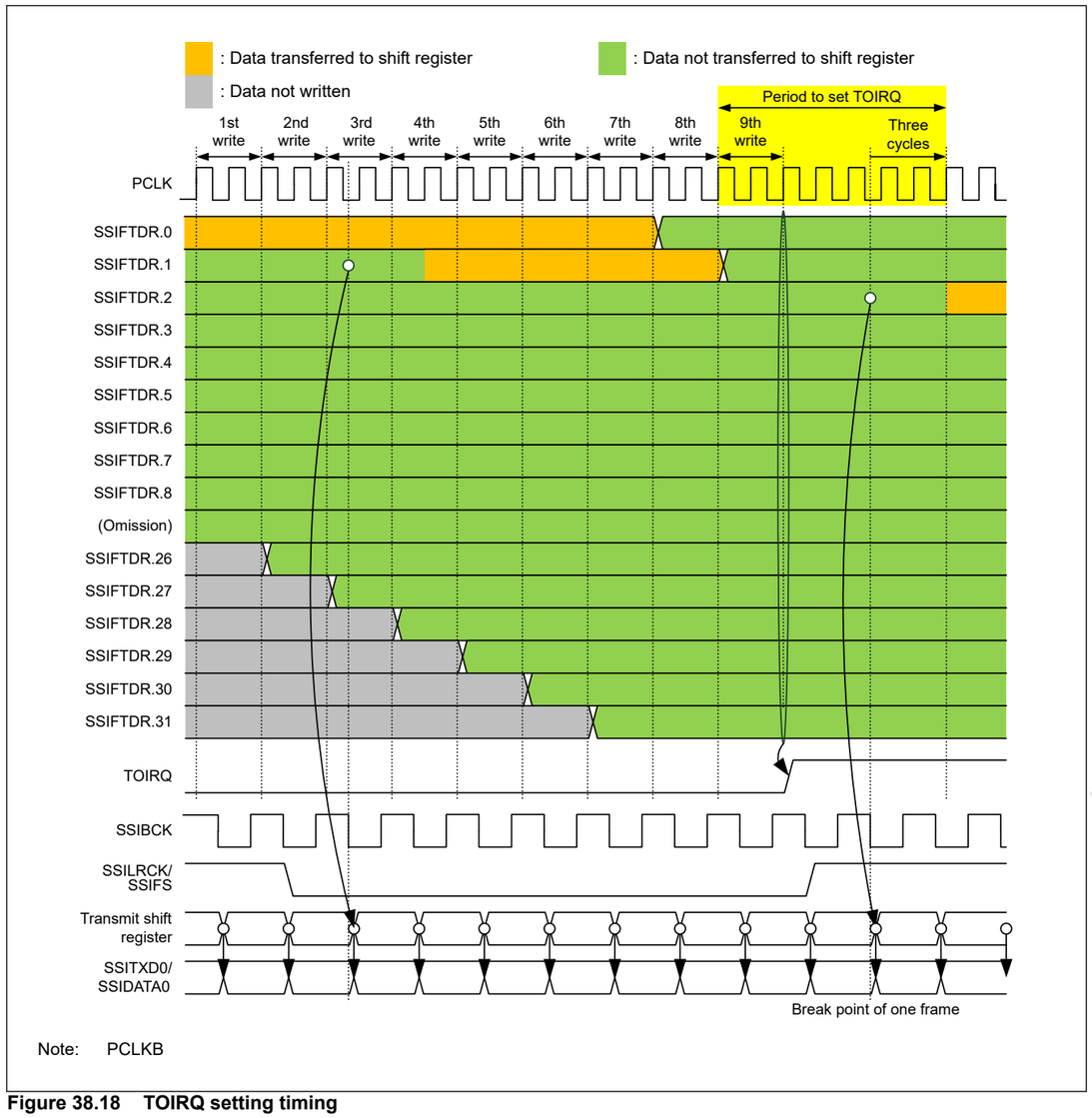


Figure 38.18 TOIRQ setting timing

TUIRQ flag (Transmit Underflow Error Status flag)

The TUIRQ flag is a status flag that indicates a transmit underflow error. This flag is set by automatic determination but it must be cleared by register access. This flag indicates that writing the serial data required for a frame to SSIFTDR did not catch up with transmission of the frame. Even if this flag is cleared after it has been set, the SSITXD0/SSIDATA0 output remains to be 0. To output the data written to the transmit FIFO data register (SSIFTDR) to the SSITXD0/SSIDATA0 pin, follow the communication stop procedure in Figure 38.56 and error-handling procedure in Figure 38.57. For the procedure to recover from an error, see section 38.8.6. Error Handling. This flag is not cleared by a reset of transmit FIFO data register (by the SSIFCR.TFRST signal).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

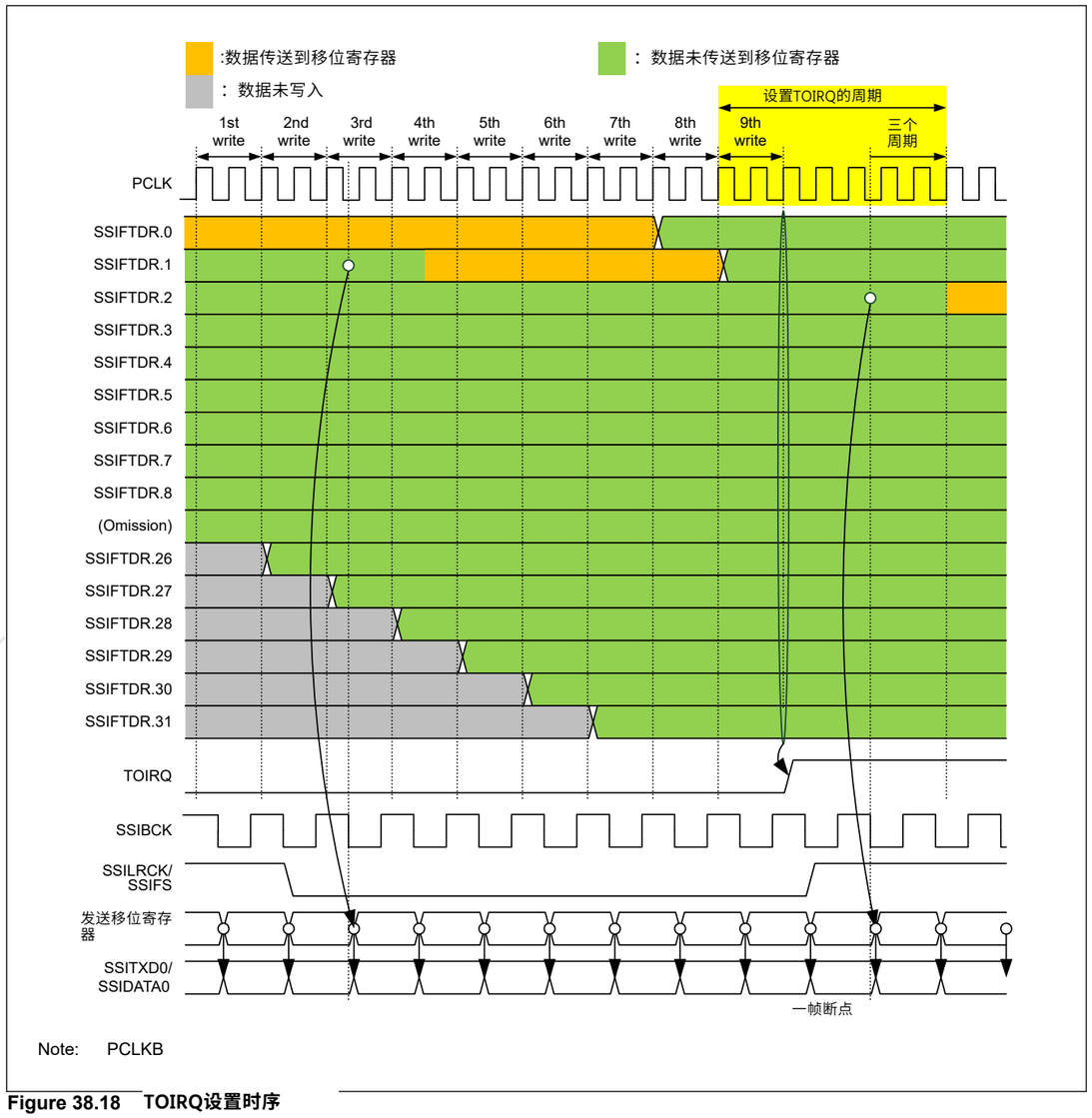


Figure 38.18 TOIRQ设置时序

TUIRQ标志（发送下溢错误状态标志）

TUIRQ标志是指示发送下溢错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。该标志表示将帧所需的串行数据写入SSIFTDR没有赶上帧的传输。即使该标志在设置后被清除，SSITXD0SSIDATA0输出仍保持为0。要将写入发送FIFO数据寄存器(SSIFTDR)的数据输出到SSITXD0SSIDATA0引脚，请遵循图38.56中的通信停止程序并图38.57中的错误处理过程。有关从错误中恢复的过程，请参阅第38.8.6节。错误处理。该标志不会通过发送FIFO数据寄存器的复位（通过SSIFCR.TFRST信号）清除。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.TEN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit
2. 1 PCLKB cycle after writing 1 to SSICR.TEN.*3

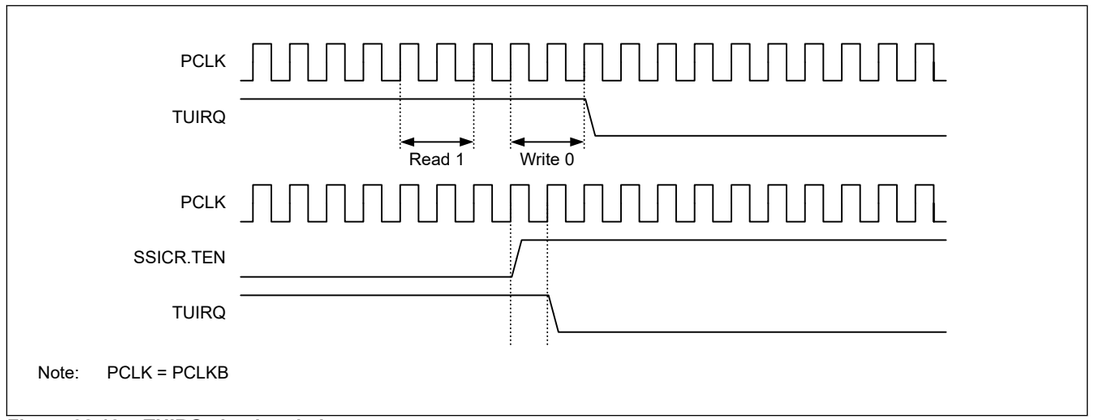


Figure 38.19 TUIRQ clearing timing

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.TEN.

Note 3. After communication is enabled (by changing the value of SSICR.TEN bit from 0 to 1), the transmission error flags (TOIRQ and TUIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the transmission error flags might be unable to be read.

[Setting condition]

When communication continues over a frame boundary, the transmit data required for the next frame has not been written to SSIFTDR. For details, see Figure 38.20 and Figure 38.21.

[Setting timing]

3 PCLKB cycles after the frame boundary. For details, see Figure 38.20.

1.从该位读取1后向该位写入0*2

2.启用通信（将SSICR.TEN从0更改为1）。

[Clearing timing]

与上述清零条件对应的清零时机

1.从该位读取1后向该位写入0

2.向SSICR.TEN写入1后的1个PCLKB周期。*3

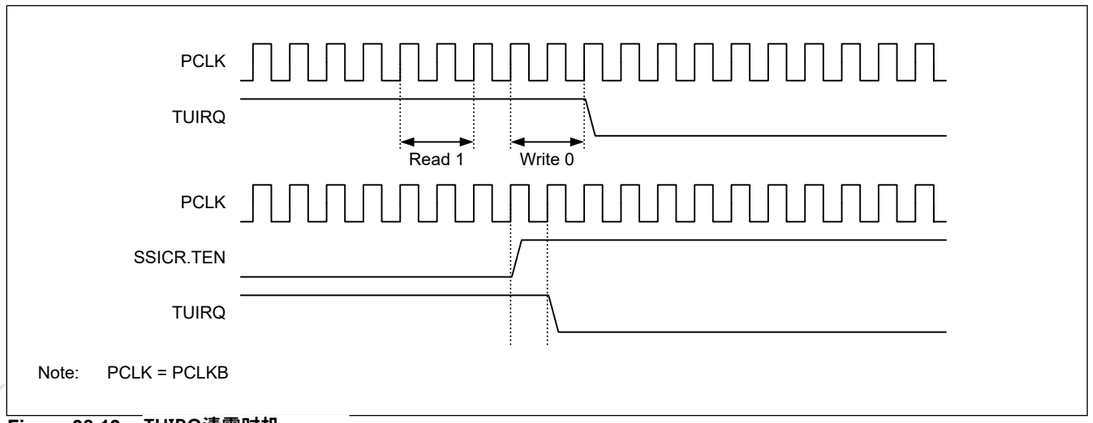


Figure 38.19 TUIRQ清零时机

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。

注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：●
- 完成软件复位(SSIFCR.SSIRST=1)。
- 读取1后，写入0完成。
- 在将1写入SSICR.TEN之后经过1个PCLKB周期。

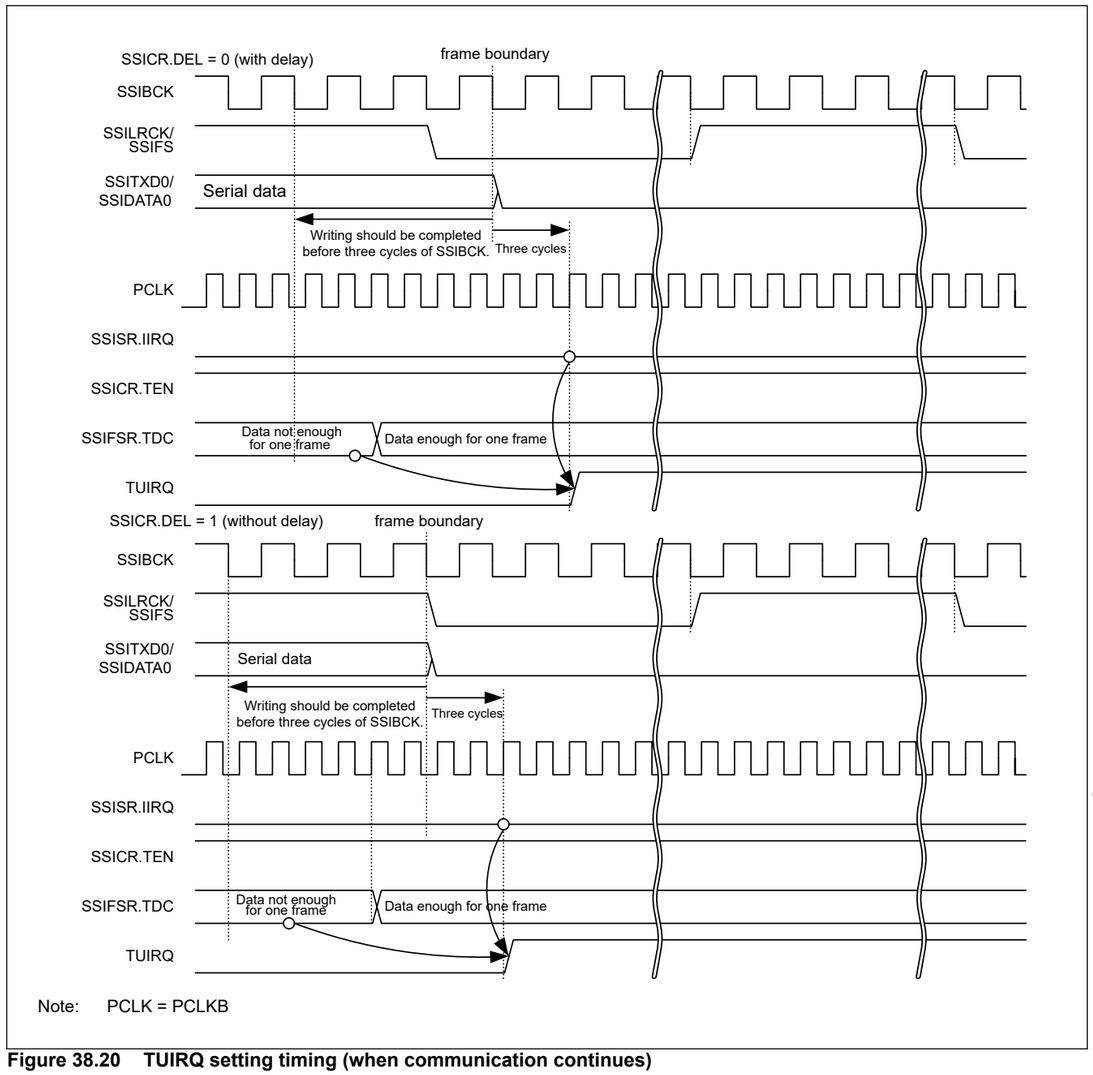
注3.使能通信后（通过将SSICR.TEN位的值从0更改为1），传输错误标志（SSISR寄存器中的TOIRQ和TUIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取传输错误标志的清除状态。

[Setting condition]

当通信继续通过帧边界时，下一帧所需的传输数据尚未写入SSIFTDR。详见图38.20和图38.21。

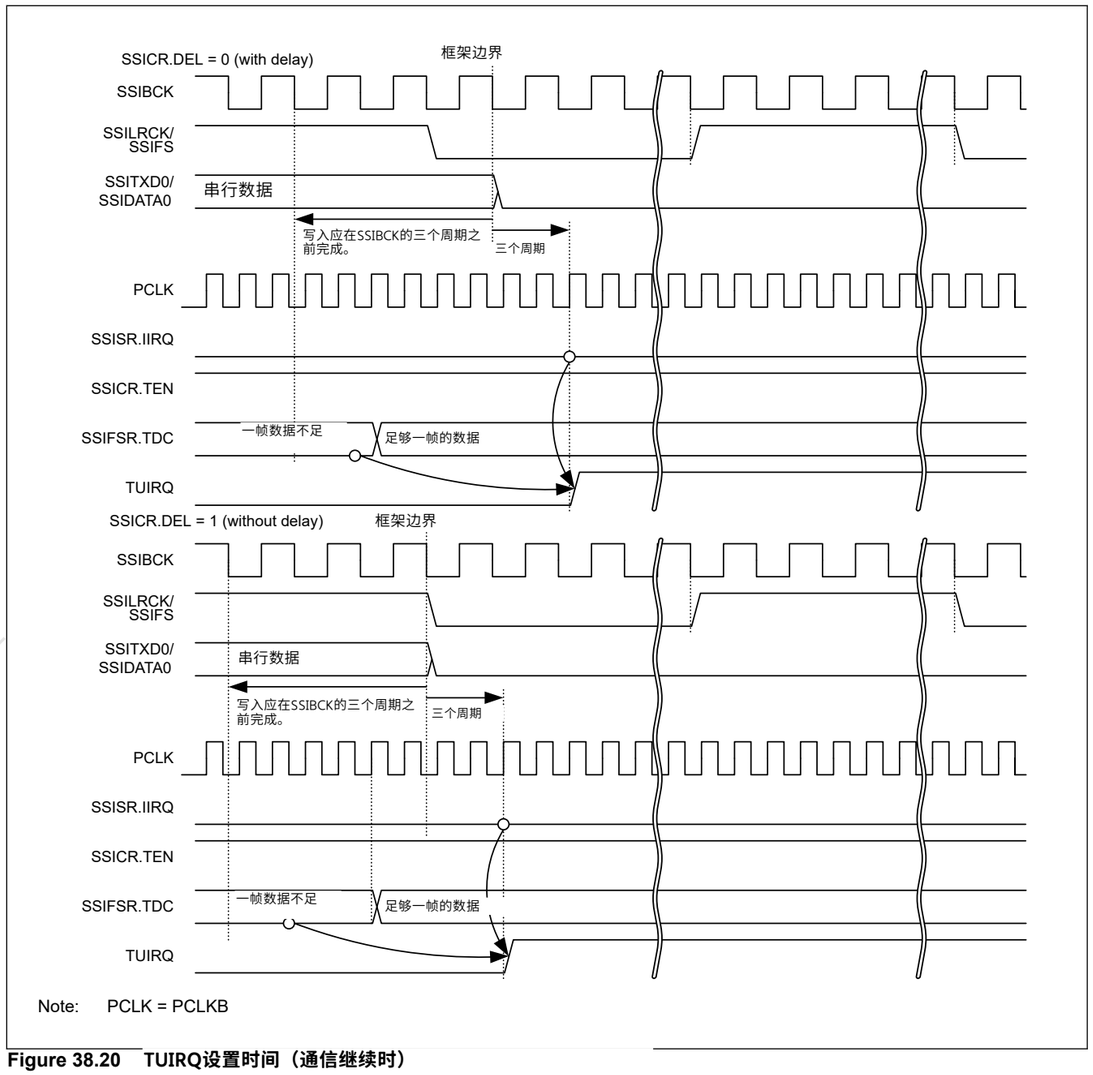
[Setting timing]

帧边界后3个PCLKB周期。详见图38.20。



Note: PCLK = PCLKB

Figure 38.20 TUIRQ setting timing (when communication continues)



Note: PCLK = PCLKB

Figure 38.20 TUIRQ设置时间（通信继续时）

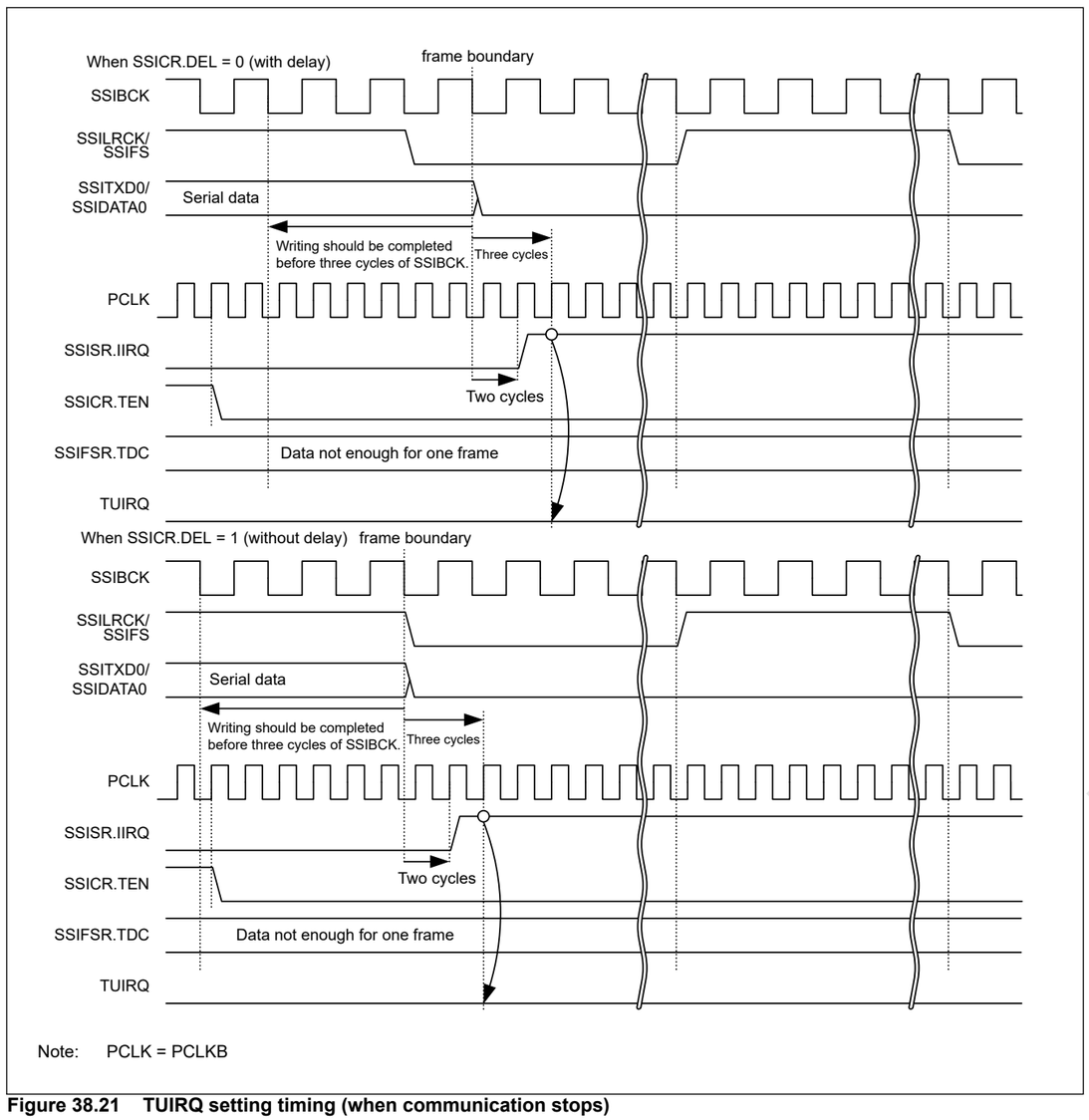


Figure 38.21 TUIRQ setting timing (when communication stops)

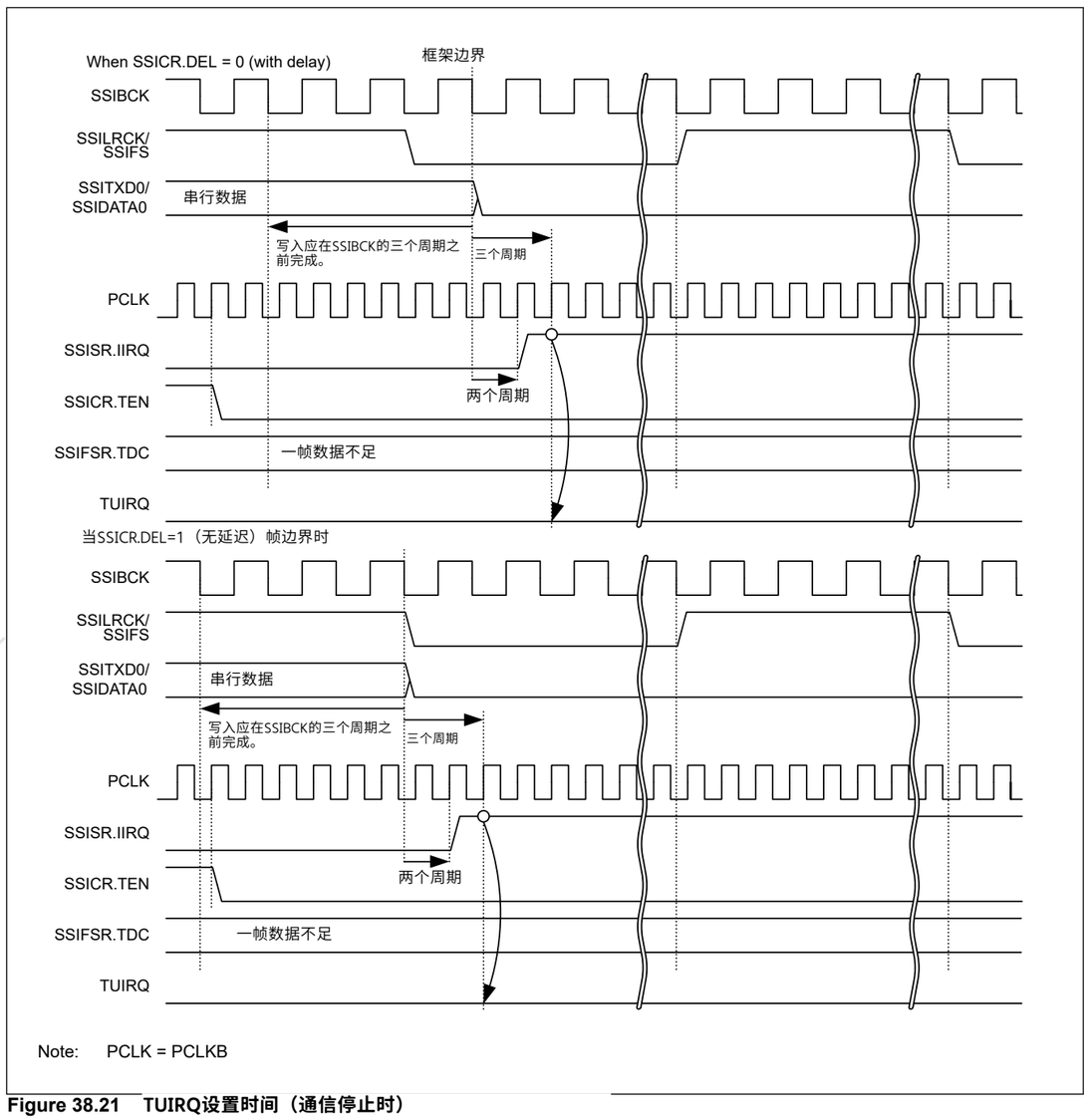


Figure 38.21 TUIRQ设置时间（通信停止时）

38.4.3 SSIFCR : FIFO Control Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFRST	Receive FIFO Data Register Reset*1 0: Clears a receive data FIFO reset condition 1: Sets a receive data FIFO reset condition	R/W
1	TFRST	Transmit FIFO Data Register Reset*1 0: Clears a transmit data FIFO reset condition 1: Sets a transmit data FIFO reset condition	R/W
2	RIE	Receive Data Full Interrupt Output Enable 0: Disables receive data full interrupts 1: Enables receive data full interrupts	R/W
3	TIE	Transmit Data Empty Interrupt Output Enable 0: Disables transmit data empty interrupts 1: Enables transmit data empty interrupts	R/W
10:4	—	These bits are read as 0. The write value should be 0.	R/W
11	BSW	Byte Swap Enable*1 0: Disables byte swap 1: Enables byte swap	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W
16	SSIRST	Software Reset 0: Clears a software reset condition 1: Sets a software reset condition	R/W
30:17	—	These bits are read as 0. The write value should be 0.	R/W
31	AUCKE	AUDIO_MCK Enable in Mastermode Communication*1 0: Disables supply of AUDIO_MCK 1: Enables supply of AUDIO_MCK	R/W

Note 1. Writing to these bits while SSIE is in a communication state (SSISR.IIRQ = 0) is prohibited. If the value of these bits is changed by rewriting, subsequent operation is unpredictable.

This register sets a software reset, byte swap, and enable/disable of interrupt requests.

RFRST bit (Receive FIFO Data Register Reset)

The RFRST bit sets a software reset of the receive FIFO data register (SSIFRDR). Writing 1 to this bit initializes the internal state related to SSIFRDR. The register bits subject to the software reset triggered by this bit are indicated by shading in Table 38.5. Because this bit is not automatically cleared after it has been set, write 0 to this bit to release the register bits from the software reset. After writing 0 to this bit, be sure to check that this bit is 0 before starting the next procedural step.

This bit is subject to the software reset by the SSIRST bit. Because the software reset by the SSIRST bit has priority over the reset by this bit, setting this bit is ignored when the SSIRST bit is set.

38.4.3 SSIFCR:FIFO控制寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RFRST	接收FIFO数据寄存器复位*1 0：清除接收数据FIFO复位条件1：设置接收数据FIFO复位条件	R/W
1	TFRST	发送FIFO数据寄存器复位*1 0：清除发送数据FIFO复位条件1：设置发送数据FIFO复位条件	R/W
2	RIE	接收数据满中断输出使能 0：禁止接收数据满中断1：使能接收数据满中断	R/W
3	TIE	发送数据空中断输出使能 0：禁用传输数据空中断1：启用传输数据空中断	R/W
10:4	—	这些位被读取为0。写入值应为0。	R/W
11	BSW	字节交换启用*1 0：禁用字节交换1：启用字节交换	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W
16	SSIRST	软件复位 0：清除软件复位条件1：设置软件复位条件	R/W
30:17	—	这些位被读取为0。写入值应为0。	R/W
31	AUCKE	AUDIO_MCK在主模式通信中启用*1 0：禁用AUDIO_MCK供应1：启用AUDIO_MCK供应	R/W

注1.禁止在SSIE处于通信状态(SSISR.IIRQ=0)时写入这些位。如果这些位的值通过重写而改变，后续的操作是不可预知的。

该寄存器设置软件复位、字节交换和中断请求的启用禁用。

RFRST位（接收FIFO数据寄存器复位）

RFRST位设置接收FIFO数据寄存器(SSIFRDR)的软件复位。向该位写入1初始化与SSIFRDR相关的内部状态。受该位触发的软件复位的寄存器位在表38.5中用阴影表示。由于该位在被设置后不会自动清零，因此向该位写入0以从软件复位中释放寄存器位。向该位写入0后，请务必在开始下一个程序步骤之前检查该位是否为0。

该位受SSIRST位软件复位的影响。由于SSIRST位的软件复位优先于该位的复位，所以当SSIRST位置位时，该位的设置将被忽略。

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Table 38.5 Bits subject to software reset by the RFRST bit

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

TFRST bit (Transmit FIFO Data Register Reset)

The TFRST bit sets a software reset of the transmit FIFO data register (SSIFTDR). Writing 1 to this bit initializes the internal state related to SSIFTDR. The register bits subject to the software reset triggered by this bit are indicated by shading in Table 38.6. Because this bit is not automatically cleared after it has been set, write 0 to this bit to release the register bits from the software reset. After writing 0 to this bit, be sure to check that this bit is 0 before starting the next procedural step.

This bit is subject to the software reset by the SSIRST bit. Because the software reset by the SSIRST bit has priority over the reset by this bit, setting this bit is ignored when the SSIRST bit is set.

Table 38.6 Bits subject to software reset by the TFRST bit (1 of 2)

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 38.5 受RFRST位软件复位的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

TFRST位（发送FIFO数据寄存器复位）

TFRST位设置发送FIFO数据寄存器(SSIFTDR)的软件复位。向该位写入1初始化与SSIFTDR相关的内部状态。受该位触发的软件复位的寄存器位在表38.6中用阴影表示。由于该位在被设置后不会自动清零，因此向该位写入0以从软件复位中释放寄存器位。向该位写入0后，请务必在开始下一个程序步骤之前检查该位是否为0。

该位受SSIRST位软件复位的影响。由于SSIRST位的软件复位优先于该位的复位，所以当SSIRST位置位时，该位的设置将被忽略。

Table 38.6 受TFRST位软件复位的位（2个中的1个）

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

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Table 38.6 Bits subject to software reset by the TFRST bit (2 of 2)

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

RIE bit (Receive Data Full Interrupt Output Enable)

The RIE bit enables/disables output of receive data full interrupts. Use a receive data full interrupt as an interrupt to trigger data reading from the receive FIFO data register. Write 1 to this bit after specifying the setting condition for receive data full interrupt (by using the SSISCR.RDFS bit). Figure 38.22 shows the timing of generating the receive data full interrupt.

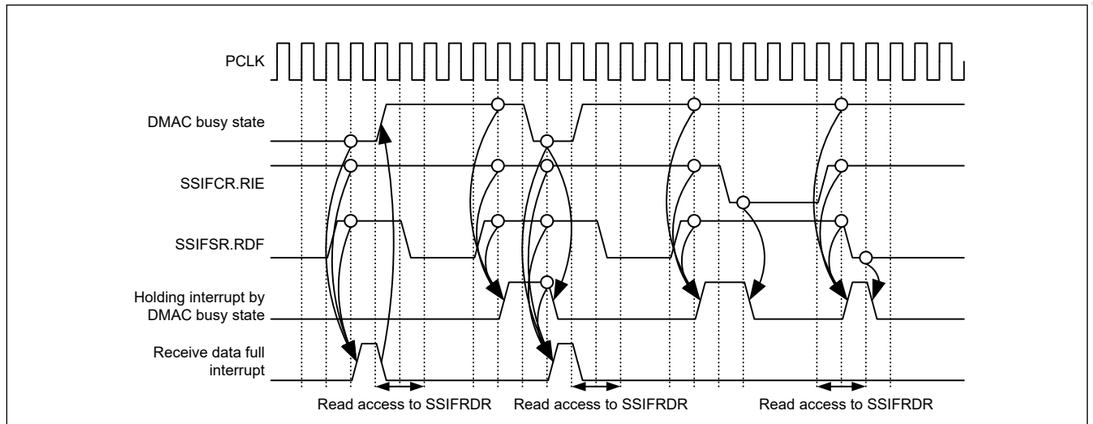


Figure 38.22 Timing of receive data full interrupt

TIE bit (Transmit Data Empty Interrupt Output Enable)

The TIE bit enables/disables output of transmit data empty interrupts. Use a transmit data empty interrupt as an interrupt to trigger data writing to the transmit FIFO data register. Write 1 to this bit after specifying the setting condition for transmit data empty interrupt (by using the SSISCR.TDES bit). Figure 38.23 shows the timing of generating the transmit data empty interrupt.

Table 38.6 受TFRST位软件复位的位（2个中的2个）

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

RIE位（接收数据满中断输出使能）

RIE位启用禁用接收数据完整中断的输出。使用接收数据满中断作为中断来触发从接收FIFO数据寄存器读取数据。指定接收数据满中断的设置条件后（通过使用SISSCR.RDFS位）向该位写入1。图38.22显示了产生接收数据满中断的时序。

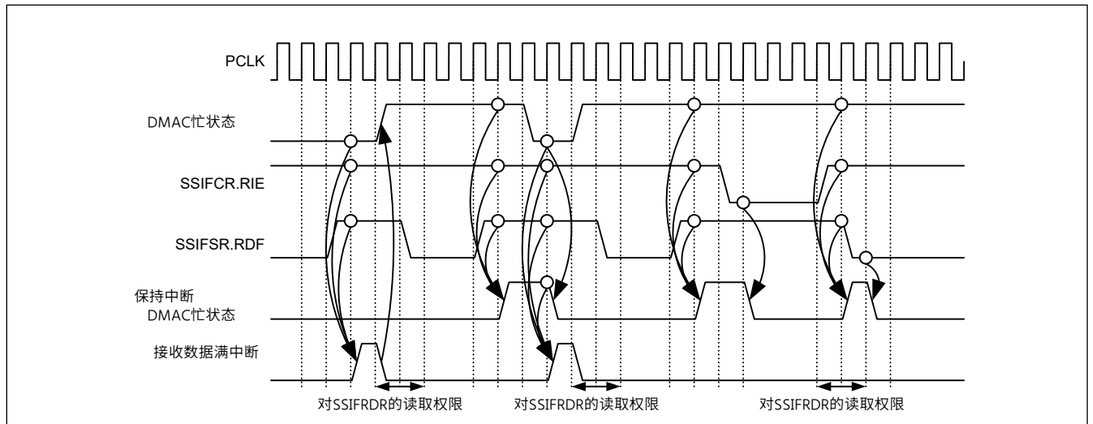


Figure 38.22 接收数据满中断的时序

TIE位（发送数据空中断输出使能）

TIE位使能禁用发送数据空中断的输出。使用发送数据空中断作为中断来触发数据写入发送FIFO数据寄存器。在指定发送数据空中断的设置条件后（通过使用SISSCR.TDES位）向该位写入1。图38.23显示了产生发送数据空中断的时序。

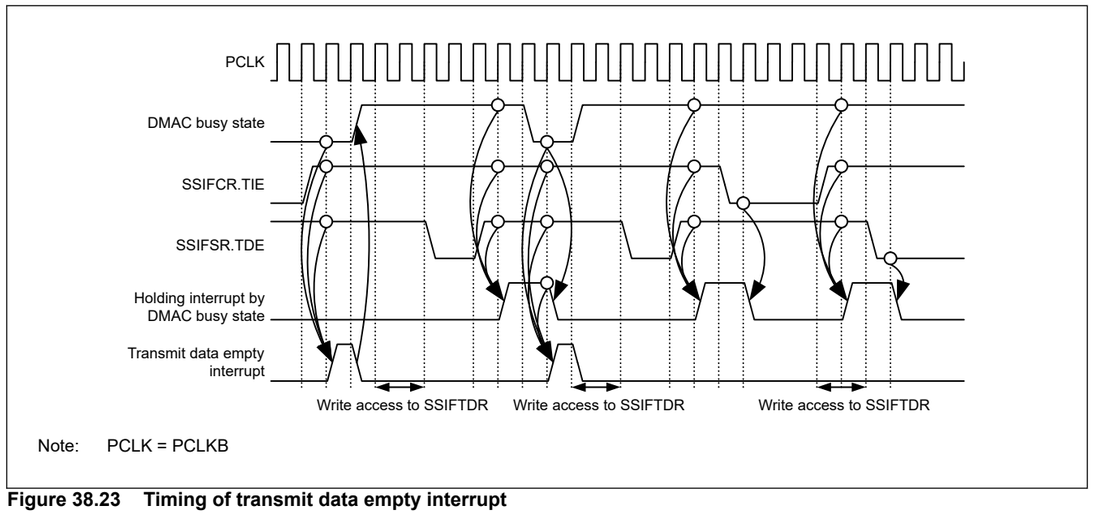


Figure 38.23 Timing of transmit data empty interrupt

BSW bit (Byte Swap Enable)

The BSW bit enables/disables byte swap of register access for the transmit FIFO data register (SSIFTDR) and the receive FIFO data register (SSIFRDR). This bit is valid only with 16-bit access or 32-bit access to SSIFTDR and SSIFRDR. For details, see Figure 38.24.

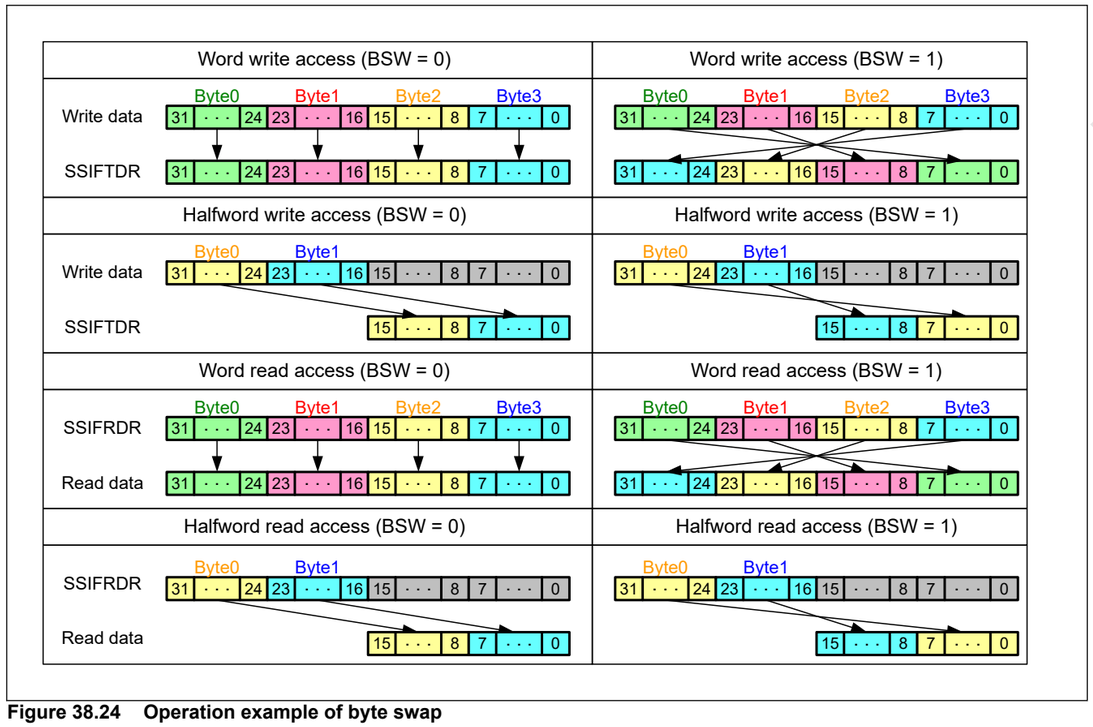


Figure 38.24 Operation example of byte swap

SSIRST bit (Software Reset)

The SSIRST bit sets a software reset of SSIE. Writing 1 to this bit initializes the internal state of SSIE. The register bits subject to the software reset triggered by this bit are indicated by shading in Table 38.7. Because this bit is not automatically

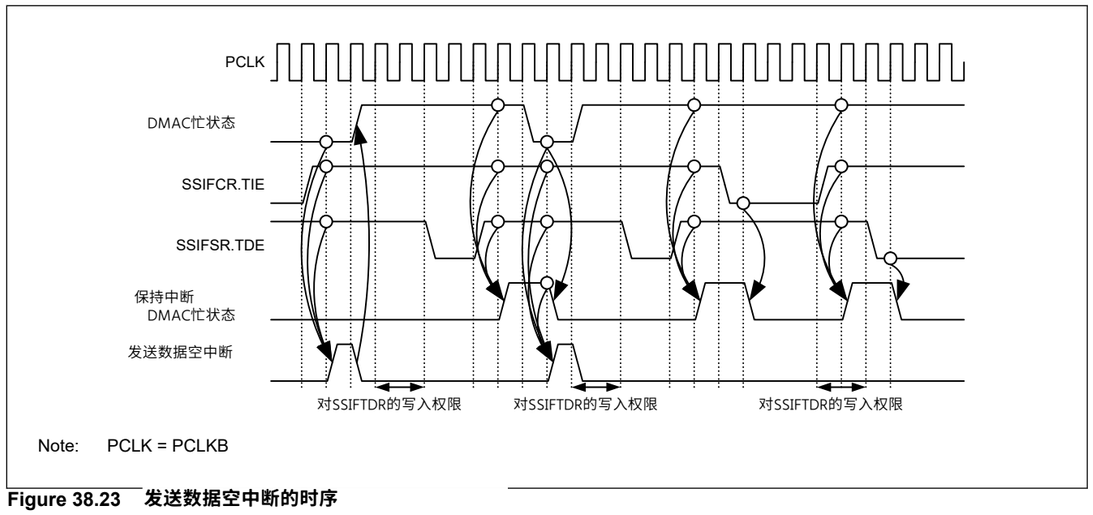


Figure 38.23 发送数据空中断的时序

BSW位（字节交换使能）

BSW位启用禁用发送FIFO数据寄存器(SSIFTDR)和接收FIFO数据寄存器(SSIFRDR)的寄存器访问字节交换。该位仅对SSIFTDR和SSIFRDR的16位访问或32位访问有效。详见图38.24。

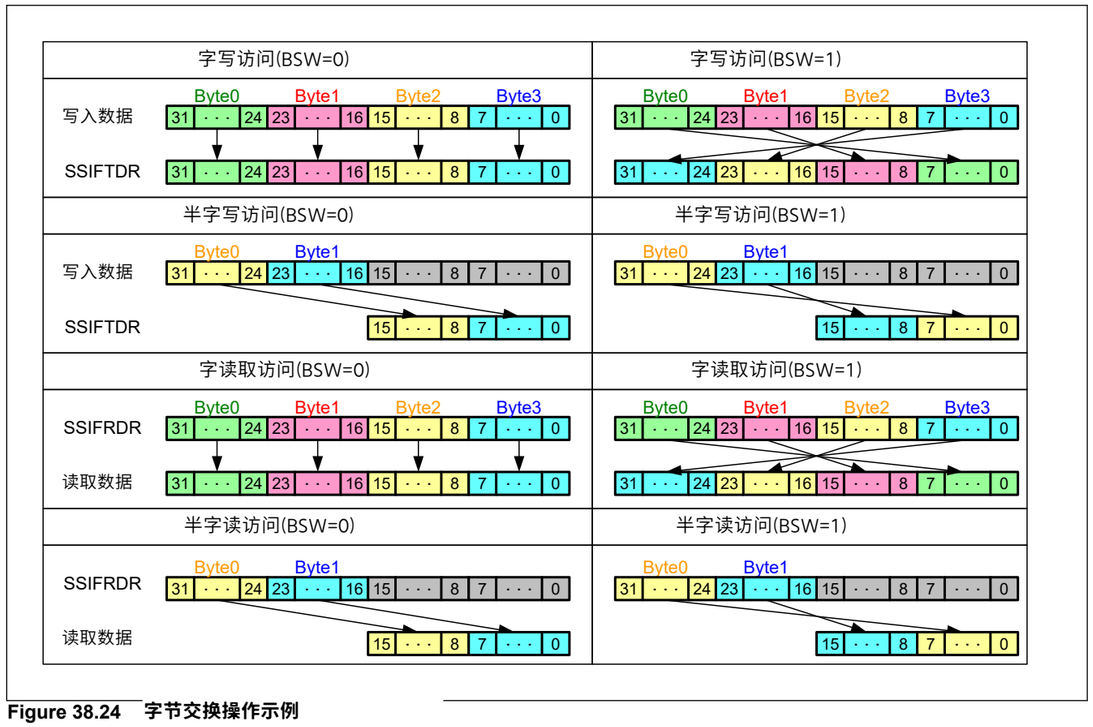


Figure 38.24 字节交换操作示例

SSIRST bit (Software Reset)

SSIRST位设置SSIE的软件复位。向该位写入1初始化SSIE的内部状态。受该位触发的软件复位的寄存器位在表38.7中用阴影表示。因为这个位不是自动的

cleared after it has been set, write 0 to this bit to release the register bits from the software reset. After writing 0 to this bit, be sure to check that this bit is 0 before starting the next procedural step.

To stop communication of SSIE immediately, after turning off the peripheral functions, write 1 to this bit. Initialization by a software reset is performed without any relation with the bit clock.

Table 38.7 Bits subject to software reset by the SSIRST bit

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

AUCKE bit (AUDIO_MCK Enable in Mastermode Communication)

The AUCKE bit enables/disables supply to AUDIO_MCK while in master-mode communication (MST = 1).

Changing the value of this bit must be performed only after specifying the settings related to AUDIO_MCK (by using the CKS, MST, BCKP, and CKDV bits in the SSICR register).

置位后清零，向该位写入0以从软件复位中释放寄存器位。向该位写入0后，请务必在开始下一个程序步骤之前检查该位是否为0。

要立即停止SSIE通信，请在关闭外围功能后，向该位写入1。通过软件复位进行的初始化与位时钟没有任何关系。

Table 38.7 受SSIRST位软件复位的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

AUCKE位（在主模式通信中启用AUDIO_MCK）

在主模式通信(MST=1)时，AUCKE位启用禁用对AUDIO_MCK的供电。

只有在指定与AUDIO_MCK相关的设置后才能更改该位的值（通过使用SSICR寄存器中的CKS、MST、BCKP和CKDV位）。

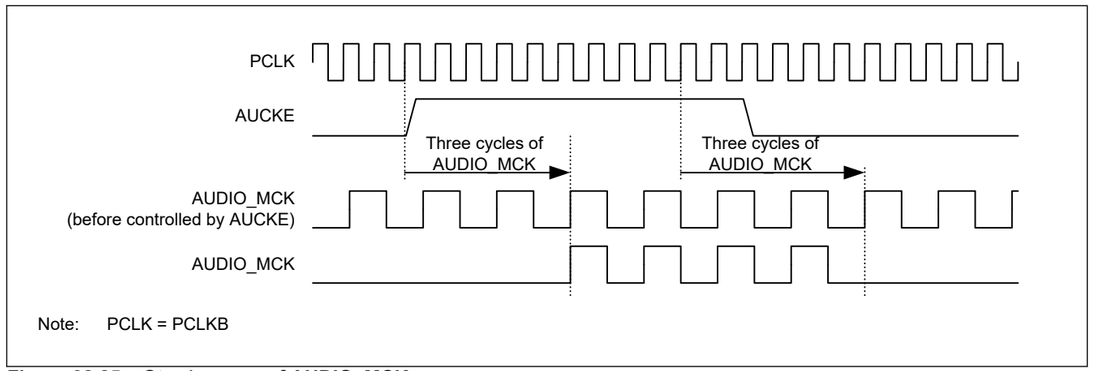


Figure 38.25 Stop/resume of AUDIO_MCK

Note: In slave-mode communication (SSICR.MST = 0), SSIE needs supply of SSIBCK. To stop BCK on the master side, make sure that SSIE is in the idle state (SSISR.IIRQ = 1). If BCK is stopped before SSIE becomes idle, take the procedure to start communication in Figure 38.52 or wait for an idle state by taking the procedure to resume communication in Figure 38.58.

In master-mode communication (SSICR.MST = 1), SSIE operates with the audio clock (AUDIO_MCK). To stop SSIE completely, make sure that SSIE is in the idle state (SSISR.IIRQ = 1) and then write 0 to SSIFCR.ADCKE. If 0 is written to SSIFCR.ADCKE before SSIE becomes idle, take the procedure to start communication in Figure 38.52.

Figure 38.26 and Figure 38.27 show the timings of signal operation in the period from setting this bit to 1 to the output to the SSIBCK pin.

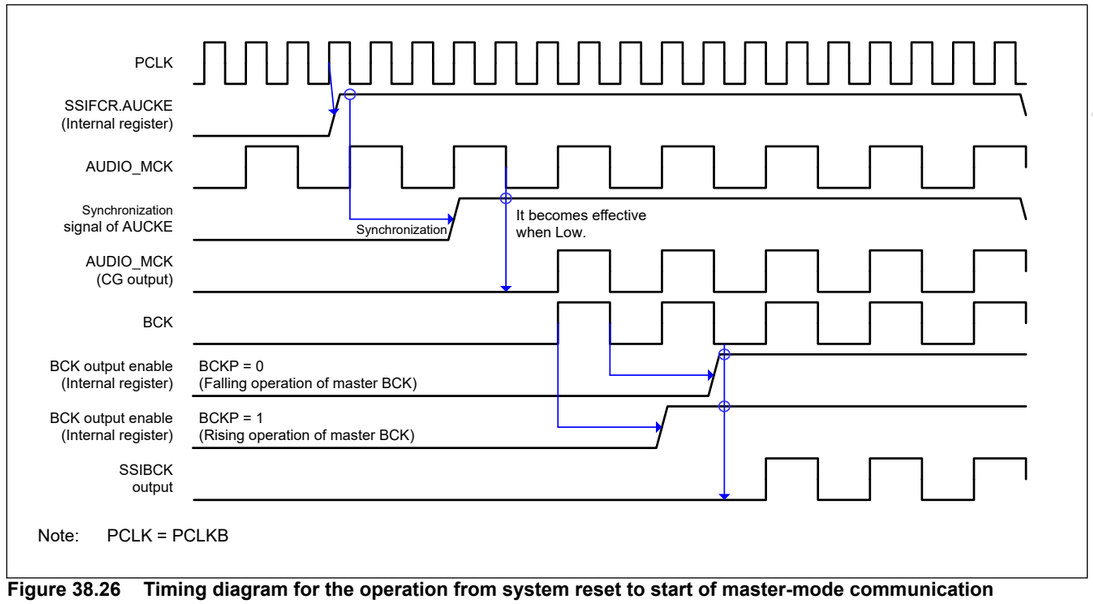


Figure 38.26 Timing diagram for the operation from system reset to start of master-mode communication

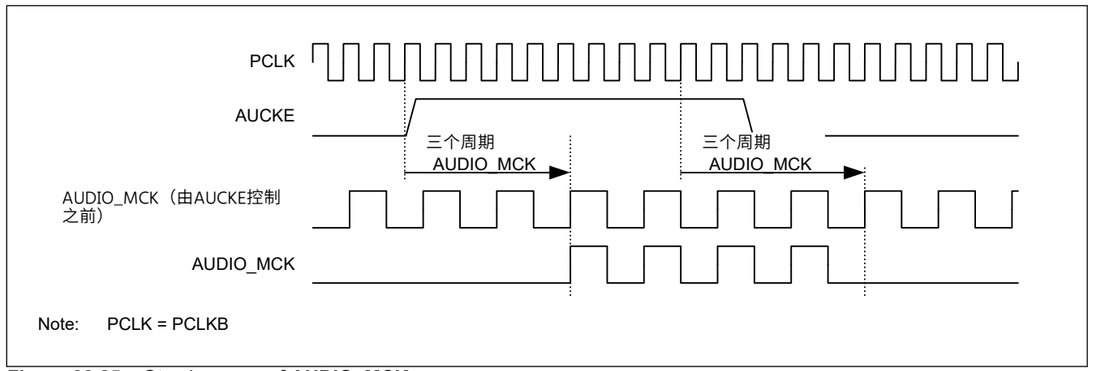


Figure 38.25 Stop/resume of AUDIO_MCK

Note: 在从模式通信(SSICR.MST=0)中，SSIE需要提供SSIBCK。要在主设备端停止BCK，请确保SSIE处于空闲状态(SSISR.IIRQ=1)。如果BCK在SSIE变为空闲之前停止，则按照图38.52中的程序开始通信，或者按照图38.58中的程序恢复通信等待空闲状态。

在主模式通信(SSICR.MST=1)中，SSIE使用音频时钟(AUDIO_MCK)运行。要完全停止SSIE，请确保SSIE处于空闲状态(SSISR.IIRQ=1)，然后将0写入SSIFCR.ADCKE。如果在SSIE空闲之前将0写入SSIFCR.ADCKE，则按照图38.52中的过程开始通信。

图38.26和图38.27显示了从将该位设置为1到输出到SSIBCK引脚期间的信号操作时序。

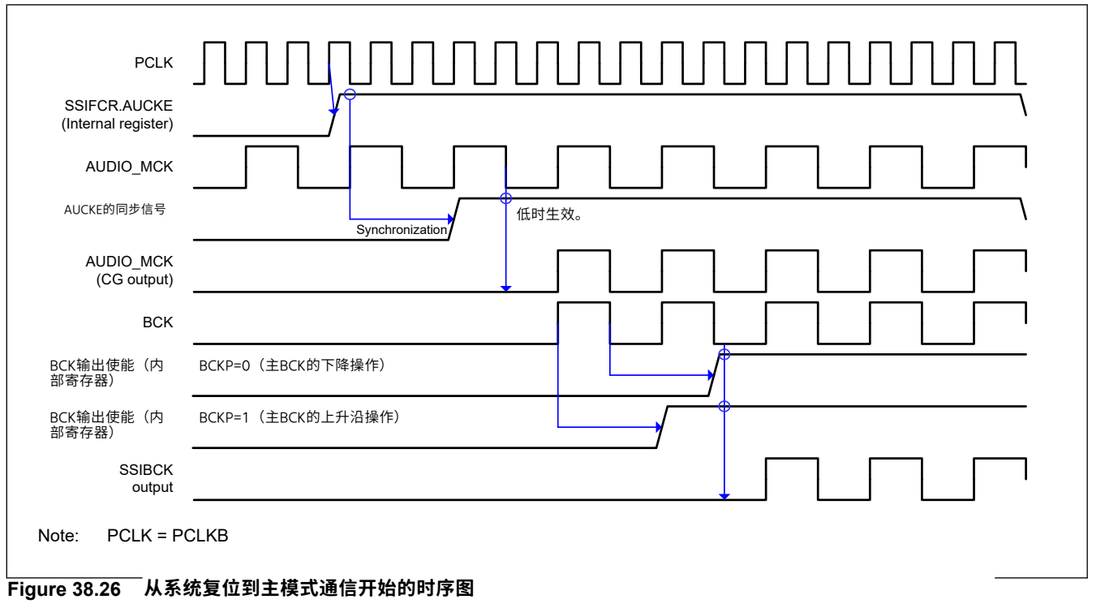


Figure 38.26 从系统复位到主模式通信开始的时序图

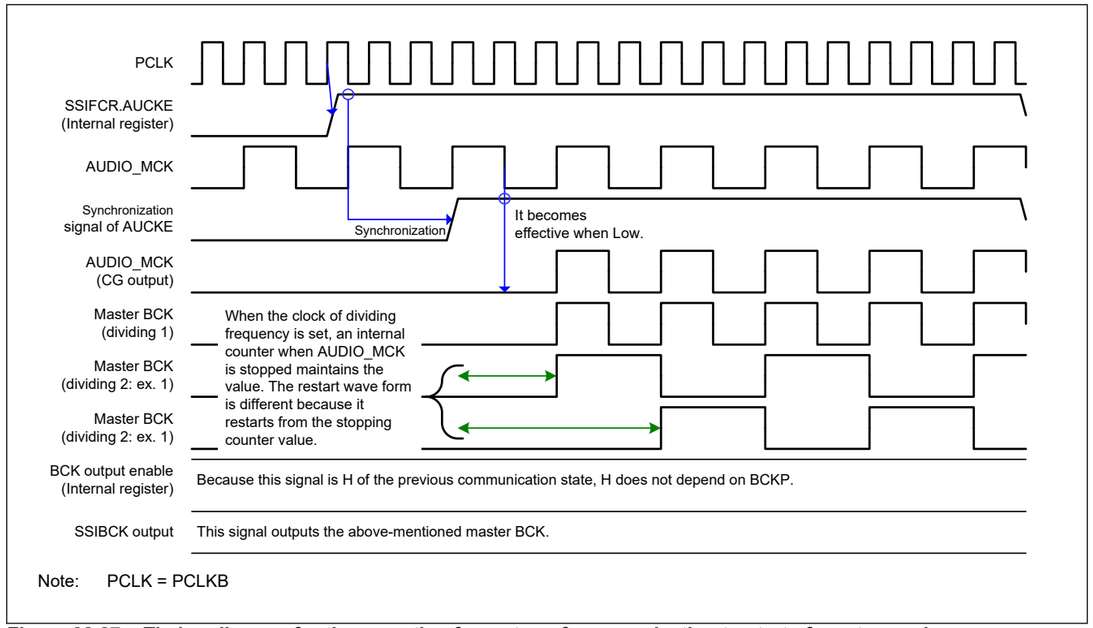


Figure 38.27 Timing diagram for the operation from stop of communication to start of master-mode communication

Note: If the supply of AUDIO_MCK stops, the value of the SSIBCK pin is held. Therefore, the SSIBCK signal might stop in the H (high level) state.

38.4.4 SSIFSR : FIFO Status Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RDF	Receive Data Full Flag 0: The size of received data in SSIFRDR is not more than the value of SSISCR.RDFS. 1: The size of received data in SSIFRDR is not less than the value of SSISCR.RDFS plus one.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
13:8	RDC[5:0]	Number of Receive FIFO Data Indication Flag Number of receive FIFO data indication flag	R
15:14	—	These bits are read as 0. The write value should be 0.	R/W

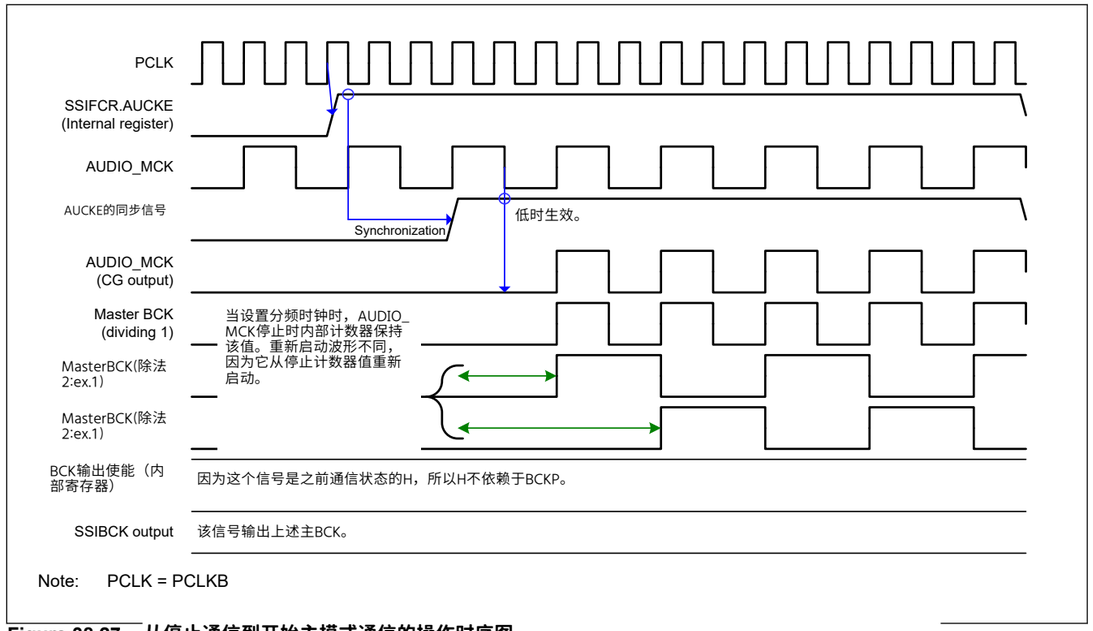


Figure 38.27 从停止通信到开始主模式通信的操作时序图

Note: 如果停止提供AUDIO_MCK，则保持SSIBCK引脚的值。因此，SSIBCK信号可能会停止在H（高电平）状态。

38.4.4 SSIFSR:FIFO状态寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	RDF	接收数据满标志 0：SSIFRDR中接收数据的大小不大于SSISCR.RDFS的值。 1：SSIFRDR中接收数据的大小不小于SSISCR.RDFS的值加一。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
13:8	RDC[5:0]	接收FIFO数据指示标志数 接收FIFO数据数指示标志	R
15:14	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
16	TDE	Transmit Data Empty Flag 0: The free space of SSIFTDR is not more than the value of SSISCR.TDES. 1: The free space of SSIFTDR is not less than the value of SSISCR.TDES plus one.	R/W
23:17	—	These bits are read as 0. The write value should be 0.	R/W
29:24	TDC[5:0]	Number of Transmit FIFO Data Indication Flag Number of transmit FIFO data indication flag	R
31:30	—	These bits are read as 0. The write value should be 0.	R/W

This register is configured with status flags that indicate the status of the transmit FIFO data register and the receive FIFO data register.

RDF flag (Receive Data Full Flag)

The RDF flag indicates that the receive FIFO data register (SSIFRDR) has unread received data not less than the amount set with the SSISCR.RDFS bit plus one. This flag is set by automatic determination but it must be cleared by register access.

[Priority order for setting and clearing]

Clearing is prioritized.

[Clearing condition]

Either of the following two:*1

1. Writing 0 to this bit after reading 1 from this bit (CPU operation)*2
2. Last access (DTC/DMAC operation) to read data from SSIFRDR by an interrupt routine using the DTC and DMAC.

[Clearing timing]

Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 38.19)
2. After the PCLKB cycle in which the last access instruction is issued to read data from SSIFRDR by an interrupt routine using the DTC and DMAC.

[Setting condition]

SSIFTDR has free space not less than the amount set with the SSIFCR.TTRG bit plus one.

[Setting timing]

At completion of transfer from the shift register that results in SSIFRDR having data not less than the amount set with the SSISCR.RDFS bit plus one.

Note 1. These bits are cleared by a software reset (SSIFCR.SSIRST = 1) and receive FIFO data register reset (SSIFCR.RFRST = 1). Reset conditions available for these bits are the software reset and receive FIFO data register reset as well as the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following four conditions is met:
- A software reset is done (SSIFCR.SSIRST = 1).
- A receive FIFO data register reset is done (SSIFCR.RFRST = 1).
- After 1 has been read, writing of 0 is complete.
- Last access is performed to read data from SSIFRDR by an interrupt routine using the DTC and DMAC.

Bit	Symbol	Function	R/W
16	TDE	传输数据空标志 0：SSIFTDR的可用空间不大于SSISCR.TDES的值。1：SSIFTDR的可用空间不小于SSISCR.TDES的值加一。	R/W
23:17	—	这些位被读取为0。写入值应为0。	R/W
29:24	TDC[5:0]	发送FIFO数据指示标志数 发送FIFO数据数指示标志	R
31:30	—	这些位被读取为0。写入值应为0。	R/W

该寄存器配置有状态标志，指示发送FIFO数据寄存器和接收FIFO数据寄存器的状态。

RDF标志（接收数据满标志）

RDF标志表示接收FIFO数据寄存器(SSIFRDR)的未读接收数据不少于SSISCR.RDFS位设置的数量加一。该标志由自动确定设置，但必须通过寄存器访问清除。

[设置和清除的优先顺序]

清算优先。

[Clearing condition]

以下两种之一：*1

1.从该位读取1后向该位写入0（CPU操作）*2

2.最后一次访问（DTCDMAC操作）通过使用DTC和DMAC的中断例程从SSIFRDR读取数据。

[Clearing timing]

与上述清零条件对应的清零时机

1.当从该位读取1后向该位写入0时（与图38.19中的时序相同）

2.在发出最后一个访问指令以通过使用DTC和DMAC的中断例程从SSIFRDR读取数据的PCLKB周期之后。

[Setting condition]

SSIFTDR的可用空间不小于SSIFCR.TTRG位设置的数量加一。

[Setting timing]

在完成从移位寄存器的传输时，导致SSIFRDR的数据不小于用
SISSCR.RDFS位加一。

注1.这些位通过软件复位(SSIFCR.SSIRST=1)和接收FIFO数据寄存器复位清零
（SSIFCR.RFRST=1）。这些位可用的复位条件是软件复位和接收FIFO数据寄存器复位以及上述清除条件。

注2.从该位读取1后，当满足以下四个条件之一时，该位被清除：●软件复位完成(SSIFCR.SSIRST=1)。●完成接收FIFO数据寄存器复位(SSIFCR.RFRST=1)。●读1后，写0完成。●使用DTC和DMAC的中断例程执行最后一次访问以从SSIFRDR读取数据。

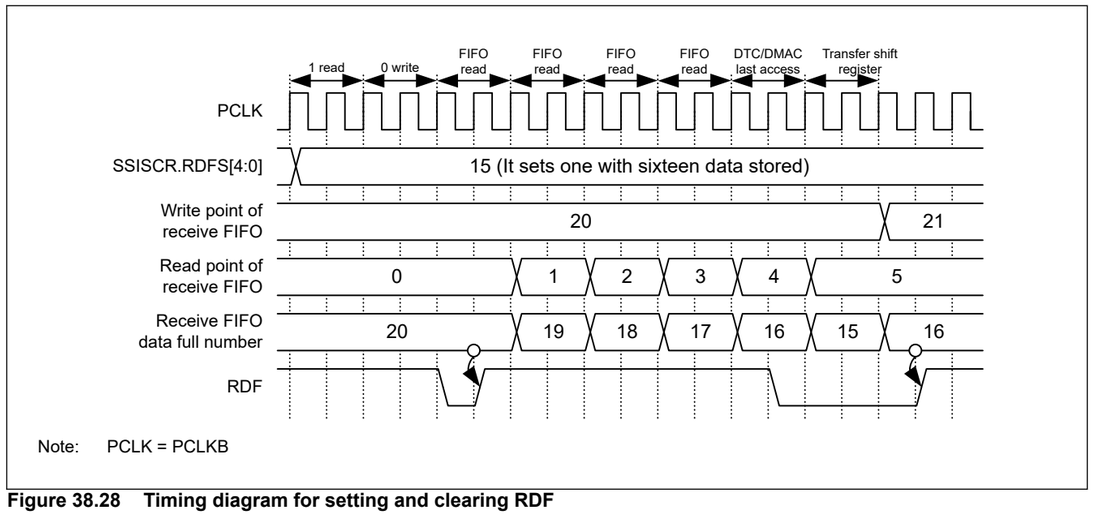


Figure 38.28 Timing diagram for setting and clearing RDF

RDC[5:0] flags (Number of Receive FIFO Data Indication Flag)

The RDC[5:0] flags indicate the number of valid data that are stored in the receive FIFO data register (SSIFRDR). With this flag as 0x00, there is no received data. With 0x20, the register is filled with received data and there is no free space.

TDE flag (Transmit Data Empty Flag)

The TDE flag indicates that the transmit FIFO data register (SSIFTDR) has free space not less than the amount set with the SSIFCR.TTRG bit plus one. This flag is set by automatic determination but it must be cleared by register access.

[Priority order for setting and clearing]

Clearing is prioritized.*1

[Clearing condition]

Either of the following two:

1. Writing 0 to this bit after reading 1 from this bit (CPU operation)*2
2. Last access (DTC/DMAC operation) to write data to SSIFTDR by an interrupt routine using the DTC and DMAC.

[Clearing timing]

Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 38.19)
2. Last access (DTC/DMAC operation) to write data to SSIFTDR by an interrupt routine using the DTC and DMAC.

[Setting condition]

SSIFTDR has free space not less than the amount set with the SSIFCR.TTRG bit plus one.

[Setting timing]

While operating on PCLKB, SSIFTDR is found to have free space not less than “size set in the SSISCR.TDES bits + 1.”

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1) and transmit FIFO data register reset (SSIFCR.TFRST = 1). The software reset and transmit FIFO data register reset have priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following four conditions is met:
- A software reset is done (SSIFCR.SSIRST = 1).
- A transmit FIFO data register reset is done (SSIFCR.TFRST = 1).
- After 1 has been read, writing of 0 is complete.
- Last access is performed to write data to SSIFTDR by an interrupt routine using the DTC and DMAC.

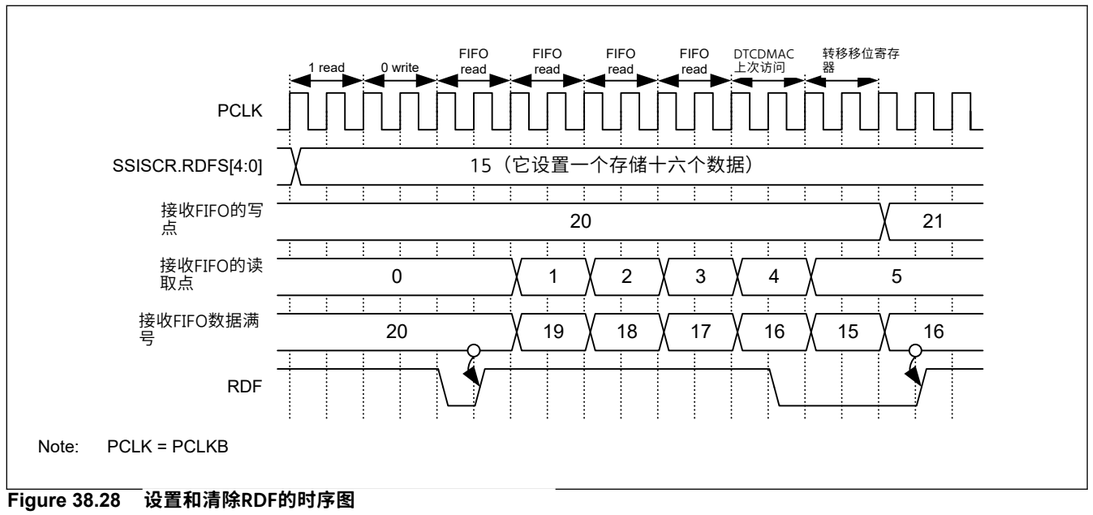


Figure 38.28 设置和清除RDF的时序图

RDC[5:0]flags（接收FIFO数据指示标志数）

RDC[5:0]标志指示存储在接收FIFO数据寄存器(SSIFRDR)中的有效数据数量。此标志为0x00时，没有接收到数据。使用0x20，寄存器被接收到的数据填充，没有可用空间。

TDE标志（传输数据空标志）

TDE标志表示发送FIFO数据寄存器(SSIFTDR)的可用空间不小于用
SSIFCR.TTRG位加一。该标志由自动确定设置，但必须通过寄存器访问清除。

[设置和清除的优先顺序]

清算优先。*1

[Clearing condition]

以下两种之一：

1.从该位读取1后向该位写入0（CPU操作）*2

2.最后访问（DTCDMAC操作）通过使用DTC和DMAC的中断例程将数据写入SSIFTDR。

[Clearing timing]

与上述清零条件对应的清零时机

1.当从该位读取1后向该位写入0时（与图38.19中的时序相同）

2.最后访问（DTCDMAC操作）通过使用DTC和DMAC的中断例程将数据写入SSIFTDR。

[Setting condition]

SSIFTDR的可用空间不小于SSIFCR.TTRG位设置的数量加一。

[Setting timing]

在PCLKB上运行时，发现SSIFTDR的可用空间不小于“SSISCR.TDES位中设置的大小+1”。

注1.该位通过软件复位(SSIFCR.SSIRST=1)和发送FIFO数据寄存器复位(SSIFCR.TFRST=1)清零。软件复位和发送FIFO数据寄存器复位优先于上述所有清除条件。

注2.从该位读取1后，当满足以下四个条件之一时，该位被清除：●软件复位完成(SSIFCR.SSIRST=1)。●发送FIFO数据寄存器复位完成(SSIFCR.TFRST=1)。●读1后，写0完成。●使用DTC和DMAC的中断例程执行最后访问以将数据写入SSIFTDR。

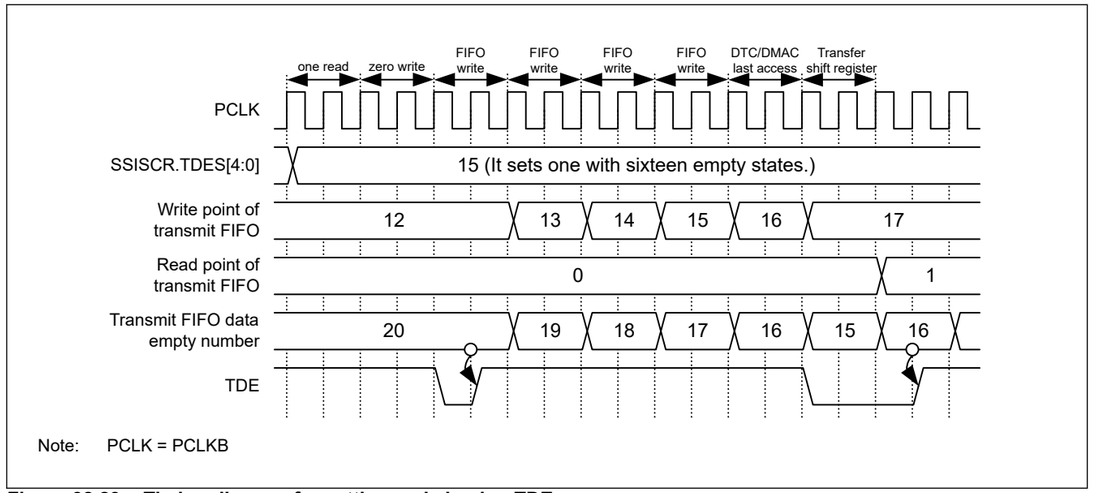


Figure 38.29 Timing diagram for setting and clearing TDE

TDC[5:0] flags (Number of Transmit FIFO Data Indication Flag)

The TDC[5:0] flags indicate the number of valid data that are stored in the transmit FIFO data register (SSIFTDR). With this flag as 0x00, there is no data to be transmitted. With 0x20, there is no space to write data.

38.4.5 SSIFTDR : Transmit FIFO Data Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x18

Bit position:	31																												0
Bit field:	SSIFTDR[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	SSIFTDR[31:0]	Transmit FIFO Data	W

This register stores data to be serially transmitted. 0 is returned when this register is read.

When you use this register for transmission, specify data writing to this register as the DTC/DMAC operation that is triggered by a transmit data empty interrupt. Determine the access size to this register according to the data word length to be communicated in Table 38.8.

Table 38.8 Register access restriction to FIFOs (1 of 2)

Access Size				
SSICR.DWL[2:0]	Data Word Length	Byte	Halfword	Word
000b	8	✓	—	—
001b	16	—	✓	—
010b	18	—	—	✓
011b	20	—	—	✓
100b	22	—	—	✓
101b	24	—	—	✓
110b	32	—	—	✓

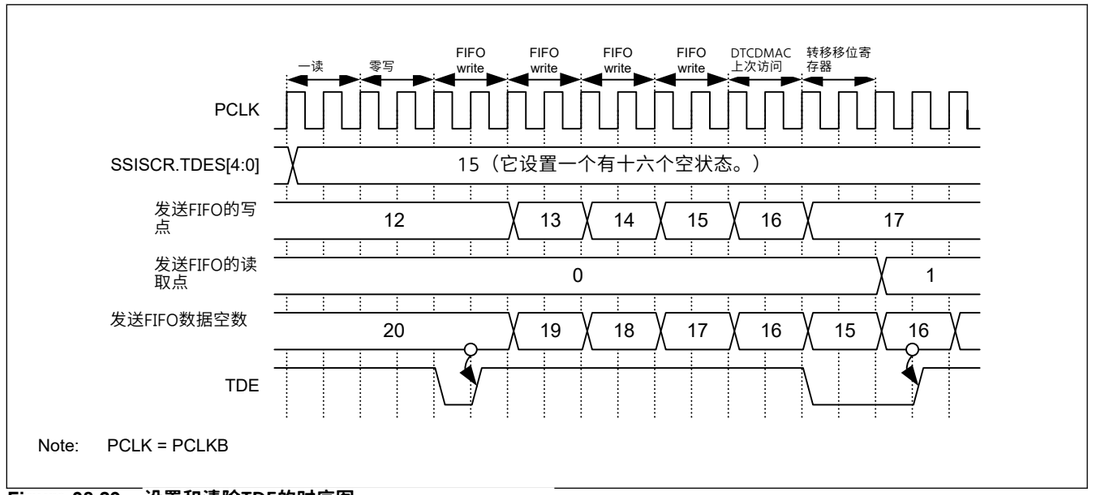


Figure 38.29 设置和清除TDE的时序图

TDC[5:0]flags（发送FIFO数据指示标志数）

TDC[5:0]标志指示存储在发送FIFO数据寄存器(SSIFTDR)中的有效数据数量。此标志为0x00时，没有要传输的数据。使用0x20，没有空间可以写入数据。

38.4.5 SSIFTDR：发送FIFO数据寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x18

Bit position:	31																												0
Bit field:	SSIFTDR[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	SSIFTDR[31:0]	发送FIFO数据	W

该寄存器存储要串行传输的数据。读取该寄存器时返回0。

当您使用该寄存器进行传输时，将数据写入该寄存器指定为由传输数据空中断触发的DTCDMAC操作。根据表38.8中要通信的数据字长确定对该寄存器的访问大小。

Table 38.8 对FIFO的寄存器访问限制（1of2）

访问大小				
SSICR.DWL[2:0]	数据字长	Byte	Halfword	Word
000b	8	✓	—	—
001b	16	—	✓	—
010b	18	—	—	✓
011b	20	—	—	✓
100b	22	—	—	✓
101b	24	—	—	✓
110b	32	—	—	✓

Table 38.8 Register access restriction to FIFOs (2 of 2)

Access Size		Byte	Halfword	Word
SSICR.DWL[2:0]	Data Word Length			
111b	Setting prohibited	—	—	—

Figure 38.30 shows register access to the transmit FIFO data register.

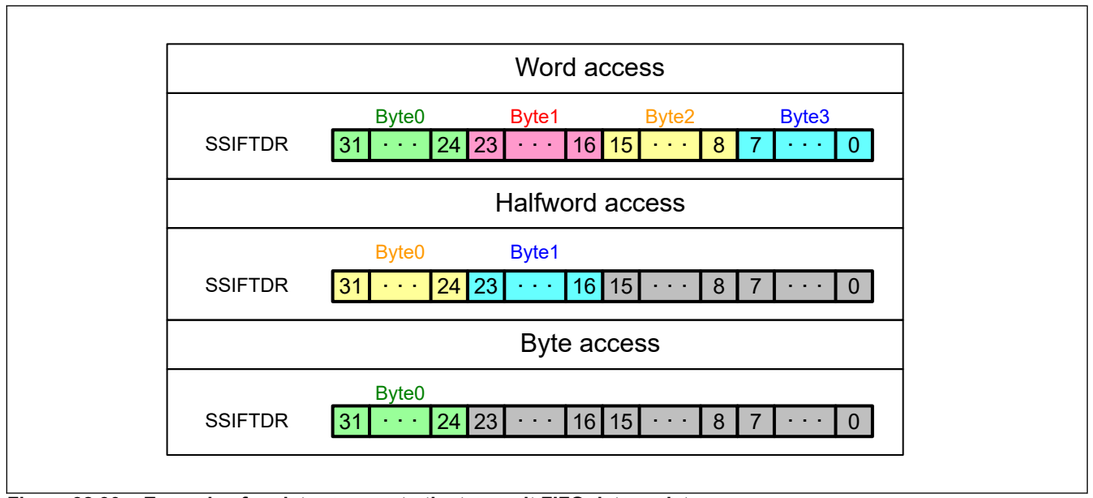


Figure 38.30 Example of register access to the transmit FIFO data register

Figure 38.31 shows the configurations and operation examples of the transmit FIFO data register and transmit shift register. The configurations are for storing data to FIFO and not related with communication.

Table 38.8 对FIFO的寄存器访问限制（2个中的2个）

访问大小		Byte	Halfword	Word
SSICR.DWL[2:0]	数据字长			
111b	禁止设定	—	—	—

图38.30显示了对发送FIFO数据寄存器的寄存器访问。

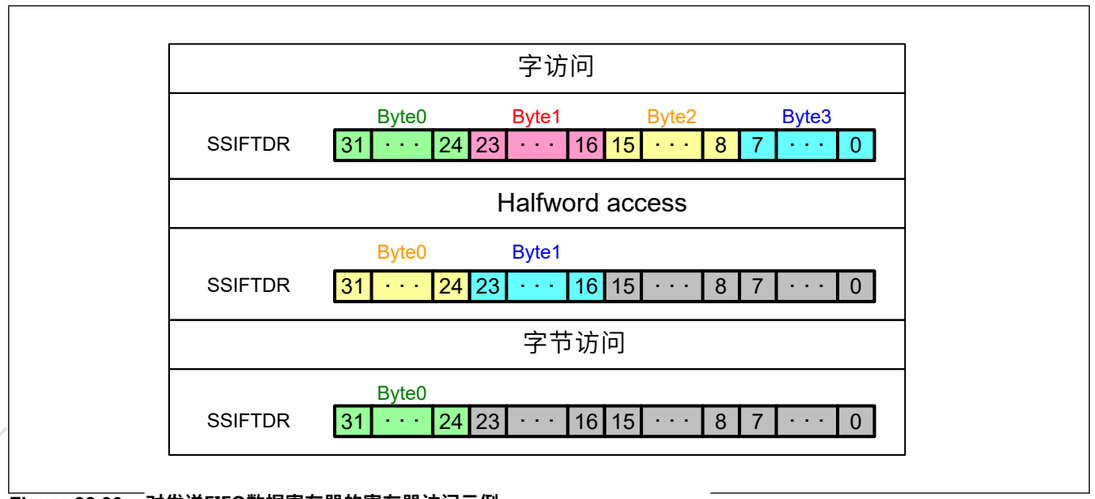
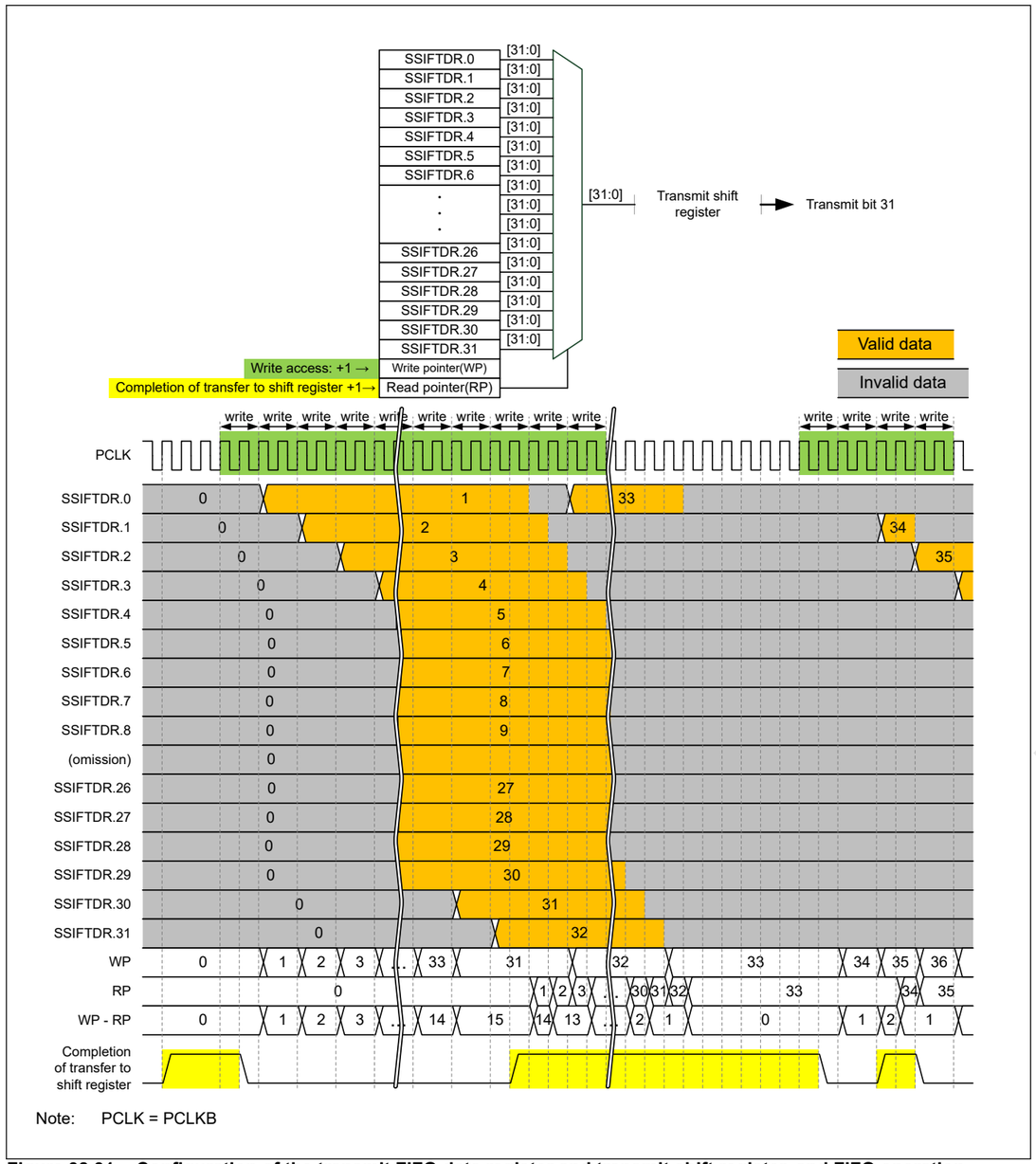


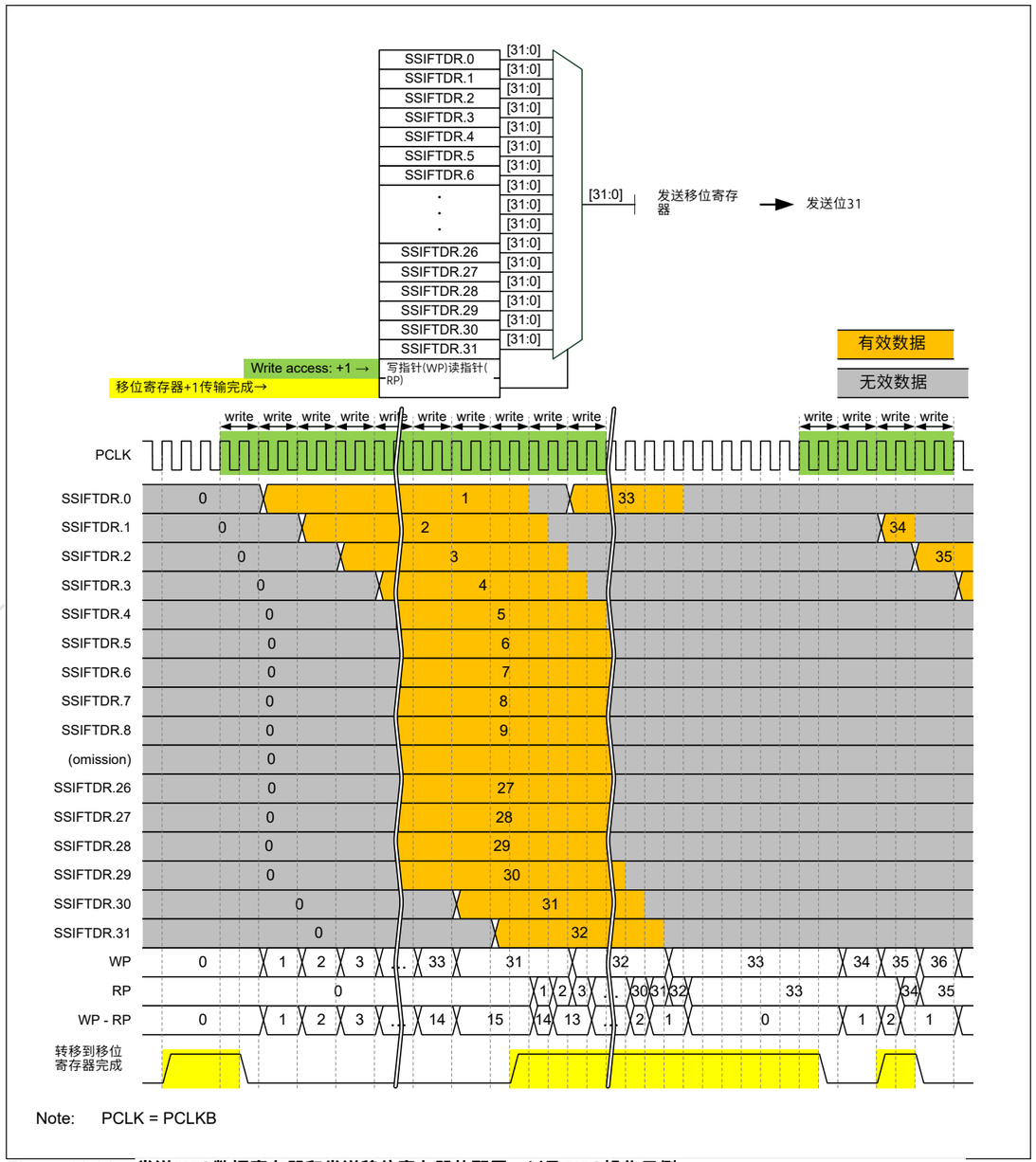
Figure 38.30 对发送FIFO数据寄存器的寄存器访问示例

图38.31显示了发送FIFO数据寄存器和发送移位寄存器的配置和操作示例。
该配置用于将数据存储到FIFO，与通信无关。



Note: PCLK = PCLKB

Figure 38.31 Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example



Note: PCLK = PCLKB

Figure 38.31 发送FIFO数据寄存器和发送移位寄存器的配置，以及FIFO操作示例

38.4.6 SSIFRDR : Receive FIFO Data Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x1C

Bit position:	31																													0
Bit field:	SSIFRDR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	SSIFRDR[31:0]	Receive FIFO Data	R

When you use this register for reception, specify data reading from this register as the DTC/DMAC operation that is triggered by a transmit data empty interrupt. Determine the access size to this register according to the data word length to be communicated in Table 38.8.

Register access to the receive FIFO data register is same as for the transmit FIFO data register.

Figure 38.31 shows the configurations and operation examples of the receive FIFO data register and receive shift register.

38.4.6 SSIFRDR:接收FIFO数据寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x1C

Bit position:	31																													0
Bit field:	SSIFRDR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

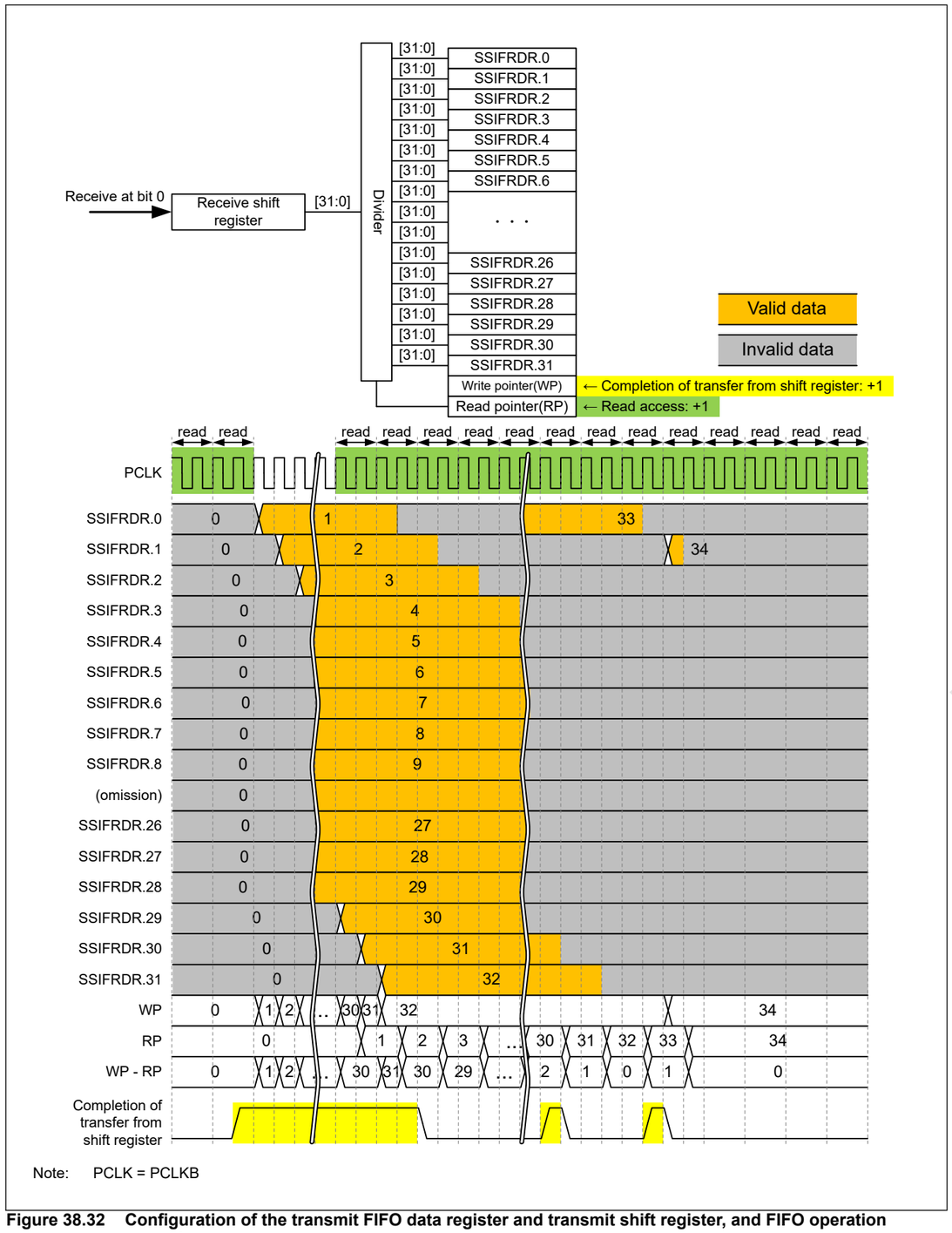
Bit	Symbol	Function	R/W
31:0	SSIFRDR[31:0]	接收FIFO数据	R

当您使用该寄存器进行接收时，将从该寄存器读取的数据指定为由发送数据空中断触发的DTCDMAC操作。根据表38.8中要通信的数据字长确定对该寄存器的访问大小。

对接收FIFO数据寄存器的寄存器访问与对发送FIFO数据寄存器的访问相同。

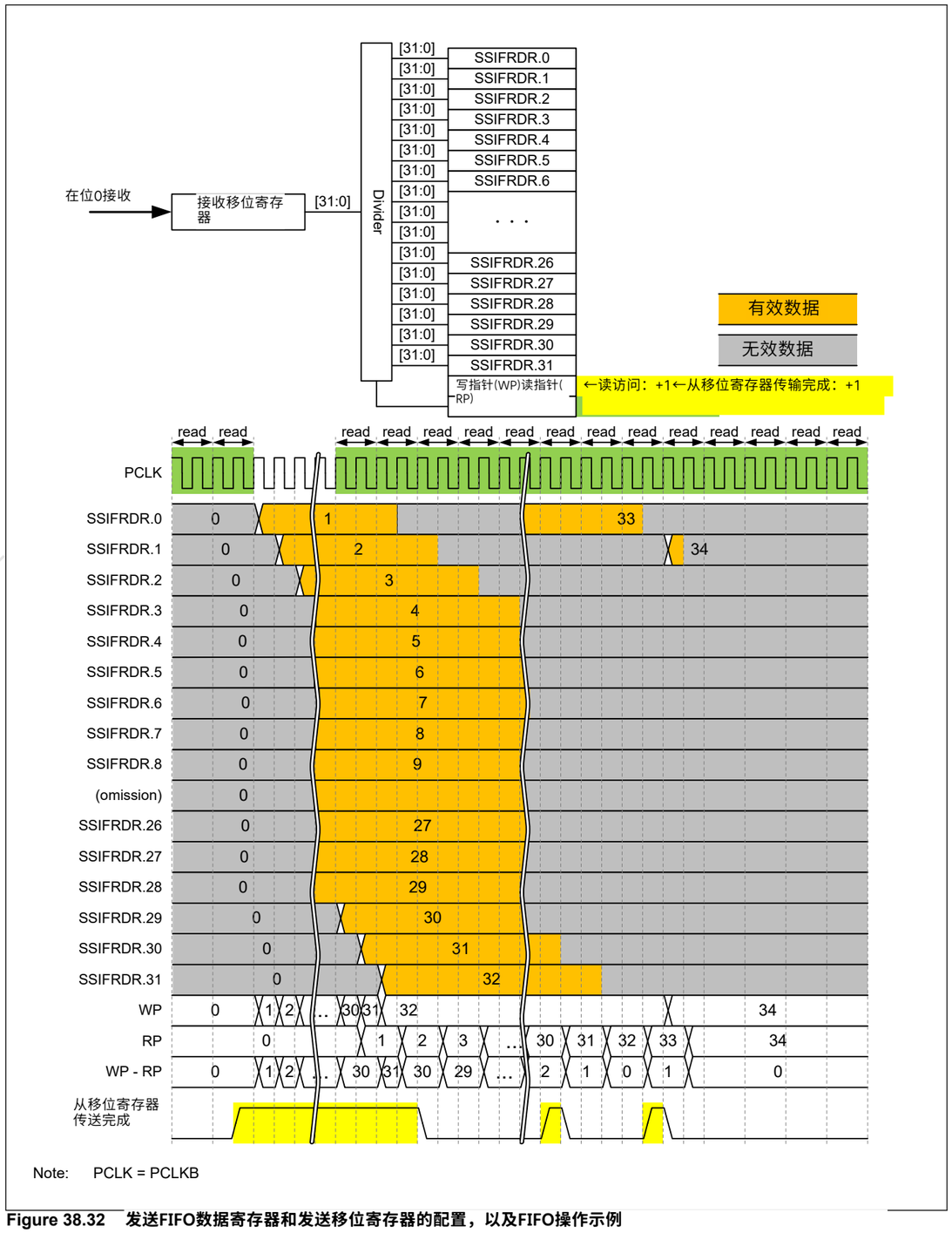
图38.31显示了接收FIFO数据寄存器和接收移位寄存器的配置和操作示例。

RA生态工作室



Note: PCLK = PCLKB

Figure 38.32 Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example



Note: PCLK = PCLKB

Figure 38.32 发送FIFO数据寄存器和发送移位寄存器的配置，以及FIFO操作示例

38.4.7 SSIOFR : Audio Format Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMOD[1:0]	Audio Format Select*3 *4 0 0: I²S format 0 1: TDM format 1 0: Monaural format 1 1: Setting prohibited	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	LRCONT	Whether to Enable LRCK/FS Continuation*1 *2 0: Disables LRCK/FS continuation 1: Enables LRCK/FS continuation	R/W
9	BCKASTP	Whether to Enable Stopping BCK Output When SSIE is in Idle Status*1 *2 0: Always outputs BCK to the SSIBCK pin 1: Automatically controls output of BCK to the SSIBCK pin	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is valid only in master-mode communication (SSICR.MST = 1). The setting is invalid in slave-mode communication (SSICR.MST = 0).
Note 2. The BCKASTP and LRCONT bits must not be set to 1 together.
Note 3. While SSIE is communicating (SSISR.IIRQ = 0), writing to these bits is prohibited. If the value of these bits is changed by writing, subsequent operation is unpredictable.
Note 4. If the communication format of other-party device is compatible with a communication format of SSIE, specify and use the communication format that enables communication with the other-party device.

This register is used to set an audio format (which involves the settings of communication format, LR clock/frame synchronization continuation mode, and BCK output stop).

OMOD[1:0] bits (Audio Format Select)

The OMOD[1:0] bits set an audio format. Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in section 38.4.7. SSIOFR : Audio Format Register.

LRCONT bit (Whether to Enable LRCK/FS Continuation)

The LRCONT bit enables or disables the output from SSILRCK/SSIFS pin when the communication mode is master-mode communication (SSICR.MST = 1) and SSIE is in the idle state (SSISR.IIRQ = 1).

Even in the idle state, a signal can output from the SSILRCK/SSIFS pin when this bit is set to 1 (to enable LR clock/frame synchronization continuation) in master mode (SSICR.MST = 1).

38.4.7 SSIOFR:音频格式寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x20

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMOD[1:0]	音频格式选择*3*4 00：I2S格式01：TDM格式10：单声道格式1 1：禁止设置	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	LRCONT	是否开启LRCKFSContinuation*1*2 0：禁用LRCKFS延续1：启用LRCKFS延续	R/W
9	BCKASTP	SSIE空闲时是否使能停止BCK输出*1*2 0：始终向SSIBCK引脚输出BCK1：自动控制向SSIBCK引脚输出BCK	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

注1.该位仅在主模式通信(SSICR.MST=1)中有效。该设置在从模式通信中无效(SSICR.MST=0)。

注2.BCKASTP和LRCONT位不能一起设置为1。
注3.当SSIE正在通信时（SSISR.IIRQ=0），禁止写入这些位。如果这些位的值通过写来改变，后续的操作是不可预知的。

注4.如果对方设备的通信格式与SSIE的通信格式兼容，请指定并使用能够与对方设备进行通信的通信格式。

该寄存器用于设置音频格式（涉及通信格式、LR时钟帧同步持续模式、BCK输出停止的设置）。

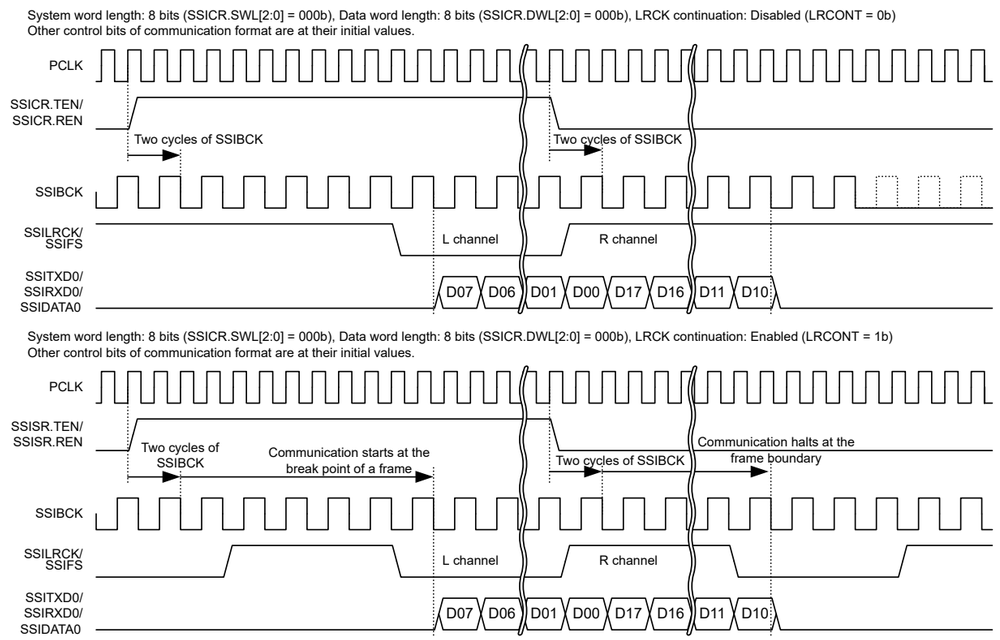
OMOD[1:0]位（音频格式选择）

OMOD[1:0]位设置音频格式。当LR时钟提供给
SSILRCKSSIFS引脚停止。LR时钟的输出详见38.4.7节LRCONT位的详细说明。SSIOFR：音频格式寄存器。

LRCONT位（是否使能LRCKFSContinuation）

当通信模式为主机模式通信(SSICR.MST=1)且SSIE处于空闲状态(SSISR.IIRQ=1)时，LRCONT位启用或禁用SSILRCKS
SIFS引脚的输出。

即使在空闲状态下，当该位在主模式(SSICR.MST=1)下设置为1（以启用LR时钟帧同步继续）时，也可以从SSILRC
KSSIFS引脚输出信号。



Note: PCLK = PCLKB

Figure 38.33 Example of LR clock/frame synchronization continuation operation

BCKASTP bit (Whether to Enable Stopping BCK Output When SSIE is in Idle Status)

The BCKASTP bit turns on or off the function to output BCK to the SSIBCK pin according to the communication shown in Figure 38.34 and Figure 38.35 in master-mode communication (SSICR.MST = 1).

Changing the value of this bit must be performed only after setting the communication format to be used.

This bit must be used in the following way:

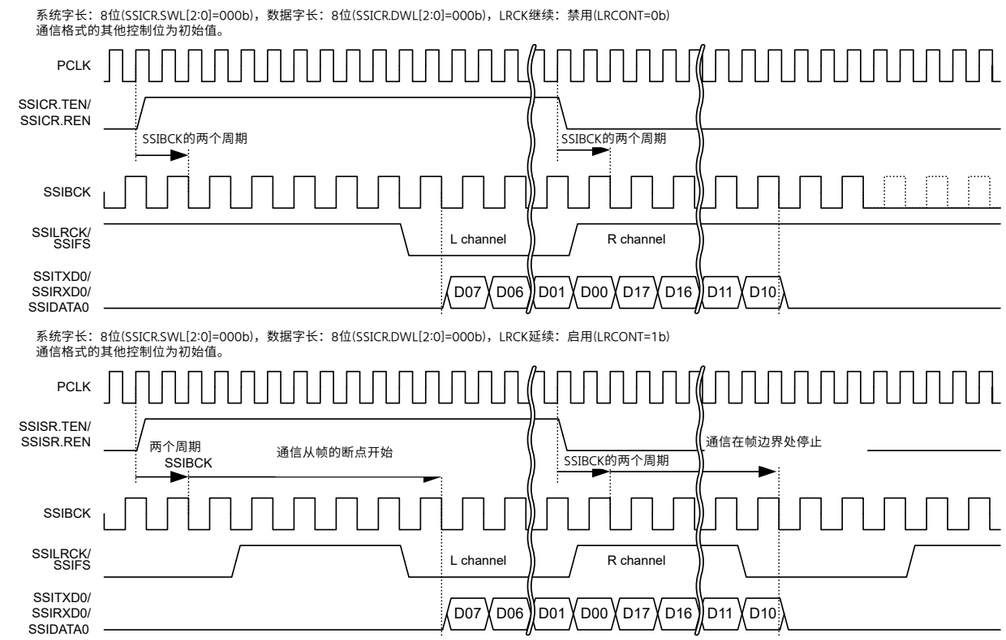
Write 0 to the BCKASTP bit, and then start communication. During the communication, write 1 to the BCKASTP bit. By this operation, the bit clock output to the SSIBCK pin stops automatically when the communication stops. To resume the communication, set SSIE to the idle state (SSICR.IIRQ = 1), enable the supply of AUDIO_MCK (SSIFCR.AUCKE = 1), and then write 0 to the BCKASTP bit.

When the communication mode is master-mode communication (SSICR.MST = 1) and SSIE is in the idle state (SSICR.IIRQ = 1):

Table 38.9 BCKASTP bit status and SSIBCK pin output

BCKASTP Bit	SSIBCK Pin Output Status
0	Output
1	Stopped

Note: The BCKASTP bit cannot be used when the other-party device (which is a slave) requires the clock output from the SSIBCK pin before and during communication. In such a case, use the BCKASTP bit to stop the clock only after communication. For the timing of enabling the clock stop function, see Figure 38.34.



Note: PCLK = PCLKB

Figure 38.33 LR时钟帧同步继续操作示例

BCKASTP位（SSIE空闲时是否使能停止BCK输出）

BCKASTP位根据中所示的通信打开或关闭将BCK输出到SSIBCK引脚的功能
图38.34和图38.35在主模式通信(SSICR.MST=1)。

只有在设置要使用的通信格式后才能更改该位的值。

该位必须按以下方式使用：

将0写入BCKASTP位，然后开始通信。在通信期间，将1写入BCKASTP位。通过该操作，当通信停止时，向SSIBCK引脚输出的位时钟自动停止。要恢复通信，请将SSIE设置为空闲状态(SSICR.IIRQ=1)，启用AUDIO_MCK电源(SSIFCR.AUCKE=1)，然后将0写入BCKASTP位。

当通信模式为主模式通信（SSICR.MST=1）且SSIE处于空闲状态（SSICR.IIRQ=1）时：

Table 38.9 BCKASTP位状态和SSIBCK引脚输出

BCKASTP Bit	SSIBCK引脚输出状态
0	Output
1	Stopped

Note: 当对方设备（作为从设备）在通信之前和通信期间需要从SSIBCK引脚输出时钟时，不能使用BCKASTP位。在这种情况下，仅在通信后使用BCKASTP位停止时钟。时钟停止功能的开启时序见图38.34。

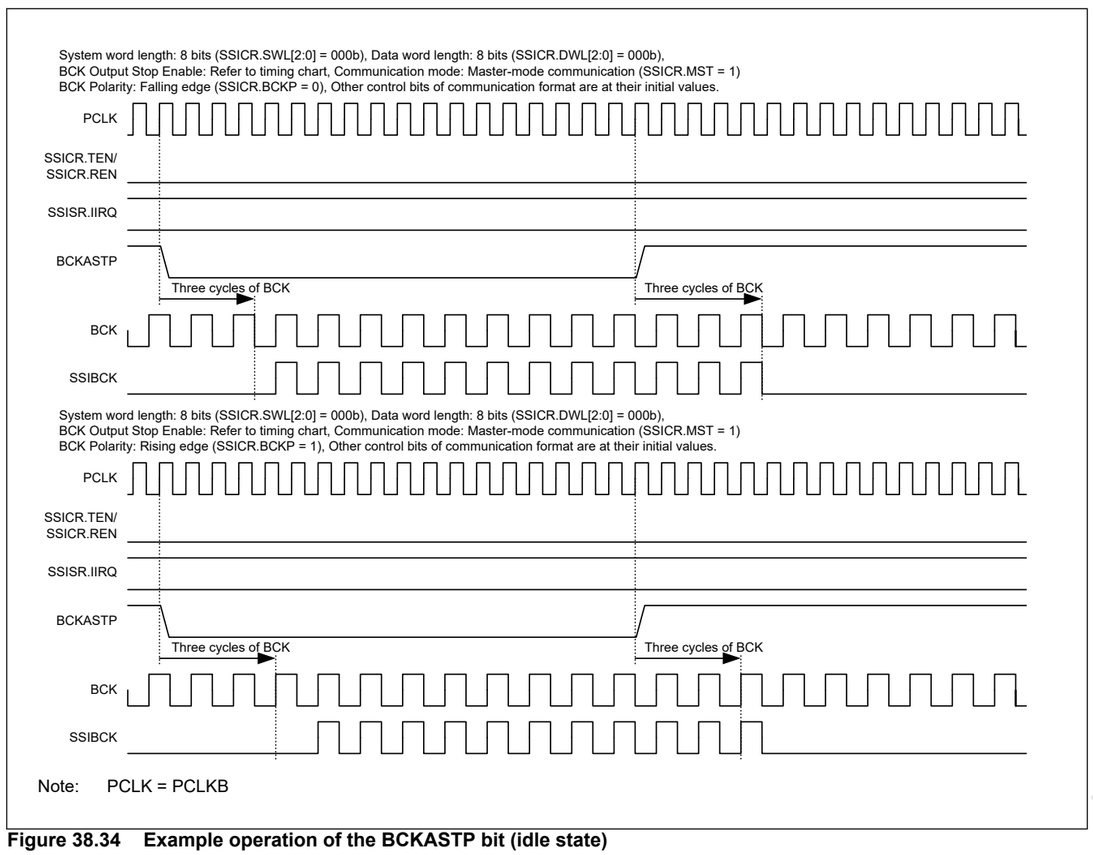


Figure 38.34 Example operation of the BCKASTP bit (idle state)

When the communication mode is master-mode communication (SSICR.MST = 1) and the BCK output stop function is enabled (BCKASTP = 1):

Details of the BCK output to the SSIBCK pin are as follows:

Output start timing: BCK is output in appropriate timing so that a valid edge is generated when the LR clock/frame synchronization signal shifts to a valid value.

Output stop timing: 1 to 1.5 clock cycles after a frame boundary.

For details about the timings, see the timing diagram in Figure 38.35.

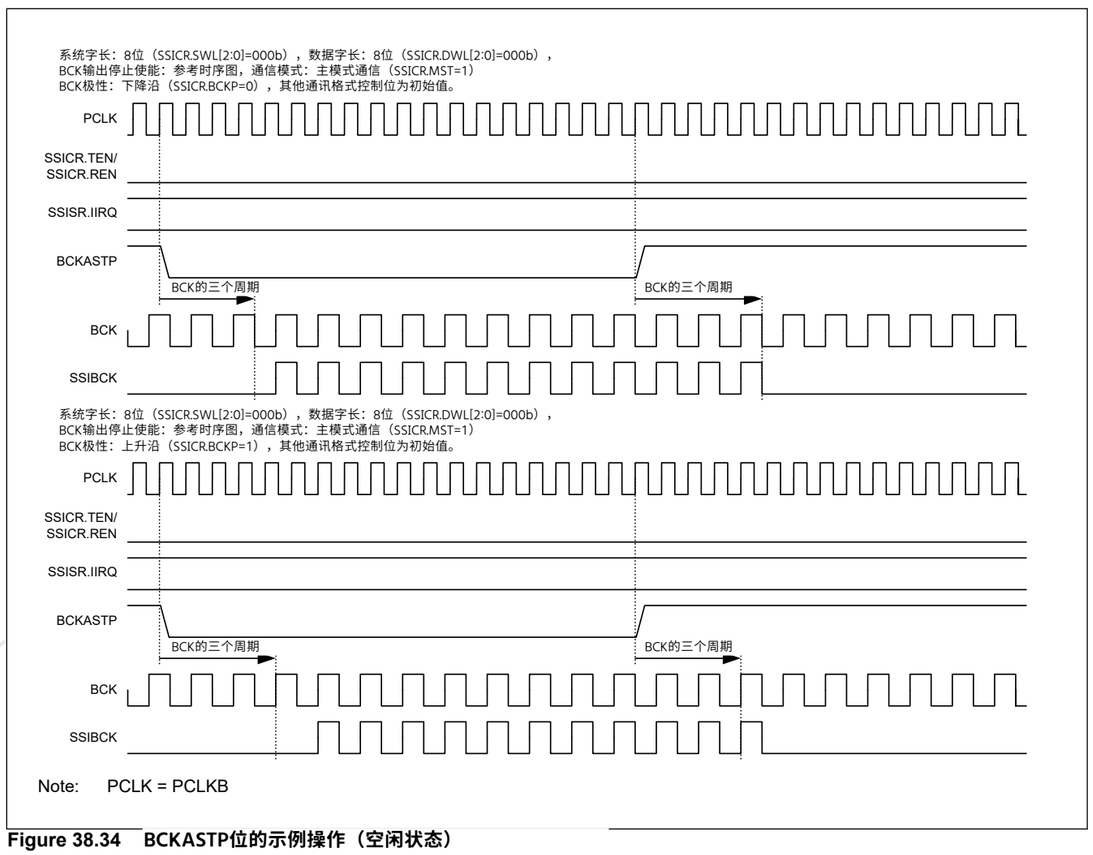


Figure 38.34 BCKASTP位的示例操作（空闲状态）

当通信模式为主机模式通信(SSICR.MST=1)且BCK输出停止功能启用(BCKASTP=1)时：

BCK输出到SSIBCK引脚的详细信息如下：

输出开始时序：在适当的时序输出BCK，以便在LR时钟帧同步信号移位到有效值时产生有效边沿。

输出停止时序：帧边界后1到1.5个时钟周期。

有关时序的详细信息，请参见图38.35中的时序图。

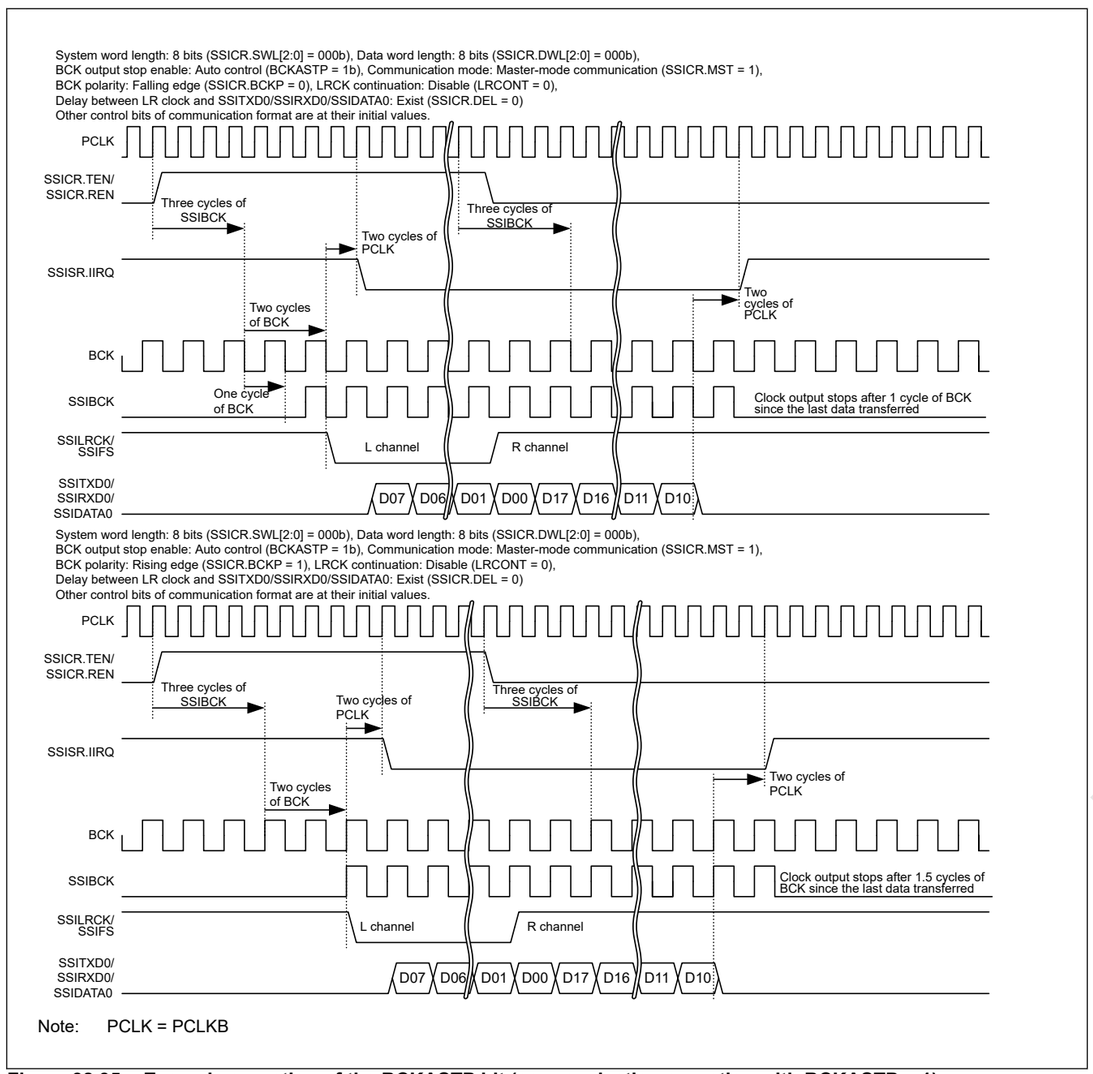


Figure 38.35 Example operation of the BCKASTP bit (communication operation with BCKASTP = 1)

38.4.8 SSISCR : Status Control Register

Base address: SSIE0 = 0x4009_D000

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

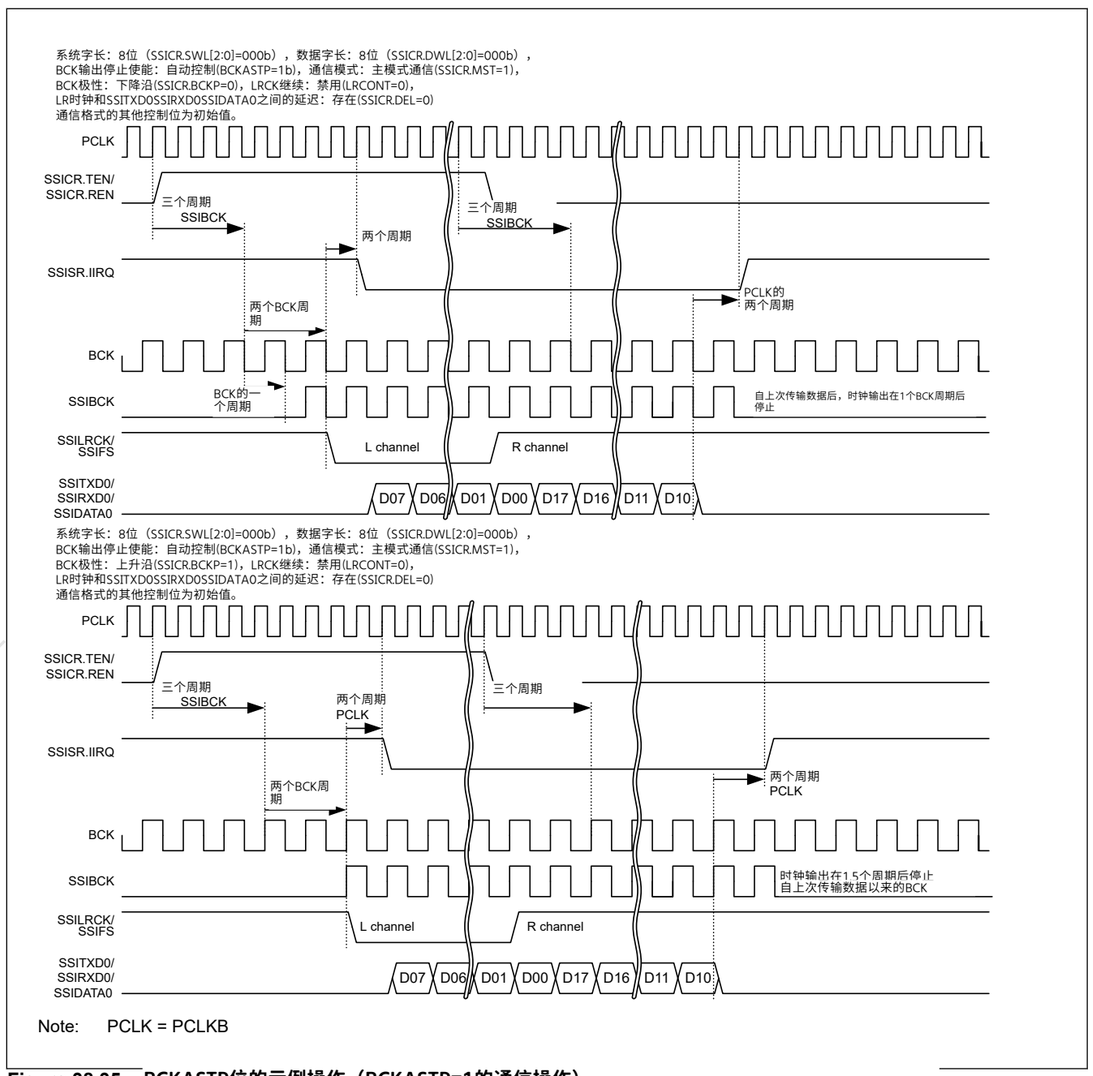


Figure 38.35 BCKASTP位的示例操作（BCKASTP=1的通信操作）

38.4.8 SISSCR:状态控制寄存器

Base address: SSIE0 = 0x4009_D000

Offset address: 0x24

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	RDFS[4:0]	RDF Setting Condition Select*1 0x00: SSIFRDR has one stage or more data size. 0x01: SSIFRDR has two stages or more data size. ⋮ 0x1E: SSIFRDR has thirty-one stages or more data size. 0x1F: SSIFRDR has thirty-two stages or more data size.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
12:8	TDES[4:0]	TDE Setting Condition Select*1 0x00: SSIFTDR has one stage or more free space. 0x01: SSIFTDR has two stages or more free space. ⋮ 0x1E: SSIFTDR has thirty-one stages or more free space. 0x1F: SSIFTDR has thirty-two stages or more free space.	R/W
31:13	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits while SSIE is in a communication state (SSISR.IIRQ = 0) is prohibited. If written, the operation performed immediately after writing is not guaranteed.

RDFS[4:0] bits (RDF Setting Condition Select)

The RDFS[4:0] bits set the setting condition of the receive data full flag (RDF).

TDES[4:0] bits (TDE Setting Condition Select)

The TDES[4:0] bits set the setting condition of the transmit data empty flag (TDE).

38.5 Communication Formats

SSIE supports three communication formats. Table 38.10 shows supported communication formats.

Table 38.10 Supported communication formats

Communication Format	SSIOFR.OMOD[1:0]
I²S format	00
TDM format	01
Monaural format	10

The following describes the serial data structure shared by communication formats. A serial data structure is defined by the system word length (set in SSICR.SWL[2:0]) and the data word length (set in SSICR.DWL[2:0]). If the data word length is shorter than the system word length, padding bits are transferred in the serial data. For details, see Figure 38.36.

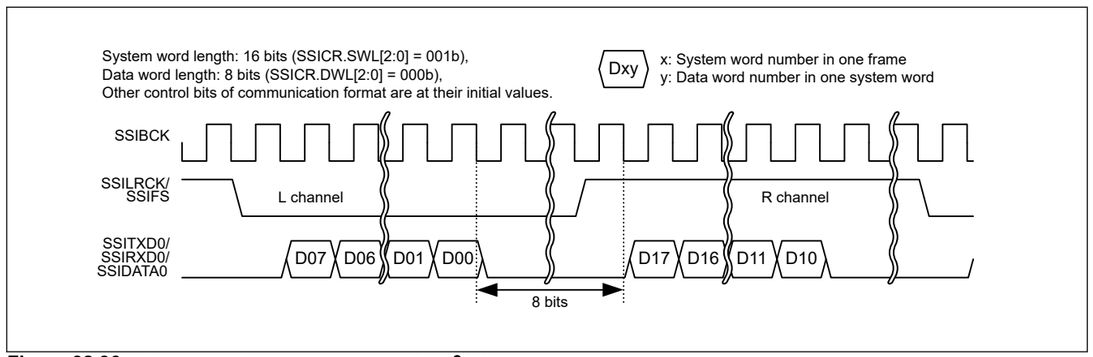


Figure 38.36 Example of padding bit transfer (I²S format: system word length > data word length)

Table 38.11 lists the number of padding bits to be transferred with each combination of system word length (SSICR.SWL[2:0]) and data word length (SSICR.DWL[2:0]). "-" indicates that the setting is prohibited.

Bit	Symbol	Function	R/W
4:0	RDFS[4:0]	RDF设置条件选择*1 0x00：SSIFRDR具有一级或更多数据大小。0x01：S SIFRDR具有两级或更多数据大小。 ⋮ 0x1E：SSIFRDR具有31级或更多数据大小。0x1F：SSIFRD R具有32级或更多数据大小。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
12:8	TDES[4:0]	TDE设定条件选择*1 0x00：SSIFTDR有一级或更多可用空间。0x01：SSIF TDR有两级或更多可用空间。 ⋮ 0x1E：SSIFTDR有31个或更多的可用空间。0x1F：SSIFTDR 有32级或更多可用空间。	R/W
31:13	—	这些位被读取为0。写入值应为0。	R/W

注1.禁止在SSIE处于通信状态(SSISR.IIRQ=0)时写入这些位。如果写入，则不保证写入后立即执行的操作。

RDFS[4:0]位（RDF设置条件选择）

RDFS[4:0]位设置接收数据满标志(RDF)的设置条件。

TDES[4:0]位（TDE设置条件选择）

TDES[4:0]位设置发送数据空标志(TDE)的设置条件。

38.5 通讯格式

SSIE支持三种通信格式。表38.10显示了支持的通信格式。

Table 38.10 支持的通讯格式

通讯格式	SSIOFR.OMOD[1:0]
I²S format	00
TDM format	01
Monaural format	10

下面介绍通信格式共享的串行数据结构。串行数据结构由系统字长（在SSICR.SWL[2:0]中设置）和数据字长（在SSICR.DWL[2:0]中设置）定义。如果数据字长短于系统字长，则在串行数据中传输填充位。详见图38.36。

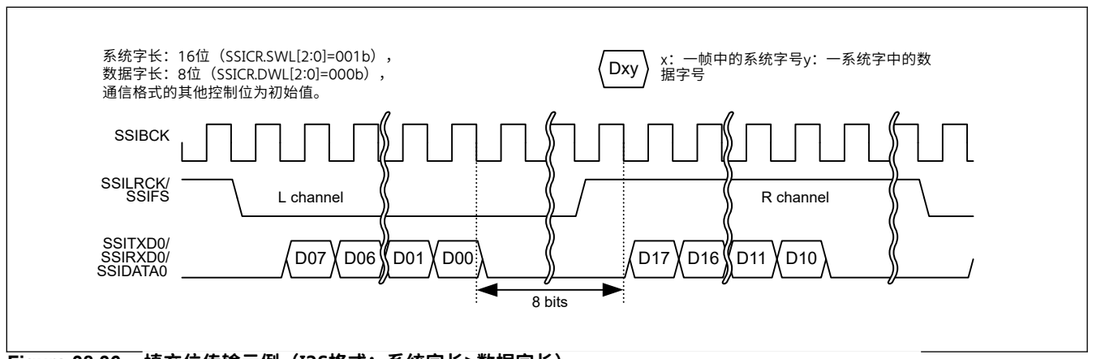


Figure 38.36 填充位传输示例（I2S格式：系统字长>数据字长）

表38.11列出了使用系统字长(SSICR.SWL[2:0])和数据字长(SSICR.DWL[2:0])的每种组合传输的填充位数。"–"表示禁止设置。

Table 38.11 Number of padding bits

	SSICR.DWL[2:0]	000b	001b	010b	011b	100b	101b	110b	111b
SSICR.SWL[2:0]	System Word Length	8	16	18	20	22	24	32	Setting prohibited
000b	8	0	—	—	—	—	—	—	—
001b	16	8	0	—	—	—	—	—	—
010b	24	16	8	6	4	2	0	—	—
011b	32	24	16	14	12	10	8	0	—
100b	48	40	32	30	28	26	24	16	—
101b	64	56	48	46	44	42	40	32	—
110b	128	120	112	110	108	106	104	96	—
111b	256	248	240	238	236	234	232	224	—

38.5.1 I²S Format

The I²S format is a communication format used for connection with I²S-compatible serial devices. With this format setting (SSIOFR.OMOD[1:0] = 00b), one frame is configured with two system words, one for the channel L and the other for channel R. The SSILRCK/SSIFS signals are at a low level for the channel L and at a high level for the channel R. Set the polarity of the signals with the SSICR.LRCKP bit. Figure 38.37 shows the I²S format without padding. See Figure 38.36 for the format with padding.

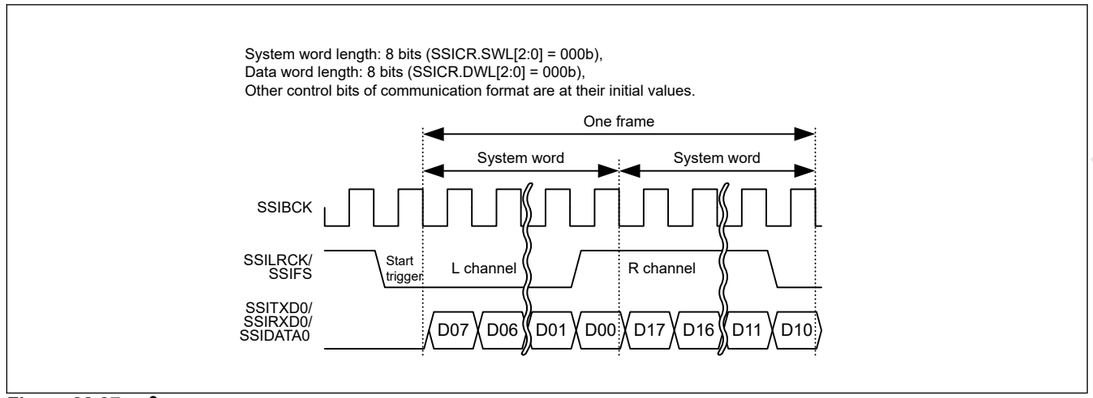


Figure 38.37 I²S format (without padding: system word length = data word length)

For the state of external pins when SSIE is in the idle state, see section 38.7.1. Idle State.

Note: SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

38.5.2 Monaural Format

The monaural format is a communication format used for connection with monaural-compatible serial devices. When the monaural format is specified (SSIOFR.OMOD[1:0] = 10b) for use, one frame consists of one system word. Also, a rising edge of the SSILRCK/SSIFS signal indicates a communication start trigger. Figure 38.38 and Figure 38.39 respectively show the monaural formats without and with padding.

Table 38.11 填充位数

	SSICR.DWL[2:0]	000b	001b	010b	011b	100b	101b	110b	111b
SSICR.SWL[2:0]	系统字 Length	8	16	18	20	22	24	32	禁止设定
000b	8	0	—	—	—	—	—	—	—
001b	16	8	0	—	—	—	—	—	—
010b	24	16	8	6	4	2	0	—	—
011b	32	24	16	14	12	10	8	0	—
100b	48	40	32	30	28	26	24	16	—
101b	64	56	48	46	44	42	40	32	—
110b	128	120	112	110	108	106	104	96	—
111b	256	248	240	238	236	234	232	224	—

38.5.1 I²S Format

I2S格式是用于连接I2S兼容串行设备的通信格式。使用此格式设置(SSIOFR.OMOD[1:0]=00b)，一帧配置有两个系统字，一个用于通道L，另一个用于通道R。SSILRCKSSIFS信号对于通道处于低电平L和通道R为高电平。使用SSICR.LRCKP位设置信号的极性。图38.37显示了没有填充的I2S格式。带填充的格式见图38.36。

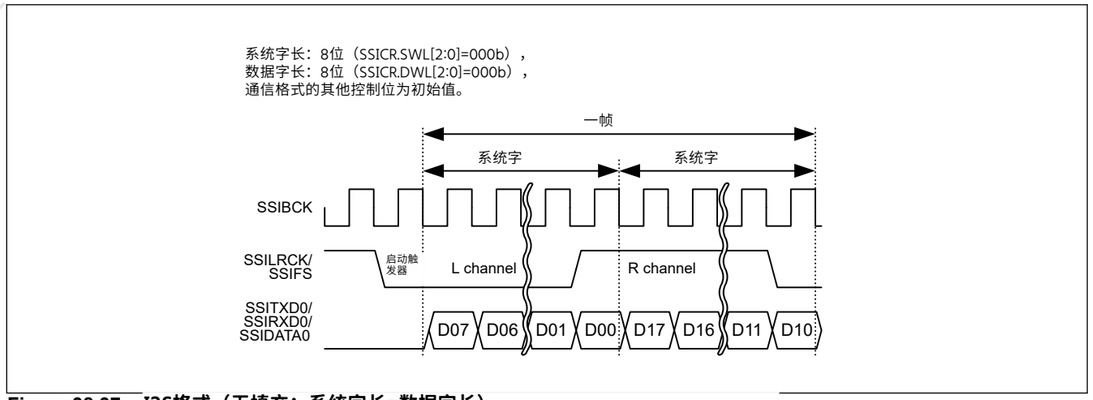


Figure 38.37 I2S格式（无填充：系统字长=数据字长）

SSIE处于空闲状态时外部管脚的状态见38.7.1节。空闲状态。

Note: SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

38.5.2 Monaural Format

单声道格式是用于连接单声道兼容串行设备的通信格式。当指定使用单声道格式(SSIOFR.OMOD[1:0]=10b)时，一帧由一个系统字组成。此外，SSILRCKSSIFS信号的上升沿表示通信开始触发。图38.38和图38.39分别显示了没有和有填充的单声道格式。

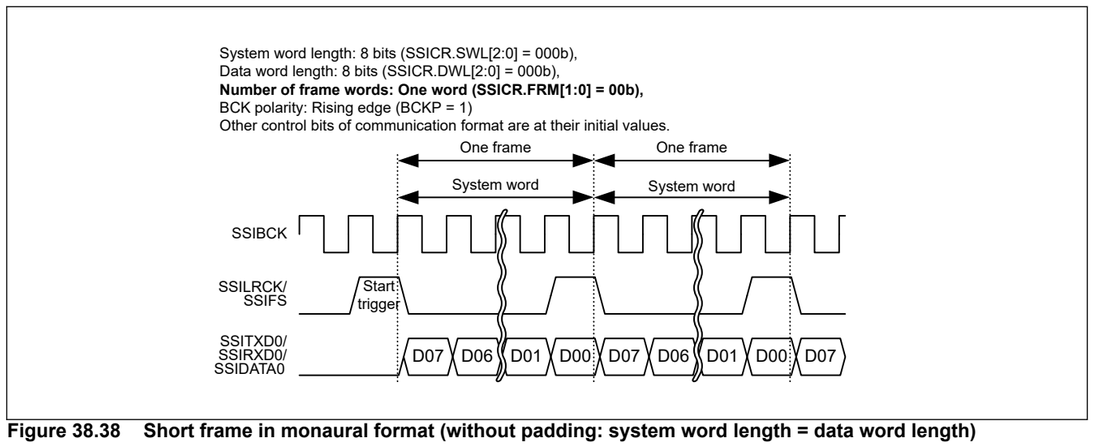


Figure 38.38 Short frame in monaural format (without padding: system word length = data word length)

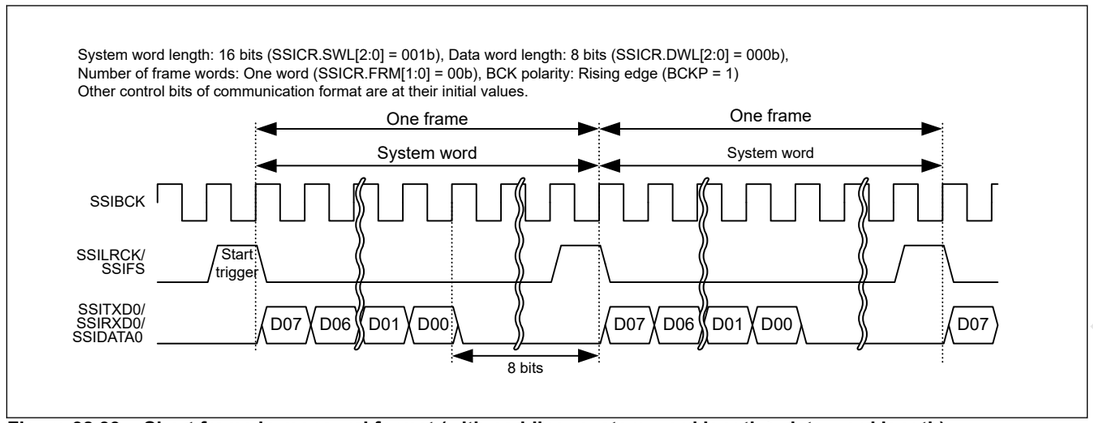


Figure 38.39 Short frame in monaural format (with padding: system word length > data word length)

The monaural formats supported by SSIE consist of short frames and long frames. See section 38.5.2.1. Short frame and section 38.5.2.2. Long frame for the difference between these two frames.

For the state of external pins state when SSIE is in the idle state, see section 38.7.1. Idle State.

Note: SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

38.5.2.1 Short frame

When a short frame is used (SSICR.DEL = 0), the SSILRCK/SSIFS signal indicating the start of serial data is set to high level only for 1 cycle of SSIBCK. Data transfer starts at the falling edge of the signal.

38.5.2.2 Long frame

When a long frame is used (SSICR.DEL = 1), the SSILRCK/SSIFS signal indicating the start of serial data is set to high level only for 2 cycles of SSIBCK. See Figure 38.40. Data transfer starts at the rising edge of the signal.

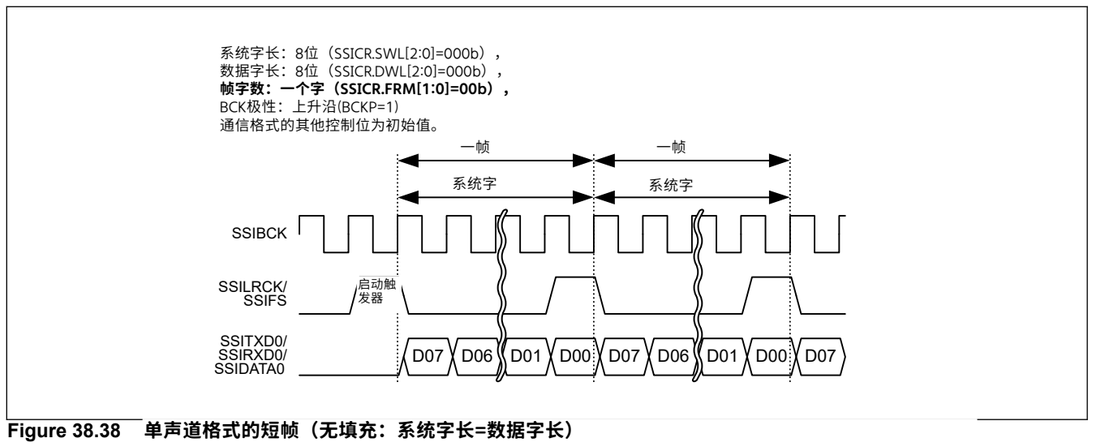


Figure 38.38 单声道格式的短帧（无填充：系统字长=数据字长）

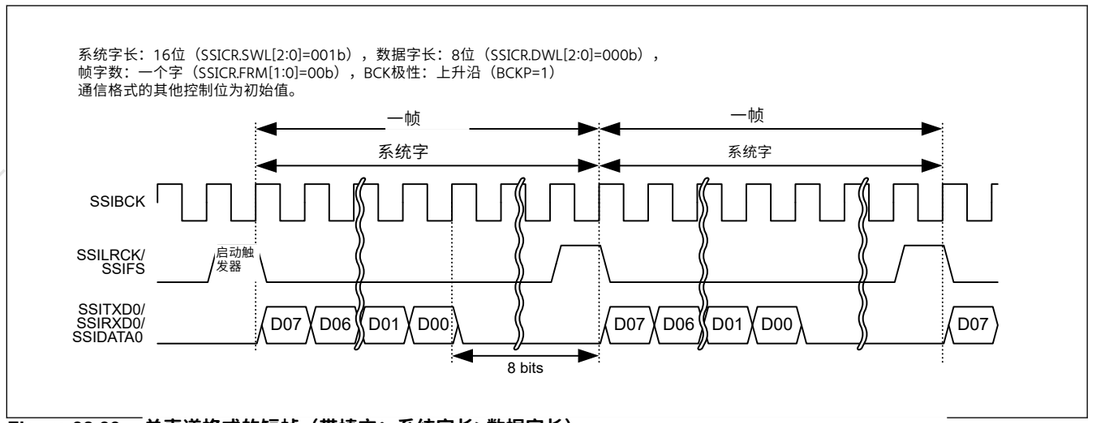


Figure 38.39 单声道格式的短帧（带填充：系统字长>数据字长）

SSIE支持的单声道格式包括短帧和长帧。请参阅第38.5.2.1节。短框架和第38.5.2.2节。长帧为这两个帧的区别。

SSIE处于空闲状态时的外部管脚状态，请参见第38.7.1节。空闲状态。

Note: SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

38.5.2.1 短框

当使用短帧时（SSICR.DEL=0），指示串行数据开始的SSILRCKSSIFS信号仅在SSIBCK的1个周期内设置为高电平。数据传输从信号的下降沿开始。

38.5.2.2 长框

当使用长帧时（SSICR.DEL=1），指示串行数据开始的SSILRCKSSIFS信号仅在SSIBCK的2个周期内设置为高电平。请参见图38.40。数据传输从信号的上升沿开始。

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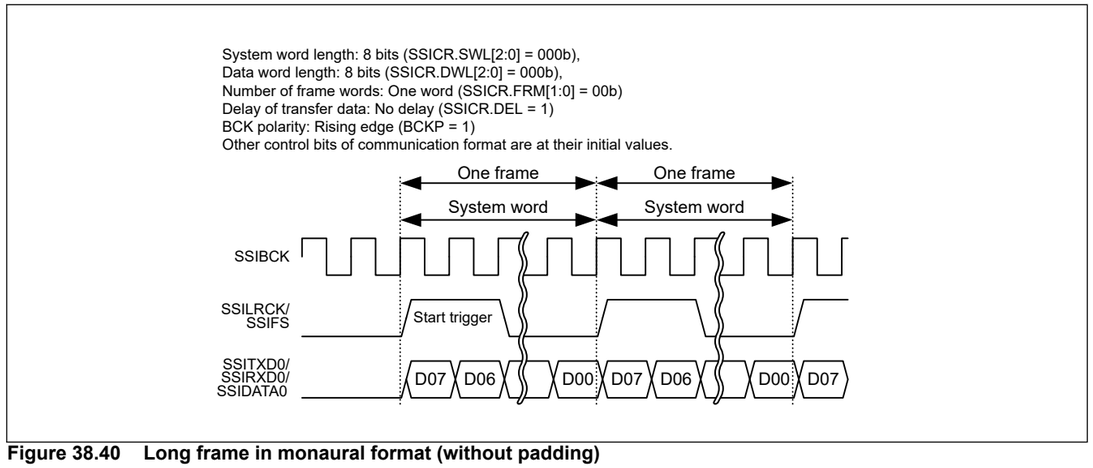

Figure 38.40 Long frame in monaural format (without padding)

38.5.3 TDM Format

The TDM format is a communication format used for connection with TDM-compatible multi-channel devices. With this format setting (SSIOFR.OMOD[1:0] = 01b), one frame is configured with four to eight system words set with the SSICR.FRM[1:0] bits. With this format, the SSILRCK/SSIFS signal is at a high level for the first one system word and at a low level for the rest. The pulse generated on the SSILRCK/SSIFS signal is defined as the SYNC pulse and its rising edge means a start of one frame. Figure 38.41 and Figure 38.42 respectively show the TDM formats without and with padding.

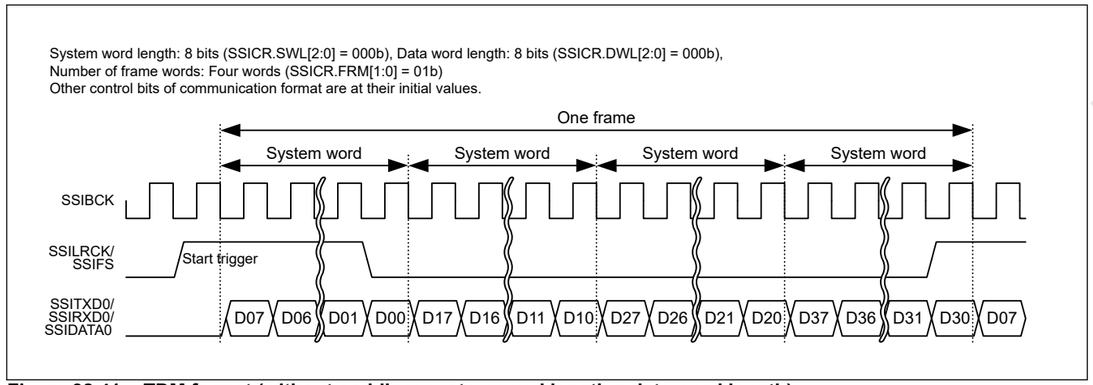

Figure 38.41 TDM format (without padding: system word length = data word length)

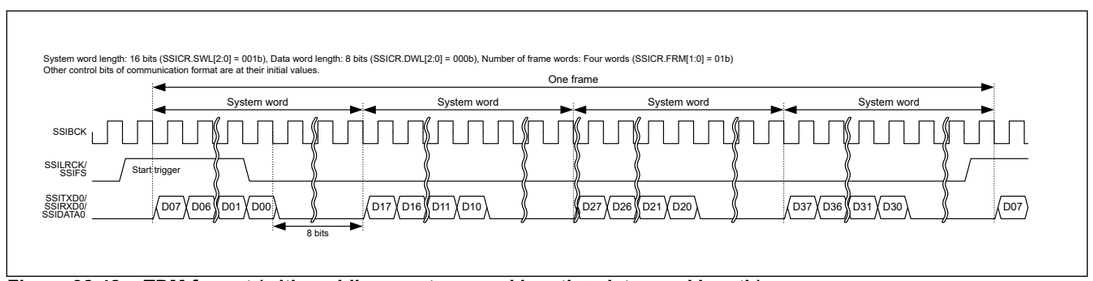

Figure 38.42 TDM format (with padding: system word length > data word length)

For the state of external pins when SSIE is in the idle state, see section 38.7.1. Idle State.

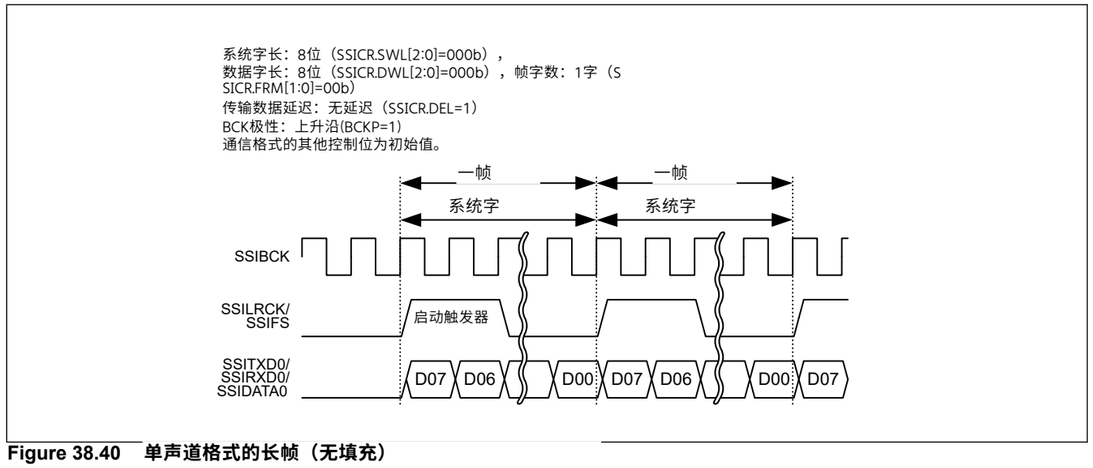

Figure 38.40 单声道格式的长帧（无填充）

38.5.3 TDM Format

TDM格式是一种用于与兼容TDM的多通道设备连接的通信格式。使用此格式设置(SSIOFR.OMOD[1:0]=01b)，一帧配置有四到八个通过SSICR.FRM[1:0]位设置的系统字。使用这种格式，SSILRCKSSIFS信号对于第一个系统字处于高电平，而对于其余系统字处于低电平。SSILRCKSSIFS信号上产生的脉冲被定义为SYNC脉冲，其上升沿表示一帧的开始。图38.41和图38.42分别显示了没有和有填充的TDM格式。

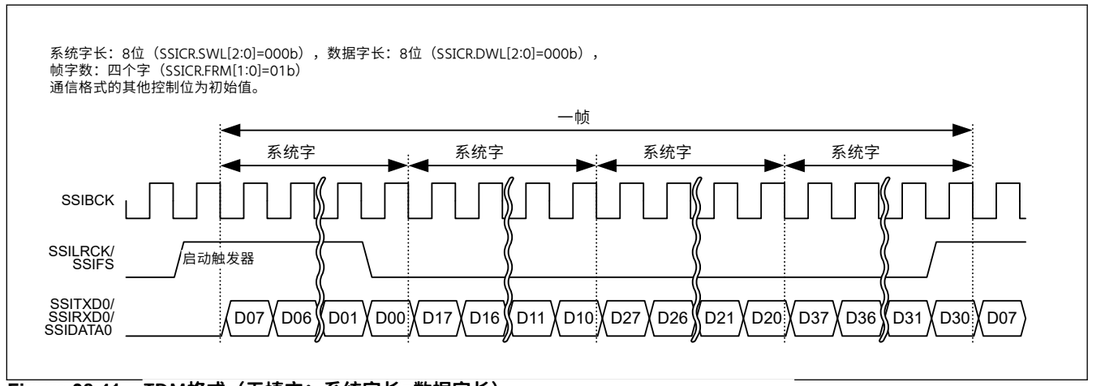

Figure 38.41 TDM格式（无填充：系统字长=数据字长）

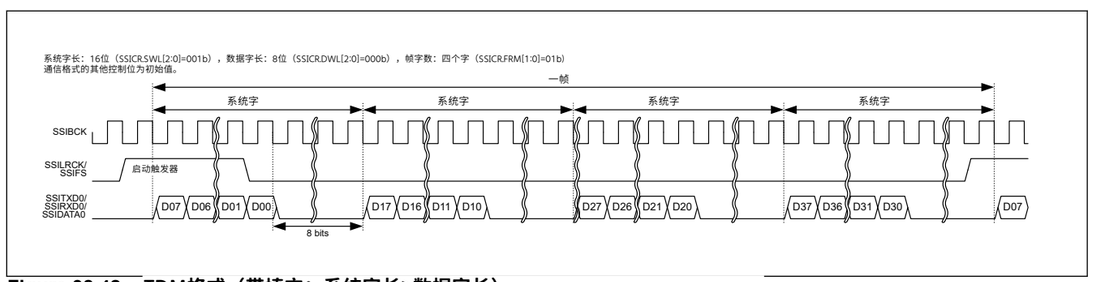

Figure 38.42 TDM格式（带填充：系统字长>数据字长）

SSIE处于空闲状态时外部管脚的状态见38.7.1节。空闲状态。

Note: SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

38.6 Communication Modes

SSIE supports the following communication modes. Table 38.13 lists the control bits that are not available with each communication mode. See section 38.6.1. Slave-mode Communication to section 38.6.5. Transmission and Reception for details of these communication modes.

Table 38.12 Communication modes

Communication Mode	SSICR.MST Bit	SSICR.REN Bit	SSICR.TEN Bit
Slave-mode transmission	0	0	1
Slave-mode reception	0	1	0
Slave-mode transmission and reception	0	1	1
Master-mode transmission	1	0	1
Master-mode reception	1	1	0
Master-mode transmission and reception	1	1	1

Table 38.13 Control bits that cannot be used in each communication mode

Control Bit	Slave-mode Reception	Slave-mode Transmission	Slave-mode Transmission and Reception	Master-mode Reception	Master-mode Transmission	Master-mode Transmission and Reception
SSICR.CKS	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.CKDV	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.MUEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.TEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.REN	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.AUCKEN	Invalid	Invalid	Invalid	Available	Available	Available
SSIFCR.TIE	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RIE	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.TFRST	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RFRST	Available	Invalid	Available	Available	Invalid	Available
SSIOFR.BCKASTP	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.LRCONT	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.OMOD	Available	Available	Available	Available	Available	Available
SSISCR.TDES	Invalid	Available	Available	Invalid	Available	Available
SSISCR.RDFS	Available	Invalid	Available	Available	Invalid	Available

“Invalid” means it has no effect on operation. Writing is possible.

38.6.1 Slave-mode Communication

SSIE operates in slave mode with SSICR.MST = 0. The SSIBCK and SSILRCK/SSIFS signals to be used for serial-data communication must be supplied from an external device. If these signals do not match the communication format set for SSIE, operation is not guaranteed.

38.6.2 Master-mode Communication

SSIE operates in master mode with SSICR.MST = 1. The SSIBCK and SSILRCK/SSIFS signals to be used for serialdata communication must be internally generated from the audio clock. These signals use the format according to the setting of

Note: SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

38.6 通讯方式

SSIE支持以下通信模式。表38.13列出了每种通信模式不可用的控制位。请参阅第38.6.1节。从模式通信到第38.6.5节。有关这些通信模式的详细信息，请参见发送和接收。

Table 38.12 通讯方式

通讯方式	SSICR.MST Bit	SSICR.REN Bit	SSICR.TEN Bit
Slave-mode transmission	0	0	1
Slave-mode reception	0	1	0
从模式发送和接收	0	1	1
Master-mode transmission	1	0	1
Master-mode reception	1	1	0
主模式传输和接收	1	1	1

Table 38.13 不能在每种通信模式下使用的控制位

控制位	Slave-mode Reception	Slave-mode Transmission	Slave-mode 传输和接收	Master-mode Reception	Master-mode Transmission	主模式传输和接收
SSICR.CKS	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.CKDV	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.MUEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.TEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.REN	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.AUCKEN	Invalid	Invalid	Invalid	Available	Available	Available
SSIFCR.TIE	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RIE	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.TFRST	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RFRST	Available	Invalid	Available	Available	Invalid	Available
SSIOFR.BCKASTP	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.LRCONT	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.OMOD	Available	Available	Available	Available	Available	Available
SSISCR.TDES	Invalid	Available	Available	Invalid	Available	Available
SSISCR.RDFS	Available	Invalid	Available	Available	Invalid	Available

“无效”是指对操作没有影响。写作是可能的。

38.6.1 Slave-mode Communication

SSIE在SSICR.MST=0的从机模式下运行。用于串行数据通信的SSIBCK和SSILRCKSSIFS信号必须由外部设备提供。如果这些信号与为SSIE设置的通信格式不匹配，则无法保证操作。

38.6.2 Master-mode Communication

SSIE在SSICR.MST=1的主模式下运行。用于串行数据通信的SSIBCK和SSILRCKSSIFS信号必须由音频时钟在内部生成。这些信号使用根据设置的格式

SSIE. If the communication format the slave device uses does not match the communication format set for SSIE, the operation is unpredictable.

38.6.3 Transmission

SSIE transmits serial data to the other-party device when the SSICR.TEN bit is 1 and the SSICR.REN bit is 0. If the communication format the other-party device uses does not match the communication format set for SSIE, the operation is unpredictable.

38.6.4 Reception

SSIE receives serial data from the other-party device when the SSICR.TEN bit is 0 and the SSICR.REN bit is 1. If the communication format the other-party device uses does not match the communication format set for SSIE, the operation is unpredictable.

38.6.5 Transmission and Reception

SSIE transmits and receives serial data to and from the other-party device when the SSICR.TEN bit is 1 and the SSICR.REN bit is 1. If the communication format the other-party device uses does not match the communication format set for SSIE, the operation is unpredictable.

38.7 Operation

SSIE has the following two main operation states Figure 38.43 shows SSIE state transition.

- Idle state (SSISR.IIRQ = 1)
- Communication state (SSISR.IIRQ = 0).

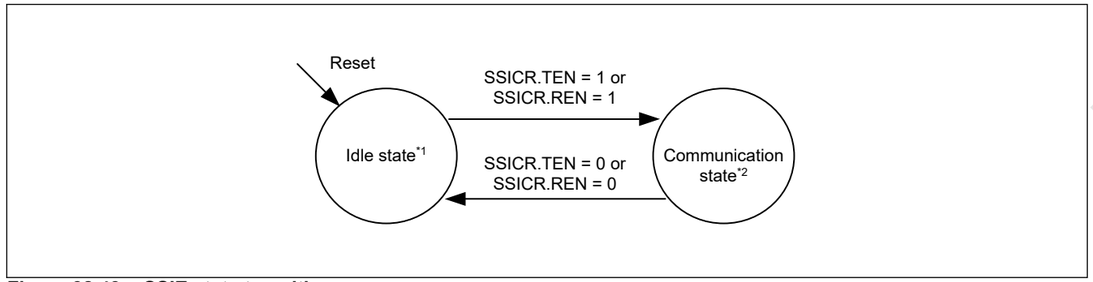

Figure 38.43 SSIE state transition

Note: See section 38.8.1. Start Communication for details of the idle state.
See section 38.8.2. Transmission for details of the communication state.

38.7.1 Idle State

In this state, communication of SSIE is halted. If, however, the SSICR.MST bit is 1, output of the BCK and LR clock/frame synchronization signals to external pins can be controlled according to the settings of SSIOFR.BCKASTP and SSIOFR.LRCONT bits. This function is common to all formats. For details, see Table 38.14.

Table 38.14 Output from external pins in the idle state (1 of 2)

SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	Output from Pins		
			SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA0
0	—	—	Stop	Stop	Stop
1	0	0	Supply	Stop	Stop
1	0	1	Supply	Supply	Stop
1	1	0	Stop	Stop	Stop

SSIE。如果从设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作是不可预测的。

38.6.3 Transmission

当SSICR.TEN位为1且SSICR.REN位为0时，SSIE向对方设备发送串口数据。如果对方设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作为不可预料的。

38.6.4 Reception

当SSICR.TEN位为0且SSICR.REN位为1时，SSIE从对方设备接收串行数据。如果对方设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作为不可预料的。

38.6.5 传输和接收

当SSICR.TEN位为1且
SSICR.REN位为1。如果对方设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作不可预知。

38.7 Operation

SSIE有以下两个主要操作状态图38.43显示了SSIE状态转换。

●空闲状态（SSISR.IIRQ=1）

●通信状态（SSISR.IIRQ=0）。

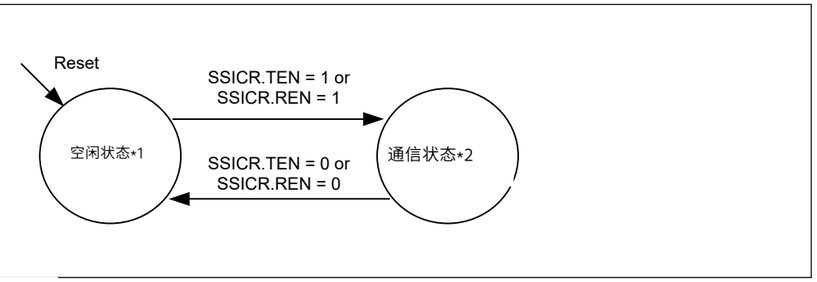

Figure 38.43 SSIE状态转换

Note: 请参阅第38.8.1节。开始通信以了解空闲状态的详细信息。
请参阅第38.8.2节。传输以获取通信状态的详细信息。

38.7.1 空闲状态

在这种状态下，SSIE的通信停止。但是，如果SSICR.MST位为1，则可以根据SSIOFR.BCKASTP和SSIOFR.LRCONT位的设置来控制向外部引脚输出BCK和LR时钟帧同步信号。此功能适用于所有格式。详见表38.14。

Table 38.14 空闲状态下外部引脚的输出（2个中的1个）

SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	引脚输出		
			SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA0
0	—	—	Stop	Stop	Stop
1	0	0	Supply	Stop	Stop
1	0	1	Supply	Supply	Stop
1	1	0	Stop	Stop	Stop

Table 38.14 Output from external pins in the idle state (2 of 2)

SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	Output from Pins		
			SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA0
1	1	1	Stop	Supply	Stop

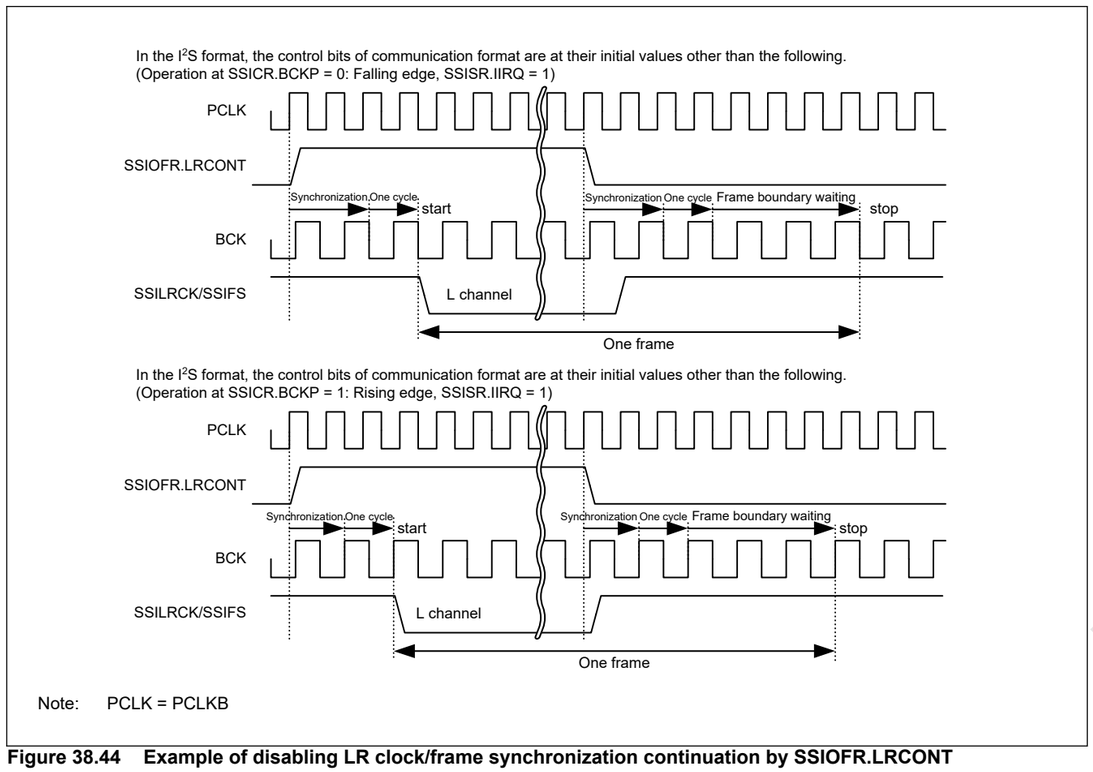

Figure 38.44 Example of disabling LR clock/frame synchronization continuation by SSIOFR.LRCONT

Note: To stop the output to the SSILRCK/SSIFS pin with SSIOFR.LRCONT when SSIE is in the idle state in mastermode communication (SSICR.MST = 1), note the following: The output stops when the value of the SSIOFR.LRCONT bit is changed from 1 to 0. Make sure that the other-party device is not affected.

Table 38.14 空闲状态下外部引脚的输出（2个中的2个）

SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	引脚输出		
			SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA0
1	1	1	Stop	Supply	Stop

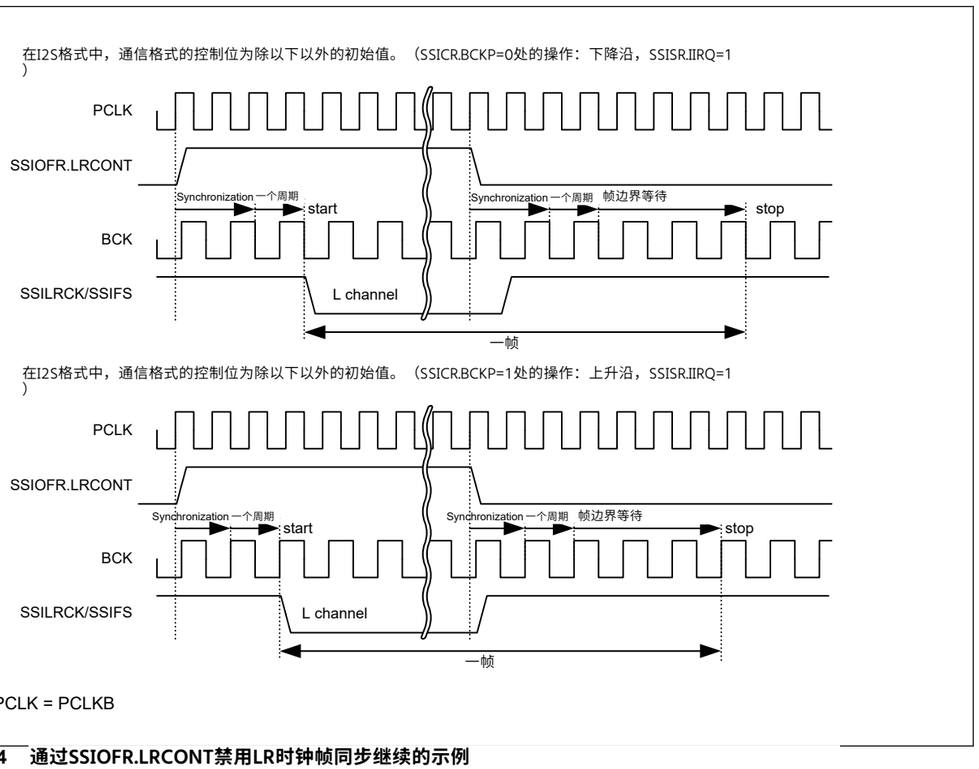

Figure 38.44 通过SSIOFR.LRCONT禁用LR时钟帧同步继续的示例

Note: 要在主模式通信（SSICR.MST=1）中SSIE处于空闲状态时通过SSIOFR.LRCONT停止向SSILRCKSSIFS引脚的输出，请注意以下几点：当SSIOFR.LRCONT位的值从1比0。确保对方设备不受影响。

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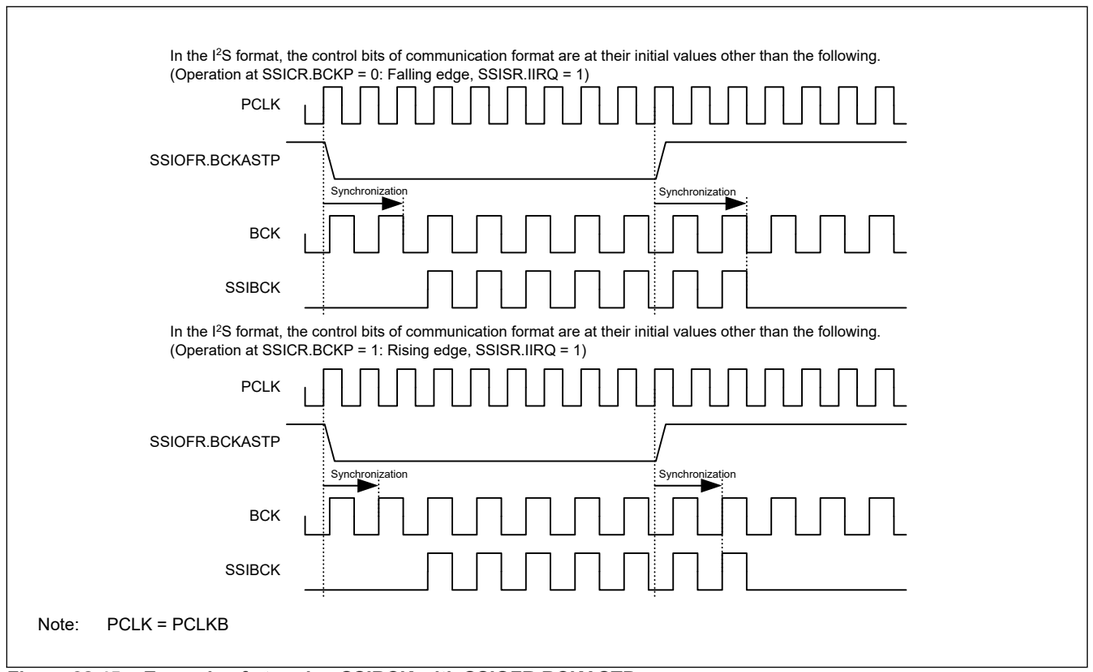


Figure 38.45 Example of stopping SSIBCK with SSIOFR.BCKASTP

Note: To stop the output to the SSIBCK pin with SSIOFR.BCKASTP in master-mode communication (SSICR.MST = 1) and while SSIE is in the idle state, note the following: The output stops when the value of the SSIOFR.BCKASTP bit is changed from 0 to 1. So, make sure that the other-party device is not affected.

38.7.2 Communication States

In this state, SSIE is during communication. Figure 38.46 shows transitions of communication states and Table 38.15 lists the conditions for transition. If the transition condition is not satisfied, the state does not transit.

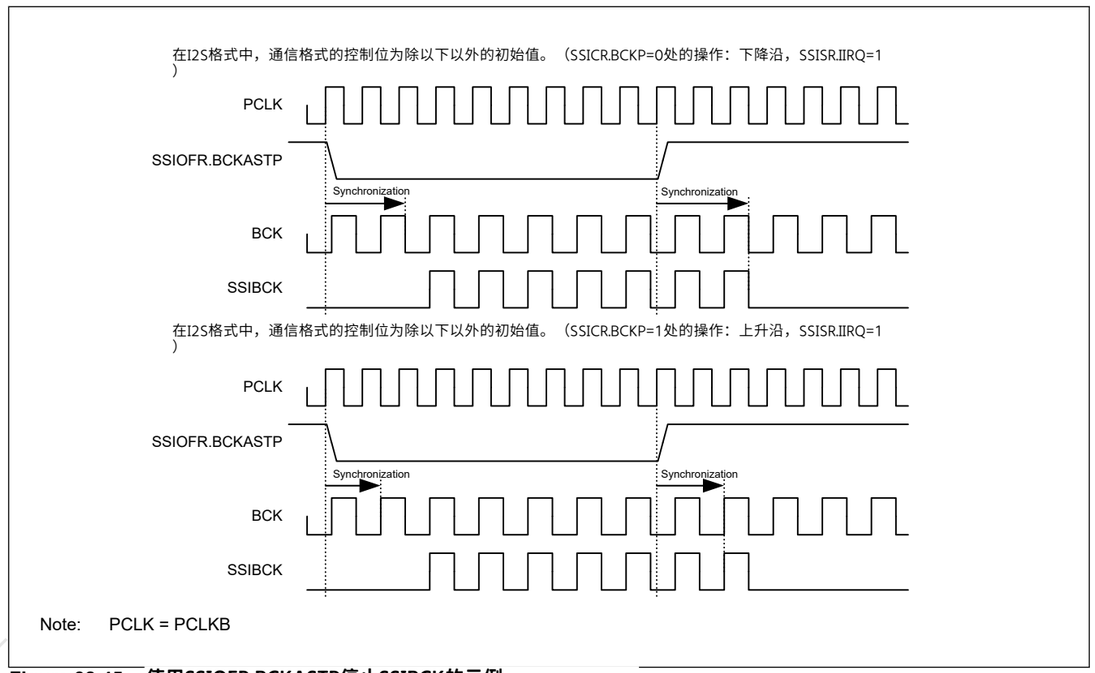


Figure 38.45 使用SSIOFR.BCKASTP停止SSIBCK的示例

Note: 要在主模式通信(SSICR.MST=1)和SSIE处于空闲状态时使用SSIOFR.BCKASTP停止向SSIBCK引脚的输出，请注意以下几点：当SSIOFR.BCKASTP位的值为从0变为1。因此，请确保对方设备不受影响。

38.7.2 通讯状态

在此状态下，SSIE处于通信过程中。图38.46显示了通信状态的转换，表38.15列出了转换的条件。如果不满足转移条件，则状态不转移。

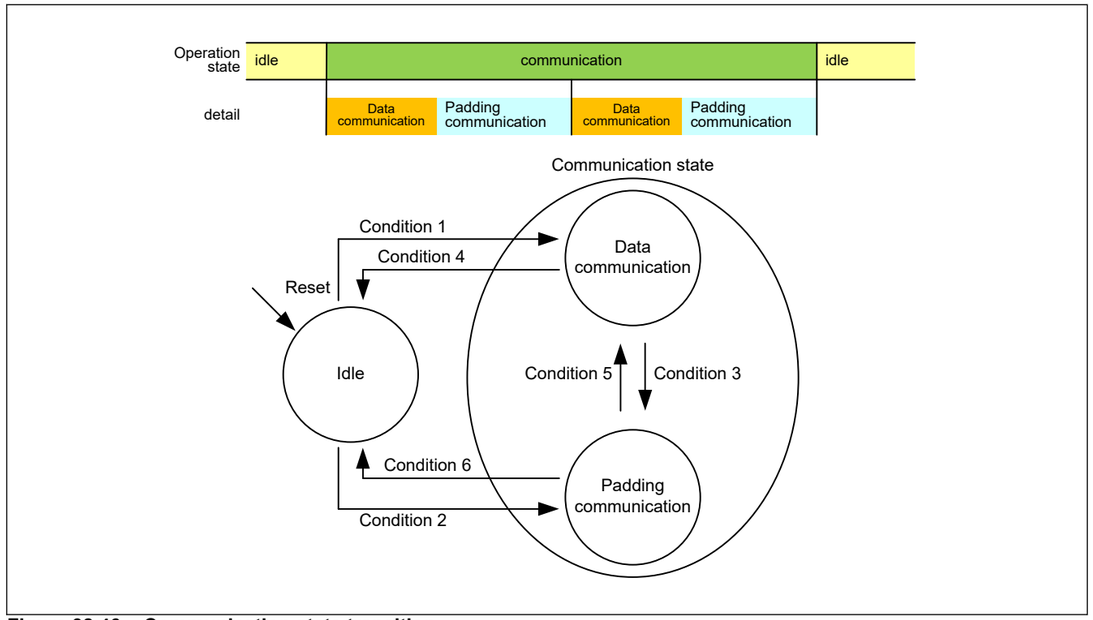


Figure 38.46 Communication state transition

Table 38.15 Condition for communication state transition

Condition Number	Condition for Transition
1	Writing SSICR.TEN = 1 or SSICR.REN = 1 while SSICR.SDTA = 0 or in the setting without padding bits.
2	Writing SSICR.TEN = 1 or SSICR.REN = 1 while SSICR.SDTA = 1 and in the setting with padding bits.
3	The following three conditions are all met: • SSICR.TEN = 1 or SSICR.REN = 1 • In the setting with padding bits • The last bit of the data words has been transferred.
4	Both the following two conditions are met: • SSICR.SDTA = 1 or without padding bits • While SSICR.TEN = 0 and SSICR.REN = 0, the last bit of the data words in a frame has been transferred.
5	Transfer of the last padding bit is completed while SSICR.TEN = 1 or SSICR.REN = 1
6	Both the following two conditions are met: • SSICR.SDTA = 0 and with padding bits • While SSICR.TEN = 0 and SSICR.REN = 0, the last padding bit has been transferred.

See Table 38.11 for the setting with/without padding bits.

38.7.2.1 Data communication state

In this state, SSIE is during communication. Data of the data word length set with the SSICR.DWL[2:0] bits is transmitted, received, or transmitted and received.

- State Transition in the Setting without Padding Bits

During communication (SSISR.IIRQ = 0), SSIE is during data communication for all the time. By disabling transmission and reception (SSICR.TEN = 0, SSICR.REN = 0), SSIE transits to the idle state. For details, see Figure 38.47 and Figure 38.48.

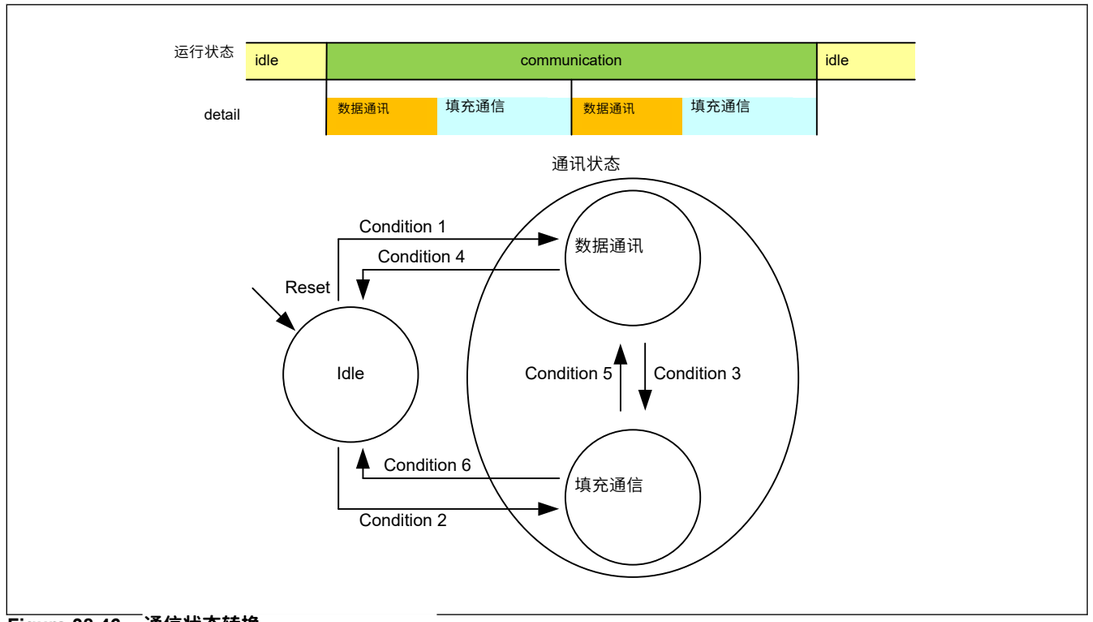


Figure 38.46 通信状态转换

Table 38.15 通信状态转移的条件

条件编号	过渡条件
1	在SSICR.SDTA=0或在没有填充位的设置中写入SSICR.TEN=1或SSICR.REN=1。
2	写入SSICR.TEN=1或SSICR.REN=1而SSICR.SDTA=1并在设置中使用填充位。
3	满足以下三个条件：● • 在带有填充位的设置中 • 数据字的最后一位已传输。
4	同时满足以下两个条件：● SSICR.SDTA=1或无填充位 • 当SSICR.TEN=0和SSICR.REN=0时，帧中数据字的最后一位已被传输。
5	当SSICR.TEN=1或SSICR.REN=1时，最后一个填充位的传输完成
6	同时满足以下两个条件：● SSICR.SDTA=0并带有填充位 • 当SSICR.TEN=0和SSICR.REN=0时，最后一个填充位已被传输。

有关不带填充位的设置，请参见表38.11。

38.7.2.1 数据通讯状态

在此状态下，SSIE处于通信过程中。使用SSICR.DWL[2:0]位设置的数据字长的数据被发送、接收或发送和接收。

●无填充位设置中的状态转换

在通信期间（SSISR.IIRQ=0），SSIE一直处于数据通信期间。通过禁用发送和接收（SSICR.TEN=0，SSICR.REN=0），SSIE转换到空闲状态。详见图38.47和图38.48。

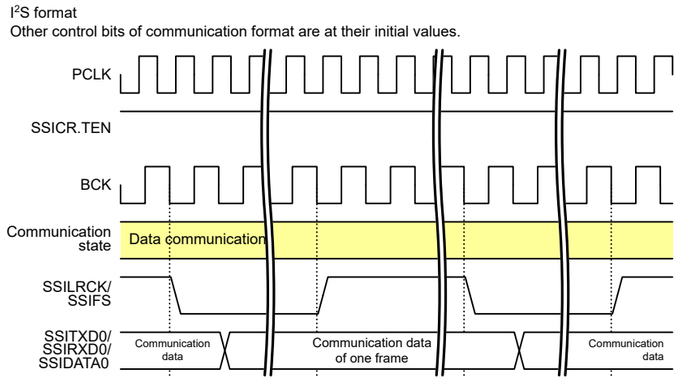


Figure 38.47 Continuation of the data communication

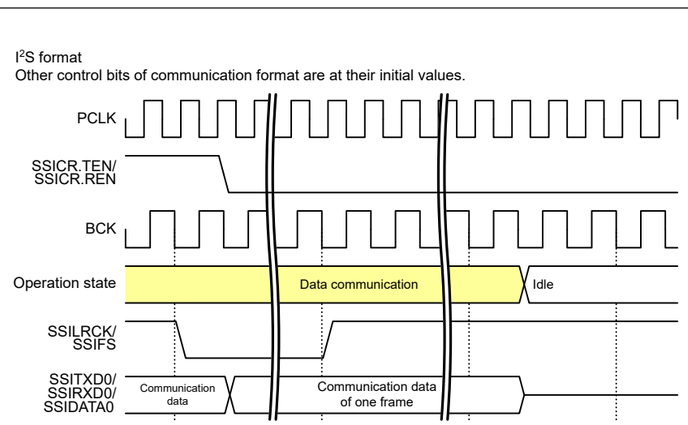


Figure 38.48 Halt from the data communication (without padding bits)

- State Transition in the Setting with Padding Bits

When SSIE ends transfer of the last bit of a data word during communication (SSISR.IIRQ = 0), SSIE transitions from the data communication state to the padding communication state in Figure 38.49. Except in the status with SSICR.SDTA = 1 and transmission and reception disabled (SSICR.TEN = 0 and SSICR.REN = 0), SSIE transitions from the data communication state to the idle state when it stops communication in Figure 38.51.

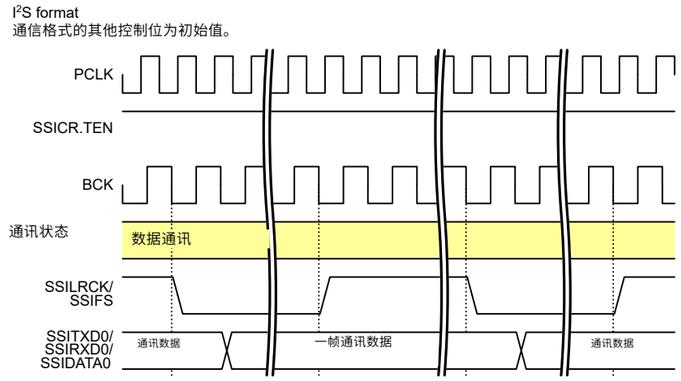


Figure 38.47 继续数据通信

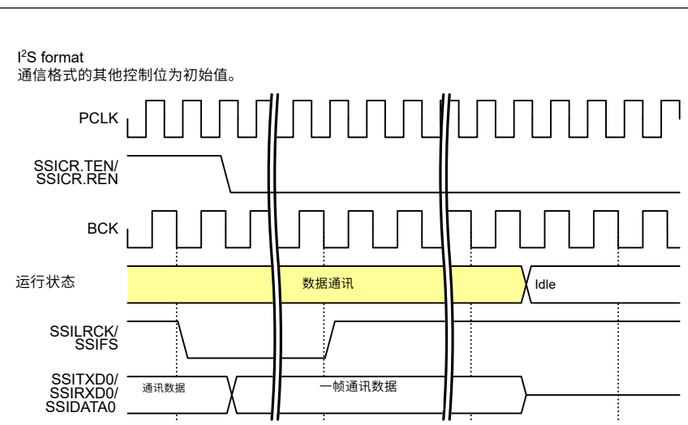


Figure 38.48 停止数据通信（无填充位）

●具有填充位的设置中的状态转换

当SSIE在通信期间结束数据字的最后一位传输时（SSISR.IIRQ=0），SSIE从数据通信状态转换到图38.49中的填充通信状态。除了在SSICR.SDTA=1和发送和接收禁用的状态下（SSICR.TEN=0和SSICR.REN=0），SSIE在图38.51中停止通信时从数据通信状态转换到空闲状态。

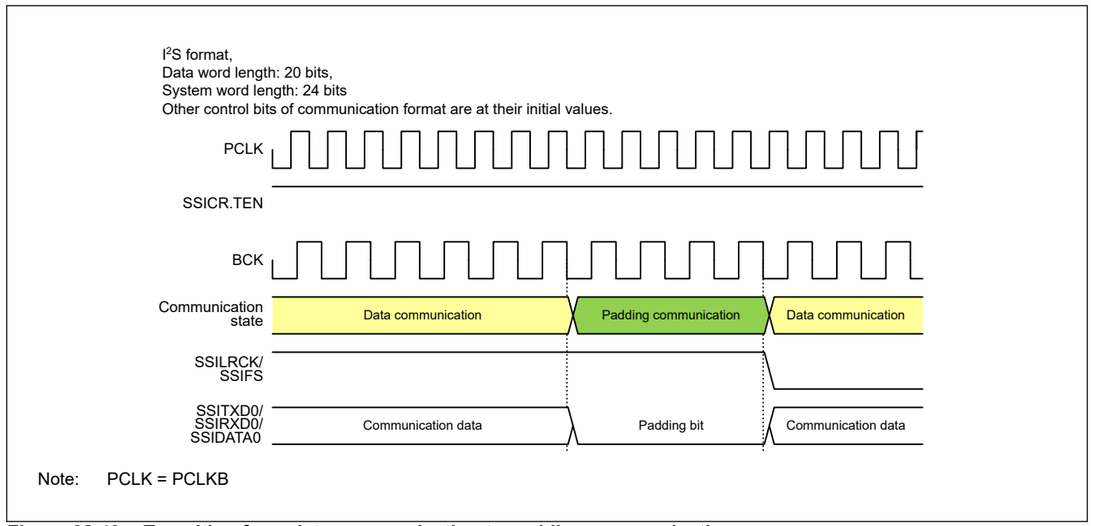


Figure 38.49 Transition from data communication to padding communication

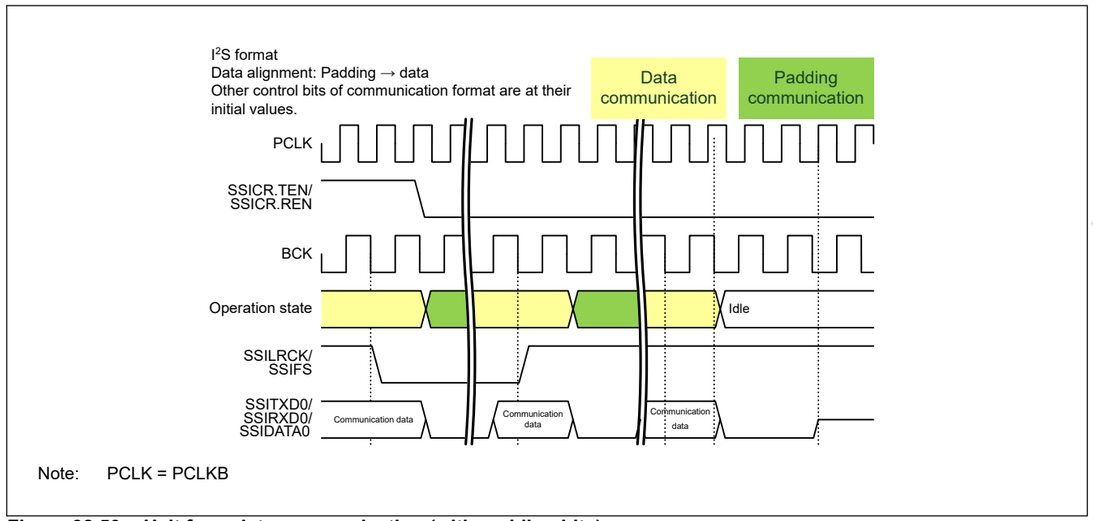


Figure 38.50 Halt from data communication (with padding bits)

38.7.2.2 Padding communication

In this state, SSIE is during communication. The padding bits set with the SSICR.SWL[2:0] bits and SSICR.DWL[2:0] bits are transmitted, received, or transmitted and received.

- State Transition in the Setting with Padding Bits

When SSIE ends transfer of the last padding bit during communication (SSISR.IIRQ = 0), SSIE transitions to the data communication state in Figure 38.49. If SSIE is in the status with SSICR.SDTA = 0 and transmission and reception disabled (SSICR.TEN = 0 and SSICR.REN = 0), SSIE transitions from the padding communication state to the idle state when it stops communication in Figure 38.51.

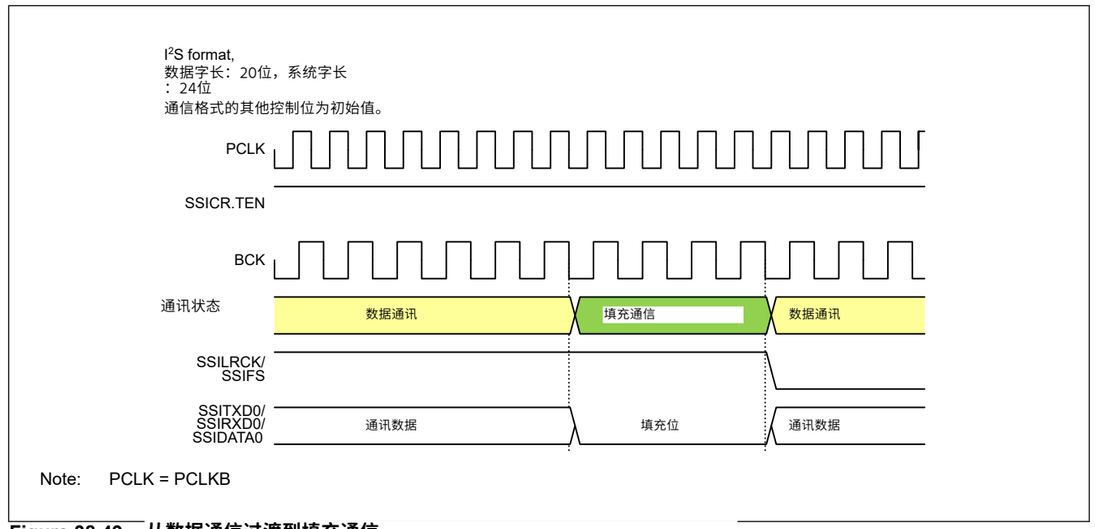


Figure 38.49 从数据通信过渡到填充通信

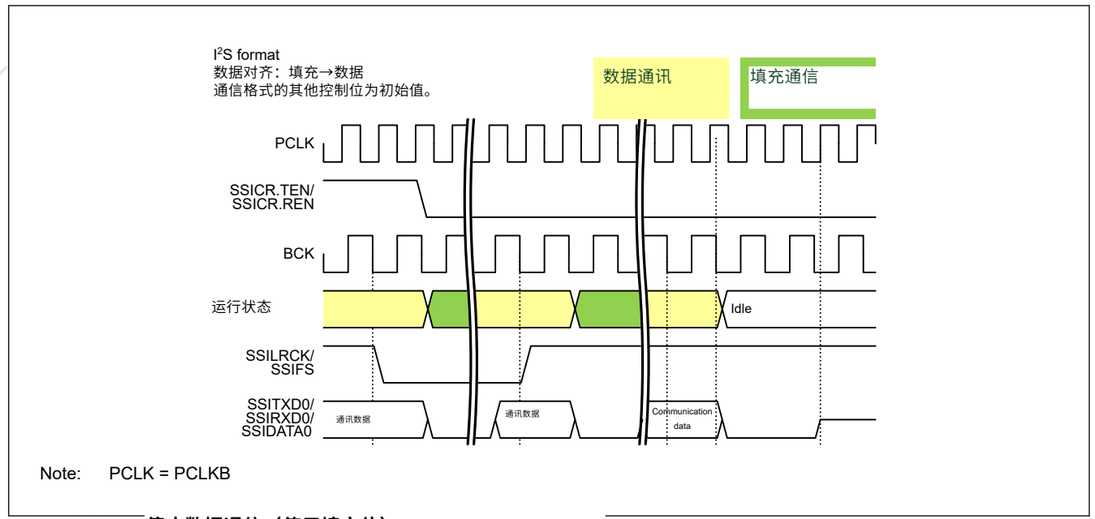


Figure 38.50 停止数据通信（使用填充位）

38.7.2.2 填充通信

在此状态下，SSIE处于通信过程中。使用SSICR.SWL[2:0]位和SSICR.DWL[2:0]位设置的填充位被发送、接收或发送和接收。

●具有填充位的设置中的状态转换

当SSIE在通信期间结束最后一个填充位的传输（SSISR.IIRQ=0）时，SSIE转换到图38.49中的数据通信状态。如果SSIE处于SSICR.SDTA=0且发送和接收禁用的状态（SSICR.TEN=0和SSICR.REN=0），则SSIE在图38.51中停止通信时从填充通信状态转换为空闲状态。

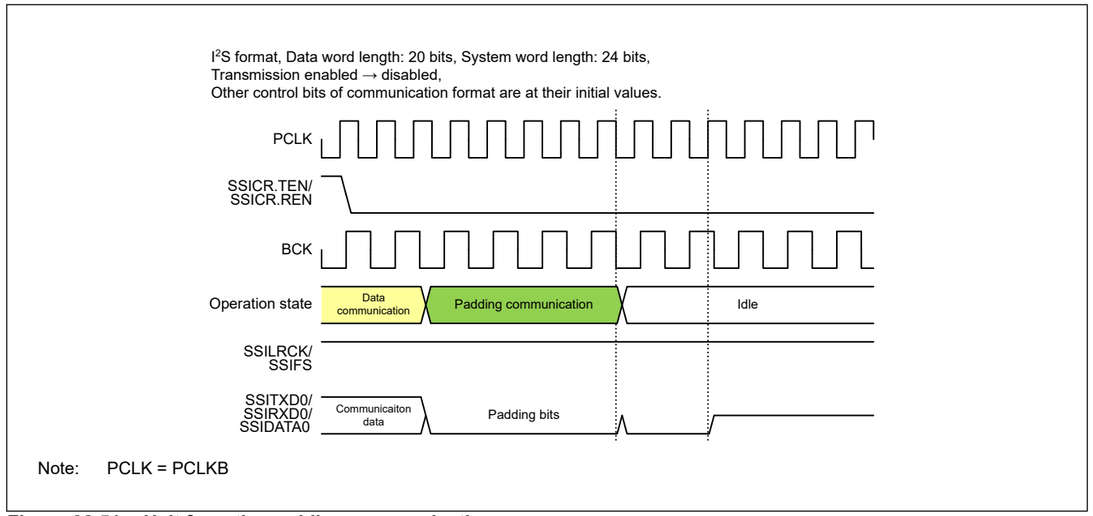


Figure 38.51 Halt from the padding communication

38.8 Communication Operation

Figure 38.52 shows the communication flow of SSIE.

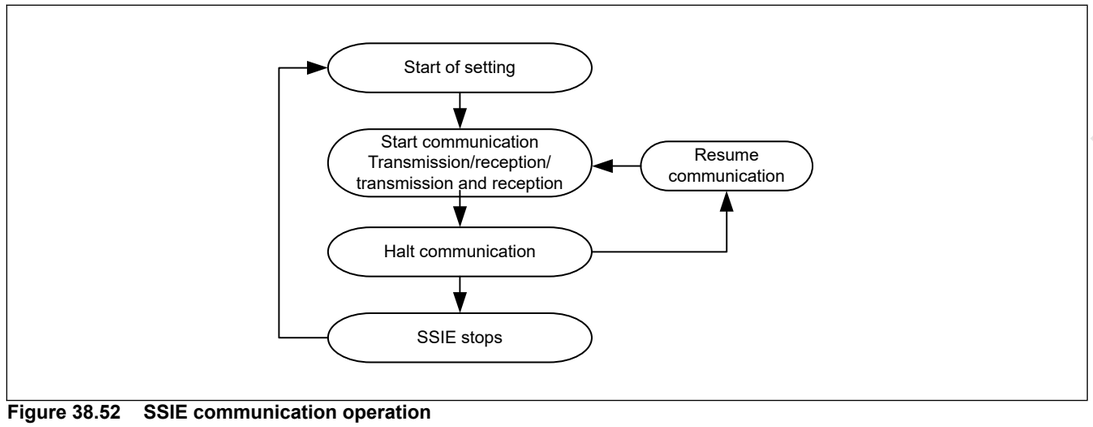


Figure 38.52 SSIE communication operation

The procedure of each operation is described from section 38.8.1. Start Communication to section 38.8.7. Resume Communication.

38.8.1 Start Communication

This section describes how to start communication of SSIE. Figure 38.53 shows the procedure to start communication. Be sure to follow the procedure. See section 38.8.2. Transmission for transmission operation and section 38.8.3. Reception for reception operation.

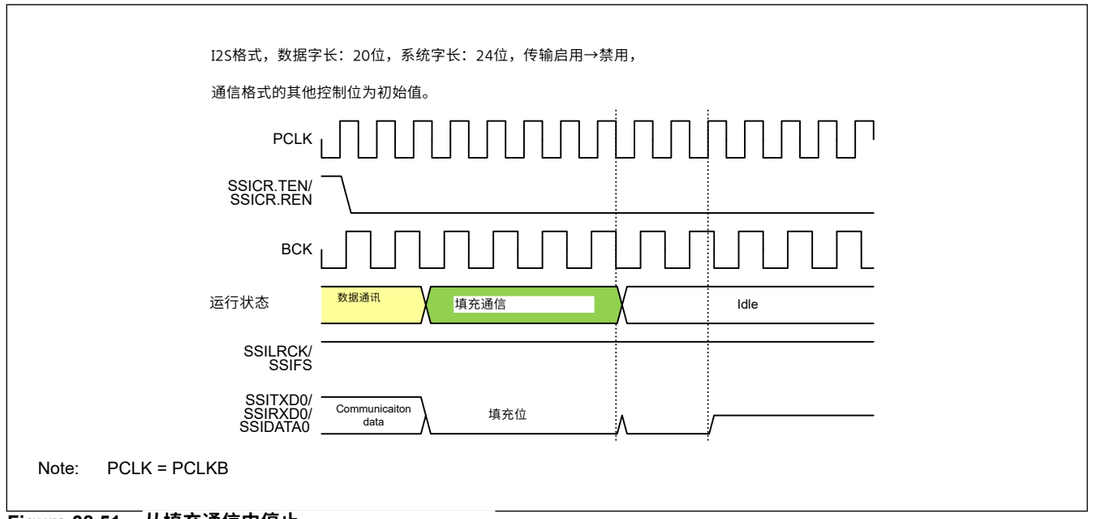


Figure 38.51 从填充通信中停止

38.8 通讯操作

图38.52显示了SSIE的通信流程。

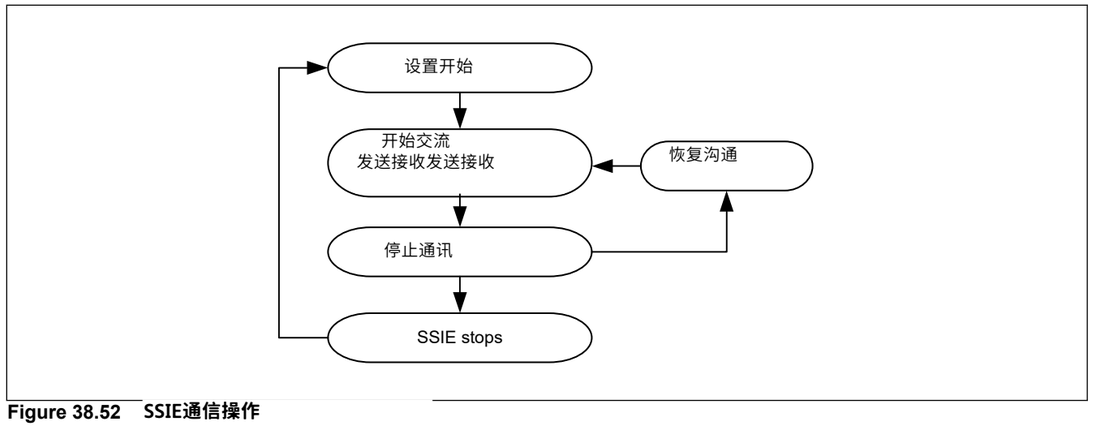
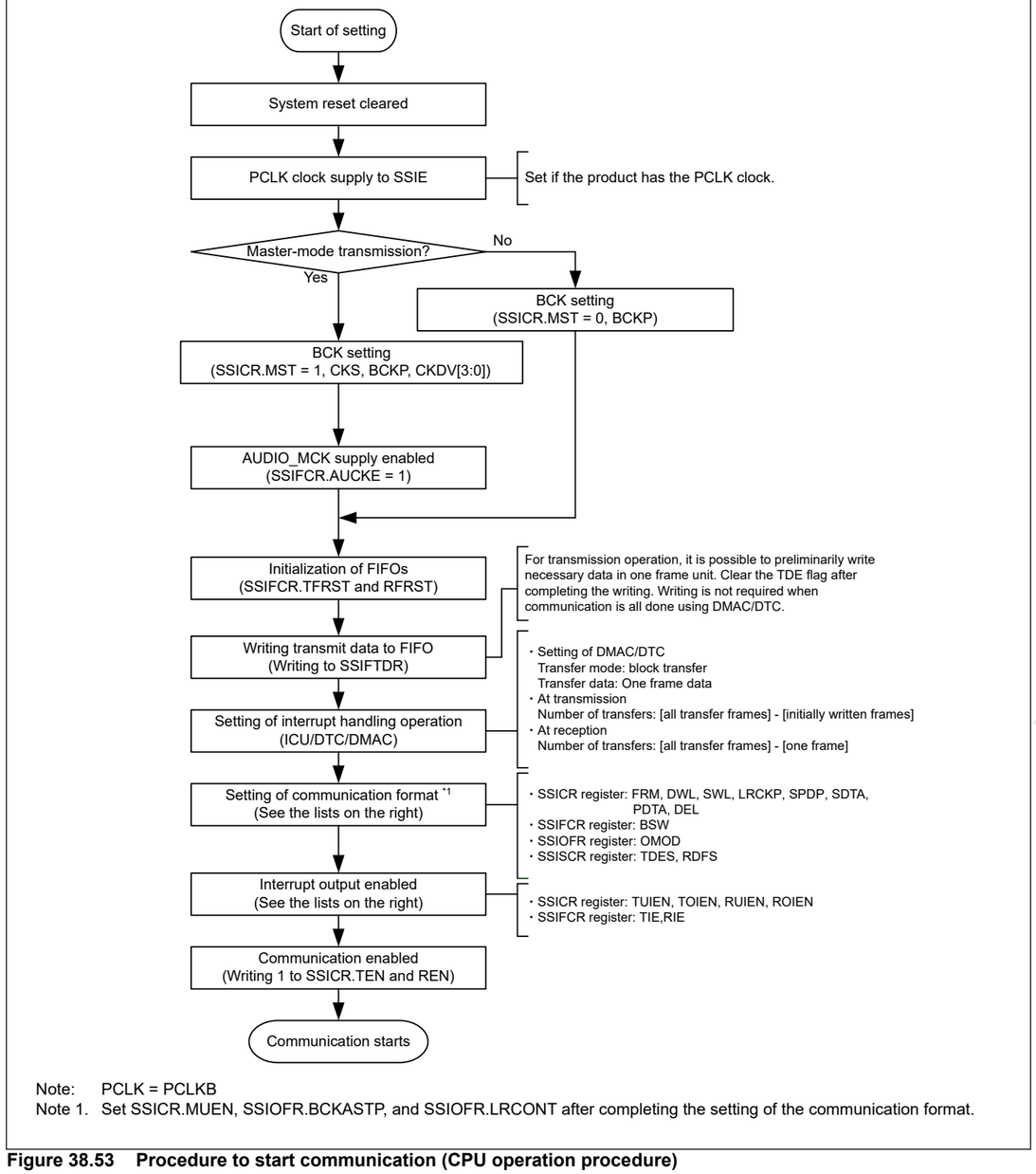


Figure 38.52 SSIE通信操作

每个操作的过程在第38.8.1节中描述。开始与第38.8.7节的通信。恢复Communication.

38.8.1 开始沟通

本节介绍如何启动SSIE通信。图38.53显示了开始通信的过程。请务必遵守程序。请参阅第38.8.2节。传输操作和第38.8.3节的传输。接收操作的接收。



Note: PCLK = PCLKB
Note 1. Set SSICR.MUEN, SSIOFR.BCKASTP, and SSIOFR.LRCONT after completing the setting of the communication format.

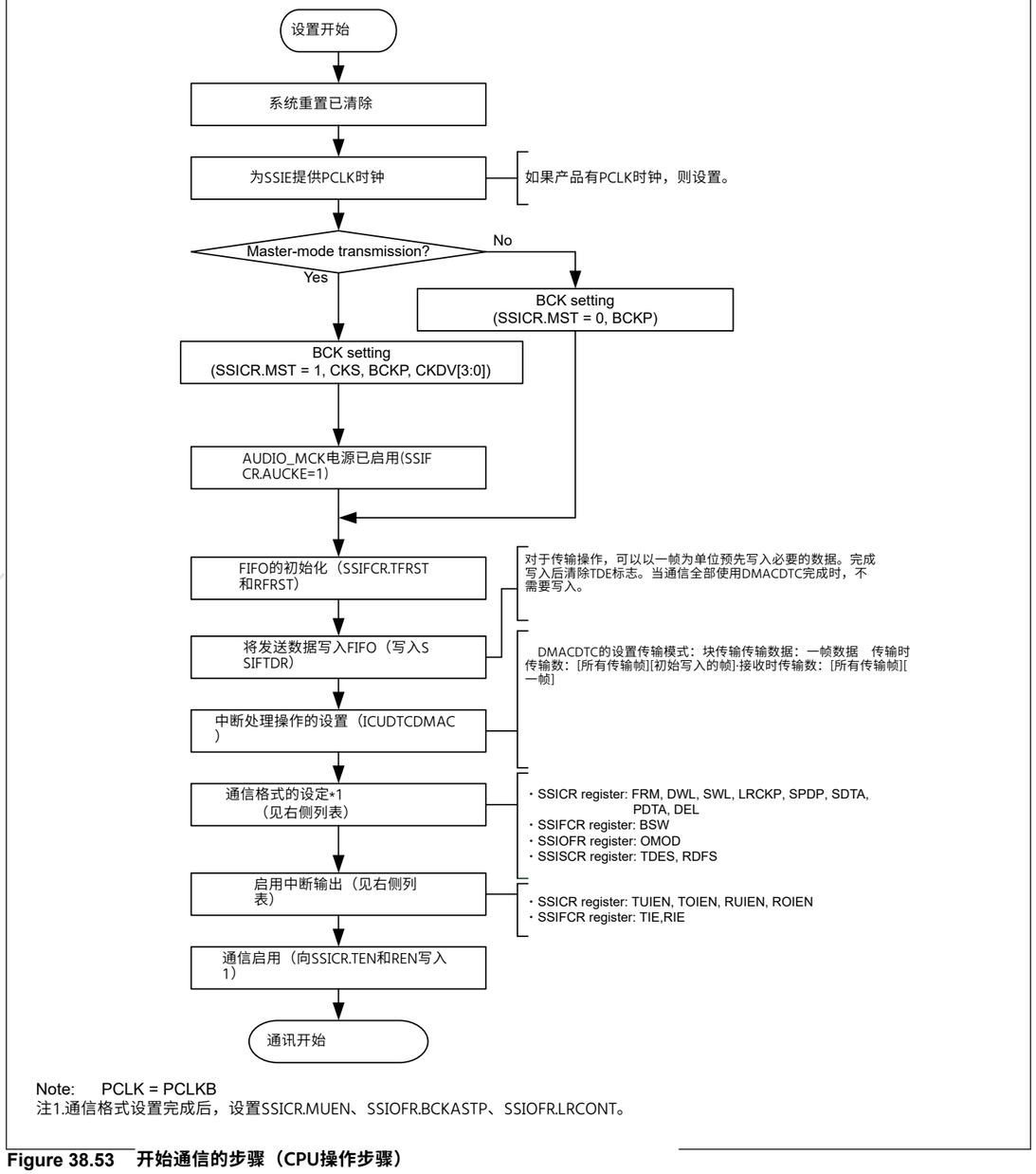
Figure 38.53 Procedure to start communication (CPU operation procedure)

SSIE can perform continuous communication based on interrupts by the DTC/DMAC. For transmission, write 1 to SSIFCR.TIE, SSICR.TUIEN, and SSICR.TOIEN. For reception, write 1 to SSIFCR.RIE, SSICR.RUIEN, and SSICR.ROIEN.

38.8.2 Transmission

The transmission procedure in Figure 38.54 must be followed throughout a transmission operation.

After transmission is enabled (SSICR.TEN = 1 and SSICR.REN = 0), SSIE starts transmission when a start trigger is generated by SSILRCK/SSIFS with the serial data for at least a frame contained in the transmit FIFO data register



Note: PCLK = PCLKB
注1.通信格式设置完成后，设置SSICR.MUEN、SSIOFR.BCKASTP、SSIOFR.LRCONT。

Figure 38.53 开始通信的步骤（CPU操作步骤）

SSIE可以根据DTCDMAC的中断执行连续通信。对于传输，写入1到SSIFCR.TIE、SSICR.TUIEN和SSICR.TOIEN。对于接收，将1写入SSIFCR.RIE、SSICR.RUIEN和SSICR.ROIEN.

38.8.2 Transmission

在整个传输操作中必须遵循图38.54中的传输过程。

使能传输后（SSICR.TEN=1和SSICR.REN=0），当SSILRCKSSIFS使用发送FIFO数据寄存器中包含的至少一帧的串行数据生成启动触发时，SSIE开始传输

(SSIFTDR). SSIE outputs a transmit data empty interrupt to the DTC/DMAC according to the TDE setting condition (SSISCR.TDES) and the status of transmit data empty interrupt enable (SSIFCR.TIE) bit specified in the communication start procedure. This interrupt requests writing to the transmit FIFO data register (SSIFTDR). In the communication start procedure, specify writing to the transmit FIFO data register (SSIFTDR) as the DTC/DMAC operation in response to the transmit data empty interrupt. With this setting, SSIE can continuously transmit data not through the CPU. The transmit data empty interrupt is generated when the free space size of transmit FIFO data register reaches the value set in SSISCR.TDES. The number of times of writing must be specified in accordance with the free space size of the transmit FIFO data register indicated by the transmit data empty interrupt. If an error occurs, perform the error-handling procedure as instructed in the communication stop procedure.

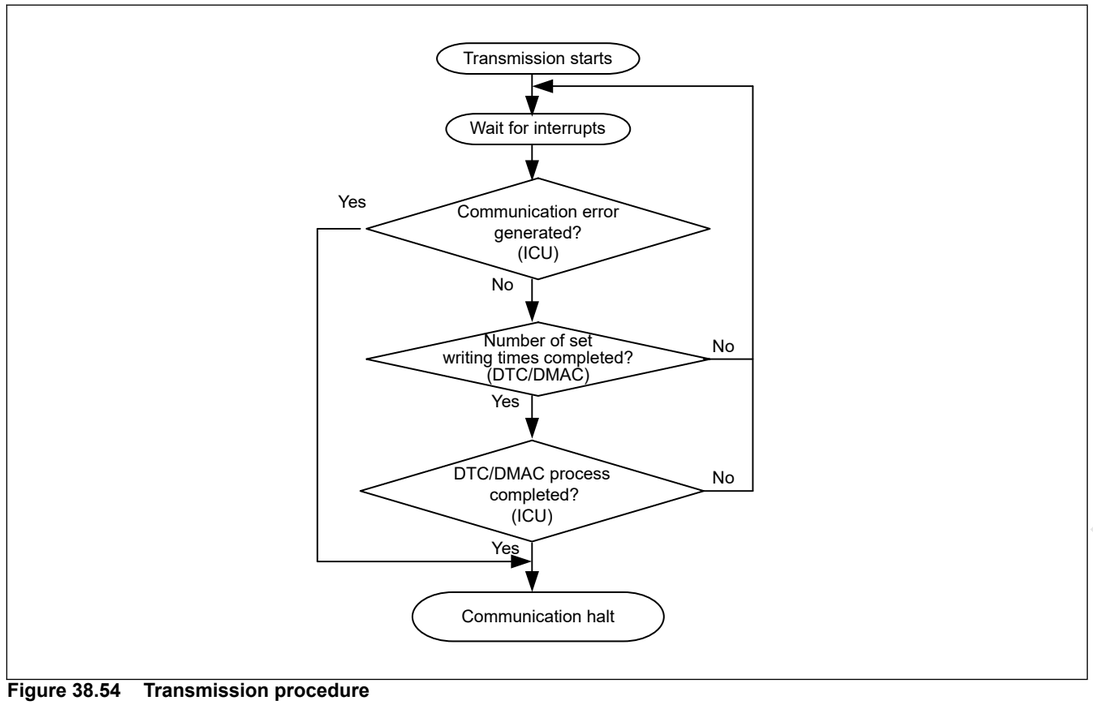


Figure 38.54 Transmission procedure

Note: The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.TDE to write data to SSIFTDR. The number of times of writing data to SSIFTDR by detecting the value 1 of SSIFSR.TDE must be in accordance with the free space size of the transmit FIFO data register specified by SSISCR.TDES. After as much transmit data as the free space size is written to SSIFTDR, the SSIFSR.TDE flag must be cleared. Continuous transmission is enabled by repeating data writing. If the SSIFSR.TDE flag is not cleared, the flag is not cleared automatically.

38.8.3 Reception

The reception procedure in Figure 38.55 must be followed throughout a reception operation.

After reception is enabled (SSICR.TEN = 0 and SSICR.REN = 1), SSIE starts reception when a start trigger is generated by SSILRCK/SSIFS. SSIE outputs a receive data full interrupt to the DTC/DMAC according to the RDF setting condition (SSISCR.RDFS) and the status of receive data full interrupt enable (SSIFCR.RIE) bit specified in the communication start procedure. This interrupt requests data reading from the receive FIFO data register (SSIFRDR). In the communication start procedure, specify reading from the receive FIFO data register (SSIFRDR) as the DTC/DMAC operation in response to the receive data full interrupt. With this setting, SSIE can continuously read data not through the CPU. The receive data full interrupt is generated when data as much as the capacity of receive FIFO data register has been stored. The number of times of reading must be specified in accordance with the data size of the receive FIFO data register indicated by the receive data full interrupt. If an error occurs, perform the error-handling procedure as instructed in the communication stop procedure.

(SSIFTDR)。SSIE根据通信启动过程中指定的TDE设置条件(SSISCR.TDES)和发送数据空中断使能(SSIFCR.TIE)位的状态，向DTCDMAC输出一个发送数据空中断。该中断请求写入发送FIFO数据寄存器(SSIFTDR)。在通信开始过程中，将写入发送FIFO数据寄存器(SSIFTDR)指定为DTCDMAC操作以响应发送数据空中断。使用此设置，SSIE可以不通过CPU连续传输数据。当发送FIFO数据寄存器的可用空间大小达到SISSCR.TDES中设置的值时，将产生发送数据空中断。写入次数必须根据发送数据空中断指示的发送FIFO数据寄存器的空闲空间大小来指定。如果发生错误，请按照通信停止程序中的说明执行错误处理程序。

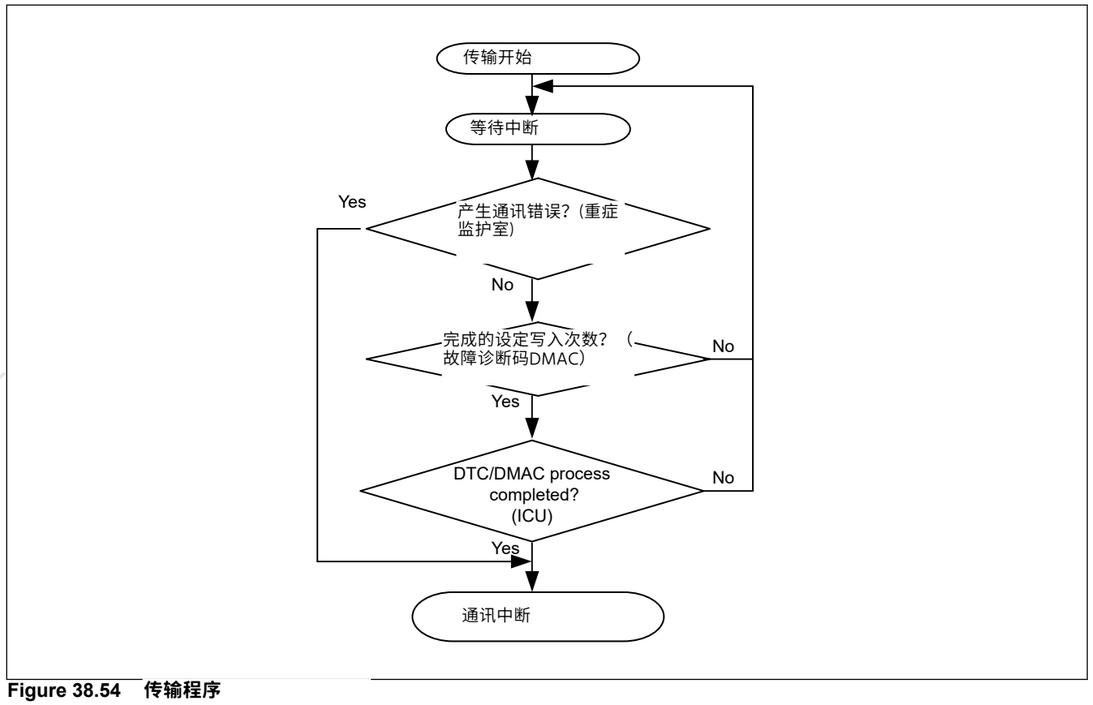


Figure 38.54 传输程序

Note: SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.TDE的值1以将数据写入SSIFTDR。通过检测SSIFSR.TDE的值为1向SSIFTDR写入数据的次数必须与SSIFSR.TDES指定的发送FIFO数据寄存器的空闲空间大小一致。在将与可用空间大小一样多的传输数据写入SSIFTDR后，必须清除SSIFSR.TDE标志。通过重复数据写入启用连续传输。如果

SSIFSR.TDE标志不清除，该标志不会自动清除。

38.8.3 Reception

在整个接收操作中必须遵循图38.55中的接收程序。

使能接收后（SSICR.TEN=0和SSICR.REN=1），SSIE会在以下条件产生开始触发时开始接收SSILRCKSSIFS。SSIE根据RDF设置条件(SSISCR.RDFS)和通信开始过程中指定的接收数据满中断使能(SSIFCR.RIE)位的状态向DTCDMAC输出一个接收数据满中断。该中断请求从接收FIFO数据寄存器(SSIFRDR)读取数据。在通信启动过程中，指定从接收FIFO数据寄存器(SSIFRDR)读取作为DTCDMAC操作以响应接收数据满中断。通过此设置，SSIE可以不通过CPU连续读取数据。当数据达到接收FIFO数据寄存器的容量时，产生接收数据满中断。读取次数必须根据接收数据满中断指示的接收FIFO数据寄存器的数据大小来指定。如果发生错误，请按照通信停止程序中的说明执行错误处理程序。

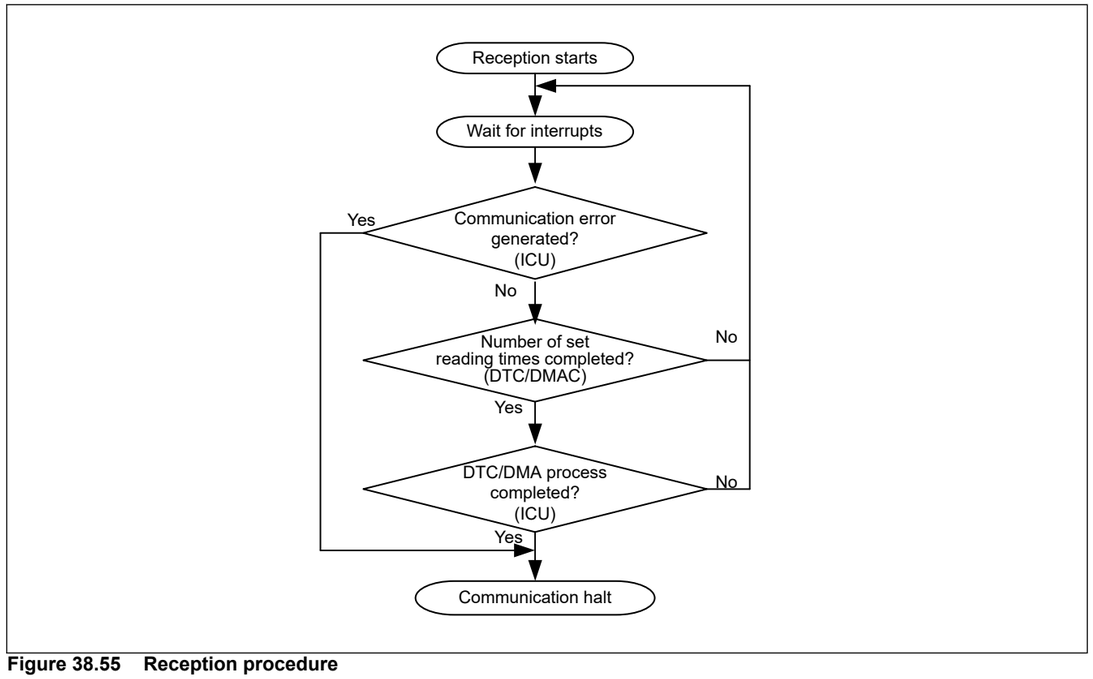


Figure 38.55 Reception procedure

Note: The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.RDF to read data from SSIFRDR. The number of times of reading data from SSIFRDR by detecting the value 1 of SSIFSR.RDF must be in accordance with the receive data storage capacity of the receive FIFO data register specified by SSISCR.RDFS. After received data is read from SSIFRDR, the SSIFSR.RDF flag must be cleared. Continuous reception is enabled by repeating data reading. If the SSIFSR.RDF flag is not cleared, the flag is not cleared automatically.

38.8.4 Transmission and Reception

After transmission and reception are enabled (SSICR.TEN = 1 and SSICR.REN = 1), SSIE starts transmission and reception when a start trigger is generated by SSILRCK/SSIFS with the serial data for at least a frame contained in the transmit FIFO data register (SSIFTDR). SSIE can continuously transmit and receive data by performing the procedures described in section 38.8.2. Transmission and section 38.8.3. Reception, respectively. For how to stop transmission and reception, see section 38.8.5. Halt Communication.

38.8.5 Halt Communication

This section describes how to halt communication of SSIE. Figure 38.56 shows the procedure to halt communication. Be sure to follow the procedure.

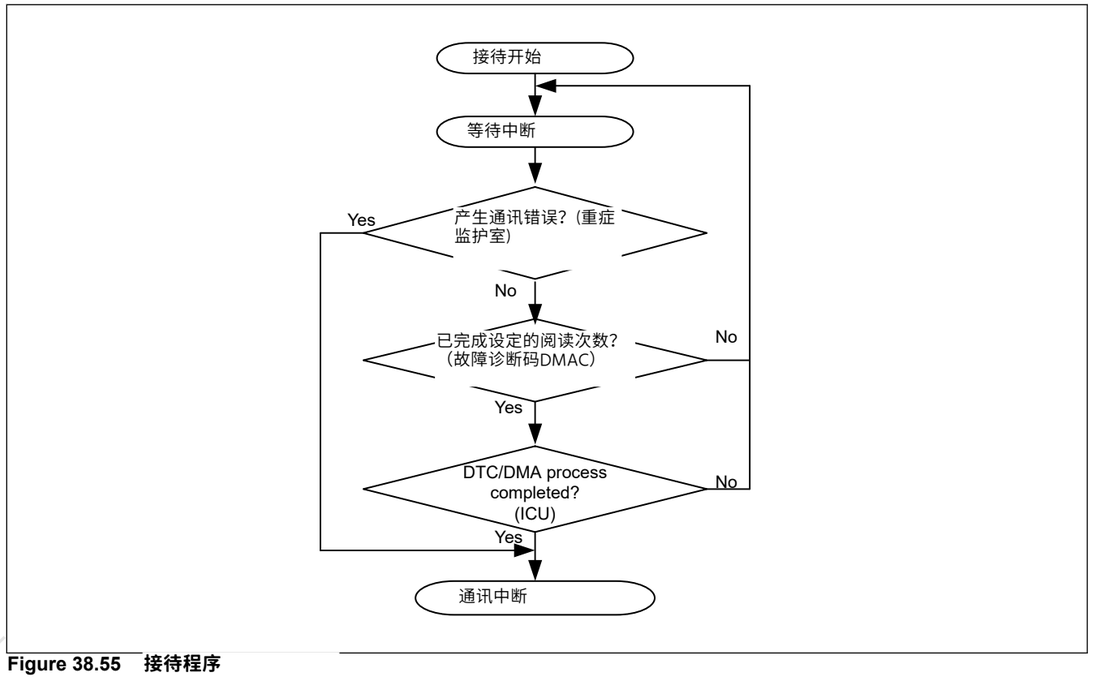


Figure 38.55 接待程序

Note: SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.RDF的值1以从SSIFRDR读取数据。检测SSIFSR.RDF的值为1从SSIFRDR读取数据的次数必须与SSISCR.RDFS指定的接收FIFO数据寄存器的接收数据存储容量一致。从SSIFRDR读取接收到的数据后，必须清除SSIFSR.RDF标志。通过重复数据读取启用连续接收。如果SSIFSR.RDF标志未清除，则该标志不会自动清除。

38.8.4 传输和接收

启用发送和接收后（SSICR.TEN=1和SSICR.REN=1），当SSILRCKSSIFS使用发送FIFO数据寄存器中包含的至少一帧的串行数据产生开始触发时，SSIE开始发送和接收(SSIFTDR)。SSIE可以通过执行第38.8.2节中描述的过程来连续发送和接收数据。传输和第38.8.3节。接待处，分别。关于如何停止发送和接收，请参见第38.8.5节。停止通讯。

38.8.5 停止通讯

本节介绍如何停止SSIE的通信。图38.56显示了停止通信的过程。请务必遵守程序。

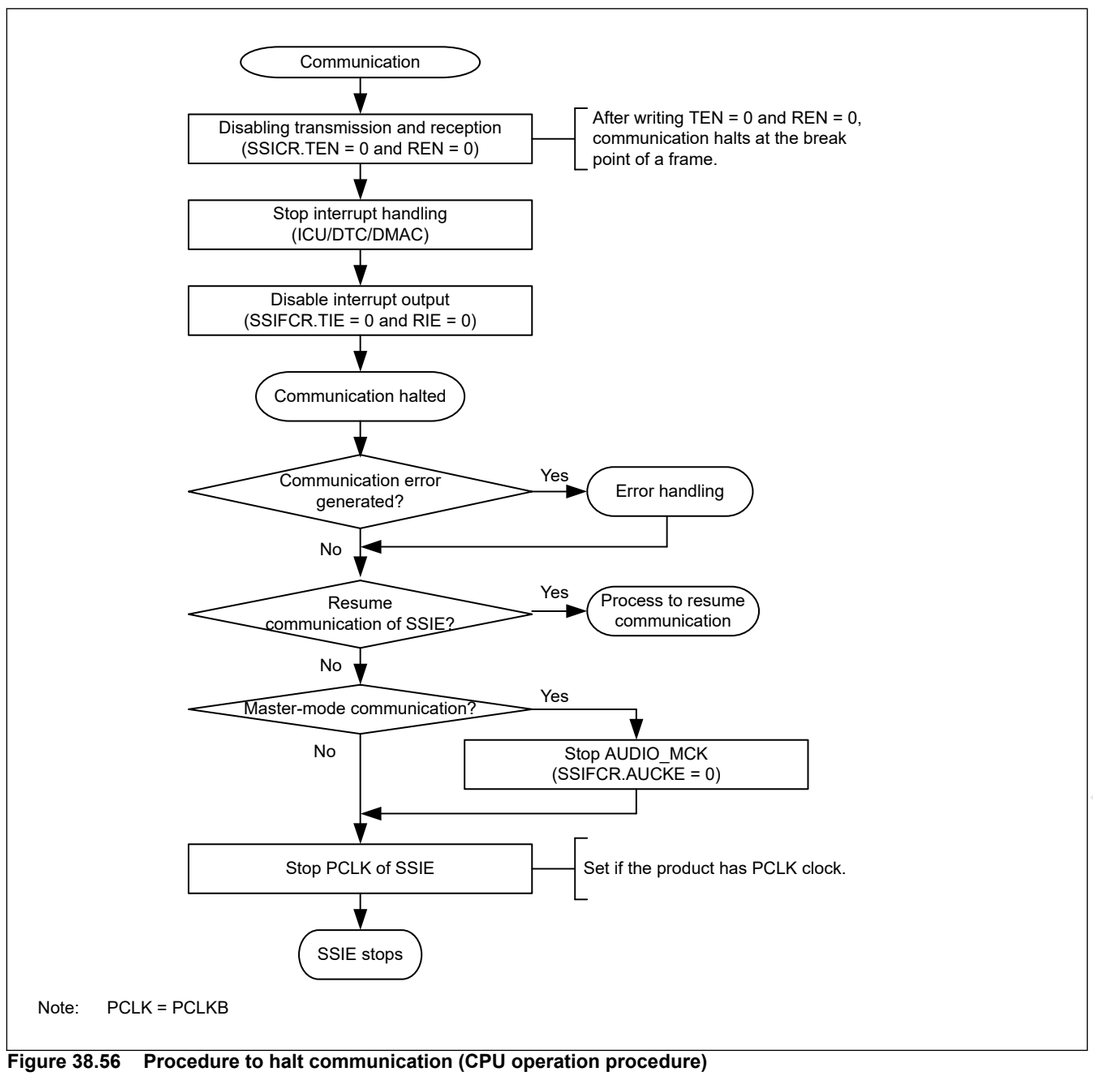


Figure 38.56 Procedure to halt communication (CPU operation procedure)

To halt the communication of SSIE, supply of the following clocks are required until the SSISR.IIRQ bit indicates an idle state.

- Input clock from the SSIBCK pin when SSICR.MST = 0
- AUDIO_MCK when SSICR.MST = 1
  To resume communication of SSIE in the previous setting, see section 38.8.7. Resume Communication.

Note: When communication of SSIE is halted according to the procedure to halt communication in Figure 38.56, resume communication according to the procedure to resume communication in Figure 38.58.

38.8.6 Error Handling

SSIE has the following four errors.

- Transmit underflow error
- Transmit overflow error
- Receive underflow error

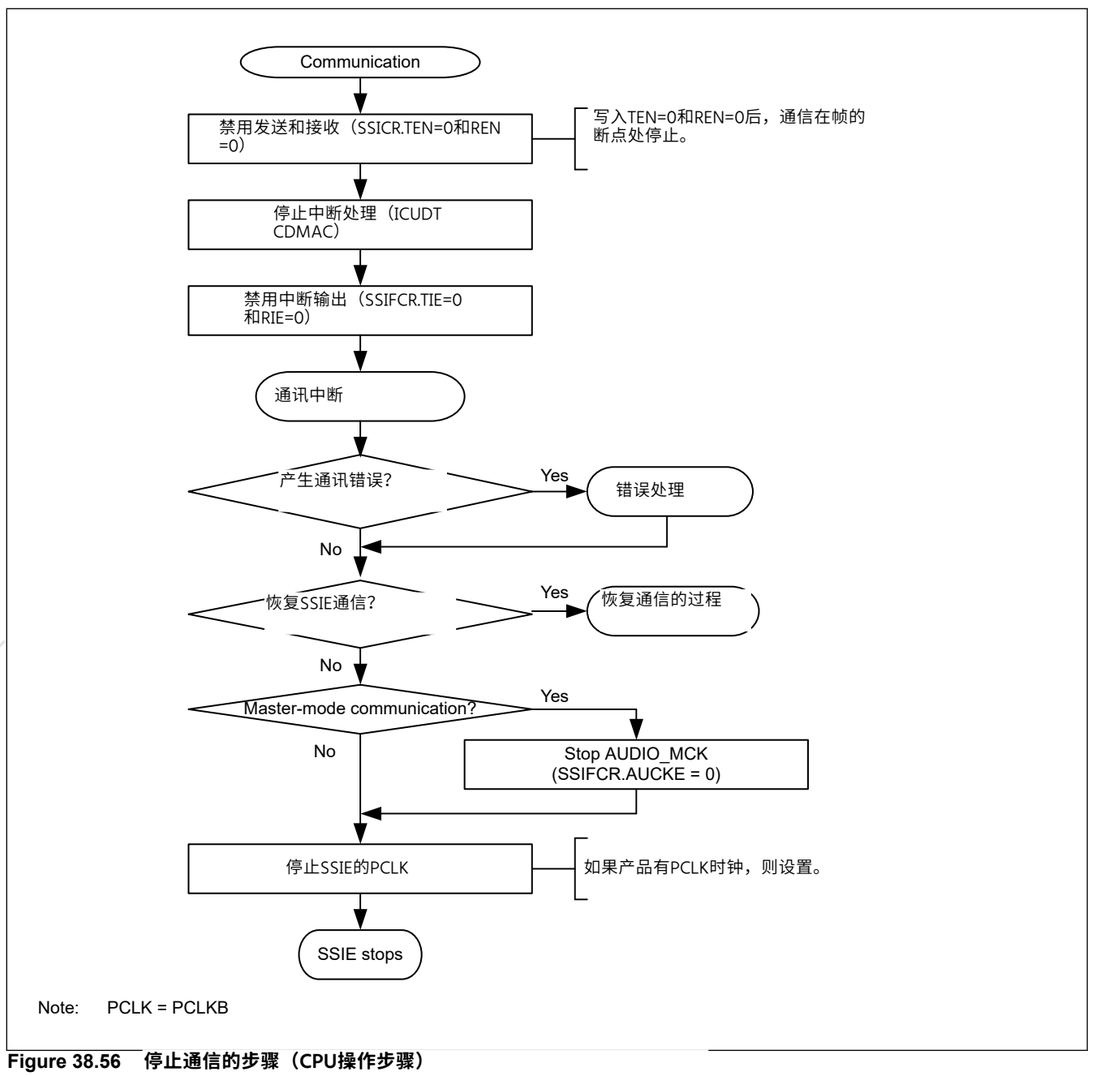


Figure 38.56 停止通信的步骤（CPU操作步骤）

要停止SSIE的通信，需要提供以下时钟，直到SSISR.IIRQ位指示空闲状态。

- ●当SSICR.MST=0时，来自SSIBCK引脚的输入时钟
- AUDIO_MCK when SSICR.MST = 1
  要恢复之前设置的SSIE通信，请参阅第38.8.7节。恢复通信。

Note: 当SSIE的通信按照图38.56中的停止通信程序停止时，按照图38.58中的恢复通信程序恢复通信。

38.8.6 错误处理

SSIE有以下四个错误。

- ●发送下溢错误
- ●发送溢出错误
- ●接收下溢错误

- Receive overflow error.

When an underflow error or overflow error is generated, SSIE need to be restarted. Follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

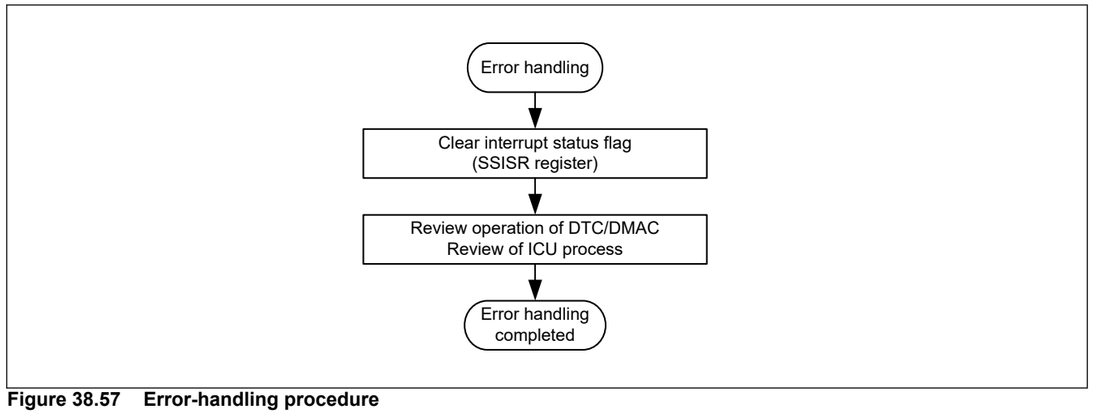


Figure 38.57 Error-handling procedure

Four error operations are described as follows. When the interrupt output enable bit of the SSICR register is enabled and error flags are set, an error interrupt is generated. See section 38.4.2. SSISR : Status Register for the setting conditions of error flags.

(1) Transmit Underflow Error

If a transmit underflow error occurs, review the number of times of writing data to the transmit FIFO data register (SSIFTDR) in response to a transmit data empty interrupt. After a transmit underflow error occurs, SSIE outputs 0s as data. To normally output the serial data written to the transmit FIFO data register (SSIFTDR) to the SSITXD0/SSIDATA0 pin, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57. After this error occurs, serial data is consumed as usual. If you resume communication, write the serial data from the beginning.

(2) Transmit Overflow Error

If a transmit overflow error occurs, review the number of times of writing data to the transmit FIFO data register (SSIFTDR) in response to transmit data empty interrupts. The serial data written to the transmit FIFO data register (SSIFTDR) that caused the transmit overflow error becomes invalid. This error can occur regardless of whether a transmission operation is being done. To recover from the error, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57. When you resume communication, deal with the invalid serial data appropriately.

(3) Receive Underflow Error

If a receive underflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The values read from the receive FIFO data register (SSIFRDR) that caused the receive underflow error are undefined. This error can occur regardless of whether a reception operation is being done. To recover from the error, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

(4) Receive Overflow Error

If a receive overflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The receive data that caused the receive overflow error cannot be stored in the receive FIFO data register (SSIFRDR). To recover from the error, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

38.8.7 Resume Communication

When you resume the communication using SSIE, follow the communication resume procedure in Figure 38.58. The communication resume procedure is designed on the assumption that you resume the communication stopped by the

●接收溢出错误。

当产生下溢错误或上溢错误时，需要重启SSIE。按照图38.56中的程序停止通信和图38.57中的错误处理程序。

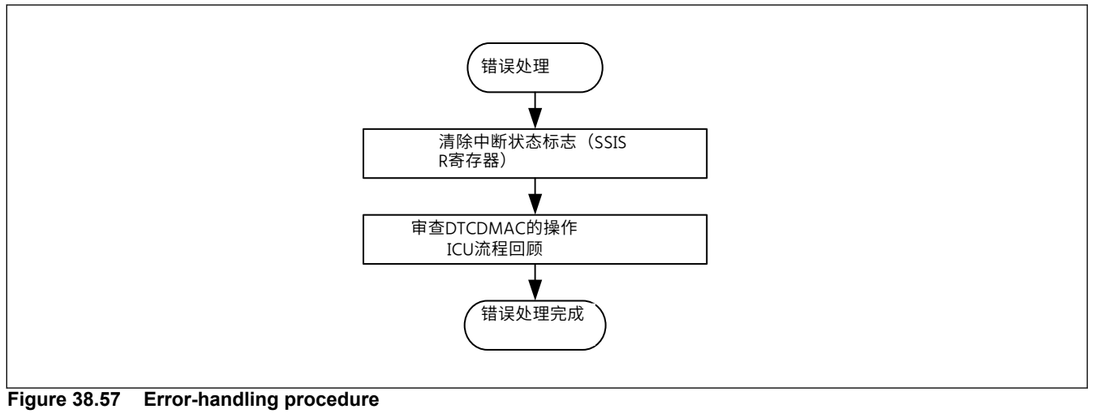


Figure 38.57 Error-handling procedure

四种错误操作描述如下。当SSICR寄存器的中断输出使能位使能且错误标志置位时，将产生错误中断。请参阅第38.4.2节。SSISR：错误标志设置条件的状态寄存器。

(1) 发送下溢错误

如果发生发送下溢错误，请查看响应发送数据空中断而将数据写入发送FIFO数据寄存器(SSIFTDR)的次数。发生发送下溢错误后，SSIE输出0作为数据。要将写入发送FIFO数据寄存器(SSIFTDR)的串行数据正常输出到SSITXD0SSIDATA0引脚，请按照图38.56中的程序停止通信和图38.57中的错误处理程序进行操作。发生此错误后，串行数据将照常使用。如果您恢复通信，请从头开始写入串行数据。

(2) 传输溢出错误

如果发生发送溢出错误，请查看响应发送数据空中断而将数据写入发送FIFO数据寄存器(SSIFTDR)的次数。写入导致发送溢出错误的发送FIFO数据寄存器(SSIFTDR)的串行数据变为无效。无论是否正在执行传输操作，都可能发生此错误。要从错误中恢复，请按照图38.56中的程序停止通信和图38.57中的错误处理程序。当您恢复通信时，请适当处理无效的串行数据。

(3) 接收下溢错误

如果发生接收下溢错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。从导致接收下溢错误的接收FIFO数据寄存器(SSIFRDR)读取的值未定义。无论是否正在执行接收操作，都可能发生此错误。要从错误中恢复，请按照图38.56中的程序停止通信和图38.57中的错误处理程序。

(4) 接收溢出错误

如果发生接收溢出错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。导致接收溢出错误的接收数据不能存储在接收FIFO数据寄存器(SSIFRDR)中。要从错误中恢复，请按照图38.56中的程序停止通信和图38.57中的错误处理程序。

38.8.7 恢复沟通

当您使用SSIE恢复通信时，请遵循图38.58中的通信恢复过程。通信恢复过程的设计假设您恢复了由

communication stop procedure without changing any settings. If you want to change clock and slave/master settings, use and follow the communication start procedure in Figure 38.53. For details about the transmission operation and reception operation after starting communication, see section 38.8.2. Transmission and section 38.8.3. Reception, respectively.

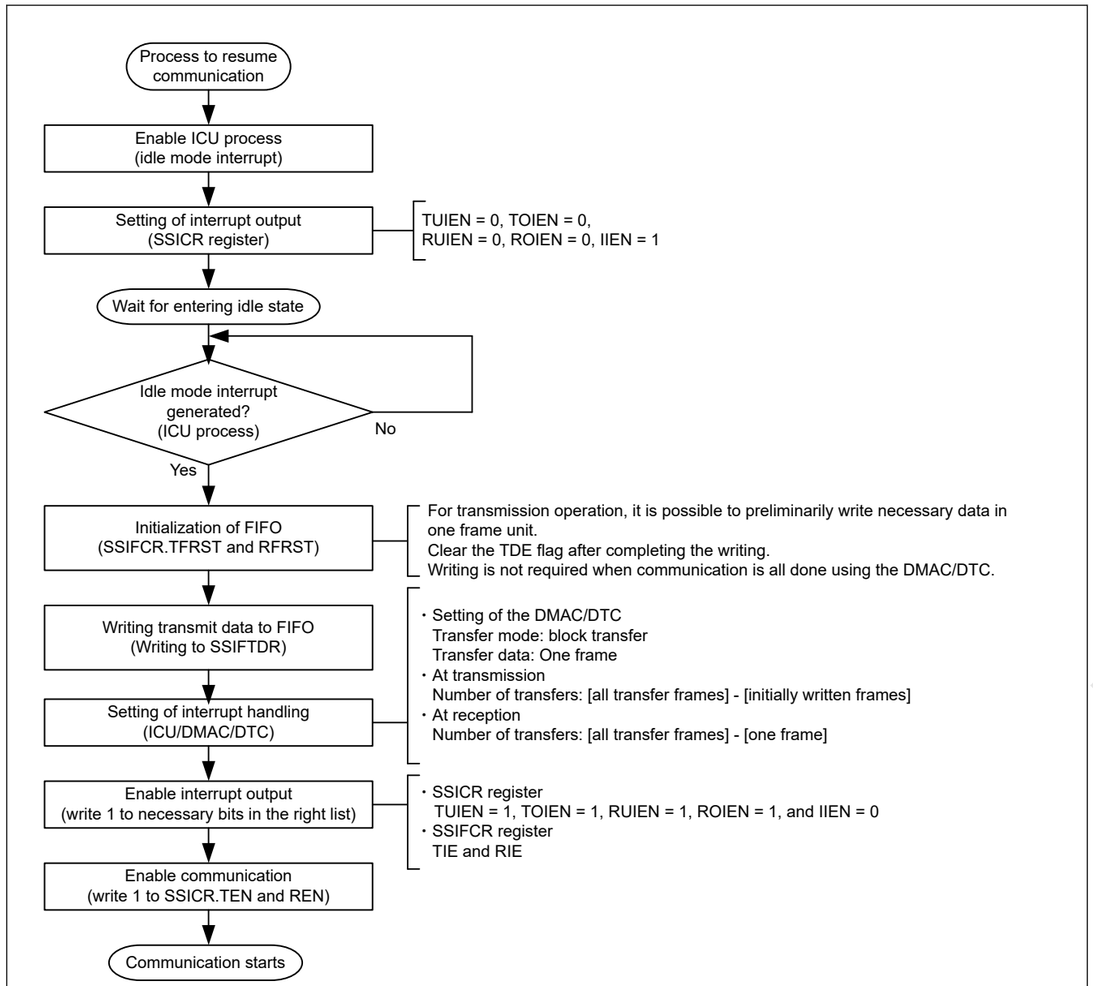


Figure 38.58 Procedure to resume communication (CPU operation procedure)

38.9 Interrupts

Table 38.16 lists the interrupt sources. Set enable/disable of interrupt output of each source with the TUIEN, TOIEN, RUIEN, ROIEN, and IIEN bits in the SSICR register and the TIE and RIE bits in the SSIFCR register.

通信停止程序，无需更改任何设置。如果要更改时钟和从主机设置，请使用并遵循图38.53中的通信启动程序。关于开始通信后的发送动作和接收动作的详细内容，请参阅38.8.2节。传输和第38.8.3节。接待处，分别。

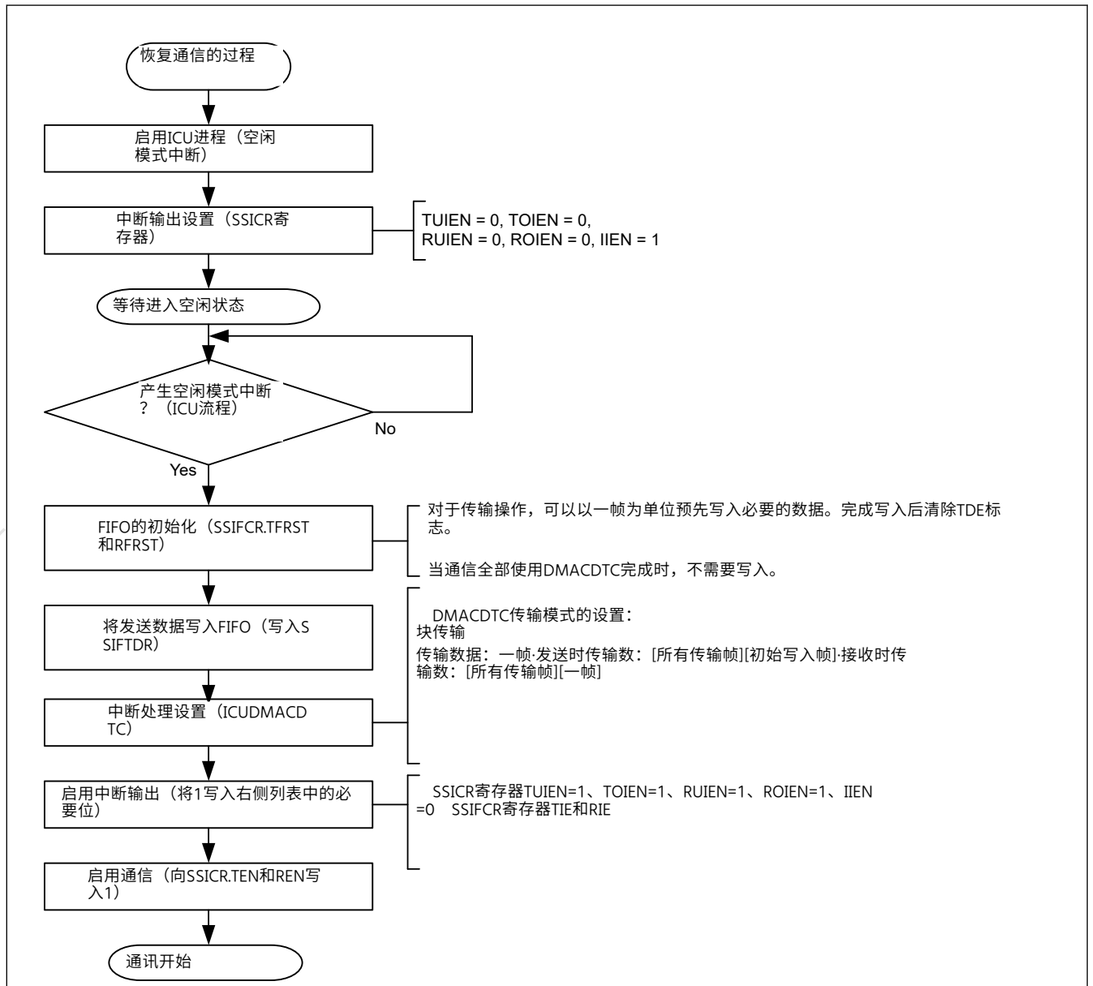


Figure 38.58 恢复通信的步骤（CPU操作步骤）

38.9 Interrupts

表38.16列出了中断源。使用TUIEN、TOIEN、SSICR寄存器中的RUIEN、ROIEN和IIEN位以及SSIFCR寄存器中的TIE和RIE位。

Table 38.16 SSIE interrupt sources

Channel	Interrupt source	Description	Interrupt flag	DMAC/DTC activation
SSIE0	SSIE0_SSIF	• Transmit underflow interrupt • Transmit overflow interrupt • Receive underflow interrupt • Receive overflow interrupt • Idle interrupt	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ	Not possible
	SSIE0_SSIRXI	Receive data full interrupt	SSIFSR.RDF	Possible
	SSIE0_SSITXI	Transmit data empty interrupt	SSIFSR.TDE	Possible

38.9.1 SSIE0_SSIF Interrupt

This interrupt source combines five interrupts. Enable output of necessary interrupts before using SSIE. The five interrupts are operated by using the flags assigned to individual interrupts and interrupt output enable bits. To clear an interrupt, set the interrupt enable to 0 or clear the interrupt flag to 0.

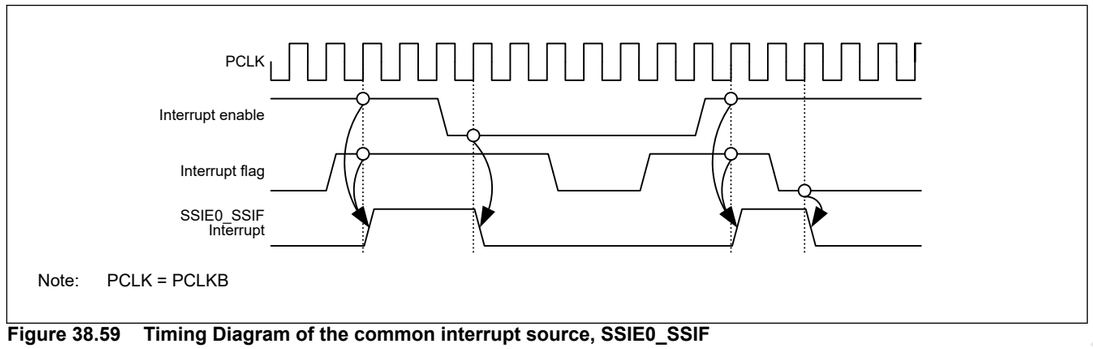


Figure 38.59 Timing Diagram of the common interrupt source, SSIE0_SSIF

- Transmit underflow interrupt

As the transmit underflow interrupt, SSISR.TUIRQ is output while SSICR.TUIEN = 1. When you use SSIE for transmission, enable the output of this interrupt (SSICR.TUIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

- Transmit overflow interrupt

As the transmit overflow interrupt, SSISR.TOIRQ is output while SSICR.TOIRQ = 1. When you use SSIE for transmission, enable the output of this interrupt (SSICR.TOIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

- Receive underflow interrupt

As the receive underflow interrupt, SSISR.RUIRQ is output while SSICR.RUIRQ = 1. When you use SSIE for reception, enable the output of this interrupt (SSICR.RUIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

- Receive overflow interrupt

As the receive overflow interrupt, SSISR.ROIRQ is output while SSICR.ROIRQ = 1. When you use SSIE for reception, enable the output of this interrupt (SSICR.ROIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

- Idle mode interrupt

As the idle mode interrupt, SSISR.IIRQ is output while SSICR.IIEN = 1. This interrupt is used to make sure that communication has stopped fully.

Table 38.16 SSIE中断源

Channel	中断源	Description	中断标志	DMAC/DTC activation
SSIE0	SSIE0_SSIF	• 发送下溢中断 • 发送溢出中断 • 接收下溢中断 • 接收溢出中断 • 空闲中断	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ	不可能
	SSIE0_SSIRXI	接收数据满中断	SSIFSR.RDF	Possible
	SSIE0_SSITXI	发送数据空中断	SSIFSR.TDE	Possible

38.9.1 SSIE0_SSIF Interrupt

该中断源结合了五个中断。在使用SSIE之前启用必要中断的输出。通过使用分配给各个中断的标志和中断输出使能位来操作五个中断。要清除中断，请将中断使能设置为0或将中断标志清除为0。

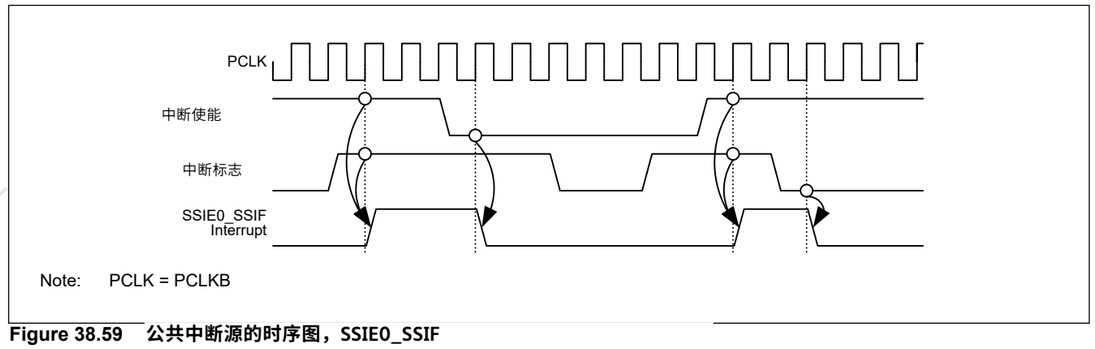


Figure 38.59 公共中断源的时序图，SSIE0_SSIF

●发送下溢中断

作为发送下溢中断，在SSICR.TUIEN=1时输出SSISR.TUIRQ。当使用SSIE进行发送时，使能该中断的输出（SSICR.TUIRQ=1）。如果发生此中断，请按照图38.56中的停止通信过程和图38.57中的错误处理过程中的说明进行操作。

●发送溢出中断

作为发送溢出中断，在SSICR.TOIRQ=1时输出SSISR.TOIRQ。当使用SSIE进行发送时，使能该中断的输出（SSICR.TOIRQ=1）。如果发生此中断，请按照图38.56中的停止通信过程和图38.57中的错误处理过程中的说明进行操作。

●接收下溢中断

作为接收下溢中断，在SSICR.RUIRQ=1时输出SSISR.RUIRQ。当使用SSIE进行接收时，使能该中断的输出（SSICR.RUIRQ=1）。如果发生此中断，请按照图38.56中的停止通信过程和图38.57中的错误处理过程中的说明进行操作。

●接收溢出中断

作为接收溢出中断，在SSICR.ROIRQ=1时输出SSISR.ROIRQ。当使用SSIE进行接收时，使能该中断的输出（SSICR.ROIRQ=1）。如果发生此中断，请按照图38.56中的停止通信过程和图38.57中的错误处理过程中的说明进行操作。

●空闲模式中断

作为空闲模式中断，在SSICR.IIEN=1时输出SSISR.IIRQ。此中断用于确保通信已完全停止。

38.9.2 SSIE0_SSITXI Interrupt

The transmit data empty interrupt is a pulse interrupt that is output when the following condition is met:

- SSIFCR.TIE = 1 and SSIFSR.TDE = 1
  SSIE operation: When the value of SSIFSR.TDE changes from 0 to 1 while the value of SSIFCR.TIE is 1
  CPU instruction: When the value of SSIFCR.TIE changes from 0 to 1 while the value of SSIFSR.TDE is 1

This interrupt is subject to the interrupt suppression function. If an interrupt condition for this interrupt occurs when the DTC/DMAC is busy (when the DTC/DMAC cannot accept interrupts), the interrupt suppression function holds the output of this interrupt. The held interrupt will be output after the DTC/DMAC is enabled to accept interrupts. For details, see Figure 38.60.

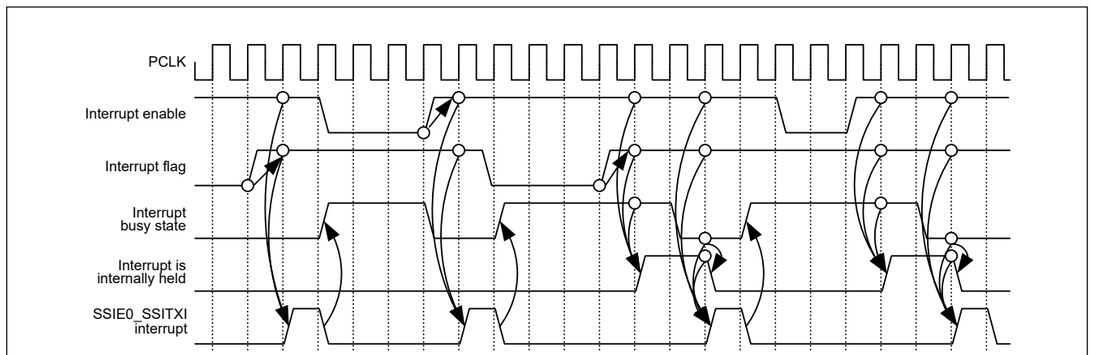


Figure 38.60 SSIE0_SSITXI interrupt timing diagram

38.9.3 SSIE0_SSIRXI Interrupt

The receive data full interrupt is a pulse interrupt that is output when the following condition is met:

- SSIFCR.RIE = 1 and SSIFSR.RDF = 1.
  SSIE operation: When the value of SSIFSR.RDF changes from 0 to 1 while the value of SSIFCR.RIE is 1
  CPU instruction: When the value of SSIFCR.RIE changes from 0 to 1 while the value of SSIFSR.RDE is 1

This interrupt is subject to the interrupt suppression function. If an interrupt condition for this interrupt occurs when the DTC/DMAC is busy (when the DTC/DMAC cannot accept interrupts), the interrupt suppression function holds the output of this interrupt. The held interrupt will be output after the DTC/DMAC is enabled to accept interrupts. The behavior of this interrupt is the same as the behavior shown in Figure 38.60.

38.10 Software Resets

SSIE has three software reset bits to reset its states.

- SSIE software reset (SSIFCR.SSIRST)
- Transmit FIFO data register reset (SSIFCR.TFRST)
- Receive FIFO data register reset (SSIFCR.RFRST).

This section describes the procedures for the three types of software resets.

38.10.1 Software Reset Procedure

(1) SSIE Software Reset

For the SSIE software reset bit (SSIFCR.SSIRST), follow the procedure shown in Figure 38.61. After a reset, the same setting is applied when it is resumed. To change the settings of clocks and slave/master mode, follow the procedure to start

38.9.2 SSIE0_SSITXI Interrupt

发送数据空中断是一个脉冲中断，当满足以下条件时输出：

- SSIFCR.TIE = 1 and SSIFSR.TDE = 1
  SSIE操作：当SSIFSR.TDE的值从0变为1且SSIFCR.TIE的值为1时CPU指令：当SSIFCR.TIE的值从0变为1且SSIFSR.TDE的值为1时

该中断受中断抑制功能影响。如果在DTCDMAC忙时（当DTCDMAC不能接受中断时）发生此中断的中断条件，则中断抑制功能保持此中断的输出。在DTCDMAC使能接受中断后，将输出保持的中断。详见图38.60。

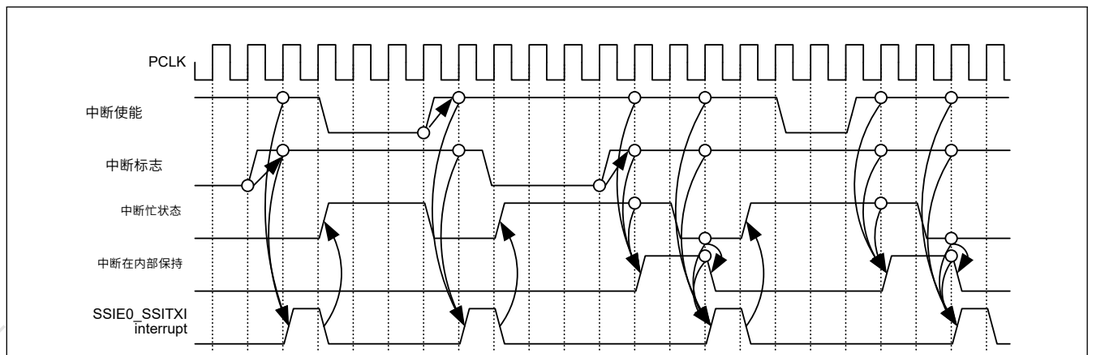


Figure 38.60 SSIE0_SSITXI中断时序图

38.9.3 SSIE0_SSIRXI Interrupt

接收数据满中断是一个脉冲中断，当满足以下条件时输出：

- SSIFCR.RIE = 1 and SSIFSR.RDF = 1.
  SSIE操作：当SSIFSR.RDF的值从0变为1且SSIFCR.RIE的值为1时CPU指令：当SSIFCR.RIE的值从0变为1且SSIFSR.RDE的值为1时

该中断受中断抑制功能影响。如果此中断的中断条件发生时，
DTCDMAC忙（当DTCDMAC不能接受中断时），中断抑制功能保持该中断的输出。在DTCDMAC使能接受中断后，将输出保持的中断。该中断的行为与图38.60中所示的行为相同。

38.10 软件复位

SSIE具有三个软件复位位来复位其状态。

- SSIE软件复位(SSIFCR.SSIRST)
- 发送FIFO数据寄存器复位(SSIFCR.TFRST)
- 接收FIFO数据寄存器复位(SSIFCR.RFRST)。

本节介绍三种软件复位的过程。

38.10.1 软件复位程序

(1) SSIE软件复位

对于SSIE软件复位位(SSIFCR.SSIRST)，请按照图38.61中所示的过程。重置后，恢复时应用相同的设置。要更改时钟和从主模式的设置，请按照以下步骤开始

communication in Figure 38.53. See section 38.8.2. Transmission and section 38.8.3. Reception respectively for transmission and reception after communication is resumed.

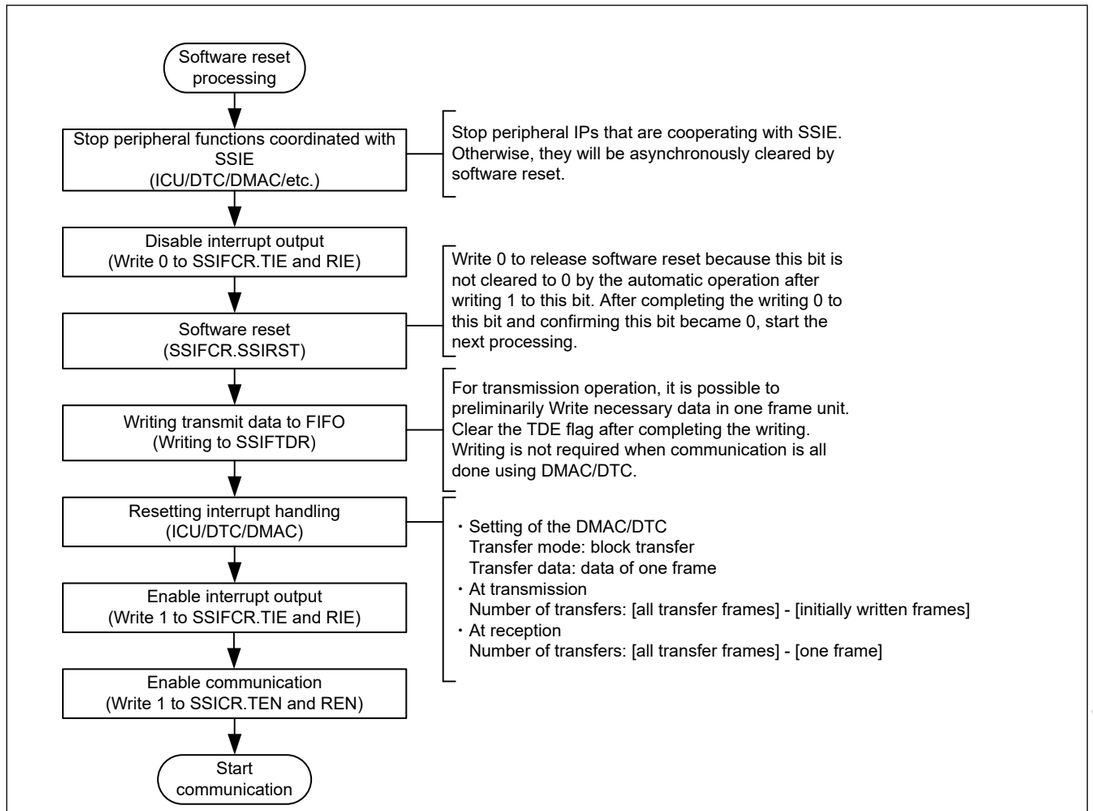


Figure 38.61 Software reset procedure (CPU operation procedure)

(2) Transmit FIFO data register reset

To perform a transmit FIFO data register reset, follow instructions in the procedure to start communication in Figure 38.53 and procedure to resume communication in Figure 38.58.

(3) Receive FIFO data register reset

To perform a receive FIFO data register reset, follow instructions in the procedure to start communication in Figure 38.53 and procedure to resume communication in Figure 38.58.

38.11 Notes

38.11.1 Notes for Slave-mode Communication

38.11.1.1 ADCKE control

In slave-mode communication (SSICR.MST = 0), SSIE needs supply of SSIBCK. To stop BCK on the master side, make sure that SSIE is in the idle state (SSISR.IIRQ = 1). If BCK is stopped before SSIE becomes idle, take the procedure to start communication in Figure 38.53 or wait for an idle state by taking the procedure to resume communication in Figure 38.58.

图38.53中的通信。请参阅第38.8.2节。传输和第38.8.3节。接收分别用于通信恢复后的发送和接收。

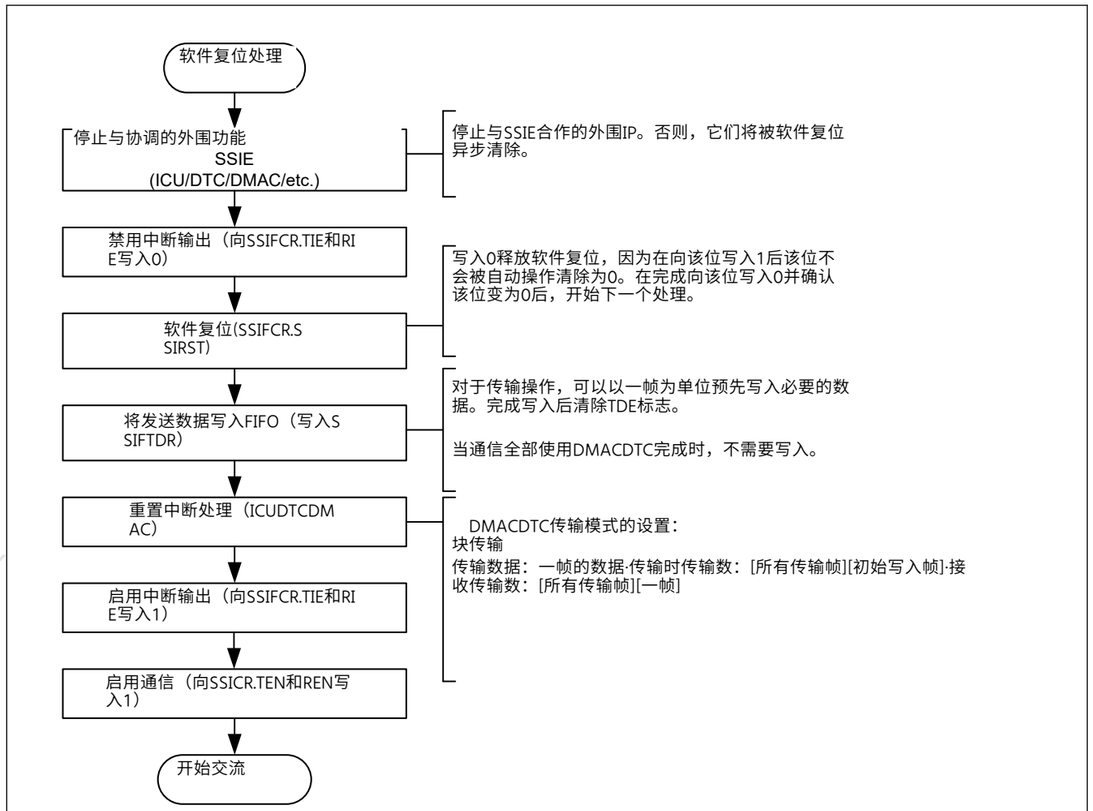


Figure 38.61 软件复位程序（CPU操作程序）

(2) 发送FIFO数据寄存器复位

要执行发送FIFO数据寄存器复位，请按照图38.53中的开始通信过程和图38.58中恢复通信的过程中的说明进行操作。

(3) 接收FIFO数据寄存器复位

要执行接收FIFO数据寄存器复位，请按照图38.53中的开始通信过程和图38.58中恢复通信的过程中的说明进行操作。

38.11 Notes

38.11.1 从模式通信注意事项

38.11.1.1 ADCKE control

在从模式通信(SSICR.MST=0)中，SSIE需要提供SSIBCK。要在主设备端停止BCK，请确保SSIE处于空闲状态(SSISR.IIRQ=1)。如果BCK在SSIE空闲之前停止，则按照图38.53中的程序开始通信，或者按照图38.58中的程序恢复通信等待空闲状态。

38.11.1.2 SSILRCK/SSIFS pin

SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

38.11.2 Notes for Master-mode Communication

38.11.2.1 ADCKE control

In master-mode communication (SSICR.MST = 1), SSIE operates with the audio clock (AUDIO_MCK). To stop SSIE completely, make sure that SSIE is in the idle state (SSISR.IIRQ = 1) and then write 0 to SSIFCR.ADCKE.

38.11.2.2 LRCONT control

To stop the output to the SSILRCK/SSIFS pin with SSIOFR.LRCONT when SSIE is in the idle state in master-mode communication (SSICR.MST = 1), note the following: The output stops when the value of the SSIOFR.LRCONT bit is changed from 1 to 0. Make sure that the other-party device is not affected. For details, see Figure 38.44.

38.11.2.3 BCKASTP control

To stop the output to the SSIBCK pin with SSIOFR.BCKASTP in master-mode communication (SSICR.MST = 1) and while SSIE is in the idle state, note the following: The output stops when the value of the SSIOFR.BCKASTP bit is changed from 0 to 1. So, make sure that the other-party device is not affected. For details, see Figure 38.45.

The BCKASTP bit cannot be used when the other-party device (which is a slave) requires the clock output from the SSIBCK pin before and during communication.

38.11.3 Notes for Communication Flow

38.11.3.1 When an error interrupt is generated

SSIE has the following four errors.

- Transmit underflow error
- Transmit overflow error
- Receive underflow error
- Receive overflow error

When an underflow error or overflow error is generated, SSIE need to be restarted. Follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

(1) Transmit Underflow Error

If a transmit underflow error occurs, review the number of times of writing data to the transmit FIFO data register (SSIFTDR) in response to a transmit data empty interrupt. After a transmit underflow error occurs, SSIE outputs 0s as data. To normally output the serial data written to the transmit FIFO data register (SSIFTDR) to the SSITXD0/SSIDATA0 pin, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57. After this error occurs, serial data is consumed as usual. If you resume communication, write the serial data from the beginning.

(2) Transmit Overflow Error

If a transmit overflow error occurs, review the number of times of writing data to the Transmit FIFO Data Register (SSIFTDR) in response to transmit data empty interrupts. The serial data written to the Transmit FIFO Data Register (SSIFTDR) that caused the transmit overflow error becomes invalid. This error can occur regardless of whether a transmission operation is being done. To recover from the error, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57. When you resume communication, deal with the invalid serial data appropriately.

38.11.1.2 SSILRCK/SSIFS pin

SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

38.11.2 主模式通信注意事项

38.11.2.1 ADCKE control

在主模式通信(SSICR.MST=1)中，SSIE使用音频时钟(AUDIO_MCK)运行。要完全停止SSIE，请确保SSIE处于空闲状态(SSISR.IIRQ=1)，然后将0写入SSIFCR.ADCKE。

38.11.2.2 LRCONT control

当SSIE在主模式通信中处于空闲状态时（SSICR.MST=1），要使用SSIOFR.LRCONT停止向SSILRCKSSIFS引脚的输出，请注意以下几点：当SSIOFR.LRCONT位的值为从1变为0。确保对方设备不受影响。详见图38.44。

38.11.2.3 BCKASTP control

要在主模式通信(SSICR.MST=1)和SSIE处于空闲状态时使用SSIOFR.BCKASTP停止向SSIBCK引脚的输出，请注意以下几点：当SSIOFR.BCKASTP位的值为从0变为1。因此，请确保对方设备不受影响。详见图38.45。

当对方设备（从设备）需要时钟输出时，不能使用BCKASTP位
SSIBCK引脚在通信之前和期间。

38.11.3 通信流程注意事项

38.11.3.1 产生错误中断时

SSIE有以下四个错误。

●发送下溢错误
●发送溢出错误
●接收下溢错误
●接收溢出错误

当产生下溢错误或上溢错误时，需要重启SSIE。按照图38.56中的程序停止通信和图38.57中的错误处理程序。

(1) 发送下溢错误

如果发生发送下溢错误，请查看响应发送数据空中断而将数据写入发送FIFO数据寄存器(SSIFTDR)的次数。发生发送下溢错误后，SSIE输出0作为数据。要将写入发送FIFO数据寄存器(SSIFTDR)的串行数据正常输出到SSITXD0SSIDATA0引脚，请按照图38.56中的程序停止通信和图38.57中的错误处理程序进行操作。发生此错误后，串行数据将照常使用。如果您恢复通信，请从头开始写入串行数据。

(2) 传输溢出错误

如果发生发送溢出错误，请检查向发送FIFO数据寄存器(SSIFTDR)写入数据以响应发送数据空中断的次数。导致发送溢出错误的写入发送FIFO数据寄存器(SSIFTDR)的串行数据变为无效。无论是否正在执行传输操作，都可能发生此错误。要从错误中恢复，请按照图38.56中的程序停止通信和图38.57中的错误处理程序。当您恢复通信时，请适当处理无效的串行数据。

(3) Receive Underflow Error

If a receive underflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The values read from the receive FIFO data register (SSIFRDR) that caused the receive underflow error are undefined. This error can occur regardless of whether a reception operation is being done. To recover from the error, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

(4) Receive Overflow Error

If a receive overflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The receive data that caused the receive overflow error cannot be stored in the receive FIFO data register (SSIFRDR). To recover from the error, follow the procedure to halt communication in Figure 38.56 and error-handling procedure in Figure 38.57.

38.11.3.2 Transmit data empty interrupt

The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.TDE to write data to SSIFTDR. The number of times of writing data to SSIFTDR by detecting the value 1 of SSIFSR.TDE must be in accordance with the free space size of the transmit FIFO data register specified by SSISCR.TDES. After as much transmit data as the free space size is written to SSIFTDR, the SSIFSR.TDE flag must be cleared. Continuous transmission is enabled by repeating data writing. If the SSIFSR.TDE flag is not cleared, the flag is not cleared automatically.

38.11.3.3 Receive data full interrupt

The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.RDF to read data from SSIFRDR. The number of times of reading data from SSIFRDR by detecting the value 1 of SSIFSR.RDF must be in accordance with the receive data storage capacity of the receive FIFO data register specified by SSISCR.RDFS. After received data is read from SSIFRDR, the SSIFSR.RDF flag must be cleared. Continuous reception is enabled by repeating data reading. If the SSIFSR.RDF flag is not cleared, the flag is not cleared automatically.

38.11.3.4 Switching transfer modes

1. For state transition from transmission, reception, and transmission and reception, disable transmission and reception (SSICR.TEN = 0, SSICR.REN = 0).
2. Confirm it is in the idle state (SSISR.IIRQ = 1).
3. In the idle state, set the SSICR.TEN bit and the SSICR.REN bit again and resume transfer.

38.11.3.5 Resume communication after halting SSIE

When communication of SSIE is halted according to the procedure to halt communication in Figure 38.56, resume communication according to the procedure to resume communication in Figure 38.58.

38.11.4 Write Access Restriction

38.11.4.1 SSICR register

If the TEN bit or REN bit is rewritten, make sure that the SSISR.IIRQ bit is in the desired status. If the value of the TEN or REN bit is changed by rewriting, subsequent operation is unpredictable. For example, when transmission or reception is enabled, check that SSISR.IIRQ is 0; when transmission or reception is disabled, check that SSISR.IIRQ is 1.

(1) TEN Bit and REN Bit

These bits enable/disable transmission and reception. When 1 is written to one of these bits, the corresponding communication operation starts in synchronization with a start trigger by the SSILRCK/SSIFS signal. For details, see section 38.8.2. Transmission, section 38.8.3. Reception, and section 38.8.4. Transmission and Reception. When 0 is written to this bit, the current communication operation stops at the next frame boundary. To use SSIE for both transmission and reception, always write 1 to these bits together. When stopping the communication using SSIE, always disable both transmission and reception (write 0 to the TEN and REN bits).

(3) 接收下溢错误

如果发生接收下溢错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。从导致接收下溢错误的接收FIFO数据寄存器(SSIFRDR)读取的值未定义。无论是否正在执行接收操作，都可能发生此错误。要从错误中恢复，请按照图38.56中的程序停止通信和图38.57中的错误处理程序。

(4) 接收溢出错误

如果发生接收溢出错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。导致接收溢出错误的接收数据不能存储在接收FIFO数据寄存器(SSIFRDR)中。要从错误中恢复，请按照图38.56中的程序停止通信和图38.57中的错误处理程序。

38.11.3.2 发送数据空中断

SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.TDE的值1以将数据写入SSIFTDR。通过检测SSIFSR.TDE的值为1向SSIFTDR写入数据的次数必须与SSIFSR.TDES指定的发送FIFO数据寄存器的可用空间大小一致。在将与可用空间大小一样多的传输数据写入SSIFTDR后，必须清除SSIFSR.TDE标志。通过重复数据写入启用连续传输。如果未清除SSIFSR.TDE标志，则不会自动清除该标志。

38.11.3.3 接收数据满中断

SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.RDF的值1以从SSIFRDR读取数据。通过检测SSIFSR.RDF的值为1从SSIFRDR读取数据的次数必须与SSISCR.RDFS指定的接收FIFO数据寄存器的接收数据存储容量一致。从SSIFRDR读取接收到的数据后，必须清除SSIFSR.RDF标志。通过重复数据读取启用连续接收。如果未清除SSIFSR.RDF标志，则不会自动清除该标志。

38.11.3.4 切换传输模式

1.对于从发送、接收和发送和接收的状态转换，禁用发送和接收（SSICR.TEN=0，SSICR.REN=0）。

2.确认它处于空闲状态（SSISR.IIRQ=1）。

3.在空闲状态下，再次设置SSICR.TEN位和SSICR.REN位并恢复传输。

38.11.3.5 停止SSIE后恢复通信

当SSIE的通信按照图38.56中的停止通信程序停止时，按照图38.58中的恢复通信程序恢复通信。

38.11.4 写访问限制

38.11.4.1 SSICR register

如果TEN位或REN位被重写，请确保SSISR.IIRQ位处于所需状态。如果TEN的值或
REN位通过改写改变，后续操作不可预知。例如，启用发送或接收时，检查SSISR.IIRQ是否为0；当发送或接收被禁用时，检查SSISR.IIRQ是否为1。

(1) 十位和仁位

这些位启用禁用发送和接收。当这些位之一写入1时，相应的通信操作与SSILRCKSSIFS信号的开始触发同步开始。有关详细信息，请参阅第38.8.2节。传输，第38.8.3节。接待处和第38.8.4节。传输和接收。当向该位写入0时，当前通信操作在下一帧边界处停止。要同时使用SSIE进行发送和接收，请始终将1一起写入这些位。使用SSIE停止通信时，始终禁用发送和接收（将0写入TEN和REN位）。

38.11.4.2 SSISR register

(1) Clearing TUIRQ and TOIRQ

After communication is enabled (by changing the value of SSICR.TEN bit from 0 to 1), the transmission error flags (TOIRQ and TUIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the transmission error flags might be unable to be read.

(2) Clearing RUIRQ and ROIRQ

After communication is enabled (by changing the value of SSICR.REN bit from 0 to 1), the reception error flags (RUIRQ and ROIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the reception error flags might be unable to be read.

38.11.4.3 Communication state

Writing to the bits with orange-shaded area in Table 38.17 is prohibited. If written, the operation performed immediately after writing is not guaranteed.

Table 38.17 Bits protected from writing during communication

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

38.11.4.2 SSISR register

(1) 清除TUIRQ和TOIRQ

启用通信后（通过将SSICR.TEN位的值从0更改为1），传输错误标志（SSISR寄存器中的TOIRQ和TUIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取传输错误标志的清除状态。

(2) 清除RUIRQ和ROIRQ

启用通信后（通过将SSICR.REN位的值从0更改为1），接收错误标志（SSISR寄存器中的RUIRQ和ROIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取接收错误标志的清除状态。

38.11.4.3 通讯状态

禁止写入表38.17中橙色阴影区域的位。如果写入，则不保证写入后立即执行的操作。

Table 38.17 通信期间防止写入的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	0x00	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	0x04	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	0x10	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	0x14	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	0x18	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	0x1C	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	0x20	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	0x24	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

39. SD/MMC Host Interface (SDHI)

39.1 Overview

The Secure Digital Host Interface (SDHI) and MultiMediaCard (MMC) Interface provide the functionality required to connect a variety of external memory cards with the MCU. The SDHI supports both 1- and 4-bit buses for connecting different memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA).

The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84- B451) device access. This interface also provides backward compatibility and supports for high-speed SDR transfer modes.

Table 39.1 lists the SD/MMC Host Interface specifications and Figure 39.1 shows a block diagram.

Table 39.1 SD/MMC Host Interface specifications

Interface	Parameter	Specifications
SD	SD bus interface	• Compatible with SD memory card and SDIO card • Transfer bus mode selectable from 4-bit wide bus mode or 1-bit default bus mode • Compatible with SD, SDHC, and SDXC formats
SD and MMC shared	SDHI clock frequency	The SDHI clock is generated by dividing PCLKB by 2^n (n = 0 to 9)
	Error check functions	CRC7 (command/response), CRC16 (transfer data)
	Interrupt sources	Card access interrupt (SDHI_MMC0_ACCS), SDIO access interrupt (SDHI_MMC0_SDI0), Card detection interrupt (SDHI_MMC0_CARD)
	DMA transfer sources	DMAC and DTC triggerable by the SBFAI interrupt SD buffer is read and write accessible using the DMAC
	Other functions	• Card detect function • Write protect support
MMC	MMC bus interface	Transfer bus mode selectable from 1-bit, 4-bit, or 8-bit
	Transfer modes	Backward compatible mode or high-speed SDR mode selectable
	Other functions	e.MMC device access supported
TrustZone Filter	Security attribution can be set	

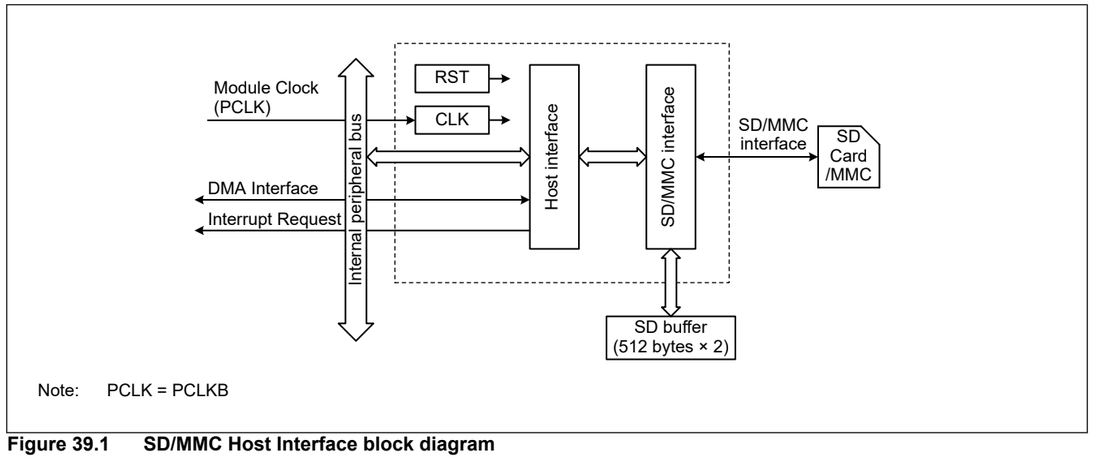


Figure 39.1 SD/MMC Host Interface block diagram

Table 39.2 SDHI I/O pins (n = 0) (1 of 2)

Channel	Pin name	I/O	Description
Ch n	SDnCLK	Output	SDHI clock

39. SDMMC主机接口(SDHI)

39.1 Overview

安全数字主机接口(SDHI)和多媒体卡(MMC)接口提供了将各种外部存储卡与MCU连接所需的功能。SDHI支持1位和4位总线，用于连接支持SD、SDHC和SDXC格式的不同存储卡。在开发符合SD规范的主机设备时，您必须遵守SD主机辅助产品许可协议(SDHALA)。

MMC接口支持提供eMMC4.51（JEDEC标准JESD84B451）器件访问的1位、4位和8位MMC总线。该接口还提供向后兼容性并支持高速SDR传输模式。

表39.1列出了SDMMC主机接口规范，图39.1显示了框图。

Table 39.1 SDMMC主机接口规格

Interface	Parameter	Specifications
SD	SD总线接口	• 兼容SD存储卡和SDIO卡 • 传输总线模式可选择4位宽总线模式或1位默认总线模式 • 兼容SD、SDHC和SDXC格式
SD和MMC共享	SDHI时钟频率	SDHI时钟由PCLKB除以2n(n=0到9)生成
	错误检查功能	CRC7 (command/response), CRC16 (transfer data)
	中断源	卡访问中断（SDHI_MMC0_ACCS）、SDIO访问中断（SDHI_MMC0_SDI0）、卡检测中断（SDHI_MMC0_CARD）
	DMA传输源	SBFAI中断可触发DMAC和DTC SD缓冲区可使用DMAC进行读写访问
	其他功能	• 卡片检测功能 • 写保护支持
MMC	MMC总线接口	传输总线模式可选择1位、4位或8位
	传输模式	向后兼容模式或高速SDR模式可选
	其他功能	支持e.MMC设备访问
TrustZone Filter	可设置安全属性	

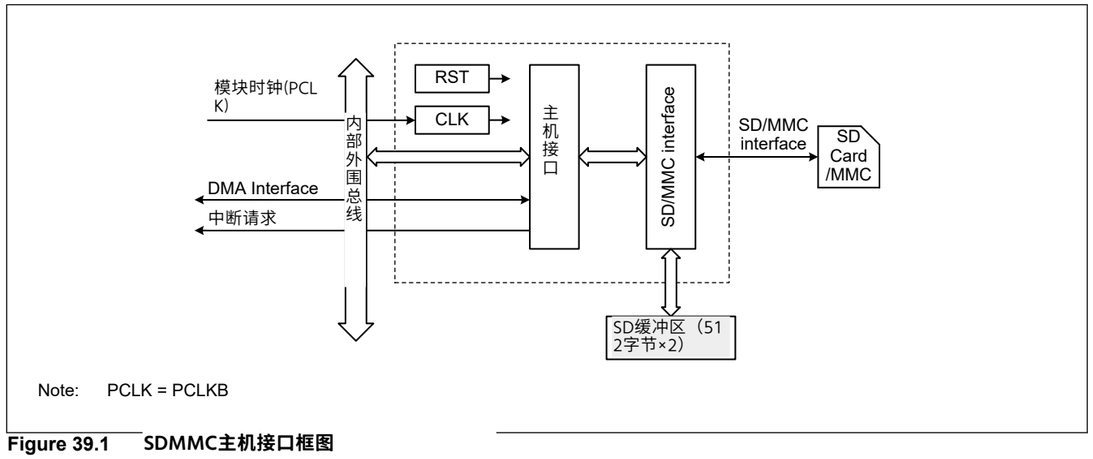


Figure 39.1 SDMMC主机接口框图

Table 39.2 SDHIIO引脚(n=0)(1of2)

Channel	引脚名称	I/O	Description
Ch n	SDnCLK	Output	SDHI clock

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Table 39.2 SDHI I/O pins (n = 0) (2 of 2)

Channel	Pin name	I/O	Description
	SDnCMD	I/O	Command output, response input
	SDnDAT0	I/O	Data 0 (DAT0)
	SDnDAT1	I/O	Data 1 (DAT1), SDIO interrupt
	SDnDAT2	I/O	Data 2 (DAT2), SDIO Read wait
	SDnDAT3	I/O	Data 3 (DAT3), SD Card detect
	SDnDAT4	I/O	MMC Data 4 (DAT4)
	SDnDAT5	I/O	MMC Data 5 (DAT5)
	SDnDAT6	I/O	MMC Data 6 (DAT6)
	SDnDAT7	I/O	MMC Data 7 (DAT7)
	SDnCD	Input	SD card detection
	SDnWP	Input	SD card write protection

39.2 Register Descriptions

39.2.1 SD_CMD : Command Type Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMD12AT[1:0]		TRSTP	CMDRW	CMDTP	RSPTP[2:0]			ACMD[1:0]		CMDIDX[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CMDIDX[5:0]	Command Index Field Value Select These bits configure the command index field value. The examples shown include the bit values for the ACMD[1:0] bits. 0x06: CMD6 0x12: CMD18 0x4D: ACMD13	R/W
7:6	ACMD[1:0]	Command Type Select 0 0: CMD 0 1: ACMD Others: Setting prohibited	R/W
10:8	RSPTP[2:0]	Response Type Select*1 0 0 0: Normal mode Depending on the command, the response type and transfer method are selected in the ACMD[1:0] and CMDIDX[5:0] bits. At this time, the values for bits 15 to 11 in this register are invalid. 0 1 1: Extended mode and no response 1 0 0: Extended mode and R1, R5, R6, or R7 response 1 0 1: Extended mode and R1b response 1 1 0: Extended mode and R2 response 1 1 1: Extended mode and R3 or R4 response Others: Setting prohibited	R/W

Table 39.2 SDHIIO引脚(n=0)(2of2)

Channel	引脚名称	I/O	Description
	SDnCMD	I/O	命令输出，响应输入
	SDnDAT0	I/O	Data 0 (DAT0)
	SDnDAT1	I/O	数据1(DAT1)，SDIO中断
	SDnDAT2	I/O	数据2(DAT2)，SDIO读取等待
	SDnDAT3	I/O	数据3(DAT3)，SD卡检测
	SDnDAT4	I/O	MMC Data 4 (DAT4)
	SDnDAT5	I/O	MMC Data 5 (DAT5)
	SDnDAT6	I/O	MMC Data 6 (DAT6)
	SDnDAT7	I/O	MMC Data 7 (DAT7)
	SDnCD	Input	SD卡检测
	SDnWP	Input	SD卡写保护

39.2 注册说明

39.2.1 SD_CMD:命令类型寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x000

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMD12AT[1:0]		TRSTP	CMDRW	CMDTP	RSPTP[2:0]			ACMD[1:0]		CMDIDX[5:0]					
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CMDIDX[5:0]	命令索引字段值选择 这些位配置命令索引字段值。所示示例包括ACMD[1:0]位的位值。 0x06: CMD6 0x12: CMD18 0x4D: ACMD13	R/W
7:6	ACMD[1:0]	命令类型选择 0 0: CMD 0 1: ACMD 其他：禁止设置	R/W
10:8	RSPTP[2:0]	响应类型选择*1 000：正常模式 根据命令，在ACMD[1:0]和CMDIDX[5:0]位中选择响应类型和传输方法。此时，该寄存器中第15位到第11位的值无效。 011：扩展模式和无响应100：扩展模式和R1、R5、R6 或R7响应101：扩展模式和R1b响应110：扩展模式和R2 响应111：扩展模式和R3或R4响应 其他：禁止设置	R/W

Bit	Symbol	Function	R/W
11	CMDTP	Data Transfer Select*2 0: Do not include data transfer (bc, bcr, or ac) in command 1: Include data transfer (adtc) in command	R/W
12	CMDRW	Data Transfer Direction Select*3 0: Write (SD/MMC Host Interface → SD card/MMC) 1: Read (SD/MMC Host Interface ← SD card/MMC)	R/W
13	TRSTP	Block Transfer Select*3 0: Single block transfer 1: Multiple blocks transfer	R/W
15:14	CMD12AT[1:0]	CMD12 Automatic Issue Select*4 0 0: Automatically issue CMD12 during multiblock transfer 0 1: Do not automatically issue CMD12 during multiblock transfer Others: Setting prohibited	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Some commands cannot be used in normal mode.
Note 2. The CMDTP bit is only valid when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b.
Note 3. Bits CMDRW and TRSTP are only valid when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b, and the CMDTP bit is 1.
Note 4. The CMD12AT[1:0] bits are only valid when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b, and the TRSTP bit is 1.

The command type and response type are set in the SD_CMD register. The command type and transfer mode must be set when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b. The sequence starts when a value is written to this register. See Table 39.8 and Table 39.9 for setting examples. Do not write to the SD_CMD register when the SD_INFO2.CBSY flag is 1.

39.2.2 SD_ARG : SD Command Argument Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	—	These bits specify command format[39:8] (argument).	R/W

The SD_ARG register is used for setting the argument field value. Set the SD_ARG register before setting the SD_CMD register. The argument field value of the automatically issued CMD12 is 0x0000_0000 regardless of the SD_ARG register value.

Bit	Symbol	Function	R/W
11	CMDTP	数据传输选择*2 0：在命令中不包括数据传输（bc、bcr或ac）1：在命令中包括数据传输（adtc）	R/W
12	CMDRW	数据传输方向选择*3 0：写入（SDMMC主机接口→SD卡MMC）1：读取（SDMMC主机接口←SD卡MMC）	R/W
13	TRSTP	块传输选择*3 0：单块传输1：多块传输	R/W
15:14	CMD12AT[1:0]	CMD12自动发行选择*4 00：在多块传输过程中自动发出CMD1201：在多块传输过程中不自动发出CMD12 其他：禁止设置	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.某些命令不能在正常模式下使用。
注2.CMDTP位仅在RSPTP[2:0]位为011b、100b、101b、110b或111b时有效。
注3.CMDRW和TRSTP位仅在RSPTP[2:0]位为011b、100b、101b、110b或111b且CMDTP位为1时有效。
注4.CMD12AT[1:0]位仅在RSPTP[2:0]位为011b、100b、101b、110b或111b且TRSTP位为1时有效。

命令类型和响应类型在SD_CMD寄存器中设置。当RSPTP[2:0]位为011b、100b、101b、110b或111b时，必须设置命令类型和传输模式。当一个值被写入该寄存器时，序列开始。设置示例见表39.8和表39.9。当SD_INFO2.CBSY标志为1时，不要写入SD_CMD寄存器。

39.2.2 SD_ARG:SD命令参数寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x008

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	—	这些位指定命令格式[39:8]（参数）。	R/W

SD_ARG寄存器用于设置参数字段值。在设置SD_CMD寄存器之前设置SD_ARG寄存器。无论SD_ARG寄存器的值如何，自动发出的CMD12的参数字段值为0x0000_0000。

39.2.3 SD_ARG1 : SD Command Argument Register 1

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits specify command format[39:24] (argument).	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The SD_ARG1 register is used for setting the argument field value. Set the SD_ARG1 register before setting the SD_CMD register. The argument field value of the automatically issued CMD12 is 0x0000_0000 regardless of the SD_ARG1 register value.

39.2.4 SD_STOP : Data Stop Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SEC	—	—	—	—	—	—	—	STP
Value after reset:	0	0	0	0	0	0	0	0*1	0	0	0	0	0	0	0	0*1

Bit	Symbol	Function	R/W
0	STP	Transfer Stop Data transfer stops when this bit is set to 1.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
8	SEC	Block Count Register Value Select*2 0: Disable SD_SECCNT register value 1: Enable SD_SECCNT register value	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. Do not rewrite this bit when the SD_INFO2.CBSY flag is 1.

The SD_STOP register stops data transfer. During a multiblock transfer sequence, the SD_SECCNT register value (number of blocks to be transferred) can be set to valid or invalid by setting the SD_STOP register.

STP bit (Transfer Stop)

When the STP bit is set to 1 during multiple block transfer, CMD12 is issued to halt the transfer through the SDHI. However, if a command sequence is halted because of a communications error or timeout, CMD12 is not issued. Although

39.2.3 SD_ARG1:SD命令参数寄存器1

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x00C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位指定命令格式[39:24]（参数）。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

SD_ARG1寄存器用于设置参数字段值。在设置SD_CMD寄存器之前设置SD_ARG1寄存器。无论SD_ARG1寄存器的值如何，自动发出的CMD12的参数字段值为0x0000_0000。

39.2.4 SD_STOP:数据停止寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x010

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SEC	—	—	—	—	—	—	—	STP
重置后的值:	0	0	0	0	0	0	0	0*1	0	0	0	0	0	0	0	0*1

Bit	Symbol	Function	R/W
0	STP	中转站 当该位设置为1时，数据传输停止。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
8	SEC	块计数寄存器值选择*2 0：禁用SD_SECCNT寄存器值1：启用SD_SECCNT寄存器值	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.当SD_INFO2.CBSY标志为1时，请勿重写该位。

SD_STOP寄存器停止数据传输。在多块传输序列期间，可以通过设置SD_STOP寄存器将SD_SECCNT寄存器值（要传输的块数）设置为有效或无效。

STP bit (Transfer Stop)

在多块传输期间STP位设置为1时，发出CMD12以停止通过SDHI的传输。
但是，如果命令序列由于通信错误或超时而停止，则不会发出CMD12。虽然

continued buffer access is possible even after STP is set to 1, the buffer access error bit (ILR or ILW) in SD_INFO2 is set accordingly.

When STP is set to 1 during transfer for single block write, the access end flag sets when SD_BUF becomes empty, and CMD12 is not issued. If SD_BUF does contain data, the access end flag sets on completion of reception of the busy state without CMD12 being issued.

When STP is set to 1 during transfer for single block read, the access end flag sets immediately after the STP bit is set, and CMD12 is not issued.

When STP is set to 1 during reception of the busy state after an R1b response, the access end flag sets on completion of reception of the busy state without CMD12 being issued.

When STP is set to 1 after a command sequence is completed, CMD12 is not issued and the access end flag does not set.

Set STP to 1 after the response end flag sets.

Set STP to 0 after the access end flag sets.

SEC bit (Block Count Register Value Select)

When SD_CMD is set in the following section to start the command sequence while the SEC bit is set to 1, CMD12 is automatically issued to stop multiblock transfer with the number of blocks set in SD_SECCNT.

CMD18 or CMD25 in normal mode (SD_CMD[10:8] = 000b)

SD_CMD[15:13] = 001b in extended mode (CMD12 is automatically issued, multiple block transfer)

When the command sequence is halted because of a communications error or timeout, CMD12 is not automatically issued.

39.2.5 SD_SECCNT : Block Count Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

When performing a multiblock transfer, SD_SECCNT is a read/write register used to set the number of blocks to be transferred. For example, when the register value is 0x0000_0001, 1 block is transferred. When the register value is 0x0000_FFFF, 65,535 blocks are transferred and when the register value is 0xFFFF_FFFF, 4,294,967,295 blocks are transferred. Do not set this register to 0x0000_0000. Do not rewrite the SD_SECCNT register when the SD_INFO2.CBSY flag is 1.

即使在STP设置为1后，仍可以继续访问缓冲区，相应地设置SD_INFO2中的缓冲区访问错误位（ILR或ILW）。

在单块写入的传输过程中将STP设置为1时，当SD_BUF为空时设置访问结束标志，并且不发出CMD12。如果SD_BUF确实包含数据，则在没有发出CMD12的忙状态接收完成时设置访问结束标志。

当STP在单块读取传输期间设置为1时，在设置STP位后立即设置访问结束标志，并且未发出CMD12。

当在R1b响应后的忙状态接收期间将STP设置为1时，在没有发出CMD12的忙状态接收完成时设置访问结束标志。

当命令序列完成后STP设置为1时，不发出CMD12并且不设置访问结束标志。

设置响应结束标志后将STP设置为1。

设置访问结束标志后将STP设置为0。

SEC位（块计数寄存器值选择）

当在以下部分中设置SD_CMD以启动命令序列而SEC位设置为1时，将自动发出CMD12以停止多块传输，其中块数在SD_SECCNT中设置。

正常模式下的CMD18或CMD25(SD_CMD[10:8]=000b)

SD_CMD[15:13]=001b扩展模式（CMD12自动发出，多块传输）

当命令序列由于通信错误或超时而停止时，不会自动发出CMD12。

39.2.5 SD_SECCNT：块计数寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

执行多块传输时，SD_SECCNT是一个读写寄存器，用于设置要传输的块数。例如，当寄存器值为0x0000_0001时，传输1个块。当寄存器值为0x0000_FFFF时，传送65 535个块，当寄存器值为0xFFFF_FFFF时，传送4 294 967 295个块。不要将此寄存器设置为0x0000_0000。当SD_INFO2.CBSY标志为1时，不要重写SD_SECCNT寄存器。

39.2.6 SD_RSPi : SD Card Response Register i (i = 10, 32, 54)

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x018; i = 10
0x020; i = 32
0x028; i = 54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

39.2.7 SD_RSPj : SD Card Response Register j (j = 1, 3, 5)

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x01C + (0x4 × (j - 1))

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	These bits store the response from the SD card/MMC.	R
31:16	—	These bits are read as 0.	R

39.2.8 SD_RSP76 : SD Card Response Register 76

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	SD_RSP76[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SD_RSP76[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	SD_RSP76[23:0]	These bits store the response from the SD card/MMC.	R
31:24	—	These bits are read as 0.	R

39.2.6 SD_RSPi:SD卡响应寄存器i(i=10 32 54)

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x018; i = 10
0x020; i = 32
0x028; i = 54

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

39.2.7 SD_RSPj:SD卡响应寄存器j(j=1 3 5)

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x01C + (0x4 × (j - 1))

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	—	这些位存储来自SD卡MMC的响应。	R
31:16	—	这些位读为0。	R

39.2.8 SD_RSP76:SD卡响应寄存器76

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x030

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	SD_RSP76[23:16]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	SD_RSP76[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
23:0	SD_RSP76[23:0]	这些位存储来自SD卡MMC的响应。	R
31:24	—	这些位读为0。	R

39.2.9 SD_RSP7 : SD Card Response Register 7

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SD_RSP7[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SD_RSP7[7:0]	These bits store the response from the SD card/MMC.	R
31:8	—	These bits are read as 0.	R

SD_RSP10, SD_RSP32, SD_RSP54, SD_RSP1, SD_RSP3, SD_RSP5, SD_RSP76, and SD_RSP7 are read-only registers that store the response from the SD card/MMC. Depending on the type of response from the SD card/MMC, the SD/MMC Host Interface divides and stores the response among the four registers.

Table 39.3 lists the correspondence between the response type and its storage destination.

Table 39.3 Correspondence between response type and storage destination

Response type	SD_RSP10 register	SD_RSP32 register	SD_RSP54 register	SD_RSP1 register	SD_RSP3 register	SD_RSP5 register	SD_RSP76 register	SD_RSP7 register
R1	[39:8]	—	[39:8]*1	—	—	—	—	—
R1b	[39:8]	—	[39:8]*1	—	—	—	—	—
R2	[39:8]	[71:40]	[103:72]	—	—	—	[127:104]	—
R3	[39:8]	—	—	—	—	—	—	—
R4	[39:8]	—	—	—	—	—	—	—
R5	[39:8]	—	—	—	—	—	—	—
R6	[39:8]	—	—	—	—	—	—	—
R7	[39:8]	—	—	—	—	—	—	—

Note 1. The responses for CMD18 and CMD25 are stored in registers SD_RSP10 and SD_RSP54. Therefore, even if the SD_RSP10 register is overwritten with the response for the automatically issued CMD12, the response for CMD18 or CMD25 can be confirmed by reading the SD_RSP54 register.

39.2.10 SD_INFO1 : SD Card Interrupt Flag Register 1

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x038

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SDD3MON	SDD3IN	SDD3RM	SDWPMON	—	SDCDMON	SDCDIN	SDCDRM	ACEND	—	RSPEND
Value after reset:	0	0	0	0	0	x	0	0	x	0	x	0	0	0*1	0	0*1

39.2.9 SD_RSP7:SD卡响应寄存器7

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x034

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	SD_RSP7[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	SD_RSP7[7:0]	这些位存储来自SD卡MMC的响应。	R
31:8	—	这些位读为0。	R

SD_RSP10、SD_RSP32、SD_RSP54、SD_RSP1、SD_RSP3、SD_RSP5、SD_RSP76和SD_RSP7是只读寄存器，用于存储来自SD卡MMC的响应。根据SD卡MMC的响应类型，SDMMC主机接口在四个寄存器之间划分和存储响应。

表39.3列出了响应类型与其存储目的地的对应关系。

Table 39.3 响应类型与存储目的地的对应关系

响应类型	SD_RSP10 register	SD_RSP32 register	SD_RSP54 register	SD_RSP1 register	SD_RSP3 register	SD_RSP5 register	SD_RSP76 register	SD_RSP7 register
R1	[39:8]	—	[39:8]*1	—	—	—	—	—
R1b	[39:8]	—	[39:8]*1	—	—	—	—	—
R2	[39:8]	[71:40]	[103:72]	—	—	—	[127:104]	—
R3	[39:8]	—	—	—	—	—	—	—
R4	[39:8]	—	—	—	—	—	—	—
R5	[39:8]	—	—	—	—	—	—	—
R6	[39:8]	—	—	—	—	—	—	—
R7	[39:8]	—	—	—	—	—	—	—

注1.CMD18和CMD25的响应存储在寄存器SD_RSP10和SD_RSP54中。因此，即使SD_RSP10寄存器被自动发出的CMD12的响应覆盖，CMD18或CMD25的响应可以通过读取SD_RSP54寄存器来确认。

39.2.10 SD_INFO1:SD卡中断标志寄存器1

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x038

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	SDD3MON	SDD3IN	SDD3RM	SDWPMON	—	SDCDMON	SDCDIN	SDCDRM	ACEND	—	RSPEND
重置后的值:	0	0	0	0	0	x	0	0	x	0	x	0	0	0*1	0	0*1

Bit	Symbol	Function	R/W
0	RSPEND	Response End Detection Flag 0: Response end not detected 1: Response end detected	R/(W)*2
1	—	This bit is read as 0. The write value should be 0.	R/W
2	ACEND	Access End Detection Flag 0: Access end not detected 1: Access end detected	R/(W)*2
3	SDCDRM	SDnCD Removal Flag 0: SD card/MMC removal not detected by the SDnCD pin 1: SD card/MMC removal detected by the SDnCD pin	R/(W)*2
4	SDCDIN	SDnCD Insertion Flag 0: SD card/MMC insertion not detected by the SDnCD pin 1: SD card/MMC insertion detected by the SDnCD pin	R/(W)*2
5	SDCDMON	SDnCD Pin Monitor Flag 0: SDnCD pin level is high*3 1: SDnCD pin level is low*3	R
6	—	This bit is read as 0. The write value should be 0.	R/W
7	SDWPMON	SDnWP Pin Monitor Flag 0: SDnWP pin level is high 1: SDnWP pin level is low	R
8	SDD3RM	SDnDAT3 Removal Flag 0: SD card/MMC removal not detected by the SDnDAT3 pin 1: SD card/MMC removal detected by the SDnDAT3 pin	R/(W)*2
9	SDD3IN	SDnDAT3 Insertion Flag 0: SD card/MMC insertion not detected by the SDnDAT3 pin 1: SD card/MMC insertion detected by the SDnDAT3 pin	R/(W)*2
10	SDD3MON	SDnDAT3 Pin Monitor Flag 0: SDnDAT3 pin level is low 1: SDnDAT3 pin level is high	R
31:11	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. The flag does not change even if set to 1. Writing 0 changes the flag value to 0.
Note 3. The flag changes when the pin level continues for the period set in the SD_OPTION.CTOP[3:0] bits or longer.

The SD_INFO1 register indicates the detection of a response end or access end for a command sequence. The SD_INFO1 register also indicates the detection SD card/MMC insertion/removal and the write protection status.

During a multiblock transfer sequence, if CMD12 or CMD52 (SDIO abort) is issued, the ACEND flag sets to 1, but the RSPEND flag remains set to 0.

If the command sequence is stopped because of a communication error or timeout, the ACEND flag or RSPEND flag sets to 1.

After a reset is canceled, the SDD3MON bit, SDD3IN flag, and SDD3RM flag values are changed in accordance with the status of the SDnDAT3 (n = 0) pin, and their values are changed when data is being transferred in wide bus mode. These 3 bits are used only for SD card. Set flags to be cleared to 0. Set flags that are not being cleared to 1.

RSPEND flag (Response End Detection Flag)

The RSPEND flag indicates that a response end was detected.

[Setting conditions]

- When reception of the response is completed
- When transmission of a command without response is completed
- When reception of the busy state after R1b response is completed
- When reception of the response to CMD52 that was issued by setting the C52PUB bit to 1 is completed for transfer of multiple block read

Bit	Symbol	Function	R/W
0	RSPEND	响应结束检测标志 0：未检测到响应结束1：检测到响应结束	R/(W)*2
1	—	该位读取为0。写入值应为0。	R/W
2	ACEND	访问结束检测标志 0：未检测到访问结束1：检测到访问结束	R/(W)*2
3	SDCDRM	SDnCD删除标志 0：SDnCD引脚未检测到SD卡MMC移除1：SDnCD引脚检测到SD卡MMC移除	R/(W)*2
4	SDCDIN	SDnCD插入标志 0：SDnCD引脚未检测到SD卡MMC插入1：SDnCD引脚检测到SD卡MMC插入	R/(W)*2
5	SDCDMON	SDnCD引脚监控标志 0：SDnCD引脚电平为高*3 1：SDnCD引脚电平低*3	R
6	—	该位读取为0。写入值应为0。	R/W
7	SDWPMON	SDnWP引脚监控标志 0：SDnWP引脚高电平1：SDnWP引脚低电平	R
8	SDD3RM	SDnDAT3删除标志 0：SDnDAT3引脚未检测到SD卡MMC移除1：SDnDAT3引脚检测到SD卡MMC移除	R/(W)*2
9	SDD3IN	SDnDAT3插入标志 0：SDnDAT3引脚未检测到SD卡MMC插入1：SDnDAT3引脚检测到SD卡MMC插入	R/(W)*2
10	SDD3MON	SDnDAT3引脚监控标志 0：SDnDAT3引脚低电平1：SDnDAT3引脚高电平	R
31:11	—	这些位被读取为0。写入值应为0。	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.即使设置为1，标志也不会改变。写入0会将标志值更改为0。
注3.当引脚电平持续SD_OPTION.CTOP[3:0]位中设置的周期或更长时间时，标志会发生变化。

SD_INFO1寄存器指示对命令序列的响应结束或访问结束的检测。SD_INFO1寄存器还指示检测SD卡MMC插入移除和写保护状态。

在多块传输序列期间，如果发出CMD12或CMD52（SDIO中止），则ACEND标志设置为1，但RSPEND标志保持设置为0。

如果命令序列由于通信错误或超时而停止，则ACEND标志或RSPEND标志设置为1。

复位取消后，SDD3MON位、SDD3IN标志和SDD3RM标志的值根据SDnDAT3(n=0)引脚的状态而改变，并且在宽总线模式下传输数据时它们的值也会改变。这3位仅用于SD卡。将要清除的标志设置为0。将未清除的标志设置为1。

RSPEND标志（响应结束检测标志）

RSPEND标志表示检测到响应结束。

[Setting conditions]

●响应接收完成时
●没有响应的命令传输完成时
●R1b响应后忙状态的接收完成时
●多块读取传送的C52PUB位为1的CMD52响应接收完成时

- When reception of the response to CMD52 that was issued by setting the C52PUB bit to 1 is completed for transfer of multiple block write
- This bit is set when a command sequence is halted because of a communications error or timeout.

[Clearing conditions]

- When 0 is written to RSPEND
- When a command without data is issued.

Note: When a command is issued in absence of data transfer, the RSPEND flag becomes 1 after the command sequence ends.

ACEND flag (Access End Detection Flag)

The ACEND flag indicates that an access end was detected.

[Setting conditions]

- When read access to the buffer is completed for transfer of single block read
- When read access to the buffer for the last block of data is completed for transfer of multiple block read
- When read access to the buffer and reception of the response to CMD12 are completed for transfer of multiple block read with automatic issuing of CMD12
- When reception of the busy state after reception of the CRC status is completed for transfer of single block write
- When reception of the busy state after reception of the CRC status of the last block of data is completed for transfer of multiple block write
- When reception of the response busy state for CMD12 is completed for transfer of multiple block write with automatic issuing of CMD12
- When reception of the response to CMD12 that was issued by setting the STP bit to1 is completed for transfer of multiple block read
- When reception of the response busy state for CMD12 that was issued by setting the STP bit to1 is completed for transfer of multiple block write
- When reception of the response to CMD52 that was issued by setting the IOABT bit to 1 is completed for transfer of multiple block read
- When reception of the response to CMD52 that was issued by setting the IOABT bit to1 is completed for transfer of multiple block write
- This bit is set when a command sequence is halted because of a communications error or timeout.

[Clearing conditions]

- When 0 is written to ACEND
- When the access end bit is set to 1.

Note: The ACEND flag becomes 1 after the command sequence ends.

SDCDRM flag (SDnCD Removal Flag)

The SDCDRM flag indicates that SDnCD was removed.

[Setting condition]

- After a change in SDnCD from 0 to 1, Mcycle elapsed with SDnCD held at 1.

[Clearing conditions]

- When 0 is written to SDCDRM.

Note: Mcycle is set in bits [3:0] in SD_OPTION.

SDCDIN flag (SDnCD Insertion Flag)

The SDCDIN flag indicates that SDnCD was inserted.

●多块写入传送的C52PUB位为1的CMD52响应接收完成时

●当命令序列由于通信错误或超时而停止时，该位被设置。

[Clearing conditions]

●RSPEND写入0时

●发出无数据指令时。

Note: 当在没有数据传输的情况下发出命令时，RSPEND标志在命令序列结束后变为1。

ACEND标志（访问结束检测标志）

ACEND标志表示检测到访问结束。

[Setting conditions]

●当完成对缓冲区的读取访问以传输单块读取时

●当完成对最后一个数据块的缓冲区的读取访问以传输多块读取时

●当对缓冲区的读取访问和对CMD12的响应的接收完成时，通过自动发出CMD12传输多块读取

●接收CRC状态后的busy状态接收完成时，用于单块写入传输

●当接收到最后一个数据块的CRC状态后的忙碌状态接收完成时，用于多块写入的传输

●当CMD12的响应忙状态接收完成时，用于传输多块写入并自动发出CMD12

●在多块读取的传送中，通过将STP位设置为1发出的对CMD12的响应的接收完成时

●多块写入的传送，通过将STP位设置为1发出的CMD12的响应忙状态接收完成时

●多块读取传送时，通过将IOABT位设置为1发出的对CMD52的响应的接收完成时

●多块写入传送的IOABT位为1的CMD52响应接收完成时

●当命令序列由于通信错误或超时而停止时，该位被设置。

[Clearing conditions]

●ACEND写入0时

●当访问结束位设置为1时。

Note: 命令序列结束后ACEND标志变为1。

SDCDRM标志（SDnCD移除标志）

SDCDRM标志表明SDnCD已被删除。

[Setting condition]

●在SDnCD从0变为1后，Mcycle过去了，而SDnCD保持在1。

[Clearing conditions]

●当0写入SDCDRM时。

Note: Mcycle在SD_OPTION的位[3:0]中设置。

SDCDIN标志（SDnCD插入标志）

SDCDIN标志表明SDnCD已插入。

[Setting condition]

- After a change in SDnCD from 1 to 0, Mcycle elapsed with SDnCD held at 0.

[Clearing conditions]

- When 0 is written to SDCDIN.

Note: Mcycle is set in bits [3:0] in SD_OPTION.

SDD3RM flag (SDnDAT3 Removal Flag)

The SDD3RM flag indicates that SDnDAT3 was removed.

[Setting condition]

- After a change in SDnDAT3 from 1 to 0, two cycles of PCLKB elapsed with SDnDAT3 held at 0.

[Clearing condition]

- When 0 is written to SDD3RM.

SDD3IN flag (SDnDAT3 Insertion Flag)

The SDD3IN flag indicates that SDnDAT3 was inserted.

[Setting condition]

- After a change in SDnDAT3 from 0 to 1, two cycles of PCLKB elapsed with SDnDAT3 held at 1.

[Clearing condition]

- When 0 is written to SDD3IN.

39.2.11 SD_INFO2 : SD Card Interrupt Flag Register 2

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x03C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ILA	CBSY	SD_CLK_CTRLEN	—	—	—	BWE	BRE	SDD0MON	RSPTO	ILR	ILW	DTO	ENDE	CRCE	CMDE
Value after reset:	0*1	0*1	1*1	0	x	0	0*1	0*1	x	0*1	0*1	0*1	0*1	0*1	0*1	0*1

Bit	Symbol	Function	R/W
0	CMDE	Command Error Detection Flag 0: Command error not detected 1: Command error detected	R/W*2
1	CRCE	CRC Error Detection Flag 0: CRC error not detected 1: CRC error detected	R/W*2
2	ENDE	End Bit Error Detection Flag 0: End bit error not detected 1: End bit error detected	R/W*2
3	DTO	Data Timeout Detection Flag 0: Data timeout not detected 1: Data timeout detected	R/W*2

[Setting condition]

●SDnCD从1变为0后，Mcycle在SDnCD保持在0的情况下经过。

[Clearing conditions]

●当0写入SDCDIN时。

Note: Mcycle在SD_OPTION的位[3:0]中设置。

SDD3RM标志（SDnDAT3移除标志）

SDD3RM标志表示SDnDAT3已被删除。

[Setting condition]

●SDnDAT3从1变为0后，经过两个PCLKB周期，SDnDAT3保持为0。

[Clearing condition]

●当0写入SDD3RM时。

SDD3IN标志（SDnDAT3插入标志）

SDD3IN标志表示SDnDAT3已插入。

[Setting condition]

●SDnDAT3从0变为1后，经过两个PCLKB周期，SDnDAT3保持在1。

[Clearing condition]

●当0写入SDD3IN时。

39.2.11 SD_INFO2:SD卡中断标志寄存器2

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x03C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ILA	CBSY	SD_CLK_CTRLEN	—	—	—	BWE	BRE	SDD0MON	RSPTO	ILR	ILW	DTO	ENDE	CRCE	CMDE
重置后的值:	0*1	0*1	1*1	0	x	0	0*1	0*1	x	0*1	0*1	0*1	0*1	0*1	0*1	0*1

Bit	Symbol	Function	R/W
0	CMDE	命令错误检测标志 0：未检测到命令错误1：检测到命令错误	R/W*2
1	CRCE	CRC错误检测标志 0：未检测到CRC错误1：检测到CRC错误	R/W*2
2	ENDE	结束位错误检测标志 0：未检测到结束位错误1：检测到结束位错误	R/W*2
3	DTO	数据超时检测标志 0：未检测到数据超时1：检测到数据超时	R/W*2

Bit	Symbol	Function	R/W
4	ILW	SD_BUF0 Illegal Write Access Detection Flag 0: Illegal write access to the SD_BUF0 register not detected 1: Illegal write access to the SD_BUF0 register detected	R/W*2
5	ILR	SD_BUF0 Illegal Read Access Detection Flag 0: Illegal read access to the SD_BUF0 register not detected 1: Illegal read access to the SD_BUF0 register detected	R/W*2
6	RSPTO	Response Timeout Detection Flag 0: Response timeout not detected 1: Response timeout detected	R/W*2
7	SDD0MON	SDHI_D0 Pin Status Flag 0: SDnDAT0 pin is low 1: SDnDAT0 pin is high	R
8	BRE	SD_BUF0 Read Enable Flag 0: Disable read access to the SD_BUF0 register 1: Enable read access to the SD_BUF0 register	R/W*2
9	BWE	SD_BUF0 Write Enable Flag 0: Disable write access to the SD_BUF0 register 1: Enable write access to the SD_BUF0 register	R/W*2
10	—	This bit is read as 0. The write value should be 0.	R/W
11	—	The read value is undefined. The write value should be 1.	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	SD_CLK_CTRLEN	SD_CLK_CTRL Write Enable Flag 0: SD/MMC bus (CMD and DAT lines) is busy, so write access to the SD_CLK_CTRL.CLKEN and CLKSEL[7:0] bits is disabled 1: SD/MMC bus (CMD and DAT lines) is not busy, so write access to the SD_CLK_CTRL.CLKEN and CLKSEL[7:0] bits is enabled	R
14	CBSY	Command Sequence Status Flag 0: Command sequence complete 1: Command sequence in progress (busy)	R
15	ILA	Illegal Access Error Detection Flag 0: Illegal access error not detected 1: Illegal access error detected	R/W*2
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. The flag does not change even if set to 1. Writing 0 changes the flag value to 0.

The SD_INFO2 register indicates the status of the SD buffer and the status of the SD card/MMC. Set flags to be cleared to 0. Set flags that are not being cleared to 1.

CMDE flag (Command Error Detection Flag)

The CMDE flag indicates that a command error was detected. The command sequence stops when a command error occurs. When the SDIO_MODE.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section section 39.3.12. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 39.3.13. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting conditions]

- The command index of the transmitted command differs from the command index of the received response.
- The command index of a command issued within a command sequence differs from the command index of the received response.

[Clearing condition]

- When 0 is written to CMDE.

Bit	Symbol	Function	R/W
4	ILW	SD_BUF0非法写访问检测标志 0：未检测到对SD_BUF0寄存器的非法写访问1：检测到对SD_BUF0寄存器的非法写访问	R/W*2
5	ILR	SD_BUF0非法读访问检测标志 0：未检测到对SD_BUF0寄存器的非法读访问1：检测到对SD_BUF0寄存器的非法读访问	R/W*2
6	RSPTO	响应超时检测标志 0：未检测到响应超时1：检测到响应超时	R/W*2
7	SDD0MON	SDHI_D0引脚状态标志 0：SDnDAT0引脚为低电平 1：SDnDAT0引脚为高电平	R
8	BRE	SD_BUF0读使能标志 0：禁用对SD_BUF0寄存器的读访问1：启用对SD_BUF0寄存器的读访问	R/W*2
9	BWE	SD_BUF0写使能标志 0：禁用对SD_BUF0寄存器的写访问1：启用对SD_BUF0寄存器的写访问	R/W*2
10	—	该位读取为0。写入值应为0。	R/W
11	—	读取值未定义。写入值应为1。	R/W
12	—	该位读取为0。写入值应为0。	R/W
13	SD_CLK_CTRLEN	SD_CLK_CTRL写使能标志 0：SDMMC总线（CMD和DAT线）忙，因此禁止对SD_CLK_CTRL.CLKEN和CLKSEL[7:0]位的写访问 1：SDMMC总线（CMD和DAT线）不忙，因此使能对SD_CLK_CTRL.CLKEN和CLKSEL[7:0]位的写访问	R
14	CBSY	命令序列状态标志 0：命令序列完成1：命令序列正在进行中（忙碌）	R
15	ILA	非法访问错误检测标志 0：未检测到非法访问错误1：检测到非法访问错误	R/W*2
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.即使设置为1，标志也不会改变。写入0会将标志值更改为0。

SD_INFO2寄存器指示SD缓冲区的状态和SD卡MMC的状态。将要清除的标志设置为0。将未清除的标志设置为1。

CMDE标志（命令错误检测标志）

CMDE标志指示检测到命令错误。发生命令错误时命令序列停止。
当SDIO_MODE.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行39.3.12节中所示的错误处理。IO_RW_EXTENDED命令（SD：CMD53多块读取）或第39.3.13节。IO_RW_EXTENDED命令（SD：CMD53MultipleBlockWrite），完成命令序列。

[Setting conditions]

●发送命令的命令索引与接收响应的命令索引不同。

●命令序列中发出的命令的命令索引与接收到的响应的命令索引不同。

[Clearing condition]

●当0写入CMDE时。

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CRCE flag (CRC Error Detection Flag)

The CRCE flag indicates that a CRC error was detected. The command sequence stops when a CRC error occurs. When the SDIO_MODE.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section 39.3.12. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 39.3.13. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting conditions]

- When an error occurs in the CRC status.
- When a CRC error occurs in the read data.
- When a CRC error occurs in the response.
- A CRC error in the response to a command issued within a command sequence.

[Clearing condition]

- When 0 is written to CRCE.

ENDE flag (End Bit Error Detection Flag)

The ENDE flag indicates that an end bit error was detected. The command sequence is stopped when an end bit error occurs. When the SDIO_MODE.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section 39.3.12. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 39.3.13. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting conditions]

- When an error occurs in the response length (and the end bit is not detected).
- When an error occurs in the read data length (and the end bit is not detected among the valid bits).
- When an error occurs in the CRC status length (and the end bit is not detected).
- An error in the length of a response to a command issued within a command sequence, for example when the end bit is not detected.

[Clearing condition]

- When 0 is written to ENDE.

DTO flag (Data Timeout Detection Flag)

The DTO flag indicates that a data timeout was detected. The command sequence stops when a data timeout occurs.

[Setting conditions]

- After R1b response, the busy state (SDnDAT0 = 0) continues for longer than Ncycle.
- After CRC status, the busy state (SDnDAT0 = 0) continues for longer than Ncycle.
- After write data, the CRC status is not received though Ncycle has elapsed.
- After read command, read data is not received though a time longer than Ncycle has elapsed.
- After CMD12 is issued within a command sequence, the busy state (SDnDAT0 = 0) for longer than Ncycle continues.
- After the reception of read data, read data for the next block are not received though a time longer than Ncycle has elapsed.
- After release of the read wait state, read data for the next block are not received though a time longer than Ncycle has elapsed.

Note: Ncycle is set in bits [7:4] in SD_OPTION.

[Clearing condition]

- When 0 is written to DTO.

CRCE标志（CRC错误检测标志）

CRCE标志表示检测到CRC错误。当发生CRC错误时，命令序列停止。当。。。的时候
SDIO_MODE.C52PUB位设置为1并自动发出CMD52，如果发生通信错误或响应超时，则命令序列未完成。执行39.3.12节中所示的错误处理。IO_RW_EXTENDED命令（SD：CMD53多块读取）或第39.3.13节。IO_RW_EXTENDED命令（SD：CMD53MultipleBlockWrite），完成命令序列。

[Setting conditions]

●CRC状态发生错误时。
●读取数据发生CRC错误时。
●当响应中出现CRC错误时。
●对命令序列中发出的命令的响应中出现CRC错误。

[Clearing condition]

●CRCE写入0时。

ENDE标志（结束位错误检测标志）

ENDE标志表示检测到结束位错误。当发生结束位错误时，命令序列停止。当SDIO_MODE.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行39.3.12节中所示的错误处理。IO_RW_EXTENDED命令（SD：CMD53多块读取）或第39.3.13节。IO_RW_EXTENDED命令（SD：CMD53MultipleBlockWrite），完成命令序列。

[Setting conditions]

●响应长度发生错误（未检测到结束位）时。
●读取数据长度出错时（有效位中未检测到结束位）。
●CRC状态长度出错（未检测到结束位）时。
●对命令序列中发出的命令的响应长度错误，例如未检测到结束位时。

[Clearing condition]

●0写入ENDE时。

DTO标志（数据超时检测标志）

DTO标志表示检测到数据超时。当发生数据超时时，命令序列停止。

[Setting conditions]

●R1b响应后，忙碌状态（SDnDAT0=0）持续时间超过Ncycle。
●CRC状态后，忙碌状态（SDnDAT0=0）持续时间超过Ncycle。
●写入数据后，虽然Ncycle已过，但仍未收到CRC状态。
●读取命令后，经过Ncycle后仍未收到读取数据。
●在命令序列内发出CMD12后，忙碌状态（SDnDAT0=0）持续时间超过Ncycle。
●读取数据接收后，虽然经过了Ncycle以上的时间，但没有接收到下一个块的读取数据。

●读取等待状态解除后，虽然经过了Ncycle以上的时间，但没有接收到下一个块的读取数据。

Note: Ncycle在SD_OPTION的位[7:4]中设置。

[Clearing condition]

●当0写入DTO时。

ILW flag (SD_BUF0 Illegal Write Access Detection Flag)

The ILW flag indicates that an SD_BUF0 illegal write access was detected.

[Setting conditions]

- When data is written to SD_BUF0 while it is not in the data read/write command state.
- When data is written to SD_BUF0 while SD_BUF is full.
- When data is written to SD_BUF0 while an error occurs in the CRC status or CRC status length.
- When data is written to SD_BUF0 while a busy state after the CRC status continues for longer than Ncycle.

Note: Ncycle is set in bits [7:4] in SD_OPTION.

[Clearing condition]

- When 0 is written to ILW.

ILR flag (SD_BUF0 Illegal Read Access Detection Flag)

The ILR flag indicates that an SD_BUF0 illegal read access was detected.

[Setting conditions]

- When SD_BUF is empty while SD_BUF0 is read.
- When data with a CRC error or END error is read from SD_BUF0.

[Clearing condition]

- When 0 is written to ILR.

RSPTO flag (Response Timeout Detection Flag)

The RSPTO flag indicates that a response timeout was detected. The command sequence is stopped when a response timeout occurs. When the SDIOMD.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section 39.3.12. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 39.3.13. IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting condition]

- When a response is not received though a time longer than 640 cycles of SD/MMC clock has elapsed (including a response to a command issued within a command sequence).

[Clearing condition]

- When 0 is written to RSPTO.

SDD0MON flag (SDHI_D0 Pin Status Flag)

The SDD0MON flag indicates the status of the SDHI_D0 pin. If the data timeout (DTO) is set but the response timeout (RSPTO) is not set after the Erase command is issued, the end of the Erase sequence (SDD0MON = 1) is confirmed by polling DAT0.

If a communication error or timeout occurs during a write sequence, the DAT0 bit might retain the value 0.

While the SD/MMC clock is stopped, the DAT0 bit retains the value before the clock is stopped.

BRE flag (SD_BUF0 Read Enable Flag)

The BRE flag indicates that SD_BUF0 is enabled for reading.

[Setting conditions]

- When data set in SD_SIZE is stored in SD_BUF0 at single block transfer.
- When data set in SD_SIZE is stored in either bank 1 or bank 2 of SD_BUF0 at multiple block transfer.

[Clearing conditions]

- When 0 is written to BRE

ILW标志（SD_BUF0非法写访问检测标志）

ILW标志表示检测到SD_BUF0非法写访问。

[Setting conditions]

●数据写入SD_BUF0时，SD_BUF0不处于数据读写命令状态。

●当SD_BUF已满而数据写入SD_BUF0时。

●当数据写入SD_BUF0且CRC状态或CRC状态长度发生错误时。

●当数据写入SD_BUF0时，CRC状态后的忙碌状态持续时间超过Ncycle。

Note: Ncycle在SD_OPTION的位[7:4]中设置。

[Clearing condition]

●当0写入ILW时。

ILR标志（SD_BUF0非法读访问检测标志）

ILR标志表示检测到SD_BUF0非法读取访问。

[Setting conditions]

●读取SD_BUF0时SD_BUF为空。

●从SD_BUF0读取CRC错误或END错误的数据时。

[Clearing condition]

●当0写入ILR时。

RSPTO标志（响应超时检测标志）

RSPTO标志表示检测到响应超时。当发生响应超时时，命令序列停止。当SDIOMD.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行39.3.12节中所示的错误处理。IO_RW_EXTENDED命令（SD：CMD53多块读取）或第39.3.13节。IO_RW_EXTENDED命令（SD：CMD53MultipleBlockWrite），完成命令序列。

[Setting condition]

●超过640个SDMMC时钟周期后仍未收到响应时（包括对命令序列内发出的命令的响应）。

[Clearing condition]

●当0写入RSPTO时。

SDD0MON标志（SDHI_D0引脚状态标志）

SDD0MON标志指示SDHI_D0引脚的状态。如果在发出擦除命令后设置了数据超时(DTO)但未设置响应超时(RSPTO)，则通过轮询DAT0确认擦除序列的结束(SDD0MON=1)。

如果在写入序列期间发生通信错误或超时，则DAT0位可能会保留值0。

SDMMC时钟停止时，DAT0位保持时钟停止前的值。

BRE标志（SD_BUF0读取启用标志）

BRE标志指示SD_BUF0已启用读取。

[Setting conditions]

●当SD_SIZE中设置的数据在单块传输时存储在SD_BUF0中。

●当SD_SIZE中设置的数据在多块传输中存储在SD_BUF0的bank1或bank2中时。

[Clearing conditions]

●BRE写入0时

- Reading of a block of data from SD_BUF0 by DMA transfer

When data is read from SD_BUF0 by the CPU, clear BRE then read the amount of data specified in SD_SIZE.
Even if a CRC error or an END error occurs while block data is read, data is stored in SD_BUF0 and BRE is set.

BWE flag (SD_BUF0 Write Enable Flag)

The BWE flag indicates that SD_BUF0 is enabled for writing.

[Setting conditions]

- When SD_BUF0 is empty at single block transfer.
- When either bank 1 or bank 2 of SD_BUF0 is empty at multiple block transfer.

[Clearing conditions]

- When 0 is written to BWE.
- Writing of a block of data to SD_BUF0 by DMA transfer.

When data is written to SD_BUF0 by the CPU, clear BWE and then write the amount of data specified in SD_SIZE.

SD_CLK_CTRLEN flag (SD_CLK_CTRL Write Enable Flag)

When a command sequence is started by writing to SD_CMD, the CBSY bit is set to 1 and, at the same time, the SD_CLK_CTRLEN bit is set to 0. The SD_CLK_CTRLEN bit is set to 1 after 8 cycles of SDCLK have elapsed after the CBSY bit clears to 0 on completion of the command sequence.

ILA flag (Illegal Access Error Detection Flag)

The ILA flag indicates that an illegal access error was detected.

[Setting conditions]

- Writing of data to SD_CMD within a command sequence (CBSY = 1).
- When SD_CMD[11] = 1 (command with data transfer) and SD_CMD[7:0] = 0000 1100b (CMD12) are set in SD_CMD.

[Clearing condition]

- When 0 is written to ILA.

39.2.12 SD_INFO1_MASK : SD INFO1 Interrupt Mask Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x040

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SDD3INM	SDD3RMM	—	—	—	SDCDINM	SDCDRMM	ACENDM	—	RSPENDM
Value after reset:	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1

Bit	Symbol	Function	R/W
0	RSPENDM	Response End Interrupt Request Mask 0: Do not mask response end interrupt request 1: Mask response end interrupt request	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W

●通过DMA传输从SD_BUF0读取数据块

当CPU从SD_BUF0读取数据时，清除BRE，然后读取SD_SIZE中指定的数据量。
即使在读取块数据时发生CRC错误或END错误，数据也会存储在SD_BUF0中并设置BRE。

BWE标志（SD_BUF0写使能标志）

BWE标志指示SD_BUF0已启用写入。

[Setting conditions]

●单块传输时SD_BUF0为空时。

●多块传输时SD_BUF0的bank1或bank2为空时。

[Clearing conditions]

●当0写入BWE时。

●通过DMA传输将数据块写入SD_BUF0。

当CPU将数据写入SD_BUF0时，清除BWE，然后写入SD_SIZE中指定的数据量。

SD_CLK_CTRLEN标志（SD_CLK_CTRL写使能标志）

当通过写入SD_CMD启动命令序列时，CBSY位设置为1，同时，
SD_CLK_CTRLEN位设置为0。SD_CLK_CTRLEN位在SDCLK 的8个周期后设置为1。
CBSY位在命令序列完成时清零。

ILA标志（非法访问错误检测标志）

ILA标志表示检测到非法访问错误。

[Setting conditions]

●在命令序列中将数据写入SD_CMD(CBSY=1)。

●当SD_CMD[11]=1（有数据传输的命令）且SD_CMD[7:0]=00001100b(CMD12)在SD_CMD中设置。

[Clearing condition]

●当0写入ILA时。

39.2.12 SD_INFO1_MASK:SDINFO1中断屏蔽寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x040

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	SDD3INM	SDD3RMM	—	—	—	SDCDINM	SDCDRMM	ACENDM	—	RSPENDM
重置后的值:	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1

Bit	Symbol	Function	R/W
0	RSPENDM	响应结束中断请求掩码 0：不屏蔽响应结束中断请求1：屏蔽响应结束中断请求	R/W
1	—	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
2	ACENDM	Access End Interrupt Request Mask 0: Do not mask access end interrupt request 1: Mask access end interrupt request	R/W
3	SDCDRMM	SDnCD Removal Interrupt Request Mask 0: Do not mask SD card/MMC removal interrupt request by the SDnCD pin 1: Mask SD card/MMC removal interrupt request by the SDnCD pin	R/W
4	SDCDINM	SDnCD Insertion Interrupt Request Mask 0: Do not mask SD card/MMC insertion interrupt request by the SDnCD pin 1: Mask SD card/MMC insertion interrupt request by the SDnCD pin	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W
8	SDD3RMM	SDnDAT3 Removal Interrupt Request Mask 0: Do not mask SD card/MMC removal interrupt request by the SDnDAT3 pin 1: Mask SD card/MMC removal interrupt request by the SDnDAT3 pin	R/W
9	SDD3INM	SDnDAT3 Insertion Interrupt Request Mask 0: Do not mask SD card/MMC insertion interrupt request by the SDnDAT3 pin 1: Mask SD card/MMC insertion interrupt request by the SDnDAT3 pin	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

The SD_INFO1_MASK register enables or disables interrupt requests from the status flags in the SD_INFO1 register. See Table 39.5, for details on the relationship between the status flags and the requested interrupt source.

39.2.13 SD_INFO2_MASK : SD INFO2 Interrupt Mask Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x044

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ILAM	—	—	—	—	—	BWEM	BREM	—	RSPTOM	ILRM	ILWM	DTOM	ENDEM	CRCEM	CMDEM
Value after reset:	1	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CMDEM	Command Error Interrupt Request Mask 0: Do not mask command error interrupt request 1: Mask command error interrupt request	R/W
1	CRCEM	CRC Error Interrupt Request Mask 0: Do not mask CRC error interrupt request 1: Mask CRC error interrupt request	R/W
2	ENDEM	End Bit Error Interrupt Request Mask 0: Do not mask end bit detection error interrupt request 1: Mask end bit detection error interrupt request	R/W
3	DTOM	Data Timeout Interrupt Request Mask 0: Do not mask data timeout interrupt request 1: Mask data timeout interrupt request	R/W
4	ILWM	SD_BUF0 Register Illegal Write Interrupt Request Mask 0: Do not mask illegal write detection interrupt request for the SD_BUF0 register 1: Mask illegal write detection interrupt request for the SD_BUF0 register	R/W
5	ILRM	SD_BUF0 Register Illegal Read Interrupt Request Mask 0: Do not mask illegal read detection interrupt request for the SD_BUF0 register 1: Mask illegal read detection interrupt request for the SD_BUF0 register	R/W

Bit	Symbol	Function	R/W
2	ACENDM	访问结束中断请求掩码 0：不屏蔽访问结束中断请求1：屏蔽访问结束中断请求	R/W
3	SDCDRMM	SDnCD移除中断请求掩码 0：不通过SDnCD引脚屏蔽SD卡MMC移除中断请求1：通过SDnCD引脚屏蔽SD卡MMC移除中断请求	R/W
4	SDCDINM	SDnCD插入中断请求掩码 0：不通过SDnCD引脚屏蔽SD卡MMC插入中断请求1：通过SDnCD引脚屏蔽SD卡MMC插入中断请求	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W
8	SDD3RMM	SDnDAT3移除中断请求掩码 0：不通过SDnDAT3引脚屏蔽SD卡MMC移除中断请求1：通过SDnDAT3引脚屏蔽SD卡MMC移除中断请求	R/W
9	SDD3INM	SDnDAT3插入中断请求掩码 0：不通过SDnDAT3引脚屏蔽SD卡MMC插入中断请求1：通过SDnDAT3引脚屏蔽SD卡MMC插入中断请求	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

SD_INFO1_MASK寄存器启用或禁用来自SD_INFO1寄存器中状态标志的中断请求。看表39.5，详细了解状态标志和请求的中断源之间的关系。

39.2.13 SD_INFO2_MASK:SDINFO2中断屏蔽寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x044

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ILAM	—	—	—	—	—	BWEM	BREM	—	RSPTOM	ILRM	ILWM	DTOM	ENDEM	CRCEM	CMDEM
重置后的值：	1	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	CMDEM	命令错误中断请求掩码 0：不屏蔽命令错误中断请求1：屏蔽命令错误中断请求	R/W
1	CRCEM	CRC错误中断请求掩码 0：不屏蔽CRC错误中断请求1：屏蔽CRC错误中断请求	R/W
2	ENDEM	结束位错误中断请求掩码 0：不屏蔽结束位检测错误中断请求1：屏蔽结束位检测错误中断请求	R/W
3	DTOM	数据超时中断请求掩码 0：不屏蔽数据超时中断请求1：屏蔽数据超时中断请求	R/W
4	ILWM	SD_BUF0寄存器非法写中断请求掩码 0：不屏蔽SD_BUF0寄存器的非法写检测中断请求1：屏蔽SD_BUF0寄存器的非法写检测中断请求	R/W
5	ILRM	SD_BUF0寄存器非法读中断请求掩码 0：不屏蔽SD_BUF0寄存器的非法读检测中断请求1：屏蔽SD_BUF0寄存器的非法读检测中断请求	R/W

Bit	Symbol	Function	R/W
6	RSPTOM	Response Timeout Interrupt Request Mask 0: Do not mask response timeout interrupt request 1: Mask response timeout interrupt request	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W
8	BREM*1	BRE Interrupt Request Mask 0: Do not mask read enable interrupt request for the SD buffer 1: Mask read enable interrupt request for the SD buffer	R/W
9	BWEM*1	BWE Interrupt Request Mask 0: Do not mask write enable interrupt request for the SD_BUF0 register 1: Mask write enable interrupt request for the SD_BUF0 register	R/W
10	—	This bit is read as 0. The write value should be 0.	R/W
11	—	This bit is read as 1.The write value should be 1.	R/W
14:12	—	These bits are read as 0. The write value should be 0.	R/W
15	ILAM	Illegal Access Error Interrupt Request Mask 0: Do not mask illegal access error interrupt request 1: Mask illegal access error interrupt request	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the SD_INFO2_MASK.BWEM bit is 0 or the SD_INFO2_MASK.BREM bit is 0, set the SD_DMAEN.DMAEN bit to 0. When the SD_DMAEN.DMAEN bit is 1, set the SD_INFO2_MASK.BWEM bit to 1 and the SD_INFO2_MASK.BREM bit to 1.

The SD_INFO2_MASK register enables or disables interrupt requests from the status flags in the SD_INFO2 register. See Table 39.5 for details on the relationship between the status flags and the requested interrupt source.

39.2.14 SD_CLK_CTRL : SD Clock Control Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x048

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CLKCTRLEN	CLKEN	CLKSEL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0*1	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CLKSEL[7:0]	SDHI Clock Frequency Select*2 0xFF PCLKB 0x00: PCLKB/2 0x01: PCLKB/4 0x02: PCLKB/8 0x04: PCLKB/16 0x08: PCLKB/32 0x10: PCLKB/64 0x20: PCLKB/128 0x40: PCLKB/256 0x80: PCLKB/512 Others: Setting prohibited	R/W
8	CLKEN	SD/MMC Clock Output Control*2 0: Disable SD/MMC clock output (fix SDnCLK signal low) 1: Enable SD/MMC clock output	R/W

Bit	Symbol	Function	R/W
6	RSPTOM	响应超时中断请求掩码 0：不屏蔽响应超时中断请求1：屏蔽响应超时中断请求	R/W
7	—	该位读取为0。写入值应为0。	R/W
8	BREM*1	BRE中断请求掩码 0：不屏蔽SD缓冲区的读使能中断请求1：屏蔽SD缓冲区的读使能中断请求	R/W
9	BWEM*1	BWE中断请求掩码 0：不屏蔽SD_BUF0寄存器的写使能中断请求1：屏蔽SD_BUF0寄存器的写使能中断请求	R/W
10	—	该位读取为0。写入值应为0。	R/W
11	—	该位读取为1。写入值应为1。	R/W
14:12	—	这些位被读取为0。写入值应为0。	R/W
15	ILAM	非法访问错误中断请求掩码 0：不屏蔽非法访问错误中断请求1：屏蔽非法访问错误中断请求	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.当SD_INFO2_MASK.BWEM位为0或SD_INFO2_MASK.BREM位为0时，将SD_DMAEN.DMAEN位设置为0。当SD_DMAEN.DMAEN位为1时，将SD_INFO2_MASK.BWEM位设置为1和SD_INFO2_MASK。BREM位为1。

SD_INFO2_MASK寄存器启用或禁用来自SD_INFO2寄存器中状态标志的中断请求。看表39.5详细说明了状态标志和请求的中断源之间的关系。

39.2.14 SD_CLK_CTRL:SD时钟控制寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x048

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CLKCTRLEN	CLKEN	CLKSEL[7:0]							
重置后的值：	0	0	0	0	0	0	0	0*1	0	0	1	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CLKSEL[7:0]	SDHI时钟频率选择*2 0xFF PCLKB 0x00: PCLKB/2 0x01: PCLKB/4 0x02: PCLKB/8 0x04: PCLKB/16 0x08: PCLKB/32 0x10: PCLKB/64 0x20: PCLKB/128 0x40: PCLKB/256 0x80: PCLKB/512 其他：禁止设置	R/W
8	CLKEN	SDMMC时钟输出控制*2 0：禁用SDMMC时钟输出（固定SDnCLK信号为低电平）1：启用SDMMC时钟输出	R/W

Bit	Symbol	Function	R/W
9	CLKCTRLEN	SD/MMC Clock Output Automatic Control Select 0: Disable automatic control of SD/MMC clock output 1: Enable automatic control of SD/MMC clock output	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. Bits CLKSEL[7:0] and CLKEN cannot be write accessed when the SD_INFO2.SD_CLK_CTRLEN flag is 0.

The SDCLKCTRL register controls the SD/MMC clock frequency settings and output. Set the CLKEN bit to 1 before writing to the SD_CMD register to start a command sequence. Do not write to the SDCLKCTRL register when the SD_INFO2.SD_CLK_CTRLEN flag is 0.

CLKCTRLEN bit (SD/MMC Clock Output Automatic Control Select)

The CLKCTRLEN bit enables or disables the automatic control function for SD/MMC clock output, which causes the SD/MMC clock to output only within a command sequence.

The timing with which SD/MMC clock output starts and stops is as follows:

- SD/MMC clock output starts after writing to SD_CMD
- SD/MMC clock output stops when 8 cycles of SD/MMC clock have elapsed after the end of the command sequence.

In addition, SD/MMC clock is fixed to 0 while SCLKEN of SD_CLK_CTRL is 0, regardless of the value of this bit.

39.2.15 SD_SIZE : Transfer Data Length Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x04C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	LEN[9:0]									
Value after reset:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	LEN[9:0]	Transfer Data Size Setting These bits specify the transfer data size.*1	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite these bits when the SD_INFO2.CBSY flag is 1.

The SD_SIZE register sets the transfer data size.

LEN[9:0] bits (Transfer Data Size Setting)

When using single block transfer, the transfer data size can be set in the LEN[9:0] bits from 1 byte to 512 bytes. When CMD12 is automatically issued during a multiblock transfer sequence (CMD18 and CMD25), the transfer data size can only be set to 512 bytes. When CMD12 is not automatically issued during a multiblock transfer sequence, the transfer data size can be set to 32, 64, 128, 256, or 512 bytes. However, a 32-, 64-, 128-, or 256-byte multiblock read transfer can only be performed during an SDIO multiblock transfer (CMD53). Do not set these bits to 0 when using a command that includes data transfer.

Bit	Symbol	Function	R/W
9	CLKCTRLEN	SDMMC时钟输出自动控制选择 0：禁止SDMMC时钟输出自动控制1：使能SDMMC时钟输出自动控制	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.当SD_INFO2.SD_CLK_CTRLEN标志为0时，不能写访问位CLKSEL[7:0]和CLKEN。

SDCLK CTRL寄存器控制SDMMC时钟频率设置和输出。在写入SD_CMD寄存器以启动命令序列之前，将CLKEN位设置为1。当SD_INFO2.SD_CLK_CTRLEN标志为0时，不要写入SDCLK CTRL寄存器。

CLKCTRLEN位（SDMMC时钟输出自动控制选择）

CLKCTRLEN位启用或禁用SDMMC时钟输出的自动控制功能，这会导致SDMMC时钟仅在命令序列内输出。

SDMMC时钟输出开始和停止的时序如下：

●写入SD_CMD后开始SDMMC时钟输出

●在命令序列结束后经过8个SDMMC时钟周期时，SDMMC时钟输出停止。

此外，SDMMC时钟固定为0，而SD_CLK_CTRL的SCLKEN为0，与该位的值无关。

39.2.15 SD_SIZE：传输数据长度寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x04C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	LEN[9:0]									
重置后的值：	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	LEN[9:0]	传输数据大小设置 这些位指定传输数据大小。*1	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

注1.当SD_INFO2.CBSY标志为1时，不要重写这些位。

SD_SIZE寄存器设置传输数据大小。

LEN[9:0]位（传输数据大小设置）

使用单块传输时，传输数据大小可以在LEN[9:0]位中设置，从1字节到512字节。什么时候CMD12在多块传输序列（CMD18和CMD25）期间自动发出，传输数据大小只能设置为512字节。在多块传输序列期间未自动发出CMD12时，传输数据大小可设置为32、64、128、256或512字节。但是，只能在SDIO多块传输(CMD53)期间执行32、64、128或256字节的多块读取传输。使用包含数据传输的命令时，请勿将这些位设置为0。

39.2.16 SD_OPTION : SD Card Access Control Option Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x050

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WIDTH	—	WIDTH8	—	—	—	—	TOUTMASK	TOP[3:0]				CTOP[3:0]			
Value after reset:	0*1	1	0*1	0	0	0	0	0*1	1*1	1*1	1*1	0*1	1*1	1*1	1*1	0*1

Bit	Symbol	Function	R/W
3:0	CTOP[3:0]	Card Detection Time Counter*2 0x0: PCLKB × 2^{10} 0x1: PCLKB × 2^{11} 0x2: PCLKB × 2^{12} 0x3: PCLKB × 2^{13} 0x4: PCLKB × 2^{14} 0x5: PCLKB × 2^{15} 0x6: PCLKB × 2^{16} 0x7: PCLKB × 2^{17} 0x8: PCLKB × 2^{18} 0x9: PCLKB × 2^{19} 0xA: PCLKB × 2^{20} 0xB: PCLKB × 2^{21} 0xC: PCLKB × 2^{22} 0xD: PCLKB × 2^{23} 0xE: PCLKB × 2^{24} 0xF: Setting prohibited	R/W
7:4	TOP[3:0]	Timeout Counter*2 0x0: SDHI clock × 2^{13} 0x1: SDHI clock × 2^{14} 0x2: SDHI clock × 2^{15} 0x3: SDHI clock × 2^{16} 0x4: SDHI clock × 2^{17} 0x5: SDHI clock × 2^{18} 0x6: SDHI clock × 2^{19} 0x7: SDHI clock × 2^{20} 0x8: SDHI clock × 2^{21} 0x9: SDHI clock × 2^{22} 0xA: SDHI clock × 2^{23} 0xB: SDHI clock × 2^{24} 0xC: SDHI clock × 2^{25} 0xD: SDHI clock × 2^{26} 0xE: SDHI clock × 2^{27} 0xF: Setting prohibited	R/W
8	TOUTMASK	Timeout Mask 0: Activate timeout 1: Inactivate timeout (do not set RSPTO and DTO bits of SD_INFO2 or CRCBSYTO, CRCTO, RDTO, BSYTO1, BSYTO0, RSPTO1 and RSPTO0 bits of SD_ERR_STS2) When timeout occurs because of an inactivated timeout, execute a software reset to terminate the command sequence.	R/W
12:9	—	These bits are read as 0. The write value should be 0.	R/W

39.2.16 SD_OPTION:SD卡访问控制选项寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x050

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	WIDTH	—	WIDTH8	—	—	—	—	兜售面膜	TOP[3:0]				CTOP[3:0]			
重置后的值:	0*1	1	0*1	0	0	0	0	0*1	1*1	1*1	1*1	0*1	1*1	1*1	1*1	0*1

Bit	Symbol	Function	R/W
3:0	CTOP[3:0]	卡片检测时间计数器*2 0x0: PCLKB × 2^{10} 0x1: PCLKB × 2^{11} 0x2: PCLKB × 2^{12} 0x3: PCLKB × 2^{13} 0x4: PCLKB × 2^{14} 0x5: PCLKB × 2^{15} 0x6: PCLKB × 2^{16} 0x7: PCLKB × 2^{17} 0x8: PCLKB × 2^{18} 0x9: PCLKB × 2^{19} 0xA: PCLKB × 2^{20} 0xB: PCLKB × 2^{21} 0xC: PCLKB × 2^{22} 0xD: PCLKB × 2^{23} 0xE: PCLKB × 2^{24} 0xF：禁止设置	R/W
7:4	TOP[3:0]	超时计数器*2 0x0: SDHI clock × 2^{13} 0x1: SDHI clock × 2^{14} 0x2: SDHI clock × 2^{15} 0x3: SDHI clock × 2^{16} 0x4: SDHI clock × 2^{17} 0x5: SDHI clock × 2^{18} 0x6: SDHI clock × 2^{19} 0x7: SDHI clock × 2^{20} 0x8: SDHI clock × 2^{21} 0x9: SDHI clock × 2^{22} 0xA: SDHI clock × 2^{23} 0xB: SDHI clock × 2^{24} 0xC: SDHI clock × 2^{25} 0xD: SDHI clock × 2^{26} 0xE: SDHI clock × 2^{27} 0xF：禁止设置	R/W
8	TOUTMASK	超时掩码 0：激活超时1：不激活超时（不要设置SD_INFO2的RSPTO和DTO位或CRCBSYTO、CRCTO、RDTO、BSYTO1、BSYTO0、RSPTO1和RSPTO0位 SD_ERR_STS2) 当由于未激活超时而发生超时时，执行软件复位以终止命令序列。	R/W
12:9	—	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Function	R/W
13	WIDTH8	Bus Width*2 See bit 15 WIDTH bit.	R/W
14	—	This bit is read as 1. The write value should be 1.	R/W
15	WIDTH	Bus Width*2 WIDTH / WIDTH8 / Bus Width: 0 / 1 / 8-bit width 0 / 0 / 4-bit width 1 / 0 / 1-bit width 1 / 1 / 1-bit width For 1-byte write transfers, set 4-bit or 1-bit width. Do not set 8-bit width.	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. Do not rewrite these bits when the SD_INFO2.CBSY flag is 1.

The SD bus width and timeout counter are set in the SD_OPTION register.

39.2.17 SD_ERR_STS1 : SD Error Status Register 1

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x058

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CRCTK[2:0]			CRCTKE	RDCRCE	RSPCRCE1	RSPCRCE0	—	—	CRCLENE	RDLENE	RSPLENE1	RSPLENE0	CMDE1	CMDE0
Value after reset:	0	0*1	1*1	0*1	0*1	0*1	0*1	0*1	0	0	0*1	0*1	0*1	0*1	0*1	0*1

Bit	Symbol	Function	R/W
0	CMDE0	Command Error Flag 0 0: No error exists in command index field value of a command*2 response 1: Error exists in command index field value of a command*2 response	R
1	CMDE1	Command Error Flag 1 0: No error exists in command index field value of a command*3 response 1: Error exists in command index field value of a command*3 response (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the CMDE0 flag)	R
2	RSPLENE0	Response Length Error Flag 0 0: No error exists in command*2 response length 1: Error exists in command*2 response length	R
3	RSPLENE1	Response Length Error Flag 1 0: No error exists in command*3 response length 1: Error exists in command*3 response length (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the RSPLENE0 flag)	R
4	RDLENE	Read Data Length Error Flag 0: No read data length error occurred 1: Read data length error occurred	R
5	CRCLENE	CRC Status Token Length Error Flag 0: No CRC status token length error occurred 1: CRC status token length error occurred	R

Bit	Symbol	Function	R/W
13	WIDTH8	总线宽度*2 请参见位15WIDTH位。	R/W
14	—	该位读取为1。写入值应为1。	R/W
15	WIDTH	总线宽度*2 WIDTH / WIDTH8 / 总线宽度: 0 / 1 / 8-bit width 0 / 0 / 4-bit width 1 / 0 / 1-bit width 1 / 1 / 1-bit width 对于1字节写传输，设置4位或1位宽度。不要设置8位宽度。	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.当SD_INFO2.CBSY标志为1时，不要重写这些位。

SD总线宽度和超时计数器在SD_OPTION寄存器中设置。

39.2.17 SD_ERR_STS1：SD错误状态寄存器1

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x058

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CRCTK[2:0]			CRCTKE	RDCRCE	RSPCRCE1	RSPCRCE0	—	—	CRCLENE	RDLENE	RSPLENE1	RSPLENE0	CMDE1	CMDE0
重置后的值:	0	0*1	1*1	0*1	0*1	0*1	0*1	0*1	0	0	0*1	0*1	0*1	0*1	0*1	0*1

Bit	Symbol	Function	R/W
0	CMDE0	命令错误标志0 0：命令*2响应的命令索引字段值不存在错误1：命令*2响应的命令索引字段值存在错误	R
1	CMDE1	命令错误标志1 0：命令*3响应的命令索引字段值中不存在错误1：命令*3响应的命令索引字段值中存在错误（带有 SD_CMD.CMDIDX[5:0]设置，CMD12问题发生的错误在CMDE0标志中指示）	R
2	RSPLENE0	响应长度错误标志0 0：指令*2响应长度无错误1：指令*2响应长度有错误	R
3	RSPLENE1	响应长度错误标志1 0：命令*3响应长度中不存在错误1：命令*3响应长度中存在错误（使用SD_CMD.CMDIDX[5:0]设置，在RSPLENE0标志中指示CMD12问题发生的错误）	R
4	RDLENE	读取数据长度错误标志 0：未发生读取数据长度错误1：发生读取数据长度错误	R
5	CRCLENE	CRC状态令牌长度错误标志 0：未发生CRC状态令牌长度错误1：发生CRC状态令牌长度错误	R

Bit	Symbol	Function	R/W
7:6	—	These bits are read as 0.	R
8	RSPCRCE0	Response CRC Error Flag 0 0: No CRC error detected in command*2 response 1: CRC error detected in command*2 response	R
9	RSPCRCE1	Response CRC Error Flag 1 0: No CRC error detected in command*3 response (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the RSPCRCE0 flag) 1: CRC error detected in command*3 response	R
10	RDCRCE	Read Data CRC Error Flag 0: No CRC error detected in read data 1: CRC error detected in read data	R
11	CRCTKE	CRC Status Token Error Flag 0: No error detected in CRC status token 1: Error detected in CRC status token	R
14:12	CRCTK[2:0]	CRC Status Token These bits store the CRC status token value (normal value is 010b).	R
15	—	This bit is read as 0.	R
31:16	—	These bits are read as 0.	R

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 3. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.

The SD_ERR_STS1 register indicates the CRC status token, CRC error, end bit error, and command error.

39.2.18 SD_ERR_STS2 : SD Error Status Register 2

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x05C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	CRCBSYTO	CRCTO	RDTO	BSYTO1	BSYTO0	RSPTO1	RSPTO0
Value after reset:	0	0	0	0	0	0	0	0	0	0*1	0*1	0*1	0*1	0*1	0*1	0*1

Bit	Symbol	Function	R/W
0	RSPTO0	Response Timeout Flag 0 0: After command*2 was issued, response was received in less than 640 cycles of the SD/MMC clock 1: After command*2 was issued, response was not received in 640 or more cycles of the SD/MMC clock	R
1	RSPTO1	Response Timeout Flag 1 0: After command*3 was issued, response was received in less than 640 cycles of the SD/MMC clock 1: After command*3 was issued, response was not received after 640 or more cycles of the SD/MMC clock (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the RSPTO0 flag)	R

Bit	Symbol	Function	R/W
7:6	—	这些位读为0。	R
8	RSPCRCE0	响应CRC错误标志0 0：在命令*2响应中未检测到CRC错误1：在命令*2响应中检测到CRC错误	R
9	RSPCRCE1	响应CRC错误标志1 0：在命令*3响应中未检测到CRC错误（使用SD_CMD.CMDIDX[5:0]设置，在RSPCRCE0标志中指示CMD12问题发生的错误） 1：在命令*3响应中检测到CRC错误	R
10	RDCRCE	读取数据CRC错误标志 0：读取数据中未检测到CRC错误1：读取数据中检测到CRC错误	R
11	CRCTKE	CRC状态令牌错误标志 0：在CRC状态令牌中未检测到错误1：在CRC状态令牌中检测到错误	R
14:12	CRCTK[2:0]	CRC状态令牌 这些位存储CRC状态令牌值（正常值为010b）。	R
15	—	该位读为0。	R
31:16	—	这些位读为0。	R

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.通过SD_CMD中的设置，CMD12之外的CMD SD_STOP中的STP位设置为1，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
注3.通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12 SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。

SD_ERR_STS1寄存器指示CRC状态令牌、CRC错误、结束位错误和命令错误。

39.2.18 SD_ERR_STS2：SD错误状态寄存器2

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x05C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	CRCBSYTO	CRCTO	RDTO	BSYTO1	BSYTO0	RSPTO1	RSPTO0
重置后的值：	0	0	0	0	0	0	0	0	0	0*1	0*1	0*1	0*1	0*1	0*1	0*1

Bit	Symbol	Function	R/W
0	RSPTO0	响应超时标志0 0：发出命令*2后，在不到640个SDMMC时钟周期内收到响应 1：发出命令*2后，在SDMMC时钟的640或更多周期内未收到响应	R
1	RSPTO1	响应超时标志1 0：发出命令*3后，在不到640个SDMMC时钟周期内收到响应 1：发出命令*3后，在SDMMC时钟的640或更多周期后未收到响应（使用SD_CMD.CMDIDX[5:0]设置，在RSPTO0标志中指示CMD12问题发生的错误）	R

Bit	Symbol	Function	R/W
2	BSYTO0	Busy Timeout Flag 0 0: After R1b response was received, SD/MMC was released from the busy state during the specified period*4 1: After R1b response was received, SD/MMC was in the busy state after the specified period*4 elapsed	R
3	BSYTO1	Busy Timeout Flag 1 0: After CMD12 was automatically issued, SD/MMC was released from the busy state during the specified period*4 1: After CMD12 was automatically issued, SD/MMC was in the busy state after the specified period*4 elapsed (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the BSYTO0 flag)	R
4	RDTO	Read Data Timeout Flag When a read command is issued, this flag sets to 1 when read data is not received after the specified period*4 elapses. When read data is received, this flag sets to 1 when the next block of read data is not received after the specified period*4 elapses. When the SD/MMC exits the read wait state, this flag sets to 1 when the next block of read data is not received after the specified period*4 elapses.	R
5	CRCTO	CRC Status Token Timeout Flag 0: After CRC data was written to the SD card/MMC, a CRC status token was received during the specified period*4 1: After CRC data was written to the SD card/MMC, a CRC status token was not received after the specified period*4 elapsed	R
6	CRCBSYTO	CRC Status Token Busy Timeout Flag 0: After a CRC status token was received, the SD/MMC was released from the busy state during the specified period*4 1: After a CRC status token was received, the SD/MMC was in the busy state after the specified period*4 elapsed	R
31:7	—	These bits are read as 0.	R

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 3. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 4. Set the SD_OPTION.TOP[3:0] bits to select the number of *n* cycles.

The SD_ERR_STS2 register indicates the timeout status.

39.2.19 SD_BUF0 : SD Buffer Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

When writing to the SD card, the write data is written to this register. When reading from the SD card, the read data is read from this register. This register is internally connected to two 512-byte buffers.

If both buffers are not empty when executing multiple block read, the SD card/MMC clock is stopped to suspend receiving data. When one of the buffers is empty, the SD card/MMC clock is supplied to resume receiving data.

Bit	Symbol	Function	R/W
2	BSYTO0	忙超时标志0 0：收到R1b响应后，SDMMC在指定时间段内从忙状态中释放*4 1：收到R1b响应后，经过指定时间*4后SDMMC处于忙碌状态	R
3	BSYTO1	忙超时标志1 0：CMD12自动下发后，SDMMC在指定时间段内从忙状态释放*4 1：自动发出CMD12后，经过指定时间*4后SDMMC处于忙碌状态（使用SD_CMD.CMDIDX[5:0]设置，在BSYTO0标志中指示CMD12发出的错误）	R
4	RDTO	读取数据超时标志 发出读取命令时，如果经过指定时间*4后仍未接收到读取数据，则此标志设置为1。当接收到读取数据时，如果经过指定的时间*4后没有接收到下一个读取数据块，则此标志设置为1。当SDMMC退出读取等待状态时，如果经过指定时间*4后未接收到下一个读取数据块，此标志设置为1。	R
5	CRCTO	CRC状态令牌超时标志 0：CRC数据写入SD卡MMC后，在指定时间段内收到CRC状态令牌*4 1：将CRC数据写入SD卡MMC后，经过指定时间*4后未收到CRC状态令牌	R
6	CRCBSYTO	CRC状态令牌忙超时标志 0：收到CRC状态令牌后，SDMMC在指定时间段内从忙碌状态中释放*4 1：收到CRC状态令牌后，经过指定时间*4后SDMMC处于忙碌状态	R
31:7	—	这些位读为0。	R

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.通过SD_CMD中的设置，CMD12之外的CMD
SD_STOP中的STP位设置为1，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
注3.通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12
SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
注4.设置SD_OPTION.TOP[3:0]位以选择n个周期数。

SD_ERR_STS2寄存器指示超时状态。

39.2.19 SD_BUF0:SD缓冲寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x060

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

写入SD卡时，写入数据写入该寄存器。从SD卡读取时，从该寄存器读取读取的数据。该寄存器在内部连接到两个512字节的缓冲区。

如果执行多块读取时两个缓冲区都不为空，则停止SD卡MMC时钟以暂停接收数据。当其中一个缓冲区为空时，提供SD卡MMC时钟以恢复接收数据。

39.2.20 SDIO_MODE : SDIO Mode Control Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x068

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	C52PUB	IOABT	—	—	—	—	—	RWREQ	—	INTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	INTEN	SDIO Interrupt Acceptance Enable*1 0: Disable SDIO interrupt acceptance 1: Enable SDIO interrupt acceptance	R/W
1	—	This bit is read as 0. The write value should be 0.	R/W
2	RWREQ	Read Wait Request 0: Allow SD/MMC to exit read wait state 1: Request for SD/MMC to enter read wait state	R/W
7:3	—	These bits are read as 0. The write value should be 0.	R/W
8	IOABT	SDIO Abort If this bit is set to 1 during multiblock transfer triggered by CMD53, CMD52 is immediately issued, and the command sequence is aborted.	R/W
9	C52PUB	SDIO None Abort If this bit is set to 1 during multiblock transfer triggered by CMD53, CMD52 is issued after the transfer process is complete, and the command sequence is completed.	R/W
31:10	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY flag is 1.

The SDIO_MODE register controls reception of the SDIO interrupt, CMD52 issuance during multiblock transfer, and read wait request. Do not set bits C52PUB and IOABT to 1 at the same time.

RWREQ bit (Read Wait Request)

When RWREQ is set to 1 in the CMD53 (multiple block) read sequence, the block transfer enters the read wait state between blocks.

[Read wait state releasing]

- The read wait state is released, when RWREQ is cleared to 0 in the read wait state.
- When IOABT is set to 1 in the read wait state, RWREQ is automatically cleared to 0 after CMD52 is issued, and then the read wait state is released.
- When C52PUB and RWREQ are set to 1 simultaneously in the CMD53 (multiple block) read sequence, the read wait state is not automatically released. Therefore, after the CMD52 response is received, clear RWREQ. You must set RWREQ and C52PUB simultaneously.

When RWREQ is set to 1 while the last block in the CMD53 (multiple block) read sequence is transferred, the read wait state is not entered and RWREQ is automatically cleared to 0 by setting access end. Set RWREQ to 1 after the response end flag sets.

IOABT bit (SDIO Abort)

When the IOABT bit is set to 1 in a CMD53 (multiple block) sequence, the CMD53 sequence is halted and CMD52 is issued. However, if a command sequence is halted because of a communication error or timeout, CMD52 is not issued.

39.2.20 SDIO_MODE:SDIO模式控制寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x068

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	C52PUB	IOABT	—	—	—	—	—	RWREQ	—	INTEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	INTEN	SDIO中断接受使能*1 0：禁止SDIO中断接受1：使能SDIO中断接受	R/W
1	—	该位读取为0。写入值应为0。	R/W
2	RWREQ	读取等待请求 0：允许SDMMC退出读取等待状态1：请求SDMMC进入读取等待状态	R/W
7:3	—	这些位被读取为0。写入值应为0。	R/W
8	IOABT	SDIO Abort 如果在CMD53触发的多块传输期间该位设置为1，则立即发出CMD52，并中止命令序列。	R/W
9	C52PUB	SDIO无中止 如果在CMD53触发的多块传输期间该位设置为1，则在传输过程完成后发出CMD52，命令序列完成。	R/W
31:10	—	这些位被读取为0。写入值应为0。	R/W

注1.当SD_INFO2.CBSY标志为1时，请勿重写该位。

SDIO_MODE寄存器控制SDIO中断的接收、多块传输期间CMD52的发布和读取等待请求。不要同时将位C52PUB和IOABT设置为1。

RWREQ位（读取等待请求）

当CMD53（多块）读取序列中RWREQ设置为1时，块传输进入块之间的读取等待状态。

[读取等待状态释放]

●在读等待状态下，当RWREQ被清0时，读等待状态被释放。

●读等待状态下IOABT置1时，发出CMD52后RWREQ自动清0，然后解除读等待状态。

●当C52PUB和RWREQ在CMD53（多块）读序列中同时置1时，读等待状态不会自动解除。因此，在收到CMD52响应后，清除RWREQ。您必须同时设置RWREQ和C52PUB。

当RWREQ设置为1时CMD53（多块）读取序列中的最后一个块被传输时，不会进入读取等待状态，并且通过设置访问结束将RWREQ自动清除为0。设置响应结束标志后将RWREQ设置为1。

IOABT bit (SDIO Abort)

当CMD53（多块）序列中的IOABT位设置为1时，CMD53序列停止并发出CMD52。但是，如果命令序列由于通信错误或超时而停止，则不会发出CMD52。

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Although continued buffer access is possible even after IOABT is set to 1, the buffer access error bit (ILR or ILW) in SD_INFO2 is set accordingly. Set SD_ARG before setting IOABT to 1.

When IOABT is set to 1 during transfer for a single block write, the access end flag sets when SD_BUF0 becomes empty, and CMD52 is not issued. If SD_BUF0 contains data, the access end flag sets on completion of reception of the busy state without CMD52 being issued.

When IOABT is set to 1 during transfer for single block read, the access end flag sets immediately after IOABT is set, and CMD52 is not issued.

When IOABT is set to 1 during reception of the busy state after an R1b response, the access end flag sets on completion of reception of the busy state without CMD52 being issued.

When IOABT is set to 1 after a command sequence is completed, CMD52 is not issued and the access end flag does not set.

Set IOABT to 1 after the response end flag sets.

Set IOABT to 0 after the access end flag sets.

C52PUB bit (SDIO None Abort)

When the C52PUB bit is set to 1 in the CMD53 (multiple block) write sequence, CMD52 is automatically issued between blocks if SD_BUF0 becomes empty. C52PUB is automatically cleared to 0 after reception of the response to CMD52 is completed. Additionally, if C52PUB is set to 1 while the last block is being transferred, CMD52 is not issued. In this case, C52PUB is automatically cleared to 0 after the access end flag sets to 1.

When C52PUB and RWREQ are set to 1 in the CMD53 (multiple block) read sequence, the block transfer enters the read wait state between blocks and CMD52 is automatically issued. C52PUB is automatically cleared to 0 after reception of the response to CMD52 is completed. Additionally, if C52PUB is set to 1 while the last block is being transferred, CMD52 is not issued. In this case, C52PUB is automatically cleared to 0 after the access end flag sets to 1.

If C52PUB is set to 1 in the CMD53 (multiple block) read sequence, you must set RWREQ to 1 in addition to C52PUB.

Set SD_ARG before setting C52PUB to 1.

Set C52PUB to 1 after the response end flag sets.

39.2.21 SDIO_INFO1 : SDIO Interrupt Flag Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x06C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EXWT	EXPUB52	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQ
Value after reset:	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	x	x	0*1

Bit	Symbol	Function	R/W
0	IOIRQ	SDIO Interrupt Status Flag 0: No SDIO interrupt detected 1: SDIO interrupt detected	R/(W)*2
2:1	—	The read values are undefined. The write value should be 1.	R/W
13:3	—	These bits are read as 0. The write value should be 0.	R/W
14	EXPUB52	EXPUB52 Status Flag Indicates the status of the EXPUB52.	R/(W)*2
15	EXWT	EXWT Status Flag Indicates the status of the EXWT.	R/(W)*2
31:16	—	These bits are read as 0. The write value should be 0.	R/W

尽管即使在IOABT设置为1后仍可以继续访问缓冲区，但缓冲区访问错误位（ILR或ILW）在SD_INFO2相应设置。在将IOABT设置为1之前设置SD_ARG。

当IOABT在单块写入传输期间设置为1时，SD_BUF0变为空时设置访问结束标志，并且不发出CMD52。如果SD_BUF0包含数据，则在未发出CMD52的忙状态接收完成时设置访问结束标志。

当IOABT在单块读取传输期间设置为1时，在设置IOABT后立即设置访问结束标志，并且未发出CMD52。

如果在R1b响应后接收忙碌状态期间将IOABT设置为1，则在没有发出CMD52的情况下完成忙碌状态接收时设置访问结束标志。

当命令序列完成后IOABT设置为1时，不发出CMD52并且不设置访问结束标志。

设置响应结束标志后将IOABT设置为1。

设置访问结束标志后将IOABT设置为0。

C52PUB位（SDIO无中止）

在CMD53（多块）写入序列中将C52PUB位设置为1时，如果SD_BUF0为空，则在块之间自动发出CMD52。C52PUB在接收到对CMD52的响应完成后自动清零。此外，如果在传输最后一个块时将C52PUB设置为1，则不会发出CMD52。在这种情况下，访问结束标志设置为1后，C52PUB自动清零。

当CMD53（多块）读序列中C52PUB和RWREQ置1时，块传输进入块间读等待状态，自动发出CMD52。C52PUB在接收到对CMD52的响应完成后自动清零。此外，如果在传输最后一个块时将C52PUB设置为1，则不会发出CMD52。在这种情况下，访问结束标志设置为1后，C52PUB自动清零。

如果在CMD53（多块）读取序列中将C52PUB设置为1，则除了C52PUB之外，还必须将RWREQ设置为1。

在将C52PUB设置为1之前设置SD_ARG。

在响应结束标志设置后将C52PUB设置为1。

39.2.21 SDIO_INFO1:SDIO中断标志 寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x06C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EXWT	EXPUB52	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQ
重置后的值:	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	x	x	0*1

Bit	Symbol	Function	R/W
0	IOIRQ	SDIO中断状态标志 0：未检测到SDIO中断1：检测到SDIO中断	R/(W)*2
2:1	—	读取的值未定义。写入值应为1。	R/W
13:3	—	这些位被读取为0。写入值应为0。	R/W
14	EXPUB52	EXPUB52状态标志 指示EXPUB52的状态。	R/(W)*2
15	EXWT	EXWT状态标志 指示EXWT的状态。	R/(W)*2
31:16	—	这些位被读取为0。写入值应为0。	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. Only 0 can be written to clear the bit.

The SDIO_INFO1 register indicates the status of the SDIO card access. Set flags to be cleared to 0. Set flags that are not being cleared to 1.

IOIRQ flag (SDIO Interrupt Status Flag)

The IOIRQ flag indicates that an SDIO interrupt occurred.

[Setting condition]

- When SDIO interrupt from an SDIO card is received while INTEN in SDIO_MODE is set to 1.

[Clearing condition]

- When 0 is written to IOIRQ.*1

Note 1. Before clearing this bit, access the SDIO card to negate the SDIO interrupt signal from the SDIO card. If the interrupt signal is not negated, this bit can be set again.

EXPUB52 flag (EXPUB52 Status Flag)

The EXPUB52 flag indicates the EXPUB52 status.

[Setting conditions]

- While the last block in the CMD53 (multiple block) sequence is transferred, C52PUB in SDIO_MODE is set to 1.
- While C52PUB is set to 1 in the CMD53 (multiple block) write sequence, the last block is transferred.

[Clearing condition]

- When 0 is written to EXPUB52.

EXWT flag (EXWT Status Flag)

The EXWT flag indicates the EXWT status.

[Setting condition]

- While the last block in the CMD53 (multiple block) read sequence is transferred, RWREQ in SDIO_MODE is set to 1.

[Clearing condition]

- When 0 is written to EXWT.

39.2.22 SDIO_INFO1_MASK : SDIO INFO1 Interrupt Mask Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x070

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EXWTM	EXPUB52M	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQM
Value after reset:	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
0	IOIRQM	IOIRQ Interrupt Mask Control 0: Do not mask IOIRQ interrupts 1: Mask IOIRQ interrupts	R/W
2:1	—	These bits are read as 1.The write value should be 1.	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。
注2.只能写入0来清除该位。

SDIO_INFO1寄存器指示SDIO卡访问的状态。将要清除的标志设置为0。将未清除的标志设置为1。

IOIRQ标志（SDIO中断状态标志）

IOIRQ标志表示发生了SDIO中断。

[Setting condition]

●当SDIO_MODE中的INTEN设置为1时，接收到来自SDIO卡的SDIO中断。

[Clearing condition]

●0写入IOIRQ时。*1

注1.在清除该位之前，访问SDIO卡以否定来自SDIO卡的SDIO中断信号。如果中断信号没有被否定，这个位可以被重新设置。

EXPUB52标志（EXPUB52状态标志）

EXPUB52标志指示EXPUB52状态。

[Setting conditions]

●当CMD53（多块）序列中的最后一个块被传输时，SDIO_MODE中的C52PUB设置为1。
●在CMD53（多块）写入序列中，当C52PUB设置为1时，传输最后一个块。

[Clearing condition]

●当0写入EXPUB52时。

EXWT标志（EXWT状态标志）

EXWT标志指示EXWT状态。

[Setting condition]

●当CMD53（多块）读取序列中的最后一个块被传输时，SDIO_MODE中的RWREQ设置为1。

[Clearing condition]

●当0写入EXWT时。

39.2.22 SDIO_INFO1_MASK:SDIOINFO1中断屏蔽寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n
Offset address: 0x070

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	EXWTM	EXPUB52M	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQM
重置后的值:	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
0	IOIRQM	IOIRQ中断屏蔽控制 0：不屏蔽IOIRQ中断1：屏蔽IOIRQ中断	R/W
2:1	—	这些位被读取为1。写入值应为1。	R/W

Bit	Symbol	Function	R/W
13:3	—	These bits are read as 0. The write value should be 0.	R/W
14	EXPUB52M	EXPUB52 Interrupt Request Mask Control 0: Do not mask EXPUB52 interrupt requests 1: Mask EXPUB52 interrupt requests	R/W
15	EXWTM	EXWT Interrupt Request Mask Control 0: Do not mask EXWT interrupt requests 1: Mask EXWT interrupt requests	R/W
31:16	—	These bits are read as 0. The write value should be 0.	R/W

The SDIO_INFO1_MASK register enables or disables interrupt requests from the status flags in the SDIO_INFO1 register. See Table 39.5 for details on the relationship between the status flags and the requested interrupt source.

39.2.23 SD_DMAEN : DMA Mode Enable Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMAEN	—
Value after reset:	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	DMAEN	DMA Transfer Enable*1 *2 0: Disable use of DMA transfer to access SD_BUF0 register 1: Enable use of DMA transfer to access SD_BUF0 register	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
4	—	This bit is read as 1. The write value should be 1.	R/W
11:5	—	These bits are read as 0. The write value should be 0.	R/W
12	—	This bit is read as 1. The write value should be 1.	R/W
31:13	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY bit is 1.
Note 2. When the SD_INFO2_MASK.BWEM bit is 0 or the SD_INFO2_MASK.BREM bit is 0, set the SD_DMAEN.DMAEN bit to 0. When the SD_DMAEN.DMAEN bit is 1, set the SD_INFO2_MASK.BWEM bit to 1 and the SD_INFO2_MASK.BREM bit to 1.

The SD_DMAEN register enables or disables DMA transfers.

DMAEN bit (DMA Transfer Enable)

When using DMA transfer to access the SD buffer, set the DMAEN bit to 1 before setting the SD_CMD register.

Bit	Symbol	Function	R/W
13:3	—	这些位被读取为0。写入值应为0。	R/W
14	EXPUB52M	EXPUB52中断请求屏蔽控制 0：不屏蔽EXPUB52中断请求1：屏蔽EXPUB52中断请求	R/W
15	EXWTM	EXWT中断请求屏蔽控制 0：不屏蔽EXWT中断请求1：屏蔽EXWT中断请求	R/W
31:16	—	这些位被读取为0。写入值应为0。	R/W

SDIO_INFO1_MASK寄存器启用或禁用来自SDIO_INFO1寄存器中状态标志的中断请求。
有关状态标志和请求的中断源之间关系的详细信息，请参见表39.5。

39.2.23 SD_DMAEN:DMA模式使能寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1B0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMAEN	—
重置后的值：	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	DMAEN	DMA传输启用*1*2 0：禁止使用DMA传输访问SD_BUF0寄存器1：启用使用DMA传输访问SD_BUF0寄存器	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
4	—	该位读取为1。写入值应为1。	R/W
11:5	—	这些位被读取为0。写入值应为0。	R/W
12	—	该位读取为1。写入值应为1。	R/W
31:13	—	这些位被读取为0。写入值应为0。	R/W

注1.当SD_INFO2.CBSY位为1时，请勿重写该位。
注2.当SD_INFO2_MASK.BWEM位为0或SD_INFO2_MASK.BREM位为0时，将SD_DMAEN.DMAEN位设置为0。当SD_DMAEN.DMAEN位为1时，将SD_INFO2_MASK.BWEM位设置为1和SD_INFO2_MASK。BREM位为1。

SD_DMAEN寄存器启用或禁用DMA传输。

DMAEN位（DMA传输使能）

使用DMA传输访问SD缓冲区时，在设置SD_CMD寄存器之前将DMAEN位设置为1。

39.2.24 SOFT_RST : Software Reset Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SDRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
0	SDRST	Software Reset Control 0: Reset SD/MMC Host Interface software 1: Cancel reset of SD/MMC Host Interface software	R/W
2:1	—	These bits are read as 1. The write value should be 1.	R/W
31:3	—	These bits are read as 0. The write value should be 0.	R/W

Table 39.4 lists the bits and flags initialized by SD/MMC Host Interface software reset.

Table 39.4 Bits and flags initialized by SD/MMC Host Interface software reset

Register	Bit/flag
SD_STOP	SEC, STP
SD_INFO1	RSPEND, ACEND
SD_INFO2	CMDE, CRCE, ENDE, DTO, ILW, ILR, RSPTO, BRE, BWE, SD_CLK_CTRLEN, CBSY, ILA
SD_CLK_CTRL	CLKEN
SD_OPTION	CTOP[3:0], TOP[3:0], TOUTMASK, WIDTH8, WIDTH
SD_ERR_STS1	CMDE0, CMDE1, RSPLENE0, RSPLENE1, RDLENE, CRCLENE, RSPCRCE0, RSPCRCE1, RDCRCE, CRCTKE, CRCTK[2:0]
SD_ERR_STS2	RSPTO0, RSPTO1, BSYTO0, BSYTO1, RDTO, CRCTO, CRCBSYTO
SDIO_INFO1	IOIRQ, EXPUB52, EXWT
SDIF_MODE	NOCHKCR

39.2.25 SDIF_MODE : SD Interface Mode Setting Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NOCHKCR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0*1	0	0	0	0	0	0	0	0

39.2.24 SOFT_RST：软件复位寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1C0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SDRST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Function	R/W
0	SDRST	软件复位控制 0：复位SDMMC主机接口软件1：取消复位SDMMC主机接口软件	R/W
2:1	—	这些位被读取为1。写入值应为1。	R/W
31:3	—	这些位被读取为0。写入值应为0。	R/W

表39.4列出了SDMMC主机接口软件复位初始化的位和标志。

Table 39.4 由SDMMC主机接口软件复位初始化的位和标志

Register	Bit/flag
SD_STOP	SEC, STP
SD_INFO1	RSPEND, ACEND
SD_INFO2	CMDE、CRCE、ENDE、DTO、ILW、ILR、RSPTO、BRE、BWE、SD_CLK_CTRLEN、CBSY、ILA
SD_CLK_CTRL	CLKEN
SD_OPTION	CTOP[3:0], TOP[3:0], TOUTMASK, WIDTH8, WIDTH
SD_ERR_STS1	CMDE0, CMDE1, RSPLENE0, RSPLENE1, RDLENE, CRCLENE, RSPCRCE0, RSPCRCE1, RDCRCE, CRCTKE, CRCTK[2:0]
SD_ERR_STS2	RSPTO0, RSPTO1, BSYTO0, BSYTO1, RDTO, CRCTO, CRCBSYTO
SDIO_INFO1	IOIRQ, EXPUB52, EXWT
SDIF_MODE	NOCHKCR

39.2.25 SDIF_MODE:SD接口模式设置寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1CC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	NOCHKCR	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0*1	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
8	NOCHKCR	CRC Check Mask CRC check mask bit for MMC test commands. Set when CRC16 or CRC status value check is not executed. 0: Enable CRC check 1: Disable CRC Check (ignore CRC16 valued when reading and ignore CRC status value when writing)	R/W
31:9	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.

NOCHKCR bit (CRC Check Mask)

The NOCHKCR bit is used for MMC test commands. This bit is set when CRC16 or CRC status value check is not executed.

39.2.26 EXT_SWAP : Swap Control Register

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	BRSWP	BWSWP	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	BWSWP	SD_BUF0 Swap Write*1 0: Normal write operation 1: Swap the byte endian order before writing to SD_BUF0 register	R/W
7	BRSWP	SD_BUF0 Swap Read*1 0: Normal read operation 1: Swap the byte endian order before reading SD_BUF0 register	R/W
31:8	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY flag is 1.

The EXT_SWAP register selects whether or not the byte endian order is swapped when accessing the SD_BUF0 register. See section 39.3.1. SD/MMC Interface for details on the differences in accessing the SD_BUF0 register based on the EXT_SWAP register value.

39.3 Operation

39.3.1 SD/MMC Interface

When data is read from the SD card/MMC, the process is as follows:

1. The SD/MMC Host Interface receives data from the SD card/MMC through the SDnDAT signal (see Figure 39.2 and Figure 39.3).
2. The received data is stored in SD_BUF of the MMC Host Interface (see Figure 39.4).
3. The data stored in SD_BUF is read from SD_BUF0 (see Figure 39.5).

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
8	NOCHKCR	CRC校验掩码 MMC测试命令的CRC校验掩码位。不执行CRC16或CRC状态值检查时置位。 0：启用CRC校验1：禁用CRC校验（读取时忽略CRC16值，写入时忽略CRC状态值）	R/W
31:9	—	这些位被读取为0。写入值应为0。	R/W

注1.该值由复位初始化，并且在由SOFT_RST.SDRST标志触发的复位时初始化。

NOCHKCR位（CRC校验掩码）

NOCHKCR位用于MMC测试命令。当不执行CRC16或CRC状态值检查时，该位置位。

39.2.26 EXT_SWAP:交换控制寄存器

Base address: SDHIn 0 = 0x4009_2000 + 0x0400 × n

Offset address: 0x1E0

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	BRSWP	BWSWP	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	BWSWP	SD_BUF0交换写入*1 0：正常写操作1：在写入SD_BUF0寄存器之前交换字节顺序	R/W
7	BRSWP	SD_BUF0交换读取*1 0：正常读取操作1：在读取SD_BUF0寄存器之前交换字节顺序	R/W
31:8	—	这些位被读取为0。写入值应为0。	R/W

注1.当SD_INFO2.CBSY标志为1时，请勿重写该位。

EXT_SWAP寄存器选择在访问SD_BUF0寄存器时是否交换字节顺序。
请参见第39.3.1节。SDMMC接口了解访问SD_BUF0寄存器的差异的详细信息，基于EXT_SWAP寄存器值。

39.3 Operation

39.3.1 SD/MMC Interface

从SD卡MMC读取数据时，流程如下：

1.SDMMC主机接口通过SDnDAT信号从SD卡MMC接收数据（参见图39.2和Figure 39.3）。

2.接收到的数据存储在MMC主机接口的SD_BUF中（见图39.4）。

3.SD_BUF中存储的数据从SD_BUF0中读取（见图39.5）。

When data is written to the SD card/MMC, the specified procedure is reversed.

When accessing SD_BUF0, pay attention to the transfer order in SDnDAT and the store order in SD_BUF. If required, you can change the byte endian of the data read from or written to SD_BUF0 using the SDSWAP register. See Figure 39.6.

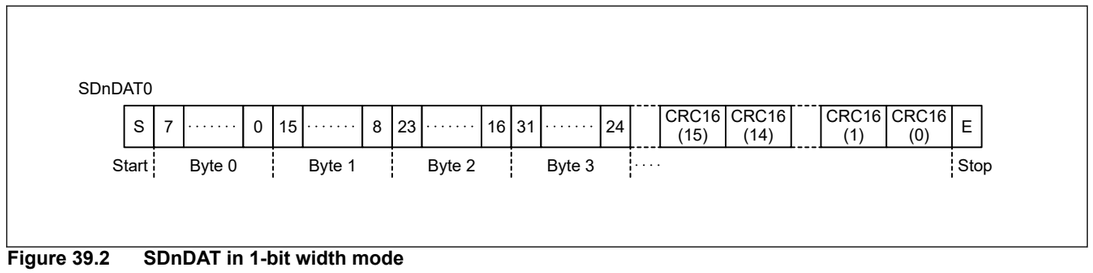

Figure 39.2 SDnDAT in 1-bit width mode

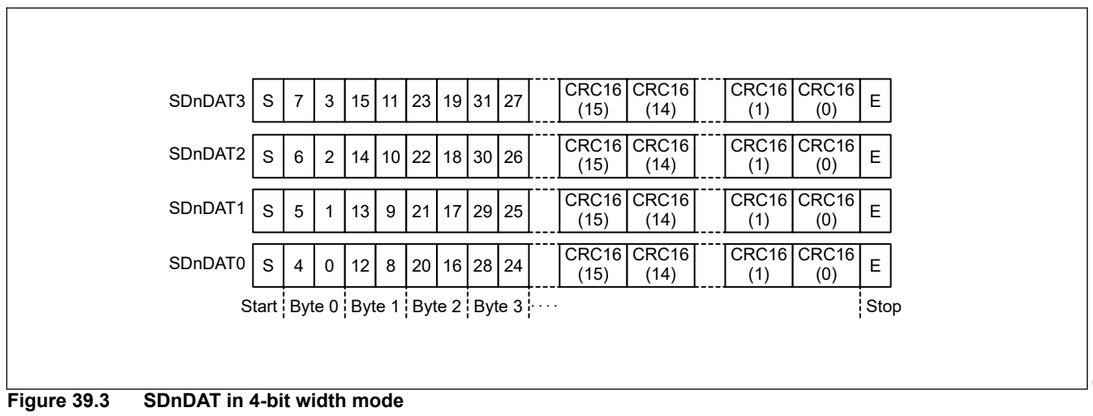

Figure 39.3 SDnDAT in 4-bit width mode

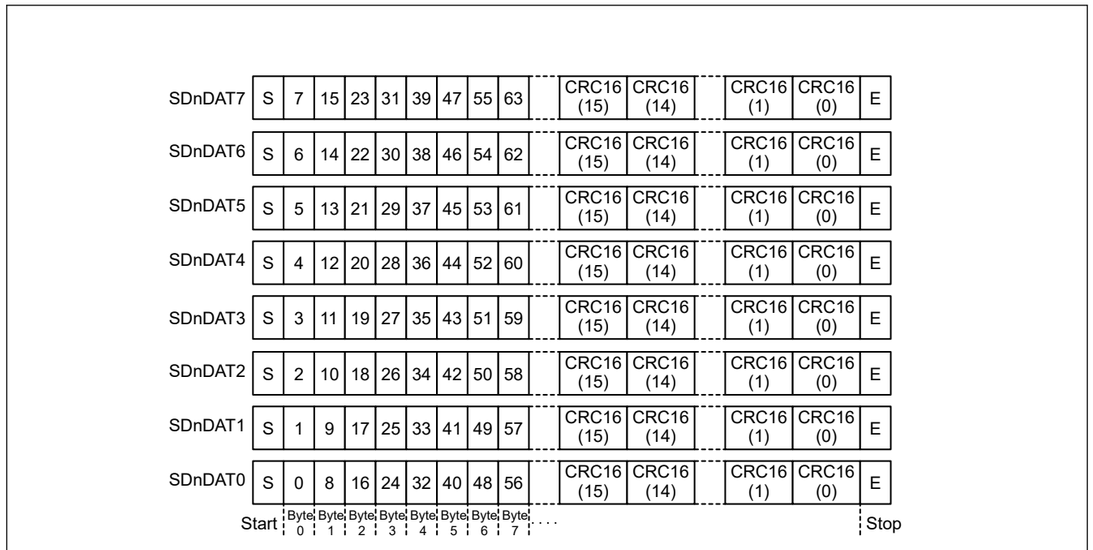

Figure 39.4 SDnDAT in 8-bit width mode

当数据写入SD卡MMC时，指定的过程相反。

访问SD_BUF0时，注意SDnDAT中的传输顺序和SD_BUF中的存储顺序。如果需要，您可以使用SDSWAP寄存器更改从SD_BUF0读取或写入数据的字节字节序。请参见图39.6。

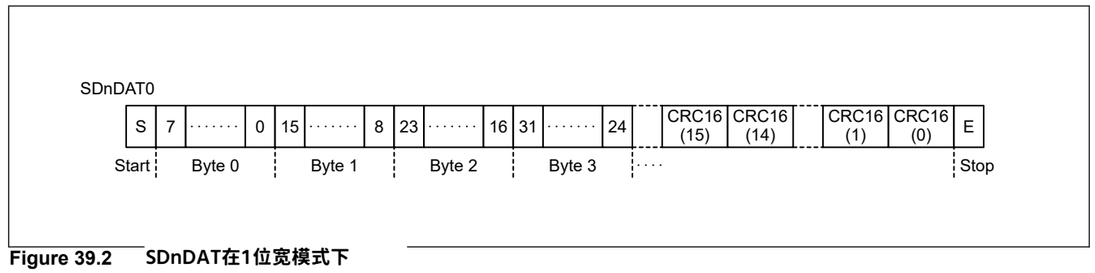

Figure 39.2 SDnDAT在1位宽模式下

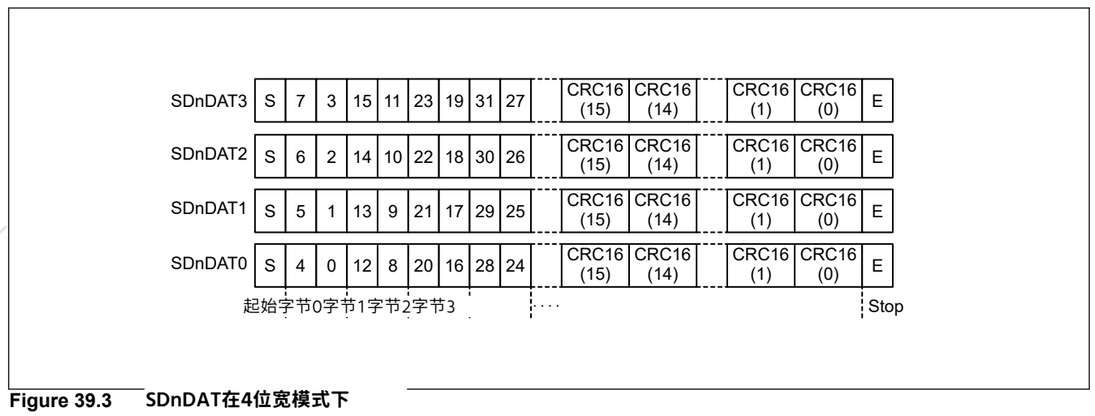

Figure 39.3 SDnDAT在4位宽模式下

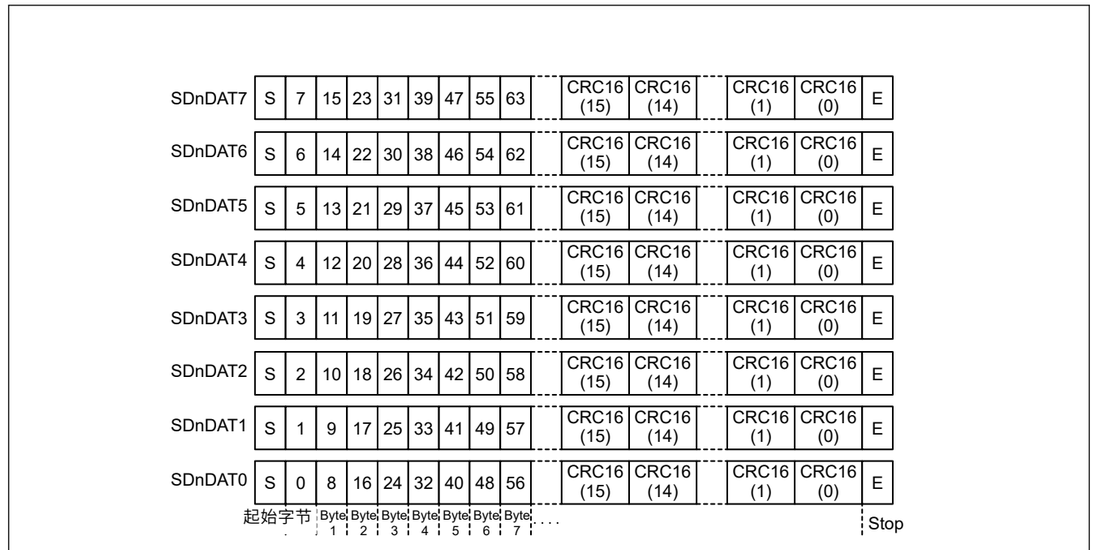

Figure 39.4 SDnDAT在8位宽度模式下

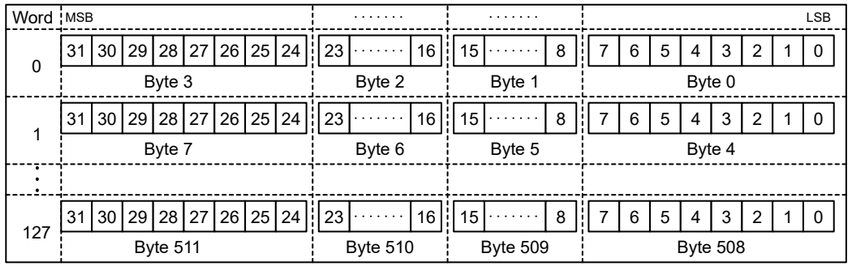

Figure 39.5 SD_BUF store data

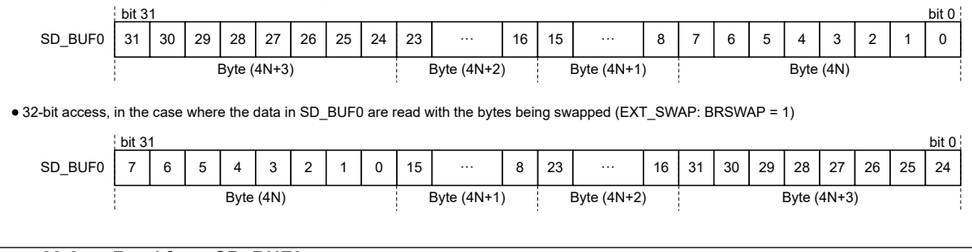

Figure 39.6 Read from SD_BUF0

39.3.2 Card Detect/Write Protect

39.3.2.1 Card detect

The SD/MMC Host Interface has two types of card detect functions.

(1) Card detect with SDnCD (n = 0)

Figure 39.7 shows the timing for card detect using SDnCD. SDnCD is connected to the card socket and pulled up on the host device. The resistance of the pull-up resistor is determined by the specification of the SD/MMC host device.

(2) Card insertion

SDnCD is pulled down when a card is inserted. At this point, if SDnCD is pulled down for the Mcycle period (set in SD_OPTION), SDCDIN in SD_INFO1 is set to 1. It is cleared by writing 0.

(3) Card removal

SDnCD is pulled up when a card is removed. At this point, if SDnCD is pulled up for the Mcycle period (set in SD_OPTION), SDCDRM in SD_INFO1 is set to 1. It is cleared by writing 0.

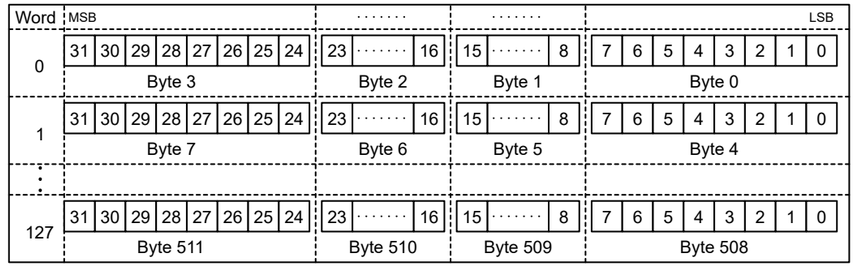

Figure 39.5 SD_BUF存储数据

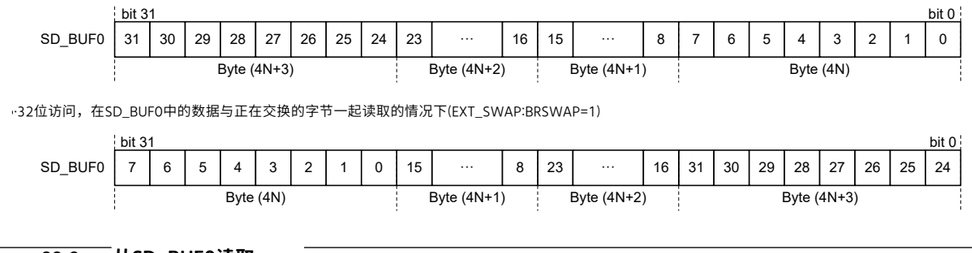

Figure 39.6 从SD_BUF0读取

39.3.2 卡检测写保护

39.3.2.1 卡检测

SDMMC主机接口有两种类型的卡检测功能。

(1) SDnCD卡检测(n=0)

图39.7显示了使用SDnCD进行卡检测的时序。SDnCD连接到卡插槽并在主机设备上拉高。上拉电阻的阻值由SDMMC主机设备的规格决定。

(2) 插卡

SDnCD在插入卡时被拉下。此时，如果SDnCD被下拉Mcycle周期（设置在SD_OPTION)，SD_INFO1中的SDCDIN设置为1。写入0清除。

(3) 取卡

取出卡时，SDnCD被拉起。此时，如果SDnCD被拉高了Mcycle周期（设置在SD_OPTION)，SD_INFO1中的SDCDRM设置为1，写入0清零。

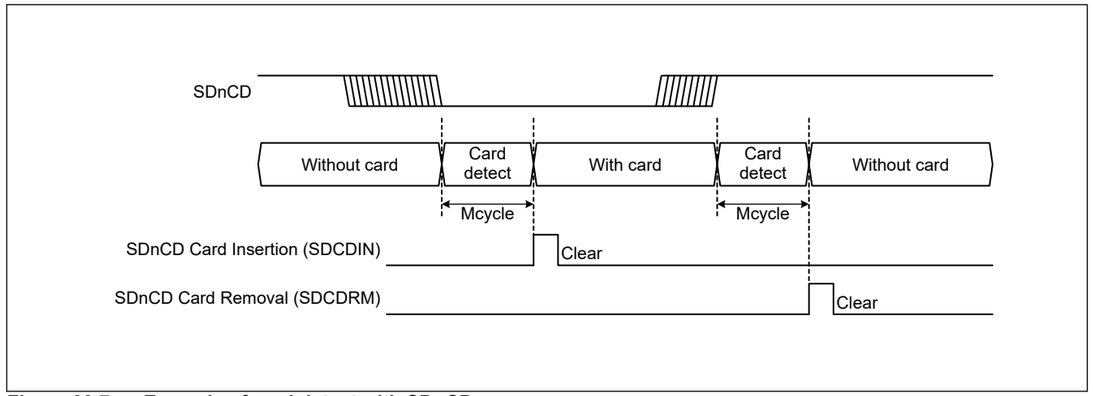

Figure 39.7 Example of card detect with SDnCD

(4) SD card detect with SDnDAT3 (n = 0)

Figure 39.8 shows the timing when the SD card is detected with SDnDAT3. In addition, SDnDAT3 is pulled down by the host device, and the resistance value for pulling down is determined by the specification of the SD host device.

(5) Card insertion

When an SD card is inserted, SDnDAT3 is pulled up and SDD3IN in SD_INFO1 is set to 1. It is cleared by writing 0.

(6) Card removal

When an SD card is removed, SDnDAT3 is pulled down and SDD3RM in SD_INFO1 is set to 1. It is cleared by writing0.

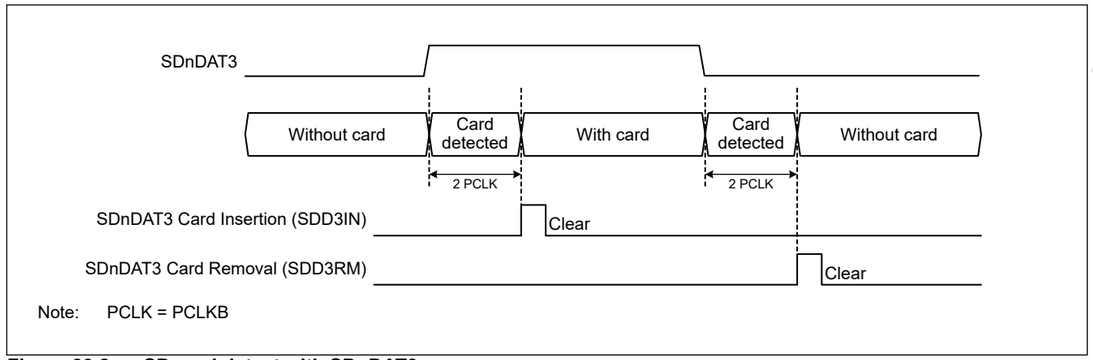

Figure 39.8 SD card detect with SDnDAT3

39.3.2.2 Write protect

The SD/MMC Host Interface has two types of write protect functions.

(1) Write protect with SDnWP (n = 0)

SDnWP is connected to the card socket and pulled up or pulled down by the card insertion. The selection of pulling up or pulling down and the resistance value is determined by the specification of the SD host device. When the SDnWP state is reflected to SDWPMON in SD_INFO1, the write protect state is set after the SD card is inserted.

(2) Write protect with command

The internal write protection of the card and the lock/unlock operation of the card are realized by the command.

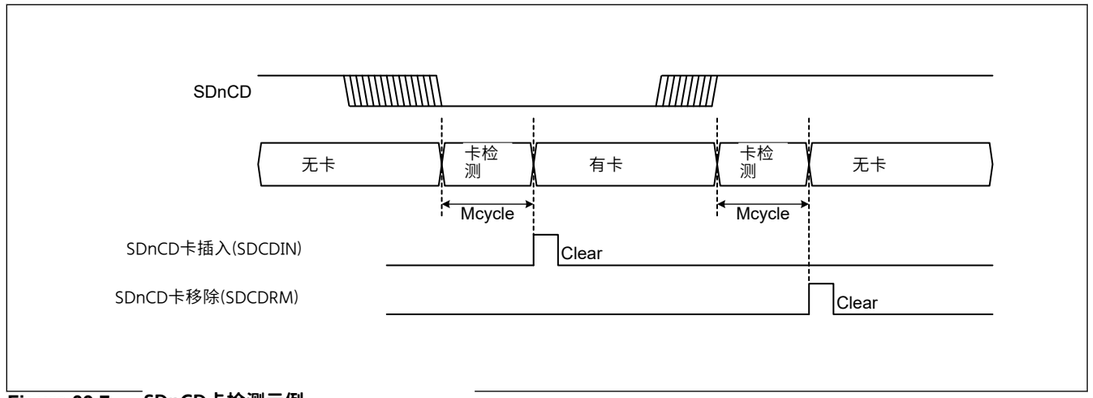

Figure 39.7 SDnCD卡检测示例

(4) 使用SDnDAT3(n=0)检测SD卡

图39.8显示了使用SDnDAT3检测到SD卡的时序。此外，SDnDAT3由主机设备下拉，下拉电阻值由SD主机设备的规格决定。

(5) 插卡

插入SD卡时，SDnDAT3上拉，SD_INFO1中的SDD3IN置1，写0清零。

(6) 取卡

取出SD卡时，SDnDAT3被拉低，SD_INFO1中的SDD3RM置1。写0清零。

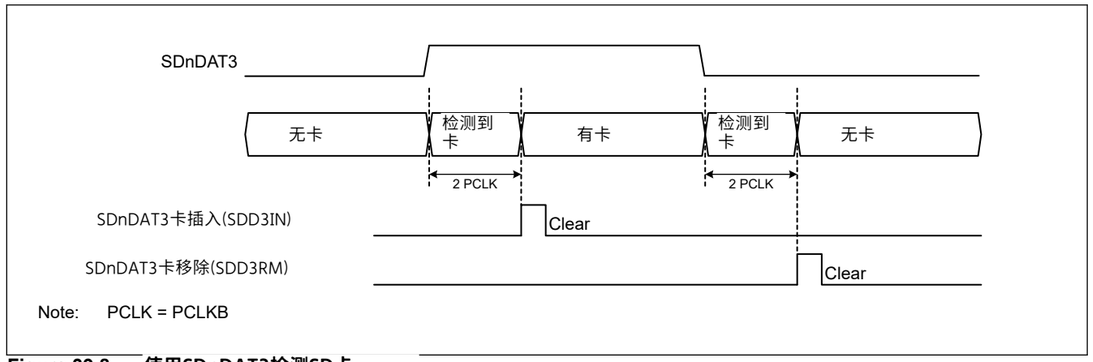

Figure 39.8 使用SDnDAT3检测SD卡

39.3.2.2 写保护

SDMMC主机接口有两种类型的写保护功能。

(1) 使用SDnWP进行写保护(n=0)

SDnWP与卡座相连，通过插卡进行上拉或下拉。上拉或下拉的选择和阻值由SD主机设备的规格决定。当SDnWP状态反映到SD_INFO1中的SDWPMON时，插入SD卡后设置写保护状态。

(2) 用命令写保护

卡的内部写保护和卡的开锁操作都是通过命令实现的。

39.3.3 Interrupt Request and DMA Transfer Request

39.3.3.1 Interrupts

Table 39.5 lists the SDHI interrupt sources. The SDHI requests an interrupt when:

- The status flags in registers SD_INFO1, SD_INFO2, and SDIO_INFO1 set to 1.
- The associated bits in the SD_INFO1_MASK, SD_INFO2_MASK, and SDIO_INFO1_MASK registers are 0.

When clearing the status flags in registers SD_INFO1, SD_INFO2, and SDIO_INFO1, write 0 to the status flags to be cleared and write 1 to the status flags that are not being cleared.

Table 39.5 Interrupt sources

Interrupt sources	Status flag register		Interrupt mask register		Interrupt name
	Register symbol	Bit symbol	Register symbol	Bit symbol	Ch n (n = 0)
Card Access Interrupt (CACI)	SD_INFO1	ACEND	SD_INFO1_MASK	ACENDM	SDHI_MMCn_ACCS
		RSPEND		RSPENDM	
	SD_INFO2	ILA	SD_INFO2_MASK	ILAM	
		BWE		BWEM	
		BRE		BREM	
		RSPTO		RSPTOM	
		ILR		ILRM	
		ILW		ILWM	
		DTO		DTOM	
		ENDE		ENDEM	
		CRCE		CRCEM	
		CMDE		CMDEM	
SDIO Access Interrupt (SDACI)	SDIO_INFO1	EXWT	SDIO_INFO1_MASK	EXWTM	SDHI_MMCn_SDIO
		EXPUB52		EXPUB52M	
		IOIRQ		IOIRQM	
Card Detect Interrupt (CDETI)	SD_INFO1	SDD3IN	SD_INFO1_MASK	SDD3INM	SDHI_MMCn_CARD
		SDD3RM		SDD3RMM	
		SDCDIN		SDCDINM	
		SDCDRM		SDCDRMM	

39.3.3.2 DMA transfer requests (SDHI_MMCn_ODMSDBREQ, n = 0)

The SD/MMC Host Interface has two types of DMA transfer requests.

(1) SD_BUF write DMA transfer request

- When the BWE bit in SD_INFO2 is set to 1 while the DMAEN bit in SD_DMAEN is set to 1, the SD_BUF write DMA transfer request is asserted.
- The SD_BUF write DMA transfer request is negated when the last data in one block (based on the transfer data size set in SD_SIZE) is transferred. The SD_BUF write DMA transfer request is also negated by clearing the SDRST bit in SOFT_RST to 0 or setting the STP bit in SD_STOP to 1. However, if a communications error or timeout occurs at the DMA transfer, the SD_BUF write DMA transfer request is not negated.
- The BWE bit in SD_INFO2 is cleared after transfer of the last data in one block following a request for writing to SD_BUF by DMA transfer.
- The number of DMA transfers must be n × one block. (n = integer, one block = the transfer data size set in SD_SIZE)
- When the IOABT bit in SDIO_MODE is set to 1, the SD_BUF write DMA transfer request is negated.

39.3.3 中断请求和DMA传输请求

39.3.3.1 Interrupts

表39.5列出了SDHI中断源。SDHI在以下情况下请求中断：

●寄存器SD_INFO1、SD_INFO2和SDIO_INFO1中的状态标志设置为1。

●SD_INFO1_MASK、SD_INFO2_MASK和SDIO_INFO1_MASK寄存器中的相关位为0。

清除寄存器SD_INFO1、SD_INFO2和SDIO_INFO1中的状态标志时，将要清除的状态标志写入0，将未清除的状态标志写入1。

Table 39.5 中断源

中断源	状态标志寄存器		中断屏蔽寄存器		中断名称
	注册符号	位符号	注册符号	位符号	Ch n (n = 0)
卡访问中断(CACI)	SD_INFO1	ACEND	SD_INFO1_MASK	ACENDM	SDHI_MMCn_ACCS
		RSPEND		RSPENDM	
	SD_INFO2	ILA	SD_INFO2_MASK	ILAM	
		BWE		BWEM	
		BRE		BREM	
		RSPTO		RSPTOM	
		ILR		ILRM	
		ILW		ILWM	
		DTO		DTOM	
		ENDE		ENDEM	
		CRCE		CRCEM	
		CMDE		CMDEM	
SDIO访问中断(SDACI)	SDIO_INFO1	EXWT	SDIO_INFO1_MASK	EXWTM	SDHI_MMCn_SDIO
		EXPUB52		EXPUB52M	
		IOIRQ		IOIRQM	
卡检测中断(CDETI)	SD_INFO1	SDD3IN	SD_INFO1_MASK	SDD3INM	SDHI_MMCn_CARD
		SDD3RM		SDD3RMM	
		SDCDIN		SDCDINM	
		SDCDRM		SDCDRMM	

39.3.3.2 DMA传输请求(SDHI_MMCn_ODMSDBREQ n=0)

SDMMC主机接口有两种类型的DMA传输请求。

(1) SD_BUF写DMA传输请求

●当SD_INFO2中的BWE位设置为1而SD_DMAEN中的DMAEN位设置为1时，SD_BUF写DMA传输请求被置位。

●当一个块中的最后一个数据（基于SD_SIZE中设置的传输数据大小）被传输时，SD_BUF写DMA传输请求被否定。SD_BUF写DMA传输请求也可以通过将SOFT_RST中的SDRST位清0或将SD_STOP中的STP位设置为1来取消。但是，如果通信错误或超时发生在
DMA传输，SD_BUF写DMA传输请求不被否定。

●SD_INFO2中的BWE位在通过DMA传输向SD_BUF写入请求后传输一个块中的最后一个数据后被清除。

●DMA传输的数量必须是n×1个块。（n=整数，1块=SD_SIZE中设置的传输数据大小）

●当SDIO_MODE中的IOABT位设置为1时，SD_BUF写DMA传输请求被否定。

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- The DMA transfer request is also negated by clearing the DMAEN bit to 0. However, the DMA transfer request is asserted again when the DMAEN bit is set to 1 before writing to SD_CMD.
- Because the BWE bit in SD_INFO2 is not cleared in response to setting the STP/IOABT bit, or to a communications error or timeout, clear the bit to 0 before issuing the next command. The next request to write to SD_BUF by DMA transfer is not issued while the BWE bit is set.

(2) SD_BUF read DMA transfer request

- When the BRE bit in SD_INFO2 is set to 1 while the DMAEN bit in the SD_DMAEN register is set to 1, the SD_BUF read DMA transfer request is asserted.
- The SD_BUF read DMA transfer request is negated when the last data in one block (based on the transfer data size set in SD_SIZE) is transferred. The SD_BUF read DMA transfer request is also negated by clearing the SDRST bit in SOFT_RST to 0 or setting the STP bit in SD_STOP to 1. However, if a communications error or timeout occurs at the DMA transfer, the SD_BUF read DMA transfer request is not negated.
- The BRE bit in SD_INFO2 is cleared after transfer of the last data in one block following a request to write to SD_BUF by DMA transfer.
- The number of DMA transfers must be n × one block. (n = integer, one block = the transfer data size set in SD_SIZE)
- When the IOABT bit in SDIO_MODE is set to 1, the SD_BUF read DMA transfer request is negated.
- The DMA transfer request is also negated by clearing the DMAEN bit to 0. However, the DMA transfer request is asserted again when the DMAEN bit is set to 1 before writing to SD_CMD.
- Because the BRE bit in SD_INFO2 is not cleared in response to setting the STP/IOABT bit or in response to a communications error or timeout, clear the bit to 0 before issuing the next command. The next request to write to SD_BUF by DMA transfer is not issued while the BRE bit is set.

39.3.4 Communication Errors and Timeouts

When a communication error or timeout error occurs, depending on the type of error, the associated status flag in the SD_INFO2 register sets to 1. Also, depending on the source of the error, the associated flag in the SD_ERR_STS1 or SD_ERR_STS2 register sets to 1.

The status flags in registers SD_ERR_STS1 and SD_ERR_STS2 clear to 0 by writing to the SD_CMD register, or by setting the SOFT_RST.SDRST bit to 0.

Table 39.6 Communication errors

Communication error	Interrupt flag register		Error status register		This occurs when…
	Register symbol	Bit symbol	Register symbol	Bit symbol	
End bit error	SD_INFO2	ENDE	SD_ERR_STS1	CRCLENE	The CRC status token length is in error
				RDLENE	The read data length is in error
				RSPLENE1	The response length is in error*1
				RSPLENE0	The response length is in error*2
CRC error		CRCE		CRCTKE	The CRC status token is in error
				RDCRCE	There is a CRC error in the read data
				RSPCRCE1	There is a CRC error in the response*1
				RSPCRCE0	There is a CRC error in the response*2
Command error		CMDE		CMDE1	The command index field value for the transmitted command and received response do not match*1
				CMDE0	The command index field value for the transmitted command and received response do not match*2

Note 1. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 2. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.

●DMA传输请求也可以通过将DMAEN位清除为0来取消。但是，当DMAEN位在写入SD_CMD之前设置为1时，DMA传输请求会再次被断言。

●由于SD_INFO2中的BWE位不会因设置STPIOABT位、通信错误或超时而被清除，所以在发出下一个命令之前将该位清除为0。当BWE位置位时，不会发出通过DMA传输写入SD_BUF的下一个请求。

(2) SD_BUF读取DMA传输请求

●当SD_INFO2中的BRE位设置为1且SD_DMAEN寄存器中的DMAEN位设置为1时，SD_BUF读取DMA传输请求被断言。

●当一个块中的最后一个数据（基于SD_SIZE中设置的传输数据大小）被传输时，SD_BUF读DMA传输请求被否定。SD_BUF读取DMA传输请求也可以通过将SOFT_RST中的SDRST位清0或将SD_STOP中的STP位设置为1来取消。但是，如果通信错误或超时发生在

DMA传输，SD_BUF读DMA传输请求不被否定。

●SD_INFO2中的BRE位在通过DMA传输请求写入SD_BUF后传输一个块中的最后一个数据后清除。

●DMA传输的数量必须是n×1个块。（n=整数，1块=SD_SIZE中设置的传输数据大小）

●当SDIO_MODE中的IOABT位设置为1时，SD_BUF读DMA传输请求被否定。

●DMA传输请求也可以通过将DMAEN位清除为0来取消。但是，当DMAEN位在写入SD_CMD之前设置为1时，DMA传输请求会再次被断言。

●因为SD_INFO2中的BRE位没有被清除以响应设置STPIOABT位或响应
通信错误或超时，在发出下一个命令之前将该位清零。当BRE位置位时，不会发出下一个通过DMA传输写入SD_BUF的请求。

39.3.4 通信错误和超时

当发生通信错误或超时错误时，根据错误类型，SD_INFO2寄存器中的相关状态标志设置为1。此外，根据错误源，SD_ERR_STS1或
SD_ERR_STS2寄存器设置为1。

通过写入SD_CMD寄存器或将SOFT_RST.SDRST位设置为0，寄存器SD_ERR_STS1和SD_ERR_STS2中的状态标志清零。

Table 39.6 通讯错误

通信故障	中断标志寄存器		错误状态寄存器		这发生在……
	注册符号	位符号	注册符号	位符号	
结束位错误	SD_INFO2	ENDE	SD_ERR_STS1	CRCLENE	CRC状态令牌长度错误
				RDLENE	读取数据长度错误
				RSPLENE1	响应长度错误*1
				RSPLENE0	响应长度错误*2
CRC error		CRCE		CRCTKE	CRC状态令牌错误
				RDCRCE	读取数据有CRC错误
				RSPCRCE1	响应中有CRC错误*1
				RSPCRCE0	响应中有CRC错误*2
命令错误		CMDE		CMDE1	发送命令和接收响应的命令索引字段值不匹配*1
				CMDE0	发送命令和接收响应的命令索引字段值不匹配*2

注1.通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12
SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
注2.通过SD_CMD中的设置，CMD12之外的CMD
SD_STOP中的STP位设置为1，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。

Table 39.7 Timeouts

Timeout	Interrupt flag register		Error status register		This occurs when…
	Register symbol	Bit symbol	Register symbol	Bit symbol	
Response timeout	SD_INFO2	RSPTO	SD_ERR_STS2	RSPTO1	A response is not received even after a minimum of 640 SDHI clock cycles elapse*1
				RSPTO0	A response is not received even after a minimum of 640 SDHI clock cycles elapse*2
Data timeout (excluding response timeout)		DTO		CRCBSYTO	After the CRC status token is received, the SDHI is busy for at least the period set*3
				CRCTO	After the write data is transmitted, the CRC status token is not received even after at least the period set*3 elapses
				RDTO	After the read command is issued, the read data is not received even after at least the period set*3 elapses
					After the read data is received, the next block read data is not received even after at least the period set*3 elapses
					After the SDHI exits the read wait state, the next block read data is not received even after at least the period set*3 elapses
				BSYTO1	After CMD12 is issued during the command sequence, the SDHI is busy for at least the period set*3
				BSYTO0	After the R1b response is received, the SDHI is busy for at least the period set*3 (a command other than CMD12 is issued during the command sequence)

Note 1. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 2. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP bit is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 3. The period is set in the SD_OPTION.TOP[3:0] bits.

39.3.5 Command without Data Transfer (SD/MMC)

Figure 39.9 and Figure 39.10 show example flows.

Table 39.7 Timeouts

Timeout	中断标志寄存器		错误状态寄存器		这发生在……
	注册符号	位符号	注册符号	位符号	
响应超时	SD_INFO2	RSPTO	SD_ERR_STS2	RSPTO1	即使经过至少640个SDHI时钟周期，也没有收到响应*1
				RSPTO0	即使经过至少640个SDHI时钟周期，也没有收到响应*2
数据超时（不包括响应超时）		DTO		CRCBSYTO	收到CRC状态令牌后，SDHI至少在设置的时间段内处于忙碌状态*3
				CRCTO	发送写入数据后，即使经过至少设置的时间段*3也不会接收到CRC状态令牌
				RDTO	发出读取命令后，即使经过至少设置的周期*3也不会接收到读取数据 elapses
					在接收到读取数据后，即使经过至少设置的时间段*3也不会接收到下一个块读取数据
					在SDHI退出读取等待状态后，即使经过至少设置的时间段*3，也不会接收到下一个块读取数据
				BSYTO1	在命令序列期间发出CMD12后，SDHI至少在设置的时间段内处于忙碌状态*3
				BSYTO0	收到R1b响应后，SDHI至少在设置的时间段*3内处于忙碌状态（在命令序列期间发出CMD12以外的命令）

注1.通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12
SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
注2.通过SD_CMD中的设置，CMD12之外的CMD
SD_STOP位中的STP位设置为1，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
注3.周期在SD_OPTION.TOP[3:0]位中设置。

39.3.5 无数据传输的命令(SDMMC)

图39.9和图39.10显示了示例流程。

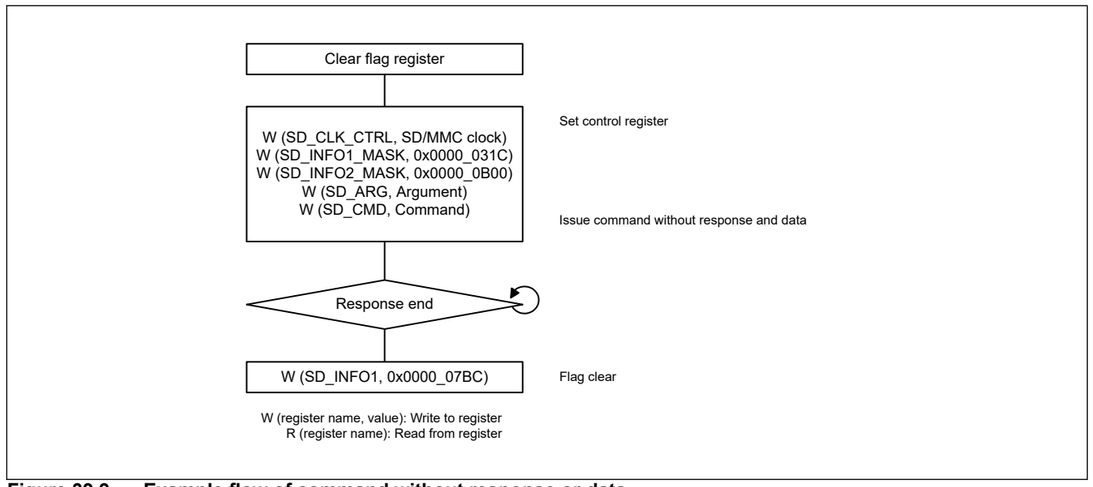

Figure 39.9 Example flow of command without response or data

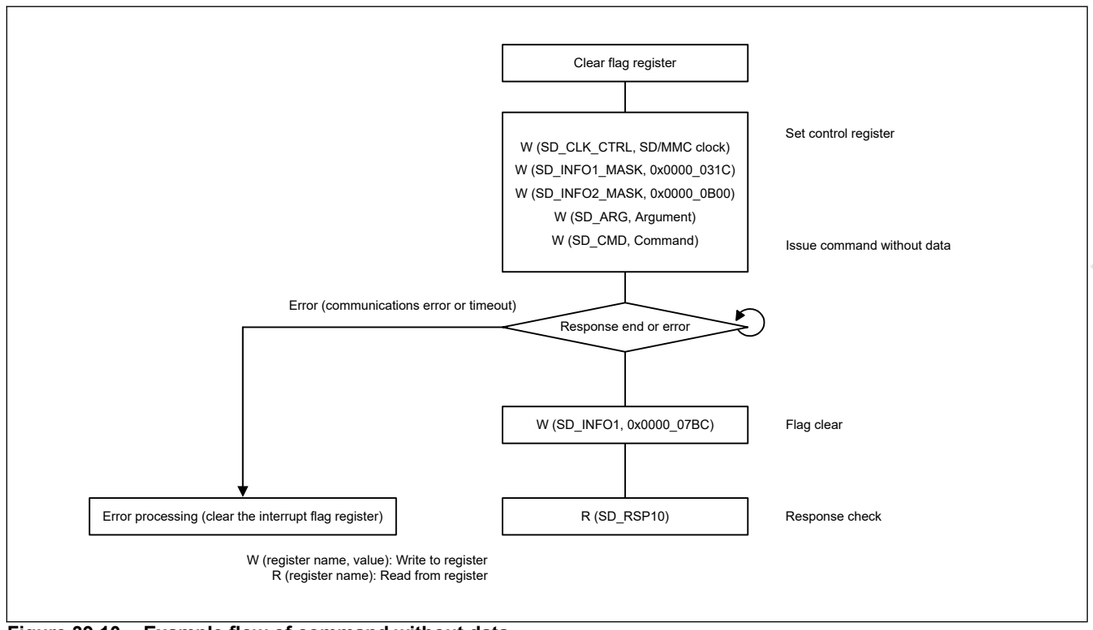

Figure 39.10 Example flow of command without data

39.3.5.1 Operation for command without data transfer

The following legend is used for description of register read/write.

W (register name, value): Write to register

R (register name): Read from register

The operation is described in the following section.

(1) Command without response and data

a. Flag register clear
First, clear the bits in the flag register. (SD_INFO1 and SD_INFO2)

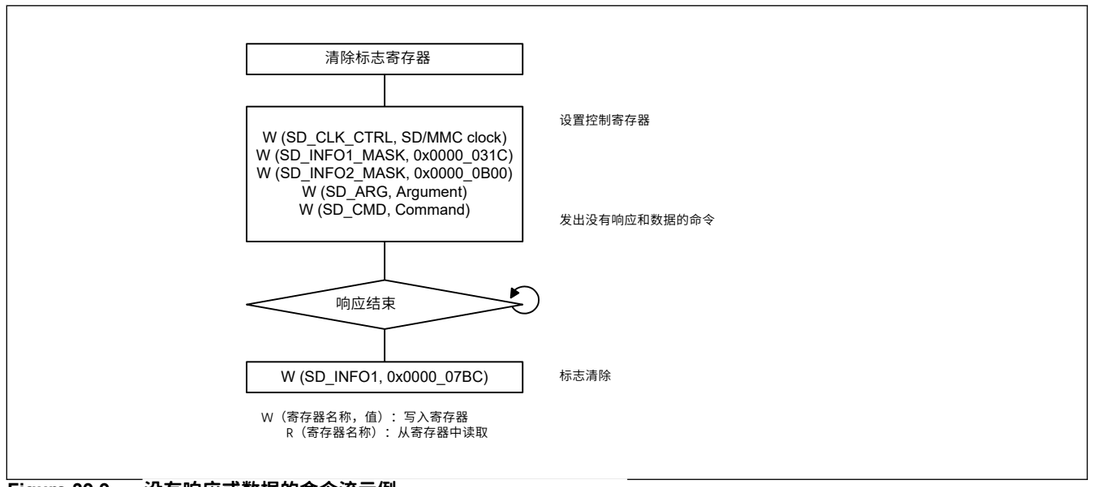

Figure 39.9 没有响应或数据的命令流示例

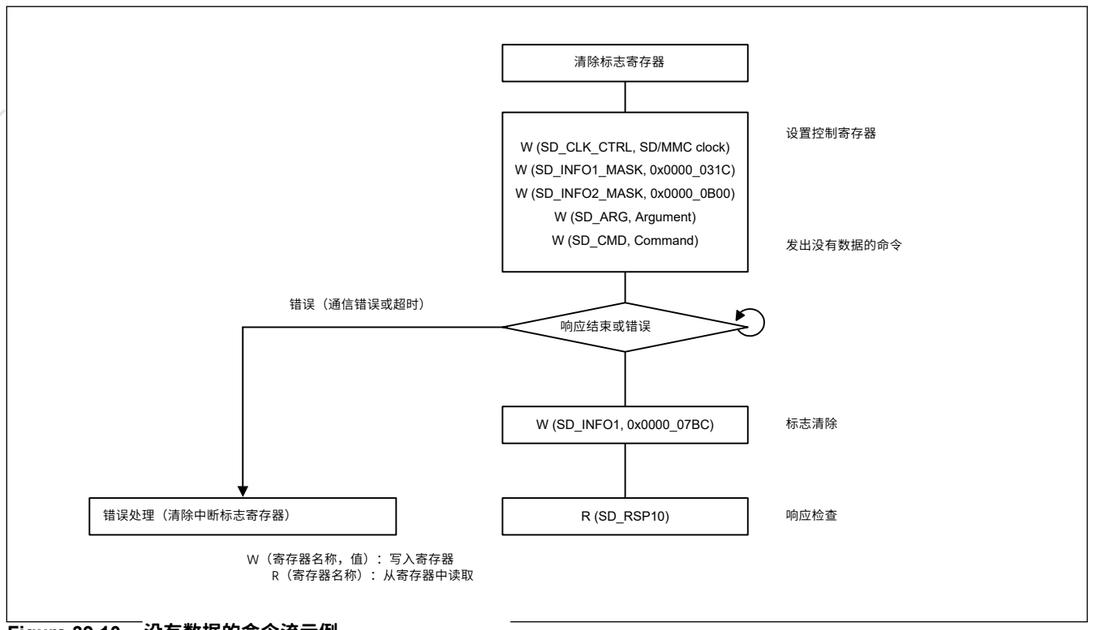

Figure 39.10 没有数据的命令流示例

39.3.5.1 无数据传输的命令操作

以下图例用于描述寄存器读写。

W（寄存器名称，值）：写入寄存器

R（寄存器名称）：从寄存器中读取

该操作在下一节中描述。

(1) 没有响应和数据的命令

a. 标志寄存器清除
首先，清除标志寄存器中的位。（SD_INFO1和SD_INFO2）

b. Control register set
Set the SD/MMC clock and interrupt masking. (SD_CLK_CTRL, SD_INFO1_MASK, and SD_INFO2_MASK)

c. Command issue
Set CMD argument in SD_ARG and write to SD_CMD.
Accordingly, CMD is issued, and the operation is started.

d. Flag clear
When transmission of a command is completed, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0.

(2) Command without data

a. Flag register clear
First, clear the bits in the flag register. (SD_INFO1 and SD_INFO2)

b. Control register set
Set the SD/MMC clock and interrupt masking. (SD_CLK_CTRL, SD_INFO1_MASK, and SD_INFO2_MASK)

c. Command issue
Set CMD argument in SD_ARG and write to the SD_CMD.
Accordingly, CMD is issued, and the operation is started.

d. Flag clear
When a response is received, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0.

e. Read a response from SD_RSP10. Additionally, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

39.3.6 Single Block Read (SD/MMC)

Figure 39.11 shows an example flow of a single block read operation.

湾。控制寄存器组
设置SDMMC时钟和中断屏蔽。（SD_CLK_CTRL、SD_INFO1_MASK和SD_INFO2_MASK）

c. 命令问题
在SD_ARG中设置CMD参数并写入SD_CMD。因此，
发出CMD，并开始操作。

d。标志清除
当命令传输完成时，SD_INFO1中的RSPEND（响应结束）设置为1以产生中断。将RSPEND清除为0。

(2) 没有数据的命令

a. 标志寄存器清除
首先，清除标志寄存器中的位。（SD_INFO1和SD_INFO2）

湾。控制寄存器组
设置SDMMC时钟和中断屏蔽。（SD_CLK_CTRL、SD_INFO1_MASK和SD_INFO2_MASK）

c. 命令问题
在SD_ARG中设置CMD参数并写入SD_CMD。
因此，发出CMD，并开始操作。

d。标志清除
当收到响应时，SD_INFO1中的RSPEND（响应结束）置1以产生中断。将RSPEND清除为0。

e. 从SD_RSP10读取响应。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）
。

39.3.6 单块读取(SDMMC)

图39.11显示了单块读取操作的示例流程。

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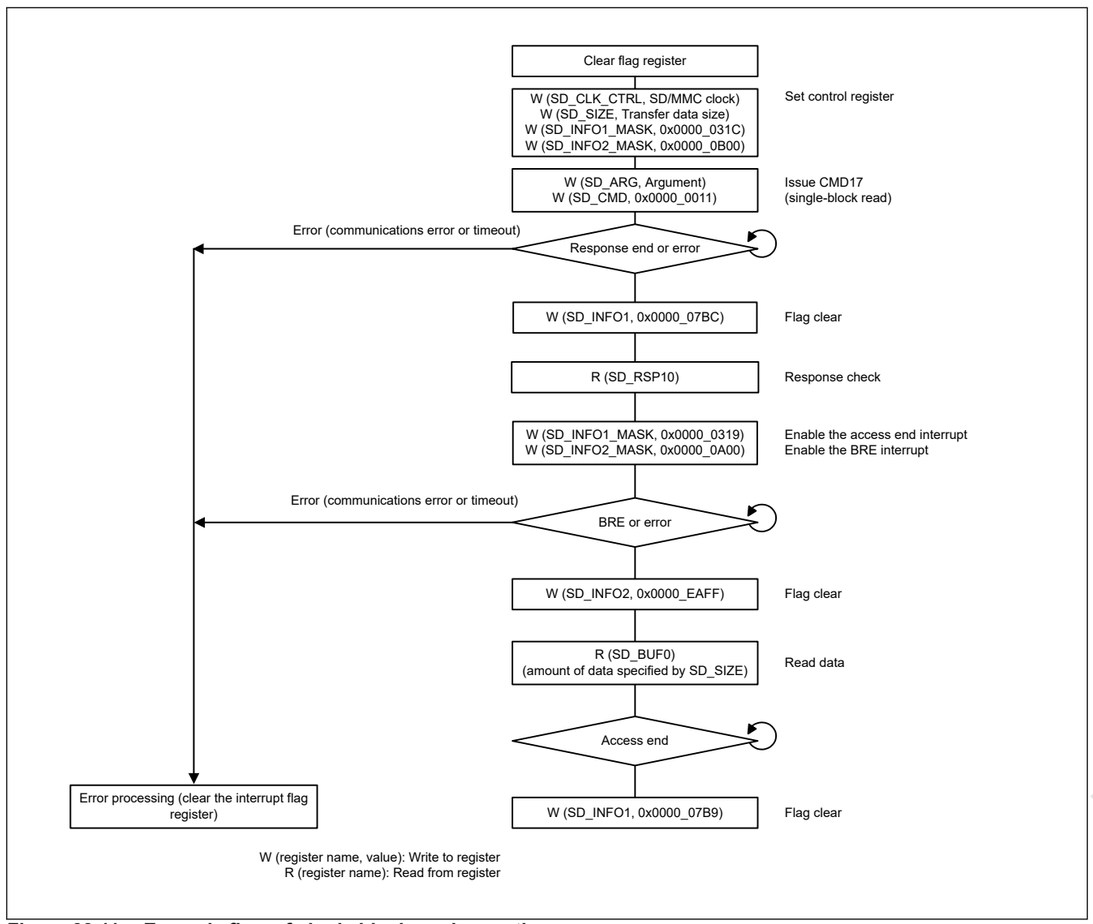

Figure 39.11 Example flow of single block read operation

39.3.6.1 Single block read operation

The operation of the single block read is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).

c. Command issue (CMD17)
Set CMD17 argument in SD_ARG and write 0x0000_0011 to SD_CMD. CMD17 is issued and the single block read operation is started.

d. Response check
On receiving the response, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0 and read the response from SD_RSP10. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP or the IOABT bit in SDIO_MODE to 1. In addition, this causes CMD12 and CMD52 to not be issued. If the ACEND bit (access end) in SD_INFO1 is set, halting the command sequence also leads to the generation of an interrupt.

e. Data receive from SD card/MMC and data read

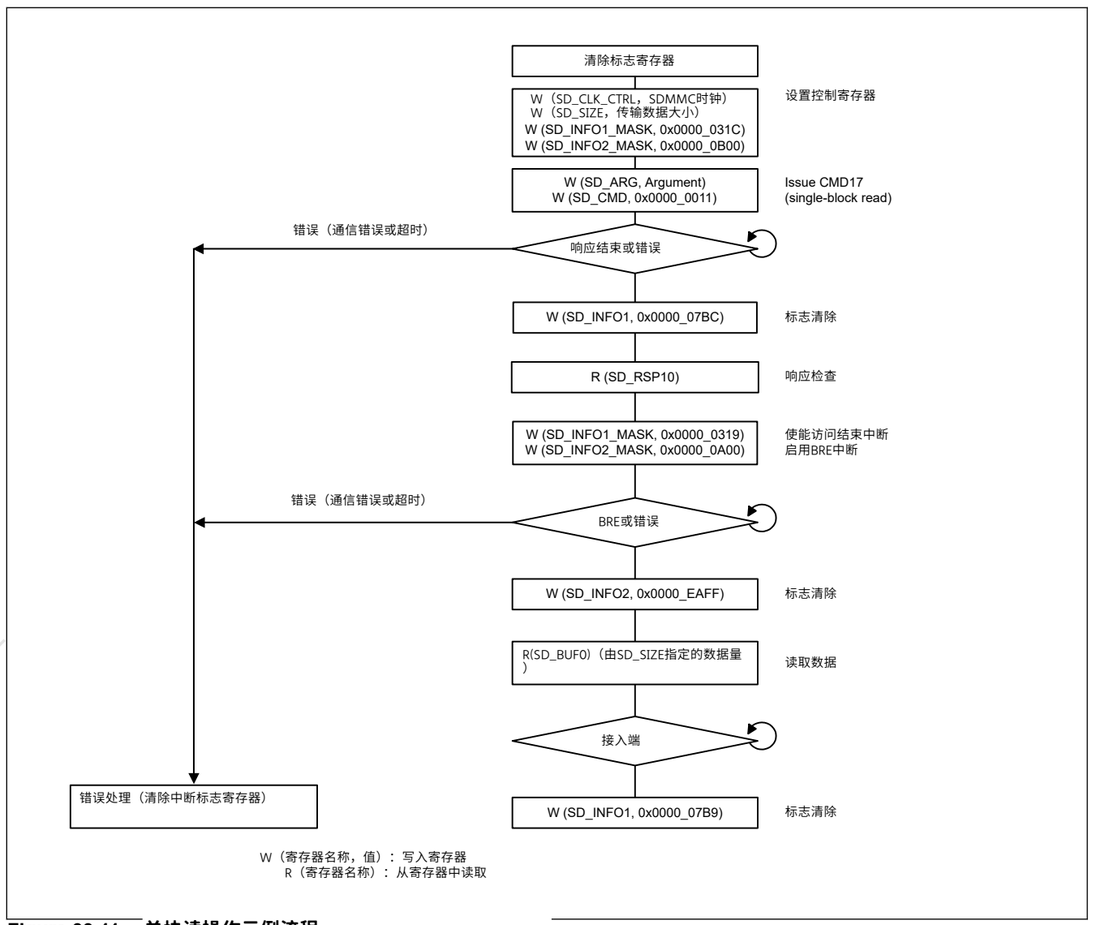

Figure 39.11 单块读操作示例流程

39.3.6.1 单块读操作

单块读取的操作描述如下：

a. 标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).

c. 命令问题(CMD17)
在SD_ARG中设置CMD17参数并将0x0000_0011写入SD_CMD。发出CMD17并开始单块读取操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND（响应结束）置1以产生中断。将RSPEND清零并从SD_RSP10读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位或SDIO_MODE中的IOABT位设置为1来停止命令序列。此外，这会导致CMD12和CMD52不发出。如果SD_INFO1中的ACEND位（访问结束）被设置，停止命令序列也会导致产生中断。

e. 从SD卡MMC接收数据并读取数据

Write 0x0000_0319 to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_0A00 to SD_INFO2_MASK to enable the BRE interrupt. When the data received from the SD card/MMC is completed, the BRE bit in SD_INFO2 is set to 1 to generate an interrupt. Clear the BRE bit to 0 and read the amount of data specified in SD_SIZE from SD_BUF0.
A communication error or timeout might be generated if data is being received while reading of SD_BUF0 is in progress.

f. Operation complete
When the data read from SD_BUF0 is completed, ACEND (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear ACEND to 0 to end the single block read operation.
Additionally, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

39.3.7 Single Block Write (SD/MMC)

Figure 39.12 shows an example flow of a single block write operation.

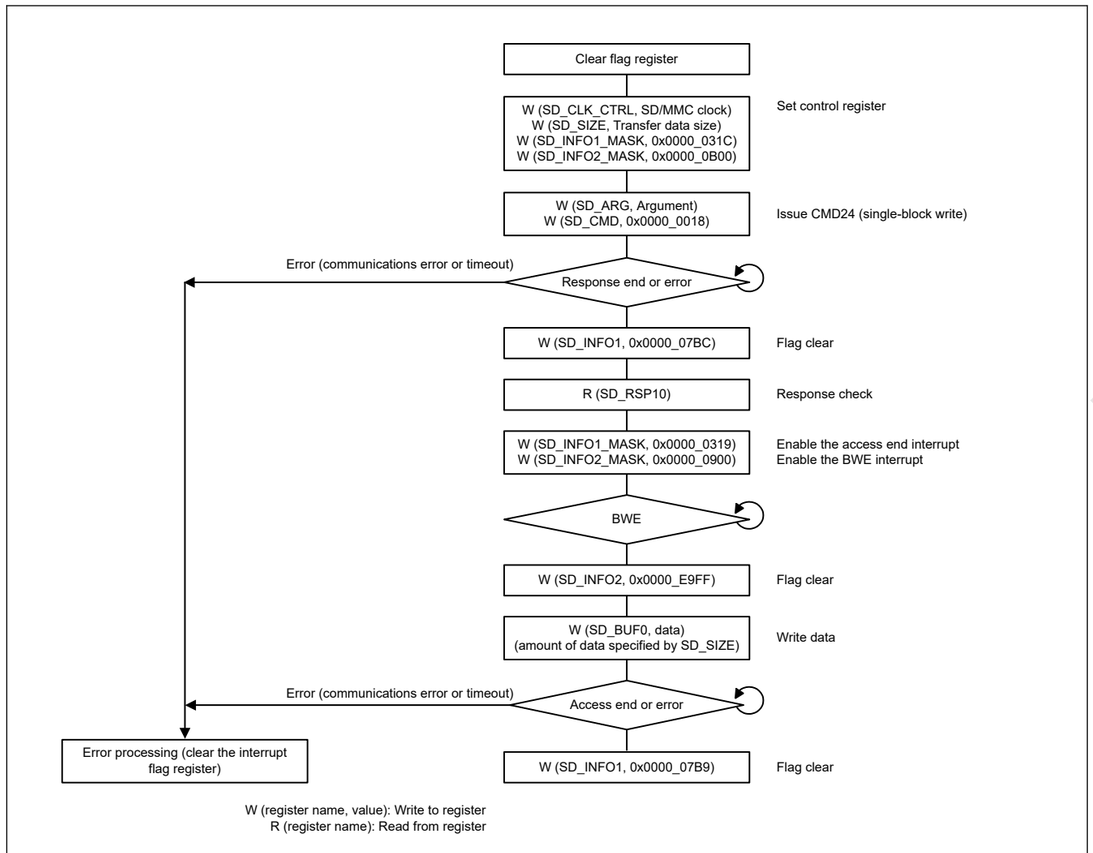

Figure 39.12 Example of single block write operation

39.3.7.1 Single block write operation

The operation of the single block write is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set

将0x0000_0319写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_0A00写入SD_INFO2_MASK启用BRE中断。当从SD卡MMC接收到数据完成时，SD_INFO2中的BRE位设置为1以产生中断。将BRE位清0并从SD_BUF0中读取SD_SIZE中指定的数据量。

如果在读取SD_BUF0时正在接收数据，则可能会产生通信错误或超时。

f. 操作完成
当从SD_BUF0读取数据完成后，SD_INFO1中的ACEND（访问结束）置1以产生中断。将ACEND清0结束单块读操作。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

39.3.7 单块写入(SDMMC)

图39.12显示了单个块写入操作的示例流程。

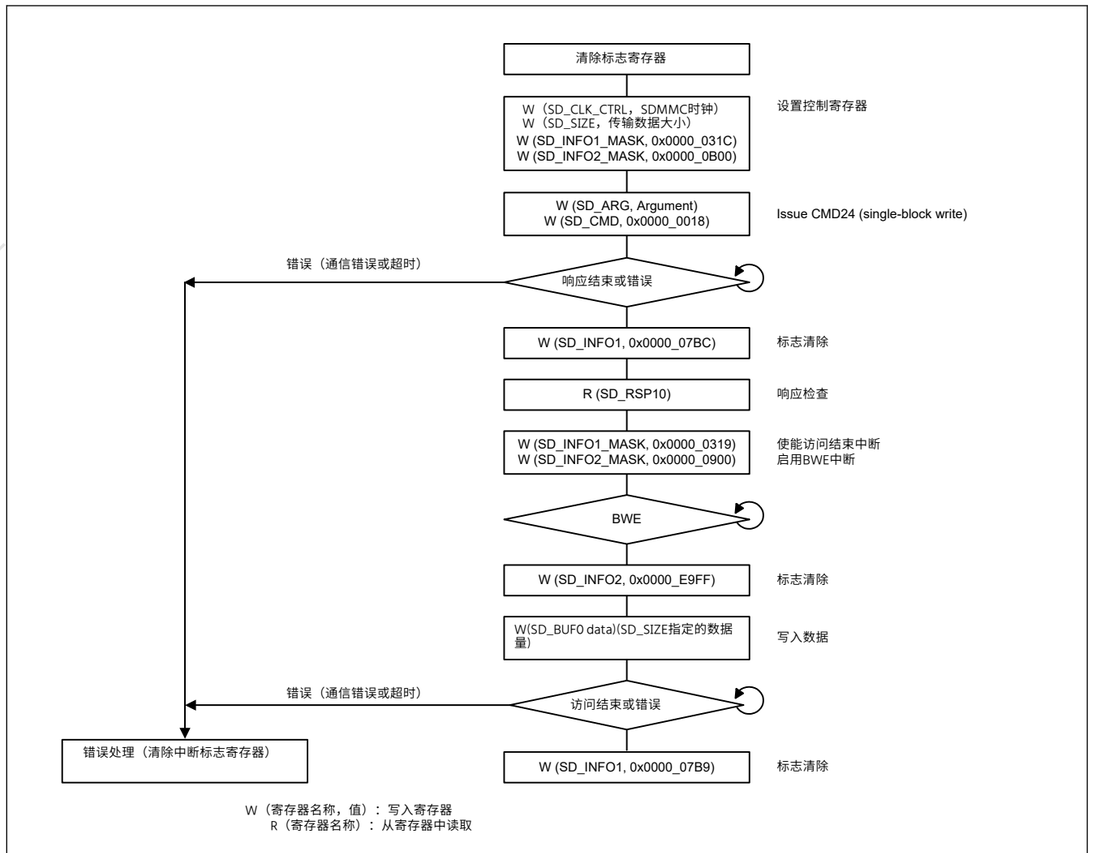

Figure 39.12 单块写操作示例

39.3.7.1 单块写操作

单块写操作描述如下：

a. 标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组

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Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).

c. Command issue (CMD24)
Set CMD24 argument in SD_ARG and write 0x0000_0018 to SD_CMD. CMD24 is issued and the single block write operation is started.

d. Response check
On receiving the response, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0 and read the response from SD_RSP10. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP or the IOABT bit in SDIO_MODE to 1. In addition, this causes CMD12 and CMD52 to not be issued. If the ACEND bit (access end) in SD_INFO is set, halting the command sequence also leads to the generation of an interrupt.

e. Data write and data transmit to SD card/MMC
Write 0x0000_0319 to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_0900 to SD_INFO2_MASK to enable the BWE interrupt. When SD_BUF0 is ready for the data to be written, the BWE bit in SD_INFO2 is set to 1 to generate an interrupt. Clear the BWE bit to 0 and write the amount of data specified in SD_SIZE to SD_BUF0. When the data write to SD_BUF0 is completed, data is transmitted to the SD card. Then, the CRC status and busy state are received from the SD card/MMC.
However, a communications error or timeout might be generated if data is being transmitted after writing to SD_BUF0.

f. Operation complete
When the CRC status and busy state are received from the SD card/MMC, ACEND (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the ACEND bit to 0 to end the single block write operation.
In addition, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

39.3.8 Multiple Block Read (SD/MMC)

Figure 39.13 shows an example flow of a multiple block read operation.

设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).

c. 命令问题(CMD24)
在SD_ARG中设置CMD24参数并将0x0000_0018写入SD_CMD。发出CMD24并开始单块写入操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND（响应结束）置1以产生中断。将RSPEND清零并从SD_RSP10读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位或SDIO_MODE中的IOABT位设置为1来停止命令序列。此外，这会导致CMD12和CMD52不发出。如果SD_INFO中的ACEND位（访问结束）被设置，停止命令序列也会导致中断的产生。

e. 数据写入和数据传输到SD卡MMC
将0x0000_0319写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_0900写入SD_INFO2_MASK以启用BWE中断。当SD_BUF0准备好写入数据时，SD_INFO2中的BWE位设置为1以产生中断。将BWE位清0并写入指定的数据量

SD_SIZE到SD_BUF0。数据写入SD_BUF0完成后，将数据传输到SD卡。然后，
从SD卡MMC接收CRC状态和忙状态。
但是，如果在写入SD_BUF0后正在传输数据，则可能会产生通信错误或超时。

f. 操作完成
当从SD卡MMC接收到CRC状态和忙状态时，SD_INFO1中的ACEND（访问端）置1以产生中断。将ACEND位清0以结束单块写操作。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

39.3.8 多块读取(SDMMC)

图39.13显示了多块读取操作的示例流程。

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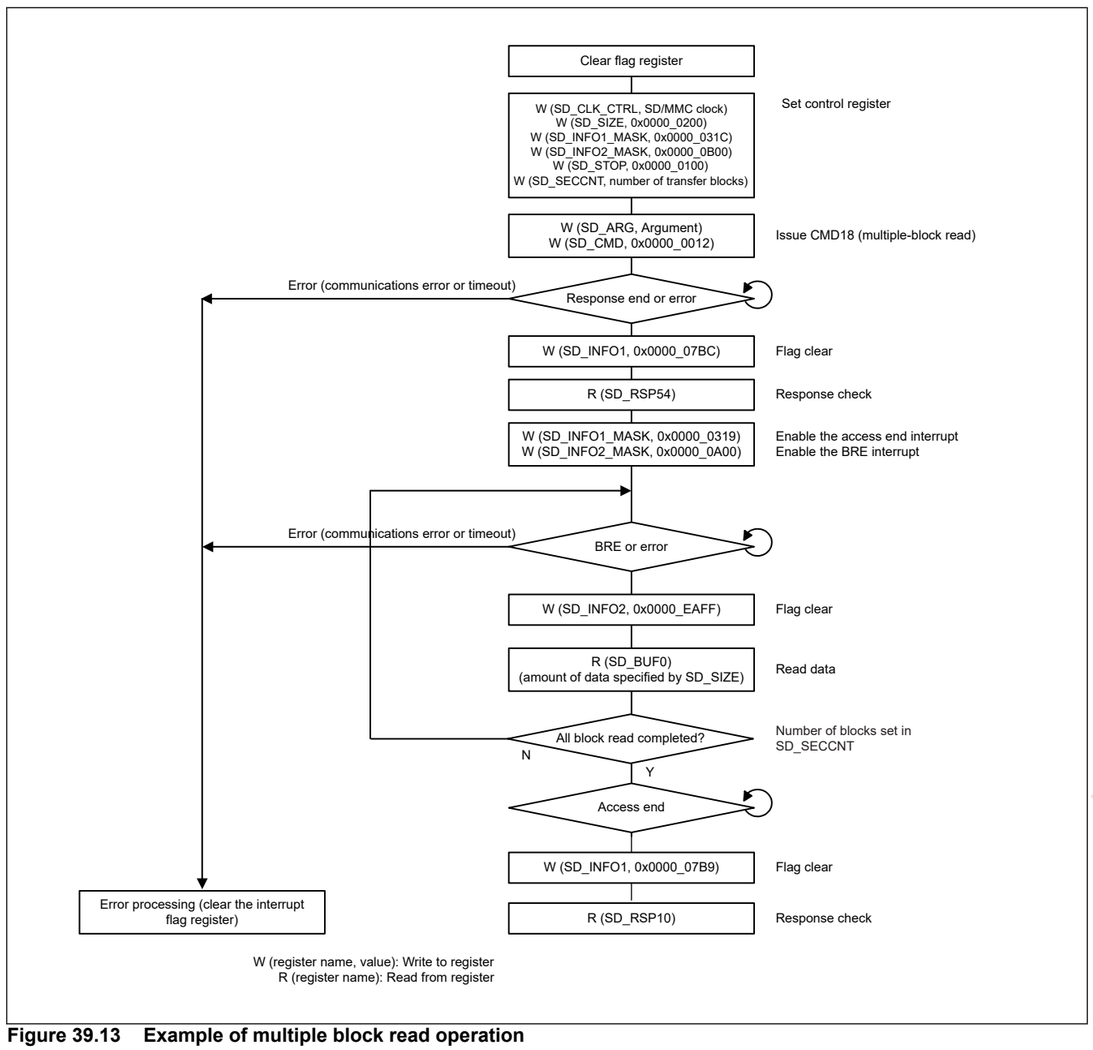

Figure 39.13 Example of multiple block read operation

39.3.8.1 Multiple block read operation

The operation of the multiple block read is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).
Set SEC in SD_STOP to 1, and set the number of transfer blocks in SD_SECCNT.

c. Command issue (CMD18)
Set CMD18 argument in SD_ARG and write 0x0000_0012 to SD_CMD. CMD18 is issued and the multiple block read operation is started.

d. Response check
On receiving the response, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0 and read the response from SD_RSP54. If the result of response decoding is an error, the command sequence can be

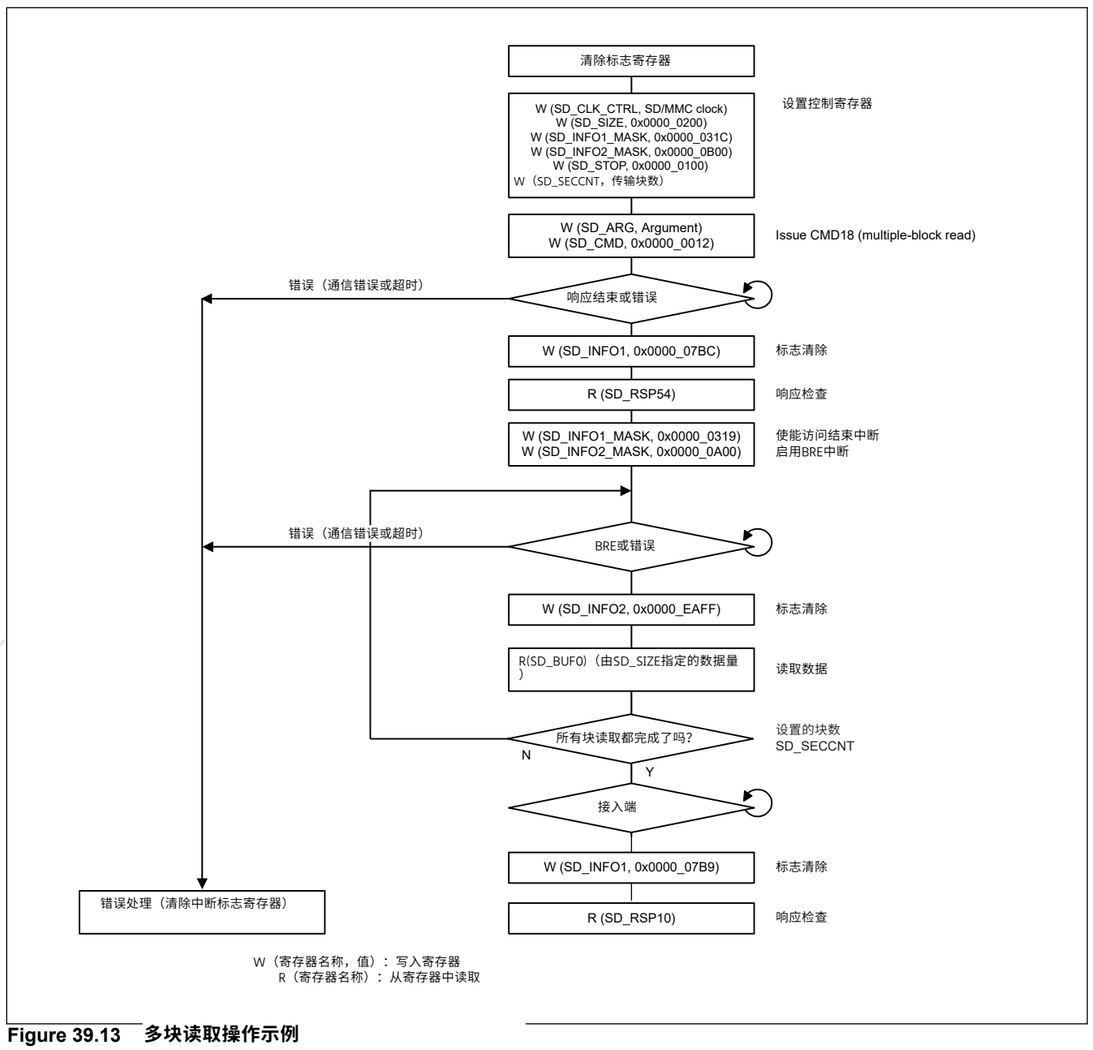

Figure 39.13 多块读取操作示例

39.3.8.1 多块读操作

多块读取的操作描述如下：

a. 标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).
将SD_STOP中的SEC设置为1，并在SD_SECCNT中设置传输块数。

c. 命令问题(CMD18)
在SD_ARG中设置CMD18参数并将0x0000_0012写入SD_CMD。发出CMD18并开始多块读取操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND（响应结束）置1以产生中断。将RSPEND清零并从SD_RSP54读取响应。
如果响应解码的结果是错误的，命令序列可以是

halted by setting the STP bit in SD_STP to 1. Setting the STP bit to 1 also causes CMD12 to be issued and the response received. If the command sequence is halted because the access end interrupt is enabled, an interrupt is generated when the ACEND bit (access end) bit in SD_INFO1 sets to 1 on completion of response reception. Clear the ACEND bit to 0 and read the response.

e. Data receive from SD card/MMC and data read
Write 0x0000_0319 to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_0A00 to SD_INFO2_MASK to enable the BRE interrupt. When one-block data received from the SD card/MMC is completed, the BRE bit in SD_INFO2 is set to 1 to generate an interrupt. Clear the BRE bit to 0 and read the amount of data specified in SD_SIZE from SD_BUF0. Doing this repeats transfer of the number of blocks set in SD_SECCNT. However, a communication error or timeout might be generated if data is being received while reading of SD_BUF0 is in progress. CMD12 is automatically issued to stop multiblock transfer with the number of blocks that is set to SD_SECCNT and the response is received. At this point, CMD12 argument is automatically set to 0x0000_0000.

f. Operation complete
When all-block data read and the CMD12 response received are completed, ACEND (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear ACEND to 0 to read the response. This is the end of multiple block read operation. In addition, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

39.3.9 Multiple Block Write (SD/MMC Using Internal Timer)

Figure 39.14 shows an example flow of a multiple block write using internal timer.

通过将SD_STP中的STP位设置为1来停止。将STP位设置为1也会导致发出CMD12并接收响应。如果由于使能访问结束中断而暂停命令序列，则在完成响应接收时SD_INFO1中的ACEND位（访问结束）位设置为1时产生中断。将ACEND位清0并读取响应。

e. 从SD卡MMC接收数据并读取数据
将0x0000_0319写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_0A00写入SD_INFO2_MASK以启用BRE中断。当从SD卡MMC接收到单块数据完成时，SD_INFO2中的BRE位被设置为1以产生中断。将BRE位清0并从SD_BUF0中读取SD_SIZE中指定的数据量。这样做会重复传输SD_SECCNT中设置的块数。但是，如果在读取SD_BUF0时正在接收数据，则可能会产生通信错误或超时。自动发出CMD12以停止多块传输，块数设置为SD_SECCNT并接收响应。此时，CMD12参数自动设置为0x0000_0000。

f. 操作完成
当全块数据读取和接收到的CMD12响应完成时，SD_INFO1中的ACEND（访问结束）置1以产生中断。将ACEND清除为0以读取响应。这是多块读取操作的结束。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

39.3.9 多块写入（使用内部定时器的SDMMC）

图39.14显示了使用内部定时器进行多块写入的示例流程。

RA生态工作室

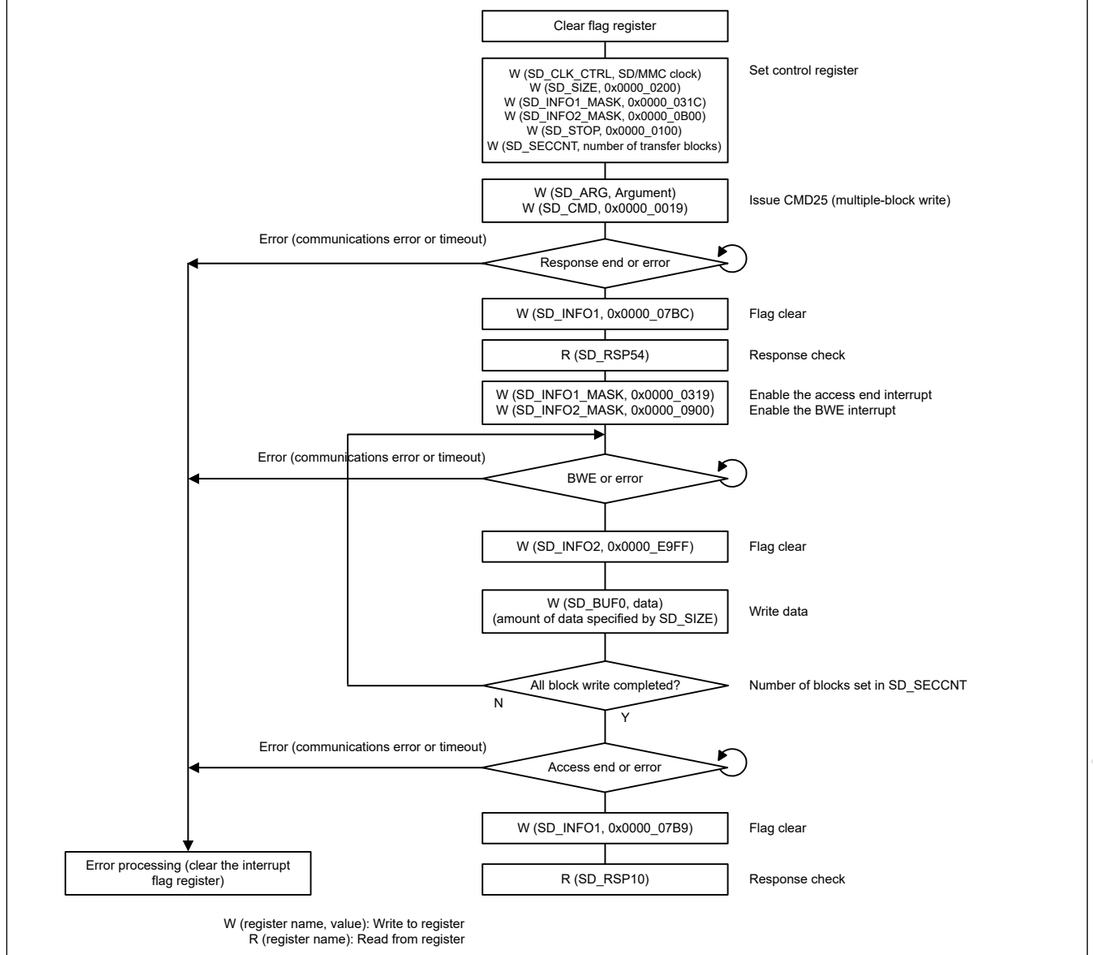

Figure 39.14 Example of multiple block write operation using internal timer

39.3.9.1 Multiple block write operation using internal timer

The operation of the multiple block write is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).
Set the SEC bit in SD_STOP to 1, and set the number of transfer blocks in SD_SECCNT.

c. Command issue (CMD25)
Set CMD25 argument in SD_ARG and write 0x0000_0019 to SD_CMD. CMD25 is issued and the multiple block write operation is started.

d. Response check
On receiving the response, the RSPEND bit (response end) in SD_INFO1 is set to 1 to generate an interrupt.
Clear the RSPEND bit to 0 and read the response from SD_RSP54. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP to 1. Setting the STP bit to 1 also causes CMD12 to

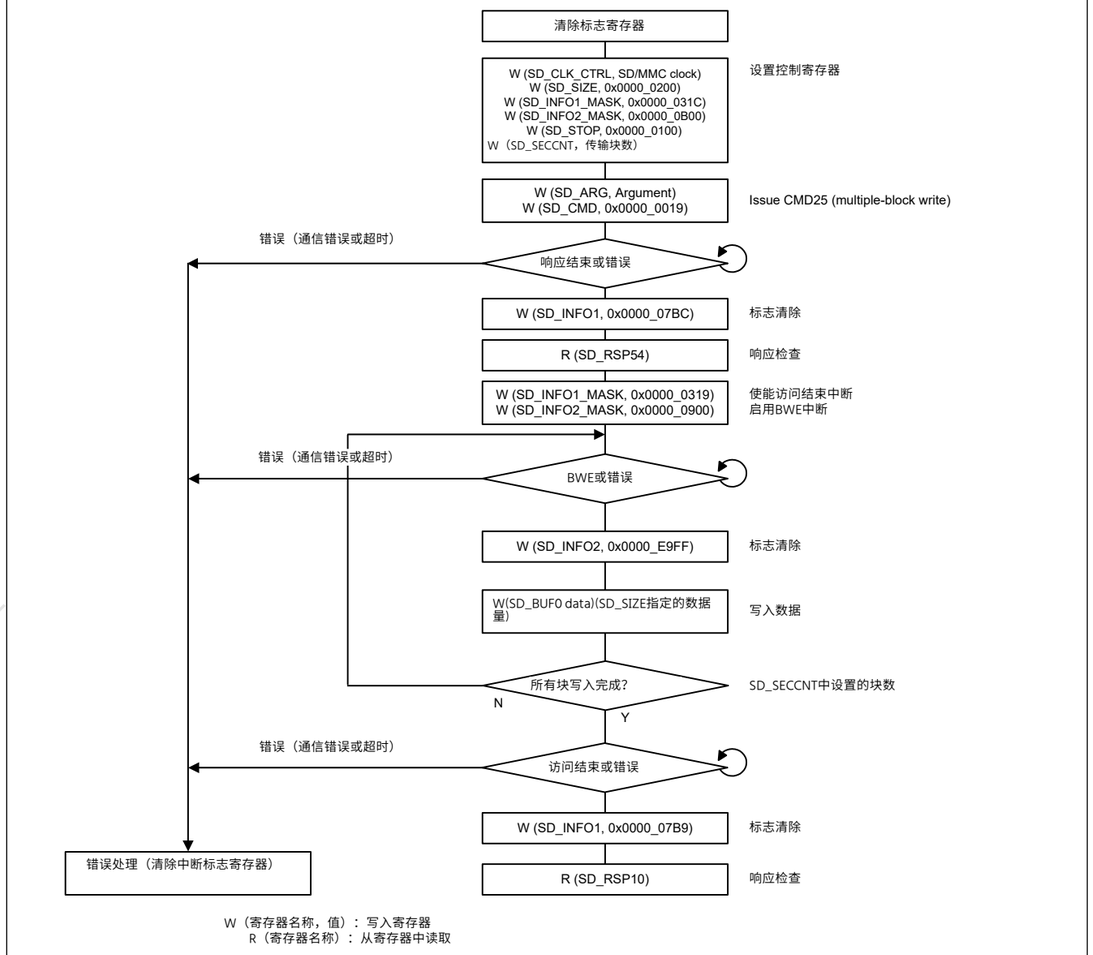

Figure 39.14 使用内部定时器的多块写入操作示例

39.3.9.1 使用内部定时器的多块写操作

多块写入的操作描述如下：

a. 标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).
将SD_STOP中的SEC位设置为1，并在SD_SECCNT中设置传输块数。

c. 命令问题(CMD25)
在SD_ARG中设置CMD25参数并将0x0000_0019写入SD_CMD。发出CMD25并开始多块写入操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND位（响应结束）置1以产生中断。
将RSPEND位清0并从SD_RSP54读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位设置为1来暂停命令序列。将STP位设置为1也会导致CMD12

be issued and the response received. If the command sequence is halted because the access end interrupt is enabled, an interrupt is generated by when the ACEND bit (access end) bit in SD_INFO1 sets to 1 on completion of response reception. Clear the ACEND bit to 0 and read the response.

e. Data write and data transmit to SD card/MMC
Write 0x0000_0319 to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_0900 to SD_INFO2_MASK to enable the BWE interrupt. When SD_BUF0 is ready for the data to be written, the BWE bit in the SD_INFO2 resister is set to 1 to generate an interrupt. Clear the BWE bit to 0 and write the amount of data specified in SD_SIZE to SD_BUF0. When the data write to SD_BUF0 is completed, data is transmitted to the SD card/MMC. The CRC status and busy state are received from the SD card/MMC. This repeats transfer of the number of blocks set in SD_SECCNT. However, a communication error or timeout might be generated if data is being received while writing to SD_BUF0 is in progress. CMD12 is automatically issued to stop multiblock transfer with the number of blocks which is set to SD_SECCNT and the response is received. At this point, CMD12 argument is automatically set to 0x0000_0000.

f. Operation complete
When all-block data transmit and the CRC status receive are completed, the ACEND bit (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the ACEND bit to 0 to read the response. This is the end of multiple block write operation. Additionally, perform error processing (clear the interrupt flag register) if a communications error or timeout occurs.

39.3.10 Multiple Block Write (MMC using external timer)

Figure 39.15 shows an example flow of a multiple block write using an external timer.

发出并收到响应。如果由于使能访问结束中断而暂停命令序列，则在完成响应接收时SD_INFO1中的ACEND位（访问结束）位设置为1时产生中断。将ACEND位清0并读取响应。

e. 数据写入和数据传输到SD卡MMC
将0x0000_0319写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_0900写入SD_INFO2_MASK启用BWE中断。当SD_BUF0准备好写入数据时，SD_INFO2寄存器设置为1以产生中断。将BWE位清除为0，并将SD_SIZE中指定的数据量写入SD_BUF0。当数据写入SD_BUF0完成后，数据被传输到SD卡MMC。这从SD卡MMC接收CRC状态和忙状态。这将重复传输设置的块数SD_SECCNT。但是，如果在写入SD_BUF0时正在接收数据，则可能会产生通信错误或超时。自动发出CMD12以停止多块传输，块数设置为SD_SECCNT并接收响应。此时，CMD12参数自动设置为0x0000_0000。

f. 操作完成
当全块数据发送和CRC状态接收完成时，SD_INFO1中的ACEND位（访问结束）置1以产生中断。将ACEND位清0以读取响应。这是多块写操作的结束。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

39.3.10 多块写入（使用外部定时器的MMC）

图39.15显示了使用外部定时器进行多块写入的示例流程。

RA生态工作室

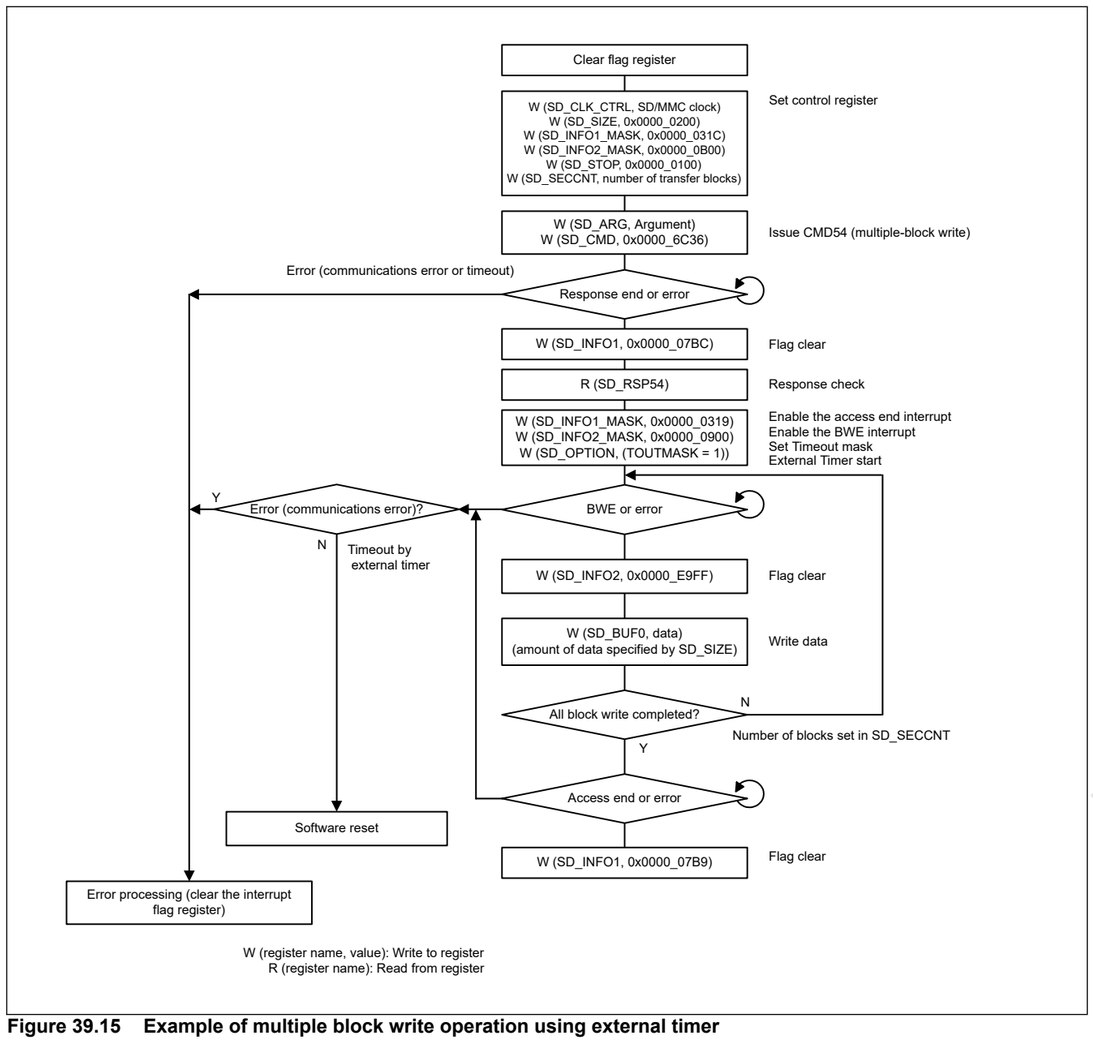

Figure 39.15 Example of multiple block write operation using external timer

39.3.10.1 Multiple block write operation using external timer

The operation of the multiple block write is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).
Set the SEC bit in SD_STOP to 1, and set the number of transfer blocks in SD_SECCNT.

c. Command issue (CMD54)
Set CMD54 Argument in SD_ARG and write 0x0000_6C36 to SD_CMD. CMD54 is issued and the multiple block write operation is started.

d. Response check
On receiving the response, the RSPEND bit (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the RSPEND bit to 0 and read the response from SD_RSP54. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP to 1. Setting the STP bit to 1 also causes CMD12 to be issued

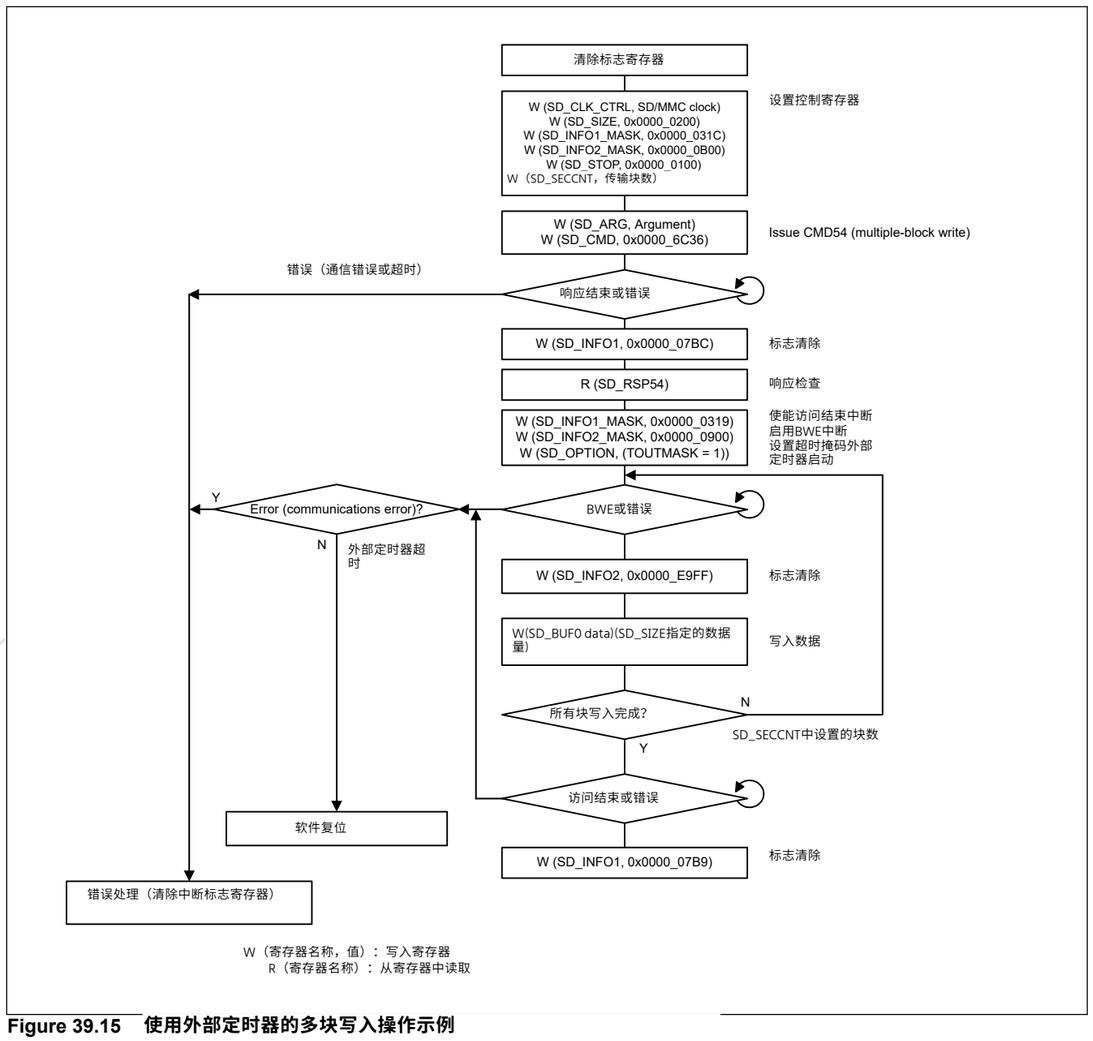

Figure 39.15 使用外部定时器的多块写入操作示例

39.3.10.1 使用外部定时器的多块写操作

多块写入的操作描述如下：

a. 标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置MMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).
将SD_STOP中的SEC位设置为1，并在SD_SECCNT中设置传输块数。

c. 命令问题(CMD54)在SD_ARG中设置CMD54参数并将0x0000_6C36写入SD_CMD。发出CMD54并开始多块写入操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND位（响应结束）置1以产生中断。将RSPEND位清0并从SD_RSP54读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位设置为1来暂停命令序列。将STP位设置为1也会导致发出CMD12

and the response received. If the command sequence is halted because the access end interrupt is enabled, an interrupt is generated by when the ACEND bit (access end) bit in SD_INFO1 sets to 1 on completion of response reception. Clear the ACEND bit to 0 and read the response.

e. Data write and data transmit to MMC
Write 0x0000_0319 to SD_INFO1_MASK to enable the access end interrupt, write 0x0000_0900 to SD_INFO2_MASK to enable the BWE interrupt and set 1 to TOUTMASK of SD_OPTION to inactivate timeout. In addition, start external timer. When SD_BUF0 is ready for the data to be written, the BWE bit in the SD_INFO2 resister is set to 1 to generate an interrupt. Clear the BWE bit to 0 and write the amount of data specified in SD_SIZE to SD_BUF0. When the data write to SD_BUF0 is completed, data is transmitted to the MMC. The CRC status and busy state are received from the MMC. Doing this repeats transfer of the number of blocks set in SD_SECCNT. However, a communication error or timeout might be generated if data is being received while writing to SD_BUF0 is in progress.

f. Operation complete
When all-block data transmit and the CRC status receive are completed, the ACEND bit (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the ACEND bit to 0 to read the response. This is the end of multiple block write operation. Additionally, perform error processing (clear the interrupt flag register) if a communications error or timeout occurs when receiving response. Execute software reset if a timeout by external timer occurs when transmitting data.

39.3.11 IO_RW_DIRECT Command (SD: CMD52)

Figure 39.16 shows an example flow of an IO_DIRECT command (CMD52) operation.

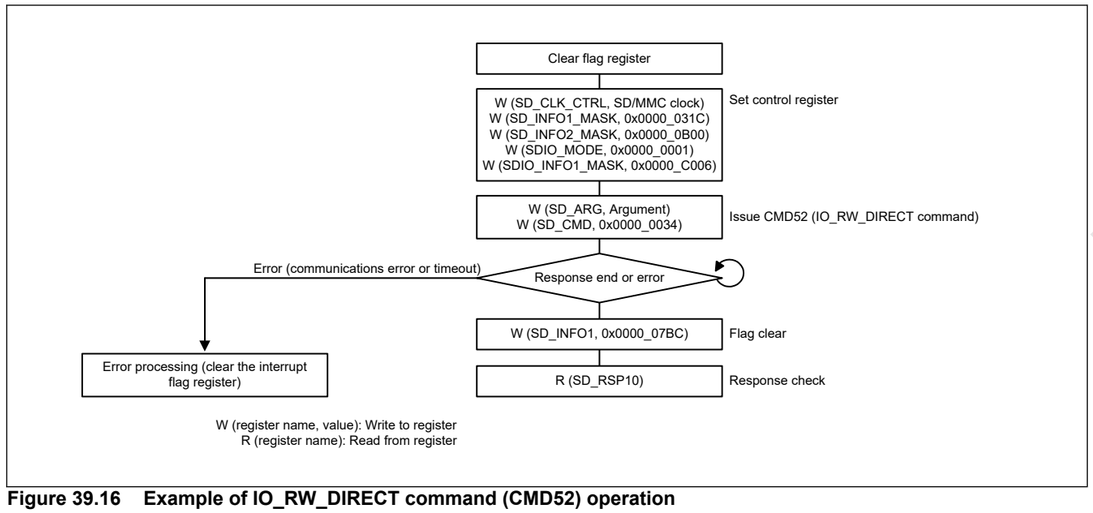

Figure 39.16 Example of IO_RW_DIRECT command (CMD52) operation

39.3.12 IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read)

Figure 39.17 shows an example flow for a CMD53 multiple block read operation.

以及收到的回复。如果由于使能访问结束中断而暂停命令序列，则在完成响应接收时SD_INFO1中的ACEND位（访问结束）位设置为1时产生中断。将ACEND位清0并读取响应。

e. 数据写入和数据传输到MMC
向SD_INFO1_MASK写入0x0000_0319使能访问结束中断，向SD_INFO1_MASK写入0x0000_0900 SD_INFO2_MASK启用BWE中断并将SD_OPTION的TOUTMASK设置为1以禁用超时。另外，启动外部定时器。当SD_BUF0准备好写入数据时，SD_INFO2寄存器中的BWE位设置为1以产生中断。将BWE位清除为0，并将SD_SIZE中指定的数据量写入SD_BUF0。当数据写入SD_BUF0完成后，数据被传输到MMC。从MMC接收CRC状态和忙碌状态。这样做会重复传输SD_SECCNT中设置的块数。但是，如果在写入SD_BUF0时正在接收数据，则可能会产生通信错误或超时。

f. 操作完成
当全块数据发送和CRC状态接收完成时，SD_INFO1中的ACEND位（访问结束）置1以产生中断。将ACEND位清0以读取响应。这是多块写操作的结束。此外，如果在接收响应时发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。如果在传输数据时发生外部定时器超时，则执行软件复位。

39.3.11 IO_RW_DIRECT Command (SD: CMD52)

图39.16显示了IO_DIRECT命令(CMD52)操作的示例流程。

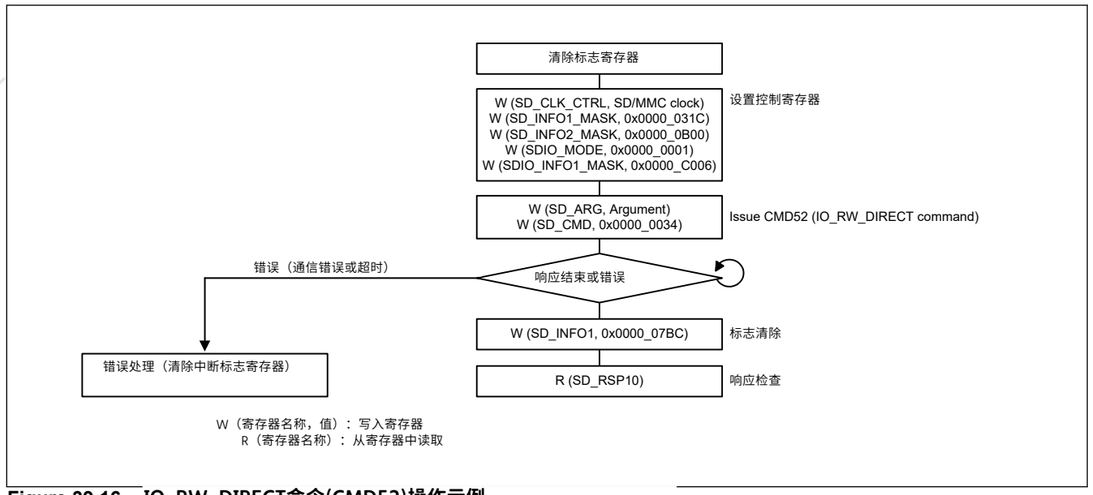

Figure 39.16 IO_RW_DIRECT命令(CMD52)操作示例

39.3.12 IO_RW_EXTENDED命令（SD：CMD53多块读取）

图39.17显示了CMD53多块读取操作的示例流程。

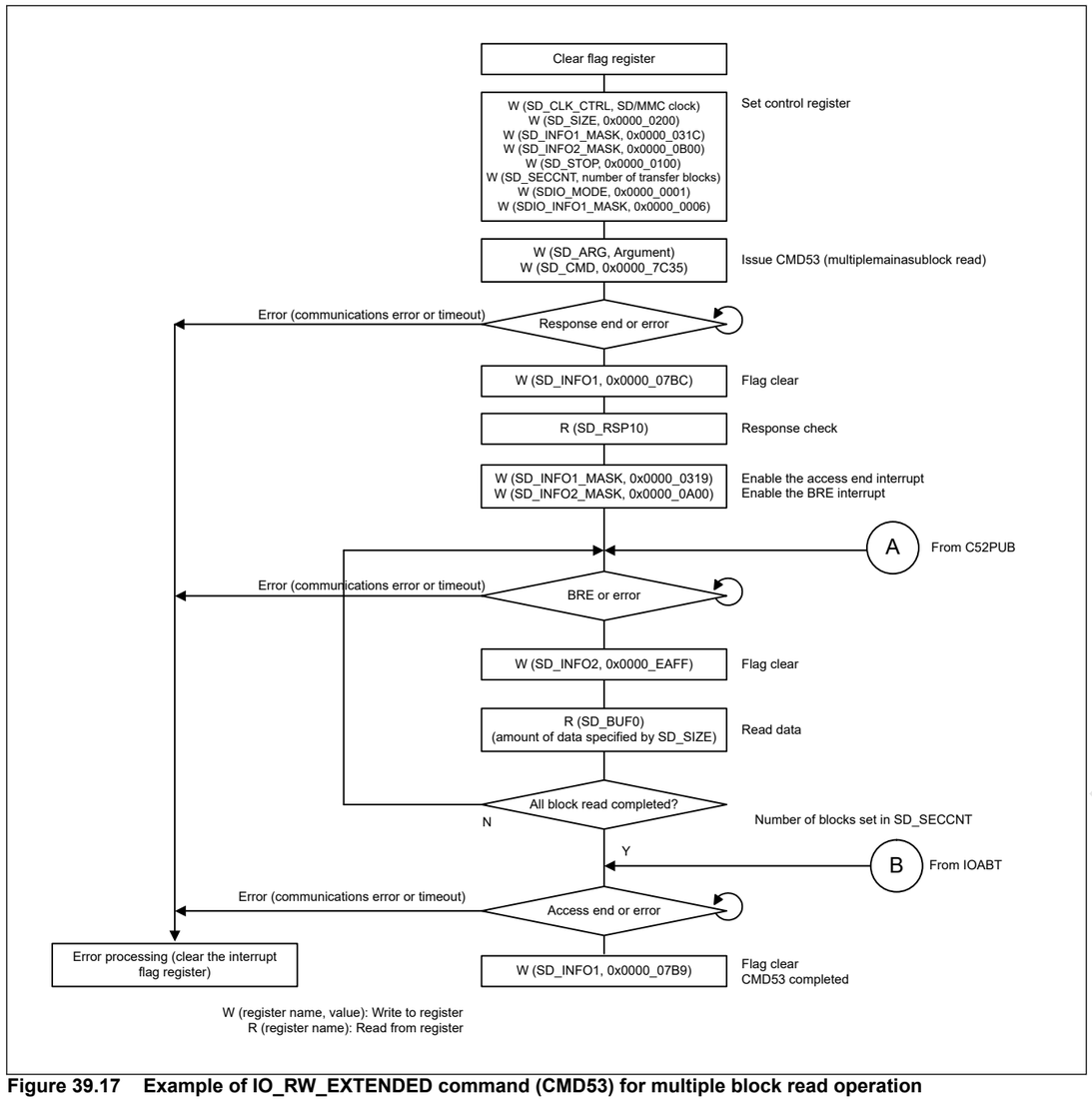

Figure 39.17 Example of IO_RW_EXTENDED command (CMD53) for multiple block read operation

Figure 39.18 shows an example flow when CMD52 (SDIO abort) is issued during a CMD53 multiple block read.

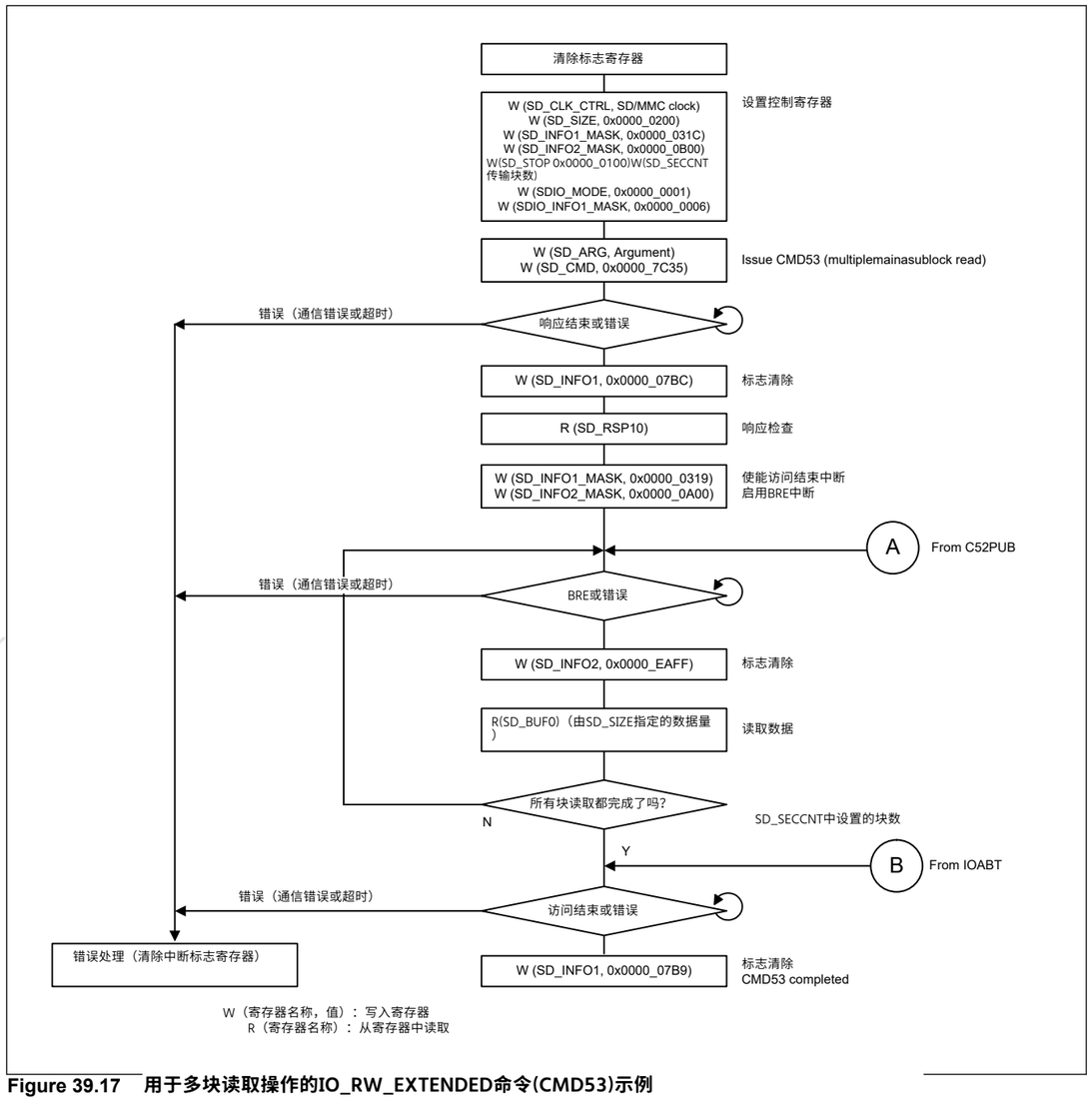

Figure 39.17 用于多块读取操作的IO_RW_EXTENDED命令(CMD53)示例

图39.18显示了在CMD53多块读取期间发出CMD52（SDIO中止）的示例流程。

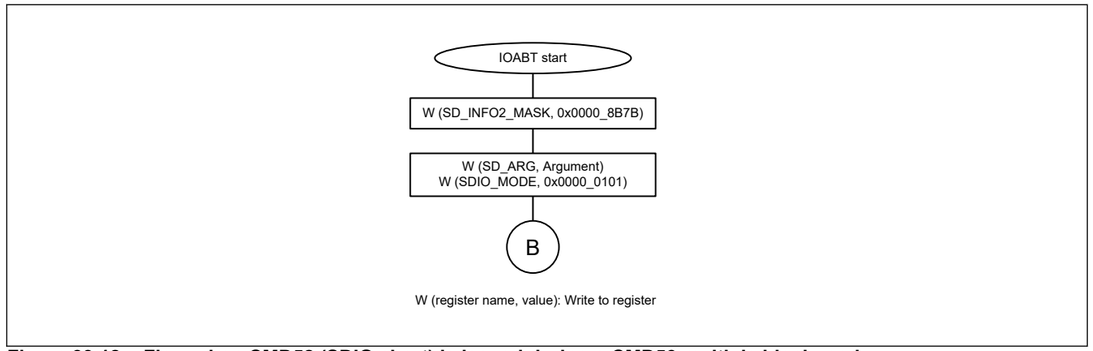

Figure 39.18 Flow when CMD52 (SDIO abort) is issued during a CMD53 multiple block read

Figure 39.19 shows an example flow when CMD52 (SDIO none abort) is issued at a CMD53 multiple block read while the SDHI is in the read wait state.

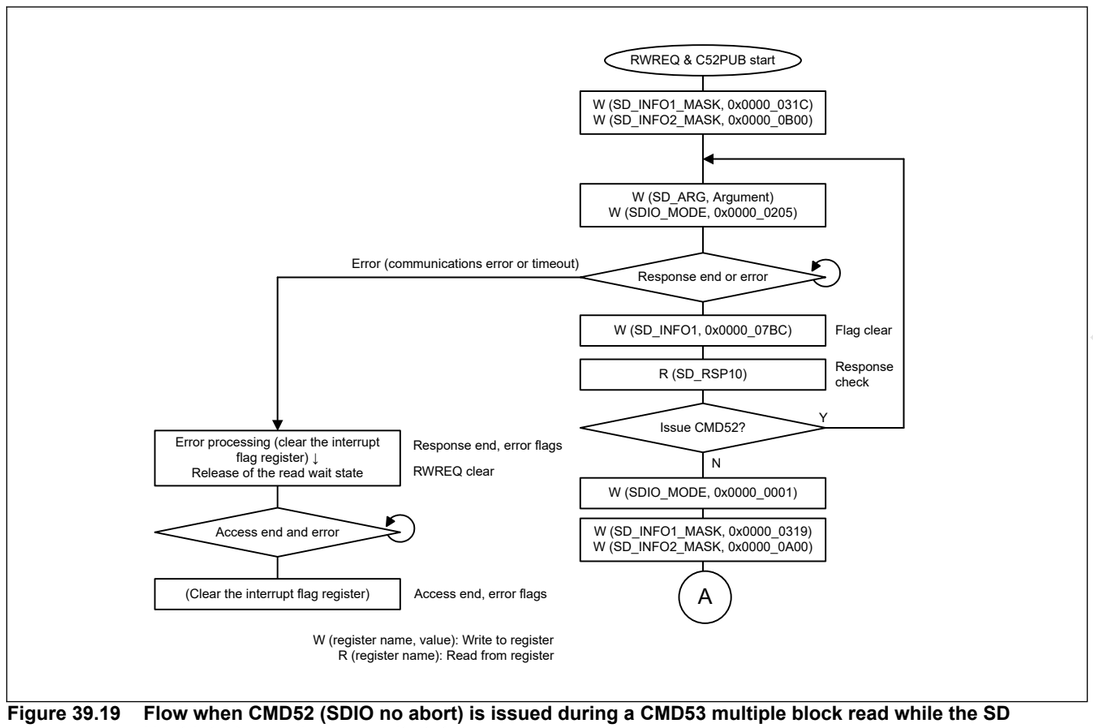

Figure 39.19 Flow when CMD52 (SDIO no abort) is issued during a CMD53 multiple block read while the SD Host Interface is in read wait state

39.3.13 IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write)

Figure 39.20 shows an example flow for a CMD53 multiple block write.

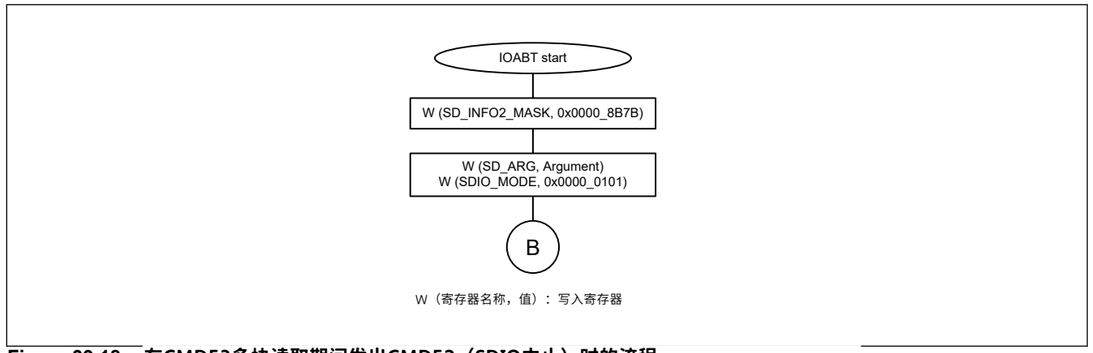

Figure 39.18 在CMD53多块读取期间发出CMD52（SDIO中止）时的流程

图39.19显示了在CMD53多块读取时发出CMD52（SDIO无中止）的示例流程，而SDHI处于读取等待状态。

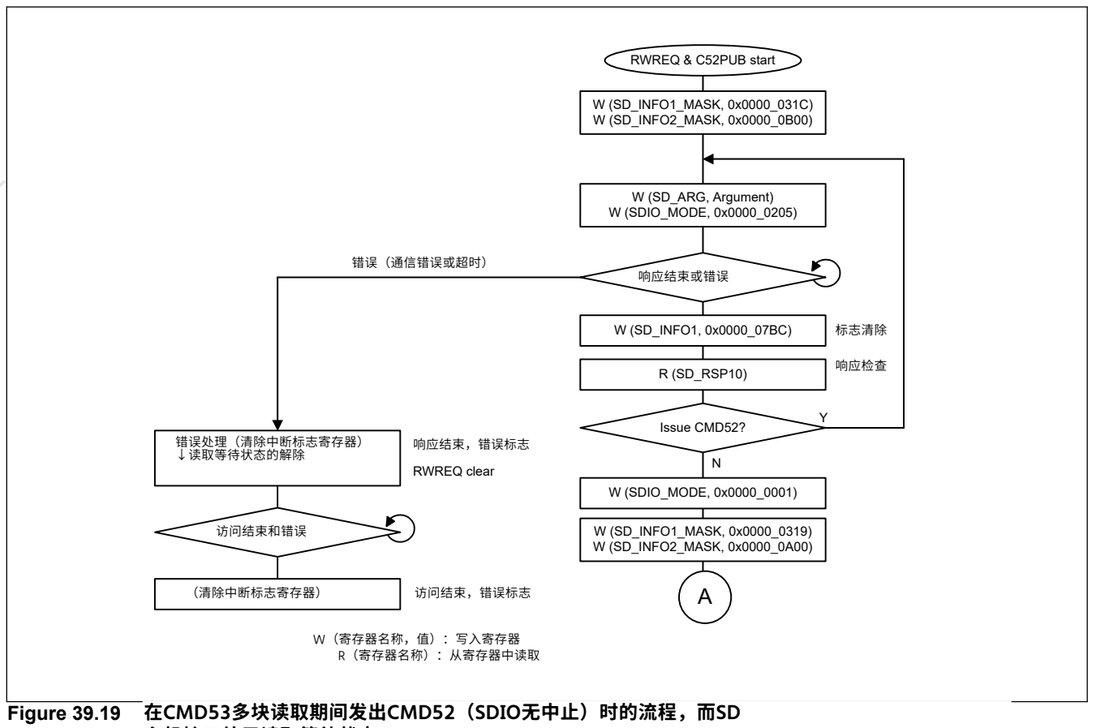

Figure 39.19 在CMD53多块读取期间发出CMD52（SDIO无中止）时的流程，而SD主机接口处于读取等待状态

39.3.13 IO_RW_EXTENDED命令（SD：CMD53多块写入）

图39.20显示了CMD53多块写入的示例流程。

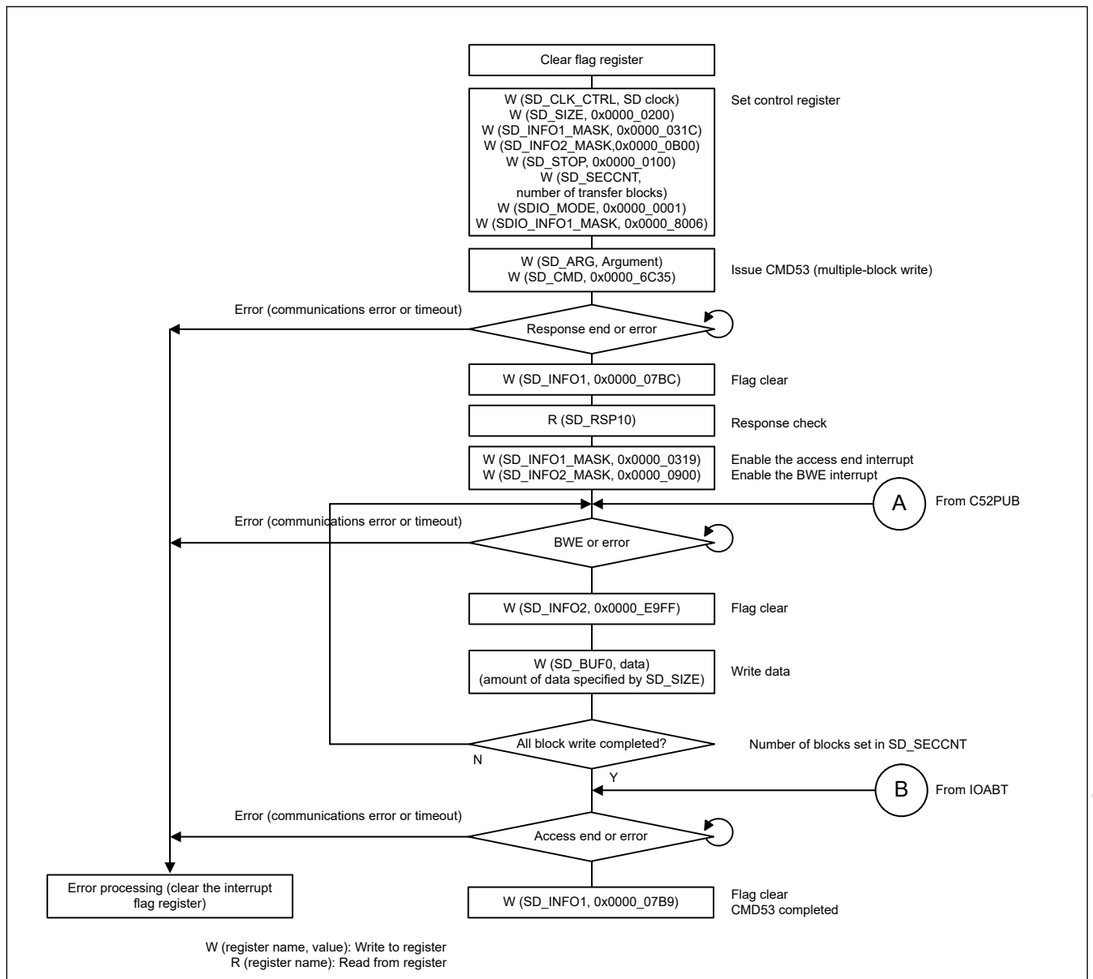

Figure 39.20 Example of IO_RW_EXTENDED command during a CMD53 multiple block write operation

Figure 39.21 shows an example flow when CMD52 (SDIO abort) is issued at CMD53 multiple block write.

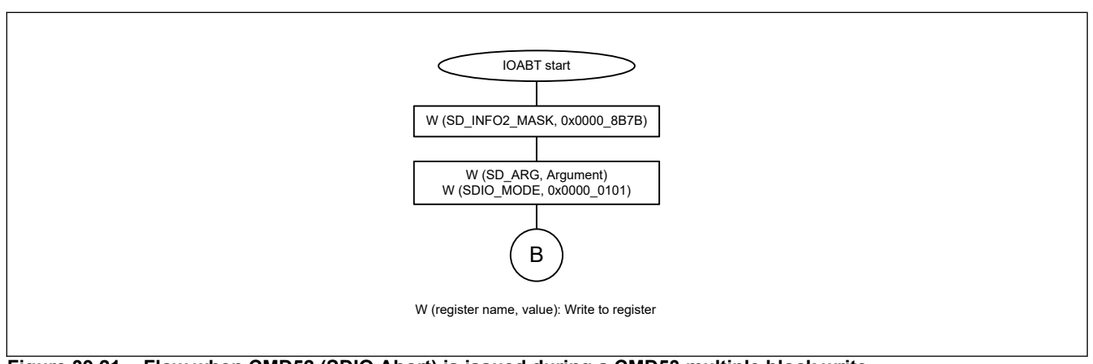

Figure 39.21 Flow when CMD52 (SDIO Abort) is issued during a CMD53 multiple block write

Figure 39.22 shows an example flow when CMD52 (SDIO none abort) is issued at CMD53 multiple block write.

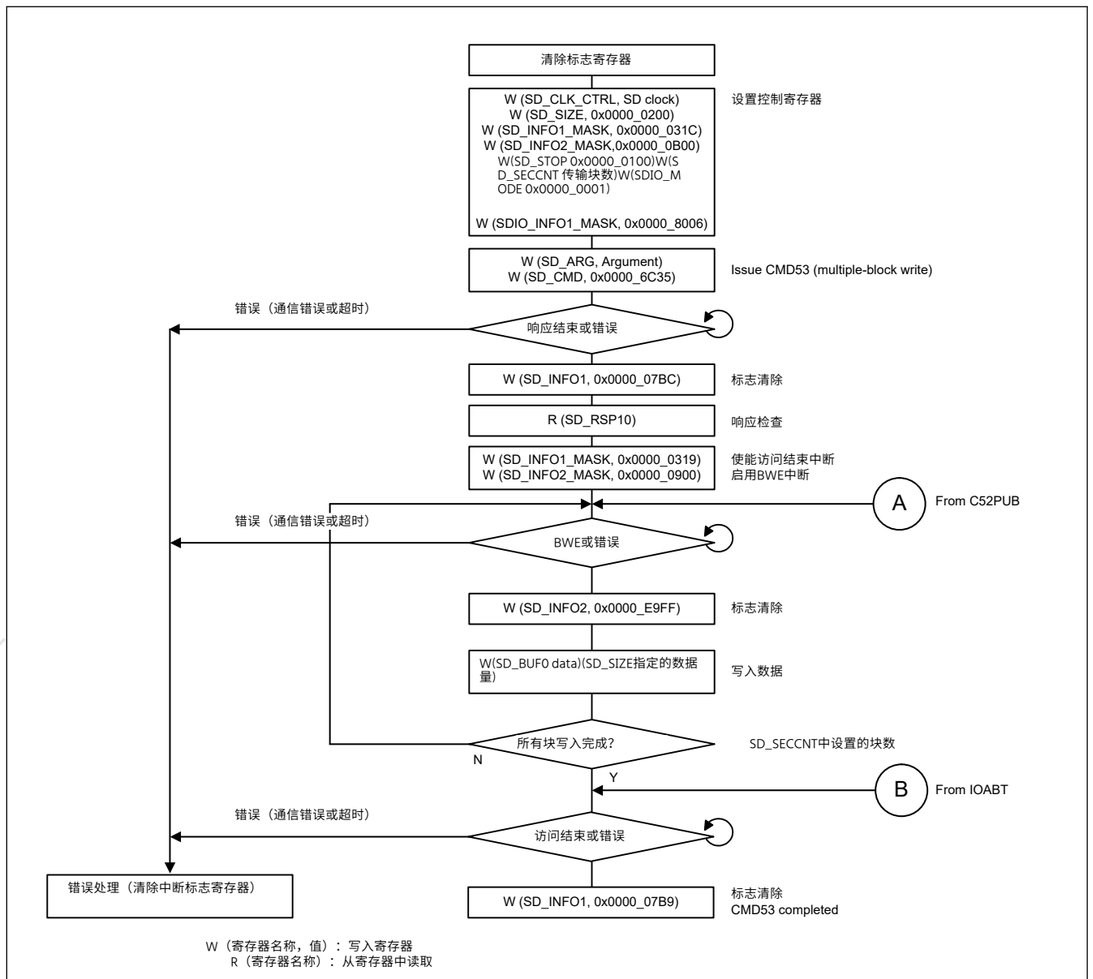

Figure 39.20 CMD53多块写入操作期间的IO_RW_EXTENDED命令示例

图39.21显示了在CMD53多块写入时发出CMD52（SDIO中止）的示例流程。

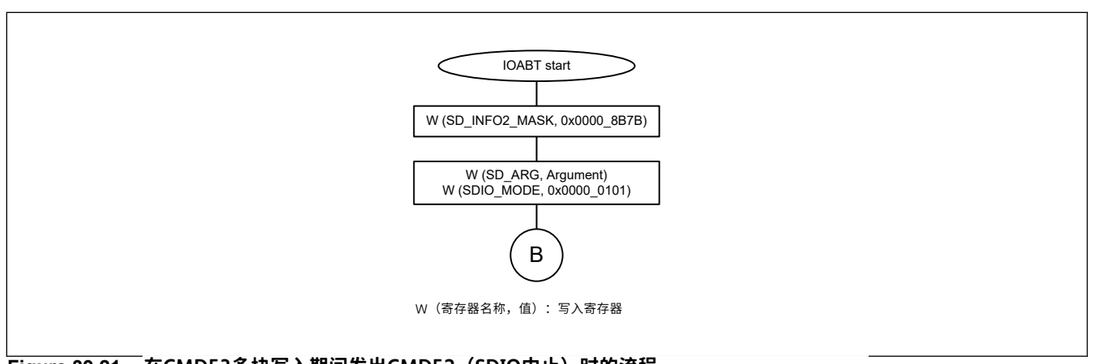

Figure 39.21 在CMD53多块写入期间发出CMD52（SDIO中止）时的流程

图39.22显示了在CMD53多块写入时发出CMD52（SDIO无中止）的示例流程。

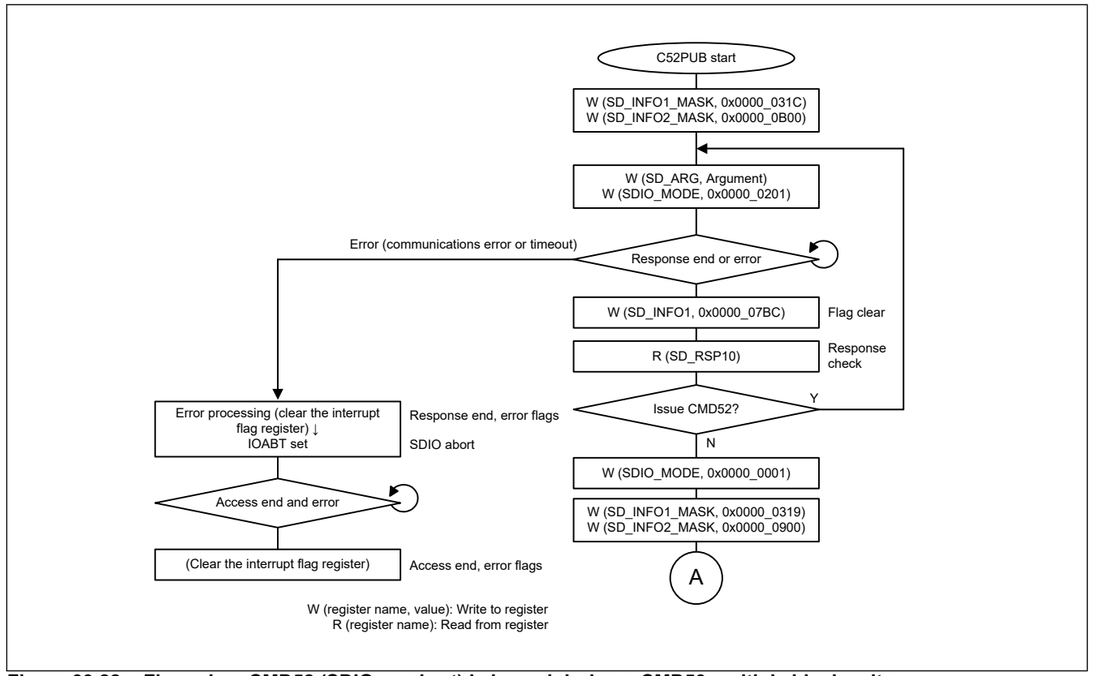

Figure 39.22 Flow when CMD52 (SDIO no abort) is issued during a CMD53 multiple block write

39.3.14 DMA Transfer (SD/MMC)

39.3.14.1 SD_BUF DMA transfer

Figure 39.23 shows an example flow for SD_BUF DMA read when CMD18 multiple block read is issued.

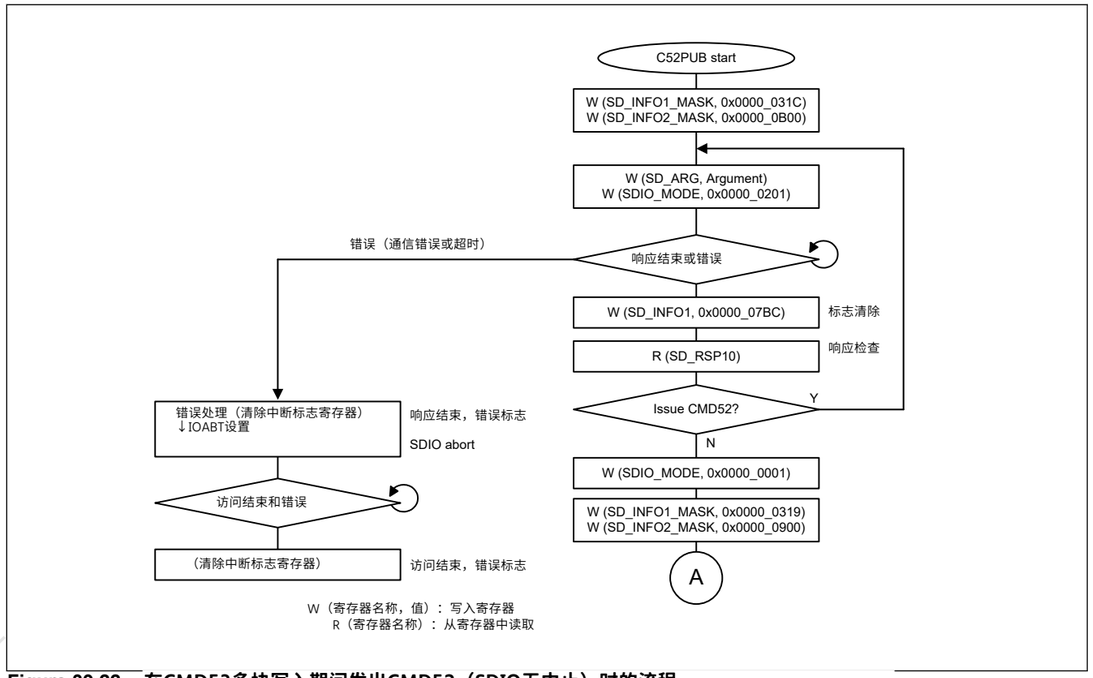

Figure 39.22 在CMD53多块写入期间发出CMD52（SDIO无中止）时的流程

39.3.14 DMA Transfer (SD/MMC)

39.3.14.1 SD_BUF DMA transfer

图39.23显示了发出CMD18多块读取时SD_BUFDMA读取的示例流程。

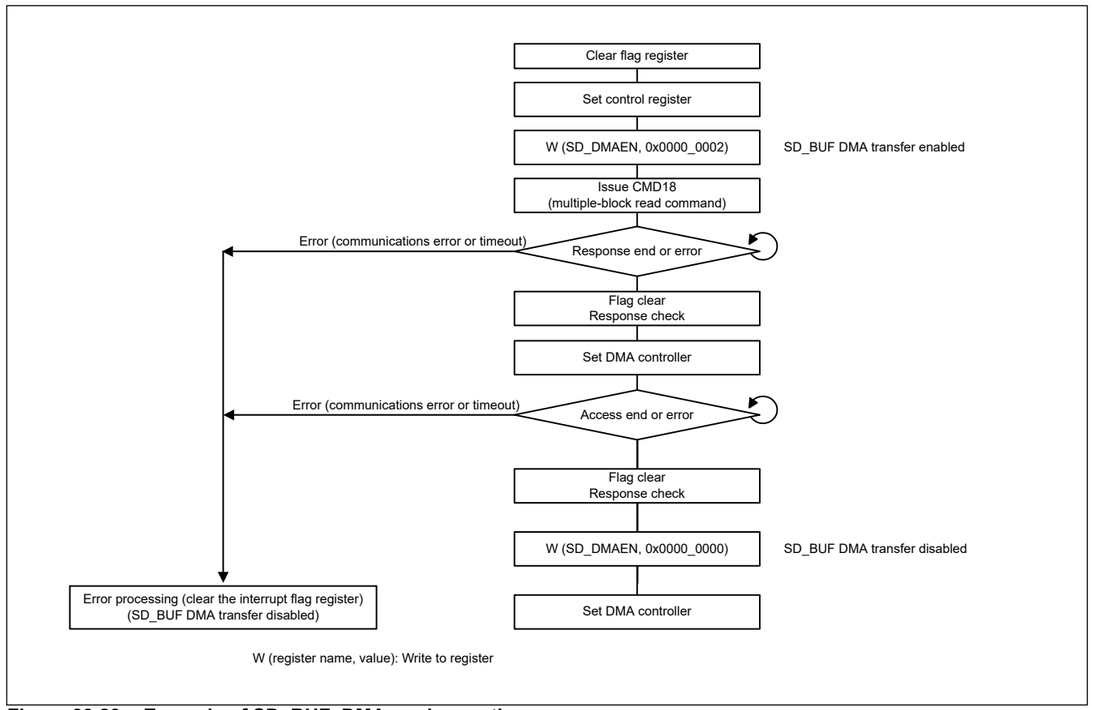

Figure 39.23 Example of SD_BUF_DMA read operation

Figure 39.24 shows an example flow for SD_BUF DMA write when CMD25 multiple block write is issued.

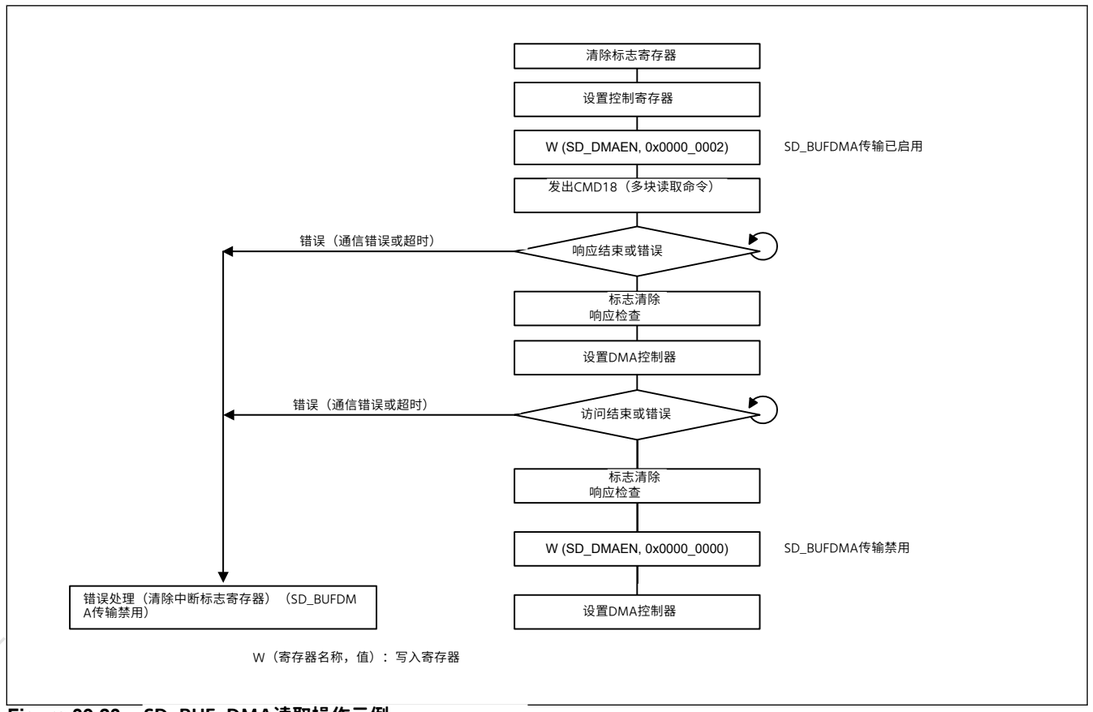

Figure 39.23 SD_BUF_DMA读取操作示例

图39.24显示了发出CMD25多块写入时SD_BUFDMA写入的示例流程。

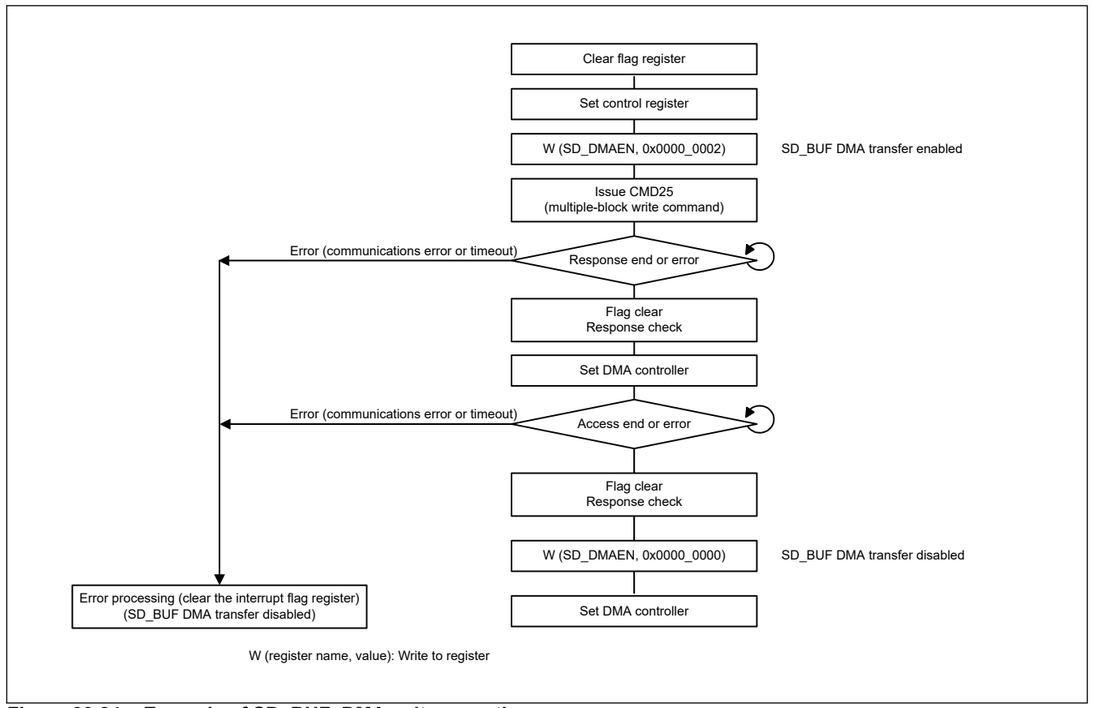

Figure 39.24 Example of SD_BUF_DMA write operation

39.3.15 Example of SD_CMD Register Setting

Table 39.8 and Table 39.9 list the SD_CMD register setting.

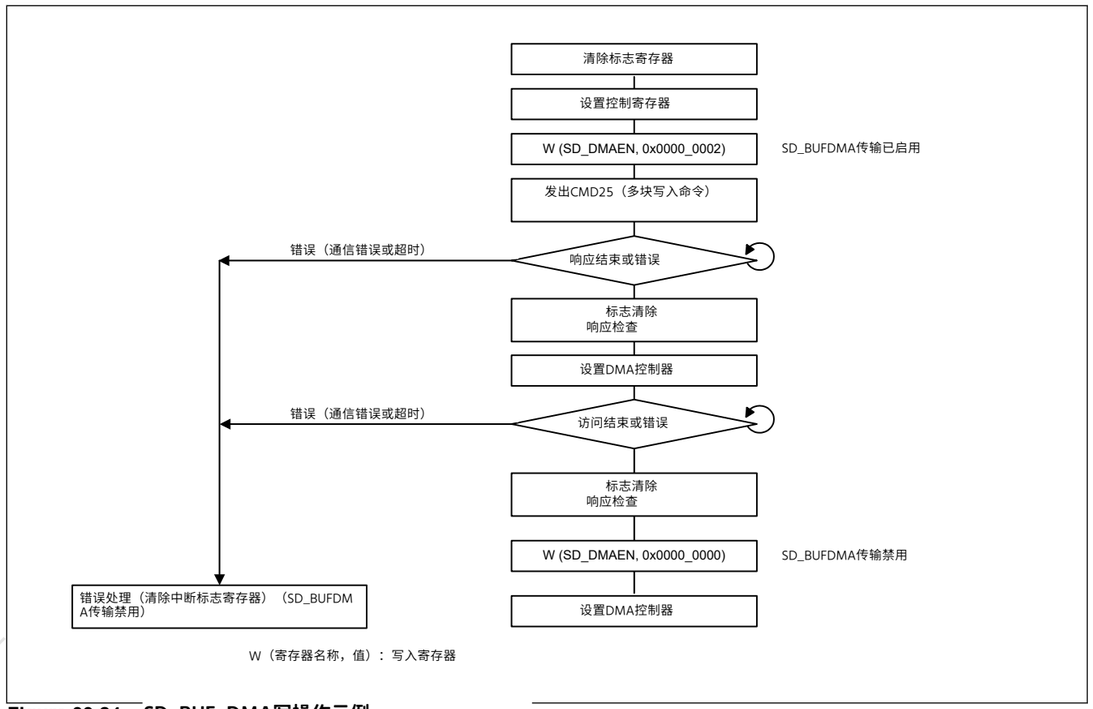

Figure 39.24 SD_BUF_DMA写操作示例

39.3.15 SD_CMD寄存器设置示例

表39.8和表39.9列出了SD_CMD寄存器设置。

Table 39.8 Example SD_CMD register settings for SD (1 of 2)

Type	Commamd	Example SD_CMD register setting	Remark
CMD	CMD0	0x0000_0000	—
	CMD2	0x0000_0002	—
	CMD3	0x0000_0003	—
	CMD4	0x0000_0004	—
	CMD5	0x0000_0705 or 0x0000_0005	—
	CMD6	0x0000_1C06 or 0x0000_0006	—
	CMD7	0x0000_0007	When the card is placed in the deselected state, the response timeout flag sets because there is no response.
	CMD8	0x0000_0408 or 0x0000_0008	—
	CMD9	0x0000_0009	—
	CMD10	0x0000_000A	—
	CMD11	0x0000_040B or 0x0000_000B	—
	CMD12	0x0000_000C	—
	CMD13	0x0000_000D	—
	CMD15	0x0000_000F	—
	CMD16	0x0000_0010	—
	CMD17	0x0000_0011	—
	CMD18	0x0000_0012	With automatic CMD12
	CMD20	0x0000_0514 or 0x0000_0014	—
	CMD24	0x0000_0018	—
	CMD25	0x0000_0019	With automatic CMD12
	CMD27	0x0000_001B	—
	CMD28	0x0000_001C	—
	CMD29	0x0000_001D	—
	CMD30	0x0000_001E	—
	CMD32	0x0000_0020	—
	CMD33	0x0000_0021	—
	CMD38	0x0000_0026	—
	CMD42	0x0000_002A	—
	CMD52	0x0000_0434 or 0x0000_0034	—
	CMD53	0x0000_1C35	Single read
		0x0000_0C35	Single write
		0x0000_7C35	Multiple read
		0x0000_6C35	Multiple write
		0x0000_0035	The value on the left can be set for both single and multiple operations. However, the CF39 bit in SD_ARG must be set as follows. Read: 0 Write: 1
	CMD55	0x0000_0037	—
	CMD56	0x0000_0038	—

Table 39.8 SD的示例SD_CMD寄存器设置（1of2）

Type	Commamd	示例SD_CMD寄存器设置	Remark
CMD	CMD0	0x0000_0000	—
	CMD2	0x0000_0002	—
	CMD3	0x0000_0003	—
	CMD4	0x0000_0004	—
	CMD5	0x0000_0705 or 0x0000_0005	—
	CMD6	0x0000_1C06 or 0x0000_0006	—
	CMD7	0x0000_0007	当卡被置于取消选择状态时，响应超时标志设置，因为没有响应。
	CMD8	0x0000_0408 or 0x0000_0008	—
	CMD9	0x0000_0009	—
	CMD10	0x0000_000A	—
	CMD11	0x0000_040B or 0x0000_000B	—
	CMD12	0x0000_000C	—
	CMD13	0x0000_000D	—
	CMD15	0x0000_000F	—
	CMD16	0x0000_0010	—
	CMD17	0x0000_0011	—
	CMD18	0x0000_0012	带自动CMD12
	CMD20	0x0000_0514 or 0x0000_0014	—
	CMD24	0x0000_0018	—
	CMD25	0x0000_0019	带自动CMD12
	CMD27	0x0000_001B	—
	CMD28	0x0000_001C	—
	CMD29	0x0000_001D	—
	CMD30	0x0000_001E	—
	CMD32	0x0000_0020	—
	CMD33	0x0000_0021	—
	CMD38	0x0000_0026	—
	CMD42	0x0000_002A	—
	CMD52	0x0000_0434 or 0x0000_0034	—
	CMD53	0x0000_1C35	单读
		0x0000_0C35	单写
		0x0000_7C35	多读
		0x0000_6C35	多次写入
		0x0000_0035	左侧的值可以设置为单个和多个操作。但是，SD_ARG中的CF39位必须如下设置。读：0写：1
	CMD55	0x0000_0037	—
	CMD56	0x0000_0038	—

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Table 39.8 Example SD_CMD register settings for SD (2 of 2)

Type	Commamd	Example SD_CMD register setting	Remark
ACMD	ACMD6	0x0000_0046	—
	ACMD13	0x0000_004D	—
	ACMD22	0x0000_0056	—
	ACMD23	0x0000_0057	—
	ACMD41	0x0000_0069	—
	ACMD42	0x0000_006A	—
	ACMD51	0x0000_0073	—

Table 39.8 SD的示例SD_CMD寄存器设置（2个中的2个）

Type	Commamd	示例SD_CMD寄存器设置	Remark
ACMD	ACMD6	0x0000_0046	—
	ACMD13	0x0000_004D	—
	ACMD22	0x0000_0056	—
	ACMD23	0x0000_0057	—
	ACMD41	0x0000_0069	—
	ACMD42	0x0000_006A	—
	ACMD51	0x0000_0073	—

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Table 39.9 Example SD_CMD register settings for MMC

Type	Command	Example SD_CMD register setting	Remark
CMD	CMD0	0x0000_0000	—
	CMD1	0x0000_0701	—
	CMD2	0x0000_0002	—
	CMD3	0x0000_0003	—
	CMD4	0x0000_0004	—
	CMD5	0x0000_0505	—
	CMD6	0x0000_0506	(with response busy)
		0x0000_0406	(without response busy)
	CMD7	0x0000_0007	When the card is placed in the deselected state, the response timeout flag sets because there is no response.
	CMD8	0x0000_1C08	—
	CMD9	0x0000_0009	—
	CMD10	0x0000_000A	—
	CMD12	0x0000_000C	—
	CMD13	0x0000_000D	—
	CMD14	0x0000_1C0E	Required setting: SD_IFMODE = 0x0000_0100 (CRC check is invalid)
	CMD15	0x0000_000F	—
	CMD16	0x0000_0010	—
	CMD17	0x0000_0011	—
	CMD18	0x0000_7C12	Pre-defined
	CMD19	0x0000_0C13	Required setting: SD_IFMODE = 0x0000_0100 (CRC check is invalid)
	CMD21	0x0000_1C15	DDR mode is inhibited
	CMD23	0x0000_0017	—
	CMD24	0x0000_0018	—
	CMD25	0x0000_6C19	Pre-defined
	CMD26	0x0000_0C1A	—
	CMD27	0x0000_001B	—
	CMD28	0x0000_001C	—
	CMD29	0x0000_001D	—
	CMD30	0x0000_001E	—
	CMD31	0x0000_1C1F	—
	CMD35	0x0000_0423	—
	CMD36	0x0000_0424	—
	CMD38	0x0000_0026	—
	CMD39	0x0000_0427	—
	CMD40	0x0000_0428	—
	CMD42	0x0000_002A	—
	CMD49	0x0000_0C31	—
	CMD53	0x0000_7C35	—
	CMD54	0x0000_6C36	—
	CMD55	0x0000_0037	—
	CMD56	0x0000_0038	—

Table 39.9 MMC的示例SD_CMD寄存器设置

Type	Command	示例SD_CMD寄存器设置	Remark
CMD	CMD0	0x0000_0000	—
	CMD1	0x0000_0701	—
	CMD2	0x0000_0002	—
	CMD3	0x0000_0003	—
	CMD4	0x0000_0004	—
	CMD5	0x0000_0505	—
	CMD6	0x0000_0506	(with response busy)
		0x0000_0406	(without response busy)
	CMD7	0x0000_0007	当卡被置于取消选择状态时，响应超时标志设置，因为没有响应。
	CMD8	0x0000_1C08	—
	CMD9	0x0000_0009	—
	CMD10	0x0000_000A	—
	CMD12	0x0000_000C	—
	CMD13	0x0000_000D	—
	CMD14	0x0000_1C0E	所需设置：SD_IFMODE=0x0000_0100（CRC校验无效）
	CMD15	0x0000_000F	—
	CMD16	0x0000_0010	—
	CMD17	0x0000_0011	—
	CMD18	0x0000_7C12	Pre-defined
	CMD19	0x0000_0C13	所需设置：SD_IFMODE=0x0000_0100（CRC校验无效）
	CMD21	0x0000_1C15	DDR模式被禁止
	CMD23	0x0000_0017	—
	CMD24	0x0000_0018	—
	CMD25	0x0000_6C19	Pre-defined
	CMD26	0x0000_0C1A	—
	CMD27	0x0000_001B	—
	CMD28	0x0000_001C	—
	CMD29	0x0000_001D	—
	CMD30	0x0000_001E	—
	CMD31	0x0000_1C1F	—
	CMD35	0x0000_0423	—
	CMD36	0x0000_0424	—
	CMD38	0x0000_0026	—
	CMD39	0x0000_0427	—
	CMD40	0x0000_0428	—
	CMD42	0x0000_002A	—
	CMD49	0x0000_0C31	—
	CMD53	0x0000_7C35	—
	CMD54	0x0000_6C36	—
	CMD55	0x0000_0037	—
	CMD56	0x0000_0038	—

39.4 Usage Notes

39.4.1 SD_BUF Illegal Write Access (SD/MMC)

When writing data to SD_BUF0 after the single block write or multi block write command is issued, the data of the size specified in SD_SIZE must be written.

If the data exceeds the size specified in SD_SIZE is written, the ERR4 bit in SD_INFO2 is set to 1. In addition, the data written to SD_BUF0 might not be transmitted and the SD_CLK_CTRLEN bit in SD_INFO2 is held at the value of 0. If this occurs, clearing the SDRST bit in SOFT_RST to 0 and then restoring its value to 1 clears the SD_CLK_CTRLEN bit to 1.

However, this does not apply to the single byte or three bytes when the SD_SIZE setting is odd, or to the fraction of bytes when the SD_SIZE setting is even (the 2 bytes that are not in a 4-byte unit), because the portion of dummy data writing is regarded as excess data and ignored.

39.4.2 Block Number Constraint for Multiple Block Read (SD)

When performing a multiple block read of one or two blocks, depending on the timing with which the SD card response register is read, the response value might not be read properly. To prevent this, do one of the following:

1. When receiving one or two blocks of data, use single block reading.
2. Read the response to CMD18 from SD_RSP54.

39.4.2.1 Mechanism of incorrect reading

Figure 39.25 shows the processing flows of the SDHI (hardware) operation and software operation when a multiple block read is performed on two blocks. As shown in the incorrect operation in Figure 39.25, when an interrupt is generated on reception of the CMD18 response and the timing with which the SD card response register (SD_RSP10) is read by the interrupt is delayed, the data during the CMD12 response reception or the CMD12 response might be read. This problem does not occur for multiple block reads of three or more blocks, because CMD12 is not issued until the block of data is read. The problem also does not occur for multiple block writes, because the CMD25 response is read before the block of data is sent.

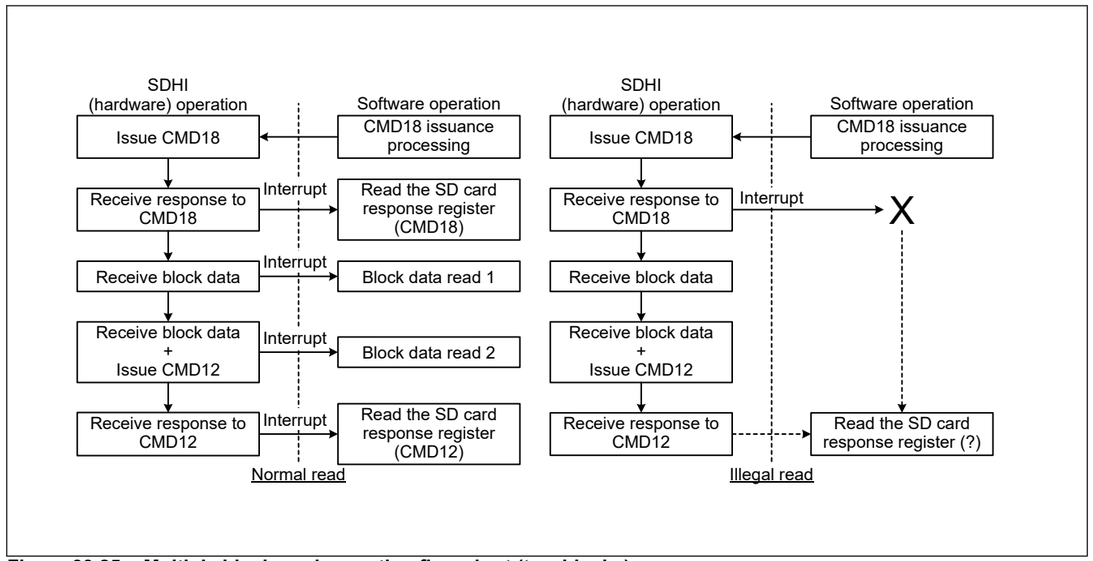

Figure 39.25 Multiple block read operation flow chart (two blocks)

39.4.3 Automatic Control of SD/MMC Clock Output (SD/MMC)

In the SD Card/MMC standard, 74 cycles of SD/MMC clock must be output before initialization of the card. For this reason, use automatic control of SD/MMC clock output after 74 cycles of SD/MMC clock are output. In addition, if

39.4 使用说明

39.4.1 SD_BUF非法写访问(SDMMC)

在发出单块写入或多块写入命令后向SD_BUF0写入数据时，必须写入SD_SIZE中指定大小的数据。

如果写入的数据超过SD_SIZE中指定的大小，则SD_INFO2中的ERR4位设置为1。此外，写入SD_BUF0的数据可能不会被传输，并且SD_INFO2中的SD_CLK_CTRLEN位将保持为0。如果这发生时，将SOFT_RST中的SDRST位清除为0，然后将其值恢复为1，将SD_CLK_CTRLEN位清除为1。

但是，这不适用于SD_SIZE设置为奇数时的单个字节或三个字节，或适用于SD_SIZE设置为偶数时的字节部分（不在4字节单元中的2个字节），因为该部分虚拟数据写入的次数被视为多余数据并被忽略。

39.4.2 多块读取(SD)的块号约束

执行1个或2个块的多块读取时，根据读取SD卡响应寄存器的时序，可能无法正确读取响应值。为防止这种情况，请执行以下操作之一：

1、接收一两块数据时，使用单块读取。

2.从SD_RSP54读取对CMD18的响应。

39.4.2.1 误读机制

图39.25显示了对两个块执行多块读取时SDHI（硬件）操作和软件操作的处理流程。如图39.25中的错误操作所示，当接收到CMD18响应时产生中断并且中断读取SD卡响应寄存器(SD_RSP10)的时序延迟时，CMD12响应接收期间的数据或可能会读取CMD12响应。对于三个或更多块的多个块读取不会出现此问题，因为在读取数据块之前不会发出CMD12。多次块写入也不会出现该问题，因为在发送数据块之前读取了CMD25响应。

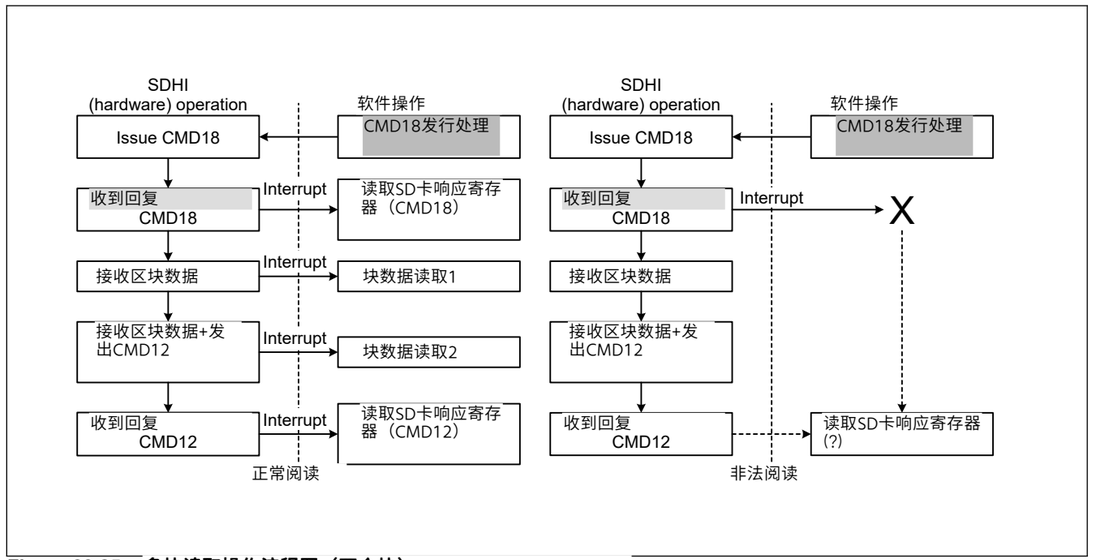

Figure 39.25 多块读取操作流程图（两个块）

39.4.3 SDMMC时钟输出(SDMMC)的自动控制

在SD卡MMC标准中，必须在卡初始化之前输出74个周期的SDMMC时钟。为此，在输出SDMMC时钟的74个周期后使用SDMMC时钟输出的自动控制。此外，如果

automatic control of SD/MMC clock output was in use, SD/MMC clock output is stopped on completion of the sequence for a communications error or timeout. When state transitions within the SD card/MMC are necessary after completion of the sequence, release automatic control of SD/MMC clock output and restart supply of the SD/MMC clock to the SD card/MMC.

39.4.4 Control of the C52PUB Setting for Multiple Block Write (SD)

If the C52PUB bit in SDIO_MODE is set to 1 during a sequence of multiple block write because of CMD53, CMD52 is not issued until SD_BUF becomes empty. For this reason, set the C52PUB bit after suspending writing to SD_BUF by using one of the following procedures, as appropriate:

(a) When DMA transfer is not in use

1. Before setting the C52PUB bit, suspend writing to SD_BUF by making the setting in SD_INFO2 to disable BWE interrupts.
2. Set the C52PUB bit in SDIO_MODE to 1 (so that CMD52 is issued when SD_BUF becomes empty).
3. After the RSPEND interrupt processing in SD_INFO1 because the issuing of CMD52 is completed, restart writing to SD_BUF by making the setting in SD_INFO2 to enable BWE interrupts.

(b) When DMA transfer is in use

1. Every time DMA transfer of the value set in SD_SIZE × n blocks (where n = 1, 2,…) proceeds, suspend writing to SD_BUF by DMA transfer before the C52PUB bit is set.
2. Set the C52PUB bit in SDIO_MODE to 1 (so that CMD52 is issued when SD_BUF becomes empty).
3. After the RSPEND interrupt processing in SD_INFO1 because the issuing of CMD52 is completed, restart writing to SD_BUF by DMA transfer.

39.4.5 Notes on SD_CLK_CTRL Register Settings (SD/MMC)

When the SD_CLK_CTRLEN bit in SD_INFO2 is 0, SD_CLK_CTRL cannot be written to. Before writing to SD_CLK_CTRL, you must check that the SD_CLK_CTRLEN bit in SD_INFO2 is 1.

39.4.6 Specification Limitations

1. The Suspend/Resume operation of the SDIO is not supported.
2. The SPI bus is not supported. (SD/MMC)
3. The shared bus and 8-bit SD bus of the embedded SDIO are not supported.
4. Stream transfer of MMC is not supported.
5. High Priority Interrupt (HPI) of MMC is not supported.
6. Boot Operation/Alternative Boot Operation of MMC is not supported.
7. Open-ended multiple block transfer of MMC is not supported.

39.4.7 STP Bit Setting during Multiple Block Read (SD/MMC)

During execution of multiple block read with automatic CMD12 execution by setting the SEC bit in SD_STOP to 1, even if the STP bit in SD_STOP is set to 1 to forcibly stop the execution, the command sequence might not stop depending on the timing of setting the STP bit.

To avoid this, when setting the STP bit in SD_STOP to 1 during multiple block transfer, clear the SEC bit in SD_STOP to 0 at the same time. (Even when the SD_CLK_CTRLEN bit in SD_INFO2 is 0, change the SEC bit from 1 to 0.)

When the command sequence does not stop because the SEC bit was not cleared to 0, the command sequence can be stopped by clearing the SDRST bit in SOFT_RST to 0.

When forcibly terminating the CMD53 multiple block transfer through the IOABT bit in SDIO_MODE, you must leave the SEC bit in SD_STOP as 1.

SDMMC时钟输出的自动控制正在使用中，SDMMC时钟输出在完成通信错误或超时的序列时停止。当序列完成后需要SD卡MMC内的状态转换时，解除SDMMC时钟输出的自动控制并重新开始向SD卡MMC提供SDMMC时钟。

39.4.4 控制多块写入(SD)的C52PUB设置

如果SDIO_MODE中的C52PUB位由于CMD53而在多个块写入序列期间设置为1，则在SD_BUF变空之前不会发出CMD52。因此，在暂停写入SD_BUF后，根据需要使用以下过程之一设置C52PUB位：

(a)不使用DMA传输时

1.在设置C52PUB位之前，通过在SD_INFO2中进行设置以禁用BWE中断来暂停写入SD_BUF。

2.将SDIO_MODE中的C52PUB位设置为1（以便当SD_BUF为空时发出CMD52）。

3.在SD_INFO1中的RSPEND中断处理后，因为CMD52的发布完成，通过在SD_INFO2中进行设置来重新开始写入SD_BUF以启用BWE中断。

(b)使用DMA传输时

1.每次对SD_SIZE×n块中设置的值（其中n=1 2 …）进行DMA传输时，在C52PUB位置位之前暂停通过DMA传输对SD_BUF的写入。

2.将SDIO_MODE中的C52PUB位设置为1（以便当SD_BUF为空时发出CMD52）。

3.SD_INFO1中的RSPEND中断处理后，因为CMD52的下发完成，通过DMA传输重新开始写入SD_BUF。

39.4.5 SD_CLK_CTRL寄存器设置注意事项(SDMMC)

当SD_INFO2中的SD_CLK_CTRLEN位为0时，无法写入SD_CLK_CTRL。在写信之前SD_CLK_CTRL，必须检查SD_INFO2中的SD_CLK_CTRLEN位是否为1。

39.4.6 规格限制

1、不支持SDIO的SuspendResume操作。

2.不支持SPI总线。(标清MMC)

3、不支持嵌入式SDIO的共享总线和8位SD总线。

4.不支持MMC的流传输。

5.不支持MMC的高优先级中断(HPI)。

6.BootOperationAlternativeBootOperation不支持MMC。

7.不支持MMC的开放式多块传输。

39.4.7 多块读取(SDMMC)期间的STP位设置

在通过将SD_STOP中的SEC位设置为1并通过自动CMD12执行执行多块读取时，即使将SD_STOP中的STP位设置为1以强制停止执行，命令序列也可能不会停止，具体取决于设置STP位。

为避免这种情况，在多块传输期间将SD_STOP中的STP位设置为1时，同时将SD_STOP中的SEC位清除为0。（即使SD_INFO2中的SD_CLK_CTRLEN位为0，也将SEC位从1更改为0。）

当由于SEC位未清0而导致命令序列未停止时，可通过将SOFT_RST中的SDRST位清0来停止命令序列。

当通过SDIO_MODE中的IOABT位强制终止CMD53多块传输时，必须离开SD_STOP中的SEC位为1。

39.4.8 Register Setting Notes

1. All registers in section 39.2. Register Descriptions are accessed in 32-bit access-only.
2. When setting registers, set them after the I/O Port Register setting.

39.4.8 注册设置注意事项

1.第39.2节中的所有寄存器。寄存器描述只能以32位访问方式访问。
2.设置寄存器时，请在IOPortRegister设置后进行设置。

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40. Cyclic Redundancy Check (CRC)

40.1 Overview

The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.

Table 40.1 lists the CRC calculator specifications and Figure 40.1 shows a block diagram.

Table 40.1 CRC calculator specifications

Item	Description	
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for data in 8n-bit units (where n is a natural number)	CRC code generated for data in 32n-bit units (where n is a natural number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials that is selectable: [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	One of two generating polynomials that is selectable: [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
TrustZone Filter	Security attribution can be set	

Note 1. This function cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

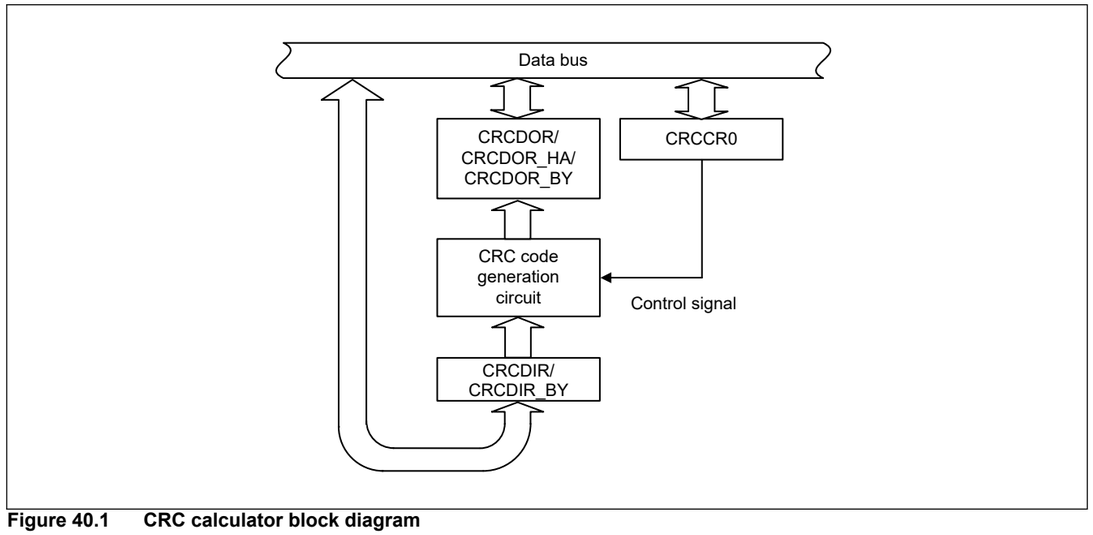


Figure 40.1 CRC calculator block diagram

40.2 Register Descriptions

40. 循环冗余校验(CRC)

40.1 Overview

循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种CRC生成多项式。

表40.1列出了CRC计算器规格，图40.1显示了框图。

Table 40.1 CRC计算器规格

Item	Description	
数据大小	8-bit	32-bit
CRC计算数据*1	为8n位单元中的数据生成的CRC码（其中n是自然数）	为32n位单元中的数据生成的CRC码（其中n是自然数）
CRC处理器单元	在8位上并行执行的操作	在32位上并行执行的操作
CRC生成多项式	可选择的三个生成多项式之一：[8位CRC]● [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT).	可选择的两个生成多项式之一：[32位CRC]● $X^{11} +$ $X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C).
CRC计算切换	CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信	
Module-stop function	可设置模块停止状态以降低功耗	
TrustZone Filter	可设置安全属性	

注1.此功能不能除以CRC计算中使用的数据。以8位或32位为单位写入数据。

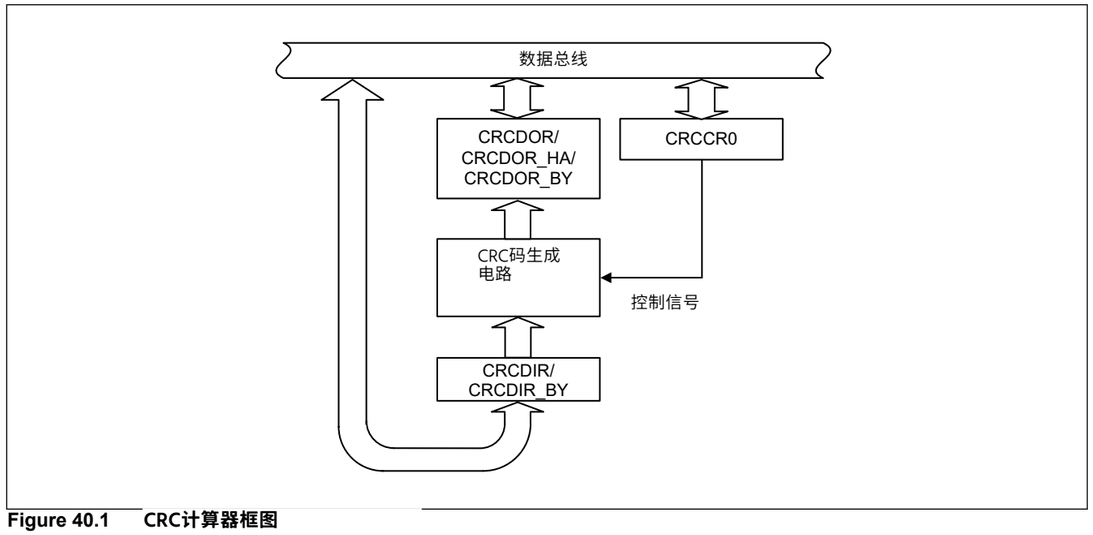


Figure 40.1 CRC计算器框图

40.2 注册说明

40.2.1 CRCCR0 : CRC Control Register 0

Base address: CRC = 0x4010_8000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC Generating Polynomial Switching 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Others: No calculation is executed	R/W
5:3	—	These bits are read as 0. The write value should be 0.	R/W
6	LMS	CRC Calculation Switching 0: Generate CRC code for LSB-first communication 1: Generate CRC code for MSB-first communication	R/W
7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear 0: No effect 1: Clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register	W

GPS[2:0] bits (CRC Generating Polynomial Switching)

The GPS[2:0] bits select the CRC generating polynomial.

LMS bit (CRC Calculation Switching)

The LMS bit selects the bit order of generated CRC code. Transmit the lower byte of the CRC code first for LSB-first communication and the upper byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 40.3. Operation.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear)

Write 1 to the DORCLR bit to set the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0x00000000. This bit is read as 0. Only 1 can be written to it.

40.2.2 CRCDIR/CRCDIR_BY : CRC Data Input Register

Base address: CRC = 0x4010_8000

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC input data The CRCDIR register is a 32-bit read/write register to write data for CRC-32 or CRC-32C calculation. The CRCDIR_BY (CRCDIR[31:24]) is an 8-bit read/write register to write data for CRC-8, CRC-16, or CRC-CCITT calculation.	R/W

40.2.1 CRCCR0:CRC控制寄存器0

Base address: CRC = 0x4010_8000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DORCLR	LMS	—	—	—	GPS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	GPS[2:0]	CRC生成多项式切换 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 其他：不执行计算	R/W
5:3	—	这些位被读取为0。写入值应为0。	R/W
6	LMS	CRC计算切换 0：生成LSB优先通信的CRC代码1：生成MSB优先通信的CRC代码	R/W
7	DORCLR	CRCDORCRCDOR_HACRCDOR_BY寄存器清零 0：无效1：清除CRCDORCRCDOR_HACRCDOR_BY寄存器	W

GPS[2:0]位（CRC生成多项式切换）

GPS[2:0]位选择CRC生成多项式。

LMS位（CRC计算切换）

LMS位选择生成的CRC码的位顺序。对于LSB在先的通信，首先发送CRC码的低字节，对于MSB在先的通信，首先发送高字节。有关发送和接收CRC码的详细信息，请参阅第40.3节。手术。

DORCLR位（CRCDORCRCDOR_HACRCDOR_BY寄存器清零）

将1写入DORCLR位以将CRCDORCRCDOR_HACRCDOR_BY寄存器设置为0x00000000。该位读为0。只能写入1。

40.2.2 CRCDIRCRCDIR_BY:CRC数据输入寄存器

Base address: CRC = 0x4010_8000

Offset address: 0x04

Bit position:	31																													0
Bit field:																														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC输入数据 CRCDIR寄存器是一个32位读写寄存器，用于写入数据以进行CRC-32或CRC-32C计算。CRCDIR_BY(CRCDIR[31:24])是一个8位读写寄存器，用于为CRC-8、CRC-16或CRC-CCITT计算写入数据。	R/W

40.2.3 CRCDOR/CRCDOR_HA/CRCDOR_BY : CRC Data Output Register

Base address: CRC = 0x4010_8000

Offset address: 0x08

Bit position:	31																												0
Bit field:																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC output data The CRCDOR register is a 32-bit read/write register for CRC-32 or CRC-32C calculation. The CRCDOR_HA (CRCDOR[31:16]) register is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. The CRCDOR_BY (CRCDOR[31:24]) register is an 8-bit read/write register for CRC-8 calculation. Because its initial value is 0x00000000, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculations using a value other than the initial value. Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0x00000000, there is no CRC error.	R/W

40.3 Operation

40.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB-first or MSB-first transfer.

The following examples show CRC code generation for input data (0xF0) using the 16-bit CRC-CCITT generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When a 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

Figure 40.2 and Figure 40.3 show the LSB-first and MSB-first data transmission examples respectively. Figure 40.4 and Figure 40.5 show the LSB-first and MSB-first data reception examples.

40.2.3 CRCDORCRCDOR_HACRCDOR_BY:CRC数据输出寄存器

Base address: CRC = 0x4010_8000

Offset address: 0x08

Bit position:	31																												0
Bit field:																													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC输出数据 CRCDOR寄存器是一个32位读写寄存器，用于CRC-32或CRC-32C计算。CRCDOR_HA(CRCDOR[31:16])寄存器是用于CRC-16或 CRC-CCITT calculation. CRCDOR_BY(CRCDOR[31:24])寄存器是一个用于CRC-8计算的8位读写寄存器。由于其初始值为0x00000000，因此重写CRCDORCRCDOR_HACRCDOR_BY寄存器以使用初始值以外的值执行计算。写入CRCDIRCRCDIR_BY寄存器的数据经过CRC计算，结果存储在CRCDORCRCDOR_HACRCDOR_BY寄存器中。如果在传输数据之后计算CRC码，结果为0x00000000，则没有CRC错误。	R/W

40.3 Operation

40.3.1 基本操作

CRC计算器生成用于LSB优先或MSB优先传输的CRC代码。

以下示例显示了使用16位CRC-CCITT生成多项式(X16+X12+X5+1)为输入数据(0xF0)生成CRC码。在这些示例中，CRC数据输出寄存器(CRCDOR_HA)的值在CRC计算之前被清除。

当使用8位CRC（多项式X8+X2+X+1）时，CRC码的有效位在CRCDOR_BY。使用32位CRC时，在CRCDOR中获取CRC码的有效位。

图40.2和图40.3分别显示了LSB-first和MSB-first数据传输示例。图40.4和图40.5显示了LSB优先和MSB优先的数据接收示例。

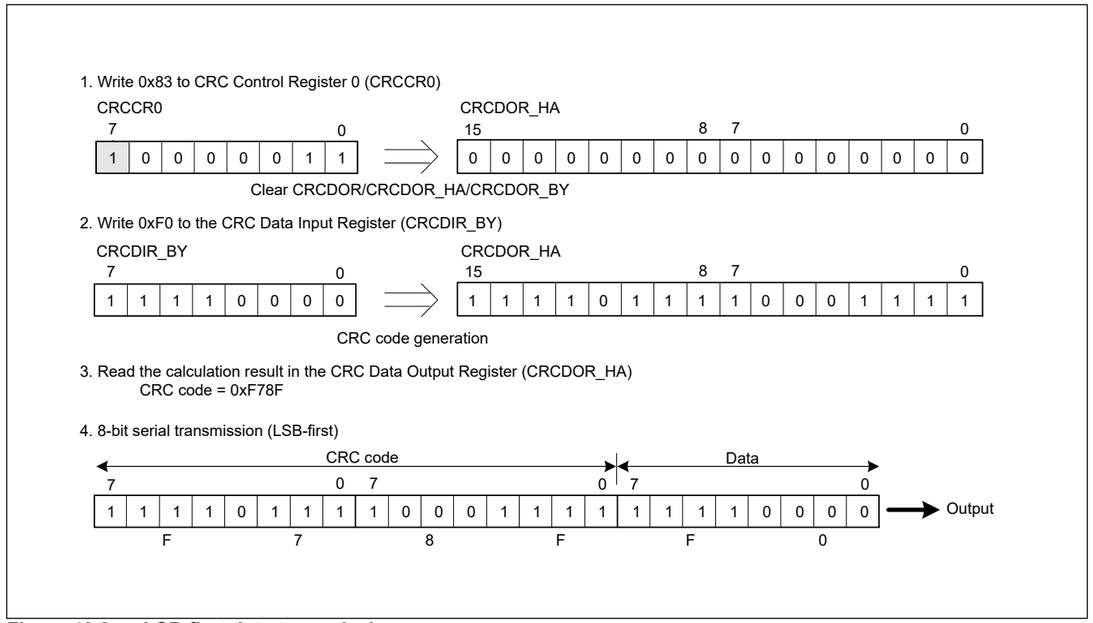


Figure 40.2 LSB-first data transmission

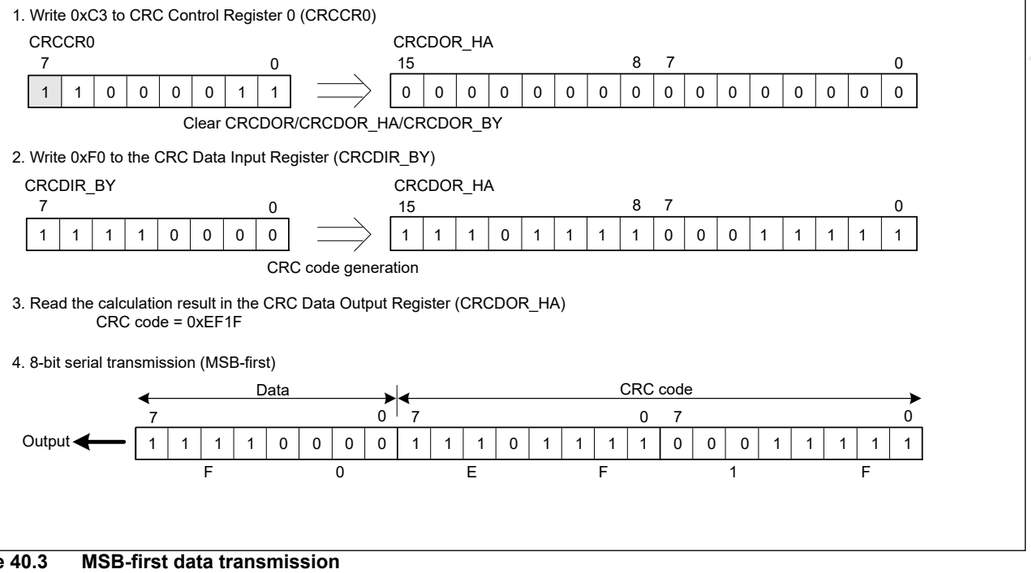


Figure 40.3 MSB-first data transmission

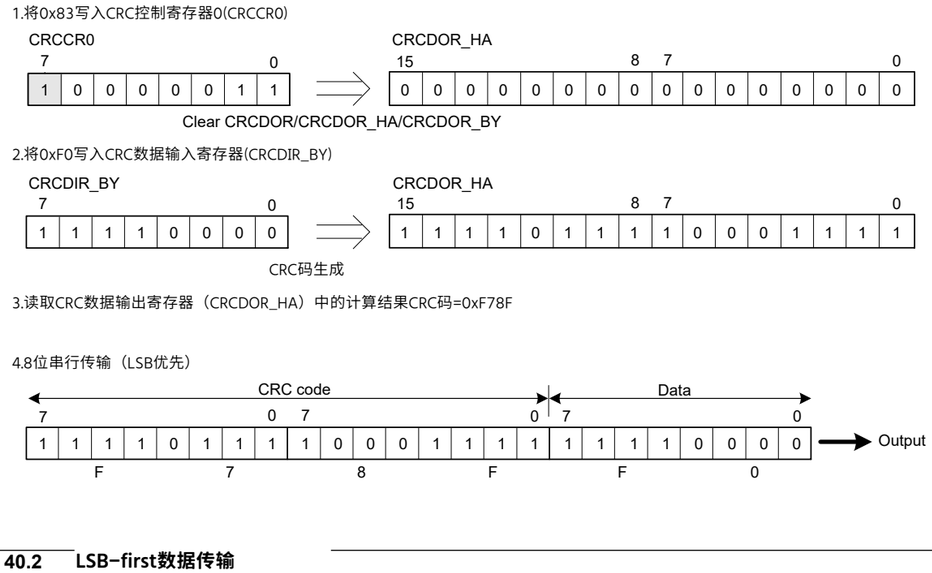


Figure 40.2 LSB-first数据传输

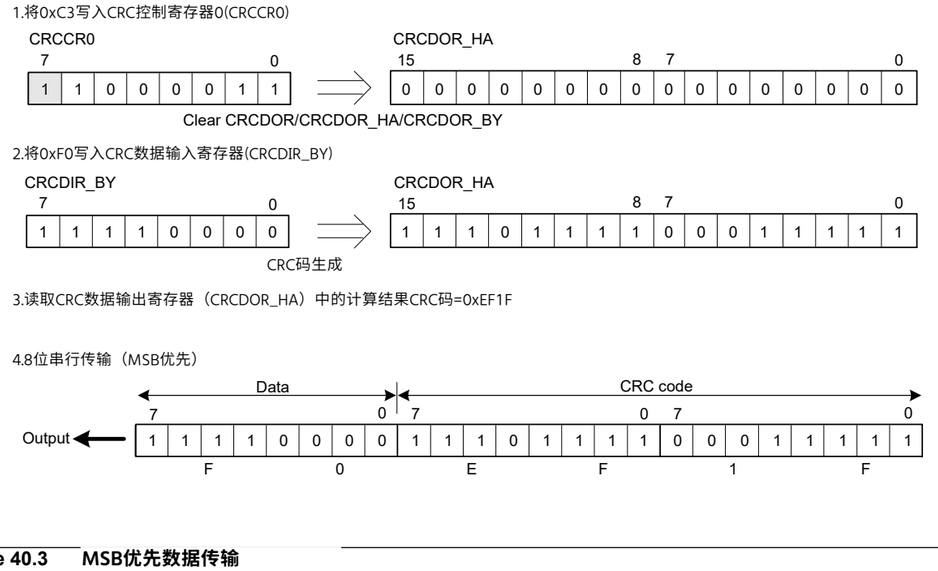


Figure 40.3 MSB优先数据传输

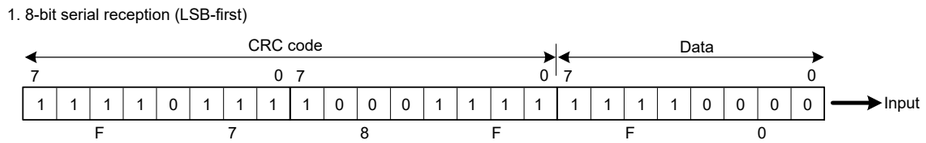


Figure 40.4 LSB-first data reception

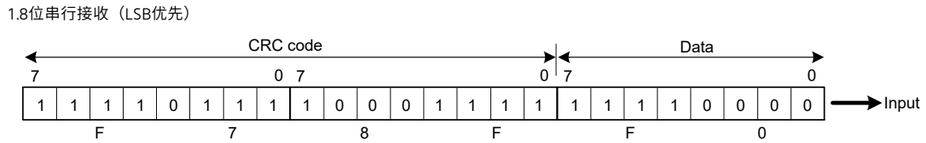


Figure 40.4 LSB-first数据接收

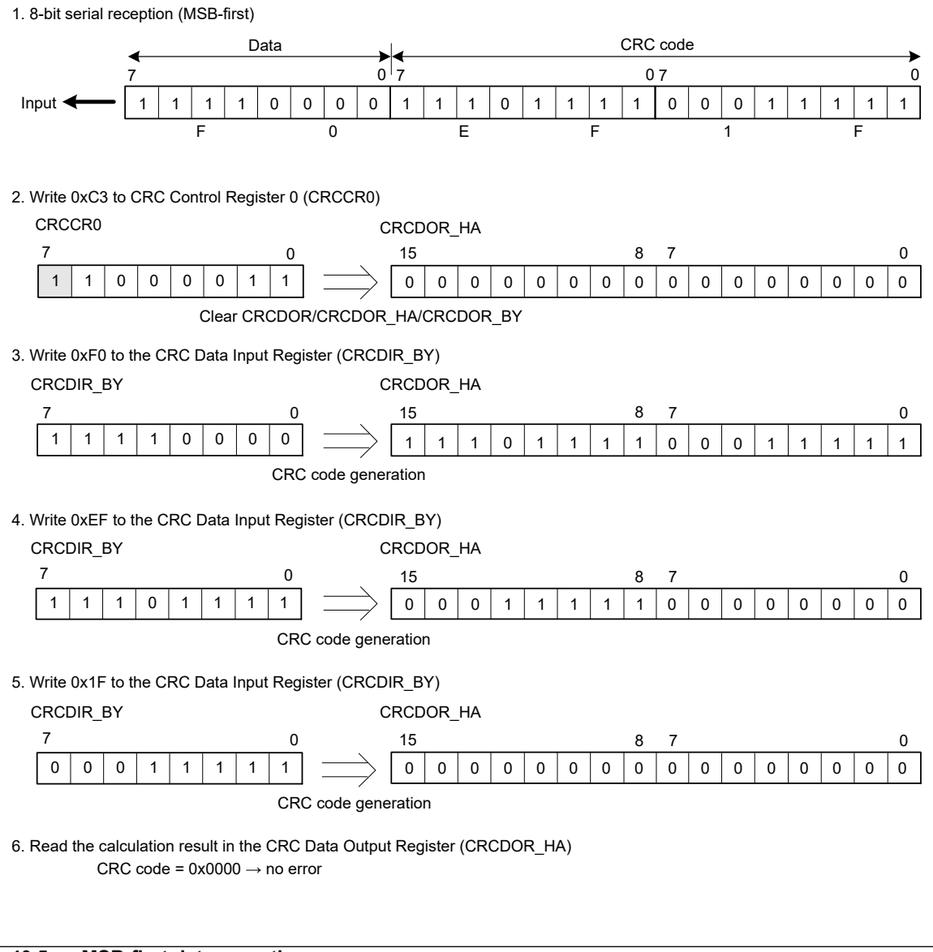


Figure 40.5 MSB-first data reception

40.4 Usage Notes

40.4.1 Settings for the Module-Stop State

The Module Stop Control Register C (MSTPCRC) can enable or disable CRC calculator operation. The CRC calculator is initially stopped after a reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

40.4.2 Note on Transmission

The transmission sequence for the CRC code differs based on whether the transmission is LSB-first or MSB-first. Figure 40.6 shows an LSB-first and MSB-first data transmission.

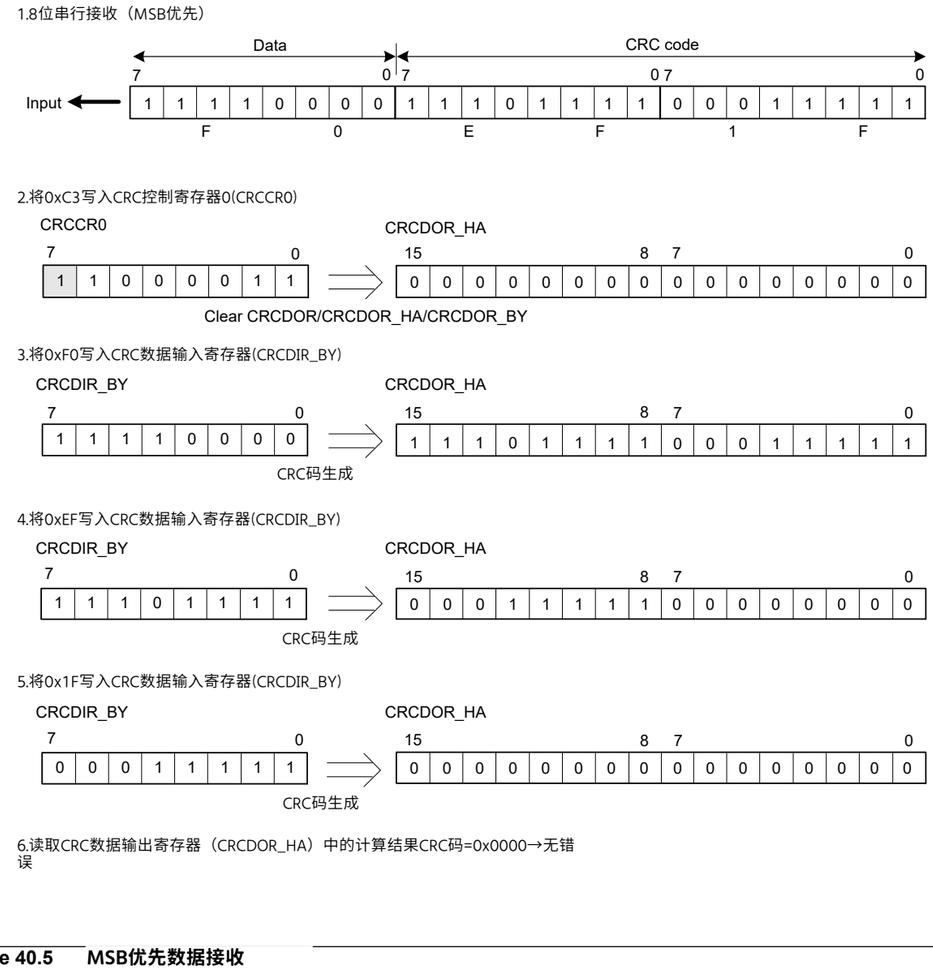


Figure 40.5 MSB优先数据接收

40.4 使用说明

40.4.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用CRC计算器操作。CRC计算器在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

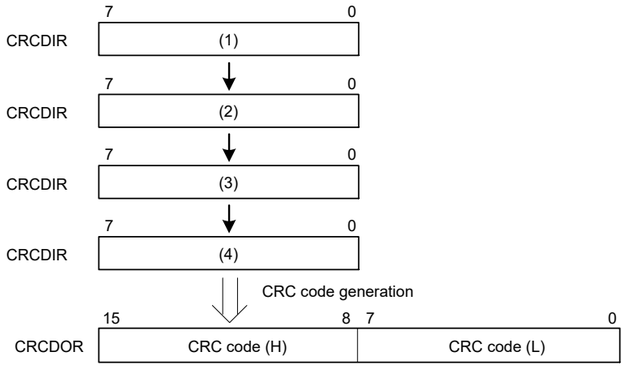
40.4.2 传输注意事项

CRC码的传输顺序根据传输是LSB在先还是MSB在先而有所不同。图40.6显示了LSB优先和MSB优先的数据传输。

When transmitting 32-bit data (for operation executed on 8 bits in parallel)

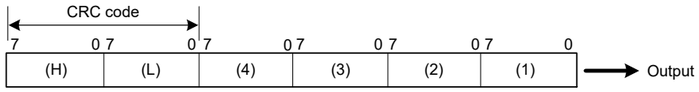
1. CRC code

After specifying the method for generation calculation, write data to CRCDIR in order of (1), (2), (3), and (4).



2. Transmit data

(i) When transmission is LSB-first



(ii) When transmission is MSB-first

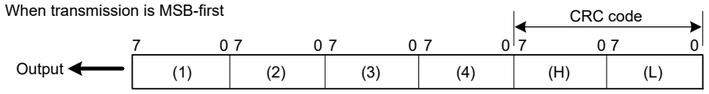
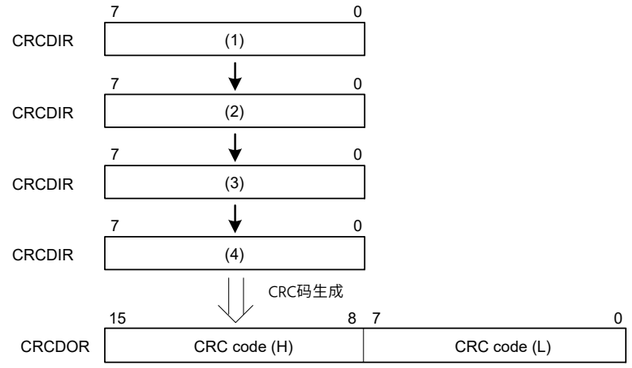


Figure 40.6 LSB-first and MSB-first data transmission

传输32位数据时（用于并行执行8位操作）

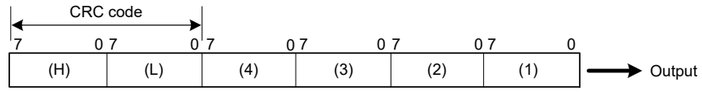
1. CRC code

指定生成计算方法后，按照（1）、（2）、（3）、（4）的顺序将数据写入CRCDIR。



2.传输数据

(i) 当传输是LSB优先时



(ii)当传输是MSB优先时

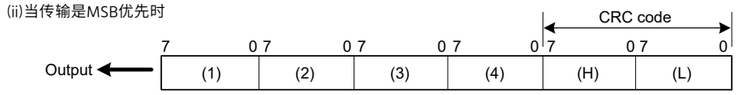


Figure 40.6 LSB-first和MSB-first数据传输

41. Boundary Scan

41.1 Overview

The boundary scan function provides a serial I/O interface based on the JTAG (Joint Test Action Group), IEEE Std.1149.1, and IEEE Standard Test Access Port and Boundary Scan Architecture. Table 41.1 lists the boundary scan specifications, Figure 41.1 shows a block diagram, and Table 41.2 lists the I/O pins.

Table 41.1 Boundary scan specifications

Parameter	Specifications
Execution condition	Boundary scan must be executed when the RES pin is driven low.
Test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

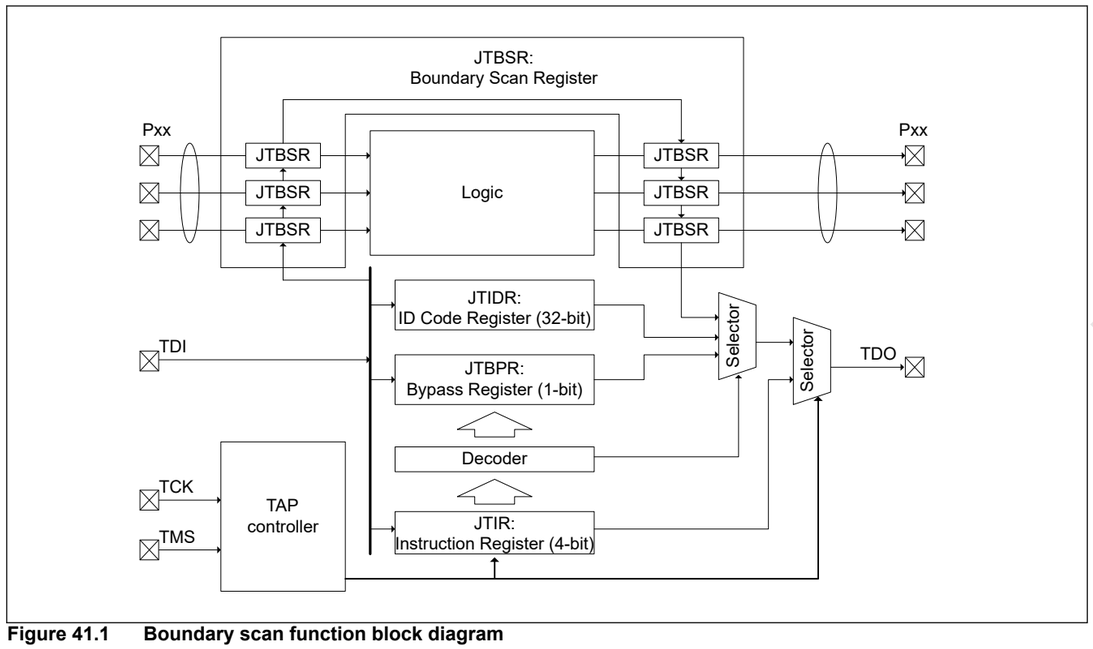


Figure 41.1 Boundary scan function block diagram

Table 41.2 Boundary scan I/O pins

Pin name	I/O	Description
TCK	Input	Test clock input pin Clock signal for boundary scan. The input clock duty cycle is 50% when the boundary scan function is used.
TMS	Input	Test mode select pin
TDI	Input	Test data input pin
TDO	Output	Test data output pin

Note: This device does not support the TRST pin for the JTAG interface.

41.2 Register Descriptions

Table 41.3 lists the boundary scan registers.

41. 边界扫描

41.1 Overview

边界扫描功能提供基于JTAG（联合测试行动组）、IEEEStd.1149.1和IEEE标准测试访问端口和边界扫描架构的串行IO接口。表41.1列出了边界扫描规范，图41.1显示了框图，表41.2列出了IO引脚。

Table 41.1 边界扫描规格

Parameter	Specifications
执行条件	当RES引脚驱动为低电平时，必须执行边界扫描。
测试模式	• 旁路模式 • EXTEST mode • SAMPLE/PRELOAD mode • 钳位模式 • HIGHZ mode • IDCODE mode

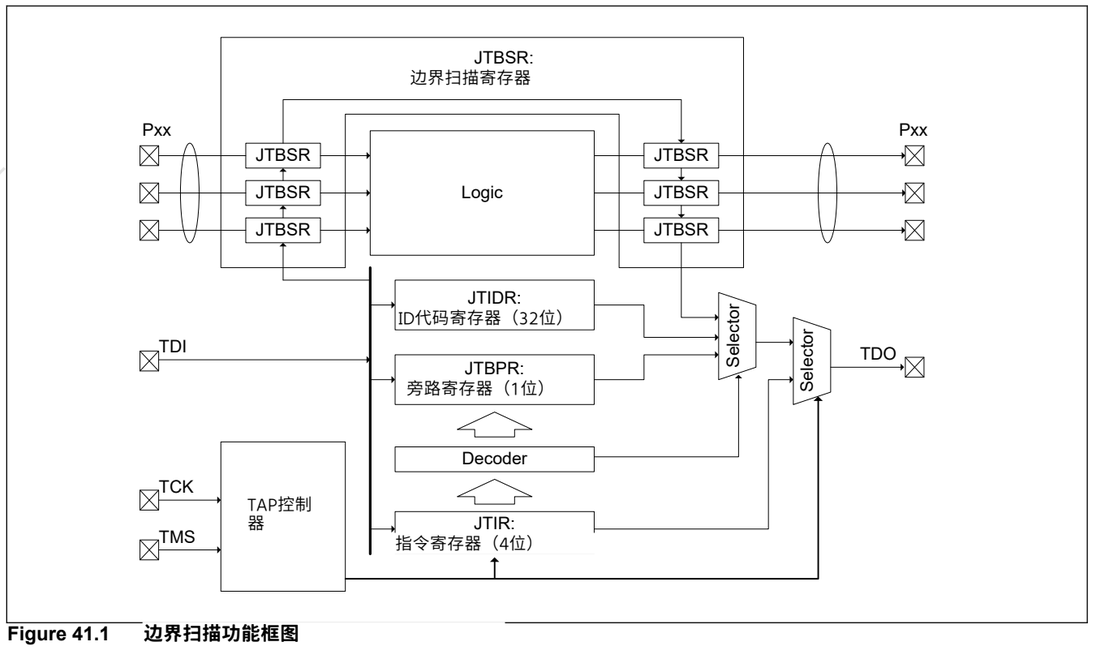


Figure 41.1 边界扫描功能框图

Table 41.2 边界扫描IO引脚

引脚名称	I/O	Description
TCK	Input	测试时钟输入引脚 边界扫描的时钟信号。使用边界扫描功能时，输入时钟占空比为50%。
TMS	Input	测试模式选择引脚
TDI	Input	测试数据输入引脚
TDO	Output	测试数据输出引脚

Note: 该器件不支持JTAG接口的TRST引脚。

41.2 注册说明

表41.3列出了边界扫描寄存器。

RA生态工作室

Table 41.3 Boundary scan registers

Register name	Symbol	Value after reset
Instruction Register	JTIR	0xE
ID Code Register	JTIDR	0x0841_2447
Bypass Register	JTBPR	Undefined
Boundary Scan Register	JTBSR	Undefined

Usage notes for the boundary scan registers:

- Instructions can be input to the Instruction Register (JTIR) through the TDI pin by serial transfer.
- The Bypass Register (JTBPR), which is a 1-bit register, is connected between the TDI and TDO pins in BYPASS mode.
- The Boundary Scan Register (JTBSR), which is configured according to the BSDL description, is connected between the TDI and TDO pins when test data is being shifted in.

Table 41.4 shows the availability of serial transfer for the registers.

Table 41.4 Serial transfer for registers

Register name	Serial input	Serial output
Instruction Register (JTIR)	Available	Available
ID Code Register (JTIDR)	Available	Available
Bypass Register (JTBPR)	Available	Available
Boundary Scan Register (JTBSR)	Available	Available

41.2.1 JTIR : Instruction Register

Bit	Symbol	Function	R/W
3:0	TS[3:0]	Test Bit Set The command configuration for these bits	—

TS[3:0]	Instruction
0x0	EXTEST
0x1	SAMPLE/PRELOAD
0x3	IDCODE (Renesas code)
0x5	CLAMP
0x6	HIGHZ
0xF	BYPASS
Others	Reserved

JTAG instructions can be transferred to the JTIR register by serial input from the TDI pin. The JTIR register is initialized when a power-on reset occurs, or when the TAP controller is in the Test-Logic-Reset state.

41.2.2 JTIDR : ID Code Register

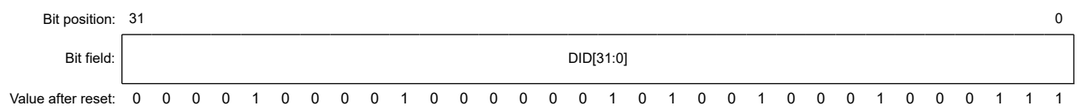


Table 41.3 边界扫描寄存器

注册名称	Symbol	重置后的值
指令寄存器	JTIR	0xE
ID代码寄存器	JTIDR	0x0841_2447
绕过寄存器	JTBPR	Undefined
边界扫描寄存器	JTBSR	Undefined

边界扫描寄存器的使用说明：

●指令可以通过串行传输的方式通过TDI引脚输入指令寄存器（JTIR）。

●BypassRegister(JTBPR)是一个1位寄存器，在BYPASS模式下连接在TDI和TDO引脚之间。

●根据BSDL描述配置的边界扫描寄存器(JTBSR)在测试数据移入时连接在TDI和TDO引脚之间。

表41.4显示了寄存器串行传输的可用性。

Table 41.4 寄存器的串行传输

注册名称	串行输入	串行输出
指令寄存器(JTIR)	Available	Available
ID代码寄存器(JTIDR)	Available	Available
旁路寄存器(JTBPR)	Available	Available
边界扫描寄存器(JTBSR)	Available	Available

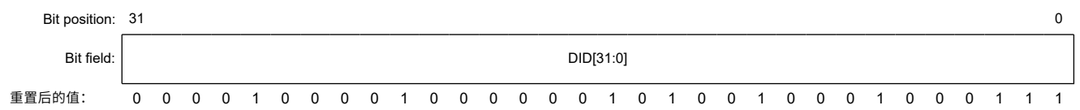
41.2.1 JTIR:指令寄存器

Bit	Symbol	Function	R/W
3:0	TS[3:0]	测试位组 这些位的命令配置	—

TS[3:0]	Instruction
0x0	EXTEST
0x1	SAMPLE/PRELOAD
0x3	IDCODE (Renesas code)
0x5	CLAMP
0x6	HIGHZ
0xF	BYPASS
Others	Reserved

JTAG指令可以通过TDI引脚的串行输入传输到JTIR寄存器。当发生上电复位或TAP控制器处于Test-Logic-Reset状态时，JTIR寄存器被初始化。

41.2.2 JTIDR:ID代码寄存器



Bit	Symbol	Function	R/W
31:0	DID[31:0]	Device ID These bits store the fixed value that indicates the device IDCODE (0x0841_2447).	—

The JTIDR register data is output from the TDO pin when the IDCODE instruction is executed. After a reset release, the DID[31:0] of JTIDR changes into the Arm® debug code. See the *Arm® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).

41.2.3 JTBPR : Bypass Register

The JTBPR register is a 1-bit register and is connected between the TDI and TDO pins when the JTIR register is set to BYPASS mode. The JTBPR register cannot be read from or written to by the CPU.

41.2.4 JTBSR : Boundary Scan Register

The JTBSR register is a shift register for controlling the external input and output pins of this device, and is distributed across the pads. To apply the JTBSR register in boundary-scan testing, issue the EXTEST, SAMPLE/PRELOAD, CLAMP, and HIGHZ instructions. The BSDL file describes the associations between the JTBSR register bits and the pins of this device. The value after reset is undefined.

41.3 Operation

During a reset, the JTAG ports, TCK, TMS, TDI, and TDO, are assigned as default pin functions. The TCK, TMS, and TDI pins are pulled up by the pull-up resistors. Boundary scan testing can be executed after the setup time elapses when POR is negated and RES is driven low.

41.3.1 TAP Controller

Figure 41.2 shows the state transition diagram of the TAP controller. All transitions are controlled by the TMS signal.

Bit	Symbol	Function	R/W
31:0	DID[31:0]	设备ID 这些位存储指示设备IDCODE(0x0841_2447)的固定值。	—

执行IDCODE指令时，从TDO引脚输出JTIDR寄存器数据。复位释放后，
JTIDR的DID[31:0]更改为Arm®调试代码。请参阅Arm®CoreSight SoC-400技术参考手册(ARMDDI0480F)。

41.2.3 JTBPR:旁路寄存器

JTBPR寄存器是一个1位寄存器，当JTIR寄存器设置为
旁路模式。CPU无法读取或写入JTBPR寄存器。

41.2.4 JTBSR:边界扫描寄存器

JTBSR寄存器是一个移位寄存器，用于控制该器件的外部输入和输出引脚，分布在各个焊盘上。要在边界扫描测试中应用JTBSR寄存器，请发出EXTEST、SAMPLEPRELOAD、CLAMP和HIGHZ指令。BSDL文件描述了JTBSR寄存器位和该器件引脚之间的关联。复位后的值未定义。

41.3 Operation

在复位期间，JTAG端口、TCK、TMS、TDI和TDO被分配为默认引脚功能。TCK、TMS和TDI引脚由上拉电阻上拉。当POR被否定并且RES被驱动为低电平时，可以在设置时间过去后执行边界扫描测试。

41.3.1 水龙头控制器

图41.2显示了TAP控制器的状态转换图。所有转换都由TMS信号控制。

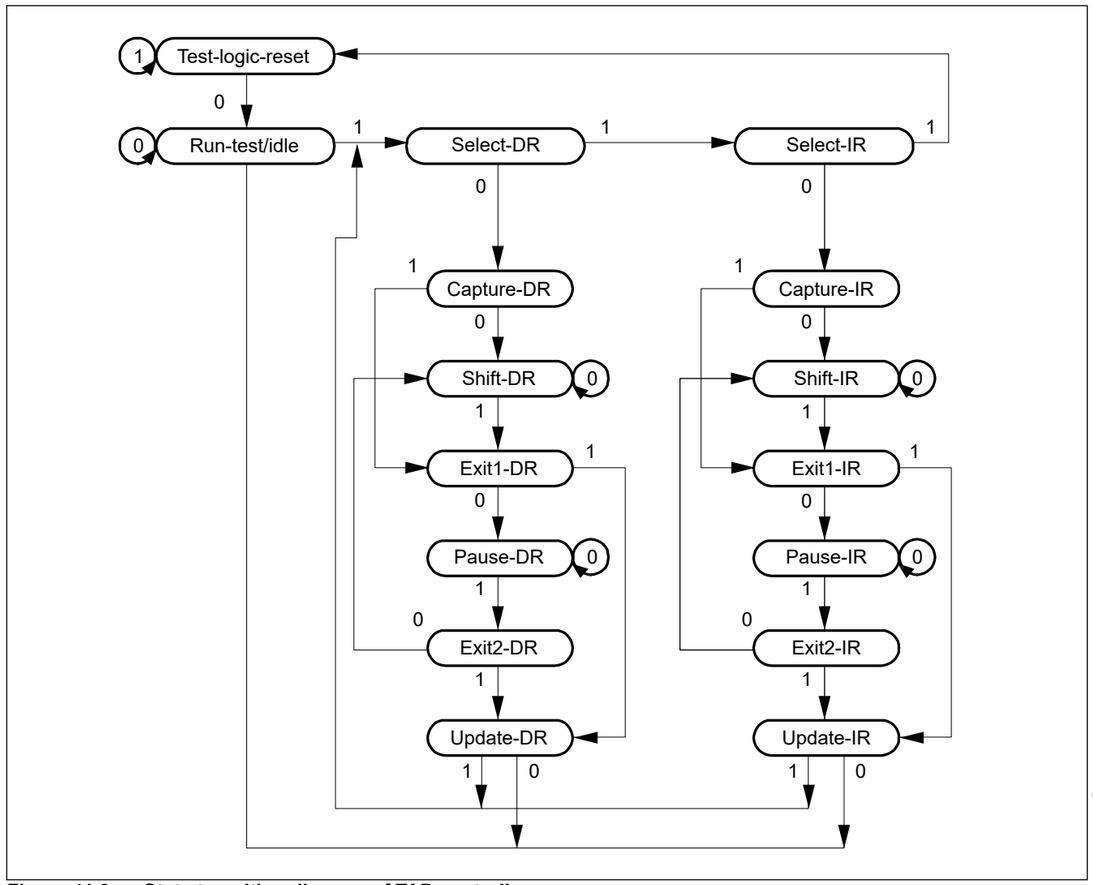


Figure 41.2 State transition diagram of TAP controller

41.3.2 Commands

(1) BYPASS

The BYPASS instruction drives the Bypass Register (JTBPR). This instruction shortens the shift path, facilitating the transfer of serial data to other LSIs on a printed circuit board at higher speeds. While this instruction is being executed, the test circuit has no effect on the system circuits.

The JTBPR register is connected between the TDI and TDO pins. Bypass operation is initiated from the Shift-DR operation. The TDO is low in the first clock cycle in the Shift-DR state. In the subsequent clock cycles, values input to the TDI pin are output from the TDO pin.

(2) EXTEST

The EXTEST instruction is used to test external circuits when this device is installed on the printed circuit board. If this instruction is executed, output pins are used to output test data (specified in the SAMPLE/PRELOAD instruction) from the Boundary Scan Register (JTBSR) to the other devices, and input pins are used to input the test result.

(3) SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to input data from the internal circuits of this device to the JTBSR register, output data from the scan path, and reload the data to the scan path. While this instruction is executed, input signals are directly input to this device and output signals are also directly output to the external circuits. This device system circuit is not affected by this instruction.

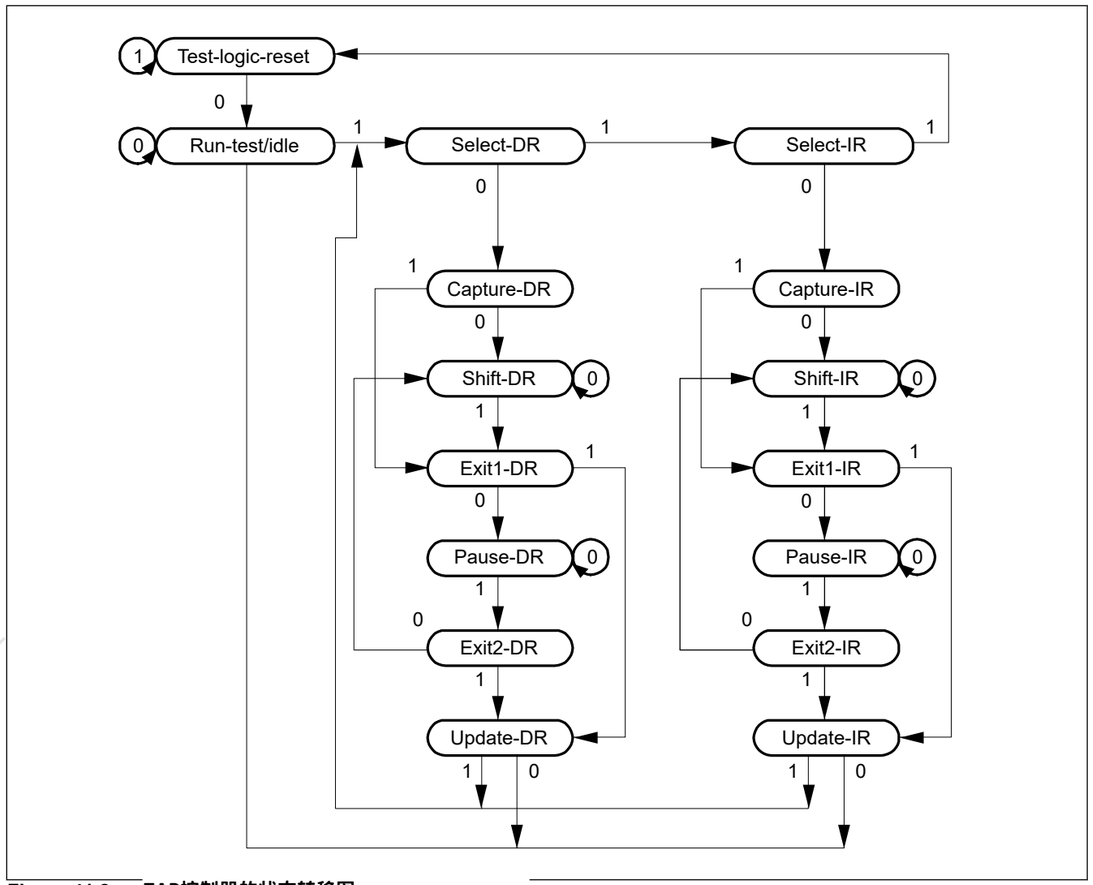


Figure 41.2 TAP控制器的状态转移图

41.3.2 Commands

(1) BYPASS

BYPASS指令驱动旁路寄存器(JTBPR)。该指令缩短了移位路径，便于将串行数据以更高的速度传输到印刷电路板上的其他LSI。在执行该指令时，测试电路对系统电路没有影响。

JTBPR寄存器连接在TDI和TDO引脚之间。旁路操作从Shift-DR操作开始。TDO在Shift-DR状态的第一个时钟周期内为低电平。在随后的时钟周期中，输入到TDI引脚的值从TDO引脚输出。

(2) EXTEST

当本设备安装在印刷电路板上时，EXTEST指令用于测试外部电路。如果执行该指令，输出引脚用于将测试数据（在SAMPLEPRELOAD指令中指定）从边界扫描寄存器(JTBSR)输出到其他设备，输入引脚用于输入测试结果。

(3) SAMPLE/PRELOAD

SAMPLEPRELOAD指令用于将数据从本器件内部电路输入到JTBSR寄存器，从扫描路径输出数据，并将数据重新加载到扫描路径。执行该指令时，输入信号直接输入到本设备，输出信号也直接输出到外部电路。本设备系统电路不受本指令影响。

In SAMPLE operation, the JTBSR register latches a snapshot of the data transferred from the input pins to the internal circuit or data transferred from the internal circuit to the output pins. The latched data is read from the scan path. The JTBSR register latches the data snapshot on the rising edge of the TCK pin in the Capture-DR state. The data snapshot is only transferred from the internal circuit to the output pins during a reset.

In PRELOAD operation, the initial value is written from the scan path to the parallel output latch of the JTBSR register prior to the EXTEST instruction execution. If EXTEST is executed without executing this PRELOAD operation, undefined values are output from the beginning to the end (transfer to the output latch) of the EXTEST sequence. (In the EXTEST instruction, output parallel latches are always output to the output pins.)

(4) IDCODE

When the IDCODE instruction is selected, the ID Code Register (JTIDR) value is output to the TDO pin in the Shift-DR state of the TAP controller. In this case, the JTIDR register value is output LSB-first. During this instruction execution, the test circuit does not affect the system circuit.

(5) CLAMP

When the CLAMP instruction is selected, output pins output the JTBSR register value that was specified in the SAMPLE/PRELOAD instruction in advance. While the CLAMP instruction is selected, the status of the JTBSR register is maintained regardless of the TAP controller state.

The JTBPR register is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

(6) HIGHZ

When the HIGHZ instruction is selected, all output pins enter high-impedance state. While the HIGHZ instruction is selected, the JTBSR register is maintained regardless of the state of the TAP controller.

The JTBPR register is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

41.4 Usage Notes

The boundary scan function is subject to the following constraints:

- The boundary scan must be executed when the RES pin is driven low
- Serial data input/output is in LSB order, as shown in Figure 41.3

在SAMPLE操作中，JTBSR寄存器锁存从输入引脚传输到内部电路的数据或从内部电路传输到输出引脚的数据的快照。从扫描路径读取锁存的数据。在Capture-DR状态下，JTBSR寄存器在TCK引脚的上升沿锁存数据快照。数据快照仅在复位期间从内部电路传输到输出引脚。

在PRELOAD操作中，在执行EXTEST指令之前，将初始值从扫描路径写入JTBSR寄存器的并行输出锁存器。如果在不执行此PRELOAD操作的情况下执行EXTEST，则从EXTEST序列的开头到结尾（传输到输出锁存器）输出未定义的值。（在EXTEST指令中，输出并行锁存器始终输出到输出引脚。）

(4) IDCODE

WhentheIDCODEinstructionisselected theIDCodeRegister(JTIDR)valueisoutputtotheTDOpinintheShift-DRstateoftheTAPcontroller.在这种情况下，JTIDR寄存器值首先输出LSB。在该指令执行期间，测试电路不影响系统电路。

(5) CLAMP

选择夹具指令时，输出引脚输出样品中指定的JTBSR寄存器值
预先PRELOAD指令。选择CLAMP指令时，无论TAP控制器状态如何，都将保持JTBSR寄存器的状态。

JTBPR寄存器连接在TDI和TDO引脚之间，导致与选择BYPASS指令时相同的操作。

(6) HIGHZ

选择Highz指令时，所有输出引脚都输入高阻抗状态。选择HIGHZ指令时，无论TAP控制器的状态如何，都会保持JTBSR寄存器。

JTBPR寄存器连接在TDI和TDO引脚之间，导致与选择BYPASS指令时相同的操作。

41.4 使用说明

边界扫描函数受以下约束：

- RES引脚拉低时必须执行边界扫描
- 串行数据输入输出按LSB顺序，如图41.3所示

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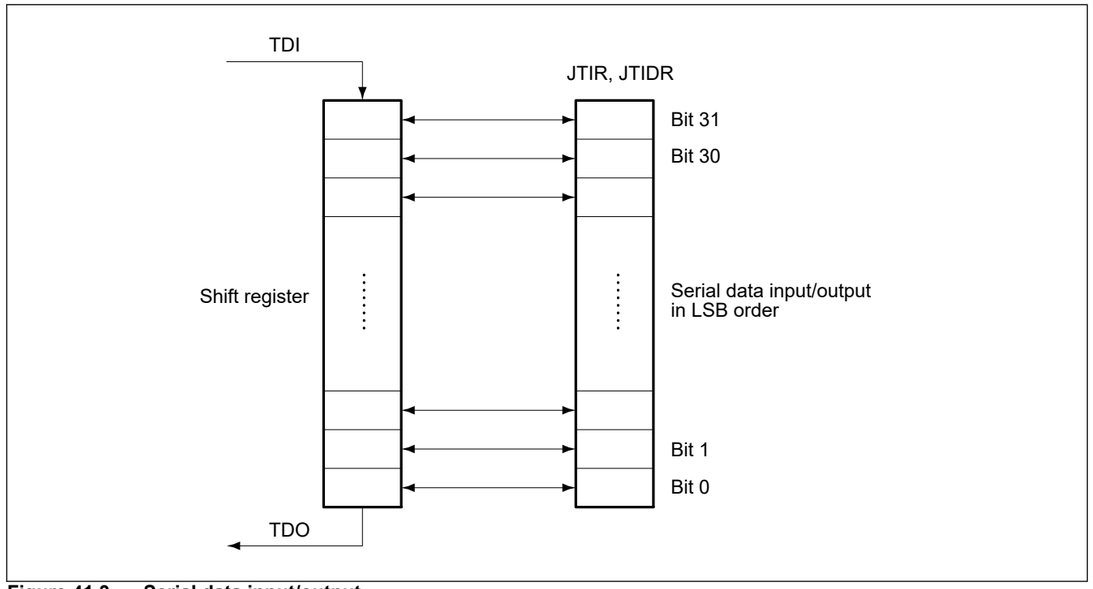

Figure 41.3 Serial data input/output

The following pins cannot be boundary-scanned:

- Power supply pins (VCC, VCL, VCL0, VSS, VBATT, AVCC0, AVSS0, VCC_USB, VSS_USB, VSS1_USBHS, VSS2_USBHS, PVSS_USBHS, and AVSS_USBHS)
- Analog reference pins (VREFH0, VREFL0, VREFH, VREFL)
- Clock pins (EXTAL, XTAL, XCIN, and XCOUT)
- Reset pin (RES)
- USB-dedicated pins (USB_DP, USB_DM, USBHS_DP, and USBHS_DM)
- The boundary-scan pins (TCK, TMS, TDI, and TDO).

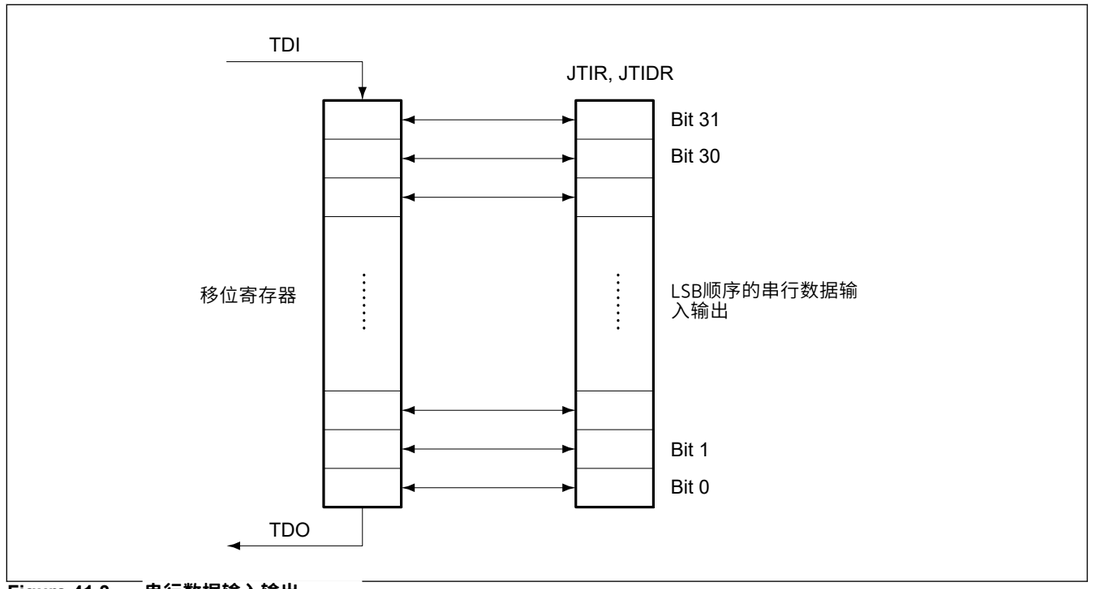

Figure 41.3 串行数据输入输出

以下引脚不能进行边界扫描：

●电源引脚（VCC、VCL、VCL0、VSS、VBATT、AVCC0、AVSS0、VCC_USB、VSS_USB、VSS1_USBHS、VSS2_USBHS、PVSS_USBHS和AVSS_USBHS）

●模拟参考引脚（VREFH0、VREFL0、VREFH、VREFL）

●时钟引脚（EXTAL、XTAL、XCIN和XCOUT）

●复位引脚（RES）

●USB专用引脚（USB_DP、USB_DM、USBHS_DP和USBHS_DM）

●边界扫描引脚（TCK、TMS、TDI和TDO）。

42. Secure Cryptographic Engine (SCE9)

42.1 Overview

The Secure Cryptographic Engine (SCE9) consists of the access management circuit, encryption engine, and random number generation circuit. In combination with the SCE9 library, the SCE9 can prevent eavesdropping (to maintain confidentiality), falsification of information (to ensuret integrity), and impersonation (to verify authenticity).

Because key information required for encryption and decryption is stored only in the SCE9 and all accesses from the outside can be blocked, SCE9 enables building a more robust security system.

Table 42.1 lists the SCE9 specifications. section 42.1. Overview shows the SCE9 block diagram.

Table 42.1 SCE9 specifications (1 of 2)

Parameter	Specifications
Access control	Access management circuit • In case of irregular access to the SCE9 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE9
Encryption engine	AES: Compliant with NIST FIPS PUB 197 • Key length: 128, 192, or 256 bits • Data block size: 128 bits • Encryption usage modes ECB, CBC, CTR: Compliant with NIST SP 800-38A CMAC: Compliant with NIST SP 800-38B CCM: Compliant with NIST SP 800-38C GCM: Compliant with NIST SP 800-38D XTS: Compliant with NIST SP 800-38E GCTR • Throughput for 128-bit data 11 PCLKA cycles for 128-bit key 13 PCLKA cycles for 192-bit key 15 PCLKA cycles for 256-bit key*1 AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Key management • Wrapped keys are only valid within the SCE9
Random number generation	128-bit true random number generation circuit
Signature generation and verification	RSA • Support for 1024-bit, 2048-bit, 3072-bit, and 4096-bit key sizes • Signature generation, signature verification, public-key encryption, private-key decryption DSA • Support for DSA key sizes: – (1024-bit, 160-bit) – (2048-bit, 224-bit) – (2048-bit, 256-bit) • Signature generation, signature verification ECC • Support for curve – NIST P-192, P-224, P-256, and P-384 – Brainpool P256r1, P384r1, and P512r1 • Signature generation, signature verification
Message digest computation	HASH • SHA224 and SHA256
Hardware Unique Key	• A read-only, 256-bit Hardware Unique Key (HUK) is exclusively accessible by the SCE access management circuit through a dedicated bus. • Key derivation functions (KDFs) combine the Hardware Unique Key with the key generation information. The derived keys implement the key wrapping for user key secure storage. • The HUK uniqueness prevents the illicit cloning and copying of keys to another MCU of the MCU group. • The HUK itself is stored in wrapped (encrypted, non-plain) format in an isolated memory area. Therefore it is protected from illicit access and copy.

42. 安全加密引擎(SCE9)

42.1 Overview

安全密码引擎（SCE9）由访问管理电路、加密引擎和随机数生成电路组成。结合SCE9库，SCE9可以防止窃听（以保持机密性）、伪造信息（以确保完整性）和假冒（以验证真实性）。

由于加密和解密所需的关键信息只存储在SCE9中，并且可以阻止来自外部的所有访问，因此SCE9可以构建更强大的安全系统。

表42.1列出了SCE9规范。第42.1节。概述显示了SCE9框图。

Table 42.1 SCE9规范（2个中的1个）

Parameter	Specifications
访问控制	访问管理电路● 如果由于程序被篡改或CPU失控而导致对SCE9的非正常访问，该电路将阻止所有后续访问并停止从SCE9输出数据
加密引擎	AES：符合NISTFIPSPUB197● 密钥长度：128、192或256位 • 数据块大小：128位 • 加密使用模式 ECB、CBC、CTR：符合NISTSP800-38A CMAC：符合NISTSP800-38BCCM：符合NISTSP800-38CGCM：符合NISTSP800-38DXTS：符合NISTSP800-38E GCTR • 128位数据的吞吐量128位密钥的1 1个PCLKA周期192位密钥的13个PCLKA周期256位密钥的15个PCLKA周期*1 AES-GCM • AES-GCM是通过结合AES-GCTR和GHASH实现的。 密钥管理● 封装的密钥仅在SCE9内有效
随机数生成	128位真随机数产生电路
签名生成和验证	RSA • 支持1024位、2048位、3072位和4096位密钥大小 ●签名生成、签名验证、公钥加密、私钥解密DSA● 支持DSA密钥大小： – (1024-bit, 160-bit) – (2048-bit, 224-bit) – (2048-bit, 256-bit) • 签名生成、签名验证 ECC • 支持曲线 – NIST P-192, P-224, P-256, and P-384 – Brainpool P256r1, P384r1, and P512r1 • 签名生成、签名验证
消息摘要计算	HASH • SHA224 and SHA256
硬件唯一密钥	• 只读的256位硬件唯一密钥(HUK)可由SCE访问管理电路通过专用总线独占访问。 • 密钥派生函数(KDF)将硬件唯一密钥与密钥生成信息相结合。派生密钥实现了用户密钥安全存储的密钥包装。 • HUK唯一性可防止将密钥非法克隆和复制到MCU组的另一个MCU。 • HUK本身以封装（加密，非纯）格式存储在隔离的内存区域中。因此，它受到保护，免受非法访问和复制。

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Table 42.1 SCE9 specifications (2 of 2)

Parameter	Specifications
Unique ID	• A read-only, 128-bit ID unique to an MCU (Unique ID) is accessible from the access management circuit. • Key derivation functions (KDFs) combine the Unique ID with the key generation information. Such derived keys are used to unwrap the HUK within the SCE boundary.
Low power consumption	Setting of the module-stop state is possible

Note 1. This does not include the overhead of calling SCE9 library functions.

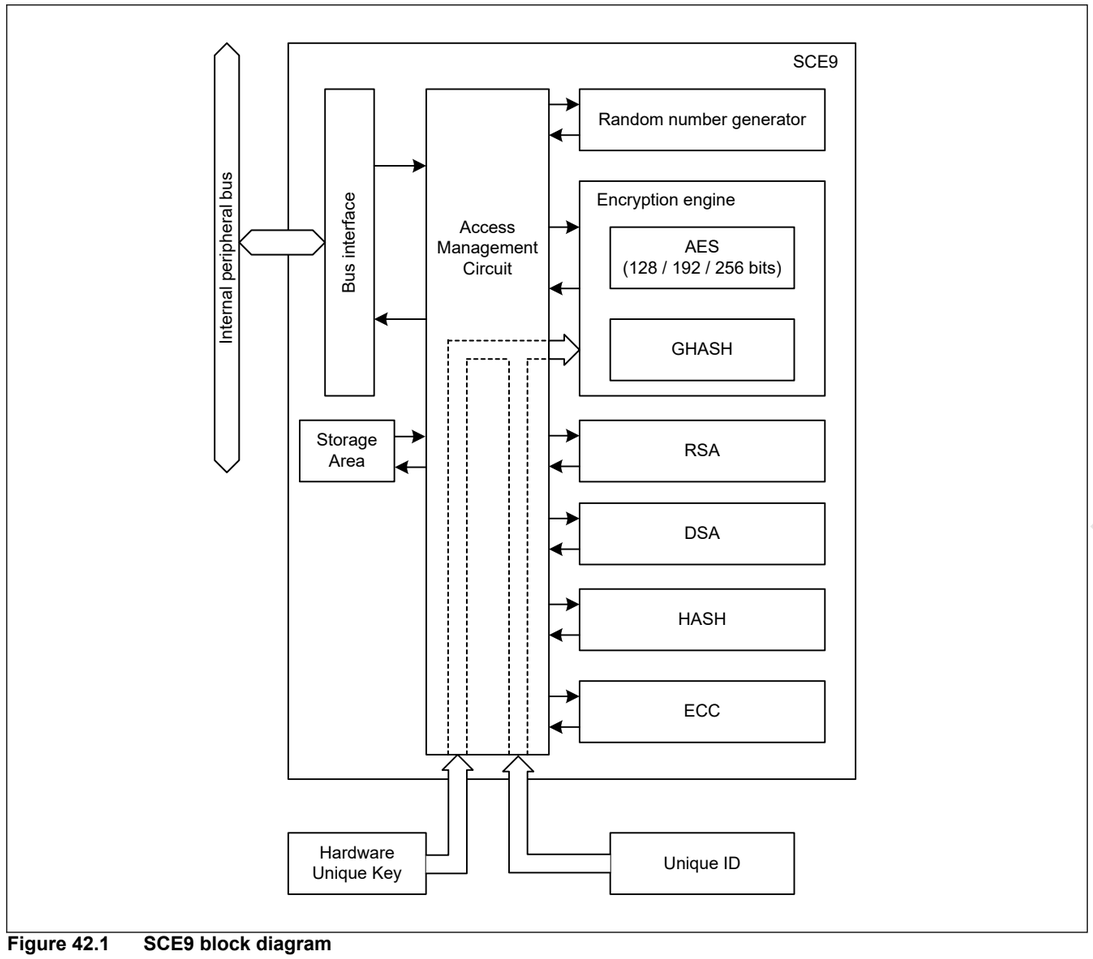

Figure 42.1 SCE9 block diagram

42.2 Operation

42.2.1 Encryption Engine

Figure 42.2 shows conceptual diagram of the encryption engine installed in the SCE9.

The encryption engine uses the key generation information, and converts the plaintext data to ciphertext or ciphertext data to plaintext through the hardware.

The encryption/decryption process can be completed without exposing the key data and the process's intermediate data to the outside of the SCE9.

Table 42.1 SCE9规范（2个中的2个）

Parameter	Specifications
唯一身份	• MCU唯一的只读128位ID（唯一ID）可从访问管理电路访问。 • 密钥派生函数(KDF)将唯一ID与密钥生成信息相结合。此类派生密钥用于在SCE边界内解开HUK。
低功耗	可以设置模块停止状态

注1.这不包括调用SCE9库函数的开销。

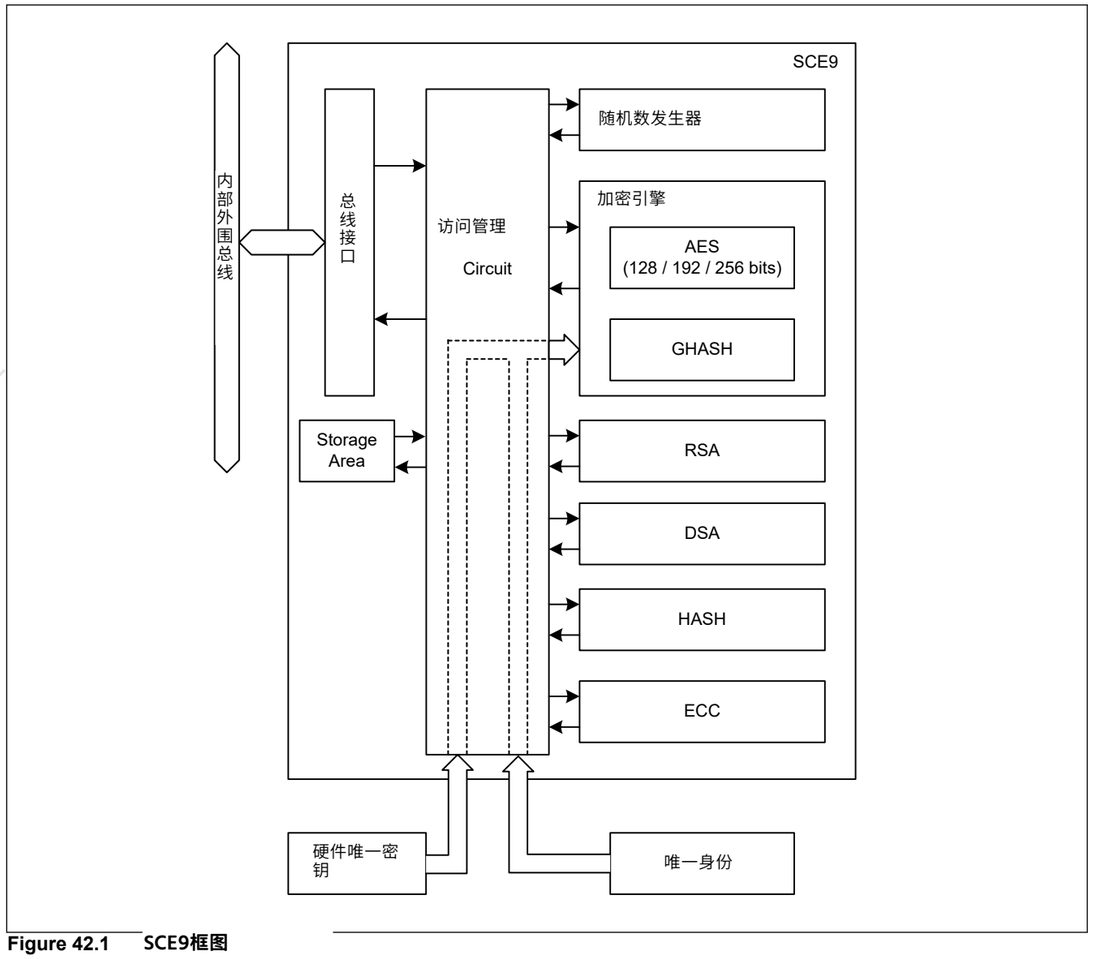

Figure 42.1 SCE9框图

42.2 Operation

42.2.1 加密引擎

图42.2显示了安装在SCE9中的加密引擎的概念图。

加密引擎使用密钥生成信息，通过硬件将明文数据转换为密文或将密文数据转换为明文。

加密解密过程可以在不将密钥数据和过程中间数据暴露在SCE9外部的情况下完成。

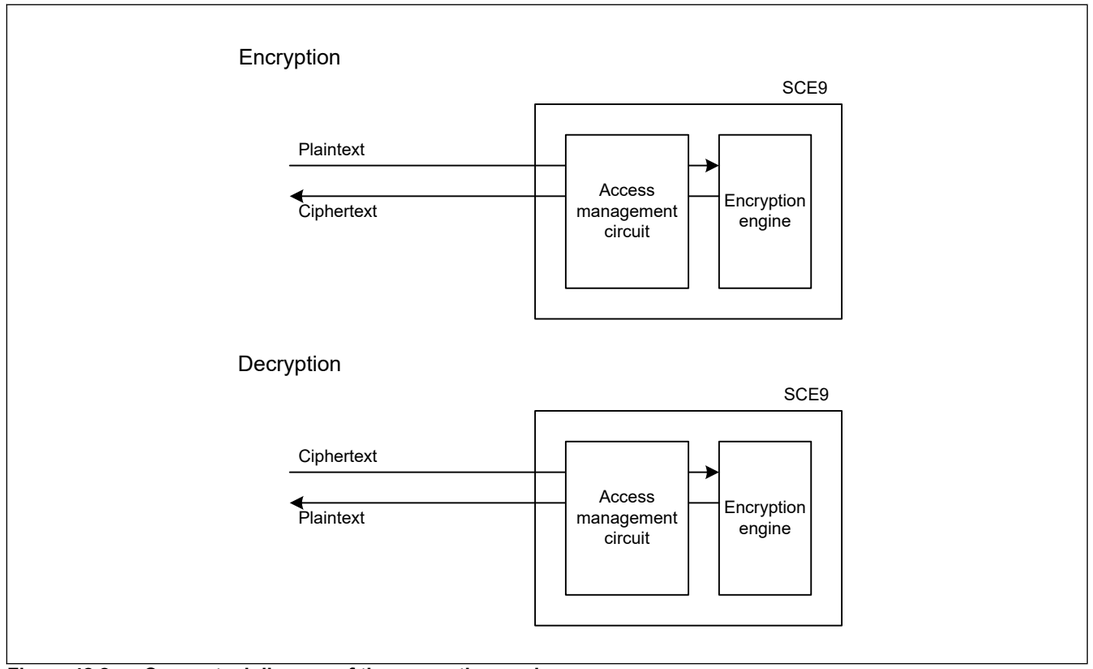

Figure 42.2 Conceptual diagram of the encryption engine

42.2.2 Encryption and Decryption

Follow the procedure below to encrypt and decrypt the data:

1. Enter the key generation information to the SCE9 and restore the key data.
2. Enter the target data to the SCE9. Plaintext data is converted to ciphertext and ciphertext data to plaintext.
3. Read the converted data.

The encryption engine has input and output buffers, and can perform encryption/decryption in parallel with data input/output. Figure 42.3 shows the encryption engine timing.

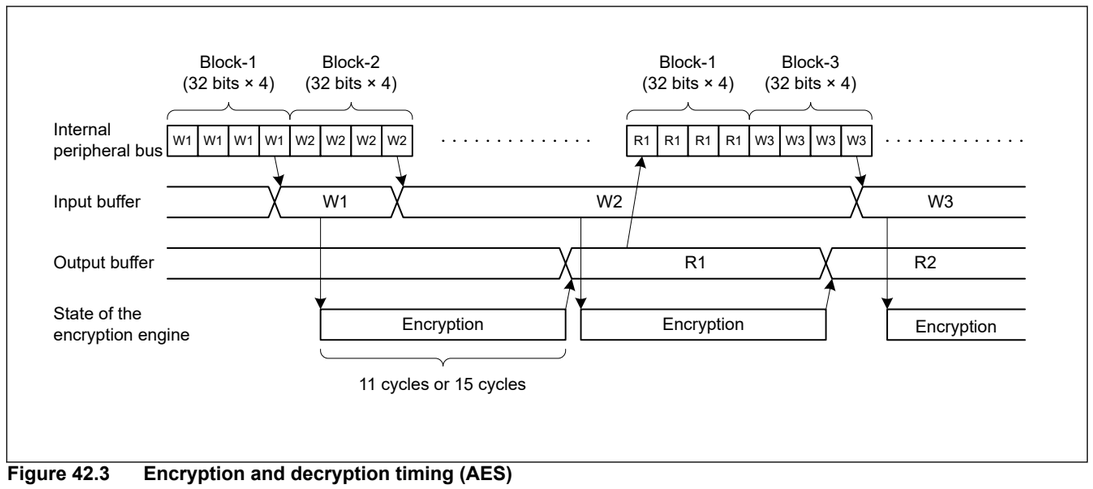

Figure 42.3 Encryption and decryption timing (AES)

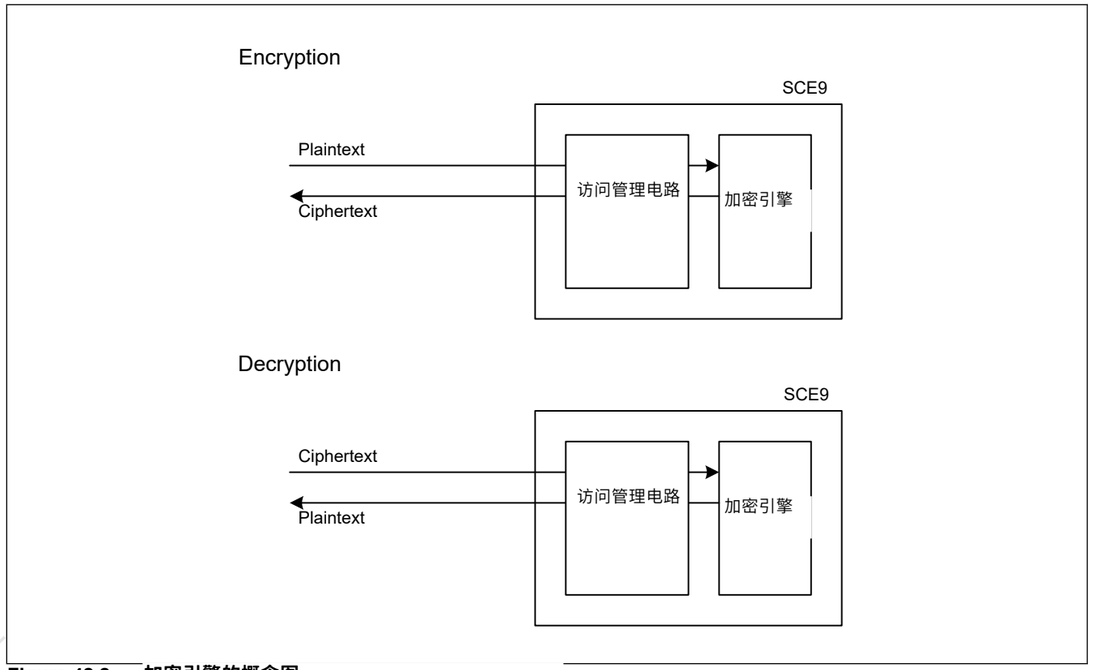

Figure 42.2 加密引擎的概念图

42.2.2 加密和解密

请按照以下步骤对数据进行加密和解密：

1.将密钥生成信息输入SCE9，恢复密钥数据。

2.将目标数据输入到SCE9。明文数据转换为密文，密文数据转换为明文。

3.读取转换后的数据。

加密引擎具有输入和输出缓冲区，可以与数据输入输出并行进行加密解密。图42.3显示了加密引擎的时序。

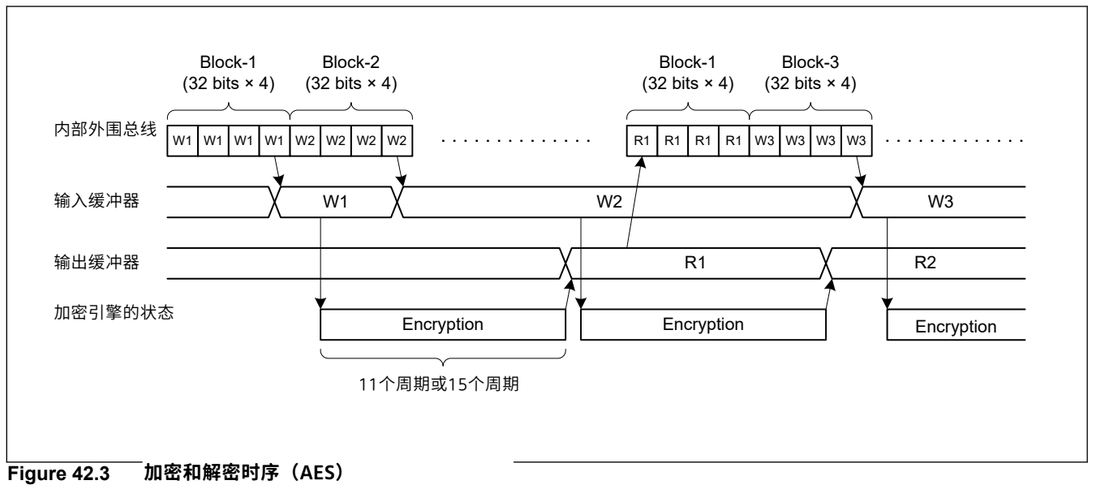

Figure 42.3 加密和解密时序（AES）

42.3 Usage Notes

42.3.1 Software Standby Mode

When the software standby mode is entered while the encryption engine is in process, proper processing cannot be resumed after the software standby mode is exited. The software standby mode should therefore be entered while the encryption engine is not running.

42.3.2 Module-Stop Function Setting

SCE9 operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The SCE9 module is initially stopped after reset. Releasing the module-stop state enables access to the registers.

42.3 使用说明

42.3.1 软件待机模式

当加密引擎正在运行时进入软件待机模式时，退出软件待机模式后无法恢复正常处理。因此，应在加密引擎未运行时进入软件待机模式。

42.3.2 模块停止功能设置

可以使用模块停止控制寄存器C(MSTPCRC)禁用或启用SCE9操作。SCE9模块在复位后最初停止。释放模块停止状态可以访问寄存器。

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43. 12-Bit A/D Converter (ADC12)

43.1 Overview

The MCU includes 12-bit successive approximation A/D converter (ADC12) units. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 16 analog input channels, temperature sensor output, internal reference voltage can be selected for conversion in respective units.

The A/D conversion accuracy is selectable from 12-bit, 10-bit, 8-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

The ADC12 supports the following operating modes:

- Single scan mode to convert analog inputs of selected channels in ascending order of channel number
- Continuous scan mode to convert analog inputs of selected channels continuously in ascending order of channel number
- Group scan mode to divide analog inputs of channels into two groups (group A and B) and convert the analog inputs of selected channels for each group in ascending order of channel number.

In group scan mode, select two groups (group A and B). You can individually select the scan start conditions for each group (group A, B) and start scanning of each group at different times. In addition, when group A priority control operation is set, the ADC12 accepts group A scan start during group B A/D conversion, suspending group B conversion. This allows you to assign higher priority to A/D conversion start for group A.

In double trigger mode, the analog input of a selected channel is converted in single scan mode or group scan mode (group A), and data converted by the first and second A/D conversion start triggers are stored in different registers, providing duplexing of A/D converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three reference voltage values generated in ADC12 is A/D converted.

The temperature sensor output and the internal reference voltage are selectable at the same time as the analog input of the channel. First A/D conversion is performed for the analog input of the channel, next the temperature sensor output, and then the internal reference voltage.

The ADC12 also provides a compare function (window A and window B). The compare function specifies the upper reference value for window A and lower reference value for window B, and outputs an interrupt when the A/D converted value of the selected channel meets the comparison conditions.

The A/D data storage buffer is a ring buffer consisting of 16 buffers to sequentially store A/D converted data.

Table 43.1lists the ADC12 specifications and Table 43.2 list the functions. Figure 43.1 shows a block diagram of ADC12 and Table 43.3 lists the I/O pins.

Table 43.1 ADC12 specifications (1 of 3)

Parameter	Specifications
Number of units	two units
Input channels	Up to 29 channels (AN000 to AN010, AN012, AN013, AN100 to AN102, AN116 to AN128) Extended
Analog function	Temperature sensor output, internal reference voltage
Conversion method	Successive approximation method
Resolution	12-bit, 10-bit, 8-bit
Conversion time	0.4 µs/channel (when 12-bit A/D conversion clock PCLKC (ADCLK) is operating at 50 MHz)
A/D conversion clock	Peripheral module clock PCLKA and A/D conversion clock PCLKC (ADCLK) can be set with the following division ratios: PCLKA to PCLKC (ADCLK) frequency ratio = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4

43. 12-Bit A/D Converter (ADC12)

43.1 Overview

MCU包括12位逐次逼近模数转换器(ADC12)单元。在单元0中，最多可选择13个模拟输入通道。在单元1中，最多可以选择16个模拟输入通道、温度传感器输出、内部参考电压进行相应单元的转换。

AD转换精度可从12位、10位、8位转换中选择，从而可以在生成数字值时优化速度和分辨率之间的权衡。

ADC12支持以下工作模式：

●单次扫描模式，以通道号升序转换所选通道的模拟输入

●连续扫描模式，以通道号升序连续转换所选通道的模拟输入

●组扫描模式，将通道的模拟输入分为两组（A组和B组），并按通道编号升序对每组所选通道的模拟输入进行转换。

在组扫描模式下，选择两个组（A组和B组）。您可以单独选择每个组（A、B组）的扫描开始条件，并在不同时间开始每个组的扫描。此外，当设置A组优先控制操作时，ADC12在B组AD转换期间接受A组扫描启动，暂停B组转换。这允许您为A组的AD转换启动分配更高的优先级。

在双触发模式下，选定通道的模拟输入转换为单扫描模式或组扫描模式（组A），由第一个和第二个AD转换启动触发器转换的数据存储在不同的寄存器中，提供AD转换数据的双工。

自诊断在每次扫描开始时执行一次，并在生成的三个参考电压值之一ADC12经过AD转换。

温度传感器输出和内部参考电压可与通道的模拟输入同时选择。首先对通道的模拟输入进行AD转换，然后是温度传感器输出，然后是内部参考电压。

ADC12还提供比较功能（窗口A和窗口B）。比较函数指定窗口A的上参考值和窗口B的下参考值，当所选通道的AD转换值满足比较条件时输出中断。

AD数据存储缓冲区是由16个缓冲区组成的环形缓冲区，用于顺序存储AD转换后的数据。

表43.1列出了ADC12规格，表43.2列出了功能。图43.1显示了ADC12的框图，表43.3列出了IO引脚。

Table 43.1 ADC12规格(1of3)

Parameter	Specifications
单位数量	两个单元
输入通道	多达29个通道（AN000至AN010、AN012、AN013、AN100至AN102、AN116至AN128）扩展
模拟功能	温度传感器输出，内部参考电压
转换方法	逐次逼近法
Resolution	12-bit, 10-bit, 8-bit
转换时间	0.4µs通道（当12位AD转换时钟PCLKC(ADCLK)工作在50MHz时）
AD转换时钟	外设模块时钟PCLKA和AD转换时钟PCLKC(ADCLK)可以设置为以下分频比：PCLKA与PCLKC(ADCLK)频率比=1:1 2:1 4:1 8:1 1:2 1:4

Table 43.1 ADC12 specifications (2 of 3)

Parameter	Specifications
Data registers*1	• 29 registers for analog input • One register for A/D-converted data duplication in double trigger mode • Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • A/D conversion results are stored in A/D data registers • 12-bit, 10-bit, 8-bit accuracy for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D-converted results is stored in the A/D data registers as a value with the conversion accuracy bit count + extended bits • Double-trigger mode (selectable in single scan and group scan modes): – The first unit of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): – A/D-converted analog input data on one selected channel is stored in the duplication register provided for the associated trigger.
Operating modes*2	• Single scan mode: – A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, on the temperature sensor output, on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of the selected channels, on the temperature sensor output, and on the internal reference voltage. • Group scan mode: – Analog inputs of selected channels, the temperature sensor output, and the internal reference voltage are divided into groups A and B. Then A/D conversion of the analog inputs selected on a group basis is performed once. – The scan start conditions can be independently selected for group A, B, allowing A/D conversion of group A, B to be started independently. • Group scan mode (when group priority operation is selected): – If a priority group trigger is input during scanning of a lower-priority group, the scanning of the lower-priority group is stopped and then scanning of the priority group is started. The order of priority is group A > group B. – It is possible to select whether to restart scanning (rescan) of the lower-priority group upon completion of the priority group scan. It is also possible to specify rescanning to be started from the first channel of the selected channels or from the channel for which A/D conversion has not been completed.
Conditions for A/D conversion start	• Software trigger • Synchronous triggers from the Event Link Controller (ELC) • Asynchronous triggering by the external trigger pins, ADTRG0 (unit 0) and ADTRG1 (unit 1)
Functions	• Variable sampling state count • Self-diagnosis of A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double-trigger mode (duplication of A/D conversion data) • Automatic clear function for A/D data registers • Digital comparison of values in the comparison register and data register, and comparison between values in the data registers • Interleave function • Ring buffer

Table 43.1 ADC12规格（2个，共3个）

Parameter	Specifications
数据寄存器*1	• 29个模拟输入寄存器 • 一个寄存器用于双触发模式下的AD转换数据复制 • 双触发模式下扩展操作期间用于AD转换数据复制的两个寄存器 • 1个温度传感器输出寄存器 • 1个内部参考电压寄存器 • 一个自我诊断寄存器 • AD转换结果存储在AD数据寄存器中 • AD转换结果的12位、10位、8位精度 • 一种D转换值相加模式，其中所有AD转换结果的总和作为转换精度位数+扩展位的值存储在AD数据寄存器中 • 双触发模式（可在单次扫描和组扫描模式下选择）： – 一个选定通道上的AD转换模拟输入数据的第一个单元存储在该通道的数据寄存器中，第二个单元存储在复制寄存器中。 • 双触发模式下的扩展操作（可用于特定触发）： – 一个选定通道上的D转换模拟输入数据存储在为相关触发提供的复制寄存器中。
操作模式*2	• 单次扫描模式： – D转换仅在任意选择通道的模拟输入、温度传感器输出和内部参考电压上执行一次。 • 连续扫描模式： 在选定通道的模拟输入、温度传感器输出和内部参考电压上重复执行D转换。 • 组扫描模式： – 所选通道的模拟输入、温度传感器输出和内部参考电压分为A组和B组。然后对按组选择的模拟输入进行一次AD转换。 – A、B组可以独立选择扫描开始条件，可以独立启动A、B组的A/D转换。 • 组扫描模式（选择组优先操作时）： – 如果在较低优先级组的扫描期间输入了优先级组触发，则较低优先级组的扫描停止，然后开始优先级组的扫描。优先顺序为A组>B组。 – 可以选择在完成优先级组扫描后是否重新开始低优先级组的扫描（重新扫描）。也可以指定从所选通道的第一个通道或未完成AD转换的通道开始重新扫描。
AD转换开始的条件	• 软件触发 • 来自事件链接控制器(ELC)的同步触发器 • 由外部触发引脚ADTRG0（单元0）和ADTRG1（单元1）异步触发
Functions	• 可变采样状态计数 • AD转换器的自诊断 • 可选择AD转换值加法模式或平均模式 • 模拟输入断线检测功能（放电和预充电功能） • 双触发模式（AD转换数据的复制） • AD数据寄存器的自动清除功能 • 比较寄存器和数据寄存器中值的数字比较，以及数据寄存器中的值之间的比较 • Interleave function • 环形缓冲区

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Table 43.1 ADC12 specifications (3 of 3)

Parameter	Specifications
Interrupt sources	• In single scan mode (double trigger deselected), an A/D scan end interrupt request (ADC12i_ADI (i = 0, 1)) and ELC event signal (ADC12i_ADI (i = 0, 1)) can be generated on completion of single scan. – A compare interrupt request (ADC12i_CMPAI (i = 0, 1)/ADC12i_CMPBI (i = 0, 1)) can be generated in response to a match with a digital comparison condition. – A window compare ELC event signal (ADC12i_WCMPM (i = 0, 1)) can be generated in response to a match with a digital comparison condition. – A window compare ELC event signal (ADC12i_WCMPUM (i = 0, 1)) can be generated in response to a mismatch with a digital comparison condition. • In single scan mode (double trigger selected), an A/D scan end interrupt request (ADC12i_ADI (i = 0, 1)) and ELC event signal (ADC12i_ADI (i = 0, 1)) is generated on completion of two scans. • In continuous scan mode, an A/D scan end interrupt request (ADC12i_ADI (i = 0, 1)) and ELC event signal (ADC12i_ADI (i = 0, 1)) is generated on completion of all the selected channel scans. • In group scan mode (double trigger deselected), an A/D scan end interrupt request (ADC12i_ADI (i = 0, 1)) and ELC event signal (ADC12i_ADI (i = 0, 1)) is generated on completion of group A scan, and an A/D scan end interrupt request for group B (ADC12i_GBADI (i = 0, 1)) can be generated on completion of group B scan. • In group scan mode (double trigger selected), an A/D scan end interrupt request (ADC12i_ADI (i = 0, 1)) and ELC event signal (ADC12i_ADI (i = 0, 1)) is generated on completion of two group A scans, and an A/D scan end interrupt request for group B (ADC12i_GBADI (i = 0, 1)) can be generated on completion of group B scan. • ADC12i_ADI (i = 0, 1), ADC12i_GBADI (i = 0, 1), ADC12i_WCMPM (i = 0, 1), and ADC12i_WCMPUM (i = 0, 1) can activate the Data Transfer Controller (DTC).
ELC interface	• An event is generated upon completion of group A scan in group-scan mode. • An event is generated upon completion of group B scan in group-scan mode. • An event is generated when all scans complete. • Scan can be started by a trigger from the ELC. • An event is generated according to conditions of the compare function window in single-scan mode.
Reference voltage	• Unit 0: VREFH0 is the high potential reference voltage. VREFL0 is the low potential reference voltage. • Unit 1: VREFH is the high potential reference voltage. VREFL is the low potential reference voltage.
Module-stop function	Module-stop state can be set to reduce power consumption.*3
TrustZone Filter	Security attribution can be set for each units

Note 1. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 43.3.7. Analog Input Sampling and Scan Conversion Time.
Note 2. When selecting the temperature sensor output, the internal reference voltage, do not use continuous scan mode or group scan mode.
Note 3. For details, see section 10, Low Power Modes.

Table 43.2 ADC12 functions (1 of 2)

Parameter			function
Analog input channel			AN000 to AN010, AN012, AN013(unit 0), AN100 to AN102, AN116 to AN128(unit 1) Internal reference voltage Temperature sensor output
Conditions for A/D conversion start	Software	Software trigger	Enabled
	Asynchronous trigger (external trigger)	Trigger input pin	ADTRGn (n = 0, 1)
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00 (unit 0) and ELC_AD10 (unit 1), ELC_AD01 (unit 0) and ELC_AD11 (unit 1)
Interrupt			ADC12i_ADI (i = 0, 1) ADC12i_GBADI (i = 0, 1) ADC12i_CMPAI (i = 0, 1) ADC12i_CMPBI (i = 0, 1)
Output to ELC			ADC12i_ADI (i = 0, 1) ADC12i_WCMPM (i = 0, 1) ADC12i_WCMPUM (i = 0, 1)

Table 43.1 ADC12规格（3个中的3个）

Parameter	Specifications
中断源	• 在单次扫描模式下（取消选择双触发），在完成单次扫描时会产生AD扫描结束中断请求（ADC12i_ADI(i=0 1)）和ELC事件信号（ADC12i_ADI(i=0 1)）。 – 比较中断请求(ADC12i_CMPAI(i=0 1)ADC12i_CMPBI(i=0 1))可以响应与数字比较条件的匹配而产生。 – 响应与数字比较条件的匹配，可以生成窗口比较ELC事件信号(ADC12i_WCMPM(i=0 1))。 – 响应与数字比较条件的不匹配，可以生成窗口比较ELC事件信号(ADC12i_WCMPUM(i=0 1))。 • 在单次扫描模式下（选择双触发），在完成两次扫描时会产生一个AD扫描结束中断请求(ADC12i_ADI(i=0 1))和ELC事件信号(ADC12i_ADI(i=0 1))。 • 在连续扫描模式下，在完成所有选定通道扫描后，将生成AD扫描结束中断请求(ADC12i_ADI(i=0 1))和ELC事件信号(ADC12i_ADI(i=0 1))。 • 在组扫描模式下（取消选择双触发），在完成A组扫描时产生AD扫描结束中断请求（ADC12i_ADI(i=0 1)）和ELC事件信号（ADC12i_ADI(i=0 1)），并且在完成B组扫描时，可以生成B组(ADC12i_GBADI(i=0 1))的AD扫描结束中断请求。 • 在组扫描模式下（选择双触发），AD扫描结束中断请求（ADC12i_ADI(i=0 1)）和ELC事件信号（ADC12i_ADI(i=0 1)）在两个A组扫描完成时产生，完成B组扫描后，可以生成B组的AD扫描结束中断请求(ADC12i_GBADI(i=0 1))。 • ADC12i_ADI(i=0 1)、ADC12i_GBADI(i=0 1)、ADC12i_WCMPM(i=0 1)和ADC12i_WCMPUM(i=0 1)可以激活数据传输控制器(DTC)。
ELC interface	• 在组扫描模式下完成A组扫描时会生成一个事件。 • 在组扫描模式下完成组B扫描时会生成一个事件。 • 当所有扫描完成时会生成一个事件。 • 扫描可以通过来自ELC的触发器启动。 • 在单扫描模式下，根据比较功能窗口的条件生成事件。
参考电压	• Unit 0: VREFH0是高电位参考电压。VREFL0是低电位参考电压。 • Unit 1: VREFH是高电位参考电压。VREFL是低电位参考电压。
Module-stop function	可设置模块停止状态以降低功耗。*3
TrustZone Filter	可以为每个单元设置安全属性

注1.更改AD转换精度也会更改AD转换时间。详见43.3.7节。模拟输入采样和扫描转换时间。
注2.选择温度传感器输出、内部参考电压时，不要使用连续扫描模式或组扫描模式。
注3.有关详细信息，请参阅第10节，低功耗模式。

Table 43.2 ADC12功能(1of2)

Parameter			function
模拟输入通道			AN000 to AN010, AN012, AN013(unit 0), AN100 to AN102, AN116 to AN128(unit 1) 内部参考电压温度传感器 输出
AD转换开始的条件	Software	软件触发	Enabled
	异步触发（外部触发）	触发输入引脚	ADTRGn (n = 0, 1)
	同步触发（来自ELC的触发）	ELC trigger	ELC_AD00 (unit 0) and ELC_AD10 (unit 1), ELC_AD01 (unit 0) and ELC_AD11 (unit 1)
Interrupt			ADC12i_ADI (i = 0, 1) ADC12i_GBADI (i = 0, 1) ADC12i_CMPAI (i = 0, 1) ADC12i_CMPBI (i = 0, 1)
输出到ELC			ADC12i_ADI (i = 0, 1) ADC12i_WCMPM (i = 0, 1) ADC12i_WCMPUM (i = 0, 1)

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Table 43.2 ADC12 functions (2 of 2)

Parameter	function
Module-stop function settings*1 *2	MSTPCRD.MSTPD16 bit (unit 0) , MSTPCRD.MSTPD15 bit (unit 1)

Note 1. For details, see section 10, Low Power Modes.
Note 2. Wait 1 µs or longer to start A/D conversion after release from the module-stop state.

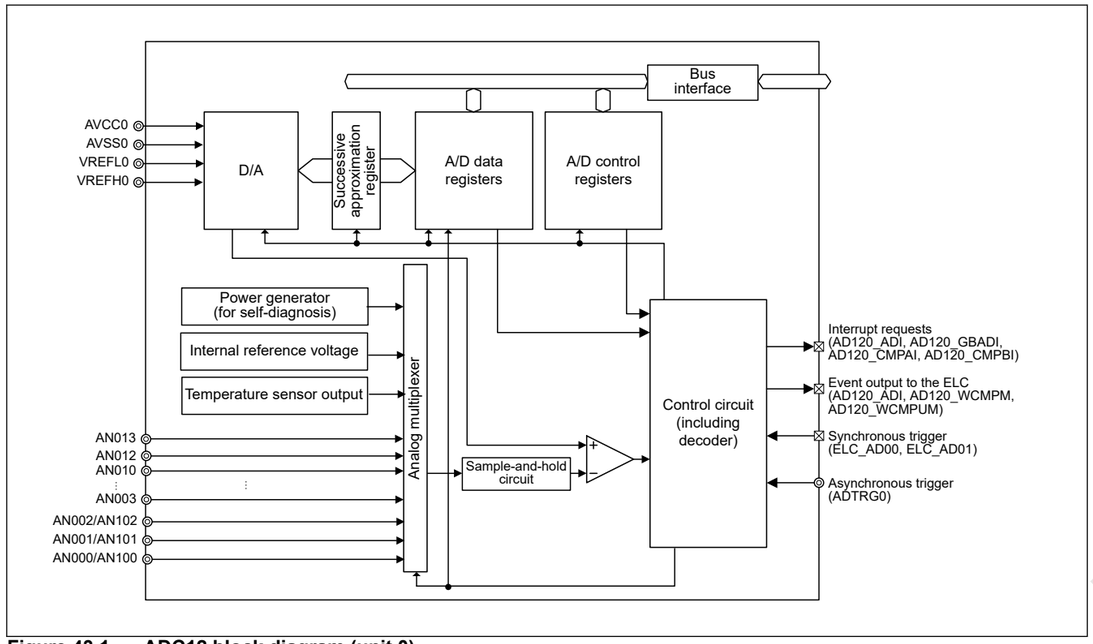

Figure 43.1 ADC12 block diagram (unit 0)

Table 43.2 ADC12功能（2个中的2个）

Parameter	function
模块停止功能设置*1*2	MSTPCRD.MSTPD16 bit (unit 0) , MSTPCRD.MSTPD15 bit (unit 1)

注1.有关详细信息，请参阅第10节，低功耗模式。
注2.从模块停止状态释放后，等待1µs或更长时间开始AD转换。

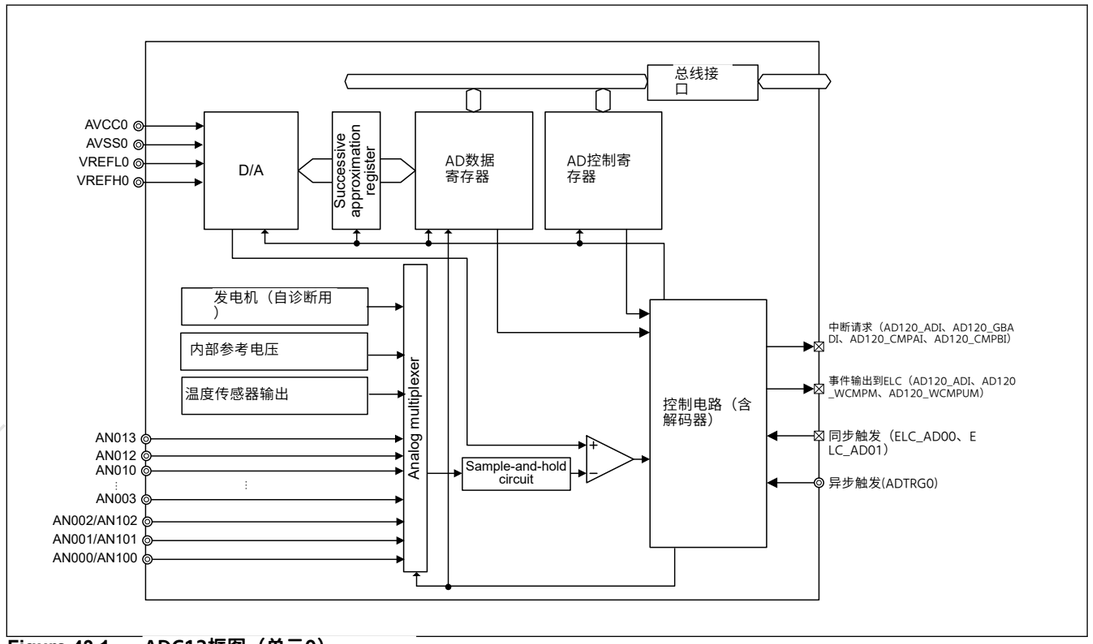

Figure 43.1 ADC12框图（单元0）

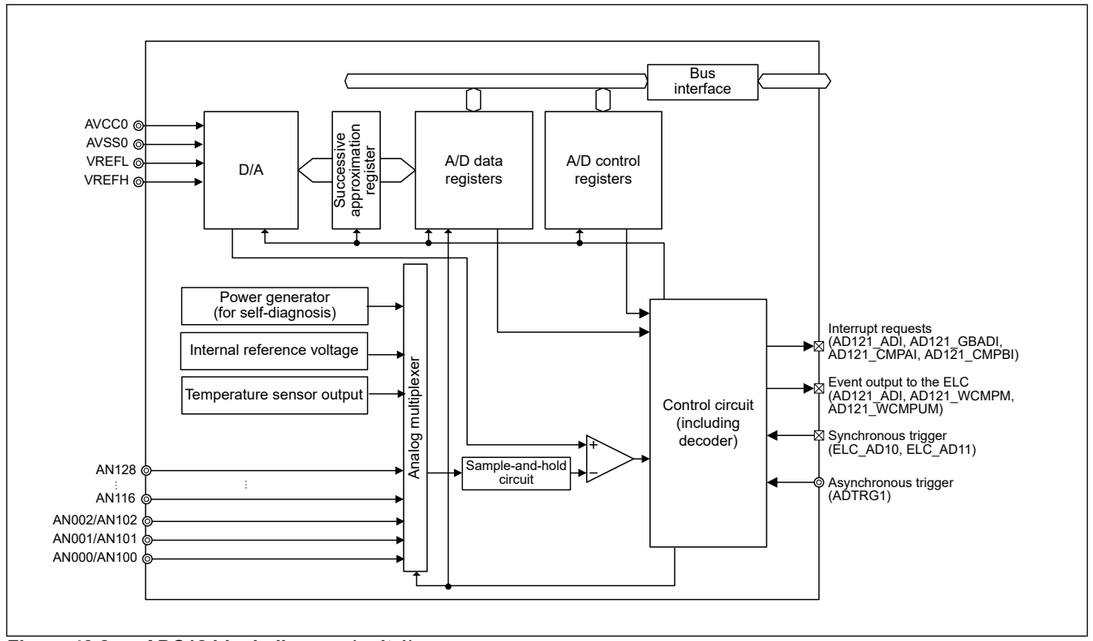

Figure 43.2 ADC12 block diagram (unit 1)

Table 43.3 lists the ADC12 I/O pins.

Table 43.3 ADC12 I/O pins (unit 0)

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin (Connect to VCC when ADC12/DAC12 is not used.)
AVSS0	Input	Analog block power supply ground pin (Connect to VSS when ADC12/DAC12 is not used.)
VREFH0	Input	Reference high-potential power supply pin
VREFL0	Input	Reference low-potential power supply ground pin
AN000 to AN010, AN012, AN013	Input	Analog input pins 0 to 10, 12, 13
ADTRG0	Input	External trigger input pin for starting A/D conversion

Table 43.4 ADC12 I/O pins (unit 1)

Pin name	I/O	Function
AVCC0	Input	Analog block power supply pin
AVSS0	Input	Analog block power supply ground pin
VREFH	Input	Reference power supply pin
VREFL	Input	Reference power supply ground pin
AN100 to AN102, AN116 to AN128	Input	Analog input pins 0 to 2, 16 to 28
ADTRG1	Input	External trigger input pin for starting A/D conversion

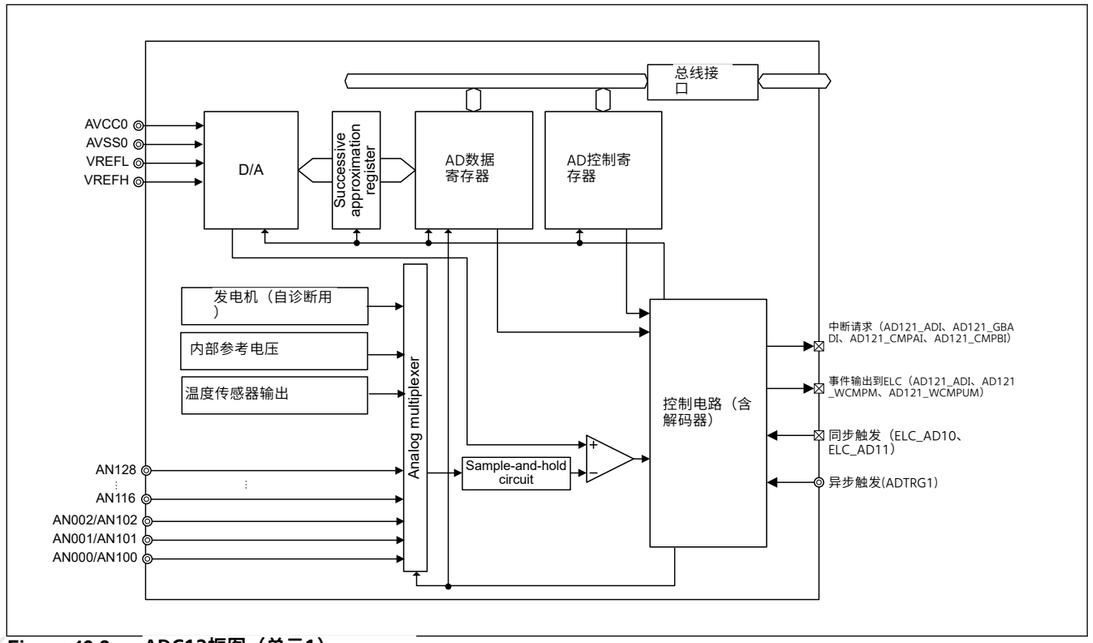

Figure 43.2 ADC12框图（单元1）

表43.3列出了ADC12IO引脚。

Table 43.3 ADC12 I/O pins (unit 0)

引脚名称	I/O	Function
AVCC0	Input	模拟模块电源引脚（不使用ADC12DAC12时连接到VCC。）
AVSS0	Input	模拟模块电源接地引脚（不使用ADC12DAC12时连接到VSS。）
VREFH0	Input	参考高电位电源引脚
VREFL0	Input	参考低电位电源接地引脚
AN000 to AN010, AN012, AN013	Input	模拟输入引脚0至10、12、13
ADTRG0	Input	用于启动AD转换的外部触发输入引脚

Table 43.4 ADC12 I/O pins (unit 1)

引脚名称	I/O	Function
AVCC0	Input	模拟模块电源引脚
AVSS0	Input	模拟模块电源接地引脚
VREFH	Input	参考电源引脚
VREFL	Input	参考电源接地引脚
AN100 to AN102, AN116 to AN128	Input	模拟输入引脚0至2、16至28
ADTRG1	Input	用于启动AD转换的外部触发输入引脚

43.2 Register Descriptions

43.2.1 ADDRn : A/D Data Registers n

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x020 + 0x2 × n (n = 0 to 10, 12, 13, m = 0)
0x020 + 0x2 × n (n = 0 to 2, 16 to 28, m = 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDRn [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDRn [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 43.5 and Table 43.6.	R

ADDRn registers are 16-bit read-only registers to store A/D conversion results.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 43.5 shows the example of bit assignment for 12-bit accuracy.

Table 43.5 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, These registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, these registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 43.6 shows example of the bit assignment for 12-bit accuracy.

43.2 注册说明

43.2.1 ADDRn:AD数据寄存器n

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x020 + 0x2 × n (n = 0 to 10, 12, 13, m = 0)
0x020 + 0x2 × n (n = 0 to 2, 16 to 28, m = 1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDRn [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDRn [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表43.5和表43.6。	R

ADDRn寄存器是16位只读寄存器，用于存储AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●AD转换精度选择位(ADCER.ADPRC[1:0])中的设置（可选择12位、10位、8位。）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表43.5显示了12位精度的位分配示例。

Table 43.5 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected TheseregistersindicatethemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位、10位、8位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式中，这些寄存器指示通过在特定通道上添加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表43.6显示了12位精度的位分配示例。

Table 43.6 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

43.2.2 ADDBLDR : A/D Data Duplexing Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x018

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 43.7 and Table 43.8.	R

ADDBLDR register is a 16-bit read-only register to store A/D conversion results in response to a second trigger in double-trigger mode.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 43.7 shows the example of bit assignment for 12-bit accuracy.

Table 43.7 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a

Table 43.6 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。	附加值13到0：AD转换结果的14位和														
具有12位精度的左对齐数据	指定1、2、3或4转换时间时	附加值15到0：AD转换结果的16位和															
	指定16个转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

43.2.2 ADDBLDR:AD数据双工寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x018

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDR [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表43.7和表43.8。	R

ADDBLDR寄存器是一个16位只读寄存器，用于存储AD转换结果，以响应双触发模式下的第二次触发。

以下条件决定了AD数据寄存器中的数据格式：

- ●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）
- ●AD转换精度选择位(ADCER.ADPRC[1:0])中的设置（可选择12位、10位、8位。）
- ●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）
- ●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表43.7显示了12位精度的位分配示例。

Table 43.7 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeiss elected ThisregisterindicatesthemeanofAD-convertedvaluesona

specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 43.8 shows example of the bit assignment for 12-bit accuracy.

Table 43.8 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

43.2.3 ADDBLDRn : A/D Data Duplexing Register n (n = A, B)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x084 (n = A)
0x086 (n = B)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDRn [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDRn [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 43.9 and Table 43.10.	R

ADDBLDRn registers are 16-bit read-only registers to store A/D conversion results in response to respective triggers during extended operation in double-trigger mode.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

具体渠道。该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位、10位、8位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表43.8显示了12位精度的位分配示例。

Table 43.8 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定1、2、3或4转换时间时	附加值15到0：AD转换结果的16位和															
	指定16个转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

43.2.3 ADDBLDRn:AD数据双工寄存器n(n=A B)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x084 (n = A)
0x086 (n = B)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADDBLDRn [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADDBLDRn [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表43.9和表43.10。	R

ADDBLDRn寄存器是16位只读寄存器，用于在双触发模式的扩展操作期间存储AD转换结果以响应相应的触发。

以下条件决定了AD数据寄存器中的数据格式：

- ●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）
- ●AD转换精度选择位(ADCER.ADPRC[1:0])中的设置（可选择12位、10位、8位。）
- ●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）
- ●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) When A/D-converted value addition/average mode is not selected

Table 43.9 shows the example of bit assignment for 12-bit accuracy.

Table 43.9 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, These registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, these registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 43.10 shows example of the bit assignment for 12-bit accuracy.

Table 43.10 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results															These bits are read as 0.

43.2.4 ADTSDR : A/D Temperature Sensor Data Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x01A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADTSDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) 未选择AD转换值加法平均模式时

表43.9显示了12位精度的位分配示例。

Table 43.9 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected TheseregistersindicatethemeanofAD−convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位、10位、8位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式中，这些寄存器指示通过在特定通道上添加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD−convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表43.10显示了12位精度的位分配示例。

Table 43.10 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定1、2、3或4转换时间时	附加值15到0：AD转换结果的16位和															
	指定16个转换时间时	附加值13到0：AD转换结果的14位和															这些位读为0。

43.2.4 ATSDR:AD温度传感器数据寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x01A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADTSDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADTSDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 43.11 and Table 43.12.	R

ADTSDR register is a 16-bit read-only register to store A/D conversion result of the temperature sensor output.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 43.11 shows the example of bit assignment for 12-bit accuracy.

Table 43.11 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 43.12 shows example of the bit assignment for 12-bit accuracy.

Table 43.12 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected (1 of 2)

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													

Bit	Symbol	Function	R/W
15:0	ADTSDR [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表43.11和表43.12。	R

ADTSDR寄存器是一个16位只读寄存器，用于存储温度传感器输出的AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●AD转换精度选择位(ADCER.ADPRC[1:0])中的设置（可选择12位、10位、8位。）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表43.11显示了12位精度的位分配示例。

Table 43.11 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected ThisregisterindicatesthemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位、10位、8位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表43.12显示了12位精度的位分配示例。

Table 43.12 选择AD转换值相加模式时12位精度的位分配示例（1of2）

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													

Table 43.12 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected (2 of 2)

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

43.2.5 ADOCDR : A/D Internal Reference Voltage Data Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x01C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADOCDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADOCDR [15:0]	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 43.13 and Table 43.14.	R

ADOCDR register is a 16-bit read-only register to store A/D conversion result of the internal reference voltage.

The following conditions determine the formats for data in the A/D data registers:

- Setting of the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- The setting in the A/D Conversion Accuracy Select bits (ADCER.ADPRC[1:0]) (12-bit, 10-bit, 8-bit is selectable.)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 43.13 shows the example of bit assignment for 12-bit accuracy.

Table 43.13 Example of bit assignment for 12-bit accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicates the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

Table 43.12 选择AD转换值相加模式时12位精度的位分配示例（2之2）

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的左对齐数据	指定1、2、3或4转换时间时	附加值15到0：AD转换结果的16位和															
	指定16个转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

43.2.5 ADocDR:AD内部参考电压数据寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x01C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADOCDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADOCDR [15:0]	将值15转换为0 功能因所选模式和精度而异。请参见表43.13和表43.14。	R

AOCDR寄存器是一个16位只读寄存器，用于存储内部参考电压的AD转换结果。

以下条件决定了AD数据寄存器中的数据格式：

●AD数据寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●AD转换精度选择位(ADCER.ADPRC[1:0])中的设置（可选择12位、10位、8位。）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表43.13显示了12位精度的位分配示例。

Table 43.13 12位精度的位分配示例

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected ThisregisterindicatesthemeanofAD-convertedvaluesonaspecificchannel.该值根据AD数据寄存器格式选择位的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于12位、10位、8位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicates the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 43.14 shows example of the bit assignment for 12-bit accuracy.

Table 43.14 Example of bit assignment for 12-bit accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.		Added Value 13 to 0: 14-bit sum of A/D conversion results													
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

43.2.6 ADRD : A/D Self-Diagnosis Data Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x01E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	AD[11:0]	Converted Value 11 to 0 12-bit A/D-converted value	R
13:12	—	These bits are read as 0.	R
15:14	DIAGST[1:0]	Self-Diagnosis Status 0 0: Self-diagnosis not executed after power-on. 0 1: Self-diagnosis was executed using the 0 V voltage. 1 0: Self-diagnosis was executed using the reference voltage*1 × 1/2. 1 1: Self-diagnosis was executed using the reference voltage *1. For details on self-diagnosis, see section 43.2.15. ADCER : A/D Control Extended Register.	R

Note: The example of the bit assignment for the right-justified data with 12-bit accuracy is indicated.
Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of the ADC12. In addition to the AD[11:0] bits indicating the A/D-converted value, it includes the Self-Diagnosis Status bit (DIAGST[1:0]).

The settings of the A/D data register format and the A/D conversion accuracy determines the formats for data in this register.

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 43.2.15. ADCER : A/D Control Extended Register.

This section describes the data formats for each condition. The register diagram and the register bit table shown in this section indicate example of the bit assignment for the left and right-justified data with 12-bit accuracy.

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器指示通过在特定通道上相加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD−convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsof theADDataRegisterFormatSelectbits.

表43.14显示了12位精度的位分配示例。

Table 43.14 选择AD转换值相加模式时12位精度的位分配示例

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。		附加值13到0：AD转换结果的14位和													
具有12位精度的左对齐数据	指定1、2、3或4转换时间时	附加值15到0：AD转换结果的16位和															
	指定16个转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

43.2.6 ADRD:AD自诊断数据寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x01E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	DIAGST[1:0]		—	—	AD[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
11:0	AD[11:0]	将值11转换为0 12-bit A/D-converted value	R
13:12	—	这些位读为0。	R
15:14	DIAGST[1:0]	Self-Diagnosis Status 00：上电后不进行自诊断。01:使用0V电压执行自诊断。10：使用基准电压*1×12执行自诊断。11：使用基准电压*1执行自诊断。 有关自诊断的详细信息，请参阅第43.2.15节。ADCER：AD控制扩展寄存器。	R

Note: 显示了具有12位精度的右对齐数据的位分配示例。
注1.参考电压是指单元0的VREFH0和单元1的VREFH。

ADRD是一个16位只读寄存器，保存基于ADC12自诊断的AD转换结果。除了指示AD转换值的AD[11:0]位外，它还包括自诊断状态位(DIAGST[1:0])。

AD数据寄存器格式和AD转换精度的设置决定了该寄存器中数据的格式。

AD转换值加法和平均模式不能应用于AD自诊断功能。有关自诊断的详细信息，请参阅第43.2.15节。ADCER：AD控制扩展寄存器。

本节介绍每个条件的数据格式。本节所示的寄存器图和寄存器位表表示以12位精度进行左右对齐数据的位分配示例。

Table 43.15 Bit assignment for each right-justified accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	DIAGST[1:0]		—		AD[11:0]											

Table 43.16 Bit assignment for each left-justified accuracy

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	AD[11:0]												—		DIAGST[1:0]	

43.2.7 ADCSR : A/D Control Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADST	ADCS[1:0]		—	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DBLANS[4:0]	Double Trigger Channel Select These bits select one analog input channel for double trigger operation. The setting is only valid in double-trigger mode.	R/W
5	—	This bit is read as 0. The write value should be 0.	R/W
6	GBADIE	Group B Scan End Interrupt and ELC Event Enable Group B scan only works in group scan mode. 0: Disable ADC12i_GBADI (i = 0, 1) interrupt generation on group B scan completion. 1: Enable ADC12i_GBADI (i = 0, 1) interrupt generation on group B scan completion.	R/W
7	DBLE	Double Trigger Mode Select 0: Deselect double-trigger mode. 1: Select double-trigger mode.	R/W
8	EXTRG	Trigger Select*1 0: Start A/D conversion by the synchronous trigger (ELC). 1: Start A/D conversion by the asynchronous trigger (ADTRG0).	R/W
9	TRGE	Trigger Start Enable 0: Disable A/D conversion to be started by the synchronous or asynchronous trigger 1: Enable A/D conversion to be started by the synchronous or asynchronous trigger	R/W
10	—	These bits are read as 0. The write value should be 0.	R/W
11	—	These bits are read as 0. The write value should be 0.	R/W
12	—	These bits are read as 0. The write value should be 0.	R/W
14:13	ADCS[1:0]	Scan Mode Select 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
15	ADST	A/D Conversion Start 0: Stop A/D conversion process. 1: Start A/D conversion process.	R/W

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0), write 1 to both the TRGE and EXTRG bits in the ADCSR register and drive the ADTRG0 pin low. With these settings, the scan conversion process starts on detection of the falling edge of ADTRG0. The pulse width of the low-level input must be at least PCLKA 1.5 clock cycles.

Table 43.15 每个右对齐精度的位分配

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	DIAGST[1:0]		—		AD[11:0]											

Table 43.16 每个左对齐精度的位分配

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的左对齐数据	AD[11:0]												—		DIAGST[1:0]	

43.2.7 ADCSR:AD控制寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADST	ADCS[1:0]		—	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
4:0	DBLANS[4:0]	双触发通道选择 这些位选择一个模拟输入通道进行双触发操作。该设置仅在双触发模式下有效。	R/W
5	—	该位读取为0。写入值应为0。	R/W
6	GBADIE	B组扫描结束中断和ELC事件启用 B组扫描仅适用于组扫描模式。 0：在B组扫描完成时禁用ADC12i_GBADI(i=0 1)中断生成。 1：在B组扫描完成时启用ADC12i_GBADI(i=0 1)中断生成。	R/W
7	DBLE	双触发模式选择 0：取消选择双触发模式。1：选择双触发模式。	R/W
8	EXTRG	触发选择*1 0：通过同步触发（ELC）启动AD转换。1：通过异步触发（ADTRG0）启动AD转换。	R/W
9	TRGE	触发启动启用 0：禁止由同步或异步触发器启动的AD转换1：使能由同步或异步触发器启动的AD转换	R/W
10	—	这些位被读取为0。写入值应为0。	R/W
11	—	这些位被读取为0。写入值应为0。	R/W
12	—	这些位被读取为0。写入值应为0。	R/W
14:13	ADCS[1:0]	扫描模式选择 00：单次扫描模式01：组扫描模式10：连续扫描模式11：禁止设置	R/W
15	ADST	AD转换开始 0：停止AD转换过程。1：开始AD转换过程。	R/W

注1.使用外部引脚（异步触发）启动AD转换：
向外部引脚(ADTRG0)输入高电平信号后，向ADCSR寄存器的TRGE和EXTRG位写入1并将ADTRG0引脚驱动为低电平。通过这些设置，扫描转换过程在检测到ADTRG0的下降沿时开始。低电平输入的脉冲宽度必须至少为PCLKA1.5个时钟周期。

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The ADCSR register sets double-trigger mode and A/D conversion start trigger, enables or disables scan end interrupt, selects the scan mode, and starts or stops A/D conversion.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one channel for A/D conversion data duplication in double trigger mode. This can be selected by setting the binary value of the channel number to be duplicated. The A/D conversion results of the analog input of the channel selected in the DBLANS[4:0] bits are stored in A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when conversion is started by the second trigger.

In double trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers are invalid, and the channel selected in the DBLANS[4:0] bits is A/D converted instead.

When double trigger mode is used in group scan mode, double trigger control is only applied to group A and not to group B. Therefore, multiple channel analog input can be selected for group B even in double trigger mode.

Only set the DBLANS[4:0] bits when the ADST bit is 0. Do not set the DBLANS[4:0] bits at the same time that you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double trigger mode, select the channel using the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

A/D-converted data from the self-diagnosis function, temperature sensor output, and internal reference voltage cannot be used in double trigger mode

GBADIE bit (Group B Scan End Interrupt and ELC Event Enable)

The GBADIE bit enables or disables group B scan end interrupt (ADC12i_GBADI (i = 0, 1)) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double-trigger mode. Double-trigger mode can only be operated by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits.

Double-trigger operation is as follows:

1. The ADC12i_ADI (i = 0, 1) interrupt is not output on completion of the first conversion but on completion of the second conversion.
2. The A/D conversion results from the duplication channel (selected in DBLANS[4:0]) started by the first trigger are stored in A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplexing Register.

When the DBLE bit is set (double trigger mode is selected), the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Double trigger mode is deselected by setting DBLE to 0. Setting DBLE to 1 again enables the same double-trigger operation described in 1. and 2. for first time scanning with the first trigger.

Do not select double trigger mode in continuous scan mode. Software triggering cannot be used in double trigger mode. Always set the ADST bit to 0 before setting the DBLE bit. Do not set the DBLE bit at that same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous or asynchronous trigger as the trigger for starting A/D conversion.

In group-scan mode, the setting of this bit takes effect on the trigger selected for group A. For groups B, A/D conversion is started by the selected synchronous trigger regardless of this bit setting.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous and asynchronous triggers. In group scan mode, set this bit to 1.

ADCS[1:0] bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs of the channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops.

ADCSR寄存器设置双触发模式和AD转换启动触发，使能或禁止扫描结束中断，选择扫描模式，启动或停止AD转换。

DBLANS[4:0]位（双触发通道选择）

DBLANS[4:0]位选择一个通道用于双触发模式下的AD转换数据复制。这可以通过设置要复制的通道号的二进制值来选择。在DBLANS[4:0]位中选择的通道的模拟输入的AD转换结果在第一次触发开始转换时存储在AD数据寄存器y中，当转换开始时存储在AD数据双工寄存器中。第二个触发器。

双触发模式下，ADANSA0和ADANSA1寄存器选择的通道无效，DBLANS[4:0]位选择的通道改为AD转换。

在组扫描模式下使用双触发模式时，双触发控制仅适用于A组，不适用于B组。
因此，即使在双触发模式下，也可以为B组选择多通道模拟输入。

仅当ADST位为0时设置DBLANS[4:0]位。不要在将1写入ADST位的同时设置DBLANS[4:0]位。

要在双触发模式下进入AD转换值加法平均模式，请使用
ADANSA0和ADANSA1寄存器中的DBLANS[4:0]位。

自诊断功能、温度传感器输出和内部参考电压的D转换数据不能用于双触发模式

GBADIE位（B组扫描结束中断和ELC事件使能）

GBADIE位在组扫描模式下启用或禁用组B扫描结束中断(ADC12i_GBADI(i=0 1))。

DBLE位（双触发模式选择）

DBLE位选择或取消选择双触发模式。双触发模式只能由在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)操作。

双触发操作如下：

1.ADC12i_ADI(i=0 1)中断不是在第一次转换完成时输出，而是在第二次转换完成时输出。

2.由第一次触发启动的复制通道（在DBLANS[4:0]中选择）的AD转换结果存储在AD数据寄存器y中，由第二次触发启动的数据存储在AD数据双工寄存器中。

当设置DBLE位（选择双触发模式）时，在ADANSA0和ADANSA1寄存器中指定的通道无效。通过将DBLE设置为0来取消选择双触发模式。再次将DBLE设置为1可以启用与1.和2.中描述的相同的双触发操作，以使用第一个触发进行首次扫描。

在连续扫描模式下不要选择双触发模式。双触发模式下不能使用软件触发。在设置DBLE位之前，始终将ADST位设置为0。不要在将DBLE位设置为1的同时
ADST bit.

EXTRG bit (Trigger Select)

EXTRG位选择同步或异步触发作为启动AD转换的触发。

在组扫描模式下，该位的设置对A组选择的触发生效。对于B组，无论该位设置如何，都由选择的同步触发启动AD转换。

TRGE位（触发启动使能）

TRGE位通过同步和异步触发启用或禁用AD转换。在组扫描模式下，将此位设置为1。

ADCS[1:0]位（扫描模式选择）

ADCS[1:0]位选择扫描模式。

在单次扫描模式下，对ADANSA0中选择的通道的模拟输入执行AD转换，并且
ADANSA1寄存器，按通道号升序排列。当所有选定通道的1个AD转换周期完成时，扫描转换停止。

In continuous scan mode, when the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs of the channels selected with the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion repeats from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion stops even if scanning is in progress.

In group scan mode:

- Group A scanning is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in the ADSTRGR register. A/D conversion is performed on group A analog inputs of the channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.
- Group B scanning is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits. A/D conversion is performed on group B analog inputs of the channels selected in the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops.

If the conversion processes in group A and B occur at the same time, those conversions cannot be controlled separately. In this case, set group A Priority Control Setting bit (ADGSPCR.PGS) in the A/D Group Scan Priority Control Register (ADGSPCR) to 1 to assign a priority to group A conversion.

In group scan mode, select different channels and triggers for group A and group B.

Only set the ADCS[1:0] bits when the ADST bit is 0. Do not set the ADCS[1:0] bits at the same time that you write 1 to the ADST bit.

Table 43.17 Selectable targets for A/D conversion depending on scan and double-trigger mode settings

Scan mode setting	Double-trigger mode setting	Targets for A/D conversion				
		Self-diagnosis	Analog input (group A)	Analog input (group B)	Temperature sensor output	Internal reference voltage
Single scan	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	✓ (1 ch only)	—	—	—
Continuous scan	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	—	—	—	—
Group scan	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	—	✓ (1 ch only)	✓	✓	✓

Note: ✓: Selectable, —: Not selectable

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and the conversion target analog input.

[Setting conditions]

- 1 is written.
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when ADCSR.EXTRG is 0 and ADCSR.TRGE is 1.
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when ADCSR.TRGE is set to 1 in group scan mode.
- The asynchronous trigger is detected when the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1 and the ADSTRGR.TRSA[5:0] bits are set to 0x00.
- When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and each time A/D conversion on the group with the lowest priority is started.

[Clearing conditions]

- 0 is written.

在连续扫描模式下，当ADCSR.ADST位为1时，ADANSA0和ADANSA1寄存器选择的通道的模拟输入按通道编号的升序执行AD转换。当所有选定通道的1个AD转换周期完成时，AD转换从第一个通道开始重复。如果

ADCSR.ADST位在连续扫描期间设置为0，即使在扫描过程中AD转换也会停止。

在组扫描模式下：

●A组扫描由在ADSTRGR寄存器的TRSA[5:0]位中选择的同步触发(ELC)启动。AD转换在ADANSA0和ADANSA1寄存器中选择的通道的A组模拟输入上执行，按通道编号的升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。

●B组扫描由在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)启动。广告
转换是在ADANSB0和ADANSB1寄存器中选择的通道的B组模拟输入上执行的，按通道编号的升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。

如果A组和B组中的转换过程同时发生，则不能单独控制这些转换。在这种情况下，将AD组扫描优先级控制寄存器(ADGSPCR)中的A组优先级控制设置位(ADGSPCR.PGS)设置为1，以将优先级分配给A组转换。

在组扫描模式下，为A组和B组选择不同的通道和触发。

仅当ADST位为0时才设置ADCS[1:0]位。不要在向寄存器写入1的同时设置ADCS[1:0]位
ADST bit.

Table 43.17 AD转换的可选目标取决于扫描和双触发模式设置

扫描模式设置	双触发模式设置	AD转换的目标				
		Self-diagnosis	模拟输入（A组）	模拟输入（B组）	温度传感器输出	内部参考电压
单次扫描	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	✓ (1 ch only)	—	—	—
连续扫描	DBLE = 0	✓	✓	—	✓	✓
	DBLE = 1	—	—	—	—	—
组扫描	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	—	✓ (1 ch only)	✓	✓	✓

Note: :可选择 —:不可选择

ADST位（AD转换开始）

ADST位启动或停止AD转换过程。在ADST位设置为1之前，设置AD转换时钟、转换模式和转换目标模拟输入。

[Setting conditions]

●写入1。

●当ADCSR.EXTRG为0且ADCSR.TRGE为1时，检测在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)。

●在组扫描模式下，当ADCSR.TRGE设置为1时，检测到在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)。

●当ADCSR.TRGE和ADCSR.EXTRG位设置为1且ADSTRGR.TRSA[5:0]位设置为0x00时，检测到异步触发
。

●当启用组优先操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRP位设置为1，并且每次对最低组进行AD转换优先启动。

[Clearing conditions]

●写入0。

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- The A/D conversion of all the selected channels, the temperature sensor output, the internal reference voltage completes in single scan mode.
- Group A scan completes in group scan mode.
- Group B scan completes in group scan mode.
- When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRSCN bit is set to 1, and A/D conversion on the group with the lowest priority started by trigger completes.

Note: When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.
Note: When group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

43.2.8 ADANSA0 : A/D Channel Select Register A0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA 15	ANSA 14	ANSA 13	ANSA 12	ANSA 11	ANSA 10	ANSA 09	ANSA 08	ANSA 07	ANSA 06	ANSA 05	ANSA 04	ANSA 03	ANSA 02	ANSA 01	ANSA 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	A/D Conversion Channels Select Bit 15 (ANSA15) is associated with ANm15 and bit 0 (ANSA00) is associated with ANm00. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSA0 register selects analog input channels for A/D conversion. In group scan mode, this register selects group A channels.

Only set the ADANSA0 register when the ADCSR.ADST bit is 0.

ANSAn bits (A/D Conversion Channels Select)

The ADANSA0 register selects any combination of analog input channels for A/D conversion. The channels and the number of channels can be arbitrarily set.

In double trigger mode, the channels selected in the ADANSA0 register are invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

43.2.9 ADANSA1 : A/D Channel Select Register A1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA 31	ANSA 30	ANSA 29	ANSA 28	ANSA 27	ANSA 26	ANSA 25	ANSA 24	ANSA 23	ANSA 22	ANSA 21	ANSA 20	ANSA 19	ANSA 18	ANSA 17	ANSA 16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

●所有选定通道的AD转换、温度传感器输出、内部参考电压均在单次扫描模式下完成。

●A组扫描在组扫描模式下完成。
●B组扫描在组扫描模式下完成。
●当组优先操作模式使能时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRSCN位设置为1，最低优先级组的AD转换开始按触发器完成。

Note: 当启用组优先操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为1。
Note: 当启用组优先操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为0。当强制终止AD转换时，请按照清除程序ADST位。

43.2.8 ADANSA0:AD通道选择寄存器A0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA 15	ANSA 14	ANSA 13	ANSA 12	ANSA 11	ANSA 10	ANSA 09	ANSA 08	ANSA 07	ANSA 06	ANSA 05	ANSA 04	ANSA 03	ANSA 02	ANSA 01	ANSA 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	AD转换通道选择 位15(ANSA15)与ANm15相关联，位0(ANSA00)与ANm00相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSA0寄存器选择用于AD转换的模拟输入通道。在组扫描模式下，该寄存器选择A组通道。

仅当ADCSR.ADST位为0时设置ADANSA0寄存器。

ANSan位（AD转换通道选择）

ADANSA0寄存器为AD转换选择任意模拟输入通道组合。通道和通道数可以任意设置。

双触发模式下，ADANSA0寄存器中选择的通道无效，在ADANSA0寄存器中选择的通道无效。
改为在A组中选择ADCSR.DBLANS[4:0]位。

选择组扫描模式时，不要选择AD通道选择寄存器B0(ADANSB0)和AD通道选择寄存器B1(ADANSB1)中指定的通道。

43.2.9 ADANSA1:AD通道选择寄存器A1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x006

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSA 31	ANSA 30	ANSA 29	ANSA 28	ANSA 27	ANSA 26	ANSA 25	ANSA 24	ANSA 23	ANSA 22	ANSA 21	ANSA 20	ANSA 19	ANSA 18	ANSA 17	ANSA 16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSAn	A/D Conversion Channels Select Bit 15 (ANSA31) is associated with ANm31 and bit 0 (ANSA16) is associated with ANm16. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16 to 28(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSA1 register selects analog input channels for A/D conversion. In group scan mode, this register selects group A channels.

Only set the ADANSA1 register when the ADCSR.ADST bit is 0.

ANSAn bits (A/D Conversion Channels Select)

The ADANSA1 register selects any combination of analog input channels for A/D conversion. The channels and the number of channels can be arbitrarily set.

In double trigger mode, the channels selected in the ADANSA1 register are invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

43.2.10 ADANSB0 : A/D Channel Select Register B0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 15	ANSB 14	ANSB 13	ANSB 12	ANSB 11	ANSB 10	ANSB 09	ANSB 08	ANSB 07	ANSB 06	ANSB 05	ANSB 04	ANSB 03	ANSB 02	ANSB 01	ANSB 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	A/D Conversion Channels Select Bit 15 (ANSB15) is associated with ANm15 and bit 0 (ANSB00) is associated with ANm00. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSB0 selects analog input channels for A/D conversion in group B when group scan mode is selected. The ADANSB0 register is not used in any scan mode other than group scan mode.

Only set the ADANSB0 register when the ADCSR.ADST bit is 0.

ANSBn bits (A/D Conversion Channels Select)

The ADANSB0 register selects any combination of analog input channels in group B for A/D conversion when group scan mode is selected. The ADANSB0 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers or the ADCSR.DBLANS[4:0] bits in double trigger mode.

Bit	Symbol	Function	R/W
15:0	ANSAn	AD转换通道选择 位15(ANSA31)与ANm31相关联，位0(ANSA16)与ANm16相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 16 to 28(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSA1寄存器选择用于AD转换的模拟输入通道。在组扫描模式下，该寄存器选择A组通道。

仅当ADCSR.ADST位为0时设置ADANSA1寄存器。

ANSan位（AD转换通道选择）

ADANSA1寄存器为AD转换选择任意模拟输入通道组合。通道和通道数可以任意设置。

双触发模式下，ADANSA1寄存器中选择的通道无效，在ADANSA1寄存器中选择的通道无效。
改为在A组中选择ADCSR.DBLANS[4:0]位。

选择组扫描模式时，不要选择AD通道选择寄存器B0(ADANSB0)和AD通道选择寄存器B1(ADANSB1)中指定的通道。

43.2.10 ADANSB0:AD通道选择寄存器B0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x014

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 15	ANSB 14	ANSB 13	ANSB 12	ANSB 11	ANSB 10	ANSB 09	ANSB 08	ANSB 07	ANSB 06	ANSB 05	ANSB 04	ANSB 03	ANSB 02	ANSB 01	ANSB 00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	AD转换通道选择 位15(ANSB15)与ANm15相关联，位0(ANSB00)与ANm00相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSB0在选择组扫描模式时选择B组中AD转换的模拟输入通道。ADANSB0寄存器不用于除组扫描模式以外的任何扫描模式。

仅当ADCSR.ADST位为0时才设置ADANSB0寄存器。

ANSBn位（AD转换通道选择）

TheADANSB0registerselectsanycombinationofanaloginputchannelsingroupBforADconversionwhengroupscanmodeisselected.ADANSB0寄存器仅用于组扫描模式，不用于任何其他模式。

不要选择在ADANSA0和ADANSA1寄存器中选择的A组中指定的通道，或者
双触发模式下的ADCSR.DBLANS[4:0]位。

43.2.11 ADANSB1 : A/D Channel Select Register B1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x016

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 31	ANSB 30	ANSB 29	ANSB 28	ANSB 27	ANSB 26	ANSB 25	ANSB 24	ANSB 23	ANSB 22	ANSB 21	ANSB 20	ANSB 19	ANSB 18	ANSB 17	ANSB 16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	A/D Conversion Channels Select Bit 15 (ANSB31) is associated with ANm31 and bit 0 (ANSB16) is associated with ANm16. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16 to 28(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADANSB1 selects analog input channels for A/D conversion in group B when group scan mode is selected. The ADANSB1 register is not used in any scan mode other than group scan mode.

Only set the ADANSB1 register when the ADCSR.ADST bit is 0.

ANSBn bits (A/D Conversion Channels Select)

The ADANSB1 register selects any combination of analog input channels in group B for A/D conversion when group scan mode is selected. The ADANSB1 register is used for group scan mode only and not for any other modes.

Do not select channels specified in group A as selected in the ADANSA0 and ADANSA1 registers or the ADCSR.DBLANS[4:0] bits in double trigger mode.

43.2.12 ADADS0 : A/D-Converted Value Addition/Average Channel Select Register 0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS15	ADS14	ADS13	ADS12	ADS11	ADS10	ADS09	ADS08	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS15) is associated with ANm15 and bit 0 (ADS00) is associated with ANm00. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

ADSn bits (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1, 2, 3, 4, or 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits in the ADANSA0 register or the DBLANS[4:0] bits in the ADCSR register

43.2.11 ADANSB1:AD通道选择寄存器B1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x016

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ANSB 31	ANSB 30	ANSB 29	ANSB 28	ANSB 27	ANSB 26	ANSB 25	ANSB 24	ANSB 23	ANSB 22	ANSB 21	ANSB 20	ANSB 19	ANSB 18	ANSB 17	ANSB 16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ANSBn	AD转换通道选择 位15(ANSB31)与ANm31相关联，位0(ANSB16)与ANm16相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 16 to 28(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADANSB1在选择组扫描模式时选择B组中AD转换的模拟输入通道。ADANSB1寄存器不用于除组扫描模式以外的任何扫描模式。

仅当ADCSR.ADST位为0时设置ADANSB1寄存器。

ANSBn位（AD转换通道选择）

TheADANSB1registerselectsanycombinationofanaloginputchannelsingroupBforADconversionwhengroupscanmodeisselected.ADANSB1寄存器仅用于组扫描模式，不用于任何其他模式。

不要选择在ADANSA0和ADANSA1寄存器中选择的A组中指定的通道，或者双触发模式下的ADCSR.DBLANS[4:0]位。

43.2.12 ADADS0:D转换值加法平均通道选择寄存器0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x008

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS15	ADS14	ADS13	ADS12	ADS11	ADS10	ADS09	ADS08	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	一个D转换的增值平均渠道选择 位15(ADS15)与ANm15相关联，位0(ADS00)与ANm00相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

ADSn位（AD转换值加法平均通道选择）

ADSn位确定哪些AD转换通道要进行AD转换值加法平均。当一个与选择用于AD转换的通道相关的ADSn位设置为1，相应通道的模拟输入的AD转换按ADC[2:0]中的规定连续执行1、2、3、4或16次ADADC寄存器中的位。

当ADADC.AVEE位为0时，相加得到的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，加法所得结果的平均值存储在AD数据寄存器中。

ADSn位仅适用于为AD转换选择的通道：

●ADANSA0寄存器中的ANSan位或ADCSR寄存器中的DBLANS[4:0]位

- The ANSBn bits in the ADANSB0 register

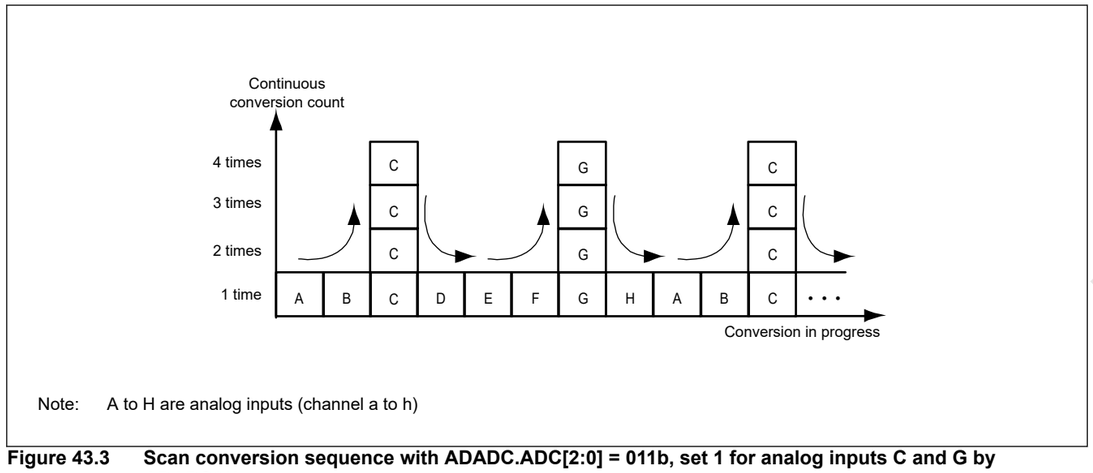
For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D data register.

Only set ADADS0 register bits when the ADCSR.ADST bit is 0.

Figure 43.3 shows a scanning operation sequence in which the ADADS0 register bits (channel c and g) are set to 1. In this figure:

- Addition mode is selected (ADADC.AVEE = 0)
- The number of conversions is set to 4 (ADADC.ADC[1:0] = 11b)
- The analog input channels (a to h) are selected by ADANSA0 register in continuous scan mode (ADCSR.ADCS[1:0] = 10b).

The conversion process begins with analog input A (channel a). The analog input C (channel c) conversion is performed successively 4 times and the added value is returned to A/D Data Register c (ADDRc). Next, the analog input D (channel d) conversion process is started. The analog input G (channel g) is performed successively 4 times and the added value is returned to A/D Data Register g (ADDRg). After conversion of analog input H (channel h), the conversion operation repeats in the same sequence starting with analog input A (channel a).



Note: A to H are analog inputs (channel a to h)

Figure 43.3 Scan conversion sequence with ADADC.ADC[2:0] = 011b, set 1 for analog inputs C and G by ADADS0/1

43.2.13 ADADS1 : A/D-Converted Value Addition/Average Channel Select Register 1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x00A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS31	ADS30	ADS29	ADS28	ADS27	ADS26	ADS25	ADS24	ADS23	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS31) is associated with ANm31 and bit 0 (ADS16) is associated with ANm16. 0: Do not select associated input channel. 1: Select associated input channel.	R/W

Note: n = 16 to 28(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

●ADANSB0寄存器中的ANSBn位

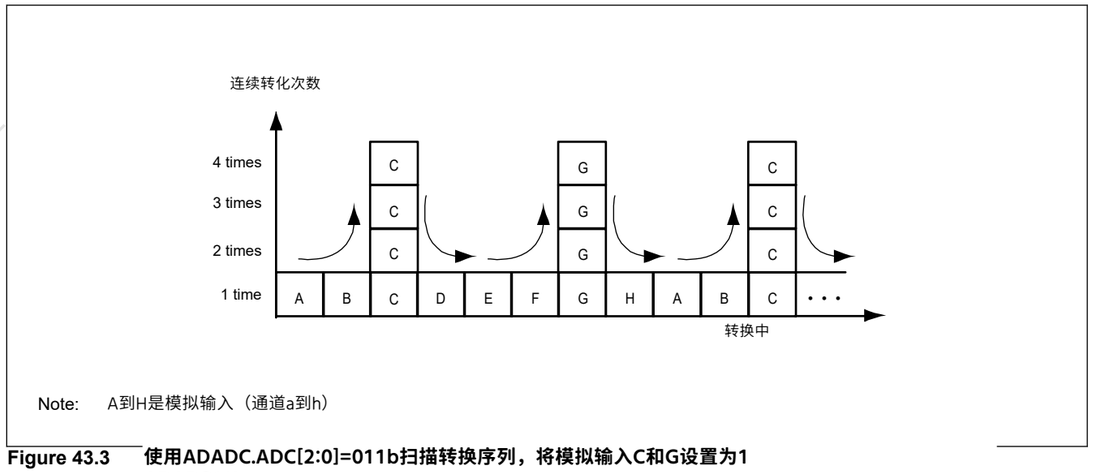
对于执行AD转换且未选择加法平均模式的通道，将执行正常的1次转换，并将转换结果存储在AD数据寄存器中。

仅当ADCSR.ADST位为0时设置ADADS0寄存器位。

图43.3显示了扫描操作序列，其中ADADS0寄存器位（通道c和g）设置为1。在该图中：

●选择加法模式（ADADC.AVEE=0）
●转换次数设置为4(ADADC.ADC[1:0]=11b)
●模拟输入通道（a到h）在连续扫描模式下由ADANSA0寄存器选择（ADCSR.ADCS[1:0]=10b）。

转换过程从模拟输入A（通道a）开始。模拟输入C（通道c）转换连续执行4次，相加后的值返回到AD数据寄存器c（ADDRc）。接下来，开始模拟输入D（通道d）转换过程。模拟输入G（通道g）连续执行4次，相加后的值返回到AD数据寄存器g（ADDRg）。模拟输入H（通道h）转换后，转换操作从模拟输入A（通道a）开始以相同的顺序重复。



Note: A到H是模拟输入（通道a到h）

Figure 43.3 使用ADADC.ADC[2:0]=011b扫描转换序列，将模拟输入C和G设置为1 ADADS0/1

43.2.13 ADADS1：一个D转换值加法平均通道选择寄存器1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x00A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADS31	ADS30	ADS29	ADS28	ADS27	ADS26	ADS25	ADS24	ADS23	ADS22	ADS21	ADS20	ADS19	ADS18	ADS17	ADS16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADSn	一个D转换的增值平均渠道选择 位15(ADS31)与ANm31相关联，位0(ADS16)与ANm16相关联。 0：不选择关联的输入通道。1：选择关联的输入通道。	R/W

Note: n = 16 to 28(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

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ADSn bits (A/D-Converted Value Addition/Average Channel Select)

The ADSn bits determine which A/D-converted channels are subject to A/D-converted value addition/averaging. When an ADSn bit associated with a channel selected for A/D conversion is set to 1, A/D conversion of the analog input of the respective channel is performed successively 1, 2, 3, 4, or 16 times, as specified in the ADC[2:0] bits in the ADADC register.

When the ADADC.AVEE bit is 0, the value obtained by addition is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition is stored in the A/D data register.

The ADSn bits apply only to channels that are selected for A/D conversion in:

- The ANSAn bits in the ADANSA1 register or the DBLANS[4:0] bits in the ADCSR register
- The ANSBn bits in the ADANSB1 register.

For channels on which the A/D conversion is performed and for which addition/average mode is not selected, a normal 1-time conversion is executed and the conversion result is stored in the A/D data register.

Only set ADADS1 register when the ADCSR.ADST bit is 0.

43.2.14 ADADC : A/D-Converted Value Addition/Average Count Select Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADC[2:0]	Addition/Average Count Select 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4-time conversion (three additions) 1 0 1: 16-time conversion (15 additions) Others: Setting prohibited	R/W
6:3	—	These bits are read as 0. The write value should be 0.	R/W
7	AVEE	Average Mode Select 0: Enable addition mode 1: Enable average mode	R/W

ADADC sets the addition or average mode and addition count for A/D conversion. Table 43.18 lists the settable combinations of ADADC register.

Table 43.18 Settable combinations of ADADC register

Average mode select (AVEE)	Conversion time				
	1-time	2-times	3-times	4-times	16-times
1'b0	✓	✓	✓	✓	✓
1'b1	✓	✓	—	✓	—

Note: ✓: Selectable, —: Not selectable

ADC[2:0] bits (Addition/Average Count Select)

The ADC[2:0] bits set the addition count in all channels for which A/D conversion and addition/average mode are selected, including the channel selected in double trigger mode with the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of the temperature sensor output and internal reference voltage.
When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b.

ADSn位（AD转换值加法平均通道选择）

ADSn位确定哪些AD转换通道要进行AD转换值加法平均。当一个
与选择用于AD转换的通道相关的ADSn位设置为1，相应通道的模拟输入的AD转换按ADC[2:0]中的规定连续执行1、2、3、4或16次ADADC寄存器中的位。

当ADADC.AVEE位为0时，相加得到的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，加法所得结果的平均值存储在AD数据寄存器中。

ADSn位仅适用于为AD转换选择的通道：

●ADANSA1寄存器中的ANSan位或ADCSR寄存器中的DBLANS[4:0]位

●ADANSB1寄存器中的ANSBn位。

对于执行AD转换且未选择加法平均模式的通道，将执行正常的1次转换，并将转换结果存储在AD数据寄存器中。

仅当ADCSR.ADST位为0时设置ADADS1寄存器。

43.2.14 ADADC:D转换值加法平均计数选择寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x00C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	AVEE	—	—	—	—	ADC[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	ADC[2:0]	加法平均计数选择 000：1次转换（不加，同普通转换）001：2次转换（1次加法）01 0：3次转换（2次加法）011：4次转换（3次加法）101：16次转换 （15次加法） Others: 禁止设定	R/W
6:3	—	这些位被读取为0。写入值应为0。	R/W
7	AVEE	平均模式选择 0：启用加法模式1：启用 平均模式	R/W

ADADC设置AD转换的加法或平均模式和加法计数。表43.18列出了ADADC寄存器的可设置组合。

Table 43.18 ADADC寄存器的可设置组合

平均模式选择 (AVEE)	转换时间				
	1-time	2-times	3-times	4-times	16-times
1'b0	✓	✓	✓	✓	✓
1'b1	✓	✓	—	✓	—

Note: :可选择 —:不可选择

ADC[2:0]位（加法平均计数选择）

ADC[2:0]位设置选择了AD转换和加法平均模式的所有通道的加法计数，包括使用ADCSR.DBLANS[4:0]位在双触发模式中选择的通道。该计数也适用于温度传感器输出和内部参考电压的AD转换。执行自诊断时(ADCER.DIAGM=1)，请勿将ADC[2:0]位设置为000b以外的任何值。

AVEE bit (Average Mode Select)

The AVEE bit selects addition or average mode in all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double-trigger mode in the ADCSR.DBLANS[4:0] bits, temperature sensor output, internal reference voltage.

43.2.15 ADCER : A/D Control Extended Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x00E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	These bits are read as 0. The write value should be 0.	R/W
2:1	ADPRC[1:0]	A/D Conversion Accuracy Specify 0 0: 12-bit accuracy 0 1: 10-bit accuracy 1 0: 8-bit accuracy 1 1: Setting prohibited	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	ACE	A/D Data Register Automatic Clearing Enable 0: Disable automatic clearing 1: Enable automatic clearing	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
9:8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select 0 0: Setting prohibited when self-diagnosis is enabled 0 1: 0 volts 1 0: Reference voltage*1 × 1/2 1 1: Reference voltage*1	R/W
10	DIAGLD	Self-Diagnosis Mode Select 0: Select rotation mode for self-diagnosis voltage 1: Select mixed mode for self-diagnosis voltage	R/W
11	DIAGM	Self-Diagnosis Enable 0: Disable ADC12 self-diagnosis 1: Enable ADC12 self-diagnosis	R/W
14:12	—	These bits are read as 0. The write value should be 0.	R/W
15	ADRFMT	A/D Data Register Format Select 0: Select right-justified for the A/D data register format 1: Select left-justified for the A/D data register format	R/W

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

ADPRC[1:0] bit (A/D Conversion Accuracy Specify)

The ADPRC[1:0] bits set the A/D conversion accuracy. Changing the A/D conversion accuracy also changes the bit width of valid data stored in the result register and the A/D conversion time. For details, see section 43.3.7. Analog Input Sampling and Scan Conversion Timesection 45.3.6, Analog Input Sampling and Scan Conversion Time. Only set the ADPRC[1:0] bits while the ADCSR.ADST bit is 0.

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0) of the ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR register after any of these registers is read by the CPU or DTC. Automatic clearing of the A/D data registers enables detection of failures that are not updated in the A/D data registers. For details, see section 43.3.8. Usage Example of A/D Data Register Automatic Clearing Function.

AVEE位（平均模式选择）

AVEE位在选择了AD转换和加法平均模式的所有通道中选择加法或平均模式，包括在ADCSR.DBLANS[4:0]位中选择的双触发模式的通道、温度传感器输出、内部参考电压.

43.2.15 ADCER:AD控制扩展寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x00E

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	这些位被读取为0。写入值应为0。	R/W
2:1	ADPRC[1:0]	AD转换精度指定 00：12位精度01：10位精度10：8位精度11：禁止设置	R/W
4:3	—	这些位被读取为0。写入值应为0。	R/W
5	ACE	AD数据寄存器自动清零使能 0：关闭自动清零1：开启自动清零	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
9:8	DIAGVAL[1:0]	自诊断转换电压选择 00：自诊断有效时禁止设置01：0伏特10：参考电压*1×1211：参考电压*1	R/W
10	DIAGLD	自诊断模式选择 0：自诊断电压选择旋转模式1：自诊断电压选择混合模式	R/W
11	DIAGM	Self-Diagnosis Enable 0：禁用ADC12自诊断1：启用ADC12自诊断	R/W
14:12	—	这些位被读取为0。写入值应为0。	R/W
15	ADRFMT	AD数据寄存器格式选择 0：AD数据寄存器格式选择右对齐1：AD数据寄存器格式选择左对齐	R/W

注1.参考电压是指单元0的VREFH0和单元1的VREFH。

ADPRC[1:0]位（AD转换精度指定）

ADPRC[1:0]位设置AD转换精度。更改AD转换精度也会更改存储在结果寄存器中的有效数据的位宽和AD转换时间。详见43.3.7节。模拟输入采样和扫描转换时间第45.3.6节，模拟输入采样和扫描转换时间。只设置

ADPRC[1:0]位，而ADCSR.ADST位为0。

ACE位（AD数据寄存器自动清除使能）

ACE位启用或禁用ADDRy、ADRD、ADDBLDR、ADDBLDRA、
在CPU或DTC读取这些寄存器中的任何一个之后，ADDBLDRB、ADTSDR或ADOCDR寄存器。自动清除AD数据寄存器可以检测未在AD数据寄存器中更新的故障。详见43.3.8节。AD数据寄存器自动清除功能的使用示例。

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DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis fixed voltage mode. For details, see the DIAGLD bit description.

Do not execute self-diagnosis by setting the DIAGLD bit to 1 when the DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis.

Setting the DIAGLD bit to 0 selects conversion of the voltages in rotation mode, where 0 V, the reference voltage × 1/2, and the reference voltage are converted, in that order. After reset and when self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The self-diagnosis voltage value does not return to 0 V when scan conversion completes. When scan conversion is restarted, rotation starts at the voltage value following the previous value.

Setting the DIAGLD bit to 1 selects fixed voltage, in which the fixed voltage specified in the ADCER.DIAGVAL[1:0] bits is converted. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

Only set the DIAGLD bit when the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis.

Self-diagnosis is used to detect a failure of the ADC12. In self-diagnosis mode, one of the three voltage values (0 V, the reference voltage × 1/2, or the reference voltage) is converted. When conversion completes, information on the converted voltage and the conversion result is stored into the A/D Self-Diagnosis Data Register (ADRD). The ADRD register can be read to determine whether the conversion result falls within the normal or abnormal range.

Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. In double trigger mode (ADCSR.DBLE = 1), self-diagnosis (DIAGM = 0) is deselected. When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately for group A and group B.

Only set the DIAGM bit when the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for data to be stored in the ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD register.

Only set the ADRFMT bit when the ADCSR.ADST bit is 0.

43.2.16 ADSTRGR : A/D Conversion Start Trigger Select Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x010

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B Select the A/D conversion start trigger for group B in group scan mode.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W
13:8	TRSA[5:0]	A/D Conversion Start Trigger Select Select the A/D conversion start trigger in single scan mode and continuous scan mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
15:14	—	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits must only be set in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B,

DIAGVAL[1:0]位（自诊断转换电压选择）

DIAGVAL[1:0]位选择用于自诊断固定电压模式的电压值。有关详细信息，请参见DIAGLD位说明。

当DIAGVAL[1:0]位设置为00b时，不要通过将DIAGLD位设置为1来执行自诊断。

DIAGLD位（自诊断模式选择）

DIAGLD位选择是旋转三个电压值还是使用固定电压进行自诊断。

将DIAGLD位设置为0选择在旋转模式下转换电压，其中0V、参考电压×12和参考电压按此顺序转换。复位后，选择自诊断电压旋转模式时，从0V开始执行自诊断。扫描转换完成时，自诊断电压值不会返回到0V。重新开始扫描转换时，从前一个值之后的电压值开始旋转。

将DIAGLD位设置为1选择固定电压，其中转换ADCER.DIAGVAL[1:0]位中指定的固定电压。如果将固定模式切换到旋转模式，则从固定电压值开始旋转。

仅当ADCSR.ADST位为0时设置DIAGLD位。

DIAGM bit (Self-Diagnosis Enable)

DIAGM位启用或禁用自诊断。

自诊断用于检测ADC12的故障。在自诊断模式下，转换三个电压值（0V、参考电压×12或参考电压）之一。转换完成后，转换电压和转换结果的信息将存储到AD自诊断数据寄存器(ADRD)中。可以读取ADRD寄存器来确定转换结果是否在正常或异常范围内。

自诊断在每次扫描开始时执行一次，并转换三个电压之一。在双触发模式(ADCSR.DBLE=1)中，自诊断(DIAGM=0)被取消选择。在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

仅当ADCSR.ADST位为0时设置DIAGM位。

ADRFMT位（AD数据寄存器格式选择）

ADRFMT位指定要存储在ADDRy、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR、ADCMPDR01、ADWINLLB、ADWINULB或ADRD寄存器。

仅当ADCSR.ADST位为0时才设置ADRFMT位。

43.2.16 ADSTRGR:AD转换开始触发选择寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x010

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	TRSB[5:0]	B组的AD转换开始触发选择 在组扫描模式下选择B组的AD转换启动触发。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W
13:8	TRSA[5:0]	AD转换开始触发选择 在单次扫描模式和连续扫描模式中选择AD转换启动触发。在组扫描模式下，选择A组的AD转换启动触发。	R/W
15:14	—	这些位被读取为0。写入值应为0。	R/W

TRSB[5:0]位（B组的AD转换开始触发选择）

TRSB[5:0]位选择触发以开始扫描组B中选择的模拟输入。TRSB[5:0]位只能在组扫描模式下设置，不得用于任何其他扫描模式。对于B组的扫描转换开始触发，

setting a software trigger or an asynchronous trigger is prohibited. In group scan mode, set the TRSB[5:0] bits to a value other than 0x00 and set the ADCSR.TRGE bit to 1.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 0x3F. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (t_{SCAN}). If the issuance period is less than t_{SCAN}, A/D conversion by the trigger might have no effect.

When the GPT module is selected as an A/D conversion start trigger, a delay for synchronization processing occurs. For details, see section 43.3.7. Analog Input Sampling and Scan Conversion Time.

Table 43.19 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

Table 43.19 Selection of A/D conversion start sources in the TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselected state	—	1	1	1	1	1	1
ELC_AD00 (unit 0) and ELC_AD10 (unit 1)	ELC	0	0	1	0	0	1
ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	0
ELC_AD00 (unit 0) and ELC_AD10 (unit 1), ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	1

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode, or the trigger to start scanning of group A analog inputs in group scan mode. When scanning is executed in group scan mode or double trigger mode, software trigger or asynchronous trigger is prohibited.

- When using a synchronous trigger (ELC), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 0.
- When using the asynchronous trigger (ADTRG0), set the TRGE bit in the ADCSR register to 1 and set the EXTRG bit in the ADCSR register to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits.

The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger might have no effect.

Table 43.20 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Table 43.20 Selection of A/D activation sources in the TRSA[5:0] bits (1 of 2)

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselected state	—	1	1	1	1	1	1
ADTRGn (n = 0, 1)	Input pin for the trigger	0	0	0	0	0	0

禁止设置软件触发或异步触发。在组扫描模式下，将TRSB[5:0]位设置为0x00以外的值，并将ADCSR.TRGE位设置为1。

当A组在组扫描模式下具有优先权时，将ADGSPCR.GBRP位设置为1允许B组在单次扫描模式下连续工作。将ADGSPCR.GBRP位设置为1时，将TRSB[5:0]位设置为0x3F。转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发器的AD转换可能无效。

WhentheGPTmoduleisselectedasanADconversionstarttrigger adelayforsynchronizationprocessingoccurs.详见43.3.7节。模拟输入采样和扫描转换时间。

表43.19列出了在TRSB[5:0]位中选择的AD转换启动源。

Table 43.19 在TRSB[5:0]位中选择AD转换起始源

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
触发源取消选择状态	—	1	1	1	1	1	1
ELC_AD00 (unit 0) and ELC_AD10 (unit 1)	ELC	0	0	1	0	0	1
ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	0
ELC_AD00 (unit 0) and ELC_AD10 (unit 1), ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	1

TRSA[5:0]位（AD转换开始触发选择）

TRSA[5:0]位选择触发以在单次扫描模式和连续扫描模式下启动AD转换，或在组扫描模式下选择启动A组模拟输入扫描的触发。在组扫描模式或双触发模式下执行扫描时，禁止软件触发或异步触发。

●使用同步触发(ELC)时，将ADCSR寄存器中的TRGE位设置为1，并将ADCSR寄存器中的EXTRG位设置为0。

●使用异步触发（ADTRG0）时，将ADCSR寄存器的TRGE位设置为1，并将ADCSR寄存器的EXTRG位设置为1。

●无论ADCSR.TRGE位、ADCSR.EXTRG位或TRSA[5:0]位的设置如何，都启用软件触发(ADCSR.ADST)。

转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发的AD转换可能无效。

表43.20列出了在TRSA[5:0]位中选择的AD转换起始源。

Table 43.20 在TRSA[5:0]位中选择AD激活源（1of2）

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
触发源取消选择状态	—	1	1	1	1	1	1
ADTRGn (n = 0, 1)	触发器的输入引脚	0	0	0	0	0	0

Table 43.20 Selection of A/D activation sources in the TRSA[5:0] bits (2 of 2)

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
ELC_AD00 (unit 0) and ELC_AD10 (unit 1)	ELC	0	0	1	0	0	1
ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	0
ELC_AD00 (unit 0) and ELC_AD10 (unit 1), ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	1

43.2.17 ADEXICR : A/D Conversion Extended Input Control Registers

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x012

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select 0: Do not select addition/average mode for temperature sensor output. 1: Select addition/average mode for temperature sensor output.	R/W
1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select 0: Do not select addition/average mode for internal reference voltage. 1: Select addition/average mode for internal reference voltage.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
8	TSSA	Temperature Sensor Output A/D Conversion Select 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output	R/W
9	OCSA	Internal Reference Voltage A/D Conversion Select 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage	R/W
10	TSSB	Temperature Sensor Output A/D Conversion Select for Group B 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output	R/W
11	OCSB	Internal Reference Voltage A/D Conversion Select for Group B 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy (see section 43.2.6. ADRD : A/D Self-Diagnosis Data Register). When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Temperature sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.

Table 43.20 在TRSA[5:0]位中选择AD激活源（2个中的2个）

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
ELC_AD00 (unit 0) and ELC_AD10 (unit 1)	ELC	0	0	1	0	0	1
ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	0
ELC_AD00 (unit 0) and ELC_AD10 (unit 1), ELC_AD01 (unit 0) and ELC_AD11 (unit 1)	ELC	0	0	1	0	1	1

43.2.17 ADEXICR:AD转换扩展输入控制寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x012

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSSAD	温度传感器输出AD转换值加法平均模式选择 0：温度传感器输出不选择加法平均模式。1：温度传感器输出选择加法平均模式。	R/W
1	OCSAD	内部参考电压AD转换值加法平均模式选择 0：内部参考电压不选择加法平均模式。1：选择内部参考电压的加法平均模式。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W
8	TSSA	温度传感器输出AD转换选择 0：禁止温度传感器输出AD转换1：使能温度传感器输出AD转换	R/W
9	OCSA	内部参考电压AD转换选择 0：禁止内部参考电压AD转换1：使能内部参考电压AD转换	R/W
10	TSSB	B组温度传感器输出AD转换选择 0：禁止温度传感器输出AD转换1：使能温度传感器输出AD转换	R/W
11	OCSB	B组的内部参考电压AD转换选择 0：禁止内部参考电压AD转换1：使能内部参考电压AD转换	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W

TSSAD位（温度传感器输出AD转换值加法平均模式选择）

当TSSAD位设置为1时，选择温度传感器输出的AD转换并连续执行ADADC中ADC[2:0]位指定的次数。最大加法计数因转换精度而异（参见第43.2.6节。ADRD：AD自诊断数据寄存器）。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD温度传感器数据寄存器(ADTSDR)。当ADADC.AVEE位为1时，平均值返回给ADTSDR。

Only set the TSSAD bit while the ADCSR.ADST bit is 0.

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy (see section 43.2.6. ADRD : A/D Self-Diagnosis Data Register). When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADOCDR.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output for group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the temperature sensor output is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the TSSA bit while the ADCSR.ADST bit is 0.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage for group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the internal reference voltage is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the OCSA bit while the ADCSR.ADST bit is 0. In addition, wait for 400 ns or more after the OCSA bit is set to 1 before starting A/D conversion.

TSSB bit (Temperature Sensor Output A/D Conversion Select for Group B)

The TSSB bit selects A/D conversion of the temperature sensor output for group B in group scan mode. Only set the TSSB bit while the ADCSR.ADST bit is 0. Do not set the TSSB bit to 1 while the TSSA bit is 1.

OCSB bit (Internal Reference Voltage A/D Conversion Select for Group B)

The OCSB bit selects A/D conversion of the internal reference voltage for group B in group scan mode. Only set the OCSB bit while the ADCSR.ADST bit is 0. Do not set the OCSB bit to 1 while the OCSA bit is 1. Moreover, start the A/D conversion after waiting for 400 ns or more after the OCSB bit is set to 1.

43.2.18 ADSSTRn/ADSSTRL/ADSSTRT/ADSSTRO : A/D Sampling State Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0E0 + 0x1 × n (n = 0 to 10, 12, 13, m = 0)
0x0E0 + 0x1 × n (n = 0 to 2, m = 1)
0x0DD (ADSSTRL)
0x0DE (ADSSTRT)
0x0DF (ADSSTRO)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]							
Value after reset:	0	0	0	0	1	0	1	1

Bit	Symbol	Function	R/W
7:0	SST[7:0]	Sampling Time Setting These bits set the sampling time in the range from 5 to 255 states.	R/W

The ADSSTRn register sets the sampling time for analog input.

The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow. The set value indicates the time for one ADCLK cycle, and the required sampling time is specified by the voltage conditions. about detail, see section 53.5. ADC12 Characteristics

The lower limit of the sampling time setting depends on the frequency ratio:

仅在ADCSR.ADST位为0时设置TSSAD位。

OCSAD位（内部参考电压AD转换值加法平均模式选择）

当OCSAD位设置为1时，选择内部参考电压的AD转换，并按ADADC的ADC[2:0]位指定的次数连续执行。最大加法计数因转换精度而异（参见第43.2.6节。ADRD：AD自诊断数据寄存器）。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD内部参考电压数据寄存器（ADocDR）。当ADADC.AVEE位为1时，平均值返回给ADOCDR。

仅在ADCSR.ADST位为0时设置OCSAD位。

TSSA位（温度传感器输出AD转换选择）

TSSA位在单次扫描模式、连续扫描模式或组扫描模式下选择A组温度传感器输出的AD转换。WhenADconversionofthetemperaturesensoroutputisselectedandperformed settheADCSR.DBLEbitto0.

仅在ADCSR.ADST位为0时设置TSSA位。

OCSA位（内部参考电压AD转换选择）

OCSA位在单次扫描模式、连续扫描模式或组扫描模式下选择A组内部参考电压的AD转换。WhenADconversionoftheinternalreferencevoltageisselectedandperformed settheADCSR.DBLEbitto0.

仅在ADCSR.ADST位为0时设置OCSA位。此外，在OCSA位设置为1后等待400ns或更长时间，然后再开始AD转换。

TSSB位（B组的温度传感器输出AD转换选择）

TSSB位选择组扫描模式下B组温度传感器输出的AD转换。仅在ADCSR.ADST位为0时设置TSSB位。不要在TSSA位为1时将TSSB位设置为1。

OCSB位（B组的内部参考电压AD转换选择）

OCSB位选择组扫描模式下B组内部参考电压的AD转换。仅在ADCSR.ADST位为0时设置OCSB位。不要在OCSA位为1时将OCSB位设置为1。此外，在OCSB位设置为1后等待400ns或更长时间后开始AD转换.

43.2.18 ADSSTRnADSSTRLADSSTRTADSSTRO:AD采样状态寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0E0 + 0x1 × n (n = 0 to 10, 12, 13, m = 0)
0x0E0 + 0x1 × n (n = 0 to 2, m = 1)
0x0DD (ADSSTRL)
0x0DE (ADSSTRT)
0x0DF (ADSSTRO)

Bit position:	7	6	5	4	3	2	1	0
Bit field:	SST[7:0]							
重置后的值：	0	0	0	0	1	0	1	1

Bit	Symbol	Function	R/W
7:0	SST[7:0]	采样时间设置 这些位在5到255个状态范围内设置采样时间。	R/W

ADSSTRn寄存器设置模拟输入的采样时间。

如果模拟输入信号源的阻抗太高而无法保证足够的采样时间，或者如果ADCLK时钟很慢，则可以调整采样时间。设定值表示一个ADCLK周期的时间，所需的采样时间由电压条件指定。有关详细信息，请参阅第53.5节。ADC12特性

采样时间设置的下限取决于频率比：

- If the frequency ratio of PCLKA to PCLKC (ADCLK) = 1:1, 2:1, 4:1, or 8:1 the sampling time must be set to a value of more than 5 states
- If the frequency ratio of PCLKA to PCLKC (ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 43.21 shows the relationship between the A/D Sampling State Register and the associated channels. For details, see section 43.3.7. Analog Input Sampling and Scan Conversion Time.

Only set the SST[7:0] bits when the ADCSR.ADST bit is 0.

Table 43.21 Relationship between A/D sampling state register and associated channels

Bit name	Associated channels
ADSSTRn.SST[7:0] bits (n = 0 to 10, 12, 13(unit 0), 0 to 2(unit 1))*1	AN000 to AN010, AN012, AN013, AN100 to AN102
ADSSTRL.SST[7:0] bits	AN116 to AN128
ADSSTRT.SST[7:0] bits	Temperature sensor output
ADSSTRO.SST[7:0] bits	Internal reference voltage

Note 1. When the self-diagnosis function is selected, the sampling time set in the ADSSTR0.SST[7:0] bits is applied.

43.2.19 ADDISCR : A/D Disconnection Detection Control Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x07A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	ADNDIS[3:0]	Disconnection Detection Assist Setting 0x00: The disconnection detection assist function is disabled 0x01: Setting prohibited Others: The number of states for the discharge or precharge period.	R/W
4	PCHG	Precharge/discharge select 0: Discharge 1: Precharge	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge, and the period of precharge or discharge for the A/D disconnection detection assist function. Only set the ADDISCR register when the ADCSR.ADST bit is 0. When the temperature sensor output or internal reference voltage is converted, the A/D converter executes discharge automatically.

Disable the disconnection detection assist function if any of the following functions are used:

- The temperature sensor
- The internal reference voltage
- A/D self-diagnosis

ADNDIS[3:0] bits (Disconnection Detection Assist Setting)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

●如果PCLKA与PCLKC(ADCLK)的频率比=1:1、2:1、4:1或8:1，则必须将采样时间设置为超过5个状态的值

●如果PCLKA与PCLKC(ADCLK)的频率比=1:2或1:4，则必须将采样时间设置为6个以上状态的值。

表43.21显示了AD采样状态寄存器和相关通道之间的关系。详见43.3.7节。模拟输入采样和扫描转换时间。

仅当ADCSR.ADST位为0时设置SST[7:0]位。

Table 43.21 AD采样状态寄存器与相关通道的关系

位名称	关联频道
ADSSTRn.SST[7:0]位（n=0到10、12、13（单元0）、0到2（单元1））*1	AN000 to AN010, AN012, AN013, AN100 to AN102
ADSSTRL.SST[7:0] bits	AN116 to AN128
ADSSTRT.SST[7:0] bits	温度传感器输出
ADSSTRO.SST[7:0] bits	内部参考电压

注1.选择自诊断功能时，应用ADSSTR0.SST[7:0]位中设置的采样时间。

43.2.19 ADDISCR:AD断线检测控制寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x07A

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PCHG	ADNDIS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	ADNDIS[3:0]	断线检测辅助设置 0x00：断线检测辅助功能禁用0x01：设置禁止 其他：放电或预充电期的状态数。	R/W
4	PCHG	Precharge/discharge select 0: Discharge 1: Precharge	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

ADDISCR寄存器选择预充电或放电，以及AD断线检测辅助功能的预充电或放电周期。仅当ADCSR.ADST位为0时才设置ADDISCR寄存器。当温度传感器输出或内部参考电压转换时，AD转换器自动执行放电。

如果使用以下任何功能，请禁用断线检测辅助功能：

●温度传感器

●内部参考电压

- A/D self-diagnosis

ADNDIS[3:0]位（断线检测辅助设置）

ADNDIS[3:0]位指定预充电或放电周期。当ADNDIS[3:0]=0000b时，断线检测辅助功能被禁用。禁止将ADNDIS[3:0]位设置为0001b。除了ADNDIS[3:0]=0000b或0001b时，指定值表示预充电或放电期间的状态数。当ADNDIS[3:0]位设置为0000b或0001b以外的任何值时，将启用断线检测辅助功能。

PCHG bit (Precharge/discharge select)

The PCHG bit selects either precharge or discharge.

43.2.20 ADGSPCR : A/D Group Scan Priority Control Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x080

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GBRP	LGRRS	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS	Group Priority Operation Setting*1 0: Operate without group priority control. 1: Operate with group priority control.	R/W
1	GBRSCN	Lower-Priority Group Restart Setting (enabled only when PGS = 1 and reserved when PGS = 0.) 0: Disable rescanning of the group that was stopped in group priority operation 1: Enable rescanning of the group that was stopped in group priority operation.	R/W
13:2	—	These bits are read as 0. The write value should be 0.	R/W
14	LGRRS	Restart Channel Select Enabled only when PGS = 1 and GBRSCN = 1. 0: Start rescanning from the first channel for scanning 1: Start rescanning from the channel for which A/D conversion is not completed.	R/W
15	GBRP	Single Scan Continuous Start*2 (enabled only when PGS = 1 and reserved when PGS = 0.) 0: Single scan is not continuously activated. 1: Single scan for the group with the lower-priority is continuously activated.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting PGS to 1. Operation is not guaranteed if these bits are set to any other value.

Note 2. When the GBRP bit is set to 1, single scan is performed continuously for the group with the lower-priority regardless of the setting in the GBRSCN bit.

PGS bit (Group Priority Operation Setting)

Set the PGS bit to 1 to enable group priority operation.

The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if the bits are set to any other value.

When the PGS bit is set to 0, a clear operation must be performed by software as described in section 43.6.3. Constraints on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings described in section 43.3.4.3. Group Priority Operation.

GBRSCN bit (Lower-Priority Group Restart Setting)

The GBRSCN bit controls the restarting of scan operation in group priority operation.

When the GBRSCN bit is set to 1, if the scan operation of a lower-priority group is stopped by a trigger input of a priority group, the lower-priority group scanning is restarted on completion of the priority group scanning. If a trigger of a lower-priority group is input during scanning of the priority group, the lower-priority group scanning is started on completion of the priority group scanning.

When the GBRSCN bit is set to 0, triggers input during scanning are ignored. Set the GBRSCN bit while the ADCSR.ADST bit is 0.

LGRRS bit (Restart Channel Select)

This bit sets the channel from which rescanning is to be started in group priority operation. The setting of the LGRRS bit is valid when the PGS and GBRSCN bits are 1.

PCHG bit (Precharge/discharge select)

PCHG位选择预充电或放电。

43.2.20 ADGSPCR:AD组扫描优先级控制寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x080

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	GBRP	LGRRS	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PGS	组优先操作设置*1 0：无组优先控制运行。1：以组优先控制运行。	R/W
1	GBRSCN	低优先级组重启设置（仅在PGS=1时启用，在PGS=0时保留。） 0：禁止重新扫描在组优先操作中停止的组1：允许重新扫描在组优先操作中停止的组。	R/W
13:2	—	这些位被读取为0。写入值应为0。	R/W
14	LGRRS	重启频道选择 仅当PGS=1且GBRSCN=1时启用。 0：从第一个扫描通道开始重新扫描1：从未完成AD转换的通道开始重新扫描。	R/W
15	GBRP	单次扫描连续启动*2 （仅在PGS=1时启用，在PGS=0时保留。） 0：单次扫描不连续激活。1：连续激活低优先级组的单次扫描。	R/W

注1.ADCSR.ADCS[1:0]位必须在PGS设置为1之前设置为01b（组扫描模式）。如果这些位设置为任何其他值，则无法保证操作。

注2.当GBRP位设置为1时，无论GBRSCN位的设置如何，都会对优先级较低的组连续执行单次扫描。

PGS位（组优先操作设置）

将PGS位设置为1以启用组优先操作。

在将PGS位设置为1之前，必须将ADCSR.ADCS[1:0]位设置为01b（组扫描模式）。如果这些位设置为任何其他值，则无法保证操作。

当PGS位设置为0时，必须通过软件执行清除操作，如第43.6.3节所述。约束停止AD转换。当PGS位设置为1时，使用第43.3.4.3节中描述的设置。团体优先Operation.

GBRSCN位（低优先级组重启设置）

GBRSCN位控制组优先操作中扫描操作的重新启动。

当GBRSCN位被设置为1时，如果低优先级组的扫描操作被优先级组的触发输入停止，则低优先级组扫描在优先级组扫描完成时重新开始。如果在优先级组扫描期间输入了较低优先级组的触发，则在完成优先级组扫描时开始较低优先级组扫描。

当GBRSCN位设置为0时，扫描期间的触发输入将被忽略。设置GBRSCN位，而ADCSR.ADST位为0。

LGRRS位（重启通道选择）

该位设置在组优先操作中要从哪个通道开始重新扫描。当PGS和GBRSCN位为1时，LGRRS位的设置有效。

If the LGRRS bit is 0, scanning of a lower-priority group that was stopped in group priority operation is restarted from the first channel after scanning of the priority group completes.

If the LGRRS bit is 1, scanning of a lower-priority group that was stopped in group priority operation is restarted (upon completion of scanning of the priority group) from the channel for which A/D conversion is not complete. If A/D conversion of the addition setting channel was not completed the specified number of times when scanning stopped, A/D conversion of the addition setting channel is performed again the specified number of times when scanning restarts.

Set the LGRRS bit while the ADCSR.ADST bit is 0.

GBRP bit (Single Scan Continuous Start)

The GBRP bit is set when a single scan operation is to be performed continuously on the group with the lower-priority.

Setting the GBRP bit to 1 starts a single scan of the group with the lower-priority. On completion of the scan, another single scan of the group with the lower-priority is started automatically. If scanning has been stopped during group priority operation, single scan of the group with the lower-priority is automatically restarted on completion of the A/D conversion of the priority group.

Before setting the GBRP bit to 1, disable input of a trigger for the lower-priority group. If the GBRP bit is set to 1, rescanning is performed only on the group with the lower-priority even if the GBRSCN bit is set to 0.

43.2.21 ADCMPCR : A/D Compare Function Control Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x090

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPAB[1:0]	Window A/B Composite Conditions Setting These bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1). 0 0: Output ADC12i_WCMPM (i = 0, 1) when window A OR window B comparison conditions are met. Otherwise, output ADC12i_WCMPUM (i = 0, 1). 0 1: Output ADC12i_WCMPM (i = 0, 1) when window A EXOR window B comparison conditions are met. Otherwise, output ADC12i_WCMPUM (i = 0, 1). 1 0: Output ADC12i_WCMPM (i = 0, 1) when window A AND window B comparison conditions are met. Otherwise, output ADC12i_WCMPUM (i = 0, 1). 1 1: Setting prohibited.	R/W
8:2	—	These bits are read as 0. The write value should be 0.	R/W
9	CMPBE	Compare Window B Operation Enable 0: Disable compare window B operation. Disable ADC12i_WCMPM (i = 0, 1) and ADC12i_WCMPUM (i = 0, 1) outputs. 1: Enable compare window B operation.	R/W
10	—	This bit is read as 0. The write value should be 0.	R/W
11	CMPAE	Compare Window A Operation Enable 0: Disable compare window A operation. Disable ADC12i_WCMPM (i = 0, 1) and ADC12i_WCMPUM (i = 0, 1) outputs. 1: Enable compare window A operation.	R/W
12	—	This bit is read as 0. The write value should be 0.	R/W
13	CMPBIE	Compare B Interrupt Enable 0: Disable ADC12i_CMPBI (i = 0, 1) interrupt when comparison conditions (window B) are met. 1: Enable ADC12i_CMPBI (i = 0, 1) interrupt when comparison conditions (window B) are met.	R/W

如果LGRRS位为0，则在优先级组扫描完成后，从第一个通道开始重新开始对在组优先级操作中停止的低优先级组的扫描。

如果LGRRS位为1，则从AD转换未完成的通道重新开始（在完成优先级组的扫描时）组优先操作中停止的低优先级组的扫描。如果在扫描停止时加法设置通道的AD转换未完成指定次数，则在扫描重新开始时再次执行加法设置通道的AD转换指定次数。

当ADCSR.ADST位为0时设置LGRRS位。

GBRP位（单次扫描连续启动）

当要对优先级较低的组连续执行单次扫描操作时，设置GBRP位。

将GBRP位设置为1开始对具有较低优先级的组进行单次扫描。扫描完成后，将自动开始对具有较低优先级的组进行另一次单次扫描。如果在组优先操作期间扫描已停止，则在优先组的AD转换完成时，将自动重新开始优先级较低的组的单次扫描。

在将GBRP位设置为1之前，禁用低优先级组的触发器输入。如果GBRP位设置为1，即使GBRSCN位设置为0，也仅对具有较低优先级的组执行重新扫描。

43.2.21 ADCMPCR:AD比较功能控制寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x090

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CMPAB[1:0]	窗口AB复合条件设置 这些位在窗口A和窗口B都启用时有效（CMPAE=1和CMPBE = 1). 00：当窗口AOR窗口B比较条件满足时，输出ADC12i_WCMPM(i=0 1)。否则，输出ADC12i_WCMPUM(i=0 1)。 01：当窗口AEXOR窗口B比较条件满足时，输出ADC12i_WCMPM(i=0 1)。否则，输出ADC12i_WCMPUM(i=0 1)。 10：当窗口A和窗口B比较条件满足时，输出ADC12i_WCMPM(i=0 1)。否则，输出ADC12i_WCMPUM(i=0 1)。 11：禁止设置。	R/W
8:2	—	这些位被读取为0。写入值应为0。	R/W
9	CMPBE	比较窗口B操作启用 0：禁止比较窗口B操作。 禁用ADC12i_WCMPM(i=0 1)和ADC12i_WCMPUM(i=0 1)输出。 1：启用比较窗口B操作。	R/W
10	—	该位读取为0。写入值应为0。	R/W
11	CMPAE	比较窗口A操作启用 0：禁止比较窗口A操作。 禁用ADC12i_WCMPM(i=0 1)和ADC12i_WCMPUM(i=0 1)输出。 1：启用比较窗口A操作。	R/W
12	—	该位读取为0。写入值应为0。	R/W
13	CMPBIE	比较B中断使能 0：当满足比较条件（窗口B）时，禁用ADC12i_CMPBI(i=0 1)中断。 1：当满足比较条件（窗口B）时，使能ADC12i_CMPBI(i=0 1)中断。	R/W

Bit	Symbol	Function	R/W
14	WCMPE	Window Function Setting 0: Disable window function Window A and window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Enable window function Window A and window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W
15	CMPAIE	Compare A Interrupt Enable 0: Disable ADC12i_CMPAI (i = 0, 1) interrupt when comparison conditions (window A) are met. 1: Enable ADC12i_CMPAI (i = 0, 1) interrupt when comparison conditions (window A) are met.	R/W

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both window A and window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCOMB. Only set the CMPAB[1:0] bits while the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare window B operation. Set the CMPBE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- CMPCHB[5:0] bits in the Window B Channel Select Register (ADCMPBNSR)

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare window A operation. Set the CMPAE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, B1 (ADANSA0, ADANSA1, ADANSB0, ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- Window A Channel Select Registers 0 and 1 (ADCMPANSR0 and ADCMPANSR1)
- Window A Extended Input Select Register (ADCMPANSER)

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC12i_CMPBI (i = 0, 1) interrupt output when the comparison conditions (window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Set the WCMPE bit while the ADCSR.ADST bit is 0.

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC12i_CMPAI (i = 0, 1) interrupt output when the comparison conditions (window A) are met.

43.2.22 ADCMPANSR0 : A/D Compare Function Window A Channel Select Register 0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x094

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA15	CMPCHA14	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA09	CMPCHA08	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14	WCMPE	窗口功能设置 0：关闭窗口功能 窗口A和窗口B用作比较器，将下侧的单个值与AD转换结果进行比较。 1：启用窗口功能 窗口A和窗口B用作比较器，将上下两个值与AD转换结果进行比较。	R/W
15	CMPAIE	比较中断使能 0：当满足比较条件（窗口A）时，禁止ADC12i_CMPAI(i=0 1)中断。 1：当满足比较条件（窗口A）时，使能ADC12i_CMPAI(i=0 1)中断。	R/W

CMPAB[1:0]位（窗口AB复合条件设置）

当窗口A和窗口B在单次扫描模式下启用（CMPAE=1和CMPBE=1）时，CMPAB[1:0]位有效。这些位指定比较函数匹配不匹配事件的输出条件和ADWINMON.MONCOMB的监视条件。仅在ADCSR.ADST位为0时设置CMPAB[1:0]位。

CMPBE位（比较窗口B操作使能）

CMPBE位启用或禁用比较窗口B操作。当ADCSR.ADST位为0时设置CMPBE位。

在设置以下寄存器之前将此位设置为0：

●AD通道选择寄存器A0、A1、B0、B1（ADANSA0、ADANSA1、ADANSB0、ADANSB1）

●AD转换扩展输入控制寄存器(ADEXICR)中的OCSB、TSSB、OCSA或TSSA位

●窗口B通道选择寄存器(ADCMPBNSR)中的CMPCHB[5:0]位

CMPAE位（比较窗口A操作使能）

CMPAE位启用或禁用比较窗口A操作。当ADCSR.ADST位为0时设置CMPAE位。

在设置以下寄存器之前将此位设置为0：

●AD通道选择寄存器A0、A1、B0、B1（ADANSA0、ADANSA1、ADANSB0、ADANSB1）

●AD转换扩展输入控制寄存器(ADEXICR)中的OCSB、TSSB、OCSA或TSSA位

●窗口A通道选择寄存器0和1（ADCMPANSR0和ADCMPANSR1）

●窗口A扩展输入选择寄存器(ADCMPANSER)

CMPBIE位（比较B中断允许）

当满足比较条件（窗口B）时，CMPBIE位启用或禁用ADC12i_CMPBI(i=0 1)中断输出。

WCMPE位（窗口功能设置）

WCMPE位启用或禁用窗口功能。当ADCSR.ADST位为0时设置WCMPE位。

CMPAIE位（比较中断允许）

当满足比较条件（窗口A）时，CMPAIE位启用或禁用ADC12i_CMPAI(i=0 1)中断输出。

43.2.22 ADCMPANSR0:AD比较功能窗口A通道选择寄存器0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x094

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA15	CMPCHA14	CMPCHA13	CMPCHA12	CMPCHA11	CMPCHA10	CMPCHA09	CMPCHA08	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	Compare Window A Channel Select Bit 15 (CMPCHA15) is associated with ANm15 and bit 0 (CMPCHA00) is associated with ANm00. 0: Disable compare function for associated input channel 1: Enable compare function for associated input channel	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPCHAn bits (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA0.ANSAn bits and the ADANSB0.ANSBn bits.

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

43.2.23 ADCMPANSR1 : A/D Compare Function Window A Channel Select Register 1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x096

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA31	CMPCHA30	CMPCHA29	CMPCHA28	CMPCHA27	CMPCHA26	CMPCHA25	CMPCHA24	CMPCHA23	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	Compare Window A Channel Select Bit 15 (CMPCHA31) is associated with ANm31 and bit 0 (CMPCHA16) is associated with ANm16. 0: Disable compare function for associated input channel 1: Enable compare function for associated input channel	R/W

Note: n = 16 to 28(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPCHAn bits (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA1.ANSAn bits and the ADANSB1.ANSBn bits.

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

43.2.24 ADCMPANSER : A/D Compare Function Window A Extended Input Select Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPTSA	Temperature Sensor Output Compare Select 0: Exclude the temperature sensor output from the compare Window A target range. 1: Include the temperature sensor output in the compare Window A target range.	R/W

Bit	Symbol	Function	R/W
15:0	CMPCHAn	比较窗口A通道选择 位15(CMPCHA15)与ANm15相关联，位0(CMPCHA00)与ANm00. 0：禁用关联输入通道的比较功能1：启用关联输入通道的比较功能	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPCHAn位（比较窗口A通道选择）

通过将1写入CMPCHAn位来启用比较功能，该位与在ADANSA0.ANSAn位和ADANSB0.ANSBn位中选择的AD转换通道的编号相同。

当ADCSR.ADST位为0时，设置CMPCHAn位。

43.2.23 ADCMPANSR1:AD比较功能窗口A通道选择寄存器1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x096

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPCHA31	CMPCHA30	CMPCHA29	CMPCHA28	CMPCHA27	CMPCHA26	CMPCHA25	CMPCHA24	CMPCHA23	CMPCHA22	CMPCHA21	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPCHAn	比较窗口A通道选择 位15(CMPCHA31)与ANm31相关联，位0(CMPCHA16)与ANm16. 0：禁用关联输入通道的比较功能1：启用关联输入通道的比较功能	R/W

Note: n = 16 to 28(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPCHAn位（比较窗口A通道选择）

通过将1写入CMPCHAn位来启用比较功能，该位与在ADANSA1.ANSAN位和ADANSB1.ANSBn位中选择的AD转换通道的编号相同。

当ADCSR.ADST位为0时，设置CMPCHAn位。

43.2.24 ADCMPANSER:AD比较功能窗口A扩展输入选择 Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)
Offset address: 0x092

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPOCA	CMPTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPTSA	温度传感器输出比较选择 0：将温度传感器输出排除在比较窗口A目标范围之外。1：将温度传感器输出包括在比较窗口A目标范围内。	R/W

Bit	Symbol	Function	R/W
1	CMPOCA	Internal Reference Voltage Compare Select 0: Exclude the internal reference voltage from the compare Window A target range. 1: Include the internal reference voltage in the compare Window A target range.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare Window A function is enabled by setting the CMPTSA bit to 1 while the ADEXICR.TSSA bit or the ADEXICR.TSSB bit is 1. Set the CMPTSA bit while the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare window A function is enabled by setting the CMPOCA bit to 1 when the ADEXICR.OCSA and ADEXICR.OCSB bit is 1. Set the CMPOCA bit when the ADCSR.ADST bit is 0.

43.2.25 ADCMPLR0 : A/D Compare Function Window A Comparison Condition Setting Register 0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x098

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA15	CMPLCHA14	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA09	CMPLCHA08	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	Compare Window A Comparison Condition Select These bits set comparison conditions for channels to which Window A comparison conditions are applied. Bit 15 (CMPLCHA15) is associated with ANm15 and bit 0 (CMPLCHA00) is associated with ANm00. Comparison conditions are shown in Figure 43.4. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPLCHAn bits (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which Window A comparison conditions are applied. These bits can be set for each analog input to be compared. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn flag sets to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

Bit	Symbol	Function	R/W
1	CMPOCA	内部参考电压比较选择 0：将内部参考电压排除在比较窗口A目标范围之外。1：在比较窗口A目标范围内包含内部参考电压。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

CMPTSA位（温度传感器输出比较选择）

比较窗口A功能通过将CMPTSA位设置为1而ADEXICR.TSSA位或ADXICR.TSSB位为1。在ADCSR.ADST位为0时设置CMPTSA位。

CMPOCA位（内部参考电压比较选择）

当ADEXICR.OCSA和ADXICR.OCSB位为1。当ADCSR.ADST位为0时，设置CMPOCA位。

43.2.25 ADCMPLR0:AD比较功能窗口A比较条件设置 Register 0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x098

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA15	CMPLCHA14	CMPLCHA13	CMPLCHA12	CMPLCHA11	CMPLCHA10	CMPLCHA09	CMPLCHA08	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	比较窗口A比较条件选择 这些位设置应用窗口A比较条件的通道的比较条件。位15(CMPLCHA15)与ANm15相关联，位0(CMPLCHA00)与 ANm00. 比较条件如图43.4所示。 0：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADCMPDR0值>D转换值当启用窗口功能时（ADCMPCR.WCMPE=1）： D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值 1：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPLCHAn位（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的通道的比较条件。可以为要比较的每个模拟输入设置这些位。当每个模拟输入的比较结果满足设置条件时，ADCMPSR0.CMPSTCHAn标志设置为1，并产生比较中断(ADC12i_CMPAI(i=0 1))。

Comparison conditions when the window function is disabled

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDR0 value ≤ A/D converted value	Not met	ADCMPDR0 value < A/D converted value	Met
ADCMPDR0 value > A/D converted value	Met	ADCMPDR0 value ≥ A/D converted value	Not met

Comparison conditions when the window function is enabled

CMPLCHAn = 0	
ADCMPDR1 value < A/D converted value	Met
ADCMPDR0 value ≤ A/D converted value ≤ ADCMPDR1 value	Not met
A/D converted value < ADCMPDR0 value	Met

CMPLCHAn = 1	
ADCMPDR1 value ≤ A/D converted value	Not met
ADCMPDR0 value < A/D converted value < ADCMPDR1 value	Met
A/D converted value ≤ ADCMPDR0 value	Not met

Figure 43.4 Explanation of comparison conditions for compare function Window A

43.2.26 ADCMPLR1 : A/D Compare Function Window A Comparison Condition Setting Register 1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x09A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA31	CMPLCHA30	CMPLCHA29	CMPLCHA28	CMPLCHA27	CMPLCHA26	CMPLCHA25	CMPLCHA24	CMPLCHA23	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

禁用窗口功能时的比较条件

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDDR0值≤AD转换值	没见过	ACMPDDR0值<AD转换值	Met
ACMPDDR0值>AD转换值	Met	ACMPDDR0值≥AD转换值	没见过

启用窗口功能时的比较条件

CMPLCHAn = 0	
ADCMPDDR1值<AD转换值	Met
ADCMPDR0值≤AD转换值≤ADCMPDR1值	没见过
AD转换值<ADCMPDR0值	Met

CMPLCHAn = 1	
ADCMPDDR1值≤AD转换值	没见过
ADCMPDR0值<AD转换值<ADCMPDR1值	Met
AD转换值≤ADCMPDR0值	没见过

Figure 43.4 比较功能窗口A的比较条件说明

43.2.26 ADCMPLR1:AD比较功能窗口A比较条件设置 Register 1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x09A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPLCHA31	CMPLCHA30	CMPLCHA29	CMPLCHA28	CMPLCHA27	CMPLCHA26	CMPLCHA25	CMPLCHA24	CMPLCHA23	CMPLCHA22	CMPLCHA21	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	Compare Window A Comparison Condition Select These bits set comparison conditions for channels to which Window A comparison conditions are applied. Bit 15 (CMPLCHA31) is associated with ANm31 and bit 0 (CMPLCHA16) is associated with ANm16. Comparison conditions are shown in Figure 43.4. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 16 to 28(unit 1)
Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPLCHAn bits (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for analog channels to which window A comparison conditions are applied. These bits can be set for each analog input to be compared. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn bit is set to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

43.2.27 ADCMPLER : A/D Compare Function Window A Extended Input Comparison Condition Setting Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x093

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select Comparison conditions are shown in Figure 43.4. 0: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value > A/D-converted valueCompare Window A Temperature Sensor Output Comparison Condition Select When window function is enabled (ADCMPCR.WCMPE = 1) : Compare Window A Temperature Sensor Output Comparison ConditionA/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1) : ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W
1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select Comparison conditions are shown in Figure 43.4. 0: When window function is disabled (ADCMPCR.WCMPE = 0) : ADCMPDR0 value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADCMPDR0 value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Bit	Symbol	Function	R/W
15:0	CMPLCHAn	比较窗口A比较条件选择 这些位设置应用窗口A比较条件的通道的比较条件。 位15(CMPLCHA31)与ANm31相关联，位0(CMPLCHA16)与ANm16. 比较条件如图43.4所示。 0：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADCMPDR0值>D转换值当启用窗口功能时（ADCMPCR.WCMPE=1）： D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值 1：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Note: n = 16 to 28(unit 1)
Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPLCHAn位（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的模拟通道的比较条件。可以为要比较的每个模拟输入设置这些位。当每个模拟输入的比较结果满足设置条件时，ADCMPSR1.CMPSTCHAn位设置为1，并产生比较中断(ADC12i_CMPAI(i=0 1))。

43.2.27 ADCMPLER:AD比较功能窗口A扩展输入比较条件设置寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x093

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPLOCA	CMPLTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPLTSA	比较窗口A温度传感器输出比较条件选择 比较条件如图43.4所示。 0：当窗口功能被禁用时（ADCMPCR.WCMPE=0）： ADCMPDDR0值>AD转换值比较窗口A温度传感器输出比较条件选择 启用窗口功能时(ADCMPCR.WCMPE=1)： 比较窗口A温度传感器输出比较条件AD转换值<ADCMPDR0值，或AD转换值>ADCMPDR1值 1：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W
1	CMPLOCA	比较窗口A内部参考电压比较条件选择 比较条件如图43.4所示。 0：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值>D转换值当窗口功能启用时（ADCMPCR.WCMPE=1）： D转换值<ADCMPDR0值，或D转换值>ADCMPDR1值 1：当窗口功能禁用时（ADCMPCR.WCMPE=0）：ADCMPDR0值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： ADCMPDR0 value < A/D-converted value < ADCMPDR1 value	R/W

Bit	Symbol	Function	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies comparison conditions when the temperature sensor output is the target for the Window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA flag sets to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies comparison conditions when the internal reference voltage is the target for the Window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA flag sets to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

43.2.28 ADCMPDRn : A/D Compare Function Window A Lower-Side/Upper-Side Level Setting Register (n = 0, 1)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x09C + (0x2 × n)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADCMPDRy (y = 0, 1) register specifies the reference data when the compare window A function is used. ADCMPDR0 sets the lower reference for window A, and ADCMPDR1 sets the upper reference for window A.

ADCMPDRy are read/write registers.

ADCMPDRy are writable even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion*1.

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0). ADCMPDR1 are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 43.5. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

Bit	Symbol	Function	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

CMPLTSA位（比较窗口A温度传感器输出比较条件选择）

当温度传感器输出是窗口A比较条件的目标时，CMPLTSA位指定比较条件。当温度传感器输出比较结果满足设置条件时，ADCMPSER.CMPSTTSA标志设置为1并产生比较中断(ADC12i_CMPAI(i=0 1))。

CMPLOCA位（比较窗口A内部参考电压比较条件选择）

当内部参考电压是窗口A比较条件的目标时，CMPLOCA位指定比较条件。当内部参考电压比较结果满足设置条件时，ADCMPSER.CMPSTOCA标志设置为1并产生比较中断(ADC12i_CMPAI(i=0 1))。

43.2.28 ADCMPDRn:AD比较功能窗口ALower-SideUpper-SideLevel设置寄存器(n=0 1)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x09C + (0x2 × n)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADCMPDRy(y=0 1)寄存器指定使用比较窗口A功能时的参考数据。ADCMPDDR0设置窗口A的下参考值，而ADCMPDR1设置窗口A的上参考值。

ADCMPDRy是读写寄存器。

ADCMPDRy即使在AD转换期间也是可写的。在AD转换*1期间，可以通过重写寄存器值来动态更改参考数据。

设置这些寄存器，使参考上限不小于参考下限(ADCMPDR1≥ADCMPDR0)。
禁用窗口功能时不使用ACMPDDR1。

注1.写入每个寄存器时，低位和高位参考值会发生变化。例如，当上参考值改变和下参考值改变时，MCU将上参考（重写后）和下参考（重写前）与AD转换结果进行比较。请参见图43.5。如果在重写这两个参考时比较错误，则在ADCSR.ADST和目标比较窗口操作使能位（ADCMPCR.CMPAE或ADCMPCR.CMPBE）都为0时重写这些参考值。

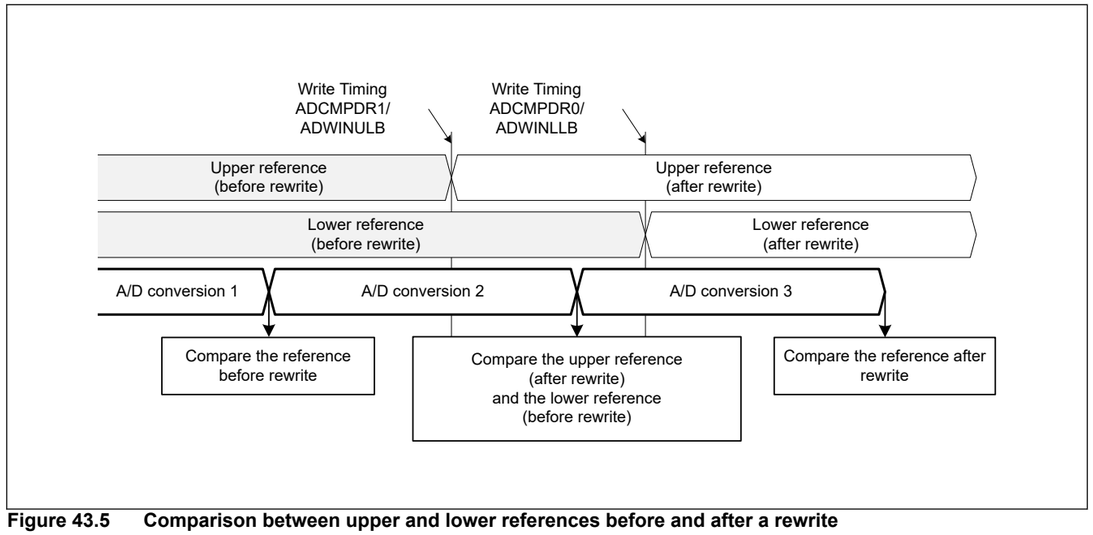

Figure 43.5 Comparison between upper and lower references before and after a rewrite

The ADCMPDRy registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of the A/D Conversion Accuracy Select bit (12-bit, 10-bit, 8-bit)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are shown as follows:

1. When A/D-converted value addition mode is not selected
   - Flush-right data with 12-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 8 bits ([7:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 10-bit accuracy — Upper 10 bits ([15:6]) are valid
   - Flush-left data with 8-bit accuracy — Upper 8 bits ([15:8]) are valid
2. When A/D-converted value addition mode is selected
   - Flush-right data with 12-bit accuracy — Lower 14 bits ([13:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 14 bits ([15:2]) are valid
   - Flush-left data with 10-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 8-bit accuracy — Upper 10 bits ([15:6]) are valid

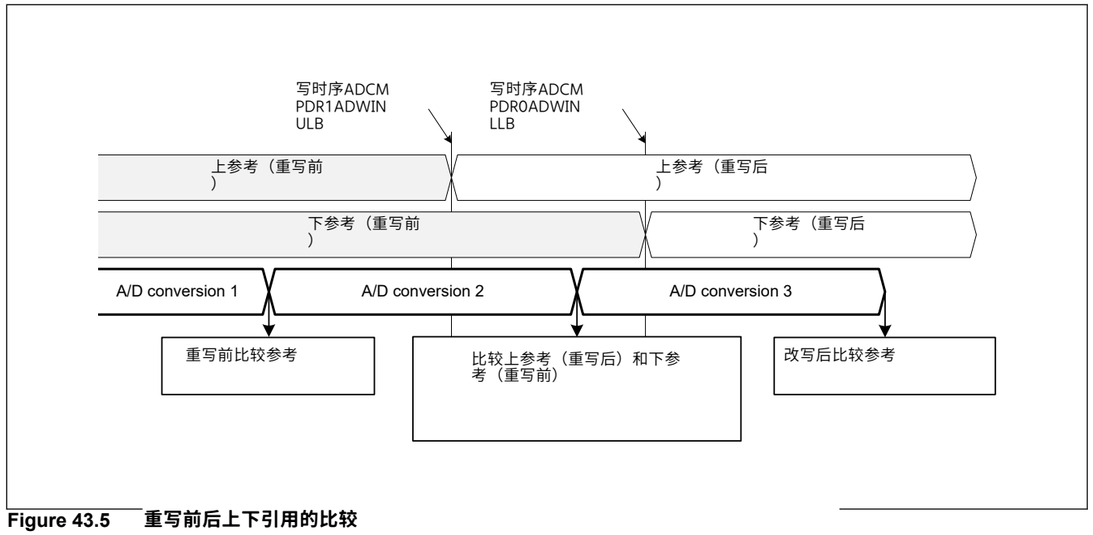

Figure 43.5 重写前后上下引用的比较

ADCMPDRy寄存器根据以下条件使用不同的格式：

●AD数据寄存器格式选择位的值（flush-rightorflush-left）

●AD转换精度选择位（12位、10位、8位）的值

●AD-ConvertedValueAdditionAverageChannelSelect位的值（选择或不选择AD-convertedvalue添加模式）。

每个条件的数据格式如下所示：

1.未选择AD转换值加法模式时

●12位精度的右冲洗数据—低12位([11:0])有效

●10位精度的右刷新数据—低10位([9:0])有效

●8位精度的右冲洗数据—低8位([7:0])有效

●12位精度的左刷新数据—高12位([15:4])有效

●10位精度的左刷新数据—高10位([15:6])有效

●8位精度的左刷新数据—高8位([15:8])有效

2.选择AD转换值加法模式时

●12位精度的右刷新数据—低14位([13:0])有效

●10位精度的右刷新数据—低12位([11:0])有效

●8位精度的右冲洗数据—低10位([9:0])有效

●12位精度的左刷新数据—高14位([15:2])有效

●10位精度的左刷新数据—高12位([15:4])有效

●8位精度的左刷新数据—高10位([15:6])有效

43.2.29 ADWINnLB : A/D Compare Function Window B Lower-Side/Upper-Side Level Setting Register (n = L, U)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A8 (n = L)
0x0AA (n = U)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The ADWINULB and ADWINLLB registers specify the reference data when the compare window B function is used. ADWINLLB sets the lower reference for window B, and ADWINULB sets the upper reference for window B.

ADWINnLB are read/write registers.

ADWINnLB are writable even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion*1.

Set these registers so that the upper reference is not less than the lower reference (ADWINULB ≥ ADWINLLB). ADWINULB are not used when the window function is disabled.

Note 1. The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after rewrite), and the lower reference (before rewrite) with the A/D conversion result. See Figure 43.6. If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST and the target Compare Window Operation Enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) are 0.

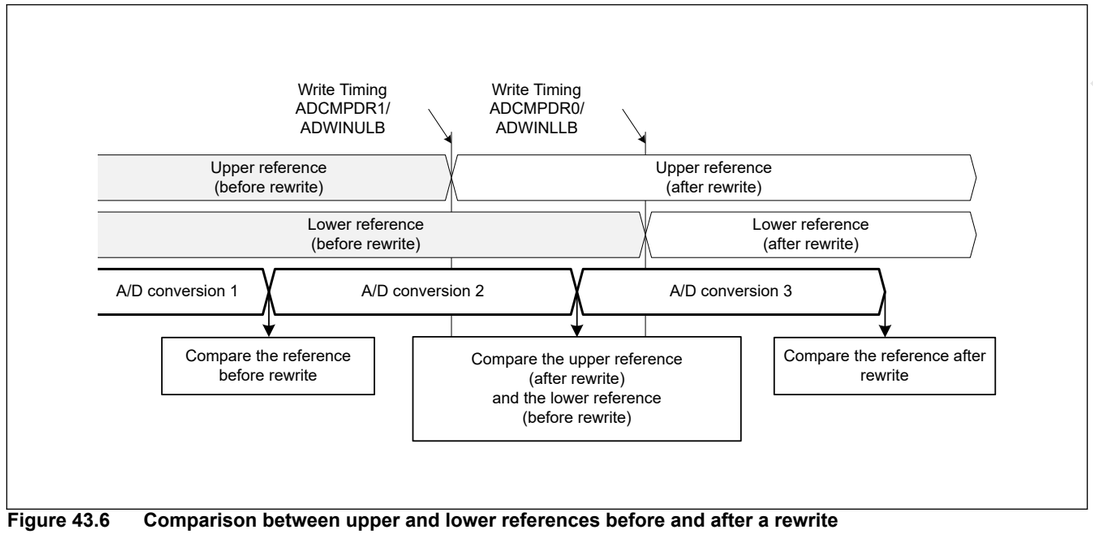

Figure 43.6 Comparison between upper and lower references before and after a rewrite

The ADWINnLB registers use different formats depending on the following conditions:

- The value of A/D Data Register Format Select bit (flush-right or flush-left)
- The value of the A/D Conversion Accuracy Select bit (12-bit, 10-bit, 8-bit)
- The value of A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are shown as follows:

1. When A/D-converted value addition mode is not selected

43.2.29 ADWINnLB:AD比较函数窗口BLower-SideUpper-SideLevel 设置寄存器(n=L U)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A8 (n = L)
0x0AA (n = U)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ADWINULB和ADWINLLB寄存器指定使用比较窗口B功能时的参考数据。
ADWINLLB设置窗口B的下参考，ADWINULB设置窗口B的上参考。

ADWINnLB是读写寄存器。

ADWINnLB即使在AD转换期间也是可写的。在AD转换*1期间，可以通过重写寄存器值来动态更改参考数据。

设置这些寄存器，使上限参考值不小于下限参考值(ADWINULB≥ADWINLLB)。
禁用窗口功能时不使用ADWINULB。

注1.写入每个寄存器时，低位和高位参考值会发生变化。例如，当上参考值改变和下参考值改变时，MCU将上参考（重写后）和下参考（重写前）与AD转换结果进行比较。请参见图43.6。如果在重写这两个参考时比较错误，则在ADCSR.ADST和目标比较窗口操作使能位（ADCMPCR.CMPAE或ADCMPCR.CMPBE）都为0时重写这些参考值。

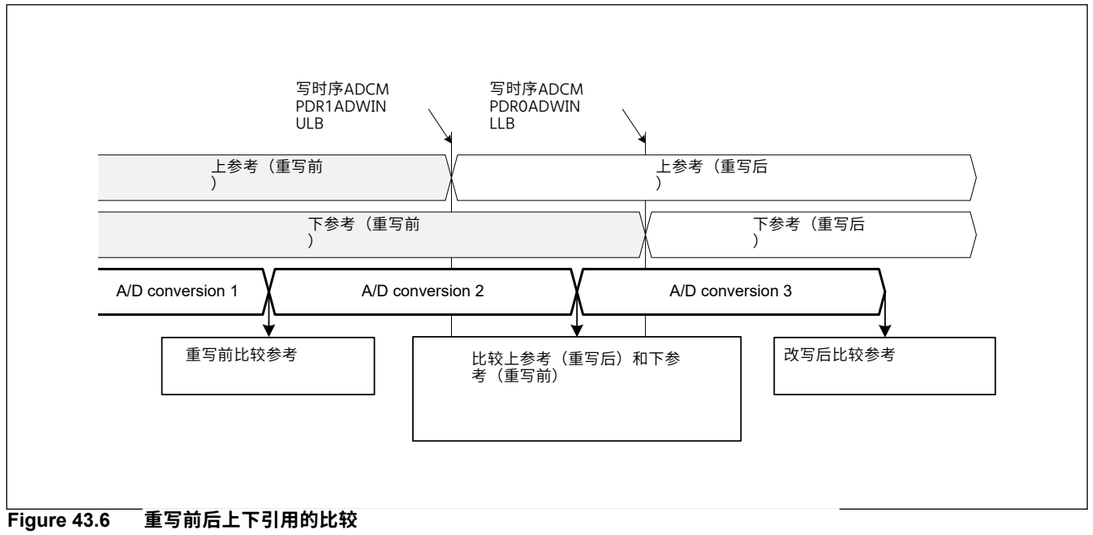

Figure 43.6 重写前后上下引用的比较

ADWINnLB寄存器根据以下条件使用不同的格式：

●AD数据寄存器格式选择位的值（flush-rightorflush-left）

●AD转换精度选择位（12位、10位、8位）的值

●AD-ConvertedValueAdditionAverageChannelSelect位的值（选择或不选择AD-convertedvalue添加模式）。

每个条件的数据格式如下所示：

1.未选择AD转换值加法模式时

- Flush-right data with 12-bit accuracy — Lower 12 bits ([11:0]) are valid
- Flush-right data with 10-bit accuracy — Lower 10 bits ([9:0]) are valid
- Flush-right data with 8-bit accuracy — Lower 8 bits ([7:0]) are valid
- Flush-left data with 12-bit accuracy — Upper 12 bits ([15:4]) are valid
- Flush-left data with 10-bit accuracy — Upper 10 bits ([15:6]) are valid
- Flush-left data with 8-bit accuracy — Upper 8 bits ([15:8]) are valid

2. When A/D-converted value addition mode is selected
   - Flush-right data with 12-bit accuracy — Lower 14 bits ([13:0]) are valid
   - Flush-right data with 10-bit accuracy — Lower 12 bits ([11:0]) are valid
   - Flush-right data with 8-bit accuracy — Lower 10 bits ([9:0]) are valid
   - Flush-left data with 12-bit accuracy — Upper 14 bits ([15:2]) are valid
   - Flush-left data with 10-bit accuracy — Upper 12 bits ([15:4]) are valid
   - Flush-left data with 8-bit accuracy — Upper 10 bits ([15:6]) are valid

43.2.30 ADCMPSR0 : A/D Compare Function Window A Channel Status Register 0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA15	CMPSTCHA14	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA09	CMPSTCHA08	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	Compare Window A Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of channels to which Window A comparison conditions are applied. Bit 15 (CMPSTCHA15) is associated with ANm15 and bit 0 (CMPSTCHA00) is associated with ANm00. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPSTCHAn flags (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied. When a comparison condition set in ADCMPLR0.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

●12位精度的右冲洗数据—低12位([11:0])有效
●10位精度的右刷新数据—低10位([9:0])有效
●8位精度的右冲洗数据—低8位([7:0])有效
●12位精度的左刷新数据—高12位([15:4])有效
●10位精度的左刷新数据—高10位([15:6])有效
●8位精度的左刷新数据—高8位([15:8])有效

2.选择AD转换值加法模式时
●12位精度的右刷新数据—低14位([13:0])有效
●10位精度的右刷新数据—低12位([11:0])有效
●8位精度的右冲洗数据—低10位([9:0])有效
●12位精度的左刷新数据—高14位([15:2])有效
●10位精度的左刷新数据—高12位([15:4])有效
●8位精度的左刷新数据—高10位([15:6])有效

43.2.30 ADCMPSR0:AD比较功能窗口A通道状态寄存器0

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA15	CMPSTCHA14	CMPSTCHA13	CMPSTCHA12	CMPSTCHA11	CMPSTCHA10	CMPSTCHA09	CMPSTCHA08	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	比较窗口A标志 当窗口A操作使能时（ADCMPCR.CMPAE=1b），这些位指示应用窗口A比较条件的通道的比较结果。位15(CMPSTTCHA15)与ANm15相关联，位0(CMPSTTCHA00)与ANm00相关联。 0：不满足比较条件。1：满足比较条件 。	R/W

Note: n = 00 to 10, 12, 13(unit 0), 00 to 02(unit 1)

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPSTCHAn标志（比较窗口A标志）

CMPSTCHAn标志指示应用窗口A比较条件的通道的比较结果。当ADCMPLR0.CMPLCHAn中设置的比较条件在AD转换结束时满足，相关的CMPSTCHAn标志设置为1。当ADCMPCR.CMPAIE位为1时，比较中断请求(ADC12i_CMPAI(i=0 1))为当此标志设置为1时生成。

将1写入CMPSTCHAn标志是无效的。

[Setting condition]

●ADCMPLR0.CMPLCHAn中设置的条件在ADCMPCR.CMPAE=1时满足。

[Clearing condition]

●读1后写0。

43.2.31 ADCMPSR1 : A/D Compare Function Window A Channel Status Register1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A2

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA31	CMPSTCHA30	CMPSTCHA29	CMPSTCHA28	CMPSTCHA27	CMPSTCHA26	CMPSTCHA25	CMPSTCHA24	CMPSTCHA23	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	Compare Window A Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of channels to which Window A comparison conditions are applied. Bit 15 (CMPSTCHA31) is associated with ANm31 and bit 0 (CMPSTCHA16) is associated with ANm16. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

Note: n = 16 to 28(unit 1)

Note: Bits associated with non-existent pins are reserved. This bit is read as 0. The write value should be 0.

CMPSTCHAn flags (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied. When the comparison condition set in ADCMPLR1.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

43.2.32 ADCMPSER : A/D Compare Function Window A Extended Input Channel Status Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W

43.2.31 ADCMPSR1:AD比较功能窗口A通道状态寄存器1

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A2

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMPSTCHA31	CMPSTCHA30	CMPSTCHA29	CMPSTCHA28	CMPSTCHA27	CMPSTCHA26	CMPSTCHA25	CMPSTCHA24	CMPSTCHA23	CMPSTCHA22	CMPSTCHA21	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CMPSTCHAn	比较窗口A标志 当窗口A操作使能（ADCMPCR.CMPAE=1）时，这些位指示应用窗口A比较条件的通道的比较结果。位15(CMPSTCHA31)与ANm31相关联，位0(CMPSTTCHA16)与ANm16相关联。 0：不满足比较条件。1：满足比较条件 。	R/W

Note: n = 16 to 28(unit 1)

Note: 与不存在的引脚相关的位被保留。该位读取为0。写入值应为0。

CMPSTCHAn标志（比较窗口A标志）

CMPSTCHAn标志指示应用窗口A比较条件的通道的比较结果。当ADCMPLR1.CMPLCHAn中设置的比较条件在AD转换结束时满足，相关的CMPSTCHAn标志设置为1。当ADCMPCR.CMPAIE位为1时，比较中断请求(ADC12i_CMPAI(i=0 1))当此标志设置为1时生成。

将1写入CMPSTCHAn标志是无效的。

[Setting condition]

●ADCMPLR1.CMPLCHAn中设置的条件在ADCMPCR.CMPAE=1时满足。

[Clearing condition]

●读1后写0。

43.2.32 ADCMPSER:AD比较功能窗口A扩展输入通道状态 Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTTSA	比较窗口A温度传感器输出比较标志 当窗口A操作使能（ADCMPCR.CMPAE=1）时，该位指示温度传感器输出比较结果。 0：不满足比较条件。1：满足比较条件 。	R/W
1	CMPSTOCA	比较窗口A内部参考电压比较标志 当窗口A操作使能时（ADCMPCR.CMPAE=1），该位指示内部参考电压比较结果。 0：不满足比较条件。1：满足比较条件 。	R/W

Bit	Symbol	Function	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The ADCMPSER register stores compare results of compare function window A.

CMPSTTSA flag (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA flag indicates the temperature sensor output comparison result. When the comparison condition set in ADCMPLER.CMPLTSA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTTSA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA flag (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA flag indicates the internal reference voltage comparison result. When the comparison condition set in ADCMPLER.CMPLOCA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTOCA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

43.2.33 ADCMPBNSR : A/D Compare Function Window B Channel Select Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A6

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

ADCMPSER寄存器存储比较功能窗口A的比较结果。

CMPSTTSA标志（比较窗口A温度传感器输出比较标志）

CMPSTTSA标志指示温度传感器输出比较结果。当比较条件设置在ADCMPLER.CMPLTSA在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求(ADC12i_CMPAI(i=0 1))。

将1写入CMPSTTSA标志无效。

[Setting condition]

●当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLTSA中设置的条件。

[Clearing condition]

●读1后写0。

CMPSTOCA标志（比较窗口A内部参考电压比较标志）

CMPSTOCA标志指示内部参考电压比较结果。当比较条件设置在ADCMPLER.CMPLOCA在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求(ADC12i_CMPAI(i=0 1))。

将1写入CMPSTOCA标志无效。

[Setting condition]

●当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLOCA中设置的条件。

[Clearing condition]

●读1后写0。

43.2.33 ADCMPBNSR:AD比较功能窗口B通道选择寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0A6

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CMPLB	—	CMPCHB[5:0]					
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	CMPCHB[5:0]	Compare Window B Channel Select These bits select channels to be compared with the compare Window B conditions. **CMPCHB[5:0] / Unit 0 / Unit 1** 0x00 / AN000 / AN100 0x01 / AN001 / AN101 0x02 / AN002 / AN102 0x03 / AN003 / Do not select ⋮ / ⋮ / ⋮ 0x0A / AN010 / Do not select 0x0C / AN012 / Do not select 0x0D / AN013 / Do not select 0x10 / Do not select / AN116 0x11 / Do not select / AN117 ⋮ / ⋮ / ⋮ 0x16 / Do not select / AN128 0x20 / Temparature sensor 0x21 / Internal reference voltage 0x3F / Do not select Others / Setting prohibited	R/W
6	—	This bit is read as 0. The write value should be 0.	R/W
7	CMPLB	Compare Window B Comparison Condition Setting This bit sets comparison conditions for channels for Window B. The comparison conditions are shown in Figure 43.7. 0: When window function is disabled (ADCMPCR.WCMPE = 0): ADWINLLB value > A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): A/D-converted value < ADWINLLB value, or ADWINULB value < A/D-converted value 1: When window function is disabled (ADCMPCR.WCMPE = 0): ADWINLLB value < A/D-converted value When window function is enabled (ADCMPCR.WCMPE = 1): ADWINLLB value < A/D-converted value < ADWINULB value	R/W

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits specify the channels to be compared with the compare Window B conditions from AN000 to AN010, AN012, AN013, AN100 to AN102, AN116 to AN128, the temperature sensor, the internal reference voltage. The compare Window B function is enabled by specifying the hexadecimal number of the A/D conversion channel selected in the ADANSA0, ADANSA1, ADANSB0, ADANSB1 registers.

Set the CMPCHB[5:0] bits while the ADCSR.ADST bit is 0.

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit specifies the comparison conditions for channels for Window B. When the comparison result of an analog input meets the set condition, the associated ADCMPBSR.CMPSTB flag sets to 1 and a compare interrupt request (ADC12i_CMPBI (i = 0, 1)) is generated.

Bit	Symbol	Function	R/W
5:0	CMPCHB[5:0]	比较窗口B通道选择 这些位选择要与比较窗口B条件进行比较的通道。 **CMPCHB[5:0] / Unit 0 / Unit 1** 0x00 / AN000 / AN100 0x01 / AN001 / AN101 0x02 / AN002 / AN102 0x03 / AN003 / 不要选择 ⋮ / ⋮ / ⋮ 0x0A / AN010 / 不要选择 0x0C / AN012 / 不要选择 0x0D / AN013 / 不要选择 0x10 / 不要选择 / AN116 0x11 / 不要选择 / AN117 ⋮ / ⋮ / ⋮ 0x16 / 不要选择 / AN128 0x20 / Temparature sensor 0x21 / 内部参考电压 0x3F / 不要选择 Others / 禁止设定	R/W
6	—	该位读取为0。写入值应为0。	R/W
7	CMPLB	比较窗口B比较条件设置 该位设置窗口B的通道比较条件。比较条件如图43.7所示。 0：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADWINLLB值>D转换值 启用窗口功能时(ADCMPCR.WCMPE=1)： D转换值<ADWINLLB值，或ADWINULB值<AD转换值 1：禁用窗口功能时（ADCMPCR.WCMPE=0）：ADWINLLB值<AD转换值 启用窗口功能时(ADCMPCR.WCMPE=1)：ADWINLLB值<AD转换值<ADWINULB值	R/W

CMPCHB[5:0]位（比较窗口B通道选择）

CMPCHB[5:0]位指定要与比较窗口B条件（从AN000到AN010、AN012、AN013、AN100到AN102、AN116到AN128、温度传感器、内部参考电压。通过指定在ADANSA0、ADANSA1、ADANSB0、ADANSB1寄存器中选择的AD转换通道的十六进制数来启用比较窗口B功能。

当ADCSR.ADST位为0时，设置CMPCHB[5:0]位。

CMPLB位（比较窗口B比较条件设置）

CMPLB位指定窗口B的通道比较条件。当模拟输入的比较结果满足设置条件时，相关的ADCMPBSR.CMPSTB标志设置为1，并发出比较中断请求(ADC12i_CMPBI(i=0 1))生成。

Compare conditions when the window function is disabled

CMPLB = 0

ADWINLLB value ≤ A/D converted value	Not met
ADWINLLB value > A/D converted value	Met

CMPLB = 1

ADWINLLB value < A/D converted value	Met
ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value <A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 43.7 Explanation of compare conditions for compare function Window B

43.2.34 ADCMPBSR : A/D Compare Function Window B Status Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0AC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTB	Compare Window B Flag When Window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of channels to which Window B comparison conditions are applied, temperature sensor output, internal reference voltage. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

CMPSTB flag (Compare Window B Flag)

The CMPSTB flag indicates the comparison result of channels to which Window B comparison conditions are applied, the temperature sensor output, internal reference voltage. When the comparison condition set in ADCMPBNSR.CMPLB is met

比较禁用窗口功能时的条件

CMPLB = 0

ADWINLLB值≤AD转换值	没见过
ADWINLLB值>AD转换值	Met

CMPLB = 1

ADWINLLB值<AD转换值	Met
ADWINLLB值≥AD转换值	没见过

启用窗口功能时比较条件

CMPLB = 0

AD转换值>ADWINULB值	Met
ADWINLLB值≤AD转换值≤ADWINULB值	没见过
AD转换值<ADWINLLB值	Met

CMPLB = 1

AD换算值≥ADWINULB值	没见过
ADWINLLB值<AD转换值<ADWINULB值	Met
AD换算值≤ADWINLLB值	没见过

Figure 43.7 比较功能窗口B的比较条件说明

43.2.34 ADCMPBSR:AD比较功能窗口B状态寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0AC

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	CMPSTB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CMPSTB	比较窗口B标志 当窗口B操作使能时（ADCMPCR.CMPBE=1），该位指示应用窗口B比较条件的通道的比较结果、温度传感器输出、内部参考电压。 0：不满足比较条件。1：满足比较条件 。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

CMPSTB标志（比较窗口B标志）

CMPSTB标志指示应用窗口B比较条件的通道的比较结果、温度传感器输出、内部参考电压。当ADCMPBNSR.CMPLB中设置的比较条件满足时

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at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt request (ADC12i_CMPBI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTB flag is invalid.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

43.2.35 ADWINMON : A/D Compare Function Window A/B Status Monitor Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x08C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MONCOMB	Combination Result Monitor This bit indicates the combination result. This bit is valid when both Window A and Window B operations are enabled. 0: Window A/B composite conditions are not met. 1: Window A/B composite conditions are met.	R
3:1	—	These bits are read as 0.	R
4	MONCMPA	Comparison Result Monitor A 0: Window A comparison conditions are not met. 1: Window A comparison conditions are met.	R
5	MONCMPB	Comparison Result Monitor B 0: Window B comparison conditions are not met. 1: Window B comparison conditions are met.	R
7:6	—	These bits are read as 0.	R

MONCOMB bit (Combination Result Monitor)

The read-only MONCOMB bit indicates the combined result of comparison condition results A and B based on the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits.
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only MONCMPA bit is read as 1 when the A/D-converted value of the Window A target channel meets the condition set in ADCMPLR0/ADCMPLR1 and ADCMPLER. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.

[Clearing conditions]

在AD转换结束时，该标志设置为1。当ADCMPCR.CMPBIE位为1时，当该标志设置为1时产生比较中断请求(ADC12i_CMPBI(i=0 1))。

将1写入CMPSTB标志无效。

[Setting condition]

●当ADCMPCR.CMPBE=1时，满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing condition]

●读1后写0。

43.2.35 ADWINMON:AD比较功能窗口AB状态监视器寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x08C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	MONCOMB	组合结果监视器 该位指示组合结果。该位在WindowA和Window都有效B操作已启用。 0：不满足窗口AB合成条件。1：满足窗口AB复合条件。	R
3:1	—	这些位读为0。	R
4	MONCMPA	比较结果监视器A 0：不满足窗口A比较条件。1：满足窗口A比较条件。	R
5	MONCMPB	比较结果监视器B 0：不满足窗口B比较条件。1：满足窗口B比较条件。	R
7:6	—	这些位读为0。	R

MONCOMB位（组合结果监视器）

只读MONCOMB位指示比较条件结果A和B基于ADCMPCR.CMPAB[1:0]位中设置的组合条件的组合结果。

[Setting condition]

●当ADCMPCR.CMPAE=1且ADCMPCR.CMPBE=1时，合并结果满足ADCMPCR.CMPAB[1:0]位中设置的合并条件。

[Clearing conditions]

●合并结果不满足ADCMPCR.CMPAB[1:0]位设置的合并条件。

- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA位（比较结果监视器A）

当窗口A目标通道的AD转换值满足ADCMPLR0ADCMPLR1和ADCMPLER中设置的条件时，只读MONCMPA位被读取为1。否则，读为0。

[Setting condition]

●当ADCMPCR.CMPAE=1时，AD转换后的值满足ADCMPLR0ADCMPLR1和ADCMPLER寄存器中设置的条件。

[Clearing conditions]

- The A/D-converted value does not meet the condition set in the ADCMPLR0/ADCMPLR1 and ADCMPLER registers when ADCMPCR.CMPAE = 1.
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only MONCMPB bit is read as 1 when the A/D-converted value of the Window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

43.2.36 ADBUFEN : A/D Data Buffer Enable Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0D0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BUFEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BUFEN	Data Buffer Enable 0: The data buffer is not used. 1: The data buffer is used.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The ADBUFEN register sets whether to enable the data buffer.

BUFEN bit (Data Buffer Enable)

This bit enables the use of the data buffer.

When BUFEN = 1b, A/D conversion result (addition result) other than self-diagnosis result is stored in ADBUFn.

Disable the data storage operation (BUFEN = 0b) before reading ADBUFPTR.

Do not use the data buffer for data duplexing, or group scan.

43.2.37 ADBUFPTR : A/D Data Buffer Pointer Register

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0D2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PTROVF	BUFPTR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	BUFPTR[3:0]	Data Buffer Pointer These bits indicate the number of data buffer to which the next A/D converted data is transferred.	R/W

●ADCMPCR.CMPAE=1时，AD转换后的值不满足ADCMPLR0ADCMPLR1和ADCMPLER寄存器中设置的条件。

●ADCMPCR.CMPAE=0（ADCMPCR.CMPAE值从1变为0时自动清零）。

MONCMPB位（比较结果监视器B）

当窗口B目标通道的AD转换值满足ADCMPBNSR.CMPLB位中设置的条件时，只读MONCMPB位被读取为1。否则，读为0。

[Setting condition]

●当ADCMPCR.CMPBE=1时，AD转换后的值满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing conditions]

●ADCMPCR.CMPBE=1时，AD转换后的值不满足ADCMPBNSR.CMPLB中设置的条件。

●ADCMPCR.CMPBE=0（ADCMPCR.CMPBE值从1变为0时自动清零）。

43.2.36 ADBUFEN:AD数据缓冲器使能寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0D0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BUFEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BUFEN	数据缓冲区启用 0：不使用数据缓冲区。1：使用数据缓冲区。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

ADBUFEN寄存器设置是否启用数据缓冲区。

BUFEN位（数据缓冲器使能）

该位使能数据缓冲区的使用。

BUFEN=1b时，ADBUFn中存储自诊断结果以外的AD转换结果（加法结果）。

在读取ADBUFPTR之前禁用数据存储操作(BUFEN=0b)。

不要将数据缓冲区用于数据双工或组扫描。

43.2.37 ADBUFPTR:AD数据缓冲区指针寄存器

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0D2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	PTROVF	BUFPTR[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	BUFPTR[3:0]	数据缓冲区指针 这些位指示下一个AD转换数据传输到的数据缓冲区的编号。	R/W

Bit	Symbol	Function	R/W
4	PTROVF	Pointer Overflow Flag 0: The data buffer pointer has not overflowed. 1: The data buffer pointer has overflowed.	R/W
7:5	—	These bits are read as 0. The write value should be 0.	R/W

ADBUFPTR is a register that indicates the data buffer pointer and overflow status.

BUFPTR[3:0] bit (Data Buffer Pointer)

These bits indicate the number of data buffer to which the next A/D converted data is transferred.

When data has been transferred to data buffer 15, the pointer value becomes 0000b and the PTROVF bit is set to 1.

When the next data has been transferred, the data in data buffer 0 is overwritten.

Writing 00h to this register clears the value of these bits. Writing a value other than 00h is disabled.

PTROVF bit (Pointer Overflow Flag)

This bit indicates whether the data buffer pointer has overflowed. This bit is set to 1 when the pointer value becomes 0000b (overflow).

Writing 00h to this register clears this bit value. Writing a value other than 00h is disabled.

43.2.38 ADBUFn : A/D Data Buffer Registers n (n = 0 to 15)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0B0 + 0x2 × n (n = 0 to 15))

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADBUFn															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADBUFn	Converted Value 15 to 0 Functions vary depending on the selected mode and accuracy. See Table 43.22 and Table 43.23.	R

ADBUFn registers are 16-bit read-only registers that sequentially store all A/D conversion results. The automatic clear function is not applied to these registers.

ADBUFn settings are the same as the A/D data register format settings. about details see section 1.2.1 ADDRn : A/D Data Registers n.

The following conditions determine the formats for data in the ADBUFn registers:

- Setting of the Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right)
- Setting of the Addition/Average Count Select bits (ADADC.ADC[2:0]) (1, 2, 3, 4, or 16 times)
- Setting of the Average Mode Enable bit (ADADC.AVEE) (addition or average).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

Table 43.22 shows the bit assignment for each accuracy.

Table 43.22 Bit assignment for each accuracy (1 of 2)

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	These bits are read as 0.				Converted Value 11 to 0: 12-bit A/D-converted value											

Bit	Symbol	Function	R/W
4	PTROVF	指针溢出标志 0：数据缓冲区指针没有溢出。1：数据缓冲区指针溢出。	R/W
7:5	—	这些位被读取为0。写入值应为0。	R/W

ADBUFPTR是指示数据缓冲区指针和溢出状态的寄存器。

BUFPTR[3:0]位（数据缓冲区指针）

这些位指示下一个AD转换数据传输到的数据缓冲区的编号。

当数据已传输到数据缓冲区15时，指针值变为0000b并且PTROVF位设置为1。

当下一个数据传输完毕后，数据缓冲区0中的数据将被覆盖。

向该寄存器写入00h会清除这些位的值。禁止写入00h以外的值。

PTROVF位（指针溢出标志）

该位指示数据缓冲区指针是否溢出。当指针值变为0000b（溢出）时，该位设置为1。

向该寄存器写入00h会清除该位值。禁止写入00h以外的值。

43.2.38 ADBUFn:AD数据缓冲寄存器n(n=0到15)

Base address: ADC12m = 0x4017_0000 + 0x0200 × m (m = 0, 1)

Offset address: 0x0B0 + 0x2 × n (n = 0 to 15))

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	ADBUFn															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	ADBUFn	将值15转换为0 功能因所选模式和精度而异。请参见表43.22和表43.23。	R

ADBUFn寄存器是16位只读寄存器，顺序存储所有AD转换结果。自动清除功能不适用于这些寄存器。

ADBUFn设置与AD数据寄存器格式设置相同。有关详细信息，请参阅第1.2.1节ADDRn:ADData Registers n.

以下条件决定了ADBUFn寄存器中数据的格式：

●寄存器格式选择位(ADCER.ADRFMT)的设置（左对齐或右对齐）

●加法平均计数选择位(ADADC.ADC[2:0])的设置（1、2、3、4或16次）

●设置平均模式启用位(ADADC.AVEE)（加法或平均）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

表43.22显示了每个精度的位分配。

Table 43.22 每个精度的位分配（1of2）

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	这些位读为0。				转换值11到0：12位AD转换值											

Table 43.22 Bit assignment for each accuracy (2 of 2)

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Left-justified data with 12-bit accuracy	Converted Value 11 to 0: 12-bit A/D-converted value												These bits are read as 0.			

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in the A/D-converted value addition mode. When A/D converted value average mode is selected, This register indicatesThese registers indicate the mean of A/D-converted values on a specific channel. The value is stored in the A/D data register based on the setting of the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 12-bit, 10-bit, 8-bit accuracy, 1, 2, 3, or 4 times can be selected in the A/D-converted value addition mode. A/D conversion results are stored in the A/D data register as a 2-bit-extended value of the specified conversion accuracy.

For 12-bit accuracy, 16 times can also be selected in the A/D-converted value addition mode. In A/D-converted value addition mode, this register indicatesthese registers indicate the value that is obtained by adding A/D-converted values on a specific channel. A/D conversion results are stored in the A/D data register as a 4-bit-extended value of the specified conversion accuracy.

When A/D-converted value addition mode is selected, the value is stored in the A/D data register based on the settings of the A/D Data Register Format Select bits.

Table 43.23 shows the bit assignment for each accuracy.

Table 43.23 Bit assignment for each accuracy when A/D-converted value addition mode is selected

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Right-justified data with 12-bit accuracy	When 16 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 1, 2, 3, or 4 conversion times is specified	These bits are read as 0.	Added Value 13 to 0: 14-bit sum of A/D conversion results														
Left-justified data with 12-bit accuracy	When 1, 2, 3, or 4 conversion times is specified	Added Value 15 to 0: 16-bit sum of A/D conversion results															
	When 16 conversion times is specified	Added Value 13 to 0: 14-bit sum of A/D conversion results														These bits are read as 0.	

43.3 Operation

43.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

Scan conversion is performed in any of the three operating modes:

- Single scan mode
- Continuous scan mode
- Group scan mode

In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until software sets the ADCSR.ADST bit to 0. In group scan mode, the selected channels in group A, B are scanned once after scan starts in response to the respective synchronous trigger.

In single scan mode and continuous scan mode, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for the ANn channels in group A selected in the ADANSA0 and ADANSA1 registers, and for the

Table 43.22 每种精度的位分配（2个中的2个）

Accuracy	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的左对齐数据	转换值11到0：12位AD转换值												这些位读为0。			

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenADconvertedvalueaveragemodeisselected ThisregisterindicatesTheseregistersindicatethemeanofAD-convertedvaluesonaspecificchannel.该值根据AD的设置存储在AD数据寄存器中

数据寄存器格式选择位的方式与正常AD转换相同。

(3) 选择AD转换值相加模式时

对于12位、10位、8位精度，可以在AD转换值相加模式中选择1、2、3或4次。AD转换结果作为指定转换精度的2位扩展值存储在AD数据寄存器中。

对于12位精度，在AD转换值相加模式中也可以选择16倍。在AD转换值相加模式下，该寄存器表示这些寄存器表示通过在特定通道上添加AD转换值获得的值。AD转换结果作为指定转换精度的4位扩展值存储在AD数据寄存器中。

WhenAD-convertedvalueadditionmodeisselected thevalueisstoredintheADdataregisterbasedonthesettingsoftheADDataRegisterFormatSelectbits.

表43.23显示了每个精度的位分配。

Table 43.23 选择AD转换值相加模式时的每个精度的位分配

Accuracy		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
具有12位精度的右对齐数据	指定16个转换时间时	附加值15到0：AD转换结果的16位和															
	指定1、2、3或4转换时间时	这些位读为0。	附加值13到0：AD转换结果的14位和														
具有12位精度的左对齐数据	指定1、2、3或4转换时间时	附加值15到0：AD转换结果的16位和															
	指定16个转换时间时	附加值13到0：AD转换结果的14位和														这些位读为0。	

43.3 Operation

43.3.1 扫描操作

扫描时，对指定通道的模拟输入依次进行AD转换。

扫描转换在以下三种操作模式中的任何一种中执行：

- ●单次扫描模式
- ●连续扫描模式
- ●组扫描模式

在单次扫描模式下，一个或多个指定通道被扫描一次。在连续扫描模式下，重复扫描一个或多个指定通道，直到软件将ADCSR.ADST位设置为0。在组扫描模式下，在扫描开始后对A、B组中选定的通道进行一次扫描，以响应相应的同步触发.

在单次扫描模式和连续扫描模式下，对选择的ANn通道进行AD转换
ADANSA0和ADANSA1寄存器，从编号n最小的通道开始。在组扫描模式下，对在ADANSA0和ADANSA1寄存器中选择的A组中的ANn通道执行AD转换，并为

RA生态工作

ANn channels in group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.

When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three reference voltages is converted.

The temperature sensor output and internal reference voltage can be selected at the same time as the analog input of the channels, and A/D conversion is performed on the analog input of channels, temperature sensor output, and internal reference voltage, in that order.

Double trigger mode can be used with single scan mode or group scan mode. With double trigger mode enabled (ADCSR.DBLE = 1), A/D conversion data of a channel selected in the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits. In group scan mode, only group A can use double trigger mode.

In the extended operation of double trigger mode, the A/D conversion operation is generated from the synchronous trigger combination selected in the ADSTRGR.TRSA[5:0] bits. In addition to normal double trigger mode operation, A/ D conversion data with odd number trigger (ELC_AD00 (unit 0) and ELC_AD10 (unit 1)) is stored in A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data with even number trigger (ELC_AD01 (unit 0) and ELC_AD11 (unit 1)) is stored in A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double trigger mode, when one of the trigger combinations occurs at the same time, the data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored in A/D Data Duplexing Register B (ADDBLDRB).

The ADC12 ignores a synchronous trigger that occurs during the A/D conversion started by another synchronous trigger.

43.3.2 Single Scan Mode

43.3.2.1 Basic Operation

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated.
4. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC12 then enters a wait state.

在ADANSB0和ADANSB1寄存器中选择的B组中的ANn通道，从具有最小编号n的通道开始。

选择自诊断时，在每次扫描开始时执行一次，并转换三个参考电压之一。

温度传感器输出和内部参考电压可以与通道的模拟输入同时选择，通道的模拟输入、温度传感器输出和内部参考电压依次进行AD转换。

双触发模式可与单扫描模式或组扫描模式一起使用。启用双触发模式(ADCSR.DBLE=1)时，仅当转换由ADSTRGR中选择的同步触发(ELC)启动时，ADCSR.DBLANS[4:0]位中选择的通道的AD转换数据才会被复制.TRSA[5:0]位。在组扫描模式下，只有A组可以使用双触发模式。

在双触发模式的扩展操作中，ADSTRGR.TRSA[5:0]位中选择的同步触发组合产生AD转换操作。除了正常的双触发模式操作外，奇数触发的AD转换数据（ELC_AD00（单元0）和ELC_AD10（单元1））存储在AD数据双工寄存器A（ADDBLDRA）中，偶数触发的AD转换数据（ELC_AD01（单元0）和ELC_AD11（单元1））存储在AD数据双工寄存器B（ADDBLDRB）中。在双触发模式的扩展操作中，当其中一种触发组合同时发生时，指定触发的数据双工寄存器设置不起作用，AD转换数据存储在AD数据双工寄存器B（ADDBLDRB）中。

ADC12忽略由另一个同步触发启动的AD转换期间发生的同步触发。

43.3.2 单次扫描模式

43.3.2.1 基本操作

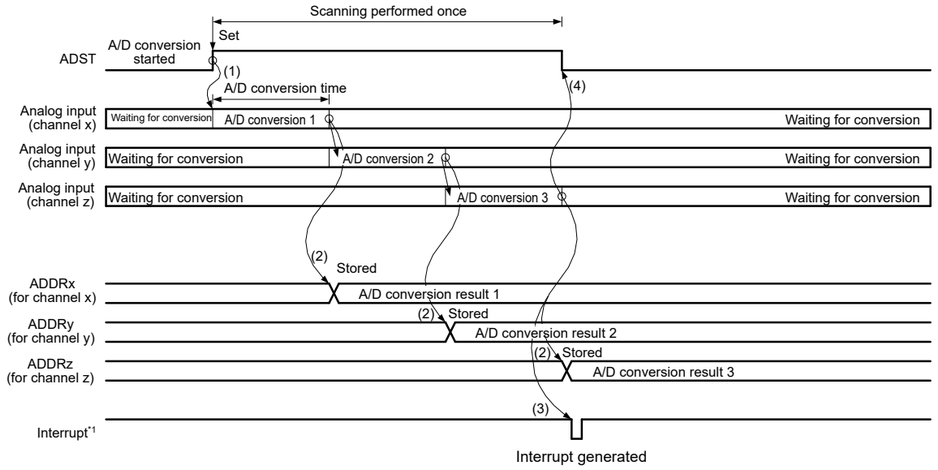
在单扫描模式的基本操作中，对指定通道的模拟输入进行一次AD转换，如下所示：

1.当通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，对在ADANSA0和ADANSA1中选择的ANn通道执行AD转换寄存器，从具有最小编号n的通道开始。

2.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器（ADDRy）中。

3.当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求。

4.ADST位在AD转换期间保持1（AD转换开始），当所有选定通道的AD转换完成时自动设置为0。ADC12然后进入等待状态。



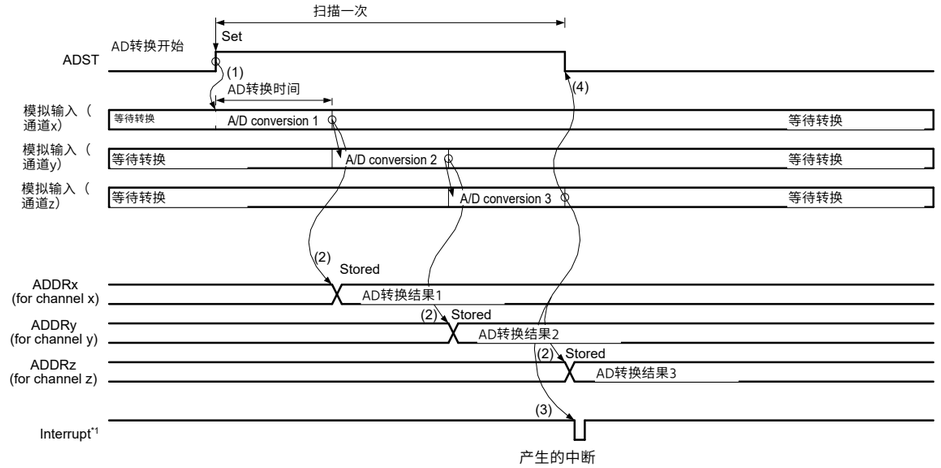
Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. ADC12i_ADI (i = 0, 1)

Figure 43.8 Example basic operation in single scan mode when the analog inputs (channel x to z) are selected

43.3.2.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0, VREFH (×0 ×1/2, or ×1), then A/D conversion is performed once on the analog input of the selected channels as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated.
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion of all the selected channels completes. The ADC12 then enters a wait state.



Note: x、y和z(x<y<z)是ADANSA01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)

Figure 43.8 选择模拟输入（通道x至z）时单次扫描模式下的基本操作示例

43.3.2.2 频道选择和自诊断

选择通道和自诊断时，首先对参考电压VREFH0进行AD转换，
VREFH(×0×12或×1)，然后在所选通道的模拟输入上执行一次AD转换，如下所示：

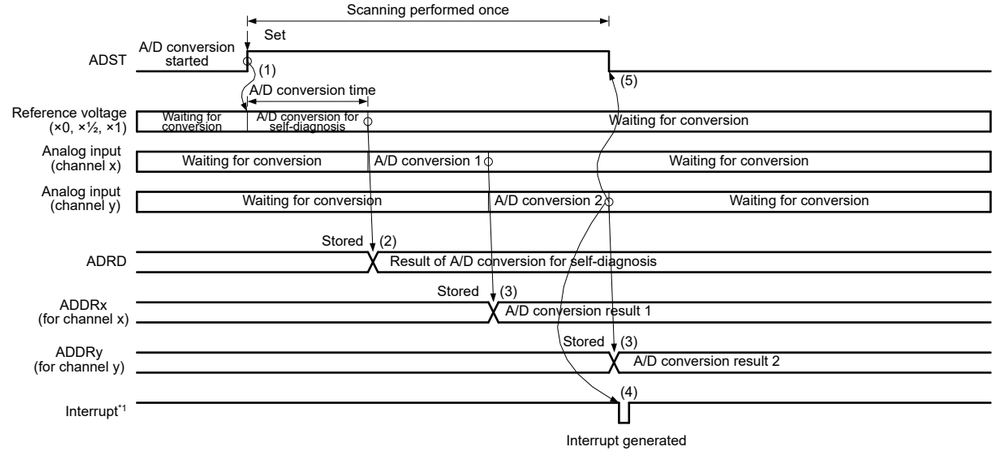
1.通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。

2.当用于自诊断的AD转换完成时，AD转换结果存储在AD自诊断数据寄存器(ADRD)中。然后对在ADANSA0和ADANSA1寄存器中选择的ANn通道执行D转换，从编号最小的通道开始。

3.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器（ADDRy）中。

4.当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求。

5.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动设置为0。ADC12然后进入等待状态。



Note: x and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. ADC12i_ADI (i = 0, 1)

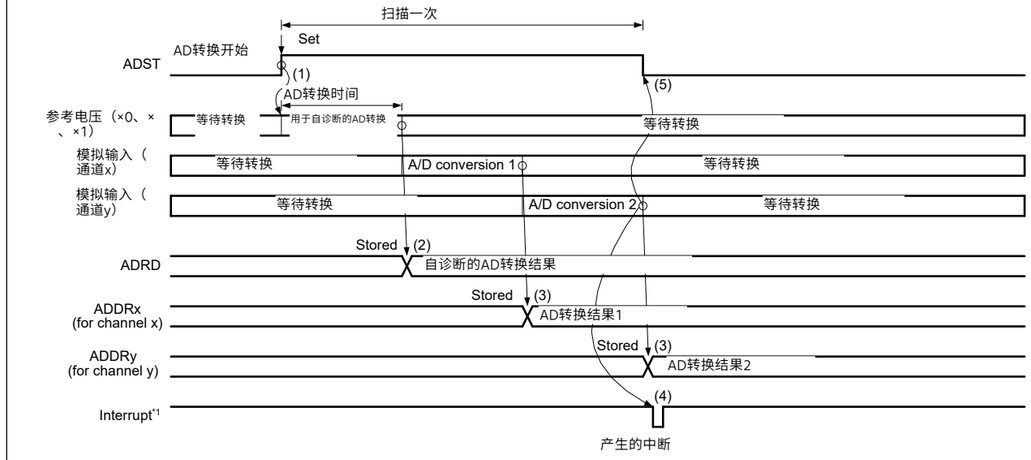
Figure 43.9 Example basic operation in single scan mode when the analog inputs (channel x and y) are selected with self- diagnosis

43.3.2.3 A/D conversion of temperature sensor output or internal reference voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is performed first on the analog input of the selected channels, and once on the temperature sensor output or internal reference voltage. When both temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order. With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of the temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 on completion of A/D conversion. Then, the ADC12 enters a wait state.



Note: x和y(x<y)是ADANSA01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)

Figure 43.9 使用自诊断选择模拟输入（通道x和y）时单次扫描模式下的基本操作示例

43.3.2.3 温度传感器输出或内部参考电压的AD转换

当同时选择通道和温度传感器输出或内部参考电压时，首先对所选通道的模拟输入进行AD转换，再对温度传感器输出或内部参考电压进行一次AD转换。当同时选择温度传感器输出和内部参考电压时，按顺序执行温度传感器输出和内部参考电压的AD转换。取消选择通道后，也可以仅选择温度传感器输出或内部参考电压。

操作如下：

1.当软件触发、同步触发(ELC)或异步触发将ADCSR.ADST位设置为1（AD转换开始）时，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从通道开始用最小的数n。

2.在通道上完成AD转换后，结果存储在相关的AD数据寄存器y(ADDRy)中，然后温度传感器输出的AD转换开始。

3.温度传感器输出的AD转换完成后，结果存储在相关的AD中
温度传感器数据寄存器(ADTSDR)，然后内部参考电压的AD转换开始。

4.内部参考电压的AD转换完成后，结果存储在相关的ADInternal
参考电压数据寄存器(AOCDR)，并产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。

5.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动清零。然后，ADC12进入等待状态。

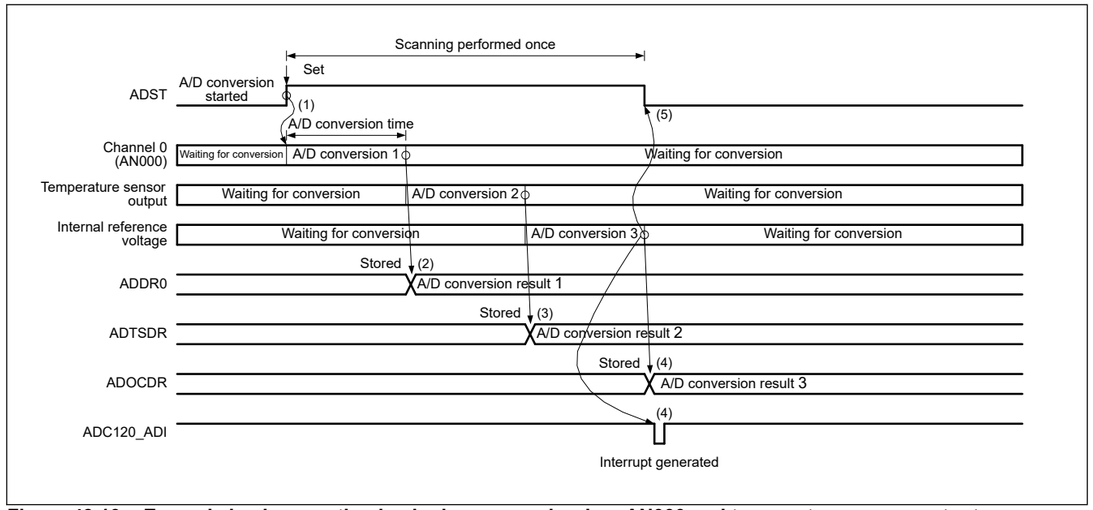


Figure 43.10 Example basic operation in single scan mode when AN000 and temperature sensor output or internal reference voltage are selected

43.3.2.4 A/D conversion in double-trigger mode

When double trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence.

Deselect self-diagnosis and set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA and ADEXICR.TSSB) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA and ADEXICR.OCSB) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double trigger mode, select a synchronous trigger (ELC) with the ADSTRGR.TRSA[5:0] bits. Additionally, set the ADCSR.EXTRG bit to 0 and the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC12 enters a wait state. An ADC12i_ADI (i = 0, 1) interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR), which is exclusively used in double-trigger mode.
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated.
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically set to 0 when A/D conversion completes. Then the ADC12 enters a wait state.

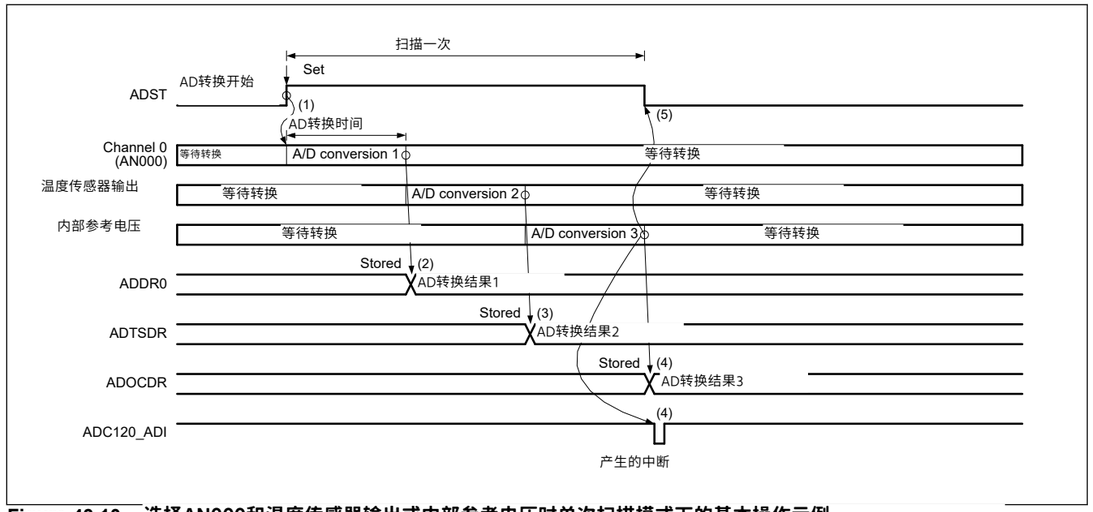


Figure 43.10 选择AN000和温度传感器输出或内部参考电压时单次扫描模式下的基本操作示例

43.3.2.4 双触发模式下的AD转换

在单扫描模式下选择双触发模式时，由同步触发(ELC)启动的两轮单扫描操作将依次执行。

取消选择自诊断并设置温度传感器输出AD转换选择位(ADEXICR.TSSA和ADEXICR.TSSB)和内部参考电压AD转换选择位(ADEXICR.OCSA和ADEXICR.OCSB)为0。

AD转换数据的复制通过在ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。当ADCSR.DBLE位设置为1时，使用ADANSA0和ADANSA1寄存器的通道选择无效。

在双触发模式下，使用ADSTRGR.TRSA[5:0]位选择同步触发(ELC)。此外，设置ADCSR.EXTRG位为0，ADCSR.TRGE位为1。不要使用软件触发。

操作如下：

1.当同步触发输入(ELC)将ADCSR.ADST位设置为1（AD转换开始）时，ADCSR.DBLANS[4:0]位中选择的单通道开始AD转换。

2.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器y(ADDRy)中。

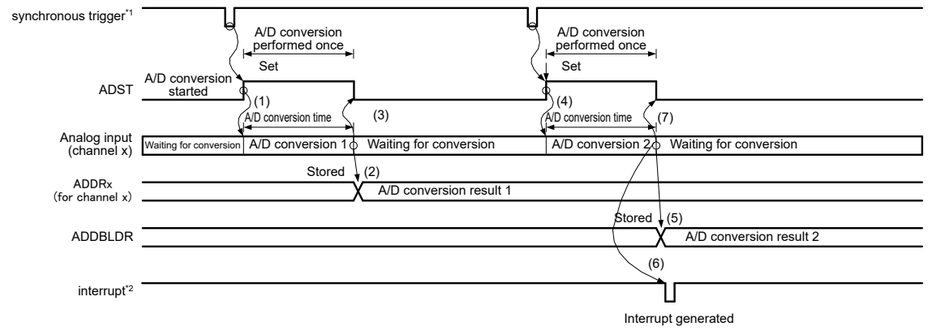
3.ADCSR.ADST位自动设置为0，ADC12进入等待状态。不会产生ADC12i_ADI(i=0 1)中断请求。

4.当第二个触发输入将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单通道上开始。

5.当AD转换完成时，结果存储在AD数据双工寄存器(ADDBLDR)中，该寄存器专用于双触发模式。

6.产生一个ADC12i_ADI(i=0 1)中断请求。

7.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动设置为0。然后ADC12进入等待状态。



Note: x is the selected channel number by ADANSA0/1.
Note 1. ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1)
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.11 Example operation in single scan mode when double-trigger mode is selected and the analog input (channel x) is duplicated

43.3.2.5 Extended operations when double-trigger mode is selected

When double trigger mode is selected in single scan mode, and a synchronous trigger (ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1)) is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

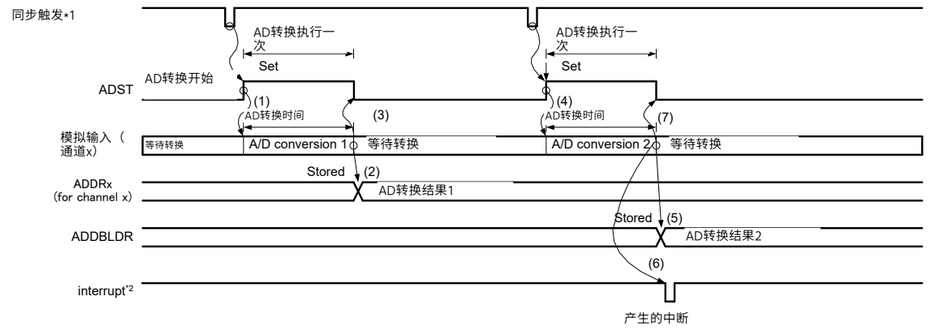
Deselect self-diagnosis and set the temperature sensor output A/D conversion select bit (ADEXICR.TSSA and ADEXICR.TSSB), and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA and ADEXICR.OCSB) to 0.

Duplication of A/D conversion data is enabled by setting the channel number to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double trigger mode, select a synchronous trigger combination ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ ELC_AD01 (unit 0) and ELC_AD11 (unit 1) by setting the ADSTRGR.TRSA[5:0] bits to 0x0B, set the ADCSR.EXTRG bit to 0, and set the ADCSR.TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1)), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the ELC_ADi0 or ELC_ADi1 trigger is input respectively (i = 1).
3. The ADCSR.ADST bit is automatically set to 0 and the ADC12 enters a wait state. An ADC12i_ADI (i = 0, 1) interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger (ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1)), A/ D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the A/D conversion result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the ELC_ADi0 or ELC_ADi1 trigger is input respectively (i = 1).
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated.



Note: x是ADANSA01选择的通道号。
注1.ELC_AD00（单元0）和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1）
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.11 选择双触发模式并复制模拟输入（通道x）时的单扫描模式操作示例

43.3.2.5 选择双触发模式时的扩展操作

在单扫描模式下选择双触发模式时，选择同步触发（ELC_AD00（单元0）和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1））作为AD转换开始的触发，执行两轮单扫描操作。

取消选择自诊断并设置温度传感器输出AD转换选择位(ADEXICR.TSSA和ADEXICR.TSSB），内部参考电压AD转换选择位（ADEXICR.OCSA和ADEXICR.OCSB）为0。

通过将要复制的通道号设置为ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1，启用AD转换数据的复制。当ADCSR.DBLE位设置为1时，通道选择使用ADANSA0和ADANSA1寄存器无效。

在扩展双触发模式下，通过将ADSTRGR.TRSA[5:0]位设置为0x0B，选择同步触发组合ELC_AD00（单元0）和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1），设置ADCSR.EXTRG位为0，ADCSR.TRGE位为1。不要使用软件触发。

操作如下：

1.当同步触发输入（ELC_AD00（单元0）和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1））将ADCSR.ADST位设置为1（AD转换开始）时，AD转换开始在ADCSR.DBLANS[4:0]位中选择的单个通道上。

2.当AD转换完成时，当ELC_ADi0或ELC_ADi1触发输入时，AD转换结果分别存储在相关的AD数据寄存器(ADDRy)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中(i=1)。

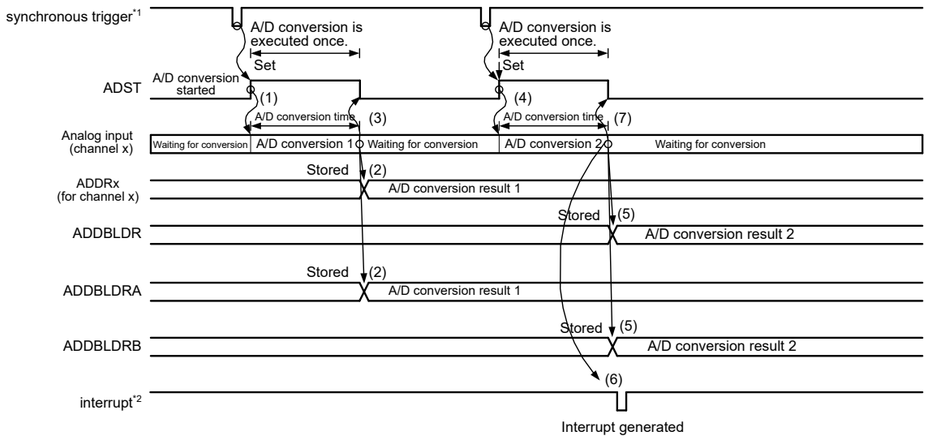
3.ADCSR.ADST位自动设置为0，ADC12进入等待状态。不会产生ADC12i_ADI(i=0 1)中断请求。

4.当ADCSR.ADST位被第二次触发(ELC_AD00(unit0)和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1）），AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。

5.当AD转换完成时，当ELC_ADi0或ELC_ADi1触发输入时，AD转换结果分别存储在AD数据双工寄存器(ADDBLDR)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中(i=1)。

6.产生一个ADC12i_ADI(i=0 1)中断请求。

7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically set to 0 when A/D conversion completes. The ADC12 then enters a wait state.



Note: x is the selected channel number by ADANSA0/1.
Note 1. ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1)
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.12 Example extended operation in double trigger mode with duplication selected for the analog input (channel x) and ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1)

43.3.3 Continuous Scan Mode

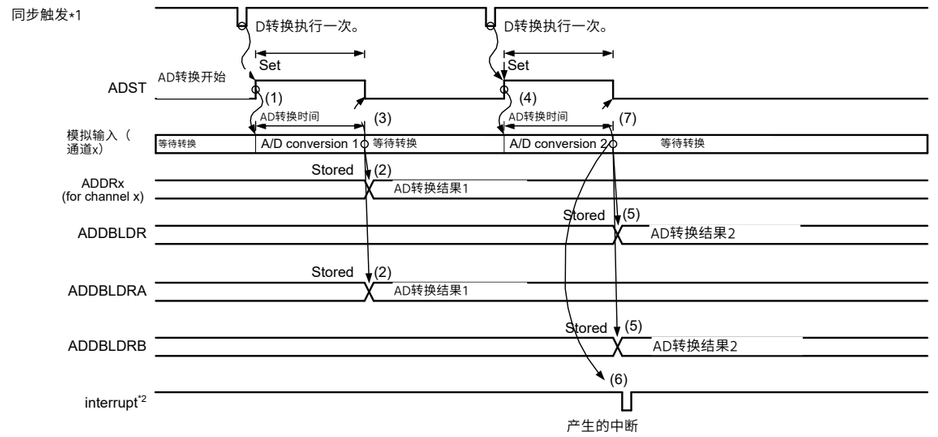
43.3.3.1 Basic Operation

In continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input, A/D conversion is performed for ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated. The ADC12 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADCSR.ADST bit is not automatically cleared, and steps 2. and 3. are repeated as long as ADCSR.ADST remains 1 (A/ D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
5. When the ADCSR.ADST bit is later set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.

7.ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动设置为0。ADC12然后进入等待状态。



Note: x是ADANSA01选择的通道号。
注1.ELC_AD00（单元0）和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1）
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.12 双触发模式下的扩展操作示例，为模拟输入（通道x）和ELC_AD00（单元0）和ELC_AD10（单元1）选择了重复ELC_AD01（单元0）和ELC_AD11（单元1）

43.3.3 连续扫描模式

43.3.3.1 基本操作

在连续扫描模式下，对指定通道的模拟输入重复进行AD转换。

操作如下：

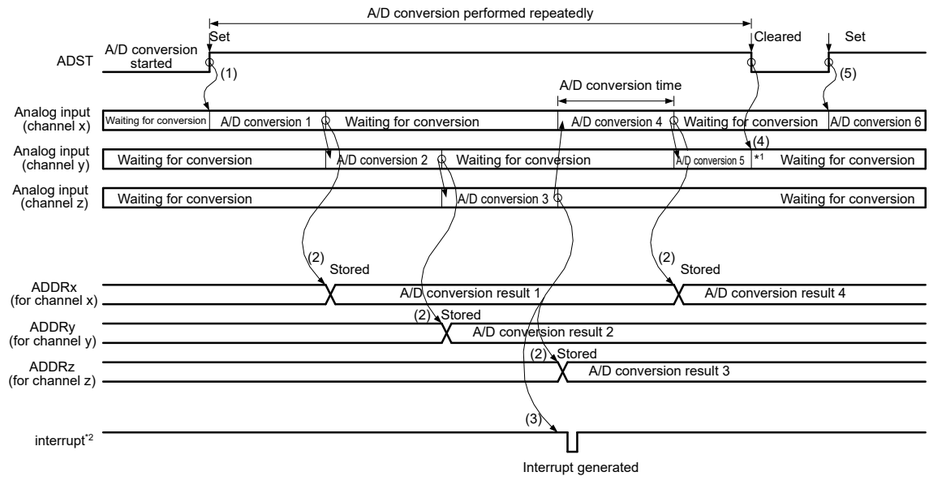
1.当软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，对在ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从编号n最小的通道开始。

2.每次完成单个通道的AD转换，AD转换结果存储在相关的AD数据寄存器(ADDRy)中。

3.当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求。ADC12从编号n最小的通道开始依次启动ADANSA0和ADANSA1寄存器中选择的ANn通道的A/D转换。

4.ADCSR.ADST位不会自动清零，只要ADCSR.ADST保持1（AD转换开始），就会重复步骤2.和3.。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。

5.当ADCSR.ADST位稍后设置为1（AD转换开始）时，AD转换再次开始在ADANSA0和ADANSA1寄存器中选择的ANn通道，从具有最小编号n的通道开始。



Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. Data for A/D conversion 5 is ignored.
Note 2. ADC12i_ADI (i = 0, 1)

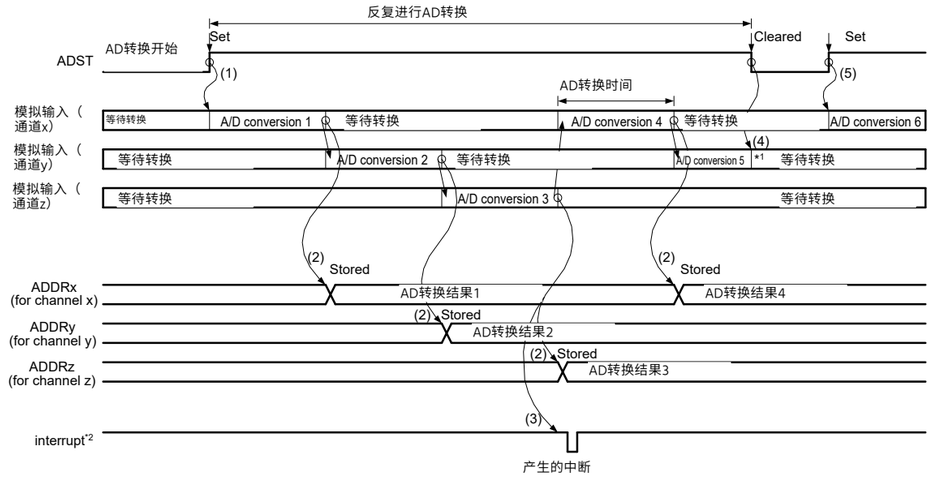
Figure 43.13 Example basic operation in continuous scan mode when the analog inputs (channel x to z) are selected

43.3.3.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0, VREFH (×0, ×1/2, or ×1) supplied to the ADC12, and A/D conversion is performed on the analog input of the selected channels. This sequence is repeated as described in the section that follows.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (ELC), or an asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the corresponding A/D Data Register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated. At the same time, the ADC12 starts A/D conversion for self-diagnosis and then on the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADCSR.ADST bit is not automatically cleared, and steps 2. to 4. are repeated as long as the ADCSR.ADST bit remains 1.When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.



Note: x、y和z(x<y<z)是ADANSA01选择的通道号。
注1.AD转换5的数据被忽略。
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.13 选择模拟输入（通道x至z）时连续扫描模式下的基本操作示例

43.3.3.2 频道选择和自诊断

同时选择通道和自诊断时，首先对参考电压进行A/D转换
提供给ADC12的VREFH0、VREFH（×0、×12或×1），并对所选通道的模拟输入执行AD转换。如以下部分所述重复此序列。

操作如下：

1.通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。

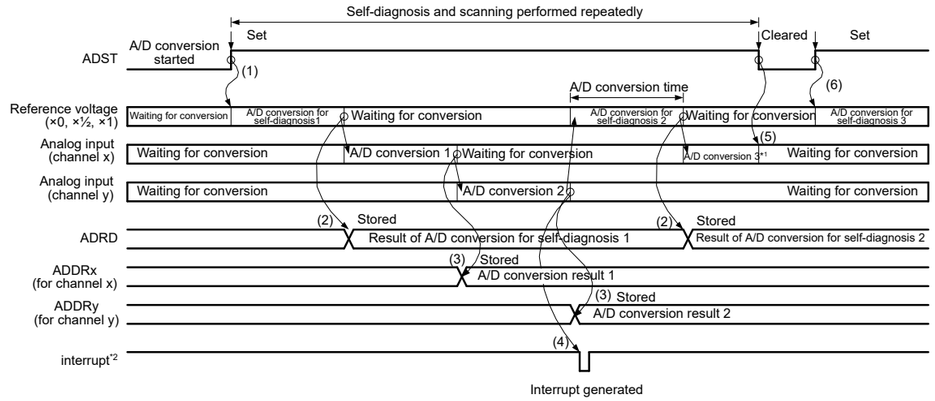
2.当用于自诊断的AD转换完成时，AD转换结果存储在AD自诊断数据寄存器(ADRD)中。然后对在ADANSA0和ADANSA1寄存器中选择的ANn通道执行D转换，从编号最小的通道开始。

3、每完成一次单通道的AD转换，AD转换结果存入对应的AD数据寄存器（ADDRy）。

4.当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求。同时，ADC12启动AD转换进行自诊断，然后在选择的ANn通道上进行自诊断。
ADANSA0和ADANSA1寄存器，从编号n最小的通道开始。

5.ADCSR.ADST位不会自动清零，只要ADCSR.ADST位保持为1，就会重复步骤2.到4.。当ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。

6.当ADST位稍后设置为1（AD转换开始）时，用于自诊断的AD转换再次开始。



Note: x and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. Data for A/D conversion 3 is ignored.
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.14 Example basic operation in continuous scan mode when the analog inputs (channel x and y) selected with self- diagnosis

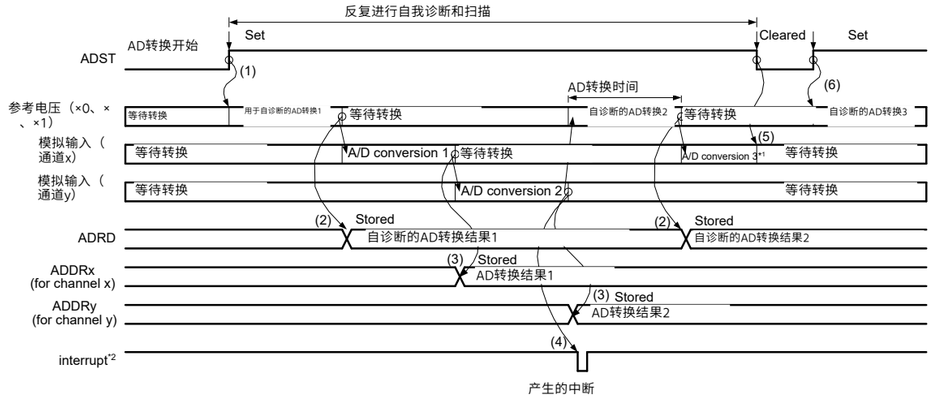
43.3.3.3 A/D conversion of temperature sensor output or internal reference voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then the A/D conversion of the temperature sensor output or internal reference voltage is repeated. When both the temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order.

With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC12i_ADI (i = 0, 1) interrupt request is generated. In addition, the ADC12 continuously starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.
5. The ADCSR.ADST bit is not cleared automatically, and steps 2 to 4 are repeated as long as this bit remains set to 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.



Note: x和y(x<y)是ADANSA01选择的通道号。
注1.AD转换3的数据被忽略。
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.14 使用自诊断选择模拟输入（通道x和y）时连续扫描模式下的基本操作示例

43.3.3.3 温度传感器输出或内部参考电压的AD转换

当同时选择通道和温度传感器输出或内部参考电压时，首先对所选通道的模拟输入进行AD转换，然后重复温度传感器输出或内部参考电压的AD转换。当同时选择温度传感器输出和内部参考电压时，按顺序执行温度传感器输出和内部参考电压的AD转换。

取消选择通道后，也可以仅选择温度传感器输出或内部参考电压。

操作如下：

1.当软件触发、同步触发(ELC)或异步触发将ADCSR.ADST位设置为1（AD转换开始）时，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从通道开始用最小的数n。

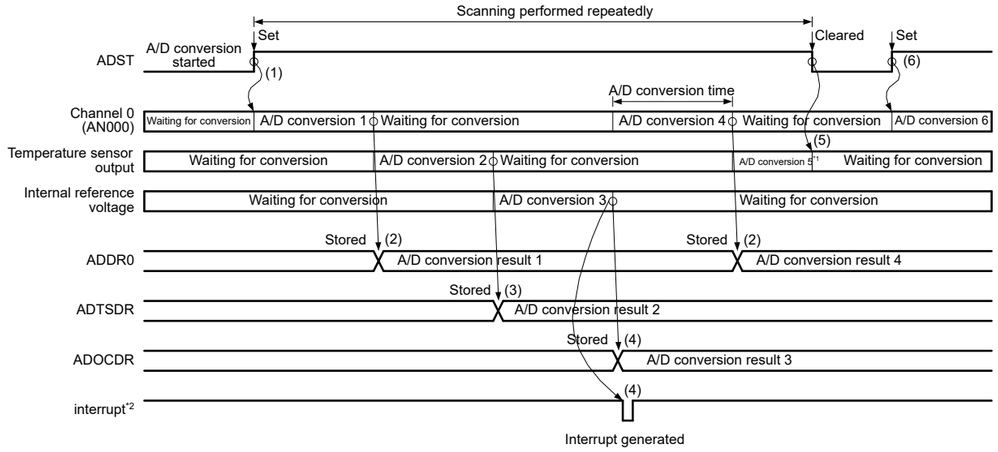
2.通道上的AD转换完成后，结果存储在相关的AD数据寄存器y(ADDRy)中，然后温度传感器输出的AD转换开始。

3.温度传感器输出的AD转换完成后，结果存储在相关的AD中
温度传感器数据寄存器(ADTSDR)，然后内部参考电压的AD转换开始。

4.内部参考电压的AD转换完成后，结果存储在相关的ADInternal
参考电压数据寄存器(AOCDR)和ADC12i_ADI(i=0 1)中断请求产生。此外，ADC12连续启动ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换，从编号最小的通道n开始。

5.ADCSR.ADST位不会自动清零，只要该位保持设置为1，就会重复步骤2到4。
当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。

6.当ADCSR.ADST位被设置为1（AD转换开始）时，AD转换再次开始在ADANSA0和ADANSA1寄存器中选择的ANn通道，从编号最小的通道n开始。



Note 1. Data for A/D conversion 5 is ignored.
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.15 Example basic operation in continuous scan mode when AN000 and temperature sensor output or internal reference voltage are selected

43.3.4 Group Scan Mode

43.3.4.1 Basic operation

In group scan mode, A/D conversion is performed once on the analog input of all the specified channels in group A and B after scanning is started by a synchronous trigger (ELC). The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for group A and B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

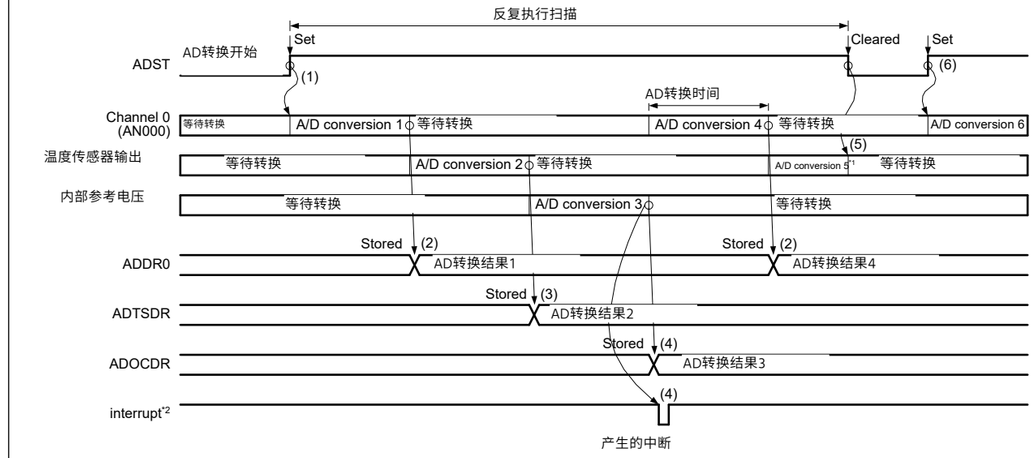
The group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers and the ADEXICR.TSSA and OCSA bits. The group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers and the ADEXICR.TSSB and OCSB bits. Group A and B cannot use the same channels.

When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for Group A and B.

The following sequence describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 (unit 0) and ELC_AD10 (unit 1) trigger from the ELC is used to start conversion of group A and the ELC_AD01 (unit 0) and ELC_AD11 (unit 1) trigger from the ELC is used to start conversion of group B. In addition, ELC_AD00 (unit 0) and ELC_AD10 (unit 1) and ELC_AD01 (unit 0) and ELC_AD11 (unit 1) are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group A is started by ELC_AD00 (unit 0) and ELC_AD10 (unit 1).
2. When group A scanning completes, an ADC12i_ADI (i = 0, 1) interrupt is generated (no register setting).
3. Scanning of group B is started by ELC_AD01 (unit 0) and ELC_AD11 (unit 1).
4. When group B scanning completes, an ADC12i_GBADI (i = 0, 1) interrupt is generated if the ADCSR.GBADIE bit is 1 (ADC12i_GBADI (i = 0, 1) interrupt when scanning completion is enabled).



注1.AD转换5的数据被忽略。
Note 2. ADC12i_ADI (i = 0, 1)

Figure 43.15 选择AN000和温度传感器输出或内部参考电压时连续扫描模式下的基本操作示例

43.3.4 组扫描模式

43.3.4.1 基本操作

在组扫描模式下，通过同步触发（ELC）开始扫描后，对A组和B组中所有指定通道的模拟输入进行一次AD转换。每组的扫描操作类似于单次扫描模式下的扫描操作。

可以在A组的ADSTRGR.TRSA[5:0]位和B组的ADSTRGR.TRSB[5:0]位中选择同步触发。对A组和B组使用不同的触发以防止同时进行AD转换两组。不要使用软件触发。

使用ADANSA0和ADANSA1寄存器选择要进行AD转换的A组通道
ADXICR.TSSA和OCSA位。要进行AD转换的B组通道使用ADANSB0和
ADANSB1寄存器以及ADXICR.TSSB和OCSB位。A组和B组不能使用相同的通道。

在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

以下序列描述了使用来自ELC的同步触发在组扫描模式下的操作。在此示例中，来自ELC的ELC_AD00（单元0）和ELC_AD10（单元1）触发器用于启动A组的转换，来自ELC的ELC_AD01（单元0）和ELC_AD11（单元1）触发器用于启动转换B组。此外，

ELC_AD00（单元0）和ELC_AD10（单元1）和ELC_AD01（单元0）和ELC_AD11（单元1）被选择用于相关ELC.ELSRn寄存器中的GPT事件。

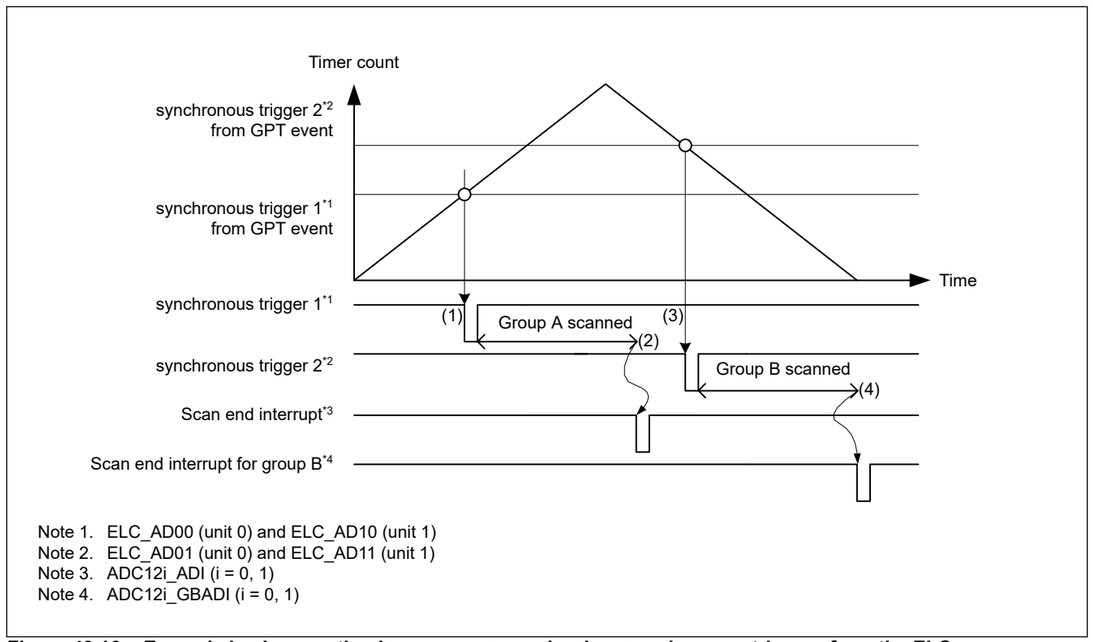
操作如下：

1.A组扫描由ELC_AD00（单元0）和ELC_AD10（单元1）启动。

2.A组扫描完成后，会产生ADC12i_ADI(i=0 1)中断（无寄存器设置）。

3.B组扫描由ELC_AD01（单元0）和ELC_AD11（单元1）启动。

4.B组扫描完成时，如果ADCSR.GBADIE位为1，则产生ADC12i_GBADI(i=0 1)中断（使能扫描完成时的ADC12i_GBADI(i=0 1)中断）。



Note 1. ELC_AD00 (unit 0) and ELC_AD10 (unit 1)
Note 2. ELC_AD01 (unit 0) and ELC_AD11 (unit 1)
Note 3. ADC12i_ADI (i = 0, 1)
Note 4. ADC12i_GBADI (i = 0, 1)

Figure 43.16 Example basic operation in group scan mode when synchronous triggers from the ELC are used

43.3.4.2 A/D conversion in double-trigger mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed as a sequence for group A. For group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, the synchronous trigger can be selected in the ADSTRGR.TRSA[5:0] bits for group A and in the ADSTRGR.TRSB[5:0] bits for group B. Use different triggers for groupA, B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger.

When an ELC_AD00 (unit 0) and ELC_AD10 (unit 1)/ELC_AD01 (unit 0) and ELC_AD11 (unit 1) is selected as group A synchronous triggers by setting the ADSTRGR.TRSA[5:0] bits to 0x0B, operation proceeds in extended double trigger mode.

The group A channel to be A/D-converted is selected using the DBLANS[4:0] bits in the ADCSR register, while the group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. Group A, B cannot use the same channels.

When double-trigger mode is selected in group scan mode, set the A/D conversion select bits for both the temperature sensor output (ADEXICR.TSSA) and the internal reference voltage (ADEXICR.OCSA) to 0 (deselected).

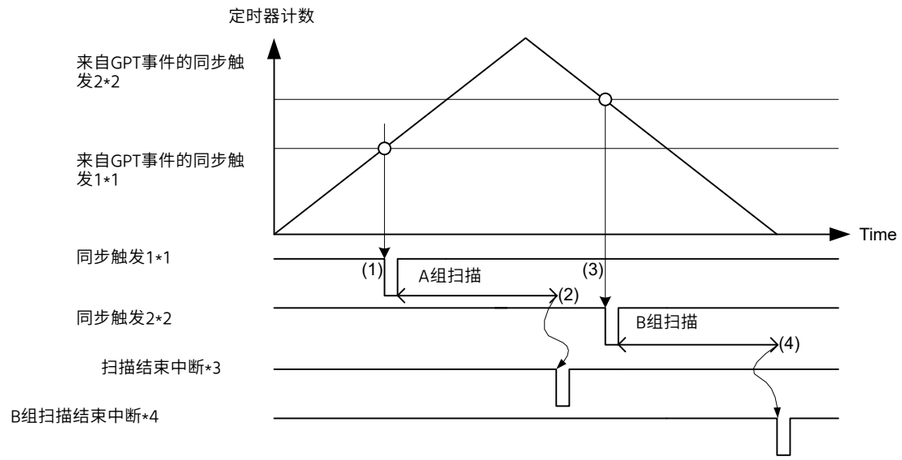
Self-diagnosis cannot be selected when double trigger mode is selected in group scan mode.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1.

The following sequence describes operation in group scan mode with double trigger mode selected and using a synchronous trigger from the ELC. In this example, the ELC_AD00 (unit 0) and ELC_AD10 (unit 1) trigger is used to start conversion of group A and the ELC_AD01 (unit 0) and ELC_AD11 (unit 1) trigger is used to start conversion of group B. In addition, ELC_AD00 (unit 0) and ELC_AD10 (unit 1) and ELC_AD01 (unit 0) and ELC_AD11 (unit 1) are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of group B is started by the ELC_AD00 (unit 0) and ELC_AD10 (unit 1) trigger from the ELC.



注1.ELC_AD00（单元0）和ELC_AD10（单元1）注2.
ELC_AD01（单元0）和ELC_AD11（单元1）
Note 3. ADC12i_ADI (i = 0, 1)
Note 4. ADC12i_GBADI (i = 0, 1)

Figure 43.16 使用来自ELC的同步触发时组扫描模式下的基本操作示例

43.3.4.2 双触发模式下的AD转换

在组扫描模式中选择双触发模式时，由同步触发(ELC)启动的两轮单扫描操作作为A组的顺序执行。对于B组，由同步触发(ELC)启动的单扫描操作是执行一次。

在组扫描模式下，可以在ADSTRGR.TRSA[5:0]位中为A组选择同步触发，并在组B的ADSTRGR.TRSB[5:0]位。对组A、B使用不同的触发，以防止两组同时进行AD转换。不要使用软件触发或异步触发。

当通过将ADSTRGR.TRSA[5:0]位设置为0x0B来选择ELC_AD00（单元0）和ELC_AD10（单元1）ELC_AD01（单元0）和ELC_AD11（单元1）作为A组同步触发时，操作以扩展方式进行双触发模式。

使用ADCSR寄存器中的DBLANS[4:0]位选择要进行AD转换的A组通道，而组使用ADANSB0和ADANSB1寄存器选择要进行AD转换的B通道。A、B组不能使用相同的通道。

在组扫描模式下选择双触发模式时，将温度传感器输出(ADEXICR.TSSA)和内部参考电压(ADEXICR.OCSA)的AD转换选择位设置为0（取消选择）。

在组扫描模式下选择双触发模式时，不能选择自诊断。

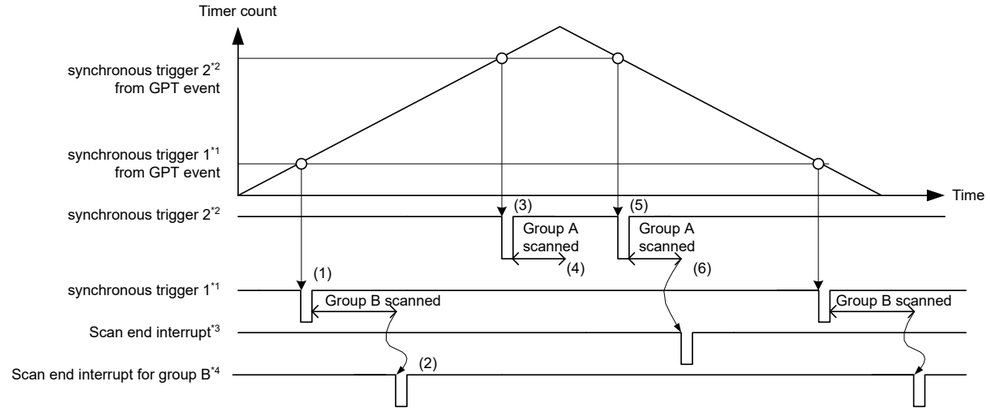
AD转换数据的复制通过在ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。

以下序列描述了组扫描模式下的操作，其中选择了双触发模式并使用来自ELC的同步触发。在此示例中，ELC_AD00（单元0）和ELC_AD10（单元1）触发器用于启动A组转换，ELC_AD01（单元0）和ELC_AD11（单元1）触发器用于启动B组转换。此外，ELC_AD00（单元0）和ELC_AD10（单元1）和ELC_AD01（单元0）和ELC_AD11（单元1）在关联的ELC.ELSRn寄存器中为GPT事件选择。

操作如下：

1.B组的扫描由ELC的ELC_AD00（单元0）和ELC_AD10（单元1）触发开始。

2. When group B scanning completes, an ADC12i_GBADI (i = 0, 1) interrupt is generated if the GBADIE bit in ADCSR is 1 (ADC12i_GBADI (i = 0, 1) interrupt when scanning completion is enabled).
3. The first scan of group A is started by the first ELC_AD01 (unit 0) and ELC_AD11 (unit 1) trigger.
4. When the first scan of group A completes, the conversion result is stored in the associated A/D Data Register y (ADDRy); an ADC12i_ADI (i = 0, 1) interrupt request is not generated.
5. The second scan of group A is started by the second ELC_AD01 (unit 0) and ELC_AD11 (unit 1) trigger.
6. When the second scan of group A completes, the conversion result is stored in ADDBLDR. An ADC12i_ADI (i = 0, 1) interrupt is generated.



Note 1. ELC_AD00 (unit 0) and ELC_AD10 (unit 1)
Note 2. ELC_AD01 (unit 0) and ELC_AD11 (unit 1)
Note 3. ADC12i_ADI (i = 0, 1)
Note 4. ADC12i_GBADI (i = 0, 1)

Figure 43.17 Example basic operation in group scan mode with double-trigger mode when synchronous triggers from the ELC are used

43.3.4.3 Group Priority Operation

Group priority operation is performed by setting the ADGSPCR.PGS bit to 1 in group-scan mode. The priority of groups is group A > group B.

When setting the PGS bit in the ADGSPCR register to 1, follow the procedure described in Figure 43.18. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

As the basic operation in group-scan mode, a trigger input generated during A/D conversion of group A, B is ignored, and the A/D conversion operation of each group is similar to the operation in single-scan mode.

In group priority operation, if a trigger for a priority group is input during scanning of a lower-priority group, A/D conversion for the lower-priority group is stopped and A/D conversion for the priority group is performed.

If the setting of the ADGSPCR.GBRSCN bit is 0, the lower-priority group enters a wait state when A/D conversion for the priority group completes. A trigger input of the lower-priority group generated during A/D conversion is ignored.

If the setting of the ADGSPCR.GBRSCN bit is 1, A/D conversion for the lower-priority group automatically restarts upon completion of A/D conversion for the priority group. A trigger input of the lower-priority group generated during A/D conversion on the priority group takes effect, and A/D conversion for the lower-priority group is automatically performed upon completion of A/D conversion on the priority group.

If the ADGSPCR.GBRSCN bit is 1 and the ADGSPCR.LGRRS bit is 0, A/D conversion for the lower-priority group is restarted from the first channel. If the setting of the ADGSPCR.LGRRS bit is 1, A/D conversion for the lower-priority group is restarted from the channel for which the conversion stopped. However, if the self-diagnosis function is used, the A/D conversion is restarted from the channel for which the conversion stopped after self-diagnosis completed.

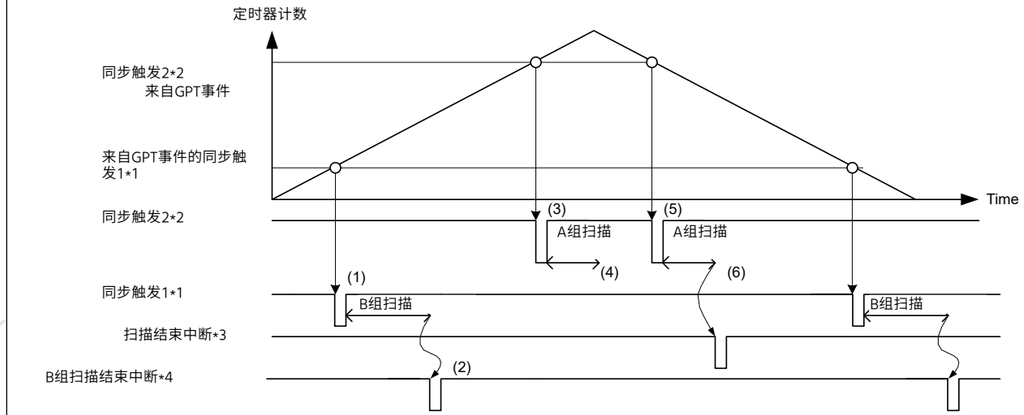
2.B组扫描完成时，如果ADCSR中的GBADIE位为1，则产生ADC12i_GBADI(i=0 1)中断（使能扫描完成时ADC12i_GBADI(i=0 1)中断）。

3.A组的第一次扫描由第一个ELC_AD01（单元0）和ELC_AD11（单元1）触发器启动。

4、A组第一次扫描完成后，转换结果存入相关的AD数据寄存器y（ADDRy）；不会产生ADC12i_ADI(i=0 1)中断请求。

5.A组的第二次扫描由第二个ELC_AD01（单元0）和ELC_AD11（单元1）触发开始。

6.A组第二次扫描完成后，转换结果存入ADDBLDR。产生一个ADC12i_ADI(i=0 1)中断。



注1.ELC_AD00（单元0）和ELC_AD10（单元1）注2.
ELC_AD01（单元0）和ELC_AD11（单元1）
Note 3. ADC12i_ADI (i = 0, 1)
Note 4. ADC12i_GBADI (i = 0, 1)

Figure 43.17 当使用来自ELC的同步触发时，具有双触发模式的组扫描模式下的基本操作示例

43.3.4.3 集团优先运营

在组扫描模式下，通过将ADGSPCR.PGS位设置为1来执行组优先级操作。组的优先级为A组>B组。

将ADGSPCR寄存器中的PGS位设置为1时，请遵循图43.18中描述的过程。如果不遵循该程序，则无法保证AD转换操作和存储数据。

作为组扫描模式下的基本操作，A、B组A/D转换过程中产生的触发输入被忽略，各组的A/D转换操作与单扫描模式下的操作类似。

在组优先操作中，如果在低优先级组的扫描期间输入了优先级组的触发，则停止低优先级组的AD转换并执行优先级组的AD转换。

如果ADGSPCR.GBRSCN位设置为0，则当优先级组的AD转换完成时，低优先级组进入等待状态。AD转换期间产生的低优先级组的触发输入被忽略。

如果ADGSPCR.GBRSCN位设置为1，则在优先级组的AD转换完成后，低优先级组的AD转换自动重新开始。对优先组进行AD转换时产生的低优先组的触发输入生效，在优先组的AD转换完成后，自动进行低优先组的AD转换。

如果ADGSPCR.GBRSCN位为1，ADGSPCR.LGRRS位为0，则从第一个通道重新开始低优先级组的AD转换。如果ADGSPCR.LGRRS位设置为1，则低优先级组的AD转换从转换停止的通道重新开始。但是，如果使用自诊断功能，则从自诊断完成后停止转换的通道重新开始AD转换。

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Table 43.24 summarizes operations in response to the input of a trigger during A/D conversion with the settings of the ADGSPCR.GBRSCN bit.

If the setting of the ADGSPCR.GBRP bit is 1, A/D conversion operation for the lowest-priority group is to continuously perform single scans.

For the trigger settings in group-scan mode, select a synchronous trigger for group A by using the ADSTRGR.TRSA[5:0] bits, a synchronous trigger for group B by using the ADSTRGR.TRSB[5:0] bits. Each trigger must be different from each other. Set the ADSTRGR.TRSB[5:0] bits to 0x3F when setting the ADGSPCR.GBRP bit to 1.

The channels to be scanned must be selected in the registers shown in section 43.3.4. Group Scan Mode.

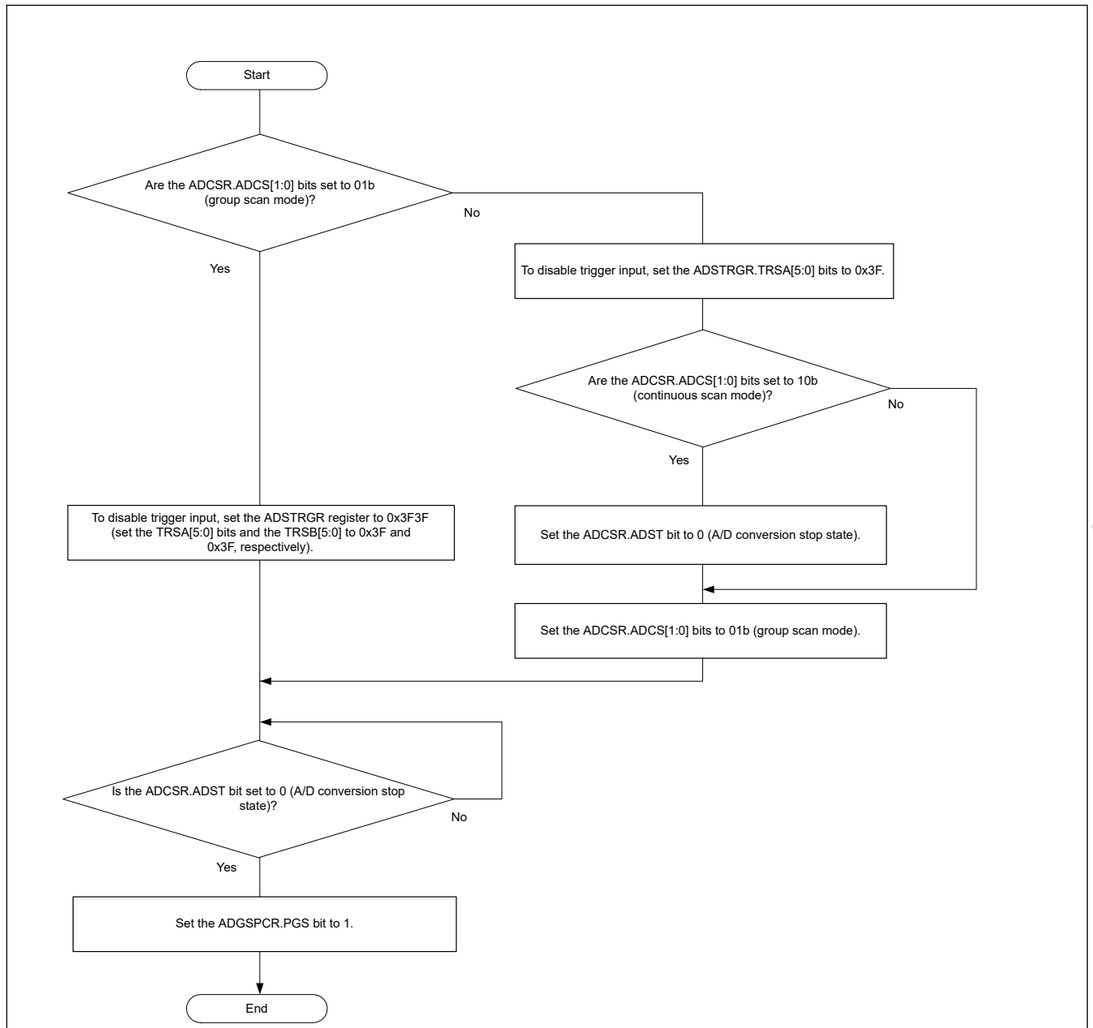

Figure 43.18 Flowchart for ADGSPCR.PGS bit setting

表43.24总结了在AD转换期间响应触发输入的操作，其中设置为ADGSPCR.GBRSCN bit.

如果ADGSPCR.GBRP位设置为1，则最低优先级组的AD转换操作是连续执行单次扫描。

对于组扫描模式下的触发设置，使用ADSTRGR.TRSA[5:0]位选择A组同步触发，使用ADSTRGR.TRSB[5:0]位选择B组同步触发。每个触发器必须彼此不同。将ADGSPCR.GBRP位设置为1时，将ADSTRGR.TRSB[5:0]位设置为0x3F。

要扫描的通道必须在第43.3.4节所示的寄存器中选择。组扫描模式。

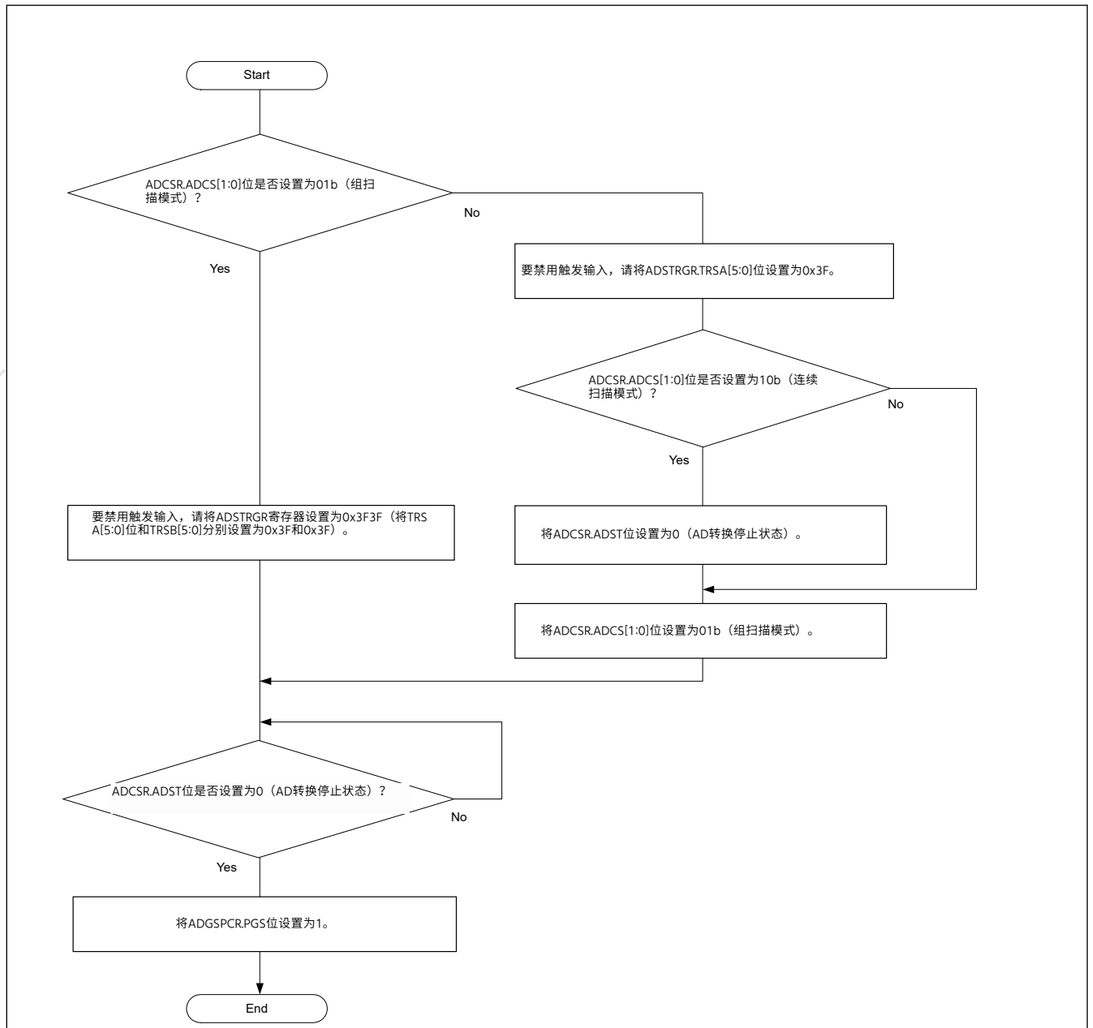

Figure 43.18 ADGSPCR.PGS位设置流程图

Table 43.24 Control of A/D conversion operations according to ADGSPCR.GBRSCN bit setting

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion for group B is performed after A/D conversion for group A completes.
When A/D conversion for group B is in progress	Input of trigger for group A	A/D conversion for group B is discontinued and A/D conversion for group A starts.	• A/D conversion for group B is discontinued and A/D conversion for group A starts. • A/D conversion for group B starts after A/D conversion for group A completes.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.

To use group priority operation mode, select the operation mode to be implemented and set the registers according to the following table.

Table 43.25 Group priority operation setting and operation mode for two groups (ADGSPCR.PGS = 1)

ADGSPCR			Operation category
GBRSCN	LGRRS	GBRP	
0	x	0	Group priority operation for two groups (groups A and B) • When a trigger of group A is input, A/D conversion for group B is terminated (and will not be restarted).
1	0	0	Group priority operation for two groups (groups A and B) • After A/D conversion for group B stopped, when A/D conversion for group A completes, A/D conversion for the group B channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order of smaller channel number.
1	1	0	Group priority operation for two groups (groups A and B) • After A/D conversion for group B stopped, when A/D conversion for group A completes, A/D conversion for the group B channels selected in the ADANSB0/1 register restarts according to the conversion order of smaller channel number, beginning from the channel for which A/D conversion stopped.*1
x	0	1	Group priority operation for two groups (groups A and B) • Single scanning for group B is continuously performed without a start trigger input. After A/D conversion for group B stopped, when A/D conversion for group A completes, single scanning for the channels selected in the ADANSB0/1 register restarts according to the conversion order of smaller channel number.
1	1	1	Group priority operation for two groups (groups A and B) • Single scanning for group B is continuously performed without a start trigger input. After A/D conversion for group B stopped, when A/D conversion for group A completes, single scanning for the channels selected in the ADANSB0/1 register restarts according to the conversion order of smaller channel number, beginning from the channel for which A/D conversion stopped.*1

Note: x: Don't care.
Note 1. When the self-diagnosis function is enabled (ADCER.DIAGM = 1), A/D conversion for the channel that has been stopped is started after self-diagnosis is performed.

(1) Group priority operation for two groups (when ADGSPCR.PGS = 1)

Operation examples 1-1 to 1-5 show group priority operations in group-scan mode (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

Operation example 1-1: "Group A trigger input during group B scan" when rescanning is enabled

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).

Table 43.24 根据ADGSPCR.GBRSCN位设置控制AD转换操作

AD转换操作	触发输入	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
正在进行A组的AD转换时	A组触发器输入	触发输入无效。	触发输入无效。
	B组触发器输入	触发输入无效。	在A组的AD转换完成后，执行B组的AD转换。
正在进行B组的AD转换时	A组触发器输入	B组的AD转换停止，A组的AD转换开始。	• B组的AD转换停止，A组的AD转换开始。 • B组的AD转换在A组的AD转换完成后开始。
	B组触发器输入	触发输入无效。	触发输入无效。

要使用组优先操作模式，请根据下表选择要执行的操作模式并设置寄存器。

Table 43.25 两组的组优先操作设置和操作模式（ADGSPCR.PGS=1）

ADGSPCR			操作类别
GBRSCN	LGRRS	GBRP	
0	x	0	两组（A组和B组）的组优先操作● 当输入A组的触发时，B组的AD转换将终止（并且不会重新启动）。
1	0	0	两组（A组和B组）的组优先操作● B组AD转换停止后，当A组AD转换完成时，ADANSB0和ADANSB1寄存器中选择的B组通道的AD转换按照通道号较小的转换顺序重新开始。
1	1	0	两组（A组和B组）的组优先操作● B组AD转换停止后，当A组AD转换完成时，ADANSB01寄存器中选择的B组通道的AD转换按照通道号较小的转换顺序重新开始，从AD转换停止的通道开始。*1
x	0	1	两组（A组和B组）的组优先操作● B组的单次扫描在没有启动触发输入的情况下连续执行。B组AD转换停止后，当A组AD转换完成时，按照通道号较小的转换顺序重新开始对ADANSB01寄存器中选择的通道进行单次扫描。
1	1	1	两组（A组和B组）的组优先操作● B组的单次扫描在没有启动触发输入的情况下连续执行。B组AD转换停止后，当A组AD转换完成时，对ADANSB01寄存器中选择的通道的单次扫描按照通道号较小的转换顺序重新开始，从AD转换停止的通道开始。*1

Note: x: Don't care.
注1.自诊断功能有效时（ADCER.DIAGM=1），自诊断完成后，已停止通道的AD转换开始。

(1) 两个组的组优先操作（当ADGSPCR.PGS=1时）

操作示例1-1到1-5显示了当为组A和通道1选择通道0时，组扫描模式下的组优先操作（当ADGSPCR.GBRSCN=1、ADGSPCR.GBRP=0和ADGSPCR.LGRRS=0时）为B组选择3至3个。

操作示例1-1：启用重新扫描时的"B组扫描期间A组触发输入"

1.当B组的触发输入将ADCSR.ADST位设置为1（开始AD转换）时，ADANSB0和ADANSB1寄存器中选择的模拟输入通道的AD转换按照转换顺序从最小通道开始号码n.

2.B组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

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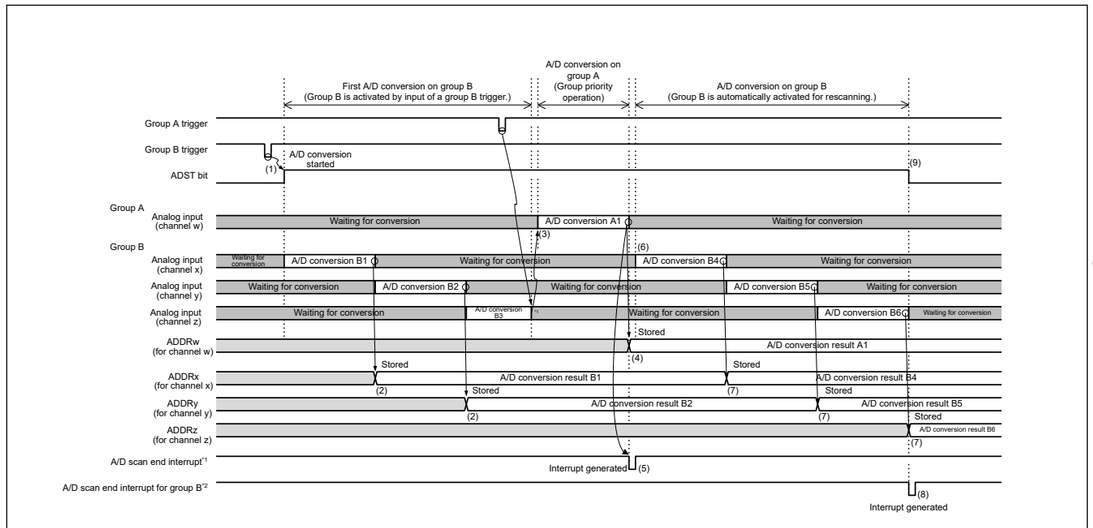
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1. Then A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion on the channels, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. An ADC120_ADI interrupt request is generated.
6. If the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning of the group that was stopped in group priority operation), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1.
7. On completion of A/D conversion on the channels, the result is stored in the corresponding A/D Data Register y (ADDRy).
8. If the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan), a group B scan end interrupt request is generated.
9. When A/D conversion for all the channels completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state.



Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1 .
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.19 Example of group priority operation 1-1: Group A trigger input during group B scanning when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-2: “Group A trigger input during rescanning of group B” when rescanning is enabled

Figure 43.20 shows the operation when a group A trigger is input during rescanning operation for group B.

Even during rescanning operation, when a trigger for group A is input, A/D conversion on group B stops and A/D conversion for group A starts. A/D conversion for group B starts after A/D conversion for group A completes.

Operations for setting the ADCSR.ADST bit, storing the A/D conversion result in the corresponding A/D Data Register y (ADDRy), and generating interrupt requests are the same as those in operation example 1-1.

3.在B组的AD转换期间输入A组的触发信号时，B组的AD转换停止，而ADCSR.ADST位保持为1。然后在ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的AD转换开始根据编号n最小的通道的转换顺序。如果AD转换在完成之前停止，则转换结果不会存储在AD数据寄存器y(ADDRy)中。

4.在通道上完成AD转换后，结果将存储在相应的AD数据寄存器y(ADDRy)中。

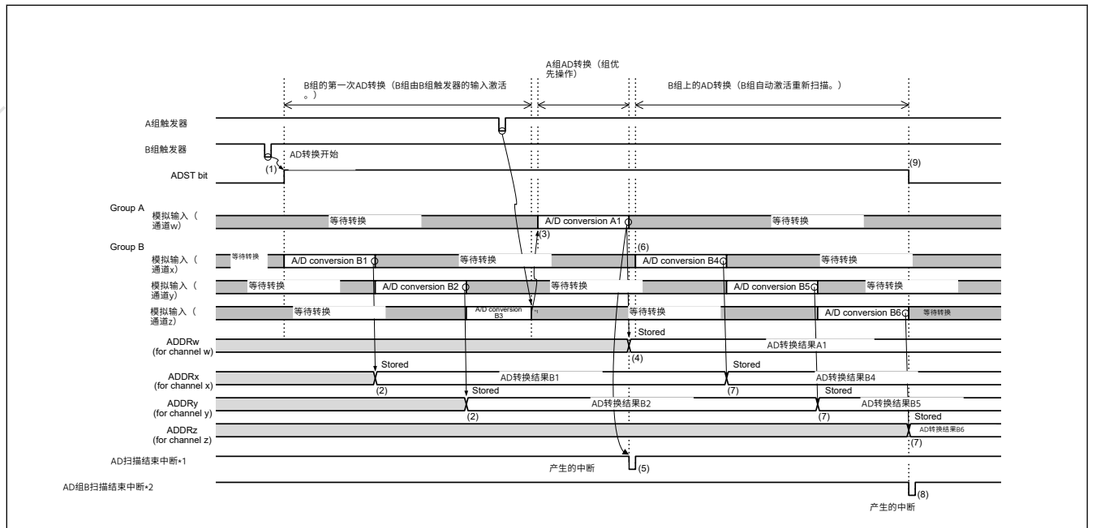
5.产生一个ADC120_ADI中断请求。

6.如果ADGSPCR.GBRSCN位设置为1（允许重新扫描在组优先操作中停止的组），则ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的AD转换根据转换顺序重新启动当ADCSR.ADST保持为1时，来自编号为n的最小通道。

7.在通道上完成AD转换后，结果将存储在相应的AD数据寄存器y(ADDRy)中。

8.如果ADCSR.GBADIE位设置为1（使能在B组扫描完成时产生中断），则产生B组扫描结束中断请求。

9.当所有通道的AD转换完成时，ADCSR.ADST位自动清零，AD转换器进入等待状态。



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.19 组优先操作1−1示例：启用重新扫描时，在B组扫描期间A组触发输入（当ADGSPCR.GBRSCN=1、ADGSPCR.GBRP=0和ADGSPCR.LGRRS=0时）

操作示例1−2：启用重新扫描时的“B组重新扫描期间A组触发输入”

图43.20显示了在B组重新扫描操作期间输入A组触发时的操作。

即使在重新扫描操作期间，当输入A组触发时，B组的AD转换停止，A组的AD转换开始。B组的AD转换在A组的AD转换完成后开始。

设置ADCSR.ADST位、将AD转换结果存储到相应的AD数据寄存器y(ADDRy)以及产生中断请求的操作与操作示例1−1中的操作相同。

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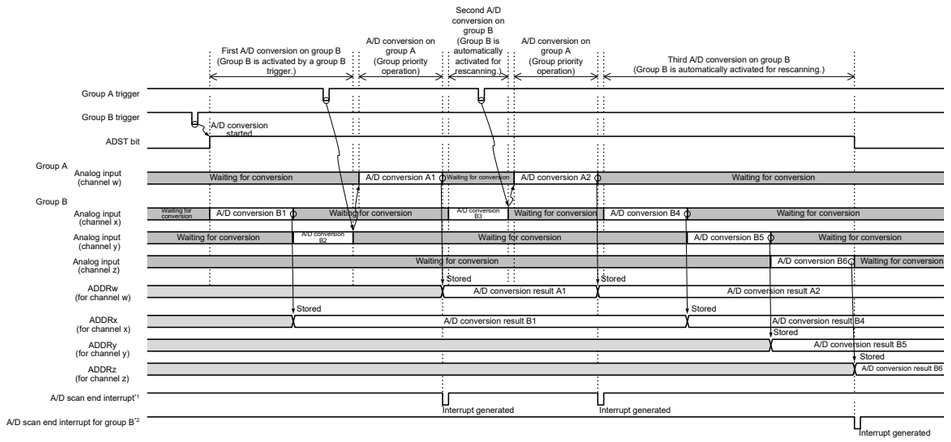


Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

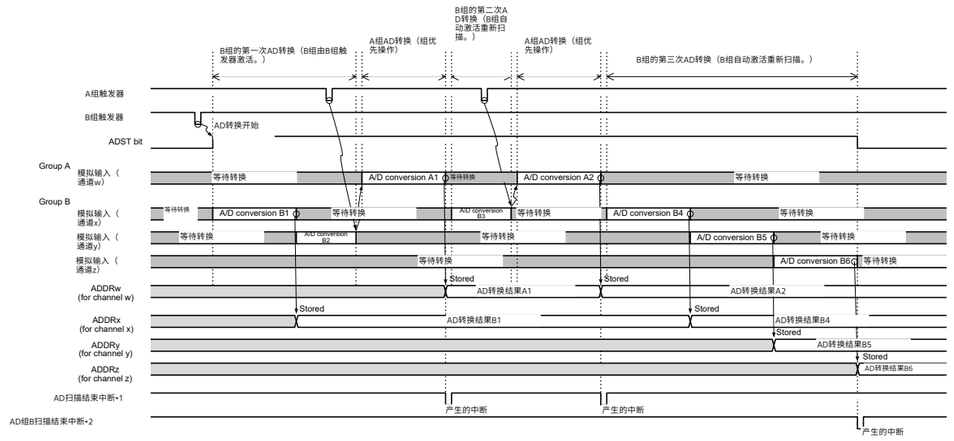
Figure 43.20 Example of group priority operation 1-2: Group A trigger input during rescanning of group B when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-3: “Group B trigger input during group A scan” when rescanning is enabled

The following describes the operation when the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning of the group that was stopped in group priority operation) and a trigger for group B is input during scanning operation for group A.

If the setting of the ADGSPCR.GBRSCN bit is 0, any trigger for group B that is input during scanning operation for group A is invalid.

1. When input of a trigger for group A sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n.
2. When a trigger for group B is input during A/D conversion for group A, group B is ready for A/D conversion.
3. On completion of A/D conversion for each channel in group A, the result is stored in the corresponding A/D Data Register y (ADDRy).
4. An ADC120_ADI interrupt request is generated.
5. When A/D conversion for group A completes, while the ADCSR.ADST bit remains 1, A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
   (As with the case of operation example 1-1, if a trigger for group A is input during A/D conversion for group B, A/D conversion for group A starts. Then A/D conversion for group B starts upon completion of A/D conversion for group A.)
6. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
7. Upon completion of A/D conversion for group B, a group B scan end interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan).
8. When A/D conversion for all the channels completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state.



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.20 组优先操作1−2示例：启用重新扫描时（当ADGSPCR.GBRSCN=1、ADGSPCR.GBRP=0和ADGSPCR.LGRRS=0时）在B组重新扫描期间A组触发输入

操作示例1−3：启用重新扫描时的“A组扫描期间B组触发输入”

下面介绍当ADGSPCR.GBRSCN位设置为1（允许重新扫描在组优先操作中停止的组）并且在A组扫描操作期间输入B组触发器时的操作。

如果ADGSPCR.GBRSCN位设置为0，则在组扫描操作期间输入的任何组B触发A无效。

1.当A组的触发输入将ADCSR.ADST位设置为1（开始AD转换）时，ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的AD转换根据通道的转换顺序开始最小的数n。

2.在A组AD转换期间输入B组触发器时，B组准备好进行AD转换。

3.A组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

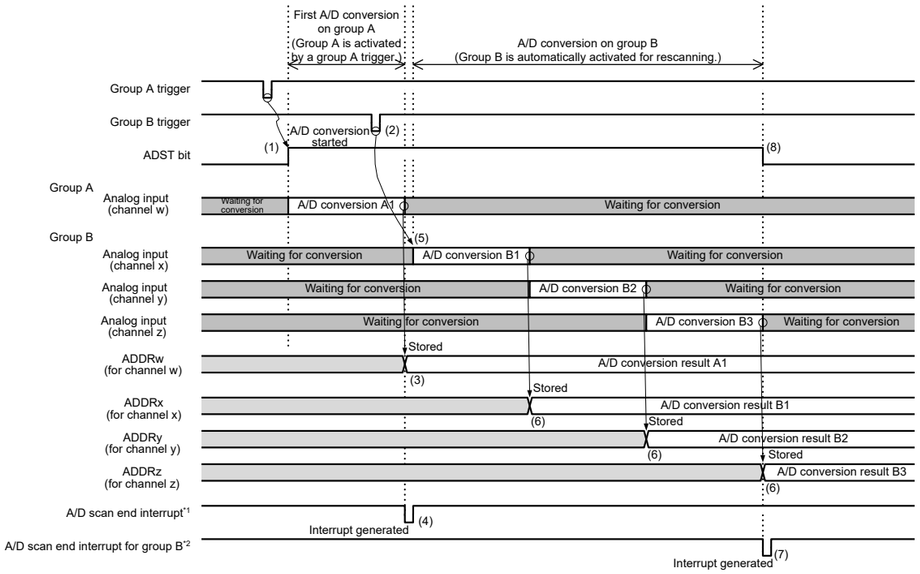
4.产生一个ADC120_ADI中断请求。

5.当A组的AD转换完成，而ADCSR.ADST位保持为1时，ADANSB0和ADANSB1寄存器中选择的B组模拟输入通道的AD转换按照编号n最小通道的转换顺序开始。（与操作示例1−1的情况一样，如果在B组的AD转换期间输入了A组的触发信号，则A组的AD转换开始。然后，在A组的AD转换完成后，开始B组的AD转换。）

6.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

7.B组的AD转换完成后，如果ADCSR.GBADIE位设置为1，则产生B组扫描结束中断请求（在B组扫描完成时允许产生中断）。

8.当所有通道的AD转换完成时，ADCSR.ADST位自动清零，AD转换器进入等待状态。



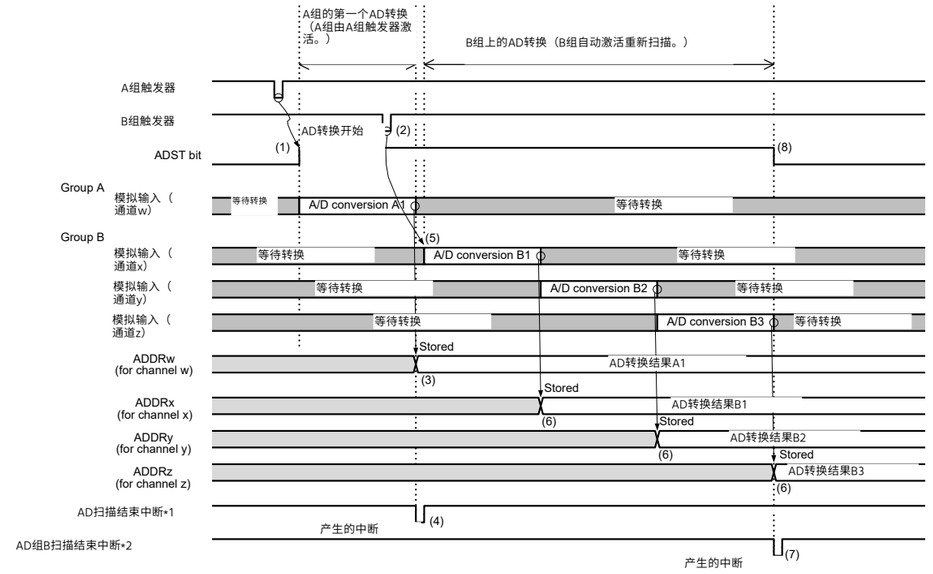
Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.21 Example of group priority operation 1-3: Group B trigger input during group A scan when rescanning is enabled (when ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-4 shows the group priority operation in group-scan mode (when ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

Operation example 1-4: “Group A trigger input during group B scan” when rescanning is disabled

1. When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1, and then A/D conversion for the group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order from the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. On completion of A/D conversion for group A, an ADC120_ADI interrupt request is generated.
6. When A/D conversion for group A completes, the ADCSR.ADST bit is automatically cleared and the A/D converter enters a wait state. A/D conversion for group B is not performed until a trigger for group B is input the next time.



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.21 组优先操作1−3示例：启用重新扫描时A组扫描期间的B组触发输入（当ADGSPCR.GBRSCN=1、ADGSPCR.GBRP=0和ADGSPCR.LGRRS=0时）

操作示例1−4显示了组扫描模式下的组优先级操作（当ADGSPCR.GBRSCN=0时，ADGSPCR.GBRP=0和ADGSPCR.LGRRS=0)当为A组选择通道0并且为B组选择通道1至3时。

操作示例1−4：禁用重新扫描时的“B组扫描期间A组触发输入”

1.当B组的触发输入将ADCSR.ADST位设置为1（开始AD转换）时，ADANSB0和ADANSB1寄存器中选择的模拟输入通道的AD转换按照转换顺序从最小通道开始号码n.

2.B组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

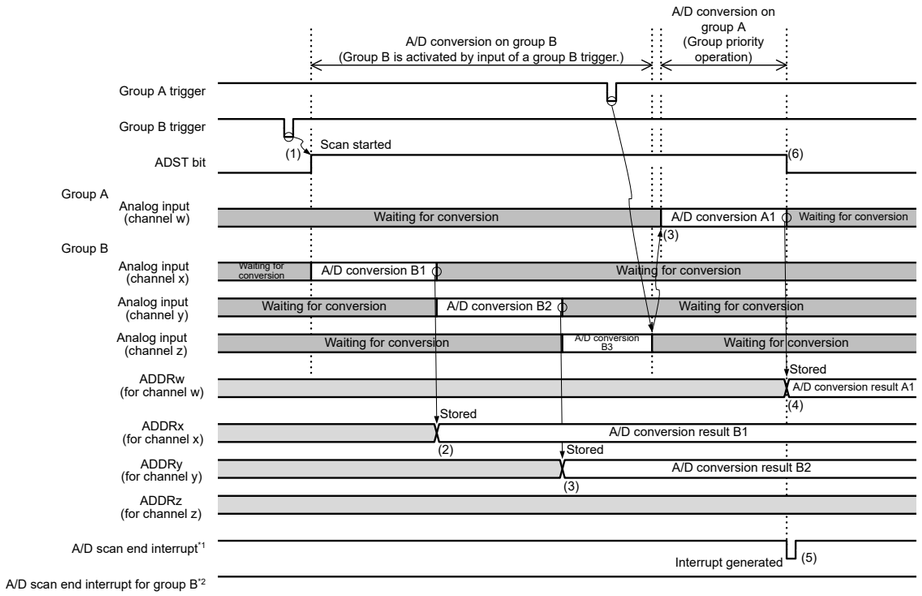
3.在B组AD转换期间输入A组触发时，在ADCSR.ADST位保持1时停止B组AD转换，然后在

ADANSA0和ADANSA1寄存器按照转换顺序从编号n最小的通道开始。如果AD转换在完成之前停止，则转换结果不会存储在AD数据寄存器y(ADDRy)中。

4.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

5.A组AD转换完成后，会产生ADC120_ADI中断请求。

6.当A组的AD转换完成时，ADCSR.ADST位自动清零，AD转换器进入等待状态。直到下次输入B组的触发后，才会执行B组的AD转换。



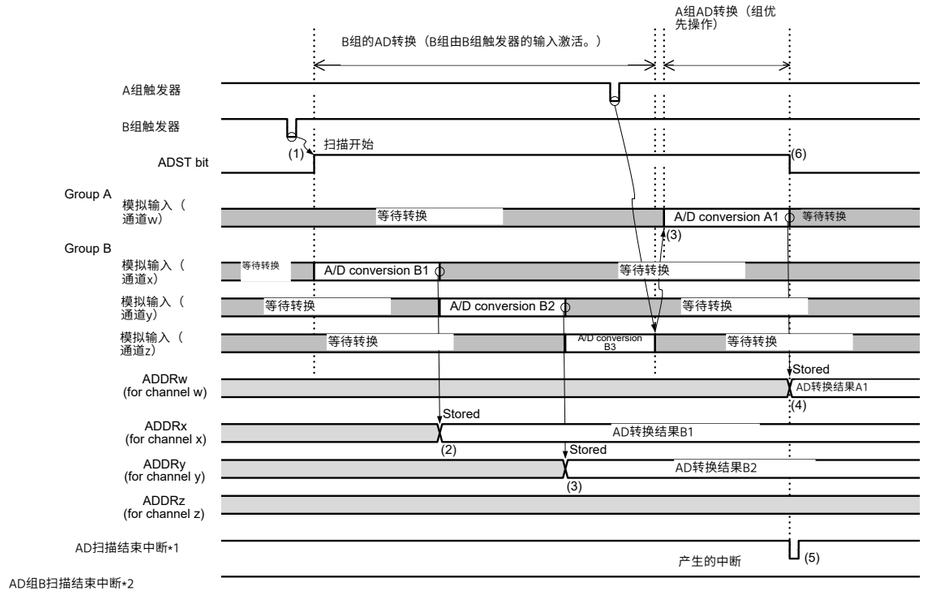
Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.22 Group priority operation example 1-4: “Group A trigger is input during group B scan” when rescanning is disabled (when ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0, and ADGSPCR.LGRRS = 0)

Operation example 1-5 shows the group priority operation in group-scan mode (when ADGSPCR.GBRP = 1, and ADGSPCR.LGRRS = 0) when channel 0 is selected for group A and channels 1 and 2 are selected for group B.

Operation example 1-5: Continuously activating single-scan operation for group B

1. When ADGSPCR.GBRP = 1 is set, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and A/D conversion for the analog input channels selected in the ADANSB0 and ADANSB1 registers starts according to the conversion order from the channel with the smallest number n.
2. On completion of A/D conversion for each channel in group B, the result is stored in the corresponding A/D Data Register y (ADDRy).
3. When a trigger for group A is input during A/D conversion for group B, A/D conversion for group B stops while the ADCSR.ADST bit remains 1, and then A/D conversion for group A analog input channels selected in the ADANSA0 and ADANSA1 registers starts according to the conversion order zfrom the channel with the smallest number n. If A/D conversion stops before it is completed, the conversion result is not stored in the A/D Data Register y (ADDRy).
4. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).
5. On completion of A/D conversion for group A, an ADC120_ADI interrupt request is generated.
6. If ADGSPCR.GBRP = 1 is set (performing single scan continuously), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1 (starting A/D conversion).
7. On completion of A/D conversion of a single channel, the result is stored in the corresponding A/D Data Register y (ADDRy).



Note: w、x、y和z(w<x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.22 组优先操作示例1−4：“在B组扫描期间输入A组触发”当禁用重新扫描时（当ADGSPCR.GBRSCN=0、ADGSPCR.GBRP=0和ADGSPCR.LGRRS=0时）

操作示例1−5显示了组扫描模式下的组优先级操作（当ADGSPCR.GBRP=1，并且ADGSPCR.LGRRS=0)当为A组选择通道0并且为B组选择通道1和2时。

操作示例1−5：B组连续激活单扫描操作

1.当设置ADGSPCR.GBRP=1时，ADCSR.ADST位设置为1（开始AD转换），并且ADANSB0和ADANSB1寄存器中选择的模拟输入通道的AD转换根据通道的转换顺序开始最小的数n。

2.B组中每个通道的AD转换完成后，将结果存储在相应的AD数据寄存器y(ADDRy)中。

3.在B组的AD转换期间输入A组的触发信号时，B组的AD转换停止，而ADCSR.ADST位保持为1，然后在ADANSA0和ADANSA1寄存器中选择的A组模拟输入通道的AD转换开始根据编号为n的通道的转换顺序z。如果AD转换在完成之前停止，则转换结果不会存储在AD数据寄存器y(ADDRy)中。

4.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

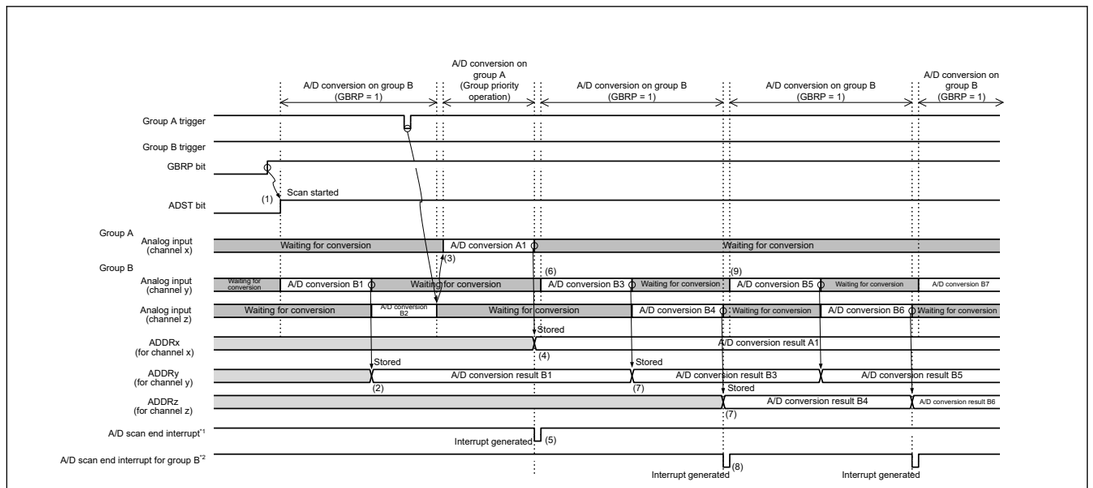
5.A组AD转换完成后，会产生ADC120_ADI中断请求。

6.如果设置ADGSPCR.GBRP=1（连续执行单次扫描），B组模拟输入的AD转换
在ADANSB0和ADANSB1寄存器中选择的通道根据转换顺序从具有最小编号n的通道重新启动，而ADCSR.ADST保持为1（开始AD转换）。

7.单通道AD转换完成后，结果存入对应的AD数据寄存器y(ADDRy)。

8. If the setting of the ADCSR.GBADIE bit is 1 (enabling interrupt generation on completion of group B scan), a group B scan end interrupt request is generated.
9. If ADGSPCR.GBRP = 1 is set (performing single scan continuously), A/D conversion for the group B analog input channels selected in the ADANSB0 and ADANSB1 registers restarts according to the conversion order from the channel with the smallest number n while the ADCSR.ADST remains 1 (starting A/D conversion).

Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1. Do not clear the ADCSR.ADST bit as long as the ADGSPCR.GBRP bit is 1. To forcibly stop A/D conversion while ADGSPCR.GBRP = 1, follow the procedure shown in Figure 43.38.



Note: x, y, and z (x < y < z) are the selected channel numbers by ADANSA0/1 or ADANSB0/1.
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.23 Group priority operation example 1-5: Continuously activating single scan for group B (when ADGSPCR.GBRP = 1 , ADGSPCR.LGRRS = 0)

Note: To continuously activate single-scan operation for group B, disable group B trigger input.

43.3.5 Interleaved operation

Interleaved operation is that two ADC units convert same one pin alternately in order to obtain the data faster. This function can be used with the channel AN000/AN100, AN001/AN101 or AN002/AN102 and can be used in single scan mode and continuous scan mode. Regarding trigger, synchronous trigger and external trigger are suitable to use. It is recommended to use synchronous trigger with AGT or GPT events in order to ensure AD conversion timing.

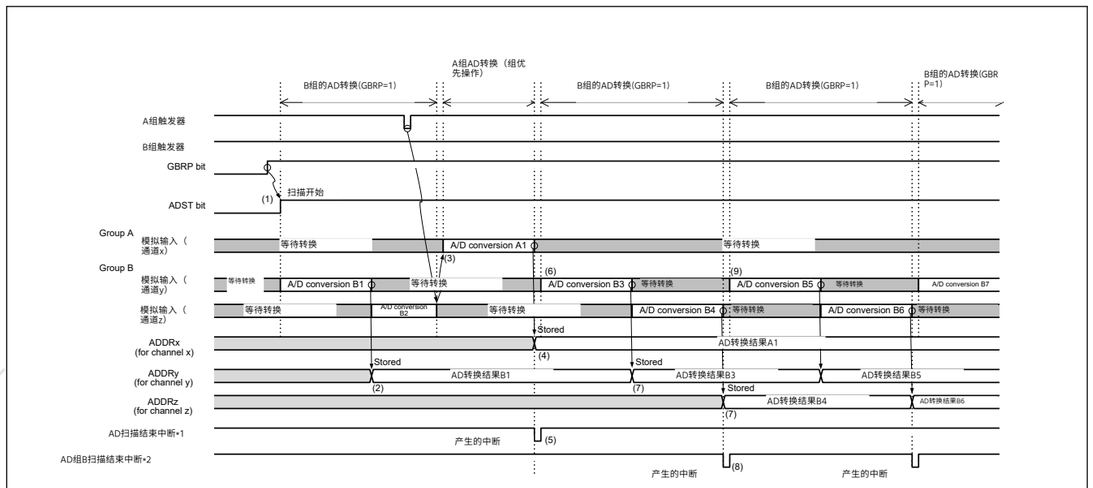
43.3.5.1 Trigger input timing

Trigger input timing for each ADC units should be controlled not to overlap each sampling period as shown in Figure 43.24 and Table 43.26. For timing parameter (t_{SPL}, t_{SAM} and t_{SCAN}), refer to Table 43.27.

8.如果ADCSR.GBADIE位设置为1（使能在B组扫描完成时产生中断），则产生B组扫描结束中断请求。

9.如果设置ADGSPCR.GBRP=1（连续执行单次扫描），B组模拟输入的AD转换
在ADANSB0和ADANSB1寄存器中选择的通道根据转换顺序从具有最小编号n的通道重新启动，而ADCSR.ADST保持为1（开始AD转换）。

只要ADGSPCR.GBRP位保持为1，就重复步骤6到9。不要清除ADCSR.ADST位，只要ADGSPCR.GBRP位为1。要在ADGSPCR.GBRP=1时强制停止AD转换，请按照以下步骤进行操作
Figure 43.38.



Note: x、y和z(x<y<z)是ADANSA01或ADANSB01选择的通道号。
Note 1. ADC12i_ADI (i = 0, 1)
Note 2. ADC12i_GBADI (i = 0, 1)

Figure 43.23 组优先操作示例1−5：B组连续激活单次扫描（当ADGSPCR.GBRP = 1 , ADGSPCR.LGRRS = 0)

Note: 要连续激活B组的单次扫描操作，请禁用B组触发输入。

43.3.5 Interleaved operation

交错操作是两个ADC单元交替转换相同的一个引脚以更快地获取数据。此功能可与通道AN000AN100、AN001AN101或AN002AN102一起使用，可用于单次扫描模式和连续扫描模式。关于触发，适合使用同步触发和外触发。建议使用与AGT或GPT事件同步触发，以确保AD转换时序。

43.3.5.1 触发输入时序

每个ADC单元的触发输入时序应控制为不与每个采样周期重叠，如图43.24和表43.26所示。关于时序参数（tSPL、tSAM和tSCAN），请参见表43.27。

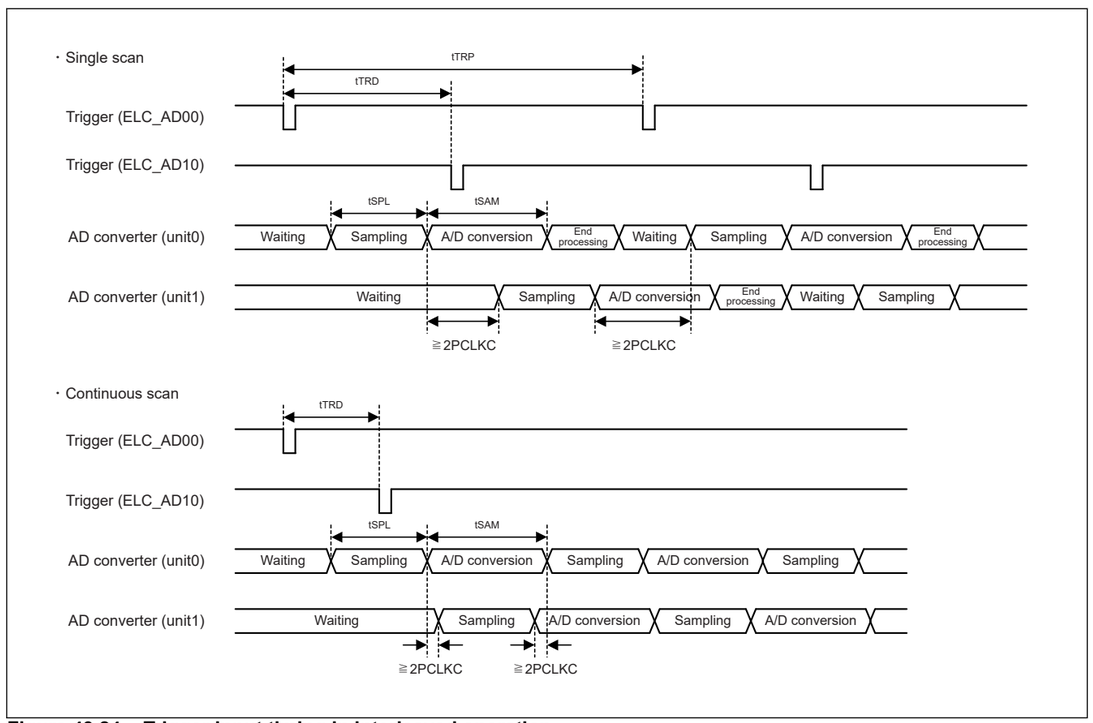


Figure 43.24 Trigger input timing in interleaved operation

Table 43.26 Setting for trigger input timing in interleaved operation

Parameter		Symbol	Min	Max
Trigger issuance delay period	Single scan	t_{TRD}	t_{SPL} + 2PCLKC	t_{TRP} - t_{SPL} - 2PCLKC
	Continuous scan	t_{TRD}	t_{SPL} + 2PCLKC	t_{SAM} - 2PCLKC
Trigger issuance period		t_{TRP}	tSCAN	—

43.3.5.2 Continuous scan mode

In this operation, assuming two ADC units are set to the same sampling period and conversion period.

The operation is as follows:

1. When the ADCSR.ADST bit of ADC0 is set to 1 by a synchronous trigger input (ELC) or asynchronous trigger input, A/D conversion is performed for the selected channel.
2. After certain period is elapsed after ADC0 starts (refer to section 43.3.5.1. Trigger input timing), when ADCSR.ADST bit of ADC1 is set to 1 by a synchronous trigger input (ELC) or asynchronous trigger input for the channel which is same analog input pin with ADC0.
3. A/D conversion of ADC0 completes prior to completion of ADC1. Then ADC120_ADI interrupt request is generated. ADC0 sequentially starts A/D conversion. A/D conversion is continued as long as ADCSR.ADST remains 1.
4. A/D conversion of ADC1 completes after completion of ADC0. Then ADC121_ADI interrupt request is generated. A/D conversion of ADC1 is continued as well as ADC0.

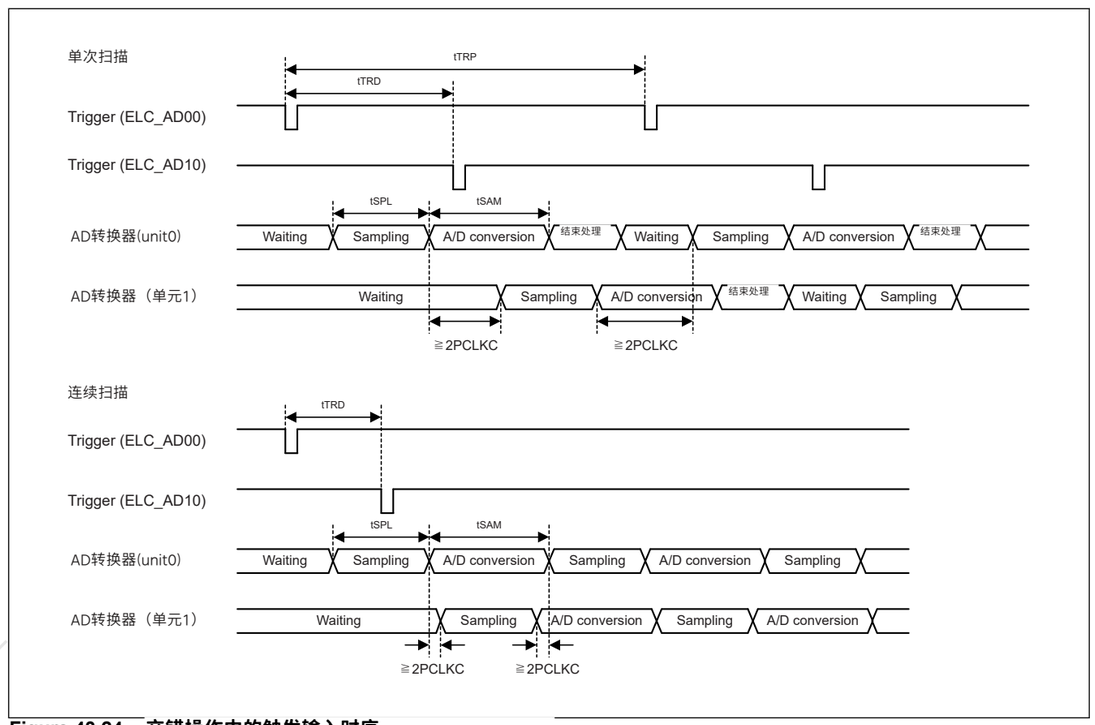


Figure 43.24 交错操作中的触发输入时序

Table 43.26 交错操作中触发输入时序的设置

Parameter		Symbol	Min	Max
触发发行延迟期	单次扫描	t_{TRD}	t_{SPL} + 2PCLKC	t_{TRP} - t_{SPL} - 2PCLKC
	连续扫描	t_{TRD}	t_{SPL} + 2PCLKC	t_{SAM} - 2PCLKC
触发发行期		t_{TRP}	tSCAN	—

43.3.5.2 连续扫描模式

在此操作中，假设两个ADC单元设置为相同的采样周期和转换周期。

操作如下：

1.当同步触发输入(ELC)或异步触发输入将ADC0的ADCSR.ADST位设置为1时，对所选通道执行AD转换。

2.ADC0启动后经过一定时间后（请参阅第43.3.5.1节。触发输入时序），当ADC1的ADCSR.ADST位通过同步触发输入(ELC)或异步触发输入设置为1的通道时，是与ADC0相同的模拟输入引脚。

3.ADC0的AD转换在ADC1完成之前完成。然后产生ADC120_ADI中断请求。ADC0依次启动AD转换。只要ADCSR.ADST保持1，D转换就会继续。

4.ADC0完成后，ADC1的AD转换完成。然后产生ADC121_ADI中断请求。ADC1的D转换与ADC0一样继续进行。

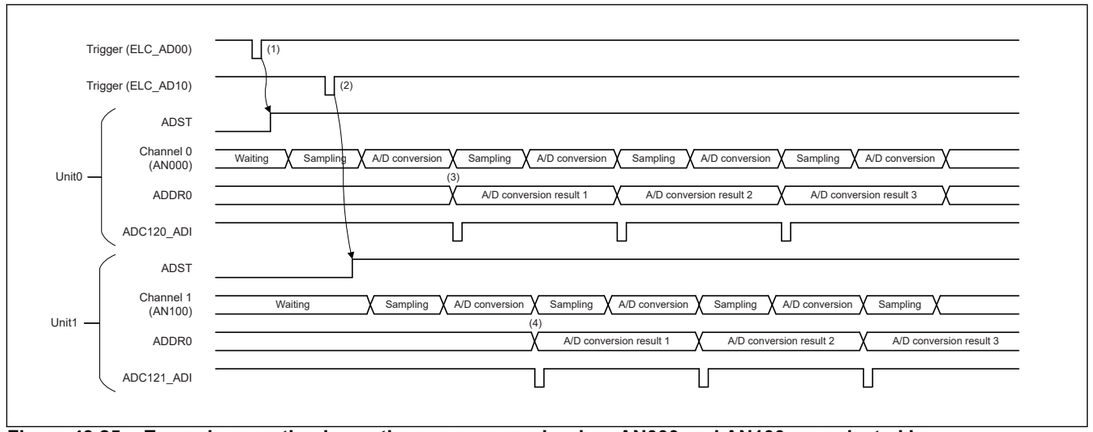


Figure 43.25 Example operation in continuous scan mode when AN000 and AN100 are selected in interleaved operation

43.3.5.3 Single scan mode

In this operation, assuming two ADC units are set to the same sampling period and conversion period.

The operation is as follows:

1. When the ADCSR.ADST bit of ADC0 is set to 1 by a synchronous trigger input (ELC) or asynchronous trigger input, A/D conversion is performed for the selected channel.
2. After certain period is elapsed after ADC0 starts (refer to section 43.3.5.1. Trigger input timing), when ADCSR.ADST bit of ADC1 is set to 1 by a synchronous trigger input (ELC) or asynchronous trigger input for the channel which is same analog input pin with ADC0.
3. A/D conversion of ADC0 completes prior to completion of ADC1. Then ADC120_ADI interrupt request is generated.
4. When A/D conversion of ADC0 completes, ADCSR.ADST bit is automatically cleared to 0. Then ADC120 enters a wait state.
5. Restart A/D conversion of ADC0. Let the sampling starts during conversion period of ADC1.
6. A/D conversion of ADC1 completes after the restart of ADC0. Then ADC121_ADI interrupt request is generated.
7. When A/D conversion of ADC1 completes, ADCSR.ADST bit is automatically cleared to 0. Then ADC121 enters a wait state.
8. Restart A/D conversion of ADC1. Let the sampling starts during conversion period of ADC0.

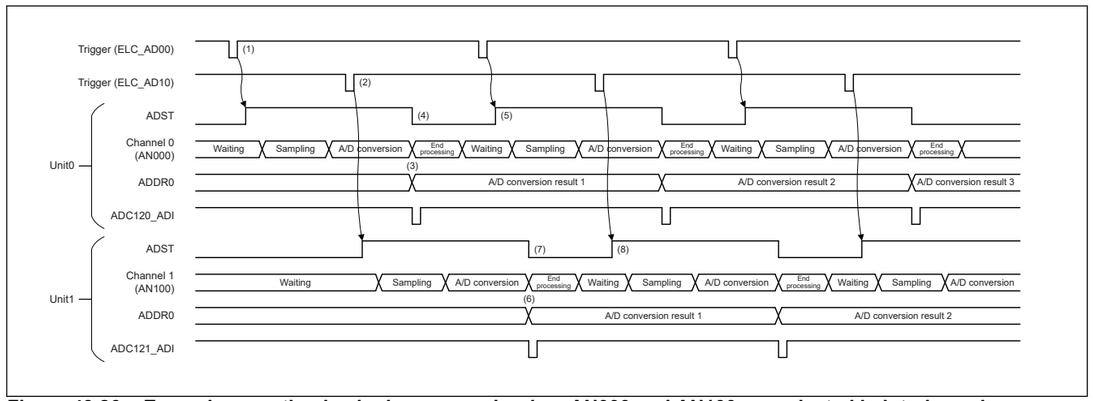


Figure 43.26 Example operation in single scan mode when AN000 and AN100 are selected in interleaved operation

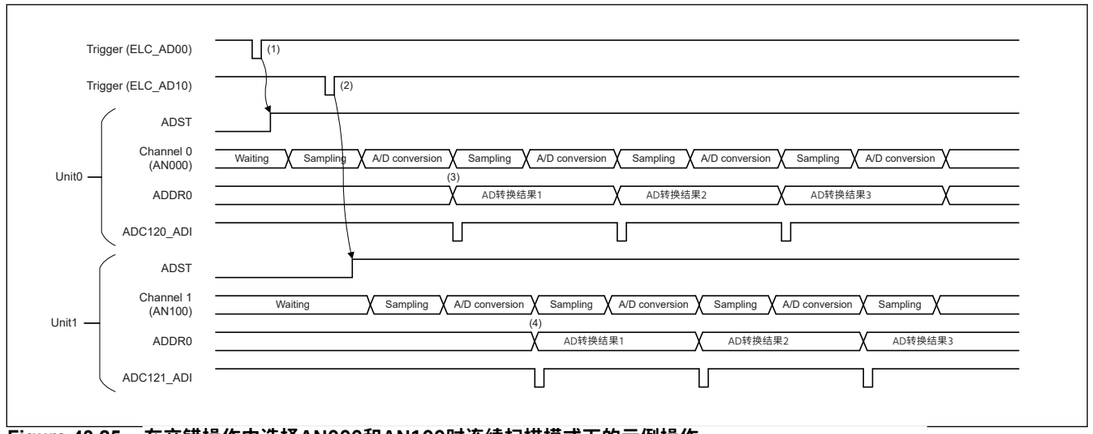


Figure 43.25 在交错操作中选择AN000和AN100时连续扫描模式下的示例操作

43.3.5.3 单次扫描模式

在此操作中，假设两个ADC单元设置为相同的采样周期和转换周期。

操作如下：

1.当同步触发输入(ELC)或异步触发输入将ADC0的ADCSR.ADST位设置为1时，对所选通道执行AD转换。

2.ADC0启动后经过一定时间后（请参阅第43.3.5.1节。触发输入时序），当ADC1的ADCSR.ADST位通过同步触发输入(ELC)或异步触发输入设置为1的通道时，是与ADC0相同的模拟输入引脚。

3.ADC0的AD转换在ADC1完成之前完成。然后产生ADC120_ADI中断请求。

4.ADC0的AD转换完成后，ADCSR.ADST位自动清0。ADC120进入等待状态。

5.重启ADC0的AD转换。让采样在ADC1的转换期间开始。

6.ADC0重启后ADC1的AD转换完成。然后产生ADC121_ADI中断请求。

7.ADC1AD转换完成后，ADCSR.ADST位自动清0。ADC121进入等待状态。

8.重新启动ADC1的AD转换。让采样在ADC0的转换期间开始。

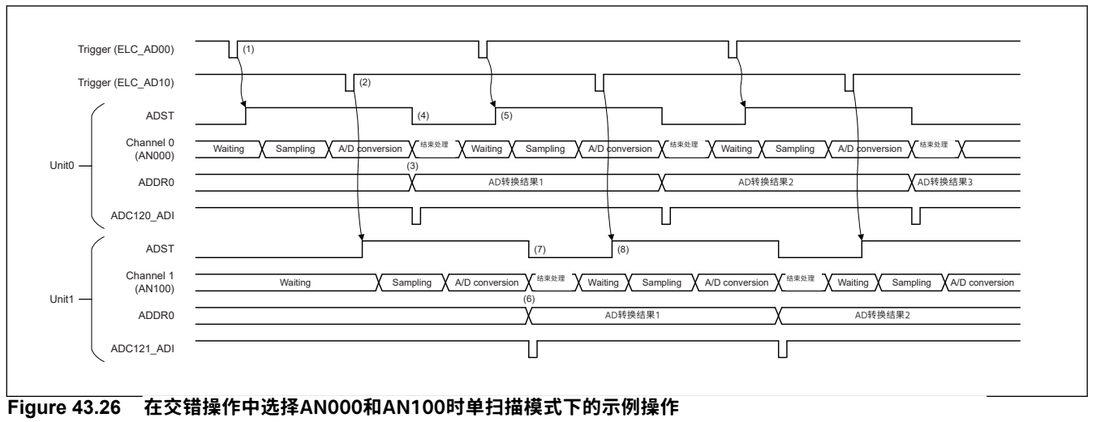


Figure 43.26 在交错操作中选择AN000和AN100时单扫描模式下的示例操作

43.3.5.4 Single scan mode with extended double-trigger mode

In this operation, assuming two ADC units are set to the same sampling period and conversion period.

For details of operation in extended double-trigger mode, please refer to section 43.3.2.5. Extended operations when double-trigger mode is selected.

This operation can decimate period of interrupt generation and the conversion data can be read in consecutive address with ADDBLDRA and ADDBLDRB register.

The operation is as follows:

1. When the ADCSR.ADST bit of ADC0 is set to 1 by a synchronous trigger input (ELC_AD00), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. After certain period is elapsed after ADC0 starts (refer to section 43.3.5.1. Trigger input timing), when ADCSR.ADST bit of ADC1 is set to 1 by a synchronous trigger input (ELC_AD10) for the channel which is same analog input pin with ADC0.
3. A/D conversion of ADC0 completes prior to completion of ADC1. The A/D conversion result is stored in the ADC0's associated A/D Data Register y (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA).
4. The ADCSR.ADST bit is automatically cleared to 0 and the ADC120 enters a wait state. An ADC120_ADI interrupt request is not generated.
5. Restart A/D conversion of ADC0 by a synchronous trigger input (ELC_AD01). Let the sampling starts during conversion period of ADC1.
6. A/D conversion of ADC1 completes. The A/D conversion result is stored in the ADC1's associated A/D Data Register y (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA).
7. The ADCSR.ADST bit is automatically cleared to 0 and the ADC121 enters a wait state. An ADC121_ADI interrupt request is not generated.
8. Restart A/D conversion of ADC1 by a synchronous trigger input (ELC_AD11). Let the sampling starts during conversion period of ADC0.
9. A/D conversion of ADC0 completes. The A/D conversion result is stored in the ADC0's A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register B (ADDBLDRB).
10. The ADCSR.ADST bit is automatically cleared to 0 and the ADC120 enters a wait state. An ADC120_ADI interrupt request is generated.
11. Restart A/D conversion of ADC0 by a synchronous trigger input (ELC_AD00). Let the sampling starts during conversion period of ADC1.
12. A/D conversion of ADC1 completes. The A/D conversion result is stored in the ADC1's A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register B (ADDBLDRB).
13. The ADCSR.ADST bit is automatically cleared to 0 and the ADC121 enters a wait state. An ADC121_ADI interrupt request is generated.
14. Restart A/D conversion of ADC1 by a synchronous trigger input (ELC_AD10). Let the sampling starts during conversion period of ADC0.

43.3.5.4 具有扩展双触发模式的单扫描模式

在此操作中，假设两个ADC单元设置为相同的采样周期和转换周期。

扩展双触发模式下的操作细节请参考43.3.2.5节。选择双触发模式时的扩展操作。

此操作可以抽取中断产生的周期，并且可以在连续地址中读取转换数据ADDBLDRA和ADDBLDRB寄存器。

操作如下：

1.当同步触发输入(ELC_AD00)将ADC0的ADCSR.ADST位设置为1时，ADCSR.DBLANS[4:0]位中选择的单通道开始AD转换。

2.ADC0启动后经过一定时间后（请参阅第43.3.5.1节。触发输入时序），当ADC1的ADCSR.ADST位被同步触发输入(ELC_AD10)设置为1时，对于相同的模拟输入通道引脚与ADC0。

3.ADC0的AD转换在ADC1完成之前完成。AD转换结果存储在ADC0相关的AD数据寄存器y(ADDRy)和AD数据双工寄存器A(ADDBLDRA)中。

4.ADCSR.ADST位自动清零，ADC120进入等待状态。不会产生ADC120_ADI中断请求。

5.通过同步触发输入(ELC_AD01)重新启动ADC0的AD转换。让采样在ADC1的转换期间开始。

6.ADC1的AD转换完成。AD转换结果存储在ADC1相关的AD数据寄存器y(ADDRy)和AD数据双工寄存器A(ADDBLDRA)中。

7.ADCSR.ADST位自动清零，ADC121进入等待状态。不会产生ADC121_ADI中断请求。

8.通过同步触发输入(ELC_AD11)重新启动ADC1的AD转换。让采样在ADC0的转换期间开始。

9.ADC0的AD转换完成。AD转换结果存储在ADC0的AD数据双工寄存器(ADDBLDR)和AD数据双工寄存器B(ADDBLDRB)中。

10.ADCSR.ADST位自动清零，ADC120进入等待状态。产生一个ADC120_ADI中断请求。

11.通过同步触发输入(ELC_AD00)重新启动ADC0的AD转换。让采样在ADC1的转换期间开始。

12.ADC1的AD转换完成。AD转换结果存储在ADC1的AD数据双工寄存器(ADDBLDR)和AD数据双工寄存器B(ADDBLDRB)中。

13.ADCSR.ADST位自动清零，ADC121进入等待状态。产生一个ADC121_ADI中断请求。

14.通过同步触发输入(ELC_AD10)重新启动ADC1的AD转换。让采样在ADC0的转换期间开始。

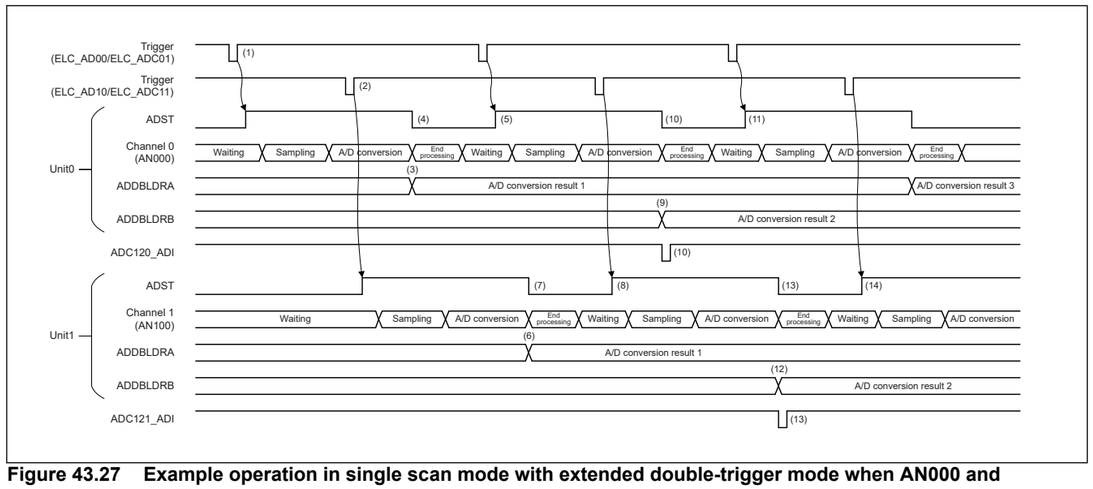


Figure 43.27 Example operation in single scan mode with extended double-trigger mode when AN000 and AN100 are selected in interleaved operation

43.3.6 Compare Function for Windows A and B

43.3.6.1 Compare function windows A and B

The compare function compares a reference value with the A/D conversion result. The reference value can be set for Window A and Window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. The main differences between Window A and Window B are their different interrupt output signals and the constraint on Window B of only one selectable channel.

This section provides an example operation that combines continuous scan mode and the compare function.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC) or an asynchronous trigger, A/D conversion starts in the order of the selected channels, temperature sensor, and internal reference voltage.
2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE = 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for Window A, the A/D conversion result is compared with the set ADCMPDR0/1 register value. When ADCMPCR.CMPBE = 1, if bits in the ADCMPBNSR register are set for Window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register setting.
3. As a result of the comparison, when Window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Window A Flag (ADCMPSR0.CMPSTCHAn, ADCMPSR1.CMPSTCHAn, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) sets 1. At this time, if the ADCMPCR.CMPAIE bit is 1, an ADC12i_CMPAI (i = 0, 1) interrupt request is generated. In the same way, when Window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Window B Flag (ADCMPBSR.CMPSTB) sets to 1. At this time, if the ADCMPCR.CMPBIE bit is 1, an ADC12i_CMPBI (i = 0, 1) interrupt request is generated.
4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC12i_CMPAI (i = 0, 1) and ADC12i_CMPBI (i = 0, 1) interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed for channels for which the compare flag is set to 1.
6. When all compare flags of Window A are cleared, the ADC12i_CMPAI (i = 0, 1) interrupt request is canceled. In the same way, when all compare flags of Window B are cleared, the ADC12i_CMPBI (i = 0, 1) interrupt request is reset. To perform comparison again, restart the A/D conversion.

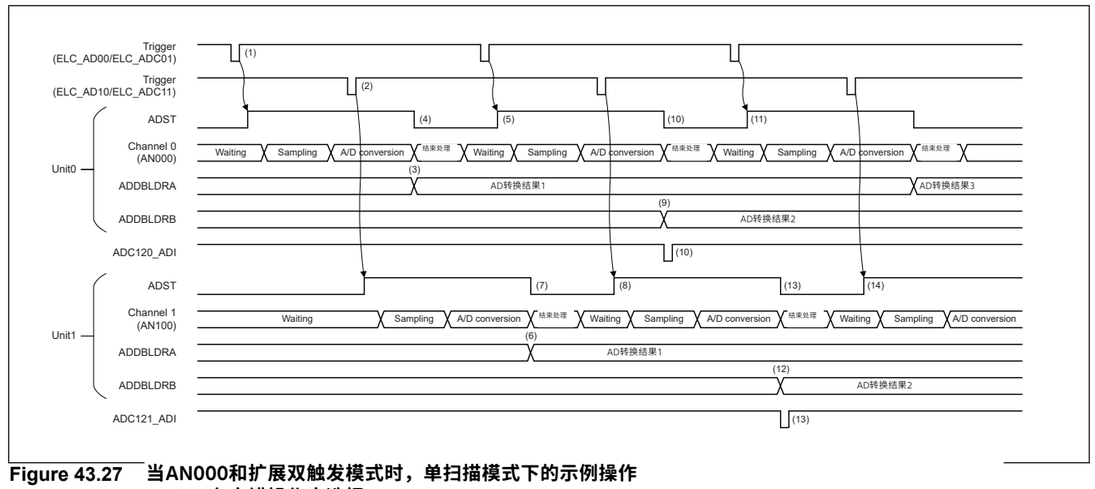


Figure 43.27 当AN000和扩展双触发模式时，单扫描模式下的示例操作 AN100在交错操作中选择

43.3.6 比较WindowsA和B的函数

43.3.6.1 比较功能窗口A和B

比较功能将参考值与AD转换结果进行比较。参考值可设置为
窗口A和窗口B独立。使用比较功能时，不能使用自诊断功能和双触发模式。WindowA和WindowB的主要区别在于它们的中断输出信号不同以及WindowB只能选择一个通道的限制。

本节提供结合连续扫描模式和比较功能的示例操作。

操作如下：

1.当ADCSR.ADST位通过软件设置为1（AD转换开始）时，同步触发(ELC)或
异步触发，AD转换按所选通道、温度传感器和内部参考电压的顺序开始。

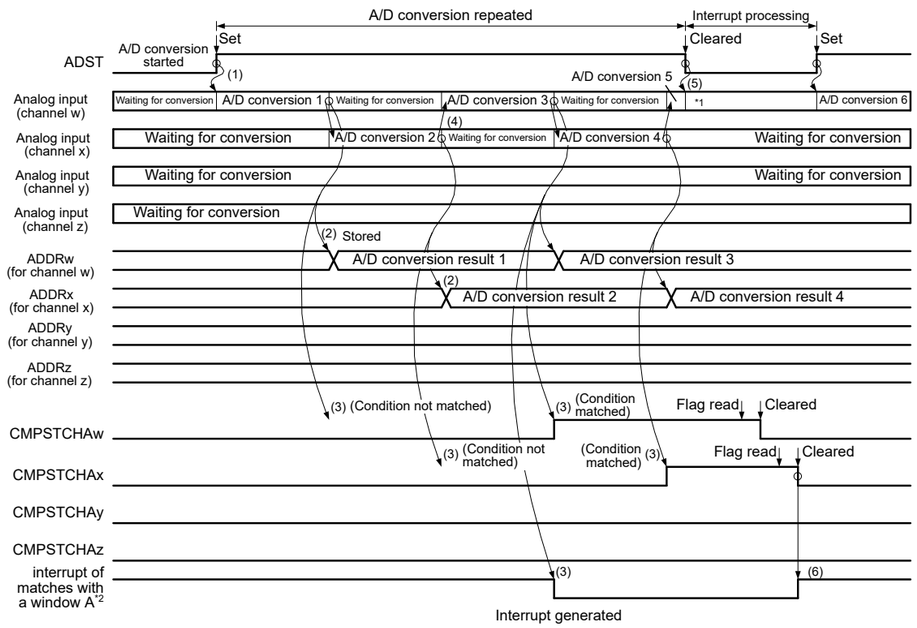
2.AD转换完成后，AD转换结果存储在相关的AD数据寄存器y（ADDRy、ADTSDR或ADOCDR）中。当ADCMPCR.CMPAE=1时，如果ADCMPANSRy寄存器或ADCMPANSER寄存器中的位为窗口A设置，则AD转换结果将与设置的ADCMPDR01寄存器值进行比较。当ADCMPCR.CMPBE=1时，如果ADCMPBNSR寄存器中的位为窗口B设置，则将AD转换结果与ADWINULBADWINLLB寄存器设置进行比较。

3.作为比较的结果，当窗口A满足在ADCMPLR01或ADCMPLER中设置的条件时，比较窗口A标志（ADCMPSR0.CMPSTCHAn、ADCMPSR1.CMPSTCHAn、ADCMPSER.CMPSTTSA或
ADCMPSER.CMPSTOCA)设置为1。此时，如果ADCMPCR.CMPAIE位为1，则产生ADC12i_CMPAI(i=0 1)中断请求。同样，当窗口B满足ADCMPBNSR.CMPLB中设置的条件时，比较窗口B标志（ADCMPBSR.CMPSTB）设置为1。此时，如果ADCMPCR.CMPBIE位为1，则
ADC12i_CMPBI(i=0 1)中断请求产生。

4.完成所有选定的AD转换和比较后，重新开始扫描。

5.接受ADC12i_CMPAI(i=0 1)和ADC12i_CMPBI(i=0 1)中断后，ADCSR.ADST位设置为0（A/D转换停止）并对比较标志的通道执行处理设置为1。

6.当窗口A的所有比较标志被清除时，ADC12i_CMPAI(i=0 1)中断请求被取消。在里面
同样，当窗口B的所有比较标志都被清除时，ADC12i_CMPBI(i=0 1)中断请求被复位。要再次进行比较，请重新开始AD转换。



Note: w, x, y, and z (w < x < y < z) are the selected channel numbers by ADANSA0/1.
Note 1. Data on conversion is ignored.
Note 2. ADC12i_CMPAI (i = 0, 1)

Figure 43.28 Example of compare function operation, when the analog inputs (channel w to z) are compared

43.3.6.2 Event output of compare function

The event output of the compare function specifies the upper-side reference voltage value and the lower-side reference voltage value for window A and window B, respectively. The output compares the A/D converted value of the selected channel with the upper and lower side reference voltage value and outputs events (ADC12i_WCMPM (i = 0, 1)/ ADC12i_WCMPUM (i = 0, 1)) based on event conditions (A or B, A and B, A xor B) and comparison result of window A and window B.

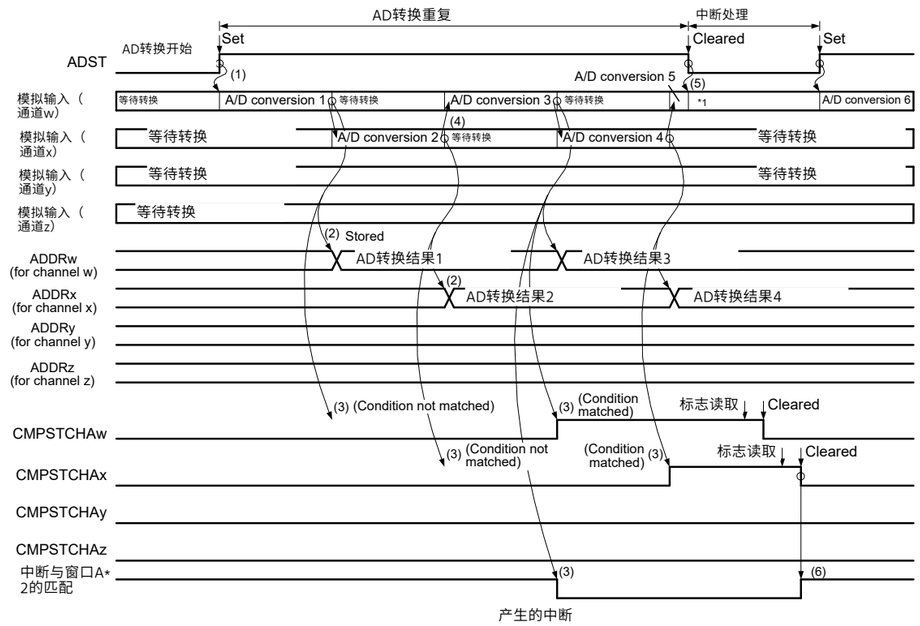
If more than one channel is selected for window A, and even when one channel in window A meets the comparison condition, the comparison result of window A is met. When using this function, perform A/D conversion in single scan mode.

Any channels from analog input, internal reference voltage, and temperature sensor output are selectable for window A.

One channel from analog input, internal reference voltage, and temperature sensor output is selectable for window B.

The following sequence is an example of how to set up and use the event output of the compare function:

1. Confirm that the value in the ADCSR.ADCS bits is 00b (single scan mode).
2. Select the channel for window A in the ADCMPANSR0/1 and ADCMPANSER registers. Set the window comparison conditions in the ADCMPLR0/1 and ADCMPLER registers. Set the upper-side and lower-side reference values in the ADCMPDR0/1 registers.
3. Select the channel and comparison conditions for Window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB and ADWINLLB registers.
4. Set the composite conditions for window A/B, window A/B operation enable, and interrupt output enable in the ADCMPCR register.



Note: w、x、y和z(w<x<y<z)是ADANSA01选择的通道号。
注1.转换数据被忽略。
Note 2. ADC12i_CMPAI (i = 0, 1)

Figure 43.28 比较功能操作示例，比较模拟输入（通道w到z）时

43.3.6.2 比较函数的事件输出

比较函数的事件输出分别指定窗口A和窗口B的上侧参考电压值和下侧参考电压值。输出将所选通道的AD转换值与上下侧参考电压值进行比较，并根据事件条件（A或B、AandB AxorB)和窗口A和窗口B的比较结果。

如果窗口A选择了多个通道，即使窗口A中的一个通道满足比较条件，也满足窗口A的比较结果。使用此功能时，请在单次扫描模式下进行AD转换。

来自模拟输入、内部参考电压和温度传感器输出的任何通道都可选择用于窗口A。

窗口B可选择模拟输入、内部参考电压和温度传感器输出的一个通道。

以下序列是如何设置和使用比较函数的事件输出的示例：

1.确认ADCSR.ADCS位中的值为00b（单次扫描模式）。

2.在ADCMPANSR01和ADCMPANSER寄存器中选择窗口A的通道。在ADCMPLR01和ADCMPLER寄存器中设置窗口比较条件。在ADCMPDR01寄存器中设置上侧和下侧参考值。

3.在ADCMPBNSR寄存器中选择窗口B的通道和比较条件，并在ADWINULB和ADWINLLB寄存器中设置上下参考值。

4.在ADCMPCR寄存器中设置窗口AB、窗口AB操作使能和中断输出使能的复合条件。

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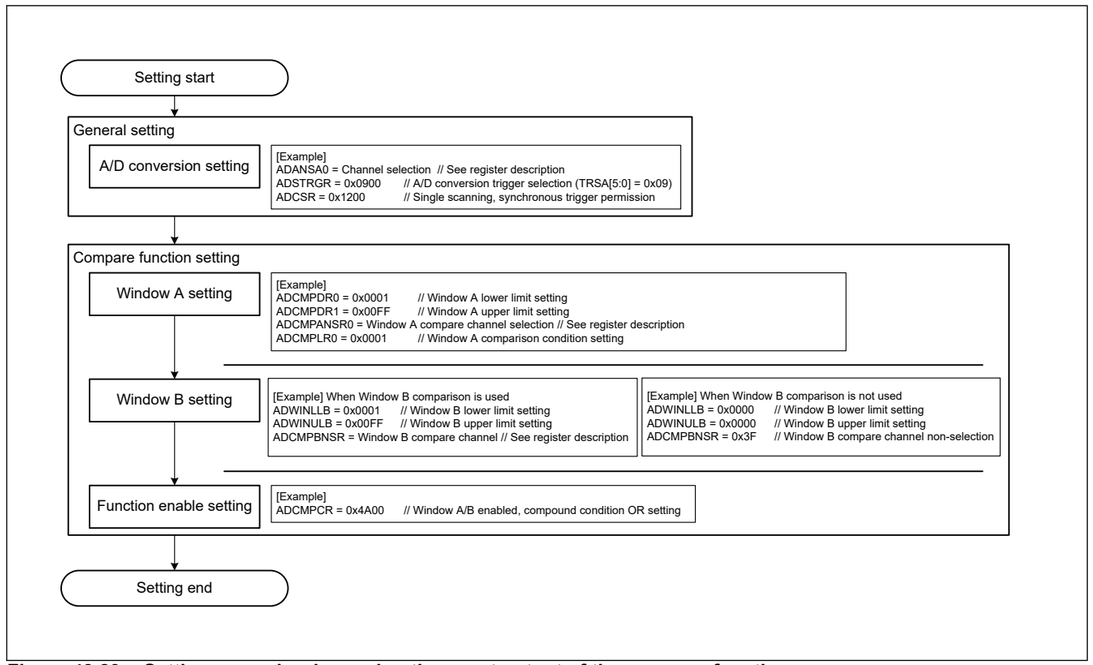


Figure 43.29 Setting example when using the event output of the compare function

For event output usage when using only window A for the compare function, note the following:

- Enable both Window A and Window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)
- Set the compound condition of Window A and Window B to “OR condition” (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of Window B to “No selection” (ADCMPBNSR.CMPCHB[5:0] = 0x3F)
- Set the compare condition of Window B to “0 < results < 0 always means mismatch”. (ADCMPCR.WCMPE = 1, ADWINLLB[15:0] = ADWINULB[15:0] = 0x0000, and ADCMPBNSR.CMPLB = 1)

Figure 43.30 shows the event output operation example of compare function.

A scan end event (ADC12i_ADI (i = 0, 1)) is output with the same timing as single scan completion. A match or mismatch event (ADC12i_WCMPM (i = 0, 1)/ADC12i_WCMPUM (i = 0, 1)) is output with 1 PCLKA cycle delay depending on the ADCMPCR.CMPAB[1:0] settings.

Note: The match and mismatch events are exclusive, so both events are never output simultaneously.

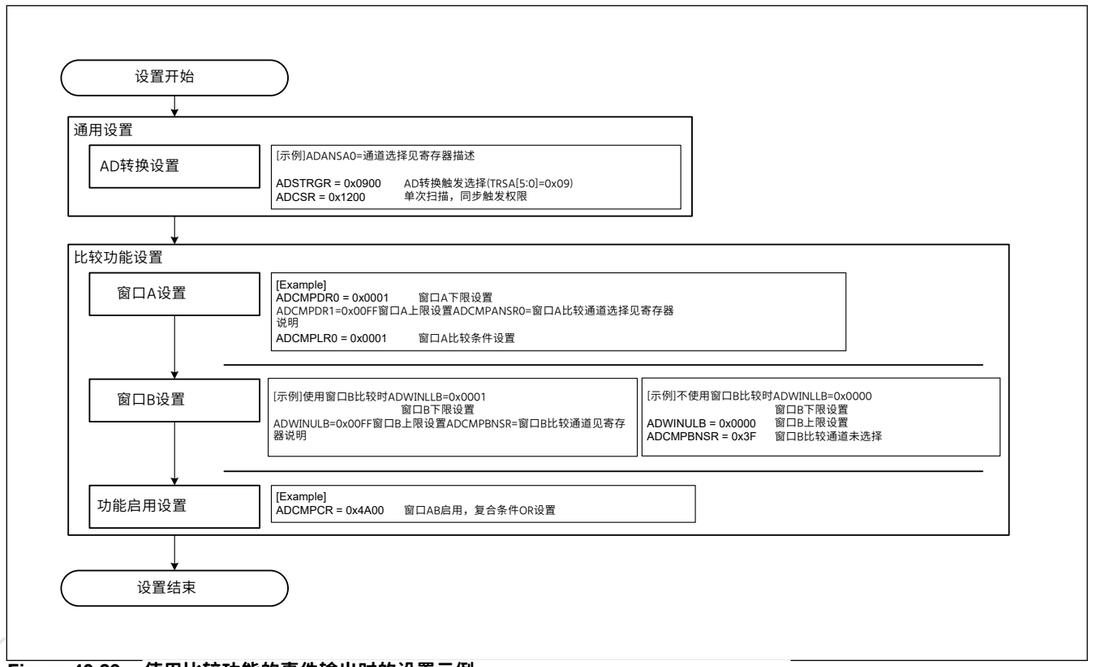


Figure 43.29 使用比较功能的事件输出时的设置示例

对于仅将窗口A用于比较功能时的事件输出用法，请注意以下几点：

●启用窗口A和窗口B(ADCMPCR.CMPAE=1 ADCMPCR.CMPBE=1)

●将窗口A和窗口B的复合条件设置为“或条件”（ADCMPCR.CMPAB[1:0]=00b）

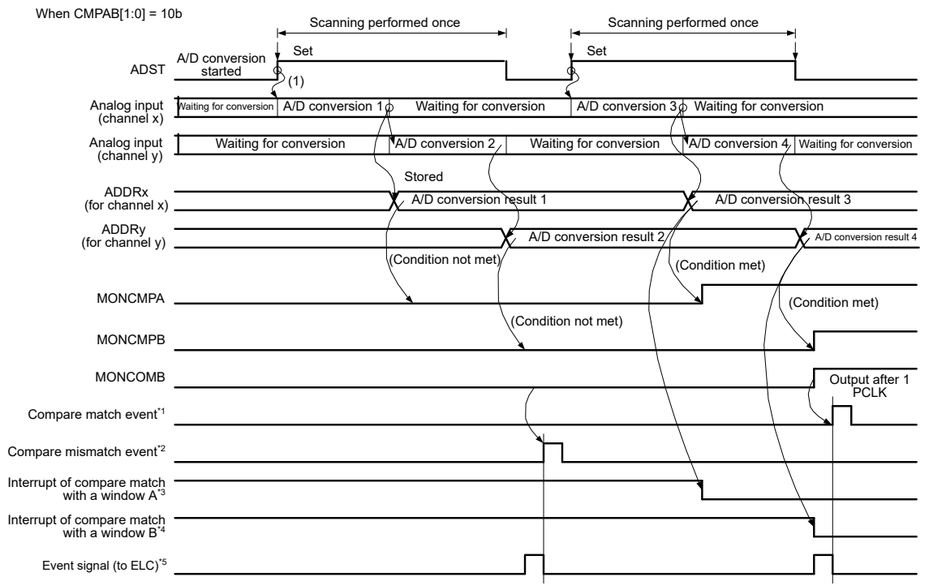
●将窗口B的比较通道设置为“无选择”（ADCMPBNSR.CMPCHB[5:0]=0x3F）

●将窗口B的比较条件设置为“0<结果<0总是不匹配”。（ADCMPCR.WCMPE=1，ADWINLLB[15:0]=ADWINULB[15:0]=0x0000，ADCMPBNSR.CMPLB=1）

图43.30显示了比较功能的事件输出操作示例。

以与单次扫描完成相同的时序输出扫描结束事件(ADC12i_ADI(i=0 1))。匹配或不匹配事件(ADC12i_WCMPM(i=0 1)ADC12i_WCMPUM(i=0 1))以1个PCLKA周期延迟输出，具体取决于ADCMPCR.CMPAB[1:0]设置。

Note: match和mismatch事件是互斥的，因此这两个事件永远不会同时输出。



Note: x, and y (x < y) are the selected channel numbers by ADANSA0/1.
Note 1. ADC12i_WCMPM (i = 0, 1)
Note 2. ADC12i_WCMPUM (i = 0, 1)
Note 3. ADC12i_CMPAI (i = 0, 1)
Note 4. ADC12i_CMPBI (i = 0, 1)
Note 5. ADC12i_ADI (i = 0, 1)

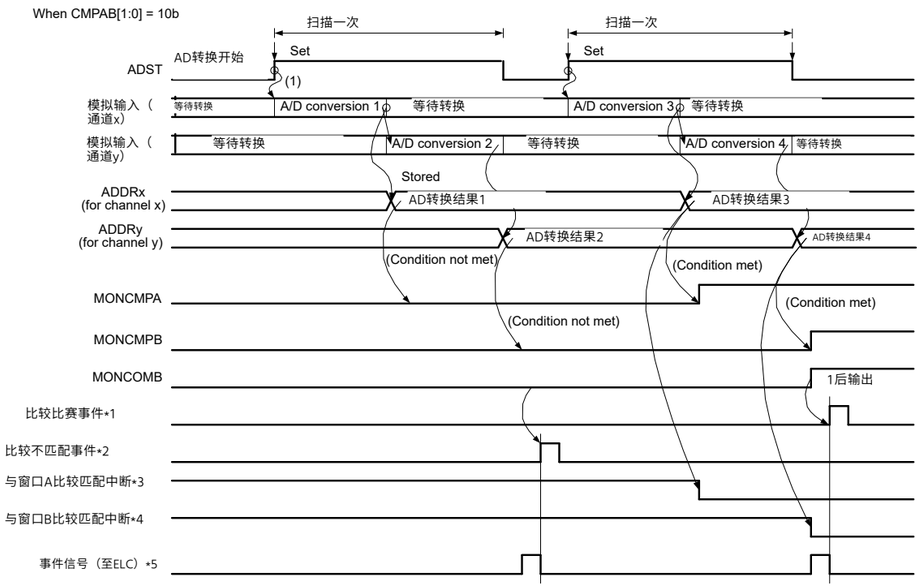
Figure 43.30 Example operation of the compare function event output, when the analog inputs (channel x and y) are compared

Note: Event output of compare function outputs match/mismatch from the comparison results of Window A and Window B, based on the ADCMPCR.CMPAB[1:0] settings.
Note: The comparison result of Window A is the logical addition of the comparison results of the comparison target channels of Window A. The comparison results of Window A and Window B are updated by each A/D conversion, and are kept even when single scan ends. Set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0 to clear the comparison results to 0.

43.3.6.3 Restrictions on the compare function

The following constraints apply for the compare function:

- The compare function cannot be used together with the self-diagnosis function or double-trigger mode. (The compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.)
- Specify single scan mode when using match/mismatch event outputs.
- When the temperature sensor output, internal reference voltage is selected for Window A, Window B operations are disabled.
- When the temperature sensor output, internal reference voltage is selected for Window B, Window A operations are disabled.
- Setting the same channel for Window A and Window B is prohibited.
- Set the reference voltage values so that the high-potential reference voltage value is equal to or larger than the low potential reference voltage value.



Note: x和y(x<y)是ADANSA01选择的通道号。
Note 1. ADC12i_WCMPM (i = 0, 1)
Note 2. ADC12i_WCMPUM (i = 0, 1)
Note 3. ADC12i_CMPAI (i = 0, 1)
Note 4. ADC12i_CMPBI (i = 0, 1)
Note 5. ADC12i_ADI (i = 0, 1)

Figure 43.30 比较模拟输入（通道x和y）时比较功能事件输出的示例操作

Note: 根据ADCMPCR.CMPAB[1:0]设置，比较函数输出的事件输出与窗口A和窗口B的比较结果匹配不匹配。

Note: 窗口A的比较结果是窗口A的比较目标通道的比较结果的逻辑相加。窗口A和窗口B的比较结果在每次AD转换时更新，即使在单次扫描结束时也会保持。将ADCMPCR.CMPAE和ADCMPCR.CMPBE设置为0，将比较结果清除为0。

43.3.6.3 比较功能的限制

以下约束适用于比较功能：

●比较功能不能与自诊断功能或双触发模式一起使用。（比较功能不适用于ADRD、ADDBLDR、ADDBLDRA和ADDBLDRB。）

●使用匹配不匹配事件输出时指定单次扫描模式。

●当温度传感器输出时，WindowA选择内部参考电压，WindowB操作被禁用。

●当温度传感器输出时，WindowB选择内部参考电压，WindowA操作被禁用。

●禁止窗口A和窗口B设置相同的通道。

●设置参考电压值，使高电位参考电压值等于或大于低电位参考电压值。

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43.3.7 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRGn (n = 0, 1)). After the start-of-scanning-delay time (t_D) has elapsed, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed, followed by processing for A/D conversion.

Figure 43.31 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 43.32 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger (ADTRGn (n = 0, 1)). The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), disconnection detection assistance processing time (t_{DIS})*1, self-diagnosis A/D conversion processing time (t_{DIAG} and t_{DSD})*2, A/D conversion processing time (t_{CONV}), and end-of-scanning-delay time (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/ D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTRn register.

The time for conversion by successive approximation (t_{SAM}) is the following

- 13 ADCLK states with 12-bit accuracy selected.
- 11 ADCLK states with 10-bit accuracy selected.
- 9 ADCLK states with 8-bit accuracy selected.

Table 43.27 shows the time for conversion by successive approximation (t_{SAM}).

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + t_{ED} + (t_{CONV} \times n)$$ *3

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} . The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed in the following:

$$(t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV} \times n)$$ *3

Note 1. When disconnection detection assistance is not selected, t_{DIS} = 0.

Only when the temperature sensor or internal reference voltage is A/D-converted, the auto-discharge period of 15 ADCLK states is inserted.

Note 2. When the self-diagnosis function is not used, t_{DIAG} = 0, t_{DSD} = 0.

Note 3. When input sampling times (t_{SPL}) of all selected channels are the same, this element equals t_{CONV} × n. If each channel has a different sampling time, this element equals that of t_{SPL} and t_{SAM} set to each selected channel.

Table 43.27 shows the times for conversion during scanning.

43.3.7 模拟输入采样和扫描转换时间

扫描转换可以通过软件触发、同步触发(ELC)或异步触发(ADTRGn(n=0 1))来激活。在经过扫描开始延迟时间(tD)之后，断线检测辅助处理和自诊断转换处理全部进行，接着进行AD转换处理。

图43.31显示了扫描转换时序，其中扫描转换由软件触发或同步触发(ELC)激活。图43.32显示了扫描转换时序，其中扫描转换由异步触发(ADTRGn(n=0 1))激活。扫描转换时间(tSCAN)包括扫描开始延迟时间(tD)、断线检测辅助处理时间(tDIS)*1、自诊断AD转换处理时间(tDIAG和tDSD)*如图2所示，AD转换处理时间(tCONV)和扫描结束延迟时间(tED)。

AD转换处理时间(tCONV)由输入采样时间(tSPL)和逐次逼近转换时间(tSAM)组成。采样时间(tSPL)用于为AD转换器中的采样保持电路充电。如果由于模拟输入信号源的高阻抗而没有足够的采样时间，或者如果AD转换时钟(ADCLK)很慢，则可以使用ADSSTRn寄存器调整采样时间。

逐次逼近转换时间(tSAM)如下

- 13个ADCLK状态，选择12位精度。
- 11个ADCLK状态，选择精度为10位。
- 选择8位精度的9个ADCLK状态。

表43.27显示了逐次逼近转换的时间(tSAM)。

选择通道数为n的单次扫描模式下的扫描转换时间(tSCAN)可以确定如下：

tSCAN=tD+tDIS×n+tDIAG+tED+tCONV×n*3

连续扫描模式下第一个周期的扫描转换时间是单次扫描的tSCAN减去tED。连续扫描模式下第二个和后续周期的扫描转换时间固定如下：tDIS×n+tDIAG+tDSD+tCONV×n*3

注1.未选择断线检测辅助时，tDIS=0。

仅当温度传感器或内部参考电压为AD转换时，自动放电周期为15 ADCLK状态被插入。

注2.不使用自诊断功能时，tDIAG=0，tDSD=0。

注3.当所有选定通道的输入采样时间(tSPL)相同时，该元素等于tCONV×n。如果每个通道具有不同的采样时间，则该元素等于为每个选定通道设置的tSPL和tSAM。

表43.27显示了扫描期间的转换时间。

Table 43.27 Conversion times during scanning (in numbers of cycles of ADCLK and PCLKA)

Item			Symbol		Type/Conditions: Synchronous trigger*4	Asynchronous trigger	Software trigger	Unit
Scan start processing time*1 *2	A/D conversion on group A under group A priority control.	Group B is to be stopped (Group A is activated after group B is stopped by of an A/D conversion source from group A).	t_D		3 PCLKA + 6 ADCLK 5 PCLKA + 3 ADCLK*5	—	—	Cycles
		Group B is not to be stopped (activation by an A/D conversion source from group A).			2 PCLKA + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled.	A/D conversion for self-diagnosis is to be started.			2 PCLKA + 6 ADCLK	4 PCLKA + 6 ADCLK	6 ADCLK	
	All other				2 PCLKA + 4 ADCLK	2 PCLKA + 4 ADCLK	4 ADCLK	
Disconnection detection assistance processing time			t_{DIS}		Setting in ADNDIS[3:0] (initial value = 0h) × ADCLK			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	Setting in ADSSTR00 (initial value = 0Bh) × ADCLK*3	—	—	
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	15 ADCLK	—	—	
		10-bit conversion accuracy			13 ADCLK	—	—	
		8-bit conversion accuracy			11 ADCLK	—	—	
	Wait time between self-diagnosis conversion end and analog channel sampling start.			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode.		t_{DSD}		2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	Setting in ADSSTRn (n = 0 to 10, 12, 13(unit 0), 0 to 2(unit 1), L, T, O) (initial value = 0Bh) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	13 ADCLK			
		10-bit conversion accuracy			11 ADCLK			
		8-bit conversion accuracy			9 ADCLK			
Scan end processing time*1			t_{ED}		1 PCLKA + 3 ADCLK 2 PCLKA + 3 ADCLK*5			

Note 1. See Figure 43.31 and Figure 43.32 for an illustration of times t_D, t_{SPLSH}, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The sampling time setting must satisfy the electrical characteristics.
Note 4. This does not include the time consumed in the path from timer output to trigger input.
Note 5. If ADCLK is faster than PCLKA (PCLKA to ADCLK frequency ratio = 1:2 or 1:4), the scan end processing time changes.

Table 43.27 扫描期间的转换时间（以ADCLK和PCLKA的周期数计）

Item			Symbol		Type/Conditions: 同步触发*4	异步触发	软件触发	Unit
扫描开始处理时间*1*2	A组优先控制下A组AD转换。	B组停止（A组的AD转换源停止B组后激活A组）。	t_D		3 PCLKA + 6 ADCLK 5 PCLKA + 3 ADCLK*5	—	—	Cycles
		B组不停止（由A组的AD转换源激活）。			2 PCLKA + 4 ADCLK	—	—	
	启用自诊断时的AD转换。	将启动用于自诊断的D转换。			2 PCLKA + 6 ADCLK	4 PCLKA + 6 ADCLK	6 ADCLK	
	所有其他				2 PCLKA + 4 ADCLK	2 PCLKA + 4 ADCLK	4 ADCLK	
断线检测辅助处理时间			t_{DIS}		ADNDIS[3:0]中的设置（初始值=0h）×ADCLK			
自诊断转换处理时间*1	采样时间		t_{DIAG}	t_{SPL}	ADSSTR00中的设置（初始值=0Bh）×ADCLK*3	—	—	
	逐次逼近转换时间	12位转换精度		t_{SAM}	15 ADCLK	—	—	
		10位转换精度			13 ADCLK	—	—	
		8位转换精度			11 ADCLK	—	—	
	自诊断转换结束到模拟通道采样开始之间的等待时间。			t_{DED}	2 ADCLK			
	连续扫描模式下最后一次通道转换结束和自诊断采样开始之间的等待时间。		t_{DSD}		2 ADCLK			
AD转换处理时间*1	采样时间		t_{CONV}	t_{SPL}	在ADSSTRn中设置（n=0到10、12、13（单元0），0到2（单元1），L, T, O) (initial value = 0Bh) × ADCLK + 0.5 ADCLK			
	逐次逼近转换时间	12位转换精度		t_{SAM}	13 ADCLK			
		10位转换精度			11 ADCLK			
		8位转换精度			9 ADCLK			
扫描结束处理时间*1			t_{ED}		1 PCLKA + 3 ADCLK 2 PCLKA + 3 ADCLK*5			

注1.有关时间tD、tSPLSH、tDIAG、tCONV和tED的说明，请参见图43.31和图43.32。注2.这是从软件写入或触发输入到AD转换开始所需的最长时间。
注3.采样时间设置必须满足电气特性。
注4.这不包括从定时器输出到触发输入的路径中消耗的时间。
注5.如果ADCLK比PCLKA快（PCLKA与ADCLK频率比=1:2或1:4），则扫描结束处理时间会发生变化。

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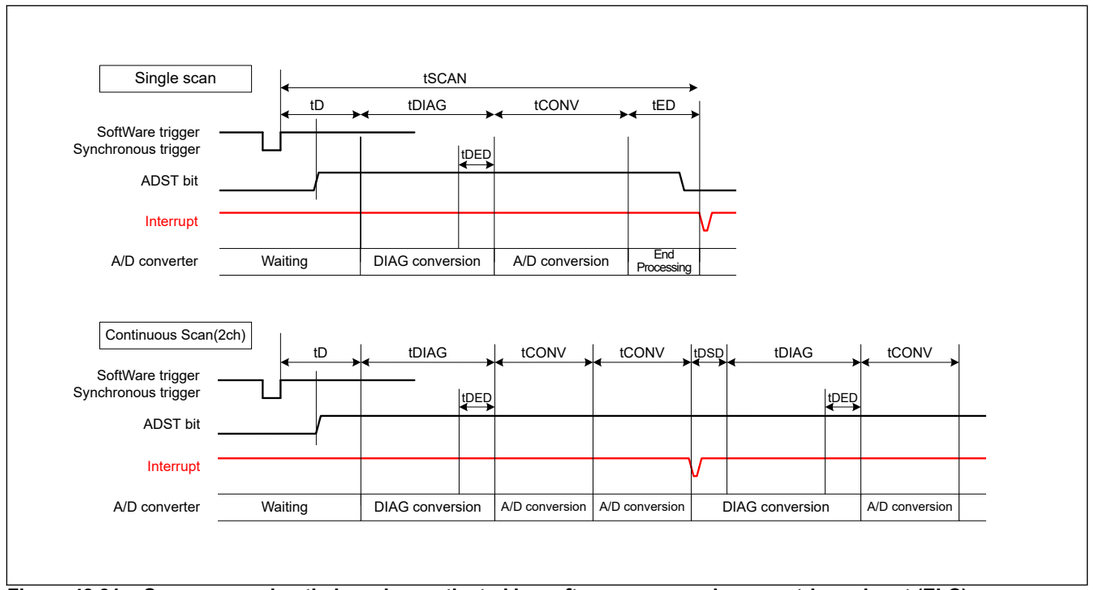

Figure 43.31 Scan conversion timing when activated by software or a synchronous trigger input (ELC)

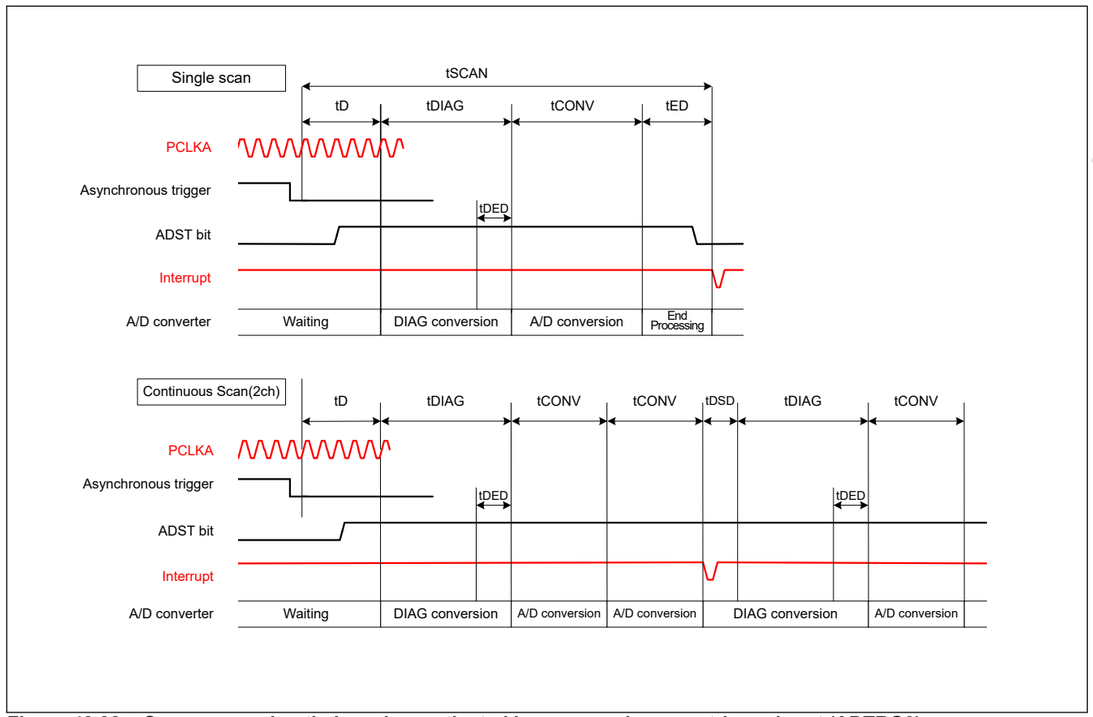

Figure 43.32 Scan conversion timing when activated by an asynchronous trigger input (ADTRG0)

43.3.8 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ADCER.ACE bit to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR) to 0x0000 when the A/D data registers are read by the CPU or DTC or DMAC.

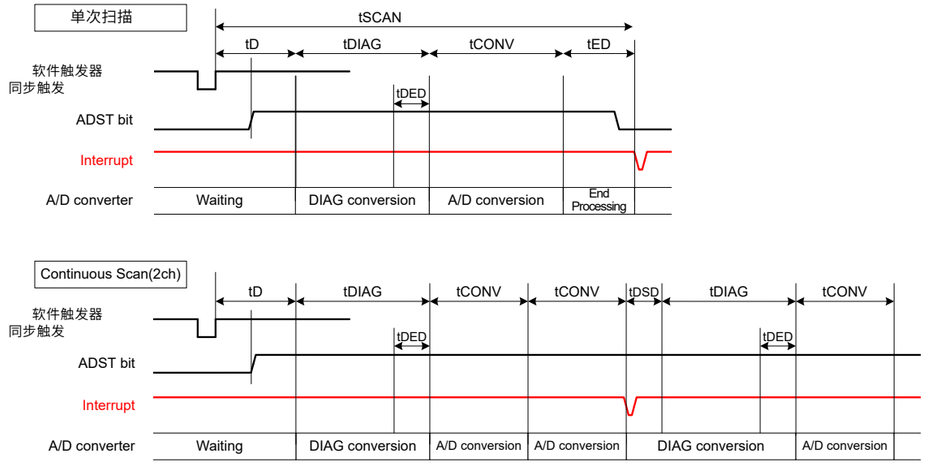

Figure 43.31 由软件或同步触发输入(ELC)激活时的扫描转换时序

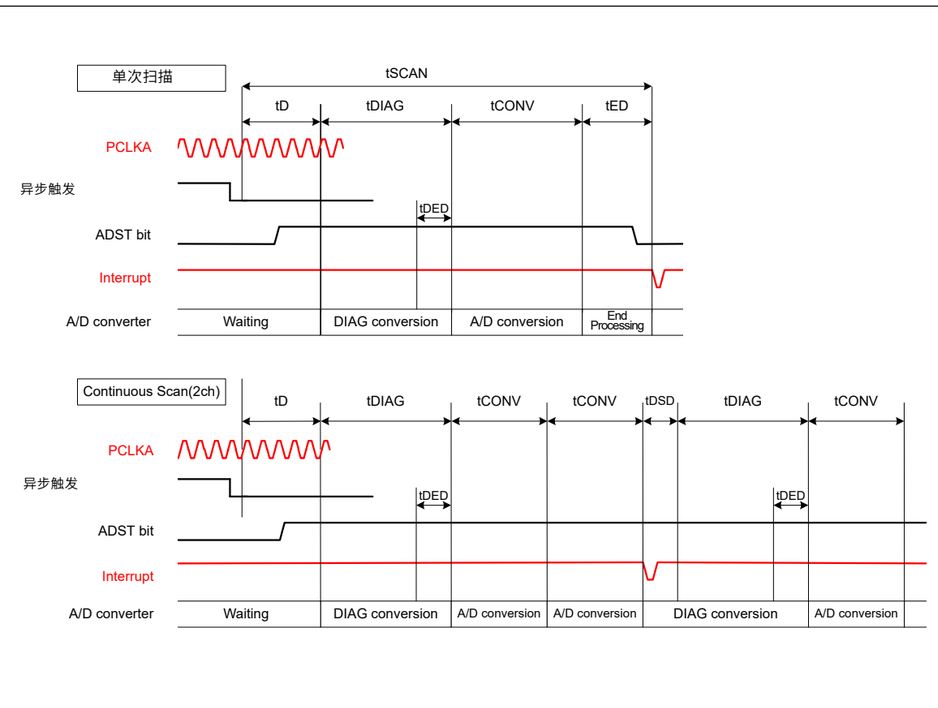

Figure 43.32 由异步触发输入(ADTRG0)激活时的扫描转换时序

43.3.8 AD数据寄存器自动清除功能的使用示例

将ADCER.ACE位设置为1会自动清除AD数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、当CPU或DTC或DMAC读取AD数据寄存器时，ADDBLDRB、ADTSDR、ADOCDR)为0x0000。

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This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR). This section describes examples in which the function to automatically clear the ADDRy register is enabled and disabled.

- If the ADCER.ACE bit is 0 (automatic clearing is disabled) and for some reason, if the A/D conversion result (0x0222) is not written to the ADDRy register, the ADDRy value retains the old data (0x0111). In addition, if this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0x0111) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.
- If the ADCER.ACE bit is 1 (automatic clearing is enabled), when ADDRy = 0x0111 is read by the CPU or DTC or DMAC, ADDRy is automatically set to 0x0000. Next, if the A/D conversion result of 0x0222 cannot be transferred to ADDRy for some reason, the cleared data (0x0000) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, 0x0000 is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0x0000.

43.3.9 A/D-Converted Value Addition/Average Mode

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, the temperature sensor output, the internal reference voltage is selected.

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16 consecutive times, and the sum of the converted values is stored in the data register. The conversion count of the addition function can be set to 16 only when 12-bit accuracy is selected. In A/D-converted value average mode, the same channel is A/D-converted 1, 2, or 4 consecutive times, and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.

The A/D-converted value addition/average function can be used when A/D conversion of the analog inputs of the selected channels or A/D conversion of the temperature sensor output or A/D conversion of the internal reference voltage is selected. The A/D-converted value addition/average function can also be used for channels for which the double-trigger function is selected.

The addition function for self-diagnosis is not provided.

43.3.10 Disconnection Detection Assist Function

The ADC12 incorporates a function to fix the charge for sampling capacitance to the specified state (VREFH0 or VREFL0 for unit 0, VREFH or VREFL for unit 1) before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

Figure 43.33 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 43.34 shows an example of disconnection detection when precharge is selected. Figure 43.35 shows an example of disconnection detection when discharge is selected.

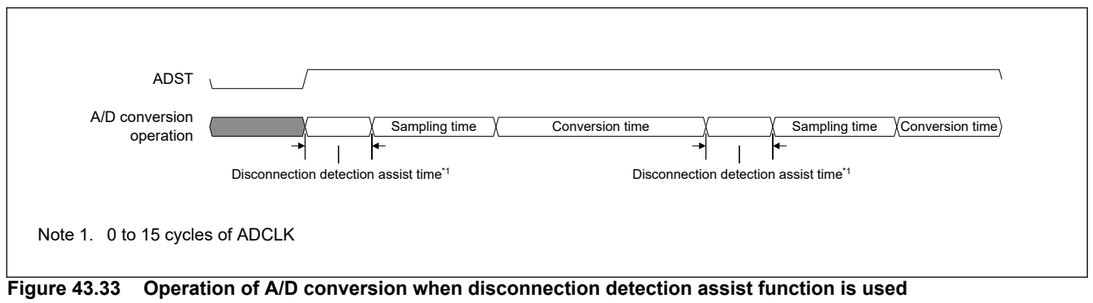


Figure 43.33 Operation of A/D conversion when disconnection detection assist function is used

此功能可以检测AD数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR、ADOCDR）。本节介绍自动清除功能的示例ADDRy寄存器被启用和禁用。

●如果ADCER.ACE位为0（禁止自动清零）并且由于某种原因，如果AD转换结果（0x0222）没有写入ADDRy寄存器，则ADDRy值保留旧数据（0x0111）。此外，如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则可以将旧数据（0x0111）保存在通用寄存器中。在检查是否有更新失败时，需要经常将旧数据保存在SRAM或通用寄存器中。

●如果ADCER.ACE位为1（使能自动清除），当ADDRy=0x0111时由CPU或DTC或DMAC ADDRy自动设置为0x0000。接下来，如果0x0222的AD转换结果由于某种原因无法传送到ADDRy，则清除的数据(0x0000)仍保留为ADDRy值。如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则将0x0000保存在通用寄存器中。ADDRy更新失败的发生可以通过检查读取的数据值为0x0000来确定。

43.3.9 一种D转换的增值平均模式

AD-convertedvalueadditionaveragemodecanbeusedwhenADconversionoftheanaloginputoftheselectedchannels thetemperaturesensoroutput theinternalreferencevoltageisselected.

在AD转换值加法模式下，同一通道连续1、2、3、4或16次AD转换，转换值的总和存储在数据寄存器中。只有选择12位精度时，才能将加法功能的转换计数设置为16。在AD转换值平均模式下，同一通道连续1、2或4次AD转换，转换值的平均值存储在数据寄存器中。根据存在的噪声成分的类型，使用这些结果的平均值可以提高AD转换的精度。但是，该功能不能始终保证AD转换精度的提高。

选择通道的模拟输入的AD转换或温度传感器输出的AD转换或内部参考电压的AD转换时，可以使用AD转换值加法平均功能。AD转换值加法平均功能也可用于选择了双触发功能的通道。

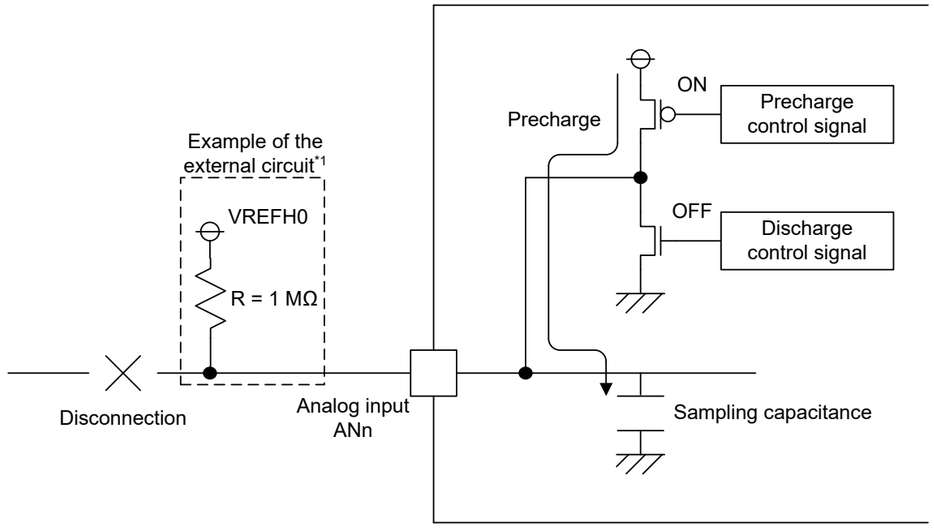
不提供自我诊断的附加功能。

43.3.10 断线检测辅助功能

ADC12具有在开始AD转换之前将采样电容的电荷固定到指定状态（单元0为VREFH0或VREFL0，单元1为VREFH或VREFL）的功能。此功能可在模拟输入接线中进行断线检测。

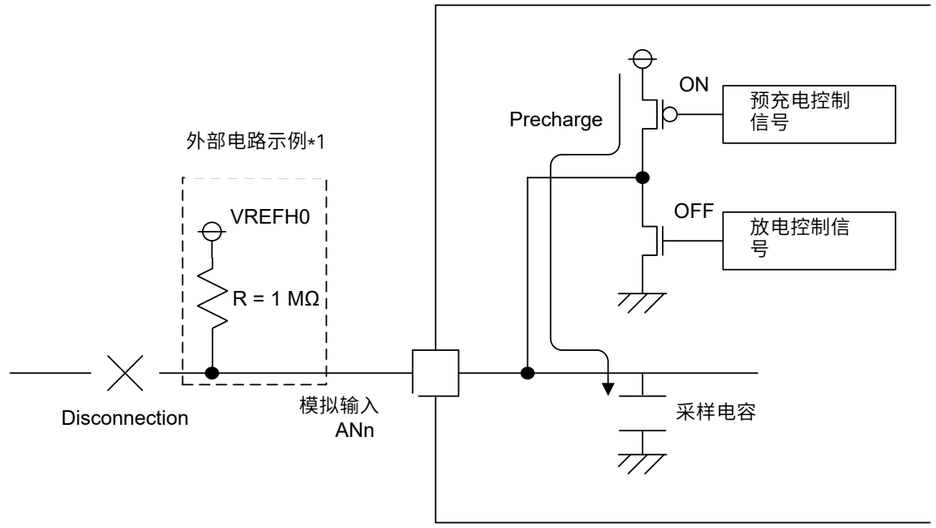
图43.33显示了使用断线检测辅助功能时的AD转换操作。图43.34显示了选择预充电时的断线检测示例。图43.35显示了选择放电时的断线检测示例。

Figure 43.33 使用断线检测辅助功能时的AD转换动作



Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 43.34 Example of disconnection detection when precharge is selected



注1.由于断线时的结果数据因外部电路而异，因此应在充分评估后使用转换结果。

Figure 43.34 选择预充电时的断线检测示例

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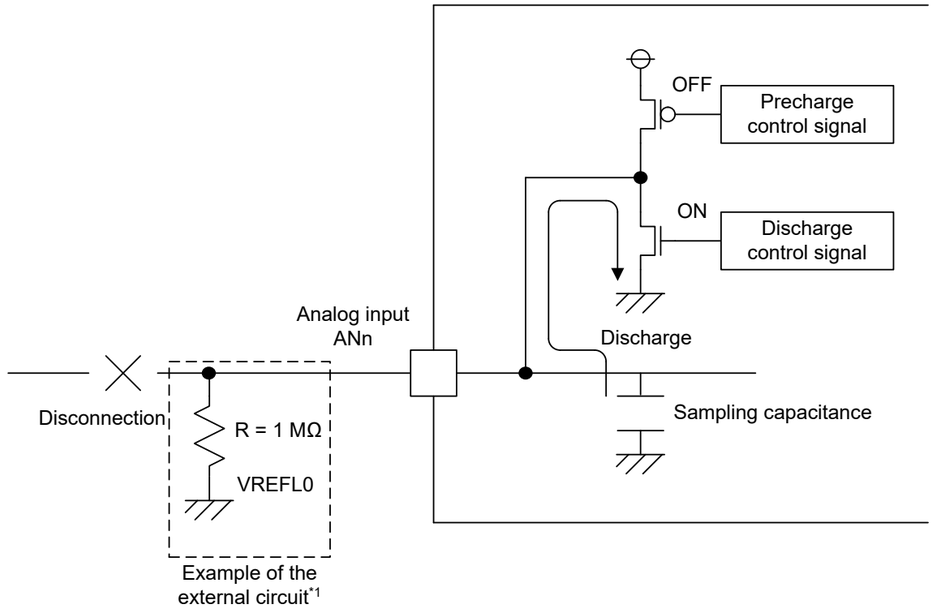


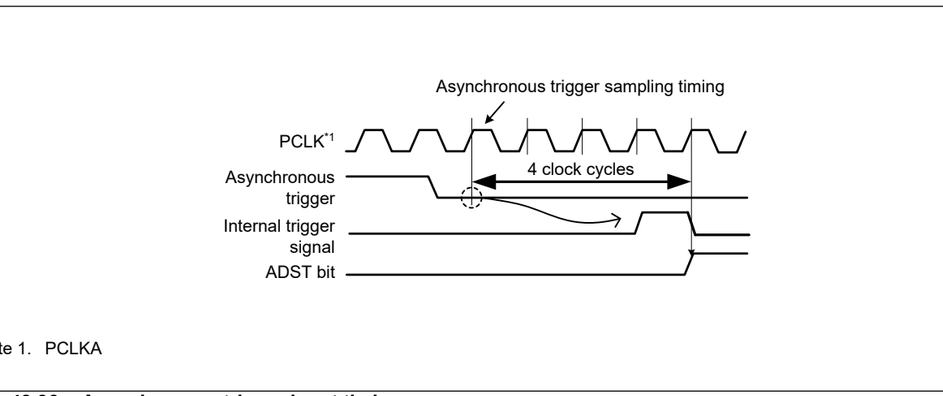
Note 1. The converted result should be used after it is fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 43.35 Example of disconnection detection when discharge is selected

43.3.11 Starting A/D Conversion with an Asynchronous Trigger

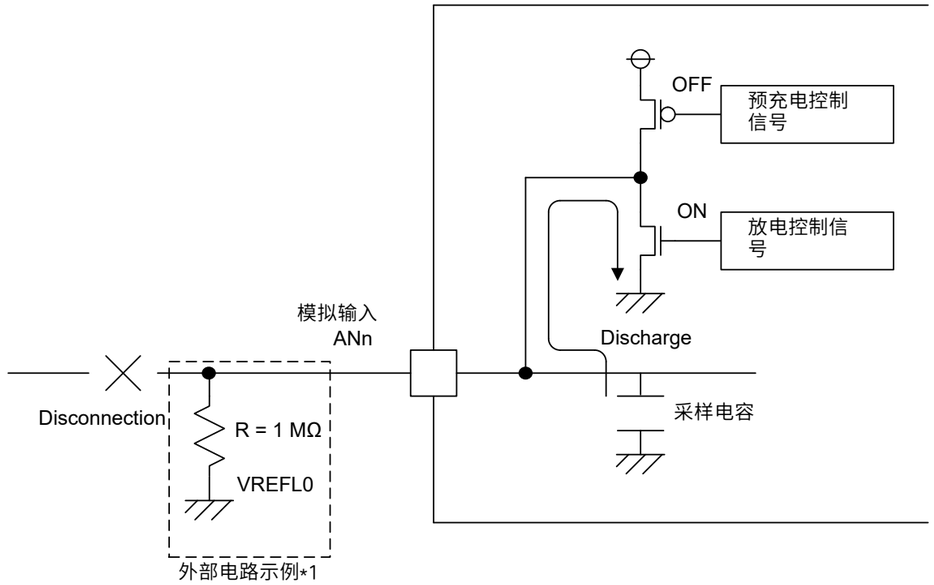
A/D conversion can be started by the input of an asynchronous trigger. To start A/D conversion by an asynchronous trigger, set the pin function in the PmnPFS register, set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 0x00, then input a high-level signal to the asynchronous trigger (ADTRGn (n = 0, 1) pin). Finally, set both the ADCSR.TRGE and ADCSR.EXTRG bits to 1. Figure 43.36 shows timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected in the A/D conversion start trigger for group B used in group scan mode. For details on setting the pin function, see section 19, I/O Ports.



Note 1. PCLKA

Figure 43.36 Asynchronous trigger input timing



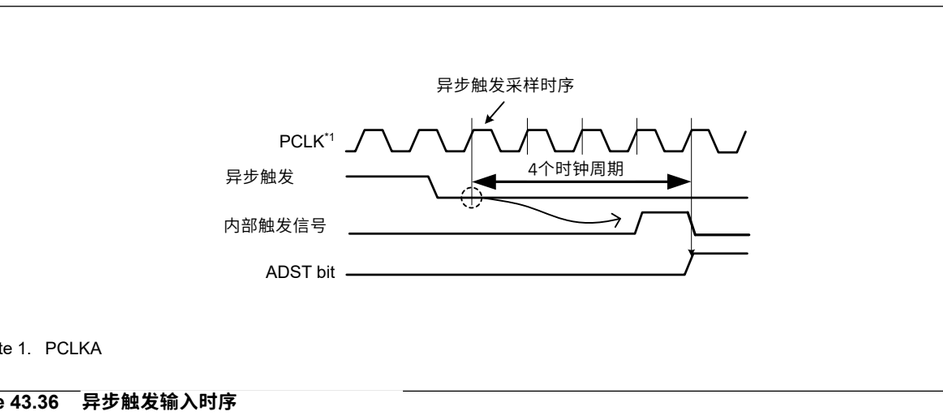
注1.由于断线时的结果数据因外部电路而异，因此应在充分评估后使用转换结果。

Figure 43.35 选择放电时的断线检测示例

43.3.11 使用异步触发启动AD转换

可以通过输入异步触发器来启动D转换。要通过异步触发启动AD转换，请在PmnPFS寄存器中设置引脚功能，将AD转换启动触发选择位(ADSTRGR.TRSA[5:0])设置为0x00，然后向异步触发输入高电平信号（ADTRGn(n=0 1)引脚）。最后，将ADCSR.TRGE和ADCSR.EXTRG位都设置为1。图43.36显示了异步触发输入的时序。

在组扫描模式中使用的B组的AD转换开始触发中不能选择异步触发。有关设置引脚功能的详细信息，请参见第19节，IO端口。



Note 1. PCLKA

Figure 43.36 异步触发输入时序

43.3.12 Starting A/D Conversion with a Synchronous Trigger from a Peripheral Module

A/D conversion can be started by a synchronous trigger (ELC). To do this, set the ADCSR.TRGE bit to 1 and the ADCSR.EXTRG bit to 0, and select the relevant sources in the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

43.3.13 Using Data Buffers

This IP is provided with a ring buffer function consisting of 16 A/D data buffers. This function sequentially stores A/D conversion results other than self-diagnosis result (including addition/average results) in data buffers (ADBUFn, n = 0 to 15).

Each conversion result is stored at the timing when the A/D conversion result is stored in the data register, and most recent 16 conversion result data are retained.

The figure-below shows the schematic of data buffers, pointer, and overflow flag operations. When the BUFEN bit is set to 1, the A/D conversion result is transferred at each end of A/D conversion. The pointer indicates the number of data buffer to which the next transferred data is to be written. When data is written to up to buffer 15, the pointer is reset to 0000b and the overflow flag is set to 1. Subsequently transferred data overwrites the previously written data.

The overflow flag is reset to the initial value by writing 00h to the ADBUFPTR register.

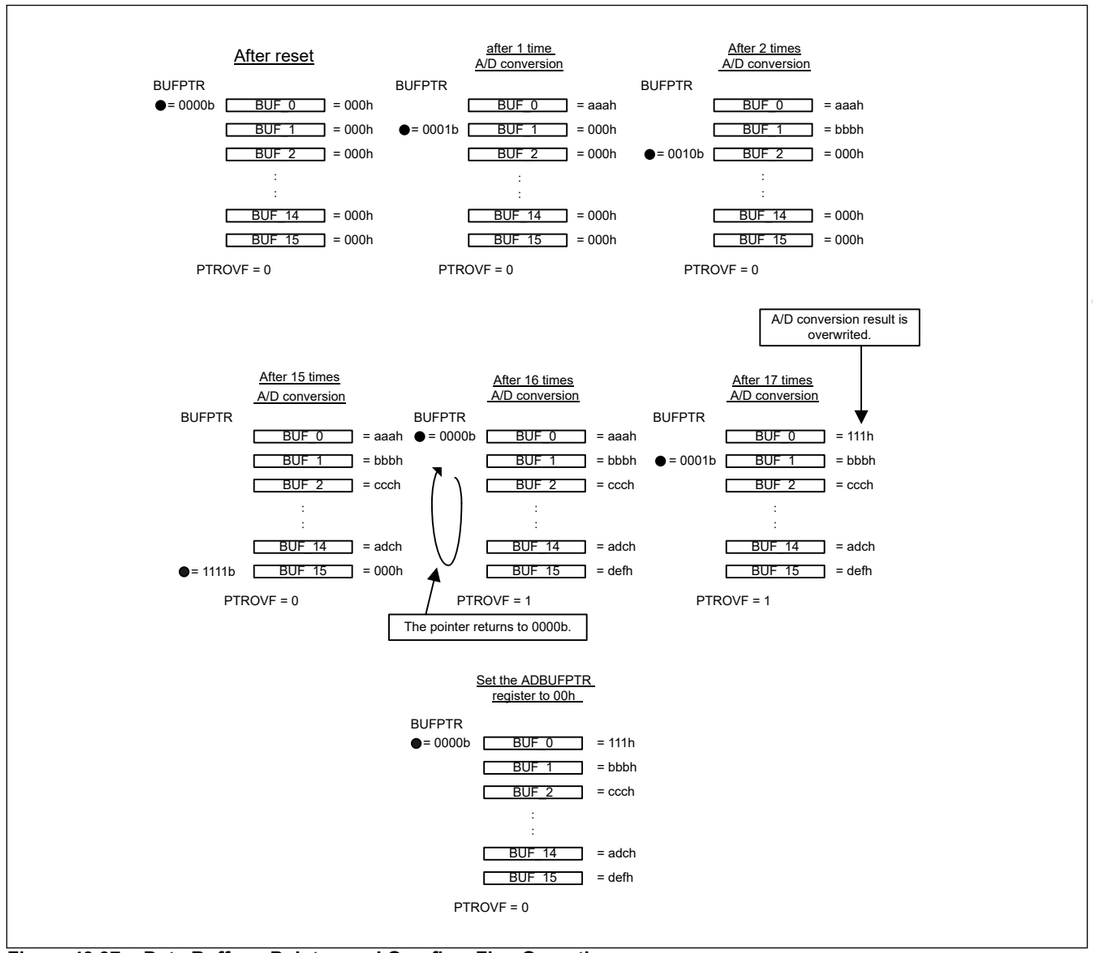


Figure 43.37 Data Buffers, Pointer, and Overflow Flag Operations

43.3.12 使用来自外设模块的同步触发启动AD转换

D转换可以通过同步触发器(ELC)启动。为此，将ADCSR.TRGE位设置为1，并将ADCSR.EXTRG位为0，并在ADSTRGR.TRSA[5:0]和ADSTRGR.TRSB[5:0]位中选择相关源。

43.3.13 使用数据缓冲区

该IP具有由16个AD数据缓冲区组成的环形缓冲区功能。该功能将除自诊断结果以外的AD转换结果（包括加法平均结果）依次存储在数据缓冲区（ADBUFn，n=0至15）中。

每个转换结果在AD转换结果存储在数据寄存器中时存储，并保留最近的16个转换结果数据。

下图显示了数据缓冲区、指针和溢出标志操作的示意图。当BUFEN位设置为1时，AD转换结果在AD转换的每一端传送。指针指示要写入下一个传输数据的数据缓冲区的编号。当数据写入缓冲区15时，指针复位为0000b，溢出标志设置为1。随后传输的数据将覆盖先前写入的数据。

通过将00h写入ADBUFPTR寄存器，溢出标志复位为初始值。

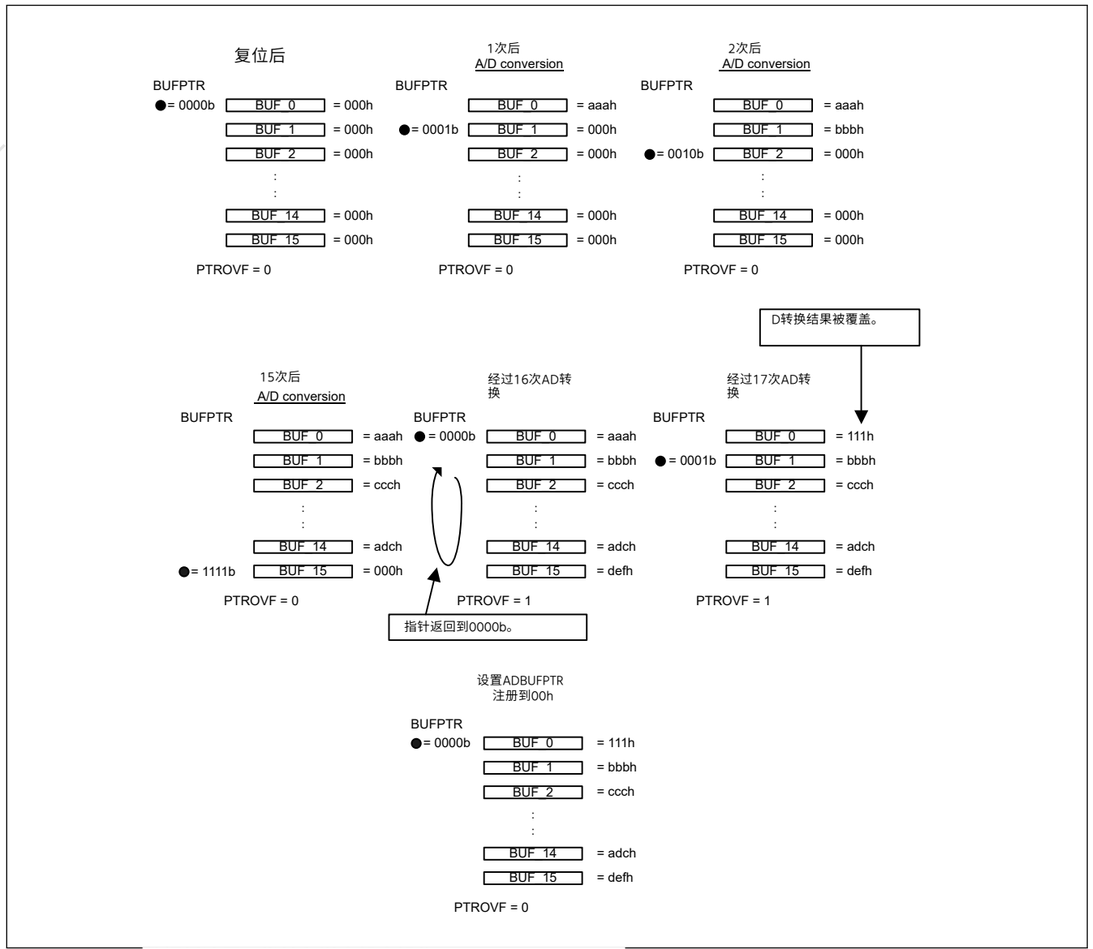


Figure 43.37 数据缓冲区、指针和溢出标志操作

43.4 Interrupt Sources and DTC, DMAC Transfer Requests

43.4.1 Interrupt Requests

The ADC12 can send scan end interrupt requests ADC12i_ADI (i = 0, 1) and ADC12i_GBADI (i = 0, 1) to the CPU. The ADC12 also generates the ADC12i_CMPAI (i = 0, 1)/ADC12i_CMPBI (i = 0, 1) interrupt for the CPU in response to matches with a condition for comparison.

An ADC12i_ADI (i = 0, 1) interrupt is always generated. An ADC12i_GBADI (i = 0, 1) interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC12i_CMPAI (i = 0, 1) and ADC12i_CMPBI (i = 0, 1) interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bit to 1.

In addition, the DTC or DMAC can be started when an ADC12i_ADI (i = 0, 1) or an ADC12i_GBADI (i = 0, 1) interrupt is generated. Using an ADC12i_ADI (i = 0, 1) or ADC12i_GBADI (i = 0, 1) interrupt to activate the DTC or DMAC to read the converted data enables continuous conversion without a burden on software.

Table 43.28 describes the interrupt sources and ELC events available for the ADC12.

Table 43.28 The interrupt source and ELC event of ADC12 (1 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare function Window A/B					
Single scan mode	Deselected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of single scan
		Selected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of single scan
			ADC12i_CMPAI (i = 0, 1)	✓	—	—	ADC12i_CMPAI (i = 0, 1) generated on a match comparison condition of Window A
			ADC12i_CMPBI (i = 0, 1)	✓	—	—	ADC12i_CMPBI (i = 0, 1) generated on a match comparison condition of Window B
			ADC12i_WCMPM (i = 0, 1)	—	✓	✓	ADC12i_WCMPM (i = 0, 1) generated on a match condition of the Window A/B compare function
			ADC12i_WCMPUM (i = 0, 1)	—	✓	✓	ADC12i_WCMPUM (i = 0, 1) generated on a mismatch condition of the Window A/B compare function
	Selected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of scans in the even numbered times
Continuous scan mode	Deselected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of scan of all selected channels
		Selected	ADC12i_CMPAI (i = 0, 1)	✓	—	—	ADC12i_CMPAI (i = 0, 1) generated on a match comparison condition of Window A
			ADC12i_CMPBI (i = 0, 1)	✓	—	—	ADC12i_CMPBI (i = 0, 1) generated on a match comparison condition of Window B

43.4 中断源和DTC、DMAC传输请求

43.4.1 中断请求

ADC12可以向CPU发送扫描结束中断请求ADC12i_ADI(i=0 1)和ADC12i_GBADI(i=0 1)。这
ADC12还为CPU生成ADC12i_CMPAI(i=0 1)ADC12i_CMPBI(i=0 1)中断，以响应与比较条件的匹配。

始终会产生ADC12i_ADI(i=0 1)中断。ADC12i_GBADI(i=0 1)中断可以通过将ADCSR.GBADIE位设置为1来产生。类似地，ADC12i_CMPAI(i=0 1)和ADC12i_CMPBI(i=0 1)中断可以通过设置ADCMPCR来产生.CMPAIE和ADCMPCR.CMPBIE位为1。

此外，当ADC12i_ADI(i=0 1)或ADC12i_GBADI(i=0 1)中断产生时，可以启动DTC或DMAC。使用ADC12i_ADI(i=0 1)或ADC12i_GBADI(i=0 1)中断来激活DTC或DMAC以读取转换后的数据可实现连续转换，而无需软件负担。

表43.28描述了ADC12可用的中断源和ELC事件。

Table 43.28 ADC12的中断源和ELC事件（1of2）

Operation			中断请求或ELC事件	中断请求	DTC或DMAC激活	ELC事件请求	Function
扫描模式	双触发模式	比较函数窗口AB					
单次扫描模式	Deselected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在单次扫描结束时生成
		Selected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在单次扫描结束时生成
			ADC12i_CMPAI (i = 0, 1)	✓	—	—	在窗口A的匹配比较条件下生成的ADC12i_CMPAI(i=0 1)
			ADC12i_CMPBI (i = 0, 1)	✓	—	—	在窗口B的匹配比较条件下生成的ADC12i_CMPBI(i=0 1)
			ADC12i_WCMPM (i = 0, 1)	—	✓	✓	ADC12i_WCMPM(i=0 1)在窗口AB比较功能的匹配条件下生成
			ADC12i_WCMPUM (i = 0, 1)	—	✓	✓	ADC12i_WCMPUM(i=0 1)在窗口AB比较功能的不匹配条件下生成
	Selected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在偶数次扫描结束时生成
连续扫描模式	Deselected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在所有选定通道的扫 描结束时生成
		Selected	ADC12i_CMPAI (i = 0, 1)	✓	—	—	在窗口A的匹配比较条件下生成的ADC12i_CMPAI(i=0 1)
			ADC12i_CMPBI (i = 0, 1)	✓	—	—	在窗口B的匹配比较条件下生成的ADC12i_CMPBI(i=0 1)

Table 43.28 The interrupt source and ELC event of ADC12 (2 of 2)

Operation			Interrupt request or ELC event	Interrupt request	DTC or DMAC activation	ELC event request	Function
Scan mode	Double trigger mode	Compare function Window A/B					
Group scan mode	Deselected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of group A scan
			ADC12i_GBADI (i = 0, 1)	✓	✓	—	ADC12i_GBADI (i = 0, 1) dedicated to group B generated at the end of group B scan
		Selected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of group A scan
			ADC12i_GBADI (i = 0, 1)	✓	✓	—	ADC12i_GBADI (i = 0, 1) dedicated to group B generated at the end of group B scan
			ADC12i_CMPAI (i = 0, 1)	✓	—	—	ADC12i_CMPAI (i = 0, 1) generated on a match comparison condition of Window A
			ADC12i_CMPBI (i = 0, 1)	✓	—	—	ADC12i_CMPBI (i = 0, 1) generated on a match comparison condition of Window B
	Selected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI (i = 0, 1) generated at the end of group A scans in the even-numbered times
			ADC12i_GBADI (i = 0, 1)	✓	✓	—	ADC12i_GBADI (i = 0, 1) dedicated to group B generated at the end of group B scan

Note: ✓ available
—: unavailable

For details on DTC settings, see section 17, Data Transfer Controller (DTC).

43.5 Event Link Function

43.5.1 Event Output to the ELC

The ELC uses the ADC12i_ADI (i = 0, 1) interrupt request signal as an event signal ADC12i_ADI (i = 0, 1), enabling link operation for the preset module. The ADC12i_GBADI (i = 0, 1) interrupt and ADC12i_CMPAI (i = 0, 1)/ADC12i_CMPBI (i = 0, 1) interrupts cannot be used as an event signal. For details, see Table 43.28.

An event signal can be output regardless of the settings of the corresponding interrupt request enable bits. For the scan end event(ADC12i_ADI (i = 0, 1)), a high-level pulse for one PCLKA cycle is output at the same output timing as the interrupt output (ADC12i_ADI (i = 0, 1)) shown in Table 43.28. For a compare match (ADC12i_WCMPM (i = 0, 1)) and mismatch event (ADC12i_WCMPUM (i = 0, 1)) to the ELC, a high-level pulse for one PCLKA cycle is output at the timing delayed by one cycle (PCLKA) from the interrupt output (ADC12i_ADI (i = 0, 1)) shown in Table 43.28.

To use compare match (ADC12i_WCMPM (i = 0, 1)) or mismatch event (ADC12i_WCMPUM (i = 0, 1)) to the ELC, specify single-scan mode.

43.5.2 ADC12 Operation through an Event from the ELC

The ADC12 can start A/D conversion by the preset event specified in the ELSRn settings for the ELC as follows:

- Select the ELC_AD00 (unit 0) signal in the ELC.ELSR8 register
- Select the ELC_AD01 (unit 0) signal in the ELC.ELSR9 register

Table 43.28 ADC12的中断源和ELC事件(2of2)

Operation			中断请求或ELC事件	中断请求	DTC或DMAC激活	ELC事件请求	Function
扫描模式	双触发模式	比较函数窗口AB					
组扫描模式	Deselected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在A组扫描结束时生成
			ADC12i_GBADI (i = 0, 1)	✓	✓	—	ADC12i_GBADI(i=0 1)专用于在B组扫描结束时生成的B组
		Selected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在A组扫描结束时生成
			ADC12i_GBADI (i = 0, 1)	✓	✓	—	ADC12i_GBADI(i=0 1)专用于在B组扫描结束时生成的B组
			ADC12i_CMPAI (i = 0, 1)	✓	—	—	在窗口A的匹配比较条件下生成的ADC12i_CMPAI(i=0 1)
			ADC12i_CMPBI (i = 0, 1)	✓	—	—	在窗口B的匹配比较条件下生成的ADC12i_CMPBI(i=0 1)
	Selected	Deselected	ADC12i_ADI (i = 0, 1)	✓	✓	✓	ADC12i_ADI(i=0 1)在偶数次扫描A组结束时生成
			ADC12i_GBADI (i = 0, 1)	✓	✓	—	ADC12i_GBADI(i=0 1)专用于在B组扫描结束时生成的B组

Note: 可用—：不可用

有关DTC设置的详细信息，请参阅第17节，数据传输控制器(DTC)。

43.5 事件链接功能

43.5.1 事件输出到ELC

ELC使用ADC12i_ADI(i=0 1)中断请求信号作为事件信号ADC12i_ADI(i=0 1)，启用预设模块的链接操作。ADC12i_GBADI(i=0 1)中断和ADC12i_CMPAI(i=0 1)ADC12i_CMPBI(i=0 1)中断不能用作事件信号。详见表43.28。

无论相应中断请求使能位的设置如何，都可以输出事件信号。对于扫描结束事件（ADC12i_ADI(i=0 1)），在与表43.28所示的中断输出（ADC12i_ADI(i=0 1)）相同的输出时序上输出一个PCLKA周期的高电平脉冲.对于到ELC的比较匹配(ADC12i_WCMPM(i=0 1))和失配事件(ADC12i_WCMPUM(i=0 1))，在延迟一个周期的时序上输出一个PCLKA周期的高电平脉冲(PCLKA)来自表43.28所示的中断输出(ADC12i_ADI(i=0 1))。

要将比较匹配(ADC12i_WCMPM(i=0 1))或不匹配事件(ADC12i_WCMPUM(i=0 1))用于ELC，请指定单扫描模式。

43.5.2 ADC12通过来自ELC的事件进行操作

ADC12可以通过ELC的ELSRn设置中指定的预设事件启动AD转换，如下所示：

●选择ELC.ELSR8寄存器中的ELC_AD00（单元0）信号

●选择ELC.ELSR9寄存器中的ELC_AD01（单元0）信号

- Select the ELC_AD10 (unit 1) signal in the ELC.ELSR10 register
- Select the ELC_AD11 (unit 1) signal in the ELC.ELSR11 register.

If an ELC event occurs during A/D conversion, the event is disabled.

43.6 Usage Notes

43.6.1 Constraints on Setting the Registers

Set each register while the ADCSR.ADST bit is 0.

43.6.2 Constraints on Reading the Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Register
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register
- A/D Data Buffer Registers n (N = 0 to 15)

If a register is read twice in byte units, that is, the upper byte and lower byte are read separately, the A/D-converted value read initially might disagree with the A/D-converted value read subsequently. To prevent this, never read the data registers in byte units.

43.6.3 Constraints on Stopping A/D Conversion

(1) A/D Conversion Stop Procedure

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure shown in Figure 43.38.

●选择ELC.ELSR10寄存器中的ELC_AD10（单元1）信号
●选择ELC.ELSR11寄存器中的ELC_AD11（单元1）信号。

如果在AD转换期间发生ELC事件，则该事件被禁用。

43.6 使用说明

43.6.1 设置寄存器的限制

当ADCSR.ADST位为0时设置每个寄存器。

43.6.2 读取数据寄存器的限制

以下寄存器必须以半字为单位读取：

●AD数据寄存器
●AD数据双工寄存器
●AD数据双工寄存器A
●AD数据双工寄存器B
●AD温度传感器数据寄存器
●AD内部参考电压寄存器
●AD自诊断数据寄存器
●AD数据缓冲寄存器n(N=0to15)

如果以字节为单位读取寄存器两次，即分别读取高字节和低字节，则最初读取的AD转换值可能与随后读取的AD转换值不一致。为防止这种情况，切勿以字节为单位读取数据寄存器。

43.6.3 停止AD转换的约束

(1) AD转换停止程序

TostopADconversionwhenanasynchronoustriggerorasynchronoustriggerisselectedastheconditionforstartingADconversion followtheprocedureshowninFigure43.38.

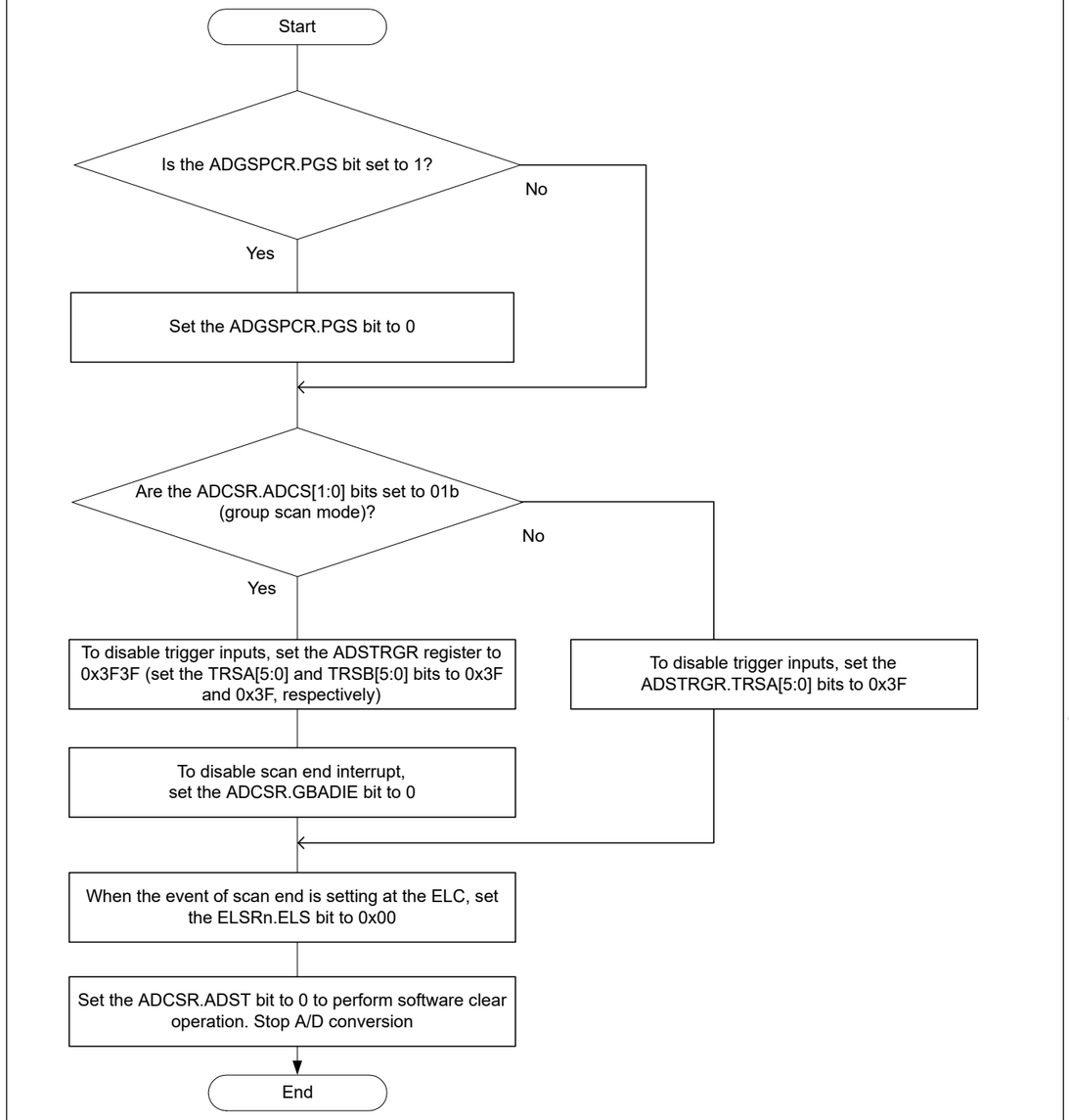


Figure 43.38 Procedures for clearing the ADCSR.ADST bit by software

To specify the following settings after performing the clear operation by software, provide a wait period for at least two ADCLK cycles.

- Enabling scan end interrupts
- Enabling scan end events for the event link controller
- Starting A/D conversion by software
- Enabling trigger input

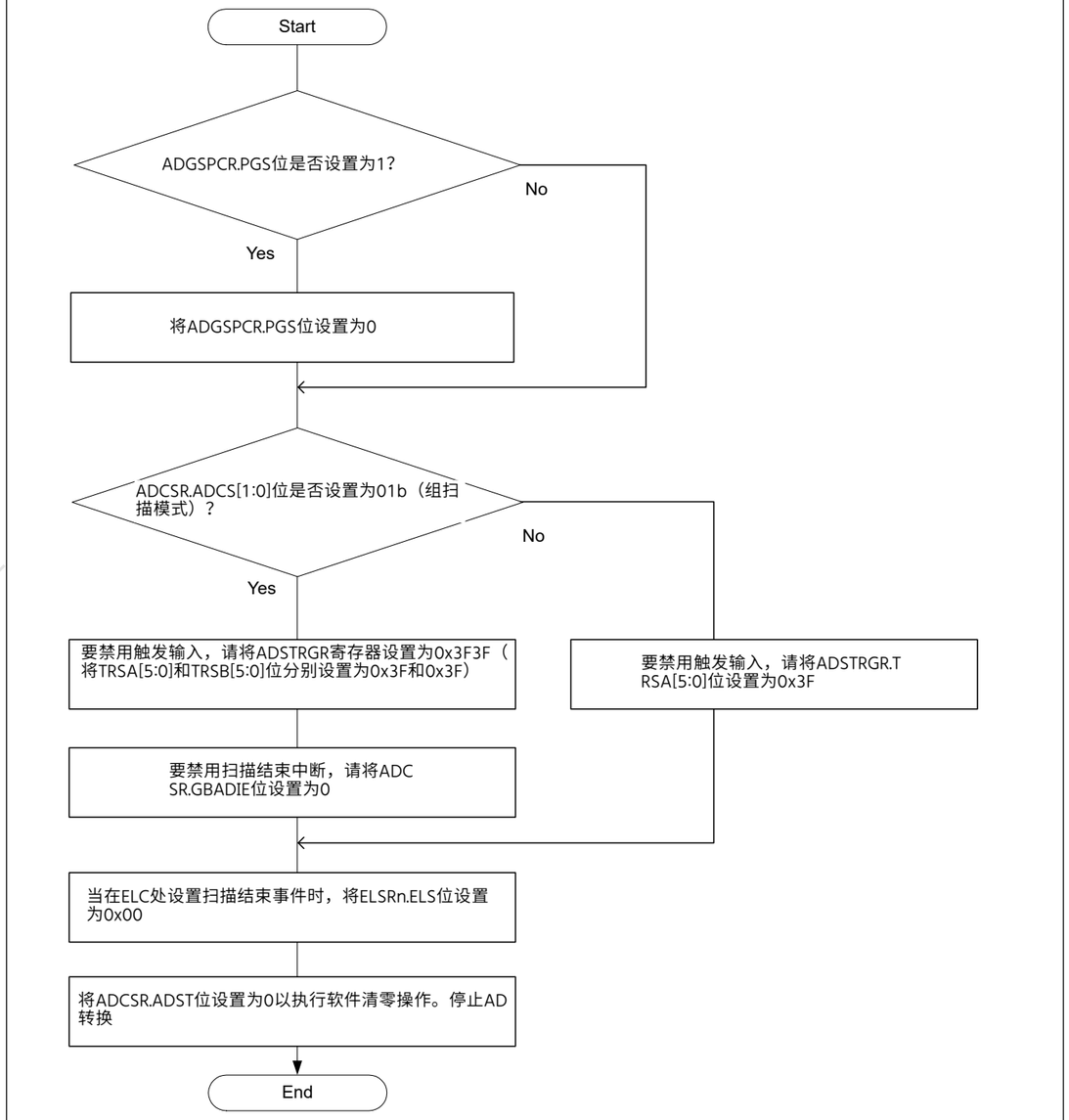


Figure 43.38 通过软件清除ADCSR.ADST位的程序

要在通过软件执行清除操作后指定以下设置，请提供至少两个等待时间ADCLK cycles.

- 启用扫描结束中断
- 为事件链接控制器启用扫描结束事件
- 通过软件启动AD转换
- 启用触发输入

(2) Notes on Modes and Status Bits

If necessary, individually initialize or set again the voltage status for self-diagnosis, the judgment of the even number or odd number specified for double-trigger mode, and the monitor flags of the compare function.

- To set again the voltage status for self-diagnosis, set the ADCER.DIAGLD bit to 1 and then set a desired value in the ADCER.DIAGVAL[1:0] bits.
- If the setting of the ADCSR.DBLE bit is changed from 0 to 1, the double-trigger mode operation starts from the first scanning.
- To initialize the monitor flags of the compare function (MONCMPA, MONCMPB, and MONCOMB), set the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits to 0.

43.6.4 A/D Conversion Restart and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit of the ADC12 to restart on setting the ADCSR.ADST bit to 1. A maximum of 2 ADCLK cycles is required for the operating analog unit of the ADC12 to terminate on setting the ADCSR.ADST bit to 0.

43.6.5 Constraints on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data. This occurs when the CPU does not complete the reading of the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

43.6.6 Settings for the Module-Stop Function

The Module Stop Control Register can enable or disable ADC12 operation. The ADC12 is initially stopped after a reset. The registers become accessible on release from the module-stop state. After release from the module-stop state, wait for at least 1 µs before starting A/D conversion. For details, see section 10, Low Power Modes.

43.6.7 Notes on Entering the Low-Power States

Before entering the module-stop state or Software Standby mode, be sure to stop A/D conversion. Set the ADCSR.ADST bit in ADCSR to 0 and secure a period of time until the analog unit of the ADC12 stops. Follow the procedure shown in Figure 43.38 to clear the ADCSR.ADST bit with software. Then, wait for 2 clock cycles of ADCLK before entering the module-stop state or Software Standby mode.

43.6.8 Error in Absolute Accuracy When Disconnection Detection Assistance Is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the ADC12. This error arises because an erroneous voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull- down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula:

$$\text{Maximum error in absolute accuracy (LSB)} = \left(2^{\text{Resolution}} - 1\right) \times \text{Rs} / \left(\text{Rs} + \text{Rp}\right)$$

Only use disconnection detection assistance after thorough evaluation.

43.6.9 Constraints on Operating Modes and Status Bits

Initialize or set again individually, if necessary, the voltage values in self-diagnosis, the value of the first scan or second scan in double trigger mode, the data buffer pointer, and status monitor in the compare function.

- Select the voltage values in self-diagnosis (ADCER.DIAGVAL[1:0]) after setting ADCER.DIAGLD to 1.
- Double-trigger mode operates as the first scan after setting ADCSR.DBLE from 0 to 1.
- The status monitor bits (MONCMPA, MONCMPB, MONCOMB) in the compare function are initialized after setting ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0.

(2) 模式和状态位注意事项

如有必要，单独初始化或重新设置电压状态以进行自诊断、双触发模式指定的偶数或奇数判断以及比较功能的监视标志。

●要再次设置自诊断的电压状态，请将ADCER.DIAGLD位设置为1，然后在ADCER.DIAGVAL[1:0]位中设置所需的值。

●如果ADCSR.DBLE位的设置从0变为1，则双触发模式操作从第一次扫描开始。

●要初始化比较函数的监控标志（MONCMPA、MONCMPB和MONCOMB），请将ADCMPCR.CMPAE和ADCMPCR.CMPBE位设置为0。

43.6.4 AD转换重启和终止时序

ADC12的空闲模拟单元最多需要6个ADCLK周期才能在将ADCSR.ADST位设置为1时重新启动。ADC12的操作模拟单元需要最多2个ADCLK周期才能在设置ADCSR时终止.ADST位为0。

43.6.5 扫描结束中断处理的约束

当使用任何触发器扫描相同的模拟输入两次时，第一个AD转换数据将被第二个AD转换数据覆盖。当CPU在

在产生第一次扫描结束中断后，第二次扫描的第一个模拟输入的D转换结束。

43.6.6 模块停止功能的设置

模块停止控制寄存器可以启用或禁用ADC12操作。ADC12在复位后最初停止。
寄存器在从模块停止状态释放时变得可访问。从模块停止状态释放后，至少等待1µs再开始AD转换。有关详细信息，请参阅第10节，低功耗模式。

43.6.7 进入低功耗状态的注意事项

在进入模块停止状态或软件待机模式之前，请务必停止AD转换。将ADCSR中的ADCSR.ADST位设置为0，并确保一段时间，直到ADC12的模拟单元停止。按照图43.38所示的过程用软件清零ADCSR.ADST位。然后，在进入模块停止状态或软件待机模式之前等待ADCLK的2个时钟周期。

43.6.8 使用断线检测辅助时的绝对精度误差

使用断开检测辅助会导致ADC12的绝对精度出现误差。由于上拉或下拉电阻(Rp)与信号源电阻(Rs)之间的电阻分压，导致错误电压输入到模拟输入引脚，因此会出现此错误。该绝对精度误差由以下公式计算得出：

绝对精度的最大误差(LSB)=2分辨率 1×RsRs+Rp)

仅在全面评估后使用断线检测辅助。

43.6.9 操作模式和状态位的限制

必要时单独初始化或重新设置自诊断中的电压值、双触发模式下的第一次扫描或第二次扫描的值、数据缓冲区指针和比较功能中的状态监视器。

●设置ADCER.DIAGLD为1后，选择自诊断中的电压值（ADCER.DIAGVAL[1:0]）。

●双触发模式在将ADCSR.DBLE从0设置为1后作为第一次扫描运行。

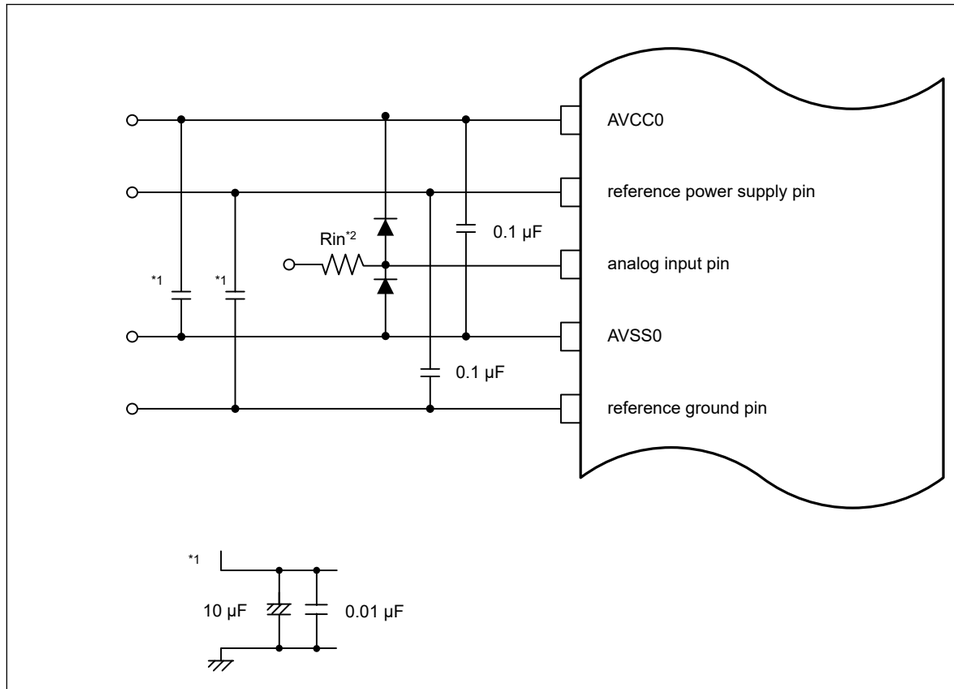
●比较功能中的状态监控位（MONCMPA、MONCMPB、MONCOMB）在设置ADCMPCR.CMPAE和ADCMPCR.CMPBE为0后被初始化。

43.6.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or be placed near each other. If these rules are not followed, noise can occur on analog signals and A/D conversion accuracy is affected. The analog input pins, reference power supply pin (VREFH0, VREFH), reference ground pin (VREFL0, VREFL), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

43.6.11 Constraints on Noise Prevention

To prevent the analog input pins from being destroyed by abnormal voltage such as excessive surge, insert a capacitor between AVCC0 and AVSS0 and between VREFH0 and VREFL0 and between VREFH and VREFL. Additionally, connect a protection circuit to protect the analog input pins as shown in Figure 43.39.



Note 1. The values shown here are reference values.
Note 2. Rin: Signal source impedance

Figure 43.39 Example protection circuit for analog inputs

43.6.12 Port Settings When Using the ADC12 Input

When using the high-precision channels, do not use PORT0 as general I/O. Renesas recommends that you do not use the digital output that is also used as the AD analog input if normal-precision channel is used. If the digital output that is also used as the AD analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

43.6.13 Notes on Canceling Software Standby Mode

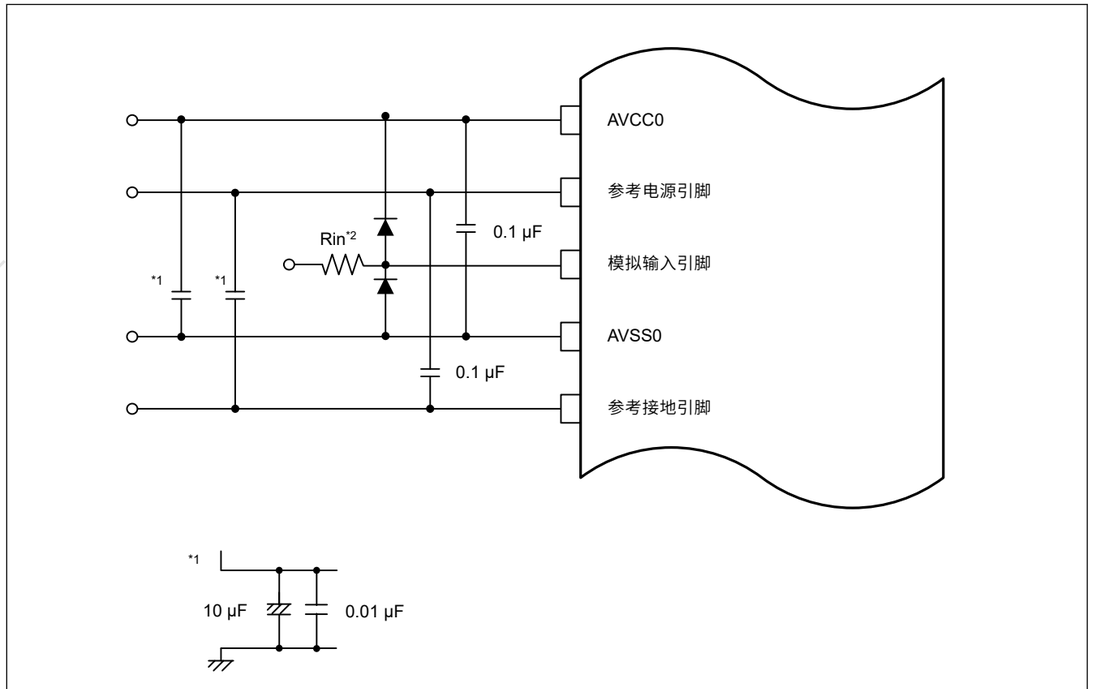
After software standby mode is canceled, wait at least 1 µs after the stabilization time for the oscillator elapses and before starting A/D conversion. For details, see section 10, Low Power Modes

43.6.10 电路板设计注意事项

电路板的设计应使数字电路和模拟电路尽可能分开。此外，数字电路信号线和模拟电路信号线不应交叉或靠近。如果不遵守这些规则，模拟信号上可能会出现噪声，影响AD转换精度。模拟输入引脚、参考电源引脚(VREFH0、VREFH)、参考接地引脚(VREFL0、VREFL)和模拟电源(AVCC0)应与使用模拟接地(AVSS0)的数字电路分开。模拟接地(AVSS0)应连接到板上的稳定数字接地(VSS)（单点接地层连接）。

43.6.11 防止噪音的限制

为防止模拟输入引脚被过大浪涌等异常电压损坏，请在AVCC0和AVSS0之间、VREFH0和VREFL0之间以及VREFH和VREFL之间插入一个电容器。此外，连接保护电路以保护模拟输入引脚，如图43.39所示。



注1.此处显示的值为参考值。
注2.Rin：信号源阻抗

Figure 43.39 模拟输入保护电路示例

43.6.12 使用ADC12输入时的端口设置

使用高精度通道时，请勿将PORT0用作通用IO。如果使用普通精度通道，瑞萨建议您不要使用同时用作AD模拟输入的数字输出。如果同时用作AD模拟输入的数字输出用于输出信号，则进行数次A/D转换，消除最大值和最小值，取其他结果的平均值。

43.6.13 关于取消软件待机模式的注意事项

取消软件待机模式后，在振荡器的稳定时间过去后至少等待1µs，然后再开始AD转换。有关详细信息，请参阅第10节，低功耗模式

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43.6.14 Calculation for sampling time

The sampling time can be easily estimated by the following figure and formula. This is the time to reach the voltage within 1/4 LSB.

$t_{SPL} = (R_{EXT} + R_{AD}) \times (C_{EXT} + C_{AD}) \times \ln (C_{AD} / (C_{EXT} + C_{AD}) \times 2^{N+2})$

R_{EXT} shows external signal source impedance
C_{EXT} shows external capacitance (pin capacitance*1 + PCB parasitic capacitance)
N = 12, 10 or 8 (conversion resolution)
C_{AD} = 5 pF (internal capacitance)
R_{AD} = 1.0 kΩ (internal resistance, case of high-speed channels)
R_{AD} = 2.0 kΩ (internal resistance, case of normal-speed channels)

Note 1. Typical value of analog input pin is 5 pF

For example, if R_{EXT} is 1 kΩ, C_{EXT} is 10 pF and N is 12 bits, t_{SPL} of high-speed channel is 258 ns.

This formula simplifies the general use case. This formula is not guaranteed and should be used only for estimation.

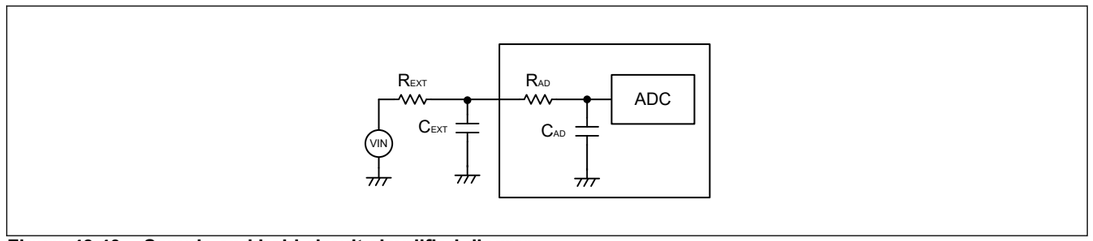

Figure 43.40 Sample and hold circuit simplified diagram

43.6.14 采样时间计算

采样时间可以通过下图和公式轻松估算。这是在14LSB内达到电压的时间。

tSPL=(REXT+RAD)×(CEXT+CAD)×ln(CAD(CEXT+CAD)×2N+2)

REXT显示外部信号源阻抗
CEXT表示外部电容（引脚电容*1+PCB寄生电容）
N = 12, 10 or 8 (conversion resolution)
C_{AD} = 5 pF (internal capacitance)
RAD=1.0kΩ（内部电阻，高速通道的情况）
RAD=2.0kΩ（内部电阻，正常速度通道的情况）

注1.模拟输入引脚的典型值为5pF

例如，如果REXT为1kΩ，CEXT为10pF，N为12位，则高速通道的tSPL为258ns。

此公式简化了一般用例。这个公式不能保证，只能用于估计。

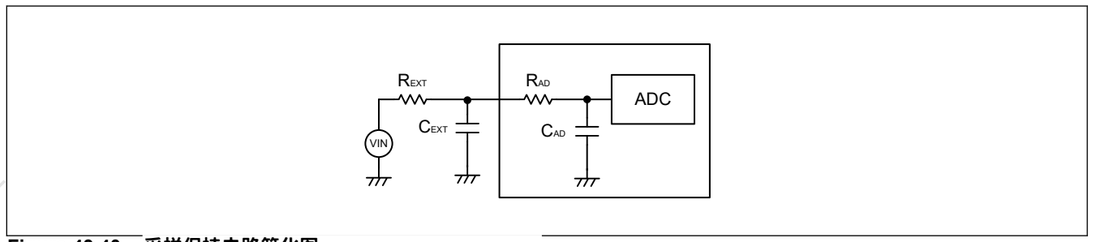

Figure 43.40 采样保持电路简化图

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44. 12-Bit D/A Converter (DAC12)

44.1 Overview

The MCU provides a 12-bit D/A Converter (DAC12) with an output amplifier. Table 44.1 lists the DAC12 specifications, Figure 44.1 shows a block diagram, and Table 44.2 lists the I/O pins.

Table 44.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
Output channels	2 channels
Interference reduction between analog modules	Methods provided to minimize interference between D/A and A/D conversion: • D/A converted data update timing is controlled by the synchronous D/A conversion enable input signal from the ADC12 (unit 1) • Degradation of A/D conversion accuracy caused by interference is reduced by controlling the DAC12 inrush current generation timing with the enable signal.
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	The DA0 and DA1 conversion can be started on input of an event signal
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used
TrsutZone Filter	Security attribution can be set

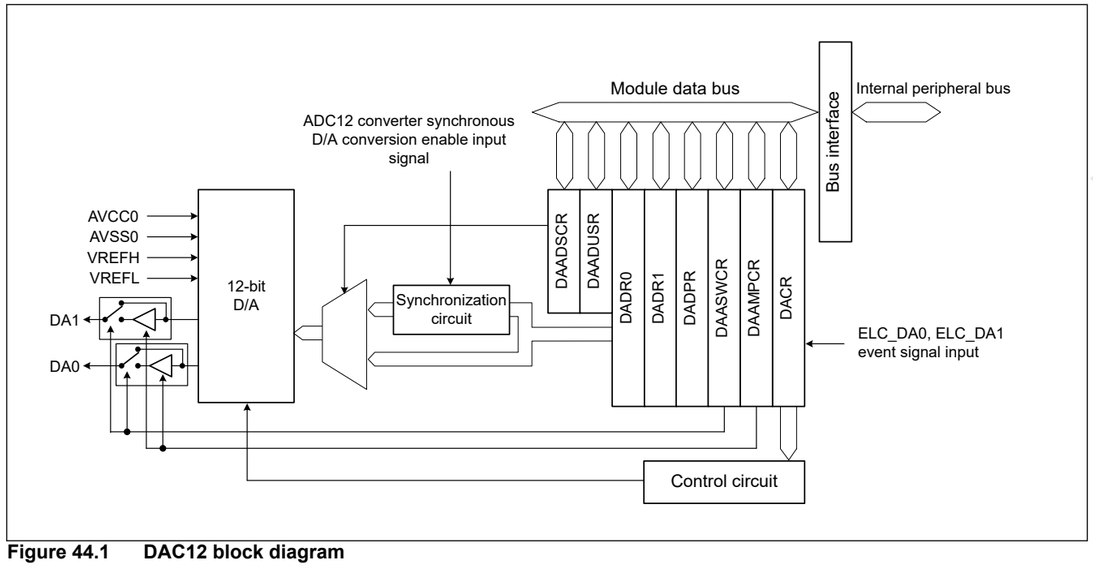

Figure 44.1 DAC12 block diagram

Table 44.2 lists the pin configuration of the DAC12.

Table 44.2 DAC12 I/O pins (1 of 2)

Pin name	I/O	Function
AVCC0	Input	• Analog power and analog reference top voltage supply pin for ADC12 and DAC12. • Connect to VCC when these modules are not used.
AVSS0	Input	• Analog ground and analog reference ground supply pin for ADC12 and DAC12. • Connect to VSS when these modules are not used.
VREFH	Input	Analog reference top voltage supply pin for the ADC12 (unit 1) and the DAC12
VREFL	Input	Analog reference ground pin for the ADC12 (unit 1) and the DAC12

44. 12-Bit D/A Converter (DAC12)

44.1 Overview

MCU提供带输出放大器的12位DA转换器(DAC12)。表44.1列出了DAC12规格，
图44.1显示了框图，表44.2列出了IO引脚。

Table 44.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
输出通道	2 channels
减少模拟模块之间的干扰	为尽量减少DA和AD转换之间的干扰提供的方法：● DA转换数据更新时序由来自ADC12（单元1）的同步DA转换使能输入信号控制 • 通过使能信号控制DAC12浪涌电流的产生时序，可以减少由干扰引起的AD转换精度下降。
Module-stop function	可设置模块停止状态以降低功耗
事件链接功能（输入）	DA0和DA1转换可以在输入事件信号时启动
DA输出放大器控制功能	控制是否使用输出放大器（用于放大器直通和放大器偏置控制）
TrsutZone Filter	可设置安全属性

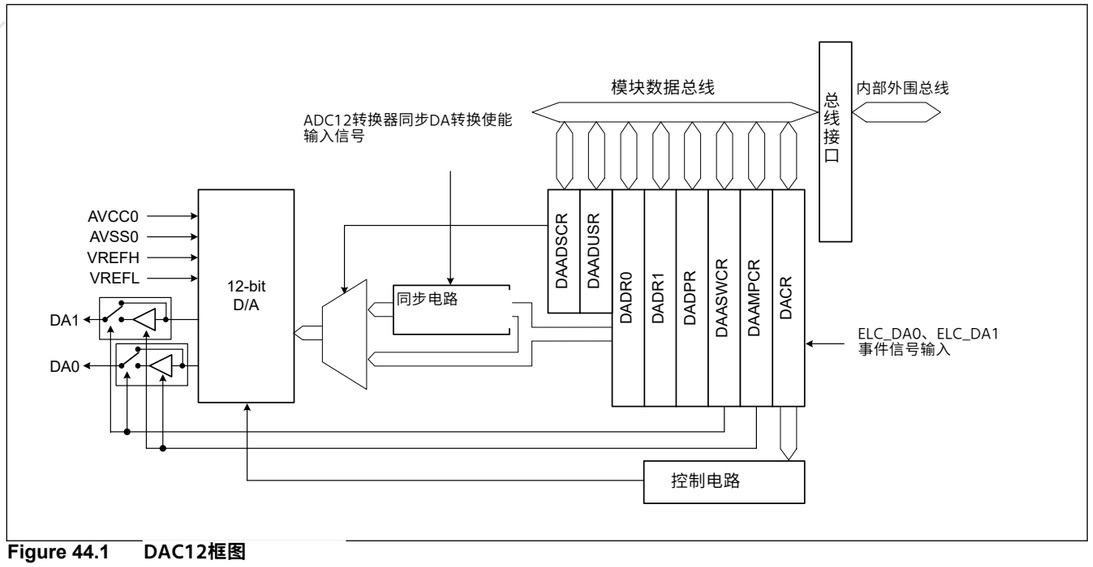

Figure 44.1 DAC12框图

表44.2列出了DAC12的引脚配置。

Table 44.2 DAC12IO引脚（2个中的1个）

引脚名称	I/O	Function
AVCC0	Input	• ADC12和DAC12的模拟电源和模拟参考最高电压电源引脚。 • 不使用这些模块时连接到VCC。
AVSS0	Input	• ADC12和DAC12的模拟地和模拟参考地电源引脚。 • 不使用这些模块时连接到VSS。
VREFH	Input	ADC12（单元1）和DAC12的模拟参考最高电压电源引脚
VREFL	Input	ADC12（单元1）和DAC12的模拟参考接地引脚

Table 44.2 DAC12 I/O pins (2 of 2)

Pin name	I/O	Function
DA0	Output	Channel 0 output pin for the analog signals processed by the DAC12
DA1	Output	Channel 1 output pin for the analog signals processed by the DAC12

44.2 Register Descriptions

44.2.1 DADRn : D/A Data Register n (n = 0, 1)

Base address: DAC12 = 0x4017_1000

Offset address: 0x00 + 0x02 × n

Bit position:	15															0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRn register is 16-bit read/write registers that store data for D/A conversion. When an analog output is enabled, the values in DADRn are converted and output to the analog output pins.

12-bit data can be formatted as left- or right-justified in the DADPR.DPSEL bit setting. In right-justified format (DADPR.DPSEL = 0), the lower 12 bits, [11:0], are valid. In left-justified format (DADPR.DPSEL = 1), the upper 12 bits, [15:4], are valid.

44.2.2 DACR : D/A Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAOE1	DAOE0	DAE	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	These bits are read as 1. The write value should be 1.	R/W
5	DAE*1	D/A Enable 0: Control D/A conversion of channels 0 and 1 individually 1: Control D/A conversion of channels 0 and 1 collectively	R/W
6	DAOE0	D/A Output Enable 0 0: Disable analog output of channel 0 (DA0) 1: Enable D/A conversion of channel 0 (DA0)	R/W
7	DAOE1	D/A Output Enable 1 0: Disable analog output of channel 1 (DA1) 1: Enable D/A conversion of channel 1 (DA1)	R/W

Note 1. This bit controls D/A conversion in combination with the DAOEi bit (i = 0, 1), which controls the output of the conversion results. For details, see Table 44.3.

Table 44.2 DAC12IO引脚（2个中的2个）

引脚名称	I/O	Function
DA0	Output	DAC12处理的模拟信号的通道0输出引脚
DA1	Output	DAC12处理的模拟信号的通道1输出引脚

44.2 注册说明

44.2.1 DADRn:DA数据寄存器n(n=0 1)

Base address: DAC12 = 0x4017_1000

Offset address: 0x00 + 0x02 × n

Bit position:	15															0
Bit field:																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRn寄存器是16位读写寄存器，用于存储用于DA转换的数据。当模拟输出使能时，DADRn中的值被转换并输出到模拟输出引脚。

在DADPR.DPSEL位设置中，12位数据可以被格式化为左对齐或右对齐。在右对齐格式(DADPR.DPSEL=0)中，低12位[11:0]有效。在左对齐格式(DADPR.DPSEL=1)中，高12位[15:4]有效。

44.2.2 DACR:DA控制寄存器

Base address: DAC12 = 0x4017_1000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAOE1	DAOE0	DAE	—	—	—	—	—
重置后的值:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	—	这些位被读取为1。写入值应为1。	R/W
5	DAE*1	D/A Enable 0：分别控制通道0和通道1的DA转换1：控制通道0和通道1的DA转换	R/W
6	DAOE0	DA输出使能0 0：禁用通道0（DA0）的模拟输出1：启用通道0（DA0）的DA转换	R/W
7	DAOE1	DA输出使能1 0：禁用通道1（DA1）的模拟输出1：启用通道1（DA1）的DA转换	R/W

注1.该位与DAOEi位(i=0 1)一起控制DA转换，DAOEi位控制转换结果的输出。详见表44.3。

Table 44.3 D/A conversion controls

DAE	DAOE1	DAOE0	Description
0	0	0	Disable D/A conversion and analog output pins (DA0, DA1)*1
		1	• Enable D/A conversion of channel 0 and disable D/A conversion of channel 1 • Enable analog output of channel 0 (DA0) and disable analog output of channel 1 (DA1)*1
	1	0	• Disable D/A conversion of channel 0 and enable D/A conversion of channel 1 • Disable analog output of channel 0 (DA0)*1 and enable analog output of channel 1 (DA1)
		1	• Enable D/A conversion of channels 0 and 1 • Enable analog output of channels 0 and 1 (DA0, DA1)
1	x	x	• Enable D/A conversion of channels 0 and 1 • Collective enable analog output of channels 0 and 1 (DA0, DA1)

Note: x: Don't care
Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

Only set this register while the ADC12 is halted when the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled). Only set DACR while the ADCSR.ADST bit is 0 and after selecting the software trigger, for the ADC12 trigger to securely stop the ADC12. This MCU only supports ADC12 (unit 1).

DAE bit (D/A Enable)

The DAE bit controls D/A conversion, amplifier operation, and analog output in combination with the DAOEi bit (i = 0, 1) and the DAMMPCR.DAAMPi bit (i = 0, 1). See Table 44.4.

When interference reduction between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the ADCSR.ADST bit of the ADC12 (unit 1) to 0. Then, select the software trigger for the ADC12 (unit 1) trigger to securely stop the ADC12 (unit 1).

DAOEi bit (D/A Output Enable i)

The DAOEi bit (i = 0, 1) controls D/A conversion, amplifier operation, and analog output in combination with the DAE bit and DAMMPCR.DAAMPi bit (i = 0, 1). See Table 44.4.

When both the DAOEi bit (i = 0, 1) and DAE bit are 0, D/A conversion of channel i (i = 0, 1) is not processed, and no conversion result is output.

When interference reduction between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the DAOEi bit while the ADCSR.ADST bit of the ADC12 (unit 1) is set to 0. Then, select the software trigger for the ADC12 (unit 1) trigger to securely stop the ADC12 (unit 1).

The event link function can be used to set the DAOEi bit to 1. The DAOE0 bit is set to 1 when the event specified in the ELSR12 register of the ELC (ELC_DA0 event) occurs, and output of the D/A conversion results starts. The DAOE1 bit is set to 1 when the event specified in the ELSR13 register of the ELC (ELC_DA1 event) occurs, and output of the D/A conversion results starts.

Table 44.4 D/A conversion and analog output control (1 of 2)

DACR		DAAMPCR	Channel i operation	Amplifier operation of channel i	Analog output of channel i
DAE	DAOEi	DAAMPi			
0	0	0	Stop	Stop	Hi-Z
		1	Stop	Stop	Hi-Z
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output

Table 44.3 DA转换控制

DAE	DAOE1	DAOE0	Description
0	0	0	禁用DA转换和模拟输出引脚(DA0 DA1)*1
		1	• 启用通道0的DA转换和禁用通道1的DA转换 • 启用通道0(DA0)的模拟输出和禁用通道1(DA1)的模拟输出*1
	1	0	• 禁用通道0的DA转换，启用通道1的DA转换 • 禁用通道0(DA0)*1的模拟输出并启用通道1(DA1)的模拟输出
		1	• 启用通道0和1的DA转换 • 启用通道0和1（DA0、DA1）的模拟输出
1	x	x	• 启用通道0和1的DA转换 • 通道0和1（DA0、DA1）的集体启用模拟输出

Note: x: Don't care
注1.当模拟输出禁用时，模拟输出信号置于Hi-Z状态。

仅当DAADSCR.DAADST位为1时ADC12停止时才设置此寄存器（之间的干扰减少DA和AD转换已启用）。只有在ADCSR.ADST位为0且选择软件触发后设置DACR，ADC12触发才能安全停止ADC12。此MCU仅支持ADC12（单元1）。

DAE位（DA启用）

DAE位与DAOEi位(i=0 1)和DAMMPCR.DAAMPi位(i=0 1)一起控制DA转换、放大器操作和模拟输出。见表44.4。

当启用DA和AD转换之间的干扰减少(DAADSCR.DAADST=1)时，设置ADC12（单元1）的ADCSR.ADST位为0。然后，选择ADC12（单元1）触发的软件触发以安全停止ADC12（单元1）。

DAOEi位（DA输出使能i）

DAOEi位(i=0 1)与DAE位和DAMMPCR.DAAMPi位(i=0 1)一起控制DA转换、放大器操作和模拟输出。见表44.4。

当DAOEi位(i=0 1)和DAE位均为0时，通道i(i=0 1)的DA转换不进行处理，也不输出转换结果。

当启用DA和AD转换之间的干扰降低时（DAADSCR.DAADST=1），设置DAOEi位，同时将ADC12（单元1）的ADCSR.ADST位设置为0。然后，选择ADC12的软件触发（单元1)触发以安全地停止ADC12（单元1）。

事件链接功能可用于将DAOEi位设置为1。当在发生ELC（ELC_DA0事件）的ELSR12寄存器，开始输出DA转换结果。当发生ELC的ELSR13寄存器中指定的事件（ELC_DA1事件）时，DAOE1位设置为1，并开始输出DA转换结果。

Table 44.4 DA转换和模拟输出控制(1of2)

DACR		DAAMPCR	通道i操作	通道i的放大器操作	通道i的模拟输出
DAE	DAOEi	DAAMPi			
0	0	0	Stop	Stop	Hi-Z
		1	Stop	Stop	Hi-Z
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	放大器输出

Table 44.4 D/A conversion and analog output control (2 of 2)

DACR		DAAMPCR	Channel i operation	Amplifier operation of channel i	Analog output of channel i
DAE	DAOEi	DAAMPi			
1	0	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output

Note: i = 0, 1

44.2.3 DADPR : DADRn Format Select Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	DPSEL	DADRn Format Select 0: Right-justified format 1: Left-justified format	R/W

44.2.4 DAADSCR : D/A A/D Synchronous Start Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	These bits are read as 0. The write value should be 0.	R/W
7	DAADST	D/A A/D Synchronous Conversion 0: Do not synchronize DAC12 with ADC12 (unit 1) operation (disable interference reduction between D/A and A/D conversion). 1: Synchronize DAC12 with ADC12 (unit 1) operation (enable interference reduction between D/A and A/D conversion).	R/W

To minimize interference between D/A and A/D conversion, the DAADSCR register enables synchronization of the start timing of D/A conversion with the ADC12 synchronous D/A conversion enable input signal.

Only set this register while the ADC12 (unit 1) is halted, that is, while the ADCSR.ADST bit is 0 after selecting the software trigger as the ADC12 (unit 1) trigger.

Select unit 1 as the target ADC12 unit before setting the DAADST bit to 1. Set DAADUSR[1] bit to 1 to select unit 1. This MCU only supports ADC12 unit 1.

Table 44.4 DA转换和模拟输出控制(2of2)

DACR		DAAMPCR	通道i操作	通道i的放大器操作	通道i的模拟输出
DAE	DAOEi	DAAMPi			
1	0	0	Run	Stop	Amplifier-through
		1	Run	Run	放大器输出
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	放大器输出

Note: i = 0, 1

44.2.3 DADPR:DADRn格式选择寄存器

Base address: DAC12 = 0x4017_1000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DPSEL	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	DPSEL	DADRn格式选择 0: Right-justified format 1: Left-justified format	R/W

44.2.4 DAADSCR:DAAD同步启动控制寄存器

Base address: DAC12 = 0x4017_1000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAADST	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
6:0	—	这些位被读取为0。写入值应为0。	R/W
7	DAADST	DAAD同步转换 0：不将DAC12与ADC12（单元1）操作同步（禁用DA和AD转换之间的干扰降低）。 1：DAC12与ADC12（单元1）操作同步（启用DA和AD转换之间的干扰降低）。	R/W

为了尽量减少DA和AD转换之间的干扰，DAADSCR寄存器使DA转换的开始时序与ADC12同步DA转换使能输入信号同步。

仅在ADC12（单元1）停止时设置该寄存器，即选择软件触发作为ADC12（单元1）触发后ADCSR.ADST位为0。

在将DAADST位设置为1之前选择单元1作为目标ADC12单元。将DAADUSR[1]位设置为1以选择单元1。这MCU仅支持ADC12单元1。

DAADST bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRn register value to be converted into analog data at any time. Setting the DAADST bit to 1 allows synchronization of D/A conversion with the synchronous D/A conversion enable input signal from the ADC12 (unit 1). With this bit set, D/A conversion does not start until the ADC12 (unit 1) completes A/D conversion, even when the DADRn register is changed.

Set this bit while the ADCSR.ADST bit is set to 0. Then, select the software trigger for the ADC12 (unit 1) trigger to securely stop the ADC12 (unit 1). Set the DAADUSR.AMADSEL1 bit to 1 before setting the DAADST bit to 1.

The event link function cannot be used when the DAADST bit is set to 1. Stop the event link function by setting the ELSR12 and ELSR13 registers of the ELC. The setting of the DAADST bit is shared by channels 0 and 1 of the DAC12.

44.2.5 DAAMPCR : D/A Output Amplifier Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAAMP1	DAAMP0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	DAAMP0	Amplifier Control 0 0: Do not use channel 0 output amplifier 1: Use channel 0 output amplifier	R/W
7	DAAMP1	Amplifier Control 1 0: Do not use channel 1 output amplifier 1: Use channel 1 output amplifier	R/W

The DAAMPCR register selects D/A output with or without using the amplifier.

DAAMP0 bit (Amplifier Control 0)

When the DAAMP0 bit is 0, analog values are output for D/A output of channel 0 without using the amplifier. When the DAAMP0 bit is 1, analog values are output for D/A output of channel 0 through the amplifier.

When both the DACR.DAE and DACR.DAOE0 bits are 0, the amplifier is not used regardless of the setting of the DAAMP0 bit. See Table 44.4 for details.

DAAMP1 bit (Amplifier Control 1)

When the DAAMP1 bit is 0, analog values are output for D/A output of channel 1 without using the amplifier. When the DAAMP1 bit is 1, analog values are output for D/A output of channel 1 through the amplifier.

When both the DACR.DAE and DACR.DAOE1 bits are 0, the amplifier is not used regardless of the setting of the DAAMP1 bit. See Table 44.4 for details.

44.2.6 DAASWCR : D/A Amplifier Stabilization Wait Control Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAASW1	DAASW0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

DAADST位（DAAD同步转换）

将DAADST位设置为0可以随时将DADRn寄存器值转换为模拟数据。设置DAADST位为1允许DA转换与来自ADC12（单元1）的同步DA转换使能输入信号同步。设置该位后，在ADC12（单元1）完成AD转换之前，即使DADRn寄存器发生更改，DA转换也不会开始。

在ADCSR.ADST位设置为0时设置该位。然后，选择ADC12（单元1）触发器的软件触发器以安全地停止ADC12（单元1）。在将DAADST位设置为1之前，将DAADUSR.AMADSEL1位设置为1。

当DAADST位设置为1时，不能使用事件链接功能。通过设置ELC的ELSR12和ELSR13寄存器。DAADST位的设置由DAC12的通道0和1共享。

44.2.5 DAAMPCR:DA输出放大器控制寄存器

Base address: DAC12 = 0x4017_1000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAAMP1	DAAMP0	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	DAAMP0	放大器控制0 0：不使用通道0输出放大器1：使用通道0输出放大器	R/W
7	DAAMP1	放大器控制1 0：不使用通道1输出放大器1：使用通道1输出放大器	R/W

DAAMPCR寄存器选择使用或不使用放大器的DA输出。

DAAMP0位（放大器控制0）

当DAAMP0位为0时，模拟值输出通道0的DA输出，而不使用放大器。当。。。的时候DAAMP0位为1，模拟值通过放大器输出通道0的DA输出。

当DACR.DAE和DACR.DAOE0位都为0时，无论设置如何都不会使用放大器DAAMP0位。详见表44.4。

DAAMP1位（放大器控制1）

当DAAMP1位为0时，模拟值输出通道1的DA输出，而不使用放大器。当。。。的时候DAAMP1位为1，模拟值通过放大器输出到通道1的DA输出。

当DACR.DAE和DACR.DAOE1位都为0时，无论设置如何都不会使用放大器DAAMP1位。详见表44.4。

44.2.6 DAASWCR:DA放大器稳定等待控制寄存器

Base address: DAC12 = 0x4017_1000

Offset address: 0x1C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	DAASW1	DAASW0	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5	—	These bits are read as 0. The write value should be 0.	R/W
6	DAASW0	D/A Amplifier Stabilization Wait 0 0: Amplifier stabilization wait off (output) for channel 0 1: Amplifier stabilization wait on (high-Z) for channel 0	R/W
7	DAASW1	D/A Amplifier Stabilization Wait 1 0: Amplifier stabilization wait off (output) for channel 1 1: Amplifier stabilization wait on (high-Z) for channel 1	R/W

The DAASWCR register controls D/A output with the output amplifier. This register is used in the initialization procedure to wait for stabilization of the D/A output amplifier. Each bit in DAASWCR should be set to 1 when both the DACR.DAE bit and the DACR.DAOEi (i = 0, 1) bit are 0. See section 44.6.5. Initialization Procedure with the Output Amplifier.

DAASW0 bit (D/A Amplifier Stabilization Wait 0)

Set the DAASW0 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 0 output amplifier. When DAASW0 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 0. When the DAASW0 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 0 is output through the output amplifier.

DAASW1 bit (D/A Amplifier Stabilization Wait 1)

Set the DAASW1 bit to 1 in the initialization procedure to wait for the stabilization of the D/A channel 1 output amplifier. When DAASW1 is set to 1, D/A conversion operates, but the conversion result of D/A is not output from channel 1. When the DAASW1 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 1 is output through the output amplifier.

44.2.7 DAADUSR : D/A A/D Synchronous Unit Select Register

Base address: DAC12 = 0x4017_1000

Offset address: 0x10C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	AMADSEL1	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	This bit is read as 0. The write value should be 0.	R/W
1	AMADSEL1	A/D Unit 1 Select 0: Do not select unit 1 1: Select unit 1	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

The DAADUSR register selects the target ADC12 unit for D/A and A/D synchronous conversions. Set the AMADSEL1 bit to 1 to select unit 1 as the target synchronous unit for the MCU. When setting the DAADSCR.DAADST bit to 1 for synchronous conversions, select the target unit in this register in advance.

Only set the DAADUSR register while the ADCSR.ADST bit of the ADC12 is set to 0 and the DAADSCR.DAADST bit is set to 0.

44.3 Operation

The DAC12 includes D/A conversion circuits for two channles, each of which can operate independently. When the DAOEn bit (n = 0, 1) in DACR is set to 1, DAC12 is enabled and the conversion result is output.

This following example shows D/A conversion on channel 0. Figure 44.2 shows the timing of this operation.

To process D/A conversion on channel 0:

1. Set the data for D/A conversion in the DADR0 register and the data format in the DADPR.DPSEL bit.

Bit	Symbol	Function	R/W
5	—	这些位被读取为0。写入值应为0。	R/W
6	DAASW0	DA放大器稳定等待0 0：通道0的放大器稳定等待关闭（输出）1：通道0的放大器稳定等待打开（高阻态）	R/W
7	DAASW1	DA放大器稳定等待1 0：通道1的放大器稳定等待关闭（输出）1：通道1的放大器稳定等待打开（高阻态）	R/W

DAASWCR寄存器通过输出放大器控制DA输出。该寄存器在初始化过程中用于等待DA输出放大器的稳定。当DACR.DAE位和DACR.DAOEi(i=0 1)位均为0时，DAASWCR中的每个位都应设置为1。请参见第44.6.5节。输出放大器的初始化程序。

DAASW0位（DA放大器稳定等待0）

在初始化过程中将DAASW0位设置为1，以等待DA通道0输出放大器稳定。当DAASW0设置为1时，DA转换进行，但DA的转换结果不从通道0输出。当DAASW0位为0时，稳定等待时间停止，通过输出输出通道0的DA转换结果放大器。

DAASW1位（DA放大器稳定等待1）

在初始化过程中将DAASW1位设置为1，以等待DA通道1输出放大器稳定。当DAASW1设置为1时，DA转换进行，但DA的转换结果不从通道1输出。当DAASW1位为0时，稳定等待时间停止，通道1的DA转换结果通过输出输出放大器。

44.2.7 DAADUSR:DAAD同步单元选择寄存器

Base address: DAC12 = 0x4017_1000

Offset address: 0x10C0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	AMADSEL1	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	—	该位读取为0。写入值应为0。	R/W
1	AMADSEL1	AD单元1选择 0：不选择单元11：选择单元1	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

DAADUSR寄存器为DA和AD同步转换选择目标ADC12单元。将AMADSEL1位设置为1以选择单元1作为MCU的目标同步单元。将DAADSCR.DAADST位设置为1以进行同步转换时，请预先在该寄存器中选择目标单位。

仅在ADC12的ADCSR.ADST位设置为0且DAADSCR.DAADST位设置为0时设置DAADUSR寄存器。

44.3 Operation

DAC12包含两个通道的DA转换电路，每个通道都可以独立工作。当。。。的时候
DACR中的DAOEn位(n=0 1)设置为1，使能DAC12并输出转换结果。

以下示例显示了通道0上的DA转换。图44.2显示了此操作的时序。

在通道0上处理DA转换：

1.在DADR0寄存器中设置用于DA转换的数据，在DADPR.DPSEL位中设置数据格式。

2. Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time t_{DCONV} elapses. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is set to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Setting in DADR0}}{4096} \times \text{VREFH}$$

3. To start conversion again, write another value to DADR0. The conversion result is output after the conversion time t_{DCONV} elapses.
   When the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled), a maximum of one A/D conversion time is required for D/A conversion to start. When ADCLK is faster than the peripheral clock, a longer time might be required.
4. To disable analog output, set the DAOE0 bit to 0.

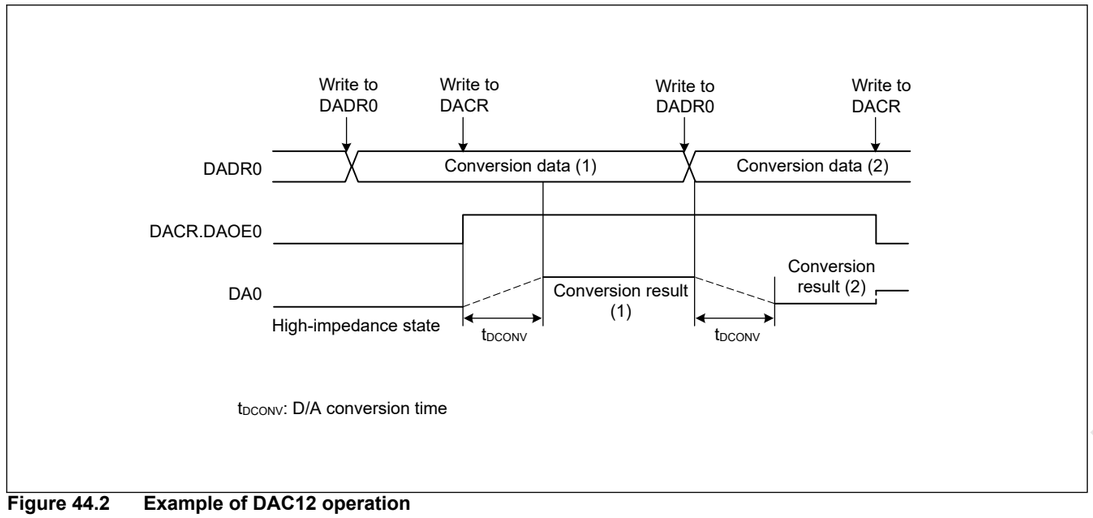

Figure 44.2 Example of DAC12 operation

44.3.1 Reducing Interference between D/A and A/D Conversion

When D/A conversion starts, the DAC12 generates inrush current. Because the DAC12 and ADC12 (unit 1) share the same analog power supply, the generated inrush current can interfere with ADC12 (unit 1) operation.

While the DAADSCR.DAADST bit is 1, D/A conversion does not start immediately on updating the DADRm register. Instead:

- If the DADRm register data is modified while the ADC12 is halted, D/A conversion starts in 1 PCLKA cycle.
- If the DADRm register data is modified while the ADC12 is performing a 12-bit A/D conversion, D/A conversion starts on A/D conversion completion. Therefore, it takes up to one A/D conversion time period for the DADRm register data update to be reflected as the D/A conversion circuit output. Until the D/A conversion completes, the DADRm register value does not correspond to the analog output value.

When the DAADSCR.DAADST bit is 1, it is not possible to check through software whether the DADRm register value was D/A-converted.

The following sequence provides an example of channel 0 D/A conversion, in which the DAC12 is synchronized with the ADC12 (unit 1). Figure 44.3 shows the timing of this operation.

To perform D/A conversion on channel 0 in synchronization with the ADC12 (unit 1):

1. Confirm that the ADC12 (unit 1) is halted and set the DAADUSR.AMADSEL1 bit to 1.
2. Confirm that the ADC12 (unit 1) is halted and set the DAADSCR.DAADST bit to 1.
3. Confirm that the ADC12 (unit 1) is halted and set the DACR.DAOE0 bit to 1.

2.将DACR.DAOE0位设置为1以启动DA转换。经过转换时间tDCONV后，转换结果从模拟输出引脚DA0输出。转换结果继续输出，直到再次写入DADR0或将DAOE0位设置为0。输出值（参考值）由以下公式表示：

$$\frac{\text{DADR04096中的设置}}{} \times \text{VREFH}$$

3.要再次开始转换，向DADR0写入另一个值。在经过转换时间tDCONV后输出转换结果。当DAADSCR.DAADST位为1时（启用DA和AD转换之间的干扰降低），最多需要一个AD转换时间才能启动DA转换。当ADCLK比外设时钟快时，可能需要更长的时间。

4.要禁用模拟输出，请将DAOE0位设置为0。

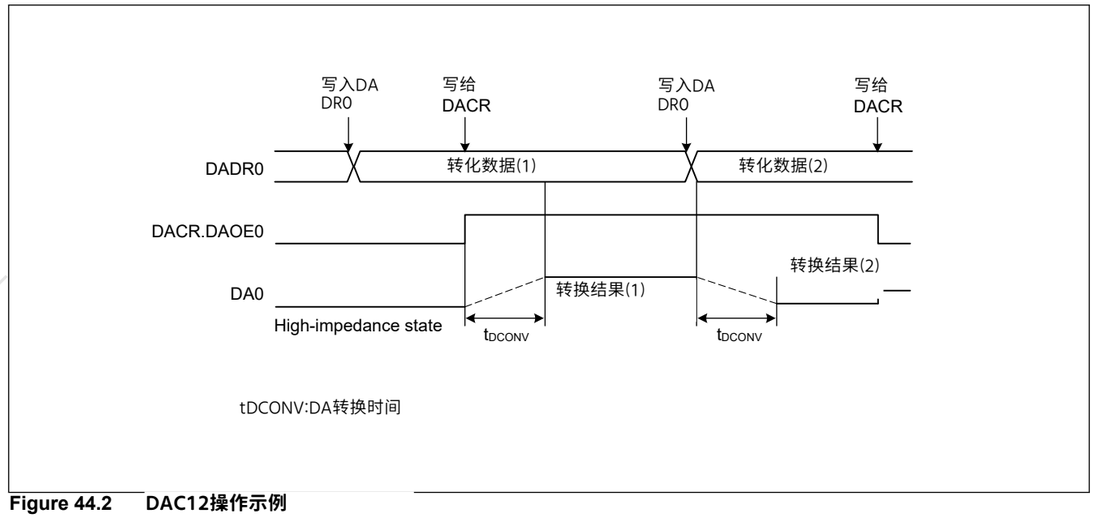

Figure 44.2 DAC12操作示例

44.3.1 减少DA和AD转换之间的干扰

当DA转换开始时，DAC12会产生浪涌电流。由于DAC12和ADC12（单元1）共享相同的模拟电源，所产生的浪涌电流会干扰ADC12（单元1）的运行。

当DAADSCR.DAADST位为1时，DA转换不会在更新DADRm寄存器时立即开始。
Instead:

●如果在ADC12停止时修改了DADRm寄存器数据，则DA转换在1个PCLKA周期内开始。

●如果在ADC12执行12位AD转换时修改了DADRm寄存器数据，则DA转换在AD转换完成时开始。因此，DADRm寄存器数据更新最多需要一个AD转换时间周期才能反映为DA转换电路输出。在DA转换完成之前，DADRm寄存器的值与模拟输出值不对应。

当DAADSCR.DAADST位为1时，无法通过软件检查DADRm寄存器值是否经过DA转换。

以下序列提供了通道0DA转换的示例，其中DAC12与
ADC12（单元1）。图44.3显示了该操作的时序。

与ADC12（单元1）同步在通道0上执行DA转换：

1.确认ADC12（单元1）已停止并将DAADUSR.AMADSEL1位设置为1。

2.确认ADC12（单元1）已停止并将DAADSCR.DAADST位设置为1。

3.确认ADC12（单元1）已停止并将DACR.DAOE0位设置为1。

4. Set the DADR0 register. If ADCLK is faster than the peripheral clock, D/A conversion might be delayed for longer than one A/D conversion time.
   - If the ADC12 (unit 1) is halted (ADCSR.ADST = 0) when the DADR0 register is modified, D/A conversion starts in 1 PCLKA cycle.
   - If the 12-bit A/D conversion is in progress (ADCSR.ADST = 1) when the DADR0 register is modified, D/A conversion starts on A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update might not be converted.

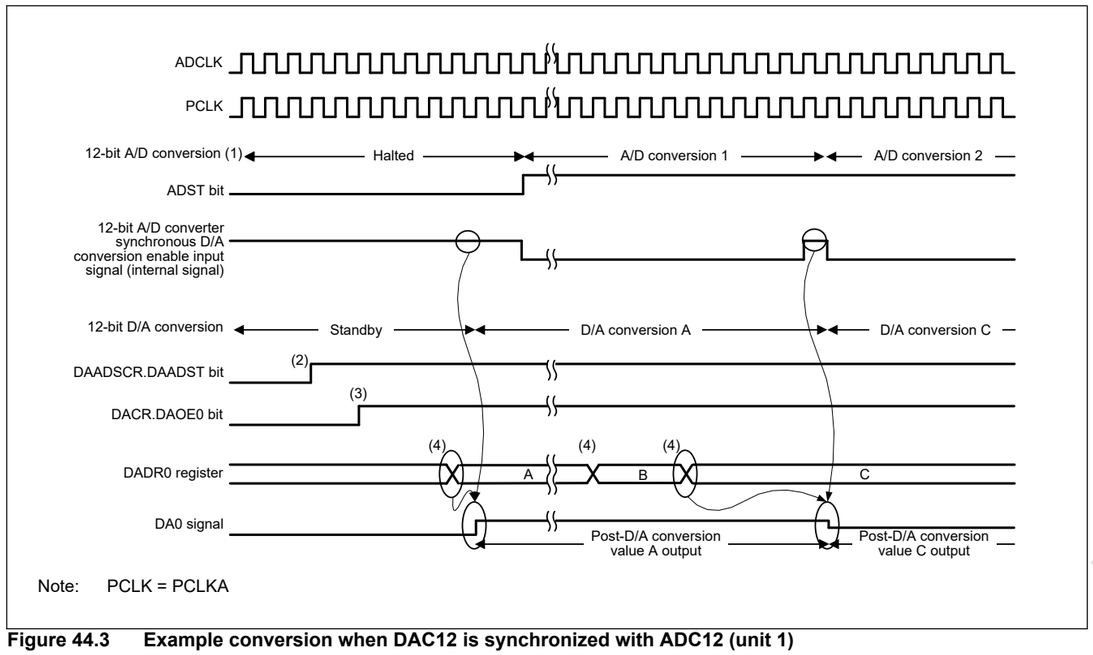

Figure 44.3 Example conversion when DAC12 is synchronized with ADC12 (unit 1)

When ADCLK is faster than PCLKA, the DAC12 might not be able to capture the synchronous D/A conversion enable input signal from the ADC12 (unit 1) during the 1 ADCLK cycle that is output between A/D conversion 1 and A/D conversion 2, as shown in Figure 44.4. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

4.设置DADR0寄存器。如果ADCLK比外设时钟快，则DA转换可能会延迟超过一次AD转换时间。

- ●如果在修改DADR0寄存器时ADC12（单元1）停止（ADCSR.ADST=0），则DA转换在1个PCLKA周期内开始。
- ●如果在修改DADR0寄存器时正在进行12位AD转换（ADCSR.ADST=1），则DA转换在AD转换完成时开始。如果在AD转换期间DADR0寄存器被修改两次，第一次更新可能不会被转换。

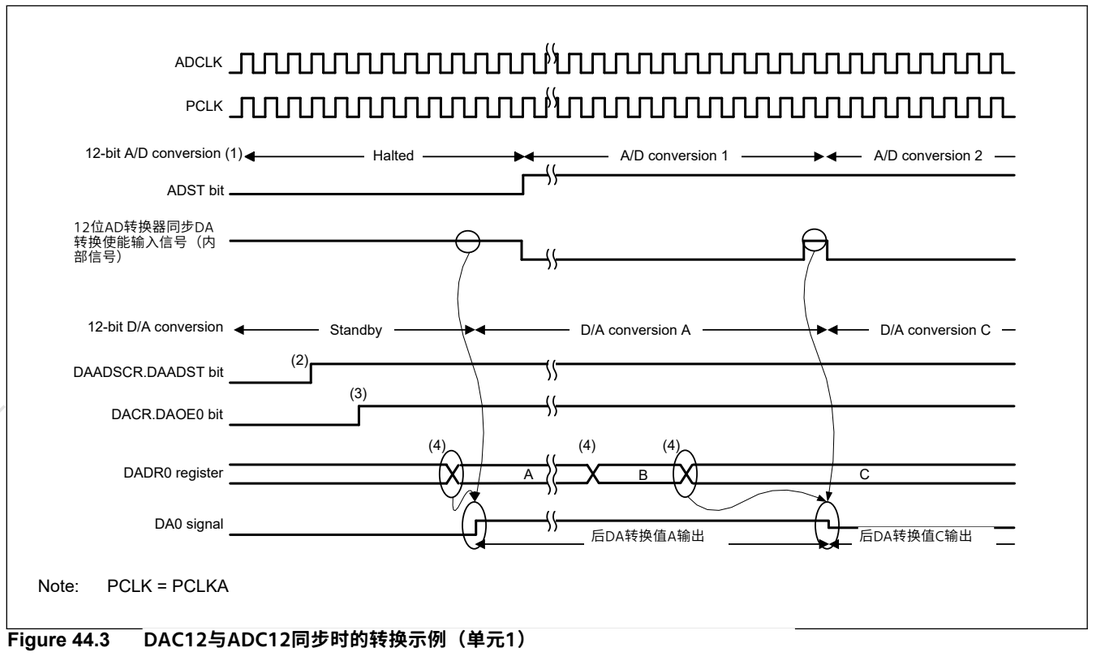

Figure 44.3 DAC12与ADC12同步时的转换示例（单元1）

当ADCLK快于PCLKA时，DAC12可能无法在AD转换1和AD转换2之间输出的1个ADCLK周期内捕获来自ADC12（单元1）的同步DA转换使能输入信号，如图所示44.4.在这种情况下，后DA转换值A作为DA0信号连续输出。

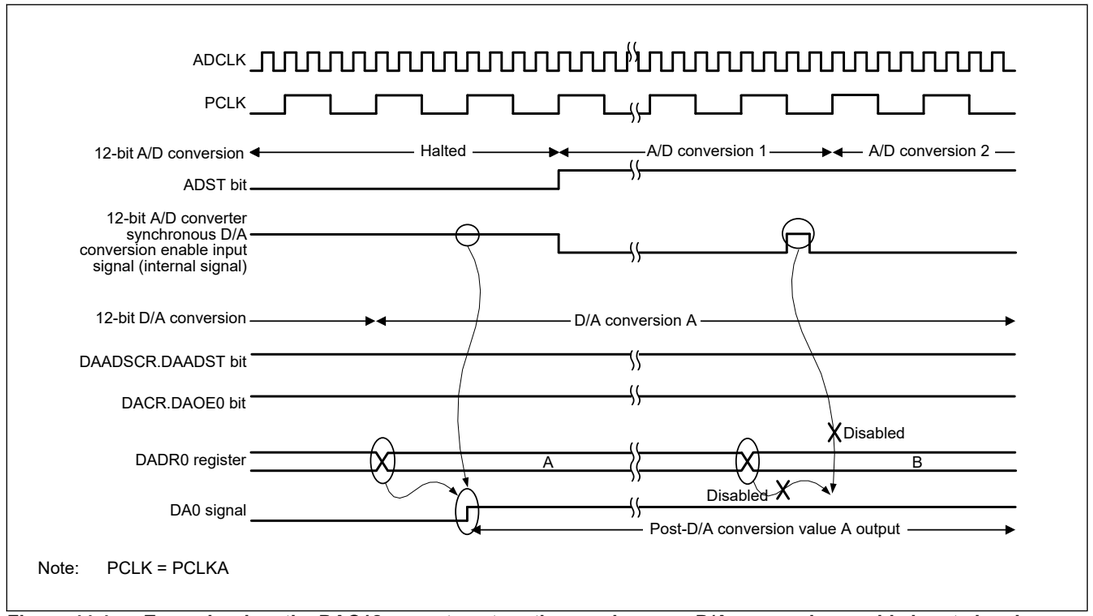

Figure 44.4 Example when the DAC12 cannot capture the synchronous D/A conversion enable input signal from the ADC12 (unit 1)

44.4 Event Link Operation Setting Procedure

This section describes the procedures used in event link operation.

44.4.1 DA0 Event Link Operation Setting Procedure

To set up DA0 event link operation:

1. Set the DADPR.DPSEL bit and the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA0 event signal to be linked to each peripheral module in the ELSR12 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit becomes 1, and D/A conversion starts on channel 0.
5. Set the ELSR12 register to 0x0000 to stop event link operation of DAC12 channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

44.4.2 DA1 Event Link Operation Setting Procedure

To set up DA1 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR1 register.
2. Set the ELC_DA1 event signal to be linked to each peripheral module in the ELSR13 register.
3. Set the ELCR.ELCON bit to 1. This enables the event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE1 bit is becomes 1, and D/A conversion starts on channel 1.
5. Set the ELSR13 register to 0x0000 to stop event link operation on DAC12 channel 1. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

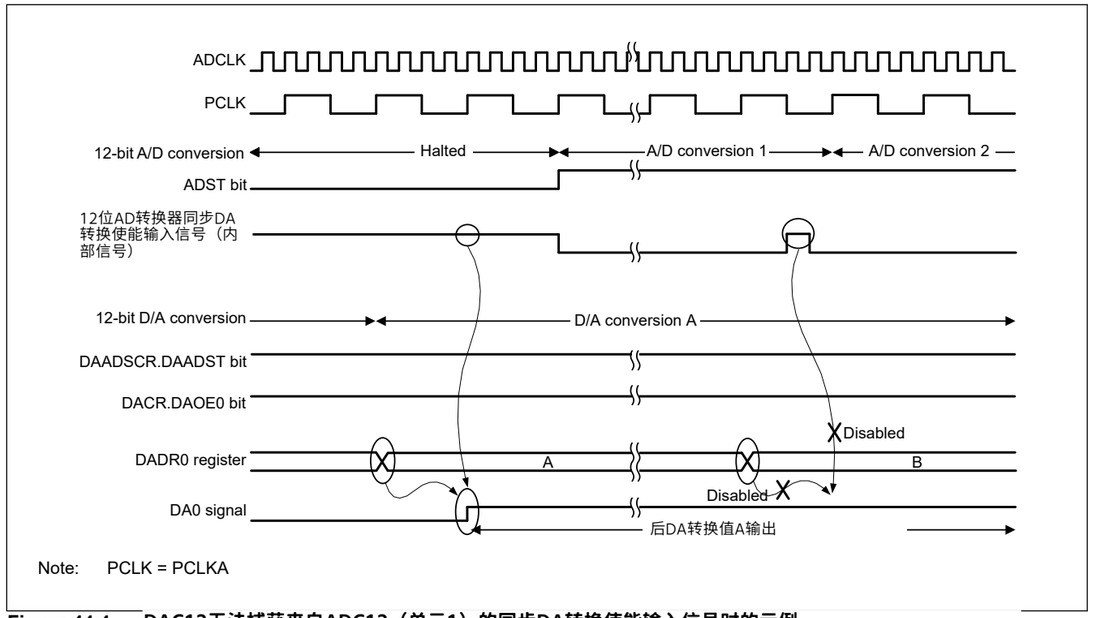

Figure 44.4 DAC12无法捕获来自ADC12（单元1）的同步DA转换使能输入信号时的示例

44.4 事件链接操作设置步骤

本节介绍事件链接操作中使用的过程。

44.4.1 DA0事件链接操作设置步骤

设置DA0事件链接操作：

1.设置DADPR.DPSEL位和DADR0寄存器中用于DA转换的数据。

2.在ELSR12寄存器中设置ELC_DA0事件信号链接到每个外围模块。

3.将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。

4.设置事件输出源模块，激活事件链接。模块输出事件后，DACR.DAOE0位变为1，通道0开始DA转换。

5.将ELSR12寄存器设置为0x0000以停止DAC12通道0的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

44.4.2 DA1事件链接操作设置步骤

设置DA1事件链接操作：

1.设置DADPR.DPSEL位并在DADR1寄存器中设置用于DA转换的数据。

2.在ELSR13寄存器中设置ELC_DA1事件信号链接到每个外围模块。

3.将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。

4.设置事件输出源模块，激活事件链接。模块输出事件后，DACR.DAOE1位变为1，通道1开始DA转换。

5.将ELSR13寄存器设置为0x0000以停止DAC12通道1上的事件链接操作。所有事件链接操作在ELCR.ELCON位设置为0时停止。

44.5 Usage Notes on Event Link Operation

- When the event link function is used, do not use the amplifier output function.
- When the event link function is used, set the DACR.DAE bit to 0.
- When the event specified for the ELC_DA0 event signal is generated while a write to the DACR.DAOE0 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA1 event signal is generated while a write to the DACR.DAOE1 bit is performed, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- Use of the event link function is prohibited when the DAADSCR.DAADST bit is set to 1 to reduce interference between D/A and A/D conversions.

44.6 Usage Notes

44.6.1 Settings for the Module-Stop Function

DAC12 operation can be disabled or enabled using the Module Stop Control Register. The DAC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

44.6.2 DAC12 Operation in the Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in the module-stop state, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

44.6.3 DAC12 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

44.6.4 Constraint on Entering Deep Software Standby Mode

When the MCU enters Deep Software Standby mode with D/A conversion enabled, the outputs of the DAC12 are placed in a high impedance state.

44.6.5 Initialization Procedure with the Output Amplifier

Use the following initialization procedures with the output amplifier. The example shows the case for channel 0.

To initialize the DAC12 with the output amplifier:

1. Write 0x0000 to the DADR0 register.
2. Set the DAASWCR.DAASW0 bit to 1.
3. Set the DAAMPCR.DAAMP0 bit to 1.
4. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1 to start operation of the amplifier.
5. Clear the DAASWCR.DAASW0 bit to 0 after waiting for the duration of D/A conversion time t_{DCONV}.
6. Write the value to be converted in the DADR0 register.

44.5 事件链接操作使用说明

●使用事件链接功能时，请勿使用放大器输出功能。

●使用事件链接功能时，将DACR.DAE位设置为0。

●如果在执行对DACR.DAOE0位的写入时产生了为ELC_DA0事件信号指定的事件，则写入周期停止，并且产生的事件优先将该位设置为1。

●如果在执行对DACR.DAOE1位的写入时产生了为ELC_DA1事件信号指定的事件，则写入周期停止，并且产生的事件优先将该位设置为1。

●DAADSCR.DAADST位设置为1时禁止使用事件链接功能，以减少DA和AD转换之间的干扰。

44.6 使用说明

44.6.1 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用DAC12操作。DAC12在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

44.6.2 DAC12在模块停止状态下的操作

当MCU进入模块停止状态并启用DA转换时，DA输出保持不变，模拟电源电流与DA转换时相同。如果在模块停止状态下必须降低模拟电源电流，则通过将DACR.DAOE1、DAOE0和DAE位设置为0来禁用DA转换。

44.6.3 DAC12在软件待机模式下的操作

当MCU进入软件待机模式并启用DA转换时，DA输出保持不变，模拟电源电流与DA转换期间相同。如果在软件待机模式下必须降低模拟电源电流，则通过将DACR.DAOE1、DAOE0和DAE位设置为0来禁用DA转换。

44.6.4 进入深度软件待机模式的限制

当MCU在启用DA转换的情况下进入深度软件待机模式时，DAC12的输出置于高阻抗状态。

44.6.5 输出放大器的初始化程序

对输出放大器使用以下初始化程序。该示例显示了通道0的情况。

使用输出放大器初始化DAC12：

1.将0x0000写入DADR0寄存器。

2.将DAASWCR.DAASW0位设置为1。

3.将DAAMPCR.DAAMP0位设置为1。

4.将DACR.DAE位或DACR.DAOE0位设置为1以启动放大器的操作。

5.等待DA转换时间tDCONV后，将DAASWCR.DAASW0位清零。

6.将要转换的值写入DADR0寄存器。

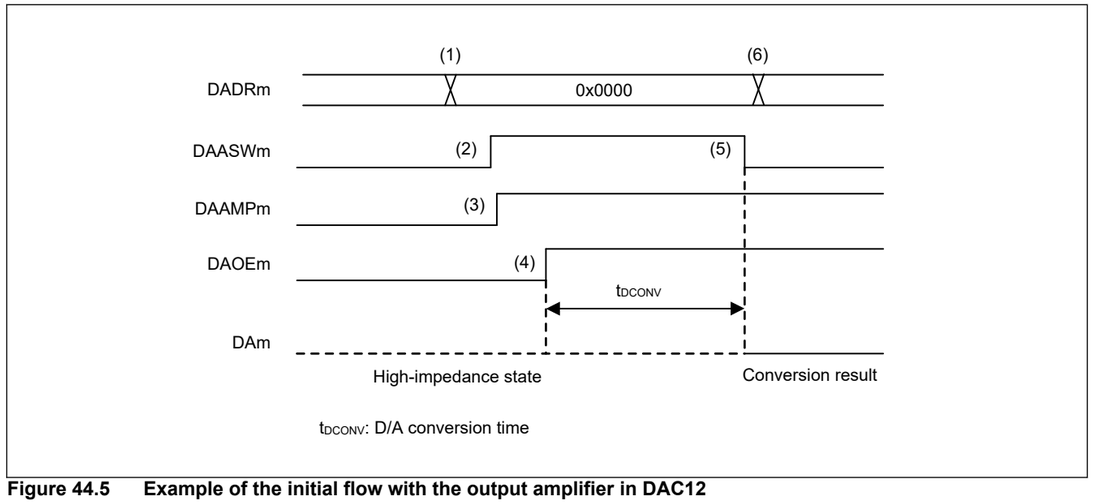

Figure 44.5 Example of the initial flow with the output amplifier in DAC12

While the amplifier is running, clearing the DACR.DAE and DACR.DAOE0 bits to 0 allows the amplifier to stop operation. To use the amplifier again, repeat steps 1 to 6.

44.6.6 Constraint on Usage When Interference Reduction between D/A and A/D Conversion Is Enabled

When the DAADSCR.DAADST bit is 1, enabling interference reduction between D/A and A/D conversion, do not place the ADC12 in the module-stop state. Doing so can halt D/A conversion in addition to A/D conversion.

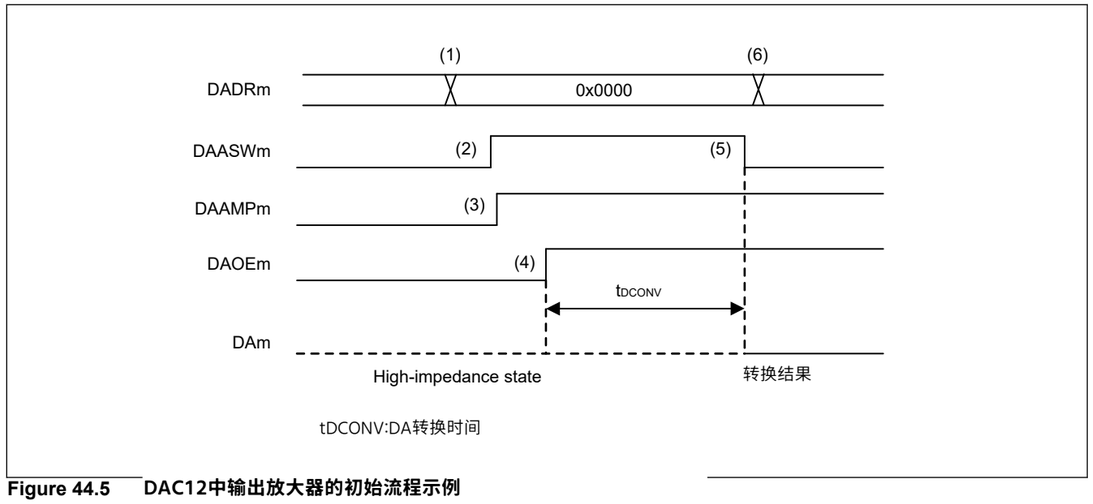

Figure 44.5 DAC12中输出放大器的初始流程示例

在放大器运行时，将DACR.DAE和DACR.DAOE0位清零可让放大器停止运行。
要再次使用放大器，请重复步骤1至6。

44.6.6 DA和AD之间减少干扰时的使用限制转换已启用

当DAADSCR.DAADST位为1时，启用DA和AD转换之间的干扰减少，不要放置ADC12处于模块停止状态。除了AD转换之外，这样做还可以停止DA转换。

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45. Temperature Sensor (TSN)

45.1 Overview

The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 45.1 lists the TSN specifications, and Figure 45.1 shows a block diagram.

Table 45.1 TSN specifications

Item	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter
Module-stop function	Module-stop state can be set to reduce power consumption
Temperature sensor calibration data	Reference data measured for each chip at factory shipment is stored in a register
TrustZone Filter	Security attribution can be set

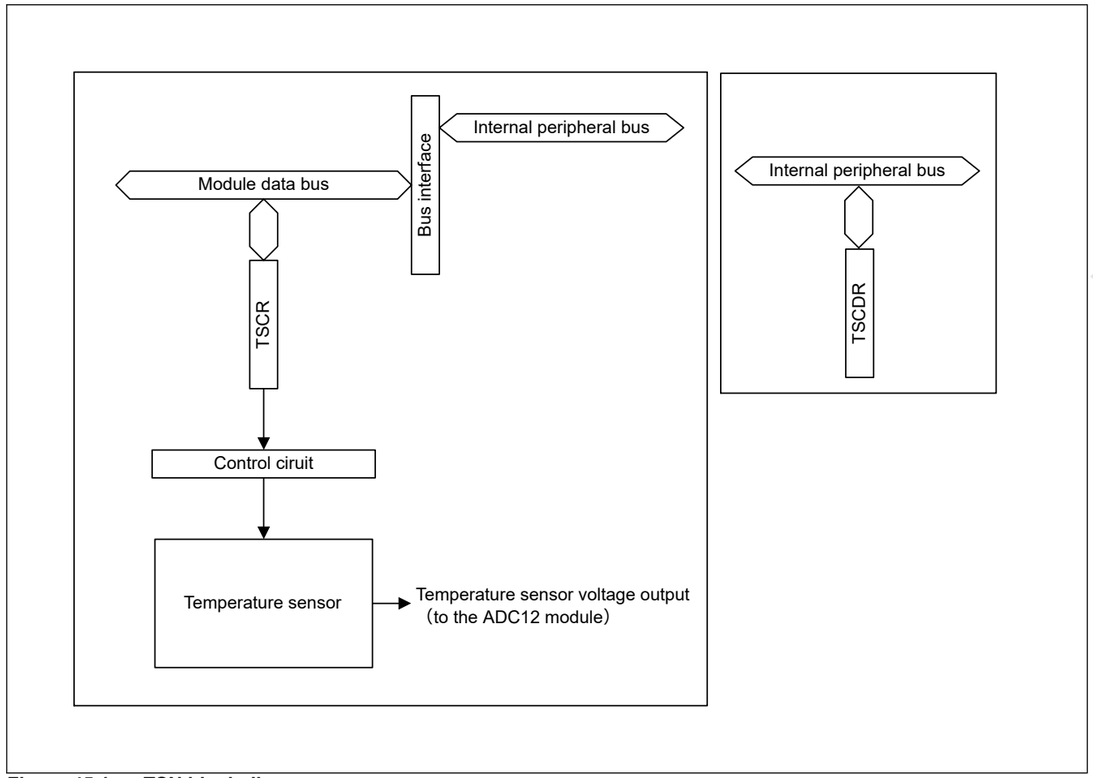

Figure 45.1 TSN block diagram

45. 温度传感器(TSN)

45.1 Overview

片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压被提供给ADC12进行转换，并且可以被最终应用进一步使用。

表45.1列出了TSN规范，图45.1显示了框图。

Table 45.1 TSN specifications

Item	Description
温度传感器电压输出	温度传感器向12位AD转换器输出电压
Module-stop function	可设置模块停止状态以降低功耗
温度传感器校准数据	出厂时为每个芯片测量的参考数据存储在寄存器中
TrustZone Filter	可设置安全属性

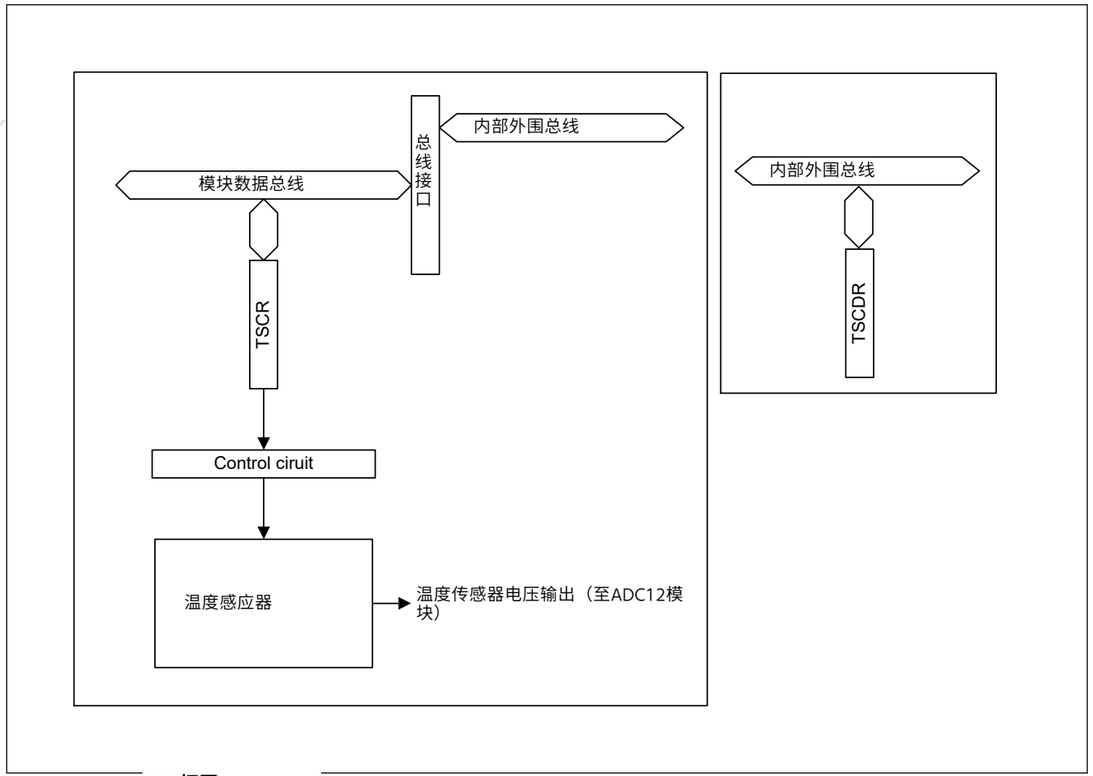

Figure 45.1 TSN框图

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45.2 Register Descriptions

45.2.1 TSCR : Temperature Sensor Control Register

Base address: TSN = 0x400F_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TSEN	—	—	TSOE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	These bits are read as 0. The write value should be 0.	R/W
4	TSOE	Temperature Sensor Output Enable 0: Disable output from the temperature sensor to the ADC12 1: Enable output from the temperature sensor to the ADC12	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	TSEN	Temperature Sensor Enable 0: Stop the temperature sensor 1: Start the temperature sensor.	R/W

The TSCR is a register which controls the temperature sensor. The timing constraints shown in Figure 45.3 apply to the settings of the TSCR register.

TSOE bit (Temperature Sensor Output Enable)

The TSOE bit enables or disables the temperature sensor output to ADC12.

TSEN bit (Temperature Sensor Enable)

The TSEN bit starts or stops the temperature sensor.

45.2.2 TSCDR : Temperature Sensor Calibration Data Register

Base address: TSD = 0x407F_B000

Offset Address: 0x017C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
Value after reset:	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	Temperature Sensor Calibration Data Chip-specific value	R
31:16	—	These bits are read as 0.	R

The TSCDR register stores temperature sensor calibration data measured for each chip at factory shipment.

Temperature sensor calibration data is the output voltage of the temperature sensor under the conditions Tj = 127°C and AVCC0 = VREFH0 = 3.3 V converted to a digital value by the 12-bit A/D converter.

The TSCDR register is a read-only 32-bit register. Read from this register in 32-bit units.

45.2 注册说明

45.2.1 TSCR：温度传感器控制寄存器

Base address: TSN = 0x400F_3000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	TSEN	—	—	TSOE	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	—	这些位被读取为0。写入值应为0。	R/W
4	TSOE	温度传感器输出使能 0：禁用从温度传感器到ADC12的输出1：启用从温度传感器到ADC12的输出	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	TSEN	温度传感器启用 0：停止温度传感器1：启动温度传感器。	R/W

TSCR是一个控制温度传感器的寄存器。图45.3所示的时序约束适用于TSCR寄存器的设置。

TSOE位（温度传感器输出使能）

TSOE位启用或禁用温度传感器输出到ADC12。

TSEN位（温度传感器使能）

TSEN位启动或停止温度传感器。

45.2.2 TSCDR:温度传感器校准数据寄存器

Base address: TSD = 0x407F_B000

Offset Address: 0x017C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	TSCDR[15:0]															
重置后的值：	Chip-specific value															

Bit	Symbol	Function	R/W
15:0	TSCDR[15:0]	温度传感器校准数据 Chip-specific value	R
31:16	—	这些位读为0。	R

TSCDR寄存器存储在出厂时为每个芯片测量的温度传感器校准数据。

温度传感器校准数据是温度传感器在条件Tj=127°C和AVCC0=VREFH0=3.3V通过12位AD转换器转换为数字值。

TSCDR寄存器是一个只读的32位寄存器。以32位为单位从该寄存器中读取。

Temperature sensor calibration data is stored in the lower 12 bits of the TSCDR register.

45.3 Using the Temperature Sensor

The temperature sensor outputs a voltage that varies with the temperature. This voltage is converted to a digital value by the 12-bit A/D converter. To obtain the die temperature, convert this value into the temperature.

45.3.1 Preparation for Using the Temperature Sensor

The ambient temperature (T) is proportional to the temperature sensor voltage output (Vs), so ambient temperature is calculated with the following formula:

T = (Vs - V1) / slope + T1

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor on temperature measurement (V)
- T1: Temperature experimentally measured at one point (°C)
- V1: Voltage output by the temperature sensor on measurement of T1 (V)
- T2: Temperature experimentally measured at a second point (°C)
- V2: Voltage output by the temperature sensor on measurement of T2 (V)
- Slope: Temperature gradient of the temperature sensor (V / °C), slope = (V2 - V1) / (T2 -T1)

Characteristics vary between sensors, so Renesas recommends measuring two different sample temperatures as follows:

1. Use the 12-bit A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Again use the 12-bit A/D converter to measure the voltage V2 output by the temperature sensor at a different temperature T2.
3. Obtain the temperature gradient (slope = (V2 - V1) / (T2 - T1)) from these results.
4. Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs - V1) / slope + T1).

If you are using the temperature gradient given in section 53, Electrical Characteristics, use the A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic using the following formula:

T = (Vs - V1) / slope + T1

Note: This method produces less accurate temperatures than measurement at two points.

In this MCU, the TSCDR register stores the temperature value (CAL127) of the temperature sensor measured under the condition Ta = Tj = 127°C and AVCC0 = VREFH0 = 3.3 V. If you use this value as the sample measurement result at the first point, you can omit the preparation before using the temperature sensor.

V1 is calculated from CAL127:

V1 = 3.3 × CAL127 / 4096 [V] (In case of 12 bit accuracy)

Using this value, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / slope + 127 [°C]

- T: Ambient temperature of MCU as calculation result (°C)
- Vs: Voltage output by the temperature sensor when the temperature is measured (V)
- V1: Voltage output by the temperature sensor when Ta = Tj = 127°C and AVCC0 = VREFH0 = 3.3 V (V)
- Slope: Temperature gradient of the temperature sensor*1 / 1000 (V/°C)

Note 1. See section 53, Electrical Characteristics

45.3.2 Procedures for Using the Temperature Sensor

Figure 45.2 shows the procedure for using the TSN.

温度传感器校准数据存储在TSCDR寄存器的低12位中。

45.3 使用温度传感器

温度传感器输出随温度变化的电压。该电压由12位AD转换器转换为数字值。要获得芯片温度，请将该值转换为温度。

45.3.1 使用温度传感器的准备工作

环境温度(T)与温度传感器电压输出(Vs)成正比，因此使用以下公式计算环境温度：

T = (Vs - V1) / slope + T1

- ●T：作为计算结果的MCU的环境温度（°C）
- ●Vs：温度传感器测温时的电压输出（V）
- ●T1：在某一点实验测量的温度(°C)
- ●V1：温度传感器在测量T1（V）时输出的电压
- ●T2：在第二点实验测量的温度(°C)
- ●V2：温度传感器在测量T2（V）时输出的电压
- ●斜率：温度传感器的温度梯度（V°C），斜率=（V2V1）（T2−T1）

传感器的特性各不相同，因此瑞萨电子建议测量两种不同的样品温度，如下所示：

1、使用12位AD转换器测量温度T1时温度传感器输出的电压V1。

2.再次使用12位AD转换器测量温度传感器在不同温度T2下输出的电压V2。

3.从这些结果中获得温度梯度（斜率=(V2V1)(T2T1)）。

4.随后，通过将斜率代入温度特性公式(T=(VsV1)斜率+T1)来获得温度。

如果您使用第53节“电气特性”中给出的温度梯度，请使用AD转换器测量温度传感器在温度T1下输出的电压V1，然后使用以下公式计算温度特性：

T = (Vs - V1) / slope + T1

Note: 这种方法产生的温度不如两点测量准确。

在此MCU中，TSCDR寄存器存储在Ta=Tj=127°C和AVCC0=VREFH0=3.3V条件下测量的温度传感器的温度值(CAL127)。如果您使用此值作为第一次的样本测量结果点，您可以省略使用温度传感器之前的准备工作。

V1由CAL127计算得出：

V1=3.3×CAL1274096[V]（在12位精度的情况下）

使用该值，可根据以下公式计算测得的温度：

T = (Vs - V1) / slope + 127 [°C]

- ●T：作为计算结果的MCU的环境温度（°C）
- ●Vs：测温时温度传感器输出的电压（V）
- ●V1：Ta=Tj=127°C且AVCC0=VREFH0=3.3V(V)时温度传感器输出的电压
- ●斜率：温度传感器的温度梯度*11000(V°C)

注1.见第53节，电气特性

45.3.2 使用温度传感器的步骤

图45.2显示了使用TSN的过程。

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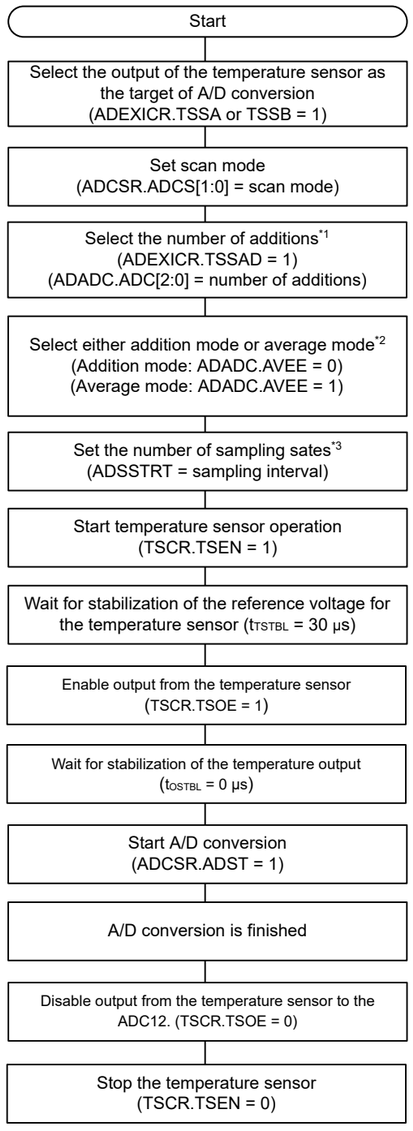
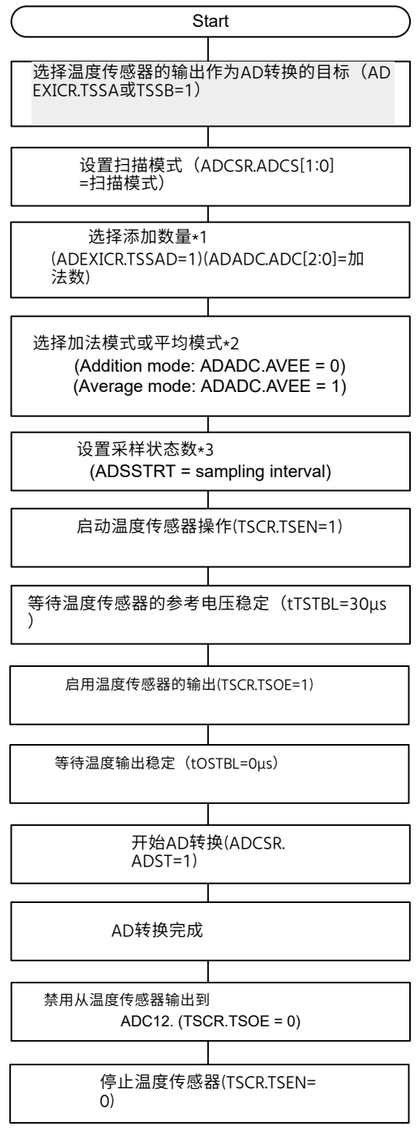
For details, see section 43, 12-Bit A/D Converter (ADC12).



Note 1. This setting is not required if addition/average mode is not set.
Note 2. The ADADC.ADC[2:0] setting is limited to some values in additions/average mode. For details on the available ADADC.ADC[2:0] settings in additions/average mode, see section 43, 12-Bit A/D Converter (ADC12).
Note 3. Set the sampling time to more than the value described in section 53, Electrical Characteristics.

Figure 45.2 Procedure example for using the TSN

有关详细信息，请参阅第43节，12位AD转换器(ADC12)。



注1.如果未设置加法平均模式，则不需要此设置。
注2.ADADC.ADC[2:0]设置仅限于加法平均模式下的某些值。有关可用的详细信息
ADADC.ADC[2:0]在加法平均模式下的设置，请参见第43节，12位AD转换器(ADC12)。
注3.将采样时间设置为大于第53节“电气特性”中描述的值。

Figure 45.2 使用TSN的过程示例

Figure 45.3 shows the timing from the start of temperature sensor operation until the completion of A/D conversion when the ADC12 is in single scan mode (the conversion target is the temperature sensor output only). The times shown in the figure are described in Table 45.2

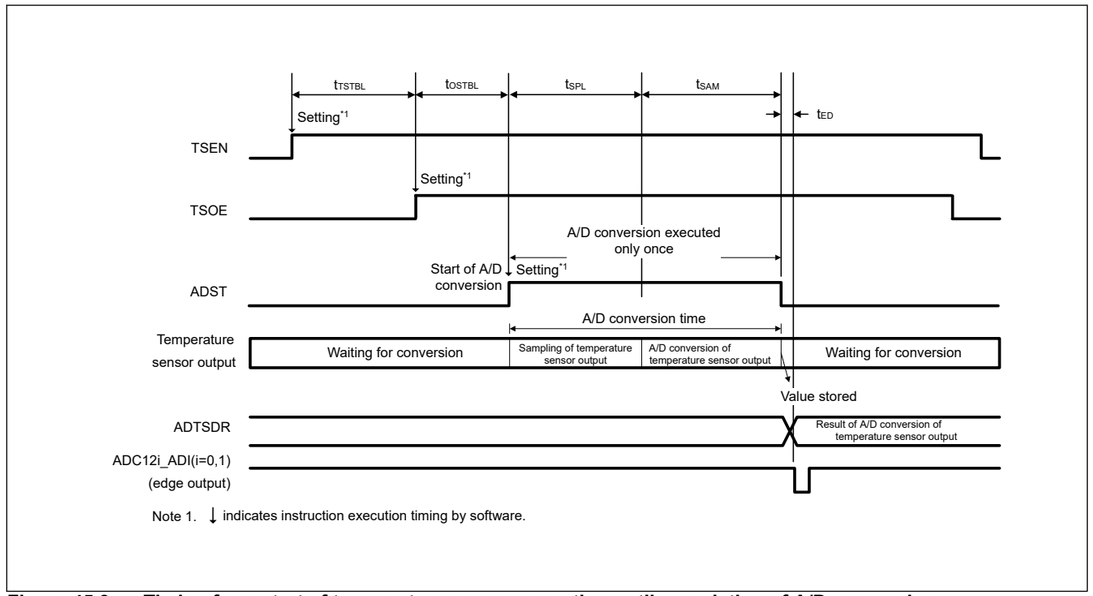


Figure 45.3 Timing from start of temperature sensor operation until completion of A/D conversion

Table 45.2 Time until completion of A/D conversion after start of temperature sensor operation

Parameter	Symbol	Time
Wait time for temperature sensor reference voltage stabilization	t_{TSTBL}	30 µs (min)
Wait time for temperature sensor output stabilization	t_{OSTBL}	0 µs (min)
A/D converter input sampling time	t_{SPL}	ADSSTRT setting × ADCLK cycles
A/D conversion time	t_{SAM}	See the table in section 43.3.7. Analog Input Sampling and Scan Conversion Time.
Scan conversion end delay	t_{ED}	

45.4 Usage Notes

45.4.1 Settings for the Module-Stop Function

TSN operation can be disabled or enabled using the associated bit in Module Stop Control Register D (MSTPCRD). The TSN is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

图45.3显示了当ADC12处于单次扫描模式（转换目标仅为温度传感器输出）时，从温度传感器操作开始到AD转换完成的时序。图中所示时间见表45.2

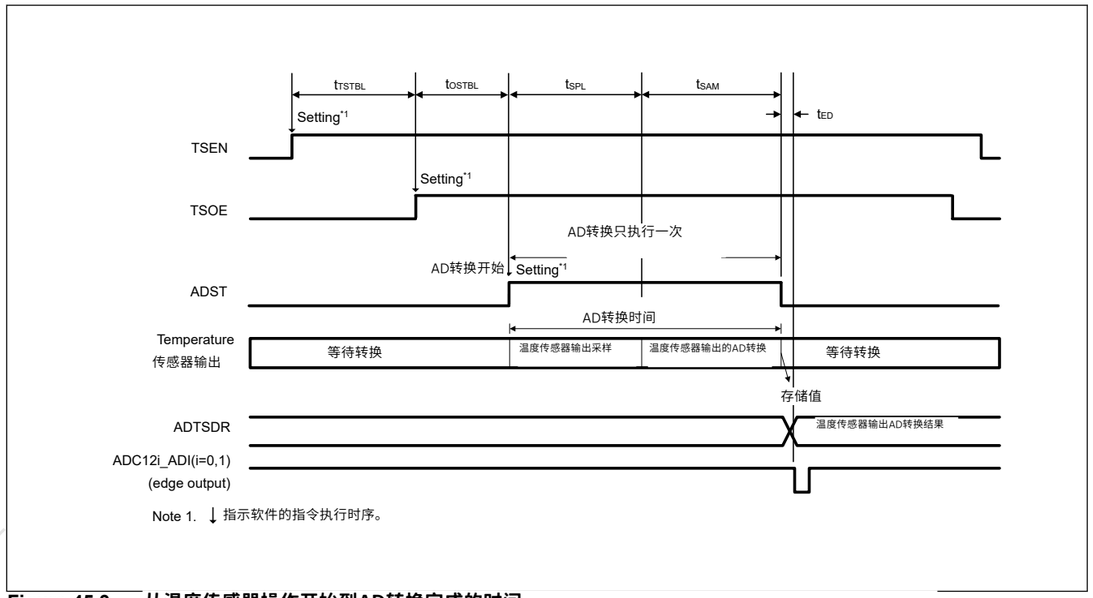


Figure 45.3 从温度传感器操作开始到AD转换完成的时间

Table 45.2 温度传感器动作开始后到AD转换完成的时间

Parameter	Symbol	Time
温度传感器参考电压稳定的等待时间	t_{TSTBL}	30 µs (min)
温度传感器输出稳定的等待时间	t_{OSTBL}	0 µs (min)
AD转换器输入采样时间	t_{SPL}	ADSTRT设置×ADCLK周期
AD转换时间	t_{SAM}	请参见第43.3.7节中的表格。模拟输入采样和扫描转换时间。
扫描转换结束延迟	t_{ED}	

45.4 使用说明

45.4.1 模块停止功能的设置

使用模块停止控制寄存器D(MSTPCRD)中的相关位可以禁用或启用TSN操作。TSN在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

46. Capacitive Touch Sensing Unit (CTSU)

46.1 Overview

The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode.

As Figure 46.1 shows, electrostatic capacitance (parasitic capacitance) exists between the electrode and the surrounding conductors. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the value of electrostatic capacitance increases.

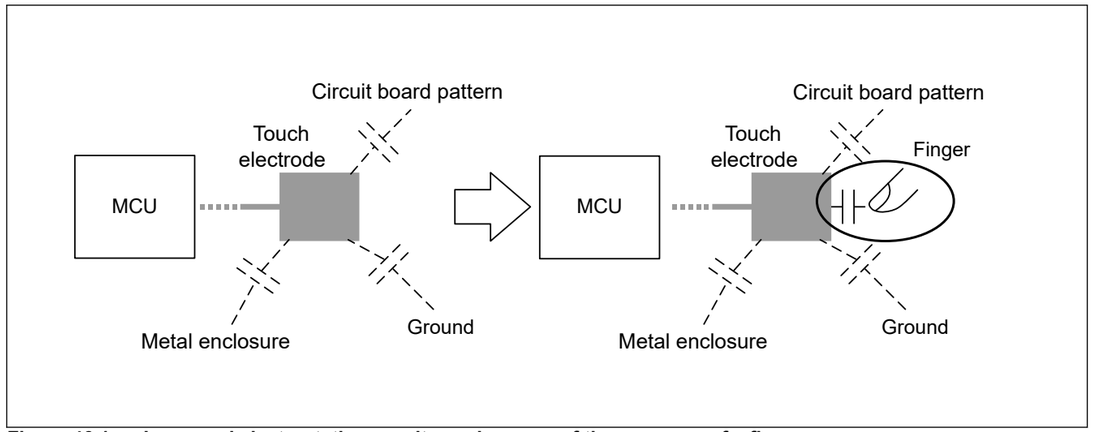


Figure 46.1 Increased electrostatic capacitance because of the presence of a finger

Electrostatic capacitance is detected by the self-capacitance and mutual capacitance methods. In the self-capacitance method, the CTSU detects electrostatic capacitance generated between a finger and a single electrode. In the mutual capacitance method, two electrodes are used one as a transmit electrode and the other as a receive electrode, and the CTSU detects the change in the electrostatic capacitance generated between the two when a finger is placed close to them.

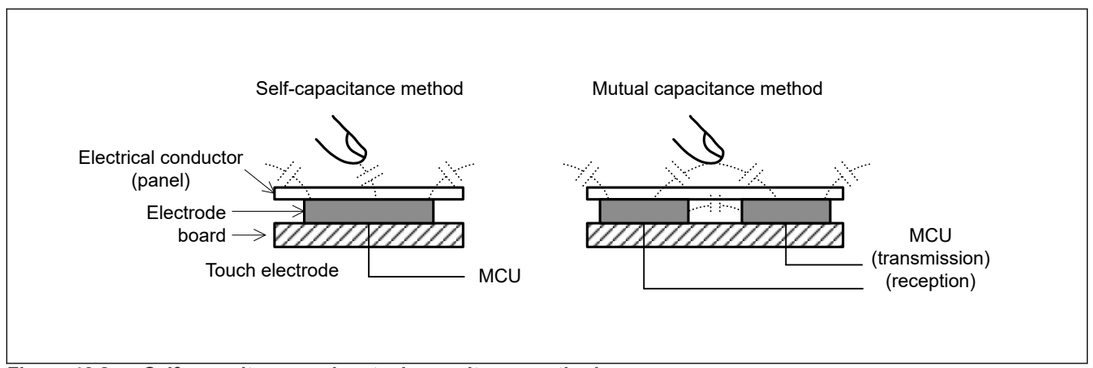


Figure 46.2 Self-capacitance and mutual capacitance methods

Electrostatic capacitance is measured by counting a clock signal whose frequency changes according to the amount of charged or discharged current, for a specified period. For details on the measurement principles of the CTSU, see section 46.3.1. Principles of Measurement Operation.

Table 46.1 lists the CTSU specifications and Figure 46.3 shows a block diagram.

46. 电容式触控感应单元(CTSU)

46.1 Overview

电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，该软件使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电导体包围，因此手指不会直接接触电极。

如图46.1所示，电极和周围导体之间存在静电电容（寄生电容）。因为人体是电导体，当手指靠近电极时，静电电容值会增加。

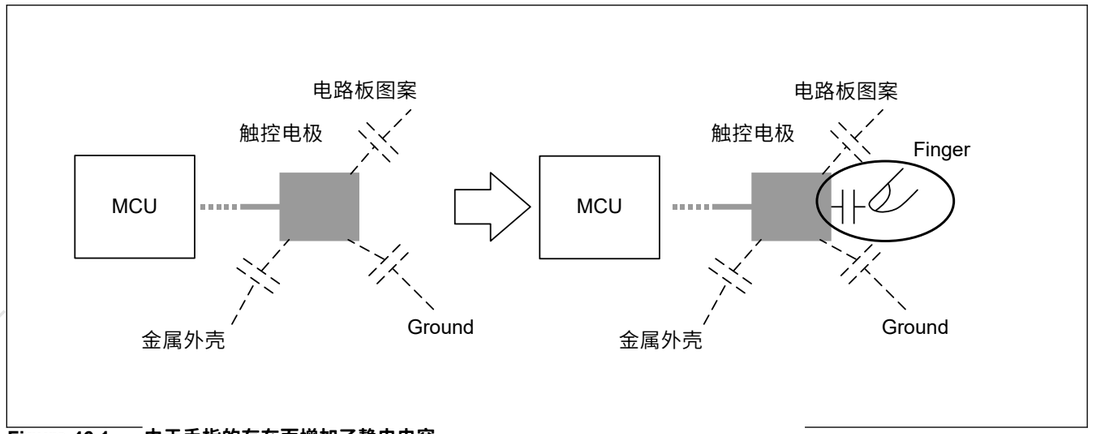


Figure 46.1 由于手指的存在而增加了静电电容

静电电容的检测方法有自电容法和互电容法。在自电容法中，CTSU检测手指和单个电极之间产生的静电电容。在互电容法中，使用两个电极，一个作为发送电极，另一个作为接收电极，当手指靠近它们时，CTSU会检测两者之间产生的静电电容的变化。

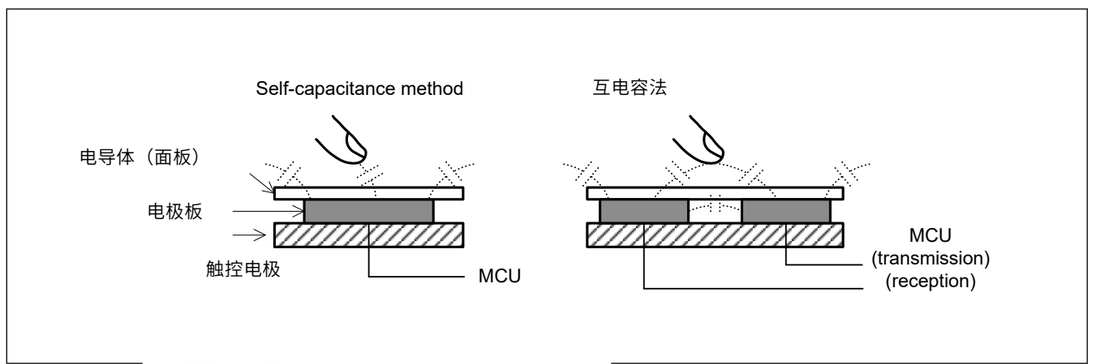


Figure 46.2 自电容和互电容方法

静电电容是通过对时钟信号进行计数来测量的，该时钟信号的频率根据充电或放电电流的大小而变化，在指定的时间段内。CTSU的测量原理详见46.3.1节。测量操作原理。

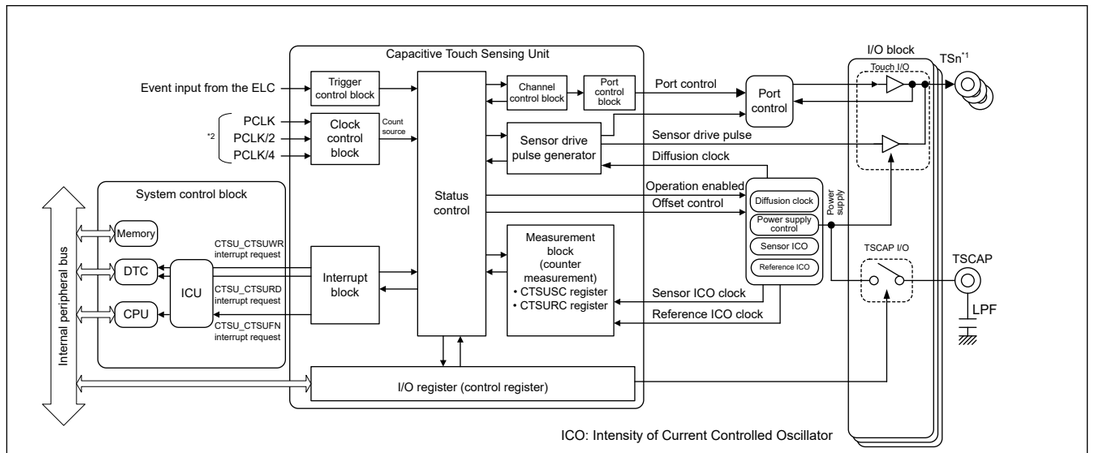
表46.1列出了CTSU规格，图46.3显示了框图。

Table 46.1 CTSU specifications

Parameter		Specifications
Operating clock		PCLKB, PCLKB/2, or PCLKB/4
Pins	Electrostatic capacitance measurement	20 channels
	TSCAP	Low Pass Filter (LPF) connection pin
Measurement modes	Self-capacitance single scan mode	Electrostatic capacitance is measured on one channel using the self-capacitance method.
	Self-capacitance multiscan mode	Electrostatic capacitance is measured successively on multiple channels using the self-capacitance method.
	Mutual capacitance full scan mode	Electrostatic capacitance is measured successively on multiple channels using the mutual capacitance method.
Calibration mode		Improvement of measured value accuracy by calibration of sensor ICO
Noise prevention		Synchronous noise prevention, high-pass noise prevention
Measurement start conditions		• Software trigger • External trigger (ELC_CTSU from the Event Link Controller (ELC))
TrustZone Filter		Security attribution can be set

As Figure 46.3 shows, the CTSU consists of the following components:

- Status control block
- Trigger control block
- Clock control block
- Channel control block
- Port control block
- Sensor drive pulse generator
- Measurement block
- Interrupt block
- I/O registers



Note 1. TSn = TS00 to TS19
Note 2. PCLK = PCLKB

Figure 46.3 CTSU block diagram

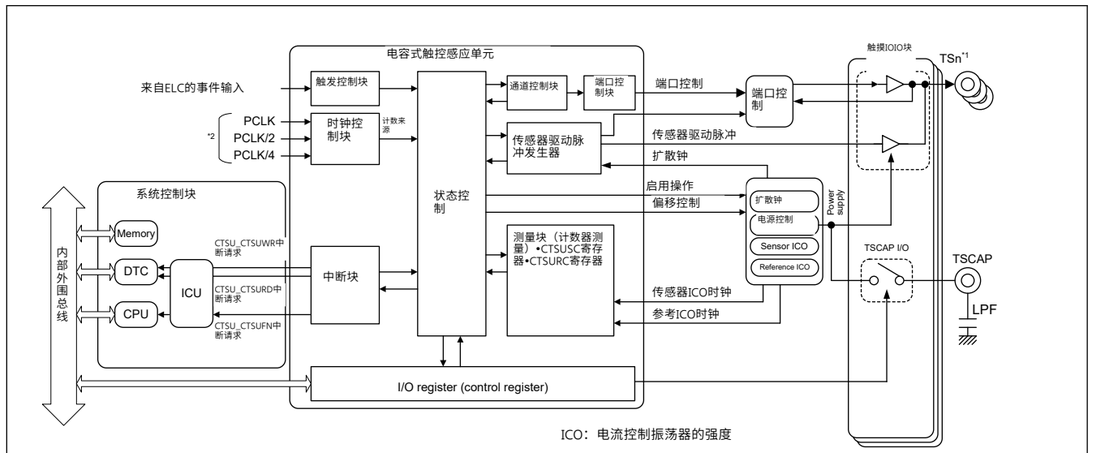
Table 46.1 CTSU specifications

Parameter		Specifications
工作时钟		PCLKB, PCLKB/2, or PCLKB/4
Pins	静电电容测量	20 channels
	TSCAP	低通滤波器(LPF)连接引脚
测量模式	自电容单次扫描模式	使用自电容法在一个通道上测量静电电容。
	Self-capacitance multiscan mode	使用自电容法在多个通道上连续测量静电电容。
	互电容全扫描模式	使用互电容法在多个通道上连续测量静电电容。
校准模式		通过传感器校准提高测量值精度 ICO
噪音预防		同步防噪、防高通防噪
测量开始条件		• 软件触发 • 外部触发器（来自事件链接控制器(ELC)的ELC_CTSU）
TrustZone Filter		可设置安全属性

如图46.3所示，CTSU由以下组件组成：

●状态控制块
●触发控制块
●时钟控制块
●通道控制块
●端口控制块
●传感器驱动脉冲发生器
●测量块
●中断块

- I/O registers



注1.TSn=TS00至TS19
Note 2. PCLK = PCLKB

Figure 46.3 CTSU框图

Table 46.2 CTSU I/O pins

Pin name	I/O	Function
TS00 to TS19	Input	Electrostatic capacitive measurement pins (touch pins)
TSCAP	—	LPF connection pin

46.2 Register Descriptions

46.2.1 CTSUCR0 : CTSU Control Register 0

Base address: CTSU = 0x400D_0000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUTXVSEL	—	—	CTSUINIT	CTSUIOC	CTSUSNZ	CTSUCAP	CTSUSTRT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CTSUSTRT	CTSU Measurement Operation Start 0: Stop measurement operation*1 1: Start measurement operation	R/W
1	CTSUCAP	CTSU Measurement Operation Start Trigger Select 0: Software trigger 1: External trigger	R/W
2	CTSUSNZ	CTSU Wait State Power-Saving Enable 0: Disable power-saving function during wait state 1: Enable power-saving function during wait state	R/W
3	CTSUIOC	CTSU Transmit Pin Control 0: The TS pins are driven low 1: The TS pins are driven high	R/W
4	CTSUINIT	CTSU Control Block Initialization Writing 1 to this bit initializes the CTSU control block and CTSUSC, CTSURC, CTSUMCH0, CTSUMCH1, and CTSUST registers. This bit is read as 0.	W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CTSUTXVSEL	CTSU Transmission Power Supply Select 0: TSCAP is selected as the power-supply voltage for the transmission pins. 1: VCL is selected as the power-supply voltage for the transmission pins.	R/W

Note 1. When the CTSU is not used, fix the value of this bit to 0.

Only set the CTSUCAP, CTSUSNZ, CTSUTXVSEL2 and CTSUTXVSEL bits when the CTSUSTRT bit is 0. These bits can be set at the same time that measurement operation starts.

CTSUSTRT bit (CTSU Measurement Operation Start)

The CTSUSTRT bit specifies whether CTSU operation starts or stops. When the CTSUSTRT bit is 0, measurement starts when the software writes 1 to the CTSUSTRT bit (software trigger) and stops when the hardware clears the CTSUSTRT bit to 0. When the CTSUSTRT bit is 1, the CTSU waits for an external trigger by writing 1 to the CTSUSTRT bit, and measurement starts on the rising edge of the external trigger. When measurement is stopped, the CTSU waits for the next external trigger and operation continues.

Table 46.3 lists the CTSU states.

Table 46.3 CTSU status (1 of 2)

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped

Table 46.2 CTSU I/O pins

引脚名称	I/O	Function
TS00 to TS19	Input	静电电容测量引脚（触摸引脚）
TSCAP	—	LPF连接引脚

46.2 注册说明

46.2.1 CTSUCR0:CTSU控制寄存器0

Base address: CTSU = 0x400D_0000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUTXVSEL	—	—	CTSUINIT	CTSUIOC	CTSUSNZ	CTSUCAP	CTSUSTRT
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CTSUSTRT	CTSU测量操作开始 0：停止测量操作*1 1：开始测量操作	R/W
1	CTSUCAP	CTSU测量操作开始触发选择 0：软件触发1：外部触发	R/W
2	CTSUSNZ	CTSU等待状态省电使能 0：等待状态下关闭省电功能1：等待状态下开启省电功能	R/W
3	CTSUIOC	CTSU发送引脚控制 0：TS引脚驱动为低电平1：TS引脚驱动为高电平	R/W
4	CTSUINIT	CTSU控制块初始化 向该位写入1初始化CTSU控制模块和CTSUSC、CTSURC、CTSUMC0、CTSUMCH1和CTSUST寄存器。该位读为0。	W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	CTSUTXVSEL	CTSU传输电源选择 0：选择TSCAP作为发送引脚的电源电压。1：选择VCL作为发送引脚的电源电压。	R/W

注1.不使用CTSU时，将该位的值固定为0。

仅当CTSUSTRT位为0时设置CTSUCAP、CTSUSNZ、CTSUTXVSEL2和CTSUTXVSEL位。这些位可以在测量操作开始的同时设置。

CTSUSTRT位（CTSU测量操作开始）

CTSUSTRT位指定CTSU操作是开始还是停止。当CTSUSTRT位为0时，软件将1写入CTSUSTRT位（软件触发）时开始测量，并在硬件将CTSUSTRT位清为0时停止测量。当CTSUSTRT位为1时，CTSU通过写入等待外部触发1到CTSUSTRT位，并在外部触发的上升沿开始测量。当测量停止时，CTSU等待下一个外部触发并继续操作。

表46.3列出了CTSU状态。

Table 46.3 CTSU状态(1of2)

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped

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Table 46.3 CTSU status (2 of 2)

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUST.CTSUSTC[2:0] flags as follows:
During measurement: CTSUST.CTSUSTC[2:0] flags ≠ 000b
While waiting for an external trigger: CTSUST.CTSUSTC[2:0] flags = 000b
When the CTSU is not used, fix the value of this bit to 0.

If the software sets the CTSUSTRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through the software when the CTSUSTRT bit is 1, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time.

CTSUCAP bit (CTSU Measurement Operation Start Trigger Select)

The CTSUCAP bit specifies the measurement start condition. For details, see CTSUSTRT bit (CTSU Measurement Operation Start).

CTSUSNZ bit (CTSU Wait State Power-Saving Enable)

The CTSUSNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU power supply, which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 46.4 shows the CTSU power supply state control.

Table 46.4 CTSU power supply state control

CTSUCR1.CTSUPON bit	CTSUSNZ bit	CTSUCAP bit	CTSUSTRT bit	CTSU power supply state
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: Other settings are prohibited.

To start measurement from the suspended state, set the CTSUSNZ bit to 0, and then set the CTSUSTRT bit to 1. To suspend the module after measurement stops, set the CTSUSNZ bit to 1.

CTSUIOC bit (CTSU Transmit Pin Control)

The CTSUIOC bit selects the logic level of the TS pin when the CTSUERRS.CTSUTSOD bit is set to 1. This bit setting is ignored when the CTSUTSOD bit is 0.

CTSUINIT bit (CTSU Control Block Initialization)

Write 1 to the CTSUINIT bit to initialize the internal control registers. To force the current operation to stop, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time. This stops the operation and initializes the internal control registers.

Do not write 1 to the CTSUINIT bit when the CTSUSTRT bit is 1.

CTSUTXVSEL bit (CTSU Transmission Power Supply Select)

The CTSUTXVSEL bit is used to switch the power supply for the transmit buffer in mutual capacitance full scan mode.

Set this bit to 0 for any other mode or when the VCC voltage is lower than 2.7 V. This bit switches the power supply for touch I/O, which is set for transmission by the CTSUCHTRCn registers. Table 46.5 lists the power supply for the TSm pin. When the VCC voltage fluctuates greatly due to switching of the output buffer, switching to the internal logic power supply can reduce the effect on the voltage fluctuation.

Table 46.3 CTSU状态（2个中的2个）

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	1	Stopped
1	0	测量中
1	1	测量中，等待外部触发*1

注1.可以从CTSUST.CTSUSTC[2:0]标志读取状态，如下所示：
测量期间：CTSUST.CTSUSTC[2:0]flags≠000b
等待外部触发时：CTSUST.CTSUSTC[2:0]flags=000b
不使用CTSU时，将该位的值固定为0。

如果在CTSUSTRT位已经为1时软件将该位设置为1，则忽略写入并继续操作。要在CTSUSTRT位为1时通过软件强制停止操作，请将CTSUSTRT位设置为0，同时将CTSUINIT位设置为1。

CTSUCAP位（CTSU测量操作开始触发选择）

CTSUCAP位指定测量开始条件。有关详细信息，请参阅CTSUSTRT位（CTSU测量Operation Start).

CTSUSNZ位（CTSU等待状态省电使能）

CTSUSNZ位在等待状态期间启用或禁用省电操作。它还可以暂停CTSU电源，从而降低等待状态下的功耗。在挂起状态下，CTSU电源关闭，而外部TSCAP仍在充电。

CTSU电源状态控制如表46.4所示。

Table 46.4 CTSU电源状态控制

CTSUCR1.CTSUPON位	CTSUSNZ位	CTSUCAP位	CTSUSTRT位	CTSU电源状态
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: 禁止其他设置。

要从暂停状态开始测量，请将CTSUSNZ位设置为0，然后将CTSUSTRT位设置为1。要在测量停止后暂停模块，请将CTSUSNZ位设置为1。

CTSUIOC位（CTSU发送引脚控制）

CTSUERRS.CTSUTSOD位设置为1时，CTSUITOC位选择TS引脚的逻辑电平。当CTSUTSOD位为0时，该位设置被忽略。

CTSUINIT位（CTSU控制块初始化）

向CTSUINIT位写入1以初始化内部控制寄存器。要强制停止当前操作，请将CTSUSTRT位为0，CTSUINIT位同时为1。这将停止操作并初始化内部控制寄存器。

当CTSUSTRT位为1时，不要将1写入CTSUINIT位。

CTSUTXVSEL位（CTSU发送电源选择）

CTSUTXVSEL位用于在互电容全扫描模式下切换发送缓冲器的电源。

对于任何其他模式或当VCC电压低于2.7V时，将该位设置为0。该位切换触摸IO的电源，由CTSUCHTRCn寄存器设置为发送。表46.5列出了TSm引脚的电源。当VCC电压因输出缓冲器的切换而大幅波动时，切换到内部逻辑电源可以减少对电压波动的影响。

Table 46.5 Power supplied to the TSm pins

Setting of CTSUCHTRCn Register	CTSUTXVSEL bit	Power supply of TSm pins
0 (Reception)	*	VCC
1 (Transmission)	0 (VCC)	
	1 (Internal logic power supply)	Internal logic power supply

46.2.2 CTSUCR1 : CTSU Control Register 1

Base address: CTSU = 0x400D_0000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUMD[1:0]		CTSUCLK[1:0]		CTSU ATUNE1	—	CTSU CSW	CTSU PON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CTSUPON	CTSU Power Supply Enable 0: Power off the CTSU 1: Power on the CTSU	R/W
1	CTSUCSW	CTSU LPF Capacitance Charging Control This bit controls charging of the LPF capacitance connected to the TSCAP pin. 0: Turn off capacitance switch 1: Turn on capacitance switch	R/W
2	—	This bit is read as 0. The write value should be 0.	R/W
3	CTSUATUNE1	CTSU Power Supply Capacity Adjustment 0: Normal output 1: High-current output	R/W
5:4	CTSUCLK[1:0]	CTSU Operating Clock Select 0 0: PCLKB 0 1: PCLKB/2 (PCLKB divided by 2) 1 0: PCLKB/4 (PCLKB divided by 4) 1 1: Setting prohibited	R/W
7:6	CTSUMD[1:0]	CTSU Measurement Mode Select 0 0: Self-capacitance single scan mode 0 1: Self-capacitance multiscan mode 1 0: Setting prohibited 1 1: Mutual capacitance full scan mode	R/W

Only set the CTSUCR1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPON bit (CTSU Power Supply Enable)

The CTSUPON bit controls the power supply to the CTSU. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUCSW bit (CTSU LPF Capacitance Charging Control)

The CTSUCSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off. After the capacitance switch is turned on, wait until the capacitance connected to the TSCAP pin is charged for the specified time before starting measurement by setting CTSUCR0.CTSUSTRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUATUNE1 bit (CTSU Power Supply Capacity Adjustment)

The CTSUATUNE1 bit sets the capacity of the CTSU power supply. Normally, set this bit to 0.

Table 46.5 为TSm引脚供电

CTSUTCHRCn寄存器CTSUTXVSEL位的设置		TSm管脚电源
0 (Reception)	*	VCC
1 (Transmission)	0 (VCC)	
	1（内部逻辑电源）内部逻辑电源	

46.2.2 CTSUCR1：CTSU控制寄存器1

Base address: CTSU = 0x400D_0000

Offset address: 0x01

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUMD[1:0]		CTSUCLK[1:0]		CTSU ATUNE1	—	CTSU CSW	CTSU PON
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	CTSUPON	CTSU电源使能 0：关闭CTSU1：打开C TSU	R/W
1	CTSUCSW	CTSULPF电容充电控制 该位控制连接到TSCAP引脚的LPF电容的充电。 0：关闭电容开关1：打开电容 开关	R/W
2	—	该位读取为0。写入值应为0。	R/W
3	CTSUATUNE1	CTSU电源容量调整 0：正常输出1：大电 流输出	R/W
5:4	CTSUCLK[1:0]	CTSU工作时钟选择 00：PCLKB01：PCLKB2（PCLKB2分 频）10：PCLKB4（PCLKB4分频）11 ：禁止设置	R/W
7:6	CTSUMD[1:0]	CTSU测量模式选择 00：自电容单扫描模式01：自电容多扫 描模式10：禁止设置11：互电容全扫描 模式	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCR1寄存器。

CTSUPON位（CTSU电源使能）

CTSUPON位控制CTSU的电源。将CTSUPON和CTSUCSW位设置为相同的值。

CTSUCSW位（CTSULPF电容充电控制）

CTSUCSW位通过打开或关闭电容开关来控制连接到TSCAP引脚的LPF电容的充电。电容开关打开后，通过设置CTSUCR0.CTSUSTRT为1，等到连接到TSCAP引脚的电容充电指定时间后开始测量。开始测量之前，使用IO端口输出低电平到TSCAP引脚，并对现有的LPF电容进行放电。将CTSUPON和CTSUCSW位设置为相同的值。

CTSUATUNE1位（CTSU电源容量调整）

CTSUATUNE1位设置CTSU电源的容量。通常，将此位设置为0。

CTSUCLK[1:0] bits (CTSU Operating Clock Select)

The CTSUCLK[1:0] bits select the operating clock.

CTSUMD[1:0] bits (CTSU Measurement Mode Select)

The CTSUMD[1:0] bits set the measurement mode. For details, see section 46.3.2. Measurement Modes.

46.2.3 CTSUSDPRS : CTSU Synchronous Noise Reduction Setting Register

Base address: CTSU = 0x400D_0000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	CTSU SOFF	CTSUPRMODE[1:0]		CTSUPRRATIO[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CTSUPRRATIO[3:0]	CTSU Measurement Time and Pulse Count Adjustment These bits set the measurement time and the measurement pulse count setting. Recommended setting: 3 (0011b)	R/W
5:4	CTSUPRMODE[1:0]	CTSU Base Period and Pulse Count Setting These bits set the base pulse count. 0 0: 510 pulses 0 1: 126 pulses 1 0: 62 pulses (recommended setting) 1 1: Setting prohibited	R/W
6	CTSUSOFF	CTSU High-Pass Noise Reduction Function Off Setting This bit turns spectrum diffusion on or off to reduce high-pass noise. 0: Turn on 1: Turn off	R/W
7	—	This bit is read as 0. The write value should be 0.	R/W

Only set the CTSUSDPRS register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPRRATIO[3:0] bits (CTSU Measurement Time and Pulse Count Adjustment)

The CTSUPRRATIO[3:0] bits are used to determine the measurement time and the measurement pulse count. These values are calculated using the following formulas, where the base pulse count is determined by the CTSUPRMODE[1:0] setting:

$$\text{Measurement pulse count} = \text{base pulse count} \times (\text{CTSUPRRATIO[3:0] bits} + 1)$$

$$\text{Measurement time} = (\text{base pulse count} \times (\text{CTSUPRRATIO[3:0] bits} + 1) + (\text{base pulse count} - 2) \times 0.25) \times \text{base clock cycle}$$

Note: For details on the base clock cycle, see section 46.2.17. CTSUSO1 : CTSU Sensor Offset Register 1.

CTSUPRMODE[1:0] bits (CTSU Base Period and Pulse Count Setting)

The CTSUPRMODE[1:0] bits select the number of base pulses that occur during measurement.

CTSUSOFF bit (CTSU High-Pass Noise Reduction Function Off Setting)

The CTSUSOFF bit turns on or off the function for reducing high-pass noise. Set this bit to 1 to turn the function off.

CTSUCLK[1:0]位（CTSU工作时钟选择）

CTSUCLK[1:0]位选择工作时钟。

CTSUMD[1:0]位（CTSU测量模式选择）

CTSUMD[1:0]位设置测量模式。有关详细信息，请参阅第46.3.2节。测量模式。

46.2.3 CTSUSDPRS:CTSU同步降噪设置寄存器

Base address: CTSU = 0x400D_0000

Offset address: 0x02

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	CTSU SOFF	CTSUPRMODE[1:0]		CTSUPRRATIO[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CTSUPRRATIO[3:0]	CTSU测量时间和脉冲计数调整 这些位设置测量时间和测量脉冲计数设置。 Recommended setting: 3 (0011b)	R/W
5:4	CTSUPRMODE[1:0]	CTSU基本周期和脉冲计数设置 这些位设置基本脉冲计数。 00：510脉冲01：126脉冲10：62脉冲 （推荐设置）11：禁止设置	R/W
6	CTSUSOFF	CTSU高通降噪功能关闭设置 该位打开或关闭频谱扩散以减少高通噪声。 0：开启1 ：关闭	R/W
7	—	该位读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUSDPRS寄存器。

CTSURRATIO[3:0]位（CTSU测量时间和脉冲计数调整）

CTSUPRRATIO[3:0]位用于确定测量时间和测量脉冲计数。这些值使用以下公式计算，其中基本脉冲计数由CTSUPRMODE[1:0]设置确定：

测量脉冲计数=基本脉冲计数×CTSUPRRATIO[3:0]位+1)

测量时间=基本脉冲计数×CTSUPRRATIO[3:0]位+1+基本脉冲计数−2×0.25×基本时钟周期)

Note: 有关基本时钟周期的详细信息，请参阅第46.2.17节。CTSUSO1：CTSU传感器偏移寄存器1。

CTSUPRMODE[1:0]位（CTSU基本周期和脉冲计数设置）

CTSUPRMODE[1:0]位选择测量期间出现的基本脉冲数。

CTSUSOFF位（CTSU高通降噪功能关闭设置）

CTSUSOFF位打开或关闭降低高通噪声的功能。将此位设置为1可关闭该功能。

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46.2.4 CTSUSST : CTSU Sensor Stabilization Wait Control Register

Base address: CTSU = 0x400D_0000

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUSST[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUSST[7:0]	CTSU Sensor Stabilization Wait Control Fix the value of these bits to 00010000b.	R/W

Only set the CTSUSST register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSST[7:0] bits (CTSU Sensor Stabilization Wait Control)

The CTSUSST[7:0] bits set the stabilization wait time for the TSCAP pin voltage. Always fix these bits to 00010000b. If these bits are not set, the TSCAP voltage will be unstable at the start of measurement, and the CTSU will be unable to obtain correct touch measurement results.

46.2.5 CTSUMCH0 : CTSU Measurement Channel Register 0

Base address: CTSU = 0x400D_0000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CTSHMCH0[4:0]				
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	CTSHMCH0[4:0]	CTSU Measurement Channel 0 In self-capacitance single scan mode, these bits set the channel to be measured. Other than when specified, starting measurement operation by setting CTSUCR0.CTSUSTRT to 1 is prohibited after these bits are set. In other measurement modes, these bits indicate the channel that is currently being measured. 0x00: TS00 0x01: TS01 ⋮ 0x12: TS18 0x13: TS19 0x1F: Measurement is being stopped. (Except in self-capacitance single scan mode)	R/W*1
7:5	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only enabled in self-capacitance single scan mode (CTSUCR1.CTSUMD[1:0] bits = 00b).

Only set the CTSUMCH0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSHMCH0[4:0] bits (CTSU Measurement Channel 0)

In self-capacitance single scan mode, the CTSHMCH0[4:0] bits set the channel to be measured. In this mode, only specify enabled channels (TS00 to TS19). In other modes, these indicate the receive channel that is being measured, and writing to these bits has no effect.

46.2.4 CTSUSST:CTSU传感器稳定等待控制寄存器

Base address: CTSU = 0x400D_0000

Offset address: 0x03

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUSST[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUSST[7:0]	CTSU传感器稳定等待控制将这些位的值 固定为00010000b。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUSST寄存器。

CTSUSST[7:0]位（CTSU传感器稳定等待控制）

CTSUSST[7:0]位设置TSCAP引脚电压的稳定等待时间。始终将这些位固定为00010000b。如果未设置这些位，TSCAP电压将在测量开始时不稳定，CTSU将无法获得正确的触摸测量结果。

46.2.5 CTSUCH0:CTSU测量通道寄存器0

Base address: CTSU = 0x400D_0000

Offset address: 0x04

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CTSHMCH0[4:0]				
重置后的值:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	CTSHMCH0[4:0]	CTSU测量通道0 在自电容单次扫描模式下，这些位设置要测量的通道。 除指定时，通过设置开始测量操作 设置这些位后，禁止CTSUCR0.CTSUSTRT为1。 在其他测量模式下，这些位指示当前正在测量的通道。 0x00: TS00 0x01: TS01 ⋮ 0x12: TS18 0x13: TS19 0x1F：测量正在停止。（自电容单次扫描模式除外）	R/W*1
7:5	—	这些位被读取为0。写入值应为0。	R/W

注1.写入这些位仅在自电容单次扫描模式下启用（CTSUCR1.CTSUMD[1:0]位=00b）。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUMCH0寄存器。

CTSHMCH0[4:0]位（CTSU测量通道0）

在自电容单次扫描模式下，CTSHMCH0[4:0]位设置要测量的通道。在此模式下，仅指定启用的通道（TS00到TS19）。在其他模式下，这些表示正在测量的接收通道，写入这些位无效。

46.2.6 CTSUMCH1 : CTSU Measurement Channel Register 1

Base address: CTSU = 0x400D_0000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CTSUMCH1[4:0]				
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	CTSUMCH1[4:0]	CTSU Measurement Channel 1 0x00: TS00 0x01: TS01 ⋮ 0x12: TS18 0x13: TS19 0x1F: Measurement is being stopped.	R
7:5	—	These bits are read as 0.	R

CTSUMCH1[4:0] bits (CTSU Measurement Channel 1)

In full scan mode, the CTSUMCH1[4:0] bits indicate the transmit channel that is being measured. They are always 0x1F when measurement is stopped, or in self-capacitance single scan and multi-scan modes.

46.2.7 CTSUCHAC0 : CTSU Channel Enable Control Register 0

Base address: CTSU = 0x400D_0000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHAC0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHAC0[7:0]	CTSU Channel Enable Control 0 These bits select whether the associated TS pin is measured. bit0 is associated with TS00 and bit7 with TS07. 0: Do not measure 1: Measure	R/W

Only set the CTSUCHAC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC0[7:0] bits (CTSU Channel Enable Control 0)

The CTSUCHAC0[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured.

46.2.6 CTSUCH1：CTSU测量通道寄存器1

Base address: CTSU = 0x400D_0000

Offset address: 0x05

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	CTSUMCH1[4:0]				
重置后的值：	0	0	0	1	1	1	1	1

Bit	Symbol	Function	R/W
4:0	CTSUMCH1[4:0]	CTSU测量通道1 0x00: TS00 0x01: TS01 ⋮ 0x12: TS18 0x13: TS19 0x1F：测量正在停止。	R
7:5	—	这些位读为0。	R

CTSUCH1[4:0]位（CTSU测量通道1）

在全扫描模式下，CTSUMCH1[4:0]位指示正在测量的发送通道。停止测量时，或在自电容单次扫描和多次扫描模式下，它们始终为0x1F。

46.2.7 CTSUCHAC0：CTSU通道使能控制寄存器0

Base address: CTSU = 0x400D_0000

Offset address: 0x06

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHAC0[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHAC0[7:0]	CTSU通道使能控制0 这些位选择是否测量相关的TS引脚。bit0与TS00相关联，而bit7与TS07相关联。 0：不测量1：测量	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC0寄存器。

CTSUCHAC0[7:0]位（CTSU通道使能控制0）

CTSUCHAC0[7:0]位选择要测量其静电电容的接收和发送引脚。

46.2.8 CTSUCHAC1 : CTSU Channel Enable Control Register 1

Base address: CTSU = 0x400D_0000

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHAC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHAC1[7:0]	CTSU Channel Enable Control 1 These bits select whether the associated TS pin is measured. bit0 is associated with TS08 and bit7 with TS15. 0: Do not measure 1: Measure	R/W

Only set the CTSUCHAC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC1[7:0] bits (CTSU Channel Enable Control 1)

The CTSUCHAC1[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured.

46.2.9 CTSUCHAC2 : CTSU Channel Enable Control Register 2

Base address: CTSU = 0x400D_0000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CTSUCHAC2[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CTSUCHAC2[3:0]	CTSU Channel Enable Control 2 These bits select whether the associated TS pin is measured. bit0 is associated with TS16 and bit3 with TS19. 0: Do not measure 1: Measure	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUCHAC2 register when the CTSUCR0.CTSUSTRT bit = 0.

CTSUCHAC2[3:0] bits (CTSU Channel Enable Control 2)

The CTSUCHAC2[3:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured.

46.2.10 CTSUCHTRC0 : CTSU Channel Transmit/Receive Control Register 0

Base address: CTSU = 0x400D_0000

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHTRC0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

46.2.8 CTSUCHAC1：CTSU通道使能控制寄存器1

Base address: CTSU = 0x400D_0000

Offset address: 0x07

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHAC1[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHAC1[7:0]	CTSU通道使能控制1 这些位选择是否测量相关的TS引脚。bit0与TS08相关联，而bit7与TS15相关联。 0：不测量1：测量	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC1寄存器。

CTSUCHAC1[7:0]位（CTSU通道使能控制1）

CTSUCHAC1[7:0]位选择要测量其静电电容的接收和发送引脚。

46.2.9 CTSUCHAC2：CTSU通道使能控制寄存器2

Base address: CTSU = 0x400D_0000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CTSUCHAC2[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CTSUCHAC2[3:0]	CTSU通道启用控制2 这些位选择是否测量相关的TS引脚。bit0与TS16相关联，而bit3与TS19相关联。 0：不测量1：测量	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位=0时设置CTSUCHAC2寄存器。

CTSUCHAC2[3:0]位（CTSU通道使能控制2）

CTSUCHAC2[3:0]位选择要测量其静电电容的接收和发送引脚。

46.2.10 CTSUCHTRC0：CTSU通道发送接收控制寄存器0

Base address: CTSU = 0x400D_0000

Offset address: 0x0B

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHTRC0[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHTRC0[7:0]	CTSU Channel Transmit/Receive Control 0 bit0 is associated with TS00 and bit7 with TS07. 0: Reception 1: Transmission	R/W

Only set the CTSUCHTRC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC0[7:0] bits (CTSU Channel Transmit/Receive Control 0)

In full scan mode, the CTSUCHTRC0[7:0] bits allocate reception or transmission to the associated TS pins. The setting is ignored in self-capacitance single scan and multi-scan modes.

46.2.11 CTSUCHTRC1 : CTSU Channel Transmit/Receive Control Register 1

Base address: CTSU = 0x400D_0000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHTRC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHTRC1[7:0]	CTSU Channel Transmit/Receive Control 1 bit0 is associated with TS08 and bit7 with TS15. 0: Reception 1: Transmission	R/W

Only set the CTSUCHTRC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC1[7:0] bits (CTSU Channel Transmit/Receive Control 1)

In full scan mode, the CTSUCHTRC1[7:0] bits allocate reception or transmission to the associated TS pins. The setting is ignored in self-capacitance single scan and multiscan modes.

46.2.12 CTSUCHTRC2 : CTSU Channel Transmit/Receive Control Register 2

Base address: CTSU = 0x400D_0000

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CTSUCHTRC2[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CTSUCHTRC2[3:0]	CTSU Channel Transmit/Receive Control 2 bit0 is associated with TS16 and bit3 with TS19. 0: Reception 1: Transmission	R/W
7:4	—	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUCHTRC2 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC2[3:0] bits (CTSU Channel Transmit/Receive Control 2)

In full scan mode, the CTSUCHTRC2[3:0] bits allocate reception or transmission to the associated TS pins. The setting is ignored in self-capacitance single scan and multiscan modes.

Bit	Symbol	Function	R/W
7:0	CTSUCHTRC0[7:0]	CTSU通道发送接收控制0位0与TS00相关联，位7与TS07相关联。 0：接收1：发送	R/W

仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC0寄存器。

CTSUCHTRC0[7:0]位（CTSU通道发送接收控制0）

在全扫描模式下，CTSUCHTRC0[7:0]位将接收或发送分配给相关的TS引脚。在自电容单次扫描和多次扫描模式下，该设置被忽略。

46.2.11 CTSUCHTRC1：CTSU通道发送接收控制寄存器1

Base address: CTSU = 0x400D_0000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUCHTRC1[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSUCHTRC1[7:0]	CTSU通道发送接收控制1位0与TS08相关联，位7与TS15相关联。 0：接收1：发送	R/W

仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC1寄存器。

CTSUCHTRC1[7:0]位（CTSU通道发送接收控制1）

在全扫描模式下，CTSUCHTRC1[7:0]位将接收或发送分配给相关的TS引脚。在自电容单扫描和多扫描模式下，该设置被忽略。

46.2.12 CTSUHTRC2：CTSU通道发送接收控制寄存器2

Base address: CTSU = 0x400D_0000

Offset address: 0x0D

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CTSUCHTRC2[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
3:0	CTSUCHTRC2[3:0]	CTSU通道发送接收控制2位0与TS16相关联，位3与TS19相关联。 0：接收1：发送	R/W
7:4	—	这些位被读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC2寄存器。

CTSUCHTRC2[3:0]位（CTSU通道发送接收控制2）

在全扫描模式下，CTSUCHTRC2[3:0]位将接收或发送分配给相关的TS引脚。在自电容单扫描和多扫描模式下，该设置被忽略。

46.2.13 CTSUDCLKC : CTSU High-Pass Noise Reduction Control Register

Base address: CTSU = 0x400D_0000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CTSUSSMOD[1:0]	CTSU Diffusion Clock Mode Select Set these bits to 00b.	R/W
3:2	—	These bits are read as 0. The write value should be 0.	R/W
5:4	CTSUSSCNT[1:0]	CTSU Diffusion Clock Mode Control Set these bits to 11b.	R/W
7:6	—	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUDCLKC register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSSMOD[1:0] bits (CTSU Diffusion Clock Mode Select)

The CTSUSSMOD[1:0] bits set the mode of the spectrum diffusion clock for high-pass noise reduction. When using the high-pass function, always fix these bits to 00b. If these bits are not set, the CTSU will be unable to effectively reduce high-pass noise.

CTSUSSCNT[1:0] bits (CTSU Diffusion Clock Mode Control)

The CTSUSSCNT[1:0] bits adjust the amount of spectrum diffusion applied to reduce high-pass noise. When using the high-pass noise reduction function, always fix these bits to 11b. If these bits are not set, touch measurement might be performed incorrectly.

46.2.14 CTSUST : CTSU Status Register

Base address: CTSU = 0x400D_0000

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CTSUSTC[2:0]	CTSU Measurement Status Counter These counters indicate the current measurement status. 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5	R
3	—	This bit is read as 0. The write value should be 0.	R/W
4	CTSUDTSR	CTSU Data Transfer Status Flag This flag indicates whether the measurement result stored in the sensor counter and the reference counter was read. 0: Read 1: Not read	R

46.2.13 CTSUDCLKC:CTSU高通降噪控制寄存器

Base address: CTSU = 0x400D_0000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CTSUSSMOD[1:0]	CTSU扩散时钟模式选择 将这些位设置为00b。	R/W
3:2	—	这些位被读取为0。写入值应为0。	R/W
5:4	CTSUSSCNT[1:0]	CTSU扩散时钟模式控制 将这些位设置为11b。	R/W
7:6	—	这些位被读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUDCLKC寄存器。

CTSUSSMOD[1:0]位（CTSU扩散时钟模式选择）

CTSUSSMOD[1:0]位设置频谱扩散时钟的模式以降低高通噪声。使用高通功能时，请始终将这些位固定为00b。如果未设置这些位，CTSU将无法有效降低高通噪声。

CTSUSSCNT[1:0]位（CTSU扩散时钟模式控制）

CTSUSSCNT[1:0]位调整应用的频谱扩散量以减少高通噪声。使用高通降噪功能时，请始终将这些位固定为11b。如果未设置这些位，则可能会错误地执行触摸测量。

46.2.14 CTSUST:CTSU状态寄存器

Base address: CTSU = 0x400D_0000

Offset address: 0x11

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	CTSUSTC[2:0]	CTSU测量状态计数器 这些计数器指示当前的测量状态。 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5	R
3	—	该位读取为0。写入值应为0。	R/W
4	CTSUDTSR	CTSU数据传输状态标志 该标志指示存储在传感器计数器和参考计数器中的测量结果是否被读取。 0：读取1： 未读取	R

Bit	Symbol	Function	R/W
5	CTSUSOVF	CTSU Sensor Counter Overflow Flag This flag indicates an overflow on the sensor counter. 0: No overflow occurred 1: Overflow occurred	R/W
6	CTSUROVF	CTSU Reference Counter Overflow Flag This flag indicates an overflow on the reference counter. 0: No overflow occurred 1: Overflow occurred	R/W
7	CTSUPS	CTSU Mutual Capacitance Status Flag This flag indicates the measurement status in mutual capacitance full scan mode. 0: First measurement 1: Second measurement	R

When using the CTSUCR0.CTSUINIT bit to clear an overflow flag, make sure that the CTSUCR0.CTSUSTRT bit is 0.

CTSUSTC[2:0] flags (CTSU Measurement Status Counter)

The CTSUSTC[2:0] flags are a counter indicating the current measurement status. For details on each status, see section 46.3.2.2. Status counter.

CTSUDTSR flag (CTSU Data Transfer Status Flag)

The CTSUDTSR flag indicates whether the measurement result stored in the sensor counter and the reference counter was read. The flag sets to 1 when measurement completes and 0 when the reference counter is read by software or the DTC. The flag can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUSOVF flag (CTSU Sensor Counter Overflow Flag)

The CTSUSOVF flag sets to 1 when the sensor counter, CTSUSC, overflows. On overflow, the counter value reads as 0xFFFF. Measurement processing continues for the specified period.

No interrupt occurs on an overflow. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. It can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUROVF flag (CTSU Reference Counter Overflow Flag)

The CTSUROVF flag sets to 1 when the reference counter, CTSURC, overflows. On overflow, the counter value reads as 0xFFFF. Measurement processing continues for the specified period.

No interrupt occurs on an overflow. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. It can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUPS flag (CTSU Mutual Capacitance Status Flag)

In mutual capacitance full scan mode, when CTSUCR1.CTSUMD[1:0] = 11b, the CTSUPS flag indicates whether the measurement is the first or second of two measurements for each channel. When measurement is stopped or in other measurement modes, this flag is always 0.

46.2.15 CTSUSSC : CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register

Base address: CTSU = 0x400D_0000

Offset address: 0x12

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5	CTSUSOVF	CTSU传感器计数器溢出标志 该标志表示传感器计数器溢出。 0：未发生溢出1：发生溢出	R/W
6	CTSUROVF	CTSU参考计数器溢出标志 该标志表示参考计数器溢出。 0：未发生溢出1：发生溢出	R/W
7	CTSUPS	CTSU互电容状态标志 该标志指示互电容全扫描模式下的测量状态。 0：第一次测量1：第二次测量	R

使用CTSUCR0.CTSUINIT位清除溢出标志时，请确保CTSUCR0.CTSUSTRT位为0。

CTSUSTC[2:0]标志（CTSU测量状态计数器）

CTSUSTC[2:0]标志是指示当前测量状态的计数器。有关每个状态的详细信息，请参阅第46.3.2.2节。状态计数器。

CTSUDTSR标志（CTSU数据传输状态标志）

CTSUDTSR标志指示存储在传感器计数器和参考计数器中的测量结果是否被读取。当测量完成时，该标志设置为1，当软件或DTC读取参考计数器时，该标志设置为0。也可以使用CTSUCR0.CTSUINIT位清除该标志。

CTSUSOVF标志（CTSU传感器计数器溢出标志）

当传感器计数器CTSUSC溢出时，CTSUSOVF标志设置为1。溢出时，计数器值读取为0xFFFF。测量处理持续指定的时间。

溢出时不发生中断。要确定发生溢出的通道，请在测量完成后读取每个通道的测量结果，由测量结束中断发出信号。

当软件读取1后写入0时清除该标志。它也可以使用CTSUCR0.CTSUINIT位清零。

CTSUROVF标志（CTSU参考计数器溢出标志）

当参考计数器CTSURC溢出时，CTSUROVF标志设置为1。溢出时，计数器值读取为0xFFFF。测量处理持续指定的时间。

溢出时不发生中断。要确定发生溢出的通道，请在测量完成后读取每个通道的测量结果，由测量结束中断发出信号。

当软件读取1后写入0时清除该标志。它也可以使用CTSUCR0.CTSUINIT位清零。

CTSUPS标志（CTSU互电容状态标志）

在互电容全扫描模式下，当CTSUCR1.CTSUMD[1:0]=11b时，CTSUPS标志指示测量是每个通道的两次测量中的第一个还是第二个。当测量停止或处于其他测量模式时，该标志始终为0。

46.2.15 CTSUSSC:CTSU高通降噪频谱扩散控制 Register

Base address: CTSU = 0x400D_0000

Offset address: 0x12

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	—	These bits are read as 0. The write value should be 0.	R/W
11:8	CTSUSSDIV[3:0]	CTSU Spectrum Diffusion Frequency Division Setting These bits specify the spectrum diffusion frequency division setting based on the base clock frequency division setting.	R/W
15:12	—	These bits are read as 0. The write value should be 0.	R/W

CTSUSSDIV[3:0] bits (CTSU Spectrum Diffusion Frequency Division Setting)

The CTSUSSDIV[3:0] bits specify the spectrum diffusion frequency derived from the base clock frequency division setting. To calculate the correct setting for CTSUSSDIV[3:0], see the relationship between base clock frequencies and the settings in Table 46.6.

Table 46.6 Relationship between base clock frequencies and CTSUSSDIV[3:0] bits settings

Base clock frequency fb (MHz)	CTSUSSDIV[3:0] bit setting
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

46.2.16 CTSUSO0 : CTSU Sensor Offset Register 0

Base address: CTSU = 0x400D_0000

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSUSNUM[5:0]						CTSUSO[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	CTSUSO[9:0]	CTSU Sensor Offset Adjustment These bits adjust the electronic capacitance when the electrode is not being touched. 0x000: Current offset is 0. 0x001: Current offset is 1. 0x002: Current offset is 2. ⋮ ⋮ 0x3FE: Current offset is 1022. 0x3FF: Current offset is maximum.	R/W

Bit	Symbol	Function	R/W
7:0	—	这些位被读取为0。写入值应为0。	R/W
11:8	CTSUSSDIV[3:0]	CTSU频谱扩散频分设置 这些位指定基于基本时钟分频设置的频谱扩散分频设置。	R/W
15:12	—	这些位被读取为0。写入值应为0。	R/W

CTSUSSDIV[3:0]位（CTSU频谱扩散频分设置）

CTSUSSDIV[3:0]位指定从基本时钟分频设置得出的频谱扩散频率。
要计算CTSUSSDIV[3:0]的正确设置，请参见表46.6中基本时钟频率和设置之间的关系。

Table 46.6 基本时钟频率与CTSUSSDIV[3:0]位设置之间的关系

基本时钟频率fb(MHz)	CTSUSSDIV[3:0]位设置
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

46.2.16 CTSUSO0：CTSU传感器偏移寄存器0

Base address: CTSU = 0x400D_0000

Offset address: 0x14

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSUSNUM[5:0]						CTSUSO[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	CTSUSO[9:0]	CTSU传感器偏移调整 这些位在电极未被触摸 时调整电子电容。 0x000：当前偏移为0。0x 001：当前偏移为1。0x00 2：当前偏移为2。 ⋮ ⋮ 0x3FE：当前偏移量为1022。0x3FF ：当前偏移量最大。	R/W

Bit	Symbol	Function	R/W
15:10	CTSUSNUM[5:0]	CTSU Measurement Count Setting These bits set the number of measurements.	R/W

CTSUSO[9:0] bits (CTSU Sensor Offset Adjustment)

The CTSUSO[9:0] bits offset the sensor ICO input current generated from electrostatic capacitance during touch measurement when the electrode is not being touched. This prevents the CTSU sensor counter from overflowing. Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt occurs.

CTSUSNUM[5:0] bits (CTSU Measurement Count Setting)

The CTSUSNUM[5:0] bits specify how many times the measurement pulse count specified in the CTSUSDPRS.CTSUPRRATIO[3:0] and CTSUSDPRS.CTSUPRMODE[1:0] bits is repeated during the measurement time. The measurement pulse count is repeated (CTSUSNUM[5:0] bits + 1) times. Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt is generated.

46.2.17 CTSUSO1 : CTSU Sensor Offset Register 1

Base address: CTSU = 0x400D_0000

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSURICOA[7:0]	CTSU Reference ICO Current Adjustment These bits adjust the input current of the reference ICO. 0x00: Current offset is 0 0x01: Current offset is 1 0x02: Current offset is 2 ⋮ 0xFE: Current offset is 254 0xFF: Current offset is maximum.	R/W

Bit	Symbol	Function	R/W
15:10	CTSUSNUM[5:0]	CTSU测量计数设置 这些位设置测量次数。	R/W

CTSUSO[9:0]位（CTSU传感器偏移调整）

CTSUSO[9:0]位在电极未被触摸 时在触摸测量期间抵消由静电电容产生的传感器ICO输入电流。这可以防止CTSU传感器计数器溢出。在发生CTSU_CTSUWR中断后设置接下来要测量的TS引脚。

CTSUSNUM[5:0]位（CTSU测量计数设置）

CTSUSNUM[5:0]位指定测量脉冲计数的次数
CTSUSDPRS.CTSUPRRATIO[3:0]和CTSUSDPRS.CTSUPRMODE[1:0]位在测量期间重复。测量脉冲计数重复(CTSUSNUM[5:0]位+1)次。在产生CTSU_CTSUWR中断后设置接下来要测量的TS引脚。

46.2.17 CTSUSO1：CTSU传感器偏移寄存器1

Base address: CTSU = 0x400D_0000

Offset address: 0x16

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	CTSURICOA[7:0]	CTSU参考ICO电流调整 这些位调整参考ICO的输入电流。 0x00：当前偏移为00x0 1：当前偏移为10x02： 当前偏移为2 ⋮ 0xFE：当前偏移量为2540xFF：当 前偏移量最大。	R/W

Bit	Symbol	Function	R/W
12:8	CTSUSDPA[4:0]	CTSU Base Clock Setting These bits are used to generate the base clock. 0x00: Operating clock divided by 2*1 0x01: Operating clock divided by 4 0x02: Operating clock divided by 6 0x03: Operating clock divided by 8 0x04: Operating clock divided by 10 0x05: Operating clock divided by 12 0x06: Operating clock divided by 14 0x07: Operating clock divided by 16 0x08: Operating clock divided by 18 0x09: Operating clock divided by 20 0x0A: Operating clock divided by 22 0x0B: Operating clock divided by 24 0x0C: Operating clock divided by 26 0x0D: Operating clock divided by 28 0x0E: Operating clock divided by 30 0x0F: Operating clock divided by 32 0x10: Operating clock divided by 34 0x11: Operating clock divided by 36 0x12: Operating clock divided by 38 0x13: Operating clock divided by 40 0x14: Operating clock divided by 42 0x15: Operating clock divided by 44 0x16: Operating clock divided by 46 0x17: Operating clock divided by 48 0x18: Operating clock divided by 50 0x19: Operating clock divided by 52 0x1A: Operating clock divided by 54 0x1B: Operating clock divided by 56 0x1C: Operating clock divided by 58 0x1D: Operating clock divided by 60 0x1E: Operating clock divided by 62 0x1F: Operating clock divided by 64	R/W
14:13	CTSUICOG[1:0]	CTSU ICO Gain Adjustment These bits adjust the output frequency gain of the sensor ICO and the reference ICO. 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain	R/W
15	—	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not set the CTSUSDPA[4:0] bits set to 00000b while the high-pass noise reduction function is turned off (CTSUSDPRS.CTSUSOFF bit = 1) in mutual capacitance full scan mode (CTSUCR1.CTSUMD[1:0] bits = 11b).

After a CTSU_CTSUWR interrupt occurs, write first to the CTSUSSC register, next to the CTSUSO0 register, and then to the CTSUSO1 register. The write to the CTSUSO1 register causes a transition to Status 3. (See Table 46.7 and Table 46.8.) Set all of the bits in a single operation when writing to the CTSUSO1 register.

CTSURICOA[7:0] bits (CTSU Reference ICO Current Adjustment)

The CTSURICOA[7:0] bits adjust the oscillation frequency using the input current of the reference ICO.

CTSUSDPA[4:0] bits (CTSU Base Clock Setting)

The CTSUSDPA[4:0] bits select the base clock used as the source for the sensor drive pulse by dividing the operating clock. For details on the setting procedure, see section 46.3.2.1. Initial settings flow.

CTSUICOG[1:0] bits (CTSU ICO Gain Adjustment)

The CTSUICOG[1:0] bits adjust the output frequency gain of the sensor ICO and the reference ICO. Normally, set these bits to 00b for the maximum gain. If changes in the capacitance between when the electrode is touched and when it is not touched greatly exceed the dynamic range of the sensor ICO, adjust the gain appropriately with this setting.

Bit	Symbol	Function	R/W
12:8	CTSUSDPA[4:0]	CTSU基本时钟设置 这些位用于生成基本时钟。 0x00：工作时钟除以2*1 0x01：工作时钟4分频0x02：工作时钟6分频0x03：工作时钟8分频0x04：工作时钟10分频0x05：工作时钟12分频0x06：工作时钟14分频0x07：工作时钟16分频0x08:工作时钟除以180x09:工作时钟除以200x0A:工作时钟除以220x0B:工作时钟除以240x0C:工作时钟除以260x0D:工作时钟除以280x0E:工作时钟除以300x0F:工作时钟32分频0x10：工作时钟34分频0x11：工作时钟36分频0x12：工作时钟38分频0x13：工作时钟40分频0x14：工作时钟42分频0x15：工作时钟44分频0x16：工作时钟时钟46分频0x17：工作时钟48分频0x18：工作时钟50分频0x19：工作时钟52分频0x1A：工作时钟54分频0x1B：工作时钟56分频0x1C：工作时钟分频by580x1D：工作时钟除以600x1E：工作时钟除以620x1F：工作时钟除以64	R/W
14:13	CTSUICOG[1:0]	CTSUICO增益调整 这些位调整传感器ICO和参考ICO的输出频率增益。 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain	R/W
15	—	该位读取为0。写入值应为0。	R/W

注1.关闭高通降噪功能时，请勿将CTSUSDPA[4:0]位设置为00000b（CTSUSDPRS.CTSUSOFF位=1）在互电容全扫描模式下（CTSUCR1.CTSUMD[1:0]位=11b）。

发生CTSU_CTSUWR中断后，先写入CTSUSSC寄存器，然后写入CTSUSO0寄存器，然后写入CTSUSO1寄存器。写入CTSUSO1寄存器会导致转换到状态3。（参见表46.7和表46.8。）在写入CTSUSO1寄存器时，在一次操作中设置所有位。

CTSURICOA[7:0]位（CTSU参考ICO电流调整）

CTSURICOA[7:0]位使用参考ICO的输入电流调整振荡频率。

CTSUSDPA[4:0]位（CTSU基本时钟设置）

CTSUSDPA[4:0]位通过对工作时钟进行分频来选择用作传感器驱动脉冲源的基本时钟。
有关设置步骤的详细信息，请参阅第46.3.2.1节。初始设置流程。

CTSUICOG[1:0]位（CTSUICO增益调整）

CTSUICOG[1:0]位调整传感器ICO和参考ICO的输出频率增益。通常，将这些位设置为00b以获得最大增益。如果触摸电极和未触摸电极之间的电容变化大大超过传感器ICO的动态范围，请使用此设置适当调整增益。

46.2.18 CTSUSC : CTSU Sensor Counter

Base address: CTSU = 0x400D_0000

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSUSC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CTSUSC[15:0]	CTSU Sensor Counter These bits indicate the measurement result of the sensor ICO. They read 0xFFFF when an overflow occurs.	R

After a CTSU_CTSURD interrupt occurs, read first from the CTSUSC counter and then from the CTSURC counter.

CTSUSC[15:0] bits (CTSU Sensor Counter)

The CTSUSC[15:0] bits are configured as an increment counter for the sensor ICO clock. Read these bits after a CTSU_CTSURD interrupt occurs. After the CTSURC counter is read, these bits are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags changes to 100b) in the next measurement. They can also be cleared using the CTSUCR0.CTSUINIT bit.

46.2.19 CTSURC : CTSU Reference Counter

Base address: CTSU = 0x400D_0000

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSURC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CTSURC[15:0]	CTSU Reference Counter These bits indicate the measurement result of the reference ICO. They read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt occurs, read first from the CTSUSC counter and then from the CTSURC counter.

Status 3 continues until the CTSURC counter is read, even if the stabilization time specified for Status 3 elapses.

CTSURC[15:0] bits (CTSU Reference Counter)

The CTSURC[15:0] bits are configured as an increment counter for the reference ICO clock. The reference ICO optimizes touch measurement performed by the sensor ICO. There is some deviation depending on the internal sensor ICO and the reference ICO in the CTSU, but both ICOs have almost the same characteristics, including the dynamic range and the current-to-frequency characteristics. The range of current amount that can be set in the reference ICO current adjustment bits is about the same as the dynamic range of both ICOs, and the current amount input to the sensor ICO must be within this dynamic range. To ensure this, use the reference ICO to check the differences between the ICOs and measure the current-to-oscillation frequency characteristics. Because the reference ICO oscillation frequency can be obtained from the reference ICO counter, the ICO oscillation frequency (counter value/measurement time) for the input current amount can be measured by setting the value in the reference ICO current adjustment bits and measuring the reference ICO counter. The reference ICO counter value measured using the maximum value in the reference ICO current adjustment bits is the maximum value of the ICO dynamic range. The current to the sensor ICO must be offset in the offset adjustment bits so that the sensor ICO counter value does not exceed this value.

46.2.18 CTSUSC:CTSU传感器计数器

Base address: CTSU = 0x400D_0000

Offset address: 0x18

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSUSC[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CTSUSC[15:0]	CTSU传感器计数器 这些位表示传感器ICO的测量结果。当发生溢出时，它们读取0xFFFF。	R

发生CTSU_CTSURD中断后，先从CTSUSC计数器读取，然后再从CTSURC计数器读取。

CTSUSC[15:0]位（CTSU传感器计数器）

CTSUSC[15:0]位配置为传感器ICO时钟的增量计数器。后读取这些位
CTSU_CTSURD中断发生。读取CTSURC计数器后，在下一次测量中CTSU测量状态计数器值变为状态4（CTSUST.CTSUSTC[2:0]标志变为100b）之前，立即清除这些位。它们也可以使用CTSUCR0.CTSUINIT位清零。

46.2.19 CTSURC:CTSU参考计数器

Base address: CTSU = 0x400D_0000

Offset address: 0x1A

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSURC[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	CTSURC[15:0]	CTSU参考计数器 这些位表示参考ICO的测量结果。它们在发生溢出时读取FFFFh。	R

发生CTSU_CTSURD中断后，先从CTSUSC计数器读取，然后再从CTSURC计数器读取。

状态3一直持续到读取CTSURC计数器为止，即使为状态3指定的稳定时间已过。

CTSURC[15:0]位（CTSU参考计数器）

CTSURC[15:0]位配置为参考ICO时钟的增量计数器。参考ICO优化了传感器ICO执行的触摸测量。CTSU中的内部传感器ICO和参考ICO存在一些偏差，但两种ICO具有几乎相同的特性，包括动态范围和电流频率特性。参考ICO电流调整位可设置的电流量范围与两个ICO的动态范围大致相同，输入到传感器ICO的电流量必须在此动态范围内。为确保这一点，请使用参考ICO检查ICO之间的差异并测量电流-振荡频率特性。因为可以从参考ICO计数器获得参考ICO振荡频率，所以可以通过设置参考ICO电流调整位中的值并测量参考ICO计数器来测量输入电流量的ICO振荡频率（计数器值测量时间）.使用参考ICO电流调整位中的最大值测量的参考ICO计数器值是ICO动态范围的最大值。传感器ICO的电流必须在偏移调整位中进行偏移，以使传感器ICO计数器值不超过此值。

Read the CTSURC[15:0] bits after a CTSU_CTSURD interrupt occurs. After these bits are read, they are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags changes to 100b) in the next measurement. They can also be cleared using the CTSUCR0.CTSUINIT bit.

46.2.20 CTSUERRS : CTSU Error Status Register

Base address: CTSU = 0x400D_0000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSUICOMP	—	—	—	—	—	—	—	CTSUTSOC	—	—	—	CTSUDRV	CTSUTSOD	CTSUSPMD[1:0]	
Value after reset:	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CTSUSPMD[1:0]	Calibration Mode 0 0: Capacitance measurement mode 1 0: Calibration mode Others: Seting prohibited	R/W
2	CTSUTSOD	TS Pin Fixed Output 0: Capacitance measurement mode 1: TS pins are forced to be high or low	R/W
3	CTSUDRV	Calibration Setting 1 0: Capacitance measurement mode 1: Calibration setting 1	R/W
6:4	—	These bits are read as 0. The write value should be 0.	R/W
7	CTSUTSOC	Calibration Setting 2 0: Capacitance measurement mode 1: Calibration setting 2	R/W
14:8	—	These bits are read as 0. The write value should be 0.	R/W
15	CTSUICOMP	TSCAP Voltage Error Monitor 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage	R

CTSUSPMD[1:0] bits (Calibration Mode)

The CTSUSPMD[1:0] bits are used to calibrate the CTSU. When measuring the capacitance, set these bits to 00b.

CTSUTSOD bit (TS Pin Fixed Output)

The CTSUTSOD bit is used to calibrate the CTSU. When setting this bit to 1, the TS pins are forced to the logic level specified by the CTSUCR0.CTSUIOC bit. When measuring the capacitance, set this bit to 0.

CTSUDRV bit (Calibration Setting 1)

The CTSUDRV bit is used to calibrate the CTSU. When measuring the capacitance, set this bit to 0.

CTSUTSOC bit (Calibration Setting 2)

The CTSUTSOC bit is used to calibrate the CTSU. When measuring capacitance, set this bit to 0.

CTSUICOMP bit (TSCAP Voltage Error Monitor)

If the offset current amount set in the CTSUSO1 register exceeds the sensor ICO input current during touch measurement, the TSCAP voltage becomes abnormal and touch measurement cannot be performed correctly. The CTSUICOMP bit monitors the TSCAP voltage and it sets to 1 if the voltage becomes abnormal.

If the TSCAP voltage becomes abnormal, the sensor ICO counter value becomes undefined, but touch measurement completes normally, so it is difficult to detect an abnormality by reading the sensor ICO counter value. If the CTSU reference ICO current adjustment bits (CTSURICOA[7:0]) in the CTSUSO1 register are set to any value other than 0, always check this bit when touch measurement completes.

在CTSU_CTSURD中断发生后读取CTSURC[15:0]位。读取这些位后，在CTSU测量状态计数器值在下一次测量中立即变为状态4（CTSUST.CTSUSTC[2:0]标志变为100b）之前将它们清零。它们也可以使用CTSUCR0.CTSUINIT位清零。

46.2.20 CTSUERRS:CTSU错误状态寄存器

Base address: CTSU = 0x400D_0000

Offset address: 0x1C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CTSUICOMP	—	—	—	—	—	—	—	CTSUTSOC	—	—	—	CTSUDRV	CTSUTSOD	CTSUSPMD[1:0]	
重置后的值：	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	CTSUSPMD[1:0]	校准模式 00：电容测量模式10：校准模式 Others: Seting prohibited	R/W
2	CTSUTSOD	TS引脚固定输出 0：电容测量模式1：TS引脚强制为高电平或低电平	R/W
3	CTSUDRV	校准设置1 0：电容测量模式1：校准设置1	R/W
6:4	—	这些位被读取为0。写入值应为0。	R/W
7	CTSUTSOC	校准设置2 0：电容测量模式1：校准设置2	R/W
14:8	—	这些位被读取为0。写入值应为0。	R/W
15	CTSUICOMP	TSCAP电压错误监视器 0：正常TSCAP电压1：异常TSCAP电压	R

CTSUSPMD[1:0] bits (Calibration Mode)

CTSUSPMD[1:0]位用于校准CTSU。测量电容时，将这些位设置为00b。

CTSUTSOD位（TS引脚固定输出）

CTSUTSOD位用于校准CTSU。将该位设置为1时，TS引脚被强制为CTSUCR0.CTSUIC位指定的逻辑电平。测量电容时，将此位设置为0。

CTSUDRV位（校准设置1）

CTSUDRV位用于校准CTSU。测量电容时，将此位设置为0。

CTSUTSOC位（校准设置2）

CTSUTSOC位用于校准CTSU。测量电容时，将此位设置为0。

CTSUICOMP位（TSCAP电压错误监视器）

如果CTSUSO1寄存器中设置的偏移电流量在触摸测量期间超过传感器ICO输入电流，则TSCAP电压会异常，无法正确执行触摸测量。CTSUICOMP位监控TSCAP电压，如果电压异常，它设置为1。

如果TSCAP电压异常，传感器ICO计数器值变得不确定，但触摸测量正常完成，因此很难通过读取传感器ICO计数器值来检测异常。如果CTSUSO1寄存器中的CTSU参考ICO电流调整位(CTSURICOA[7:0])设置为0以外的任何值，则在触摸测量完成时始终检查该位。

This bit is cleared by writing 0 to the CTSUCR1.CTSUPON bit and turning off the power supply.

46.2.21 CTSUTRMR : CTSU Reference Current Calibration Register

Base address: CTSU = 0x400D_0000

Offset address: 0x20

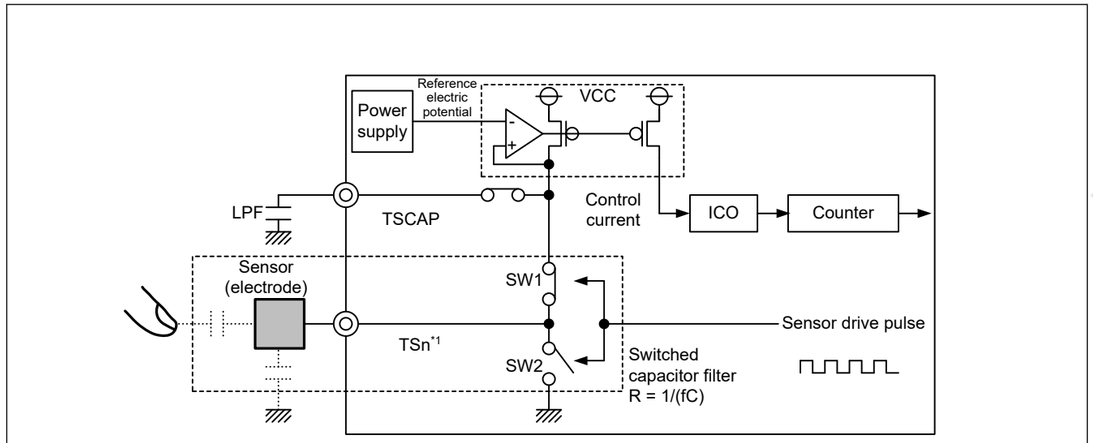
Bit position:	7	6	5	4	3	2	1	0
Bit field:								
Value after reset:	Unique value for each chip							

The CTSUTRMR resister stores a reference current value calibrated under the specified condition for each chip at factory shipment. When rewriting this register, set the CTSUERRS.CTSUSPMD[1:0] bits to 10b (calibration mode). When resetting the MCU, the values returns to the factory setting value. Do not rewrite this register when the CTSUSPMD[1:0] bits are 00b (capacitance measurement mode).

46.3 Operation

46.3.1 Principles of Measurement Operation

Figure 46.4 shows the measurement circuit.



Note 1. TSn = TS00 to TS19

Figure 46.4 Measurement circuit

Figure 46.5 to Figure 46.7 explain the electrostatic capacitance measurement operation principles of the CTSU current frequency conversion. The operation is as follows:

1. The electrostatic capacitance of the electrode is charged by turning SW1 on and SW2 off (Figure 46.5).
2. The charged capacitance is discharged by turning SW1 off and SW2 on (Figure 46.6).
3. Current flows to the switched capacitor filter by switching between charging and discharging. At this point, if a finger is in close proximity, the capacitance and the flowing current change. A clock is generated by supplying the control current, which is proportional to the amount of current flowing through the switched capacitor filter, from the circuit that generates the TSCAP power supply to the ICO. The counter measures the clock frequency that changes depending on whether a finger is in close proximity. The software uses the value read from the counter to determine contact with a finger (Figure 46.7).

通过向CTSUCR1.CTSUPON位写入0并关闭电源来清除该位。

46.2.21 CTSUTRMR:CTSU参考电流校准寄存器

Base address: CTSU = 0x400D_0000

Offset address: 0x20

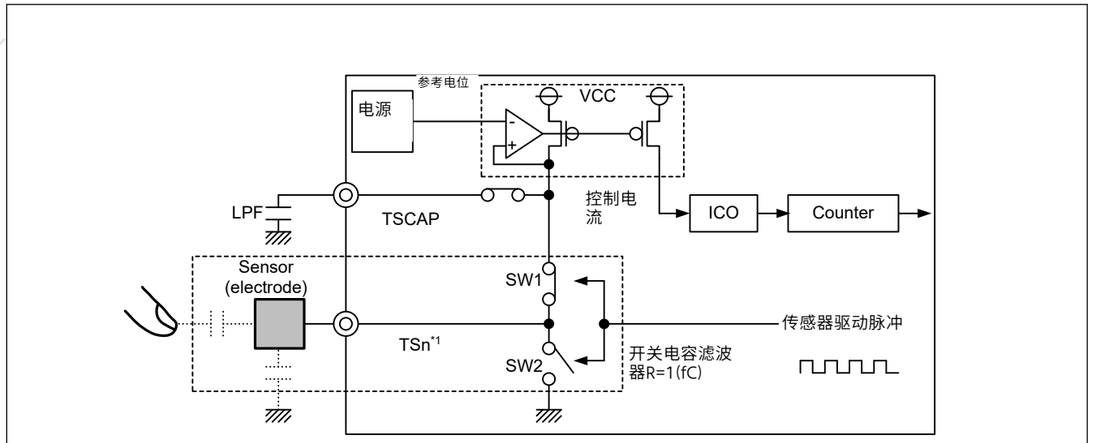
Bit position:	7	6	5	4	3	2	1	0
Bit field:								
重置后的值：	每个芯片的独特价值							

CTSUTRMR电阻存储在出厂时为每个芯片在指定条件下校准的参考电流值。重写此寄存器时，将CTSUERRS.CTSUSPMD[1:0]位设置为10b（校准模式）。复位MCU时，数值恢复为出厂设置值。当CTSSPMD[1:0]位为00b（电容测量模式）时，请勿重写此寄存器。

46.3 Operation

46.3.1 测量操作原理

图46.4显示了测量电路。



注1.TSn=TS00至TS19

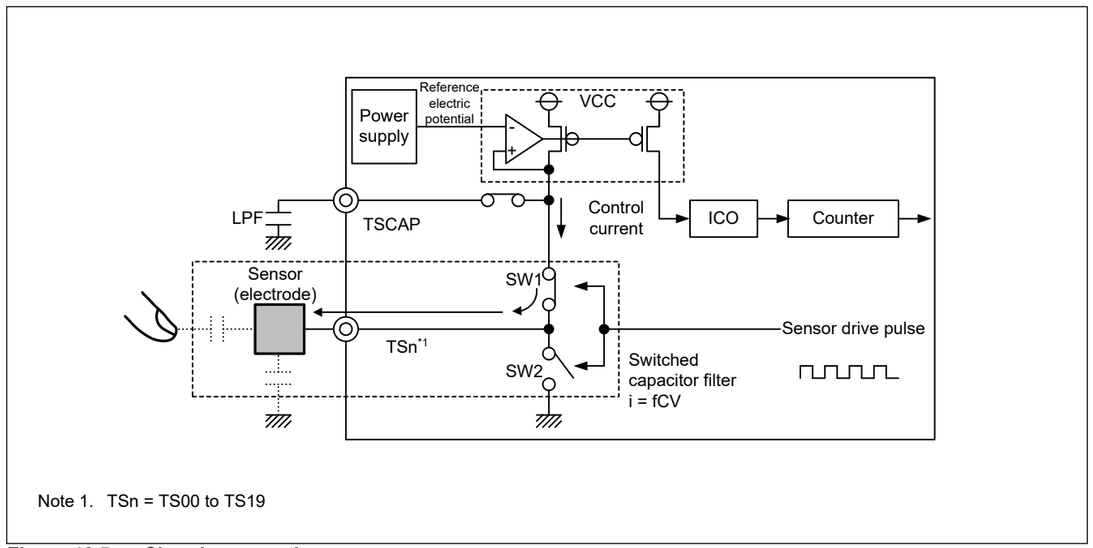
Figure 46.4 测量电路

图46.5至图46.7说明了CTSU电流变频的静电电容测量操作原理。操作如下：

1.通过打开SW1和关闭SW2对电极的静电电容进行充电（图46.5）。

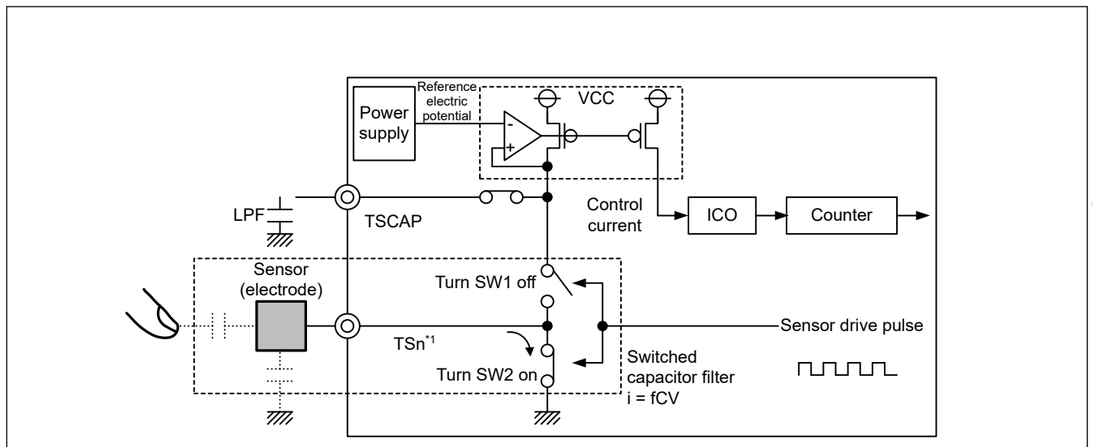
2.通过关闭SW1和打开SW2对充电的电容进行放电（图46.6）。

3.电流通过在充电和放电之间切换而流向开关电容滤波器。此时，如果手指靠近，则电容和流动电流会发生变化。通过从产生TSCAP电源的电路向ICO提供与流过开关电容滤波器的电流量成比例的控制电流来产生时钟。计数器测量时钟频率，该频率根据手指是否靠近而变化。软件使用从计数器读取的值来确定与手指的接触（图46.7）。



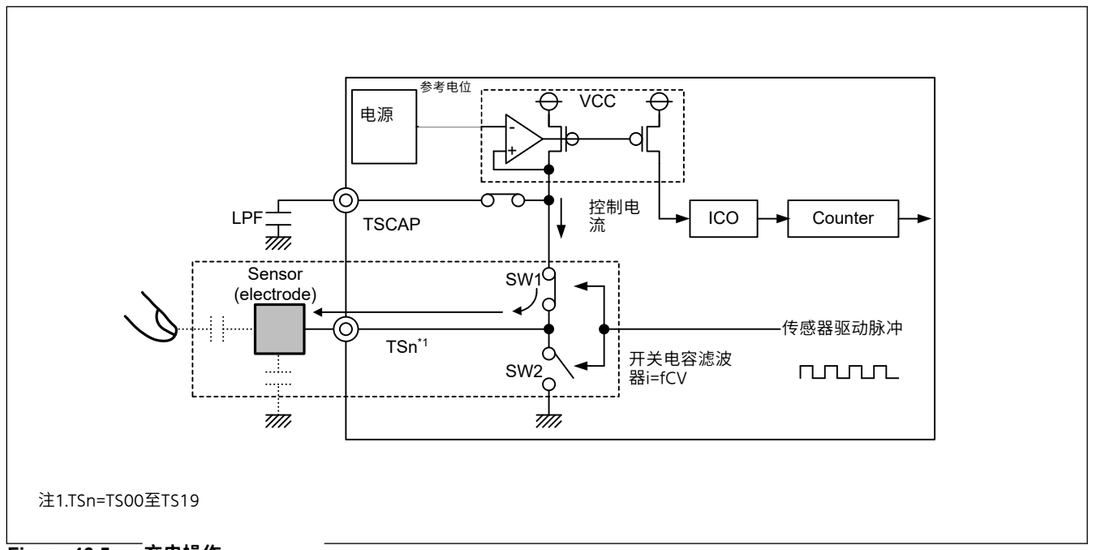
Note 1. TSn = TS00 to TS19

Figure 46.5 Charging operation



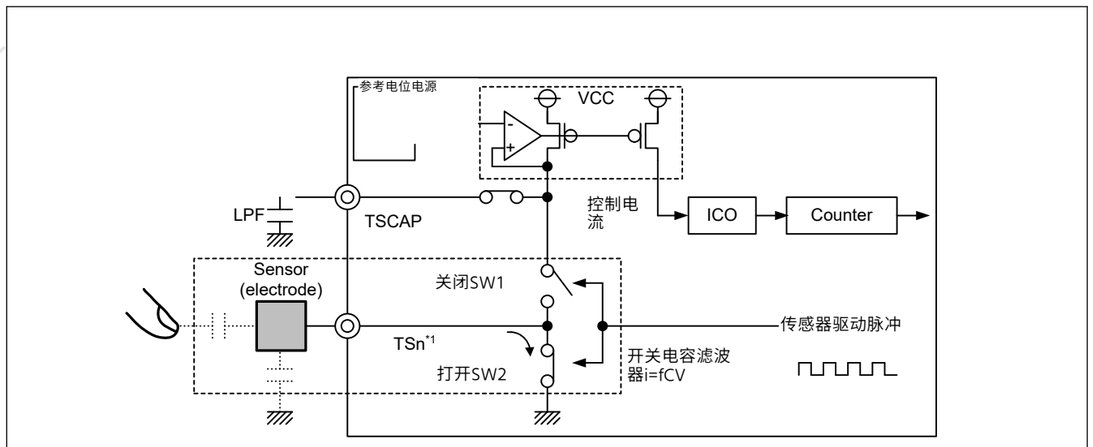
Note 1. TSn = TS00 to TS19

Figure 46.6 Discharging operation



注1.TSn=TS00至TS19

Figure 46.5 充电操作



注1.TSn=TS00至TS19

Figure 46.6 卸料作业

RA生态工作室

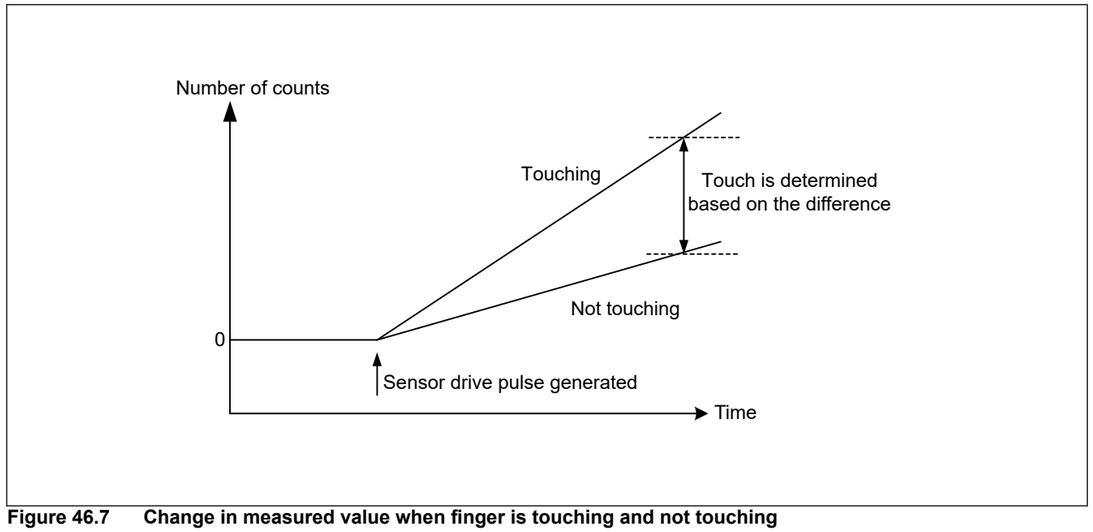
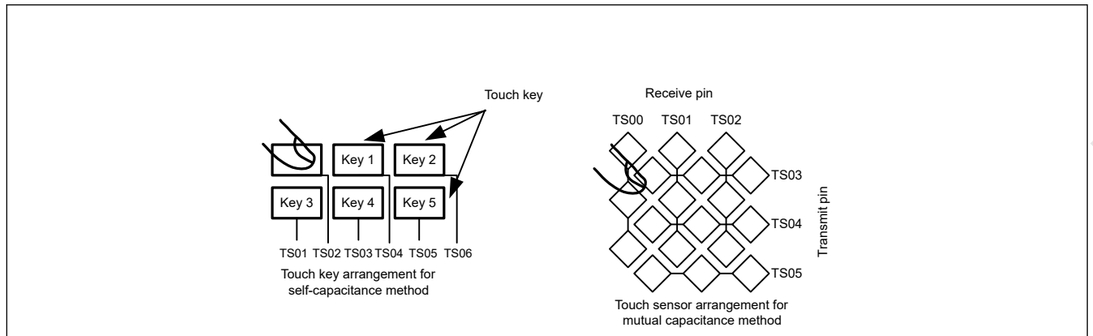


Figure 46.7 Change in measured value when finger is touching and not touching

46.3.2 Measurement Modes

The CTSU supports self-capacitance and mutual capacitance methods. Figure 46.8 illustrates these methods.



Note: This figure indicates a usage example. About available pins, see Table 46.2

Figure 46.8 Overview of self-capacitance method and mutual capacitance method

In the self-capacitance method, a single touch pin is allocated to a single touch key to measure individual electrostatic capacitance when a finger is in close proximity. In this method, capacitance can be measured in both single scan and multiscan modes.

In the mutual capacitance method, the capacitance between two opposing electrodes (transmit and receive pins) is measured.

46.3.2.1 Initial settings flow

Figure 46.9 shows the flow for the CTSU initial settings.

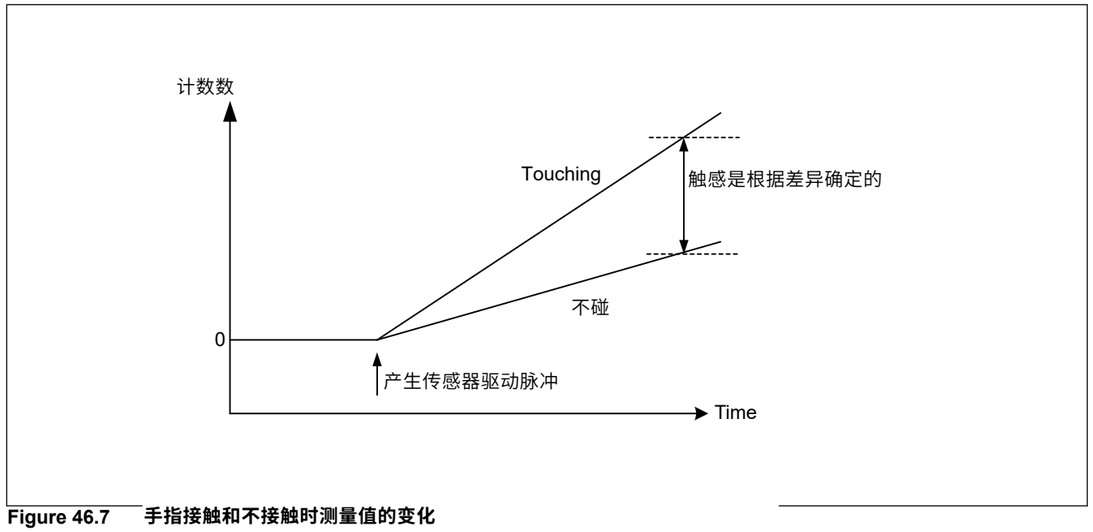
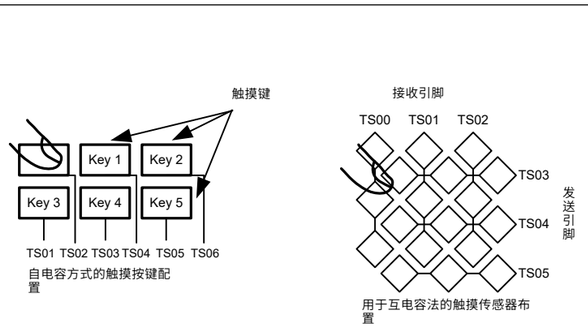


Figure 46.7 手指接触和不接触时测量值的变化

46.3.2 测量模式

CTSU支持自电容和互电容方法。图46.8说明了这些方法。



Note: 该图表示使用示例。关于可用引脚，请参见表46.2

Figure 46.8 自电容法和互电容法概述

在自电容法中，将单个触摸引脚分配给单个触摸键，以在手指靠近时测量单个静电电容。在这种方法中，可以在单扫描和多扫描模式下测量电容。

在互电容法中，测量两个相对电极（发送和接收引脚）之间的电容。

46.3.2.1 初始设置流程

图46.9显示了CTSU初始设置的流程。

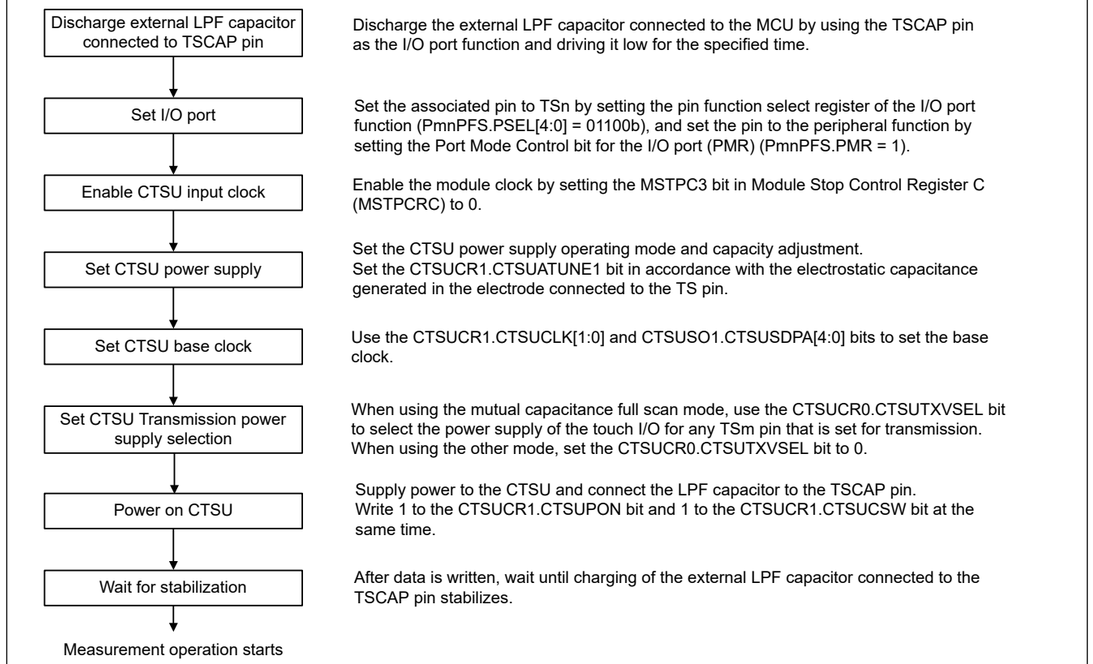


Figure 46.9 CTSU initial settings flow

Figure 46.10 shows the flow for stopping CTSU operation and invoking the standby state.

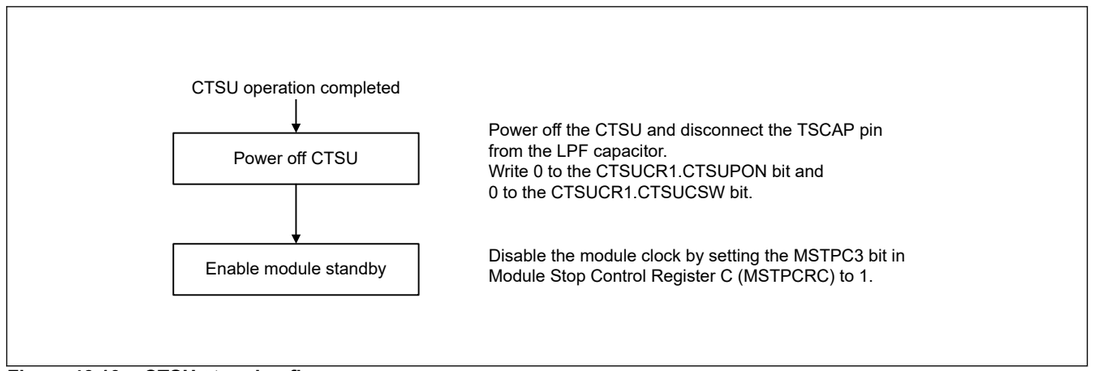


Figure 46.10 CTSU stopping flow

When restarting operation after it stops, follow the initial settings flow shown in Figure 46.9.

46.3.2.2 Status counter

The measurement status counter of the CTSU Status Register (CTSUST) indicates the current measurement status. The measurement status is shared by all three modes. Figure 46.11 shows the status operation transitions.

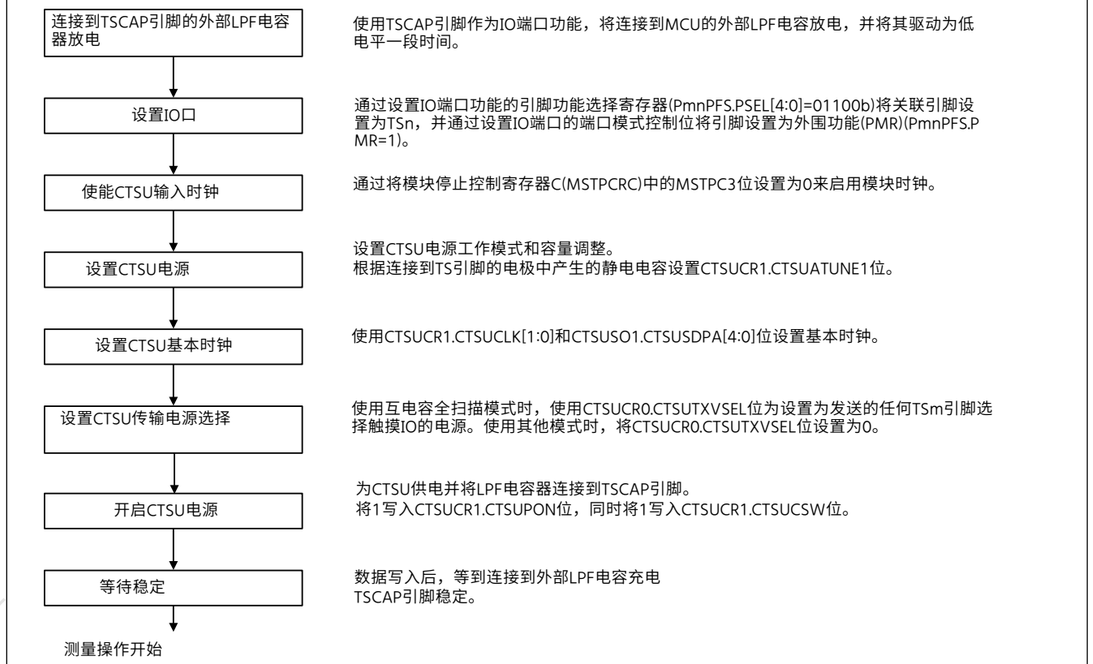


Figure 46.9 CTSU初始设置流程

图46.10显示了停止CTSU操作并调用待机状态的流程。

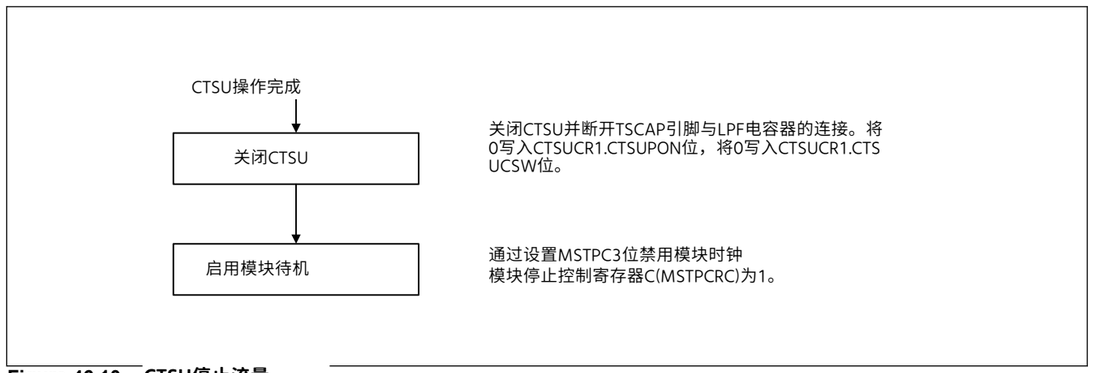
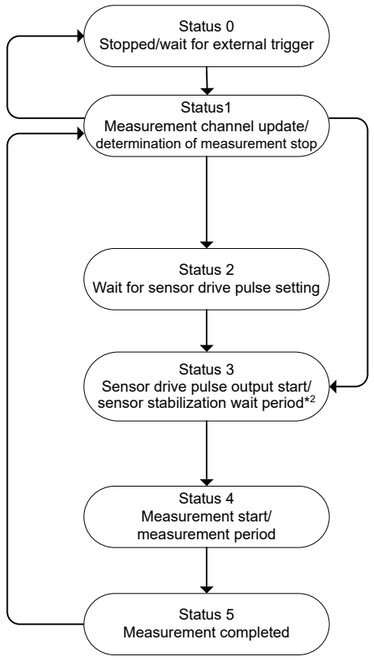


Figure 46.10 CTSU停止流量

停止后重新开始运行时，请按照图46.9所示的初始设置流程进行操作。

46.3.2.2 状态计数器

CTSU状态寄存器(CTSUST)的测量状态计数器指示当前测量状态。测量状态由所有三种模式共享。图46.11显示了状态操作转换。



Conditions for transition to Status 1:
- If CTSUCR0.CTSUCAP bit = 0, CTSUCR0.CTSUSTRT bit = 1
- If CTSUCR0.CTSUCAP bit = 1, CTSUCR0.CTSUSTRT bit = 1 and the rising edge of the external trigger is detected.

Condition for transition to Status 0:
- There is no channel to be measured next. (A CTSU_CTSUFN interrupt occurs and measurement stops.)

Condition for transition to Status 2:
- Update of the measurement channel completes.

Condition for transition to Status 3:
- CTSUST.CTSUPS = 1 (second measurement) in mutual capacitance full scan mode.

Condition for transition to Status 3:
- Write access to the CTSUSO1 register.*1

Condition for transition to Status 4:
- CTSUST.CTSUDTSR flag = 0 when the sensor stabilization time elapses after supply of the sensor drive pulse starts.

Condition for transition to Status 5:
- The measurement time elapses after measurement started. For details on the measurement time.

Condition for transition to Status 1:
- Two clocks of the operating clock elapse.

Note 1. When using the DTC or ICU to set the registers during CTSU_CTSUWR interrupt handling, write to the CTSUSO1 register last.
Note 2. If the CTSUST.CTSUDTSR flag = 1, wait until the previous measurement result is transferred.

Figure 46.11 Status operation transitions

The status counter transitions to Status 0 when all of the specified measurement channels are measured.

The CTSUCR0.CTSUSTRT bit is set to 0 by hardware when a software trigger is used. When an external trigger is used, the value of 1 is retained, and the CTSU waits for the next trigger.

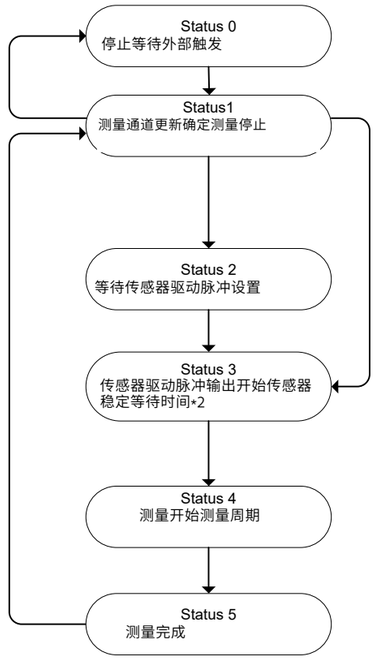
When operation is forced to stop during measurement or the trigger wait state, by a simultaneous 0 write to the CTSUCR0.CTSUSTRT bit and a 1 write to the CTSUCR0.CTSUINIT bit, the status transitions to Status 0 and measurement stops.

If the channel to be measured is not set in the CTSUCHAC0 to CTSUCHAC2 or CTSUCHTRC0 to CTSUCHTRC2 registers, a CTSU_CTSUFN interrupt occurs immediately after a transition to Status 1, and then the status transitions to Status 0.

In the following situations, there is no channel to be measured:

- No measurement target channel is specified in the CTSUCHAC0 to CTSUCHAC2 registers.
- In self-capacitance single scan mode, the channel specified in the CTSUMCH0 register is not a measurement target in the CTSUCHAC0 to CTSUCHAC2 registers.
- In full scan modes, there is no transmit channel or receive channel to be measured based on the combined settings of the CTSUCHAC0 to CTSUCHAC2 and CTSUCHTRC0 to CTSUCHTRC2 registers.

If there is no channel to be measured based on these settings, a CTSU_CTSUFN interrupt occurs immediately after a transition to Status 1, and the counter transitions to Status 0.



转换到状态1的条件：•如果CTSUCR0.CTSUCAP位=0，CTSUCR0.CTSUSTRT位=1•如果CTSUCR0.CTSUCAP位=1，CTSUCR0.CTSUSTRT位=1，并且检测到外部触发的上升沿。

转换到状态0的条件：•没有下一个要测量的通道。（发生CTSU_CTSUFN中断并停止测量。）转换到状态2的条件：•测量通道更新完成。转换到状态3的条件：•CTSUST.CTSUPS=1（第二次测量），互电容全扫描模式。

转换到状态3的条件：•对CTSUSO1寄存器的写访问。*1

转换到状态4的条件：•CTSUST.CTSUDTSR标志=0，当传感器驱动脉冲开始供应后传感器稳定时间过去时。

转换到状态5的条件：•测量开始后测量时间已过。有关测量时间的详细信息。

转换到状态1的条件：•运行时钟的两个时钟过去。

注1.在CTSU_CTSUWR中断处理期间使用DTC或ICU设置寄存器时，最后写入CTSUSO1寄存器。

注2.如果CTSUST.CTSUDTSR标志=1，则等待前一个测量结果被传输。

Figure 46.11 状态操作转换

当测量所有指定的测量通道时，状态计数器转换为状态0。

当使用软件触发时，CTSUCR0.CTSUSTRT位由硬件设置为0。使用外部触发时，保留值1，CTSU等待下一次触发。

在测量或触发等待状态期间强制停止操作时，通过同时向CTSUCR0.CTSUSTRT位写入0和向CTSUCR0.CTSUINIT位写入1，状态转换为状态0并停止测量。

如果要测量的通道未在CTSUCHAC0到CTSUCHAC2或CTSUCHTC0到CTSUCHRC2寄存器中设置，则在转换到状态1后立即发生CTSU_CTSUFN中断，然后状态转换到状态0。

在以下情况下，没有要测量的通道：

●CTSUCHAC0至CTSUCHAC2寄存器中未指定测量目标通道。

●在自电容单次扫描模式下，CTSUCHAC0寄存器中指定的通道不是CTSUCHAC0至CTSUCHAC2寄存器中的测量目标。

●在全扫描模式下，根据CTSUCHAC0到CTSUCHAC2和CTSUCHAC0到CTSUCHAC2寄存器的组合设置，没有要测量的发送通道或接收通道。

如果根据这些设置没有要测量的通道，则在转换到状态1后立即发生CTSU_CTSUFN中断，并且计数器转换到状态0。

46.3.2.3 Self-capacitance single scan mode operation

In self-capacitance single scan mode, electrostatic capacitance on one channel is measured. Figure 46.12 shows the software flow and an operation example, and Figure 46.13 shows the timing.

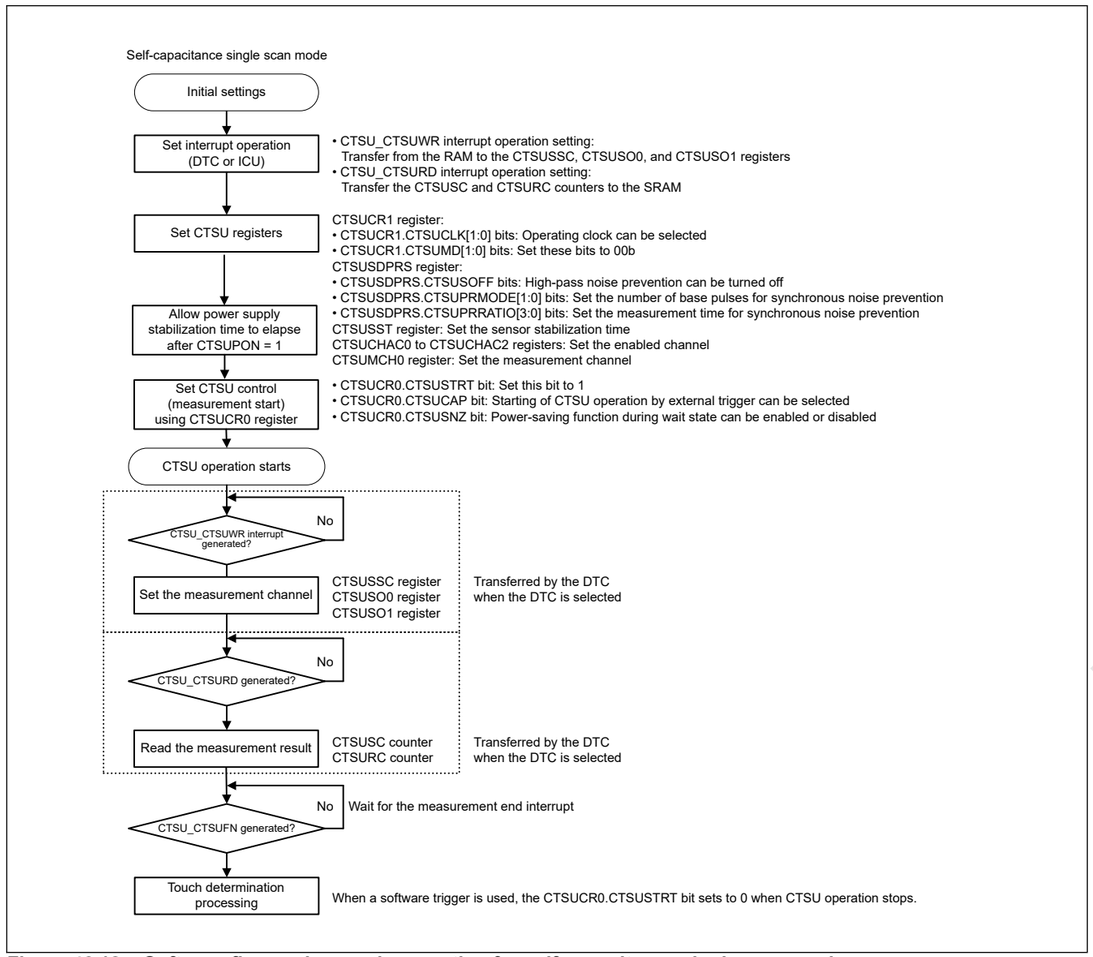


Figure 46.12 Software flow and example operation for self-capacitance single scan mode

46.3.2.3 自电容单次扫描模式操作

在自电容单次扫描模式下，测量一个通道上的静电电容。图46.12显示了软件流程和操作示例，图46.13显示了时序。

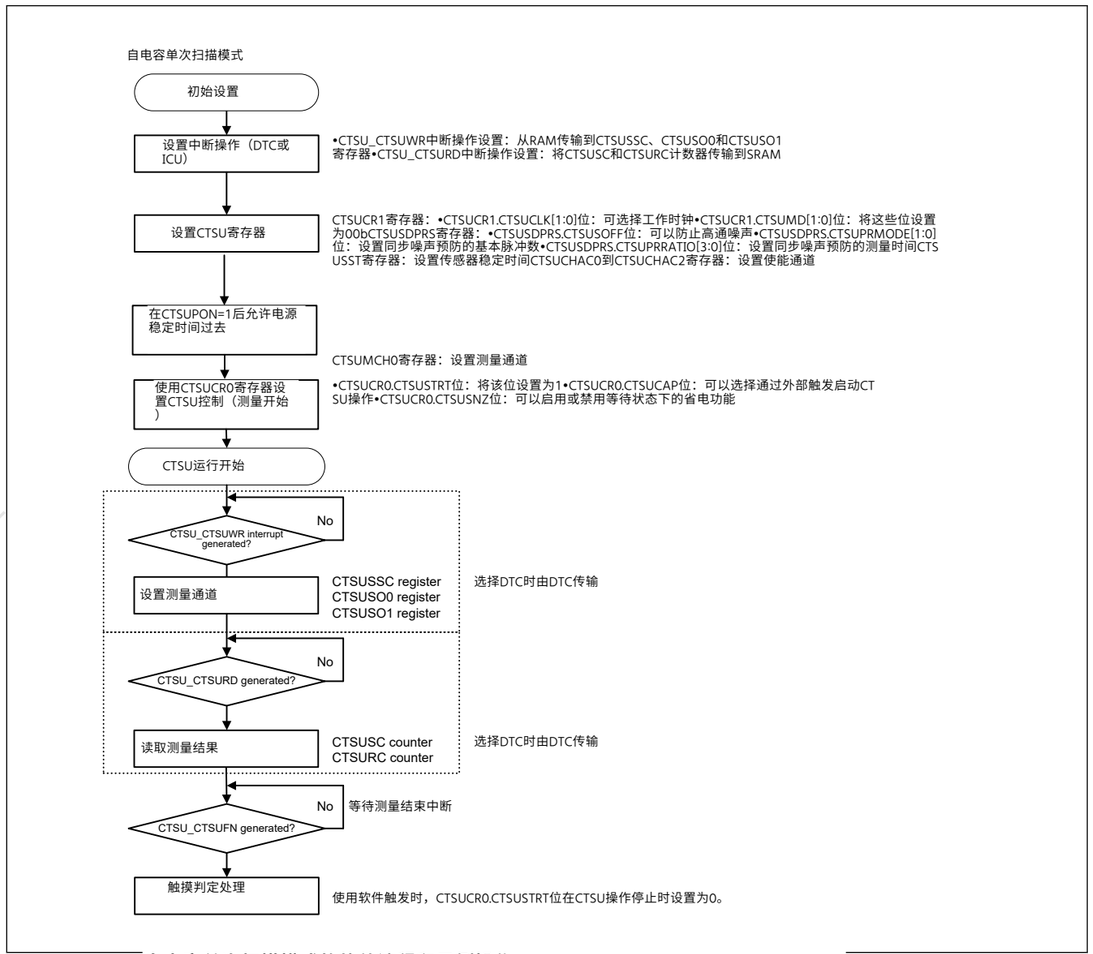


Figure 46.12 自电容单次扫描模式的软件流程和示例操作

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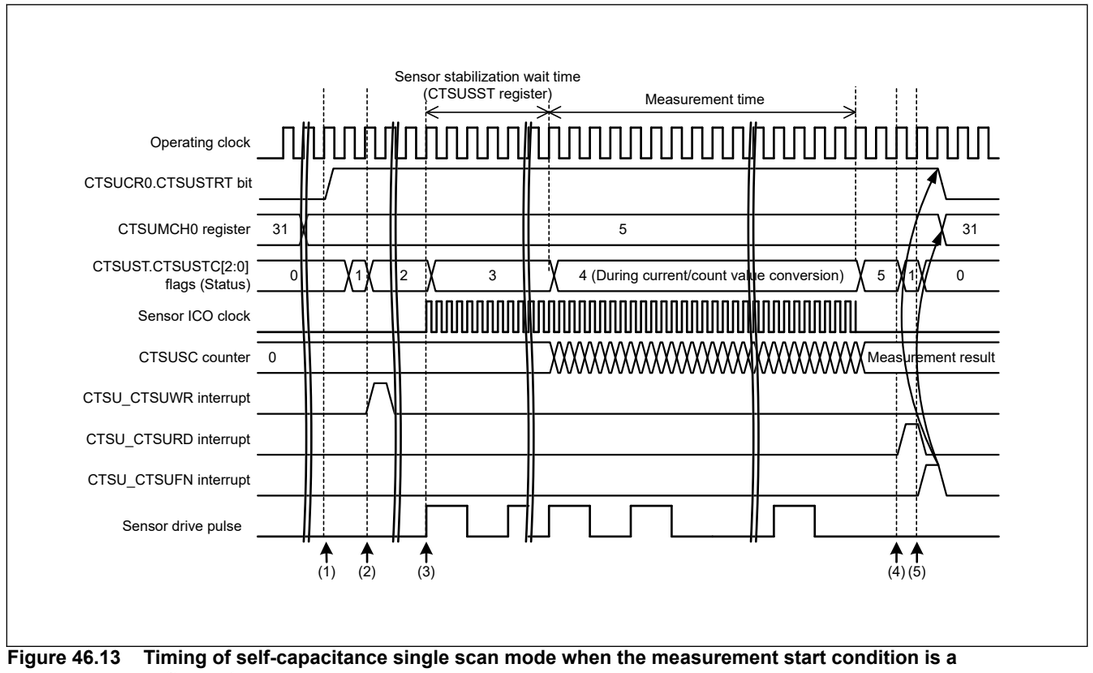


Figure 46.13 Timing of self-capacitance single scan mode when the measurement start condition is a software trigger

The following describes the operation shown in Figure 46.13.

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined in accordance with the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time elapse, and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. A measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

Table 46.7 lists the touch pin states in self-capacitance single scan mode.

Table 46.7 Touch pin states in self-capacitance single scan mode

Status	Touch pin	
	Measured channel	Non-measured channel
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

46.3.2.4 Self-capacitance multi-scan mode operation

In self-capacitance multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets in the CTSUCHAC0 to CTSUCHAC2 registers is measured sequentially in ascending order. Figure 46.14 shows the software flow and an operation example, and Figure 46.15 shows the timing.

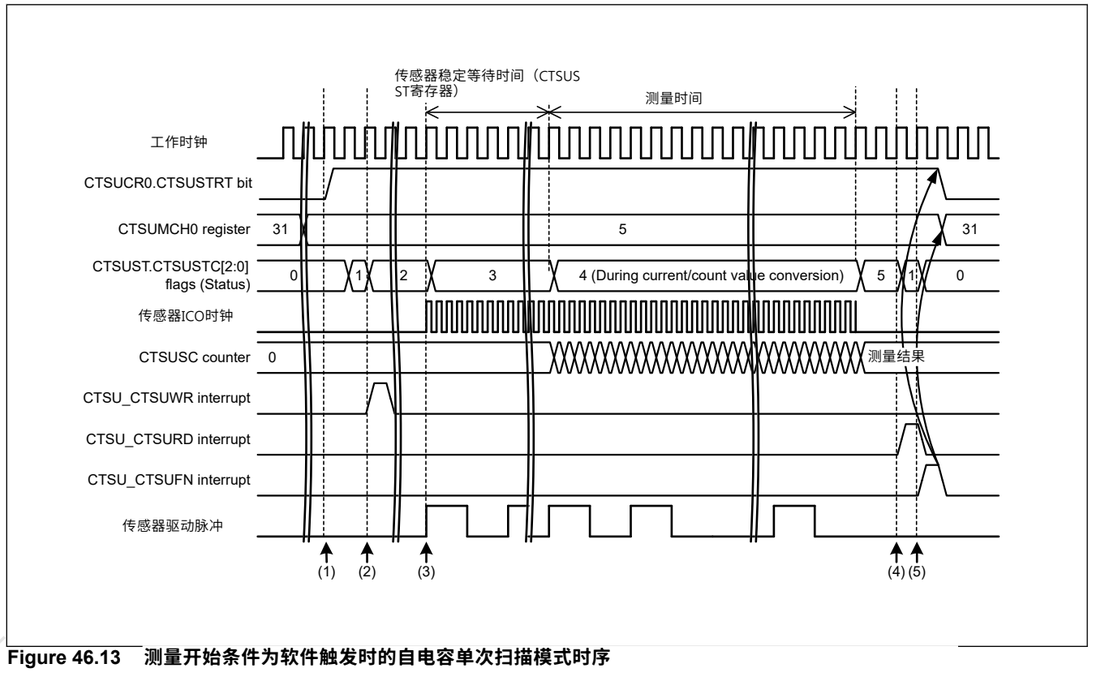


Figure 46.13 测量开始条件为软件触发时的自电容单次扫描模式时序

下面介绍图46.13所示的操作。

1.进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。

2、根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。

3.写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。

4.经过传感器稳定等待时间和测量时间后，测量停止，输出测量结果读取请求（CTSU_CTSURD）。

5.输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

表46.7列出了自电容单次扫描模式下的触摸引脚状态。

Table 46.7 自电容单次扫描模式下的触摸引脚状态

Status	触摸针	
	测量通道	Non-measured channel
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

46.3.2.4 自电容多扫描模式操作

在自电容多重扫描模式下，CTSUCHAC0至CTSUCHAC2寄存器中指定为测量目标的所有通道上的静电电容按升序顺序测量。图46.14显示了软件流程和操作示例，图46.15显示了时序。

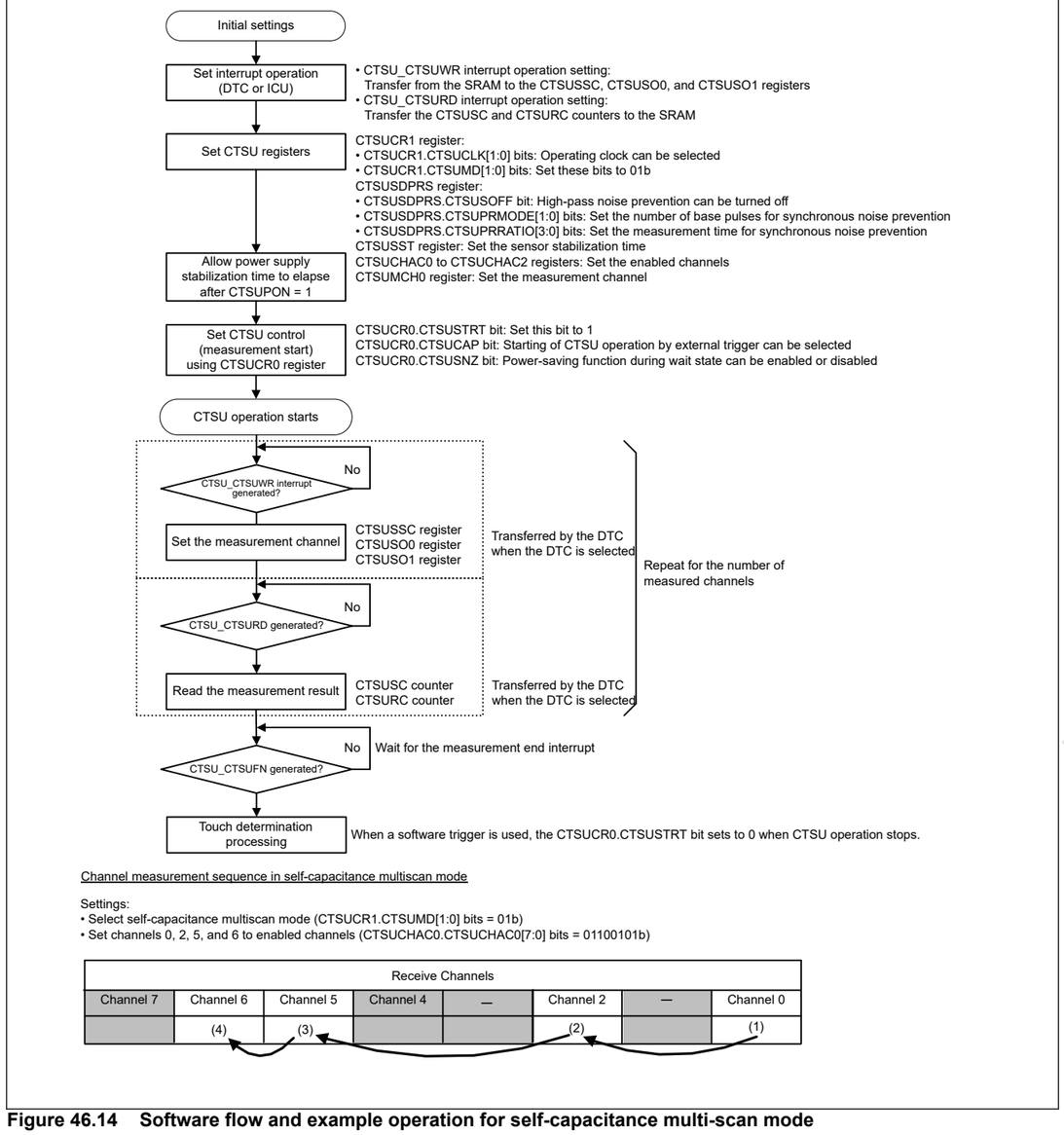


Figure 46.14 Software flow and example operation for self-capacitance multi-scan mode

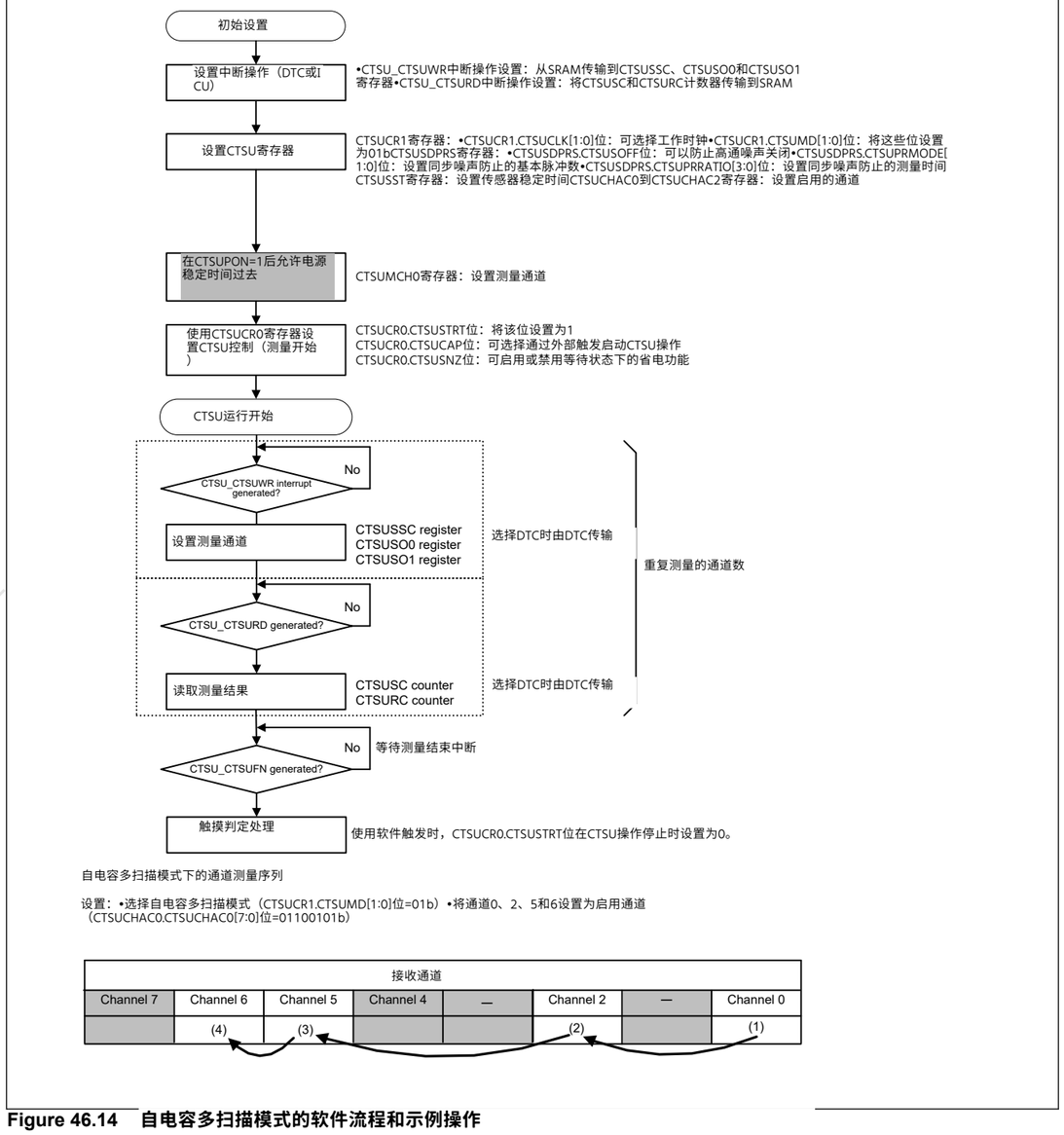


Figure 46.14 自电容多扫描模式的软件流程和示例操作

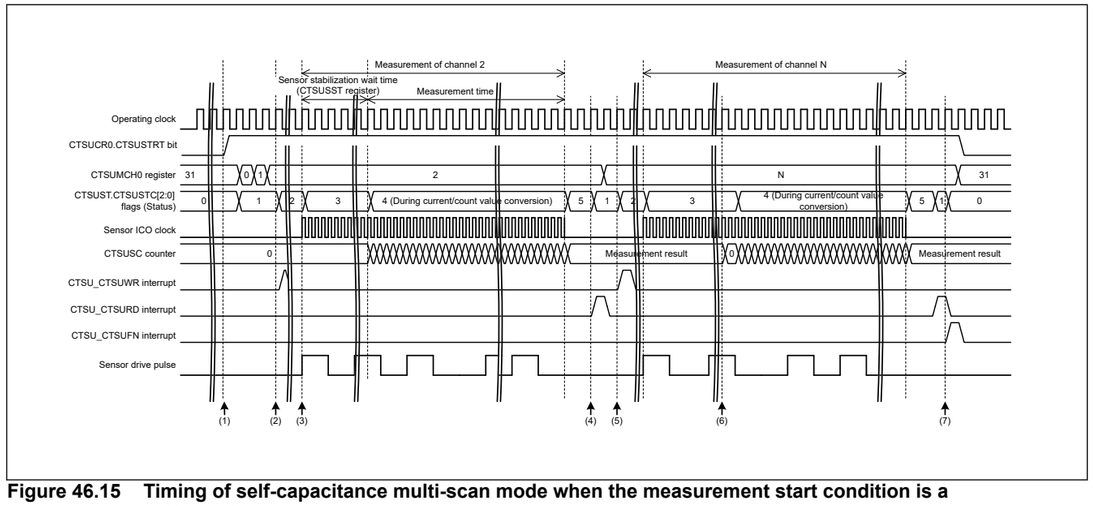


Figure 46.15 Timing of self-capacitance multi-scan mode when the measurement start condition is a software trigger

The following describes the operation shown in Figure 46.15:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined in accordance with the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time elapse, and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. After the channel to be measured next is determined, a measurement channel setting request (CTSU_CTSUWR) is output.
6. After the stabilization wait time elapses and when the previous measurement is read, the result is cleared and measurement starts.
7. On completion of all measurement channels, a measurement end interrupt (CTSU_CTSUFN) is output and measurement is stopped (transition to Status 0).

Table 46.8 lists the touch pin states in self-capacitance multi-scan mode.

Table 46.8 Touch pin states in self-capacitance multi-scan mode

Status	Touch pin	
	Measured channel	Non-measured channel
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

46.3.2.5 Mutual capacitance full scan mode operation

In mutual capacitance full scan mode, measurement is performed during the high-level period of the sensor drive pulse on the receive channel by applying the edge to the target transmit channel to be measured. A single measurement target is measured twice, on the rising and falling edges. The difference between the data of these two measurements determines whether or not the electrode was touched, which results in a higher touch sensitivity.

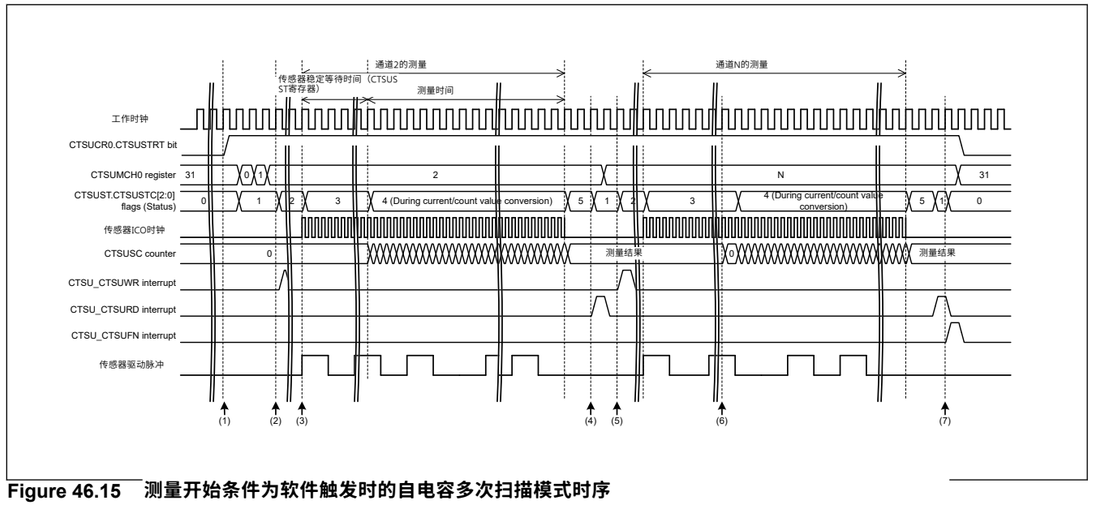


Figure 46.15 测量开始条件为软件触发时的自电容多次扫描模式时序

下面介绍图46.15所示的操作：

1.进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。

2、根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。

3.写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。

4.经过传感器稳定等待时间和测量时间后，测量停止，输出测量结果读取请求（CTSU_CTSURD）。

5、确定下一个要测量的通道后，输出测量通道设置请求（CTSU_CTSUWR）。

6.经过稳定等待时间后，当读取前一次测量时，结果被清除并开始测量。

7.所有测量通道完成后，输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

表46.8列出了自电容多扫描模式下的触摸引脚状态。

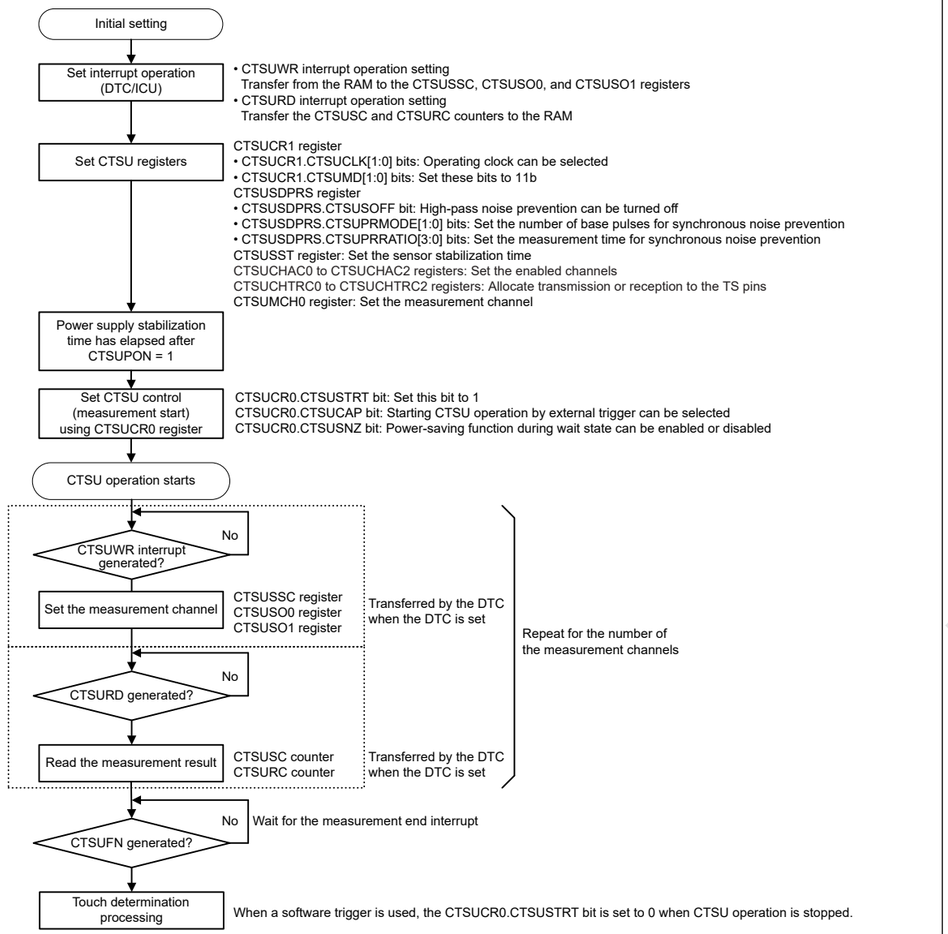
Table 46.8 自电容多扫描模式下的触摸引脚状态

Status	触摸针	
	测量通道	Non-measured channel
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

46.3.2.5 互电容全扫描模式操作

在互电容全扫描模式下，在接收通道上的传感器驱动脉冲的高电平期间通过将边沿施加到要测量的目标发送通道来执行测量。在上升沿和下降沿对单个测量目标进行两次测量。这两次测量的数据之间的差异决定了电极是否被触摸，从而导致更高的触摸灵敏度。

Electrostatic capacitance is measured sequentially on channels set to transmission or reception in the CTSUCHTRC0 to CTSUCHTRC2 registers, and specified as measurement targets in the CTSUCHAC0 to CTSUCHAC2 registers. The capacitance is measured by combining these signals. Figure 46.16 shows the software flow and an operation example, and Figure 46.17 shows the timing.



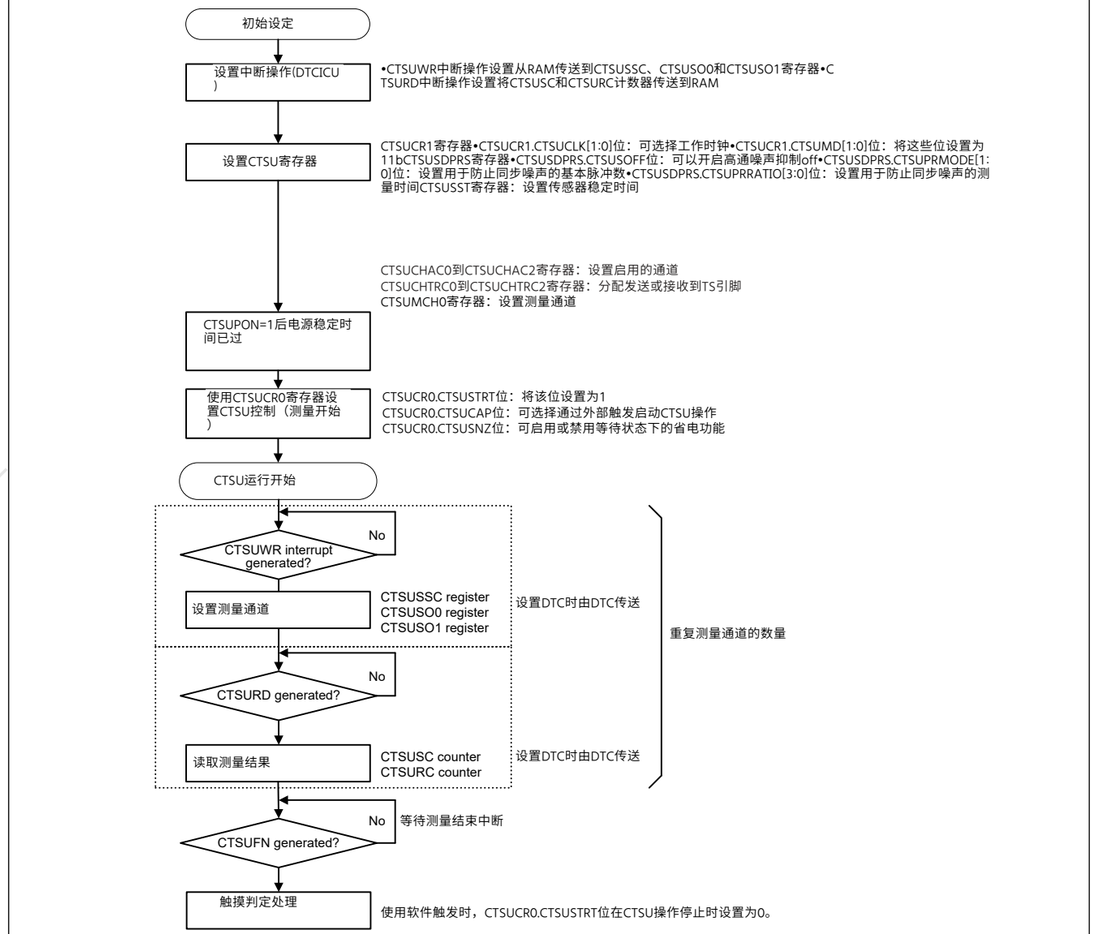
Channel measurement sequence in mutual capacitance full scan mode

Settings:
- Select mutual capacitance full scan mode (CTSUCR1.CTSUMD[1:0] = 11b)
- Set channels 0, 2, 5, and 6 to enabled channels (CTSUCHAC0.CTSUCHAC0[7:0] bits = 01100101b)
- Set channels 0, 2 to receive channels and channels 4 to 7 to transmit channels (CTSUCHTRC0.CTSUCHTRC0[7:0] bits = 11110000b)

		Receive Channels			
		—	Channel 2	—	Channel 0
Transmit channels	Channel 4				
	Channel 5		(3)		(1)
	Channel 6		(4)		(2)
	Channel 7				

Figure 46.16 Software flow and example operation for mutual capacitance full scan mode

在CTSUCHTRC0中设置为发送或接收的通道上依次测量静电电容CTSUCHAC2寄存器，并在CTSUCHAC0至CTSUCHAC2寄存器中指定为测量目标。通过组合这些信号来测量电容。图46.16显示了软件流程和操作示例，图46.17显示了时序。



互电容全扫描模式下的通道测量序列

设置：•选择互电容全扫描模式（CTSUCR1.CTSUMD[1:0]=11b）•将通道0、2、5和6设置为使能通道（CTSUCHAC0.CTSUCHAC0[7:0]位=01100101b）•设置通道0、2用于接收通道，通道4至7用于发送通道（CTSUCHTRC0.CTSUCHTRC0[7:0]位=11110000b）

		接收通道			
		—	Channel 2	—	Channel 0
传输通道	Channel 4				
	Channel 5		(3)		(1)
	Channel 6		(4)		(2)
	Channel 7				

Figure 46.16 互电容全扫描模式的软件流程和示例操作

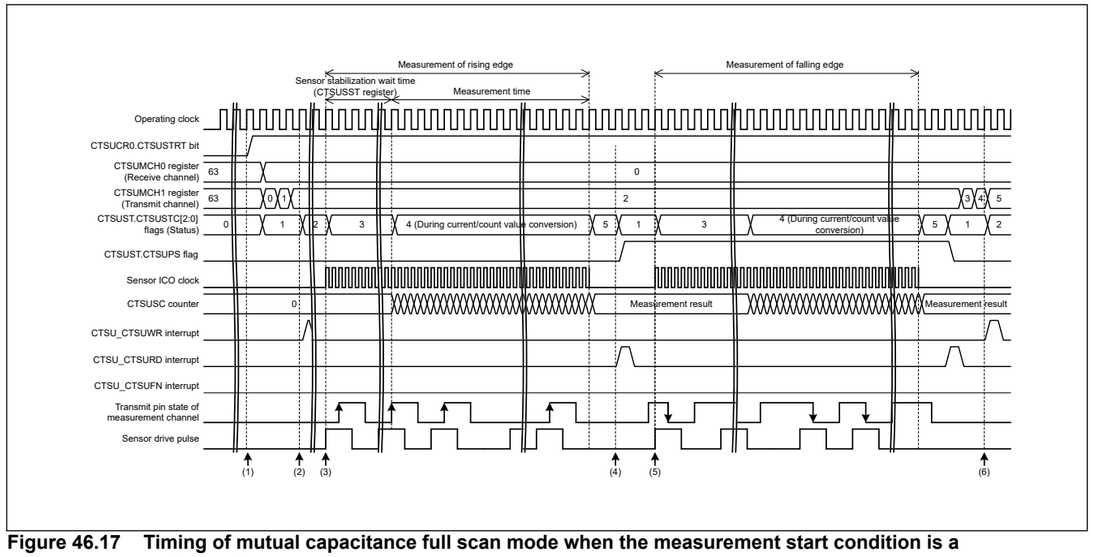


Figure 46.17 Timing of mutual capacitance full scan mode when the measurement start condition is a software trigger

The following describes the operation shown in Figure 46.17

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined in accordance with the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate. At the same time, a pulse detected on the rising edge is output to the transmit pin on the measurement channel during the high-level period of the sensor drive pulse.
4. After the sensor stabilization wait time and the measurement time elapsed and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. The same channel is measured by outputting a pulse detected on the falling edge during the high-level period of the sensor drive pulse.
6. After the same channel is measured twice, the channel to be measured next is determined and measured in the same way.
7. On completion of all measurement channels, a measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

The mutual capacitance measurement status flag (CTSUST.CTSUPS bit) changes when Status 5 transitions to Status 1. Table 46.9 lists the touch pin states in mutual capacitance full scan mode.

Table 46.9 Touch pin states in mutual capacitance full scan mode (1 of 2)

Status	Touch pins for receive channels		Touch pins for transmit channels		Remarks
	Measured channel	Non-measured channel	Measured channel	Non-measured channel	
0	Low	Low	Low	Low	—
1	Low	Low	Low/high	Low	—
2	Low	Low	Low	Low	—
3	Pulse	Low	Pulse	Low	The phase pulse is the same as that of the receive channel on the first measurement and opposite on the second measurement.
4	Pulse	Low	Pulse	Low	—

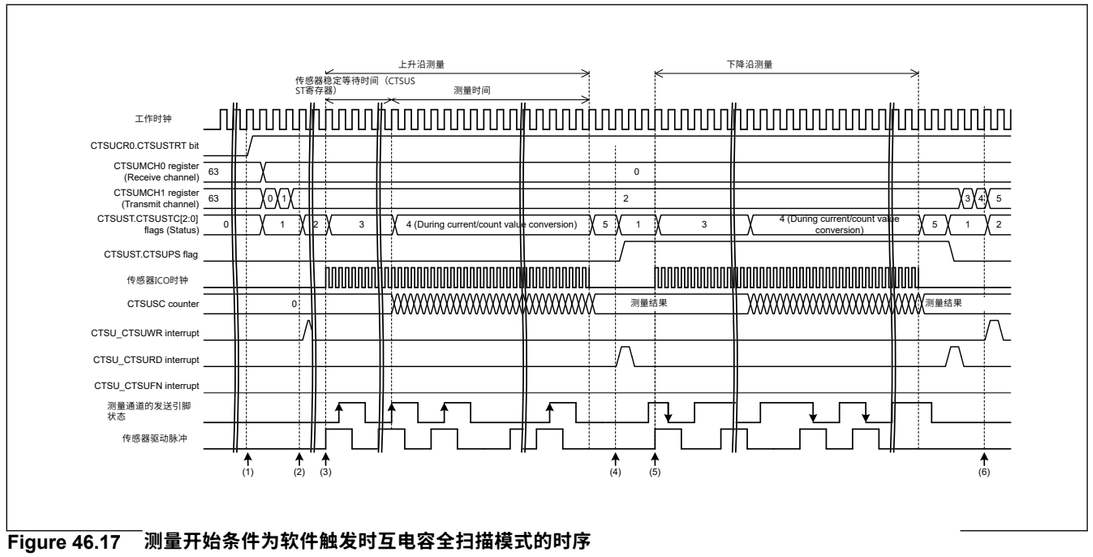


Figure 46.17 测量开始条件为软件触发时互电容全扫描模式的时序

下面介绍图46.17所示的操作

1.进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。

2、根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。

3.写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。同时，在传感器驱动脉冲的高电平期间，将在上升沿检测到的脉冲输出到测量通道的发送引脚。

4.在传感器稳定等待时间和测量时间过去并停止测量后，输出测量结果读取请求（CTSU_CTSURD）。

5.通过在传感器驱动脉冲的高电平期间输出下降沿检测到的脉冲来测量同一通道。

6、同一个通道测量两次后，确定下一个要测量的通道，用同样的方法测量。

7.所有测量通道完成后，输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

互电容测量状态标志（CTSUST.CTSUPS位）在状态5转换为状态1时发生变化。
表46.9列出了互电容全扫描模式下的触摸引脚状态。

Table 46.9 互电容全扫描模式下的触摸引脚状态（1of2）

Status	接收通道的触摸引脚		用于传输通道的触摸引脚		Remarks
	测量通道	Non-measured channel	测量通道	Non-measured channel	
0	Low	Low	Low	Low	—
1	Low	Low	Low/high	Low	—
2	Low	Low	Low	Low	—
3	Pulse	Low	Pulse	Low	相位脉冲在第一次测量时与接收通道的相位脉冲相同，而在第二次测量时则相反。
4	Pulse	Low	Pulse	Low	—

Table 46.9 Touch pin states in mutual capacitance full scan mode (2 of 2)

Status	Touch pins for receive channels		Touch pins for transmit channels		Remarks
	Measured channel	Non-measured channel	Measured channel	Non-measured channel	
5	Low	Low	Low	Low	—

46.3.3 Parameters Common to Multiple Modes

46.3.3.1 Sensor stabilization wait time and measurement time

Figure 46.18 shows the timing of the sensor stabilization wait and measurement.

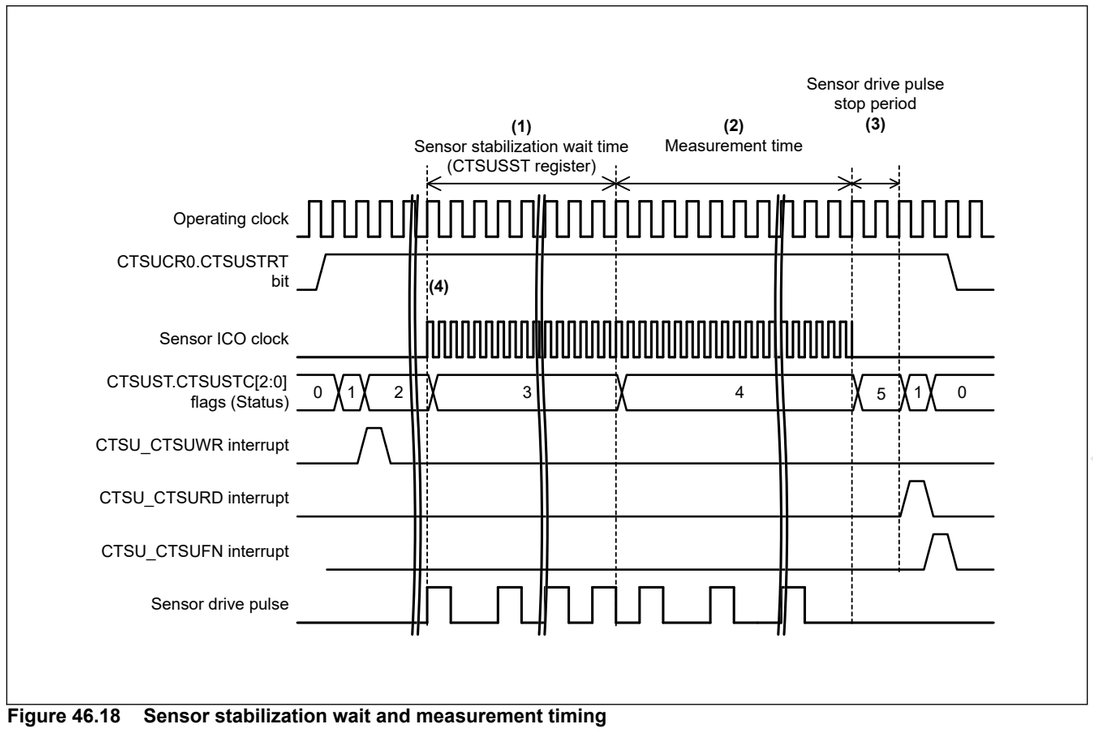


Figure 46.18 Sensor stabilization wait and measurement timing

The following describes the operation shown in Figure 46.18:

1. In response to the CTSU_CTSUWR interrupt request, output of the sensor drive pulse is started by a write access to the CTSUSO1 register. The CTSU waits for the stabilization time set in the CTSUSST register.
2. When the sensor stabilization time elapses and the CTSUST.CTSUDTSR flag clears to 0, measurement starts on transition to Status 4. The measurement time is determined by the base clock cycle setting and the CTSUSDPRS.CTSUPRMODE[1:0], CTSUPRRATIO[3:0], and CTSUSO0.CTSUSNUM[5:0] bits. When the measurement time elapses, measurement of the channel stops.
3. After the measurement time elapses, the status transitions to Status 1 after two operating clock cycles, and a CTSU_CTSURD interrupt occurs. Read the data from the CTSUSC and CTSURC counters. At this time, the sensor drive pulse is output at the low level. When measurement of all specified channels is completed, the CTSUCR0.CTSUSTRT bit clears to 0.
4. The sensor ICO clock oscillates while the CTSUST.CTSUSTC[2:0] flags = 011b (Status 3) or 100b (Status 4).

Table 46.9 互电容全扫描模式下的触摸引脚状态（2个中的2个）

Status	接收通道的触摸引脚		用于传输通道的触摸引脚		Remarks
	测量通道	Non-measured channel	测量通道	Non-measured channel	
5	Low	Low	Low	Low	—

46.3.3 多种模式共有的参数

46.3.3.1 传感器稳定等待时间和测量时间

图46.18显示了传感器稳定等待和测量的时序。

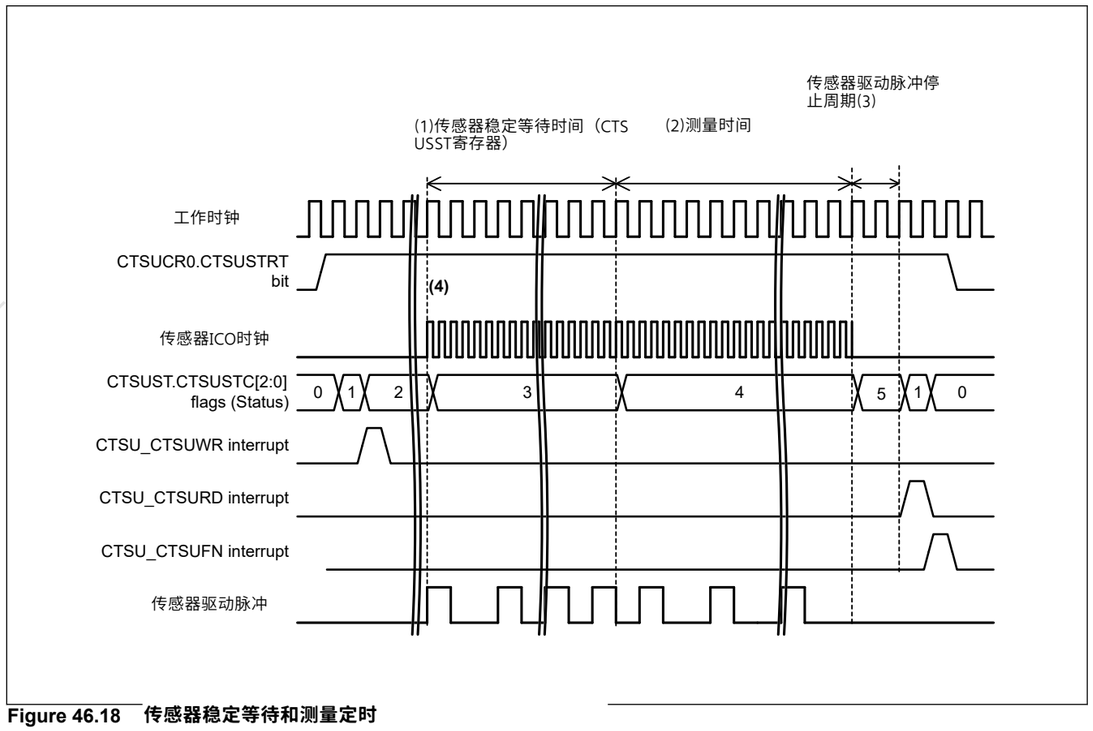


Figure 46.18 传感器稳定等待和测量定时

下面介绍图46.18所示的操作：

1.响应CTSU_CTSUWR中断请求，通过对CTSUSO1寄存器的写访问开始输出传感器驱动脉冲。CTSU等待CTSUSST寄存器中设置的稳定时间。

2.当传感器稳定时间过去且CTSUST.CTSUDTSR标志清除为0时，测量开始转换到状态4。测量时间由基本时钟周期设置和CTSUSDPRS.CTSUPRMODE[1:0]、CTSUPRATIO[3:0]和CTSUSO0.CTSUSNUM[5:0]位。当测量时间过去时，通道的测量将停止。

3.测量时间过去后，状态会在两个工作时钟周期后转换为状态1，并且
CTSU_CTSURD中断发生。从CTSUSC和CTSURC计数器读取数据。此时，传感器驱动脉冲输出为低电平。
完成所有指定通道的测量后，CTSUCR0.CTSUSTRT位清零。

4.传感器ICO时钟在CTSUST.CTSUSTC[2:0]标志=011b（状态3）或100b（状态4）时振荡。

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46.3.3.2 Interrupts

The CTSU supports the following interrupts:

- Write request interrupt for setting registers for each channel (CTSU_CTSUWR)
- Measurement data transfer request interrupt (CTSU_CTSURD)
- Measurement end interrupt (CTSU_CTSUFN)

(1) Write request interrupt for setting registers for each channel (CTSU_CTSUWR)

Store the settings for each measurement channel in the SRAM, and set up the DTC or ICU transfer associated with the CTSU_CTSUWR interrupt in advance. The CTSU_CTSUWR interrupt is output when Status 1 transitions to Status 2. Write the settings for the selected channel from the SRAM to the CTSUSSC, CTSUSO0, and CTSUSO1 registers (Figure 46.19). Because write access to the CTSUSO1 register controls the transition to the next status, you must set this register last.

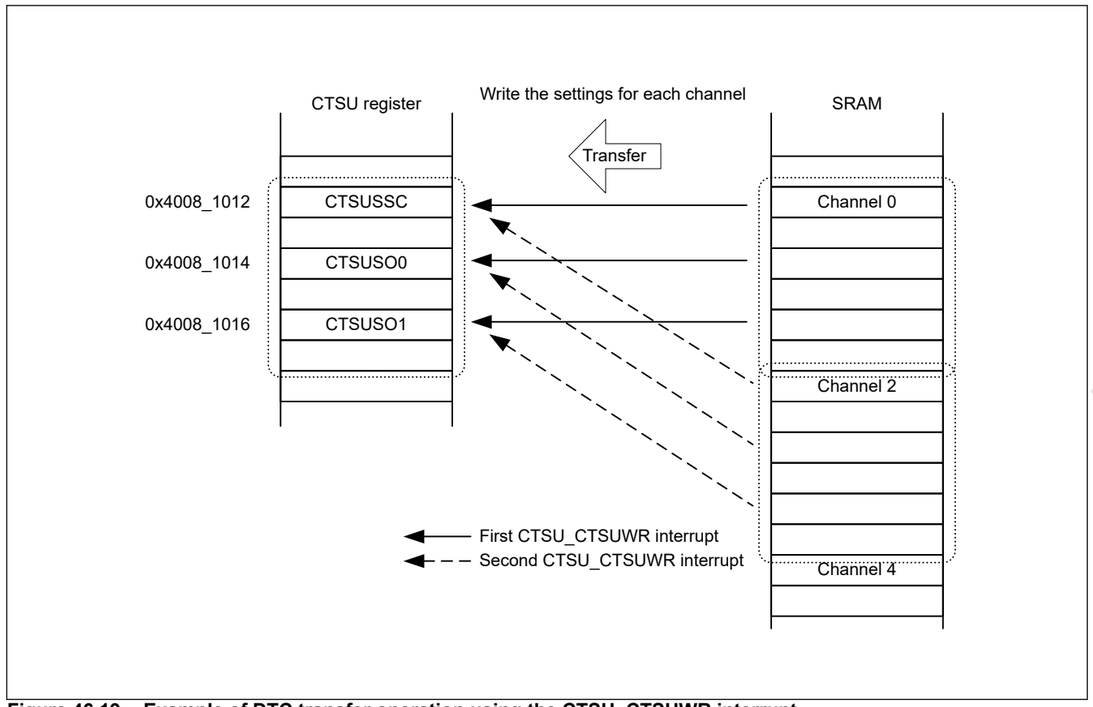


Figure 46.19 Example of DTC transfer operation using the CTSU_CTSUWR interrupt

The registers to be set (CTSUSSC, CTSUSO0, and CTSUSO1) are allocated at sequential addresses. On CTSU_CTSUWR interrupt generation, set up the operation as follows:

- Transfer destination address: CTSUSSC register address
- Handling at the transfer destination address: Transfer 2-byte data three times with a single interrupt. The address of the start byte is fixed.
- Transfer source address: CTSUSSC register data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer source address: Transfer 2-byte data three times with a single interrupt. The address of the first byte is continued from the previous interrupt handling.
- Number of transfers per interrupt: Specify the number of measurements.

46.3.3.2 Interrupts

CTSU支持以下中断：

●各通道设置寄存器的写请求中断(CTSU_CTSUWR)

●测量数据传输请求中断（CTSU_CTSURD）

●测量结束中断（CTSU_CTSUFN）

(1) 为每个通道设置寄存器的写请求中断(CTSU_CTSUWR)

将每个测量通道的设置存储在SRAM中，并提前设置与CTSU_CTSUWR中断相关的DTC或ICU传输。当状态1转换到状态2时输出CTSU_CTSUWR中断。

将所选通道的设置从SRAM写入CTSUSSC、CTSUSO0和CTSUSO1寄存器（图46.19）。因为对CTSUSO1寄存器的写访问控制到下一个状态的转换，所以您必须最后设置该寄存器。

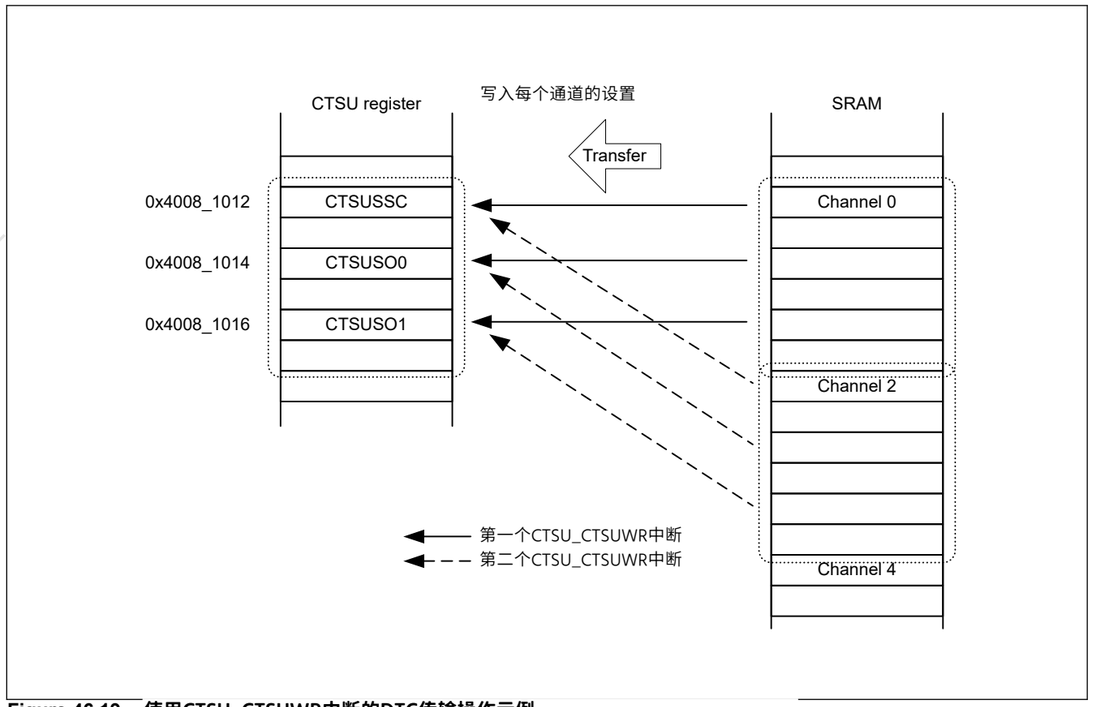


Figure 46.19 使用CTSU_CTSUWR中断的DTC传输操作示例

要设置的寄存器（CTSUSSC、CTSUSO0和CTSUSO1）分配在顺序地址。在产生CTSU_CTSUWR中断时，按如下方式设置操作：

●传输目标地址：CTSUSSC寄存器地址

●在传送目标地址处处理：一次中断传送3次2字节数据。起始字节的地址是固定的。

●传输源地址：CTSUSSC寄存器数据存储地址，用于存储在SRAM中的设置中的最低编号通道

●在传输源地址处处理：一次中断传输3次2字节数据。第一个字节的地址从先前的中断处理继续。

●每个中断的传输次数：指定测量次数。

(2) Measurement data transfer request interrupt (CTSU_CTSURD)

Set up the DTC or ICU transfer associated with the CTSU_CTSURD interrupt in advance. The CTSU_CTSURD interrupt is output when Status 5 transitions to Status 1. Read the measurement result from the CTSUSC and CTSURC counters (Figure 46.20).

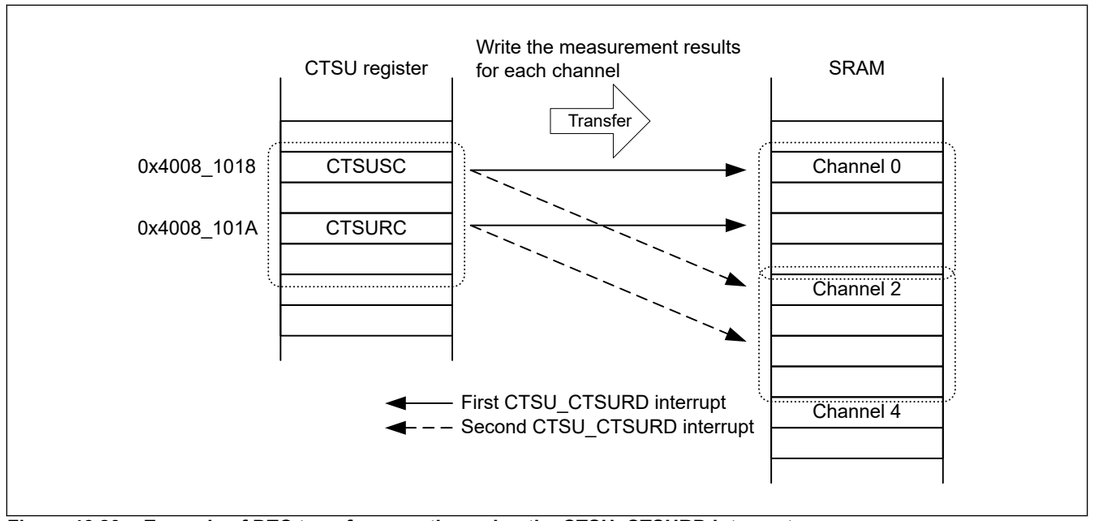


Figure 46.20 Example of DTC transfer operation using the CTSU_CTSURD interrupt

The measurement result registers (CTSUSC and CTSURC counters) used as transfer sources are allocated at sequential addresses. On CTSU_CTSURD interrupt generation, set up the operation as follows:

- Transfer source address: CTSUSC counter address
- Handling at the transfer source address: Transfer 2-byte data twice with a single interrupt. The start address is fixed.
- Transfer destination address: CTSUSC counter data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer destination address: Transfer 2-byte data twice with a single interrupt. The start address is continued from the previous interrupt handling.
- Number of transfers per interrupt: Specify the number of measurements.

(3) Measurement end interrupt (CTSU_CTSUFN)

When all channels are measured, an interrupt occurs when Status 1 transitions to Status 0. In the software, check the overflow flags (CTSUST.CTSUSOVF and CTSUROVF) and read the measurement results to determine whether or not the electrode was touched. Interrupt requests are accepted or disabled in the interrupt control block.

46.4 Usage Notes

46.4.1 Measurement Result Data (CTSUSC and CTSURC Counters)

Read access during measurement is prohibited. If the measurement result data is accessed, an incorrect value might be read because of asynchronous operation.

46.4.2 Constraint on Software Trigger

When 10b (PCLKB/4) is selected in the CTSUCR1.CTSUCLK[1:0] bits, to restart measurement by writing 1 to the CTSUR0.CTSUSTRT bit after measurement is complete, wait for at least 3 cycles to elapse after an interrupt occurs, and then write to the CTSUCR0.CTSUSTRT bit.

(2) 测量数据传输请求中断(CTSU_CTSURD)

提前设置与CTSU_CTSURD中断相关的DTC或ICU传输。当状态5转换为状态1时输出CTSU_CTSURD中断。从CTSUSC和CTSURC计数器读取测量结果（图46.20）。

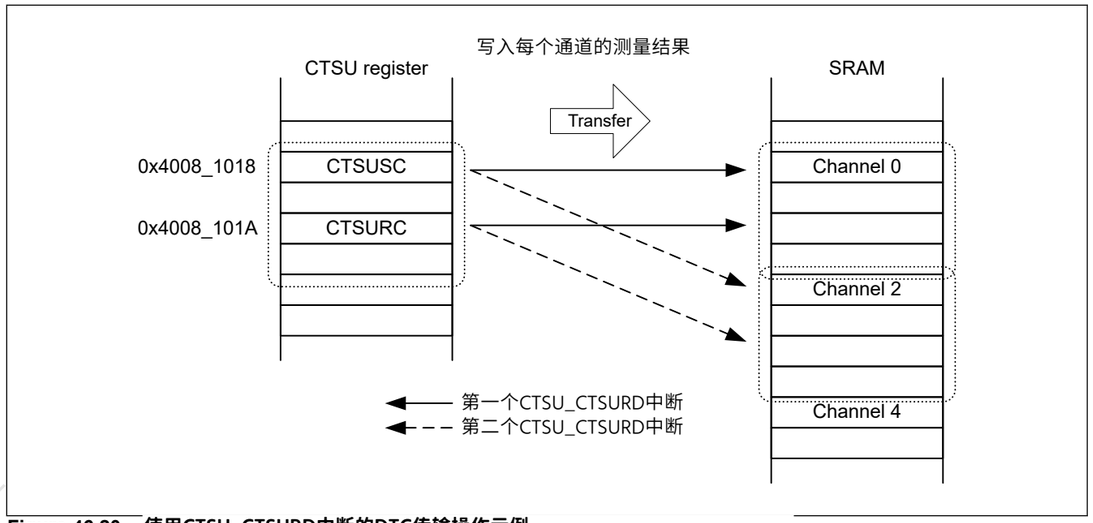


Figure 46.20 使用CTSU_CTSURD中断的DTC传输操作示例

用作传输源的测量结果寄存器（CTSUSC和CTSURC计数器）按顺序分配。在CTSU_CTSURD中断生成时，按如下方式设置操作：

●传输源地址：CTSUSC计数器地址

●在传输源地址处处理：一次中断传输2字节数据两次。起始地址是固定的。

●传输目标地址：SRAM中存储的设置中编号最小的通道的CTSUSC计数器数据存储地址

●传送目标地址处的处理：一次中断传送2字节数据两次。起始地址从先前的中断处理继续。

●每个中断的传输次数：指定测量次数。

(3) 测量结束中断(CTSU_CTSUFN)

测量所有通道时，状态1转换为状态0时发生中断。在软件中，检查溢出标志（CTSUST.CTSUSOVF和CTSUROVF）并读取测量结果以确定电极是否被触摸。在中断控制块中接受或禁用中断请求。

46.4 使用说明

46.4.1 测量结果数据（CTSUSC和CTSURC计数器）

禁止在测量期间进行读取访问。如果访问测量结果数据，可能会因为异步操作而读取到不正确的值。

46.4.2 软件触发约束

当在CTSUCR1.CTSUCLK[1:0]位中选择10b(PCLKB4)时，通过将1写入
测量完成后CTSUR0.CTSUSTRT位，在发生中断后至少等待3个周期，然后写入CTSUCR0.CTSUSTRT位。

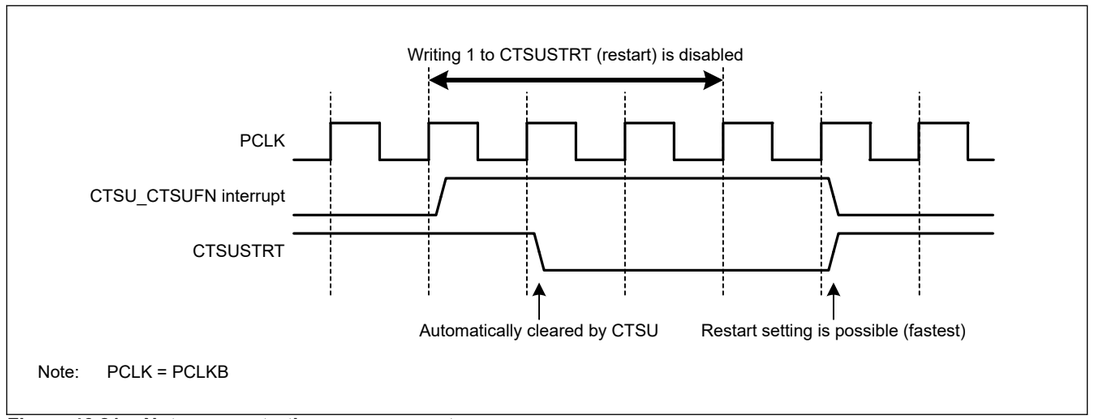


Figure 46.21 Notes on restarting measurement

46.4.3 Constraints on External Triggers

- If an external trigger is input during the measurement time, measurement does not start. The next external event is enabled after 1 cycle of the operating clock when a CTSU_CTSUFN interrupt occurs.
- To stop external trigger mode, write 0 to the CTSUCR0.CTSUSTRT bit and 0 to the CTSUCR0.CTSUINIT bit at the same time (forced stop).

46.4.4 Constraints on Forced Stops

To force the current operation to stop, write 0 to the CTSUCR0.CTSUSTRT bit and 1 to the CTSUCR0.CTSUINIT bit at the same time. After this setting, the operation is stopped and the internal control registers are initialized.

When the CTSUCR0.CTSUINIT bit is used for initialization, the following registers are initialized in addition to the initialization of the internal measurement state.

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter

If operation is forced to stop, an interrupt request might be generated depending on the internal state. After a forced stop, also perform the processing for stopping and disabling the DTC or ICU. If a DTC transfer is stopped in an installed system for some reason, also perform the processing for forcing stop to and initializing the CTSU.

46.4.5 TSCAP Pin

The TSCAP pin requires an external decoupling capacitor to stabilize CTSU internal voltage. The traces between the TSCAP pin and the capacitor, and the capacitor and ground should be as short and wide as physically possible.

The capacitor connected to the TSCAP pin should be fully discharged using I/O port control to output a low level, before turning on the switch (CTSUCR1.CTSUCSW bit = 1) to establish a connection.

46.4.6 Constraints on Measurement Operation (CTSUCR0.CTSUSTRT Bit = 1)

During measurement (CTSUCR0.CTSUSTRT bit = 1), do not use the settings for stopping the peripheral clock or changing the port settings related to the touch pins (TSn and TSCAP pins) and Transmission power supply selection (CTSUCR0.CTSUTXVSEL) in the higher layers of the system.

If control settings non-compliant with these constraints are made, operation is forced to stop (CTSUCR0.CTSUSTRT bit = 0 and CTSUCR0.CTSUINIT bit = 1), write 0 to the CTSUCR1.CTSUPON bit and 0 to the CTSUCR1.CTSUCSW bit at the same time, and set the CTSUCR0.CTSUSNZ bit to 0. Next, restart from the initial settings flow shown in Figure 46.9.

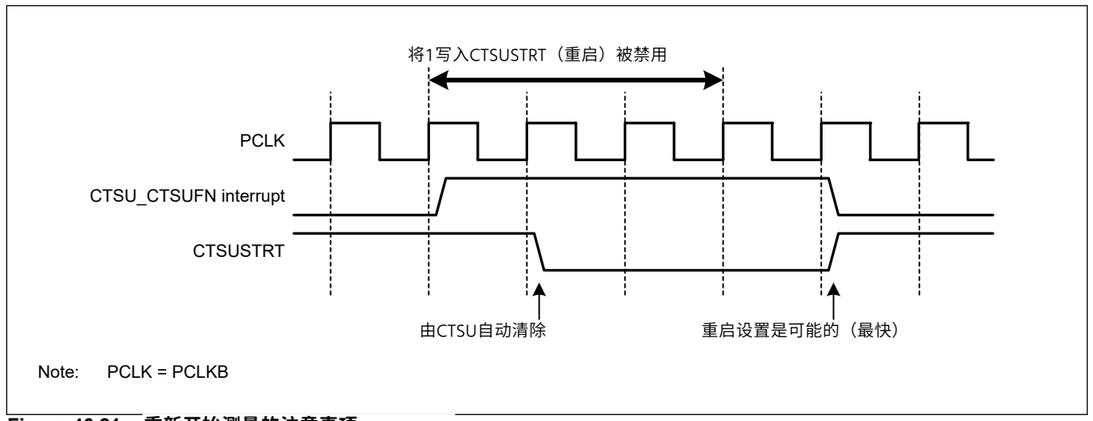


Figure 46.21 重新开始测量的注意事项

46.4.3 外部触发器的约束

●如果在测量期间输入了外部触发，则测量不会开始。当CTSU_CTSUFN中断发生时，下一个外部事件在工作时钟的1个周期后启用。

●要停止外部触发模式，同时将0写入CTSUCR0.CTSUSTRT位和0写入CTSUCR0.CTSUINIT位（强制停止）。

46.4.4 强制停止的约束

要强制停止当前操作，请同时向CTSUCR0.CTSUSTRT位写入0，向CTSUCR0.CTSUINIT位写入1。设置完成后，操作停止，内部控制寄存器初始化。

当CTSUCR0.CTSUINIT位用于初始化时，除了内部测量状态的初始化之外，还初始化以下寄存器。

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter

如果操作被强制停止，根据内部状态可能会产生中断请求。强制停止后，还要执行停止和禁用DTC或ICU的处理。如果由于某种原因在已安装的系统中停止了DTC传输，则还要执行强制停止和初始化CTSU的处理。

46.4.5 TSCAP Pin

TSCAP引脚需要一个外部去耦电容来稳定CTSU内部电压。之间的痕迹
TSCAP引脚和电容器，以及电容器和地线应尽可能短且宽。

在打开开关（CTSUCR1.CTSUCSW位=1）建立连接之前，应使用IO端口控制将连接到TSCAP引脚的电容器完全放电以输出低电平。

46.4.6 测量操作的限制（CTSUCR0.CTSUSTRT位=1）

在测量期间（CTSUCR0.CTSUSTRT位=1），请勿使用与触摸引脚（TSn和TSCAP引脚）和发送电源选择（CTSUCR0.CTSUTXVSEL）相关的端口设置停止外围时钟或更改高位系统的层次。

如果进行了不符合这些约束的控制设置，则强制停止操作（CTSUCR0.CTSUSTRT位=0且CTSUCR0.CTSUINIT位=1），将0写入CTSUCR1.CTSUPON位并将0写入CTSUCR1.CTSUCSW位同时，将CTSUCR0.CTSUSNZ位设置为0。接下来，从图46.9所示的初始设置流程重新启动。

47. Data Operation Circuit (DOC)

47.1 Overview

The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. Table 47.1 lists the DOC specifications and Figure 47.1 shows a block diagram.

Table 47.1 DOC specifications

Item	Description
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	The module-stop state can be set to reduce power consumption.
Interrupts and event link function (DOC_DOPCI)	An interrupt occurs on the following conditions: • The compared values either match or mismatch • The result of data addition is greater than 0xFFFF • The result of data subtraction is less than 0x0000
TrustZone Filter	Security attribution can be set

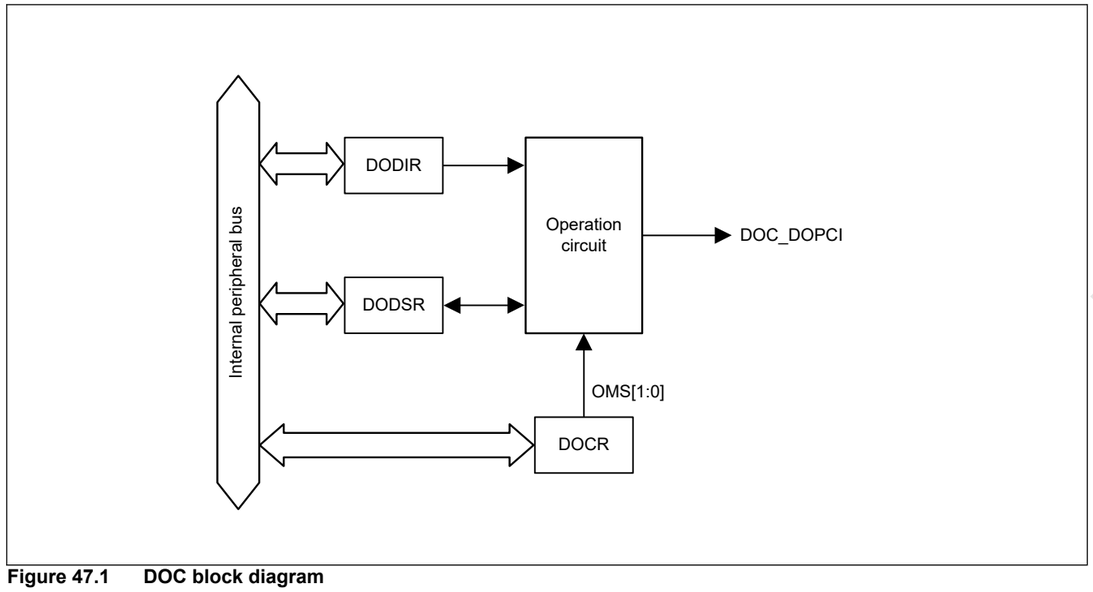


Figure 47.1 DOC block diagram

47.2 DOC Register Descriptions

47.2.1 DOCR : DOC Control Register

Base address: DOC = 0x4010_9000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

47. 数据运算电路(DOC)

47.1 Overview

数据运算电路(DOC)对16位数据进行比较、加法和减法。当适用选定条件时，比较16位数据并可以生成中断。表47.1列出了DOC规范，图47.1显示了框图。

Table 47.1 文档规范

Item	Description
数据运算功能	16位数据比较、加法和减法
Module-stop function	可设置模块停止状态以降低功耗。
中断和事件链接功能（DOC_DOPCI）	在以下情况下会发生中断：● 比较的值匹配或不匹配 • 数据相加结果大于0xFFFF • 数据减法结果小于0x0000
TrustZone Filter	可设置安全属性

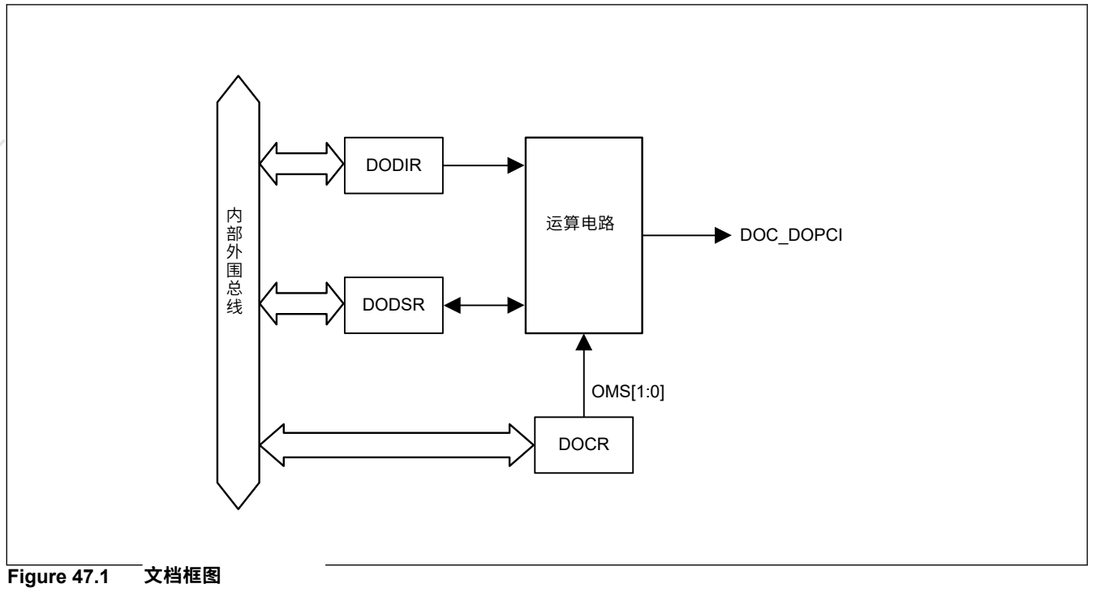


Figure 47.1 文档框图

47.2 DOC寄存器说明

47.2.1 DOCR:DOC控制寄存器

Base address: DOC = 0x4010_9000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	Operating Mode Select 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
2	DCSEL*1	Detection Condition Select 0: Set DOPCF flag when data mismatch is detected 1: Set DOPCF flag when data match is detected	R/W
4:3	—	These bits are read as 0. The write value should be 0.	R/W
5	DOPCF	DOC Flag Indicates the result of an operation.	R
6	DOPCFCL	DOPCF Clear 0: Retain DOPCF flag state 1: Clear DOPCF flag	R/W
7	—	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (DOC Flag)

The DOPCF flag indicates the result of an operation.

[Setting conditions]

- The result of data comparison matches the condition selected in the DCSEL bit
- A data addition result is greater than 0xFFFF
- A data subtraction result is less than 0x0000

[Clearing condition]

- Writing 1 to the DOPCFCL bit

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

47.2.2 DODIR : DOC Data Input Register

Base address: DOC = 0x4010_9000

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	It stores 16-bit data used in the operations.	R/W

Bit	Symbol	Function	R/W
1:0	OMS[1:0]	操作模式选择 00：数据比较模式01：数据加法模式10：数据减法模式11：禁止设置	R/W
2	DCSEL*1	检测条件选择 0：检测到数据不匹配时设置DOPCF标志1：检测到数据匹配时设置DOPCF标志	R/W
4:3	—	这些位被读取为0。写入值应为0。	R/W
5	DOPCF	文档标志 表示操作的结果。	R
6	DOPCFCL	DOPCF Clear 0：保持DOPCF标志状态1：清除DOPCF标志	R/W
7	—	这些位被读取为0。写入值应为0。	R/W

注1.仅在选择数据比较模式时有效。

OMS[1:0]位（操作模式选择）

OMS[1:0]位选择DOC的工作模式。

DCSEL位（检测条件选择）

DCSEL位选择数据比较模式下的检测条件。该位仅在选择数据比较模式时有效。

DOPCF flag (DOC Flag)

DOPCF标志指示操作的结果。

[Setting conditions]

●数据比较的结果符合DCSEL位中选择的条件

●数据相加结果大于0xFFFF

●数据减法结果小于0x0000

[Clearing condition]

●DOPCFCL位写1

DOPCFCL bit (DOPCF Clear)

将DOPCFCL位设置为1会清除DOPCF标志。该位读为0。

47.2.2 DODIR:DOC数据输入寄存器

Base address: DOC = 0x4010_9000

Offset address: 0x02

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	它存储操作中使用的16位数据。	R/W

47.2.3 DODSR : DOC Data Setting Register

Base address: DOC = 0x4010_9000

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	It stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.	R/W

47.3 Operation

47.3.1 Data Comparison Mode

Figure 47.2 shows an example operation in data comparison mode operation by the DOC. The following sequence is an example operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison):

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set 16-bit reference data in DODSR.
3. Write the 16-bit data for comparison to DODIR.
4. Continue writing the 16-bit data until all data for comparison is written to DODIR.
5. If a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1.

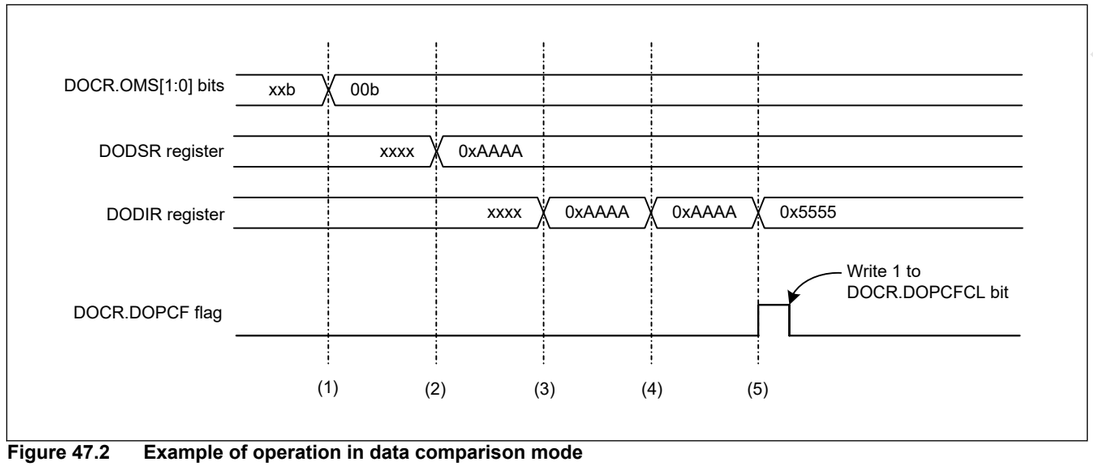


Figure 47.2 Example of operation in data comparison mode

47.3.2 Data Addition Mode

Figure 47.3 shows an example operation in data addition mode. The steps are as follows:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be added to the DODIR register. The result of the operation is stored in the DODSR register.
4. Continue writing the 16-bit data until all data to be added is written to the DODIR.
5. If the result of an operation is greater than 0xFFFF, the DOCR.DOPCF flag is set to 1.

47.2.3 DODSR:DOC数据设置寄存器

Base address: DOC = 0x4010_9000

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
15:0	n/a	它存储在数据比较模式中用作参考的16位数据。该寄存器还存储数据加法和减法模式下的运算结果。	R/W

47.3 Operation

47.3.1 数据比较模式

图47.2显示了DOC在数据比较模式操作中的示例操作。以下序列是DCSEL设置为0时的示例操作（通过数据比较检测到数据不匹配）：

1.将00b写入DOCR.OMS[1:0]位以选择数据比较模式。

2.在DODSR中设置16位参考数据。

3.将16位数据写入DODIR进行比较。

4.继续写入16位数据，直到所有用于比较的数据都写入DODIR。

5.如果写入DODIR的值与DODSR中的值不匹配，则DOCR.DOPCF标志设置为1。

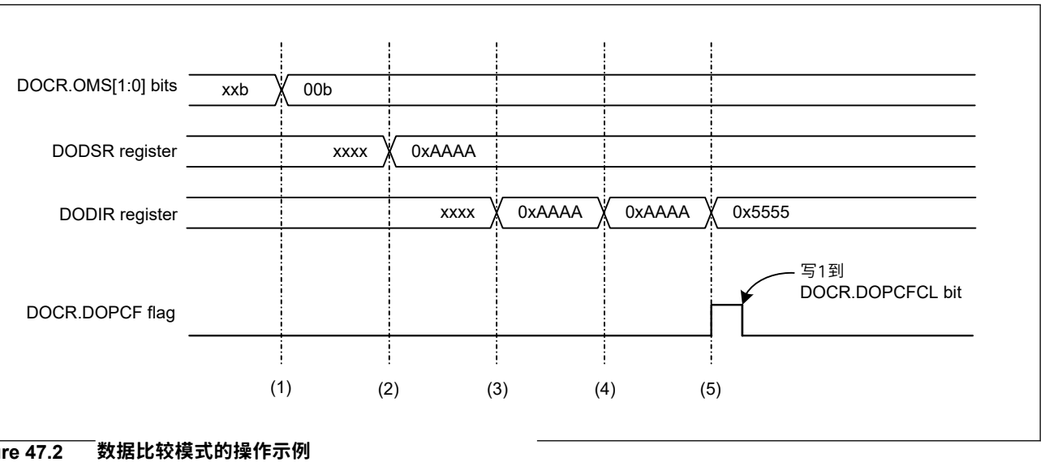


Figure 47.2 数据比较模式的操作示例

47.3.2 数据加法模式

图47.3显示了数据添加模式下的示例操作。步骤如下：

1.将01b写入DOCR.OMS[1:0]位以选择数据添加模式。

2.在DODSR寄存器中设置16位数据作为初始值。

3.将要添加的16位数据写入DODIR寄存器。运算结果存储在DODSR寄存器中。

4.继续写入16位数据，直到所有要添加的数据都写入DODIR。

5.如果运算结果大于0xFFFF，则DOCR.DOPCF标志设置为1。

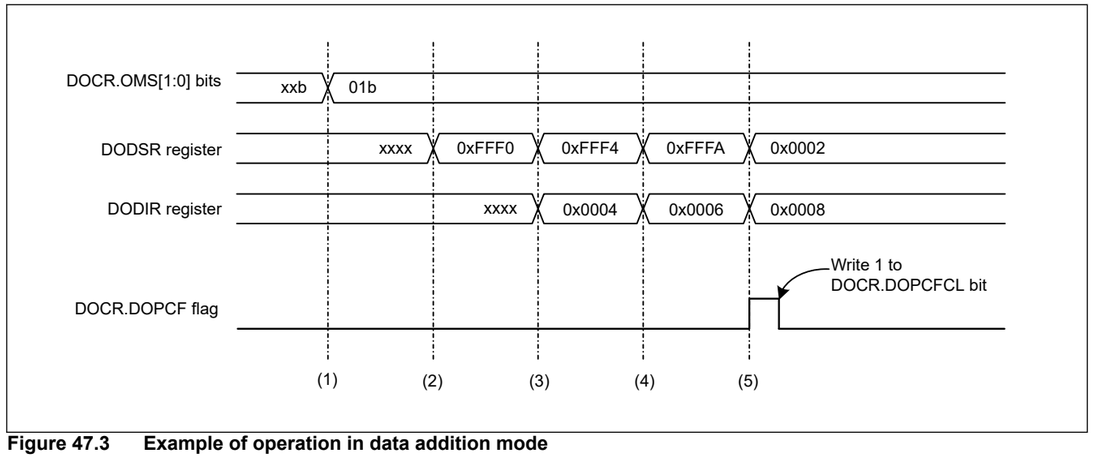


Figure 47.3 Example of operation in data addition mode

47.3.3 Data Subtraction Mode

Figure 47.4 shows an example operation in data subtraction mode. The steps are as follows:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data as the initial value in the DODSR register.
3. Write the 16-bit data to be subtracted to the DODIR register. The result of the operation is stored in DODSR.
4. Continue writing the 16-bit data to the DODIR register until all data to be subtracted is written.
5. If the result of an operation is less than 0x0000, the DOCR.DOPCF flag is set to 1.

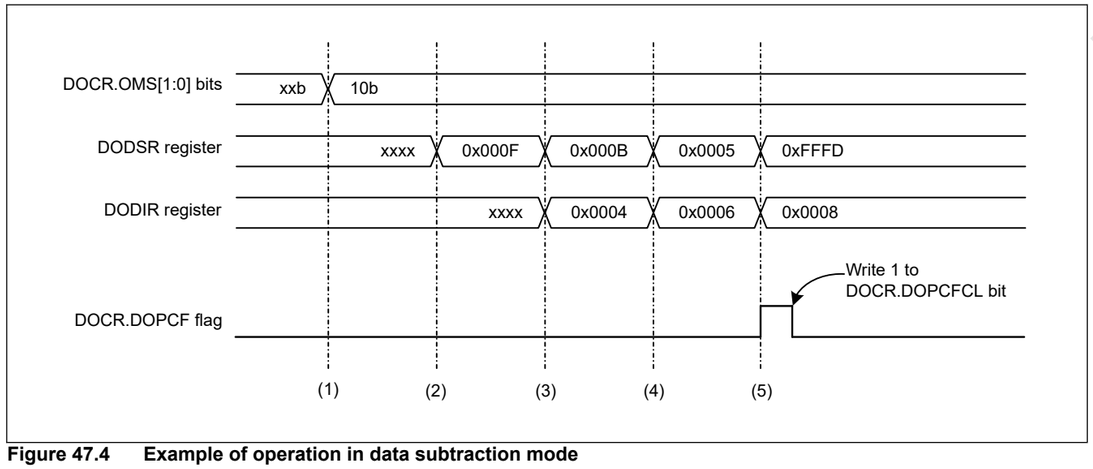


Figure 47.4 Example of operation in data subtraction mode

47.4 Interrupt Source

The DOC generates the DOC interrupt (DOC_DOPCI) as an interrupt request. Table 47.2 describes the DOC interrupt request.

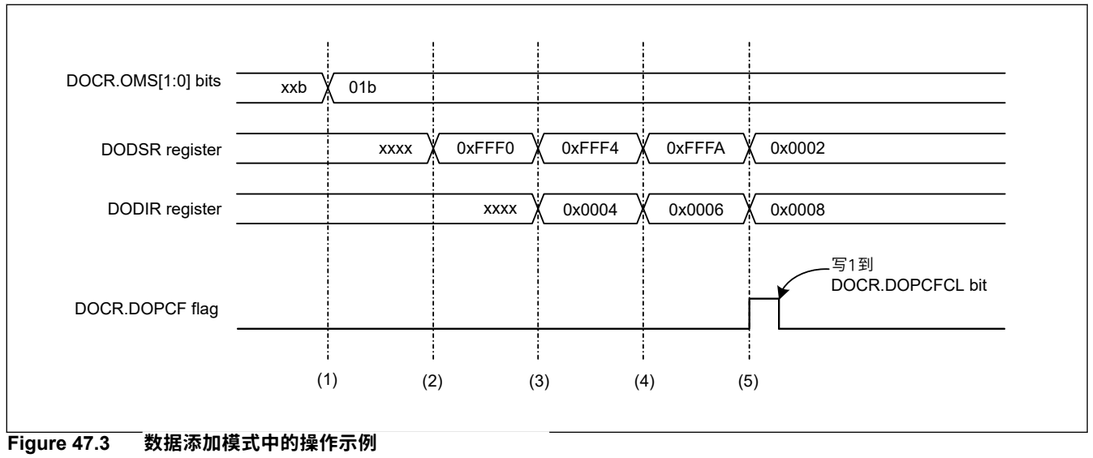


Figure 47.3 数据添加模式中的操作示例

47.3.3 数据减法模式

图47.4显示了数据减法模式下的示例操作。步骤如下：

1.将10b写入DOCR.OMS[1:0]位以选择数据减法模式。

2.在DODSR寄存器中设置16位数据作为初始值。

3.将要减去的16位数据写入DODIR寄存器。操作结果存储在DODSR中。

4.继续将16位数据写入DODIR寄存器，直到写入所有要减去的数据。

5.如果运算结果小于0x0000，则DOCR.DOPCF标志设置为1。

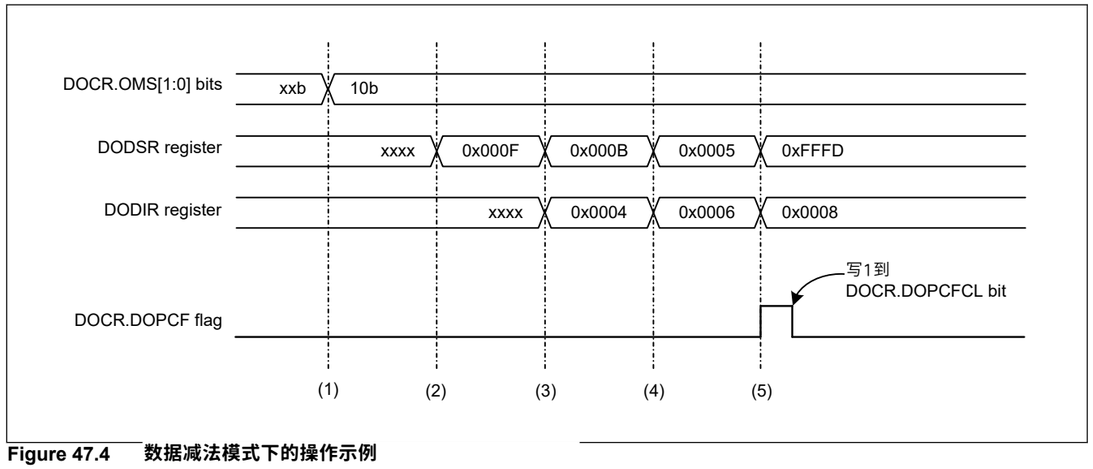


Figure 47.4 数据减法模式下的操作示例

47.4 中断源

DOC生成DOC中断(DOC_DOPCI)作为中断请求。表47.2描述了DOC中断请求。

Table 47.2 Interrupt request from DOC

Interrupt request	Status flag	Interrupt source
DOC interrupt	DOPCF	• The result of data comparison matches the condition selected in the DOCR.DCSEL bit. • The result of data addition is greater than 0xFFFF. • The result of data subtraction is less than 0x0000.

47.5 Output of an Event Signal to the Event Link Controller (ELC)

The DOC outputs an event signal for the ELC under the following conditions:

- The compared values either match or mismatch
- The data addition result is greater than 0xFFFF
- The data subtraction result is less than 0x0000

This signal can be used to initiate operations by other modules selected in advance and can also be used as an interrupt request. When an event signal is generated, the DOC Flag (DOCR.DOPCF) is set to 1.

47.6 Usage Notes

47.6.1 Settings for the Module-Stop State

The module Stop Control Register C (MSTPCRC) can enable or disable DOC operation. The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 10, Low Power Modes.

Table 47.2 来自DOC的中断请求

中断请求	状态标志	中断源
文档中断	DOPCF	• 数据比较的结果与DOCR.DCSEL位中选择的条件相匹配。 • 数据相加的结果大于0xFFFF。 • 数据减法的结果小于0x0000。

47.5 将事件信号输出到事件链接控制器(ELC)

DOC在以下条件下为ELC输出事件信号：

●比较值匹配或不匹配

●数据相加结果大于0xFFFF

●数据减法结果小于0x0000

该信号可用于启动其他预先选择的模块的操作，也可用作中断请求。生成事件信号时，DOC标志(DOCR.DOPCF)设置为1。

47.6 使用说明

47.6.1 模块停止状态的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用DOC操作。DOC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第10节，低功耗模式。

RA生态工作室

48. SRAM

48.1 Overview

The MCU provides an on-chip, high-density SRAM module with either parity-bit checking or Error Correction Code (ECC). The first 64 KB area of the SRAM0 is the ECC. Parity check is performed on the other areas.

Table 48.1 lists the SRAM specifications.

Table 48.1 SRAM specifications

Parameter	Without ECC	With ECC
SRAM capacity	SRAM0: 448 KB	SRAM0: 64 KB
SRAM address	SRAM0: 0x2001_0000 to 0x2007_FFFF	SRAM0: 0x2000_0000 to 0x2000_FFFF
Access	Wait states are inserted into the read cycle by default. If the ICLK frequency is faster than 100 MHz, wait state is required. If the ICLK frequency is 100 MHz or less, a wait state is not required. For details, see section 48.3.9. Access Cycle	
Data retention function	Not available in deep standby mode	
Module-stop function	Module-stop state can be set to reduce power consumption	
Parity	Even parity with 8-bit data and 1-bit parity	No parity
Error checking	even-parity（Date:8bit, parity:1bit）	SEC-DED (Single-Error Correction and Double-Error Detection Code)
Security	TrustZone Filter is integrated for memory access and SFR access. Access to the memory space is controlled by setting the memory Security Attribution (SA). And, access to I/O space (SFR) space is controlled by setting the register SA. See section 48.3.6. TrustZone Filter function.	

48.2 Register Descriptions

48.2.1 SRAMSAR : SRAM Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SRAMSA2	SRAMSA1	SRAMSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SRAMSA0	Security attributes of registers for SRAM Protection 0: Secure 1: Non-Secure	R/W
1	SRAMSA1	Security attributes of registers for SRAM Protection 2 0: Secure 1: Non-Secure	R/W
2	SRAMSA2	Security attributes of registers for ECC Relation 0: Secure 1: Non-Secure	R/W
31:3	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

48. SRAM

48.1 Overview

MCU提供片上高密度SRAM模块，具有奇偶校验位检查或纠错码(ECC)。SRAM0的第一个64KB区域是ECC。对其他区域执行奇偶校验。

表48.1列出了SRAM规格。

Table 48.1 SRAM specifications

Parameter	Without ECC	With ECC
SRAM capacity	SRAM0: 448 KB	SRAM0: 64 KB
SRAM address	SRAM0: 0x2001_0000 to 0x2007_FFFF	SRAM0: 0x2000_0000 to 0x2000_FFFF
Access	默认情况下，等待状态被插入到读取周期中。如果ICLK频率快于100MHz，则需要等待状态。如果ICLK频率为100MHz或更低，则不需要等待状态。详见48.3.9节。访问周期	
数据保留功能	在深度待机模式下不可用	
Module-stop function	可设置模块停止状态以降低功耗	
Parity	8位数据和1位奇偶校验的偶校验	无平价
错误检查	even-parity（Date:8bit, parity:1bit）	SEC-DED（单纠错和双纠错 Detection Code)
Security	TrustZone过滤器集成用于内存访问和SFR访问。通过设置内存安全属性（SA）来控制对内存空间的访问。并且，通过设置寄存器SA来控制对IO空间(SFR)空间的访问。请参见第48.3.6节。TrustZone过滤功能。	

48.2 注册说明

48.2.1 SRAMSAR：SRAM安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	SRAMSA2	SRAMSA1	SRAMSA0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	SRAMSA0	SRAM保护寄存器的安全属性 0: Secure 1: Non-Secure	R/W
1	SRAMSA1	SRAM保护2的寄存器的安全属性 0: Secure 1: Non-Secure	R/W
2	SRAMSA2	ECC关系寄存器的安全属性 0: Secure 1: Non-Secure	R/W
31:3	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: This register is write-protected by PRCR register.

SRAMSA0 bit (Security attributes of registers for SRAM Protection)

Security attributes of registers for SRAM Protection. The target registers are as follow.

- PARIOAD
- SRAMPRCR

SRAMSA1 bit (Security attributes of registers for SRAM Protection 2)

Security attributes of registers for SRAM Protection 2. The target registers are as follow.

- SRAMWTSC
- SRAMPRCR2

SRAMSA2 bit (Security attributes of registers for ECC Relation)

Security attributes of registers for ECC Relation. The target registers are as follow.

- ECCMODE
- ECC2STS
- ECC1STSEN
- ECC1STS
- ECCPRCR
- ECCPRCR2
- ECCETST
- ECCOAD

48.2.2 PARIOAD : SRAM Parity Error Operation After Detection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Reset 1: Non-maskable interrupt	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writes. Always set the SRAMPRCR bit in SRAMPRCR to enabled before writing to this bit. Do not write to the PARIOAD register while accessing the SRAM.

OAD bit (Operation After Detection)

The OAD bit specifies either a reset or non-maskable interrupt when a parity error is detected. The OAD bit is used for SRAM0 (without ECC)/Standby SRAM.

Note: 该寄存器由PRCR寄存器写保护。

SRAMSA0位（SRAM保护寄存器的安全属性）

SRAM保护寄存器的安全属性。目标寄存器如下。

- PARIOAD
- SRAMPRCR

SRAMSA1位（SRAM保护2寄存器的安全属性）

SRAM保护寄存器的安全属性2。目标寄存器如下。

- SRAMWTSC
- SRAMPRCR2

SRAMSA2位（ECC关系寄存器的安全属性）

ECC关系的寄存器的安全属性。目标寄存器如下。

- ECCMODE
- ECC2STS
- ECC1STSEN
- ECC1STS
- ECCPRCR
- ECCPRCR2
- ECCETST
- ECCOAD

48.2.2 PARIOAD：检测寄存器后的SRAM奇偶校验错误操作

Base address: SRAM = 0x4000_2000

Offset address: 0x00

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：复位1：不可屏蔽中断	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

PARIOAD寄存器控制检测奇偶校验错误时的操作。SRAM保护寄存器(SRAMPRCR)保护该寄存器不被写入。在写入该位之前，始终将SRAMPRCR中的SRAMPRCR位设置为启用。访问SRAM时不要写入PARIOAD寄存器。

OAD位（检测后操作）

当检测到奇偶校验错误时，OAD位指定复位或不可屏蔽中断。OAD位用于SRAM0 (without ECC)/Standby SRAM.

48.2.3 SRAMPRCR : SRAM Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0x04

Bit position:	7						1	0
Bit field:	KW[6:0]							SRAMPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR	Register Write Control 0: Disable writes to protected registers 1: Enable writes to protected registers	R/W
7:1	KW[6:0]	Write Key Code These bits enable or disable writes to the SRAMPRCR bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the PARIOAD register. Setting the bit to 1 enables writes to the PARIOAD register. When you write to this bit, always write 0x78 to KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, always write 0x78 to these bits simultaneously. When a value other than 0x78 is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

48.2.4 SRAMWTSC : SRAM Wait State Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SRAM0WTEN
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	SRAM0WTEN	SRAM0 wait enable 0: No wait 1: Add wait state in read access cycle to SRAM0	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

This register can be rewritten only when the SRAMPRCR2 bit in the SRAMPRCR2 register is 1.

The protection register (SRAMPRCR2) protects this register against writing. Change the effective bit in the protection register (SRAMPRCR2) to write in this register.

Do not write to SRAMWTSC while access to SRAM is in progress.

48.2.3 SRAMPRCR:SRAM保护寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0x04

Bit position:	7						1	0
Bit field:	KW[6:0]							SRAMPRCR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR	寄存器写控制 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W
7:1	KW[6:0]	编写关键代码 这些位启用或禁用对SRAMPRCR位的写入	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SRAMPRCR位（寄存器写控制）

SRAMPRCR位控制PARIOAD寄存器的写模式。将该位设置为1可以写入PARIOAD寄存器。写入该位时，始终同时将0x78写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对SRAMPRCR位的写入。当您写入SRAMPRCR位时，请始终同时将0x78写入这些位。当向KW[6:0]写入0x78以外的值时，SRAMPRCR位不会更新。KW[6:0]位总是被读取为0x00。

48.2.4 SRAMWTSC:SRAM等待状态控制寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0x08

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	SRAM0WTEN
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	SRAM0WTEN	SRAM0等待使能 0：无等待1：在SRAM0读访问周期中添加等待状态	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

只有当SRAMPRCR2寄存器中的SRAMPRCR2位为1时，才能重写该寄存器。

保护寄存器(SRAMPRCR2)保护该寄存器不被写入。更改保护寄存器(SRAMPRCR2)中的有效位以写入该寄存器。

在访问SRAM的过程中不要写入SRAMWTSC。

SRAM0WTEN bit (SRAM0 wait enable)

This bit sets the wait cycle to the operation region in SRAM0 (Both parity and ECC areas). When it is set 1 in the SRAM0WTEN bit, 1 wait cycle is inserted into the read cycle of operation region in SRAM0. And also 1 wait cycle is also inserted between the “write to read/write” sequential cycle in the same mat of SRAM0. When read access frequency is more than 100 MHz, it is necessary to set 1 wait cycle in SRAM0WTEN bit.

48.2.5 SRAMPRCR2 : SRAM Protection Register 2

Base address: SRAM = 0x4000_2000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							SRAMPRCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR2	Register Write Control 0: Disable writes to the protectedregisters 1: Enable writes to the protected registers	R/W
7:1	KW[6:0]	Write Key Code These bits enable or disable writes to the SRAMPRCR2 bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

SRAMPRCR2 bit (Register Write Control)

The SRAMPRCR2 bit controls the write mode of the SRAMWTSC register. Setting the bit to 1 enables writes to the SRAMWTSC register. When you write to this bit, always write 0x78 to KW[6:0] at the same time.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR2 bit. When you write to SRAMPRCR2 bit, always write 0x78 to these bits at the same time. When a value other than 0x78 is written to KW[6:0], the SRAMPRCR2 bit is not updated. The KW[6:0] bits are always read as 0x00.

48.2.6 ECCMODE : ECC Operating Mode Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ECCMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ECCMOD[1:0]	ECC Operating Mode Select 0 0: Disable ECC function 0 1: Setting prohibited 1 0: Enable ECC function without error checking 1 1: Enable ECC function with error checking	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

SRAM0WTEN位（SRAM0等待使能）

该位将等待周期设置为SRAM0中的操作区域（奇偶校验和ECC区域）。当它设置为1时SRAM0WTEN位，1个等待周期插入到SRAM0中操作区的读周期。并且在SRAM0的同一块中的“写到读”顺序周期之间也插入了1个等待周期。当读访问频率大于100MHz时，需要在SRAM0WTEN位中设置1个等待周期。

48.2.5 SRAMPRCR2：SRAM保护寄存器2

Base address: SRAM = 0x4000_2000

Offset address: 0x0C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							SRAMPRCR2
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SRAMPRCR2	寄存器写控制 0：禁止写保护寄存器1：允许写保护寄存器	R/W
7:1	KW[6:0]	编写关键代码 这些位启用或禁用对SRAMPRCR2位的写入	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

SRAMPRCR2位（寄存器写控制）

SRAMPRCR2位控制SRAMWTSC寄存器的写模式。将该位设置为1可以写入SRAMWTSC寄存器。写入该位时，始终同时将0x78写入KW[6:0]。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对SRAMPRCR2位的写入。当您写入SRAMPRCR2位时，请始终同时向这些位写入0x78。当向KW[6:0]写入0x78以外的值时，SRAMPRCR2位不会更新。KW[6:0]位总是被读取为0x00。

48.2.6 ECCMODE:ECC操作模式控制寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	ECCMOD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	ECCMOD[1:0]	ECC操作模式选择 00：禁用ECC功能01：设置禁止10：启用ECC功能不进行错误检查11：启用ECC功能并进行错误检查	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

The ECCMODE register specifies the ECC operating mode. The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this register, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCMODE register while accessing the SRAM.

ECCMOD[1:0] bits (ECC Operating Mode Select)

The ECCMOD[1:0] bits set the access mode to the ECC area in SRAM0.

48.2.7 ECC2STS : ECC 2-Bit Error Status Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC2ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC2ERR	ECC 2-Bit Error Status 0: No 2-bit ECC error occurred 1: 2-bit ECC error occurred	R/W*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the bit.

ECC2ERR bit (ECC 2-Bit Error Status)

The ECC2ERR bit indicates whether a 2-bit ECC error occurred in the ECC area of SRAM0. When a 2-bit error is detected while ECC operations are enabled and error checking is selected, theECC2ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 2-bit ECC error can be cleared by writing 0 to the ECC2ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in SRAM0 while writing 0 to this register.

48.2.8 ECC1STSEN : ECC 1-Bit Error Information Update Enable Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	E1STSEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	E1STSEN	ECC 1-Bit Error Information Update Enable 0: Disable updating of 1-bit ECC error information 1: Enable updating of 1-bit ECC error information	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

ECCMODE寄存器指定ECC工作模式。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该寄存器之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。访问SRAM时不要写入ECCMODE寄存器。

ECCMOD[1:0]位（ECC操作模式选择）

ECCMOD[1:0]位将访问模式设置为SRAM0中的ECC区域。

48.2.7 ECC2STS：ECC2位错误状态寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC1

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC2ERR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC2ERR	ECC2位错误状态 0：未发生2位ECC错误1：发生2位ECC错误	R/W*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

注1.只能写入0来清除该位。

ECC2ERR位（ECC2位错误状态）

ECC2ERR位指示SRAM0的ECC区域是否发生2位ECC错误。当启用ECC操作并选择错误检查时检测到2位错误时，ECC2ERR位设置为1。此时SRAM错误信号也被置位。将0写入ECC2ERR位可清除2位ECC错误。

SRAM错误可以指定为不可屏蔽中断或ECCOAD寄存器中的复位。向该寄存器写入0时不要访问SRAM0中的ECC区域。

48.2.8 ECC1STSEN：ECC1位错误信息更新使能寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC2

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	E1STSEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	E1STSEN	ECC1位错误信息更新启用 0：禁止更新1位ECC错误信息1：允许更新1位ECC错误信息	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

The ECC1STSEN register enables or disables updating of the ECC 1-bit Error Status Register (ECC1STS) in response to a 1-bit error ECC error in the SRAM0 (ECC area).

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled).

E1STSEN bit (ECC 1-Bit Error Information Update Enable)

The E1STSEN bit enables or disables updating of the SRAM (ECC area) 1-Bit Error Status Register (ECC1STS) in response to a 1-bit error in the ECC area of SRAM0. This register also functions as an interrupt or a reset mask.

48.2.9 ECC1STS : ECC 1-Bit Error Status Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC1ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC1ERR	ECC 1-Bit Error Status 0: No 1-bit ECC error occurred 1: 1-bit ECC error occurred	R/(W)*1
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:

- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

- Secure and Non-secure access are allowed.

Note 1. Only 0 can be written to clear the bit.

ECC1ERR bit (ECC 1-Bit Error Status)

The ECC1ERR bit indicates whether a 1-bit ECC error occurred in the ECC area of SRAM0. When a 1-bit error is detected while ECC operations are enabled and error checking is selected, theECC1ERR bit is set to 1. The SRAM error signal is also asserted at this time. The 1-bit ECC error can be cleared by writing 0 to the ECC1ERR bit.

The SRAM error can be specified as a non-maskable interrupt or a reset in the ECCOAD register. Do not access the ECC area in SRAM0 while writing 0 to this register.

48.2.10 ECCPRCR : ECC Protection Register

Base address: SRAM = 0x4000_2000

Offset address: 0xC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							ECCPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR	Register Write Control 0: Disable writes to the protected registers 1: Enable writes to the protected registers	R/W

- 允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

ECC1STSEN寄存器启用或禁用ECC1位错误状态寄存器(ECC1STS)的更新，以响应SRAM0（ECC区域）中的1位错误ECC错误。

ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。

E1STSEN位（ECC1位错误信息更新使能）

E1STSEN位启用或禁用SRAM（ECC区域）1位错误状态寄存器(ECC1STS)的更新，以响应SRAM0的ECC区域中的1位错误。该寄存器还用作中断或复位掩码。

48.2.9 ECC1STS:ECC1位错误状态寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC3

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	ECC1ERR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECC1ERR	ECC1位错误状态 0：未发生1位ECC错误1：发生1位ECC错误	R/(W)*1
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●

允许安全访问和非安全读取访问

- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●

允许安全和非安全访问。

注1.只能写入0来清除该位。

ECC1ERR位（ECC1位错误状态）

ECC1ERR位指示SRAM0的ECC区域是否发生1位ECC错误。如果在启用ECC操作并选择错误检查时检测到1位错误，则ECC1ERR位设置为1。此时SRAM错误信号也被置位。将0写入ECC1ERR位可清除1位ECC错误。

SRAM错误可以指定为不可屏蔽中断或ECCOAD寄存器中的复位。向该寄存器写入0时不要访问SRAM0中的ECC区域。

48.2.10 ECPCRR:ECC保护寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xC4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW[6:0]							ECCPRCR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR	寄存器写控制 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W

Bit	Symbol	Function	R/W
7:1	KW[6:0]	Write Key Code 0x78: Enable write to the ECCPRCR bit Others: Disable write to the ECCPRCR bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ECCPRCR bit (Register Write Control)

The ECCPRCR bit controls the write of the ECCMODE, ECC1STSEN, and ECCOAD registers. When this bit is set to 1, writing to the ECCMODE, ECC1STSEN, and ECCOAD registers is enabled. When writing to this bit, write 0x78 to the KW[6:0] bits at the same time.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the ECCPRCR bit. When writing toECCPRCR bit, write 0x78 to the KW[6:0] bits at the same time. When a value other than 0x78 is written to theKW[6:0] bits, the ECCPRCR bit is not updated. The KW[6:0] bits are always read as 0x00.

48.2.11 ECCPRCR2 : ECC Protection Register 2

Base address: SRAM = 0x4000_2000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW2[6:0]							ECCPRCR2
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR2	Register Write Control 0: Disable writes to the protected registers 1: Enable writes to the protected registers	R/W
7:1	KW2[6:0]	Write Key Code 0x78: Enable write to the ECCPRCR2 bit Others: Disable write to the ECCPRCR2 bit	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

ECCPRCR2 bit (Register Write Control)

The ECCPRCR2 bit controls the write mode of the ECCETST register. When the ECCPRCR2 bit is set to 1, writes to the ECCETST register is enabled. When writing to this bit, write 0x78 to the KW2[6:0] bits at the same time.

KW2[6:0] bits (Write Key Code)

The KW2[6:0] bits enable or disable writes to the ECCPRCR2 bit. When writing to ECCPRCR2 bit, write 0x78 to the KW2[6:0] bits at the same time. When a value other than 0x78 is written to the KW2[6:0] bits, the ECCPRCR2 bit is not updated. The KW2[6:0] bits are always read as 0x00.

Bit	Symbol	Function	R/W
7:1	KW[6:0]	编写关键代码 0x78：允许写入ECPCRR位 其他：禁止写入ECPCRR位	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECPCRR位（寄存器写控制）

ECPCRR位控制ECCMODE、ECC1STSEN和ECCOAD寄存器的写入。当该位设置为1时，允许写入ECCMODE、ECC1STSEN和ECCOAD寄存器。写入该位时，同时将0x78写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对ECPCRR位的写入。写入ECCPRCR位时，同时向KW[6:0]位写入0x78。当向KW[6:0]位写入0x78以外的值时，不会更新ECPCRR位。KW[6:0]位总是被读取为0x00。

48.2.11 ECPCRR2:ECC保护寄存器2

Base address: SRAM = 0x4000_2000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	KW2[6:0]							ECCPRCR2
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ECCPRCR2	寄存器写控制 0：禁止写入受保护寄存器1：允许写入受保护寄存器	R/W
7:1	KW2[6:0]	编写关键代码 0x78：允许写入ECPCRR2位 其他：禁止写入ECPCRR2位	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECPCRR2位（寄存器写控制）

ECPCRR2位控制ECCETST寄存器的写模式。当ECPCRR2位设置为1时，写入ECCETST寄存器使能。写入该位时，同时向KW2[6:0]位写入0x78。

KW2[6:0]位（写入密钥代码）

KW2[6:0]位启用或禁用对ECPCRR2位的写入。当写入ECPCRR2位时，将0x78写入KW2[6:0]位。当向KW2[6:0]位写入0x78以外的值时，不会更新ECPCRR2位。KW2[6:0]位总是读为0x00。

48.2.12 ECCETST : ECC Test Control Register

Base address: SRAM = 0x4000_2000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TSTBYP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTBYP	ECC Bypass Select 0: Disable ECC bypass 1: Enable ECC bypass	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECC Protection Register 2 (ECCPRCR2) protects this register against writes. Before writing to this bit, set the ECCPRCR2 bit in the ECCPRCR2 register to 1 (write protection disabled). Do not write to the ECCETST register while accessing the SRAM.

TSTBYP bit (ECC Bypass Select)

The TSTBYP bit enables direct access to the ECC code by bypassing the ECC function. When the ECC bypass function is used, the ECCMOD[1:0] bits in the ECCMODE register are set to 00b. The ECC must be accessed in 32 bits using the same address for 32-bit data. The ECC code is assigned to the lower 7 bits of the 32-bit data. When writing the ECC code, the upper 25 bits are ignored. When reading the ECC code, the upper 25 bits are undefined.

Note: For details of ECC test, see section 48.3.4. ECC Decoder Testing.

48.2.13 ECCOAD : SRAM ECC Error Operation After Detection Register

Base address: SRAM = 0x4000_2000

Offset address: 0xD8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation After Detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

The ECC Protection Register (ECCPRCR) protects this register against writes. Before writing to this bit, set the ECCPRCR bit in the ECCPRCR register to 1 (write protection disabled). Do not write to the ECCOAD register while accessing the SRAM.

48.2.12 ECCETST:ECC测试控制寄存器

Base address: SRAM = 0x4000_2000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	TSTBYP
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	TSTBYP	ECC旁路选择 0：禁用ECC旁路1：启用ECC旁路	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECC保护寄存器2(ECCPRCR2)保护该寄存器不被写入。在写入该位之前，将ECPCRR2寄存器中的ECPCRR2位为1（写保护禁用）。访问SRAM时不要写入ECCETST寄存器。

TSTBYP位（ECC旁路选择）

TSTBYP位允许通过绕过ECC功能直接访问ECC代码。使用ECC旁路功能时，ECCMODE寄存器中的ECCMOD[1:0]位设置为00b。必须使用32位数据的相同地址以32位访问ECC。ECC代码分配给32位数据的低7位。写入ECC代码时，忽略高25位。读取ECC码时，高25位未定义。

Note: 有关ECC测试的详细信息，请参见第48.3.4节。ECC解码器测试。

48.2.13 ECCOAD：检测寄存器后的SRAMECC错误操作

Base address: SRAM = 0x4000_2000

Offset address: 0xD8

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	OAD
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后的操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将ECPCRR寄存器中的ECPCRR位设置为1（禁用写保护）。访问SRAM时不要写入ECCOAD寄存器。

OAD bit (Operation After Detection)

The OAD bit selects whether to generate a reset or a non-maskable interrupt when an ECC error is detected. The OAD bit in the ECCOAD register is used for SRAM0 (ECC area).

48.3 Operation

48.3.1 Module Stop Function

Power consumption can be reduced by setting module stop control register A (MSTPCRA) to stop supply of the clock signal to SRAM.

SRAM0 is controlled by SRAM0 bit in MSTPCRA register and, in the case of 1, SRAM0 becomes the clock stop state.

The SRAM is thus placed in the module-stop state by stopping supply of the clock signals. The SRAM operates after a reset.

SRAM is not accessible if it is in the module-stop state. A transition to the module-stop state should not be made while access to SRAM is in progress.

Access to the SRAM in the module-stop state is prohibited. If access is attempted, correct operation is not guaranteed.

For details on the MSTPCRA register, see section 10, Low Power Modes.

48.3.2 Correction of ECC errors

Enabling and disabling of ECC error correction can be selected through ECCMODE register setting. In the initial state, ECC error correction is disabled. The ECC check type is SEC-DED (Single-Error Correction and Double-Error Detection Code).

When ECC function is enabled, 7-bit check bits are appended to 32-bit data for writing. For reading, 39-bit (data: 32 bits, check bits: 7 bits) data is read out from the SRAM (ECC area).

When ECC function is enabled and error checking is selected by setting ECCMOD[1:0] in the ECCMODE register to 00b, error correction is done if a 1-bit error occurs and the ECC1ERR bit in the ECC1STS register is set to 1 if the E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, error detection is done and the ECC2ERR bit in the ECC2STS register is set to 1, though error correction is not performed.

When ECC function is enabled and the error checking is disable, error correction is done if a 1-bit error occurs but ECC1ERR bit in the ECC1STS register is not updated although E1STSEN bit in the ECC1STSEN register is 1. If a 2-bit error occurs, this error is detected but the ECC2ERR bit in the ECC2STS register is not updated, and error correction is not performed.

When ECC function is disable, neither error correction nor error detection is done although 1-bit or 2-bit error occur.

So ECC1ERR bit and ECC2ERR bit are not updated.

There is no way to confirm the location where the error was found. Therefore, when after the occurrence of an error, update all the data.

When updating all the data after the occurrence of an error, the only support of 32 bit data writing.

Since the SRAM data is undefined after power on and release from deep software standby mode, accessing the SRAM when ECC function is enabled and error checking is selected causes an ECC error to occur. Therefore, before using ECC function, initial writing with 32bit data size to the area to be used in the SRAM should be done.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, please do not perform the read access in a row after the write access.

48.3.3 ECC Error Interrupt Function

When ECC function is enabled and error checking is applied to the SRAM (ECC area), an ECC error occurs when either the ECC2ERR bit in the ECC2STS register or the ECC1ERR bit in the ECC1STS register becomes 1 to indicate that ECC checking revealed a 2-bit error or a 1-bit error, respectively.

An ECC erroris output with a pulse width of ICLK.When the ECC 1-bit error is to be masked, set the ECC1STSEN.E1STSEN bit to 0 to disable updating of the ECC1ERR bit. An ECC error will not be generated while ECC function is disabled or when ECC function is enabled but error checking is not selected.

OAD位（检测后操作）

OAD位选择在检测到ECC错误时是否产生复位或不可屏蔽中断。ECCOAD寄存器中的OAD位用于SRAM0（ECC区域）。

48.3 Operation

48.3.1 模块停止功能

通过设置模块停止控制寄存器A(MSTPCRA)停止向SRAM提供时钟信号，可以降低功耗。

SRAM0由MSTPCRA寄存器中的SRAM0位控制，在为1的情况下，SRAM0变为时钟停止状态。

因此，通过停止提供时钟信号，SRAM被置于模块停止状态。SRAM在复位后运行。

如果SRAM处于模块停止状态，则无法访问。在访问SRAM的过程中，不应转换到模块停止状态。

禁止在模块停止状态下访问SRAM。如果尝试访问，则无法保证正确操作。

有关MSTPCRA寄存器的详细信息，请参见第10节，低功耗模式。

48.3.2 纠正ECC错误

可以通过ECCMODE寄存器设置来选择ECC纠错的启用和禁用。在初始状态下，ECC纠错被禁用。ECC校验类型为SEC-DED（单纠错双错误检测码）。

当ECC功能使能时，7位校验位被附加到32位数据中进行写入。读取时，从SRAM（ECC区域）中读取39位（数据：32位，校验位：7位）数据。

当ECC功能使能并且通过将ECCMODE寄存器中的ECCMOD[1:0]设置为00b来选择错误检查时，如果发生1位错误，则进行纠错，并且如果ECC1STS寄存器中的ECC1ERR位设置为1，则ECC1STSEN寄存器中的E1STSEN位为1。如果发生2位错误，则进行错误检测并将ECC2STS寄存器中的ECC2ERR位设置为1，但不执行错误纠正。

当启用ECC功能且禁用错误检查时，如果发生1位错误，则进行错误纠正，但尽管ECC1STSEN寄存器中的E1STSEN位为1，但ECC1STS寄存器中的ECC1ERR位不更新。如果发生2位错误，则会检测到该错误，但不会更新ECC2STS寄存器中的ECC2ERR位，也不执行纠错。

当ECC功能被禁用时，即使发生1位或2位错误，也不会进行纠错或错误检测。

因此ECC1ERR位和ECC2ERR位不会更新。

无法确认发现错误的位置。因此，当发生错误后，更新所有数据。

发生错误后更新所有数据时，仅支持32位数据写入。

由于上电并从深度软件待机模式释放后SRAM数据未定义，因此在启用ECC功能并选择错误检查时访问SRAM会导致发生ECC错误。因此，在使用ECC功能之前，应先将32位数据大小的数据写入SRAM中要使用的区域。

在写访问之后连续执行读访问时，优先执行读访问。因此，在初始化过程中，请不要在写访问之后连续进行读访问。

48.3.3 ECC错误中断功能

当启用ECC功能并对SRAM（ECC区域）应用错误检查时，当任一ECC2STS寄存器中的ECC2ERR位或ECC1STS寄存器中的ECC1ERR位变为1，分别表示ECC检查发现2位错误或1位错误。

脉冲宽度为ICLK的ECC错误输出。当要屏蔽ECC1位错误时，设置ECC1STSEN.E1STSEN位为0以禁用ECC1ERR位的更新。禁用ECC功能或启用ECC功能但未选择错误检查时，不会产生ECC错误。

ECC error can choose non maskable interrupt or reset by ECCOAD register. When set 1 in the OAD bit of the ECCOAD register, ECC error is output to the Reset function. When set 0 in the OAD bit of the ECCOAD register, ECC Error interrupt is output to the ICU as non-maskable interrupt.

48.3.4 ECC Decoder Testing

Figure 48.1 shows the ECC decoder testing.

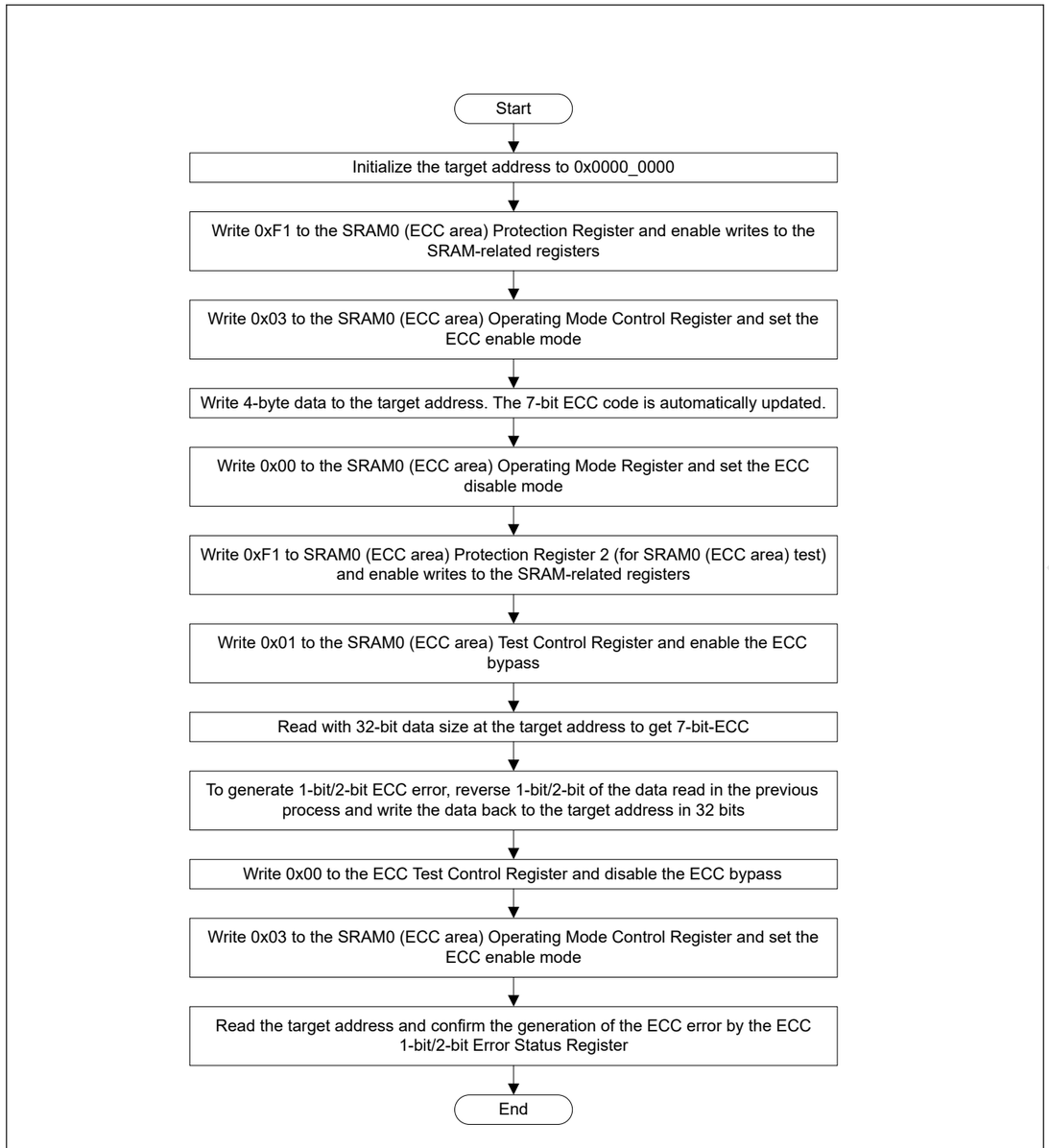


Figure 48.1 ECC decoder testing

ECC错误可以选择不可屏蔽中断或通过ECCOAD寄存器复位。当ECCOAD寄存器的OAD位设置为1时，ECC错误输出到复位功能。当ECCOAD寄存器的OAD位设置为0时，ECC错误中断作为不可屏蔽中断输出到ICU。

48.3.4 ECC解码器测试

图48.1显示了ECC解码器测试。

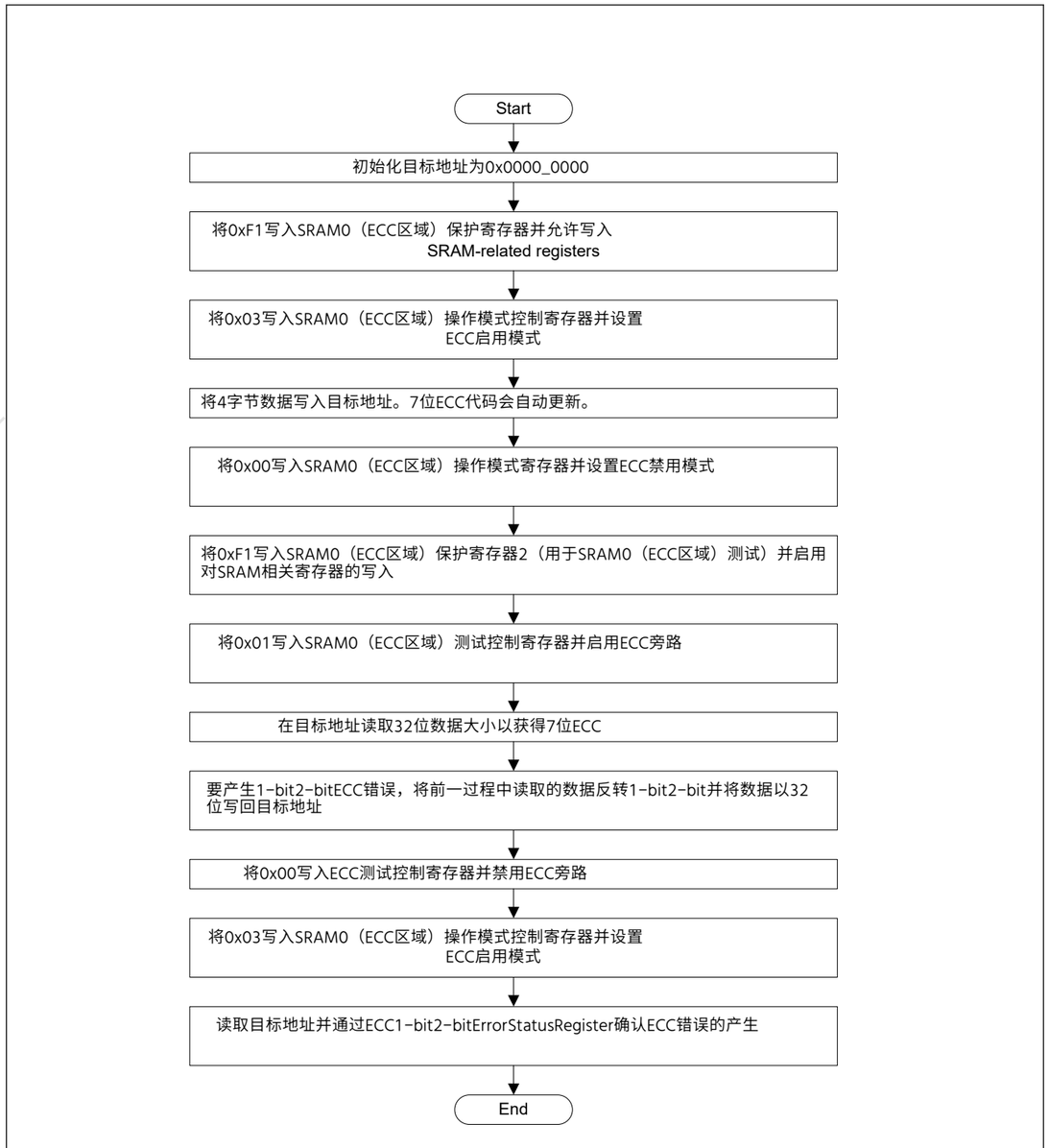


Figure 48.1 ECC解码器测试

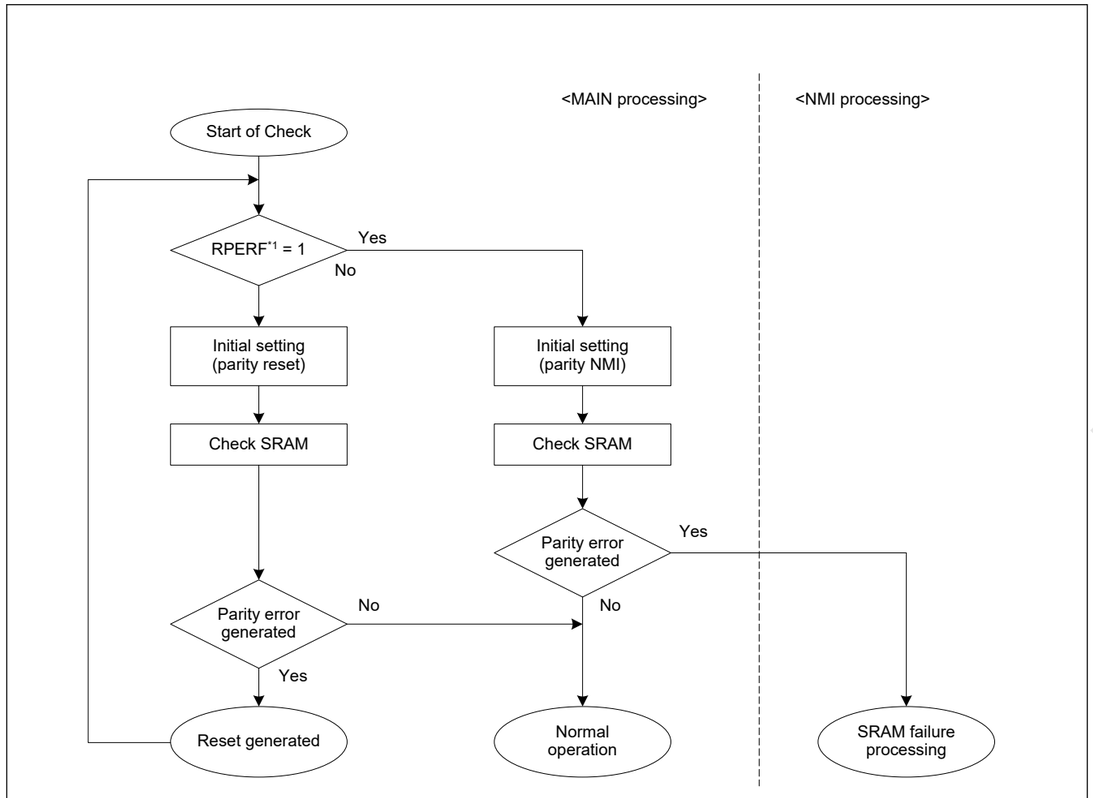
48.3.5 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. When data is written, a parity bit is added to every 8-bit data in the SRAM which has 32-bit data width, and when data is read, the parity is checked. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset.

The parity-error notification can be specified as a non-maskable interrupt or a reset in the OAD bit of the PARIOAD register. When the OAD bit is set to 1, a parity error is output to the reset function. When the OAD bit is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause of the parity error is noise or corruption, follow the parity check flows shown in Figure 48.2 and Figure 48.3.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, do not perform the read access in a row after the write access.



Note 1. RPERF: SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF bit)

Figure 48.2 Flow of SRAM parity check when SRAM parity reset is enabled

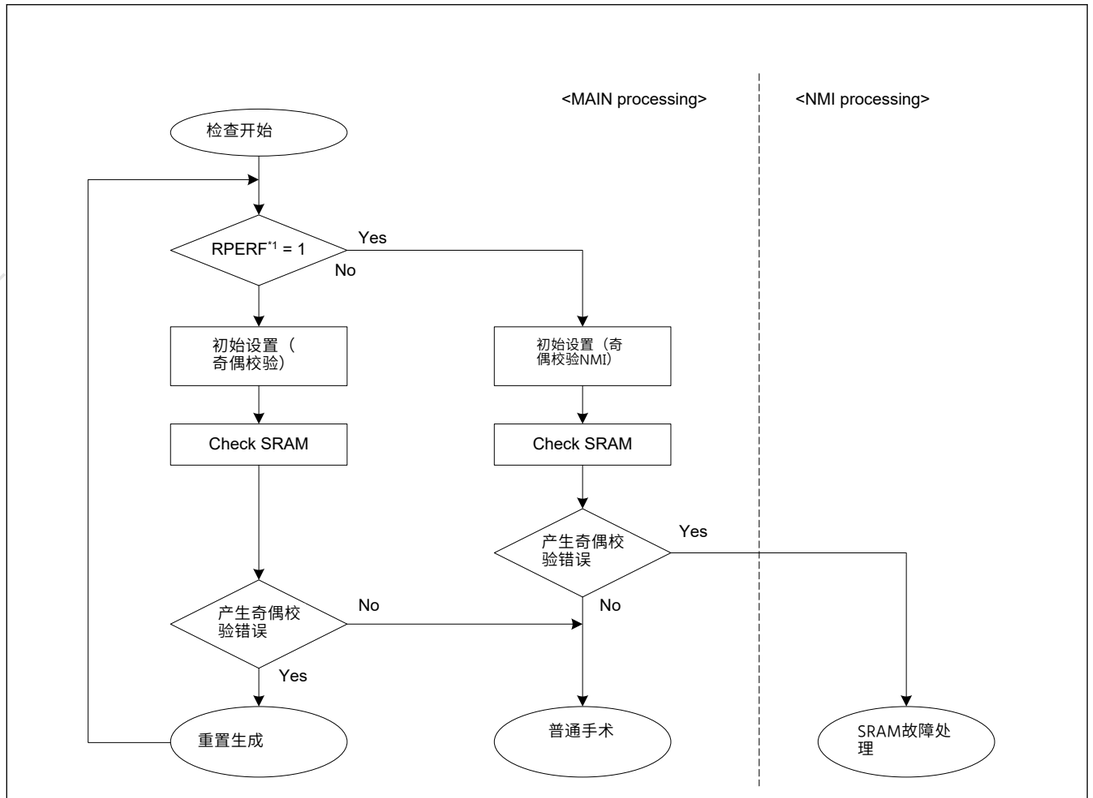
48.3.5 奇偶校验计算功能

IEC60730标准要求检查SRAM数据。写入数据时，对32位数据宽度的SRAM中的每8位数据添加一个奇偶校验位，读取数据时检查奇偶校验位。发生奇偶校验错误时，会生成奇偶校验错误通知。此功能也可用于触发复位。

奇偶校验错误通知可以指定为不可屏蔽中断或PARIOAD寄存器的OAD位中的复位。当OAD位设置为1时，奇偶校验错误输出到复位功能。当OAD位设置为0时，奇偶校验错误作为不可屏蔽中断输出到ICU。

奇偶校验错误经常因噪声而发生。要确认奇偶校验错误的原因是噪声还是损坏，请遵循图48.2和图48.3所示的奇偶校验流程。

在写访问之后连续执行读访问时，优先执行读访问。因此，在初始化过程中，不要在写访问之后连续执行读访问。



注1.RPERF：SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF位）

Figure 48.2 启用SRAM奇偶校验复位时的SRAM奇偶校验流程

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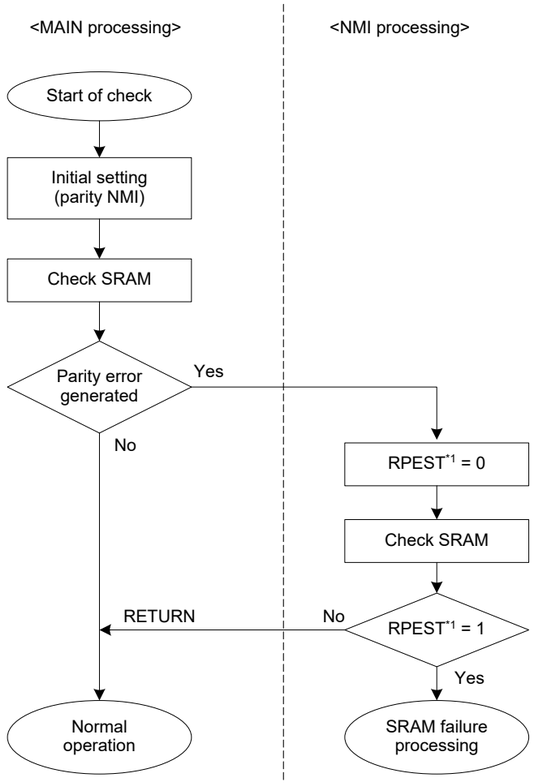


Note 1. RPEST: SRAM Parity Error Interrupt Status Flag (NMISR.RPEST bit)

Figure 48.3 Flow of SRAM parity check when SRAM parity interrupt is enabled

48.3.6 TrustZone Filter function

There are two types of TrustZone Filter function for SRAM.

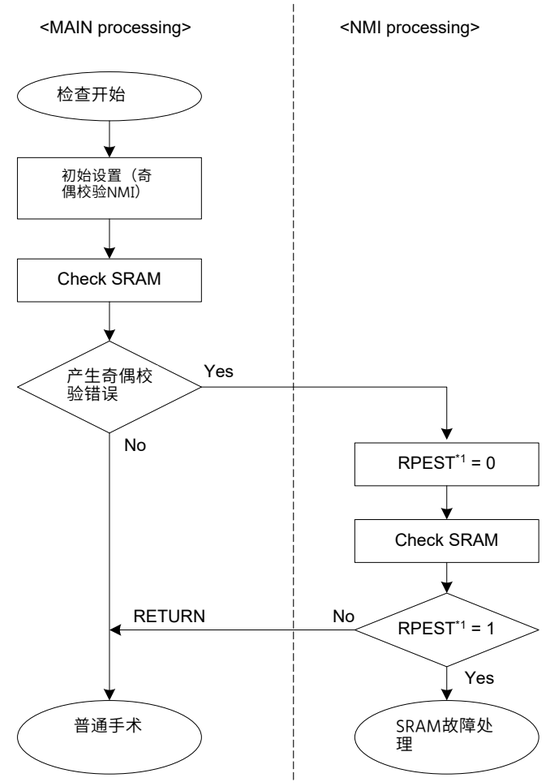
- TrustZone Filter for SRAM register protection
- TrustZone Filter for SRAM memory protection

48.3.6.1 TrustZone Filter for SRAM register protection

SRAM registers can be protected with a Security Attribution (SA) from Non-secure access. When SA indicates that SRAM registers are secure status, non-secure access can not overwrite them because TrustZone Filter detects finds an error and protects the write access. SA for SRAM registers is just one to be used commonly among SRAM registers.

Table 48.2 Register protection (1 of 2)

SA	Access status	Write access	Read access
Secure	Secure	Permit	Permit
	Non-secure	TrustZone Filter error Protected	Permit



注1.RPEST：SRAM奇偶校验错误中断状态标志（NMISR.RPEST位）

Figure 48.3 启用SRAM奇偶校验中断时的SRAM奇偶校验流程

48.3.6 TrustZone过滤器功能

SRAM有两种TrustZoneFilter功能。

- 用于SRAM寄存器保护的TrustZone过滤器
- 用于SRAM内存保护的TrustZone过滤器

48.3.6.1 用于SRAM寄存器保护的TrustZone过滤器

可以使用安全属性(SA)保护SRAM寄存器免受非安全访问。当SA指示SRAM寄存器处于安全状态时，非安全访问无法覆盖它们，因为TrustZoneFilter检测到发现错误并保护写访问。SRAM寄存器的SA只是SRAM寄存器中常用的一种。

Table 48.2 寄存器保护(1of2)

SA	访问状态	写访问	读取权限
Secure	Secure	Permit	Permit
	Non-secure	TrustZone过滤器错误受保护	Permit

Table 48.2 Register protection (2 of 2)

SA	Access status	Write access	Read access
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

When TrustZone Filter error for SRAM register access occurs, no error notification and no error response occurs.

48.3.6.2 TrustZone Filter for SRAM memory protection

SRAM memory, e.g. SRAM0 include ECC region and Parity can be divided into Secure/Non secure callable/Non secure status with Memory Security Attribution (MSA) and can be protected from Non-secure access. When MSA indicates that SRAM memory region are Secure or Non secure callable status, Non-secure access can't overwrite them.

Table 48.3 Memory protection

SA	Access status	Write access	Read access
Secure / Non secure callable	Secure	Permit	Permit
	Non-secure	TrustZone Filter error ● Protected ● Error response occurs	TrustZone Filter error ● Read data is 0 ● Error response occurs
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

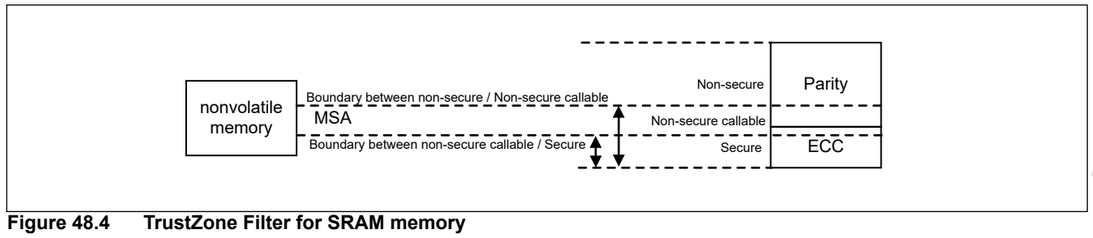


Figure 48.4 TrustZone Filter for SRAM memory

When TrustZone Filter error for SRAM memory access occurs, an error notification which become Reset request or NMI request occurs. See section 52.2. Arm TrustZone Security .

48.3.7 Interrupt Source

The SRAM interrupt source includes an ECC error, Parity error and TrustZone filter error. ECC error and Parity error can choose non-maskable interrupt or reset by OAD bit. When the debugger is connected, reset and non-maskable interrupt are maskable. Also, if these masks are set by the debugger, each status register is not set even if an ECC error occurs. For details on the debug mode, see section 2, CPU.

Table 48.4 SRAM Interrupt Source

Name	Interrupt Source	DTC Activation	DMAC Activation
ECCERR	ECC error (ECC operation region in SRAM0)	Not possible	Not possible
PARITYERR	Parity error	Not possible	Not possible
TZFLT	TrustZone filter error	Not possible	Not possible

48.3.8 Wait state

When ICLK frequencies is SRAM0 = 200 MHz to 100 MHz, if you want to access to the SRAM0, do not set 0x00 in wait enable bit for each RAM of the SRAMWTSC register, in order to insert a wait cycle. When the wait is not inserted, we cannot guarantee the operation.

Depending on the operating frequency of ICLK, the WAIT setting for SRAM access has the following conditions.

Table 48.2 注册保护(2of2)

SA	访问状态	写访问	读取权限
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

当发生SRAM寄存器访问的TrustZoneFilter错误时，不会发生错误通知和错误响应。

48.3.6.2 用于SRAM内存保护的TrustZone过滤器

SRAM存储器，例如SRAM0包括ECC区域和Parity可分为SecureNonsecurecallableNonsecurestatuswithMemory SecurityAttribution(MSA)并可防止非安全访问。当MSA指示SRAM内存区域为安全或非安全可调用状态时，非安全访问无法覆盖它们。

Table 48.3 内存保护

SA	访问状态	写访问	读取权限
安全非安全可调用	Secure	Permit	Permit
	Non-secure	TrustZone过滤器错误● ● 发生错误响应	TrustZone过滤器错误●读取数据为0 ● 发生错误响应
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

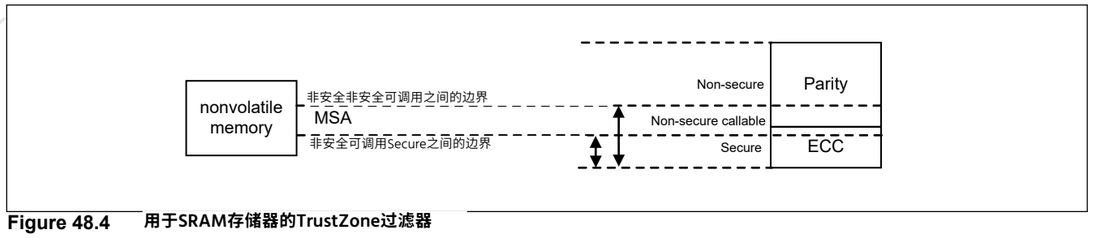


Figure 48.4 用于SRAM存储器的TrustZone过滤器

当发生SRAM内存访问的TrustZoneFilter错误时，会发生错误通知，成为Resetrequest或NMIrequest。请参阅第52.2节。ArmTrustZone安全。

48.3.7 中断源

SRAM中断源包括ECC错误、奇偶校验错误和TrustZone过滤器错误。ECC错误和奇偶校验错误可以选择不可屏蔽中断或通过OAD位复位。当调试器连接时，复位和不可屏蔽中断都是可屏蔽的。此外，如果调试器设置了这些掩码，则即使发生ECC错误，也不会设置每个状态寄存器。有关调试模式的详细信息，请参见第2节CPU。

Table 48.4 SRAM中断源

Name	中断源	DTC Activation	DMAC Activation
ECCERR	ECC错误（SRAM0中的ECC操作区域）	不可能	不可能
PARITYERR	奇偶校验错误	不可能	不可能
TZFLT	TrustZone过滤器错误	不可能	不可能

48.3.8 等待状态

当ICLK频率为SRAM0=200MHz至100MHz时，如果要访问SRAM0，请不要将SRAMWTSC寄存器的每个RAM的等待使能位设置为0x00，以便插入等待周期。当未插入等待时，我们无法保证操作。

根据ICLK的工作频率，SRAM访问的WAIT设置具有以下条件。

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[ICLK frequency] (SRAM0):

- 200 MHz ≥ ICLK > 100 MHz = 1 wait
- 100 MHz ≥ ICLK = No-wait

48.3.9 Access Cycle

■ Number of cycles from the CPU

- When the cache is hit, access is one cycle.
- For cache off or non cacheable

Table 48.5 SRAM0 (ECC Area)

Register Setting		Read (cycles)		Write (cycles)	
		Word access	Half-word/Byte access	Word access	Half-word/Byte access
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		2*1	
	SRAM0WTEN = 1	4		2*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		2*1	4
	SRAM0WTEN = 1	4		2*1	4

Note 1. For efficiency of the access, when read access occurs to the same memory after write, memory write by the precedent write command delays it until for the next idle cycle or the next write access. When read continues, it is given priority to read.

Table 48.6 SRAM0 (Parity Area)

Register Setting	Read (cycles)		Write (cycles)	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
SRAM0WTEN = 0	3		2*1	
SRAM0WTEN = 1	4		2*1	

Note 1. For efficiency of the access, when read access occurs to the same memory after write, memory write by the precedent write command delays it until for the next idle cycle or the next write access. When read continues, it is given priority to read.

- For cache on and cacheble (When the cache miss hit)

Table 48.7 SRAM0 (ECC Area)

Register Setting		Read (cycles)		Write (cycles)	
		Word access	Half-word/Byte access	Word access	Half-word/Byte access
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	

Note 1. For efficiency of the access, when read access occurs to the same memory after write, memory write by the precedent write command delays it until for the next idle cycle or the next write access. When read continues, it is given priority to read.

Table 48.8 SRAM0 (Parity Area)

Register Setting	Read (cycles)		Write (cycles)	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
SRAM0WTEN = 0	3		1*1	
SRAM0WTEN = 1	4		1*1	

[ICLK frequency] (SRAM0):

- 200 MHz ≥ ICLK > 100 MHz = 1 wait
- 100 MHz ≥ ICLK = No-wait

48.3.9 访问周期

■CPU的周期数

●当缓存命中时，访问为一个周期。

●对于缓存关闭或不可缓存

Table 48.5 SRAM0 (ECC Area)

寄存器设置		Read (cycles)		Write (cycles)	
		字访问	Half-word/Byte access	字访问	Half-word/Byte access
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		2*1	
	SRAM0WTEN = 1	4		2*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		2*1	4
	SRAM0WTEN = 1	4		2*1	4

注1.为提高访问效率，当写入后对同一内存进行读取访问时，先行写入命令的内存写入会将其延迟到下一个空闲周期或下一次写入访问。继续读取时，优先读取。

Table 48.6 SRAM0 (Parity Area)

寄存器设置	Read (cycles)		Write (cycles)	
	字访问	Half-word/Byte access	字访问	Half-word/Byte access
SRAM0WTEN = 0	3		2*1	
SRAM0WTEN = 1	4		2*1	

注1.为提高访问效率，当写入后对同一内存进行读取访问时，先行写入命令的内存写入会将其延迟到下一个空闲周期或下一次写入访问。继续读取时，优先读取。

●forcacheonandcacheble（当缓存未命中时）

Table 48.7 SRAM0 (ECC Area)

寄存器设置		Read (cycles)		Write (cycles)	
		字访问	Half-word/Byte access	字访问	Half-word/Byte access
ECC Off ECCMOD[1] = 0	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	
ECC On ECCMOD[1] = 1	SRAM0WTEN = 0	3		1*1	
	SRAM0WTEN = 1	4		1*1	

注1.为提高访问效率，当写入后对同一内存进行读取访问时，先行写入命令的内存写入会将其延迟到下一个空闲周期或下一次写入访问。继续读取时，优先读取。

Table 48.8 SRAM0 (Parity Area)

寄存器设置	Read (cycles)		Write (cycles)	
	字访问	Half-word/Byte access	字访问	Half-word/Byte access
SRAM0WTEN = 0	3		1*1	
SRAM0WTEN = 1	4		1*1	

Note 1. For efficiency of the access, when read access occurs to the same memory after write, memory write by the precedent write command delays it until for the next idle cycle or the next write access. When read continues, it is given priority to read.

48.3.10 ECC encode specification

The following table shows ECC encoding specifications. Add the ECC cord (eout [6:0]) formed by the following calculating formula to higher 7 bits (din [38:32]) of write data and write in it at SRAM.

Table 48.9 ECC encode

ECC code	calculation formula
eout[6]	(din[13] ^ din[12] ^ din[11] ^ din[10] ^ din[9] ^ din[8] ^ din[7] ^ din[6] ^ din[5] ^ din[4] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[5]	(din[23] ^ din[22] ^ din[21] ^ din[20] ^ din[19] ^ din[18] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[4]	(din[29] ^ din[28] ^ din[27] ^ din[26] ^ din[25] ^ din[24] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[7] ^ din[6] ^ din[5] ^ din[4])
eout[3]	(din[31] ^ din[30] ^ din[26] ^ din[25] ^ din[24] ^ din[20] ^ din[19] ^ din[18] ^ din[14] ^ din[10] ^ din[9] ^ din[8] ^ din[4] ^ din[0])
eout[2]	(din[31] ^ din[30] ^ din[28] ^ din[27] ^ din[24] ^ din[22] ^ din[21] ^ din[18] ^ din[15] ^ din[12] ^ din[11] ^ din[8] ^ din[5] ^ din[1])
eout[1]	~(din[30] ^ din[29] ^ din[27] ^ din[25] ^ din[23] ^ din[21] ^ din[19] ^ din[16] ^ din[13] ^ din[11] ^ din[9] ^ din[6] ^ din[2] ^ din[0])
eout[0]	~(din[31] ^ din[29] ^ din[28] ^ din[26] ^ din[23] ^ din[22] ^ din[20] ^ din[17] ^ din[13] ^ din[12] ^ din[10] ^ din[7] ^ din[3] ^ din[0])

Note: eout[6:0] = ECC code, din[31:0] = write data

注1.为提高访问效率，当写入后对同一内存进行读取访问时，先行写入命令的内存写入会将其延迟到下一个空闲周期或下一次写入访问。继续读取时，优先读取。

48.3.10 ECC编码规范

下表显示了ECC编码规范。将由以下计算公式形成的ECC线（eout[6:0]）添加到写入数据的高7位（din[38:32]）中，并写入SRAM中。

Table 48.9 ECC encode

ECC code	计算公式
eout[6]	(din[13] ^ din[12] ^ din[11] ^ din[10] ^ din[9] ^ din[8] ^ din[7] ^ din[6] ^ din[5] ^ din[4] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[5]	(din[23] ^ din[22] ^ din[21] ^ din[20] ^ din[19] ^ din[18] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[3] ^ din[2] ^ din[1] ^ din[0])
eout[4]	(din[29] ^ din[28] ^ din[27] ^ din[26] ^ din[25] ^ din[24] ^ din[17] ^ din[16] ^ din[15] ^ din[14] ^ din[7] ^ din[6] ^ din[5] ^ din[4])
eout[3]	(din[31] ^ din[30] ^ din[26] ^ din[25] ^ din[24] ^ din[20] ^ din[19] ^ din[18] ^ din[14] ^ din[10] ^ din[9] ^ din[8] ^ din[4] ^ din[0])
eout[2]	(din[31] ^ din[30] ^ din[28] ^ din[27] ^ din[24] ^ din[22] ^ din[21] ^ din[18] ^ din[15] ^ din[12] ^ din[11] ^ din[8] ^ din[5] ^ din[1])
eout[1]	~(din[30] ^ din[29] ^ din[27] ^ din[25] ^ din[23] ^ din[21] ^ din[19] ^ din[16] ^ din[13] ^ din[11] ^ din[9] ^ din[6] ^ din[2] ^ din[0])
eout[0]	~(din[31] ^ din[29] ^ din[28] ^ din[26] ^ din[23] ^ din[22] ^ din[20] ^ din[17] ^ din[13] ^ din[12] ^ din[10] ^ din[7] ^ din[3] ^ din[0])

Note: eout[6:0]=ECC代码，din[31:0]=写入数据

RA生态工作室

49. Standby SRAM

49.1 Overview

An on-chip SRAM is provided to retain data in Deep Software Standby mode. Table 49.1 lists the Standby SRAM specifications.

Table 49.1 Standby SRAM specifications

Item	Description
SRAM capacity	1 KB
SRAM address	0x2800_0000 to 0x2800_03FF
Access	Standby SRAM clock is the same clock as the PCLKB. See section 49.3.5. Access Cycle for details.
Data retention function	Data can be retained in deep standby mode. See section 49.3.1. Data Retention for details.
parity	Even parity (data: 8 bits, parity: 1 bit)
Module-stop function	Module-stop state can be set to reduce power consumption. See section 49.3.2. Setting for the Module-stop Function for details.
Security	Permits the read and write operations to Standby RAM following TrustZone Filter function. See section 49.3.4. TrustZone Filter function for details.

49.2 Register Descriptions

49.2.1 STBRAMSAR : Standby RAM memory Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	NSBSTBR[3:0]			
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	NSBSTBR[3:0]	Security attributes of each region for Standby RAM 0x0: Region7-0 are all Secure. 0x1: Region7 is Non-secure. Region6-0 are Secure 0x2: Region7-6 are Non-secure. Region5-0 are Secure. 0x3: Region7-5 are Non-secure. Region4-0 are Secure. 0x4: Region7-4 are Non-secure. Region 3-0 are Secure. 0x5: Region7-3 are Non-secure. Region 2-0 are Secure. 0x6: Region7-2 are Non-secure. Region 1-0 are Secure. 0x7: Region7-1 are Non-Secure. Region0 is Secure. Others: Region7-0 are all Non-Secure.	R/W
31:4	—	This bit is read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

49. Standby SRAM

49.1 Overview

提供片上SRAM以在深度软件待机模式下保留数据。表49.1列出了备用SRAM规格。

Table 49.1 备用SRAM规格

Item	Description
SRAM capacity	1 KB
SRAM address	0x2800_0000 to 0x2800_03FF
Access	备用SRAM时钟与PCLKB时钟相同。请参阅第49.3.5节。访问周期了解详情。
数据保留功能	数据可以在深度待机模式下保留。请参阅第49.3.1节。有关详细信息的数据保留。
parity	偶校验（数据：8位，奇偶校验：1位）
Module-stop function	可设置模块停止状态以降低功耗。请参见第49.3.2节。设置为 模块停止功能了解详情。
Security	允许在TrustZone过滤器功能之后对备用RAM进行读取和写入操作。请参见第49.3.4节。TrustZone过滤器功能了解详情。

49.2 注册说明

49.2.1 STBRAMSAR:备用RAM内存安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x014

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	NSBSTBR[3:0]			
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

Bit	Symbol	Function	R/W
3:0	NSBSTBR[3:0]	StandbyRAM各区域的安全属性 0x0：Region7-0都是安全的。0x1：Region7不安全。Region6-0是安全的0x2：Region7-6是非安全的。Region5-0是安全的。0x3：Region7-5不安全。Region4-0是安全的。0x4：Region7-4不安全。区域3-0是安全的。0x5：Region7-3不安全。区域2-0是安全的。0x6：Region7-2不安全。区域1-0是安全的。0x7：Region7-1是非安全的。Region0是安全的。 其他：Region7-0都是非安全的。	R/W
31:4	—	该位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

NSBSTBR[3:0] bit (Security attributes of each region for Standby RAM)

Standby RAM is divided into 8 regions. Each region can be set as Secure or Non-secure state with NSBSTBR[3:0]

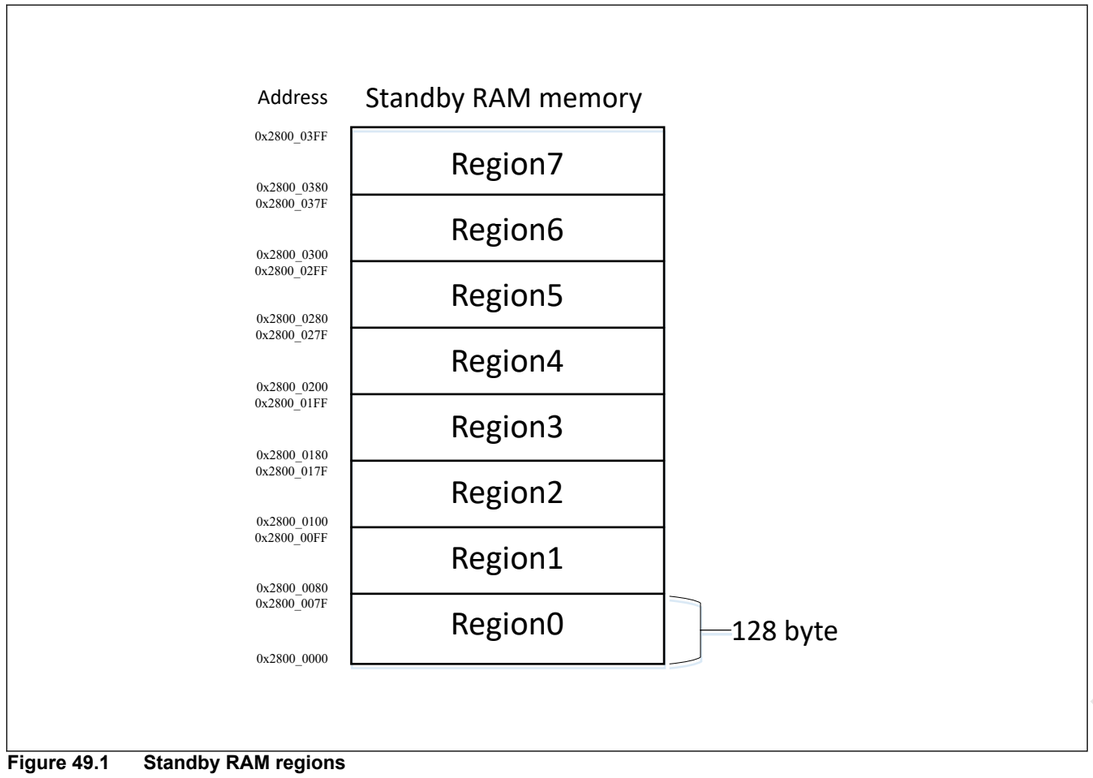

Figure 49.1 Standby RAM regions

49.3 Operation

49.3.1 Data Retention

The power supply to the Standby SRAM in Deep Software Standby mode is enabled by the DPSBYCR.DEEPCUT[1:0] bits. If the DPSBYCR.DEEPCUT[1:0] bits are set to 00b, data in the Standby SRAM is retained in Deep Software Standby mode. See section 10, Low Power Modes, for details on the DPSBYCR.DEEPCUT[1:0] bits.

49.3.2 Setting for the Module-stop Function

Power consumption can be reduced by setting module stop control register A (MSTPCRA) to stop supply of the clock signal to SRAM.

If the Standby SRAM bit in MSTPCRA is set to 1, supply of the clock signal to the Standby SRAM is stopped.

The Standby SRAM is thus placed in the module-stop state by stopping supply of the clock signals. The Standby SRAM operates after a reset.

The Standby SRAM is not accessible if it is in the module-stop state. A transition to the module-stop state should not be made while access to the standby SRAM is in progress.

For details on the MSTPCRA register, see section 10, Low Power Modes.

49.3.3 Parity Calculation Function

The parity calculation Function for Standby SRAM is as same as SRAM without ECC.

NSBSTBR[3:0]位（StandbyRAM每个区域的安全属性）

备用RAM分为8个区域。每个区域都可以通过NSBSTBR[3:0]设置为安全或非安全状态

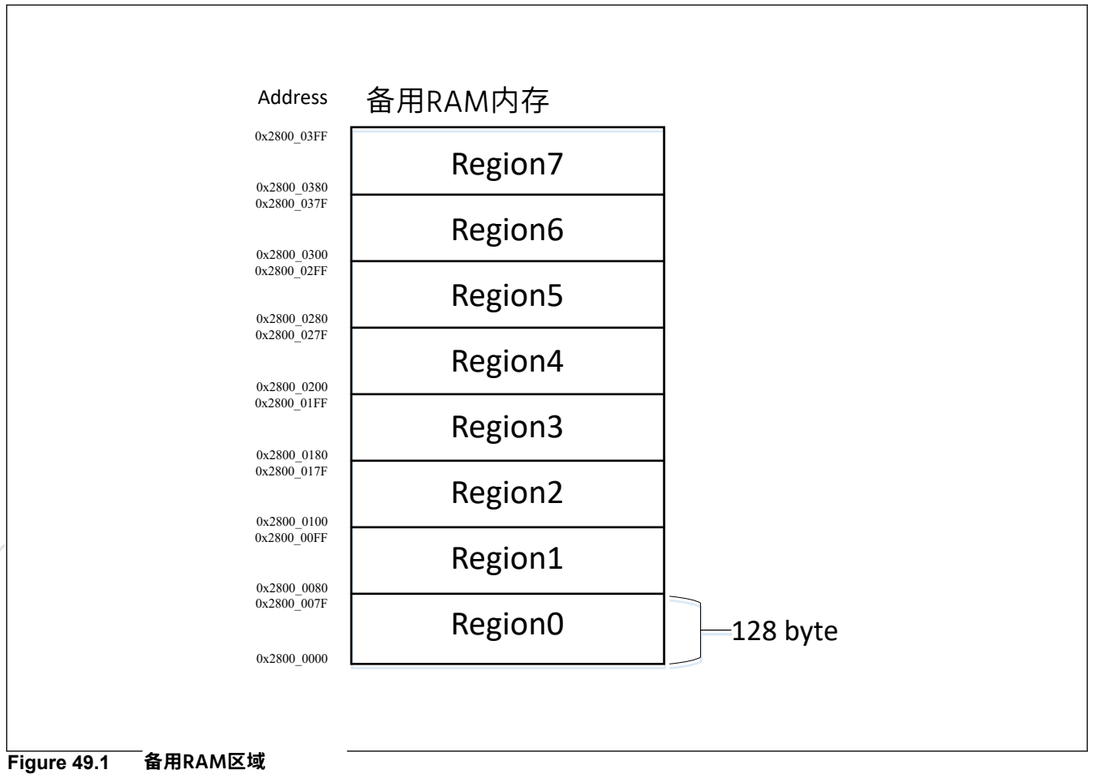

Figure 49.1 备用RAM区域

49.3 Operation

49.3.1 数据保留

深度软件待机模式下的待机SRAM电源由DPSBYCR.DEEPCUT[1:0]位启用。如果DPSBYCR.DEEPCUT[1:0]位设置为00b，则待机SRAM中的数据将保留在深度软件待机模式中。有关DPSBYCR.DEEPCUT[1:0]位的详细信息，请参见第10节，低功耗模式。

49.3.2 模块停止功能的设置

通过设置模块停止控制寄存器A(MSTPCRA)停止向SRAM提供时钟信号，可以降低功耗。

如果MSPCRA中的StandbySRAM位设置为1，则停止向StandbySRAM提供时钟信号。
因此，通过停止提供时钟信号，备用SRAM进入模块停止状态。待机SRAM在复位后运行。

如果处于模块停止状态，则无法访问备用SRAM。在访问备用SRAM的过程中，不应转换到模块停止状态。

有关MSTPCRA寄存器的详细信息，请参见第10节，低功耗模式。

49.3.3 奇偶校验计算功能

StandbySRAM的奇偶校验计算功能与无ECC的SRAM相同。

See section 48.3.5. Parity Calculation Function and section 48.3.7. Interrupt Source.

OAD bit in PARIOAD register is commonly used for SRAM0 (without ECC) / Standby SRAM.

49.3.4 TrustZone Filter function

There is only one type of TrustZone Filter function for Standby SRAM and that is, TrustZone Filter for SRAM memory protection

49.3.4.1 TrustZone Filter for Standby SRAM Memory Protection

Standby SRAM memory can be divided into 8 regions, 128 bytes each with a Security Attribution (SA) to be protected from Non-secure access. When SA indicates that the region in Standby SRAM is secure status, non-secure access can not overwrite them because TrustZone Filter detects finds an error and protects the write access.

Table 49.2 Security Attribution and Access status

SA	Access status	Write access	Read access
Secure	Secure	Permit	Permit
	Non-secure	TrustZone Filter error - Protected	TrustZone Filter error - Read data is 0
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

When TrustZone Filter error for Standby SRAM access occurs, no error notification and no error response occurs.

49.3.5 Access Cycle

Number of cycles from the CPU.

For Standby SRAM, cache always has non-cacheable access.

Table 49.3 Standby SRAM (Parity Area 0x2800_0000 to 0x2800_03FF)

	Read cycle		Write cycle	
	Word access	Half-word/Byte access	Word access	Half-word/Byte access
ICLK ≥ PCLKB	Min.: 2 ICLK + 2 PCLKB Max.: (n + 1) ICLK + 2 PCLKB		Min.: 1 ICLK + 1 PCLKB Max.: n ICLK + 1 PCLKB	

Note: When the frequency ratio of ICLK : PCLKB is n : 1

49.4 Usage Notes

49.4.1 Instruction Fetch from the Standby SRAM Area

When using Standby SRAM to operate a program, initialize the Standby SRAM area so that the CPU can correctly prefetch data. A parity error might occur if the CPU prefetches from an area that is not initialized. Initialize the additional 12-byte area from the end address of the program with the 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

请参阅第48.3.5节。奇偶校验计算函数和第48.3.7节。中断源。

PARIOAD寄存器中的OAD位常用于SRAM0（无ECC）备用SRAM。

49.3.4 TrustZone过滤器功能

StandbySRAM只有一种TrustZoneFilter功能，即用于SRAM内存保护的TrustZoneFilter

49.3.4.1 用于备用SRAM内存保护的TrustZone过滤器

备用SRAM存储器可分为8个区域，每个128字节具有安全属性(SA)
非安全访问。当SA指示StandbySRAM中的区域为安全状态时，非安全访问无法覆盖它们，因为TrustZone Filter检测发现错误并保护写访问。

Table 49.2 安全属性和访问状态

SA	访问状态	写访问	读取权限
Secure	Secure	Permit	Permit
	Non-secure	TrustZone过滤器错 误受保护	TrustZone过滤器错 误读取数据为0
Non-secure	Secure	Permit	Permit
	Non-secure	Permit	Permit

当StandbySRAM访问的TrustZoneFilter错误发生时，不会发生错误通知和错误响应。

49.3.5 访问周期

CPU的周期数。

对于备用SRAM，缓存始终具有不可缓存的访问权限。

Table 49.3 备用SRAM（奇偶校验区0x2800_0000至0x2800_03FF）

	读周期		写周期	
	字访问	Half-word/Byte access	字访问	Half-word/Byte access
ICLK ≥ PCLKB	Min.: 2 ICLK + 2 PCLKB Max.: (n + 1) ICLK + 2 PCLKB		Min.: 1 ICLK + 1 PCLKB Max.: n ICLK + 1 PCLKB	

Note: 当ICLK:PCLKB的频率比为n:1时

49.4 使用说明

49.4.1 从备用SRAM区域取指令

使用StandbySRAM操作程序时，初始化StandbySRAM区域，以便CPU可以正确预取数据。如果CPU从未初始化的区域预取，则可能发生奇偶校验错误。用4字节边界从程序的结束地址初始化额外的12字节区域。瑞萨推荐使用NOP指令进行数据初始化。

50. Flash Memory

This MCU incorporates code flash memory, data flash memory, and option-setting memory. The code flash memory stores instructions and operands, and the data flash memory stores data. For option-setting memory, see section 6, Option-Setting Memory.

50.1 Overview

Table 50.1 lists the specifications of the flash memory, and Figure 50.1 is block diagrams of the flash memory related modules.

The I/O pins used in boot mode, see Table 50.33.

The FCU (flash control unit) controls programming and erasure of the flash memory. The FACI (flash application command interface) controls the FCU according to the specified FACI commands.

Regarding the configuration of the code flash memory, see Figure 50.2 to Figure 50.3, and for the configuration of the data flash memory, see Figure 50.4.

Table 50.1 Specifications of flash memory (1 of 2)

Item	Code flash memory	Data flash memory
Memory capacity	User area: 2 Mbytes max	Data area: 8 Kbytes
Read cycle	See section 50.16.3. Access Cycle	See section 50.16.3. Access Cycle
Value after erasure	0xFF	Undefined
Programming/erasing method	• Programming and erasing the code flash memory and data flash memory, and programming the option-setting memory are handled by the FACI commands specified in the FACI command issuing area (0x407E_0000) (self-programming). • Programming/erasure through transfer by a serial-programmer via a serial interface (serial programming)	
Protection	Protects against erroneous rewriting of the flash memory	
Dual bank function	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area. • Dual mode: the code flash memory is divided into two areas.	Not available
Block swap function	The block swap structure makes a safe update for a part of non-secure application possible in case where programming is suspended.	Not available
Background operations (BGOs)	• The code flash memory can be read while the code flash memory is being programmed or erased.*1 • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area:4/8/16 bytes • Unit of erasure for the data area:64/128/256 bytes
Other functions	Interrupts can be accepted during self-programming. In the initial settings of this MCU, an expansion area of the option-setting memory can be set.	

50. 闪存

该MCU包含代码闪存、数据闪存和选项设置存储器。代码闪存存储指令和操作数，数据闪存存储数据。有关选项设置内存，请参阅第6节，选项设置内存。

50.1 Overview

表50.1列出了闪存的规格，图50.1是闪存相关模块的框图。

引导模式下使用的IO引脚，请参见表50.33。

FCU（闪存控制单元）控制闪存的编程和擦除。FACI（闪存应用命令接口）根据指定的FACI命令控制FCU。

代码闪存的配置见图50.2～图50.3，数据闪存的配置见图50.4。

Table 50.1 闪存规格(1of2)

Item	代码闪存	数据闪存
内存容量	用户区：最大2MB	Data area: 8 Kbytes
读周期	请参阅第50.16.3节。访问周期	请参阅第50.16.3节。访问周期
擦除后的值	0xFF	Undefined
Programming/erasing method	• 编程和擦除代码闪存和数据闪存以及编程选项设置存储器由FACI命令发出区域(0x407E_0000)中指定的FACI命令处理（自编程）。 • 通过串行编程器通过串行接口传输的编程擦除（串行编程）	
Protection	防止闪存的错误重写	
双银行功能	双存储体结构可以在编程暂停的情况下进行安全更新。● 线性模式：代码闪存作为一个区域使用。 • 双模式：代码闪存分为两个区域。	无法使用
区块交换功能	块交换结构可以在编程暂停的情况下对部分非安全应用程序进行安全更新。	无法使用
后台操作(BGO)	• 在对代码闪存进行编程或擦除时，可以读取代码闪存。*1 • 在对代码闪存进行编程或擦除时，可以读取数据闪存。 • 在对数据闪存进行编程或擦除时，可以读取代码闪存。	
编程和擦除单元	• 用户区编程单位：128字节 • 用户区擦除单位：块单位	• 数据区编程单位：4816字节 • 数据区擦除单位：64128256字节
其他功能	自编程期间可以接受中断。 在此MCU的初始设置中，可以设置选项设置存储器的扩展区域。	

Table 50.1 Specifications of flash memory (2 of 2)

Item	Code flash memory	Data flash memory
On-board programming (four types)	Programming/erasure in boot mode (for the SCI interface) ● The asynchronous serial interface (SCI9) is used. ● The transfer rate is adjusted automatically. Programming/erasure in boot mode (for the USB interface) ● USBFS is used. ● Dedicated hardware is not required, so direct connection to a PC is possible. Programming/erasure in On-chip debug mode ● JTAG or SWD interface is used Programming and erasure by self-programming ● This allows code flash memory programming/erasure without resetting the system.	
Unique ID	A 16-byte ID code provided for each MCU	
FACI command	Program : 128 bytes Block erase: 1 block (8 KB or 32 KB) P/E suspend P/E resume Forced Stop Status Clear Configuration set (16 bytes)	Program: 4/8/16 bytes Block Erase: 1 block (64 bytes) Multi Block Erase: 64/128/256 bytes P/E suspend P/E resume Forced Stop Blank Check: 4 bytes to data flash memory capacity Status Clear
Security function	Protects against illicit tampering with or reading out of data in flash memory Startup area select setting protection ● BTFLG and FSUACR registers are protected by the FSPR bit. Permanent block protect setting protection ● Code flash memory is permanently protected from programming/erasure operation by the permanent block protect function. Flash memory protection for TrustZone ● Protection for flash memory area (P/E) ● Protection for flash memory area (read) ● Protection for register ● Protection during FACI command operation. ● Code flash P/E mode entry protection	
Safety function	Software protection ● FACI command protection by FENTRYR register. ● Flash memory is protected by FWEPROR register ● The user area is protected by the block protect setting Error protection ● Error is detected when unintended commands or prohibited settings occur. The FACI command is not accepted after an error detection. Boot area protection ● The start-up area select function allows customer to safely update the boot firmware. The size of the start-up area is 8 KB.	
Interrupt request	● FRDYI (flash sequencer ready (processing end)) : Enabled by FRDYIE bit. ● FIFERR (flash sequencer error) : Enabled by CFAEIE/CMDLKIE/DFAEIE bits	
Address conversion	Start-up area select function is supported in linear mode Dual mode and Linear mode ● Bank swap function is supported in dual mode ● Block swap function is supported in linear mode	

Note 1. Limitations apply to the combinations of the address ranges for programming/erasure process and reading process: see Table 50.35.

Figure 50.1 shows how modules related to flash memory can be configured. The flash sequencer is configured with the FCU and FACI. The FCU executes basic control for rewriting of the flash memory. The FACI receives FACI commands using peripheral bus, and controls FCU operations accordingly.

In response to a reset, the FACI transfers data from the flash memory to the option byte storage registers.

Table 50.1 闪存规格(2of2)

Item	代码闪存	数据闪存
On-board programming (four types)	引导模式下的编程擦除（用于SCI接口）● 使用异步串行接口(SCI9)。 ● 传输速率会自动调整。 引导模式下的编程擦除（针对USB接口）● 使用USBFS。 ● 不需要专用硬件，因此可以直接连接到PC。 片上调试模式下的编程擦除● 使用JTAG或SWD接口 通过自编程进行编程和擦除● 这允许在不重置系统的情况下擦除代码闪存编程。	
唯一身份	为每个MCU提供一个16字节的ID代码	
FACI命令	程序：128字节 块擦除：1个块（8KB或32KB） PE暂停PE恢 复强制停止 状态清除 配置集（16字节）	Program: 4/8/16 bytes Block Erase: 1 block (64 bytes) 多块擦除：64128256字节 PE暂停PE恢 复强制停止 空白检查：4字节到数据闪存容量状态清除
安全功能	防止非法篡改或读取闪存中的数据 启动区选择设置保护● BTFLG和FSUACR寄存器受FSPR位保护。 永久块保护设置保护● 永久块保护功能永久保护代码闪存免受编程擦除操作的影响。TrustZone的闪存保护● 闪存区保护(PE) ● 保护闪存区域（读取） ● 注册保护 ● FACI命令操作期间的保护。 ● CodeflashPE模式进入保护	
安全功能	软件保护● FACI命令由FENTRYR寄存器保护。 ● 闪存受FWEPROR寄存器保护 ● 用户区受块保护 设置保护 错误保护● 发生意外命令或禁止设置时会检测到错误。错误检测后不接受FACI命令。引导区保护● 启动区域选择功能允许客户安全地更新启动固件。启动区的大小为8KB。	
中断请求	● FRDYI（闪存序列器就绪（处理结束））： 由FRDYIE位启用。 ● FIFERR (flash sequencer error) : 由CFAEIECMDLKIEDFAEIE位启用	
地址转换	线性模式下支持启动区域选择功能 双模式和线性模式● 双模式支持银行互换功能 ● 线性模式下支持块交换功能	

注1.限制适用于编程擦除过程和读取过程的地址范围组合：见表50.35。

图50.1显示了如何配置与闪存相关的模块。闪存定序器配置有FCU和FACI。FCU执行闪存重写的基本控制。FACI使用外围总线接收FACI命令，并相应地控制FCU操作。

响应复位，FACI将数据从闪存传输到选项字节存储寄存器。

RA生态工作室

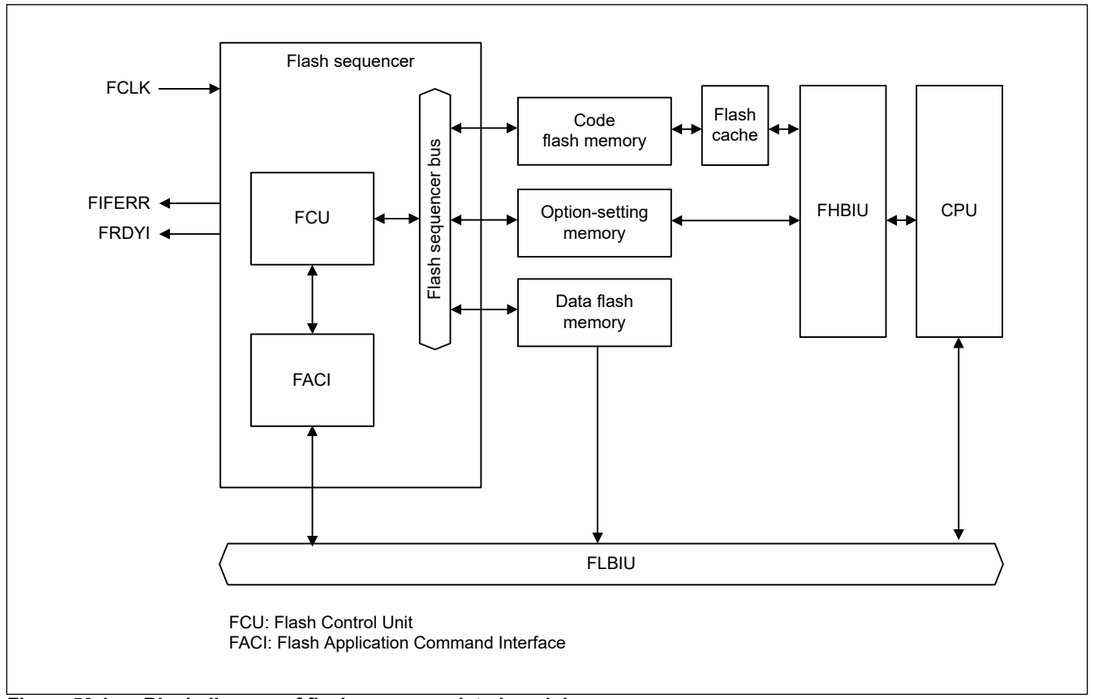

Figure 50.1 Block diagram of flash memory-related modules

50.2 Structure of Memory

Figure 50.2 shows the memory map of code flash memory in linear mode. Figure 50.3 shows the memory map of code flash memory in dual mode. This MCU can use the code flash memory as 2 bank areas by using the dual bank function. This dual-bank structure allows a safe update of a program while a user program is running.

The user area of the code flash memory in this MCU is divided into 8- and 32-Kbyte blocks, which serve as the units of erasure.

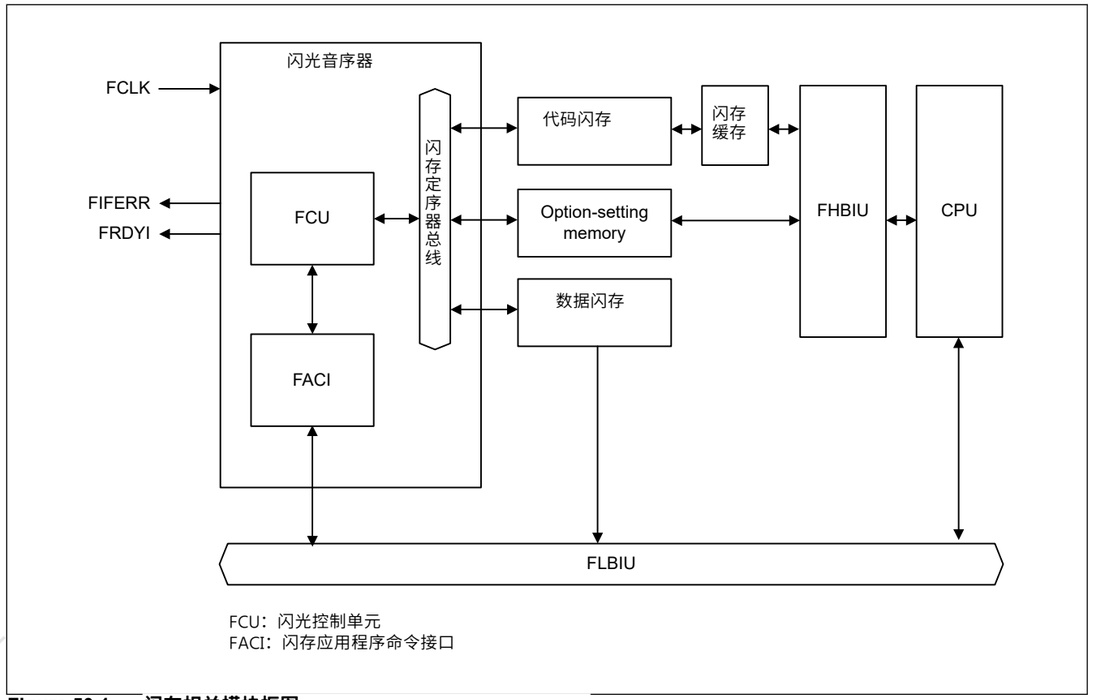

Figure 50.1 闪存相关模块框图

50.2 内存结构

图50.2显示了线性模式下代码闪存的存储器映射。图50.3显示了双模式下代码闪存的存储器映射。该MCU通过使用双存储区功能，可以将代码闪存用作2个存储区。这种双库结构允许在用户程序运行时安全地更新程序。

本MCU中代码闪存的用户区分为8和32KB块，作为擦除单位。

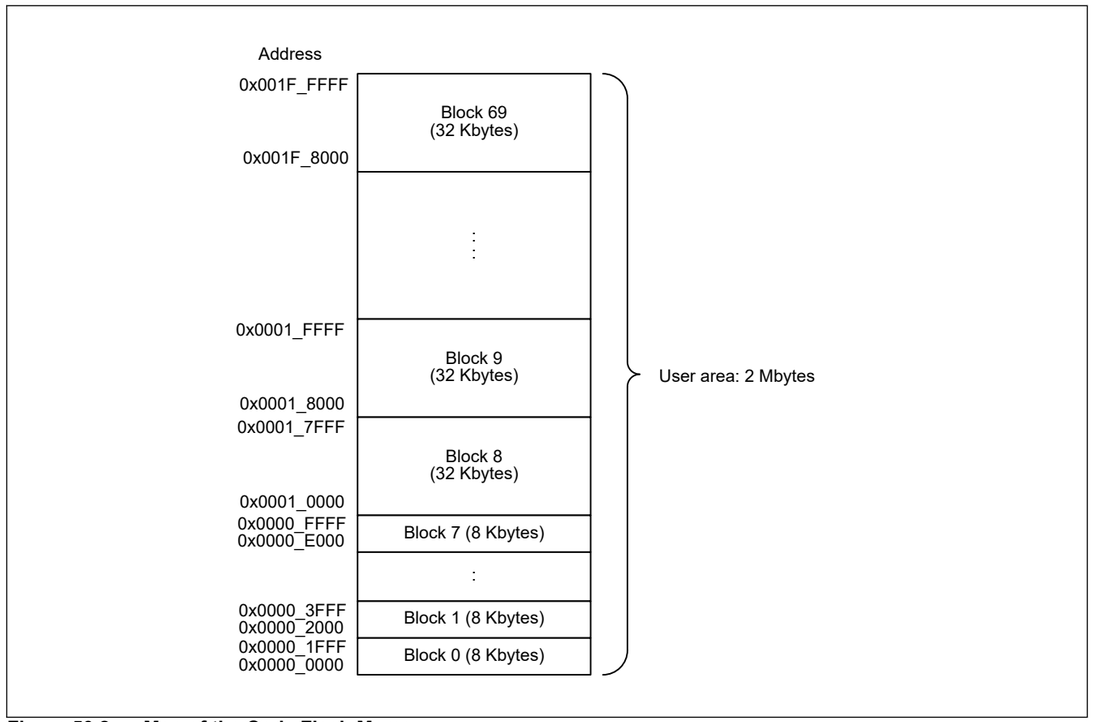

Figure 50.2 Map of the Code Flash Memory

Table 50.2 Read and programming/erasure address by product for the code flash memory

Product	Address	Number of blocks
2 Mbytes product	0x0000_0000h to 0x001F_FFFF	0 to 69
1.5 Mbytes product	0x0000_0000h to 0x0017_FFFF	0 to 53
1 Mbytes product	0x0000_0000h to 0x000F_FFFF	0 to 37

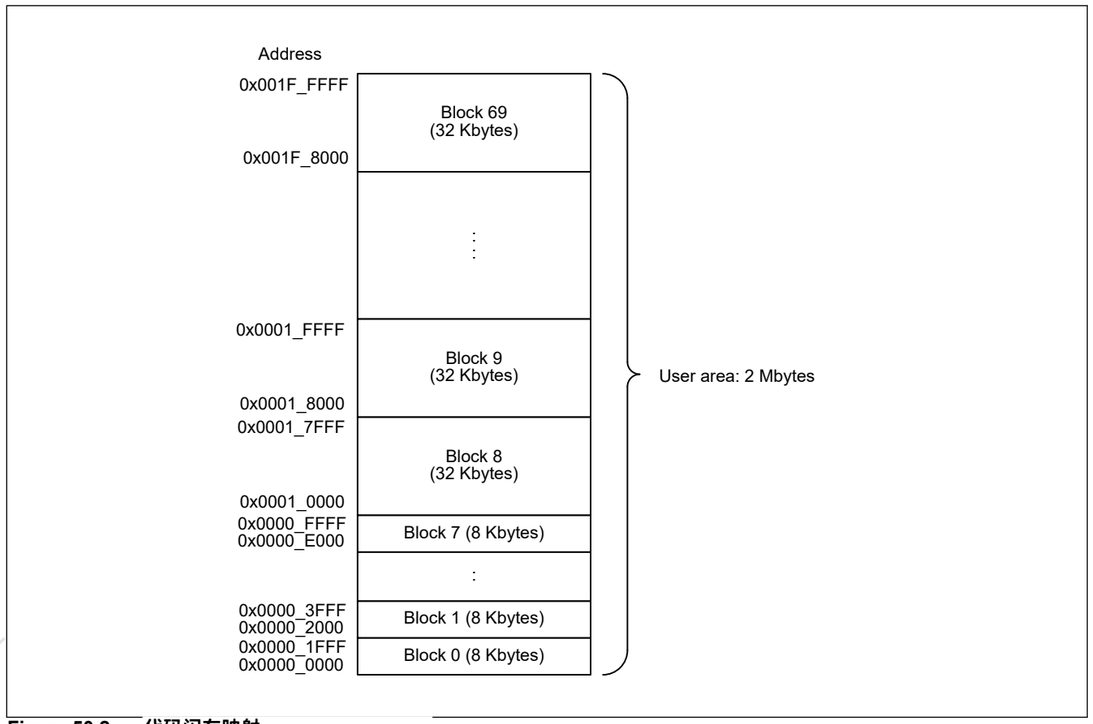

Figure 50.2 代码闪存映射

Table 50.2 按产品读取和编程代码闪存的擦除地址

Product	Address	块数
2 Mbytes product	0x0000_0000h to 0x001F_FFFF	0 to 69
1.5 Mbytes product	0x0000_0000h to 0x0017_FFFF	0 to 53
1 Mbytes product	0x0000_0000h to 0x000F_FFFF	0 to 37

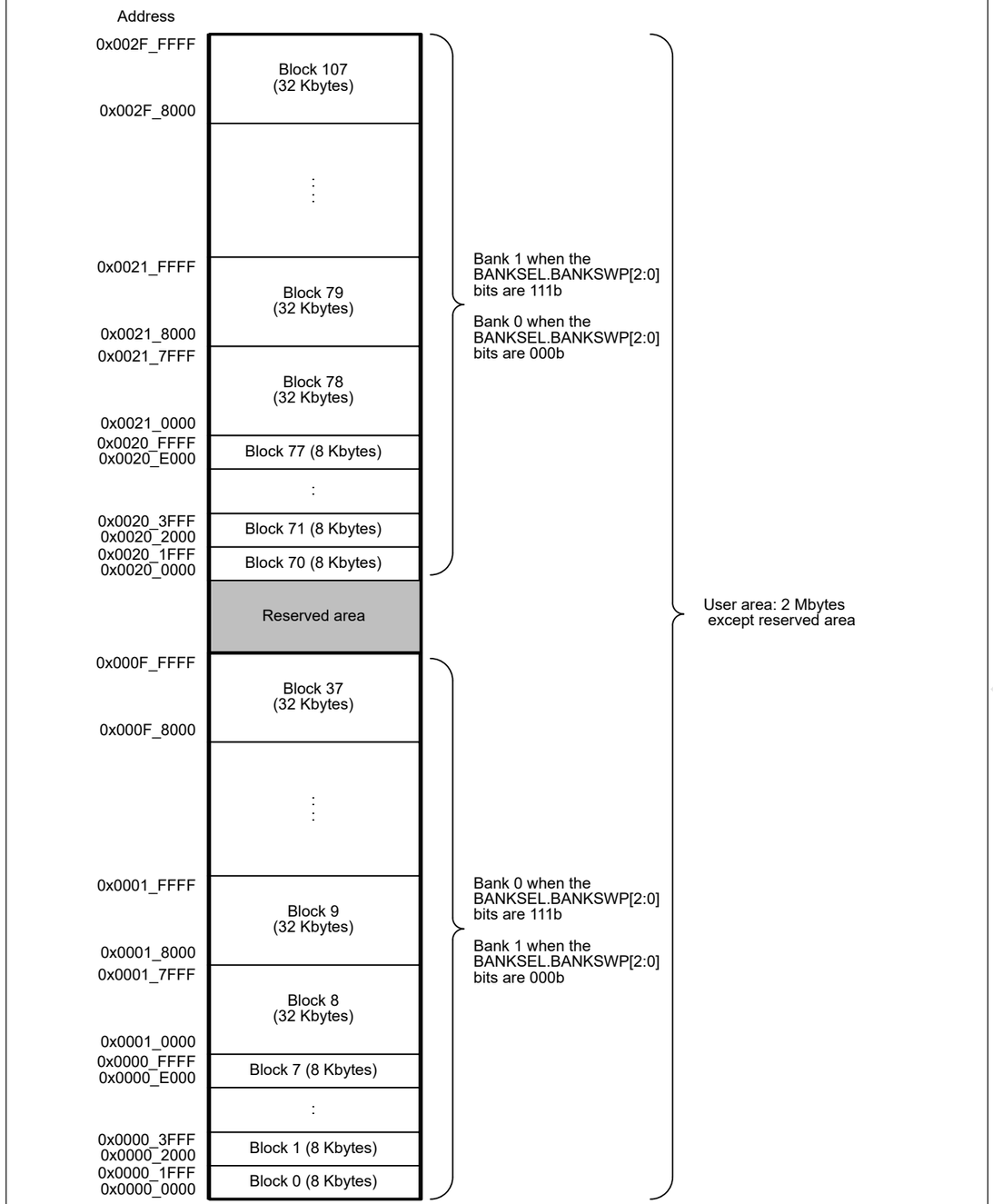

Figure 50.3 Map of the Code Flash Memory in Dual Mode

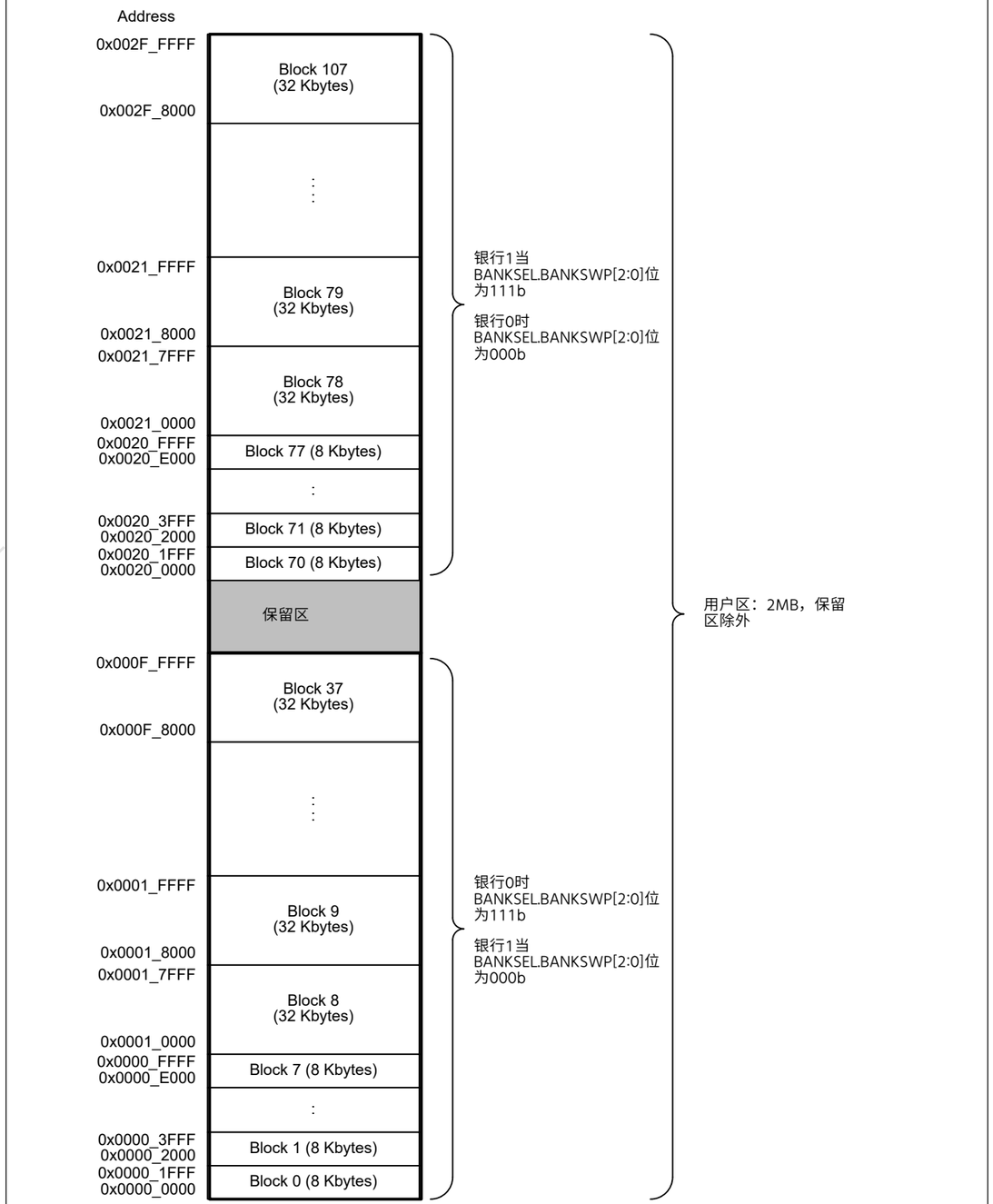

Figure 50.3 双模式下的代码闪存映射

Table 50.3 Read and programming/erasure address by product for the code flash memory

Product	Address	Number of blocks
2 Mbytes product, lower side bank	0x0000_0000 to 0x000F_FFFF	0 to 37
2 Mbytes product, upper side bank	0x0020_0000 to 0x002F_FFFF	70 to 107
1.5 Mbytes product, lower side bank	0x0000_0000 to 0x000B_FFFF	0 to 29
1.5 Mbytes product, upper side bank	0x0020_0000 to 0x002B_FFFF	70 to 99
1 Mbytes product, lower side bank	0x0000_0000 to 0x0007_FFFF	0 to 21
1 Mbytes product, upper side bank	0x0020_0000 to 0x0027_FFFF	70 to 91

The data area of the data flash memory in this MCU is divided into 64-byte blocks, with each being a unit for erasure. Figure 50.4 shows the mapping of the data flash memory.

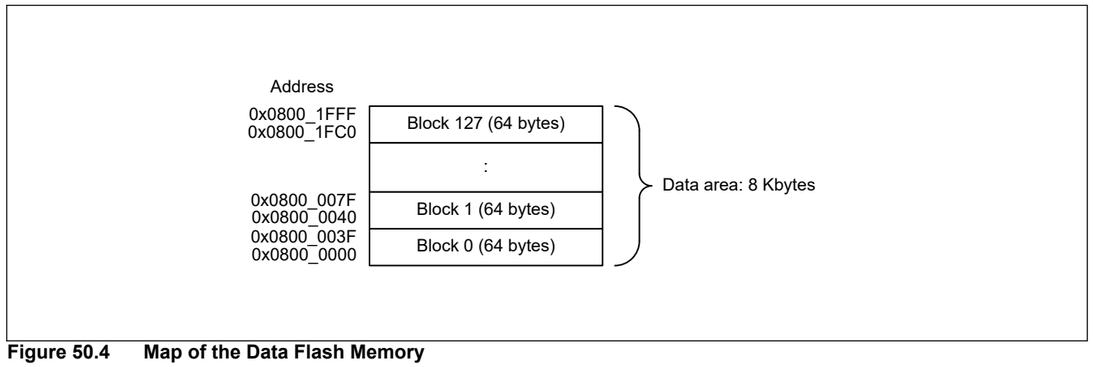

Figure 50.4 Map of the Data Flash Memory

50.3 Address Space

Using the hardware interface with flash memory requires access to all registers of the hardware, which is for issuing FACI commands. Table 50.4 provides information about the hardware interface.

Table 50.4 Information on the hardware interface area

Area	Address	Capacity
Area containing various registers of the hardware	See section 50.4. Register Descriptions.	See section 50.4. Register Descriptions.
FACI command-issuing area	0x407E_0000	4 bytes

For the address information of the flash memory, see Figure 50.2.

50.4 Register Descriptions

50.4.1 FCACHEE : Flash Cache Enable Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCAC HEEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 50.3 按产品读取和编程代码闪存的擦除地址

Product	Address	块数
2MB产品，下侧银行	0x0000_0000 to 0x000F_FFFF	0 to 37
2MB产品，上侧银行	0x0020_0000 to 0x002F_FFFF	70 to 107
1.5MB产品，下侧银行	0x0000_0000 to 0x000B_FFFF	0 to 29
1.5MB产品，上侧银行	0x0020_0000 to 0x002B_FFFF	70 to 99
1MB产品，下侧银行	0x0000_0000 to 0x0007_FFFF	0 to 21
1MB产品，上侧银行	0x0020_0000 to 0x0027_FFFF	70 to 91

本单片机中数据闪存的数据区被划分为64字节块，每个块为一个擦除单元。
图50.4显示了数据闪存的映射。

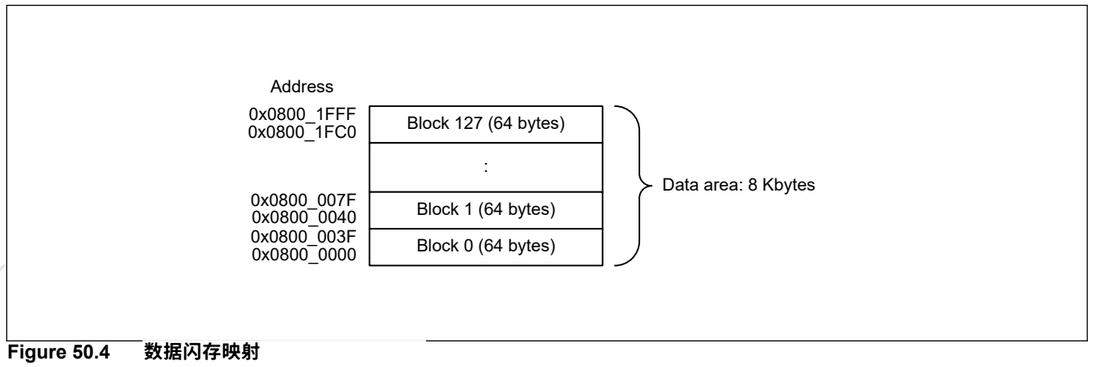

Figure 50.4 数据闪存映射

50.3 地址空间

使用带有闪存的硬件接口需要访问硬件的所有寄存器，用于发出FACI命令。表50.4提供了有关硬件接口的信息。

Table 50.4 硬件接口区信息

Area	Address	Capacity
包含各种硬件寄存器的区域	请参阅第50.4节。注册说明。	请参阅第50.4节。注册说明。
FACI指挥区	0x407E_0000	4 bytes

Flash存储器的地址信息见图50.2。

50.4 注册说明

50.4.1 FCACHEE:闪存缓存启用寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x000

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCAC HEEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEEN	Flash Cache Enable 0: FCACHE is disabled 1: FCACHE is enabled	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is not controlled by any security attribute register.

FCACHEEN bit (Flash Cache Enable)

FCACHEE.FCACHEEN bit enable and disables the function of Flash Cache of FCACHE1, FCACHE2 and FLPF.

FCACHEE.FCACHEEN bit dose not influence for FCACHEIV.FCACHEIV.

When FCACHE is enabled, it works for accesses marked as cacheable.

It is prohibited to disable FCACHE after enabling.

50.4.2 FCACHEIV : Flash Cache Invalidate Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEIV	Flash Cache Invalidate 0: Read: Do not invalidate. Write: The setting is ignored. 1: Invalidate FCACHE is invalidated.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

This register is not controlled by any security attribute register.

FCACHEIV bit (Flash Cache Invalidate)

When 1 is written to FCACHEIV.FCACHEIV bit, the Flash cache data of FCACHE1, FCACHE2 and FLPF is invalidated.

Invalidate FCACHE with keeping FCACHE enabled after programming or erasing the code flash or the option setting memory.

50.4.3 FLWT : Flash Wait Cycle Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x01C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLWT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	FLWT[2:0]	Flash Wait Cycle 0 0 0: 0 wait (ICLK ≤ 50 MHz) 0 0 1: 1 wait (50 MHz < ICLK ≤ 100 MHz)	R/W

Bit	Symbol	Function	R/W
0	FCACHEEN	闪存缓存启用 0：禁用FCACHE1：启用FCACHE	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器不受任何安全属性寄存器的控制。

FCACHEEN位（闪存使能）

FCACHEE.FCACHEEN位启用和禁用FCACHE1、FCACHE2和FLPF的FlashCache功能。

FCACHEE.FCACHEEN位对FCACHEIV.FCACHEIV没有影响。

启用FCACHE后，它适用于标记为可缓存的访问。

禁止启用后禁用FCACHE。

50.4.2 FCACHEIV:闪存缓存无效寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x004

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FCACHEIV	闪存缓存失效 0：读取：不无效。 写入：忽略该设置。 1: Invalidate FCACHE无效。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

该寄存器不受任何安全属性寄存器的控制。

FCACHEIV位（FlashCache无效）

当FCACHEIV.FCACHEIV位写入1时，FCACHE1、FCACHE2和FLPF的Flash缓存数据无效。

在编程或擦除代码闪存或选项设置存储器后保持FCACHE使能，使FCACHE无效。

50.4.3 FLWT：闪存等待周期寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x01C

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	FLWT[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	FLWT[2:0]	闪存等待周期 0 0 0: 0 wait (ICLK ≤ 50 MHz) 0 0 1: 1 wait (50 MHz < ICLK ≤ 100 MHz)	R/W

Bit	Symbol	Function	R/W
		0 1 0: 2 wait (100 MHz < ICLK ≤ 150 MHz) 0 1 1: 3 wait (ICLK > 150 MHz) Others: Setting prohibited	
7:3	—	These bits are read as 0. The write value should be 0.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

FLWT[2:0] bits (Flash Wait Cycle)

The Flash Wait Cycle Register (FLWT) sets the access wait count for the flash memory.

For faster clock frequencies, set FLWT.FLWT before changing the clock frequency. For slower clock frequencies, set FLWT.FLWT after changing the clock frequency.

For information on the frequency setting, see section 8, Clock Generation Circuit.

50.4.4 FSAR : Flash Security Attribution Register

Base address: FCACHE = 0x4001_C100

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FCKMHZSA	—	—	—	—	—	—	—	FLWTSA
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	FLWTSA	FLWT Security Attribution Target register : FLWT 0: Secure 1: Non-Secure	R/W
7:1	—	These bits are read as 1. The write value should be 1.	R/W
8	FCKMHZSA	FCKMHZ Security Attribution Target register : FCKMHZ 0: Secure 1: Non-Secure	R/W
15:9	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

Write access is invalid when PRCR.PRC4 bit is 0. See section 12, Register Write Protection.

FLWTSA bit (FLWT Security Attribution)

This bit sets the security attribute of FLWT.

FCKMHZSA bit (FCKMHZ Security Attribution)

This bit sets the security attribute of FCKMHZ.

Bit	Symbol	Function	R/W
		0 1 0: 2 wait (100 MHz < ICLK ≤ 150 MHz) 0 1 1: 3 wait (ICLK > 150 MHz) 其他：禁止设置	
7:3	—	这些位被读取为0。写入值应为0。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

FLWT[2:0]位（闪存等待周期）

闪存等待周期寄存器(FLWT)设置闪存的访问等待计数。

要获得更快的时钟频率，请在更改时钟频率之前设置FLWT.FLWT。对于较慢的时钟频率，设置改变时钟频率后的FLWT.FLWT。

有关频率设置的信息，请参见第8节，时钟生成电路。

50.4.4 FSAR:Flash安全属性寄存器

Base address: FCACHE = 0x4001_C100

Offset address: 0x040

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FCKMHZSA	—	—	—	—	—	—	—	FLWTSA
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	FLWTSA	FLWT安全归因 目标寄存器：FLWT 0: Secure 1: Non-Secure	R/W
7:1	—	这些位被读取为1。写入值应为1。	R/W
8	FCKMHZSA	FCKMHZ安全归属地 目标寄存器：FCKMHZ 0: Secure 1: Non-Secure	R/W
15:9	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

当PRCR.PRC4位为0时，写访问无效。参见第12节，寄存器写保护。

FLWTSA位（FLWT安全属性）

该位设置FLWT的安全属性。

FCKMHZSA位（FCKMHZ安全属性）

该位设置FCKMHZ的安全属性。

50.4.5 UIDRn : Unique ID Registers n (n = 0 to 3)

Address: 0x0100_8190 + n × 4

Bit position:	31															0
Bit field:	UID															
Value after reset:	Unique value for each chip															

Bit	Symbol	Function	R/W
31:0	UID	Unique ID	R

The UIDRn is a read-only register that stores a 16-byte ID code (unique ID) for identifying the individual MCU. The UIDRn register should be read in 32-bit units. When reading by the signature request command of the serial programming interface, the data is read in order from the data with the large address. That is, the data in 0x0100_819F is read first, and in 0x0100_8190 is read last.

50.4.6 PNRn : Part Numbering Register n (n = 0 to 3)

Address: 0x0100_80F0 + n × 4

Bit position:	31															0
Bit field:	PNR															
Value after reset:	Unique value for each chip															

Bit	Symbol	Function	R/W
31:0	PNR	Part Number	R

The PNRn is a read-only register that stores a 16-byte part numbering. The PNRn register should be read in 32-bit units. Each byte corresponds to the ASCII code representation of the product part number as detailed in Table 1.13 Product list. The first character ("R", 0x52 in ASCII code) of the part number is stored in the byte with the smallest address (0x0100_80F0). When reading by the signature request command of the serial programming interface, the data is read in order from the data with the small address. That is, the data in 0x0100_80F0 is read first, and in 0x0100_80FF is read last.

50.4.7 MCUVER : MCU Version Register

Address: 0x0100_81B0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MCUVE							
Value after reset:	Value depend on the chip							

Bit	Symbol	Function	R/W
7:0	MCUVE	MCU Version	R

The MCUVER is a read-only register that stores a MCU version. The MCUVER register should be read in 8-bit units.

50.4.5 UIDRn：唯一ID寄存器n（n=0到3）

Address: 0x0100_8190 + n × 4

Bit position:	31															0
Bit field:	UID															
重置后的值：	每个芯片的独特价值															

Bit	Symbol	Function	R/W
31:0	UID	唯一身份	R

UIDRn是一个只读寄存器，它存储一个16字节的ID代码（唯一ID），用于识别单个MCU。这
UIDRn寄存器应以32位为单位读取。通过串口编程接口的签名请求命令读取时，从地址大的数据开始依次读取。
即先读取0x0100_819F中的数据，最后读取0x0100_8190中的数据。

50.4.6 PNRn：零件编号寄存器n（n=0到3）

Address: 0x0100_80F0 + n × 4

Bit position:	31															0
Bit field:	PNR															
重置后的值：	每个芯片的独特价值															

Bit	Symbol	Function	R/W
31:0	PNR	零件号	R

PNRn是一个只读寄存器，存储一个16字节的零件编号。PNRn寄存器应以32位为单位读取。每个字节对应于表1.13产品列表中详细说明的产品部件号的ASCII代码表示。部件号的第一个字符（“R”，ASCII码中的0x52）存储在地址最小的字节中（0x0100_80F0）。通过串行编程接口的签名请求命令读取时，从地址小的数据开始依次读取。即先读取0x0100_80F0中的数据，最后读取0x0100_80FF中的数据。

50.4.7 MCUVER:MCU版本寄存器

Address: 0x0100_81B0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	MCUVE							
重置后的值：	价值取决于芯片							

Bit	Symbol	Function	R/W
7:0	MCUVE	MCU Version	R

MCUVER是一个只读寄存器，用于存储MCU版本。MCUVER寄存器应以8位为单位读取。

50.4.8 FWEPROR : Flash P/E Protect Register

Base address: SYSC = 0x4001_E000

Offset address: 0x416

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	FLWE[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	FLWE[1:0]	Flash Programming and Erasure 0 0: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 0 1: Permits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 1 0: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing. 1 1: Prohibits Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing.	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W

It is possible that Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command processing are prohibited by software.

The FWEPROR register is initialized by a reset from the following:

- All reset source
- Transition to Deep Software Standby mode
- Transition to Software Standby mode.

FLWE[1:0] bits (Flash Programming and Erasure)

The FLWE[1:0] bits are used to set the flash P/E protection. The value after reset is 10b.

If these bits are set to other than 01b that does not allow programming and erasure of the flash memory, the following commands cannot be executed. Issuing any of the following commands leads to setting of the FLWEERR bit in the FSTATR register to 1.

Program / Block Erase / Multi Block Erase / Blank Check / Configuration set command

50.4.9 FASTAT : Flash Access Status Register

Base address: FACI = 0x407F_E000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAE	—	—	CMDLK	DFAE	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	DFAE	Data Flash Memory Access Violation Flag 0: No data flash memory access violation has occurred 1: A data flash memory access violation has occurred.	R/W*1
4	CMDLK	Command Lock Flag 0: The flash sequencer is not in the command-locked state 1: The flash sequencer is in the command-locked state.	R

50.4.8 FWEPROR:FlashPE保护寄存器

Base address: SYSC = 0x4001_E000

Offset address: 0x416

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	FLWE[1:0]	
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	Function	R/W
1:0	FLWE[1:0]	闪存编程和擦除 00：禁止编程、块擦除、多块擦除、空白检查和配置设置命令处理。 01：允许编程、块擦除、多块擦除、空白检查和配置设置命令处理。 10：禁止编程、块擦除、多块擦除、空白检查和配置设置命令处理。 11：禁止Program、BlockErase、MultiBlockErase、BlankCheck和Configurationset命令处理。	R/W
7:2	—	这些位被读取为0。写入值应为0。	R/W

程序、块擦除、多块擦除、空白检查和配置设置命令处理可能被软件禁止。

FWEPROR寄存器通过以下复位进行初始化：

●所有复位源

●转换到深度软件待机模式

●转换到软件待机模式。

FLWE[1:0]位（闪存编程和擦除）

FLWE[1:0]位用于设置flashPE保护。复位后的值为10b。

如果这些位设置为不允许对闪存进行编程和擦除的01b以外，则无法执行以下命令。发出以下任何命令都会将FSTATR寄存器中的FLWEERR位设置为1。

ProgramBlockEraseMultiBlockEraseBlankCheckConfigurationset命令

50.4.9 FASTAT：闪存访问状态寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x10

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAE	—	—	CMDLK	DFAE	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	DFAE	数据闪存访问违规标志 0：未发生数据闪存访问违规1：发生数据闪存访问违规。	R/W*1
4	CMDLK	命令锁定标志 0：flash定序器不处于命令锁定状态1：flash定序器处于命令锁定状态。	R

Bit	Symbol	Function	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CFAE	Code Flash Memory Access Violation Flag 0: No code flash memory access violation has occurred 1: A code flash memory access violation has occurred.	R/W*1

Note 1. Only 0 can be written to clear the flag after 1 is read.

The FASTAT register indicates whether a code flash or data flash memory access violation has occurred. If any of the CFAE, CMDLK, and DFAE bits is set to 1, the flash sequencer enters the command-locked state (see section 50.11.2. Error Protection). To release it from the command-locked state, issue a status clear command or Forced Stop command to the flash sequencer.

DFAE bit (Data Flash Memory Access Violation Flag)

The DFAE bit indicates whether a data flash memory access violation occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting conditions]

FACI commands issued in the data flash P/E mode are as follows:

- The setting of the FSADDR or FEADDR register is the reserved portion of the data area
- FACI commands of non-secure access are issued while the setting of the FSADDR or FEADDR register is the secure region address.

[Clearing conditions]

- When this bit is written as 0 after it is set to 1
- When the flash sequencer starts to process the Status Clear or Forced Stop command.

CMDLK bit (Command Lock Flag)

The CMDLK bit indicates that the flash sequencer is in the command-locked state.

[Setting conditions]

- The flash sequencer detects an error and enters the command-locked state.

[Clearing conditions]

- When the flash sequencer starts to process the Status Clear or Forced Stop command.

CFAE bit (Code Flash Memory Access Violation Flag)

The CFAE bit indicates whether a code flash memory access violation has occurred. When this bit is set to 1, the ILGLERR bit in the FSTATR register is set to 1, placing the flash sequencer in the command-locked state.

[Setting conditions]

FACI commands issued in the code flash P/E mode are as follows:

- The setting of the FSADDR register is the reserved portion of the user area
- The Configuration set command is issued while the setting of the FSADDR register is from 0x0000A100 to 0x0000A2F0 in self-programming mode
- FACI commands of non-secure access are issued while the setting of the FSADDR register is the secure region address.

[Clearing conditions]

- When this bit is written as 0 after it is set to 1
- When the flash sequencer starts to process the Status Clear or Forced Stop command.

Bit	Symbol	Function	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	CFAE	代码闪存访问违规标志 0：未发生代码闪存访问违规1：发生代码闪存访问违规 。	R/W*1

注1.读取1后，只能写入0以清除标志。

FASTAT寄存器指示是否发生了代码闪存或数据闪存访问违规。如果任何一个CFAE、CMDLK和DFAE位设置为1，闪存定序器进入命令锁定状态（请参阅第50.11.2节。错误保护）。要将其从命令锁定状态释放，请向闪存定序器发出状态清除命令或强制停止命令。

DFAE位（数据闪存访问违规标志）

DFAE位指示是否发生数据闪存访问违规。当该位设置为1时，FSTATR寄存器中的ILGLERR位设置为1，将闪存定序器置于命令锁定状态。

[Setting conditions]

数据闪存PE模式下发出的FACI命令如下：

●FSADDR或FEADDR寄存器的设置是数据区的保留部分

●FSADDR或FEADDR寄存器的设置是安全区域地址时发出非安全访问的FACI命令。

[Clearing conditions]

●该位设置为1后写入0时

●当flashsequencer开始处理StatusClear或ForcedStop命令时。

CMDLK位（命令锁定标志）

CMDLK位指示闪存定序器处于命令锁定状态。

[Setting conditions]

●闪存定序器检测到错误并进入命令锁定状态。

[Clearing conditions]

●当flashsequencer开始处理StatusClear或ForcedStop命令时。

CFAE位（代码闪存访问违规标志）

CFAE位指示是否发生代码闪存访问违规。当该位设置为1时，FSTATR寄存器中的ILGLERR位设置为1，将闪存定序器置于命令锁定状态。

[Setting conditions]

CodeflashPE模式下发出的FACI命令如下：

●FSADDR寄存器的设置是用户区的保留部分

●自编程模式下FSADDR寄存器的设置从0x0000A100到0x0000A2F0时发出配置设置命令

●FSADDR寄存器的设置是安全区域地址时发出非安全访问的FACI命令。

[Clearing conditions]

●该位设置为1后写入0时

●当flashsequencer开始处理StatusClear或ForcedStop命令时。

50.4.10 FAEINT : Flash Access Error Interrupt Enable Register

Base address: FACI = 0x407F_E000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
Value after reset:	1	0	0	1	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	These bits are read as 0. The write value should be 0.	R/W
3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.DFAE is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.DFAE is set to 1.	R/W
4	CMDLKIE	Command Lock Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.CMDLK is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CMDLK is set to 1.	R/W
6:5	—	These bits are read as 0. The write value should be 0.	R/W
7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable 0: Generation of an FIFERR interrupt request is disabled when FASTAT.CFAE is set to 1 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CFAE is set to 1.	R/W

The FAEINT register enables or disables generation of a flash access error (FIFERR) interrupt request.

DFAEIE bit (Data Flash Memory Access Violation Interrupt Enable)

The DFAEIE bit enables or disables generation of an FIFERR interrupt request when a data flash memory access violation occurs, setting the DFAE bit in the FASTAT register to 1.

CMDLKIE bit (Command Lock Interrupt Enable)

The CMDLKIE bit enables or disables generation of an FIFERR interrupt request when the flash sequencer enters the command-locked state, setting the CMDLK bit in the FASTAT register to 1.

CFAEIE bit (Code Flash Memory Access Violation Interrupt Enable)

The CFAEIE bit enables or disables generation of an FIFERR interrupt request when a code flash memory access violation occur, setting the CFAE bit in the FASTAT register to 1.

50.4.11 FRDYIE : Flash Ready Interrupt Enable Register

Base address: FACI = 0x407F_E000

Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRDYIE
Value after reset:	0	0	0	0	0	0	0	0

50.4.10 FAEINT：闪存访问错误中断使能寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x14

Bit position:	7	6	5	4	3	2	1	0
Bit field:	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
重置后的值：	1	0	0	1	1	0	0	0

Bit	Symbol	Function	R/W
2:0	—	这些位被读取为0。写入值应为0。	R/W
3	DFAEIE	数据闪存访问冲突中断使能 0：当FASTAT.DFAE设置为1时，禁止生成FIFERR中断请求 1：当FASTAT.DFAE设置为1时，使能FIFERR中断请求的生成。	R/W
4	CMDLKIE	命令锁定中断使能 0：当FASTAT.CMDLK设置为1时，禁止生成FIFERR中断请求 1：当FASTAT.CMDLK设置为1时，使能FIFERR中断请求的生成。	R/W
6:5	—	这些位被读取为0。写入值应为0。	R/W
7	CFAEIE	代码闪存访问冲突中断启用 0：当FASTAT.CFAE设置为1时，禁止生成FIFERR中断请求 1：当FASTAT.CFAE设置为1时，使能FIFERR中断请求的生成。	R/W

FAEINT寄存器启用或禁用闪存访问错误(FIFERR)中断请求的生成。

DFAEIE位（数据闪存访问冲突中断允许）

当发生数据闪存访问违规时，DFAEIE位启用或禁用FIFERR中断请求的生成，将FASTAT寄存器中的DFAE位设置为1。

CMDLKIE位（命令锁定中断使能）

当闪存定序器进入命令锁定状态时，CMDLKIE位启用或禁用FIFERR中断请求的生成，将FASTAT寄存器中的CMDLK位设置为1。

CFAEIE位（代码闪存访问冲突中断允许）

当发生代码闪存访问违规时，CFAEIE位启用或禁用FIFERR中断请求的生成，将FASTAT寄存器中的CFAE位设置为1。

50.4.11 FRDYIE:闪存就绪中断使能寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x18

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	FRDYIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FRDYIE	Flash Ready Interrupt Enable 0: Generation of an FRDY interrupt request is disabled 1: Generation of an FRDY interrupt request is enabled.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

The FRDYIE register enables or disables generation of a flash ready (FRDY) interrupt.

FRDYIE bit (Flash Ready Interrupt Enable)

The FRDYIE bit enables or disables generation of an FRDY interrupt request when the FRDY bit in the FSTATR register is changed from 0 to 1 on completion of processing by the flash sequencer of the Program, Block Erase, Multi Block Erase, Blank Check, and Configuration set command.

50.4.12 FSADDR : FACI Command Start Address Register

Base address: FACI = 0x407F_E000

Offset address: 0x30

Bit position:	31																												0
Bit field:	FSADDR[31:0]																												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FSADDR[31:0]	Start Address for FACI Command Processing	R/W*1

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0. Note that b0 and b1 are read-only.

Table 50.5 FACI command addres boundary

Command	Address Boundary
Program (code flash memory)	128-byte
Program (data flash memory)	4, 8, 16 -byte
Block Erase (code flash memory)	8-KB or 32-KB
Block Erase (data flash memory)	64-byte
Multi Block Erase (data flash memory)	64-byte
Blank Check (data flash memory)	4-byte
Configuration set	16-byte

The FSADDR register specifies the address where the target area for command processing starts when the FACI command for Program, Block Erase, Multi Block Erase, Blank Check, or Configuration set is issued.

The FSADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FSADDR[31:0] bits (Start Address for FACI Command Processing)

The FSADDR[31:0] bits specify the start address for FACI command processing. Bits [31:24] are ignored in FACI command processing for the code flash memory. Bits [31:17] are ignored in FACI command processing for the data flash memory. Bits associated with the address bits of lower order than the address boundary listed in Table 50.5 are also ignored.

For information on the addresses of the code flash memory and the data flash memory, see section 50.2. Structure of Memory.

For information on the addresses of the configuration setting, see section 50.9.3.15. Configuration Set Command.

Bit	Symbol	Function	R/W
0	FRDYIE	闪存就绪中断使能 0：禁止产生FRDY中断请求1：允许产生FRDY中断请求 。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

FRDYIE寄存器启用或禁用闪存就绪(FRDY)中断的生成。

FRDYIE位（闪存就绪中断使能）

当FSTATR寄存器中的FRDY位在程序、块擦除、多块擦除、空白检查和配置的闪存序列器的处理完成时从0变为1时，FRDYIE位启用或禁用FRDY中断请求的产生设置命令。

50.4.12 FSADDR:FACI命令起始地址寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x30

Bit position:	31																												0
Bit field:	FSADDR[31:0]																												
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FSADDR[31:0]	FACI命令处理的起始地址	R/W*1

注1.当FSTATR寄存器中的FRDY位为1时可以写入这些位。当FRDY位为0时忽略写入这些位。
请注意，b0和b1是只读的。

Table 50.5 FACI命令地址边界

Command	地址边界
程序（代码闪存）	128-byte
程序（数据闪存）	4, 8, 16 -byte
块擦除（代码闪存）	8-KB or 32-KB
块擦除（数据闪存）	64-byte
多块擦除（数据闪存）	64-byte
空白检查（数据闪存）	4-byte
配置集	16-byte

FSADDR寄存器指定在发出用于编程、块擦除、多块擦除、空白检查或配置集的FACI命令时命令处理的目标区域开始的地址。

FSADDR值在FSUINITR寄存器中的SUINIT位设置为1时被初始化。它也通过复位被初始化。

FSADDR[31:0]位（FACI命令处理的起始地址）

FSADDR[31:0]位指定FACI命令处理的起始地址。在代码闪存的FACI命令处理中忽略位[31:24]。在数据闪存的FACI命令处理中忽略位[31:17]。与低于表50.5中列出的地址边界的地址位相关的位也被忽略。

有关代码闪存和数据闪存地址的信息，请参见第50.2节。结构
Memory.

有关配置设置地址的信息，请参阅第50.9.3.15节。配置集命令。

50.4.13 FEADDR : FACI Command End Address Register

Base address: FACI = 0x407F_E000

Offset address: 0x34

Bit position:	31																													0
Bit field:	FEADDR[31:0]																													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FEADDR[31:0]	End Address for FACI Command Processing	R/W*1

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0. Note that bit [0] and bit [1] are read-only.

The FEADDR register specifies the end address of the target area for Multi Block Erase and Blank Check command processing. When incremental mode is selected as the addressing mode for Blank Checking (when FBCCNT.BCDIR = 0), the address specified in the FSADDR register should be equal to or smaller than the address in the FEADDR register. Conversely, the address in the FSADDR register should be equal to or larger than the address in the FEADDR register when decremental mode is selected as the addressing mode for Blank Check (i.e. when FBCCNT.BCDIR = 1). If the BCDIR, FSADDR, and FEADDR bit settings are inconsistent with the specified rules, the flash sequencer enters the command-locked state (see section 50.11.2. Error Protection).

The FEADDR value is initialized when the SUINIT bit in the FSUINITR register is set to 1. It is also initialized by a reset.

FEADDR[31:0] bits (End Address for FACI Command Processing)

The FEADDR[31:0] bits specify the end address for Multi Block Erase and Blank Check command processing. In command processing, bits 31 to 17 and any bits that do not reach the address boundaries listed in the section 50.4.12. FSADDR : FACI Command Start Address Register are ignored.

For information on the addresses of the flash memory, see section 50.2. Structure of Memory.

50.4.14 FMEPROT : Flash P/E Mode Entry Protection Register

Base address: FACI = 0x407F_E000

Offset address: 0x44

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	CEPROT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CEPROT	Code Flash P/E Mode Entry Protection 0: FENTRYC bit is not protected 1: FENTRYC bit is protected.	R/W*1 *2 *4
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	R/W*3

Note 1. Writing to this bit is only possible when the FRDY bit in the FSTATR register is 1. Writing to this bit while the FRDY bit = 0 is ignored.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY bits is D9h.
Note 3. Written values are not retained by these bits (always read as 0x00).
Note 4. Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, but TrustZone access error is note generated.

CEPROT bit (Code Flash P/E Mode Entry Protection)

The CEPROT bit specifies the protection setting of the FRNTRYC bit in the FENTRYR register.

50.4.13 FEADDR:FACI命令结束地址寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x34

Bit position:	31																													0
Bit field:	FEADDR[31:0]																													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	FEADDR[31:0]	FACI命令处理的结束地址	R/W*1

注1.当FSTATR寄存器中的FRDY位为1时可以写入这些位。当FRDY位为0时忽略写入这些位。
请注意，位[0]和位[1]是只读的。

FEADDR寄存器指定多块擦除和空白检查命令处理的目标区域的结束地址。Whenincrementalmodeisselectedasth eaddressingmodeforBlankChecking(whenFBCCNT.BCDIR=0) theaddressspecifiedintheFSADDRregistershouldbeeq ualtoorsmallerthantheaddressintheFEADDRregister.Conversely theaddressintheFSADDRregistershouldbeequalto orlargerthantheaddressintheFEADDRregisterwhendecrementalmodeisselectedastheaddressingmodeforBlankChe ck(i.e.whenFBCCNT.BCDIR=1).如果BCDIR、FSADDR和FEADDR位设置与指定规则不一致，则闪存定序器进入命令锁定状态（请参阅第50.11.2.错误保护部分）。

FEADDR值在FSUINITR寄存器中的SUINIT位设置为1时被初始化。它也通过复位被初始化。

FEADDR[31:0]位（FACI命令处理的结束地址）

FEADDR[31:0]位指定多块擦除和空白检查命令处理的结束地址。在命令处理中，位31到17以及任何未到达50.4.12节中列出的地址边界的位。FSADDR：FACI命令起始地址寄存器被忽略。

有关闪存地址的信息，请参阅第50.2节。内存结构。

50.4.14 FMEPROT:FlashPE模式进入保护寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x44

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	CEPROT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	CEPROT	CodeFlashPE模式进入保护 0：FENTRYC位不受保护1：FENTRYC位受保护。	R/W*1 *2 *4
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	R/W*3

注1.仅当FSTATR寄存器中的FRDY位为1时才可以写入该位。当FRDY位=0时写入该位被忽略。

注2.仅当写入16位且写入KEY位的值为D9h时才能写入该位。
注3.这些位不保留写入的值（始终读取为0x00）。
注4.只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问。非安全写入访问被拒绝，但生成了TrustZone访问错误。

CEPROT位（代码闪存PE模式进入保护）

CEPROT位指定FENTRYR寄存器中FRNTRYC位的保护设置。

[Setting condition]

- 1 being written to the CEPROT bit while writing to FMEPROT is enabled.

[Clearing condition]

- 0 being written to the CEPROT bit while writing to FMEPROT is enabled.

50.4.15 FBPROT0 : Flash Block Protection Register

Base address: FACI = 0x407F_E000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPCN0	Block Protection for Non-secure Cancel 0: Block protection is enabled 1: Block protection is disabled.	R/W*1 *2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	R/W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x78.
Note 3. Written values are not retained by these bits (always read as 0x00).

The FBPROT0 register is used to disable the block protect function for non-secure. When the block protect setting is locked by the permanent block setting, it cannot be disabled by this register.

The FBPROT0 value is initialized when the SUINIT bit in the FSUINITR is set to 1, because the FENTRYR value is initialized to 0x0000. It is also initialized by a reset.

BPCN0 bit (Block Protection for Non-secure Cancel)

The BPCN0 bit disables the block protect setting for non-secure function.

[Setting condition]

- When the write-enabling conditions are satisfied and the FENTRYR is not 0x0000, write 1 to this bit.

[Clearing conditions]

- 8 bits being written to FBPROT0 while the FRDY bit is 1.
- A value other than 0x78 specified in the KEY bits and 16 bits are written to FBPROT0 while the FRDY bit is 1.
- 0 being written to the BPCN0 bit while writing to FBPROT0 is enabled.
- The FENTRYR register value is 0x0000.

50.4.16 FBPROT1 : Flash Block Protection for Secure Register

Base address: FACI = 0x407F_E000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Setting condition]

●写入FMEPROT时将1写入CEPROT位使能。

[Clearing condition]

●使能写入FMEPROT时将0写入CEPROT位。

50.4.15 FBPROT0：闪存块保护寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x78

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BPCN0	非安全取消的块保护 0：启用块保护1：禁用块保护 。	R/W*1 *2
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	R/W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入该位。当FRDY位为0时忽略写入该位。
注2.仅当写入16位且写入KEY[7:0]位的值为0x78时，才能写入该位。
注3.这些位不保留写入的值（始终读取为0x00）。

FBPROT0寄存器用于禁用非安全的块保护功能。当块保护设置被永久块设置锁定时，该寄存器不能将其禁用。

FBPROT0值在FSUINITR中的SUINIT位设置为1时被初始化，因为FENTRYR值被初始化为0x0000。它也由复位初始化。

BPCN0位（非安全取消的块保护）

BPCN0位禁用非安全功能的块保护设置。

[Setting condition]

●当写使能条件满足且FENTRYR不为0x0000时，向该位写1。

[Clearing conditions]

●FRDY位为1时，将8位写入FBPROT0。
●当FRDY位为1时，将KEY位中指定的0x78和16位以外的值写入FBPROT0。
●写入FBPROT0时将0写入BPCN0位使能。
●FENTRYR寄存器值为0x0000。

50.4.16 FBPROT1：安全寄存器的闪存块保护

Base address: FACI = 0x407F_E000

Offset address: 0x7C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	BPCN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Function	R/W
0	BPCN1	Block Protection for Secure Cancel 0: Block protection is enabled 1: Block protection is disabled.	R/W*1 *2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	R/W*3

Note 1. Writing to this bit is only possible when the FRDY bit in the FSTATR register is 1. Writing to this bit while FRDY bit = 0 is ignored.
Note 2. Writing to this bit is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0xB1.
Note 3. Written values are not retained by these bits (always read as 0x00).

The FBPROT1 register is used to disable the block protect function for secure developer. When the block protect setting is locked by the permanent block setting, it cannot be disabled by this register.

The FBPROT1 value is initialized when the SUINIT bit in the FSUINITR is set to 1, because the FENTRYR value is initialized to 0x0000. It is also initialized by a reset.

BPCN1 bit (Block Protection for Secure Cancel)

The BPCN1 bit disables the block protect setting for secure function.

[Setting condition]

- When the write-enabling conditions are satisfied and the FENTRYR is not 0x0000, write 1 to BPCN1.

[Clearing conditions]

- 8 bits being written to FBPROT1 while the FRDY bit is 1.
- A value other than 0xB1 specified in the KEY bits and 16 bits are written to FBPROT1 while the FRDY bit is 1.
- 0 being written to the BPCN1 bit while writing to FBPROT1 is enabled.
- The FENTRYR register value is 0x0000.

50.4.17 FSTATR : Flash Status Register

Base address: FACI = 0x407F_E000

Offset address: 0x80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	These bits are read as 0. The write value should be 0.	R/W
6	FLWEERR	Flash Write/Erase Protect Error Flag 0: An error has not occurred 1: An error has occurred.	R
7	—	These bits are read as 0. The write value should be 0.	R/W
8	PRGSPD	Programming Suspend Status Flag 0: The flash sequencer is in a state other than those corresponding to the value 1 1: The flash sequencer is in the programming suspension processing state or programming suspended state.	R

Bit	Symbol	Function	R/W
0	BPCN1	安全取消的块保护 0：启用块保护1：禁用块保护 。	R/W*1 *2
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	R/W*3

注1.仅当FSTATR寄存器中的FRDY位为1时才可以写入该位。当FRDY位=0时写入该位被忽略。
注2.仅当写入16位且写入KEY[7:0]位的值为0xB1时，才能写入该位。
注3.这些位不保留写入的值（始终读取为0x00）。

FBPROT1寄存器用于禁用安全开发人员的块保护功能。当块保护设置被永久块设置锁定时，该寄存器不能将其禁用。

FBPROT1值在FSUINITR中的SUINIT位设置为1时被初始化，因为FENTRYR值被初始化为0x0000。它也由复位初始化。

BPCN1位（安全取消的块保护）

BPCN1位禁用安全功能的块保护设置。

[Setting condition]

●当写使能条件满足且FENTRYR不为0x0000时，向BPCN1写1。

[Clearing conditions]

●FRDY位为1时，将8位写入FBPROT1。
●当FRDY位为1时，将KEY位中指定的0xB1和16位以外的值写入FBPROT1。
●写入FBPROT1时将0写入BPCN1位使能。
●FENTRYR寄存器值为0x0000。

50.4.17 FSTATR：闪存状态寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x80

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
5:0	—	这些位被读取为0。写入值应为0。	R/W
6	FLWEERR	闪存写擦除保护错误标志 0：未发生错误1：发生错误 。	R
7	—	这些位被读取为0。写入值应为0。	R/W
8	PRGSPD	编程挂起状态标志 0：flashsequencer处于与值1对应的状态以外的状态1：flashsequencer处于编程暂停处理状态或编程暂停状态。	R

Bit	Symbol	Function	R/W
9	ERSSPD	Erasure Suspend Status Flag 0: The flash sequencer is in a state other than those corresponding to the value 1 1: The flash sequencer is in the erasure suspension processing state or the erasure suspended state.	R
10	DBFULL	Data Buffer Full Flag 0: The data buffer is empty 1: The data buffer is full.	R
11	SUSRDY	Suspend Ready Flag 0: The flash sequencer cannot receive P/E suspend commands 1: The flash sequencer can receive P/E suspend commands.	R
12	PRGERR	Programming Error Flag 0: Programming has completed successfully 1: An error has occurred during programming.	R
13	ERSERR	Erasure Error Flag 0: Erasure has completed successfully 1: An error has occurred during erasure.	R
14	ILGLERR	Illegal Command Error Flag 0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	R
15	FRDY	Flash Ready Flag 0: Program, Block Erase, Multi Block Erase, P/E suspend, P/E resume, Forced Stop, Blank Check, or Configuration set command processing is in progress 1: None of the above is in progress.	R
19:16	—	These bits are read as 0. The write value should be 0.	R/W
20	OTERR	Other Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
21	SECERR	Security Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R/W
22	FESETERR	FENTRY Setting Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
23	ILGCOMERR	Illegal Command Error 0: A status clear or forced stop command processing is complete 1: An error has occurred.	R
31:24	—	These bits are read as 0. The write value should be 0.	R/W

The FSTATR register indicates the state of the flash sequencer.

FLWEERR flag (Flash Write/Erase Protect Error Flag)

The FLWEERR flag indicates a violation of the flash memory overwrite protection setting in the FWEPROR register. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The flash sequencer starts processing the Forced Stop command.

PRGSPD flag (Programming Suspend Status Flag)

The PRGSPD flag indicates that the flash sequencer is in the programming suspension processing state or programming suspended state.

[Setting condition]

Bit	Symbol	Function	R/W
9	ERSSPD	擦除挂起状态标志 0：闪存定序器处于与值1对应的状态以外的状态1：闪存定序器处于擦除暂停处理状态或擦除暂停状态。	R
10	DBFULL	数据缓冲区满标志 0：数据缓冲区为空1：数据缓冲区已满。	R
11	SUSRDY	挂起就绪标志 0：flash定序器不能接收PE挂起命令1：flash定序器可以接收PE挂起命令。	R
12	PRGERR	编程错误标志 0：烧录成功1：烧录出错。	R
13	ERSERR	擦除错误标志 0：擦除已成功完成1：擦除过程中发生错误。	R
14	ILGLERR	非法命令错误标志 0：闪存定序器未检测到非法FACI命令或非法闪存访问 1：闪存定序器检测到非法FACI命令或非法闪存访问。	R
15	FRDY	闪存就绪标志 0：正在处理编程、块擦除、多块擦除、PE暂停、PE恢复、强制停止、空白检查或配置设置命令处理 1：以上均未进行。	R
19:16	—	这些位被读取为0。写入值应为0。	R/W
20	OTERR	其他错误 0：状态清除或强制停止命令处理完成1：发生错误。	R
21	SECERR	安全错误 0：状态清除或强制停止命令处理完成1：发生错误。	R/W
22	FESETERR	FENTRY设置错误 0：状态清除或强制停止命令处理完成1：发生错误。	R
23	ILGCOMERR	非法命令错误 0：状态清除或强制停止命令处理完成1：发生错误。	R
31:24	—	这些位被读取为0。写入值应为0。	R/W

FSTATR寄存器指示闪存定序器的状态。

FLWEERR标志（闪存写擦除保护错误标志）

FLWEERR标志表示违反了FWEPROR寄存器中的闪存覆盖保护设置。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●闪存定序器开始处理强制停止命令。

PRGSPD标志（编程暂停状态标志）

PRGSPD标志指示闪存定序器处于编程暂停处理状态或编程暂停状态。

[Setting condition]

- The flash sequencer starts processing in response to the programming suspend command.

[Clearing conditions]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- The flash sequencer starts processing the Forced Stop command.

ERSSPD flag (Erasure Suspend Status Flag)

The ERSSPD flag indicates that the flash sequencer is in the erasure suspension processing state or erasure suspended state.

[Setting condition]

- The flash sequencer starts processing in response to an erasure suspend command.

[Clearing condition]

- Reception of the P/E resume command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- The flash sequencer starts processing of the Forced Stop command.

DBFULL flag (Data Buffer Full Flag)

The DBFULL flag indicates the state of the data buffer when the program command is issued. The flash sequencer incorporates a buffer for write data (data buffer). When data for writing to the flash memory are written to the FACI command-issuing area while the data buffer is full, the flash sequencer inserts a wait cycle in the peripheral bus.

[Setting condition]

- The data buffer becomes full while program commands are issued.

[Clearing condition]

- The data buffer becomes empty.

SUSRDY flag (Suspend Ready Flag)

The SUSRDY flag indicates whether the flash sequencer can receive a P/E suspend command.

[Setting condition]

- After starting programming/erasure processing, the flash sequencer enters a state in which P/E suspend commands can be received.

[Clearing conditions]

- Reception of the P/E suspend command or Forced Stop command by the flash sequencer (after write access to the FACI command-issuing area is complete)
- During programming or erasure, the flash sequencer enters the command-locked state
- Programming or erasure has completed.

PRGERR flag (Programming Error Flag)

The PRGERR flag indicates the result of programming of the flash memory. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting condition]

- An error has occurred during programming.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

ERSERR flag (Erasure Error Flag)

The ERSERR flag indicates the result of erasure of the flash memory. When this flag is 1, the flash sequencer is in the command-locked state.

●闪存定序器响应编程暂停命令开始处理。

[Clearing conditions]

●闪存定序器接收到PEresume命令（在对FACI命令发出区域的写访问完成后）

●闪存定序器开始处理强制停止命令。

ERSSPD标志（擦除挂起状态标志）

ERSSPD标志指示闪存定序器处于擦除暂停处理状态或擦除暂停状态。

[Setting condition]

●闪存定序器响应擦除挂起命令开始处理。

[Clearing condition]

●闪存定序器接收到PEresume命令（在对FACI命令发出区域的写访问完成后）

●闪存定序器开始处理强制停止命令。

DBFULL标志（数据缓冲区满标志）

DBFULL标志指示发出程序命令时数据缓冲区的状态。闪存定序器包含一个用于写入数据的缓冲区（数据缓冲区）。当用于写入闪存的数据写入到FACI命令发布区，而数据缓冲区已满时，闪存定序器会在外围总线中插入一个等待周期。

[Setting condition]

●发出程序命令时数据缓冲区已满。

[Clearing condition]

●数据缓冲区变空。

SUSRDY标志（挂起就绪标志）

SUSRDY标志指示闪存定序器是否可以接收PE挂起命令。

[Setting condition]

●开始编程擦除处理后，flash定序器进入可以接收PE挂起命令的状态。

[Clearing conditions]

●闪存定序器接收到PE暂停命令或强制停止命令（在对FACI命令发布区域的写访问完成后）

●在编程或擦除期间，闪存定序器进入命令锁定状态

●编程或擦除已完成。

PRGERR标志（编程错误标志）

PRGERR标志指示闪存的编程结果。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●编程过程中出现错误。

[Clearing condition]

●闪存定序器开始处理状态清除或强制停止命令。

ERSERR标志（擦除错误标志）

ERSERR标志指示闪存擦除的结果。当该标志为1时，闪存定序器处于命令锁定状态。

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[Setting condition]

- An error has occurred during erasure.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

ILGLERR flag (Illegal Command Error Flag)

The ILGLERR flag indicates that the flash sequencer has detected an illegal FACI command or flash memory access. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting conditions]

- See section 50.11.2. Error Protection.

[Clearing condition]

- The flash sequencer starts processing of the Status Clear or Forced Stop command.

FRDY flag (Flash Ready Flag)

The FRDY flag indicates the command processing state of the flash sequencer.

[Setting conditions]

- The flash sequencer completes command processing
- The flash sequencer receives a P/E suspend command and suspends programming of the flash memory
- The flash sequencer received the Forced Stop command and ended command processing.

[Clearing conditions]

- The flash sequencer received an FACI command
- For Program and Configuration setting, the first write access to the FACI command-issuing area
- For other commands, the last write access to the FACI command-issuing area.

OTERR flag (Other Error)

See Table 50.26. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

SECERR flag (Security Error)

See Table 50.26. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

FESETERR flag (FENTRY Setting Error)

See Table 50.26. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

[Setting condition]

●擦除过程中发生错误。

[Clearing condition]

●闪存定序器开始处理状态清除或强制停止命令。

ILGLERR标志（非法命令错误标志）

ILGLERR标志表示闪存定序器检测到非法FACI命令或闪存访问。如果该标志为1，则闪存定序器处于命令锁定状态。

[Setting conditions]

●请参阅第50.11.2节。错误保护。

[Clearing condition]

●闪存定序器开始处理状态清除或强制停止命令。

FRDY标志（闪存就绪标志）

FRDY标志指示闪存定序器的命令处理状态。

[Setting conditions]

●flashsequencer完成命令处理

●闪存定序器收到PE暂停命令并暂停闪存的编程

●闪存定序器收到强制停止命令并结束命令处理。

[Clearing conditions]

●闪存定序器收到FACI命令

●对于ProgramandConfiguration设置，对FACI命令发布区的第一次写访问

●对于其他命令，对FACI命令发布区的最后一次写访问。

OTERR flag (Other Error)

见表50.26。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

SECERR flag (Security Error)

见表50.26。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

FESETERR标志（FENTRY设置错误）

见表50.26。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

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ILGCOMERR flag (Illegal Command Error)

See Table 50.26. When this flag is 1, the flash sequencer is in the command-lock state.

[Setting condition]

- An error has occurred.

[Clearing condition]

- The status clear or forced stop command processing is complete.

50.4.18 FENTRYR : Flash P/E Mode Entry Register

Base address: FACI = 0x407F_E000

Offset address: 0x84

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRYC	Code Flash P/E Mode Entry 0: Code flash is in read mode 1: Code flash is in P/E mode.	R/W*1*2
6:1	—	These bits are read as 0. The write value should be 0.	R/W
7	FENTRYD	Data Flash P/E Mode Entry 0: Data flash is in read mode 1: Data flash is in P/E mode.	R/W*1*2
15:8	KEY[7:0]	Key Code	R/W*3

Note 1. These bits can be written when the FRDY bit in the FSTATR register is 1. Writing to these bits are ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0xAA.
Note 3. Written values are not retained by these bits (always read 0x00).

FENTRYR is used to specify code flash P/E mode or data flash P/E mode. To specify the code flash P/E mode or data flash P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.

FENTRYR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

Note: Writing a value of 0XAA81 to this register causes the ILGLERR bit in the FSTATR register to be set to 1, resulting in the flash sequencer being placed in the command-locked state.

FENTRYC bit (Code Flash P/E Mode Entry)

The FENTRYC bit specifies P/E mode for the code flash memory.

[Setting condition]

- Write 1 to the FENTRYC bit while writing to FENTRYR is enabled and FENTRYR is 0x0000.

[Clearing conditions]

- Write 8 bits to FENTRYR while the FRDY bit is 1
- A value other than 0xAA is specified in the KEY[7:0] bits and 16 bits are written to FENTRYR while the FRDY bit is 1
- Write 0 to the FENTRYC bit while writing to FENTRYR is enabled
- Write to FENTRYR while writing is enabled and its value is other than 0x0000
- The protection of FMEPROT register is enabled.

FENTRYD bit (Data Flash P/E Mode Entry)

The FENTRYD bit specifies P/E mode for the data flash memory.

ILGCOMERR标志（非法命令错误）

见表50.26。当该标志为1时，闪存定序器处于命令锁定状态。

[Setting condition]

●发生错误。

[Clearing condition]

●状态清除或强制停止命令处理完成。

50.4.18 FENTRYR:FlashPE模式进入寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x84

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	FENTRYC	CodeFlashPE模式进入 0：Codeflash处于读取模式1 ：Codeflash处于PE模式。	R/W*1*2
6:1	—	这些位被读取为0。写入值应为0。	R/W
7	FENTRYD	数据闪存PE模式进入 0：数据闪存处于读取模式1 ：数据闪存处于PE模式。	R/W*1*2
15:8	KEY[7:0]	关键代码	R/W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入这些位。当FRDY位为0时忽略写入这些位。
注2.仅当写入16位且写入KEY[7:0]位的值为0xAA时，才能写入这些位。
注3.这些位不保留写入的值（始终读取0x00）。

FENTRYR用于指定代码闪存PE模式或数据闪存PE模式。要指定代码闪存PE模式或数据闪存PE模式，以便闪存定序器可以接收FACI命令，请将FENTRYD或FENTRYC位设置为1以将闪存定序器置于PE模式。

当FSUNITR中的SUINIT位设置为1时，FENTRYR被初始化。它也被复位初始化。

Note: 将值0XAA81写入该寄存器会导致FSTATR寄存器中的ILGLERR位设置为1，从而导致闪存定序器置于命令锁定状态。

FENTRYC位（代码闪存PE模式进入）

FENTRYC位指定代码闪存的PE模式。

[Setting condition]

●写入1到FENTRYC位，同时写入FENTRYR使能并且FENTRYR为0x0000。

[Clearing conditions]

●FRDY位为1时向FENTRYR写入8位
●KEY[7:0]位中指定了0xAA以外的值，当FRDY位为1时，将16位写入FENTRYR
●使能写入FENTRYR时向FENTRYC位写入0
●启用写入时写入FENTRYR，其值不是0x0000
●FMEPROT寄存器保护使能。

FENTRYD位（数据闪存PE模式进入）

FENTRYD位指定数据闪存的PE模式。

[Setting condition]

- Write 1 to the FENTRYD bit while writing to FENTRYR is enabled and FENTRYR is 0x0000.

[Clearing conditions]

- Write 8 bits to FENTRYR while the FRDY bit is 1
- Writing of 16 bits to FENTRYR with a value other than 0xAA specified for the KEY[7:0] bits while the FRDY bit is 1
- Write 0 to the FENTRYD bit while writing to FENTRYR is enabled
- Write to FENTRYR while writing is enabled and its value is other than 0x0000.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the FENTRYD or FENTRYC bits.

50.4.19 FSUINITR : Flash Sequencer Setup Initialization Register

Base address: FACI = 0x407F_E000

Offset address: 0x8C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SUINIT	Set-Up Initialization 0: The FSADDR, FEADDR, FBPROT0, FBPROT1, FENTRYR, FBCCNT, and FCPSR flash sequencer setup registers keep their current values 1: The FSADDR, FEADDR, FBPROT0, FBRPOT1, FENTRYR, FBCCNT, and FCPSR flash sequencer setup registers are initialized.	R/W*1*2
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	R/W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x2D.
Note 3. Written values are not retained by these bits (always read 0x00).

FSUINITR is used for initialization of the flash sequencer setup.

SUINIT bit (Set-Up Initialization)

The SUINIT bit initializes the following flash sequencer setup registers:

- FSADDR
- FEADDR
- FBPROT0
- FBPROT1
- FENTRYR
- FBCCNT
- FCPSR.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the SUINIT bit.

[Setting condition]

●写入1到FENTRYD位，同时写入FENTRYR使能并且FENTRYR为0x0000。

[Clearing conditions]

●FRDY位为1时向FENTRYR写入8位
●当FRDY位为1时，将16位写入FENTRYR，其中KEY[7:0]位指定的值不是0xAA
●使能写入FENTRYR时向FENTRYD位写入0
●写入启用时写入FENTRYR，其值不是0x0000。

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对FENTRYD或FENTRYC位的写入权限。

50.4.19 FSUINITR：闪存定序器设置初始化寄存器

Base address: FACI = 0x407F_E000

Offset address: 0x8C

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	SUINIT	Set-Up Initialization 0：FSADDR、FEADDR、FBPROT0、FBPROT1、FENTRYR、FBCCNT和FCPSR闪存定序器设置寄存器保持其当前值 1：初始化FSADDR、FEADDR、FBPROT0、FBRPOT1、FENTRYR、FBCCNT和FCPSR闪存定序器设置寄存器。	R/W*1*2
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	R/W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入该位。当FRDY位为0时忽略写入该位。
注2.仅当写入16位且写入KEY[7:0]位的值为0x2D时才能写入这些位。
注3.这些位不保留写入的值（始终读取0x00）。

FSUINITR用于初始化闪存定序器设置。

SUINIT bit (Set-Up Initialization)

SUINIT位初始化以下闪存序列器设置寄存器：

- FSADDR
- FEADDR
- FBPROT0
- FBPROT1
- FENTRYR
- FBCCNT
- FCPSR.

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对SUINIT位的写入权限。

50.4.20 FCMDR : FACI Command Register

Base address: FACI = 0x407F_E000

Offset address: 0xA0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMDR[7:0]								PCMDR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	PCMDR[7:0]	Pre-command Flag The command just before the latest command is stored.	R
15:8	CMDR[7:0]	Command Flag The latest command is stored.	R

FCMDR records the two most recent commands accepted by the flash sequencer.

PCMDR[7:0] bits (Pre-command Flag)

The PCMDR[7:0] bits indicate the command received immediately before the latest command received by the flash sequencer.

CMDR[7:0] bits (Command Flag)

The CMDR[7:0] bits indicate the latest command received by the flash sequencer.

Table 50.6 States of FCMDR after receiving commands

Command	CMDR	PCMDR
Program	0xE8	Previous command
Block erase	0xD0	0x20
Multi block erase	0xD0	0x21
P/E suspend	0xB0	Previous command
P/E resume	0xD0	Previous command
Status Clear	0x50	Previous command
Forced Stop	0xB3	Previous command
Blank Check	0xD0	0x71
Configuration set	0x40	Previous command

50.4.21 FBCCNT : Blank Check Control Register

Base address: FACI = 0x407F_E000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCDIR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCDIR	Blank Check Direction 0: Blank checking is executed from the lower addresses to the higher addresses (incremental mode) 1: Blank checking is executed from the higher addresses to the lower addresses (decremental mode).	R/W

50.4.20 FCMDR:FACI命令寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xA0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	CMDR[7:0]								PCMDR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
7:0	PCMDR[7:0]	Pre-command Flag 存储最新命令之前的命令。	R
15:8	CMDR[7:0]	命令标志 存储最新的命令。	R

FCMDR记录闪存定序器最近接受的两个命令。

PCMDR[7:0] bits (Pre-command Flag)

PCMDR[7:0]位指示在闪存定序器接收到的最新命令之前收到的命令。

CMDR[7:0] bits (Command Flag)

CMDR[7:0]位指示闪存定序器接收到的最新命令。

Table 50.6 FCMDR收到指令后的状态

Command	CMDR	PCMDR
Program	0xE8	上一条命令
块擦除	0xD0	0x20
多块擦除	0xD0	0x21
P/E suspend	0xB0	上一条命令
P/E resume	0xD0	上一条命令
状态清除	0x50	上一条命令
强制停止	0xB3	上一条命令
空白支票	0xD0	0x71
配置集	0x40	上一条命令

50.4.21 FBCCNT:空白检查控制寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xD0

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCDIR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCDIR	空白支票方向 0：从低地址到高地址执行空白检查（增量模式） 1：从高地址到低地址执行空白检查（递减模式）。	R/W

Bit	Symbol	Function	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FBCCNT specifies the addressing mode in processing the Blank Check command. FBCCNT is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

BCDIR bit (Blank Check Direction)

The BCDIR bit specifies the addressing mode for Blank Check.

50.4.22 FBCSTAT : Blank Check Status Register

Base address: FACI = 0x407F_E000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCST	Blank Check Status Flag 0: The target area is in the non-programmed state, that is, the area has been erased but has not yet been reprogrammed 1: The target area has been programmed with 0s or 1s.	R
7:1	—	These bits are read as 0. The write value should be 0.	R/W

FBCSTAT stores the results of checking in response to the Blank Check command.

BCST flag (Blank Check Status Flag)

The BCST flag indicates the results of checking in response to the Blank Check command.

50.4.23 FPSADDR : Data Flash Programming Start Address Register

Base address: FACI = 0x407F_E000

Offset address: 0xD8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16:0]																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
16:0	PSADR[16:0]	Programmed Area Start Address The address of the first programmed area	R
31:17	—	These bits are read as 0. The write value should be 0.	R/W

FPSADDR indicates the address of the first programmed area found in processing of the Blank Check command.

PSADR[16:0] bits (Programmed Area Start Address)

The PSADR[16:0] bits indicate the address of the first programmed area found in processing of the Blank Check command. The address is an offset from the address where the data flash memory starts. The setting of these bits is only valid if the BCST bit in the FBCSTAT register is 1 and while the FRDY bit in the FSTATR register is 1. When the BCST bit in the FBCSTAT register is 0, the PSADR[16:0] bits hold the address produced by the previous check.

Bit	Symbol	Function	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W

FBCCNT指定处理空白检查命令的寻址模式。当FSUINITR中的SUINIT位设置为1时，FBCCNT被初始化。它也被复位初始化。

BCDIR位（空白检查方向）

BCDIR位指定空白检查的寻址模式。

50.4.22 FBCSTAT:空白检查状态寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xD4

Bit position:	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	BCST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	BCST	空白检查状态标志 0：目标区域处于非编程状态，即该区域已被擦除但尚未重新编程 1：目标区域已编程为0或1。	R
7:1	—	这些位被读取为0。写入值应为0。	R/W

FBCSTAT存储响应空白检查命令的检查结果。

BCST标志（空白检查状态标志）

BCST标志指示响应空白检查命令的检查结果。

50.4.23 FPSADDR:数据闪存编程起始地址寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xD8

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16:0]																
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
16:0	PSADR[16:0]	编程区起始地址 第一个编程区域的地址	R
31:17	—	这些位被读取为0。写入值应为0。	R/W

FPSADDR指示在处理空白检查命令时发现的第一个编程区域的地址。

PSADR[16:0]位（编程区起始地址）

PSADR[16:0]位指示在处理空白检查命令时发现的第一个编程区域的地址。
该地址是数据闪存起始地址的偏移量。仅当FBCSTAT寄存器中的BCST位为1且FSTATR寄存器中的FRDY位为1时，这些位的设置才有效。当
FBCSTAT寄存器为0，PSADR[16:0]位保存上一次检查产生的地址。

50.4.24 FSUASMON : Flash Startup Area Select Monitor Register

Base address: FACI = 0x407F_E000

Offset address: 0xDC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0. The write value should be 0.	R
15	FSPR	Protection Programming Flag to set Boot Flag and Startup Area Control 0: Protected state 1: Non-protected state.	R
30:16	—	These bits are read as 0. The write value should be 0.	R
31	BTFLG	Flag of Startup Area Select for Boot Swap 0: The startup area is the alternate block (block 1) 1: The startup area is the default block (block 0).	R

FSPR bit (Protection Programming Flag to set Boot Flag and Startup Area Control)

The FSPR bit indicates the protection state against the configuration set command for the BTFLG bit, and FSUACR Register.

In response to a reset or configuration set command, the FACI transfers data from flash memory to this register.

BTFLG bit (Flag of Startup Area Select for Boot Swap)

The BTFLG bit indicates whether the address of the startup area is exchanged for the boot swap function or not.

In response to a reset or configuration set command, the FACI transfers data from flash memory to this register.

50.4.25 FCPSR : Flash Sequencer Processing Switching Register

Base address: FACI = 0x407F_E000

Offset address: 0xE0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESUSPMD	Erasure Suspend Mode 0: Suspension priority mode 1: Erasure priority mode.	R/W
15:1	—	These bits are read as 0. The write value should be 0.	R/W

FCPSR selects the erasure suspension mode. FCPSR is initialized when the SUINIT bit in FSUINITR is set to 1. It is also initialized by a reset.

50.4.24 FSUASMON:闪存启动区选择监控寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xDC

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	BTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	FSPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位被读取为0。写入值应为0。	R
15	FSPR	保护编程标志设置引导标志和启动区控制 0：保护状态1：非保护状态。	R
30:16	—	这些位被读取为0。写入值应为0。	R
31	BTFLG	引导交换的启动区域选择标志 0：启动区为alternateblock（block1）1：启动区为defaultblock（block0）。	R

FSPR位（用于设置引导标志和启动区域控制的保护编程标志）

FSPR位指示针对BTFLG位的配置设置命令的保护状态，而FSUACR Register.

响应复位或配置设置命令，FACI将数据从闪存传输到该寄存器。

BTFLG位（用于引导交换的启动区域选择标志）

BTFLG位指示启动区域的地址是否被交换为引导交换功能。

响应复位或配置设置命令，FACI将数据从闪存传输到该寄存器。

50.4.25 FCPSR:闪存定序器处理切换寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xE0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	ESUSPMD	擦除挂起模式 0：暂停优先模式1：擦除优先模式。	R/W
15:1	—	这些位被读取为0。写入值应为0。	R/W

FCPSR选择擦除暂停模式。当FSUINITR中的SUINIT位设置为1时，FCPSR被初始化。它也被复位初始化。

ESUSPMD bit (Erasure Suspend Mode)

The ESUSPMD bit selects the erasure suspension mode when a P/E suspend command is issued while the flash sequencer is executing erasure processing (see section 50.9.3.10. P/E Suspend Command). This bit should be set before issuing Block Erase or Multi Block Erase command.

50.4.26 FPCKAR : Flash Sequencer Processing Clock Notification Register

Base address: FACI = 0x407F_E000

Offset address: 0xE4

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								PCKA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bit	Symbol	Function	R/W
7:0	PCKA[7:0]	Flash Sequencer Operating Clock Notification These bits are used to set the operating frequency of the flash sequencer while processing FACI commands.	R/W*1*2
15:8	KEY[7:0]	Key Code	R/W*3

Note 1. This bit can be written when the FRDY bit in the FSTATR register is 1. Writing to this bit is ignored when the FRDY bit is 0.
Note 2. Writing to these bits is only possible when 16 bits are written and the value written to the KEY[7:0] bits is 0x1E.
Note 3. Written values are not retained by these bits (always read 0x00).

FPCKAR specifies the operating frequency of the flash sequencer while processing FACI commands. The highest operating frequency for the given product is set as the initial value.

PCKA[7:0] bits (Flash Sequencer Operating Clock Notification)

The PCKA[7:0] bits specify the operating frequency of the flash sequencer while processing FACI commands. Set the desired frequency for these bits before issuing an FACI command. Specifically, convert the frequency in MHz to a binary number and set it for these bits.

Example:

Frequency is 35.9 MHz (PCKA = 0x24)

Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number.

If the value set in these bits is smaller than the actual operating frequency of the flash sequencer, the flash memory programming/erasure characteristics cannot be guaranteed. If the value set in these bits is greater than the actual operating frequency of the flash sequencer, the flash memory programming/erasure characteristics can be guaranteed but the FACI command processing time such as the time programming/erasure takes will increase. The minimum FACI command processing time is obtained when the operating frequency of the flash sequencer is the same as the PCKA value.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the PCKA bit.

50.4.27 FSUACR : Flash Startup Area Control Register

Base address: FACI = 0x407F_E000

Offset address: 0xE8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ESUSPMD位（擦除挂起模式）

当闪存定序器正在执行擦除处理时发出PE暂停命令时，ESUSPMD位选择擦除暂停模式（请参阅第50.9.3.10节。PE暂停命令）。该位应在发出块擦除或多块擦除命令之前设置。

50.4.26 FPCKAR:闪存定序器处理时钟通知寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xE4

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								PCKA[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

Bit	Symbol	Function	R/W
7:0	PCKA[7:0]	闪存定序器工作时钟通知 这些位用于在处理时设置闪存定序器的工作频率 FACI命令。	R/W*1*2
15:8	KEY[7:0]	关键代码	R/W*3

注1.当FSTATR寄存器中的FRDY位为1时可以写入该位。当FRDY位为0时忽略写入该位。
注2.仅当写入16位且写入KEY[7:0]位的值为0x1E时，才能写入这些位。
注3.这些位不保留写入的值（始终读取0x00）。

FPCKAR在处理FACI命令时指定闪存定序器的工作频率。将给定产品的最高工作频率设置为初始值。

PCKA[7:0]位（闪存定序器工作时钟通知）

PCKA[7:0]位指定闪存定序器在处理FACI命令时的工作频率。在发出FACI命令之前为这些位设置所需的频率。具体来说，将以MHz为单位的频率转换为二进制数并为这些位设置它。

Example:

频率为35.9MHz(PCKA=0x24)

将35.9MHz的第一个小数位四舍五入为整数(=36)并将其转换为二进制数。

如果这些位中设置的值小于闪存定序器的实际工作频率，则无法保证闪存编程擦除特性。如果这些位中设置的值大于闪存定序器的实际工作频率，则可以保证闪存编程擦除特性，但FACI命令处理时间（例如编程擦除所花费的时间）会增加。当闪存定序器的工作频率与PCKA值相同时，得到最小FACI命令处理时间。

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对PCKA位的写入权限。

50.4.27 FSUACR：闪存启动区控制寄存器

Base address: FACI = 0x407F_E000

Offset address: 0xE8

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
1:0	SAS[1:0]	Startup Area Select 0 0: Startup area is selected by BTFLG bit 0 1: Startup area is selected by BTFLG bit 1 0: Startup area is temporarily switched to the default area (block 0) 1 1: Startup area is temporarily switched to the alternate area (block 1).	R/W*1 *3
7:2	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	Key Code	R/W*2

Note 1. Following described the write condition of thisese bits (these conditions are required at the same time).
1. Access size to this register is 16 bits
2. The value of KEY[7:0] is 0x66
3. The FSPR bit is 1.

Note 2. Written values are not retained by these bits (always read 0x00).

Note 3. Only secure access can write to this register. Both secure access and non-secure read access are allowed. Non-secure write access is denied, but TrustZone access error is note generated.

FSUACR sets the startup area for the boot swap function. Do not use this register in dual mode (the DUALSEL.BANKMD[2:0] bits are 000b). In dual mode, starting up proceeds from startup area 0.

SAS[1:0] bits (Startup Area Select)

The SAS[1:0] bits select the startup area. Three methods are available for changing the startup area.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits control writing permission to the SAS [1:0] bits.

50.4.28 FCKMHZ : Data Flash Access Frequency Register

Base address: FLAD = 0x407F_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FCKMHZ[7:0]							
Value after reset:	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	FCKMHZ[7:0]	Data Flash Access Frequency Register These bits optimize the speed of reading the data flash memory.	R/W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

This register optimizes the speed of reading the data flash memory.

Set the frequency of the peripheral module clock (FCLK) of internal peripheral bus which is the clock for access to the data flash memory, in MHz units. For example, 35.9 MHz should be rounded up and set the frequency to 36. Number of cycles required for access to the data flash memory are inserted according to the frequency. When changing the frequency of the FCLK, follow the procedure below to modify the value of the data flash access frequency register (FCKMHZ) in either of the following ways according to whether operation is at a lower frequency before or after the change.

- When changing the speed from low to high: Modify FCKMHZ. After confirming the change by reading FCKMHZ, change the frequency.
- When changing the speed from high to low: Change the frequency. After the frequency is changed, modify FCKMHZ.

50.5 Flash Cache

Bit	Symbol	Function	R/W
1:0	SAS[1:0]	启动区域选择 00：启动区域由BTFLG位选择01：启动区域由BTFLG位选择10：启动区域暂时切换到默认区域（块0）11：启动区域暂时切换到备用区域（块1）。	R/W*1 *3
7:2	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	关键代码	R/W*2

注1.下面描述了这些位的写入条件（这些条件是同时需要的）。1.对该寄存器的访问大小为16位2.KEY[7:0]的值为0x663.FSPR位为1。

注2.这些位不保留写入的值（始终读取0x00）。

注3.只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问。非安全写入访问被拒绝，但生成了TrustZone访问错误。

FSUACR设置引导交换功能的启动区域。不要在双模式下使用该寄存器（DUALSEL.BANKMD[2:0]位为000b)。在双模式下，从启动区域0开始启动。

SAS[1:0]位（启动区域选择）

SAS[1:0]位选择启动区域。三种方法可用于更改启动区域。

KEY[7:0] bits (Key Code)

KEY[7:0]位控制对SAS[1:0]位的写入权限。

50.4.28 FCKMHZ:数据闪存访问频率寄存器

Base address: FLAD = 0x407F_C000

Offset address: 0x40

Bit position:	7	6	5	4	3	2	1	0
Bit field:	FCKMHZ[7:0]							
重置后的值：	0	0	1	1	1	1	0	0

Bit	Symbol	Function	R/W
7:0	FCKMHZ[7:0]	数据闪存访问频率寄存器 这些位优化了数据闪存的读取速度。	R/W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

该寄存器优化了数据闪存的读取速度。

设置内部外围总线的外围模块时钟(FCLK)的频率，它是访问数据闪存的时钟，以MHz为单位。例如，35.9MHz应向上取整，并将频率设置为36。根据频率插入访问数据闪存所需的周期数。当改变FCLK的频率时，根据改变之前或之后是在较低频率下操作，按照以下步骤，通过以下任一方式修改数据闪存访问频率寄存器(FCKMHZ)的值。

●转速由低变高时：修改FCKMHZ。通过读取FCKMHZ确认更改后，更改频率。

●速度由高变低时：改变频率。频率改变后，修改FCKMHZ。

50.5 闪存缓存

50.5.1 Feature of flash cache

The FCACHE (Flash Cache) speeds up read access from bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and access from EDMAC
- FLPF, for the prefetch access in CPU instruction fetches

Table 50.7 Flash Cache 1 (FCACHE1) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU instruction Fetch
Capacity	256 Bytes
Associativity	8WAY set associative
	128 bits/entry (128 bit aligned data), 2 entries/way
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

Table 50.8 Flash Cache 2 (FCACHE2) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Target Bus Master	CPU Operand Access and Access from EDMAC
Capacity	16 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 1 entry
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

Table 50.9 Prefetch Buffer (FLPF) overview

Cache Target Region	0x0000_0000 - 0x007F_FFFF
Capacity	32 Bytes
Associativity	Full Associative
	128 bits/entry (128 bit aligned data), 2 entries
Request Address	Next address of previous CPU Instruction
Access Cycle	Cache Hit : 0 wait Cache Miss : wait number of Flash Wait Cycle Register

50.5.1 闪存缓存的特点

FCACHE(FlashCache)加快了从总线主机到闪存的读取访问。FCACHE包括：

●FCACHE1，用于CPU取指

●FCACHE2，用于CPU操作数访问和EDMAC访问

●FLPF，用于CPU取指中的预取访问

Table 50.7 闪存1(FCACHE1)概述

缓存目标区域	0x0000_0000 - 0x007F_FFFF
目标总线主控	CPU指令取指
Capacity	256 Bytes
Associativity	8WAY集合关联
	128位入口（128位对齐数据），2入口方式
访问周期	缓存命中：0等待 CacheMiss:Flash等待周期寄存器的等待数

Table 50.8 闪存2(FCACHE2)概述

缓存目标区域	0x0000_0000 - 0x007F_FFFF
目标总线主控	CPU操作数访问和来自EDMAC的访问
Capacity	16 Bytes
Associativity	全联想
	128位条目（128位对齐数据），1个条目
访问周期	缓存命中：0等待 CacheMiss:Flash等待周期寄存器的等待数

Table 50.9 预取缓冲区(FLPF)概述

缓存目标区域	0x0000_0000 - 0x007F_FFFF
Capacity	32 Bytes
Associativity	全联想
	128位条目（128位对齐数据），2个条目
请求地址	上一条CPU指令的下一个地址
访问周期	缓存命中：0等待 CacheMiss:Flash等待周期寄存器的等待数

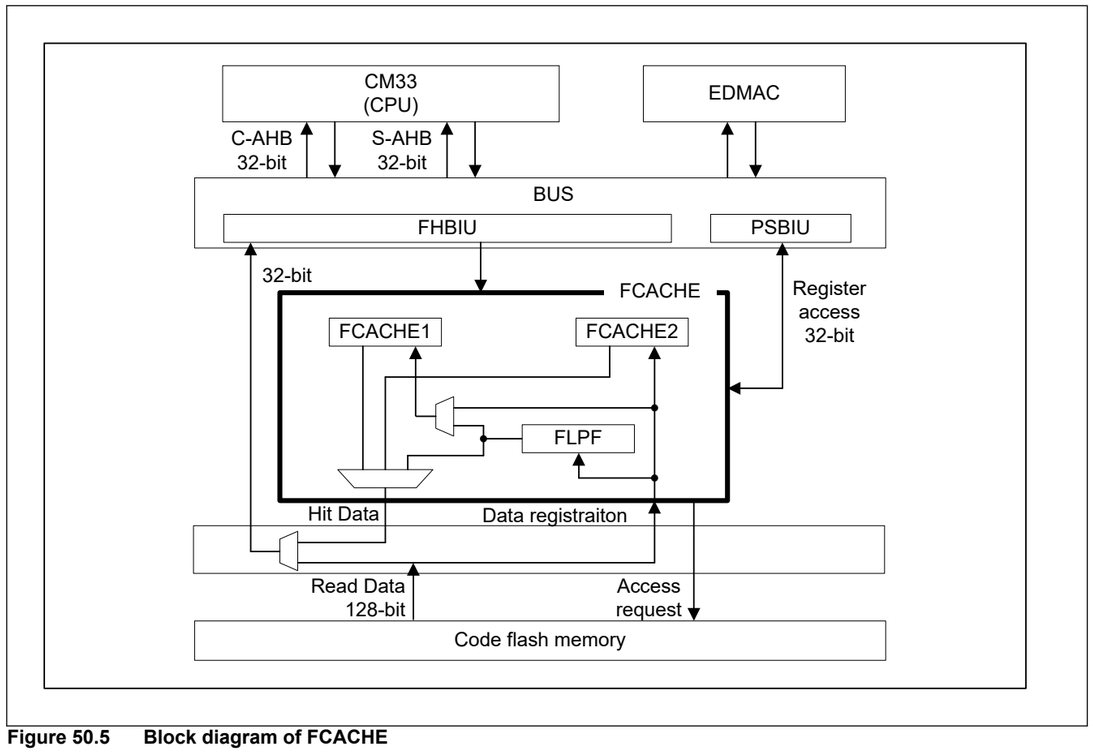

Figure 50.5 Block diagram of FCACHE

50.6 Operating Modes Associated with Flash Memory

Figure 50.6 is a diagram of the mode transitions associated with the flash memory. For the procedures for setting the modes, see section 6, Option-Setting Memory.

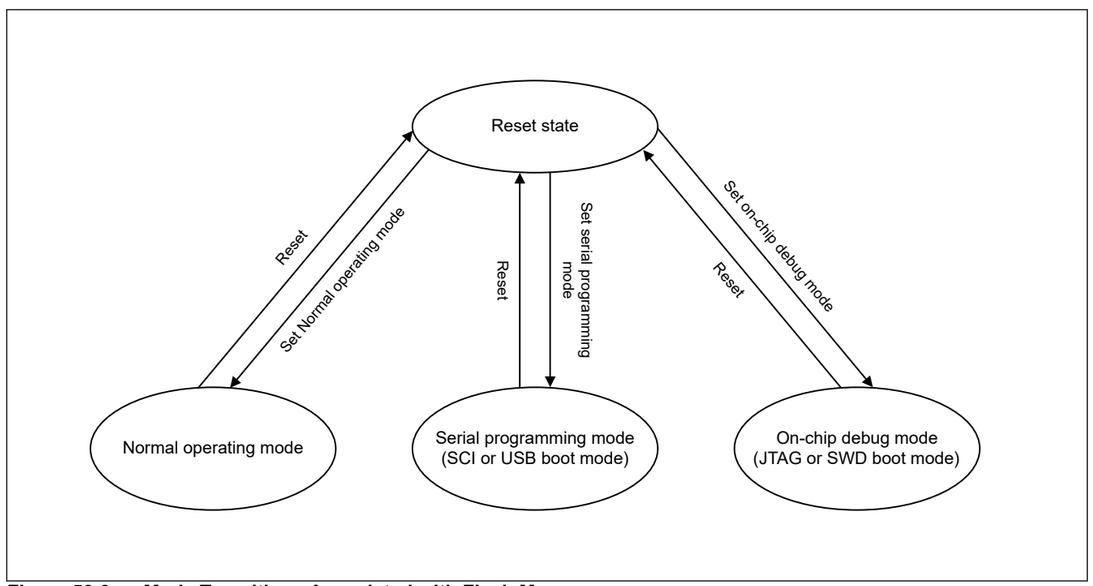

Figure 50.6 Mode Transitions Associated with Flash Memory

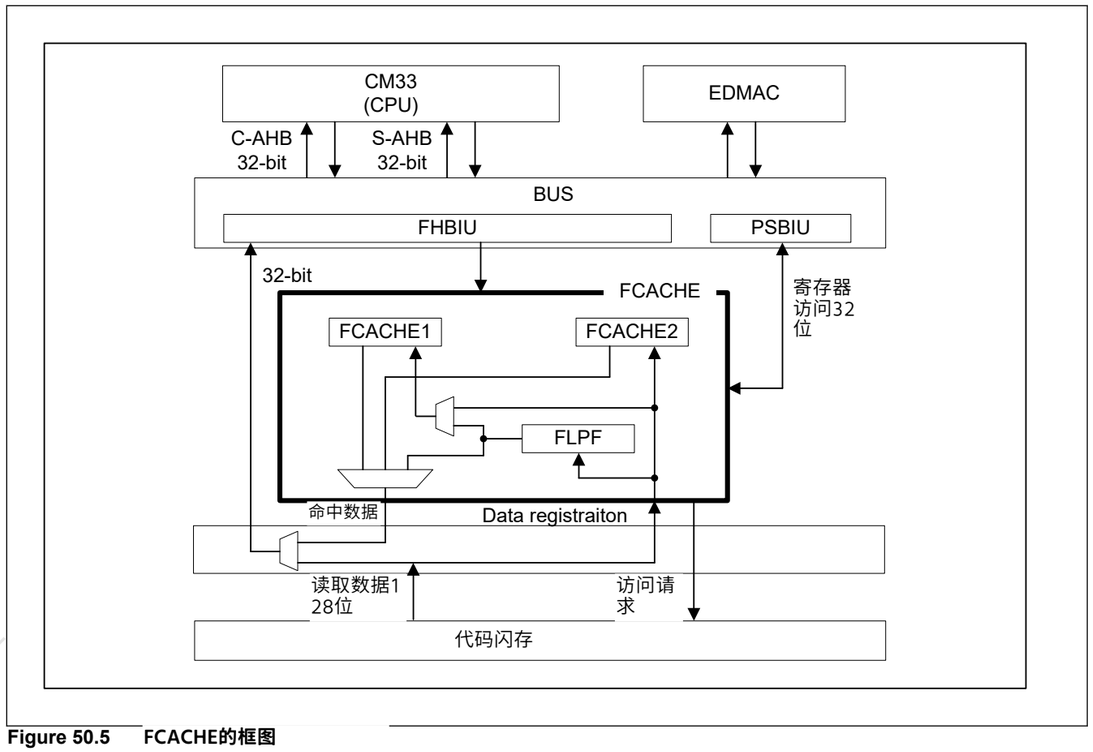

Figure 50.5 FCACHE的框图

50.6 与闪存相关的操作模式

图50.6是与闪存相关的模式转换图。有关设置模式的步骤，请参阅第6节，选项设置内存。

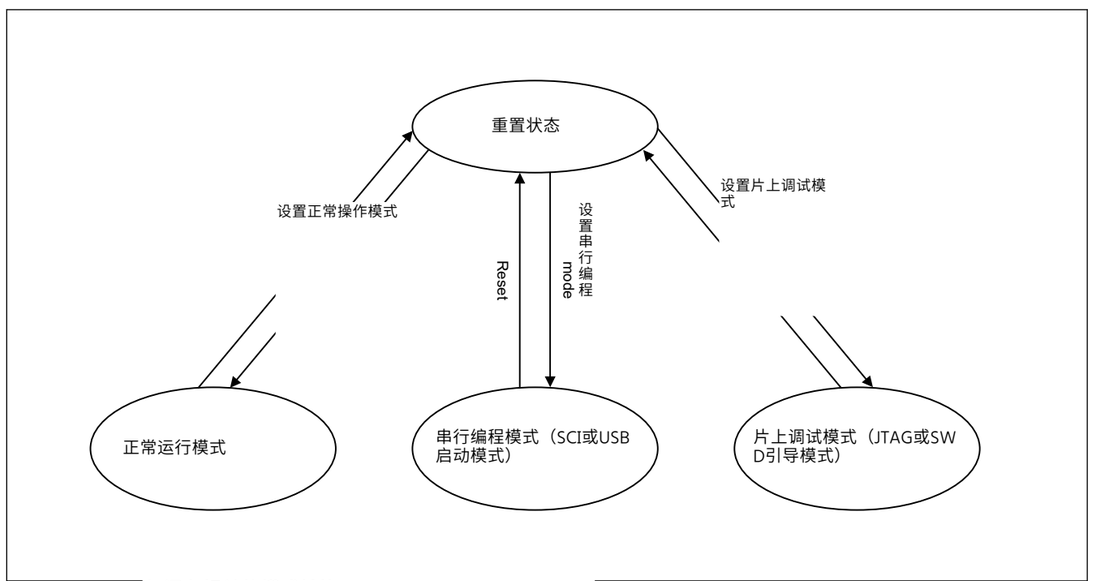

Figure 50.6 与闪存相关的模式转换

The flash memory area where programming and erasure are permitted and the boot program after a reset are different according to each mode. The differences between modes are listed in Table 50.10.

Table 50.10 Differences between Modes

Parameter	Normal operating mode	Serial programming mode (SCI or USB boot mode)	On-chip debug mode (JTAG or SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory • Option setting memory (programming only)	• Code flash memory • Data flash memory • Option-setting memory (programming only)	• Code flash memory • Data flash memory • Option setting memory (programming only)
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

50.7 Overview of Functions

By using a dedicated flash-memory programmer to program the flash memory through a serial interface (serial programming) or JTAG/SWD interface (on-chip debug mode), the device can be rewritten regardless of whether this is before or after it is mounted on the target system.

Furthermore, security functions to prohibit rewriting or reading of the user program written to the flash memory are incorporated, and this can prevent falsification and illicit reading of the programs by third parties.

Programming by the user program (self-programming) is available to suit applications where the application on the target system may require updating after manufacturing or shipment. Protection features for the safe rewriting of the flash memory are also incorporated. Furthermore, interrupt processing during self-programming is supported, so programming can proceed at the same time as processing for external communications, etc., and this is the case in various situations. Table 50.11 lists the overview of the methods of programming and the corresponding operating modes.

Table 50.11 Programming methods

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer through the SCI or USBFS interface enables on-board programming of the flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer through the SCI or USBFS interface and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from the code flash memory while the data flash memory is programmed. As a result, a program resident in the code flash memory is able to program the data flash memory. For background operations that are not possible, instructions in the code flash memory cannot be fetched and data cannot be accessed while the code flash memory is being programmed by self-programming. In such cases, a program for programming from the internal SRAM or external memory must be transferred in advance and executed.	Normal operating mode
JTAG or SWD programming	A dedicated flash-memory programmer or an on-chip debugger through JTAG or SWD enables on-board programming of the flash memory after the device is mounted on the target system. A dedicated flash-memory programmer or an on-chip debugger through JTAG or SWD and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	On-chip debug mode

Table 50.12 lists the functions of the flash memory. Serial programmer commands realize each function of serial programming, while reading of the flash memory by an FACI command or the user program realizes each function of self-programming.

允许编程和擦除的闪存区域和复位后的引导程序根据每种模式而不同。模式之间的差异在表50.10中列出。

Table 50.10 模式之间的差异

Parameter	正常运行模式	串行编程模式（SCI或USB启动模式）	片上调试模式（JTAG或SWD引导模式）
可编程和可擦除区域	• 代码闪存 • 数据闪存 • 选项设置内存（仅编程）	• 代码闪存 • 数据闪存 • Option-setting memory (programming only)	• 代码闪存 • 数据闪存 • 选项设置内存（仅编程）
以块为单位擦除	Possible	Possible	Possible
复位时的引导程序	用户区程序	用于串行编程的嵌入式程序	取决于调试命令

50.7 功能概述

通过使用专用闪存编程器通过串行接口（串行编程）或JTAGSWD接口（片上调试模式）对闪存进行编程，无论是在安装之前还是之后，都可以重写设备目标系统。

此外，内置了禁止重写或读取写入闪存的用户程序的安全功能，这可以防止第三方篡改和非法读取程序。

用户程序编程（自编程）适用于目标系统上的应用程序在制造或发货后可能需要更新的应用程序。还集成了用于安全重写闪存的保护功能。此外，支持自编程期间的中断处理，因此可以与外部通信处理等同时进行编程，这在各种情况下都是如此。表50.11列出了编程方法和相应操作模式的概述。

Table 50.11 编程方法

编程方法	功能概览	操作模式
串行编程	通过SCI或USBFS接口的专用闪存编程器可在器件安装到目标系统后对闪存进行板载编程。	串行编程模式
	通过SCI或USBFS接口的专用闪存编程器和专用编程适配器板允许对闪存进行板外编程，例如，在将设备安装到目标系统之前对其进行编程。	
Self-programming	在串行编程执行之前写入存储器的用户程序也可以对闪存进行编程。后台操作能力使得在对数据闪存进行编程时，可以从代码闪存中获取指令或以其他方式读取数据。结果，驻留在代码闪存中的程序能够对数据闪存进行编程。对于无法进行的后台操作，在自编程对代码闪存进行编程时，无法获取代码闪存中的指令并且无法访问数据。在这种情况下，必须预先传输并执行从内部SRAM或外部存储器进行编程的程序。	正常运行模式
JTAG或SWD编程	专用闪存编程器或通过JTAG或SWD的片上调试器可在器件安装到目标系统后对闪存进行板载编程。专用闪存编程器或片上调试器通过 JTAG或SWD和专用编程适配器板允许对闪存进行板外编程，例如，在将器件安装到目标系统之前对其进行编程。	片上调试模式

表50.12列出了闪存的功能。串行编程器命令实现串行编程的各个功能，而通过FACI命令或用户程序读取闪存实现自编程的各个功能。

Table 50.12 Basic Functions

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing is written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not proceeded after erasure.	Not supported	Supported (data flash programming only)
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
CRC	Calculates the CRC in the specified range of the flash memory and transfers it to the flash programmer	Supported	Non supported
Read	Reads data programmed in the flash memory	Supported	Not supported (read by user program is possible)
Start-up program protection functions	Configures the start-up program protection functions	Supported	Supported
Option function selection	Selects the option function, and modifies the initial setting of this MCU	Supported	Supported
Dual bank function	Switches different modes (linear or dual)	Supported	Supported
Block swap function	Setting block swap functions	Supported	Supported
Block protection	Setting block protection	Supported	Supported
Device lifecycle transition	Transitions the device lifecycle	Supported	Not supported
Memory security attribution	Setting the memory security attribution	Supported	Not supported
Key	Injects key	Supported	Supported (except the key related to device lifecycle transition)
All erasure	Erase the flash memory to the state after shipment	Supported	Not supported

The flash memory supports various security functions.

Table 50.13 lists the security functions supported by the flash memory.

Table 50.13 Lists of Security Functions

Function	Description
Security flag for Start-up area select	Start-up area selection can be protected by setting of security flag (FSPR).
Permanently block protection	Programming or erasure of each block of code flash memory can be protected permanently.
Protection for TrustZone	Programming or erasure area, readable area, register access, and FACI command operation are protected by ARM TrustZone security.
Programming or erasure mode protection	Only secure developer can enter the programming or erasure mode for code flash.

50.8 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in Figure 50.7. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the value of the FENTRYR register is 0x0000, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and data flash memory are both readable.

When the value of the FENTRYR register is 0x0001, the flash sequencer is in code flash P/E mode where the code flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is readable. In addition, the code flash memory is not readable if background operation (BGO) is disabled. If BGO is enabled, the code flash memory that is not selected by FSADDR register is readable when the FRDY bit in the FSTATR register is 0. As for the condition for enabling BGO, see section 50.15.2. Background Operation.

Table 50.12 基本功能

Function	功能概览	Availability	
		串行编程	自编程
空白支票	检查指定的块以确保尚未对其进行写入。无法保证从擦除后没有写入任何内容的数据闪存中读取的结果，因此使用空白检查来确认擦除后没有继续写入内存。	不支持	支持（仅数据闪存编程）
块擦除	擦除指定块中的内存内容	Supported	Supported
Programming	写入指定地址	Supported	Supported
CRC	计算flash存储器指定范围内的CRC，并传送给flash编程器	Supported	不支持
Read	读取闪存中编程的数据	Supported	不支持（可由用户程序读取）
启动程序保护功能	配置启动程序保护功能	Supported	Supported
选项功能选择	选择选项功能，修改本MCU的初始设置	Supported	Supported
双银行功能	切换不同的模式（线性或双）	Supported	Supported
区块交换功能	设置块交换功能	Supported	Supported
块保护	设置块保护	Supported	Supported
设备生命周期过渡	过渡设备生命周期	Supported	不支持
内存安全归属	设置内存安全属性	Supported	不支持
Key	注入密钥	Supported	支持（设备生命周期转换相关的key除外）
全部擦除	擦除闪存到出货后的状态	Supported	不支持

闪存支持各种安全功能。

表50.13列出了闪存支持的安全功能。

Table 50.13 安全功能列表

Function	Description
启动区域选择的安全标志	启动区域选择可以通过设置安全标志(FSPR)来保护。
永久阻止保护	可以永久保护每个代码闪存块的编程或擦除。
保护TrustZone	编程或擦除区域、可读区域、寄存器访问和FACI命令操作受ARMTrustZone安全保护。
编程或擦除模式保护	只有安全的开发人员才能进入代码闪存的编程或擦除模式。

50.8 FlashSequencer的操作模式

闪存定序器具有三种操作模式，如图50.7所示。通过更改FENTRYR寄存器的值来启动模式之间的转换。

当FENTRYR寄存器的值为0x0000时，闪存定序器处于读取模式。在这种模式下，它不接收FACI命令。代码闪存和数据闪存都是可读的。

当FENTRYR寄存器的值为0x0001时，闪存定序器处于代码闪存PE模式，代码闪存可以通过FACI命令进行编程或擦除。在这种模式下，数据闪存是可读的。此外，如果禁用后台操作(BGO)，则代码闪存不可读。如果BGO使能，则当FSTATR寄存器中的FRDY位为0时，可以读取FSADDR寄存器未选择的代码闪存。关于使能BGO的条件，请参见50.15.2节。后台操作。

When the value of the FENTRYR register is 0x0080, the flash sequencer is in data flash P/E mode where the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

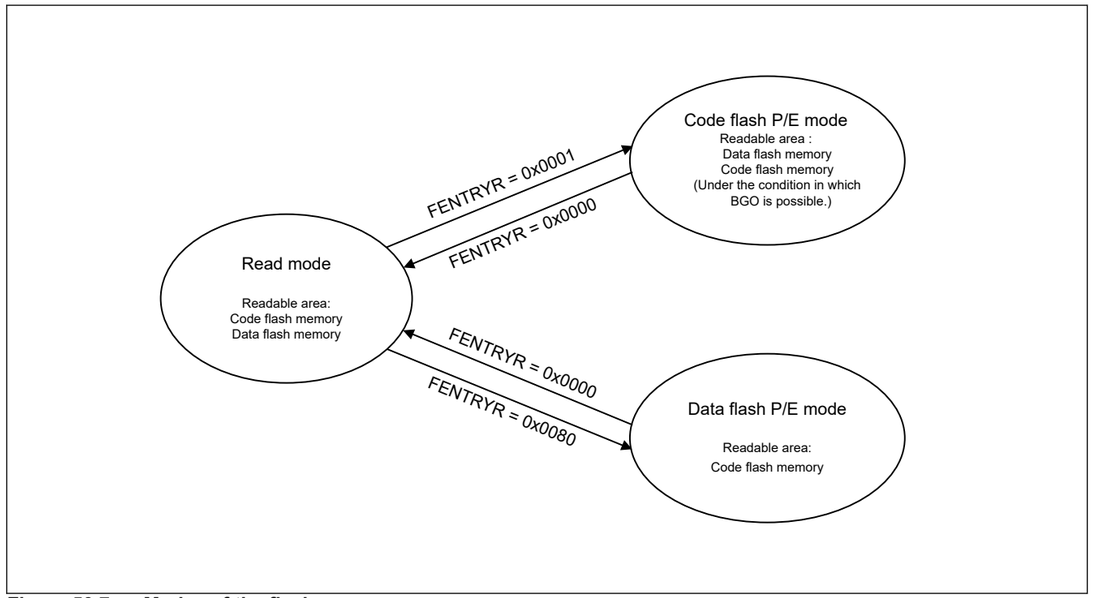

Figure 50.7 Modes of the flash sequencer

50.9 FACI Commands

50.9.1 List of FACI Commands

The FACI controls the FCU according to the specified FACI commands.

This section describes information about the FACI commands and Table 50.14 lists the FACI commands.

Table 50.14 FACI commands (1 of 2)

FACI command	Function
Program	Programs the user area and data area. Units of programming are 128 bytes for the user area and 4, 8, or 16 bytes for the data area.
Block erase	Erases user area and data area. The erase unit is 8 KB or 32 KB for user area, and 64 bytes for data flash.
Multi block erase	Erases data area. The erase unit is 64, 128, 256 bytes for data flash.
P/E suspend	Suspends programming or erasure processing.
P/E resume	Resumes suspended programming or erasure processing.
Status clear	Initializes the ILGLERR, ERSERR, PRGERR, ILGCOMERR, FESETERR, SECERR, and OTERR bits in the FSTATR register and the CMDLK, CFAE, and DFAE bits in the FASTAT register, and the flash sequencer released from command-locked state.
Forced stop	Forcibly stops processing of FACI commands and initializes the FSTATR and FASTAT registers.

当FENTRYR寄存器的值为0x0080时，闪存定序器处于数据闪存PE模式，可以通过FACI命令对数据闪存进行编程或擦除。在这种模式下，数据闪存是不可读的。但是，代码闪存是可读的。

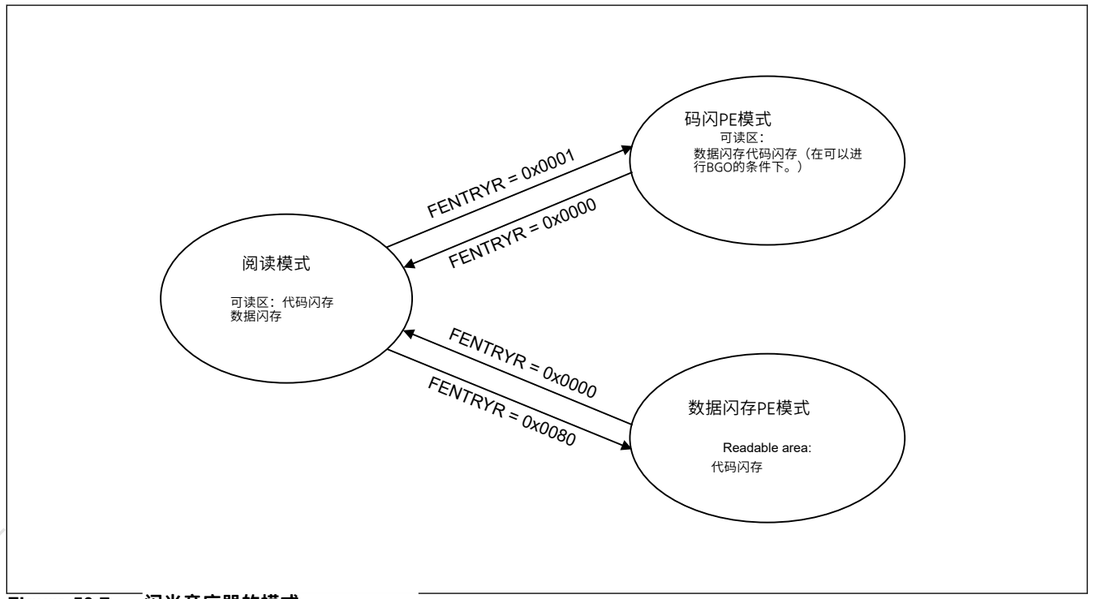

Figure 50.7 闪光音序器的模式

50.9 FACI命令

50.9.1 FACI命令列表

FACI根据指定的FACI命令控制FCU。

本节介绍有关FACI命令的信息，表50.14列出了FACI命令。

Table 50.14 FACI命令(1of2)

FACI命令	Function
Program	对用户区和数据区进行编程。 用户区的编程单元为128字节，数据区为4、8或16字节。
块擦除	擦除用户区和数据区。 用户区的擦除单元为8KB或32KB，数据闪存为64字节。
多块擦除	擦除数据区。 数据闪存的擦除单元为64、128、256字节。
P/E suspend	暂停编程或擦除处理。
P/E resume	恢复暂停的编程或擦除处理。
状态清除	Initializes the ILGLERR, ERSERR, PRGERR, ILGCOMERR, FSTATR寄存器中的FESETERR、SECERR和OTERR位以及FASTAT寄存器中的CMDLK、CFAE和DFAE位，并且闪存定序器从命令锁定状态释放。
强制停止	强制停止处理FACI命令并初始化 FSTATR和FASTAT寄存器。

Table 50.14 FACI commands (2 of 2)

FACI command	Function
Blank check	Checks if data areas are blank. Units of Blank Check: 4 bytes to data flash memory capacity (specified in 4-byte units).
Configuration set	Sets the option-setting memory. Units of setting: 16 bytes.

The FACI commands are issued by writing to the FACI command-issuing area (see Table 50.4). When write access as shown in Table 50.15 proceeds in the specified state, the flash sequencer executes the processing associated with the given command (see section 50.9.2. Relationship between the Flash Sequencer State and FACI Commands).

Table 50.15 FACI command formats

FACI commands	Number of write access	Write data to the FACI command-issuing area			
		1st access	2nd access	3rd to (N+2)th access	(N+3)th access
Program (user area) N = 64	67	0xE8	0x40 (=N)	WD1 to WD64	0xD0
Program (data area) 4-byte programming: N = 2 8-byte programming: N = 4 16-byte programming: N = 8	N+3	0xE8	0x02 (=N) 0x04 (=N) 0x08 (=N)	WD1 to WDN	0xD0
Block Erase (user area 8K/32K Bytes)	2	0x20	0xD0	—	—
Block Erase (data area 64 bytes)	2	0x20	0xD0	—	—
Multi block erase (data area 64/128/256 bytes)	2	0x21	0xD0	—	—
P/E suspend	1	0xB0	—	—	—
P/E resume	1	0xD0	—	—	—
Status Clear	1	0x50	—	—	—
Forced Stop	1	0xB3	—	—	—
Blank Check	2	0x71	0xD0	—	—
Configuration set N = 8	11	0x40	0x08 (=N)	WD1 to WD8	0xD0

Note: WDN (N = 1, 2, …): Nth 16-bit data to be programmed.

The flash sequencer clears the FSTATR.FRDY bit to 0 at the start of a command processing other than the Status Clear command, and sets this bit to 1 on completion.

If the FRDYIE.FRDYIE bit setting is 1, a flash ready (FRDY) interrupt is generated when the FSTATR.FRDY bit is set to 1.

50.9.2 Relationship between the Flash Sequencer State and FACI Commands

The FACI commands are accepted according to the mode/state of the flash sequencer. FACI commands should be issued after transitioning of the flash sequencer to the code flash P/E mode or data flash P/E mode and after checking the state of the flash sequencer.

Use the FSTATR and FASTAT registers to check the state of the flash sequencer. In addition, the occurrence of errors in general can be checked by reading the CMDLK bit in the FASTAT register. The value of the CMDLK bit is the logical OR of the following bits in the FSTATR register:

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR

Table 50.14 FACI命令（2个中的2个）

FACI命令	Function
空白支票	检查数据区域是否为空白。 空白检查单位：4字节到数据闪存容量（以4字节为单位指定）。
配置集	设置选项设置内存。 设置单位：16字节。

FACI命令通过写入FACI命令发布区域来发布（参见表50.4）。当如表50.15所示的写访问在指定状态下进行时，闪存定序器执行与给定命令相关的处理（请参阅第50.9.2节。闪存定序器状态和FACI命令之间的关系）。

Table 50.15 FACI命令格式

FACI命令	写访问次数	将数据写入FACI命令发布区			
		1st access	2nd access	第3次到第(N+2)次访问	(N+3)th access
Program (user area) N = 64	67	0xE8	0x40 (=N)	WD1 to WD64	0xD0
Program (data area) 4-byte programming: N = 2 8-byte programming: N = 4 16-byte programming: N = 8	N+3	0xE8	0x02 (=N) 0x04 (=N) 0x08 (=N)	WD1 to WDN	0xD0
块擦除（用户区8K32K字节）	2	0x20	0xD0	—	—
块擦除（数据区64字节）	2	0x20	0xD0	—	—
多块擦除（数据区64128256字节）	2	0x21	0xD0	—	—
P/E suspend	1	0xB0	—	—	—
P/E resume	1	0xD0	—	—	—
状态清除	1	0x50	—	—	—
强制停止	1	0xB3	—	—	—
空白支票	2	0x71	0xD0	—	—
配置集 N = 8	11	0x40	0x08 (=N)	WD1 to WD8	0xD0

Note: WDN(N=1 2 …)：要编程的第N个16位数据。

闪存定序器在除状态清除命令之外的命令处理开始时将FSTATR.FRDY位清除为0，并在完成时将此位设置为1。

如果FRDYIE.FRDYIE位设置为1，则当FSTATR.FRDY位设置为1时会产生闪存就绪(FRDY)中断。

50.9.2 FlashSequencerState和FACI命令之间的关系

根据闪存定序器的模式状态接受FACI命令。FACI命令应在闪存定序器转换到代码闪存PE模式或数据闪存PE模式并检查闪存定序器的状态之后发出。

使用FSTATR和FASTAT寄存器检查闪存序列器的状态。此外，一般可以通过读取FASTAT寄存器中的CMDLK位来检查错误的发生。CMDLK位的值是FSTATR寄存器中以下位的逻辑或：

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR

RA生态工作室

- OTERR
- ERSERR
- PRGERR
- FLWEERR.

Table 50.16 lists the available FACI commands in each operating mode.

Table 50.16 Operating mode and available FACI commands

Operating mode	FENTRYR	Available FACI commands
Read mode	0x0000	None
Code flash P/E mode	0x0001	Program Block erase P/E suspend P/E resume Status Clear Forced Stop Configuration set
Data flash P/E mode	0x0080	Program Block erase Multi block erase P/E suspend P/E resume Status Clear Forced Stop Blank Check

Table 50.17 shows the state of the flash sequencer and acceptable FACI commands. An appropriate mode is assumed to have been set before the commands are executed.

Table 50.17 Acceptable FACI commands and state of the flash sequencer (1 of 2)

	Program, block erase or multi block erase command processing	Configuration set command processing	Program, block erase or multi block erase command suspension processing	Blank check command processing	Programming suspended	Erasure suspended	Programming while erasure is suspended	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	Processing of forced stop command	Other state
FRDY bit	0	0	0	0	1	1	0	1	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD bit	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK bit	0	0	0	0	0	0	0	1	1	0	0
Program	X	X*4	X	X	X	O*3	X	X	X	X	O
Block erase or multi block erase	X	X*4	X	X	X	X	X	X	X	X	O
P/E suspend	O	X*4	X	X	X	X	X	—	X	X	—

- OTERR
- ERSERR
- PRGERR
- FLWEERR.

表50.16列出了每种操作模式下可用的FACI命令。

Table 50.16 操作模式和可用的FACI命令

操作模式	FENTRYR	可用的FACI命令
阅读模式	0x0000	None
码闪PE模式	0x0001	Program 块擦除PE暂 停PE恢复状 态清除强制 停止 配置集
数据闪存PE模式	0x0080	Program 块擦除多块擦除 PE暂停PE恢 复状态清除 强制停止空 白检查

表50.17显示了闪存定序器的状态和可接受的FACI命令。假设在执行命令之前已经设置了适当的模式。

Table 50.17 可接受的FACI命令和闪存定序器的状态(1of2)

	编程、块擦除或多块擦除命令处理	配置集命令处理	编程、命令暂停处理块擦除或多块擦除	空白检查命令处理	编程暂停	擦除暂停	擦除暂停时编程	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	强制停止指令的处理	其他状态
FRDY bit	0	0	0	0	1	1	0	1	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD bit	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK bit	0	0	0	0	0	0	0	1	1	0	0
Program	X	X*4	X	X	X	O*3	X	X	X	X	O
块擦除或多块擦除	X	X*4	X	X	X	X	X	X	X	X	O
P/E suspend	O	X*4	X	X	X	X	X	—	X	X	—

Table 50.17 Acceptable FACI commands and state of the flash sequencer (2 of 2)

	Program, block erase or multi block erase command processing	Configuration set command processing	Program, block erase or multi block erase command suspension processing	Blank check command processing	Programming suspended	Erasure suspended	Programming while erasure is suspended	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	Processing of forced stop command	Other state
P/E resume	X	X*4	X	X	O	O	X	X	X	X	X
Status clear	X	X*4	X	X	O	O	X	O	X	X	O
Forced stop	O	O*4	O	O	O	O	O	O	O	O	O
Blank check	X	X*4	X	X	O*1	O*1	X	X	X	X	O*1
Configuration set	X	X*4	X	X	X	X	X	X	X	X	O*2

Note: O: Acceptable
X: Not acceptable (places the sequencer in the command-locked state)
—: Ignored
Note 1. Only acceptable in data flash P/E mode.
Note 2. Only acceptable in code flash P/E mode
Note 3. Acceptable when programming area is other than erase suspending block.
Note 4. When configuration set is processing and when FSTATR.DBFULL bit is 1, do not issue this command.

50.9.3 Usage of FACI Commands

50.9.3.1 Overview of Command Usage in Code Flash P/E Mode

Figure 50.8 show an overview of FACI command usage in code flash P/E mode. For the available commands in code flash P/E mode, see Table 50.16.

Table 50.17 可接受的FACI命令和闪存定序器的状态（2个中的2个）

	编程、块擦除或多块擦除命令处理	配置集命令处理	编程、块擦除或多块擦除命令暂停处理	空白检查命令处理	编程暂停	擦除暂停	擦除暂停时编程	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	强制停止指令的处理	其他状态
P/E resume	X	X*4	X	X	O	O	X	X	X	X	X
状态清除	X	X*4	X	X	O	O	X	O	X	X	O
强制停止	O	O*4	O	O	O	O	O	O	O	O	O
空白支票	X	X*4	X	X	O*1	O*1	X	X	X	X	O*1
配置集	X	X*4	X	X	X	X	X	X	X	X	O*2

Note: O: Acceptable
X：不可接受（将定序器置于命令锁定状态）—：忽略
注1.仅在数据闪存PE模式下可接受。注2.仅在代码
闪存PE模式下可接受
注3.当编程区域不是擦除暂停块时可接受。
注4.当配置集正在处理并且FSTATR.DBFULL位为1时，不要发出此命令。

50.9.3 FACI命令的使用

50.9.3.1 CodeFlashPE模式中的命令使用概述

图50.8显示了代码闪存PE模式下的FACI命令使用概览。对于代码闪存中的可用命令PE模式，见表50.16。

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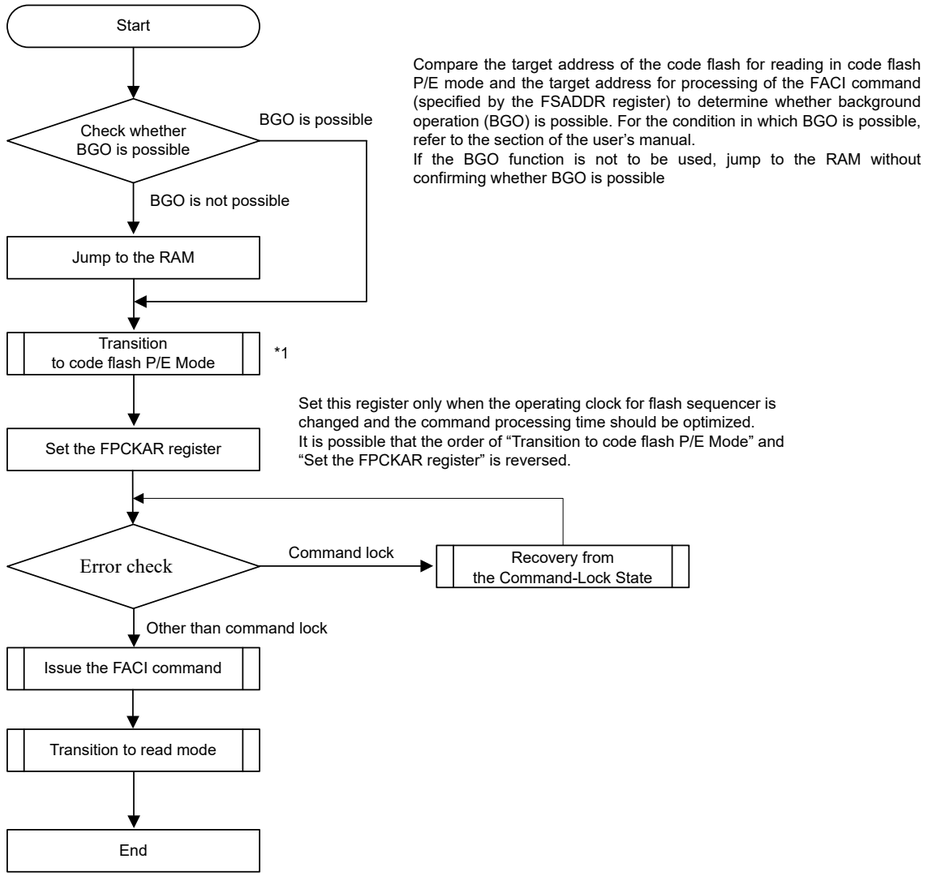
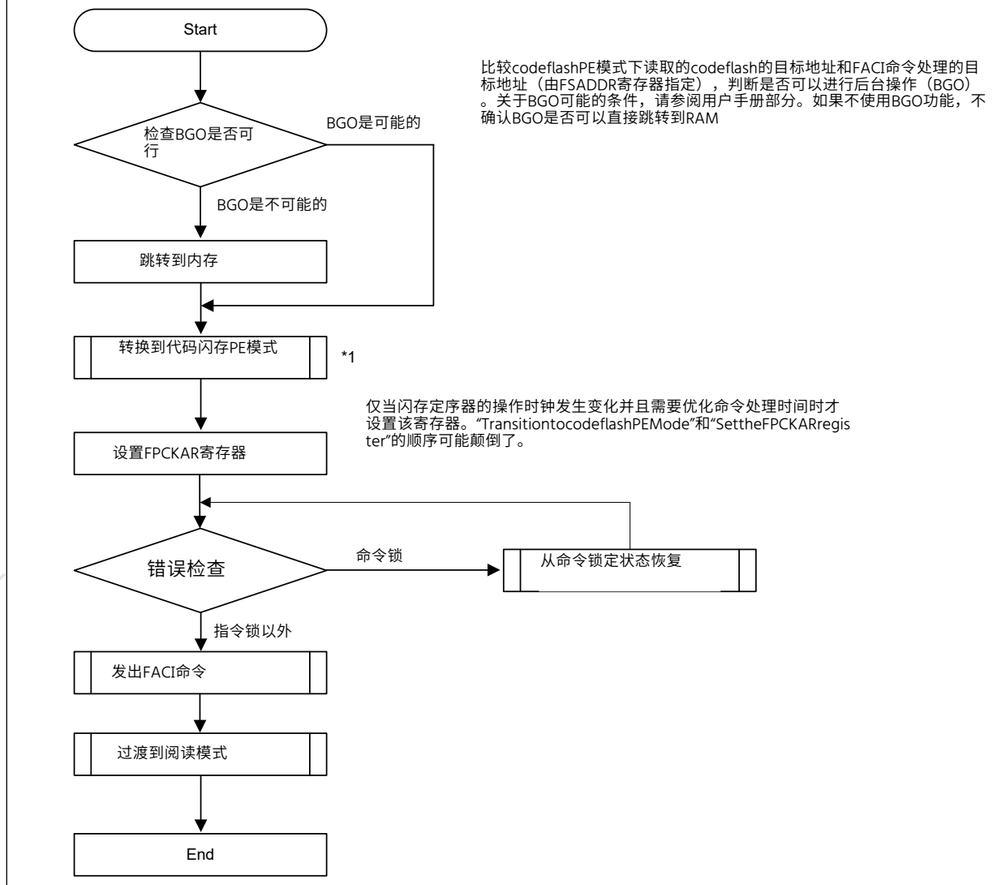


Note 1. See section 50.9.3.3. Transition to Code Flash P/E Mode

Figure 50.8 Overview of command usage in code flash P/E mode

50.9.3.2 Overview of Command Usage in Data Flash P/E Mode

Figure 50.9 shows an overview of FACI command usage in data flash P/E and Table 50.16 lists the available commands in data flash P/E mode.



注1.见第50.9.3.3节。转换到CodeFlashPE模式

Figure 50.8 CodeflashPE模式下的命令使用概述

50.9.3.2 DataFlashPE模式下的命令使用概述

图50.9显示了数据闪存PE中FACI命令使用的概述，表50.16列出了数据闪存PE模式下的可用命令。

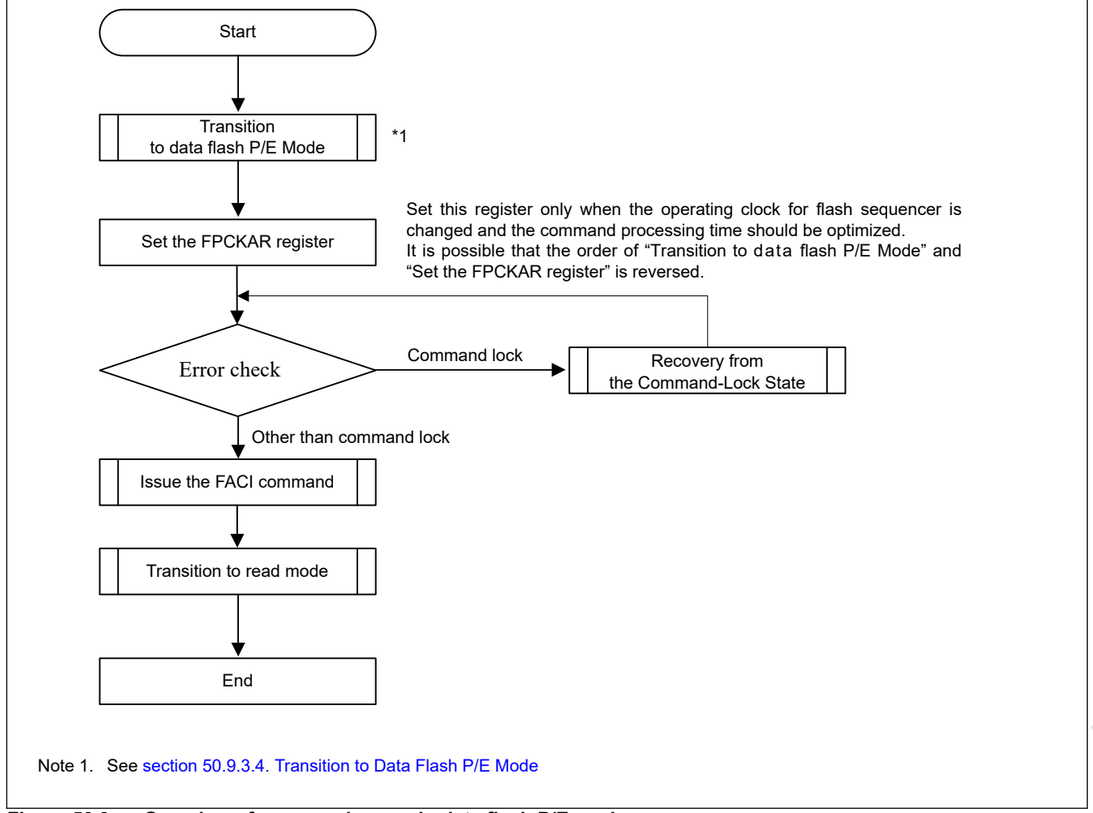


Figure 50.9 Overview of command usage in data flash P/E mode

50.9.3.3 Transition to Code Flash P/E Mode

To issue FACI commands for the code flash memory, a transition to code flash P/E mode is required by setting the FENTRYC bit in the FENTRYR register to 1.

Figure 50.10 shows the procedure to transition to code flash P/E mode.

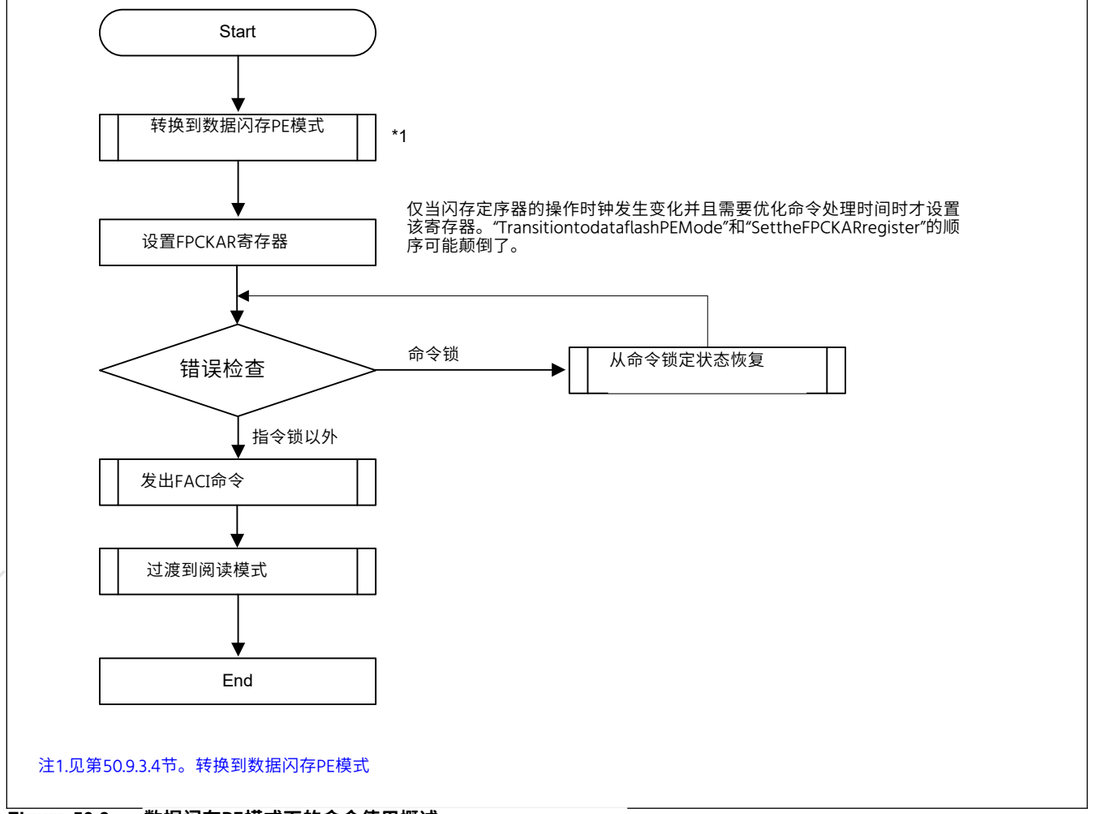


Figure 50.9 数据闪存PE模式下的命令使用概述

50.9.3.3 转换到CodeFlashPE模式

要为代码闪存发出FACI命令，需要通过设置FENTRYR寄存器中的FENTRYC位为1。

图50.10显示了转换到代码闪存PE模式的过程。

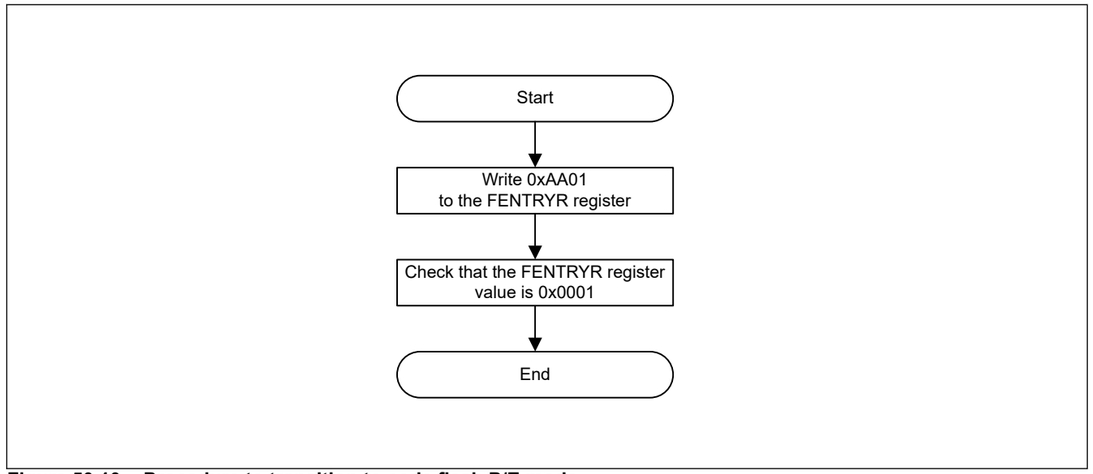


Figure 50.10 Procedure to transition to code flash P/E mode

50.9.3.4 Transition to Data Flash P/E Mode

To issue FACI commands for the data flash memory, a transition to data flash P/E mode is required by setting the FENTRYD bit in the FENTRYR register to 1.

Figure 50.11 shows the procedure to transition to data flash P/E mode.

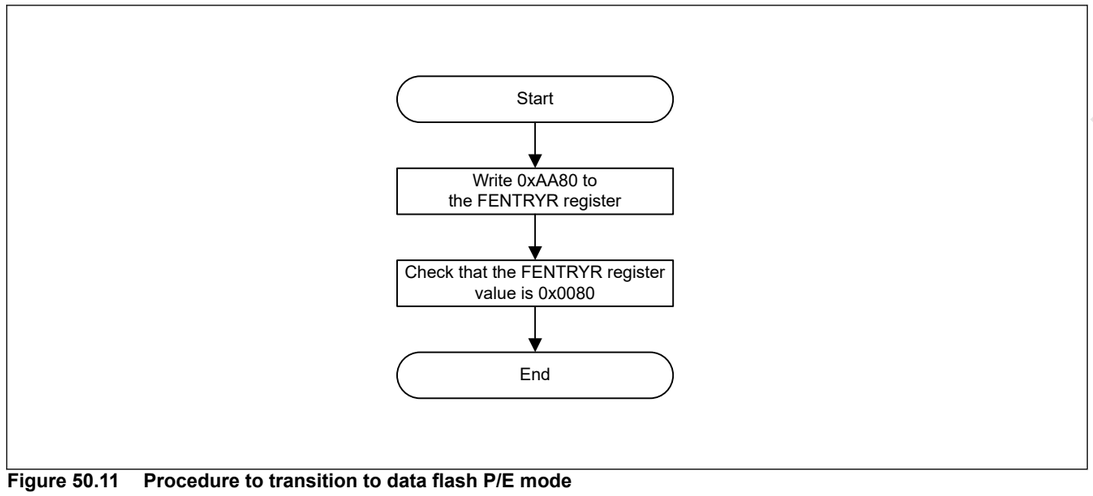


Figure 50.11 Procedure to transition to data flash P/E mode

50.9.3.5 Transition to Read Mode

To read the flash memory, a transition to read mode is required by setting the FENTRYR register to 0x0000. The transition to read mode should be made after the flash sequencer completes the processing and while operation is not in the command-locked state.

Figure 50.12 shows the procedure to transition to read mode.

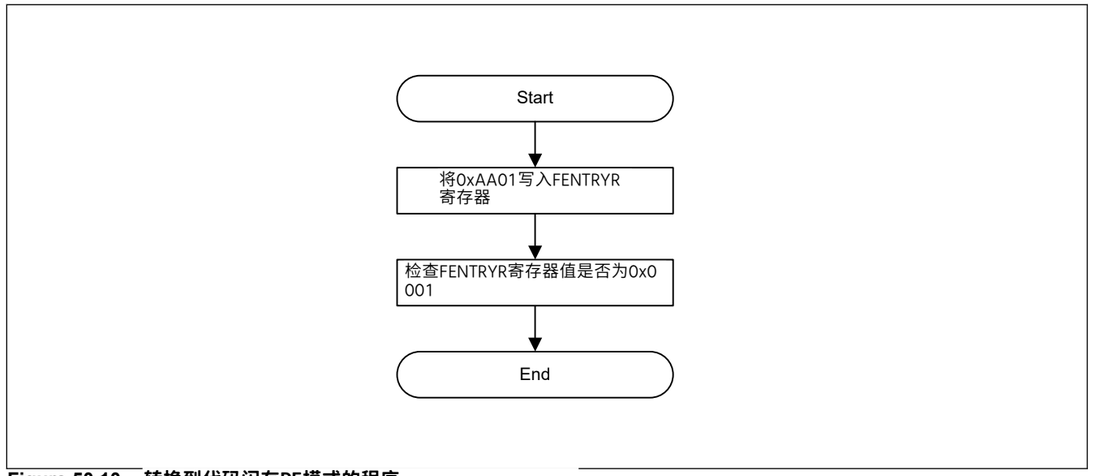


Figure 50.10 转换到代码闪存PE模式的程序

50.9.3.4 转换到数据闪存PE模式

要为数据闪存发出FACI命令，需要通过设置FENTRYR寄存器中的FENTRYD位为1。

图50.11显示了转换到数据闪存PE模式的过程。

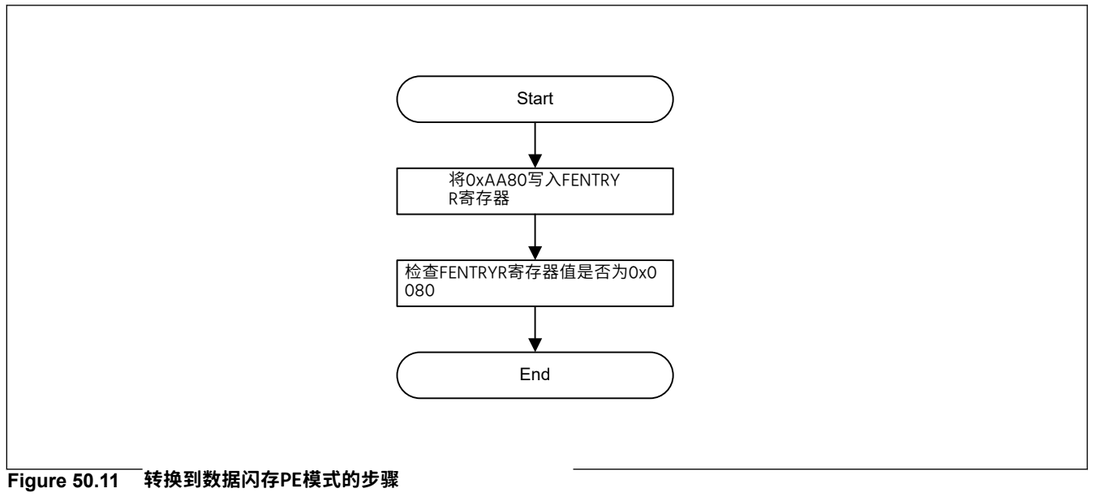
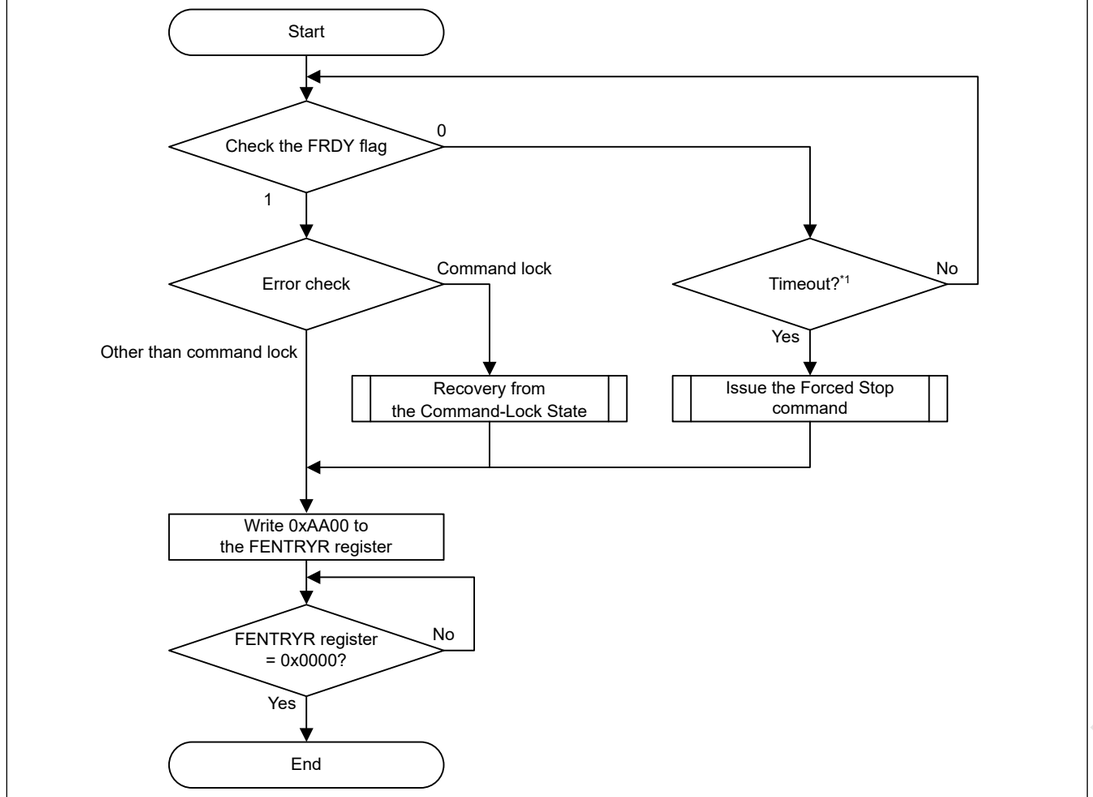


Figure 50.11 转换到数据闪存PE模式的步骤

50.9.3.5 过渡到阅读模式

要读取闪存，需要通过将FENTRYR寄存器设置为0x0000转换到读取模式。闪存定序器完成处理后且操作未处于命令锁定状态时，应转换到读取模式。

图50.12显示了转换到读取模式的过程。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 53, Electrical Characteristics)

Figure 50.12 Procedure to transition to read mode

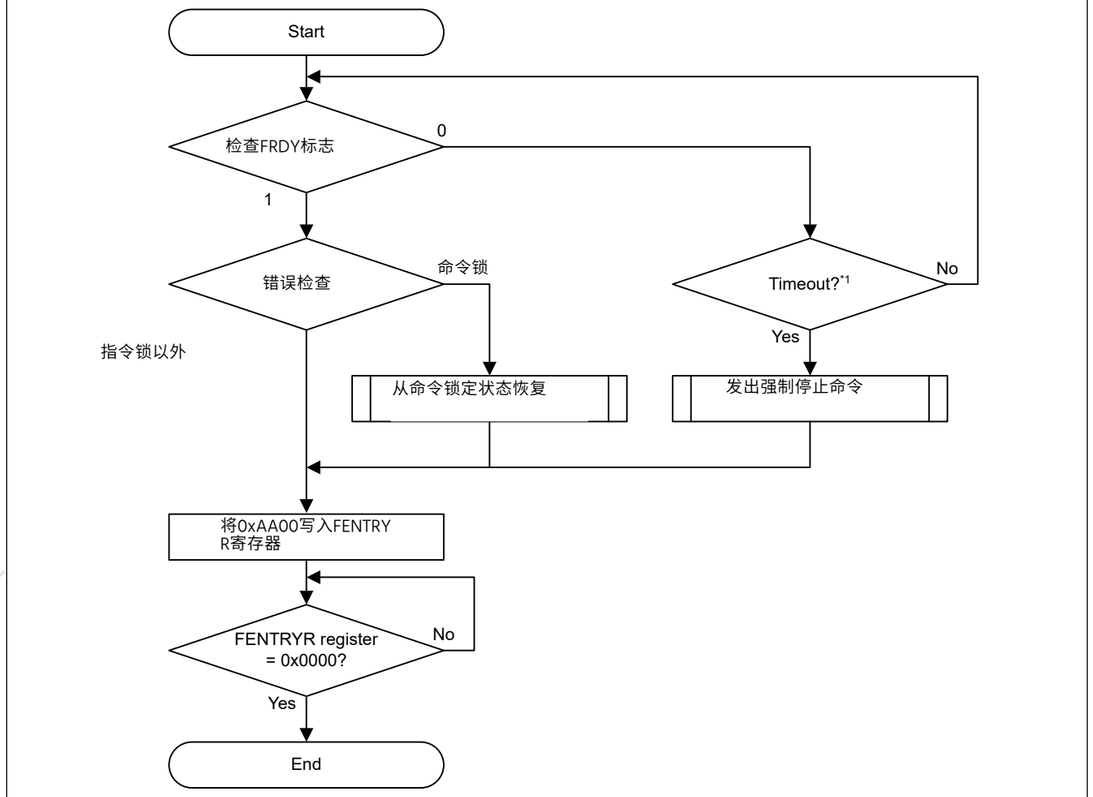
50.9.3.6 Recovery from the Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the sequencer from the command-locked state, use the status clear command, forced stop command, or FASTAT register.

When the command-locked state is detected by checking for an error before issuing the P/E suspend command, the FRDY bit in the FSTATR register might be 0 even though command processing has not completed. If processing is not complete by the maximum programming/erasure time specified in the electrical characteristics, this is a timeout and the flash sequencer must be stopped with the forced stop command.

The FLWEERR bit in the FSTATR register does not change from 1 to 0 with the status clear command. When these bits are set to 1, use the forced stop command to release from the command-locked state. Bits other than FRDY and FLWEERR in FSTATR register that indicate the command-locked state can be changed from 1 to 0 with the status clear or forced stop command.

Figure 50.13 shows the recovery flow from the command-locked state.



注1.超时的判断是基于1.1倍的FACI命令处理正在进行的最长时间（见第53节，电气特性）

Figure 50.12 转换到阅读模式的过程

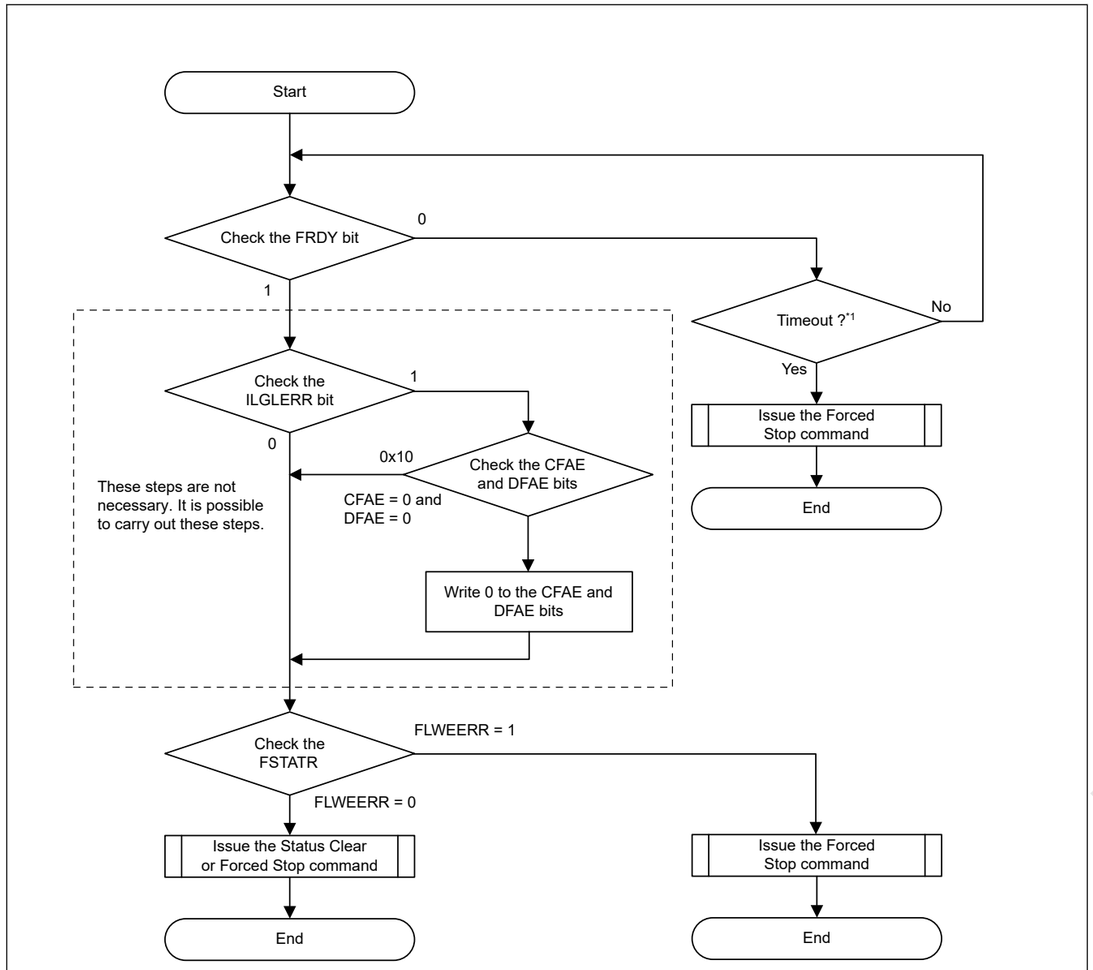
50.9.3.6 从命令锁定状态恢复

当闪存定序器进入命令锁定状态时，无法接受FACI命令。要从命令锁定状态释放定序器，请使用状态清除命令、强制停止命令或FASTAT寄存器。

当通过在发出PE挂起命令之前检查错误来检测命令锁定状态时，即使命令处理尚未完成，FSTATR寄存器中的FRDY位也可能为0。如果在电气特性中指定的最大编程擦除时间未完成处理，则这是一个超时，并且必须使用强制停止命令停止闪存定序器。

FSTATR寄存器中的FLWEERR位不会随着状态清除命令从1变为0。当这些位设置为1时，使用强制停止命令从命令锁定状态中释放。FSTATR寄存器中除FRDY和FLWEERR以外的位指示命令锁定状态可以通过状态清除或强制停止命令从1更改为0。

图50.13显示了从命令锁定状态的恢复流程。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (see section 53, Electrical Characteristics)

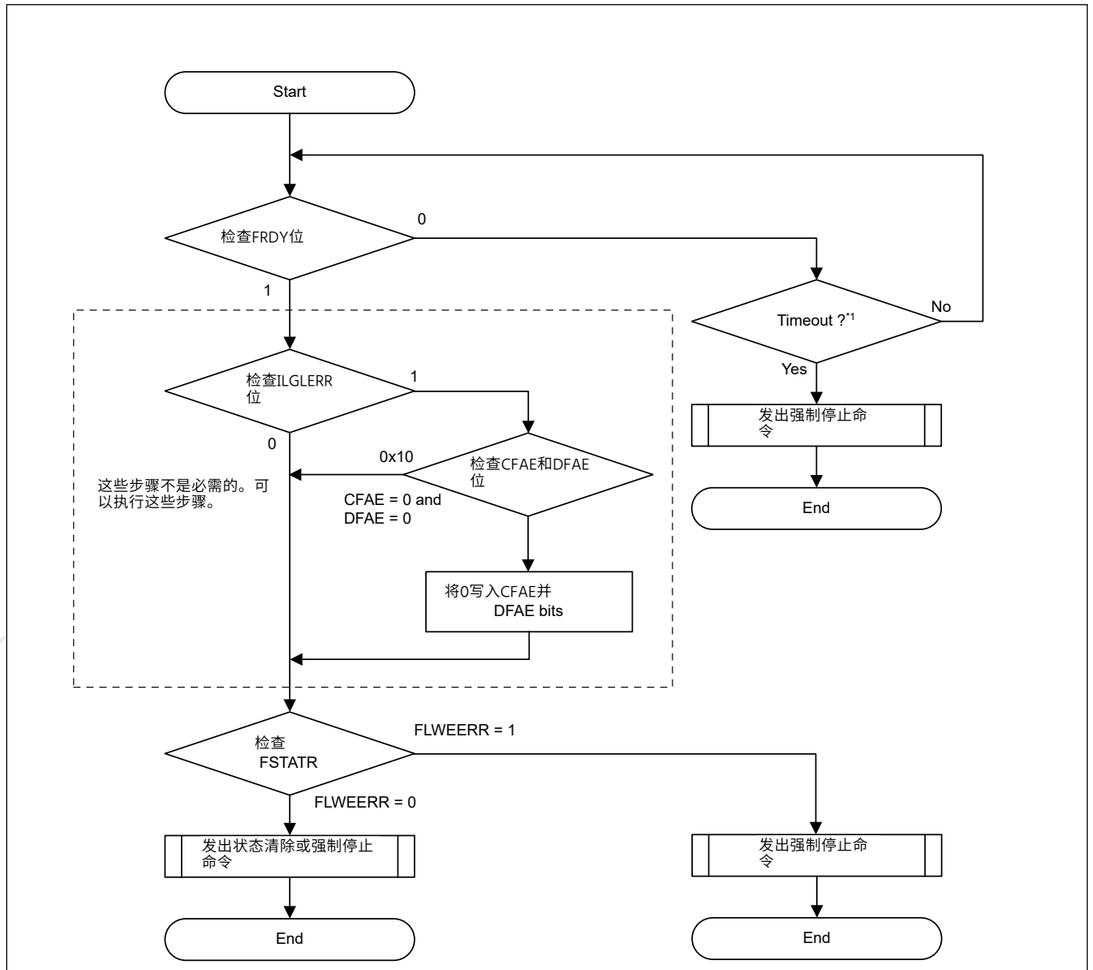
Figure 50.13 Recovery flow from the command-locked state

50.9.3.7 Program Command

The program command is used for writing to the user area and data area. Before issuing the FACI program command, set the first address of the target block in the FSADDR register. Writing 0xD0 at the final access of the FACI command-issuing area starts the program command processing. If the target area of program command processing contains area that are not for writing, write 0xFFFF to the corresponding area.

Issuing the program command while the FACI internal data buffer is full leads to a wait on the peripheral bus that might affect communications performance of other peripheral modules. To avoid a wait, set the DBFULL bit in the FSTATR register to 0 when issuing the FACI command. Writing to the data area does not lead to the data buffer becoming full.

Figure 50.14 shows the usage of the program command.



注1.超时的判断是基于1.1倍的FACI命令处理正在进行的最长时间（见第53节，电气特性）

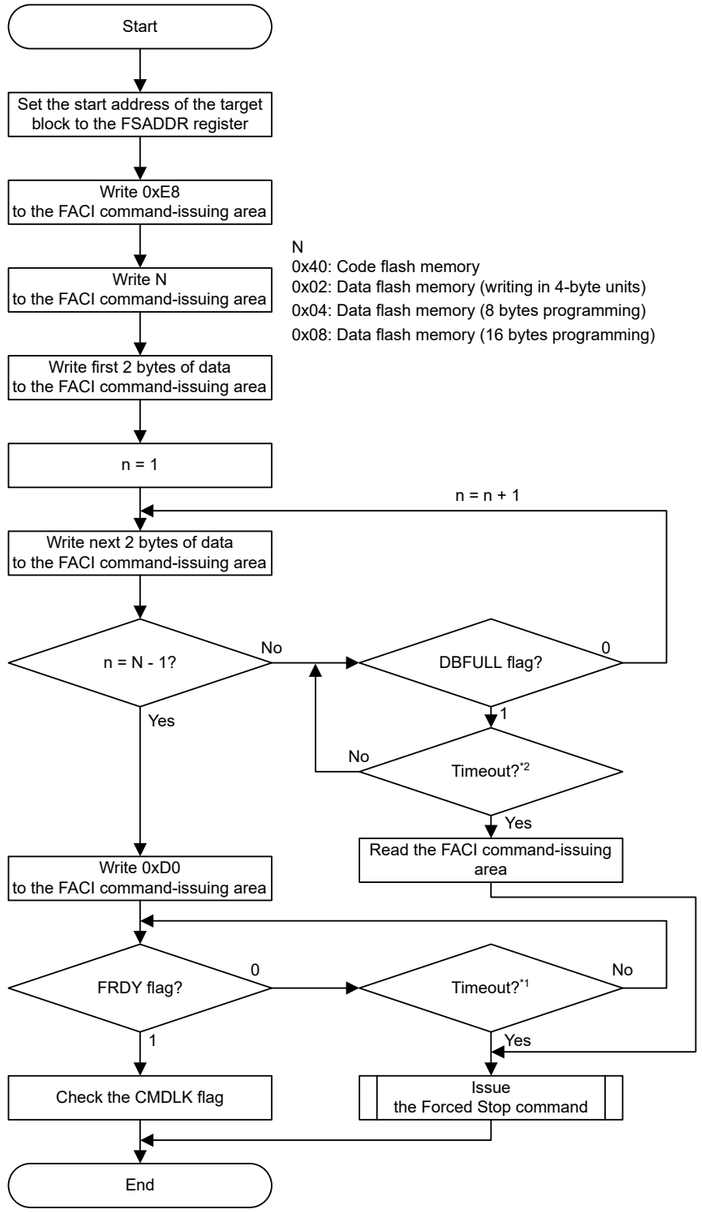
Figure 50.13 从命令锁定状态恢复流程

50.9.3.7 程序命令

程序命令用于写入用户区和数据区。在发出FACI程序命令之前，在FSADDR寄存器中设置目标块的首地址。在最终访问FACI命令发布区域时写入0xD0开始程序命令处理。如果程序命令处理的目标区域包含非写入区域，则将0xFFFF写入相应区域。

在FACI内部数据缓冲区已满时发出程序命令会导致外围总线等待，这可能会影响其他外围模块的通信性能。为避免等待，请在发出FACI命令时将FSTATR寄存器中的DBFULL位设置为0。写入数据区不会导致数据缓冲区变满。

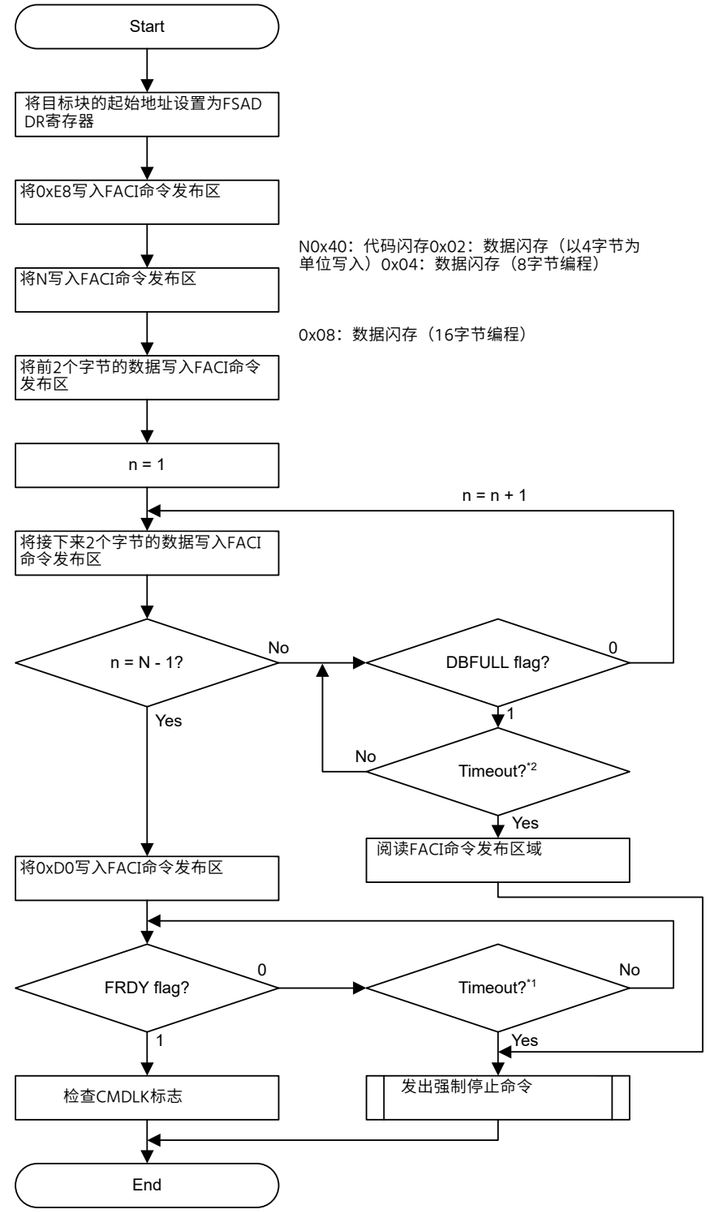
图50.14显示了程序命令的用法。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programming. See section 53, Electrical Characteristics about those time

Note 2. 1.4 µs (f_{FCLK} ≥ 20 MHz)

Figure 50.14 Usage flow of the program command



注1.超时的判断是基于最大编程时间的1.1倍。见第53节，电气那个时代的特征

Note 2. 1.4 µs (f_{FCLK} ≥ 20 MHz)

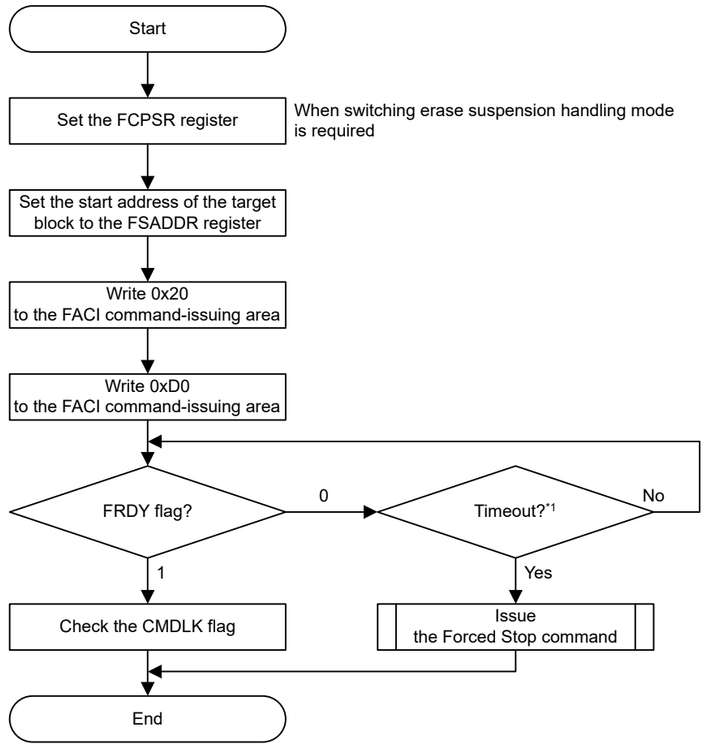
Figure 50.14 程序指令的使用流程

50.9.3.8 Block Erase Command

The block erase command is used for erasing user area or data area. The erase unit is one block. Before issuing a block erase command, set the first address of the target block to FSADRR register. Writing 0xD0 at the second write access of the FACI command triggers the FACI to start the block erase command processing. Completion of command processing can be confirmed with the FRDY bit of FSTATR register.

Set the FCPSR registers before issuing the block erase command. Additionally, FCPSR must be set when the erasure-suspended mode is to be switched.

Figure 50.15 shows the usage of the block erase command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of erasure. See section 53, Electrical Characteristics.

Figure 50.15 Usage flow of the block erase command

50.9.3.9 Multi Block Erase Command

The multi block erase command is used for erasing data area. The erase unit is 64, 128, or 256 bytes. Before issuing the multi block erase command, set the start address to FSADRR register and the end address to FEADDR register. Writing 0xD0 at the second write access of the FACI command triggers FACI to start the multi block erase command processing. Completion of command processing can be confirmed with the FRDY bit of FSTATR register.

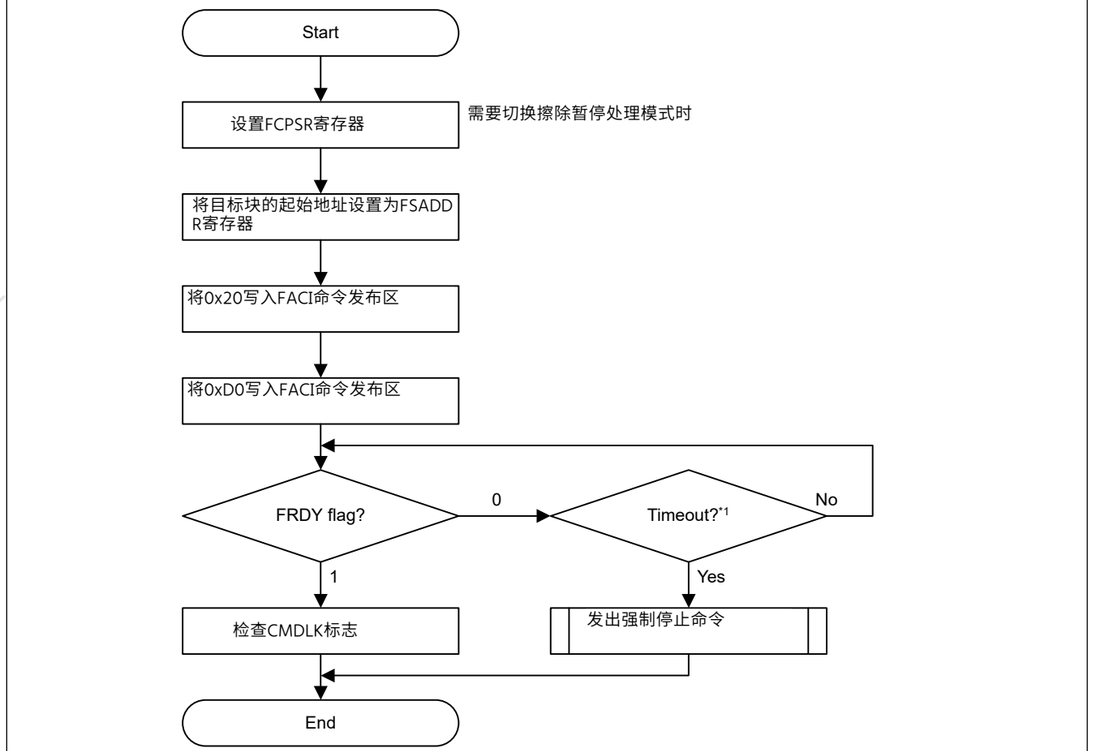
Set the FCPSR registers before issuing the multi block erase command. Additionally, FCPSR must be set when the erasure-suspended mode is to be switched.

50.9.3.8 块擦除命令

块擦除命令用于擦除用户区或数据区。擦除单位是一个块。在发出块擦除命令之前，将目标块的首地址设置为FSADRR寄存器。在FACI命令的第二次写访问时写入0xD0会触发FACI开始块擦除命令处理。命令处理的完成可以通过FSTATR寄存器的FRDY位来确认。

在发出块擦除命令之前设置FCPSR寄存器。此外，当要切换擦除暂停模式时，必须设置FCPSR。

图50.15显示了块擦除命令的用法。



注1.超时的判断是基于最大擦除时间的1.1倍。
参见第53节，电气特性。

Figure 50.15 块擦除命令的使用流程

50.9.3.9 多块擦除命令

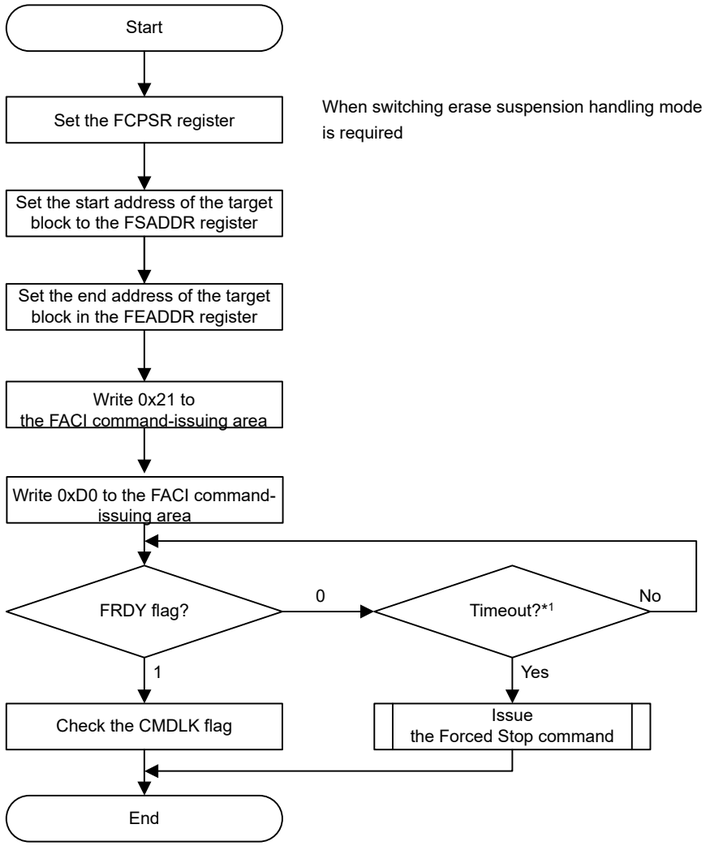
多块擦除命令用于擦除数据区域。擦除单元为64、128或256字节。在发出多块擦除命令之前，将起始地址设置为FSADRR寄存器，将结束地址设置为FEADDR寄存器。在FACI命令的第二次写访问时写入0xD0会触发FACI开始多块擦除命令处理。命令处理的完成可以通过FSTATR寄存器的FRDY位来确认。

在发出多块擦除命令之前设置FCPSR寄存器。此外，当要切换擦除暂停模式时，必须设置FCPSR。

The erase size is specified by both the FSADDR and FEADDR settings. Table 50.18 describes how to set the FSADDR and FEADDR.

Table 50.18 Settings for the erase size

Erase size	FSADDR	FEADDR
64 bytes	FSA0 to FSA5 = 0 (64 byte-boundary)	FSADDR + 0x3C
128 bytes	FSA0 to FSA6 = 0 (128 byte-boundary)	FSADDR + 0x7C
256 bytes	FSA0 to FSA7 = 0 (256 byte-boundary)	FSADDR + 0xFC



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of erasure. See section 53, Electrical Characteristics.

Figure 50.16 Usage flow of the multi block command

50.9.3.10 P/E Suspend Command

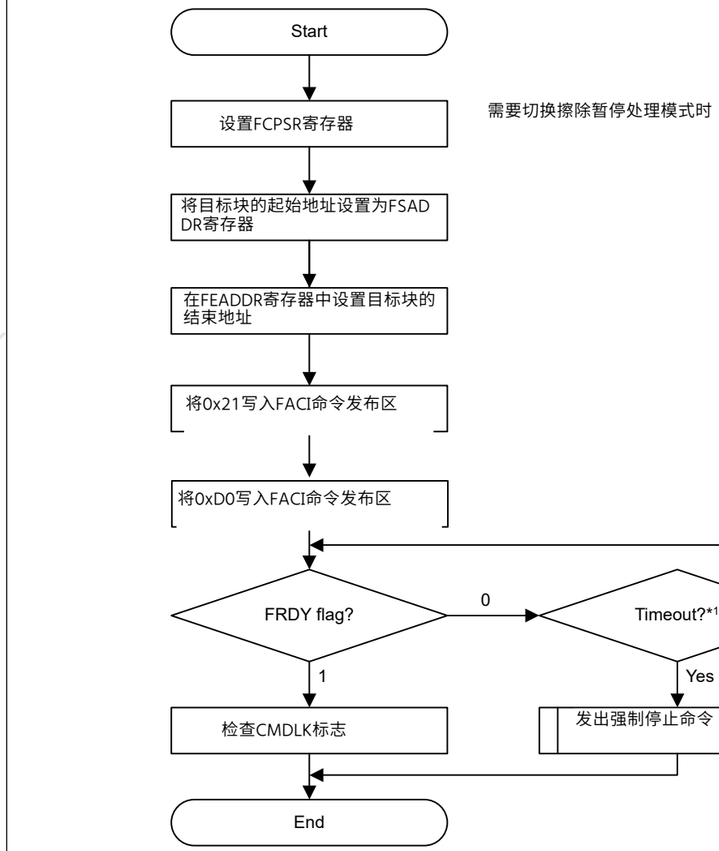
The P/E suspend command is used to suspend programming/erasure. Before issuing a P/E suspend command, check that the CMDLK bit in the FASTAT register is 0, and that the execution of programming/erasure is performed normally. To confirm that the P/E suspend command can be received, check that the SUSRDY bit in the FSTATR register is 1. After issuing a P/E suspend command, read the CMDLK bit to confirm that no error occurs.

If an error occurs during programming/erasure, the CMDLK bit is set to 1. When programming/erasure processing has finished from the time when the SUSRDY bit is 1 to when the P/E suspend command is received, no error occurs and the

擦除大小由FSADDR和FEADDR设置指定。表50.18描述了如何设置FSADDR和FEADDR.

Table 50.18 擦除大小的设置

擦除大小	FSADDR	FEADDR
64 bytes	FSA0 to FSA5 = 0 (64 byte-boundary)	FSADDR + 0x3C
128 bytes	FSA0 to FSA6 = 0 (128 byte-boundary)	FSADDR + 0x7C
256 bytes	FSA0 to FSA7 = 0 (256 byte-boundary)	FSADDR + 0xFC



注1.超时的判断是基于最大擦除时间的1.1倍。
参见第53节，电气特性。

Figure 50.16 多块命令的使用流程

50.9.3.10 PE挂起命令

PE暂停命令用于暂停编程擦除。在发出PE挂起命令之前，请检查FASTAT寄存器中的CMDLK位是否为0，并且编程擦除的执行是否正常执行。要确认可以接收到PE挂起命令，请检查FSTATR寄存器中的SUSRDY位是否为1。发出PE挂起命令后，读取CMDLK位以确认没有错误发生。

如果在编程擦除过程中发生错误，则将CMDLK位设置为1。从SUSRDY位为1到接收到PE暂停命令时，当编程擦除处理完成时，不会发生错误，并且

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suspended state is not entered (the FRDY bit in the FSTATR register is 1 and the ERSSPD and PRGSPD bits in FSTATR are 0).

When a P/E suspend command is received and the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FRDY bit is set to 1, and the ERSSPD or PRGSPD bit is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD bit is 1 and the suspended state is entered, then proceed with the subsequent flow. If a P/E resume command is issued in the subsequent flow even when the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state (see section 50.11.2. Error Protection).

If the erasure suspended state is entered, programming to blocks other than an erasure target block can be performed. Additionally, the programming and erasure suspended states can shift to read mode by clearing the FENTRYR register.

Figure 50.17 shows the usage of the P/E suspend command.

未进入挂起状态（FSTATR寄存器中的FRDY位为1，FSTATR中的ERSSPD和PRGSPD位为0）。

当接收到PE挂起命令并且编程擦除挂起处理正常完成时，闪存定序器进入挂起状态，FRDY位设置为1，ERSPD或PRGSPD位为1。发出PE挂起命令后，检查是否ERSSPD或PRGSPD位为1，进入挂起状态，然后进行后续流程。如果即使在未进入挂起状态的情况下在后续流程中发出PEresume命令，也会发生非法命令错误，并且闪存定序器会切换到命令锁定状态（请参阅第50.11.2节。错误保护）。

如果进入擦除暂停状态，则可以执行对擦除目标块以外的块的编程。
此外，通过清除FENTRYR寄存器，编程和擦除暂停状态可以转换为读取模式。

图50.17显示了PE挂起命令的用法。

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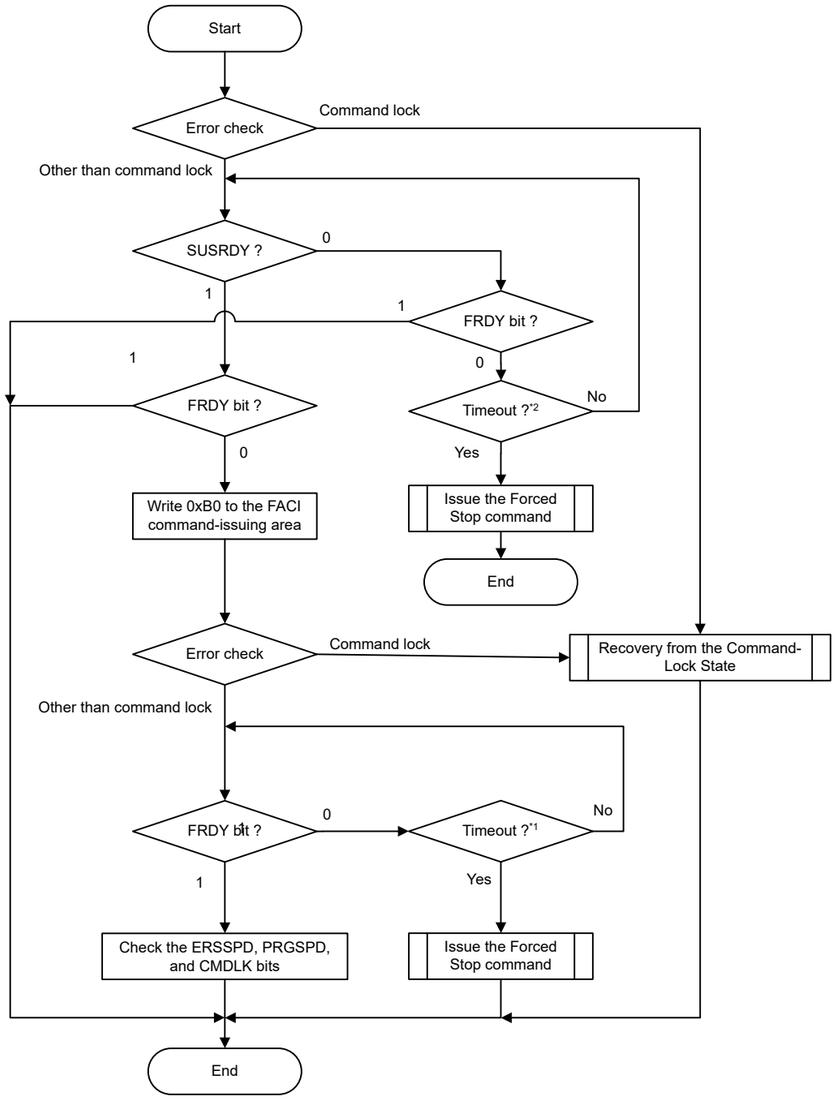
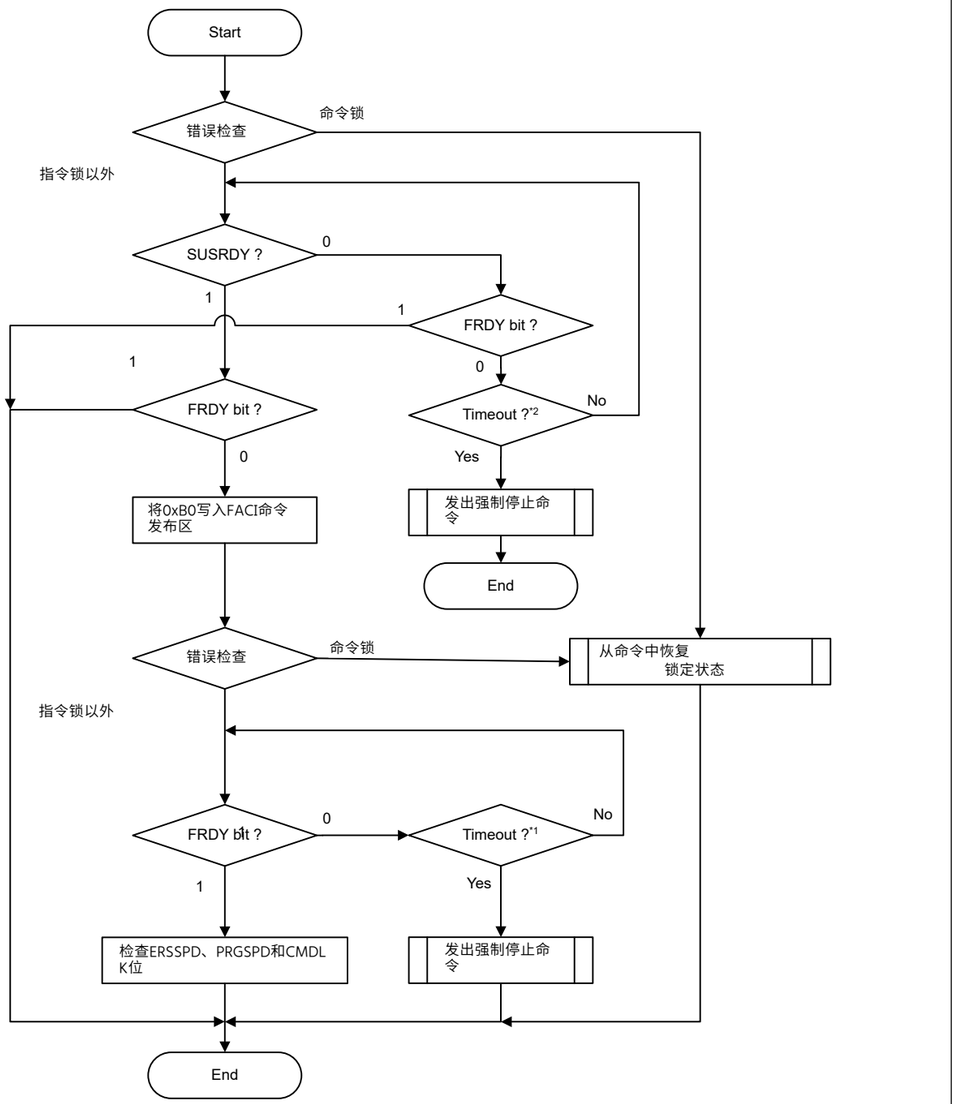


Note 1. Judgment of the timeout is based on 1.1 times the maximum time of suspend delay during erasure for both code flash and data flash.
See section 53, Electrical Characteristics.
Note 2. 4.4µs (f_{FCLK} >= 20MHz)

Figure 50.17 Usage flow of the P/E suspend command

(1) Suspension during Programming

When issuing a P/E suspend command during flash memory programming, the flash sequencer suspends programming processing. Figure 50.18 shows the suspend programming operation. When receiving programming-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start programming. If the flash sequencer enters the state



注1.超时的判断是基于1.1倍的擦除期间挂起延迟最大时间的代码闪存和数据闪存。参见第53节，电气特性。

Note 2. 4.4µs (f_{FCLK} >= 20MHz)

Figure 50.17 PE挂起命令的使用流程

(1) 编程期间暂停

在闪存编程期间发出PE暂停命令时，闪存定序器暂停编程处理。图50.18显示了挂起编程操作。当接收到编程相关命令时，flashsequencer将FSTATR寄存器中的FRDY位清0以开始编程。如果闪存定序器进入状态

in which the P/E suspend command can be received after programming starts, it sets the SUSRDY bit in the FSTATR register to 1.

When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0. If the flash sequencer receives a P/E suspend command while a programming pulse is applied, the flash sequencer continues with the pulse. After the specified pulse application time, the flash sequencer finishes pulse application, starts the programming suspend processing, and sets the PRGSPD bit in the FSTATR register to 1.

When a suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the flash sequencer clears the FRDY and PRGSPD bits to 0 and resumes programming.

Figure 50.18 shows the timing for suspension during programming.

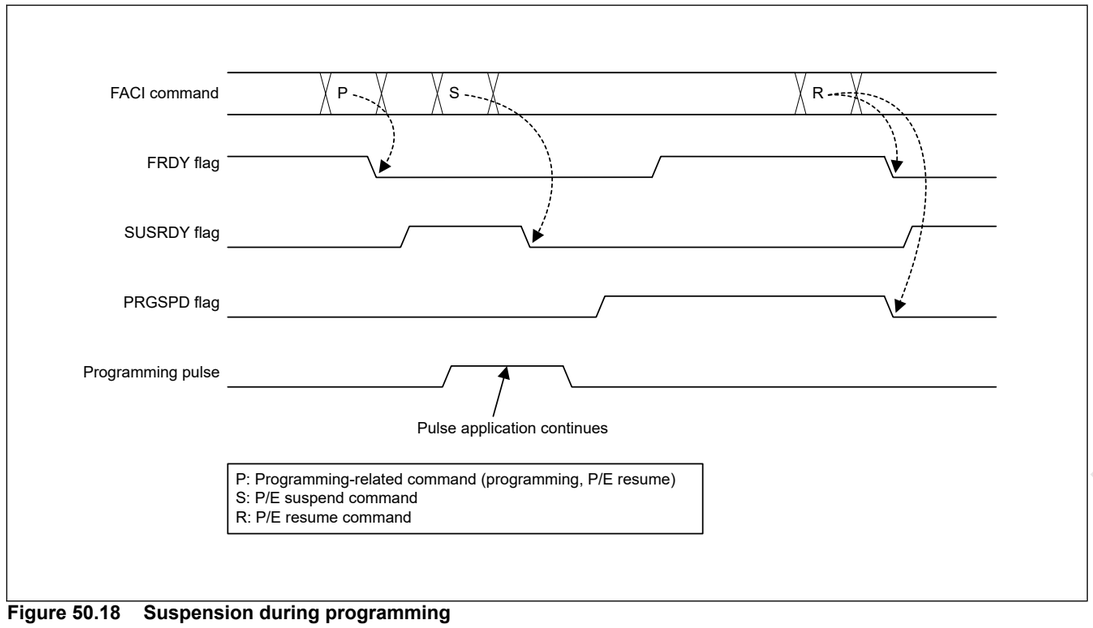


Figure 50.18 Suspension during programming

(2) Suspension during Erasure (Suspension Priority Mode)

The flash sequencer has a suspension priority mode for the suspension of erasure. Figure 50.19 shows the suspend operation of erasure when the erasure suspend mode is set to the suspension priority mode (the ESUSPMD bit in the FCPSR register is 0).

When receiving an erasure-related command, the flash sequencer clears the FRDY bit in the FSTATR register to 0 to start erasure. If the flash sequencer enters the state in which the P/E suspend command can be received after erasure starts, it sets the SUSRDY bit in the FSTATR register to 1.

When a P/E suspend command is issued, the flash sequencer receives the command and clears the SUSRDY bit to 0.

When receiving a suspend command during erasure, the flash sequencer starts the suspend processing and sets the ERSSPD bit in the FSTATR register to 1 even when it is applying an erasure pulse. When the suspended processing finishes, the flash sequencer sets the FRDY bit to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the flash sequencer clears the FRDY and ERSSPD bits to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD bits at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.

The setting of the erasure suspend mode affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has not been previously suspended is being applied, the flash sequencer suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed with a P/E resume command, the flash sequencer

在编程开始后可以接收PE挂起命令的情况下，它将FSTATR寄存器中的SUSRDY位设置为1。

当发出PE暂停命令时，闪存定序器接收该命令并将SUSRDY位清除为0。如果在施加编程脉冲时闪存定序器接收到PE暂停命令，则闪存定序器继续执行该脉冲。在指定的脉冲施加时间之后，闪存序列器完成脉冲施加，开始编程暂停处理，并将FSTATR寄存器中的PRGSPD位设置为1。

当暂停处理完成时，闪存定序器将FRDY位设置为1以进入编程暂停状态。当在编程暂停状态下接收到PEresume命令时，闪存定序器将FRDY和PRGSPD位清除为0并恢复编程。

图50.18显示了编程期间暂停的时序。

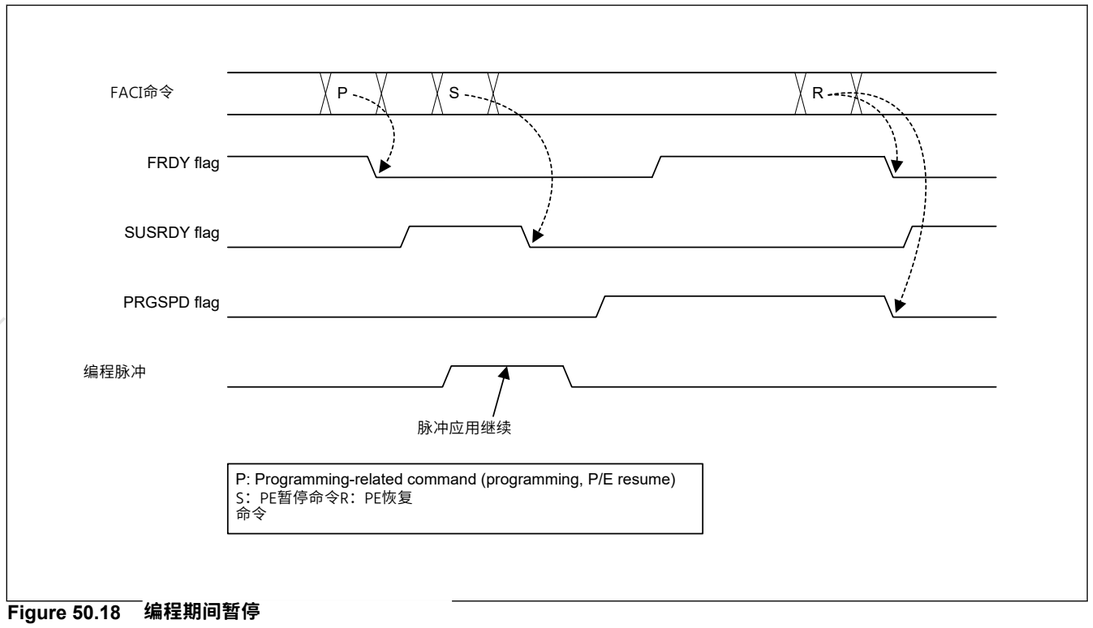


Figure 50.18 编程期间暂停

(2) 擦除期间暂停（暂停优先模式）

闪存定序器具有用于暂停擦除的暂停优先模式。图50.19显示了擦除挂起模式设置为挂起优先模式（FCPSR寄存器中的ESUSPMD位为0）时的擦除挂起操作。

当接收到擦除相关命令时，闪存定序器将FSTATR寄存器中的FRDY位清零以开始擦除。如果闪存序列器在擦除开始后进入可以接收PE挂起命令的状态，它会将FSTATR寄存器中的SUSRDY位设置为1。

当发出PE挂起命令时，闪存定序器接收该命令并将SUSRDY位清除为0。

在擦除期间接收到挂起命令时，闪存定序器启动挂起处理并将FSTATR寄存器中的ERSSPD位设置为1，即使它正在施加擦除脉冲。当挂起处理完成时，闪存定序器将FRDY位设置为1以进入擦除挂起状态。当在擦除暂停状态下接收到PE恢复命令时，闪存定序器将FRDY和ERSSPD位清除为0并恢复擦除。无论擦除暂停模式如何，FRDY、SUSRDY和ERSSPD位在擦除暂停和恢复时的操作都是相同的。

擦除暂停模式的设置会影响擦除脉冲的控制方法。在挂起优先模式下，当在施加先前未被挂起的擦除脉冲A的同时接收到PE挂起命令时，闪存定序器挂起擦除脉冲A的施加并进入擦除挂起状态。在使用PE恢复命令恢复擦除后，在重新应用擦除脉冲A的同时接收到PE暂停命令时，闪存定序器

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continues to apply erasure pulse A. After the specified pulse application time, the flash sequencer finishes erasure pulse application and enters the erasure suspended state.

When the flash sequencer receives a P/E resume command next and erasure pulse B is being applied, the flash sequencer receives a P/E suspend command again, and the application of erasure pulse B is then suspended. In suspension priority mode, delays due to suspension can be minimized because the application of an erasure pulse is suspended once per pulse, and priority is given to the suspend processing.

If the interval of suspension after resume is longer than t_{REST1} (Resume time: priority on suspension, resume after the 1st suspend for the same pulse), suspend delay will be always t_{SESD1} (Suspend delay: priority on suspension, the 1st suspend for the same pulse).

If the interval of suspension after resume is shorter than t_{REST1}, suspend delay becomes either t_{SESD1} or t_{SESD2} (Suspend delay: priority on suspension, the 2nd suspend for the same pulse).

(The value of t_{REST1} / t_{SESD1} / t_{SESD2}, see section 53, Electrical Characteristics.)

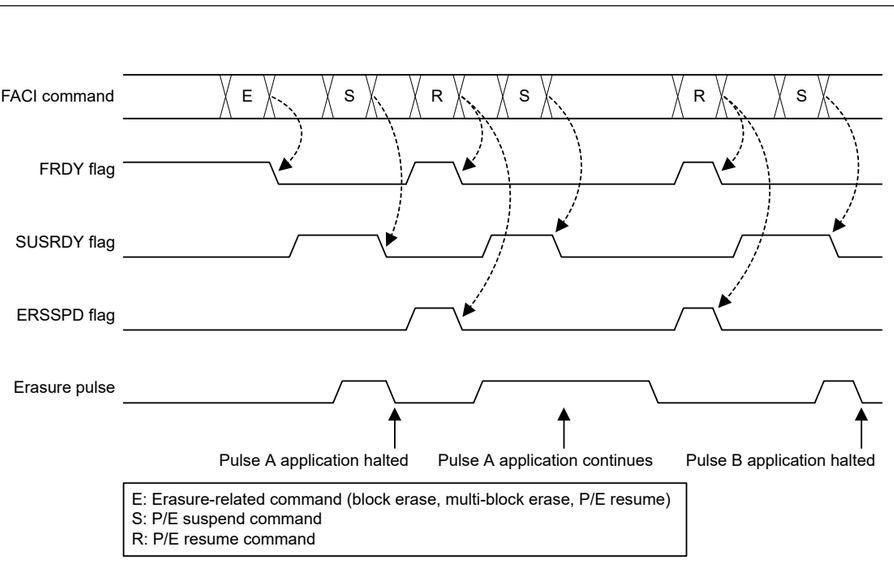

Figure 50.19 Suspension during erasure (suspension priority mode)

(3) Suspension during Erasure (Erasure Priority Mode)

The flash sequencer has an erasure priority mode for the suspension of erasure. Figure 50.20 shows the suspend operation of erasure when the erasure suspend mode is set to the erasure priority mode (the ESUSPMD bit in the FCPSR register is 1). The control method of erasure pulses in erasure priority mode is the same as that of programming pulses for the programming suspend processing.

If the flash sequencer receives a P/E suspend command while an erasure pulse is applied, the flash sequencer continues to apply the pulse. In this mode, the required time for the erasure processing can be reduced compared to the suspension priority mode because the re-application of erasure pulses does not occur when a P/E resume command is issued.

继续施加擦除脉冲A。在指定的脉冲施加时间之后，闪存定序器完成擦除脉冲施加并进入擦除暂停状态。

当闪存定序器接下来接收到PE恢复命令并且正在施加擦除脉冲B时，闪存定序器再次接收到PE暂停命令，然后暂停擦除脉冲B的施加。在挂起优先模式中，由于擦除脉冲的施加在每个脉冲中挂起一次，因此挂起引起的延迟可以被最小化，并且挂起处理具有优先权。

如果恢复后挂起的时间间隔大于tREST1（恢复时间：挂起优先，相同脉冲第一次挂起后恢复），挂起延迟将始终为tSESD1（挂起延迟：挂起优先，第一次挂起相同的脉冲）。

如果恢复后的暂停间隔小于tREST1，则暂停延迟变为tSESD1或tSESD2（暂停延迟：暂停优先，相同脉冲的第2次暂停）。

（tREST1tSESD1tSESD2的值，请参见第53节，电气特性。）

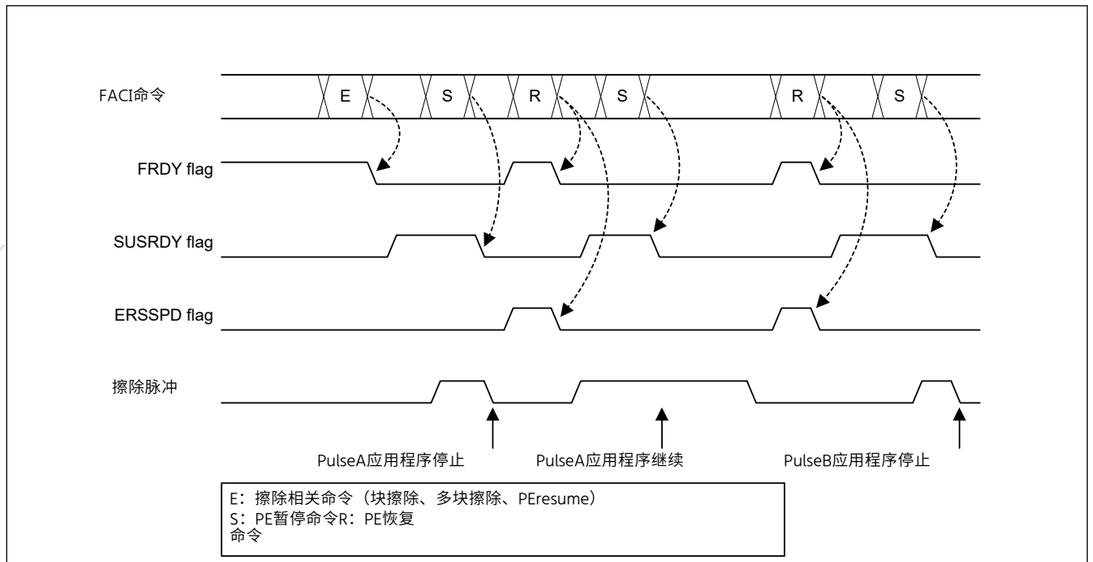

Figure 50.19 擦除期间暂停（暂停优先模式）

(3) 擦除期间暂停（擦除优先模式）

闪存定序器具有用于暂停擦除的擦除优先模式。图50.20显示了擦除挂起模式设置为擦除优先模式时的擦除挂起操作（FCPSR寄存器中的ESUSPMD位为1）。擦除优先模式中擦除脉冲的控制方法与用于编程暂停处理的编程脉冲的控制方法相同。

如果在施加擦除脉冲时闪存定序器接收到PE暂停命令，则闪存定序器继续施加脉冲。在这种模式下，与暂停优先模式相比，擦除处理所需的时间可以减少，因为当发出PE恢复命令时不会发生擦除脉冲的重新施加。

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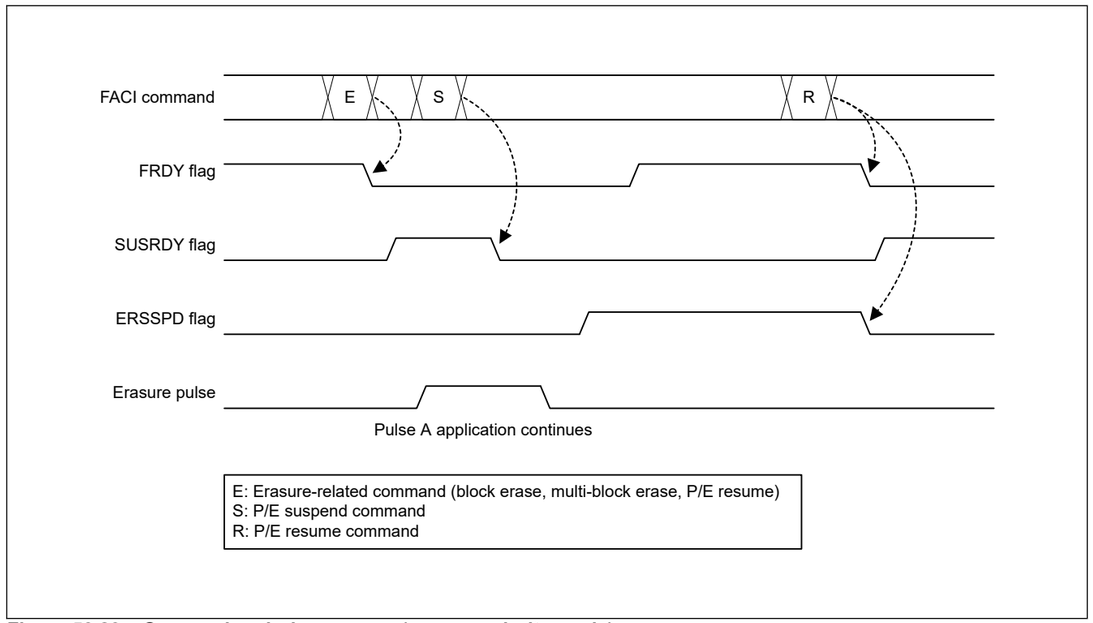
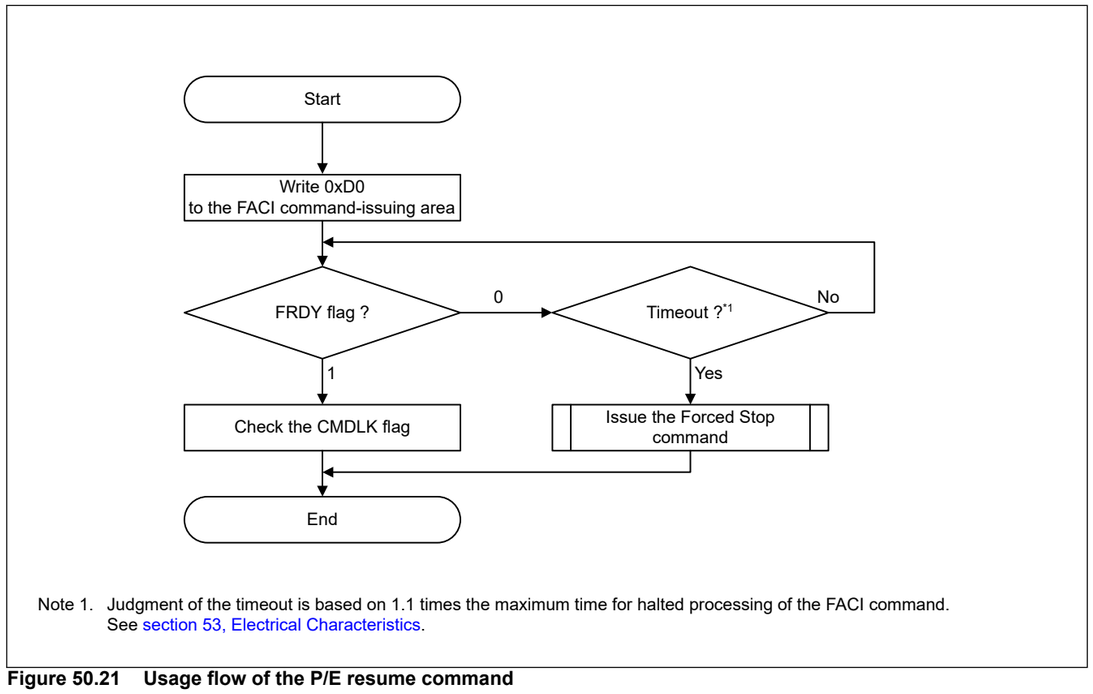


Figure 50.20 Suspension during erasure (erasure priority mode)

50.9.3.11 P/E Resume Command

The P/E resume command is used to resume suspended programming or erasure. If the FENTRYR setting has been modified during suspension, issue a P/E resume command only after resetting FENTRYR to the previous value that was held before the P/E suspend command was issued. Figure 50.21 shows usage of the P/E resume command.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command. See section 53, Electrical Characteristics.

Figure 50.21 Usage flow of the P/E resume command

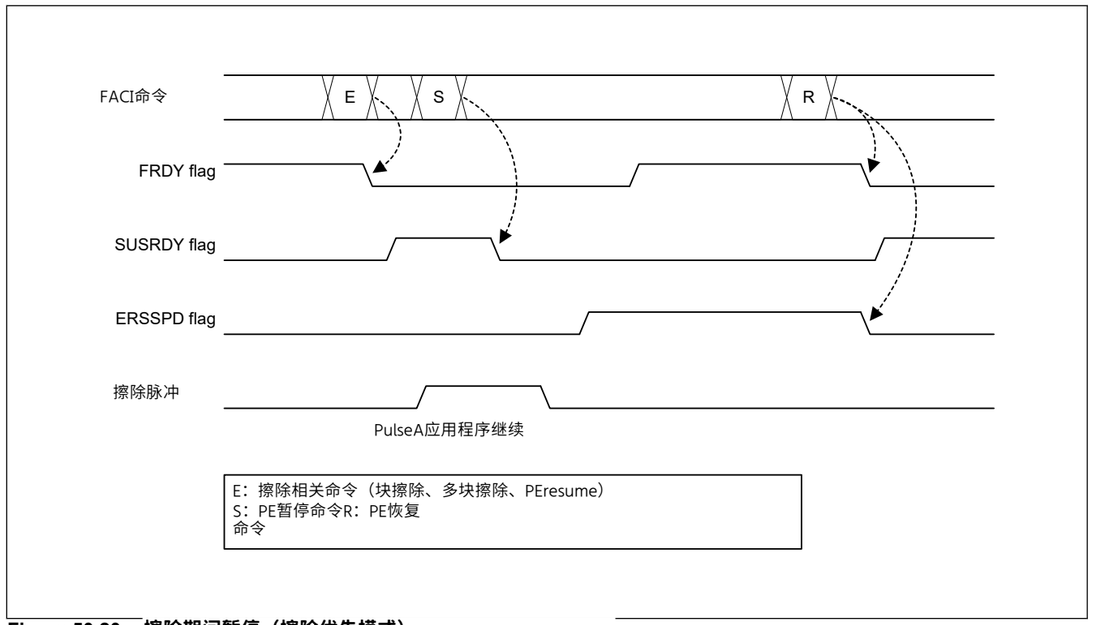
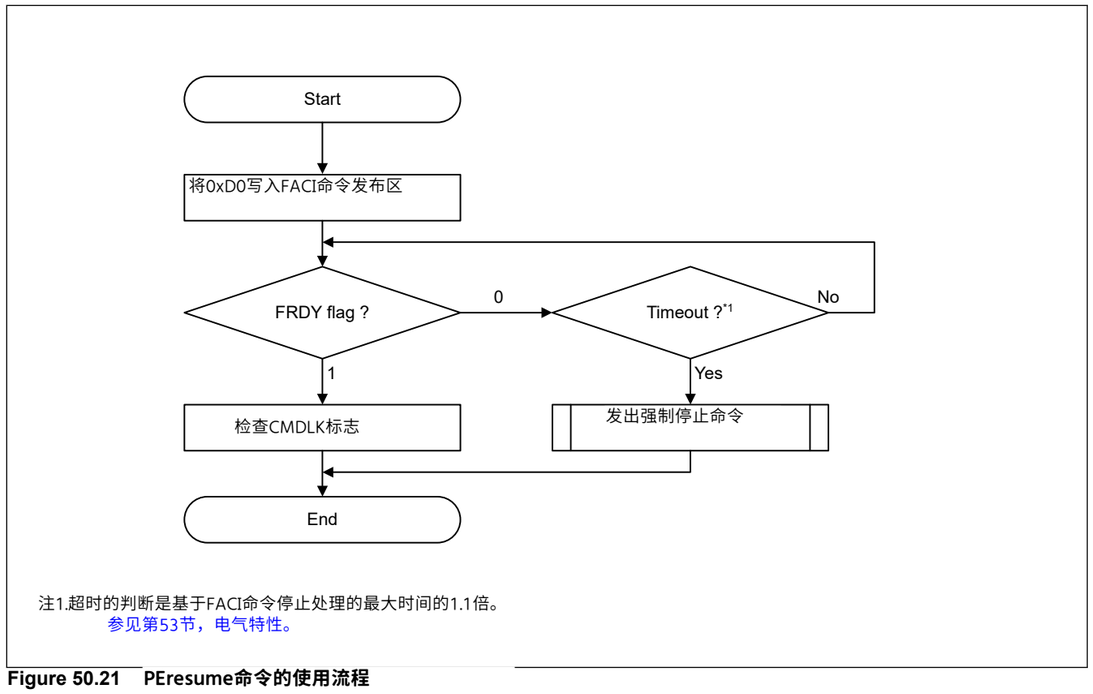


Figure 50.20 擦除期间暂停（擦除优先模式）

50.9.3.11 PE恢复命令

PEresume命令用于恢复暂停的编程或擦除。如果在挂起期间修改了FENTRYR设置，则仅在将FENTRYR重置为发出PE挂起命令之前保持的先前值之后才发出PEresume命令。图50.21显示了PEresume命令的用法。



注1.超时的判断是基于FACI命令停止处理的最大时间的1.1倍。
参见第53节，电气特性。

Figure 50.21 PEresume命令的使用流程

50.9.3.12 Status Clear Command

The status clear command is used to clear the command-locked state (see section 50.9.3.6. Recovery from the Command-Locked State).

You can use the status clear command to clear the following bits in the FSTATR register in the command-locked state:

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR

Figure 50.22 shows usage of the status clear command.

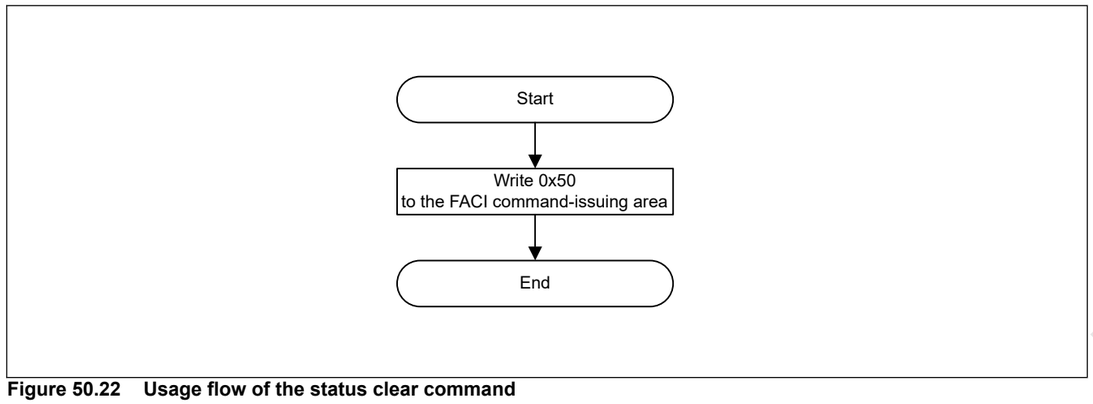


Figure 50.22 Usage flow of the status clear command

50.9.3.13 Forced Stop Command

The forced stop command is used to forcibly end command processing by the flash sequencer. Although this command halts command processing more quickly than the P/E suspension command, values from the programming or erasure that are in progress are not guaranteed. Additionally, resumption of processing is not possible. Processing of programming or erasure that is halted by the forced stop command is also defined as one programming round.

Executing the forced stop command also initializes part of the FACI, the whole FCU, the FSTATR and FASTAT registers. This command can be used in the procedure for recovery from the command-locked state and for processing in response to a timeout of the flash sequencer (see section 50.9.3.6. Recovery from the Command-Locked State).

Figure 50.23 shows usage of the forced stop command.

50.9.3.12 状态清除命令

statusclear命令用于清除命令锁定状态（参见第50.9.3.6节。从命令中恢复锁定状态）。

在命令锁定状态下，您可以使用statusclear命令清除FSTATR寄存器中的以下位：

- ILGLERR
- ILGCOMERR
- FESETERR
- SECERR
- OTERR
- ERSERR
- PRGERR

图50.22显示了statusclear命令的用法。

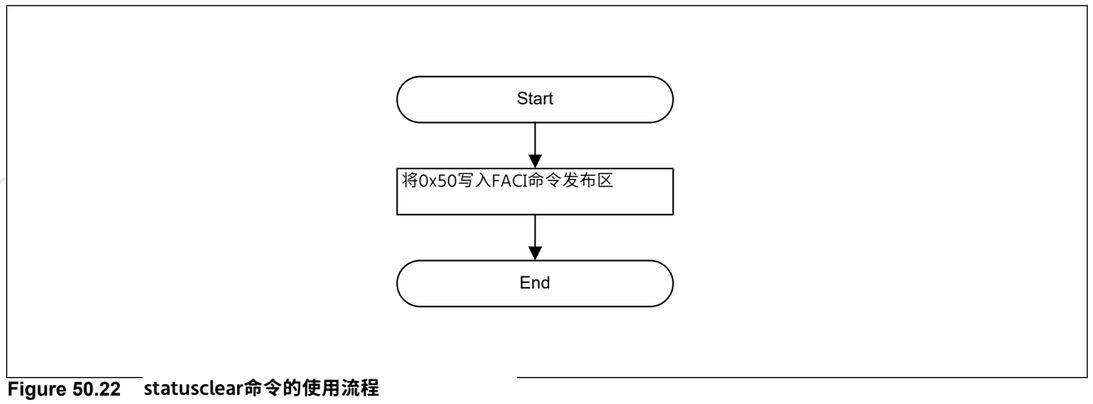


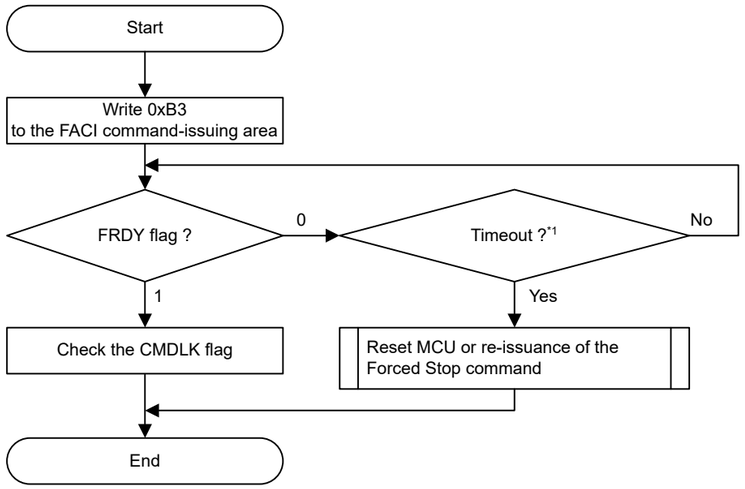
Figure 50.22 statusclear命令的使用流程

50.9.3.13 强制停止命令

强制停止命令用于强制结束闪存定序器的命令处理。尽管此命令比PE暂停命令更快地停止命令处理，但不能保证正在进行的编程或擦除的值。此外，无法恢复处理。由强制停止命令停止的编程或擦除的处理也被定义为一轮编程。

执行强制停止命令还会初始化部分FACI、整个FCU、FSTATR和FASTAT寄存器。
此命令可用于从命令锁定状态恢复的过程以及响应闪存定序器超时的处理（请参阅第50.9.3.6节。从命令锁定状态恢复）。

图50.23显示了强制停止命令的用法。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of the Forced Stop command latency.
See section 53, Electrical Characteristics.

Figure 50.23 Usage flow of the forced stop command

(1) Notes on Using the Forced Stop Command during Command Issue

When using the forced stop command at the timeout occurrence by DBFULL bit of the program command, writing in the FACI command-issuing area is sometimes processed as writing in data of the program command. See Table 50.4 in section 50.3. Address Space for information on the FACI command-issuing area to force a command lock. Then issue a forced stop command with return method from the command lock status (see Figure 50.14). Locking commands is possible in any case where the unit for reading the FACI command issuing area is 8, 16, or 32 bits.

50.9.3.14 Blank Check Command

The blank check command is used to confirm that an area is in the non-programmed state. Values read from the data flash memory that have been erased but not yet programmed again that is in the non-programmed state, are undefined.

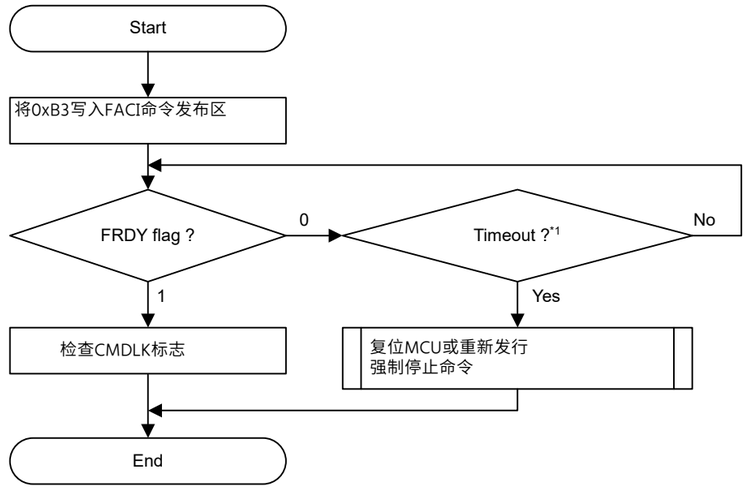
Before issuing the Blank Check command, set addressing mode, start address, and end address of the target area for Blank Check to the FBCCNT, FSADDR, and FEADDR registers. When Blank Check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = 1), address specified in FSADDR should be equal to or larger than address in FEADDR.

On the other hand, the address in FSADDR should be equal to or smaller than address in FEADDR when Blank Check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = 0).

If the settings of the BCDIR bit, FSADDR, and FEADDR are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for Blank Check is in the range from 4 bytes to the data flash memory capacity and is set in units of 4 bytes.

Write 0x71 and 0xD0 to the FACI command-issuing area to start Blank Check. Completion of processing can be confirmed by the FRDY bit of the FSTATR register. At the end of processing, the result of Blank Check is stored in the BCST bit in the FBCSTAT register. If non-programmed data exists within the target area for Blank Check, flash sequencer stops Blank Check command operation. In this case, address of non-programmed data is indicated to FPSADDR register.

Figure 50.24 shows usage of the blank check command.



注1.超时的判断基于强制停止命令延迟的最大时间的1.1倍。
参见第53节，电气特性。

Figure 50.23 强制停止命令的使用流程

(1) 命令发出期间使用强制停止命令的注意事项

通过程序命令的DBFULL位在超时发生时使用强制停止命令时，写入
FACI命令发布区域有时被处理为写入程序命令的数据。请参见第50.3节中的表50.4。FACI命令发布区域信息的地址空间以强制命令锁定。然后从命令锁定状态发出带返回方法的强制停止命令（见图50.14）。在读取FACI命令发布区域的单位为8、16或32位的任何情况下，锁定命令都是可能的。

50.9.3.14 空白检查命令

空白检查命令用于确认某个区域处于非编程状态。从处于未编程状态的已擦除但尚未再次编程的数据闪存读取的值未定义。

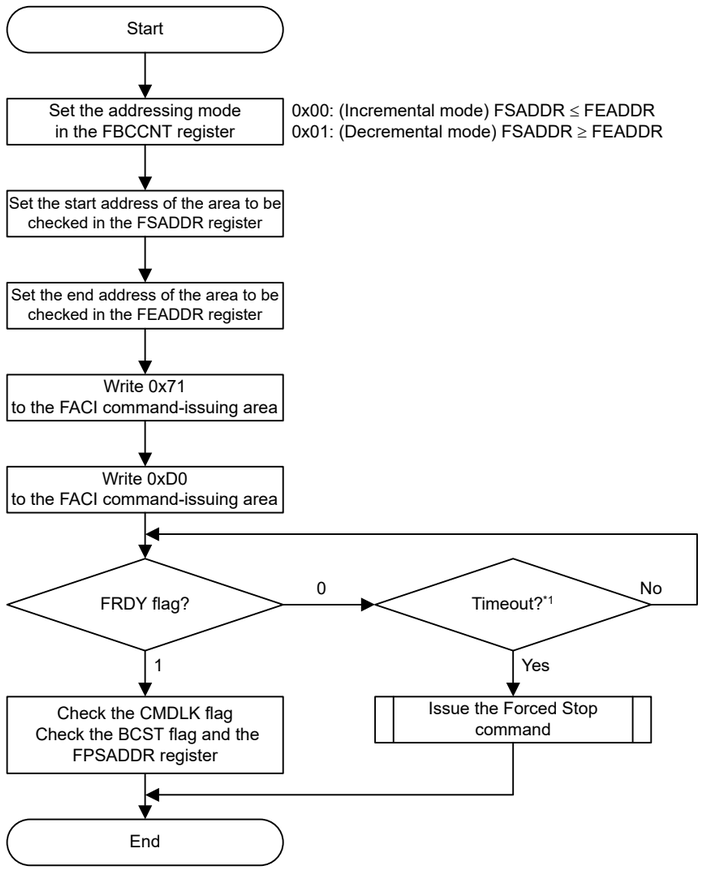
在发出空白检查命令之前，设置空白目标区域的寻址方式、起始地址和结束地址
检查FBCCNT、FSADDR和FEADDR寄存器。当空白检查寻址模式设置为递减模式（即FBCCNT.BCDIR=1）时，FSADDR中指定的地址应等于或大于FEADDR中的地址。

另一方面，当空白检查寻址模式设置为增量模式（即FBCCNT.BCDIR=0）时，FSADDR中的地址应等于或小于FEADDR中的地址。

如果BCDIR位、FSADDR和FEADDR的设置不一致，则flashsequencer进入command-locked状态。BlankCheck的目标区域大小在4字节到数据闪存容量的范围内，以4字节为单位设置。

将0x71和0xD0写入FACI命令发出区域以启动空白检查。可通过FSTATR寄存器的FRDY位确认处理完成。处理结束时，空白检查的结果存储在FBCSTAT寄存器的BCST位中。如果空白检查的目标区域内存在未编程的数据，闪存定序器将停止空白
检查命令操作。在这种情况下，非编程数据的地址被指示到FPSADDR寄存器。

图50.24显示了空白检查命令的用法。



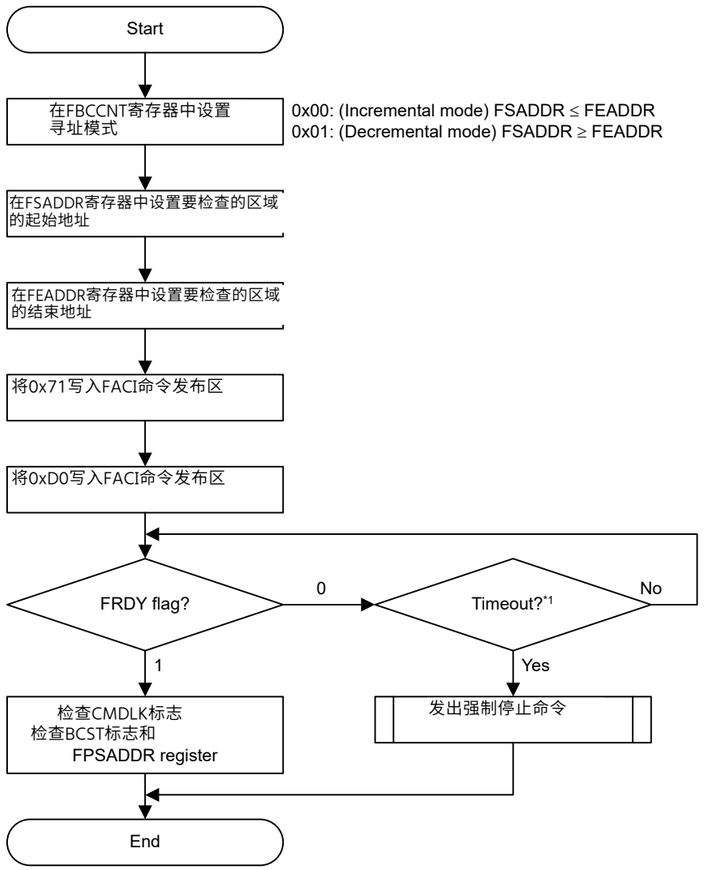
Note 1. Judgment of the timeout is based on 1.1 times the maximum time of Blank Checking for the whole target range. See section 53, Electrical Characteristics.

Figure 50.24 Usage flow of the blank check command

50.9.3.15 Configuration Set Command

The Configuration set command is used to set option-setting memory. Before issuing the Configuration set command, set the specified address (shown in Table 50.19) in the FSADDR register. Writing 0xD0 to the FACI command-issuing area in the final access for issuing the FACI command starts FACI processing of the Configuration set command.

Figure 50.25 shows usage of the configuration set command.



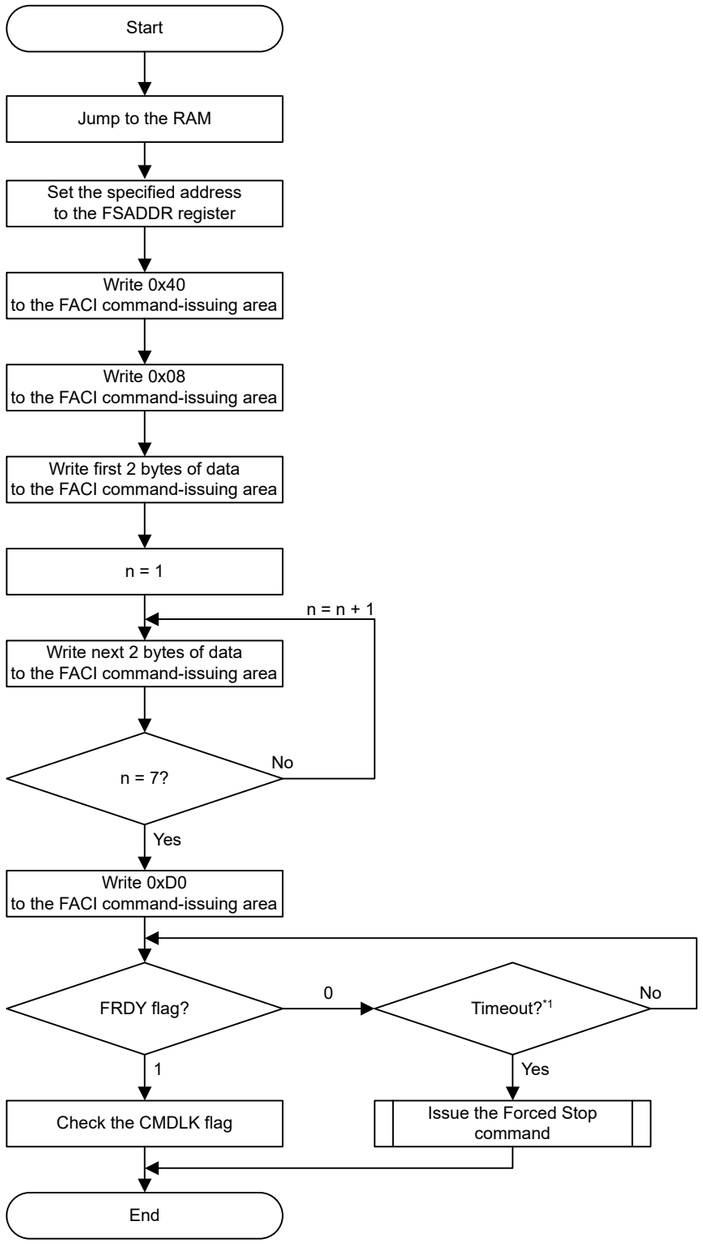
注1.超时的判断是基于1.1倍的整个目标范围的BlankChecking最大时间。看第53节，电气特性。

Figure 50.24 空白检查命令的使用流程

50.9.3.15 配置集命令

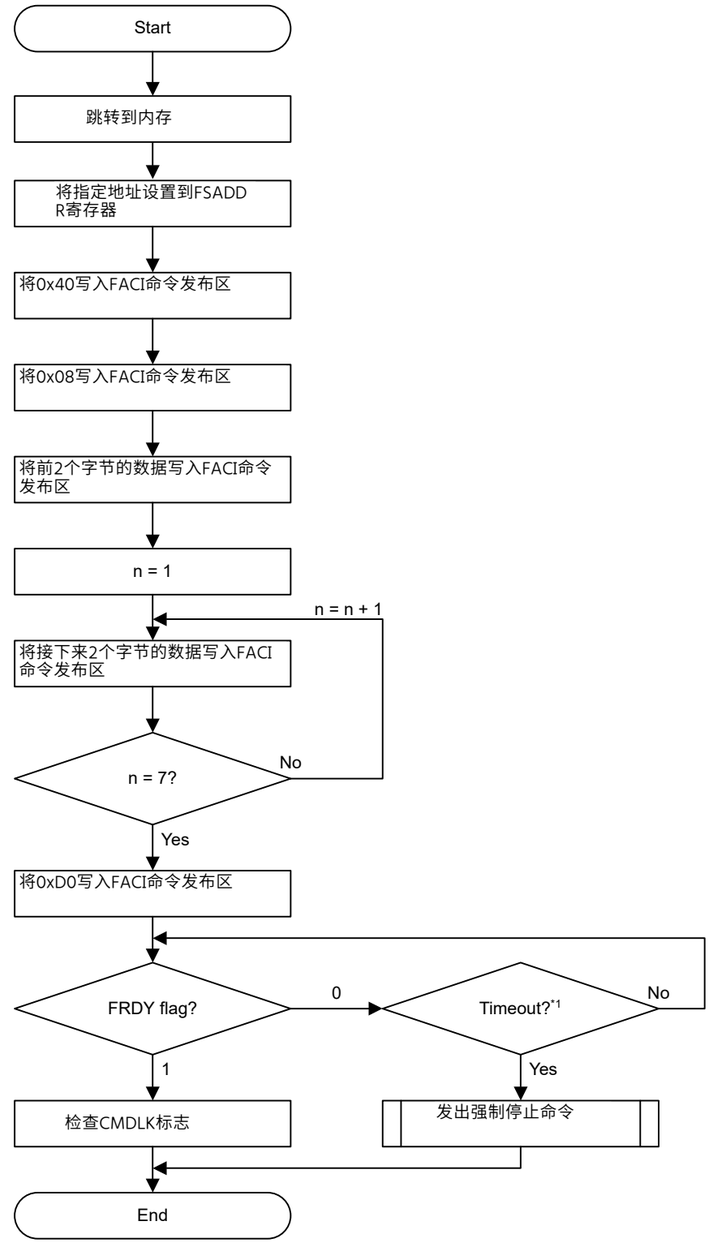
Configurationset命令用于设置选项设置内存。在发出配置设置命令之前，在FSADDR寄存器中设置指定的地址（如表50.19所示）。在发出FACI命令的最终访问中将0xD0写入FACI命令发出区域，开始配置设置命令的FACI处理。

图50.25显示了配置集命令的用法。



Note 1. Judgment of the timeout is based on 1.1 times the maximum time of programing in option-setting memory. See section 53, Electrical Characteristics.

Figure 50.25 Usage flow of the configuration set command



注1.超时的判断是基于选项设置内存中最大编程时间的1.1倍。参见第53节，电气特性。

Figure 50.25 配置集命令使用流程

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in Table 50.19. For details, see section 50.4.12. FSADDR : FACI Command Start Address Register.

Table 50.19 Address Used by Configuration Set Command

Address	FSADDR Register Value	Setting Data	Operation of additional writing		Timing when the Setting is Enabled
			SAS.FSPR bit is 1	SAS.FSPR bit is 0	
0x0100_A100	0x0100_A100	Option Function Select Register 0 (OFS0)	Writable	Writable	At a reset
0x0100_A110	0x0100_A110	Dual Mode Select Register (DULSEL)	Writable	Writable	At a reset
0x0100_A134	0x0100_A130	Start-up Area Setting Register (SAS)	Writable	Not writable*1	When a reset or command is executed
0x0100_A180	0x0100_A180	Option Function Select Register 1 (OFS1)	Writable	Writable	At a reset
0x0100_A190	0x0100_A190	Bank Select Register (BANKSEL)	Writable	Writable	At a reset
0x0100_A1C0	0x0100_A1C0	Block Protect Setting Register (BPS)	Writable*2	Writable*2	When a reset or command is executed
0x0100_A1E0	0x0100_A1E0	Permanent Block Protect Setting Register (PBPS)	Writable*3 (from 1 to 0 only)	Writable*3 (from 1 to 0 only)	When a reset or command is executed
0x0100_A200	0x0100_A200	Option Function Select Register 1 Secure (OFS1_SEC)	Writable	Writable	At a reset
0x0100_A210	0x0100_A210	Bank Select Register Secure (BANKSEL_SEC)	Writable	Writable	At a reset
0x0100_A240	0x0100_A240	Block Protect Setting Register Secure (BPS_SEC)	Writable*4	Writable*4	When a reset or command is executed
0x0100_A260	0x0100_A260	Permanent Block Protect Setting Register Secure (PBPS_SEC)	Writable*5 (from 1 to 0 only)	Writable*5 (from 1 to 0 only)	When a reset or command is executed
0x0100_A280	0x0100_A280	Option Function Select Register 1 Select (OFS1_SEL)	Writable	Writable	At a reset
0x0100_A290	0x0100_A290	Bank Select Register Select (BANKSEL_SEL)	Writable	Writable	At a reset
0x0100_A2C0	0x0100_A2C0	Block Protect Setting Register Select (BPS_SEL)	Writable	Writable	At a reset

Note 1. The SAS.FSPR bit cannot be restored to 1 by using the Configuration set command once it is set to 0. Therefore, setting the start-up area select flags again becomes impossible. (when the Configuration set command is issued to the address of 0x0100A134, the command is locked.) Exercise extra caution when handling the SAS.FSPRbit.
Note 2. Once PBPS[n] bit is set to 0, the BPS[n] bit cannot be restored to 1 by using the Configuration set command.
Note 3. Once these bits are set to 0, the bits cannot be restored to 1 by using the Configuration set command. The PBPS[n] bit can not be set to 0 by using the Configuration set command when the BPS[n] bit is 1.
Note 4. Once PBPS_SEC[n] bit is set to 0, the BPS_SEC[n] bit cannot be restored to 1 by using the Configuration set command.
Note 5. Once these bits are set to 0, the bits cannot be restored to 1 by using the Configuration set command. The PBPS_SEC[n] bit cannot be set to 0 by using the Configuration set command when the BPS_SEC[n] bit is 1.

50.10 Suspend Operation

Reading from the flash memory is not possible during programming or erasure if the conditions for background operation given in Table 50.35 are not satisfied. When a P/E suspend command is issued to suspend the programming or erasure of the flash memory, reading from the flash memory is enabled. Regarding P/E suspend commands, there are one suspend command mode for programming and two suspend command modes for erasure (suspension priority mode and erasure priority mode). To resume suspended programming or erasure, the P/E resume command is available. See details on the suspend operation, refer to Figure 50.17.

配置设置的可能目标数据与FSADDR寄存器中设置的地址值的对应关系如表50.19所示。有关详细信息，请参阅第50.4.12节。FSADDR：FACI命令起始地址寄存器。

Table 50.19 配置设置命令使用的地址

Address	FSADDR 寄存器值设置数据		追加写入的操作		启用设置的时间
			SAS.FSPR位为1	SAS.FSPR位为0	
0x0100_A100	0x0100_A100	选项功能选择寄存器0(OFS0)	Writable	Writable	复位时
0x0100_A110	0x0100_A110	双模式选择寄存器(DULSEL)	Writable	Writable	复位时
0x0100_A134	0x0100_A130	启动区设置寄存器(SAS)	Writable	Not writable*1	执行复位或命令时
0x0100_A180	0x0100_A180	选项功能选择寄存器1(OFS1)	Writable	Writable	复位时
0x0100_A190	0x0100_A190	银行选择寄存器(BANKSEL)	Writable	Writable	复位时
0x0100_A1C0	0x0100_A1C0	块保护设置寄存器(BPS)	Writable*2	Writable*2	执行复位或命令时
0x0100_A1E0	0x0100_A1E0	永久块保护设置 Register (PBPS)	Writable*3 (from 1 to 0 only)	Writable*3 (from 1 to 0 only)	执行复位或命令时
0x0100_A200	0x0100_A200	选项功能选择寄存器1 Secure (OFS1_SEC)	Writable	Writable	复位时
0x0100_A210	0x0100_A210	银行选择寄存器安全(BANKSEL_SEC)	Writable	Writable	复位时
0x0100_A240	0x0100_A240	块保护设置寄存器 Secure (BPS_SEC)	Writable*4	Writable*4	执行复位或命令时
0x0100_A260	0x0100_A260	永久块保护设置 注册安全(PBPS_SEC)	Writable*5 (from 1 to 0 only)	Writable*5 (from 1 to 0 only)	执行复位或命令时
0x0100_A280	0x0100_A280	选项功能选择寄存器1 Select (OFS1_SEL)	Writable	Writable	复位时
0x0100_A290	0x0100_A290	银行选择寄存器选择（BANKSEL_SEL)	Writable	Writable	复位时
0x0100_A2C0	0x0100_A2C0	块保护设置寄存器 Select (BPS_SEL)	Writable	Writable	复位时

注1.SAS.FSPR位一旦设置为0，就无法通过Configurationset命令恢复为1。因此，再次设置启动区域选择标志变得不可能。（当向0x0100A134地址发出Configurationset命令时，该命令被锁定。）处理SAS.FSPRbit时要格外小心。

注2.一旦PBPS[n]位设置为0，BPS[n]位不能通过使用配置设置命令恢复为1。
注3.一旦这些位设置为0，就不能使用配置设置命令将这些位恢复为1。当BPS[n]位为1时，不能使用配置设置命令将PBPS[n]位设置为0。

注4.一旦PBPS_SEC[n]位设置为0，则BPS_SEC[n]位无法通过使用配置设置命令恢复为1。
注5.一旦这些位设置为0，就不能使用配置设置命令将这些位恢复为1。当BPS_SEC[n]位为1时，无法使用配置设置命令将PBPS_SEC[n]位设置为0。

50.10 暂停操作

如果不满足表50.35中给出的后台操作条件，则在编程或擦除期间无法从闪存读取。当发出PE暂停命令以暂停闪存的编程或擦除时，将启用从闪存读取。关于PE挂起命令，有一种用于编程的挂起命令模式和两种用于擦除的挂起命令模式（挂起优先模式和擦除优先模式）。要恢复暂停的编程或擦除，可以使用PEresume命令。详见挂起操作，参见图50.17。

50.11 Protection Function

50.11.1 Software Protection

Software protection disables programming and erasure of the code flash memory through the settings of control registers and block protect setting in the user area. If an attempt is made to issue an FACI command against software protection, the flash sequencer enters the command-locked state.

50.11.1.1 Protection through FWEPROR

Unless the FWEPROR.FLWE[1:0] bits are set to 01b, programming cannot proceed in any mode.

50.11.1.2 Protection by FENTRYR

When the FENTRYR register is set to 0x0000, the flash sequencer enters read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

50.11.1.3 Protection by Block Protect Setting

Each block in user area has the block protect setting (BPS or BPS_SEC). When the FBPROT0 or FBPROT1 register is 0x0000 and the block protect bit is 0, issuing the Program or Block Erase command to user area of the code flash causes the command-locked state. To program or erase the block whose block protect bit is 0, set the FBPROT0 or FBPROT1 register to 0x0001.

The block protect setting can be locked by the permanent block protect setting (PBPS or PBPS_SEC). When the permanent block protect setting and the block protect setting are 0, issuing a Program or Block erase command to user area of the code flash causes the flash sequencer to enter the command-locked state regardless of the FBPROT0 and FBPROT1 register settings.

Valid block protect setting (BPS or BPS_SEC) depends on the Block Protect Select bit (BPS_SEL).

See section 50.12.2. Permanent Block Protect Setting for details of the block protect setting and permanent block protect setting. See section 50.4.15. FBPROT0 : Flash Block Protection Register and section 50.4.16. FBPROT1 : Flash Block Protection for Secure Register for more information.

For details of block protect setting (BPS or BPS_SEC) and block protect select (BPS_SEL), see section 6, Option-Setting Memory.

The protected area by the block protect setting is always determined by the address of the FSADDR register setting regardless of the address swapping function setting (the startup area select, the block swap in linear mode, and the startup bank select in dual mode). Table 50.20 to Table 50.25 show the relation of user area and the block protect setting in each function setting.

(1) In case of the linear mode

- BPS[0] to BPS[n] or BPS_SEC[0] to BPS_SEC[n] are assigned to the block of user area (for example, address is 0x00_0000 to the last block address).
- BPS[0]/BPS_SEC[0] and BPS[1]/BPS_SEC[1] are assigned to the block of user area depending on the startup area select setting (SAS.BTFLG bit). (See section 50.11.3. Start-Up Program Protection).
- The second half of FLI user area is assigned to block protect setting depending on the block swap select setting (BANKSEL.BLCKSWP[2:0] bits). See section 50.11.5. Block Swap Function.

Table 50.20 shows the block protect setting when the startup area select is disabled (not swapping).

Table 50.20 show example of the block protect setting when the address conversion function is used.

Table 50.20 Example of Block Protect setting when SAS.BTFLG is 1 (1 of 2)

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n] or BPS_SEC[n]	Block n	—

50.11 保护功能

50.11.1 软件保护

软件保护通过控制寄存器的设置和用户区的块保护设置禁用代码闪存的编程和擦除。如果尝试针对软件保护发出FACI命令，则闪存定序器进入命令锁定状态。

50.11.1.1 通过FWEPROR进行保护

除非FWEPROR.FLWE[1:0]位设置为01b，否则无法在任何模式下进行编程。

50.11.1.2 FENTRYR的保护

当FENTRYR寄存器设置为0x0000时，闪存定序器进入读取模式。在读取模式下，无法接受FACI命令。如果尝试在读取模式下发出FACI命令，则闪存定序器进入命令锁定状态。

50.11.1.3 通过块保护设置进行保护

用户区的每个块都有块保护设置（BPS或BPS_SEC）。当FBPROT0或FBPROT1寄存器为0x0000且块保护位为0时，向代码闪存的用户区发出Program或BlockErase命令会导致命令锁定状态。要编程或擦除块保护位为0的块，请将FBPROT0或FBPROT1寄存器设置为0x0001。

块保护设置可以通过永久块保护设置（PBPS或PBPS_SEC）锁定。当永久块保护设置和块保护设置为0时，无论FBPROT0和FBPROT1寄存器设置如何，向代码闪存的用户区发出程序或块擦除命令都会使闪存定序器进入命令锁定状态。

有效的块保护设置（BPS或BPS_SEC）取决于块保护选择位（BPS_SEL）。

请参阅第50.12.2节。永久块保护设置有关块保护设置和永久块保护设置的详细信息。请参阅第50.4.15节。FBPROT0：闪存块保护寄存器和第50.4.16节。FBPROT1：安全寄存器的闪存块保护了解更多信息。

有关块保护设置（BPS或BPS_SEC）和块保护选择（BPS_SEL）的详细信息，请参阅第6节，选项设置Memory.

块保护设置的保护区域始终由FSADDR寄存器设置的地址决定，与地址交换功能设置无关（启动区域选择、线性模式下的块交换和双模式下的启动库选择）。表50.20至表50.25显示了每个功能设置中用户区和块保护设置的关系。

(1) 在线性模式的情况下

●BPS[0]到BPS[n]或BPS_SEC[0]到BPS_SEC[n]分配给用户区的块（例如，地址是0x00_0000到最后一个块地址）。

●BPS[0]BPS_SEC[0]和BPS[1]BPS_SEC[1]根据启动区选择设置（SAS.BTFLG位）分配给用户区块。（参见第50.11.3节。启动程序保护）。

●FLI用户区的后半部分根据块交换选择设置（BANKSEL.BLCKSWP[2:0]位）分配给块保护设置。请参阅第50.11.5节。块交换功能。

表50.20显示了禁用启动区域选择（不交换）时的块保护设置。

表50.20显示了使用地址转换功能时的块保护设置示例。

Table 50.20 SAS.BTFLG为1时的块保护设置示例（1of2）

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
最后一个区块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	—

Table 50.20 Example of Block Protect setting when SAS.BTFLG is 1 (2 of 2)

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	Not swap block 0 and block 1 in this startup area select setting
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	Not swap block 0 and block 1 in this startup area select setting

Table 50.21 Example of Block Protect setting when SAS.BTFLG is 0

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 0	Swap block 0 and block 1 in this startup area select setting
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 1	Swap block 0 and block 1 in this startup area select setting

Table 50.22 Example of Block Protect setting when BANKSEL.BLCKSWP is 1 (1 of 2)

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
The upper side address of the block swap target	32 KB	BPS[b] or BPS_SEC[b]	Block b	Not swap block a and block b in this block swap select setting
⋮	⋮	⋮	⋮	—
The lower side address of the block swap target	32 KB	BPS[a] or BPS_SEC[a]	Block a	Not swap block a and block b in this block swap select setting
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—

Table 50.20 SAS.BTFLG为1时的块保护设置示例(2of2)

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	不交换此启动区域中的块0和块1选择设置
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	不交换此启动区域中的块0和块1选择设置

Table 50.21 SAS.BTFLG为0时的块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
最后一个区块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 0	在此启动区域选择设置中交换块0和块1
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 1	在此启动区域选择设置中交换块0和块1

Table 50.22 BANKSEL.BLCKSWP为1时的块保护设置示例(1of2)

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
最后一个区块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
块交换目标的高位地址	32 KB	BPS[b] or BPS_SEC[b]	Block b	在此块交换选择设置中不交换块a和块b
⋮	⋮	⋮	⋮	—
块交换目标的低端地址	32 KB	BPS[a] or BPS_SEC[a]	Block a	在此块交换选择设置中不交换块a和块b
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—

Table 50.22 Example of Block Protect setting when BANKSEL.BLCKSWP is 1 (2 of 2)

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
⋮	⋮	⋮	⋮	—
0x002000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	—
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	—

Table 50.23 Example of Block Protect setting when BANKSEL.BLCKSWP is 0

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
The updating side address of the block swap target	32 KB	BPS[b] or BPS_SEC[b]	Block a	Swap block a and block b in this block swap select setting
⋮	⋮	⋮	⋮	—
The operating side address of the block swap target	32 KB	BPS[a] or BPS_SEC[a]	Block b	Swap block a and block b in this block swap select setting
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	—
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	—

(2) In case of the dual mode (DUALSEL.BANKMD[2:0] = 000b)

- BPS[0] to BPS[n] or BPS_SEC[0] to BPS_SEC[n] are assigned the block of bank 0 user area (for example, address is 0x00000000 to the last block address in the lower side bank).
- BPS[70] to BPS[70 + n] or BPS_SEC[70] to BPS_SEC[70 + n] are assigned to the block of bank 1 user area (for example, address is 0x00200000 to the last block address in the upper side bank).

Bank0 is upper side bank (BANKSEL.BANKSWP[2:0] = 000b)

- BPS[0] to BPS[n] or BPS_SEC[0] to BPS_SEC[n] are assigned to the block of bank1 user area (e.g. Address is 0x00_0000 to The last block address in lower side bank).
- BPS[70] to BPS[70+n] or BPS_SEC[70] to BPS_SEC[70+n] are assigned to the block of bank0 user area (e.g. Address is 0x20_0000 to The last block address in upper side bank).

Table 50.24 and Table 50.25 show example of the block protect setting in the dual mode. See section 50.11.4. Dual Bank Function for details of dual bank function (DUALSEL.BANKMD[2:0] and BANKSEL.BANKSWP[2:0] bits).

Table 50.22 BANKSEL.BLCKSWP为1时的块保护设置示例(2of2)

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
⋮	⋮	⋮	⋮	—
0x002000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	—
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	—

Table 50.23 BANKSEL.BLCKSWP为0时的块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
最后一个区块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	—
⋮	⋮	⋮	⋮	—
块交换目标的更新端地址	32 KB	BPS[b] or BPS_SEC[b]	Block a	在此块交换选择设置中交换块a和块b
⋮	⋮	⋮	⋮	—
块交换目标的操作端地址	32 KB	BPS[a] or BPS_SEC[a]	Block b	在此块交换选择设置中交换块a和块b
⋮	⋮	⋮	⋮	—
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	—
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	—
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	—
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	—
⋮	⋮	⋮	⋮	—
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	—
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	—

(2) 在双模式的情况下（DUALSEL.BANKMD[2:0]=000b）

●BPS[0]到BPS[n]或BPS_SEC[0]到BPS_SEC[n]分配了bank0用户区的块（例如，地址是0x00000000到下侧bank中的最后一个块地址）。

●BPS[70]到BPS[70+n]或BPS_SEC[70]到BPS_SEC[70+n]分配给bank1用户区的块（例如，地址为0x00200000到上侧的最后一个块地址银行）。

Bank0是上侧银行(BANKSEL.BANKSWP[2:0]=000b)

●BPS[0]到BPS[n]或BPS_SEC[0]到BPS_SEC[n]分配给bank1用户区的块（例如，地址是0x00_0000到下侧bank中的最后一个块地址）。

●BPS[70]到BPS[70+n]或BPS_SEC[70]到BPS_SEC[70+n]分配给bank0用户区的块（例如地址是0x20_0000到上侧bank中的最后一个块地址）。

表50.24和表50.25显示了双模式下的块保护设置示例。请参阅第50.11.4节。双银行详细了解双组功能的功能（DUALSEL.BANKMD[2:0]和BANKSEL.BANKSWP[2:0]位）。

Table 50.24 Example of Block Protect setting when BANKSEL.BANKSWP[2:0] is 111b

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address in upper side bank	32 KB	BPS[70 + n] or BPS_SEC[70 + n]	Block 70 + n	Not swap bank 0 and bank 1 in this startup bank switch setting
⋮	⋮	⋮	⋮	
0x21_8000 to 0x21_FFFF	32 KB	BPS[79] or BPS_SEC[79]	Block 79	
0x21_0000 to 0x21_7FFF	32 KB	BPS[78] or BPS_SEC[78]	Block 78	
0x20_E000 to 0x20_FFFF	8 KB	BPS[77] or BPS_SEC[77]	Block 77	
0x20_C000 to 0x20_DFFF	8 KB	BPS[76] or BPS_SEC[76]	Block 76	
⋮	⋮	⋮	⋮	
0x20_2000 to 0x20_3FFF	8 KB	BPS[71] or BPS_SEC[71]	Block 71	
0x20_0000 to 0x20_1FFF	8 KB	BPS[70] or BPS_SEC[70]	Block 70	
The last block address in lower side bank	32 KB	BPS[n] or BPS_SEC[n]	Block n	Not swap bank 0 and bank 1 in this startup bank switch setting
⋮	⋮	⋮	⋮	
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	
⋮	⋮	⋮	⋮	
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	

Table 50.25 Relation of User area and Block Protect setting when BANKSEL.BANKSWP[2:0] is 000b (1 of 2)

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address in the upper side bank	32 KB	BPS[70 + n] or BPS_SEC[70 + n]	Block n	Swap bank 0 and bank 1 in this startup bank switch setting
⋮	⋮	⋮	⋮	
0x21_8000 to 0x21_FFFF	32 KB	BPS[79] or BPS_SEC[79]	Block 9	
0x21_0000 to 0x21_7FFF	32 KB	BPS[78] or BPS_SEC[78]	Block 8	
0x20_E000 to 0x20_FFFF	8 KB	BPS[77] or BPS_SEC[77]	Block 7	
0x20_C000 to 0x20_DFFF	8 KB	BPS[76] or BPS_SEC[76]	Block 6	
⋮	⋮	⋮	⋮	
0x20_2000 to 0x20_3FFF	8 KB	BPS[71] or BPS_SEC[71]	Block 1	
0x20_0000 to 0x20_1FFF	8 KB	BPS[70] or BPS_SEC[70]	Block 0	

Table 50.24 BANKSEL.BANKSWP[2:0]为111b时的块保护设置示例

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
上侧bank中的最后一个块地址	32 KB	BPS[70 + n] or BPS_SEC[70 + n]	Block 70 + n	在此启动银行开关设置中不交换银行0和银行1
⋮	⋮	⋮	⋮	
0x21_8000 to 0x21_FFFF	32 KB	BPS[79] or BPS_SEC[79]	Block 79	
0x21_0000 to 0x21_7FFF	32 KB	BPS[78] or BPS_SEC[78]	Block 78	
0x20_E000 to 0x20_FFFF	8 KB	BPS[77] or BPS_SEC[77]	Block 77	
0x20_C000 to 0x20_DFFF	8 KB	BPS[76] or BPS_SEC[76]	Block 76	
⋮	⋮	⋮	⋮	
0x20_2000 to 0x20_3FFF	8 KB	BPS[71] or BPS_SEC[71]	Block 71	
0x20_0000 to 0x20_1FFF	8 KB	BPS[70] or BPS_SEC[70]	Block 70	
下侧bank中的最后一个块地址	32 KB	BPS[n] or BPS_SEC[n]	Block n	在此启动银行开关设置中不交换银行0和银行1
⋮	⋮	⋮	⋮	
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 9	
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 8	
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 7	
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 6	
⋮	⋮	⋮	⋮	
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 1	
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 0	

Table 50.25 当BANKSEL.BANKSWP[2:0]为000b(1of2)时用户区和块保护设置的关系

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
上侧bank中的最后一个块地址	32 KB	BPS[70 + n] or BPS_SEC[70 + n]	Block n	在此启动银行开关设置中交换银行0和银行1
⋮	⋮	⋮	⋮	
0x21_8000 to 0x21_FFFF	32 KB	BPS[79] or BPS_SEC[79]	Block 9	
0x21_0000 to 0x21_7FFF	32 KB	BPS[78] or BPS_SEC[78]	Block 8	
0x20_E000 to 0x20_FFFF	8 KB	BPS[77] or BPS_SEC[77]	Block 7	
0x20_C000 to 0x20_DFFF	8 KB	BPS[76] or BPS_SEC[76]	Block 6	
⋮	⋮	⋮	⋮	
0x20_2000 to 0x20_3FFF	8 KB	BPS[71] or BPS_SEC[71]	Block 1	
0x20_0000 to 0x20_1FFF	8 KB	BPS[70] or BPS_SEC[70]	Block 0	

Table 50.25 Relation of User area and Block Protect setting when BANKSEL.BANKSWP[2:0] is 000b (2 of 2)

FSADDR[23:0]	Block size	Block protect setting	User area block number	Notes
The last block address in the lower side bank	32 KB	BPS[n] or BPS_SEC[n]	Block 70 + n	Swap bank 0 and bank 1 in this startup bank switch setting
⋮	⋮	⋮	⋮	
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 79	
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 78	
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 77	
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 76	
⋮	⋮	⋮	⋮	
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 71	
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 70	

50.11.2 Error Protection

Error protection detects the issuing of illegal FACI commands, illegal access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue the Status Clear or Forced Stop command. The Status Clear command can only be used while the FRDY bit in the FSTATR register is 1. The Forced Stop command can be used regardless of the value of the FRDY bit. While the CMDLKIE bit in the FAEINT register is 1, a flash access error (FIFERR) interrupt is generated if the flash sequencer enters the command-locked state (the CMDLK bit in the FASTAT register is set to 1).

If the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during programming or erasure processing, the flash sequencer continues the processing for programming or erasure. In this state, the P/E suspend command cannot be used to suspend the processing for programming or erasure. If a command is issued in the command-locked state, the ILGLERR bit becomes 1 and the other bits retain the values set from previous error detection.

Table 50.26 shows the error protection types and status bit values after error detections.

Table 50.26 Error protection type (1 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR setting error	The value set in FENTRYR is not 0x0000, 0x0001, or 0x0080	0	1	0	0	1	0	0	0	0	0
	The FENTRYR setting at suspension is different from that at resumption	0	1	0	0	1	0	0	0	0	0

Table 50.25 当BANKSEL.BANKSWP[2:0]为000b(2of2)时用户区域和块保护设置的关系

FSADDR[23:0]	块大小	块保护设置	用户区块号	Notes
下侧bank中的最后一个块地址	32 KB	BPS[n] or BPS_SEC[n]	Block 70 + n	在此启动银行开关设置中交换银行0和银行1
⋮	⋮	⋮	⋮	
0x01_8000 to 0x01_FFFF	32 KB	BPS[9] or BPS_SEC[9]	Block 79	
0x01_0000 to 0x01_7FFF	32 KB	BPS[8] or BPS_SEC[8]	Block 78	
0x00_E000 to 0x00_FFFF	8 KB	BPS[7] or BPS_SEC[7]	Block 77	
0x00_C000 to 0x00_DFFF	8 KB	BPS[6] or BPS_SEC[6]	Block 76	
⋮	⋮	⋮	⋮	
0x00_2000 to 0x00_3FFF	8 KB	BPS[1] or BPS_SEC[1]	Block 71	
0x00_0000 to 0x00_1FFF	8 KB	BPS[0] or BPS_SEC[0]	Block 70	

50.11.2 错误保护

错误保护检测非法FACI命令的发出、非法访问和闪存定序器故障。FACI命令接受被禁用（命令锁定状态）以响应检测到这些错误。闪存定序器处于命令锁定状态时，无法对闪存进行编程或擦除。要从命令锁定状态释放，请发出状态清除或强制停止命令。状态清除命令只能在FSTATR寄存器中的FRDY位为1时使用。无论FRDY位的值如何，都可以使用强制停止命令。当FAEINT寄存器中的CMDLKIE位为1时，如果闪存定序器进入命令锁定状态（FASTAT寄存器中的CMDLK位设置为1），则会产生闪存访问错误(FIFERR)中断。

如果闪存定序器在编程或擦除处理期间响应于除了PE暂停命令之外的命令而进入命令锁定状态，则闪存定序器继续进行编程或擦除处理。在这种状态下，PE挂起命令不能用于挂起编程或擦除处理。如果在命令锁定状态下发出命令，则ILGLERR位变为1，其他位保留先前错误检测设置的值。

表50.26显示了错误检测后的错误保护类型和状态位值。

Table 50.26 错误保护类型(1of3)

错误类型	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR设置错误	FENTRYR中设置的值不是0x0000、0x0001或0x0080	0	1	0	0	1	0	0	0	0	0
	暂停时的FENTRYR设置与恢复时的设置不同	0	1	0	0	1	0	0	0	0	0

Table 50.26 Error protection type (2 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Illegal command error	An undefined size is specified in the first cycle of the command. (not byte-write)	1	0	0	0	1	0	0	0	0	0
	An undefined code is written in the first access of the FACI command	1	0	0	0	1	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not 0xD0	1	0	0	0	1	0	0	0	0	0
	The value (N) specified in the second write access of the FACI command in the program or configuration set command is wrong	1	0	0	0	1	0	0	0	0	0
	Blank Check command is issued with inconsistent BCDIR, FSADDR, and FEADDR settings (see section 50.4.13. FEADDR : FACI Command End Address Register)	1	0	0	0	1	0	0	0	0	0/1 *1
	A multi block erase command is issued with inconsistent FSADDR and FEADDR settings. ● FSADDR > FEADDR ● FEADDR is set to reserved area.	1	0	0	0	1	0	0	0	0	0/1 *1
	An FACI command not acceptable in each mode is issued (see Table 50.16)	1	0	0	0	1	0	0	0	0	0
	An FACI command is issued when command acceptance conditions are not satisfied (see Table 50.17)	0/1	0/1	0/1	0/1	1	0/1	0/1	0/1	0/1	0/1
	A program or block erase command is issued against the area protected by the block protect setting (see section 50.11.1.3. Protection by Block Protect Setting)	1	0	0	0	1	0	0	0	0	0
	A program command is issued against the erase area in erase suspend	1	0	0	0	1	0	0	0	0	0
Erasure error	An error occurs during erasure	0	0	0	0	0	1	0	0	0	0
Programming error	An error occurs during programming	0	0	0	0	0	0	1	0	0	0
Code flash memory access violation	An FACI command is issued to the reserved portion of the user area in code flash P/E mode	0	0	0	0	1	0	0	0	1	0
	Configuration set command is issued to the reserved option-setting memory	0	0	0	0	1	0	0	0	1	0
	Configuration set command of non-secure access is issued to the secure region of TrustZone in the code flash	0	0	0	0	1	0	0	0	1	0
	Program or block erase command of non-secure access is issued to the secure region of user area.	0	0	0	0	1	0	0	0	1	0

Table 50.26 错误保护类型（2个，共3个）

错误类型	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
非法命令错误	在命令的第一个循环中指定了未定义的大小。（不是字节写入）	1	0	0	0	1	0	0	0	0	0
	在FACI命令的第一次访问中写入了未定义的代码	1	0	0	0	1	0	0	0	0	0
	多路访问FACI命令的最后一次访问指定的值不是0xD0	1	0	0	0	1	0	0	0	0	0
	程序或配置集命令中FACI命令的第二次写访问指定的值（N）错误	1	0	0	0	1	0	0	0	0	0
	使用不一致的BCDIR、FSADDR和FEADDR设置发出空白检查命令（请参阅第50.4.13节。 FEADDR:FACI命令结束地址 Register)	1	0	0	0	1	0	0	0	0	0/1 *1
	使用不一致的FSADDR和FEADDR设置发出多块擦除命令。● ● FEADDR设置为保留区域。	1	0	0	0	1	0	0	0	0	0/1 *1
	发出了在每种模式下都不可接受的FACI命令（参见表50.16）	1	0	0	0	1	0	0	0	0	0
	当命令接受条件不满足时发出FACI命令（见表50.17）	0/1	0/1	0/1	0/1	1	0/1	0/1	0/1	0/1	0/1
	对受块保护设置保护的区域发出编程或块擦除命令（请参阅第50.11.1.3节。块保护设置保护）	1	0	0	0	1	0	0	0	0	0
	在擦除挂起中针对擦除区域发出编程命令	1	0	0	0	1	0	0	0	0	0
擦除错误	擦除过程中发生错误	0	0	0	0	0	1	0	0	0	0
编程错误	编程过程中出现错误	0	0	0	0	0	0	1	0	0	0
代码闪存访问冲突	在代码闪存PE模式下，向用户区的保留部分发出FACI命令	0	0	0	0	1	0	0	0	1	0
	向保留的选项设置内存发出配置设置命令	0	0	0	0	1	0	0	0	1	0
	向代码闪存中的TrustZone的安全区域发出非安全访问的配置集命令	0	0	0	0	1	0	0	0	1	0
	对用户区的安全区域发出非安全访问的程序或块擦除命令。	0	0	0	0	1	0	0	0	1	0

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Table 50.26 Error protection type (3 of 3)

Error type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Data flash memory access violation	A program or block erase command is issued to the reserved data area in data flash P/E mode	0	0	0	0	1	0	0	0	0	1
	A multi block erase command is issued to the reserved data area in data flash P/E mode. (FSADDR is set to reserved data area).	1	0	0	0	1	0	0	0	0	1
	Blank Check command is issued to reserved data area in data flash P/E mode. (FSADDR is set to reserved data area).	1	0	0	0	1	0	0	0	0	1
	A program, block erase, multi block erase, or blank check command of non-secure access is issued to the secure region of data area.	0	0	0	0	1	0	0	0	0	1
Security error	Configuration set command for the SAS.BTFLG bit setting is issued when the SAS.FSPR bit is 0 (see section 50.9.3.15. Configuration Set Command)	0	0	1	0	1	0	0	0	0	0
Others	An FACI command-issuing area is accessed in read mode	0	0	0	1	1	0	0	0	0	0
	An FACI command-issuing area is read in code flash P/E mode or data flash P/E mode	0	0	0	1	1	0	0	0	0	0
Flash write erase protection error	A flash memory write protection error is detected by the FWEPROR register setting*2 during command processing by the flash sequencer	0	0	0	0	0	0/1	0/1	1	0	0

Note 1. DFAE value depends on the FSADDR setting.
Note 2. For details on the FWEPROR register, see section 50.4.8. FWEPROR : Flash P/E Protect Register.

50.11.3 Start-Up Program Protection

Protection of the startup program is for protection of the program to be started after a reset (the startup program). This function provides a way to safely update the startup program when rewriting is suspended during a reset.

The startup area is 8 Kbytes in size and is assigned to the user area in the code flash memory. This function uses the values of the SAS.BTFLG bit and the FSUACR.SAS[1:0] bits to change the area where the startup program is stored in block units (see Figure 50.26 to Figure 50.29).

In protection of the startup program, the state of the selection of the startup area can be fixed by the FSPR bit. However, the SAS.FSPR bit never be restored to 1 once the flag is set to 0. Exercise extra caution when handling the SAS.FSPR bit.

In addition, this protection cannot be used when dual mode is selected by the bank mode switching function (when the BANKMD[2:0] bits are 000b).

For details of SAS.FSPR bit and DUALSEL.BANKMD[2:0] bits, see section 6, Option-Setting Memory.

Table 50.26 错误保护类型（3之3）

错误类型	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
数据闪存访问违规	在数据闪存PE模式下，向保留数据区域发出程序或块擦除命令	0	0	0	0	1	0	0	0	0	1
	在数据闪存PE模式下，向保留数据区域发出多块擦除命令。（FSADDR设置为保留数据区）。	1	0	0	0	1	0	0	0	0	1
	在数据闪存PE模式下，向保留数据区域发出空白检查命令。（FSADDR设置为保留数据区）。	1	0	0	0	1	0	0	0	0	1
	向数据区域的安全区域发出非安全访问的编程、块擦除、多块擦除或空白检查命令。	0	0	0	0	1	0	0	0	0	1
安全错误	当SAS.FSPR位为0时，发出SAS.BTFLG位设置的配置设置命令（请参阅第50.9.3.15节。配置设置命令）	0	0	1	0	1	0	0	0	0	0
Others	以读取模式访问FACI命令发布区域	0	0	0	1	1	0	0	0	0	0
	在代码闪存PE模式或数据闪存PE模式下读取FACI命令发布区域	0	0	0	1	1	0	0	0	0	0
Flash写擦除保护错误	在闪存定序器的命令处理期间，通过FWEPROR寄存器设置*2检测到闪存写保护错误	0	0	0	0	0	0/1	0/1	1	0	0

注1.DFAE值取决于FSADDR设置。
注2.有关FWEPROR寄存器的详细信息，请参阅第50.4.8节。FWEPROR：闪存PE保护寄存器。

50.11.3 启动程序保护

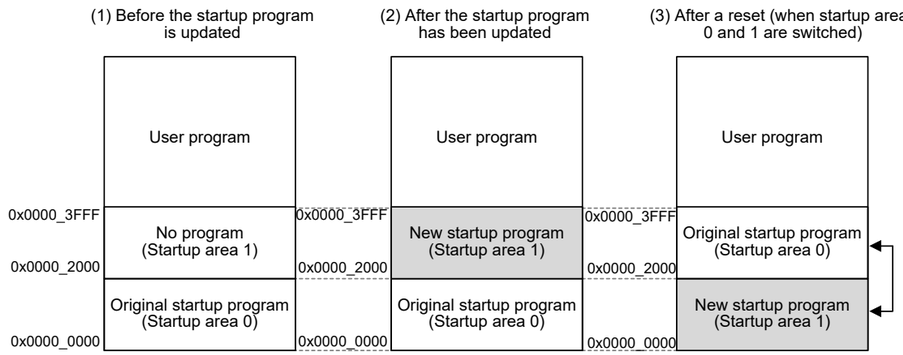
启动程序的保护是为了保护复位后要启动的程序（启动程序）。此功能提供了一种在复位期间暂停重写时安全更新启动程序的方法。

启动区大小为8KB，分配给代码闪存中的用户区。该函数使用SAS.BTFLG位和FSUACR.SAS[1:0]位的值来改变以块为单位存储启动程序的区域（见图50.26至图50.29）。

在启动程序的保护中，启动区域的选择状态可以通过FSPR位来固定。但是，那一旦标志设置为0，SAS.FSPR位永远不会恢复为1。处理SAS.FSPR位时要格外小心。

此外，当通过组模式切换功能选择双模式时（当BANKMD[2:0]位为000b)。

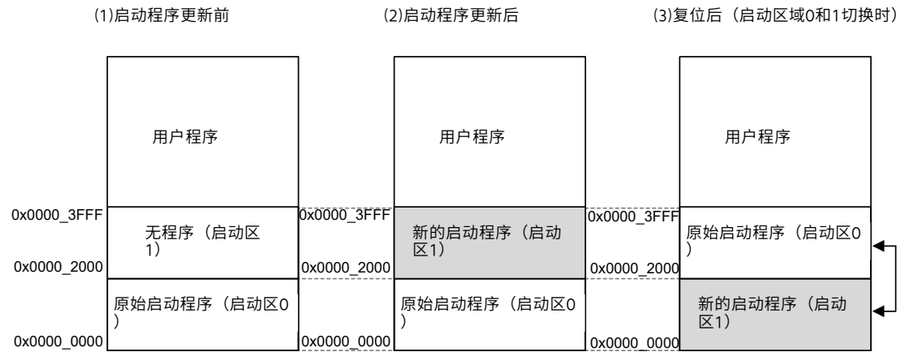
有关SAS.FSPR位和DUALSEL.BANKMD[2:0]位的详细信息，请参见第6节，选项设置存储器。



Note: The addresses are used for reading, programming, and erasure. Startup area 0 is erased when Block Erase command is issued for the address 0x00000000 with allocation shown under 3.

1. Before the startup program is updated
   When the SAS.BTFLG bit is 1 and the FSUACR.SAS[1:0] bits are 0xb, the address range from 0x00002000 to 0x00003FFF is selected as startup area 1 and the address range from 0x00000000 to 0x00001FFF is selected as startup area 0.
2. After the startup program has been updated
   A new startup program can be written to startup area 1. At this time, startup area 0 will still contain the previous startup program, so rewriting by starting up from startup area 0 remains possible if rewriting to the startup area 1 fails.
3. After a reset (when startup areas 0 and 1 are switched)
   When rewriting startup area 1 is successfully completed, switch the assignment of startup areas 0 and 1 by rewriting the startup area selection bit (the SAS.BTFLG bit) with Configuration set command. Afterwards, the program is started up from startup area 1 after a reset.

Figure 50.26 Concept of Protection of the Startup Program



Note: 这些地址用于读取、编程和擦除。当对地址0x00000000发出块擦除命令时，启动区域0被擦除，分配如下3所示。1.更新启动程序之前

当SAS.BTFLG位为1且FSUACR.SAS[1:0]位为0xb时，选择0x00002000到0x00003FFF的地址范围作为启动区1，选择从0x00000000到0x00001FFF的地址范围作为启动区0。2.启动程序更新后

可以将新的启动程序写入启动区1。此时启动区0仍会包含之前的启动程序，因此如果对启动区1的重写失败，仍然可以从启动区0启动进行重写。3.复位后（启动区域0和1切换时）

成功完成启动区1的重写后，通过Configurationset命令重写启动区选择位（SAS.BTFLG位）来切换启动区0和1的分配。之后，程序在复位后从启动区1启动。

Figure 50.26 保护启动程序的概念

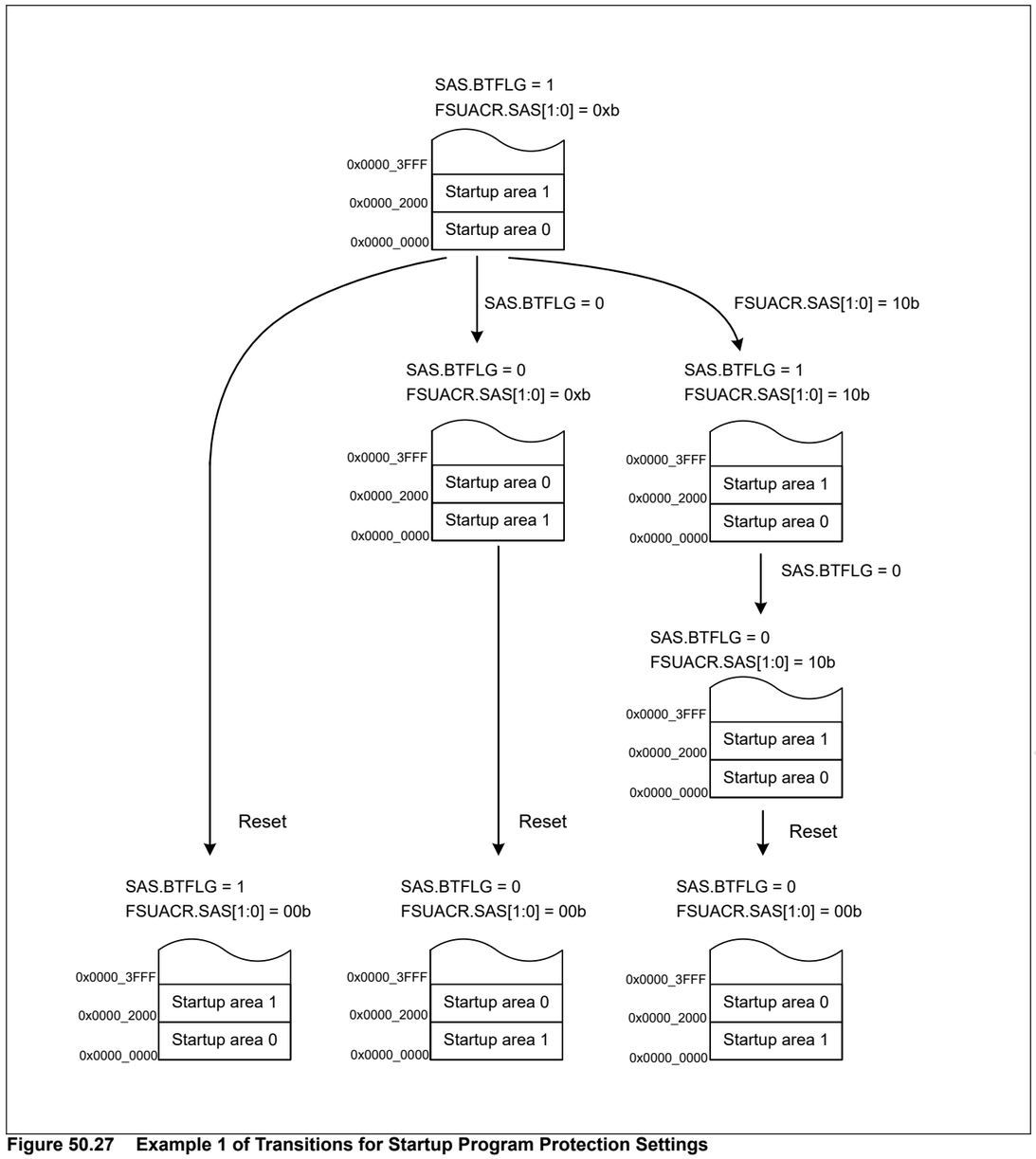


Figure 50.27 Example 1 of Transitions for Startup Program Protection Settings

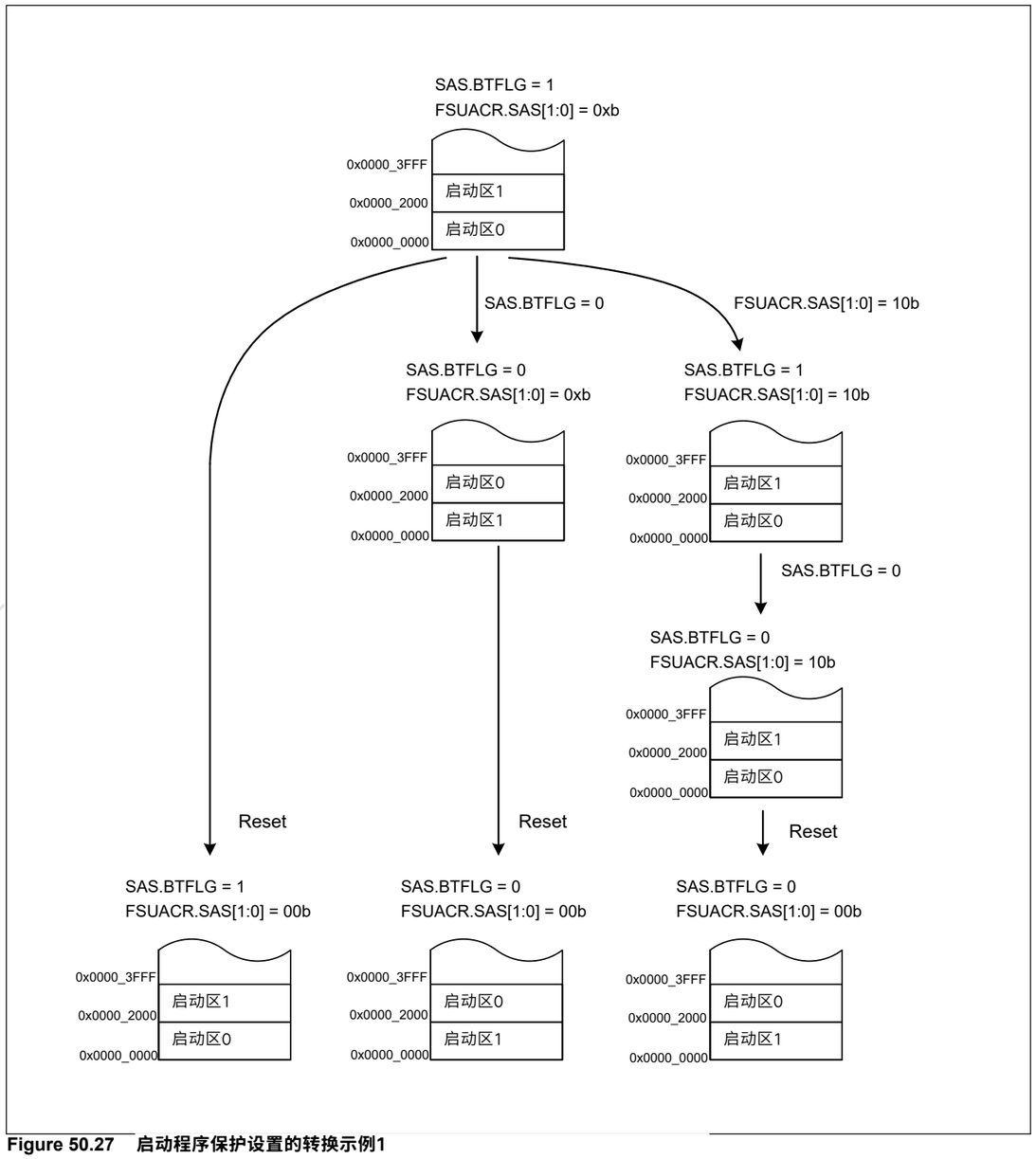


Figure 50.27 启动程序保护设置的转换示例1

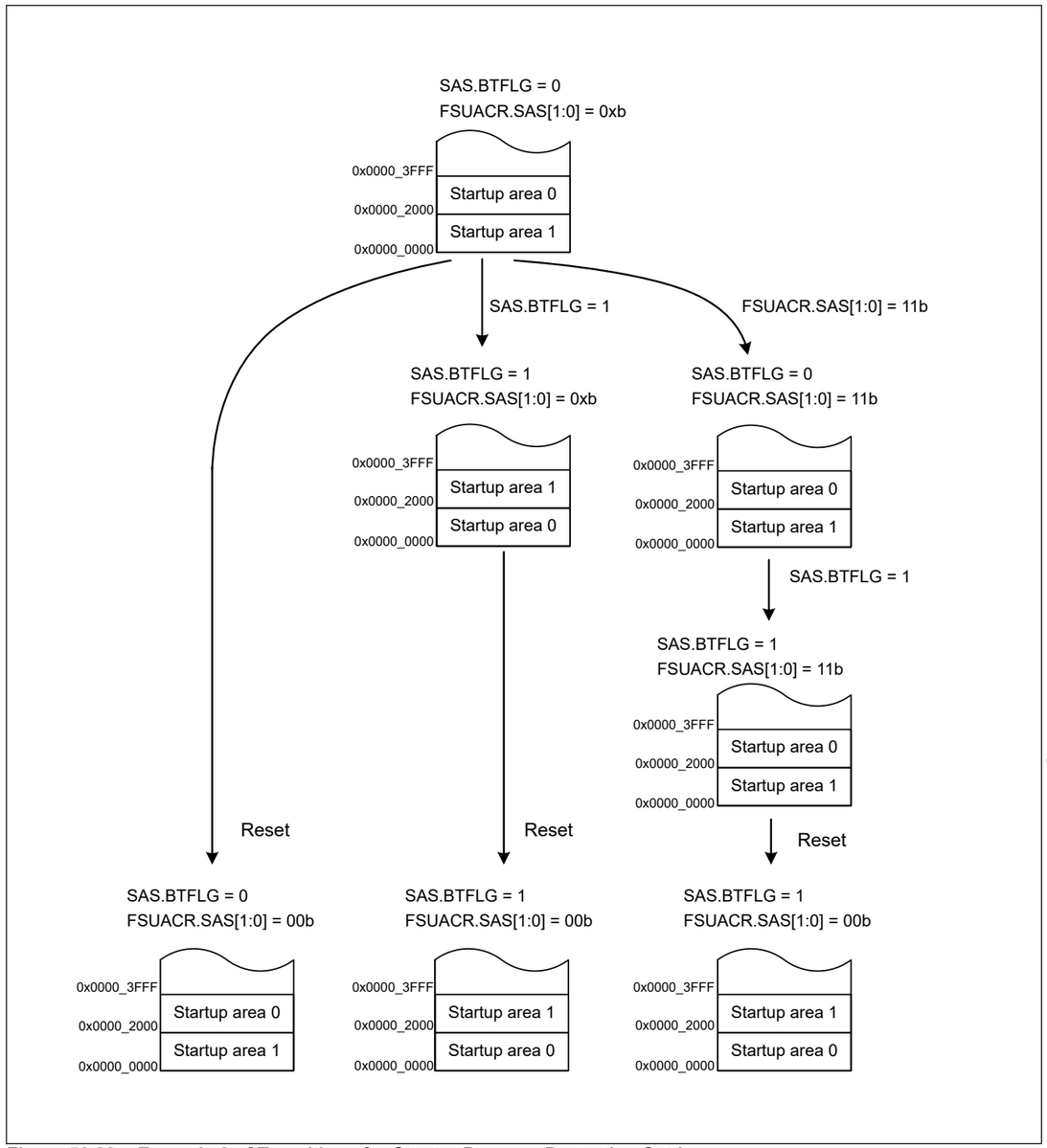


Figure 50.28 Example 2 of Transitions for Startup Program Protection Settings

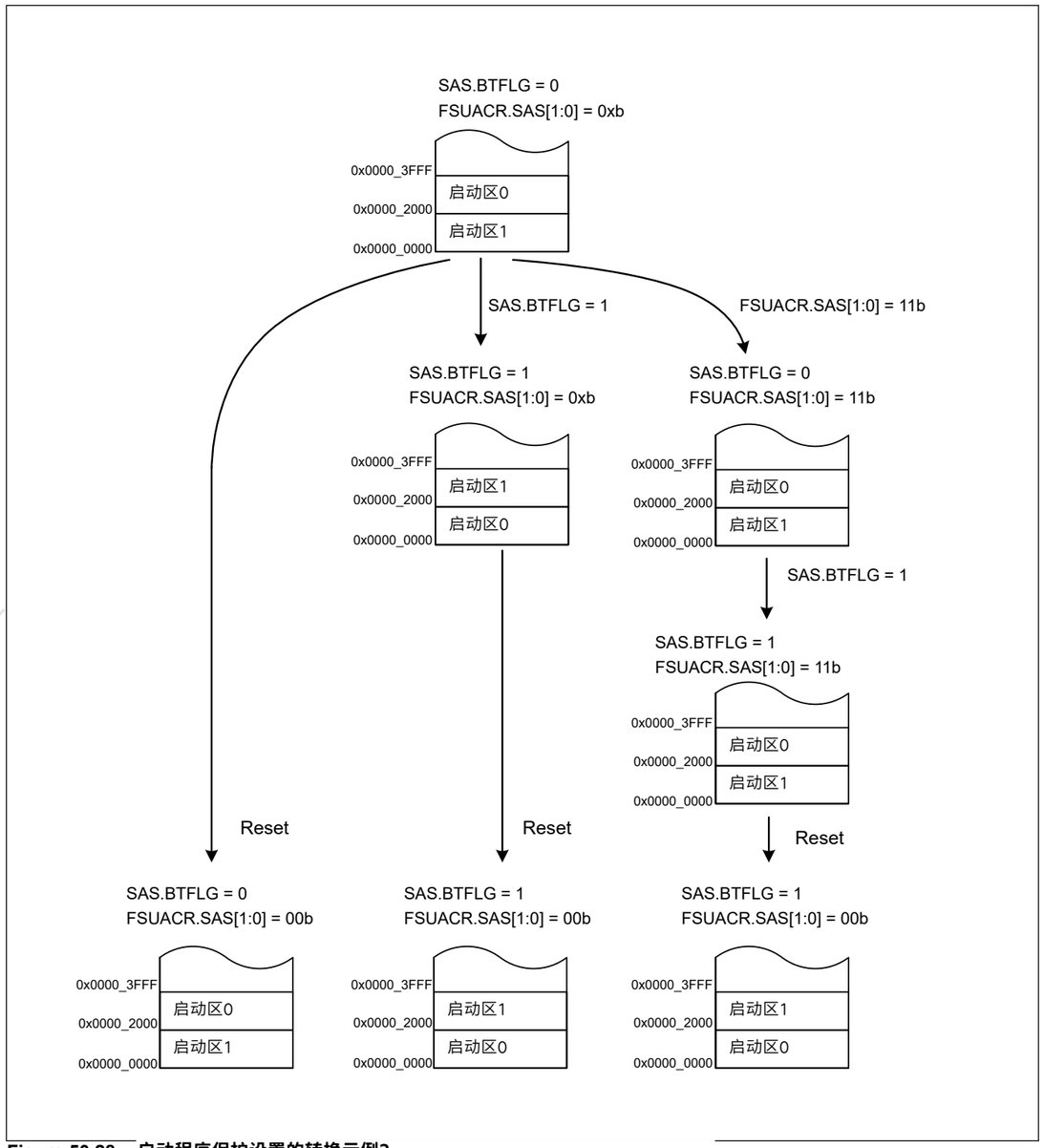
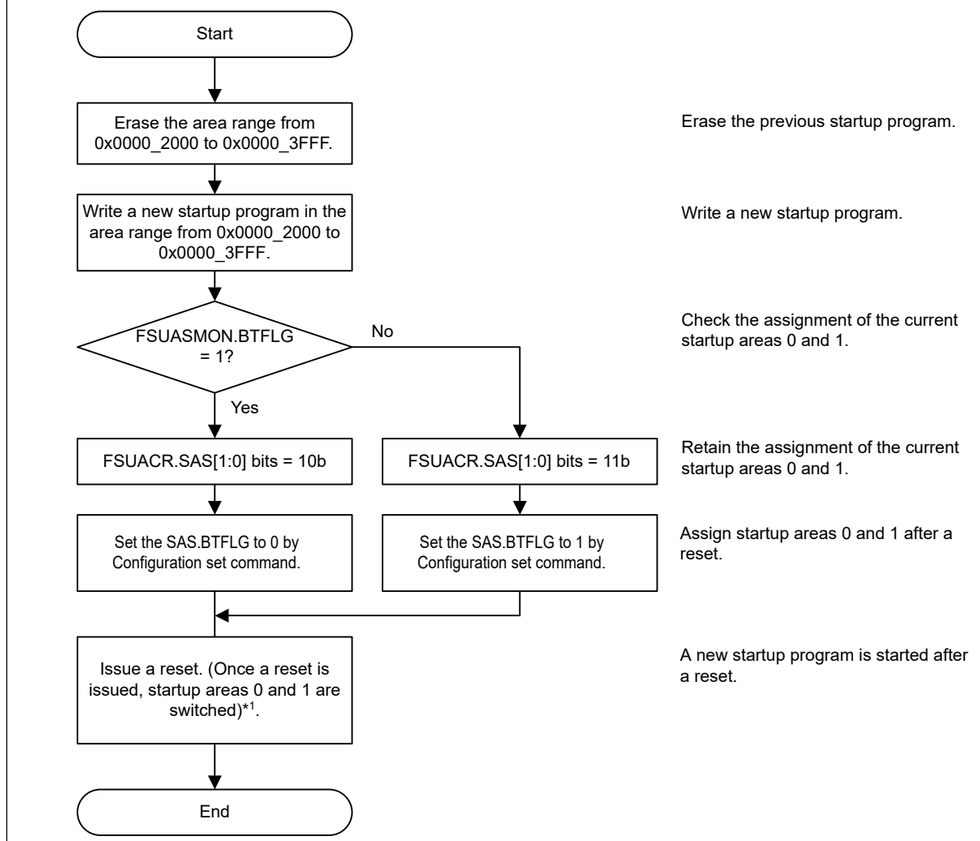


Figure 50.28 启动程序保护设置的转换示例2



Note 1. For details, see Figure 50.27 and Figure 50.28.

Figure 50.29 Concept of Protection of the Startup Program

50.11.4 Dual Bank Function

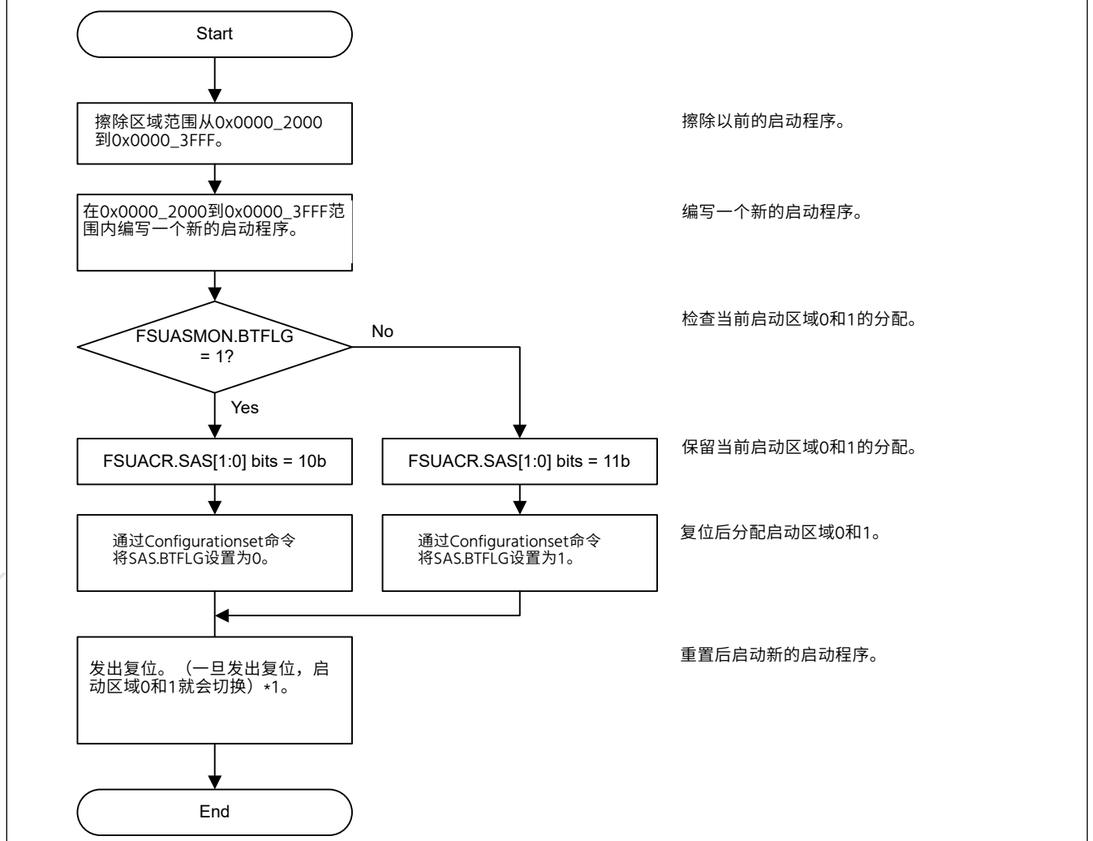
This protection uses the functions of bank mode switching and startup bank selection to update a program while a user program is running and to provide a safe method of updating in cases where programming is suspended during a reset.

50.11.4.1 Switching Bank Modes

The bank mode switching function selects either linear mode in which the user area in the code flash memory is used as one area, or dual mode in which the user area is divided into two bank areas. Figure 50.30 shows an example of flow of switching bank modes. A reset after setting the DUALSEL.BANKMD[2:0] bits in the option setting memory determines the mode of the bank mode switching function. Selecting dual mode enables the startup bank selection function.

When dual mode is selected by bank mode switching function (the DUALSEL.BANKMD[2:0] bits are 000b), start-up program protection function cannot be used.

For details of DUALSEL.BANKMD[2:0] bits, see section 6, Option-Setting Memory.



注1.详见图50.27和图50.28。

Figure 50.29 保护启动程序的概念

50.11.4 双银行功能

该保护使用存储区模式切换和启动存储区选择功能在用户程序运行时更新程序，并在复位期间编程暂停的情况下提供安全的更新方法。

50.11.4.1 切换银行模式

存储体模式切换功能选择将代码闪存中的用户区域用作一个区域的线性模式或将用户区域划分为两个存储体区域的双重模式。图50.30显示了切换存储区模式的流程示例。设置选项设置存储器中的DUALSEL.BANKMD[2:0]位后的复位决定了组模式切换功能的模式。选择双模式启用启动库选择功能。

当通过组模式切换功能（DUALSEL.BANKMD[2:0]位为000b）选择双模式时，不能使用启动程序保护功能。

有关DUALSEL.BANKMD[2:0]位的详细信息，请参阅第6节，选项设置存储器。

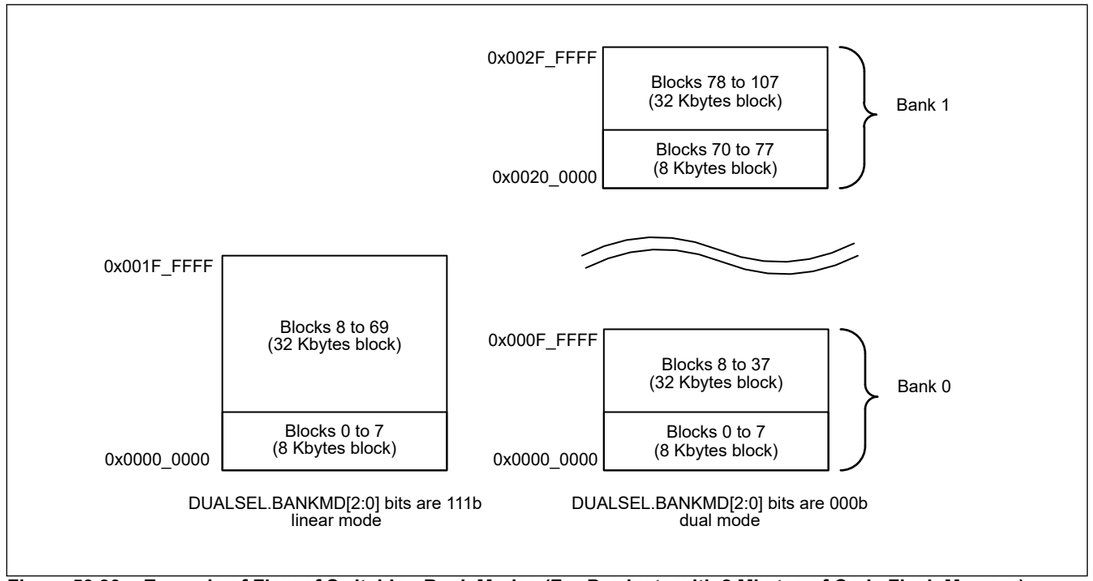


Figure 50.30 Example of Flow of Switching Bank Modes (For Products with 2 Mbytes of Code Flash Memory)

50.11.4.2 Selecting the Startup Bank

Startup bank selection provides a way to safely update the program by selecting a bank area to be started in dual mode (when the DUALSEL.BANKMD[2:0] bits are 000b) when programming is suspended during a reset. Figure 50.31 is a schematic view of startup bank selection and Table 50.27 shows an example of the flow of startup bank selection. A reset after setting the value of the BANKSEL.BANKSWP[2:0] bits in the option-setting memory changes the addresses of banks 0 and 1 and booting up a program proceeds from the updated area. When the address is switched by using startup bank selection, the programming/erasure target for the FACI commands is also switched. This function is invalid in linear mode.

For details of DUALSEL.BANKMD[2:0] bits and BANKSEL.BANKSWP[2:0] bits, see section 6, Option-Setting Memory.

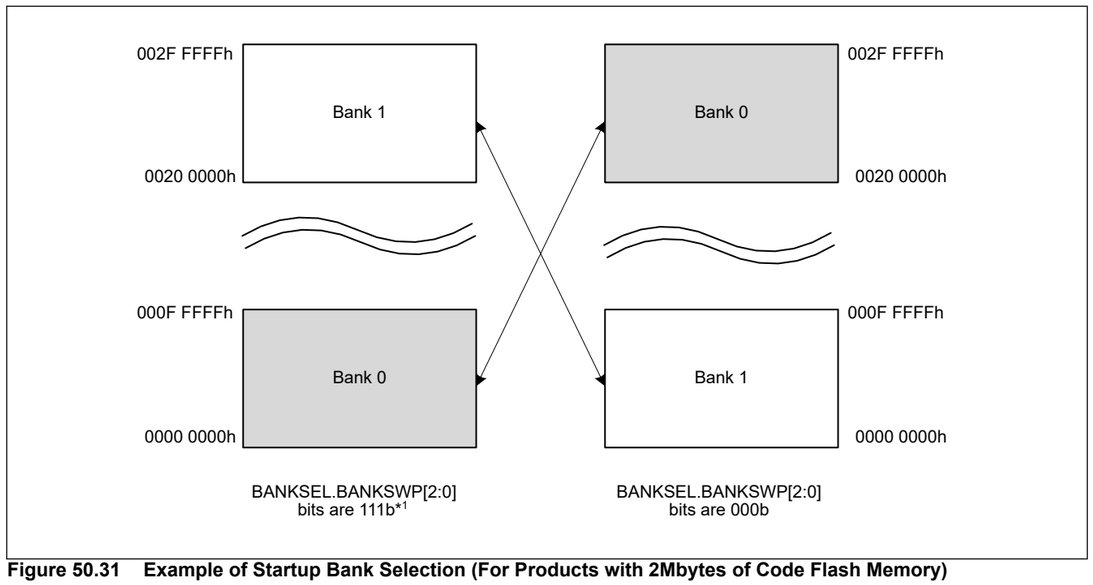


Figure 50.31 Example of Startup Bank Selection (For Products with 2Mbytes of Code Flash Memory)

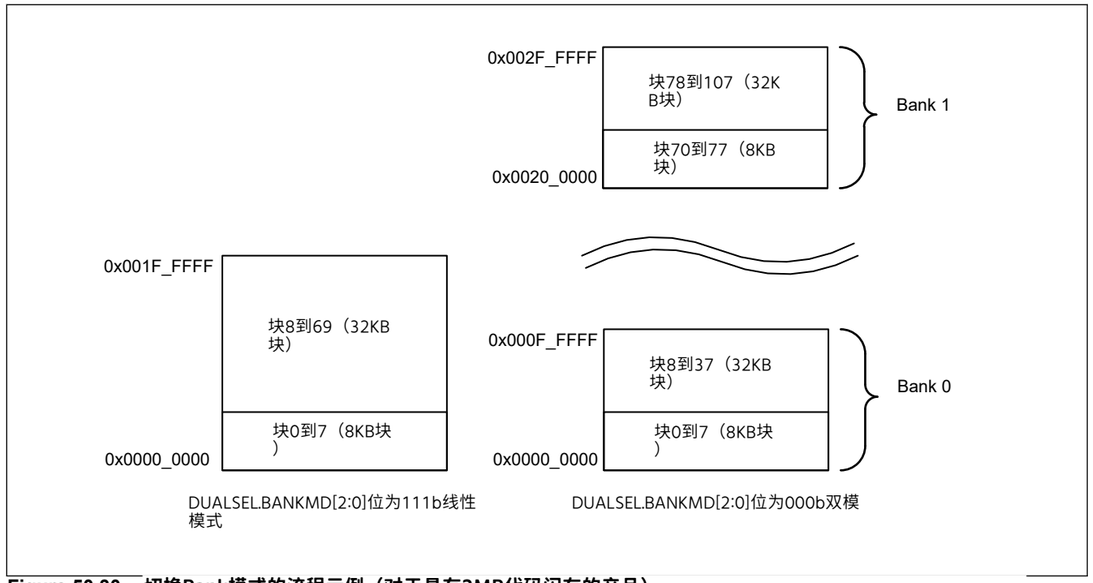


Figure 50.30 切换Bank模式的流程示例（对于具有2MB代码闪存的产品）

50.11.4.2 选择启动银行

启动存储区选择提供了一种安全更新程序的方法，方法是在复位期间暂停编程时选择要以双模式启动的存储区（当DUALSEL.BANKMD[2:0]位为000b时）。图50.31是启动银行选择的示意图，表50.27显示了启动银行选择流程的示例。设置选项设置存储器中BANKSEL.BANKSWP[2:0]位的值后复位会更改存储体0和1的地址，并从更新的区域启动程序。当使用启动库选择切换地址时，FACI命令的编程擦除目标也被切换。该功能在线性模式下无效。

有关DUALSEL.BANKMD[2:0]位和BANKSEL.BANKSWP[2:0]位的详细信息，请参见第6节，选项设置存储器。

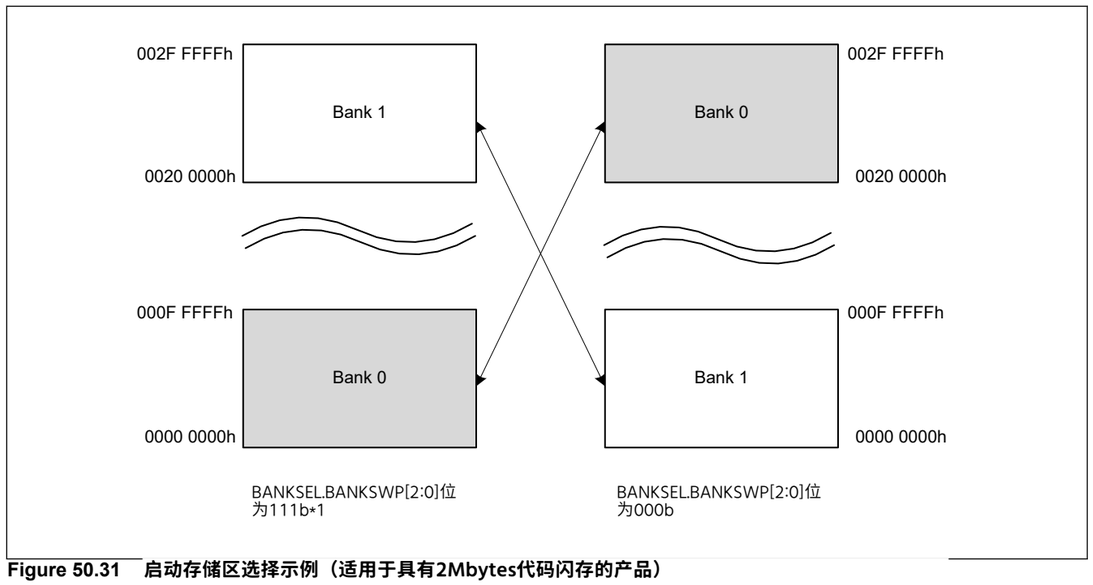


Figure 50.31 启动存储区选择示例（适用于具有2Mbytes代码闪存的产品）

Table 50.27 Example of Startup Bank Selection Flow (For Products with 2 Mbytes of Code Flash Memory)

No.	Step Name	Description
1	Erase block	Erase blocks to be programed in the address range from 0x0020_0000 to 0x002F_FFFF
2	Program a new software	Program a new software in the address range from 0x0020_0000 to 0x002F_FFFF
3	Read the value	Read the value of the BANKSEL.BANKSWP[2:0] bits.
4	Write an inverted value	Write an inverted value in the BANKSEL.BANKSWP[2:0] bits*1.
5	Issue a reset	Issue a reset (A reset switches the banks.)

Note 1. Set the inverse of the read value of the BANKSEL.BANKSWP[2:0] bits (000b or 111b).

50.11.5 Block Swap Function

This protection uses the functions of block swap selection to update a program while a user program is running and to provide a safe method of updating in cases where programming is suspended during a reset.

50.11.5.1 Selecting the Block Swap

Block swap selection provides a way to safely update the program when programming is suspended during a reset. Figure 50.32 is a schematic view of block swap selection and Figure 50.33 shows an example of the flow of block swap selection. A reset after setting the value of the BANKSEL.BLCKSWP bit in the option-setting memory changes the addresses of block A and B. When the address is switched, the Programming/erasure target for the FACI commands is also switched.

In addition, this protection cannot be used when dual mode is selected by the bank mode switching function (when the DUALSEL.BANKMD[2:0] bits are 000b).

For details of DUALSEL.BANKMD[2:0] bits and BANKSEL.BLCKSWP bit, see section 6, Option-Setting Memory.

Table 50.27 启动Bank选择流程示例（适用于具有2MB代码闪存的产品）

No.	步骤名称	Description
1	擦除块	擦除从0x0020_0000到0x002F_FFFF的地址范围内要编程的块
2	编写新软件	在0x0020_0000到0x002F_FFFF的地址范围内编写一个新软件
3	读取值	读取值 BANKSEL.BANKSWP[2:0] bits.
4	写一个反转的值	在 BANKSEL.BANKSWP[2:0] bits*1.
5	发出重置	发出复位（复位切换组。）

注1.设置BANKSEL.BANKSWP[2:0]位（000b或111b）的读取值的倒数。

50.11.5 区块交换功能

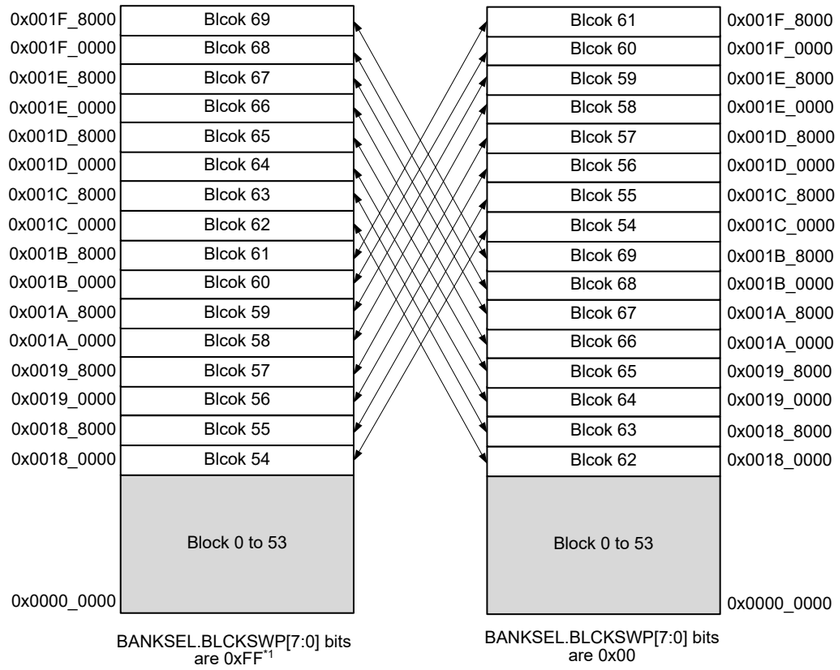
此保护使用块交换选择功能在用户程序运行时更新程序，并在复位期间暂停编程的情况下提供安全的更新方法。

50.11.5.1 选择块交换

块交换选择提供了一种在复位期间编程暂停时安全更新程序的方法。图50.32是块交换选择的示意图，图50.33显示了块交换选择流程的示例。设置选项设置存储器中的BANKSEL.BLCKSWP位的值后的复位会改变块A和B的地址。当地址切换时，FACI命令的编程擦除目标也会切换。

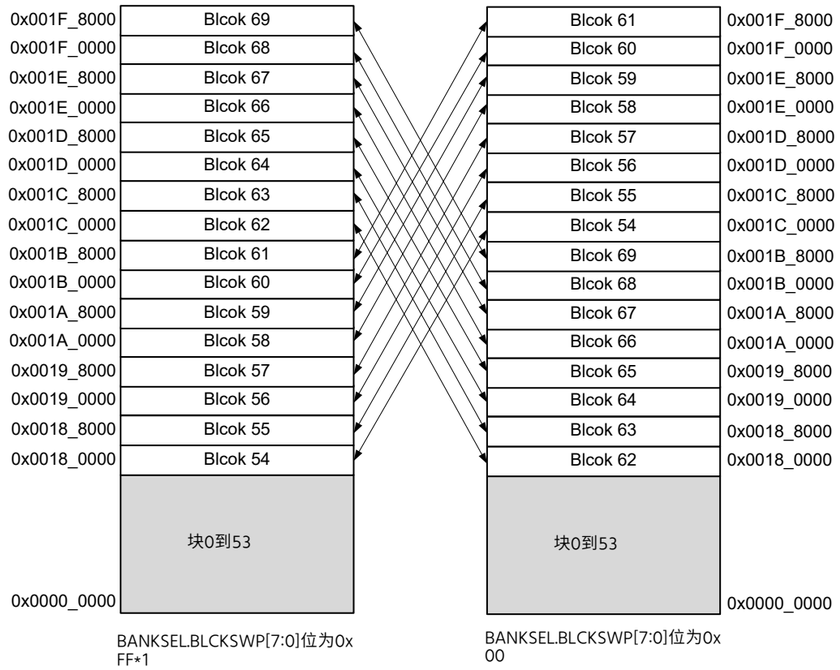
此外，当通过组模式切换功能选择双模式时（当DUALSEL.BANKMD[2:0]位为000b）。

有关DUALSEL.BANKMD[2:0]位和BANKSEL.BLCKSWP位的详细信息，请参见第6节，选项设置存储器。



Note 1. For products without setting of the option-setting memory, the BANKSEL.BLCKSWP[7:0] bits are 1111b

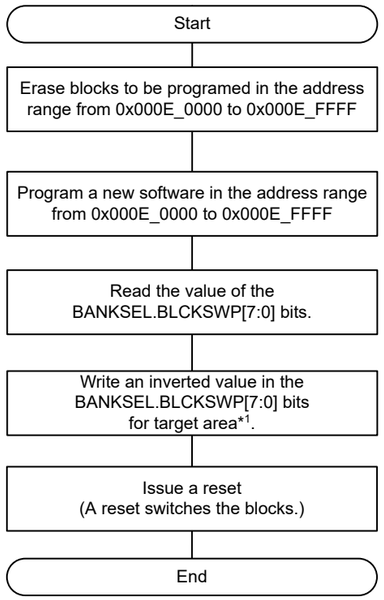
Figure 50.32 Example of Block Swap Selection (For Products with 2 Mbytes of Code Flash Memory)



注1.对于没有设置选项设置存储器的产品，BANKSEL.BLCKSWP[7:0]位为1111b

Figure 50.32 块交换选择示例（适用于具有2MB代码闪存的产品）

RA生态工作室



Note 1. See Table 6.2 for the correspondence between the target region and the BANKSEL.BLCKSWP[7:0] bit.

Figure 50.33 Example of Block Swap Selection Flow (For Products with 2 Mbytes of Code Flash Memory)

50.12 Security Function

The flash sequencer supports the following security functions:

- Security flag for startup area
- Permanent block protect setting
- Flash memory protection for TrustZone

50.12.1 Security Flag for Startup Area Select

The security flag (SAS.FSPR) for the startup area is located in the option-setting memory.

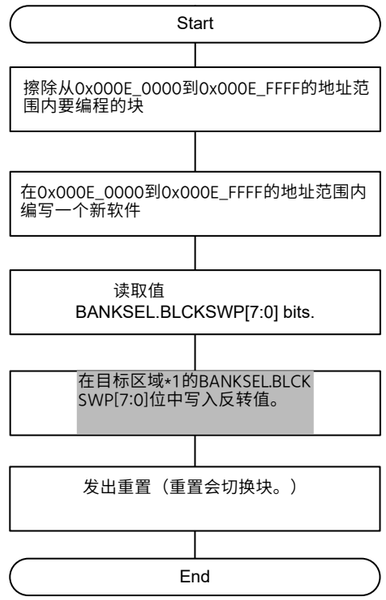
When the SAS.FSPR bit is 0, issuing the configuration set command to change the SAS.BTFLG bit causes the flash sequencer to be in the command-locked state. Also, when the SAS.FSPR bit is 0, it is invalid to write to the Startup Area Select bits SAS[1:0] in the FSUACR register. The SAS.FSPR bit enables protection.

50.12.2 Permanent Block Protect Setting

The permanent block protect setting is the clear protection for the block protection setting. User area cannot be permanently updated by the FACI command when the permanent block protect setting is enabled. See section 50.11.1.3. Protection by Block Protect Setting for more details.

The block protect setting and the permanent block protect setting have the write/clear protection against the configuration set command. The flash sequencer does not detect an error when the configuration set command is issued to the write/clear protected settings.

Figure 50.34 and Table 50.28 show the write/clear protection against the block protect setting (BPS[n]) and the permanent protect setting (PBPS[n]). Figure 50.35 and Table 50.29 show the write/clear protection against the block protect setting for secure (BPS_SEC[n]) and permanent protect setting for secure (PBPS_SEC[n]).



注1.目标区域与BANKSEL.BLCKSWP[7:0]位的对应关系见表6.2。

Figure 50.33 块交换选择流程示例（适用于具有2MB代码闪存的产品）

50.12 安全功能

闪存定序器支持以下安全功能：

●启动区安全标志

●永久封锁保护设置

●TrustZone的闪存保护

50.12.1 启动区域选择的安全标志

启动区域的安全标志(SAS.FSPR)位于选项设置内存中。

当SAS.FSPR位为0时，发出配置设置命令来更改SAS.BTFLG位会导致闪存定序器处于命令锁定状态。此外，当SAS.FSPR位为0时，写入FSUACR寄存器中的启动区域选择位SAS[1:0]无效。SAS.FSPR位启用保护。

50.12.2 永久块保护设置

永久块保护设置是对块保护设置的明确保护。启用永久块保护设置后，FACI命令无法永久更新用户区域。请参阅第50.11.1.3节。通过块保护设置进行保护以获取更多详细信息。

块保护设置和永久块保护设置具有针对配置集命令的写清除保护。向写清除保护设置发出配置设置命令时，闪存定序器不会检测到错误。

图50.34和表50.28显示了针对块保护设置(BPS[n])和永久保护设置(PBPS[n])的写清除保护。图50.35和表50.29显示了针对安全的块保护设置(BPS_SEC[n])和安全的永久保护设置(PBPS_SEC[n])的写清除保护。

Effective permanent block protect setting (PBPS or PBPS_SEC) depends on block protect select (BPS_SEL). For details of permanent block protect setting (PBPS or PBPS_SEC) and block protect select (BPS_SEL), see section 6, Option-Setting Memory.

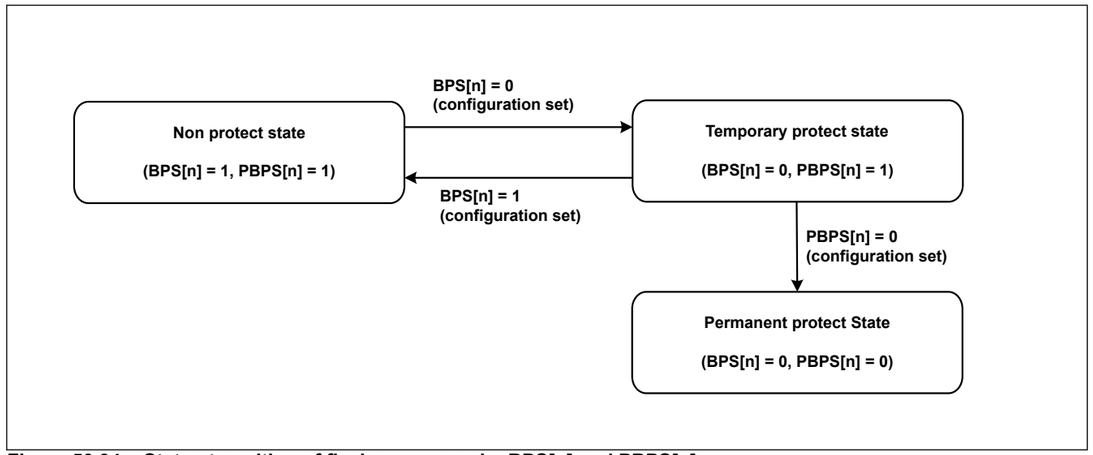


Figure 50.34 Status transition of flash sequencer by BPS[n] and PBPS[n]

Table 50.28 Write/clear protection of BPS[n] and PBPS[n]

Current state		Updatable state by configuration set command			
BPS[n]	PBPS[n]	BPS[n] = 1	BPS[n] = 0	PBPS[n] = 1	PBPS[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- ✓ indicates updatable by configuration set command.
- X indicates not updatable by configuration set command (error does not occur).
- — indicates not reaching to this state.

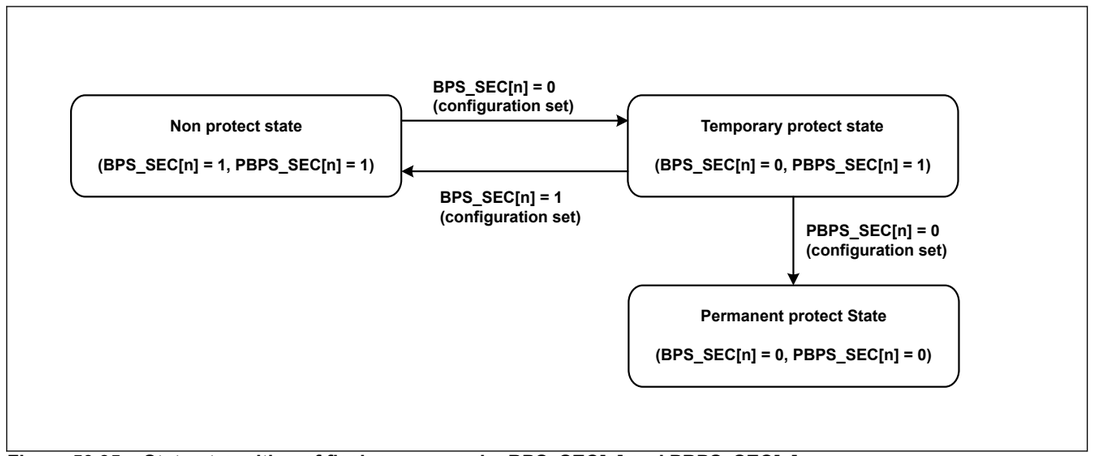


Figure 50.35 Status transition of flash sequencer by BPS_SEC[n] and PBPS_SEC[n]

有效的永久块保护设置（PBPS或PBPS_SEC）取决于块保护选择（BPS_SEL）。有关永久块保护设置（PBPS或PBPS_SEC）和块保护选择（BPS_SEL）的详细信息，请参见第6节，选项设置存储器。

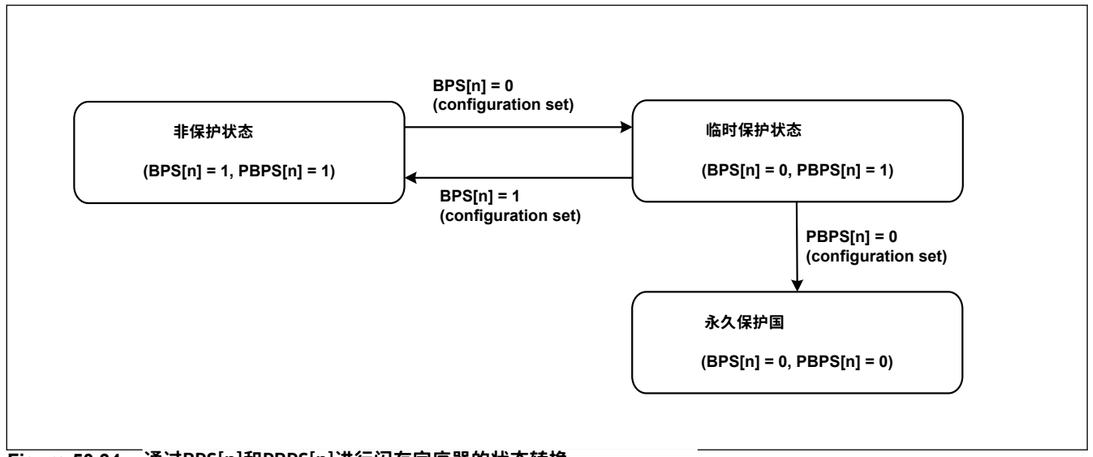


Figure 50.34 通过BPS[n]和PBPS[n]进行闪存定序器的状态转换

Table 50.28 BPS[n]和PBPS[n]的写清除保护

当前状态		可通过配置设置命令更新状态			
BPS[n]	PBPS[n]	BPS[n] = 1	BPS[n] = 0	PBPS[n] = 1	PBPS[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- 表示可通过配置设置命令更新。
- X表示不能通过配置设置命令更新（不发生错误）。
- —表示未达到此状态。

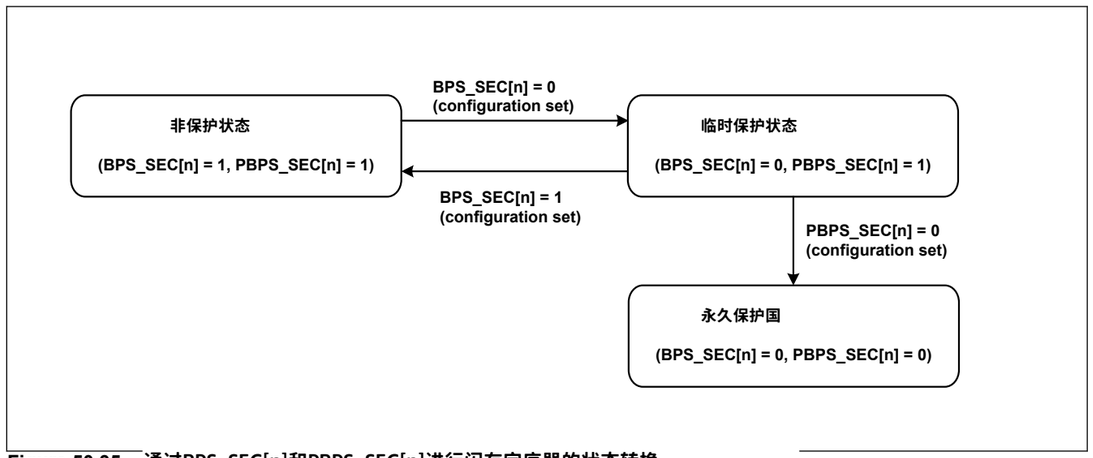


Figure 50.35 通过BPS_SEC[n]和PBPS_SEC[n]进行闪存定序器的状态转换

Table 50.29 Write/clear protection of BPS_SEC[n] and PBPS_SEC[n]

Current state		Updatable state by configuration set command			
BPS_SEC[n]	PBPS_SEC[n]	BPS_SEC[n] = 1	BPS_SEC[n] = 0	PBPS_SEC[n] = 1	PBPS_SEC[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- ✓ indicates updatable by configuration set command.
- X indicates not updatable by configuration set command (error does not occur).
- — indicates not reaching to this state.

50.12.3 Flash Memory Protection for TrustZone

Information in this section focuses on the flash sequencer operation.

The flash memory provides the following types of protect function against non-secure access:

- Protection for flash memory area (P/E)
- Protection for flash memory area (read)
- Protection for registers
- Protection during FACI command operation
- Code flash P/E mode entry protection

50.12.3.1 Protection for Flash Memory Area (P/E)

This function protects the secure region of the code flash and data flash from FACI commands of non-secure access. The condition of protection depends on the FACI command, the access attribution, and the memory boundary setting.

For details of secure region, see section 52, Security Features .

See Table 50.30 for information on protection of the flash memory area (P/E).

Table 50.30 Protection for the flash memory area (P/E)

FACI command	Target area		Issuing of FACI command by non-secure access	Issuing of FACI command by secure access
Program Block erase	Code flash memory	User area (non-secure area)	✓	✓
		User area (secure area)	X	✓
	Data flash memory	Data area (non-secure area)	✓	✓
		Data area (secure area)	X	✓
Multi block erase Blank check	Data flash memory	Data area (non-secure area)	✓	✓
		Data area (secure area)	X	✓
Configuration set	Code flash memory	option-setting memory (non-secure area)	✓	✓
		option-setting memory (secure area)	X	✓

Note:
- ✓ indicates FACI command operation is not prohibited.
- X indicates FACI command operation is prohibited. Error occurs when the area is selected, and the FACI command is executed.

When the target area of FACI command is the user area of code flash, the flash sequencer compares the FSADDR register setting with the memory boundary setting of the code flash and determines whether the target area is in the secure region.

In linear mode, the memory boundary can be set to 0x0000_0000 to 0x00FF_8000 in 32 KB unit.

In dual mode, the memory boundary can be set to 0x0000_0000 to 0x0020_0000 in 32 KB unit. When the memory boundary is set to 0x0020_0000 or greater in the dual mode, the entire user area is defined as the secure region.

Figure 50.36 shows details of the non-secure/secure attribute of user area in the code flash.

Table 50.29 BPS_SEC[n]和PBPS_SEC[n]的写清除保护

当前状态		可通过配置设置命令更新状态			
BPS_SEC[n]	PBPS_SEC[n]	BPS_SEC[n] = 1	BPS_SEC[n] = 0	PBPS_SEC[n] = 1	PBPS_SEC[n] = 0
1	1	✓	✓	✓	X
1	0	—	—	—	—
0	1	✓	✓	✓	✓
0	0	X	✓	X	✓

Note:
- 表示可通过配置设置命令更新。
- X表示不能通过配置设置命令更新（不发生错误）。
- —表示未达到此状态。

50.12.3 TrustZone的闪存保护

本节中的信息侧重于闪存定序器的操作。

闪存提供以下类型的保护功能以防止非安全访问：

- ●保护闪存区（PE）
- ●保护闪存区域（读取）
- ●寄存器保护
- ●FACI命令操作期间的保护
- ●CodeflashPE模式进入保护

50.12.3.1 对闪存区域(PE)的保护

此功能保护代码闪存和数据闪存的安全区域免受非安全访问的FACI命令的影响。保护条件取决于FACI命令、访问属性和内存边界设置。

有关安全区域的详细信息，请参阅第52节，安全功能。

有关保护闪存区域(PE)的信息，请参见表50.30。

Table 50.30 对闪存区域(PE)的保护

FACI命令	目标区域		通过非安全访问发出FACI命令	通过安全访问发出FACI命令
Program 块擦除	代码闪存	用户区（非安全区）	✓	✓
		用户区（安全区）	X	✓
	数据闪存	数据区（非安全区）	✓	✓
		数据区（安全区）	X	✓
多块擦除 空白支票	数据闪存	数据区（非安全区）	✓	✓
		数据区（安全区）	X	✓
配置集	代码闪存	option-setting memory (non-secure area)	✓	✓
		option-setting memory (secure area)	X	✓

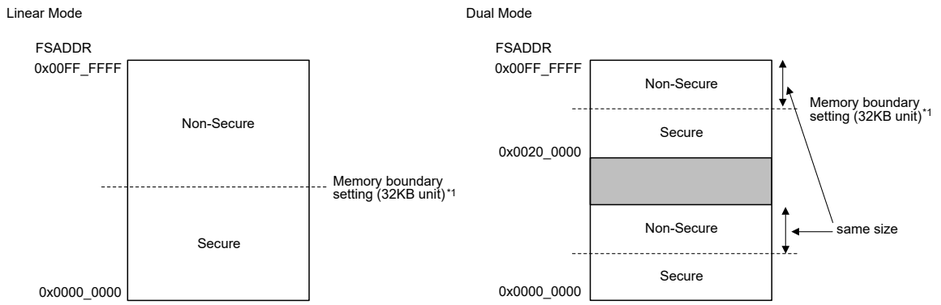
Note:
- 表示不禁止FACI命令操作。
- X表示禁止FACI命令操作。选择区域时发生错误，执行FACI命令。

当FACI命令的目标区域是代码闪存的用户区域时，闪存定序器将FSADDR寄存器设置与代码闪存的内存边界设置进行比较，并确定目标区域是否在安全区域中。

在线性模式下，内存边界可以以32KB为单位设置为0x0000_0000到0x00FF_8000。

在双模式下，内存边界可以以32KB为单位设置为0x0000_0000到0x0020_0000。当内存边界在双模式下设置为0x0020_0000或更大时，整个用户区域被定义为安全区域。

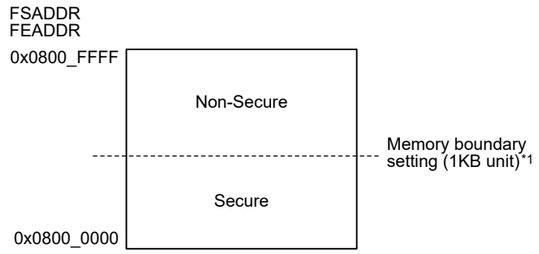
图50.36显示了代码flash中用户区的非安全安全属性的详细信息。



Note 1. Comparing FSADDR with memory boundary setting of user area and judges whether the target area is in secure area.

Figure 50.36 Secure/non-secure region in user area

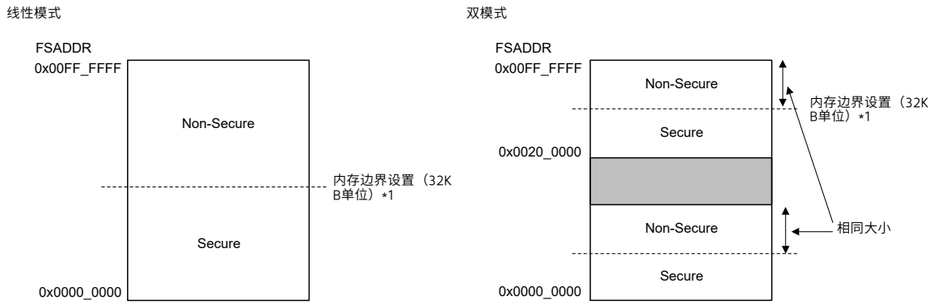
When the target area of the issuing FACI command is the data area of data flash, the flash sequencer compares the FSADDR/FEADDR register setting with the memory boundary setting of the data flash and determines whether the target area is in secure region. The memory boundary can be set to 0x0800_0000 to 0x0800_FC00 in 1 KB unit. Figure 50.37 shows details of the non-secure/secure attribute of data area in the data flash.



Note 1. Comparing FSADDR/FEADDR with memory boundary setting of data area and judges whether the target area is in secure area.

Figure 50.37 Secure/non-secure region in data area

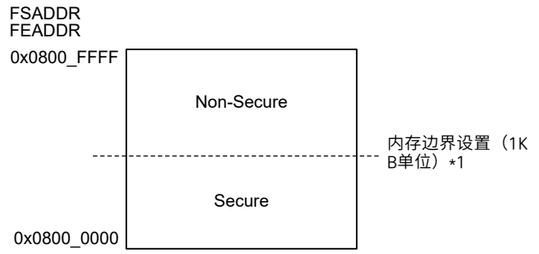
See Figure 50.38 in the details of non-secure/secure region of option-setting memory. The flash sequencer judges that target area is secure region from the FSADDR register setting.



注1.将FSADDR与用户区的内存边界设置进行比较，判断目标区是否在安全区。

Figure 50.36 用户区域中的安全非安全区域

当发出FACI命令的目标区域是数据flash的数据区域时，flashsequencer比较FSADDRFEADDR寄存器设置与数据闪存的内存边界设置并确定目标区域是否在安全区域中。内存边界可以以1KB为单位设置为0x0800_0000到0x0800_FC00。图50.37显示了数据闪存中数据区域的非安全安全属性的详细信息。



注1.将FSADDRFEADDR与数据区域的内存边界设置进行比较，判断目标区域是否在安全区域。

Figure 50.37 数据区域中的安全非安全区域

有关选项设置内存的非安全安全区域的详细信息，请参见图50.38。闪存定序器根据FSADDR寄存器设置判断目标区域是安全区域。

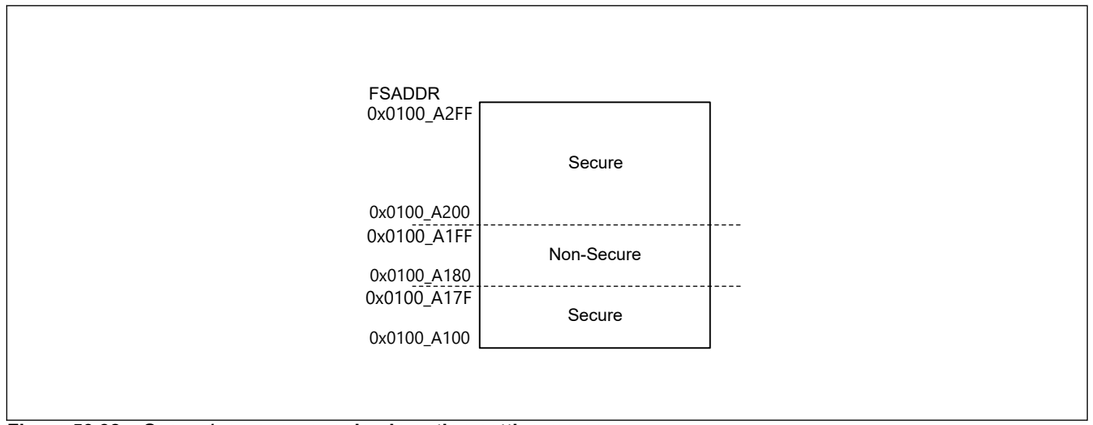


Figure 50.38 Secure/non-secure region in option-setting memory

50.12.3.2 Protection for Flash Memory Area (Read)

This function protects the secure region of code flash and data flash from non-secure bus access.

For details of secure region, see section 52, Security Features .

50.12.3.3 Protection for Register

The flash sequencer registers have write-access protection against non-secure access. Table 50.31 shows details of the protected registers of the flash sequencer.

Table 50.31 Protected registers of the flash sequencer for TrustZone

Protection target register	Security attribute setting	Notes
FCKMHZ	Security attribution register setting (FSAR.FCKMHZSA)	See section 50.4.4. FSAR : Flash Security Attribution Register
FMEPROT	Always secure	See section 50.4.14. FMEPROT : Flash P/E Mode Entry Protection Register
FBPROT1	Always secure	See section 50.4.16. FBPROT1 : Flash Block Protection for Secure Register
FSUACR	Always secure	See section 50.4.27. FSUACR : Flash Startup Area Control Register
FACI command-issuing area and all registers of FACI (Base address is FACI) and FWEPROR register	During FACI command processing by secure access	See section 50.12.3.4. Protection during FACI Command Operation

50.12.3.4 Protection during FACI Command Operation

This function protects read/write access to the FACI command-issuing area, including all registers of FACI (Base address is FACI) and FWEPROR register by the non-secure access during the FACI command processing of the secure access. The protect condition includes the suspending period of the program, block erase, or multi block erase command by the P/E suspend command of the secure access. See Figure 50.39 and Table 50.32 for details of the protection during the FACI command operation.

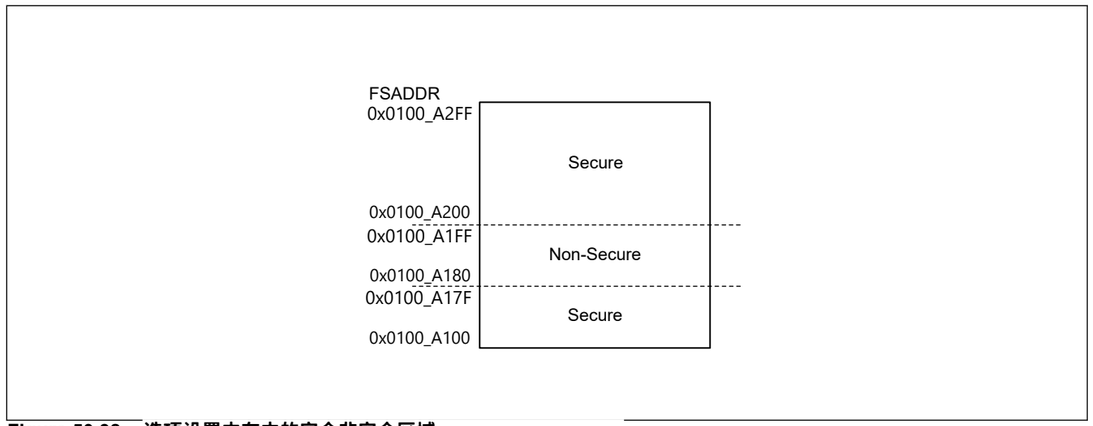


Figure 50.38 选项设置内存中的安全非安全区域

50.12.3.2 保护闪存区域（读取）

该功能保护代码闪存和数据闪存的安全区域免受非安全总线访问。

有关安全区域的详细信息，请参阅第52节，安全功能。

50.12.3.3 注册保护

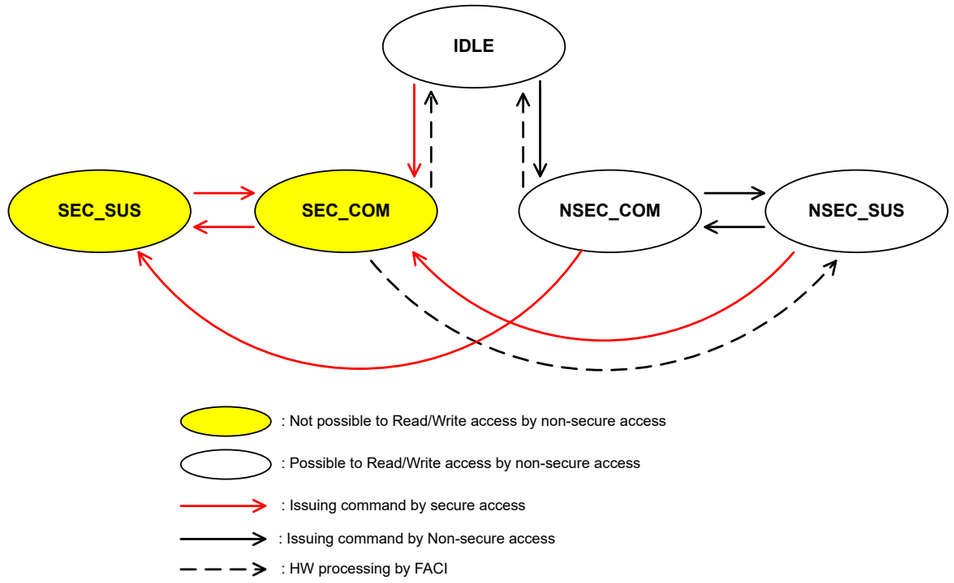
闪存定序器寄存器具有针对非安全访问的写访问保护。表50.31显示了闪存序列器的受保护寄存器的详细信息。

Table 50.31 TrustZone的闪存定序器的受保护寄存器

保护对象寄存器	安全属性设置	Notes
FCKMHZ	安全属性寄存器设置(FSAR.FCKMHZSA)	请参阅第50.4.4节。FSAR：闪存安全归属登记
FMEPROT	始终安全	请参阅第50.4.14节。FMEPROT:闪存PE模式进入保护寄存器
FBPROT1	始终安全	请参阅第50.4.16节。FBPROT1：闪存安全寄存器的块保护
FSUACR	始终安全	请参阅第50.4.27节。FSUACR:闪光启动区控制寄存器
FACI命令发布区和FACI的所有寄存器（基地址为FACI）和FWEPROR寄存器	通过安全访问处理FACI命令期间	请参阅第50.12.3.4节。保护期间FACI命令操作

50.12.3.4 FACI指挥行动期间的保护

此功能保护对FACI命令发布区域的读写访问，包括FACI的所有寄存器（基地址为FACI)和FWEPROR在安全访问的FACI命令处理期间由非安全访问注册。保护条件包括程序的暂停周期、块擦除或由安全访问的PE暂停命令执行的多块擦除命令。FACI命令操作期间的保护细节见图50.39和表50.32。

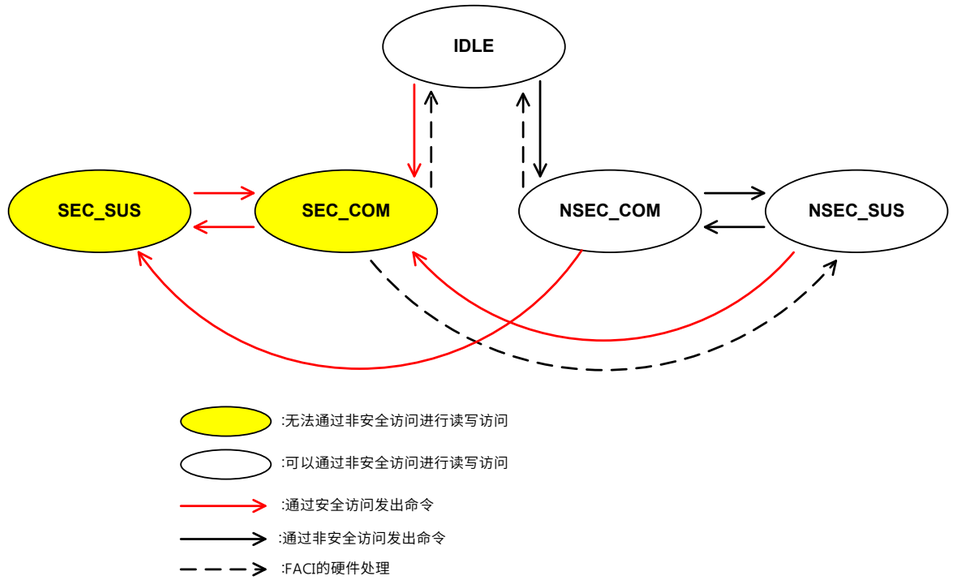


Note: IDLE: State of not executing FACI command
SEC_COM: State of executing FACI command by secure access
SEC_SUS: State of "P/E Suspend" by secure access
NSEC_COM: State of executing FACI command by non-secure access
NSEC_SUS: State of P/E Suspend by non-secure access

Figure 50.39 State of protection during FACI command operation

Table 50.32 Protection during FACI command operation (1 of 2)

	Flash sequencer is not operating	Program, Block erase, Multi block erase, Blank check, or Configuration set command processing		Command lock state		Forced stop command processing		While suspend Program, Block erase, or Multi block erase command		Program command processing while suspend Block erase or Multi block erase command by secure access		Program command processing while suspend Block erase or Multi block erase command by non-secure access		P/E resume command processing while suspend Program, Block erase, or Multi block erase command by secure access		P/E Resume command processing while suspend Program, Block erase, or Multi block erase command by non-secure access	
FACI command attribute	—	S	NS	S	NS	S	NS	S	NS	S	NS *1	S	NS	S	NS *1	S	NS
FRDY bit	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0
PRGSPD or ERSSPD bit	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
CMDLK bit	0	0	0	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0



Note: IDLE：未执行FACI命令的状态
SEC_COM：通过安全访问执行FACI命令的状态
SEC_SUS：安全访问的"PESuspend"状态
NSEC_COM：非安全访问执行FACI命令的状态
NSEC_SUS：PE状态被非安全访问暂停

Figure 50.39 FACI指挥运行期间的保护状态

Table 50.32 FACI命令操作期间的保护(1of2)

	闪存定序器未运行	检查或配置设置命令		命令锁定状态		强制停止指令处理		暂停编程、块擦除或多块擦除命令		块擦除或多块擦除命令由安全访问暂停时的程序命令处理		块擦除或多块擦除命令由non-secure access暂停时的程序命令处理		暂停编程、块擦除或多块擦除命令通过安全访问PE恢复命令处理while		暂停编程、块擦除或多块擦除命令通过非安全访问PE恢复命令处理while	
FACI命令属性	—	S	NS	S	NS	S	NS	S	NS	S	NS *1	S	NS	S	NS *1	S	NS
FRDY bit	1	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0
PRGSPD或ERSSPD位	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
CMDLK bit	0	0	0	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0

Table 50.32 Protection during FACI command operation (2 of 2)

	Flash sequencer is not operating		Program, Block erase, Multi block erase, Blank check, or Configuration set command processing		Command lock state		Forced stop command processing		While suspend Program, Block erase, or Multi block erase command		Program command processing while suspend Block erase or Multi block erase command by secure access		Program command processing while suspend Block erase or Multi block erase command by non-secure access		P/E resume command processing while suspend Program, Block erase, or Multi block erase command by secure access		P/E Resume command processing while suspend Program, Block erase, or Multi block erase command by non-secure access	
Non-secure access	✓	X	✓	✓	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓

Note:
- S indicates the FACI command by the secure access.
- NS indicates the FACI command by the non-secure access.
- ✓ indicates read/write access is possible by the non-secure access.
- X indicates read/write access is not possible by the non-secure access. Write data is ignored and read data is always 0.

Note 1. The FACI command issued by the non-secure access is not allowed.

Code flash programming/erasure can be protected by the FMEPROT register of secure function. Therefore, it does not assume that secure function issues P/E suspend command during code flash programming/erasure of non-secure function. Data flash programming/erasure of non-secure can be suspended by secure function. If secure function issues P/E suspend command during data flash programming/erasure of non-secure function, secure function should issue P/E resume command. When secure function issues P/E resume command, secure function should notify non-secure function that data flash programming/erasure is complete and return to non-secure function. See Figure 50.40 and Figure 50.41 in example of issuing P/E suspend of secure function during programming/erasure of non-secure function.

Table 50.32 FACI命令操作期间的保护(2of2)

	闪存定序器未运行		编程、块擦除、多块擦除、空白检查或配置设置命令 processing		命令锁定状态		强制停止指令处理		暂停编程、块擦除或多块擦除命令		块擦除或多块擦除命令由暂停时的程序命令处理安全访问		块擦除或多块擦除命令由暂停时的程序命令处理 non-secure access		暂停编程、块擦除或多块PE恢复命令处理while通过安全访问擦除命令		暂停编程、块擦除或多块PE恢复命令处理while通过非安全访问擦除命令	
Non-secure access	✓	X	✓	✓	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓	X	✓

Note:
- S表示通过安全访问的FACI命令。
- NS通过非安全访问指示FACI命令。
- 表示非安全访问可以进行读写访问。
- X表示非安全访问无法进行读写访问。写入数据被忽略，读取数据始终为0。

注1.非安全访问发出的FACI命令是不允许的。

代码闪存编程擦除可以通过安全功能的FMEPROT寄存器进行保护。因此，不假设安全功能在非安全功能的代码闪存编程擦除期间发出PE挂起命令。

非安全的数据闪存编程擦除可以通过安全功能暂停。如果在非安全功能的数据闪存编程擦除期间安全功能发出PE暂停命令，安全功能应发出PE恢复命令。当安全功能发出PEresume命令时，安全功能应通知非安全功能数据闪存编程擦除完成并返回到非安全功能。在非安全功能的编程擦除期间发出PE安全功能挂起的示例参见图50.40和图50.41。

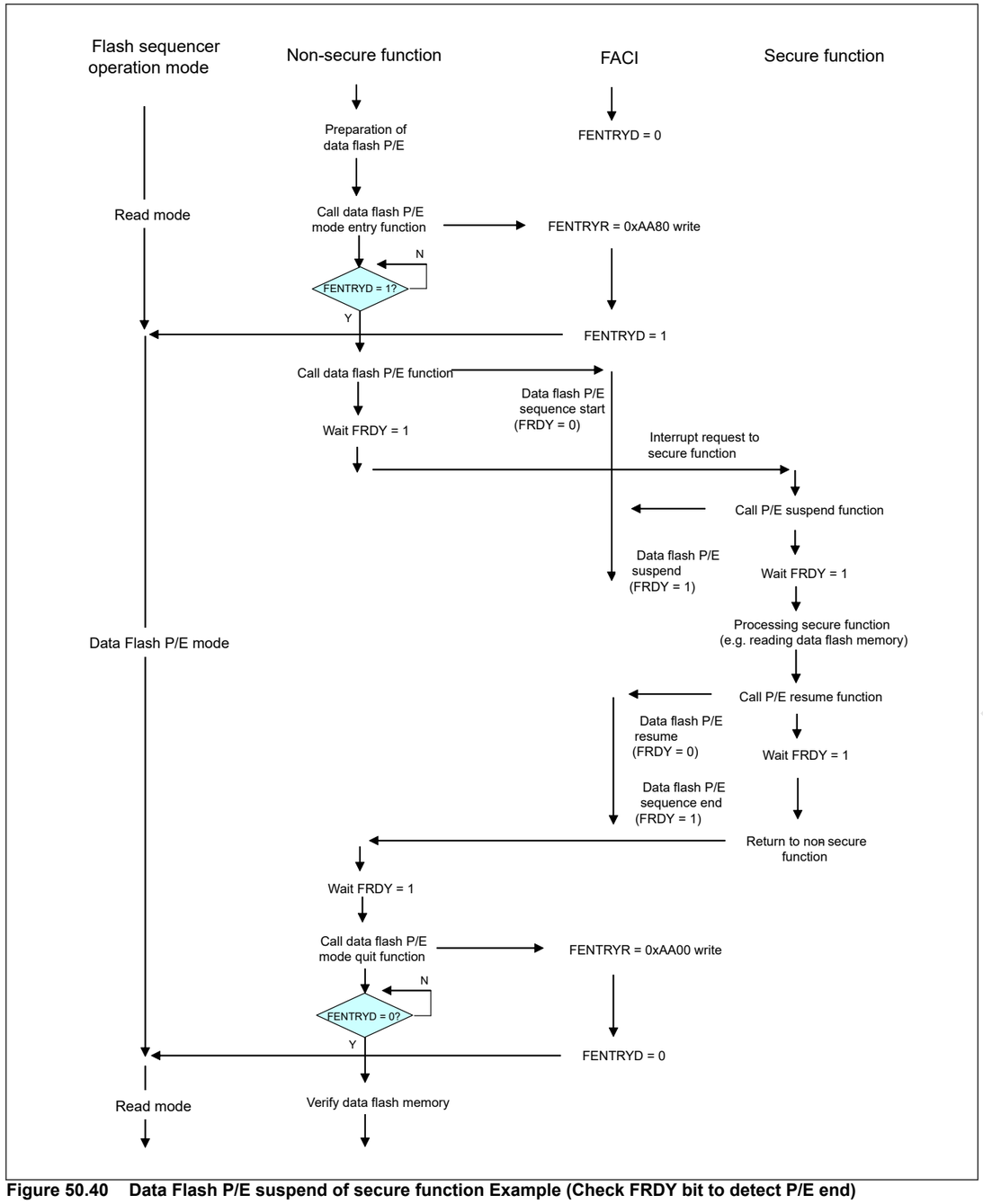


Figure 50.40 Data Flash P/E suspend of secure function Example (Check FRDY bit to detect P/E end)

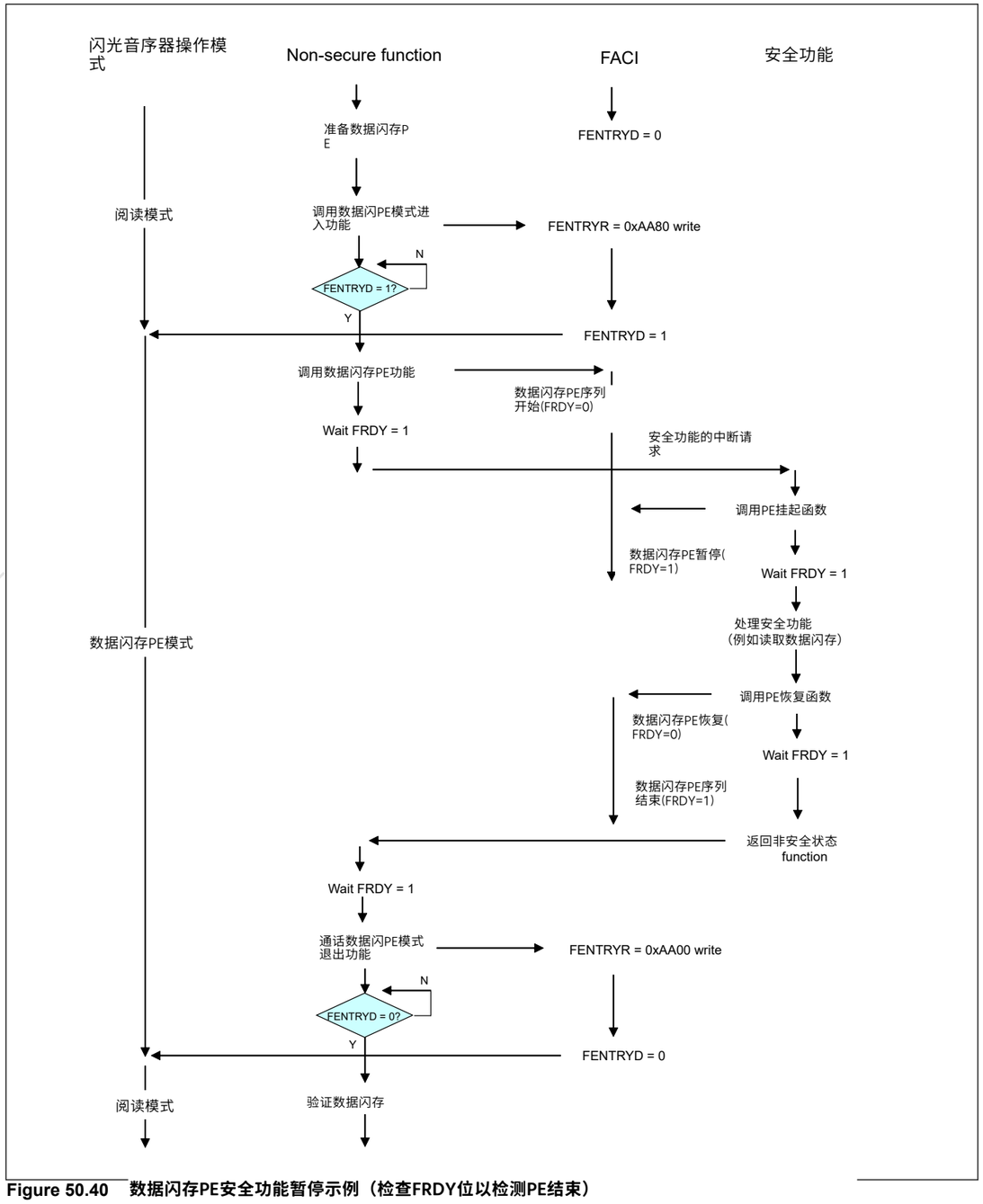


Figure 50.40 数据闪存PE安全功能暂停示例（检查FRDY位以检测PE结束）

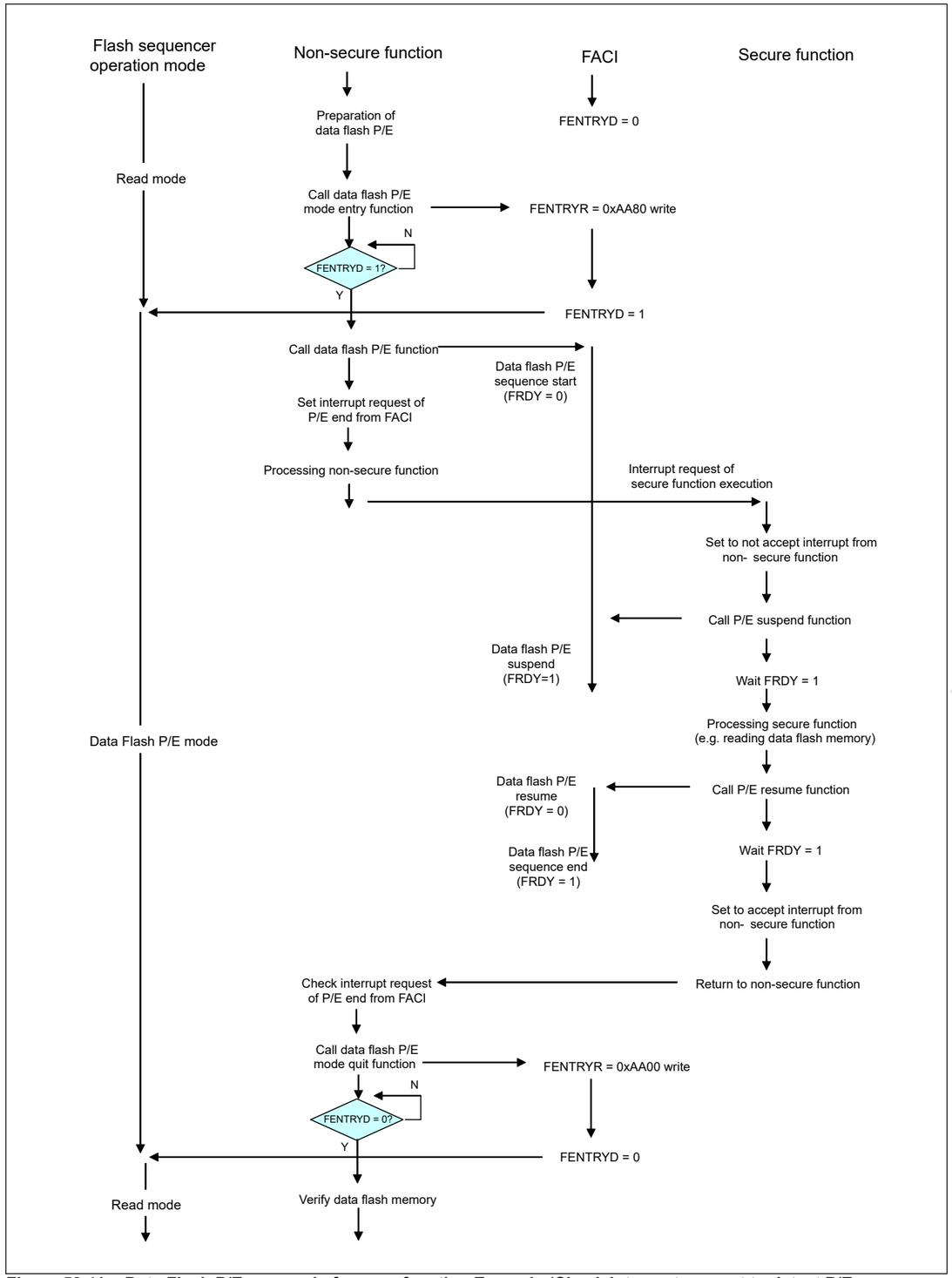


Figure 50.41 Data Flash P/E suspend of secure function Example (Check interrupt request to detect P/E end)

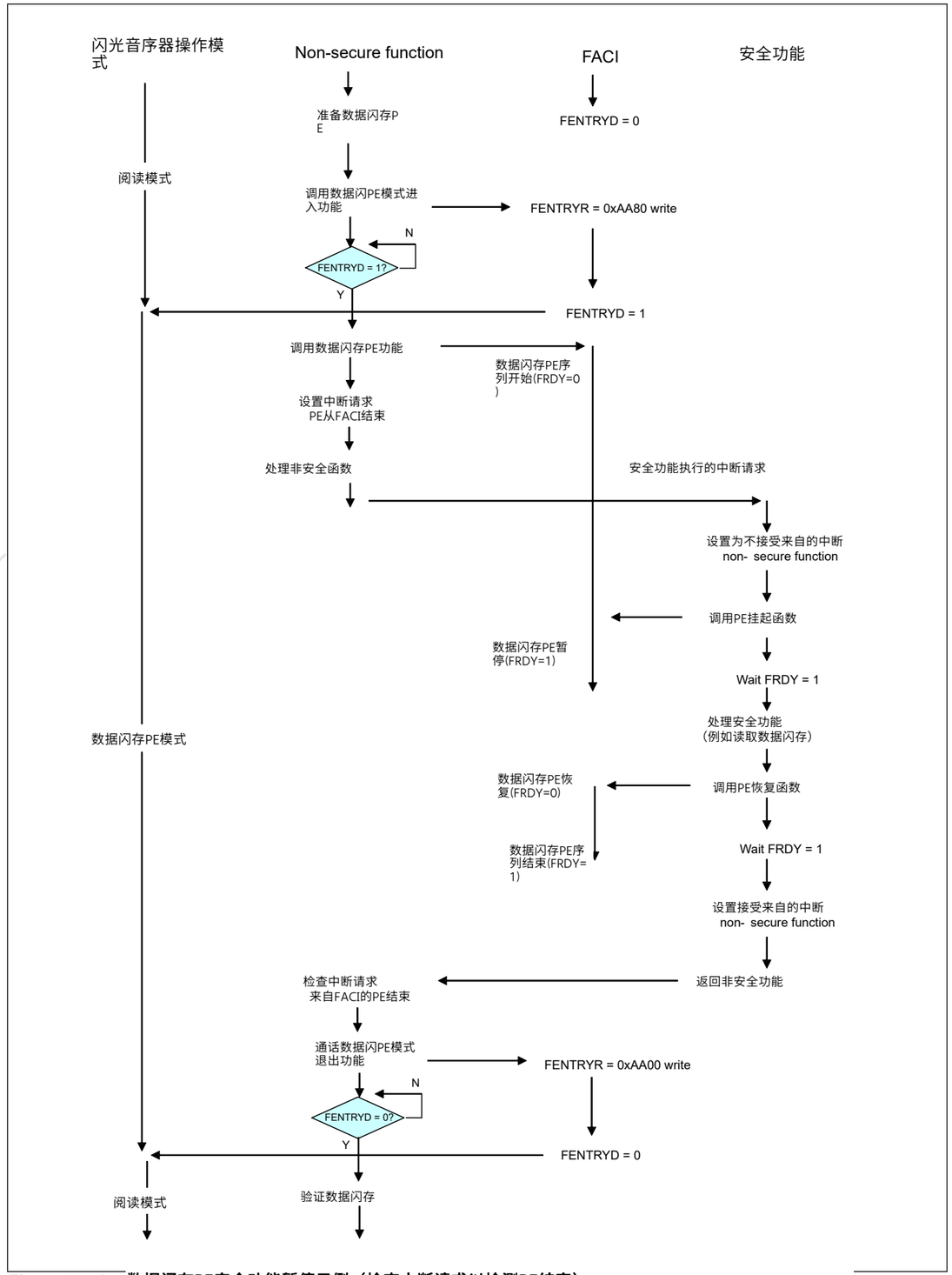


Figure 50.41 数据闪存PE安全功能暂停示例（检查中断请求以检测PE结束）

50.12.3.5 Code Flash P/E Mode Entry Protection

The flash sequencer has protection function of code flash P/E by the FMEPROT register for the secure developer. Secure function can prevent disturbance of reading code flash memory by this protection function. See section 50.4.14. FMEPROT : Flash P/E Mode Entry Protection Register.

For applications that do not require non-secure region programming/erasure other than from secure function, it is recommended to always disable non-secure function of code flash programming/erasure by enabling the protection function of FMEPROT register.

See Figure 50.42 in details of the code flash P/E sequence example by non-secure function.

50.12.3.5 CodeFlashPE模式进入保护

闪存定序器通过FMEPROT寄存器为安全开发人员提供代码闪存PE的保护功能。安全功能可以通过此保护功能防止读取代码闪存的干扰。请参阅第50.4.14节。FMEPROT：FlashPE模式进入保护寄存器。

对于除安全功能外不需要非安全区域编程擦除的应用，建议始终通过启用FMEPROT寄存器的保护功能来禁用代码闪存编程擦除的非安全功能。

有关非安全功能的代码闪存PE序列示例的详细信息，请参见图50.42。

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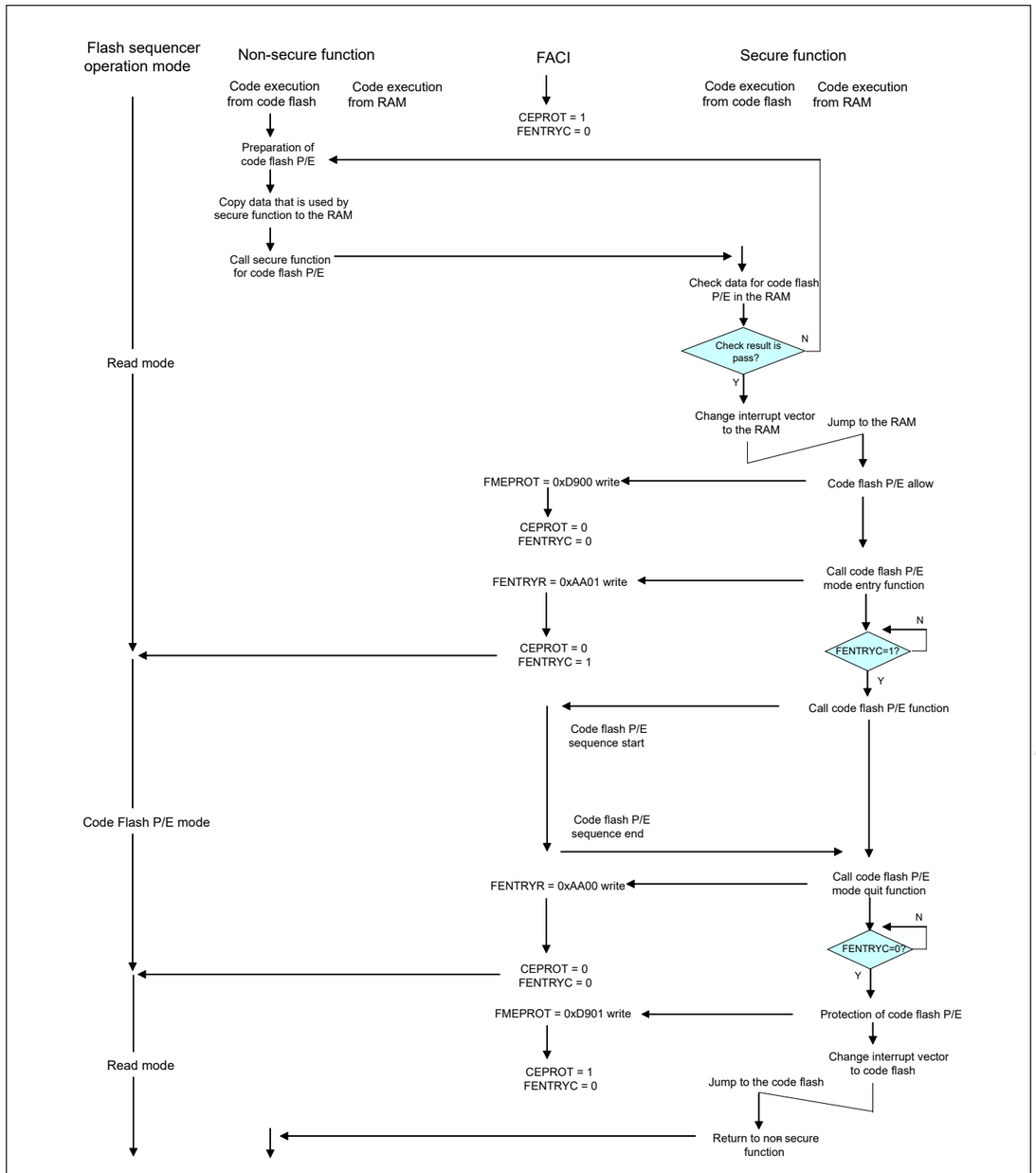

Figure 50.42 Code Flash P/E Sequence Example by non-secure function (Using secure function for code flash P/E)

50.13 Boot Mode

There are two serial programming modes; the boot mode (for the SCI interface) with SCI9 and the boot mode (for the USB interface) with USBFS. Table 50.33 lists the I/O pins used in boot mode. Table 50.34 lists the available communication interface used in the boot mode.

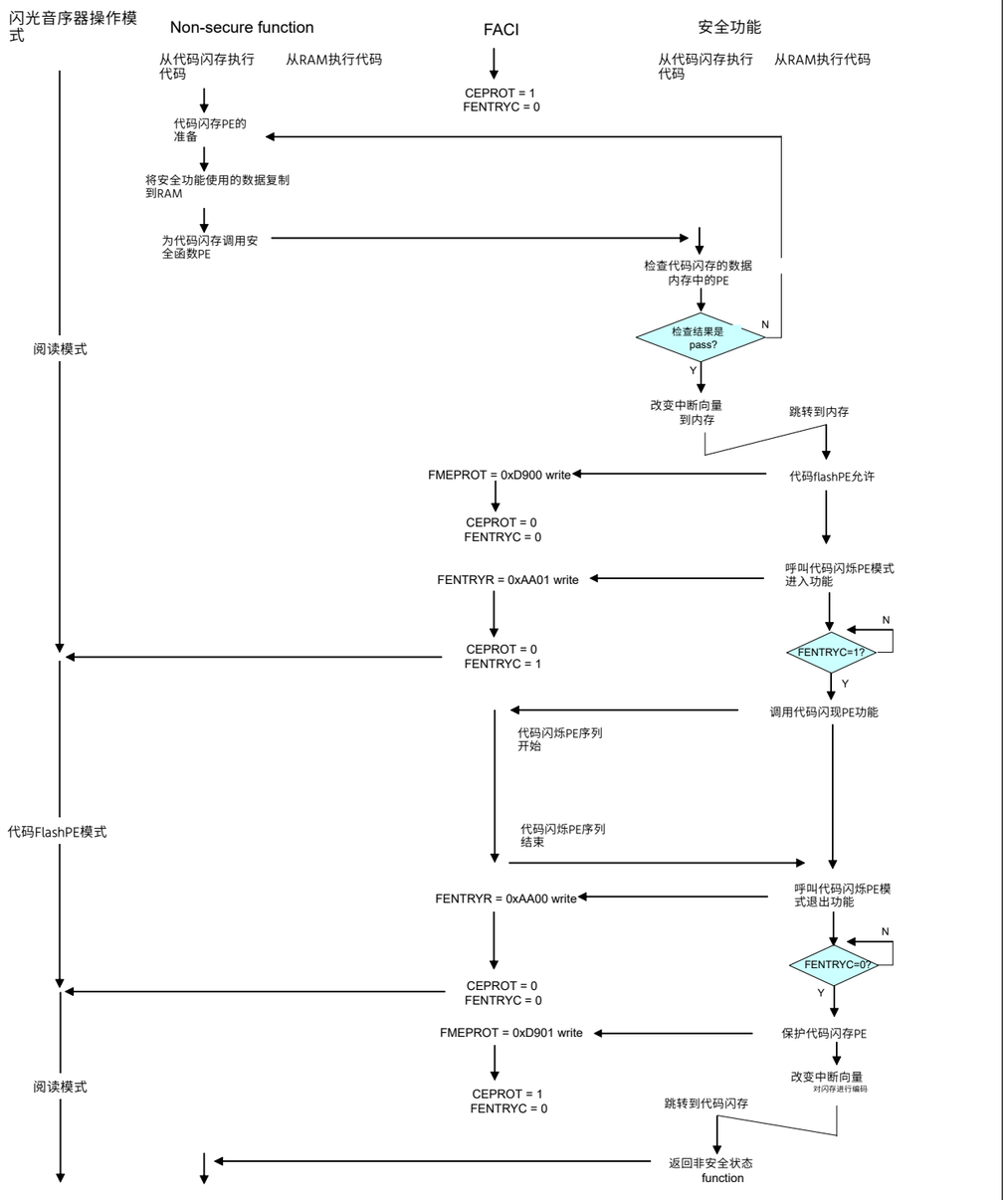

Figure 50.42 CodeFlashPESequenceExamplebynon−securefunction(Usingsecurefunctionforcodeflash PE)

50.13 引导模式

有两种串行编程模式；SCI9的引导模式（SCI接口）和USBFS的引导模式（USB接口）。表50.33列出了引导模式中使用的IO引脚。表50.34列出了启动模式中使用的可用通信接口。

Table 50.33 I/O Pins Used in Boot Mode

Pin Name	I/O	Mode to be Used	Use
MD	Input	Boot mode (for the SCI interface) Boot mode (for the USB interface)	Selection of operating mode
P110/RXD9	Input	Boot mode (for the SCI interface)	For host communication (to receive data through SCI)
P109/TXD9	Output		For host communication (to transmit data through SCI)
USB_DP, USB_DM	I/O	Boot mode (for the USB interface)	Data input/output of USB
USB_VBUS	Input		Detection of connection and disconnection of USB cables

Table 50.34 Available Communication Interface Used in Boot Mode

Main clock oscillator or external clock is connected	Yes	No	No
Sub clockoscillator is connected*1	Yes or No	Yes	No
Available interface	SCI or USB	SCI or USB	SCI
Tool connection time*2	Up to 1 second	Up to 2 seconds	Up to 3 seconds

Note 1. The drive capability of the sub clock oscillator is set to standard by SOMCR.SODRV bit. Note that if you use the crystal corresponding the low drive capability on your board, the crystal may not oscillate in the boot mode.
Note 2. See the boot firmware manual for the detail connection time.

50.13.1 Boot Mode (for the SCI Interface)

In boot mode (for the SCI interface), the host sends control commands and data for programming, and the flash memory is programmed or erased accordingly. An on-chip SCI handles transfer between the host and this MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When this MCU is activated in boot mode (for the SCI interface), the program on the dedicated area the MCU is executed. The boot program automatically adjusts the bit rate of the SCI and controls programming/erasure by receiving control commands from the host.

Figure 50.43 shows the system configuration for operations in boot mode (for the SCI interface).

Table 50.33 引导模式下使用的IO引脚

引脚名称	I/O	使用模式	Use
MD	Input	Boot模式（用于SCI接口）Boot模式（用于USB接口）	操作模式的选择
P110/RXD9	Input	引导模式（用于SCI接口）	用于主机通信（通过SCI接收数据）
P109/TXD9	Output		用于主机通信（通过SCI传输数据）
USB_DP, USB_DM	I/O	引导模式（用于USB接口）	USB数据输入输出
USB_VBUS	Input		检测USB电缆的连接和断开

Table 50.34 引导模式中使用的可用通信接口

连接主时钟振荡器或外部时钟	Yes	No	No
副时钟振荡器已连接 *1	是还是不是	Yes	No
可用接口	SCI或USB	SCI或USB	SCI
工具连接时间*2	最多1秒	最多2秒	最多3秒

注1.副时钟振荡器的驱动能力由SOMCR.SODRV位设置为标准。请注意，如果您使用与板上低驱动能力相对应的晶体，则晶体可能不会在引导模式下振荡。
注2.详细连接时间请参见启动固件手册。

50.13.1 引导模式（用于SCI接口）

在引导模式下（针对SCI接口），主机发送控制命令和数据进行编程，相应地对闪存进行编程或擦除。片上SCI以异步模式处理主机和该MCU之间的传输。主机中必须准备好用于传输控制命令和编程数据的工具。

当这个MCU在启动模式下被激活时（对于SCI接口），在MCU的专用区域上的程序被执行。
引导程序通过接收来自主机的控制命令自动调整SCI的比特率并控制编程擦除。

图50.43显示了引导模式下操作的系统配置（对于SCI接口）。

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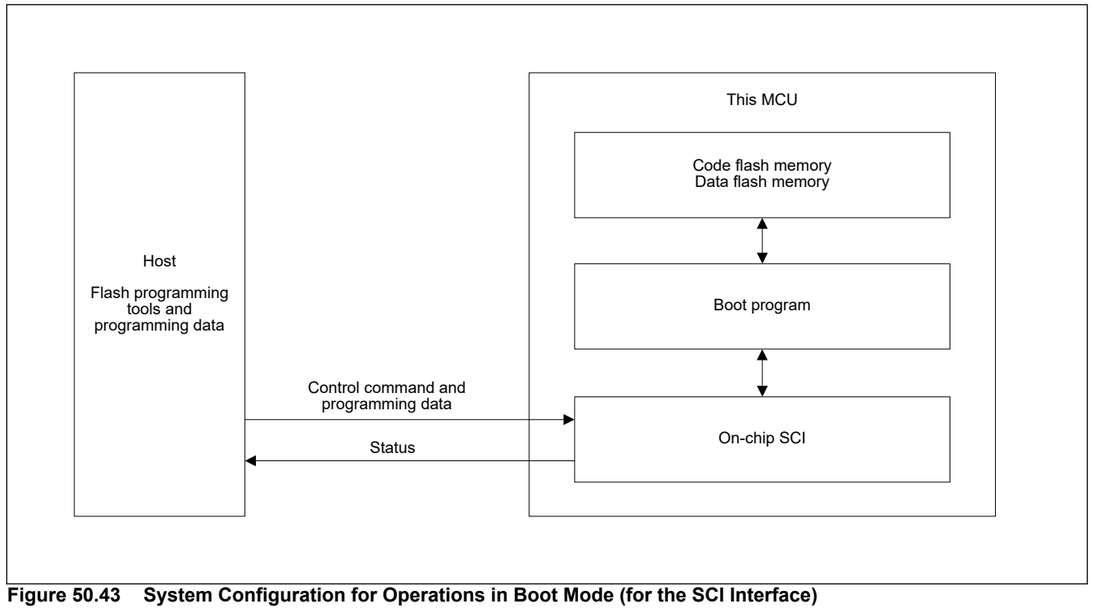

Figure 50.43 System Configuration for Operations in Boot Mode (for the SCI Interface)

50.13.2 Boot Mode (for the USB Interface)

In boot mode (with the USB interface), the flash memory can be programmed or erased by sending control commands and program data from the host. An on-chip USB is used for communications between the host and this MCU. The host requires tools for sending control commands and data for programming. Figure 50.44 shows the configuration of a system for use in boot mode (for the USB interface). The USB cable must be connected on reset release.

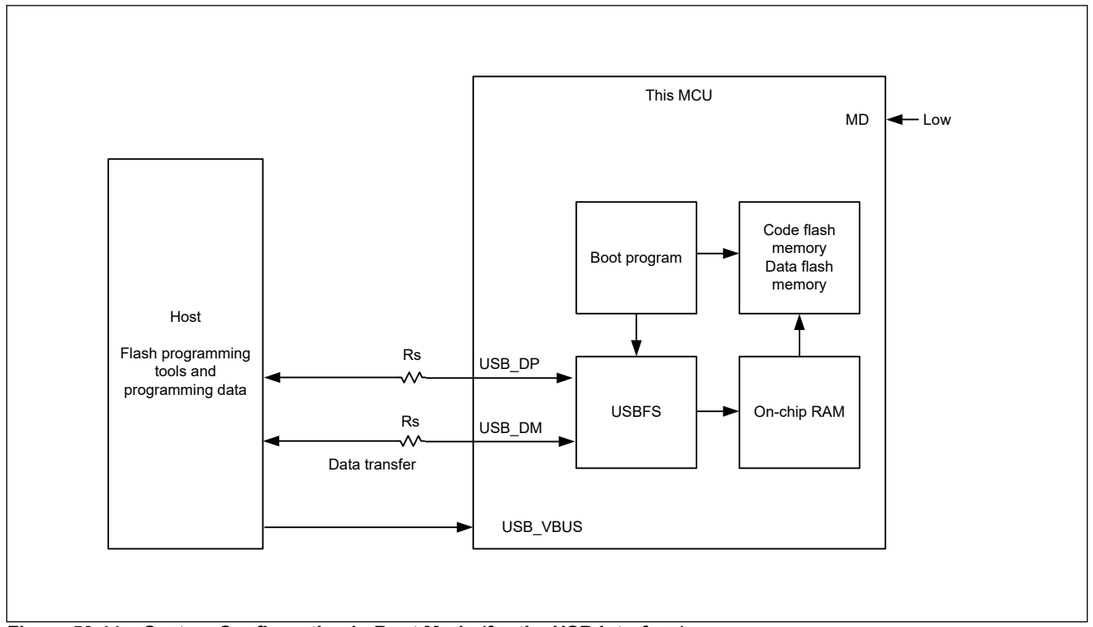

Figure 50.44 System Configuration in Boot Mode (for the USB Interface)

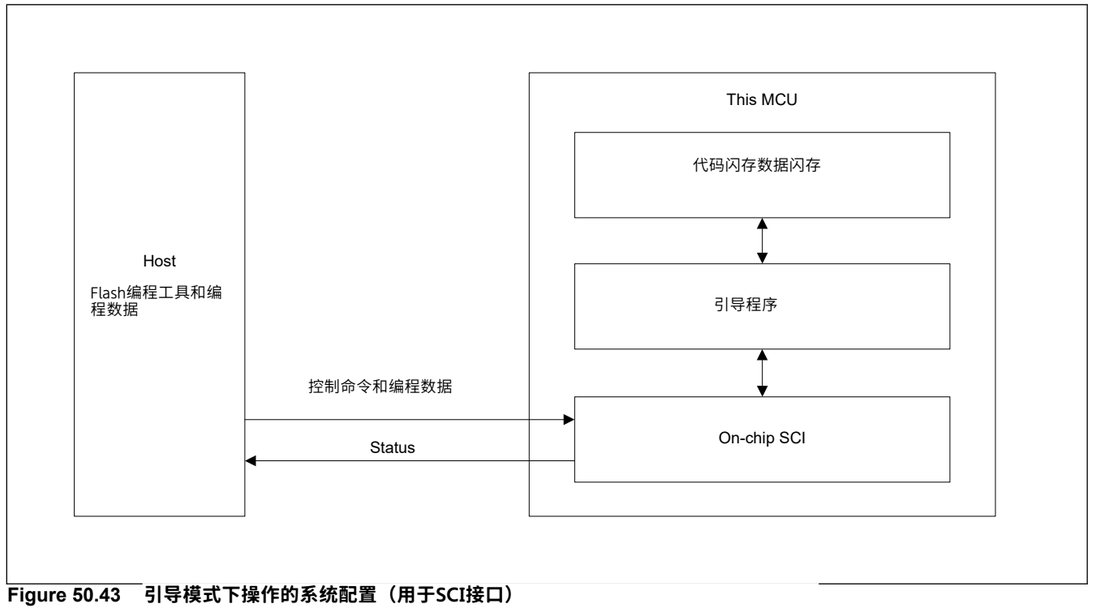

Figure 50.43 引导模式下操作的系统配置（用于SCI接口）

50.13.2 引导模式（用于USB接口）

在引导模式下（使用USB接口），可以通过从主机发送控制命令和编程数据来对闪存进行编程或擦除。片上USB用于主机和该MCU之间的通信。主机需要用于发送控制命令和编程数据的工具。图50.44显示了在引导模式下使用的系统配置（用于USB接口）。USB电缆必须在复位释放时连接。

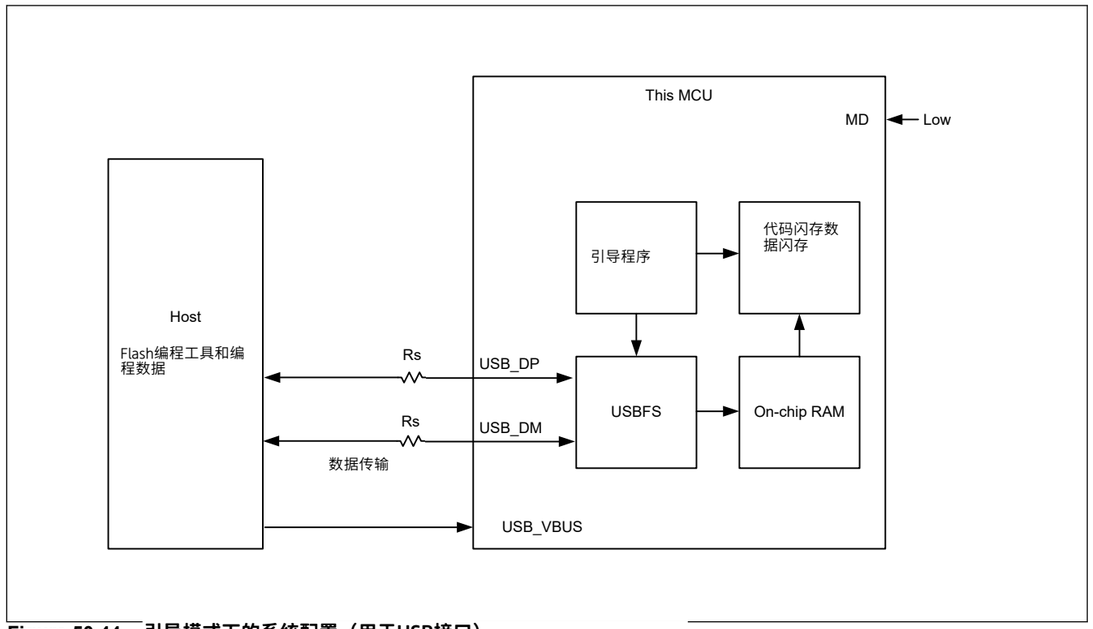

Figure 50.44 引导模式下的系统配置（用于USB接口）

50.14 Using the Serial Programmer for Rewriting

A serial programmer can be used to rewrite flash memory in boot mode.

(1) Serial Programming

This MCU is mounted on the system board at the time of serial programming. Providing a connector to the board enables rewriting of this MCU by the serial programmer to proceed.

50.14.1 Environments for Serial Programming

The recommended environments for rewriting the flash memory of the MCU with data are described below.

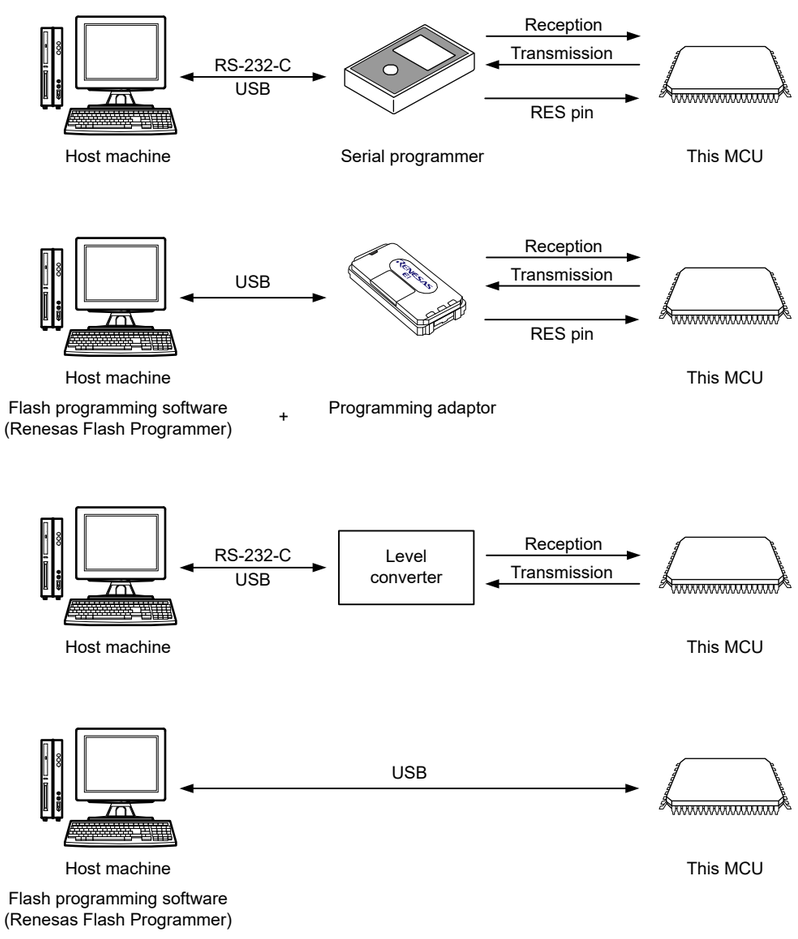

Figure 50.45 Environments for Rewriting the Flash Memory

50.14 使用串行编程器进行重写

串行编程器可用于在引导模式下重写闪存。

(1) 串行编程

该MCU在串行编程时安装在系统板上。为电路板提供连接器可以让串行编程器重写该MCU以继续进行。

50.14.1 串行编程环境

使用数据重写MCU的闪存的推荐环境如下所述。

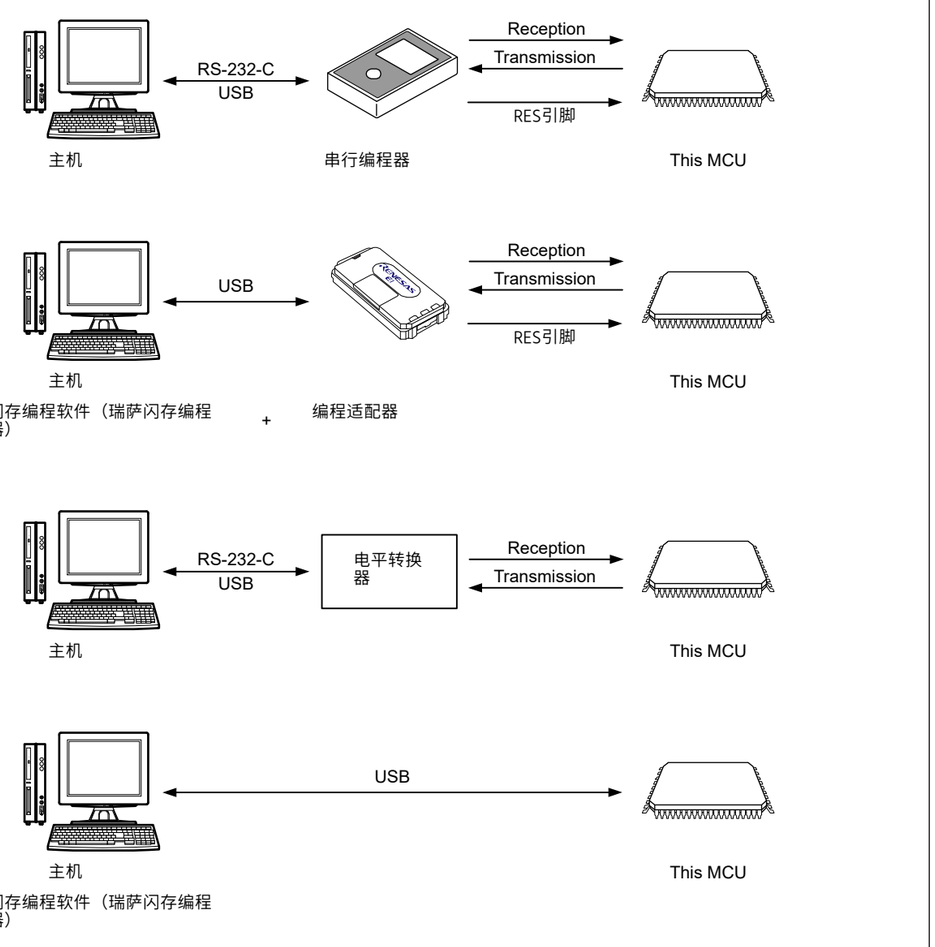

Figure 50.45 重写闪存的环境

50.15 Programming through Self-Programming

50.15.1 Overview

This MCU supports programming of the flash memory by the user program itself. The FACI commands can be used with user programs for writing to the flash memory. This allows upgrading of user programs and rewriting of constant data fields.

The program for rewriting must be transferred to the internal RAM or external memory in advance when the BGO is not available or when rewriting the option-setting memory.

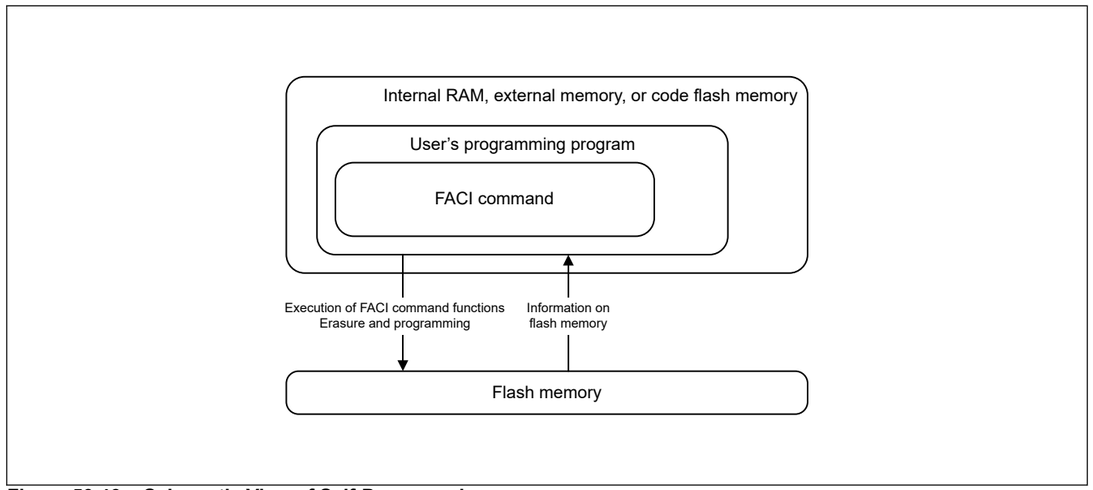

Figure 50.46 Schematic View of Self-Programming

For comprehensive information on the self-programming, refer to section 50.9. FACI Commands

50.15.2 Background Operation

The background operation (BGO) can be used to execute the flash rewrite routine on the code flash memory when the data flash memory or other area of code flash memory is rewritten.

Background operations can be used when the combination of the flash memory for rewriting and the flash memory for reading is any of those listed below.

Table 50.35 Conditions under which Background Operation is Usable (1 of 2)

		Range for rewriting	Range for reading
		Code flash memory	Data flash memory
Common to linear and dual modes		Data flash memory	Code flash memory
Liner mode	Products with 2 Mbytes of code flash memory	First half (1 Mbytes) of the code flash memory (addresses 0x0000 0000 to 0x000F_FFFF)	Second half (1 Mbytes) of the code flash memory (addresses 0x0010_0000 to 001F_FFFF)
		Second half (1 Mbytes) of the code flash memory (addresses 0x0010_0000 to 0x001F_FFFF)	First half (1 Mbytes) of the code flash memory (addresses 0x0000_0000 to 0x000F_FFFF)
Liner mode	Products with 1.5 Mbytes of code flash memory	First half (0.75 Mbytes) of the code flash memory (addresses 0x0000_ 0000 to 0x000B_FFFF)	Second half (0.75 Mbytes) of the code flash memory (addresses 0x000C_0000 to 0x0017_FFFF)

50.15 通过自编程进行编程

50.15.1 Overview

该MCU支持用户程序本身对闪存进行编程。FACI命令可与用户程序一起用于写入闪存。这允许升级用户程序和重写常量数据字段。

当BGO不可用或重写选项设置存储器时，必须将重写程序提前传送到内部RAM或外部存储器。

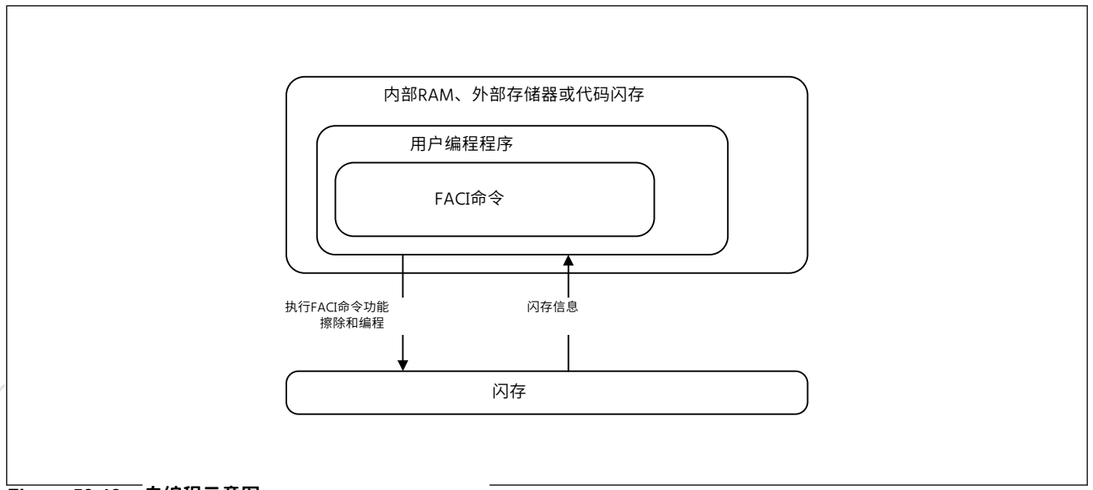

Figure 50.46 自编程示意图

有关自编程的全面信息，请参阅第50.9节。FACI命令

50.15.2 后台操作

当数据闪存或代码闪存的其他区域被重写时，后台操作（BGO）可用于在代码闪存上执行闪存重写例程。

当用于重写的闪存和用于读取的闪存的组合为下列任何一种时，可以使用后台操作。

Table 50.35 后台操作可用的条件(1of2)

		重写范围	读取范围
		代码闪存	数据闪存
常见于线性和双模		数据闪存	代码闪存
线性模式	具有2MB代码闪存的产品	代码闪存的前半部分（1MB）（地址0x00000000到0x000F_FFFF）	代码闪存的后半部分（1MB）（地址0x0010_0000到001F_FFFF）
		代码闪存的后半部分（1MB）（地址0x0010_0000到0x001F_FFFF）	代码闪存的前半部分（1MB）（地址0x0000_0000到0x000F_FFFF）
线性模式	具有1.5MB代码闪存的产品	代码闪存的前半部分（0.75MB）（地址0x0000_0000到0x000B_FFFF）	代码闪存的后半部分（0.75MB）（地址0x000C_0000到0x0017_FFFF）

Table 50.35 Conditions under which Background Operation is Usable (2 of 2)

		Range for rewriting	Range for reading
		Second half (0.75 Mbytes) of the code flash memory (addresses 0x000C_0000 to 0x0017_FFFF)	First half (0.75 Mbytes) of the code flash memory (addresses 0x0000_0000 to 0x000B_FFFF)
Liner mode	Products with 1 Mbytes of code flash memory	First half (0.5 Mbytes) of the code flash memory (addresses 0x0000_0000 to 0x0007_FFFF)	Second half (0.5 Mbytes) of the code flash memory (addresses 0x0008_0000 to 0x000F_FFFF)
		Second half (0.5 Mbytes) of the code flash memory (addresses 0x0008_0000 to 0x000F_FFFF)	First half (0.5 Mbytes) of the code flash memory (addresses 0x0000_0000 to 0x0007_FFFF)
Dual mode	When the BANKSEL.BANKSWP[2:0] bits are 111b	Bank 1 area of the code flash memory	Bank 0 area of the code flash memory
	When the BANKSEL.BANKSWP[2:0] bits are 000b	Bank 0 area of the code flash memory	Bank 1 area of the code flash memory

50.16 Reading Flash Memory

50.16.1 Reading Code Flash Memory

Special settings are not required to read code flash memory after release from the reset state. Data can simply be read out through access to addresses in the code flash memory.

When reading code flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state), all bits are read as 1.

50.16.2 Reading Data Flash Memory

Special settings are not required to read data flash memory after release from the reset state. Data can simply be read out through access to addresses in the data flash memory.

Values read from data flash memory that has been erased but not yet been programming again (i.e. that is in the non-programmed state) are undefined. Use blank checking when you need to confirm that an area is in the non-programmed state.

50.16.3 Access Cycle

When the CPU cache is hit, access is one cycle.

For the CPU cache is missed while CPU cache operation is enabled, or CPU cache is disabled. (This operation only guarantees the first read access of a wrapping burst in AHB protocol. Otherwise, access wait occurs until the CPU cache is filled.)

Table 50.36 Code Flash Memory

Flash Cache Operation	FLWT Register Setting	Read cycle (ICLK)
enable and hit	—	3
disable or miss	0x00	3
	0x01	4
	0x02	5
	0x03	6

Table 50.35 后台操作可用的条件(2of2)

		重写范围	读取范围
		代码闪存的后半部分（0.75MB）（地址0x000C_0000到0x0017_FFFF）	代码闪存的前半部分（0.75MB）（地址0x0000_0000到0x000B_FFFF）
线性模式	具有1MB代码闪存的产品	代码闪存的前半部分（0.5MB）（地址0x0000_0000到0x0007_FFFF）	代码闪存的后半部分（0.5MB）（地址0x0008_0000到0x000F_FFFF）
		代码闪存的后半部分（0.5MB）（地址0x0008_0000到0x000F_FFFF）	代码闪存的前半部分（0.5MB）（地址0x0000_0000到0x0007_FFFF）
双模式	当。。。的时候 BANKSEL.BANKSWP[2:0]位为111b	代码闪存的Bank1区域	代码闪存的Bank0区域
	当。。。的时候 BANKSEL.BANKSWP[2:0]位为000b	代码闪存的Bank0区域	代码闪存的Bank1区域

50.16 读取闪存

50.16.1 读码闪存

从复位状态释放后，读取代码闪存不需要特殊设置。可以通过访问代码闪存中的地址来简单地读取数据。

当读取已擦除但尚未再次编程的代码闪存时（即处于未编程状态），所有位都被读取为1。

50.16.2 读取数据闪存

从复位状态释放后读取数据闪存不需要特殊设置。通过访问数据闪存中的地址可以简单地读取数据。

从已擦除但尚未再次编程（即处于未编程状态）的数据闪存中读取的值未定义。当您需要确认某个区域处于非编程状态时，请使用空白检查。

50.16.3 访问周期

当CPU缓存被命中时，访问为一个周期。

启用CPU缓存操作或禁用CPU缓存时CPU缓存丢失。（此操作仅保证AHB协议中包装突发的第一次读取访问。否则，将等待访问，直到CPU缓存被填满。）

Table 50.36 代码闪存

闪存缓存操作	FLWT寄存器设置	读周期(ICLK)
启用并点击	—	3
禁用或错过	0x00	3
	0x01	4
	0x02	5
	0x03	6

Table 50.37 Data Flash Memory

FCKMHZ Register Setting	Read (cycle)
0x00 to 0x09	Min: 2 ICLK + 3 FCLK Max: (n + 1) ICLK + 3 FCLK
0x0A to 0x13	Min: 2 ICLK + 4 FCLK Max: (n + 1) ICLK + 4 FCLK
0x14 to 0x1D	Min: 2 ICLK + 5 FCLK Max: (n + 1) ICLK + 5 FCLK
0x1E to 0x27	Min: 2 ICLK + 6 FCLK Max: (n + 1) ICLK + 6 FCLK
0x28 to 0x31	Min: 2 ICLK + 7 FCLK Max: (n + 1) ICLK + 7 FCLK
0x32	Min: 2 ICLK + 8 FCLK Max: (n + 1) ICLK + 8 FCLK

Note: When the frequency ratio of ICLK : FCLK is n : 1

50.17 Usage Notes

(1) Reading Area Where Programming/Erasure was Interrupted and Area Targeted for Suspension

The data stored in the area where programming or erasure has been suspended or the area where programming or erasure has been suspended by using the suspend command are undefined. To avoid faulty operation caused by reading undefined data, take care not to fetch instructions or read data from areas where programming or erasure was suspended and where programming or erasure was suspended by using the suspend command.

(2) Suspension During Programming/Erasure

When processing of programming/erasure is stopped by issuing the P/E suspend command, the programming/erasure processing can be resumed by issuing the P/E resume command. If the flash sequencer enters the command-locked state for any reason and issues the forced stop command after the suspended processing is normally completed and the ERSSPD flag or PRGSPD flag is set to 1, the suspended processing cannot be resumed. In addition, the values in the area where the processing was suspended are not guaranteed. Erase that area

(3) Prohibition of Additional Programming

Programming a given area of the code flash memory or data flash memory twice is not possible. To program the code flash memory or data flash memory where has been programed, erase the target area. Programming can be added to the option-setting memory.

(4) Resets During Programming/Erasure, or Blank Checking

In the case of a reset due to the signal on the RES pin during programming/erasure, or blank checking of the flash memory, wait for at least t_{RESW} (see section 53, Electrical Characteristics) of the reset input period once the operating voltage is within the range stipulated in the electrical characteristics, then release the device from the reset state.

(5) Allocation of Vectors for Interrupts and Other Exceptions During Programming/Erasure

Generation of an interrupt or other exception during programming/erasure may lead to fetching of the vector from the code flash memory. Under conditions where BGO cannot be used, set the address of the vector to an address that is not in the code flash memory. Alternatively, make sure that no handling of interrupts or exceptions proceeds during programming/erasure.

(6) Items Prohibited During Programming/Erasure, or Blank Checking

High voltage is applied to the flash memory during programming/erasure, or blank checking. To prevent damage to the flash memory, do not perform the following operations.

- Have the operating voltage from the power supply go beyond the permitted range.
- Change the FWEPROR.FLWE[1:0]bits.

Table 50.37 数据闪存

FCKMHZ寄存器设置	Read (cycle)
0x00 to 0x09	Min: 2 ICLK + 3 FCLK Max: (n + 1) ICLK + 3 FCLK
0x0A to 0x13	Min: 2 ICLK + 4 FCLK Max: (n + 1) ICLK + 4 FCLK
0x14 to 0x1D	Min: 2 ICLK + 5 FCLK Max: (n + 1) ICLK + 5 FCLK
0x1E to 0x27	Min: 2 ICLK + 6 FCLK Max: (n + 1) ICLK + 6 FCLK
0x28 to 0x31	Min: 2 ICLK + 7 FCLK Max: (n + 1) ICLK + 7 FCLK
0x32	Min: 2 ICLK + 8 FCLK Max: (n + 1) ICLK + 8 FCLK

Note: 当ICLK:FCLK的频率比为n:1时

50.17 使用说明

(1) 编程擦除被中断的阅读区域和暂停的目标区域

存储在已暂停编程或擦除的区域或已使用suspend命令暂停编程或擦除的区域中的数据是未定义的。为避免因读取未定义数据而导致错误操作，请注意不要从暂停编程或擦除的区域以及使用暂停命令暂停编程或擦除的区域获取指令或读取数据。

(2) 编程擦除期间的暂停

当通过发出PE暂停命令停止编程擦除处理时，可以通过发出PE恢复命令来恢复编程擦除处理。如果闪存定序器由于任何原因进入命令锁定状态并在挂起处理正常完成并且ERSSPD标志或PRGSPD标志设置为1后发出强制停止命令，则无法恢复挂起的处理。此外，不能保证处理暂停的区域中的值。擦除该区域

(3) 禁止额外编程

不能对代码闪存或数据闪存的给定区域进行两次编程。要对已编程的代码闪存或数据闪存进行编程，请擦除目标区域。可以将编程添加到选项设置存储器中。

(4) 在编程擦除或空白检查期间复位

如果在编程擦除期间由于RES引脚上的信号而导致复位，或者闪存的空白检查，一旦工作电压为在电气特性规定的范围内，然后将设备从复位状态释放。

(5) 在编程擦除期间为中断和其他异常分配向量

在编程擦除期间产生中断或其他异常可能会导致从代码闪存中获取向量。在无法使用BGO的情况下，将向量的地址设置为不在代码闪存中的地址。或者，确保在编程擦除期间不处理中断或异常。

(6) 编程擦除或空白检查期间禁止的项目

在编程擦除或空白检查期间向闪存施加高电压。为防止损坏闪存，请勿执行以下操作。

- 电源的工作电压是否超出允许范围。
- 改变FWEPROR.FLWE[1:0]位。

- Change the OPCCR.OPCM[2:0] and SOPCCR.SOPCM bits.
- Change the SCKDIVCR.FCK[2:0]bits.
- Change the SCKSCR.CKSEL[2:0]bits.
- Transition to the software standby mode, or deep software standby mode.

(7) Programming/Erasure in Low-Speed Modes and Subosc-Speed Mode

Do not programming/erasure the flash memory when low-speed mode or subosc-speed mode is selected with the operating power control register (OPCCR or SOPCCR).

(8) Setting dual bank mode and programming in Boot Mode

The initial mode of the MCU shipped from Renesas is linear mode. In customer's factory when programming dual bank mode and customer's applications on MCU set in linear mode, it is recommended that only area1 in Figure 50.47 is programed in boot mode and area2 is kept blank. After reset, MCU starts in dual mode and the application is in bank0. Use self-programming when programming area2 for updating in the field. See section 52.5. Field Updating in Dual Mode for details

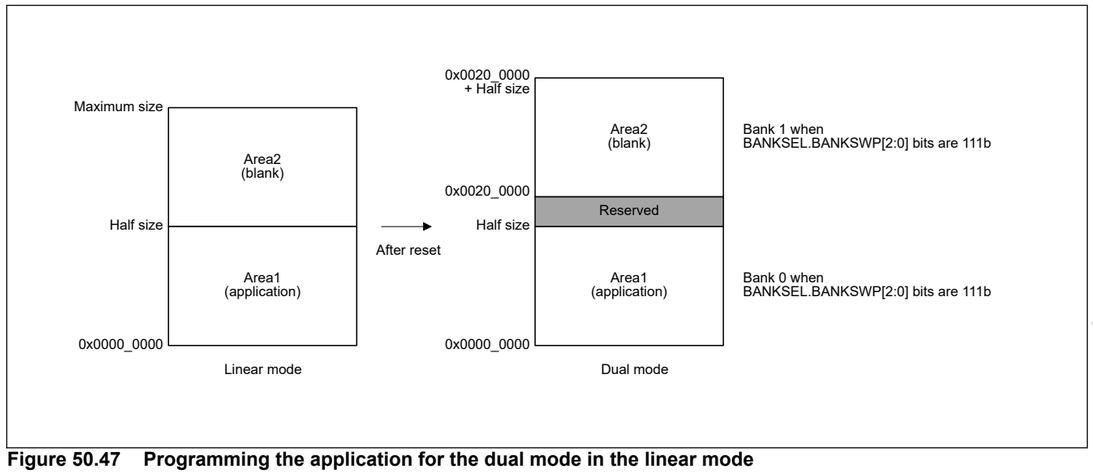

Figure 50.47 Programming the application for the dual mode in the linear mode

(9) Emulator Connection

Renesas provides the emulator which supports both debugging using SWD or JTAG communication and serial programming using SCI communication. This emulator makes it easy to switch between debugging and serial programming.

Table 50.38 shows the pinout of 10 pin or 20 pin socket pinouts when using this emulator. The pinout of SWD and JTAG is ARM standard, and MD, TXD, RXD pins are added for the serial programming using SCI communication.

The serial programming interface must be used to program the TrustZone IDAU boundary register settings.

It is recommended to connect P300/SWCLK/TCK and P201/MD pins using wired OR circuit on the board to use both debugging and serial programming

Table 50.38 Pin assign for emulator (1 of 2)

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	P108/SWDIO	P108/TMS	NC
4	P300/SWCLK Wired OR with P201/MD	P300/TCK Wired OR with P201/MD	P201/MD
6	P109/SWO/TXD9	P109/TDO/TXD9	P109/TXD9
8	P110/RXD9	P110/TDI/RXD9	P110/RXD9

●更改OPCCR.OPCM[2:0]和SOPCCR.SOPCM位。
●更改SCKDIVCR.FCK[2:0]位。
●更改SCKSCR.CKSEL[2:0]位。
●转换到软件待机模式或深度软件待机模式。

(7) 低速模式和Subosc-Speed模式下的编程擦除

当使用工作电源控制寄存器（OPCCR或SOPCCR）选择低速模式或subosc-speed模式时，不要对闪存进行编程擦除。

(8) 设置双组模式并在引导模式下编程

Renesas出厂的MCU的初始模式是线性模式。在客户工厂对双组模式进行编程时，以及客户在MCU上的应用程序设置为线性模式时，建议仅在引导模式下对图50.47中的区域1进行编程，区域2保持空白。复位后，MCU以双模式启动，应用程序位于bank0。对area2进行编程以进行现场更新时，请使用自编程。见第52.5节。双模式现场更新了解详情

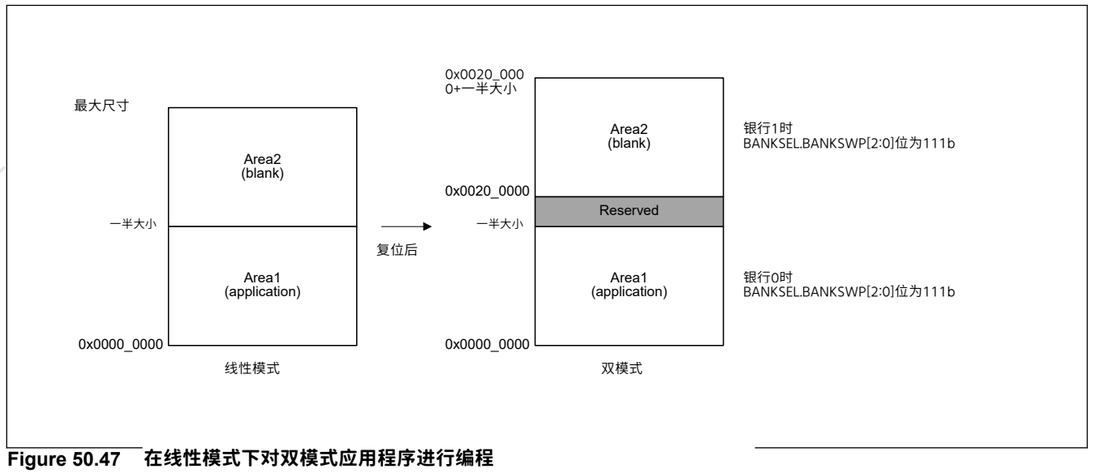

Figure 50.47 在线性模式下对双模式应用程序进行编程

(9) 仿真器连接

瑞萨电子提供的仿真器支持使用SWD或JTAG通信进行调试和使用SCI通信进行串行编程。该仿真器可以轻松地在调试和串行编程之间切换。

表50.38显示了使用该仿真器时10针或20针插座的引脚排列。SWD和JTAG的管脚是ARM标准，并增加了MD、TXD、RXD引脚用于使用SCI通信的串行编程。

必须使用串行编程接口对TrustZoneIDAU边界寄存器设置进行编程。

建议使用板上的有线OR电路连接P300SWCLKTCK和P201MD引脚，以同时使用调试和串行编程

Table 50.38 模拟器的引脚分配（2个中的1个）

针号	SWD	JTAG	使用SCI进行串行编程
1	VCC	VCC	VCC
2	P108/SWDIO	P108/TMS	NC
4	P300/SWCLK 有线或带P201MD	P300/TCK 有线或带P201MD	P201/MD
6	P109/SWO/TXD9	P109/TDO/TXD9	P109/TXD9
8	P110/RXD9	P110/TDI/RXD9	P110/RXD9

Table 50.38 Pin assign for emulator (2 of 2)

Pin No.	SWD	JTAG	Serial Programming using SCI
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	P214/TCLK	P214/TCLK	NC
14	P211/TDATA[0]	P211/TDATA[0]	NC
16	P210/TDATA[1]	P210/TDATA[1]	NC
18	P209/TDATA[2]	P209/TDATA[2]	NC
20	P209/TDATA[3]	P208/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

Table 50.38 仿真器的引脚分配（2个中的2个）

针号	SWD	JTAG	使用SCI进行串行编程
9	GNDdetect	GNDdetect	GNDdetect
10	nRESET	nRESET	nRESET
12	P214/TCLK	P214/TCLK	NC
14	P211/TDATA[0]	P211/TDATA[0]	NC
16	P210/TDATA[1]	P210/TDATA[1]	NC
18	P209/TDATA[2]	P209/TDATA[2]	NC
20	P209/TDATA[3]	P208/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

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51. Internal Voltage Regulator

51.1 Overview

The MCU includes one internal voltage regulator:

- Linear regulator (LDO)

This regulator supplies voltage to all internal circuits and memory except for I/O, analog, USB, and battery backup power domains.

51.2 Operation

Table 51.1 lists the LDO mode pin settings, and Figure 51.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 51.1 LDO mode pin

Pins	Setting descriptions
All VCC	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-μF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL, VCL0	Connect the each pin to VSS through a 0.1-μF multilayer ceramic capacitor. Place the capacitor close to the pin.

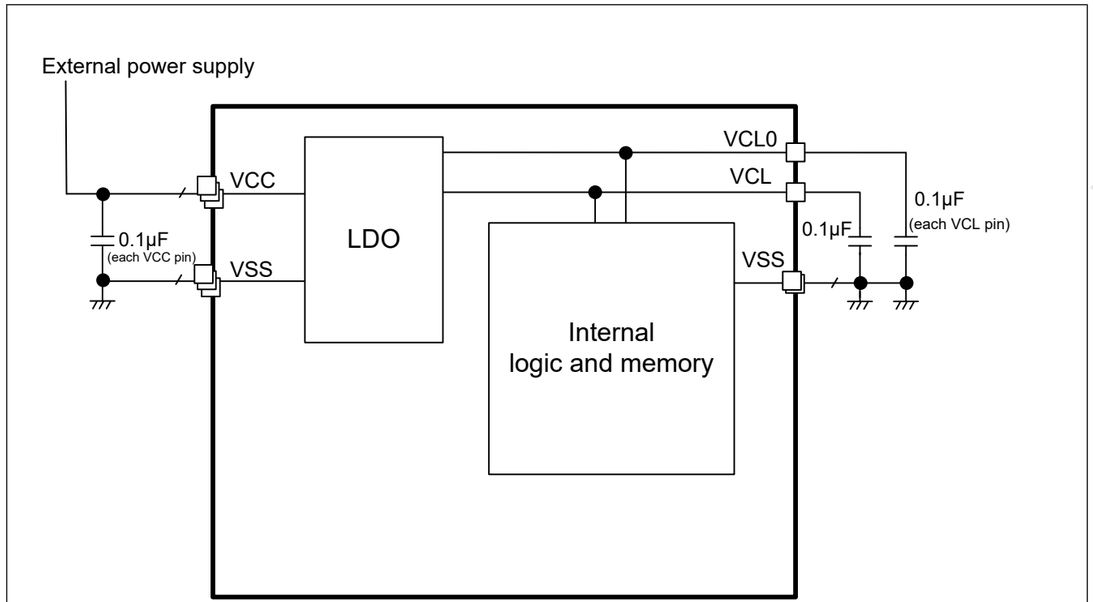

Figure 51.1 LDO mode settings

51. 内部稳压器

51.1 Overview

MCU包含一个内部稳压器：

●线性稳压器（LDO）

该稳压器为除IO、模拟、USB和电池备用电源域之外的所有内部电路和存储器提供电压。

51.2 Operation

表51.1列出了LDO模式引脚设置，图51.1显示了LDO模式设置。在LDO模式下，内部电压由VCC产生。

Table 51.1 LDO模式引脚

Pins	设置说明
All VCC	• 将每个引脚连接到系统电源。 • 通过一个0.1μF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
VCL, VCL0	通过一个0.1μF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。

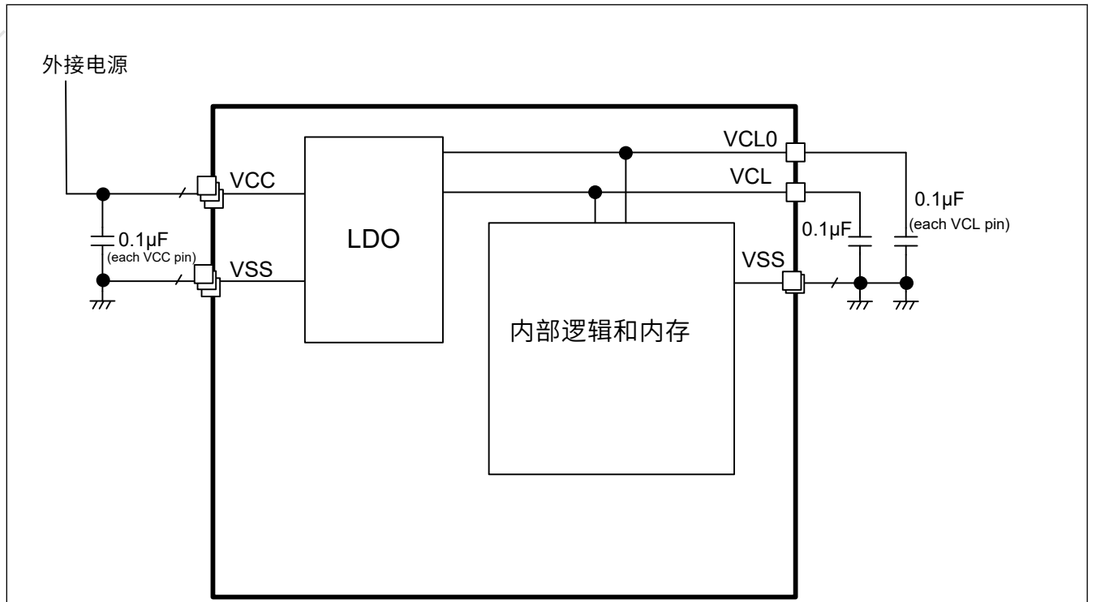

Figure 51.1 LDO模式设置

52. Security Features

52.1 Features

- ARMv8-M TrustZone security
  - Eight regions IDAU for memory space
    - Up to three or six regions for the code flash, depending on the bank mode
    - Up to two regions for the data flash
    - Up to three regions for the SRAM
    - IDAU setting is common for the CPU, DMAC, and DTC
  - SAU is not implemented
  - Secure or Non-secure region for the Standby SRAM
  - Secure or Non-secure region for the VBATT backup registers
  - Individual Secure or Non-secure security attribution for each peripheral
  - Some peripherals support both Secure and Non-secure security attributions
- Device lifecycle management
- Three debug access levels
  - DBG2: The debugger connection is allowed, and no restriction to access memories and peripherals
  - DBG1: The debugger connection is allowed, and restricted to access only non-secure memory regions and peripherals
  - DBG0: The debugger connection is not allowed
- Key injection
- Cryptographic accelerator
  - See section 42, Secure Cryptographic Engine (SCE9)
- Secure pin multiplexing
  - All I/O port pins can be configured individually as secure or non-secure
  - Pin functions of SCI3, SPI0, IIC0, GPT321 and GPT165 can be configured as secure pin
  - See section 19, I/O Ports

52.2 Arm TrustZone Security

52.2.1 Arm TrustZone Technology

Arm TrustZone technology divides the system and the application into Secure and Non-secure domains. Secure application can access both Secure and Non-secure memory and resources. Non-secure application can only access Non-secure memory and resources.

The system starts up in Secure state by default. The security state of CPU can be either Secure or Non-secure.

52.2.2 Memory Security Attribution

The code flash, the data flash, and the SRAM are divided into Secure (S), Non-secure (NS) and Non-secure callable (NSC) regions. These memory security attributions are set into the nonvolatile memory by the serial programming command when the device lifecycle is SSD state. These memory security attributions are loaded into the IDAU and the memory controller before application execution. These memory security attributions cannot be updated by application but can be through the dedicated registers.

The code flash can be divided in up to three regions in the linear mode and six regions in the dual mode. The area of three regions is same between bank0 and bank1 in the dual mode. The data flash can be divided in up to two regions. The SRAM can be divided in up to three regions. Figure 52.1 shows the memory mapping. Table 52.1 shows the size of memory region.

52. 安全功能

52.1 Features

- ARMv8-M TrustZone security

  八个区域IDAU用于存储空间
  - 代码闪存最多三个或六个区域，具体取决于存储库模式
  - 最多两个区域用于数据闪存
  - SRAM最多三个区域
  - IDAU设置对于CPU、DMAC和DTC是通用的

  SAU未实施

  备用SRAM的安全或非安全区域

  VBATT备份寄存器的安全或非安全区域

  每个外围设备的单独安全或非安全安全属性

  一些外围设备同时支持安全和非安全安全属性

●设备生命周期管理

●三个调试访问级别

  DBG2：允许调试器连接，并且对访问内存和外设没有限制

  DBG1：允许调试器连接，但仅限于访问非安全内存区域和外围设备

  DBG0：不允许调试器连接

●密钥注入

●密码加速器

  参见第42节，安全加密引擎(SCE9)

●安全引脚复用

  所有IO端口引脚都可以单独配置为安全或非安全

  SCI3、SPI0、IIC0、GPT321和GPT165的引脚功能可配置为安全引脚

  参见第19节，IO端口

52.2 ArmTrustZone安全

52.2.1 ArmTrustZone技术

ArmTrustZone技术将系统和应用程序划分为安全和非安全域。安全应用程序可以访问安全和非安全内存和资源。非安全应用程序只能访问非安全内存和资源。

系统默认以安全状态启动。CPU的安全状态可以是Secure或Non-secure。

52.2.2 内存安全归属

代码闪存、数据闪存和SRAM分为安全(S)、非安全(NS)和非安全可调用(NSC)区域。当设备生命周期为SSD状态时，这些内存安全属性由串行编程命令设置到非易失性内存中。这些内存安全属性在应用程序执行之前被加载到IDAU和内存控制器中。这些内存安全属性不能由应用程序更新，但可以通过专用寄存器来更新。

代码闪存在线性模式下最多可以划分为三个区域，在双模式下最多可以划分为六个区域。双模式下bank0和bank1的三个区域面积相同。数据闪存最多可分为两个区域。SRAM最多可分为三个区域。图52.1显示了内存映射。表52.1显示了内存区域的大小。

Note: It is prohibited to place Secure or Non-secure callable regions in a block swappable area in the linear mode because the secure application will be placed in the non-secure region after block swapping.

Note: The contents in Secure or Non-secure callable regions must be same in both bank0 and bank1 in the dual mode. Otherwise, the contents of secure or non-secure regions may not be latest by the field updating of non-secure region. See section 52.5. Field Updating in Dual Mode.

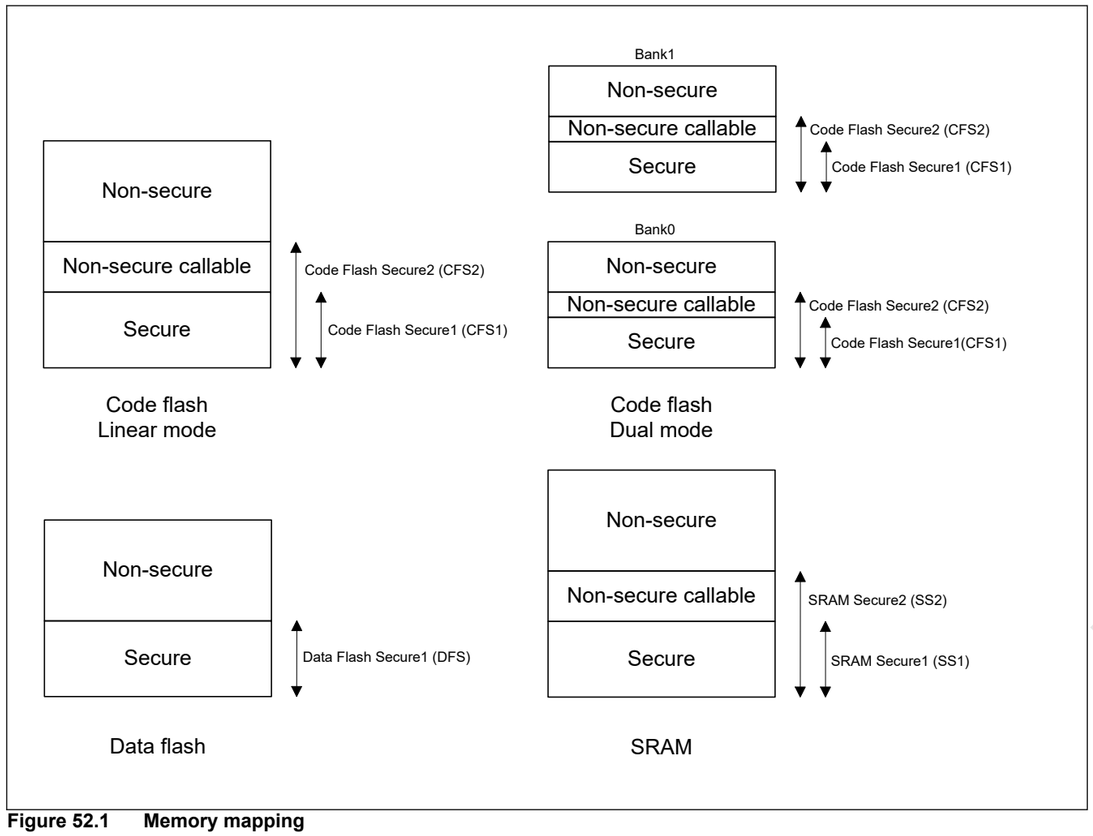

Figure 52.1 Memory mapping

Table 52.1 Memory Region Size (1 of 2)

Memory region		Start address	Size
Linear mode	Code flash secure	0x0000_0000	CFS1 × 1 KB
	Code flash non-secure callable	CFS1 × 1KB	CFS2 × 32 KB - CFS1 × 1 KB
	Code flash non-secure	CFS2 × 32 KB	Code flash size - CFS2 × 32 KB
Dual mode	Code flash bank0 secure	0x0000_0000	CFS1 × 1 KB
	Code flash bank0 non-secure callable	CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
	Code flash bank0 non-secure	CFS2 × 32 KB	Code flash size/2 - CFS2 × 32 KB
	Code flash bank1 secure	0x0020_0000	CFS1 × 1 KB
	Code flash bank1 non-secure callable	0x0020_0000 + CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
	Code flash bank1 non-secure	0x0020_0000 + CFS2 × 32 KB	Code flash size/2 - CFS2 × 32 KB
Data flash secure		0x0800_0000	DFS × 1 KB

Note: 禁止在线性模式下将Secure或Non-securecallable区域放置在块可交换区域中，因为在块交换后安全应用程序将被放置在非安全区域中。

Note: 双模式下，安全或非安全可调用区域的内容在bank0和bank1中必须相同。
否则，通过非安全区域的字段更新，安全或非安全区域的内容可能不是最新的。见第52.5节。双模式下的现场更新。

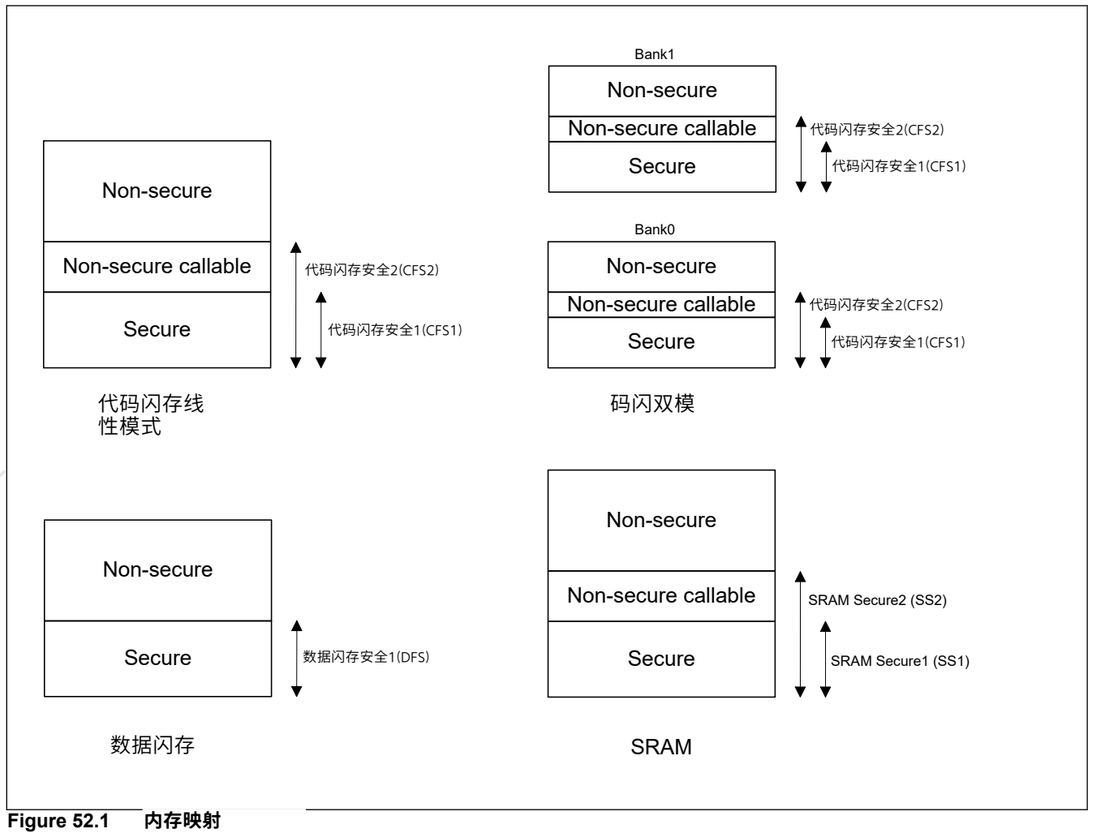

Figure 52.1 内存映射

Table 52.1 内存区域大小(1of2)

内存区域		起始地址	Size
线性模式	代码闪存安全	0x0000_0000	CFS1 × 1 KB
	代码闪存非安全可调用	CFS1 × 1KB	CFS2 × 32 KB - CFS1 × 1 KB
	代码闪存不安全	CFS2 × 32 KB	代码闪存大小CFS2×32KB
双模式	代码闪存bank0安全	0x0000_0000	CFS1 × 1 KB
	Codeflashbank0非安全可调用	CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
	代码闪存bank0不安全	CFS2 × 32 KB	代码闪存大小2CFS2×32KB
	代码闪存bank1安全	0x0020_0000	CFS1 × 1 KB
	Codeflashbank1非安全可调用	0x0020_0000 + CFS1 × 1 KB	CFS2 × 32 KB - CFS1 × 1 KB
	代码闪存bank1不安全	0x0020_0000 + CFS2 × 32 KB	代码闪存大小2CFS2×32KB
数据闪存安全		0x0800_0000	DFS × 1 KB

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Table 52.1 Memory Region Size (2 of 2)

Memory region	Start address	Size
Data flash non-secure	0x0800_0000 + DFS × 1 KB	Data flash size - DFS × 1 KB
SRAM secure	0x2000_0000	SS1 × 1 KB
SRAM non-secure callable	0x2000_0000 + SS1 × 1 KB	SS2 × 8 KB - SS1 × 1 KB
SRAM non-secure	0x2000_0000 + SS2 × 8 KB	SRAM size - SS2 × 8KB

The Standby SRAM is divided 8 regions. Security attribution can be set for each region, but both secure region and non-secure region must be contiguous. In other words, the Standby SRAM can have one contiguous secure region and one contiguous non-secure region. The Standby SRAM security attribution is set to the dedicated register by the secure application. See section 49, Standby SRAM for the details.

The VBATT backup register is divided 8 regions. Security attribution can be set for each region, but both secure region and non-secure region must be contiguous. In other words, the VBATT backup register can have one contiguous Secure region and one contiguous Non-secure region. The VBATT backup register security attribution is set to the dedicated register by the secure application. See section 11, Battery Backup Function for the details.

Table 52.2 shows the access permission of the memory.

Table 52.2 Access Permission of Memory

Memory	Secure access	Non-secure access
Code flash, Data flash, SRAM configured as Secure or Non-secure callable	allowed	Write ignored / Read ignored TrustZone Access error is generated
Code flash, Data flash, SRAM configured as non-secure	allowed	allowed
Standby SRAM, VBATT backup register configured as Secure	allowed	Write ignored / Read 0x00 TrustZone Access error is not generated
Standby SRAM, VBATT backup register configured as Non-secure	allowed	allowed

52.2.3 Peripheral Security Attribution

Each peripheral can be configured to be Secure or Non-secure.

Peripherals are divided into two types.

Type-1 peripherals has the one security attribution. Access to all registers is controlled by one security attribution. Type-1 peripheral security attribution is set to the PSARx (x = B to E) register by the secure application.

Type-2 peripherals has the security attribution for each register or for each bit. Access to each register or bit field is controlled according to these security attributions. Type-2 peripheral security attribution is set to the Security Attribution register in each module by the secure application. For the Security Attribution register, see sections in the user manual for each peripheral.

Table 52.3 shows the classification of peripheral type.

Table 52.3 Peripheral Type Classification

Type	Peripheral
Type-1	SCI, SPI, USBFS, USBHS, CANFD, IIC, CEC, SCE9, DOC, SDHI, SSIE, CTSU, CRC, CAC, TSN, ADC12, DAC12, POEG, AGT, GPT, RTC, IWDT, WDT
Type-2	System control (Resets, LVD, Clock Generation Circuit, Low Power Modes, Battery Backup Function), FLASH CACHE, SRAM controller, CPU CACHE, DMAC, DTC, ICU, MPU, BUS, Security setting, ELC, I/O ports
Always Non-secure	CS Area Controller, QSPI, OSPI, ETHERC, EDMAC

Table 52.4 shows the access permission of type-1 peripherals. The access permission of type-2 peripherals is different by peripherals. See section Register Description of each peripherals.

Table 52.1 内存区域大小（2个中的2个）

内存区域	起始地址	Size
数据闪存不安全	0x0800_0000 + DFS × 1 KB	数据闪存大小DFS×1KB
SRAM secure	0x2000_0000	SS1 × 1 KB
SRAM non-secure callable	0x2000_0000 + SS1 × 1 KB	SS2 × 8 KB - SS1 × 1 KB
SRAM non-secure	0x2000_0000 + SS2 × 8 KB	SRAM size - SS2 × 8KB

备用SRAM分为8个区域。可以为每个区域设置安全属性，但安全区域和非安全区域必须是连续的。换言之，StandbySRAM可以有一个连续的安全区域和一个连续的非安全区域。备用SRAM安全属性由安全应用程序设置到专用寄存器。有关详细信息，请参见第49节，备用SRAM。

VBATT备份寄存器分为8个区域。可以为每个区域设置安全属性，但安全区域和非安全区域必须是连续的。换句话说，VBATT备份寄存器可以有一个连续的安全区域和一个连续的非安全区域。VBATT备份寄存器安全属性由安全应用程序设置为专用寄存器。有关详细信息，请参阅第11节，电池备份功能。

表52.2显示了内存的访问权限。

Table 52.2 内存访问权限

Memory	安全访问	Non-secure access
代码闪存、数据闪存、SRAM配置为安全或非安全可调用	allowed	写被忽略读被忽略 生成TrustZone访问错误
代码闪存、数据闪存、配置为非安全的SRAM	allowed	allowed
备用SRAM、VBATT备份寄存器配置为安全	allowed	写入忽略读取0x00 未生成TrustZone访问错误
备用SRAM、VBATT备份寄存器配置为非安全	allowed	allowed

52.2.3 外围安全属性

每个外围设备都可以配置为安全或非安全。

外设分为两种。

Type-1外围设备具有唯一的安全属性。对所有寄存器的访问由一个安全属性控制。类型1外设安全属性由安全应用程序设置到PSARx（x=B到E）寄存器。

Type-2外设对每个寄存器或每个位都有安全属性。根据这些安全属性控制对每个寄存器或位字段的访问。类型2外围安全属性由安全应用程序设置到每个模块中的安全属性寄存器。对于安全属性寄存器，请参阅每个外设的用户手册中的部分。

表52.3显示了外围类型的分类。

Table 52.3 外设类型分类

Type	Peripheral
Type-1	SCI、SPI、USBFS、USBHS、CANFD、IIC、CEC、SCE9、DOC、SDHI、SSIE、CTSU、CRC、CAC、TSN、ADC12、DAC12、POEG, AGT, GPT, RTC, IWDT, WDT
Type-2	系统控制（复位、LVD、时钟生成电路、低功耗模式、电池备份功能）、FLASH CACHE、SRAM控制器、CPUCACHE、DMAC、DTC、ICU、MPU、BUS、安全设置、ELC、IO端口
Always Non-secure	CS区域控制器、QSPI、OSPI、ETHERC、EDMAC

表52.4显示了type-1外设的访问权限。type-2外设的访问权限因外设而异。请参阅每个外设的寄存器描述部分。

Table 52.4 The access permission of type-1 peripherals

Permission	Secure access	Non-secure access
Peripheral configured as secure	allowed	Write ignored / Read ignored TrustZone Access error is generated
Peripheral configured as non-secure	allowed	allowed

52.2.4 Flash Sequencer Security Attribution

The flash sequencer is used to program or erase the flash.

The flash sequencer has the special security attribution. Table 52.5 shows the access permission of flash sequencer.

Table 52.5 Access Permissions of Flash Sequencer

	Secure access	Non-secure access
FACI command issuing area	allowed	When the FACI command is issued to the secure region of code flash, data flash and option-setting memory ● Issued FACI command is invalid ● Flash sequencer error is generated When the FACI command is issued to the non-secure region of code flash, data flash and option-setting memory ● Issued FACI command is valid
FBPROT1, FSUACR, FMEPROT registers	allowed	Write ignored / Readable TrustZone Access error is not generated
FCKMHZ register	allowed	Configured by Flash Security Attribution register When configured as Secure, ● Write ignored / Readable ● TrustZone Access error is not generated. When configured as Non-secure ● allowed
Other registers	allowed	During programming/erasure or during suspend programming/erasure by secure application ● Write ignored / Read 0x00 ● TrustZone Access error is not generated In other state ● allowed

52.2.5 Address Space Security Attribution

Table 52.6 shows the security attribution of the address space.

Table 52.6 Address Space Security Attribution

Region	Attribution
Code flash secure	Secure
Code flash non-secure callable	Non-secure callable
Code flash non-secure	Non-secure
Data flash secure	Secure
Data flash non-secure	Non-Secure
SRAM secure	Secure
SRAM non-secure callable	Non-secure callable
SRAM non-secure	Non-secure
Peripherals	Exempt
External address space	Exempt
Other area	Exempt

Note: Exempt: No check will be done. All bus transactions are propagated.

Table 52.4 type-1外设的访问权限

Permission	安全访问	Non-secure access
外设配置为安全	allowed	写被忽略读被忽略 生成TrustZone访问错误
外设配置为非安全	allowed	allowed

52.2.4 FlashSequencer安全属性

闪存定序器用于对闪存进行编程或擦除。

闪存定序器具有特殊的安全属性。表52.5显示了flashsequencer的访问权限。

Table 52.5 FlashSequencer的访问权限

	安全访问	Non-secure access
FACI指令发布区	allowed	当FACI命令被发送到代码闪存、数据闪存和选项设置存储器的安全区域时● 发出的FACI命令无效 ● 产生闪存定序器错误 当FACI命令被发送到代码闪存、数据闪存和选项设置存储器的非安全区域时● 发出的FACI命令有效
FBPROT1, FSUACR, FMEPROT registers	allowed	写忽略可读 未生成TrustZone访问错误
FCKMHZ register	allowed	由Flash安全属性寄存器配置 当配置为安全时，● 写忽略可读 ● 未生成TrustZone访问错误。 当配置为非安全时●
其他寄存器	allowed	在编程擦除期间或在安全应用程序的暂停编程擦除期间● 写入忽略读取0x00 ● 未生成TrustZone访问错误 在其他状态 ●

52.2.5 地址空间安全属性

表52.6显示了地址空间的安全属性。

Table 52.6 地址空间安全属性

Region	Attribution
代码闪存安全	Secure
代码闪存非安全可调用	Non-secure callable
代码闪存不安全	Non-secure
数据闪存安全	Secure
数据闪存不安全	Non-Secure
SRAM secure	Secure
SRAM non-secure callable	Non-secure callable
SRAM non-secure	Non-secure
Peripherals	Exempt
外部地址空间	Exempt
其他区域	Exempt

Note: 豁免：不会进行任何检查。传播所有总线事务。

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52.2.6 TrustZone Access Error

Table 52.7 shows the behavior when TrustZone access error. The behavior varies depending on the master or slave area to be accessed.

Table 52.7 The Behavior When TrustZone Access Error

Area	CPU	DMAC/DTC	EDMAC
Code flash, Data flash, SRAM	Detect SecureFault exception*2	• Transfer does not start • Occur NMI or reset*1 • Occur interrupt (DMA_TRANSERR)	• Stop transfer • Occur NMI or reset*1 • Occur interrupt (ETHER_EINT0)*3
Other area	• Detect BusFault exception*2 *4 • Occur NMI or reset*1*2 *4	• Stop transfer*5 • Occur NMI or reset*1 *5 • Occur interrupt (DMA_TRANSERR)*5	No TrustZone access error occurs

Note 1. NMI or reset is selected with TZFOAD.OAD bit.
Note 2. When TrustZone access error occurs by the debugger access, exception, NMI, or reset does not occurs. Only the error response is returned.
Note 3. Address error flag in EESR.ADE bit is set. The interrupt occurs when interrupt is enabled in EESIPR.ADEIP bit.
Note 4. These error behaviors does not occur for write access to the PHBIU or PLBIU address space which memory attribute is set to "Early Write Acknowledgment" by the ARM MPU.
Note 5. These error behaviors does not occer for write access from DMAC to the PHBIU or PLBIU address space when the bufferable write is enabled by DMBWR.BWE.

52.3 Device Lifecycle Management

Device lifecycle identifies the current phase of the device and controls the capabilities of the debug interface, the serial programming interface and Renesas test mode. Figure 52.2 is the illustration of the device lifecycle. Table 52.8 shows the lifecycle definition and capability in each lifecycle.

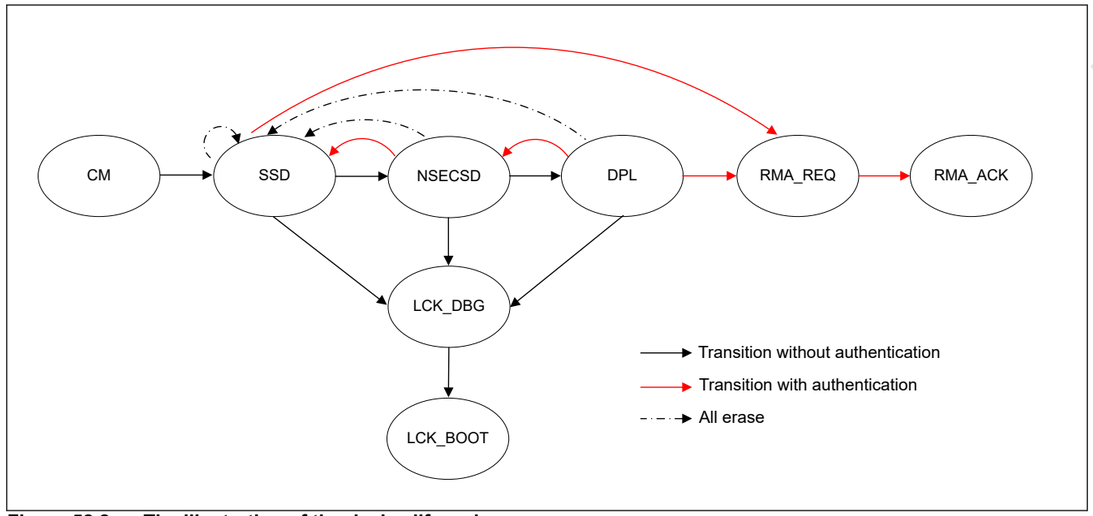

Figure 52.2 The illustration of the device lifecycle

Table 52.8 The lifecycle definition and the capability can be used in each lifecycle (1 of 2)

Lifecycle	Definition	Debug level	Serial programming	Renesas test mode
CM	"Chip Manufacturing" The device is in Renesas factory. The state when the customer received the device.	DBG2	Available cannot access code/data flash area	Not available

52.2.6 TrustZone访问错误

表52.7显示了TrustZone访问错误时的行为。行为因要访问的主区域或从区域而异。

Table 52.7 TrustZone访问错误时的行为

Area	CPU	DMAC/DTC	EDMAC
代码闪存、数据闪存、SRAM	检测SecureFault异常*2	• 传输未开始 • 发生NMI或复位*1 • 发生中断(DMA_TRANSERR)	• 停止转移 • 发生NMI或复位*1 • 发生中断(ETHER_EINT0)*3
其他区域	• 检测BusFault异常*2*4 • 发生NMI或复位*1*2 *4	• 停止传输*5 • 发生NMI或复位*1*5 • 发生中断(DMA_TRANSERR)*5	未发生TrustZone访问错误

注1.通过TZFOAD.OAD位选择NMI或复位。
注2.当调试器访问发生TrustZone访问错误时，不会发生异常、NMI或复位。只返回错误响应。

注3.设置EESR.ADE位中的地址错误标志。当在ESIPR.ADEIP位中使能中断时，会发生中断。
注4.对内存属性设置为"Early"的PHBIU或PLBIU地址空间的写访问不会发生这些错误行为
ARMMPU的"写确认"。
注5.当DMBWR.BWE启用可缓冲写时，这些错误行为不会发生在从DMAC到PHBIU或PLBIU地址空间的写访问中。

52.3 设备生命周期管理

设备生命周期识别设备的当前阶段并控制调试接口、串行编程接口和瑞萨测试模式的功能。图52.2是设备生命周期的图示。表52.8显示了每个生命周期中的生命周期定义和能力。

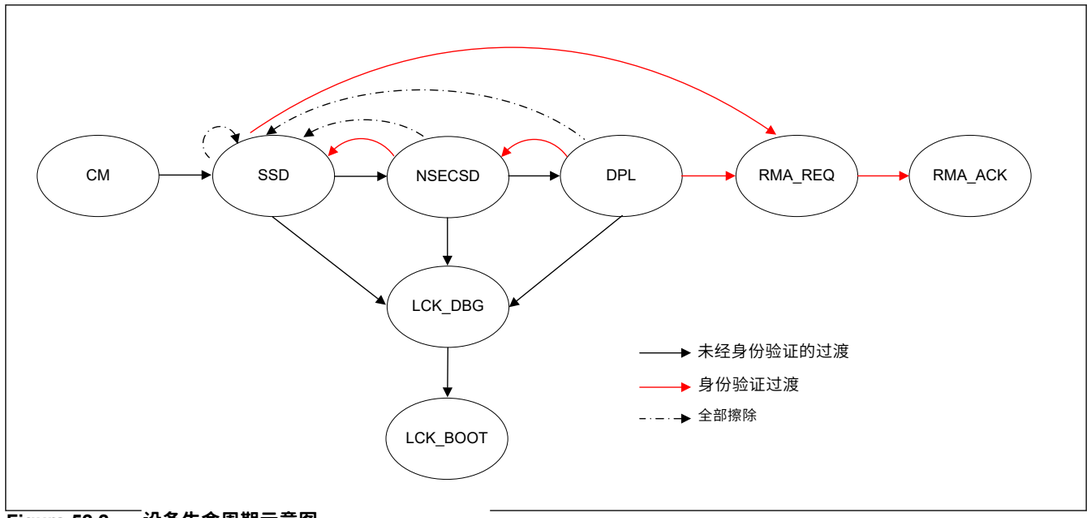

Figure 52.2 设备生命周期示意图

Table 52.8 生命周期定义和能力可以在每个生命周期中使用（1of2）

Lifecycle	Definition	调试级别	串行编程	瑞萨测试模式
CM	"Chip Manufacturing" 该设备在瑞萨电子工厂。客户收到设备时的状态。	DBG2	Available 无法访问代码数据闪存区	无法使用

Table 52.8 The lifecycle definition and the capability can be used in each lifecycle (2 of 2)

Lifecycle	Definition	Debug level	Serial programming	Renesas test mode
SSD	“Secure Software Development” The secure part of application is being developed.	DBG2	Available can program/erase/read all code/data flash area	Not available
NSECSD	“Non-SECure Software Development” The non-secure part of application is being developed.	DBG1	Available can program/erase/read only non-secure code/data flash area	Not available
DPL	“DePLoyed” The device is in-field.	DBG0	Available cannot access code/data flash area	Not available
LCK_DBG	“LoCKed DeBuG” The debug interface is permanently disabled.	DBG0	Available cannot access code/data flash area	Not available
LCK_BOOT	“LoCKed BOOT interface” The debug interface and the serial programming interface are permanently disabled.	DBG0	Not available	Not available
RMA_REQ	“Return Material Authorization REQuest” Request for RMA. The customer must send the device to Renesas in this state.	DBG0	Available cannot access code/data flash area	Not available
RMA_ACK	“Return Material Authorization ACKnowledged” Failure analysis in Renesas	DBG2	Available cannot access code/data flash area	Available

52.3.1 Changing the Lifecycle State

Use the serial programming commands to change the device lifecycle state. See the boot firmware application note for the detail of command. The lifecycle cannot be updated by application but can read through the dedicated registers.

As shown in Figure 52.2, there are three types lifecycle transition.

The first one is to change to lower debug access level or restrict the serial programming mode. This change can be done with no restriction.

Note: The debug interface is permanently disabled in LCK_DBG. After changed to LCK_DBG, the debug interface cannot be used forever.

Note: The debug interface and serial programming interface are permanently disabled in LCK_BOOT. After changed to LCK_BOOT, the debug interface and the serial programming interface cannot be used forever.

The second one is to change to higher debug access level or request for RMA. This change needs key authentication. The key length is 128 bits. The secure developer needs to inject two keys when the lifecycle is SSD state. One is “SECDBG_KEY” which is used to authentication to change the lifecycle from NSECSD to SSD. Other one is “RMA_KEY” which is used to authentication to change the lifecycle from SSD or DPL to RMA_REQ. The non-secure developer needs to inject one key when the lifecycle is NSECSD state. This is “NONSECDBG_KEY” which is used to authentication to change the lifecycle from DPL to NSECSD. See section 52.4. Key Injection for the detail of how to inject the key. The key authentication uses a challenge and response authentication or authentication using the unique ID. The authentication using the unique ID is available only transition to RMA_REQ. The following is the process of how to calculate the response, challenge and response authentication, or the authentication code using unique ID.

Response = HMAC-SHA256 (KEY, 128bits challenge || fixed value (256bits))

Authentication code = HMAC-SHA256 (KEY, 128bits unique ID || fixed value (256 bits))

fixed value = 9e56dc41 cf0c9648 1b811141 f8f9ba1e 4dd77746 6d403593 17f46d64 fe64fdf6

Note: That "||" represents concatenation, not logical or.

Table 52.8 可以在每个生命周期中使用生命周期定义和能力（2个中的2个）

Lifecycle	Definition	调试级别	串行编程	瑞萨测试模式
SSD	“Secure Software Development” 应用程序的安全部分正在开发中。	DBG2	Available 可以编程擦除读取所有代码数据闪存区域	无法使用
NSECSD	“Non-SECure Software Development” 应用程序的非安全部分正在开发中。	DBG1	Available 可以编程擦除只读非安全代码数据闪存区域	无法使用
DPL	“DePLoyed” 该设备在现场。	DBG0	Available 无法访问代码数据闪存区	无法使用
LCK_DBG	“LoCKed DeBuG” 调试接口被永久禁用。	DBG0	Available 无法访问代码数据闪存区	无法使用
LCK_BOOT	“LoCKed BOOT interface” 调试接口和串行编程接口被永久禁用。	DBG0	无法使用	无法使用
RMA_REQ	“退货授权请求” 请求RMA。客户必须在此状态下将设备发送给瑞萨电子。	DBG0	Available 无法访问代码数据闪存区	无法使用
RMA_ACK	“已确认退货授权” 瑞萨电子的故障分析	DBG2	Available 无法访问代码数据闪存区	Available

52.3.1 更改生命周期状态

使用串行编程命令更改设备生命周期状态。有关命令的详细信息，请参见启动固件应用说明。生命周期不能由应用程序更新，但可以通过专用寄存器读取。

如图52.2所示，生命周期转换分为三种。

第一个是更改为降低调试访问级别或限制串行编程模式。这种改变可以不受限制地进行。

Note: 调试接口在LCK_DBG中被永久禁用。改成LCK_DBG后，调试接口就不能一直使用了。

Note: 调试接口和串行编程接口在LCK_BOOT中永久禁用。改成之后LCK_BOOT、调试接口和串行编程接口不能永远使用。

第二个是更改为更高的调试访问级别或请求RMA。此更改需要密钥身份验证。密钥长度为128位。当生命周期为SSD状态时，安全开发人员需要注入两个密钥。一种是“SECDBG_KEY”，用于身份验证以将生命周期从NSECSD更改为SSD。另一种是“RMA_KEY”，用于身份验证以将生命周期从SSD或DPL更改为RMA_REQ。当生命周期为NSECSD状态时，非安全开发者需要注入一个密钥。这是“NONSECDBG_KEY”，用于身份验证以将生命周期从DPL更改为NSECSD。见第52.4节。KeyInjection有关如何注入密钥的详细信息。密钥身份验证使用质询和响应身份验证或使用唯一ID的身份验证。使用唯一ID的身份验证只能转换到RMA_REQ。以下是如何计算响应、挑战和响应身份验证或使用唯一ID的身份验证码的过程。

响应=HMAC-SHA256(KEY 128bitschallengeFixedvalue(256bits))

认证码=HMAC-SHA256（KEY，128bits唯一ID固定值（256bits））

固定值=9e56dc41cf0c96481b811141f8f9ba1e4dd777466d40359317f46d64fe64fdf6

Note: 那“”代表连接，不是逻辑或。

Note: In case the key is not injected, these lifecycle changes cannot be done.

Note: In the lifecycle transition from NSECSD to SSD or form DPL to NSECSD, the contents on the flash memory are not erased.

Note: MCU does not respond after changing to higher debug access level or RMA_REQ. If you continue to use the serial programming commands, need to re-enter the boot mode after a reset. See the boot firmware application note for the detail.

Note: In the lifecycle transition to RMA_REQ, the contents on the flash memory except permanently locked block or setting or BPS_SEL register are erased. The contents in the permanently locked block or register can be read by Renesas at failure analysis. Permanently rocked block means the block which programming and erasure is disabled permanently by PBPS, PBPS_SEC and BPS_SEL register. Permanently rocked register means SAS register which programming and erasure is disabled permanently by FSPR bit.

The third one is all erase. This is done by an initialize command unless an initialize command itself is disabled. The lifecycle is back to SSD and the contents on the flash memory is erased. If there is permanently locked block or register, an initialize command does not execute. In case of the all bits of PBPS and PBPS_SEC register are 1 and FSPR bit is1, an initialize command is executable.

Note: The initialize command can be issued by everyone, so contents on the flash memory are easily erased. Developers who do not want this can invalidate the initialize command permanently by parameter setting command.

Note: MCU does not respond after executing the initialize command. If you continue to use the serial programming commands, need to re-enter the boot mode after a reset. See the boot firmware application note for the detail.

52.3.2 Debug access level

There are three debug access levels, and the debug access level changes according to the lifecycle state.

- DBG2: The debugger connection is allowed, and no restriction to access memories and peripherals
- DBG1: The debugger connection is allowed, and restricted to access only non-secure memory regions and peripherals
- DBG0: The debugger connection is not allowed

52.3.3 Serial Programming

Whether a serial programmer can be connected and the range of flash memory that can be accessed depends on the lifecycle state as shown in Table 52.8. And the accepted serial programming command differs depending on the lifecycle state. See the boot firmware application note for the detail of command.

52.3.4 Lifecycle changing example

The following is a typical lifecycle changing example.

Secure developer

- Change the lifecycle from CM to SSD by using the serial programming command.
- Set the memory security attribution of the code flash, data flash and SRAM by using the serial programming command.
- Program the secure application by using the serial programming interface and debug the secure application. Debug is possible if the lifecycle is CM, but it is impossible to set the memory security attribution in CM state. If the memory security attribution is not set, all area of the code flash, data flash and SRAM is Secure.

Note: Need to configure the registers listed in Table 52.10 as Non-secure only in NSECSD state. See section 52.7.1. Restrictions on setting the security attribution for details.

- Inject “SECDBG_KEY” and “RMA_KEY” by using the serial programming command (if need).
- Inject AES, RSA, ECC, HMAC keys listed in Table 52.9 (if need).
- Disable the all erase by using the serial programming command (if need).
- Change the lifecycle from SSD to NSECSD by using the serial programming command.

Note: 如果未注入密钥，则无法完成这些生命周期更改。

Note: 在从NSECSD到SSD或从DPL到NSECSD的生命周期转换中，闪存上的内容不会被擦除。

Note: 更改为更高的调试访问级别或RMA_REQ后，MCU没有响应。如果继续使用串口编程命令，需要复位后重新进入开机模式。有关详细信息，请参阅启动固件应用说明。

Note: 在到RMA_REQ的生命周期转换中，闪存上的内容除了永久锁定的块或设置或BPS_SEL寄存器外被擦除。瑞萨在故障分析时可以读取永久锁定的块或寄存器中的内容。永久摇动块是指被PBPS、PBPS_SEC和BPS_SEL寄存器永久禁用编程和擦除的块。永久摇动寄存器是指通过FSPR位永久禁用编程和擦除的SAS寄存器。

第三个是全部擦除。这由初始化命令完成，除非初始化命令本身被禁用。生命周期回到SSD，闪存上的内容被擦除。如果存在永久锁定的块或寄存器，则不会执行初始化命令。如果PBPS和PBPS_SEC寄存器的所有位为1，FSPR位为1，则可执行初始化命令。

Note: 每个人都可以发出初始化命令，因此闪存上的内容很容易被擦除。不希望这样的开发者可以通过参数设置命令使初始化命令永久无效。

Note: 执行初始化命令后MCU没有响应。如果继续使用串口编程命令，需要复位后重新进入开机模式。有关详细信息，请参阅启动固件应用说明。

52.3.2 调试访问级别

共有三个调试访问级别，调试访问级别根据生命周期状态而变化。

●DBG2：允许调试器连接，不限制访问内存和外设

●DBG1：允许调试器连接，但仅限于访问非安全内存区域和外围设备

●DBG0：不允许调试器连接

52.3.3 串行编程

是否可以连接串行编程器以及可以访问的闪存范围取决于生命周期状态，如表52.8所示。并且接受的串行编程命令根据生命周期状态而有所不同。有关命令的详细信息，请参见启动固件应用说明。

52.3.4 生命周期更改示例

以下是一个典型的生命周期更改示例。

安全开发人员

●使用串行编程命令将生命周期从CM更改为SSD。

●使用串行编程命令设置codeflash、dataflash和SRAM的内存安全属性。

●使用串行编程接口对安全应用程序进行编程并调试安全应用程序。如果生命周期是CM，则可以调试，但无法在CM状态下设置内存安全属性。如果未设置内存安全属性，则代码闪存、数据闪存和SRAM的所有区域都是安全的。

Note: 仅在NSECSD状态下需要将表52.10中列出的寄存器配置为非安全。请参阅第52.7.1节。
设置安全属性的限制以获取详细信息。

●使用串行编程命令（如果需要）注入“SECDBG_KEY”和“RMA_KEY”。

●注入表52.9中列出的AES、RSA、ECC、HMAC密钥（如果需要）。

●使用串行编程命令禁用全部擦除（如果需要）。

●使用串行编程命令将生命周期从SSD更改为NSECSD。

Non-secure developer

- Program the Non-secure application by using the serial programming interface and debug the Non-secure application.
- Inject “NONSECDBG_KEY” by using the serial programming command (if need).
- Inject AES, RSA, ECC, HMAC keys listed in Table 52.9 (if need).
- Disable the all erase by using the serial programming command (if need).
- Change the lifecycle to DPL by using the serial programming command.

52.3.5 Failure analysis

If the customer requests the failure analysis to Renesas, it is necessary to send the device after changing the lifecycle to RMA_REQ. If the lifecycle is not RMA_REQ, Renesas can not do the failure analysis. Because RMA_REQ is permanent state, it can not back to the another state after changing to RMA_REQ. It is assumed to change to SSD or NSECSD and analyze before changing to RMA_REQ.

Devices sent to Renesas will not be returned to customers. The device will be discarded.

Note: As described in the section 52.3.1. Changing the Lifecycle State, RMA_KEY is needed to change the lifecycle to RMA_REQ. If the customer forgets the RMA_KEY, Renesas can not do the failure analysis.

52.4 Key Injection

There are three steps required to inject a user key into the MCU.

First, the customer needs to create the 128 bits installation key. This key is called User Factory Programming Key (UFPK) and used to encrypt a user key. The customer gets the key of the wrapped version (W-UFPK) through the Renesas Key Wrapping Service.

Second the customer encrypts the user key using UFPK as the AES key.

Last the customer sends W-UFPK and the encrypted user key to the MCU by using serial programming interface. The sent user key is decrypted, wrapped with the hardware unique key, and then stored in the nonvolatile memory.

Figure 52.3 is the illustration of key injection. Table 52.9 shows the keys that can be injected by serial programming interface.

User Key is also used for authentication during the life cycle transition.

Non-secure developer

●使用串行编程接口对非安全应用程序进行编程并调试非安全应用程序。

●使用串行编程命令（如果需要）注入“NONSECDBG_KEY”。

●注入表52.9中列出的AES、RSA、ECC、HMAC密钥（如果需要）。

●使用串行编程命令禁用全部擦除（如果需要）。

●使用串行编程命令将生命周期更改为DPL。

52.3.5 故障分析

如果客户要求对瑞萨进行故障分析，则需要在将生命周期更改为RMA_REQ后发送设备。如果生命周期不是RMA_REQ，瑞萨将无法进行故障分析。因为RMA_REQ是永久状态，所以在更改为RMA_REQ后不能回到另一个状态。假设更改为SSD或NSECSD并在更改为RMA_REQ之前进行分析。

发送给瑞萨的设备将不会退还给客户。该设备将被丢弃。

Note: 如第52.3.1节所述。更改LifecycleState，需要RMA_KEY才能将生命周期更改为RMA_REQ。如果客户忘记了RMA_KEY，瑞萨将无法进行故障分析。

52.4 密钥注入

将用户密钥注入MCU需要三个步骤。

首先，客户需要创建128位安装密钥。此密钥称为用户工厂编程密钥(UFPK)，用于加密用户密钥。客户通过RenesasKeyWrappingService获得打包版本(W-UFPK)的密钥。

其次，客户使用UFPK作为AES密钥对用户密钥进行加密。

最后客户通过串行编程接口将W-UFPK和加密的用户密钥发送给MCU。发送的用户密钥被解密，用硬件唯一密钥包装，然后存储在非易失性存储器中。

图52.3是密钥注入的示意图。表52.9显示了串行编程接口可以注入的密钥。

用户密钥还用于生命周期转换期间的身份验证。

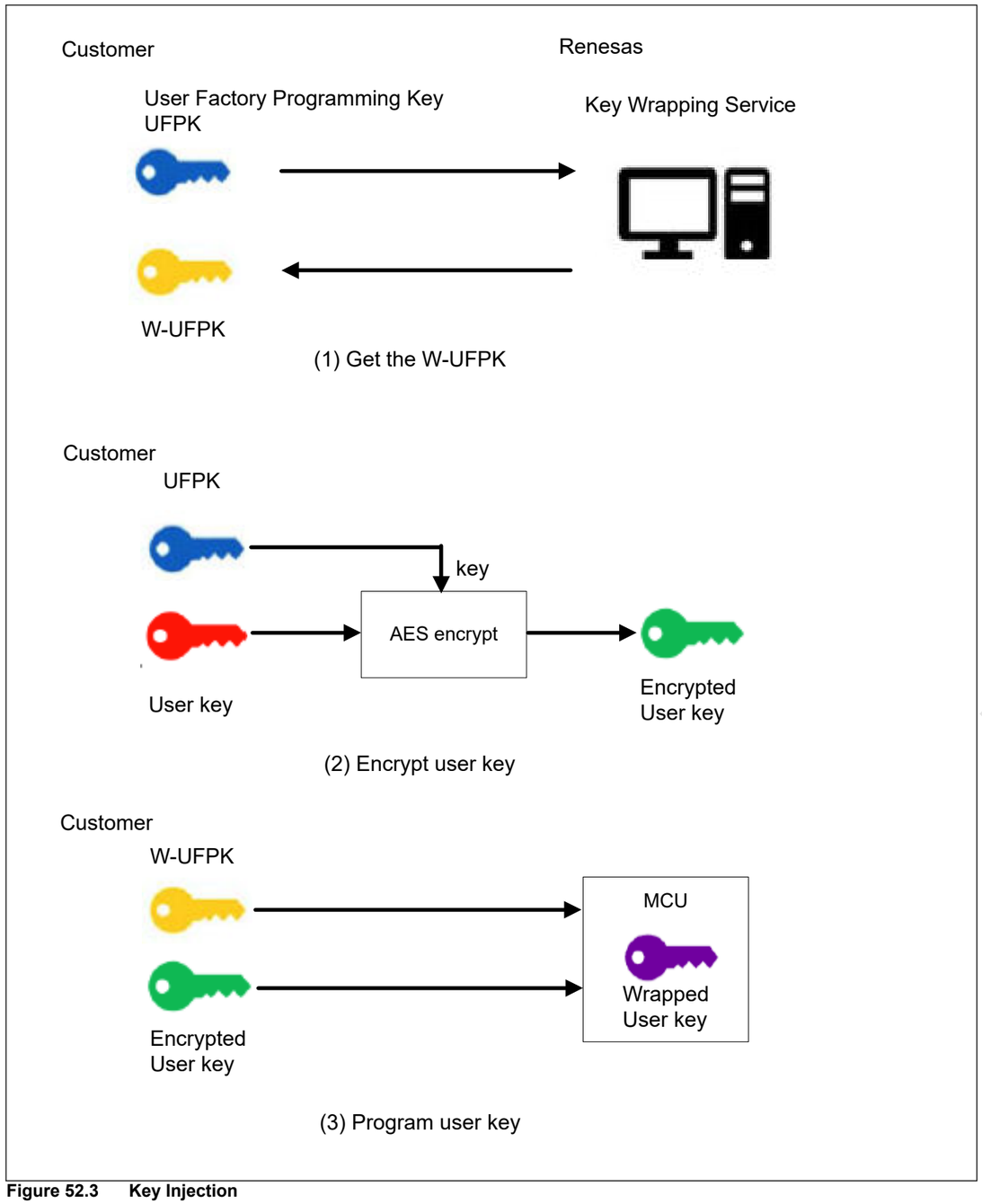

Figure 52.3 Key Injection

Table 52.9 The keys that can be injected by serial programming (1 of 2)

Lifecycle transition	SECDBG_KEY, NONSECDBG_KEY, RMA_KEY
AES	AES-128, AES-192, AES-256, AES-XTS-128, AES-XTS-256
RSA	RSA-1024, RSA-2048, RSA-3072, RSA-4096 (Public and Private)

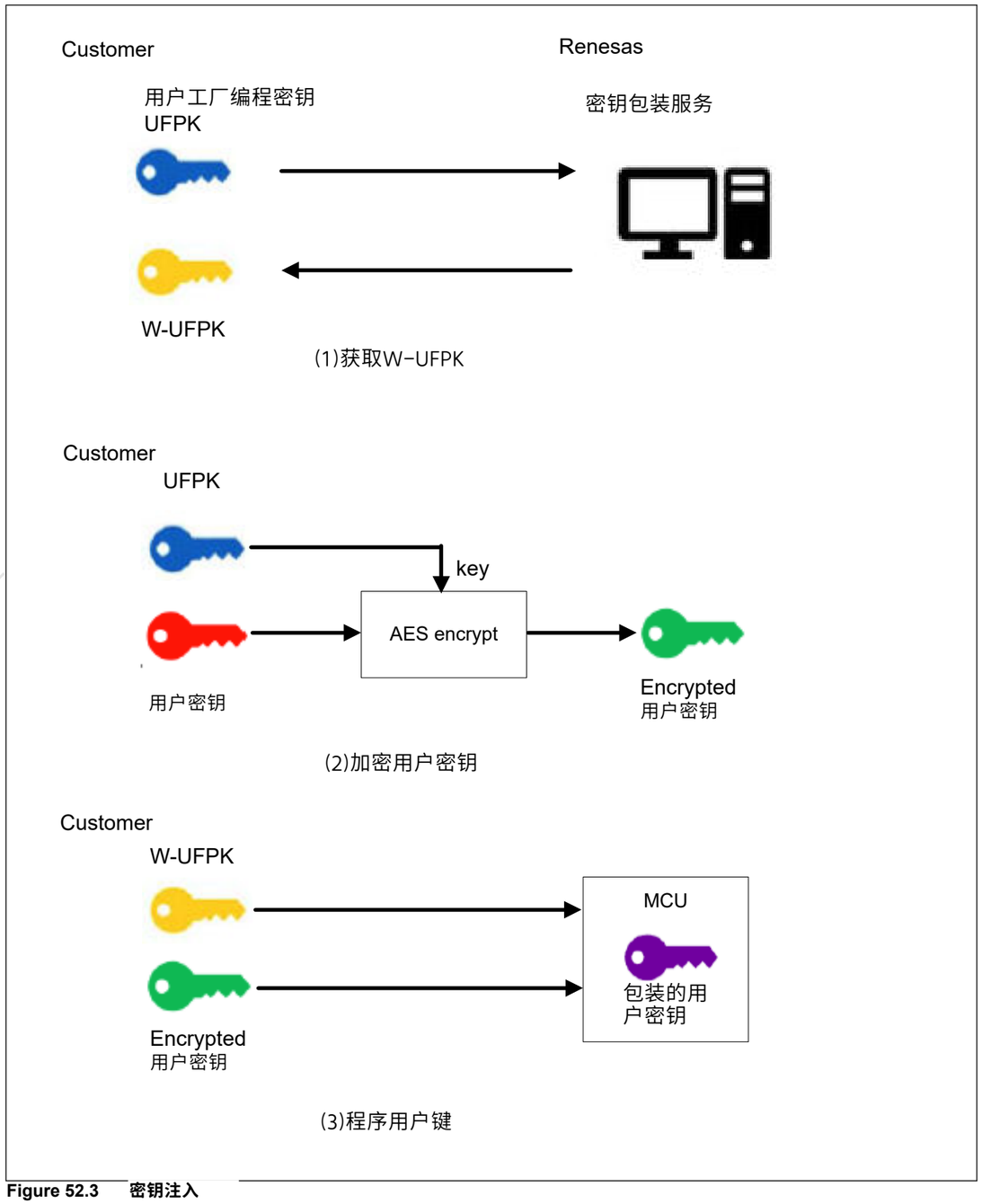

Figure 52.3 密钥注入

Table 52.9 可以通过串行编程注入的密钥（1of2）

生命周期过渡	SECDBG_KEY, NONSECDBG_KEY, RMA_KEY
AES	AES-128, AES-192, AES-256, AES-XTS-128, AES-XTS-256
RSA	RSA-1024, RSA-2048, RSA-3072, RSA-4096 (Public and Private)

Table 52.9 The keys that can be injected by serial programming (2 of 2)

ECC	ECC P192, ECC P224, ECC P256, ECC P384, ECC P512 (Public and Private)
HMAC	HMAC-SHA224, HMAC-SHA256

52.5 Field Updating in Dual Mode

Be careful when performing in-field update of information to keep the contents of secure or non-secure regions after bank swapping in the dual mode. Figure 52.4 and Figure 52.5 shows the performing in-field update of information flow of secure or non-secure regions in the dual mode.

In this example of Figure 52.4, BANK0 is valid, and Version 1 information is stored in NS and S or NSC.

BANK1 is blank. To update the S or NSC information in the field to Version 2, first copy the version 1 information of BANK0 to NS, update the S or NSC to Version 2, and then execute the Bank swap.

In this example of Figure 52.5, BANK0 is valid, and Version 1 information is stored in NS and S or NSC. BANK1 is blank.

To update the NS information in the field and set it to Version 2, First of all, non-secure users should have the Secure user copy the version 1 information of BANK0 to BANK1.

After that, Non secure user should update NS information to Version 2 and execute BANK swap.

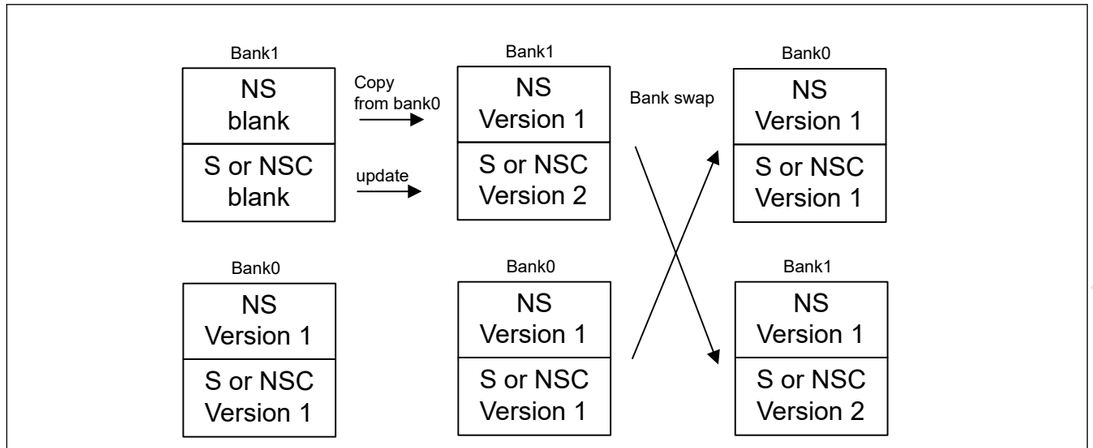

Figure 52.4 The field updating flow of secure or non-secure callable regions

Table 52.9 可以通过串行编程注入的密钥(2of2)

ECC	ECC P192, ECC P224, ECC P256, ECC P384, ECC P512 (Public and Private)
HMAC	HMAC-SHA224, HMAC-SHA256

52.5 双模式下的现场更新

执行信息的现场更新时要小心，以在双模式下进行银行交换后保持安全或非安全区域的内容。图52.4和图52.5显示了在双模式下对安全或非安全区域的信息流进行现场更新。

在图52.4的这个例子中，BANK0是有效的，版本1信息存储在NS和S或NSC中。

BANK1为空白。要将字段中的S或NSC信息更新到版本2，首先复制版本1的信息BANK0到NS，将S或NSC更新到版本2，然后执行Bank交换。

在图52.5的这个例子中，BANK0是有效的，版本1信息存储在NS和S或NSC中。BANK1为空白。

要更新字段中的NS信息并将其设置为版本2，首先，非安全用户应让安全用户将BANK0的版本1信息复制到BANK1。

之后，非安全用户应将NS信息更新到版本2并执行BANK交换。

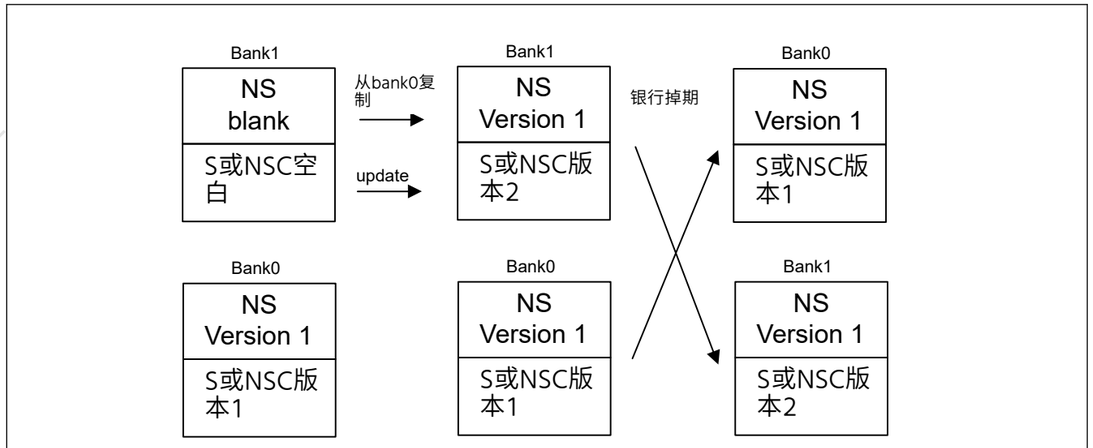

Figure 52.4 安全或非安全可调用区域的字段更新流程

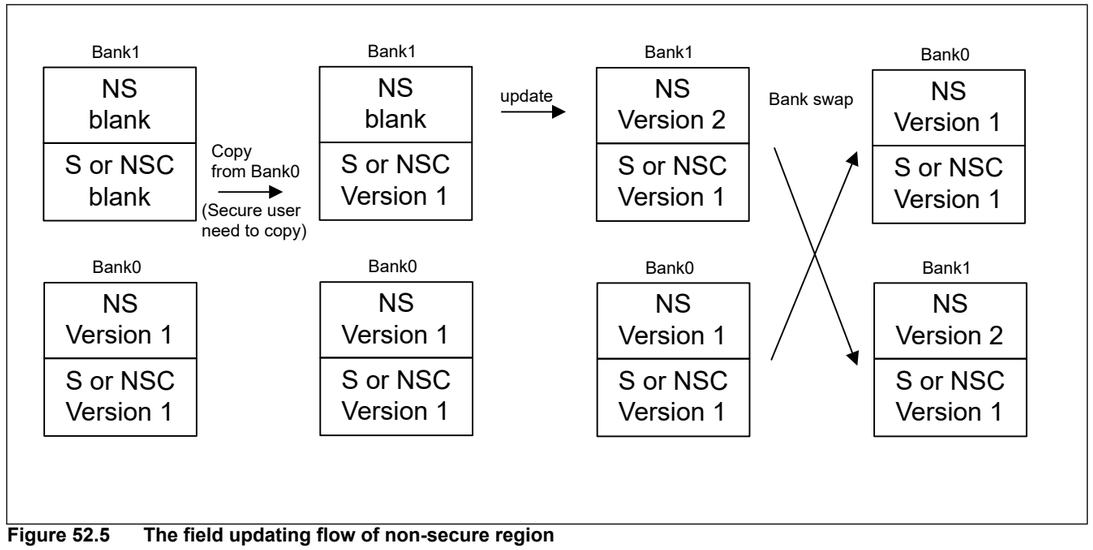

Figure 52.5 The field updating flow of non-secure region

52.6 Register Description

52.6.1 PSARB : Peripheral Security Attribution Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARB31	PSARB30	PSARB29	PSARB28	PSARB27	PSARB26	PSARB25	PSARB24	PSARB23	PSARB22	—	—	PSARB19	PSARB18	—	PSARB16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSARB15	—	—	PSARB12	PSARB11	—	PSARB9	PSARB8	PSARB7	PSARB6—	—	—	PSARB3	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	—	This bit is read as 1. The write value should be 1.	R/W
1	—	This bit is read as 1. The write value should be 1.	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	PSARB3	CEC and the MSTPCRB.MSTPB3 bit security attribution 0: Secure 1: Non-secure	R/W
5:4	—	These bits are read as 1. The write value should be 1.	R/W
6	PSARB6	QSPI and the MSTPCRB.MSTPB6 bit security attribution This bit is read as 1 (non-secure).	R
6	—	This bit is read as 1. The write value should be 1.	R/W
7	PSARB7	IIC2 and the MSTPCRB.MSTPB7 bit security attribution 0: Secure 1: Non-secure	R/W

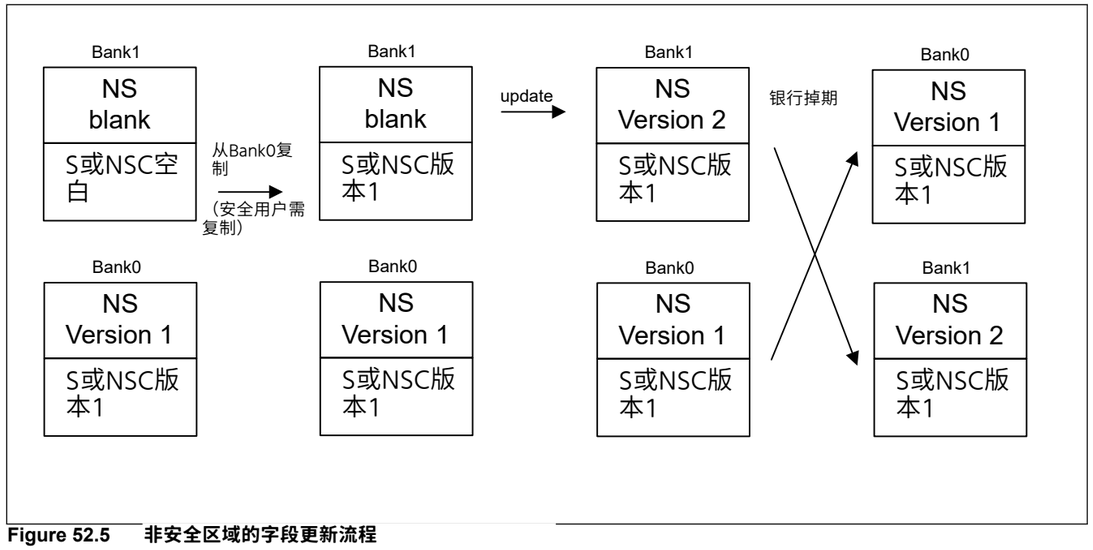

Figure 52.5 非安全区域的字段更新流程

52.6 注册说明

52.6.1 PSARB:外设安全属性寄存器B

Base address: PSCU = 0x400E_0000

Offset address: 0x04

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARB31	PSARB30	PSARB29	PSARB28	PSARB27	PSARB26	PSARB25	PSARB24	PSARB23	PSARB22	—	—	PSARB19	PSARB18	—	PSARB16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSARB15	—	—	PSARB12	PSARB11	—	PSARB9	PSARB8	PSARB7	PSARB6—	—	—	PSARB3	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	—	该位读取为1。写入值应为1。	R/W
1	—	该位读取为1。写入值应为1。	R/W
2	—	该位读取为1。写入值应为1。	R/W
3	PSARB3	CEC和MSTPCRB.MSTPB3位安全归属 0: Secure 1: Non-secure	R/W
5:4	—	这些位被读取为1。写入值应为1。	R/W
6	PSARB6	QSPI和MSTPCRB.MSTPB6位安全属性 该位读为1（非安全）。	R
6	—	该位读取为1。写入值应为1。	R/W
7	PSARB7	IIC2和MSTPCRB.MSTPB7位安全归属 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
8	PSARB8	IIC1 and the MSTPCRB.MSTPB8 bit security attribution 0: Secure 1: Non-secure	R/W
9	PSARB9	IIC0 and the MSTPCRB.MSTPB9 bit security attribution 0: Secure 1: Non-secure	R/W
10	—	This bit is read as 1. The write value should be 1.	R/W
11	PSARB11	USBFS and the MSTPCRB.MSTPB11 bit security attribution 0: Secure 1: Non-secure	R/W
12	PSARB12	USBHS and the MSTPCRB.MSTPB12 bit security attribution 0: Secure 1: Non-secure	R/W
14:13	—	These bits are read as 1. The write value should be 1.	R/W
15	PSARB15	ETHER0/EDMAC0, the MSTPCRB.MSTPB15 bit and the PFENET.PHYMODE0 bit security attribution This bit is read as 1 (non-secure).	R
16	PSARB16	OSPI and the MSTPCRB.MSTPB16 bit security attribution This bit is read as 1 (non-secure).	R
17	—	This bit is read as 1. The write value should be 1.	R/W
18	PSARB18	SPI1 and the MSTPCRB.MSTPB18 bit security attribution 0: Secure 1: Non-secure	R/W
19	PSARB19	SPI0 and the MSTPCRB.MSTPB19 bit security attribution 0: Secure 1: Non-secure	R/W
21:20	—	These bits are read as 1. The write value should be 1.	R/W
22	PSARB22	SCI9 and the MSTPCRB.MSTPB22 bit security attribution 0: Secure 1: Non-secure	R/W
23	PSARB23	SCI8 and the MSTPCRB.MSTPB23 bit security attribution 0: Secure 1: Non-secure	R/W
24	PSARB24	SCI7 and the MSTPCRB.MSTPB24 bit security attribution 0: Secure 1: Non-secure	R/W
25	PSARB25	SCI6 and the MSTPCRB.MSTPB25 bit security attribution 0: Secure 1: Non-secure	R/W
26	PSARB26	SCI5 and the MSTPCRB.MSTPB26 bit security attribution 0: Secure 1: Non-secure	R/W
27	PSARB27	SCI4 and the MSTPCRB.MSTPB27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARB28	SCI3 and the MSTPCRB.MSTPB28 bit security attribution 0: Secure 1: Non-secure	R/W
29	PSARB29	SCI2 and the MSTPCRB.MSTPB29 bit security attribution 0: Secure 1: Non-secure	R/W
30	PSARB30	SCI1 and the MSTPCRB.MSTPB30 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
8	PSARB8	IIC1和MSTPCRB.MSTPB8位安全归属 0: Secure 1: Non-secure	R/W
9	PSARB9	IIC0和MSTPCRB.MSTPB9位安全归属 0: Secure 1: Non-secure	R/W
10	—	该位读取为1。写入值应为1。	R/W
11	PSARB11	USBFS和MSTPCRB.MSTPB11位安全属性 0: Secure 1: Non-secure	R/W
12	PSARB12	USBHS和MSTPCRB.MSTPB12位安全属性 0: Secure 1: Non-secure	R/W
14:13	—	这些位被读取为1。写入值应为1。	R/W
15	PSARB15	ETHER0EDMAC0、MSTPCRB.MSTPB15位和PFENET.PHYMODE0位安全属性该位读为1（非安全）。	R
16	PSARB16	OSPI和MSTPCRB.MSTPB16位安全属性 该位读为1（非安全）。	R
17	—	该位读取为1。写入值应为1。	R/W
18	PSARB18	SPI1和MSTPCRB.MSTPB18位安全归属 0: Secure 1: Non-secure	R/W
19	PSARB19	SPI0和MSTPCRB.MSTPB19位安全归属 0: Secure 1: Non-secure	R/W
21:20	—	这些位被读取为1。写入值应为1。	R/W
22	PSARB22	SCI9和MSTPCRB.MSTPB22位安全归属 0: Secure 1: Non-secure	R/W
23	PSARB23	SCI8和MSTPCRB.MSTPB23位安全归属 0: Secure 1: Non-secure	R/W
24	PSARB24	SCI7和MSTPCRB.MSTPB24位安全归属 0: Secure 1: Non-secure	R/W
25	PSARB25	SCI6和MSTPCRB.MSTPB25位安全归属 0: Secure 1: Non-secure	R/W
26	PSARB26	SCI5和MSTPCRB.MSTPB26位安全归属 0: Secure 1: Non-secure	R/W
27	PSARB27	SCI4和MSTPCRB.MSTPB27位安全归属 0: Secure 1: Non-secure	R/W
28	PSARB28	SCI3和MSTPCRB.MSTPB28位安全归属 0: Secure 1: Non-secure	R/W
29	PSARB29	SCI2和MSTPCRB.MSTPB29位安全归属 0: Secure 1: Non-secure	R/W
30	PSARB30	SCI1和MSTPCRB.MSTPB30位安全归属 0: Secure 1: Non-secure	R/W

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Bit	Symbol	Function	R/W
31	PSARB31	SCI0 and the MSTPCRB.MSTPB31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: A bit undefined in this table is reserved bit. The reserved bit should be kept the initial value.
Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARB specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

52.6.2 PSARC : Peripheral Security Attribution Register C

Base address: PSCU = 0x400E_0000

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARC31	—	—	—	PSARC27	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PSARC13	PSARC12	—	—	—	PSARC8	—	—	—	—	PSARC3	—	PSARC1	PSARC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARC0	CAC and the MSTPCRC.MSTPC0 bit security attribution 0: Secure 1: Non-secure	R/W
1	PSARC1	CRC and the MSTPCRC.MSTPC1 bit security attribution 0: Secure 1: Non-secure	R/W
2	—	This bit is read as 1. The write value should be 1.	R/W
3	PSARC3	CTSU and the MSTPCRC.MSTPC3 bit security attribution 0: Secure 1: Non-secure	R/W
7:4	—	These bits are read as 1. The write value should be 1.	R/W
8	PSARC8	SSIE0 and the MSTPCRC.MSTPC8 bit security attribution 0: Secure 1: Non-secure	R/W
11:9	—	These bits are read as 1. The write value should be 1.	R/W
12	PSARC12	SDHI0 and the MSTPCRC.MSTPC12 bit security attribution 0: Secure 1: Non-secure	R/W
13	PSARC13	DOC and the MSTPCRC.MSTPC13 bit security attribution 0: Secure 1: Non-secure	R/W
19:14	—	These bits are read as 1. The write value should be 1.	R/W
20	—	This bit is read as 1. The write value should be 1.	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
26:22	—	These bits are read as 1. The write value should be 1.	R/W
27	PSARC27	CANFD0 and the MSTPCRC.MSTPC27 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
31	PSARB31	SCI0和MSTPCRB.MSTPB31位安全归属 0: Secure 1: Non-secure	R/W

Note: 该表中未定义的位是保留位。保留位应保持初始值。
Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARB指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

52.6.2 PSARC:外设安全属性寄存器C

Base address: PSCU = 0x400E_0000

Offset address: 0x08

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARC31	—	—	—	PSARC27	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	PSARC13	PSARC12	—	—	—	PSARC8	—	—	—	—	PSARC3	—	PSARC1	PSARC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARC0	CAC和MSTPCRC.MSTPC0位安全属性 0: Secure 1: Non-secure	R/W
1	PSARC1	CRC和MSTPCRC.MSTPC1位安全属性 0: Secure 1: Non-secure	R/W
2	—	该位读取为1。写入值应为1。	R/W
3	PSARC3	CTSU和MSTPCRC.MSTPC3位安全属性 0: Secure 1: Non-secure	R/W
7:4	—	这些位被读取为1。写入值应为1。	R/W
8	PSARC8	SSIE0和MSTPCRC.MSTPC8位安全属性 0: Secure 1: Non-secure	R/W
11:9	—	这些位被读取为1。写入值应为1。	R/W
12	PSARC12	SDHI0和MSTPCRC.MSTPC12位安全属性 0: Secure 1: Non-secure	R/W
13	PSARC13	DOC和MSTPCRC.MSTPC13位安全属性 0: Secure 1: Non-secure	R/W
19:14	—	这些位被读取为1。写入值应为1。	R/W
20	—	该位读取为1。写入值应为1。	R/W
21	—	该位读取为1。写入值应为1。	R/W
26:22	—	这些位被读取为1。写入值应为1。	R/W
27	PSARC27	CANFD0和MSTPCRC.MSTPC27位安全属性 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
30:28	—	These bits are read as 1. The write value should be 1.	R/W
31	PSARC31	SCE9 and the MSTPCRC.MSTPC31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARC specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

52.6.3 PSARD : Peripheral Security Attribution Register D

Base address: PSCU = 0x400E_0000
Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	PSARD22	—	PSARD20	—	—	—	PSARD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSARD15	PSARD14	PSARD13	PSARD12	PSARD11	—	—	—	—	—	—	—	PSARD3	PSARD2	PSARD1	PSARD0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARD0	AGT3 and the MSTPCRD.MSTPD0 bit security attribution 0: Secure 1: Non-secure	R/W
1	PSARD1	AGT2 and the MSTPCRD.MSTPD1 bit security attribution 0: Secure 1: Non-secure	R/W
2	PSARD2	AGT1 and the MSTPCRD.MSTPD2 bit security attribution 0: Secure 1: Non-secure	R/W
3	PSARD3	AGT0 and the MSTPCRD.MSTPD3 bit security attribution 0: Secure 1: Non-secure	R/W
10:4	—	These bits are read as 1. The write value should be 1.	R/W
11	PSARD11	POEG Group D and the MSTPCRD.MSTPD11 bit security attribution 0: Secure 1: Non-secure	R/W
12	PSARD12	POEG Group C and the MSTPCRD.MSTPD12 bit security attribution 0: Secure 1: Non-secure	R/W
13	PSARD13	POEG Group B and the MSTPCRD.MSTPD13 bit security attribution 0: Secure 1: Non-secure	R/W
14	PSARD14	POEG Group A and the MSTPCRD.MSTPD14 bit security attribution 0: Secure 1: Non-secure	R/W
15	PSARD15	ADC121 and the MSTPCRD.MSTPD15 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
30:28	—	这些位被读取为1。写入值应为1。	R/W
31	PSARC31	SCE9和MSTPCRC.MSTPC31位安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARC指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

52.6.3 PSARD:外围安全属性寄存器D

Base address: PSCU = 0x400E_0000
Offset address: 0x0C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	PSARD22	—	PSARD20	—	—	—	PSARD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSARD15	PSARD14	PSARD13	PSARD12	PSARD11	—	—	—	—	—	—	—	PSARD3	PSARD2	PSARD1	PSARD0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARD0	AGT3和MSTPCRD.MSTPD0位安全归属 0: Secure 1: Non-secure	R/W
1	PSARD1	AGT2和MSTPCRD.MSTPD1位安全归属 0: Secure 1: Non-secure	R/W
2	PSARD2	AGT1和MSTPCRD.MSTPD2位安全归属 0: Secure 1: Non-secure	R/W
3	PSARD3	AGT0和MSTPCRD.MSTPD3位安全属性 0: Secure 1: Non-secure	R/W
10:4	—	这些位被读取为1。写入值应为1。	R/W
11	PSARD11	POEGGroupD和MSTPCRD.MSTPD11位安全归属 0: Secure 1: Non-secure	R/W
12	PSARD12	POEGGroupC和MSTPCRD.MSTPD12位安全归属 0: Secure 1: Non-secure	R/W
13	PSARD13	POEGGroupB和MSTPCRD.MSTPD13位安全归属 0: Secure 1: Non-secure	R/W
14	PSARD14	POEGGroupA和MSTPCRD.MSTPD14位安全归属 0: Secure 1: Non-secure	R/W
15	PSARD15	ADC121和MSTPRD.MSTPD15位安全归属 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
16	PSARD16	ADC120 and the MSTPCRD.MSTPD16 bit security attribution 0: Secure 1: Non-secure	R/W
19:17	—	These bits are read as 1. The write value should be 1.	R/W
20	PSARD20	DAC12 and the MSTPCRD.MSTPD20 bit security attribution 0: Secure 1: Non-secure	R/W
21	—	This bit is read as 1. The write value should be 1.	R/W
22	PSARD22	TSN and the MSTPCRD.MSTPD22 bit security attribution 0: Secure 1: Non-secure	R/W
31:23	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARD specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

52.6.4 PSARE : Peripheral Security Attribution Register E

Base address: PSCU = 0x400E_0000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARE31	PSARE30	PSARE29	PSARE28	PSARE27	PSARE26	PSARE25	PSARE24	PSARE23	PSARE22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSARE15	PSARE14	—	—	—	—	—	—	—	—	—	—	—	PSARE2	PSARE1	PSARE0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARE0	WDT security attribution 0: Secure 1: Non-secure	R/W
1	PSARE1	IWDT security attribution 0: Secure 1: Non-secure	R/W
2	PSARE2	RTC security attribution 0: Secure 1: Non-secure	R/W
13:3	—	These bits are read as 1. The write value should be 1.	R/W
14	PSARE14	AGT5 and the MSTPCRE.MSTPE14 bit security attribution 0: Secure 1: Non-secure	R/W
15	PSARE15	AGT4 and the MSTPCRE.MSTPE15 bit security attribution 0: Secure 1: Non-secure	R/W
21:16	—	These bits are read as 1. The write value should be 1.	R/W
22	PSARE22	GPT9 and the MSTPCRE.MSTPE22 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
16	PSARD16	ADC120和MSTPRD.MSTPD16位安全属性 0: Secure 1: Non-secure	R/W
19:17	—	这些位被读取为1。写入值应为1。	R/W
20	PSARD20	DAC12和MSTPCRD.MSTPD20位安全归属 0: Secure 1: Non-secure	R/W
21	—	该位读取为1。写入值应为1。	R/W
22	PSARD22	TSN和MSTPCRD.MSTPD22位安全属性 0: Secure 1: Non-secure	R/W
31:23	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARD指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

52.6.4 PSARE:外设安全属性寄存器E

Base address: PSCU = 0x400E_0000

Offset address: 0x10

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	PSARE31	PSARE30	PSARE29	PSARE28	PSARE27	PSARE26	PSARE25	PSARE24	PSARE23	PSARE22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	PSARE15	PSARE14	—	—	—	—	—	—	—	—	—	—	—	PSARE2	PSARE1	PSARE0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	PSARE0	WDT安全归属 0: Secure 1: Non-secure	R/W
1	PSARE1	IWDT安全归属 0: Secure 1: Non-secure	R/W
2	PSARE2	RTC安全归属 0: Secure 1: Non-secure	R/W
13:3	—	这些位被读取为1。写入值应为1。	R/W
14	PSARE14	AGT5和MSTPCRE.MSTPE14位安全属性 0: Secure 1: Non-secure	R/W
15	PSARE15	AGT4和MSTPCRE.MSTPE15位安全属性 0: Secure 1: Non-secure	R/W
21:16	—	这些位被读取为1。写入值应为1。	R/W
22	PSARE22	GPT9和MSTPCRE.MSTPE22位安全属性 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
23	PSARE23	GPT8 and the MSTPCRE.MSTPE23 bit security attribution 0: Secure 1: Non-secure	R/W
24	PSARE24	GPT7 and the MSTPCRE.MSTPE24 bit security attribution 0: Secure 1: Non-secure	R/W
25	PSARE25	GPT6 and the MSTPCRE.MSTPE25 bit security attribution 0: Secure 1: Non-secure	R/W
26	PSARE26	GPT5 and the MSTPCRE.MSTPE26 bit security attribution 0: Secure 1: Non-secure	R/W
27	PSARE27	GPT4 and the MSTPCRE.MSTPE27 bit security attribution 0: Secure 1: Non-secure	R/W
28	PSARE28	GPT3 and the MSTPCRE.MSTPE28 bit security attribution 0: Secure 1: Non-secure	R/W
29	PSARE29	GPT2 and the MSTPCRE.MSTPE29 bit security attribution 0: Secure 1: Non-secure	R/W
30	PSARE30	GPT1 and the MSTPCRE.MSTPE30 bit security attribution 0: Secure 1: Non-secure	R/W
31	PSARE31	GPT0, GPT_OPS and the MSTPCRE.MSTPE31 bit security attribution 0: Secure 1: Non-secure	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The PSARE specifies the security attribution for each module and the corresponding bit in Module Stop Control Register.

52.6.5 MSSAR : Module Stop Security Attribution Register

Base address: PSCU = 0x400E_0000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MSSAR3	MSSAR2	MSSAR1	MSSAR0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSSAR0	The MSTPCRC.MSTPC14 bit security attribution 0: Secure 1: Non-secure	R/W
1	MSSAR1	The MSTPCRA.MSTPA22 bit security attribution 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
23	PSARE23	GPT8和MSTPCRE.MSTPE23位安全属性 0: Secure 1: Non-secure	R/W
24	PSARE24	GPT7和MSTPCRE.MSTPE24位安全属性 0: Secure 1: Non-secure	R/W
25	PSARE25	GPT6和MSTPCRE.MSTPE25位安全属性 0: Secure 1: Non-secure	R/W
26	PSARE26	GPT5和MSTPCRE.MSTPE26位安全属性 0: Secure 1: Non-secure	R/W
27	PSARE27	GPT4和MSTPCRE.MSTPE27位安全属性 0: Secure 1: Non-secure	R/W
28	PSARE28	GPT3和MSTPCRE.MSTPE28位安全属性 0: Secure 1: Non-secure	R/W
29	PSARE29	GPT2和MSTPCRE.MSTPE29位安全属性 0: Secure 1: Non-secure	R/W
30	PSARE30	GPT1和MSTPCRE.MSTPE30位安全属性 0: Secure 1: Non-secure	R/W
31	PSARE31	GPT0、GPT_OPS和MSTPCRE.MSTPE31位安全属性 0: Secure 1: Non-secure	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

PSARE指定每个模块的安全属性以及模块停止控制寄存器中的相应位。

52.6.5 MSSAR：模块停止安全属性寄存器

Base address: PSCU = 0x400E_0000

Offset address: 0x14

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	MSSAR3	MSSAR2	MSSAR1	MSSAR0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
0	MSSAR0	MSTPCRC.MSTPC14位安全属性 0: Secure 1: Non-secure	R/W
1	MSSAR1	MSTPCRA.MSTPA22位安全属性 0: Secure 1: Non-secure	R/W

Bit	Symbol	Function	R/W
2	MSSAR2	The MSTPCRA.MSTPA7 bit security attribution 0: Secure 1: Non-secure	R/W
3	MSSAR3	The MSTPCRA.MSTPA0 bit security attribution 0: Secure 1: Non-secure	R/W
31:4	—	These bits are read as 1. The write value should be 1.	R/W

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.
Note: This register is write-protected by PRCR register.

The MSSAR specifies the security attribution for the corresponding bit in Module Stop Control Register.

52.6.6 CFSAMONA : Code Flash Security Attribution Monitor Register A

Base address: PSCU = 0x400E_0000
Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CFS2[8:0]									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	The value set by user									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	These bits are read as 0.	R
23:15	CFS2[8:0]	Code Flash Secure area 2 Indicate the total area of secure region and non-secure callable region for code flash.	R
31:24	—	These bits are read as 0.	R

Note: The CFSAMONA does not have security attribution.

52.6.7 CFSAMONB : Code Flash Security Attribution Monitor Register B

Base address: PSCU = 0x400E_0000
Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CFS1[13:0]														—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	The value set by user														0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0.	R
23:10	CFS1[13:0]	Code Flash Secure area 1 Indicate the area of secure region for code flash.	R
31:24	—	These bits are read as 0.	R

Note: The CFSAMONB does not have security attribution.

Bit	Symbol	Function	R/W
2	MSSAR2	MSTPCRA.MSTPA7位安全属性 0: Secure 1: Non-secure	R/W
3	MSSAR3	MSTPCRA.MSTPA0位安全属性 0: Secure 1: Non-secure	R/W
31:4	—	这些位被读取为1。写入值应为1。	R/W

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。
Note: 该寄存器由PRCR寄存器写保护。

MSSAR指定模块停止控制寄存器中相应位的安全属性。

52.6.6 CFSAMONA：代码闪存安全属性监控寄存器A

Base address: PSCU = 0x400E_0000
Offset address: 0x18

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CFS2[8:0]									—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
14:0	—	这些位读为0。	R
23:15	CFS2[8:0]	CodeFlash安全区2 指示代码闪存的安全区域和非安全可调用区域的总面积。	R
31:24	—	这些位读为0。	R

Note: CFSAMONA没有安全属性。

52.6.7 CFSAMONB:代码闪存安全属性监控寄存器B

Base address: PSCU = 0x400E_0000
Offset address: 0x1C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	CFS1[13:0]														—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	用户设置的值														0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	这些位读为0。	R
23:10	CFS1[13:0]	CodeFlash安全区1 指示代码闪存的安全区域区域。	R
31:24	—	这些位读为0。	R

Note: CFSAMONB没有安全属性。

52.6.8 DFSAMON : Data Flash Security Attribution Monitor Register

Base address: PSCU = 0x400E_0000

Offset address: 0x20

Bit position:	31															15									10									0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFS[5:0]									—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	The value set by user									0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0.	R
15:10	DFS[5:0]	Data flash Secure area Indicate the area of Secure region for data flash.	R
31:16	—	These bits are read as 0.	R

Note: The DFSAMON does not have security attribution.

52.6.9 SSAMONA : SRAM Security Attribution Monitor Register A

Base address: PSCU = 0x400E_0000

Offset address: 0x24

Bit position:	31											20												13											0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SS2[7:0]												—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	The value set by user												0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
12:0	—	These bits are read as 0.	R
20:13	SS2[7:0]	SRAM Secure area 2 Indicate the total area of Secure region and non-secure callable region for SRAM.	R
31:21	—	These bits are read as 0.	R

Note: The SSAMONA does not have security attribution.

52.6.10 SSAMONB : SRAM Security Attribution Monitor Register B

Base address: PSCU = 0x400E_0000

Offset address: 0x28

Bit position:	31											20										10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SS1[10:0]										—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	The value set by user										0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	These bits are read as 0.	R
20:10	SS1[10:0]	SRAM secure area 1 Indicate the area of secure region for SRAM.	R
31:21	—	These bits are read as 0.	R

Note: The SSAMONB does not have security attribution.

52.6.8 DFSAMON:数据闪存安全属性监控寄存器

Base address: PSCU = 0x400E_0000

Offset address: 0x20

Bit position:	31															15									10									0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFS[5:0]									—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	用户设置的值									0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	这些位读为0。	R
15:10	DFS[5:0]	数据闪存安全区 指示数据闪存的安全区域区域。	R
31:16	—	这些位读为0。	R

Note: DFSAMON没有安全属性。

52.6.9 SSAMONA:SRAM安全属性监控寄存器A

Base address: PSCU = 0x400E_0000

Offset address: 0x24

Bit position:	31											20												13											0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SS2[7:0]												—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	用户设置的值												0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
12:0	—	这些位读为0。	R
20:13	SS2[7:0]	SRAM安全区域2 指示SRAM的安全区域和非安全可调用区域的总面积。	R
31:21	—	这些位读为0。	R

Note: SSAMONA没有安全属性。

52.6.10 SSAMONB:SRAM安全属性监控寄存器B

Base address: PSCU = 0x400E_0000

Offset address: 0x28

Bit position:	31											20										10										0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	SS1[10:0]										—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	用户设置的值										0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
9:0	—	这些位读为0。	R
20:10	SS1[10:0]	SRAM安全区1 指示SRAM的安全区域区域。	R
31:21	—	这些位读为0。	R

Note: SSAMONB没有安全属性。

52.6.11 DLMMON : Device Lifecycle Management State Monitor Register

Base address: PSCU = 0x400E_0000

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	DLMMON[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	DLM status value			

Bit	Symbol	Function	R/W
3:0	DLMMON[3:0]	Device Lifecycle Management State Monitor 0x1: CM 0x2: SSD 0x3: NSECSD 0x4: DPL 0x5: LCK_DBG 0x6: LCK_BOOT 0x7: RMA_REQ 0x8: RMA_ACK Others: Reserved	R
31:4	—	These bits are read as 0. The write value should be 0.	R

Note: The DLMMON does not have security attribution.

52.6.12 TZFSAR : TrustZone Filter Security Attribution Register

Base address: CPSCU = 0x4000_8000

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZFSA0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	TZFSA0	Security attributes of registers for TrustZone Filter 0: Secure 1: Non-secure	R/W
31:1	—	These bits are read as 1.	R

Note: Only secure access can write to this register. Both secure access and Non-secure read access are allowed but Non-secure write access is not allowed and TrustZone access error is not generated.

Note: This register is write-protected by PRCR register.

TZFSA0 bit (Security attributes of registers for TrustZone Filter)

Security attributes of register for TZFOAD and TZFPT registers.

52.6.11 DLMMON:设备生命周期管理状态监视器寄存器

Base address: PSCU = 0x400E_0000

Offset address: 0x2C

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	DLMMON[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	DLM状态值			

Bit	Symbol	Function	R/W
3:0	DLMMON[3:0]	设备生命周期管理状态监视器 0x1: CM 0x2: SSD 0x3: NSECSD 0x4: DPL 0x5: LCK_DBG 0x6: LCK_BOOT 0x7: RMA_REQ 0x8: RMA_ACK Others: Reserved	R
31:4	—	这些位被读取为0。写入值应为0。	R

Note: DLMMON没有安全属性。

52.6.12 TZFSAR:TrustZone过滤器安全属性寄存器

Base address: CPSCU = 0x4000_8000

Offset address: 0x180

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZFSA0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit	Symbol	Function	R/W
0	TZFSA0	TrustZone过滤器寄存器的安全属性 0: Secure 1: Non-secure	R/W
31:1	—	这些位读为1。	R

Note: 只有安全访问才能写入该寄存器。允许安全访问和非安全读取访问，但不允许非安全写入访问，并且不会生成TrustZone访问错误。

Note: 该寄存器由PRCR寄存器写保护。

TZFSA0位（TrustZone过滤器寄存器的安全属性）

TZFOAD和TZFPT寄存器的寄存器安全属性。

52.6.13 TZFOAD : TrustZone Filter Operation After Detection Register

Base address: TZF = 0x4000_0E00

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	Operation after detection 0: Non-maskable interrupt 1: Reset	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	KeyCode This bit is used to enable or disable writing of the OAD bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:
- Secure and Non-secure access are allowed.

OAD bit (Operation after detection)

The OAD bit is specified to generate either reset or non-maskable interrupt when the access to the protect region is detected by the TrustZone Filter.

When the OAD bit is set, write 0xA5 in the KEY[7:0] bits at the same time.

KEY[7:0] bits (KeyCode)

The KEY[7:0] bits are used to enable or disable writing of the OAD bit. When writing the OAD bit, write 0xA5 in the KEY[7:0] bits at the same time.

When the KEY[7:0] bits value except 0xA5 is written in, the OAD bit is not updated.

The KEY[7:0] bits are read always as 0x00.

52.6.14 TZFPT : TrustZone Filter Protect Register

Base address: TZF = 0x4000_0E00

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	Protection of register 0: All Bus TrustZone Filter register writing is protected. Read is possible. 1: All Bus TrustZone Filter register writing is possible.	R/W
7:1	—	These bits are read as 0. The write value should be 0.	R/W
15:8	KEY[7:0]	KeyCode This bit is used to enable or disable writing of the PROTECT bit.	W

Note: If the security attribution is configured as secure:
- Secure access and Non-secure read access are allowed
- Non-secure write access is ignored, and TrustZone access error is not generated.

If the security attribution is configured as Non-secure:

52.6.13 TZFOAD：检测寄存器后的TrustZone过滤器操作

Base address: TZF = 0x4000_0E00

Offset address: 0x00

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	OAD	检测后操作 0：不可屏蔽中断1：复位	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	KeyCode 该位用于启用或禁用OAD位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：●
允许安全和非安全访问。

OAD位（检测后的操作）

当TrustZone过滤器检测到对保护区域的访问时，OAD位被指定为产生复位或不可屏蔽中断。

当OAD位置位时，同时向KEY[7:0]位写入0xA5。

KEY[7:0] bits (KeyCode)

KEY[7:0]位用于启用或禁用OAD位的写入。写入OAD位时，将0xA5写入KEY[7:0]位。

当KEY[7:0]位值除0xA5被写入时，OAD位不会更新。

KEY[7:0]位总是被读取为0x00。

52.6.14 TZFPT:TrustZone过滤器保护寄存器

Base address: TZF = 0x4000_0E00

Offset address: 0x04

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	KEY[7:0]								—	—	—	—	—	—	—	保护
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
0	PROTECT	注册保护 0：所有总线TrustZone过滤器寄存器写入受到保护。读取是可能的。1：所有总线TrustZone过滤器寄存器写入都是可能的。	R/W
7:1	—	这些位被读取为0。写入值应为0。	R/W
15:8	KEY[7:0]	KeyCode 该位用于启用或禁用PROTECT位的写入。	W

Note: 如果安全属性配置为安全：●
允许安全访问和非安全读取访问
- 忽略非安全写入访问，不会生成TrustZone访问错误。

如果安全属性配置为非安全：

- Secure and Non-secure access are allowed.

PROTECT bit (Protection of register)

The PROTECT bit controls enable or disable writing to the corresponding registers to be protected. TZFOAD register is protected by PROTECT.

When the PROTECT bit is set, write 0xA5 in the KEY[7:0] bits at the same time.

KEY[7:0] bits (KeyCode)

The KEY[7:0] bits are used to enable or disable writing of the PROTECT bit. When writing the PROTECT bit, write 0xA5 in the KEY[7:0] bits at the same time.

When the KEY[7:0] bits value except 0xA5 is written in, the PROTECT bit is not updated.

The KEY[7:0] bits are read always as 0x00.

52.7 Usage Notes

52.7.1 Restrictions on setting the security attribution

To set the software breakpoint, the debugger need to re-program the flash. Table 52.10 shows the registers that the debugger sets to re-program the flash. If the security attribution of the register listed in Table 52.10 is configured as secure, the debugger can not set the software breakpoint in NSECSD state because the debugger can not change the register setting. Secure developper need to configure the registers listed in Table 52.10 as non-secure only in NSECSD state.

Table 52.10 The registers that the debugger sets to re-program the flash

Function name	Register name
Clock Generation Circuit	SCKDIVCR, SCKCR, PLLCCR, PLLCR, HOCOCR, MOCOCR
Low-Power modes	OPCCR, SOPCCR

52.7.2 SAU setting

After reset, all of address space is marked as Secure by SAU default setting. SAU_CTRL register should be set to 0x2 to enable the IDAU security attribution. That is, after setting SAU_CTRL register to 0x2, the address space security attribution becomes as shown in Table 52.6.

52.7.3 Non-secure exception during the setting of FACI registers

As shown in Table 52.5, the registers related to FACI are protected from non-secure access only during programming/erasure or during suspend programming/erasure. Outside of this state, the access from non-secure region is not protected. For example, when programming by the secure user, the non-secure user can rewrite the FSADDR if a non-secure exception occurs immediately after “Set the start address of the target block to the FSADDR register” flow in Figure 50.14. If the FACI command is issued after the non-secure exception processing is completed and the CPU state returns to the secure state, data will be programmed to an address not intended by the secure user.

To prevent such a things, secure user needs to set not to accept the non-secure exception during the following period.

- Set not to accept the non-secure exeption before setting FWEPROR to 01h or setting FENTRYR to other than 0000h, that is before lereasing the protection of FWEPROR or FENTRYR.
- Set to accept the non-secure exception after all write access to the FACI command-issuing area is completed.

52.7.4 FCU interrupt usage

It is recommended that secure users do not use the FCU interrupts, but rather use the register polling. Because non-secure users can program/erase the data flash without calling the secure gateway, if secure user uses FCU interrupts, the unintentional exception handliing may be exeuted when data flash is programmed/erased by a non-secure user.

- 允许安全和非安全访问。

PROTECT位（寄存器保护）

PROTECT位控制启用或禁用对受保护的相应寄存器的写入。TZFOAD寄存器受PROTECT保护。

当PROTECT位置位时，同时向KEY[7:0]位写入0xA5。

KEY[7:0] bits (KeyCode)

KEY[7:0]位用于启用或禁用PROTECT位的写入。写入PROTECT位时，同时向KEY[7:0]位写入0xA5。

写入除0xA5以外的KEY[7:0]位值时，PROTECT位不更新。

KEY[7:0]位总是被读取为0x00。

52.7 使用说明

52.7.1 设置安全属性的限制

要设置软件断点，调试器需要重新编程闪存。表52.10显示了调试器为重新编程闪存而设置的寄存器。如果表52.10中列出的寄存器的安全属性配置为安全，则调试器无法在NSECSD状态下设置软件断点，因为调试器无法更改寄存器设置。仅在NSECSD状态下，安全开发人员需要将表52.10中列出的寄存器配置为非安全。

Table 52.10 调试器设置的用于重新编程闪存的寄存器

函数名称	注册名称
时钟产生电路	SCKDIVCR, SCKCR, PLLCCR, PLLCR, HOCOCR, MOCOCR
Low-Power modes	OPCCR, SOPCCR

52.7.2 SAU设置

复位后，SAU默认设置将所有地址空间标记为安全。SAU_CTRL寄存器应设置为0x2以启用IDAU安全属性。即设置SAU_CTRL寄存器为0x2后，地址空间安全属性变为如表52.6所示。

52.7.3 FACI寄存器设置期间的非安全异常

如表52.5所示，与FACI相关的寄存器仅在编程擦除或挂起编程擦除期间受到保护，不会受到非安全访问。在此状态之外，来自非安全区域的访问不受保护。例如，当由安全用户编程时，如果在图50.14中的“将目标块的起始地址设置为FSADDR寄存器”流程之后立即发生非安全异常，则非安全用户可以重写FSADDR。如果在非安全异常处理完成后发出FACI命令并且CPU状态返回到安全状态，则数据将被编程到安全用户不打算使用的地址。

为了防止这样的事情发生，安全用户需要在接下来的时间段内设置不接受非安全异常。

- 在将FWEPROR设置为01h或将FENTRYR设置为0000h以外的值之前，即在解除对FWEPROR或FENTRYR的保护之前，设置不接受非安全例外。
- 设置为在对FACI命令发布区域的所有写访问完成后接受非安全异常。

52.7.4 FCU中断使用

建议安全用户不要使用FCU中断，而是使用寄存器轮询。由于非安全用户可以在不调用安全网关的情况下对数据闪存进行编程擦除，因此如果安全用户使用FCU中断，则在数据闪存被非安全用户编程擦除时可能会执行意外异常处理。

53. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = AVSS_USBHS = PVSS_USBHS = 0 V
- $T_a = T_{opr}$

Figure 53.1 shows the timing conditions.

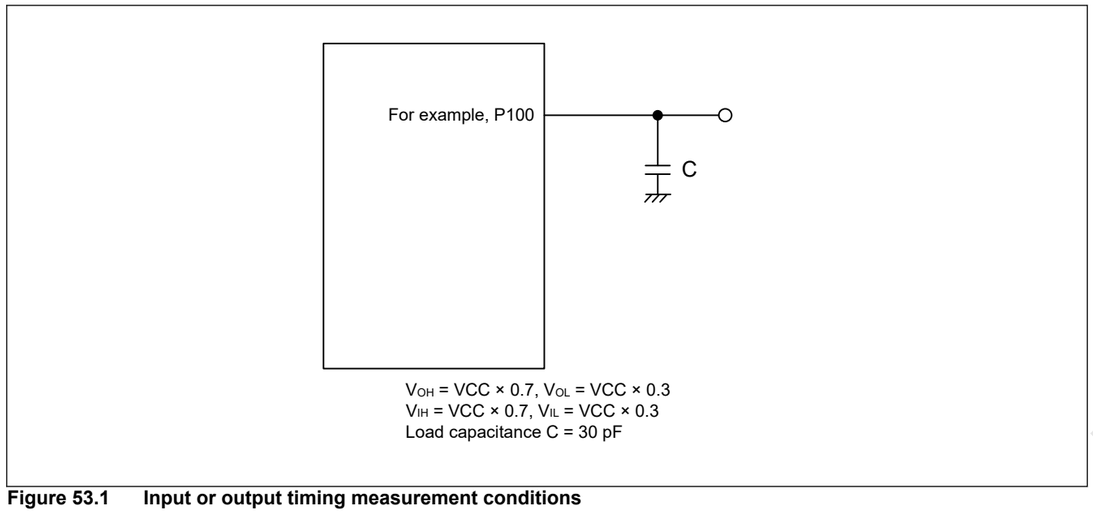

Figure 53.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

53.1 Absolute Maximum Ratings

Table 53.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB*2	–0.3 to +4.0	V
VBATT power supply voltage	VBATT	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
USBHS power supply voltage	VCC_USBHS	–0.3 to +4.0	V
USBHS analog power supply voltage	AVCC_USBHS	–0.3 to +4.0	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, and P708 to P713 are 5 V tolerant.

53. 电气特性

支持的外围功能和引脚因产品名称而异。

除非另有规定，MCU的电气特性在以下条件下定义：

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = AVSS_USBHS = PVSS_USBHS = 0 V
- $T_a = T_{opr}$

图53.1显示了时序条件。

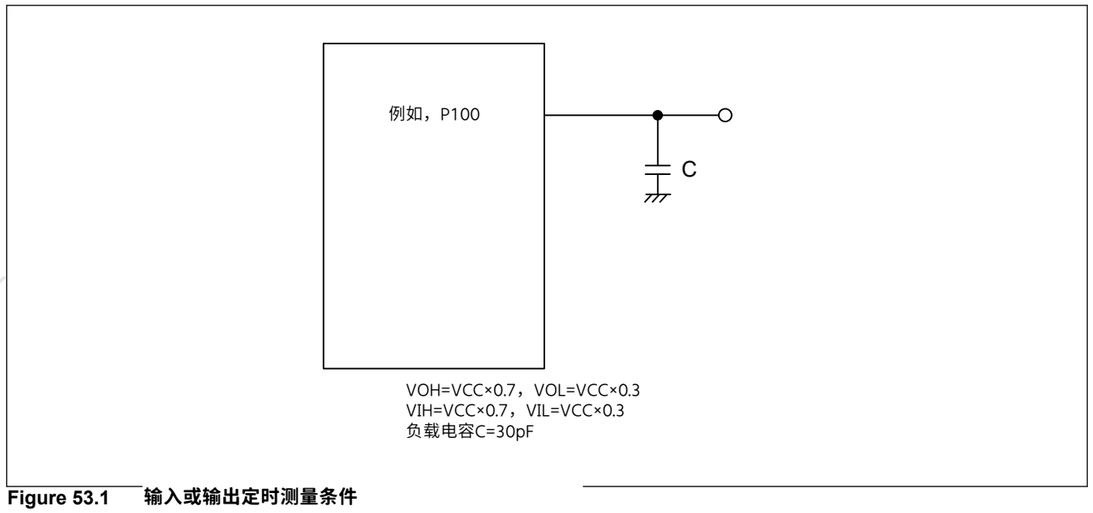

Figure 53.1 输入或输出定时测量条件

所提供的每个外设时序规范的推荐测量条件是为了实现最佳外设操作。确保调整每个引脚的驱动能力以满足您的条件。

53.1 绝对最大额定值

Table 53.1 绝对最大额定值

Parameter	Symbol	Value	Unit
电源电压	VCC, VCC_USB*2	–0.3 to +4.0	V
VBATT电源电压	VBATT	–0.3 to +4.0	V
输入电压（5V容限端口*1除外）	V_{in}	–0.3 to VCC + 0.3	V
输入电压（5V耐压端口*1）	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
参考电源电压	VREFH/VREFH0	–0.3 to VCC + 0.3	V
USBHS电源电压	VCC_USBHS	–0.3 to +4.0	V
USBHS模拟电源电压	AVCC_USBHS	–0.3 to +4.0	V
模拟电源电压	AVCC0*2	–0.3 to +4.0	V
模拟输入电压	V_{AN}	–0.3 to AVCC0 + 0.3	V
工作温度*3*4	T_{opr}	–40 to +105	°C
贮存温度	T_{stg}	–55 to +125	°C

注1.端口P205、P206、P400、P401、P407至P415、P511、P512和P708至P713可承受5V。

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Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 53.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 53.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/USBHS is not used	2.7	—	3.6	V
		When USB/USBHS is used	3.0	—	3.6	V
	VSS		—	0	—	V
USB power supply voltages	VCC_USB, VCC_USBHS		—	VCC	—	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		—	0	—	V
VBATT power supply voltage	VBATT		1.65	—	3.6	V
Analog power supply voltages	AVCC0*1		—	VCC	—	V
	AVSS0		—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter and the D/A converter are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.
Note 2. Low CL crystal cannot be used below VBATT = 1.8V.

53.2 DC Characteristics

53.2.1 Tj/Ta Definition

Table 53.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.
Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3. Part Numbering. If the part number shows the operation temperature to 85°C, then Tj max is 105°C, otherwise, 125°C.

注2.将AVCC0和VCC_USB连接到VCC。
注3：见第53.2.1节。TjTa定义。
注4.有关在Ta=+85°C至+105°C时降额运行的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Table 53.2 推荐工作条件

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC	不使用USBUSBHS时	2.7	—	3.6	V
		使用USBUSBHS时	3.0	—	3.6	V
	VSS		—	0	—	V
USB电源电压	VCC_USB, VCC_USBHS		—	VCC	—	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		—	0	—	V
VBATT电源电压	VBATT		1.65	—	3.6	V
模拟电源电压	AVCC0*1		—	VCC	—	V
	AVSS0		—	0	—	V

注1.将AVCC0连接到VCC。不使用AD转换器和DA转换器时，不要离开AVCC0、VREFHVREFH0、AVSS0和VREFLVREFL0引脚打开。将AVCC0和VREFHVREFH0引脚连接到VCC，以及AVSS0和VREFLVREFL0引脚分别连接到VSS。
注2.低于VBATT=1.8V时不能使用低CL晶振。

53.2 DC Characteristics

53.2.1 Tj/Ta Definition

Table 53.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+$I_{CC}max \times VCC$.
注1.工作温度上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节。零件编号。如果部件号显示工作温度为85°C，则Tjmax为105°C，否则为125°C。

53.2.2 I/O V_{IH}, V_{IL}

Table 53.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), WAIT, SPI (except RSPCK), OSPI (except ECS)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		D00 to D15	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
		ETHERC	V_{IH}	2.3	—	—	
			V_{IL}	—	—	VCC × 0.2	
		IIC (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

53.2.2 IOVIH

Table 53.4 IOVIH VIL(1of2)

Parameter			符号最小值		Typ	Max	Unit
输入电压（施密特触发器输入引脚除外）	外设功能引脚	EXTAL（外部时钟输入）、WAIT、SPI（除RSPCK), OSPI (except ECS)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		D00 to D15	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
		ETHERC	V_{IH}	2.3	—	—	
			V_{IL}	—	—	VCC × 0.2	
		IIC (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

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Table 53.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter					Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)			V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
					V_{IL}	—	—	VCC × 0.3	
					ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*1 *5			V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	—	V_{BATT} + 0.3	
					V_{IL}	—	—	V_{BATT} × 0.2	
					ΔV_T	V_{BATT} × 0.05	—	—	
				When VCC power supply is selected	V_{IH}	VCC × 0.8	—	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	—	VCC + 0.3	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
		Other input pins*2			V_{IH}	VCC × 0.8	—	—	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*3 *5			V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
					V_{IL}	—	—	VCC × 0.2	
		Other input pins*4			V_{IH}	VCC × 0.8	—	—	
					V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 22 pins).
Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 21 pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

Table 53.4 IOVIH VIL(2of2)

Parameter					符号	最小值	Typ	Max	Unit
施密特触发器输入电压	外设功能引脚	IIC (except for SMBus)			V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
					V_{IL}	—	—	VCC × 0.3	
					ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*1 *5			V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
		RTCIC0, RTCIC1, RTCIC2	使用备用电池时 Function	选择VBATT电源时	V_{IH}	V_{BATT} × 0.8	—	V_{BATT} + 0.3	
					V_{IL}	—	—	V_{BATT} × 0.2	
					ΔV_T	V_{BATT} × 0.05	—	—	
				选择VCC电源时	V_{IH}	VCC × 0.8	—	更高的电压 VCC+0.3V或 VBATT+0.3 V	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
			不使用备用电池时 Function		V_{IH}	VCC × 0.8	—	VCC + 0.3	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
		其他输入引脚*2			V_{IH}	VCC × 0.8	—	—	
					V_{IL}	—	—	VCC × 0.2	
					ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*3 *5			V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
					V_{IL}	—	—	VCC × 0.2	
		其他输入引脚*4			V_{IH}	VCC × 0.8	—	—	
					V_{IL}	—	—	VCC × 0.2	

注1.与P205、P206、P400、P401、P407至P415、P511、P512、P708至P713相关的RES和外围功能引脚（共22个引脚）。

注2.除表中已描述的外围功能引脚外的所有输入引脚。注3.P205、P206、P400、P401、P40
7～P415、P511、P512、P708～P713（共21个引脚）。
注4.除表中已描述的端口外的所有输入引脚。
注5.当VCC小于2.7V时，5V容限端口的输入电压应小于3.6V，否则可能发生击穿，因为5V容限端口是电气控制的，以免违反击穿电压。

53.2.3 I/O I_{OH}, I_{OL}

Table 53.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P010, P014, P015, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	Ports P205, P206, P407 to P415, P708 to P713, PB01 (total 18 pins)	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Ports P100 to P107, P208 to P211, P214, P600, P601 (total 15 pins)	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		High spped high drive*4	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA

53.2.3 我爱我哦

Table 53.5 IOIOH IOL(1of2)

Parameter			Symbol	最小值	典型值	最大值	单位
允许输出电流（每个引脚的平均值）	端口P000至P010、P014、P015、P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	端口P205、P206、P407至P415、P708至P713, PB01 (total 18 pins)	低驱动*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高速驱动*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	端口P100至P107、P208至P211、P214、P600, P601 (total 15 pins)	低驱动*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高速驱动*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
		高速高速驱动*4	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	其他输出引脚*5	低驱动*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		中间驱动器*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		高速驱动*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA

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Table 53.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (max value per pin)	Ports P000 to P010, P014, P015, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	Ports P205, P206, P407 to P415, P708 to P713, PB01 (total 18 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Ports P100 to P107, P208 to P211, P214, P600, P601 (total 15 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
		High spped high drive*4	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins		$\Sigma I_{OH\ (max)}$	—	—	–80	mA
			$\Sigma I_{OL\ (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. This is the value when high speed high driving ability is selected in the Port Drive Capability in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. Except for P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Table 53.5 IOIOH IOL(2/2)

Parameter			Symbol	最小值	典型值	最大值	单位
允许输出电流（每个引脚的最大值）	端口P000至P010、P014、P015、P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	端口P205、P206、P407至P415、P708至P713, PB01 (total 18 pins)	低驱动*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		高速驱动*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	端口P100至P107、P208至P211、P214、P600, P601 (total 15 pins)	低驱动*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		高速驱动*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
		高速高速驱动*4	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	其他输出引脚*5	低驱动*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		中间驱动器*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		高速驱动*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA
允许输出电流（所有引脚总和的最大值）	所有输出引脚的最大值		$\Sigma I_{OH\ (max)}$	—	—	–80	mA
			$\Sigma I_{OL\ (max)}$	—	—	80	mA

注1.这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注2.这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注3.这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注4.这是在PmnPFS寄存器的端口驱动能力中选择高速高速驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

注5.P200除外，它是一个输入端口。

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流表示在100μs期间测量的电流平均值。

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53.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 53.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	IIC*1	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
		V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.4		I_{OL} = 1.0 mA
	Ports P205, P206, P407 to P415, P708 to P713, PB01 (total of 18 pins)*2	V_{OH}	VCC – 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
		V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	V_{OH}	VCC – 0.5	—	—		I_{OH} = –1.0 mA
		V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\|I_{in}\|$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Port P200		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	$\|I_{TSI}\|$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P200)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to PB	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, and ports P014, P015, P400, P401, P511, P512	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Other input pins		—	—	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

53.2.4 IOVOH VOL和其他特性

Table 53.6 IOVOH、VOL和其他特性

Parameter		符号	最小值	典型	最大	单元	测试条件
输出电压	IIC	V_{OL}	—	—	0.4	V	我OL=3.0毫安
		V_{OL}	—	—	0.6		我OL=6.0毫安
	IIC*1	V_{OL}	—	—	0.4		IOL=15.0mA(ICFER.FMPE=1)
		V_{OL}	—	0.4	—		IOL=20.0mA(ICFER.FMPE=1)
	ETHERC	V_{OH}	VCC – 0.5	—	—		IOH= 1.0毫安
		V_{OL}	—	—	0.4		我OL=1.0毫安
	端口P205、P206、P407至P415、P708～P713、PB01（共18针）*2	V_{OH}	VCC – 1.0	—	—		IOH= 20mAV CC=3.3V
		V_{OL}	—	—	1.0		我OL=20毫 安VCC=3.3V
	其他输出引脚	V_{OH}	VCC – 0.5	—	—		IOH= 1.0毫安
		V_{OL}	—	—	0.5		我OL=1.0毫安
输入漏电流	RES	$\|I_{in}\|$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Port P200		—	—	1.0		V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5 V-tolerant ports	$\|I_{TSI}\|$	—	—	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	其他港口（港口除外）P200)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉MOS电流	端口P0到PB	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
输入电容	USB_DP、USB_DM和端口P014, P015, P400, P401, P511, P512	C_{in}	—	—	16	pF	Vbias = 0 V Vamp=20mVf =1MHzTa=25° C
	其他输入引脚		—	—	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
注2.这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。
在深度软件待机模式下会保留所选的驾驶能力。

53.2.5 Operating and Standby Current

Table 53.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	—	—	143	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz BCLK = 100 MHz
		Maximum (without USBHS)			—	—	130		
		CoreMark®*5 *6			—	22	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		—	32	—		
			All peripheral clocks disabled, while (1) code executing from flash*5 *6		—	18	—		
		Sleep mode*5 *6			—	11	55		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode*5 *9				—	1.9	—		ICLK = 1 MHz
	Subosc-speed mode*5 *10				—	1.7	—		ICLK = 32.768 kHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	40		—
			SNZCR.RXDREQEN = 0		—	2.1	—		—
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			—	16.9	131	μA	—
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low power function disabled		—	11.8	33.7		—
			Power-on reset circuit low power function enabled		—	4.8	23.8		—
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		—	4.5	—		—
			When a crystal oscillator for low clock loads is in use		—	1.2	—		—
			When a crystal oscillator for standard clock loads is in use		—	1.5	—		—
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		—	0.9	—		V_{BATT} = 1.8 V, VCC = 0 V
					—	1.3	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		—	1.1	—		V_{BATT} = 1.8 V, VCC = 0 V
					—	1.8	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on returning from deep software standby mode		Inrush current*7	I_{RUSH}	—	160	—	mA	
			Energy of inrush current*7	E_{RUSH}	—	1.0	—	μC	

53.2.5 工作和待机电流

Table 53.7 工作和待机电流(1of2)

Parameter				Symbol	Min	Typ	最大	单元	测试条件
供电电流*1	High-speed mode	Maximum*2		I_{CC}*3	—	—	143	mA	ICLK = 200 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz BCLK = 100 MHz
		Maximum (without USBHS)			—	—	130		
		CoreMark®*5 *6			—	22	—		
		正常模式	启用所有外设时钟，同时(1)代码从闪存执行*4		—	32	—		
			禁用所有外设时钟，同时(1)代码从闪存执行*5*6		—	18	—		
		睡眠模式*5*6			—	11	55		
		BGO运行期间增加	数据闪存PE		—	6	—		
			代码闪存PE		—	8	—		
	Low-speed mode*5 *9				—	1.9	—		ICLK = 1 MHz
	Subosc-speed mode*5 *10				—	1.7	—		ICLK = 32.768 kHz
	软件待机模式		SNZCR.RXDREQEN = 1		—	—	40		—
			SNZCR.RXDREQEN = 0		—	2.1	—		—
	Deep 软件待机模式	为备用SRAM和USB恢复检测单元供电			—	16.9	131	μA	—
		未向SRAM或USB恢复检测单元供电	上电复位电路低功耗功能禁用		—	11.8	33.7		—
			上电复位电路低功耗功能启用		—	4.8	23.8		—
		RTC和AGT运行时增加	使用低速片上振荡器(LOCO)时		—	4.5	—		—
			当使用用于低时钟负载的晶体振荡器时		—	1.2	—		—
			当使用标准时钟负载的晶体振荡器时		—	1.5	—		—
	VCC关闭时RTC运行（具有电池备份功能，只有RTC和副时钟振荡器运行）		当使用用于低时钟负载的晶体振荡器时		—	0.9	—		V_{BATT} = 1.8 V, VCC = 0 V
					—	1.3	—		V_{BATT} = 3.3 V, VCC = 0 V
			当使用标准时钟负载的晶体振荡器时		—	1.1	—		V_{BATT} = 1.8 V, VCC = 0 V
					—	1.8	—		V_{BATT} = 3.3 V, VCC = 0 V
	从深度软件待机模式返回时的浪涌电流		Inrush current*7	I_{RUSH}	—	160	—	mA	
			浪涌电流能量*7	E_{RUSH}	—	1.0	—	μC	

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Table 53.7 Operating and standby current (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion		AI_{CC}	—	0.8	1.1	mA	—
	Temperature sensor			—	0.1	0.2	mA	—
	During D/A conversion (per unit)	Without AMP output		—	0.1	0.2	mA	—
		With AMP output		—	0.6	1.1	mA	—
	Waiting for A/D, D/A conversion (all units)			—	0.9	1.6	mA	—
	ADC12, DAC12 in standby modes (all units)*8			—	2	8	µA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)		AI_{REFH0}	—	70	120	µA	—
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	µA	—
	ADC12 in standby modes (unit 0)			—	0.07	0.5	µA	—
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)		AI_{REFH}	—	70	120	µA	—
	During D/A conversion (per unit)	Without AMP output		—	0.1	0.4	mA	—
		With AMP ouput		—	0.1	0.4	mA	—
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion			—	0.07	0.8	µA	—
	ADC12 unit 1 in standby modes			—	0.07	0.8	µA	—
USB operating current	Low speed	USB	$I_{CCUSBLS}$	—	3.5	6.5	mA	VCC_USB
		USBHS		—	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		—	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	Full speed	USB	$I_{CCUSBFS}$	—	4.0	10.0	mA	VCC_USB
		USBHS		—	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		—	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	High speed	USBHS	$I_{CCUSBHS}$	—	50	65	mA	VCC_USBHS = AVCC_USBHS
	Standby mode (direct power down)	USBHS	$I_{CCUSBSBY}$	—	0.5	4.5	µA	VCC_USBHS = AVCC_USBHS

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.
I_{CC} Max. = 0.34 × f + 58 (max. operation in high-speed mode)
I_{CC} Typ. = 0.07 × f + 3.7 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.2 × f + 1.7 (low-speed mode)
I_{CC} Max. = 0.035 × f + 58 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
Note 7. Reference value
Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D converter 1 module stop bit) are in the module-stop state.
Note 9. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
Note 10. BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.

Table 53.7 工作和待机电流(2of2)

Parameter			Symbol	Min	Typ	最大	单元	测试条件
模拟电源电流	在12位AD转换期间		AI_{CC}	—	0.8	1.1	mA	—
	温度感应器			—	0.1	0.2	mA	—
	DA转换期间（每单位）	无AMP输出		—	0.1	0.2	mA	—
		带AMP输出		—	0.6	1.1	mA	—
	等待AD、DA转换（所有单位）			—	0.9	1.6	mA	—
	待机模式下的ADC12、DAC12（所有单元）*8			—	2	8	µA	—
参考电源电流(VREFH0)	在12位AD转换期间（单元0）		AI_{REFH0}	—	70	120	µA	—
	等待12位AD转换（单元0）			—	0.07	0.5	µA	—
	ADC12处于待机模式（单元0）			—	0.07	0.5	µA	—
参考电源电流(VREFH)	在12位AD转换期间（单元1）		AI_{REFH}	—	70	120	µA	—
	DA转换期间（每单位）	无AMP输出		—	0.1	0.4	mA	—
		带AMP输出		—	0.1	0.4	mA	—
	等待12位AD（单元1）、DA（所有单元）转换			—	0.07	0.8	µA	—
	ADC12单元1处于待机模式			—	0.07	0.8	µA	—
USB工作电流	低速	USB	$I_{CCUSBLS}$	—	3.5	6.5	mA	VCC_USB
		USBHS		—	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		—	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	全速	USB	$I_{CCUSBFS}$	—	4.0	10.0	mA	VCC_USB
		USBHS		—	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		—	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	高速	USBHS	$I_{CCUSBHS}$	—	50	65	mA	VCC_USBHS = AVCC_USBHS
	待机模式（直接断电）	USBHS	$I_{CCUSBSBY}$	—	0.5	4.5	µA	VCC_USBHS = AVCC_USBHS

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。
注2.使用提供给外设功能的时钟测量。这不包括BGO操作。
注3.ICC取决于f(ICLK)，如下所示。
我CC最大。=0.34×f+58（高速模式下的最大操作）
我CC典型。=0.07×f+3.7（高速模式下正常运行，所有外设时钟禁用）
I_{CC} Typ. = 0.2 × f + 1.7 (low-speed mode)
I_{CC} Max. = 0.035 × f + 58 (sleep mode)
注4.这不包括BGO操作。
注5.在此状态下停止向外围设备提供时钟信号。这不包括BGO操作。
注6.FCLK、BCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为除以64(3.125MHz)。
注7.参考值
注8.当MCU处于软件待机模式或MSTPCRD.MSTPD16（12位AD转换器0模块停止位）和
MSTPCRD.MSTPD15（12位AD转换器1模块停止位）处于模块停止状态。
注9.FCLK、BCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频（15.6kHz）。
注10.BCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为除以64(512Hz)。FCLK与ICLK的频率相同。

Table 53.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark		I_{CC}	107	µA/MHz	ICLK = 200MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = 3.125MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2		104		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2		87		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Table 53.8 Coremark和正常模式电流

Parameter			Symbol	Typ	Unit	测试条件
电源电流*1	Coremark		I_{CC}	107	µA/MHz	ICLK = 200MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = 3.125MHz
	正常模式	禁用所有外设时钟，开启缓存，同时(1)从闪存执行代码*2		104		
		所有外设时钟禁用，缓存关闭，同时(1)代码从闪存执行*2		87		

注1.电源电流值是在所有输出引脚空载且所有输入上拉MOS处于关闭状态时的值。
注2.在此状态下停止向外围设备提供时钟信号。这不包括BGO操作。

产品评估过程中测试上限样品的平均vaAverage值。-40

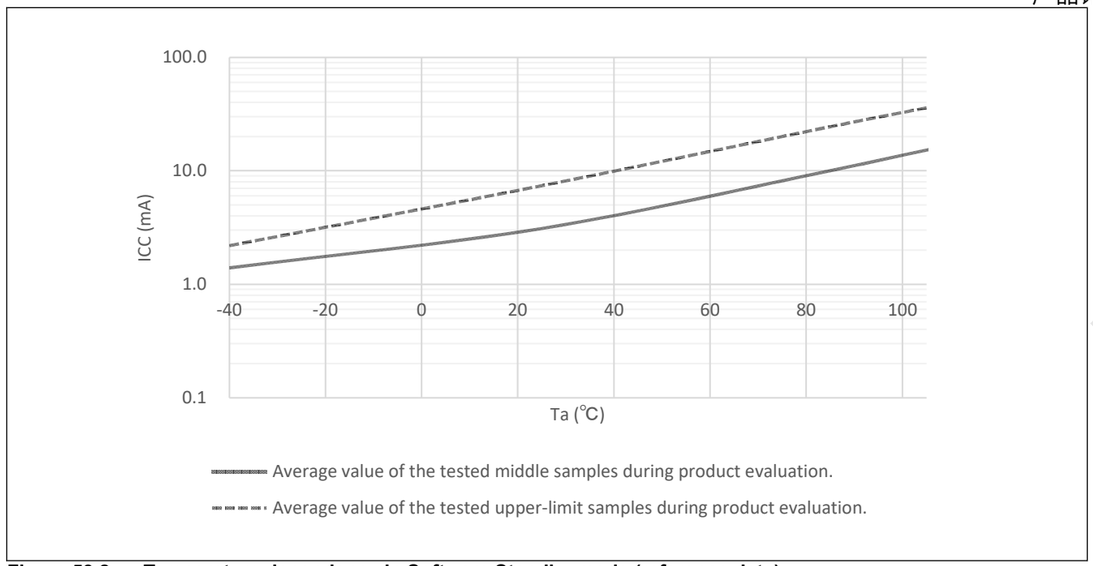

Figure 53.2 Temperature dependency in Software Standby mode (reference data)

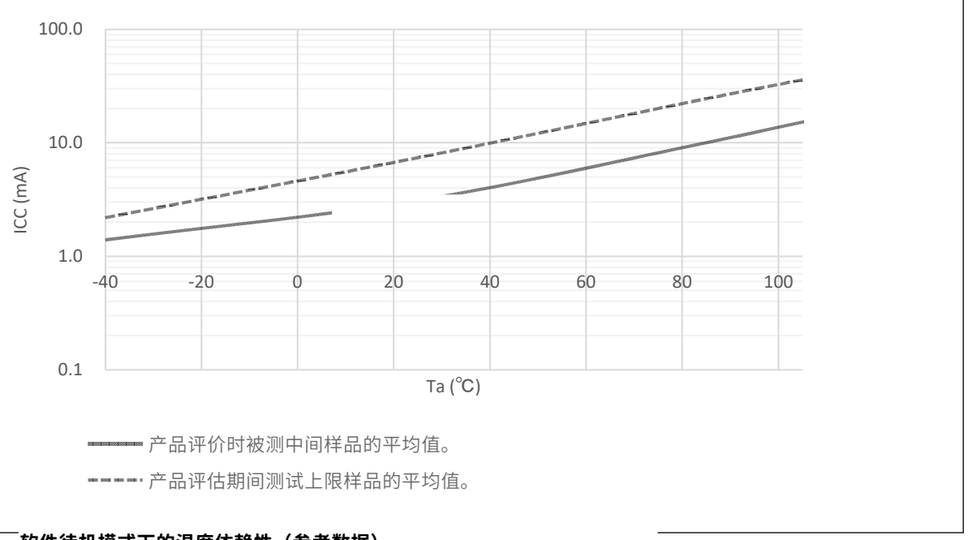

Figure 53.2图5 软件待机模式下的温度依赖性（参考数据）

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产品评估过程中测试上限样品的平均vaAverage值。-40

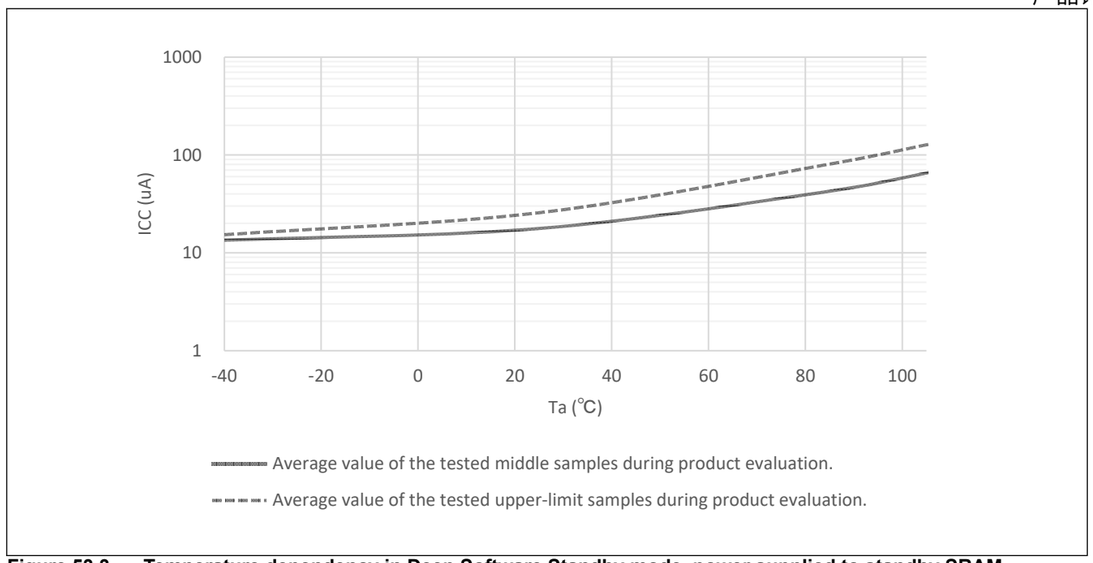

Figure 53.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)

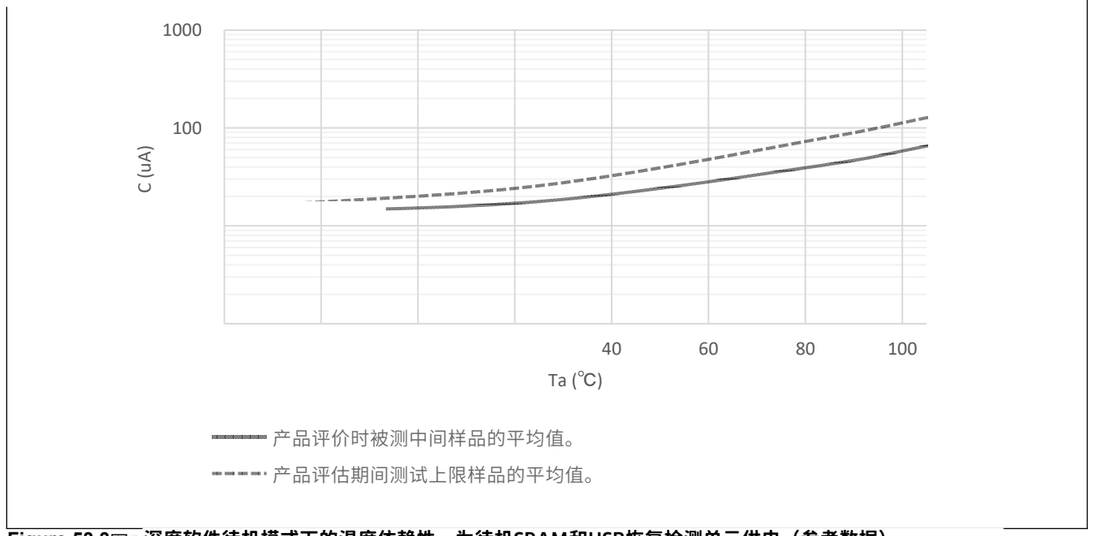

Figure 53.3图5 深度软件待机模式下的温度依赖性、为待机SRAM和USB恢复检测单元供电（参考数据）

产品评估过程中测试上限样品的平均vaAverage值。-40

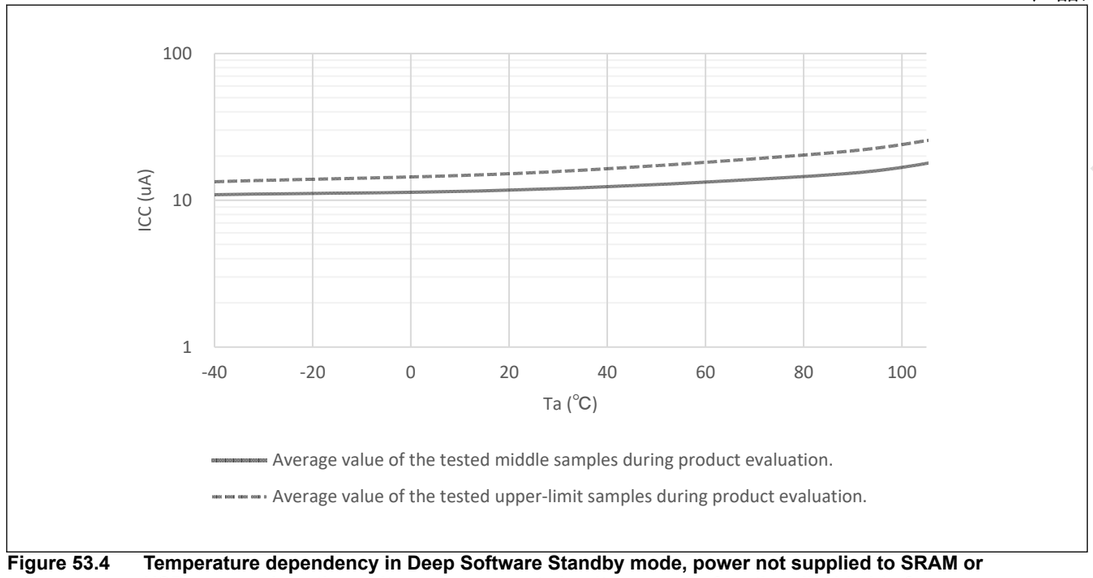

Figure 53.4 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)

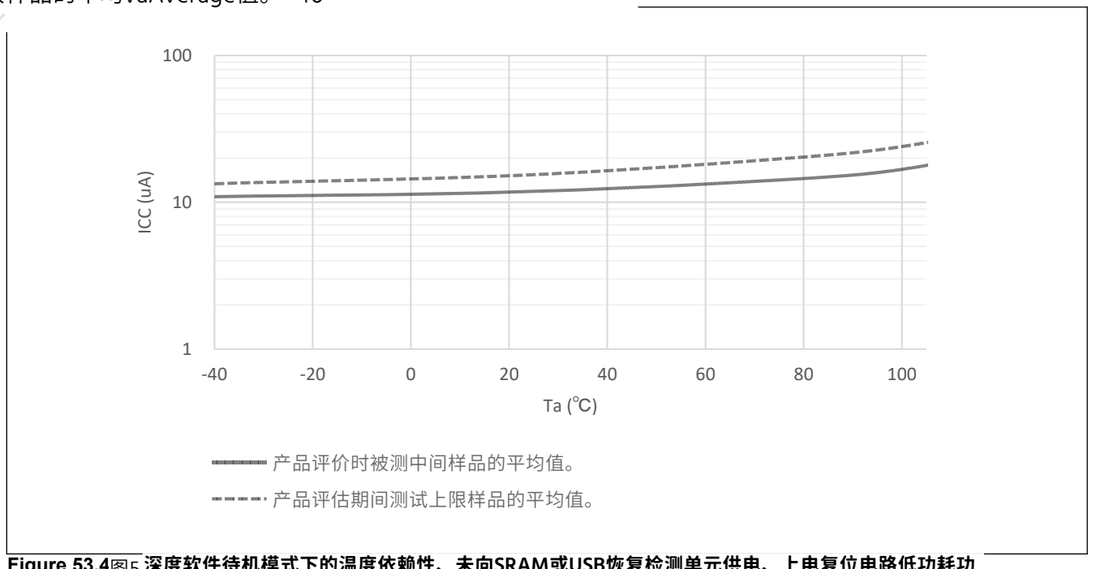

Figure 53.4图5 深度软件待机模式下的温度依赖性、未向SRAM或USB恢复检测单元供电、上电复位电路低功耗功能禁用（参考数据）

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产品评估过程中测试上限样品的平均vaAverage值。-40

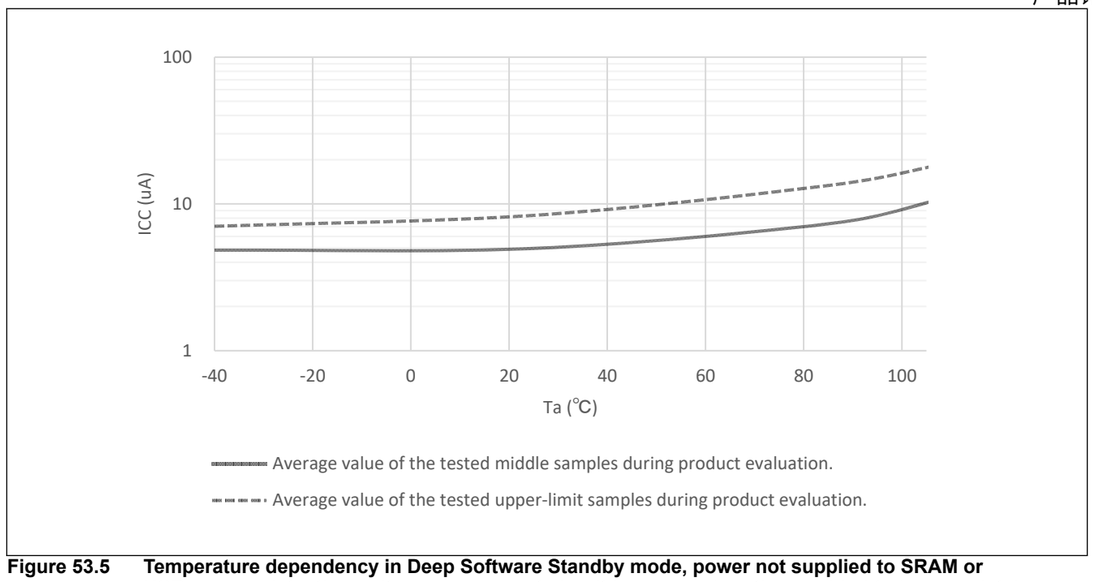

Figure 53.5 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)

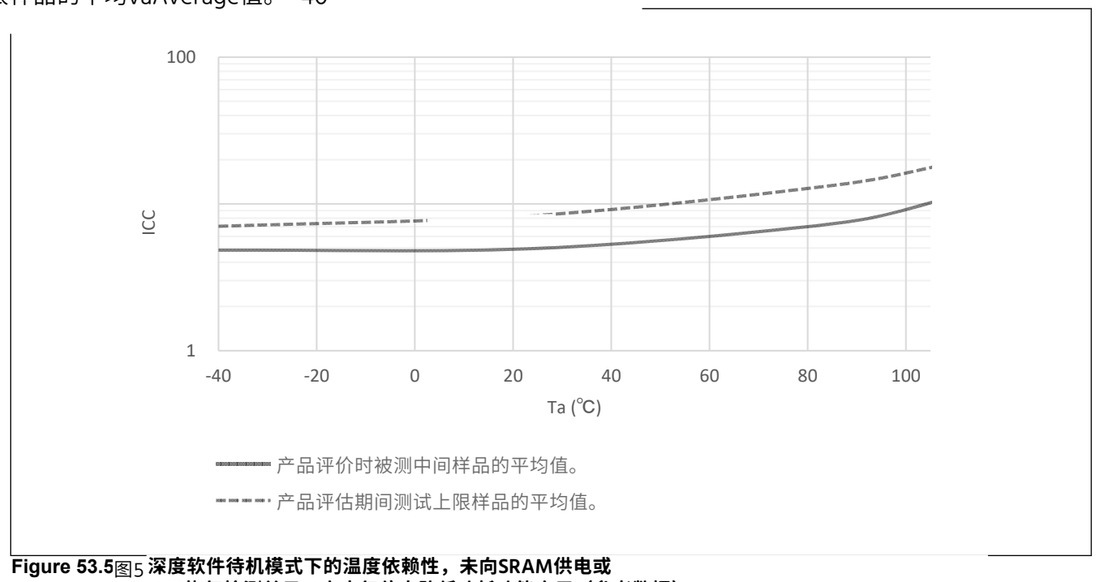

Figure 53.5图5 深度软件待机模式下的温度依赖性，未向SRAM供电或USB恢复检测单元，上电复位电路低功耗功能启用（参考数据）

53.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 53.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI/USB boot mode*1		0.0084	—	20		—
VCC falling gradient*2		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

Table 53.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

53.2.6 VCC上升和下降梯度和纹波频率

Table 53.9 上升和下降梯度特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.0084	—	20	ms/V	—
	启动时启用电压监视器0复位		0.0084	—	—		—
	SCIUSB启动模式*1		0.0084	—	20		—
VCC下降梯度*2		SfVCC	0.0084	—	—	ms/V	—

注1.在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。
注2.这适用于使用VBATT时。

Table 53.10 上升下降梯度和纹波频率特性

纹波电压必须在VCC上限(3.6V)和下限(2.7
五）。当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 53.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
允许电压变化上升下降梯度	dt/dVCC	1.0	—	—	ms/V	当VCC变化超过VCC ±10%

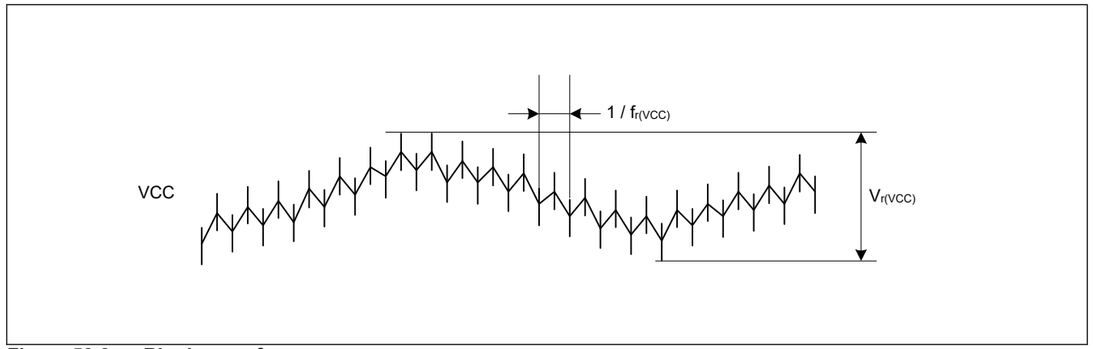

Figure 53.6 Ripple waveform

53.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 53.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 53.11.

Table 53.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	100-pin LQFP (PLQP0100KB-B)	θja	35.0	°C/W	JESD 51-2 and 51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		33.0		
	176-pin LQFP (PLQP0176KB-C)		32.3		
	176-pin BGA (PLBG0176GF-A)		35.4		JESD 51-2 and 51-9 compliant
	100-pin LQFP (PLQP0100KB-B)	Ψjt	0.76	°C/W	JESD 51-2 and 51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		0.63		
	176-pin LQFP (PLQP0176KB-C)		0.48		
	176-pin BGA (PLBG0176GF-A)		0.52		JESD 51-2 and 51-9 compliant

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

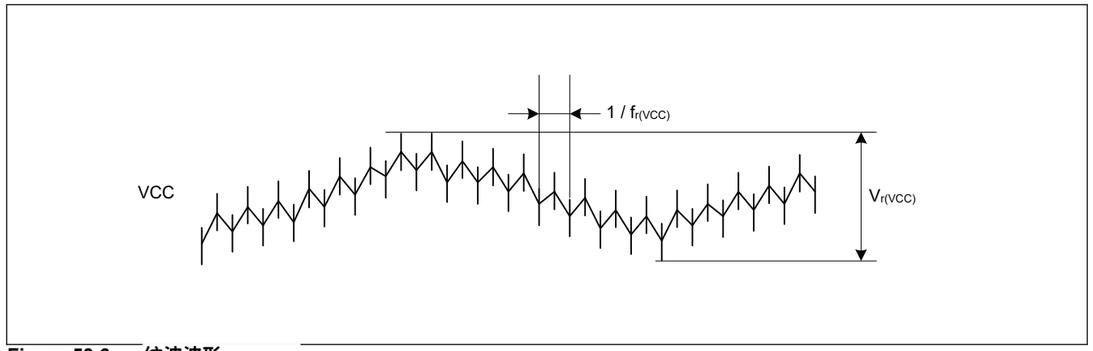

Figure 53.6 纹波波形

53.2.7 热特性

结温（Tj）的最大值不得超过"第53.2.1节的值。TjTa定义"。

Tj通过以下任一公式计算。

●Tj=Ta+θja×总功耗

●Tj=Tt+Ψjt×总功耗

Tj：结温(°C)

Ta：环境温度（°C）

Tt：顶部中心外壳温度(°C)

θja："结"到"环境"的热阻(°CW)

Ψjt："结"到"顶部中心外壳"的热阻(°CW)

●总功耗=电压×（漏电流+动态电流）

●IO漏电流=Σ(IOL×VOL)电压+Σ(IOH×VCC VOH)电压

●IO的动态电流=ΣIO(Cin+Cload)×IO开关频率×电压

Cin:输入电容

C负载：输出电容

关于θja和Ψjt，请参阅表53.11。

Table 53.11 热阻

Parameter	Package	Symbol	Value*1	Unit	测试条件
热阻	100-pin LQFP (PLQP0100KB-B)	θja	35.0	°C/W	符合JESD51-2和51-7
	144-pin LQFP (PLQP0144KA-B)		33.0		
	176-pin LQFP (PLQP0176KB-C)		32.3		
	176-pin BGA (PLBG0176GF-A)		35.4		符合JESD51-2和51-9
	100-pin LQFP (PLQP0100KB-B)	Ψjt	0.76	°C/W	符合JESD51-2和51-7
	144-pin LQFP (PLQP0144KA-B)		0.63		
	176-pin LQFP (PLQP0176KB-C)		0.48		
	176-pin BGA (PLBG0176GF-A)		0.52		符合JESD51-2和51-9

注1.数值为使用4层板时的参考值。热阻取决于板的层数或尺寸。有关详细信息，请参阅JEDEC标准。

53.2.7.1 Calculation guide of I_{CC}max

Table 53.12 shows the power consumption of each unit.

Table 53.12 Power consumption of each unit

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	28.6
			Ta = 85 °C*3	—	—	34.0
			Ta = 95 °C*3	—	—	41.1
			Ta = 105 °C*3	—	—	50.5
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	200	90.786	18.16
	Peripheral Unit	Timer	GPT16 (6ch)*4	100	5.101	0.51
			GPT32 (4ch)*4	100	3.990	0.40
			POEG (4 Groups)*4	50	1.364	0.07
			AGT (6ch)*4	50	11.852	0.59
			RTC	50	4.872	0.24
			WDT	50	0.740	0.04
			IWDT	50	0.282	0.01
		Communication interfaces	ETHERC	100	8.307	0.83
			USBFS	50	9.631	0.48
			USBHS	50	23.571	1.18
			SCI (10ch)*4	100	12.631	1.26
			IIC (2ch)*4	50	4.210	0.21
			CAN/CANFD (2ch)*4	50	23.346	1.17
			CEC	100	0.336	0.03
			SPI (2ch)*4	100	7.503	0.75
			OSPI	50	33.444	1.67
			QSPI	100	2.511	0.25
			SSIE	50	3.480	0.17
			SDHI	50	7.781	0.39
		Analog	ADC12 (2 Units)*4	100	4.725	0.47
			DAC12 (2ch)*4	100	3.630	0.36
			TSN	50	0.161	0.01
		Human machine interfaces	CTSU	50	0.761	0.04
		Event link	ELC	50	1.002	0.05
		Security	SCE9	100	218.100	21.81
		Data processing	CRC	100	0.569	0.06
			DOC	100	0.441	0.04
		System	CAC	50	0.990	0.05
		DMA	DMAC	200	4.519	0.90
			DTC	200	4.427	0.89

53.2.7.1 ICCmax的计算指南

表53.12显示了每个单元的功耗。

Table 53.12 各单元耗电量

动态电流漏电流	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
漏电流	Analog	LDO和泄漏*2	Ta = 75 °C*3	—	—	28.6
			Ta = 85 °C*3	—	—	34.0
			Ta = 95 °C*3	—	—	41.1
			Ta = 105 °C*3	—	—	50.5
动态电流	CPU	操作与闪存和SRAM	Coremark	200	90.786	18.16
	外围单元	Timer	GPT16 (6ch)*4	100	5.101	0.51
			GPT32 (4ch)*4	100	3.990	0.40
			POEG (4 Groups)*4	50	1.364	0.07
			AGT (6ch)*4	50	11.852	0.59
			RTC	50	4.872	0.24
			WDT	50	0.740	0.04
			IWDT	50	0.282	0.01
		通讯接口	ETHERC	100	8.307	0.83
			USBFS	50	9.631	0.48
			USBHS	50	23.571	1.18
			SCI (10ch)*4	100	12.631	1.26
			IIC (2ch)*4	50	4.210	0.21
			CAN/CANFD (2ch)*4	50	23.346	1.17
			CEC	100	0.336	0.03
			SPI (2ch)*4	100	7.503	0.75
			OSPI	50	33.444	1.67
			QSPI	100	2.511	0.25
			SSIE	50	3.480	0.17
			SDHI	50	7.781	0.39
		Analog	ADC12 (2 Units)*4	100	4.725	0.47
			DAC12 (2ch)*4	100	3.630	0.36
			TSN	50	0.161	0.01
		人机界面	CTSU	50	0.761	0.04
		活动链接	ELC	50	1.002	0.05
		Security	SCE9	100	218.100	21.81
		数据处理	CRC	100	0.569	0.06
			DOC	100	0.441	0.04
		System	CAC	50	0.990	0.05
		DMA	DMAC	200	4.519	0.90
			DTC	200	4.427	0.89

RA生态工作室

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 53.13 shows the outline of operation for each unit.

Table 53.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.
RTC	RTC is operating with LOCO.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
ETHERC	Operation modes is set to full-duplex mode. ETHERC is operating using Reduced Media Independent Interface (RMII).
USBFS	Transfer types is set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps).
USBHS	Transfer types is set to bulk transfer. USBHS is operating using High-speed transfer.
SCI	SCI is transmitting data in clock synchronous mode.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 8-bit width data.
OSPI	Transfer mode is single continuous write mode. OSPI is issuing memory write command to OctaRAM.
QSPI	QSPI is issuing Fast Read Quad I/O Instruction.
SSIE	Communication mode is set to Master. System word length is set to 32 bits. Data word length is set to 20 bits. SSIE is transmitting data using I2S format.
CEC	CEC operation clock is set to CECCLK. CEC is transmitting and receiving header block and data block.
SDHI	Transfer bus mode is set to 4-bit wide bus mode. SDHI is issuing CMD24 (single-block write).
ADC12	Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
TSN	TSN is operating.
CTSU	CTSU is operating in self-capacitance single scan mode.
ELC	Only clear module stop bit.
SCE9	SCE9 is executing built-in self test.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data addition mode.

注1.数值由设计保证。
注2.LDO和Leak是内部稳压器的电流和MCU的漏电流。
根据Ta的温度选择。
注3.测量电流时考虑Δ(Tj-Ta)=20°C。
注4.要确定每个通道或单元的电流消耗，请将电流[mA]除以通道 、组或单元的数量。

表53.13显示了每个单元的操作概要。

Table 53.13 每个单元的操作概要（2个中的1个）

Peripheral	操作概要
GPT	操作模式设置为锯齿波PWM模式。 GPT使用PCLKD运行。
POEG	只清除模块停止位。
AGT	AGT使用PCLKB运行。
RTC	RTC与LOCO一起运行。
WDT	WDT使用PCLKB运行。
IWDT	IWDT使用IWDTCLK运行。
ETHERC	操作模式设置为全双工模式。 ETHERC使用精简媒体独立接口(RMII)运行。
USBFS	传输类型设置为批量传输。 USBFS使用全速传输(12Mbps)运行。
USBHS	传输类型设置为批量传输。 USBHS使用高速传输运行。
SCI	SCI在时钟同步模式下传输数据。
IIC	通信格式设置为I2C总线格式。 IIC在主机模式下传输数据。
CANFD	CANFD在自检模式1下发送和接收数据。
SPI	SPI模式设置为SPI操作（4线方法）。 SPI主从模式设置为主模式。 SPI正在传输8位宽度的数据。
OSPI	传输模式为单次连续写入模式。 OSPI正在向OctaRAM发出内存写入命令。
QSPI	QSPI正在发出快速读取四线IO指令。
SSIE	通信模式设置为主。 系统字长设置为32位。 数据字长设置为20位。 SSIE使用I2S格式传输数据。
CEC	CEC操作时钟设置为CECCLK。 CEC是发送和接收头块和数据块。
SDHI	传输总线模式设置为4位宽总线模式。 SDHI正在发布CMD24（单块写入）。
ADC12	分辨率设置为12位精度。 数据寄存器设置为AD转换值加法模式。 ADC12在连续扫描模式下转换模拟输入。
DAC12	DAC12在更新数据寄存器值的同时输出转换结果。
TSN	TSN正在运行。
CTSU	CTSU在自电容单次扫描模式下运行。
ELC	只清除模块停止位。
SCE9	SCE9正在执行内置自检。
CRC	CRC使用32位CRC32-C多项式生成CRC码。
DOC	DOC在数据添加模式下运行。

Table 53.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

53.2.7.2 Example of T_j calculation

Assumption :

- Package 176-pin LQFP : θja = 32.3 °C/W
- Ta = 100 °C
- I_{CC}max = 70 mA
- VCC = 3.5 V (VCC = AVCC0 = AVCC_USBHS = VCC_USB = VCC_USBHS)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 12 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 8 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 12 Outputs
- C_{in} = 8 pF, 32 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 32 pins, Output frequency = 10 MHz

Leakage current of IO = Σ (V_{OL} × I_{OL}) / Voltage + Σ ((VCC - V_{OH}) × I_{OH}) / Voltage
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
= ((8 pF × 32) × 10 MHz + (30 pF × 32) × 10 MHz) × 3.5 V
= 42.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)
= (70 mA × 3.5 V) + (49.1 mA + 42.6 mA) × 3.5 V
= 566 mW (0.566 W)

Tj = Ta + θja × Total power consumption
= 100 °C + 32.3 °C/W × 0.566W
= 118.7 °C

53.3 AC Characteristics

Table 53.13 每个单元的操作概要（2个中的2个）

Peripheral	操作概要
CAC	测量目标时钟设置为PCLKB。 测量参考时钟设置为PCLKB。CAC正在测量时钟 频率精度。
DMAC	传输数据的位长设置为32位。 传输模式设置为块传输模式。 DMAC正在将数据从SRAM0传输到SRAM0。
DTC	传输数据的位长设置为32位。 传输模式设置为块传输模式。 DTC正在将数据从SRAM0传输到SRAM0。

53.2.7.2 Tj计算示例

Assumption :

- Package 176-pin LQFP : θja = 32.3 °C/W
- Ta = 100 °C

●ICC最大值=70mA

- VCC = 3.5 V (VCC = AVCC0 = AVCC_USBHS = VCC_USB = VCC_USBHS)

●IOH=1mA，VOH=VCC 0.5V，12个输出

●IOL=20mA，VOL=1.0V，8个输出

●IOL=1mA，VOL=0.5V，12路输出

●Cin=8pF，32引脚，输入频率=10MHz

●C负载=30pF，32引脚，输出频率=10MHz

IO的漏电流=Σ(VOL×IOL)电压+Σ((VCCVOH)×IOH)电压
= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V
= 45.7 mA + 1.71 mA + 1.71 mA
= 49.1 mA

IO的动态电流 =ΣIO(Cin+Cload)×IO开关频率×电压
= ((8 pF × 32) × 10 MHz + (30 pF × 32) × 10 MHz) × 3.5 V
= 42.6 mA

总功耗 =电压×(漏电流+动态电流)
= (70 mA × 3.5 V) + (49.1 mA + 42.6 mA) × 3.5 V
= 566 mW (0.566 W)

Tj =Ta+θja×总功耗
= 100 °C + 32.3 °C/W × 0.566W
= 118.7 °C

53.3 交流特性

53.3.1 Frequency

Table 53.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)	f	—	—	200	MHz
	Peripheral module clock (PCLKA)*2		—	—	100	
	Peripheral module clock (PCLKB)*2		—	—	50	
	Peripheral module clock (PCLKC)*2		—*3	—	50	
	Peripheral module clock (PCLKD)*2		—	—	100	
	Flash interface clock (FCLK)*2		—*1	—	50	
	External bus clock (BCLK)*2		—	—	100	
	EBCLK pin output		—	—	50	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 53.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	—	—	1	MHz
	Peripheral module clock (PCLKA)*2		—	—	1	
	Peripheral module clock (PCLKB)*2		—	—	1	
	Peripheral module clock (PCLKC)*2 *3		—*3	—	1	
	Peripheral module clock (PCLKD)*2		—	—	1	
	Flash interface clock (FCLK)*1 *2		—	—	1	
	External bus clock (BCLK)		—	—	1	
	EBCLK pin output		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 53.16 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	29.4	—	36.1	kHz
	Peripheral module clock (PCLKA)*2		—	—	36.1	
	Peripheral module clock (PCLKB)*2		—	—	36.1	
	Peripheral module clock (PCLKC)*2 *3		—	—	36.1	
	Peripheral module clock (PCLKD)*2		—	—	36.1	
	Flash interface clock (FCLK)*1 *2		29.4	—	36.1	
	External bus clock (BCLK)*2		—	—	36.1	
	EBCLK pin output		—	—	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. See section 8, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. The ADC12 cannot be used.

53.3.1 Frequency

Table 53.14 高速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟（ICLK*2）	f	—	—	200	MHz
	外围模块时钟(PCLKA)*2		—	—	100	
	外围模块时钟(PCLKB)*2		—	—	50	
	外围模块时钟(PCLKC)*2		—*3	—	50	
	外围模块时钟(PCLKD)*2		—	—	100	
	闪存接口时钟(FCLK)*2		—*1	—	50	
	外部总线时钟(BCLK)*2		—	—	100	
	EBCLK引脚输出		—	—	50	

注1.在对闪存进行编程或擦除时，FCLK必须以至少4MHz的频率运行。
注2.有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率之间的关系，请参见第8节“时钟生成电路”。

注3.使用ADC12时，PCLKC频率必须至少为1MHz。

Table 53.15 低速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	—	—	1	MHz
	外围模块时钟(PCLKA)*2		—	—	1	
	外围模块时钟(PCLKB)*2		—	—	1	
	外围模块时钟(PCLKC)*2*3		—*3	—	1	
	外围模块时钟(PCLKD)*2		—	—	1	
	Flash接口时钟(FCLK)*1*2		—	—	1	
	外部总线时钟(BCLK)		—	—	1	
	EBCLK引脚输出		—	—	1	

注1.在低速模式下禁止对闪存进行编程或擦除。
注2.有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率之间的关系，请参见第8节“时钟生成电路”。

注3.使用ADC12时，PCLKC频率必须设置为至少1MHz。

Table 53.16 Subosc-speed模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	29.4	—	36.1	kHz
	外围模块时钟(PCLKA)*2		—	—	36.1	
	外围模块时钟(PCLKB)*2		—	—	36.1	
	外围模块时钟(PCLKC)*2*3		—	—	36.1	
	外围模块时钟(PCLKD)*2		—	—	36.1	
	Flash接口时钟(FCLK)*1*2		29.4	—	36.1	
	外部总线时钟(BCLK)*2		—	—	36.1	
	EBCLK引脚输出		—	—	36.1	

注1.在Subosc速度模式下，编程或擦除闪存被禁用。
注2.有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK频率之间的关系，请参见第8节“时钟生成电路”。

注3.ADC12不能使用。

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53.3.2 Clock Timing

Table 53.17 Clock timing except for sub-clock oscillator

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time		t_{Bcyc}	20	—	—	ns	Figure 53.7
EBCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
EBCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
EBCLK pin output rise time		t_{Cr}	—	—	5.0	ns	
EBCLK pin output fall time		t_{Cf}	—	—	5.0	ns	
EXTAL external clock input cycle time		t_{EXcyc}	41.66	—	—	ns	Figure 53.8
EXTAL external clock input high pulse width		t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 53.9
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	µs	Figure 53.10
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter		—	—	±85	—	ps	—
FLL stabilization wait time		t_{FLLWT}	—	—	1.8	ms	—
PLL clock frequency		f_{PLL}	120	—	200	MHz	—
PLL2 clock frequency		f_{PLL2}	120	—	240	MHz	—
PLL/PLL2 clock oscillation stabilization wait time		t_{PLLWT}	—	—	174.9	µs	Figure 53.11
PLL/PLL2 period jitter		—	—	±100	—	ps	—
PLL/PLL2 long term jitter		—	—	±300	—	ps	Term: 1µs, 10µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

53.3.2 时钟时序

Table 53.17 除副时钟振荡器外的时钟时序

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
EBCLK引脚输出周期时间		t_{Bcyc}	20	—	—	ns	Figure 53.7
EBCLK引脚输出高脉冲宽度		t_{CH}	3.3	—	—	ns	
EBCLK引脚输出低脉冲宽度		t_{CL}	3.3	—	—	ns	
EBCLK引脚输出上升时间		t_{Cr}	—	—	5.0	ns	
EBCLK引脚输出下降时间		t_{Cf}	—	—	5.0	ns	
EXTAL外部时钟输入周期时间		t_{EXcyc}	41.66	—	—	ns	Figure 53.8
EXTAL外部时钟输入高脉冲宽度		t_{EXH}	15.83	—	—	ns	
EXTAL外部时钟输入低脉冲宽度		t_{EXL}	15.83	—	—	ns	
EXTAL外部时钟上升时间		t_{EXr}	—	—	5.0	ns	
EXTAL外部时钟下降时间		t_{EXf}	—	—	5.0	ns	
主时钟振荡器频率		f_{MAIN}	8	—	24	MHz	—
主时钟振荡稳定等待时间（晶体）*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 53.9
LOCO时钟振荡频率		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO时钟振荡稳定等待时间		t_{LOCOWT}	—	—	60.4	µs	Figure 53.10
ILOCO时钟振荡频率		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO时钟振荡稳定等待时间		t_{MOCOWT}	—	—	15.0	µs	—
HOCO时钟振荡器振荡频率	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		40≤Ta≤105°C副时钟频率精度为±50ppm。
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO时钟振荡稳定等待时间*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO周期抖动		—	—	±85	—	ps	—
FLL稳定等待时间		t_{FLLWT}	—	—	1.8	ms	—
锁相环时钟频率		f_{PLL}	120	—	200	MHz	—
PLL2时钟频率		f_{PLL2}	120	—	240	MHz	—
PLLPLL2时钟振荡稳定等待时间		t_{PLLWT}	—	—	174.9	µs	Figure 53.11
PLLPLL2周期抖动		—	—	±100	—	ps	—
PLLPLL2长期抖动		—	—	±300	—	ps	Term: 1µs, 10µs

注1.设置主时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟振荡器。

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Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 53.18 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 53.12

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

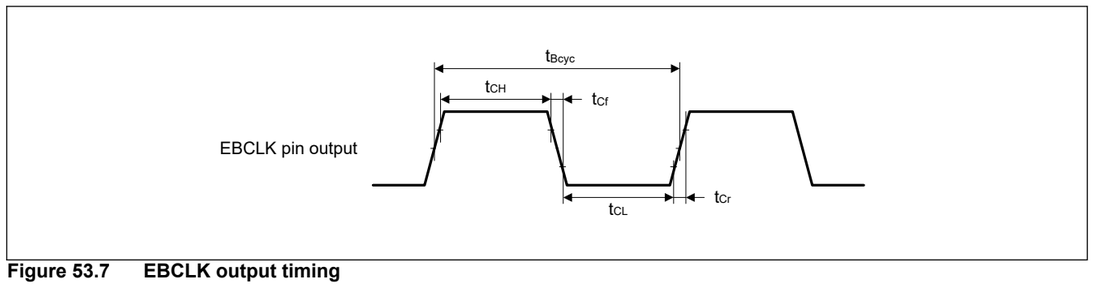


Figure 53.7 EBCLK output timing

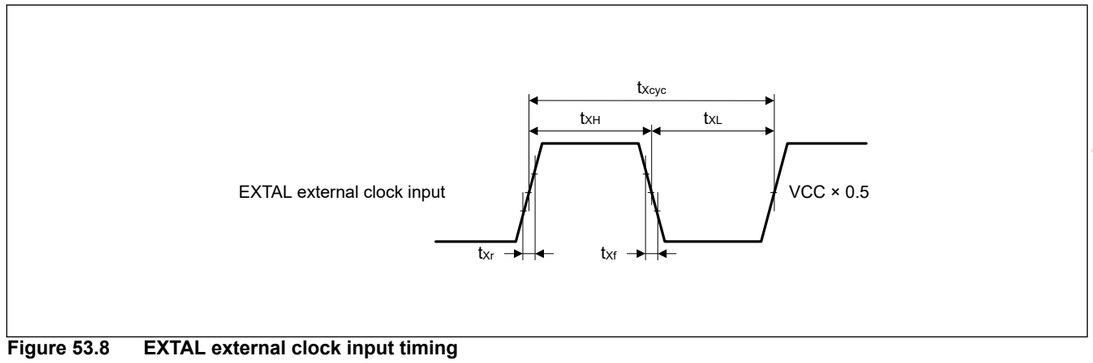


Figure 53.8 EXTAL external clock input timing

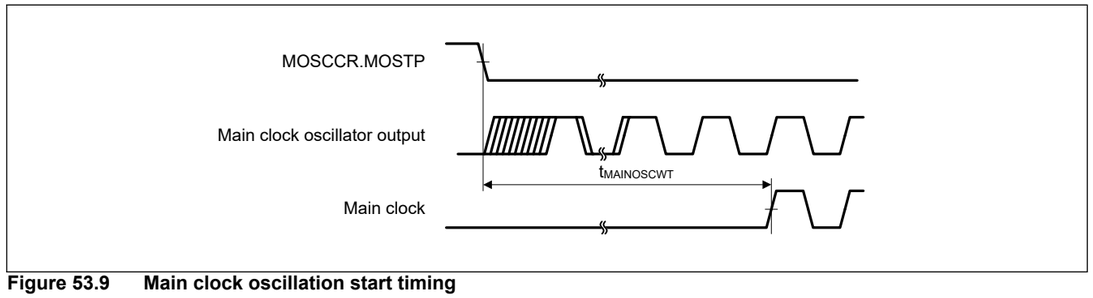


Figure 53.9 Main clock oscillation start timing

注2.这是从复位状态释放到HOCO振荡频率(fHOCO)达到保证工作范围的时间。

Table 53.18 副时钟振荡器的时钟时序

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
副时钟振荡稳定等待时间	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 53.12

注1.设置副时钟振荡器时，请咨询振荡器制造商进行振荡评估，并将结果作为推荐的振荡稳定时间。更改SOSCCR.SOSTP位的设置以启动副时钟操作后，只有在副时钟振荡稳定时间过去并留有足够余量后才开始使用副时钟振荡器。建议使用两倍于显示值的值。

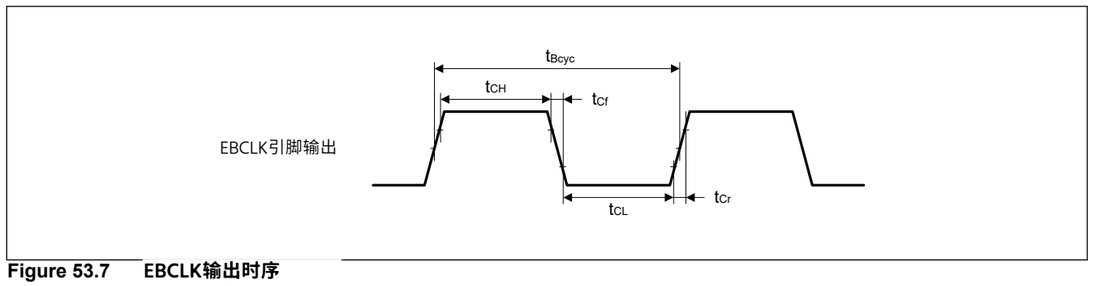


Figure 53.7 EBCLK输出时序

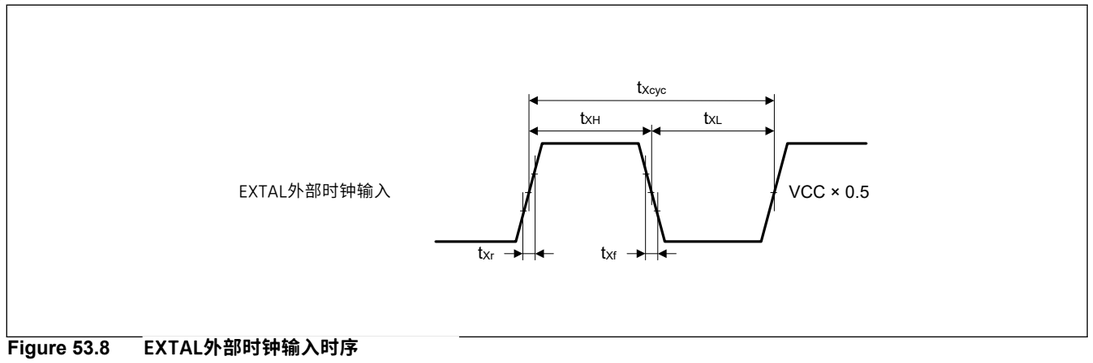


Figure 53.8 EXTAL外部时钟输入时序

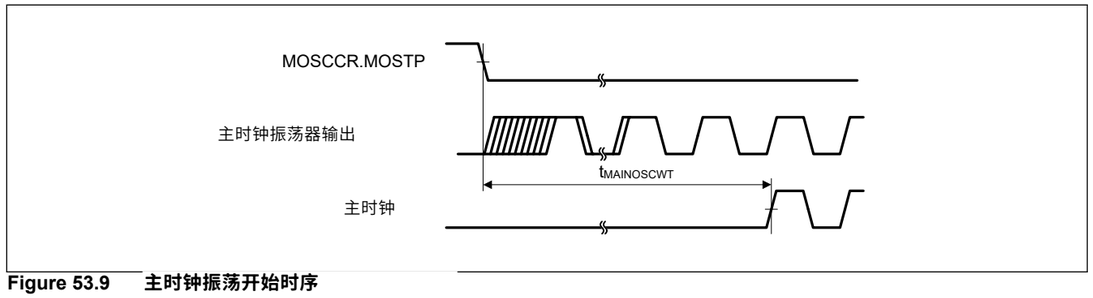


Figure 53.9 主时钟振荡开始时序

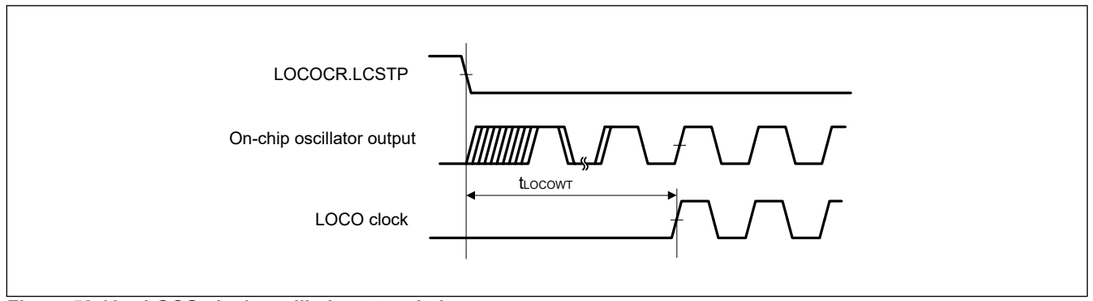


Figure 53.10 LOCO clock oscillation start timing

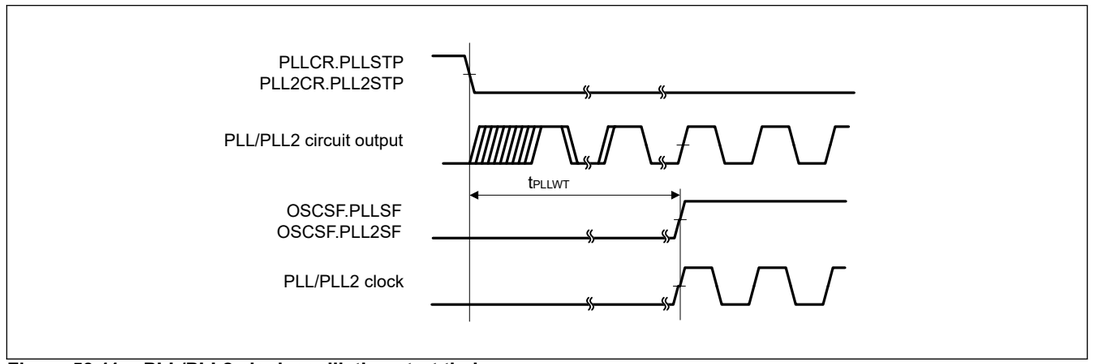


Figure 53.11 PLL/PLL2 clock oscillation start timing

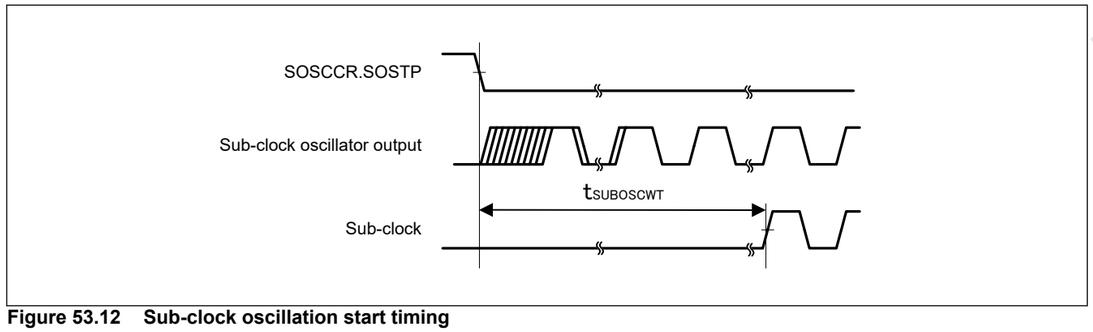


Figure 53.12 Sub-clock oscillation start timing

53.3.3 Reset Timing

Table 53.19 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 53.13
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 53.14
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 53.13

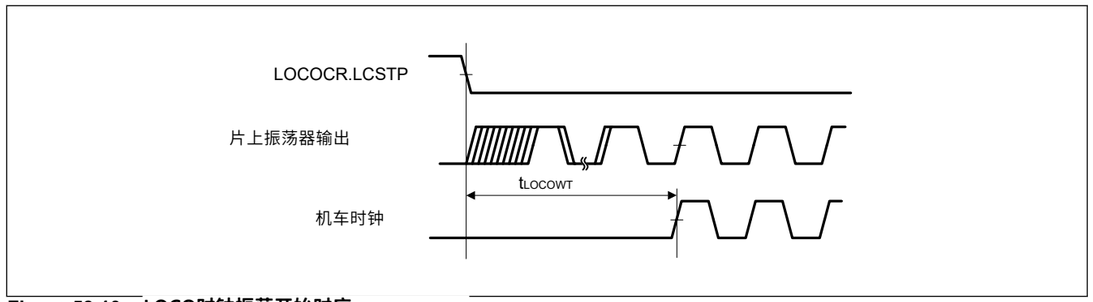


Figure 53.10 LOCO时钟振荡开始时序

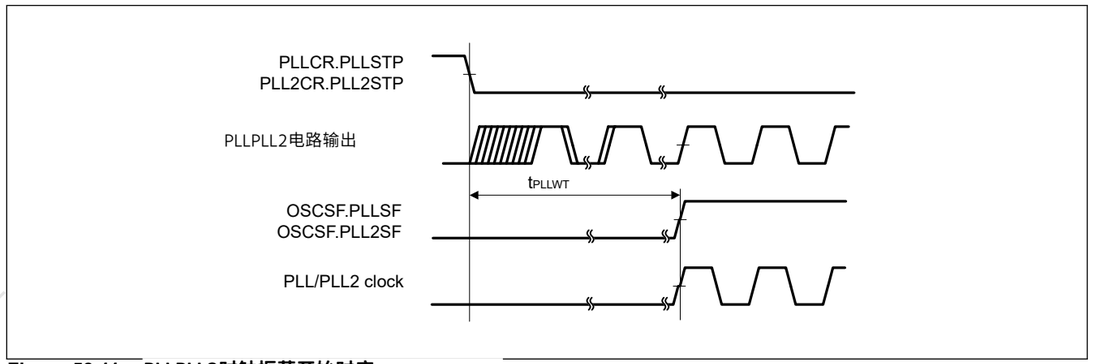


Figure 53.11 PLLPLL2时钟振荡开始时序

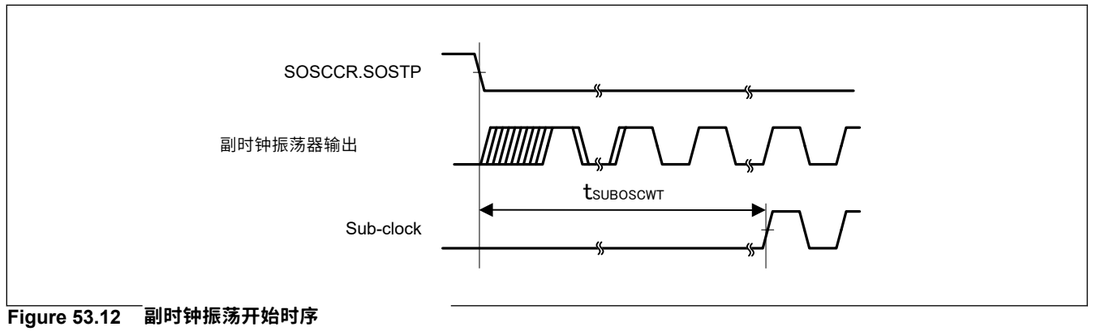


Figure 53.12 副时钟振荡开始时序

53.3.3 重置时间

Table 53.19 重置时间(1of2)

Parameter		符号	最小值	典型值	Max	单元	测试条件
RES脉冲宽度	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 53.13
	深度软件待机模式	t_{RESWD}	0.6	—	—	ms	Figure 53.14
	软件待机模式，Subosc速度模式	t_{RESWS}	0.3	—	—	ms	
	所有其他	t_{RESW}	200	—	—	µs	
RES取消后的等待时间		t_{RESWT}	—	37.3	41.2	µs	Figure 53.13

Table 53.19 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)	t_{RESW2}	—	324	397.7	µs	—

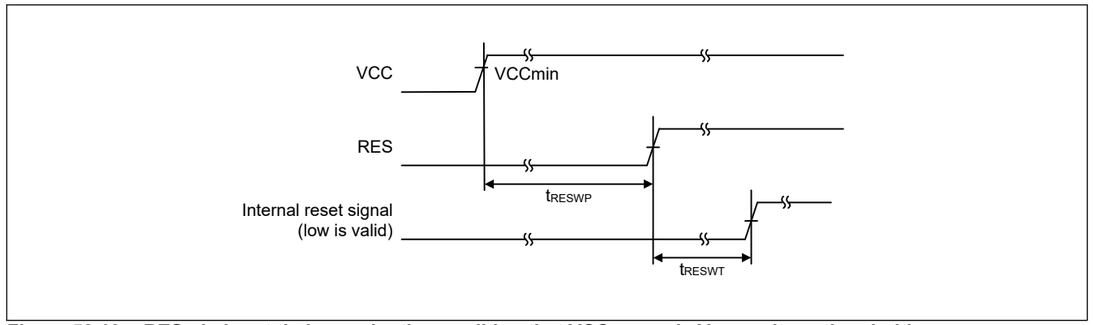


Figure 53.13 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

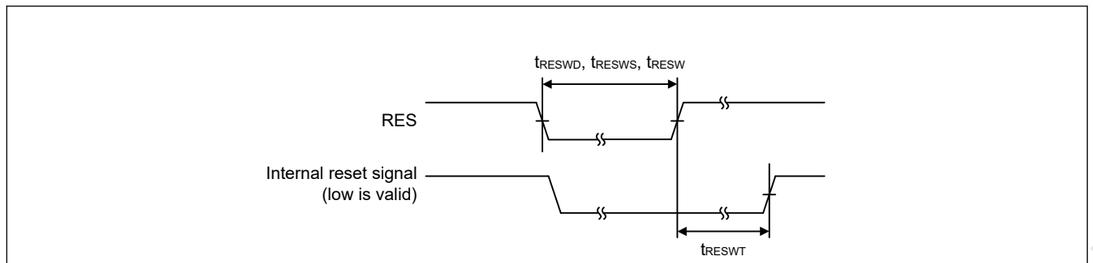


Figure 53.14 Reset input timing

53.3.4 Wakeup Timing

Table 53.20 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 53.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*13	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*13	—	170	255	µs	
	System clock source is sub-clock oscillator*6 *11		t_{SBYSC}*13	—	0.7	0.8	ms	
	System clock source is LOCO*7 *11		t_{SBYLO}*13	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*8		t_{SBYHO}*13	—	55	130	µs	
	System clock source is PLL with HOCO*9		t_{SBYPH}*13	—	175	265	µs	
	System clock source is MOCO clock oscillator*10		t_{SBYMO}*13	—	35	65	µs	

Table 53.19 重置时间（2之2）

Parameter	符号	最小值	典型值	Max	单元	测试条件
内部复位取消后的等待时间（IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、SRAMECC错误复位、总线主控MPU错误复位、TrustZone错误复位、缓存奇偶校验错误复位）	t_{RESW2}	—	324	397.7	µs	—

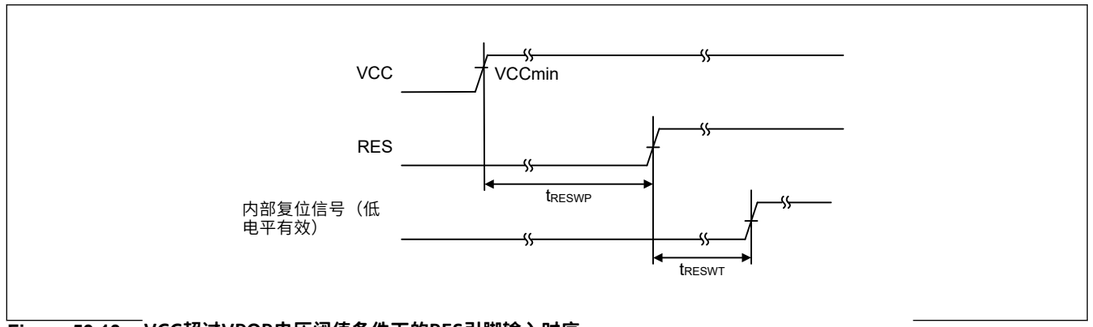


Figure 53.13 VCC超过VPOR电压阈值条件下的RES引脚输入时序

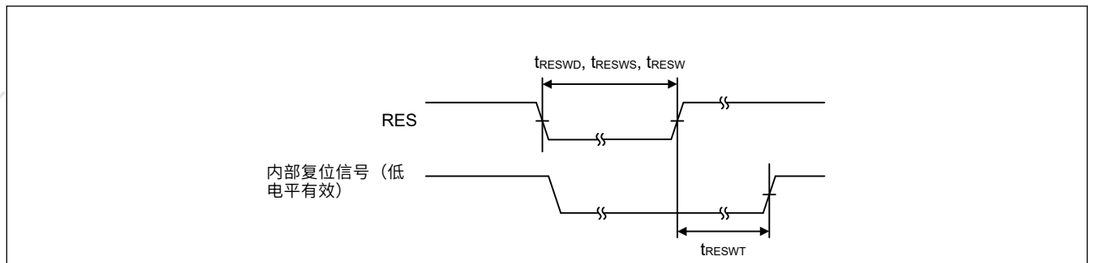


Figure 53.14 复位输入时序

53.3.4 唤醒时间

Table 53.20 从低功耗模式恢复的时间（2个中的1个）

Parameter			Symbol	Min	Typ	Max	单元	测试条件
恢复时间从软件待机模式*1	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 53.15 所有振荡器的分频比为1。
		系统时钟源为带主时钟振荡器的PLL*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器*4	t_{SBYEX}*13	—	45	125	µs	
		系统时钟源为带主时钟振荡器的PLL*5	t_{SBYPE}*13	—	170	255	µs	
	系统时钟源为副时钟振荡器*6*11		t_{SBYSC}*13	—	0.7	0.8	ms	
	系统时钟源为LOCO*7*11		t_{SBYLO}*13	—	0.7	0.9	ms	
	系统时钟源为HOCO时钟振荡器*8		t_{SBYHO}*13	—	55	130	µs	
	系统时钟源是带有HOCO*9的PLL		t_{SBYPH}*13	—	175	265	µs	
	系统时钟源为MOCO时钟振荡器*10		t_{SBYMO}*13	—	35	65	µs	

Table 53.20 Timing of recovery from low power modes (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E	t_{DSBY}	—	0.38	0.54	ms	Figure 53.16
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19	t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode		t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	—	35*12	70*12	µs	Figure 53.17
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	—	11*12	14*12	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop))
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 13. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

Table 53.20 从低功耗模式恢复的时间（2个中的2个）

Parameter		Symbol	Min	Typ	Max	单元	测试条件
恢复时间从深度软件待机模式	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E	t_{DSBY}	—	0.38	0.54	ms	Figure 53.16
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19	t_{DSBY}	—	0.55	0.73	ms	
取消深度软件待机模式后的等待时间		t_{DSBYWT}	56	—	57	t_{cyc}	
恢复时间从软件待机模式到贪睡模式	系统时钟源为高速模式 HOCO (20 MHz)	t_{SNZ}	—	35*12	70*12	µs	Figure 53.17
	系统时钟源为高速模式 MOCO (8 MHz)	t_{SNZ}	—	11*12	14*12	µs	

注1.恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=一个振荡器作为系统时钟源的恢复时间+系统时钟有效振荡器中的最长tSBYOSCWTtSBYOSCWT+2个LOCO周期（当LOCO正在运行）+Subosc正在振荡且MSTPC0=0（CAC模块停止））

注2.当晶振频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05）且内部时钟分频设置的最大值为1时。

注3.当PLL的频率为200MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x05）且内部时钟分频设置的最大值为4时。

注4.当外部时钟频率为24MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00）且内部时钟分频设置的最大值为1时。

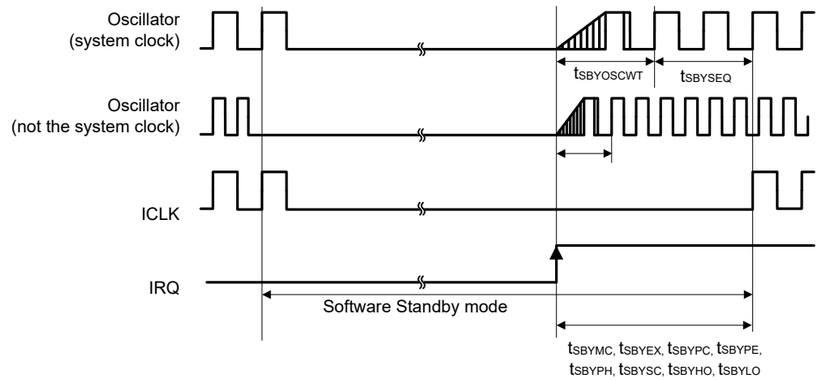
注5.当PLL的频率为200MHz（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为0x00）且内部时钟分频设置的最大值为4时。

注6.副时钟振荡器频率为32.768KHz，内部时钟分频设置的最大值为1。
注7.LOCO频率为32.768kHz，内部时钟分频设置的最大值为1。
注8.HOCO频率为20MHz，内部时钟分频设置最大值为1。注9.PLL频率为200MHz，内部时钟分频设置最大值为4。注10.MOCO频率为8MHz，内部时钟分频设置的最大值为1。

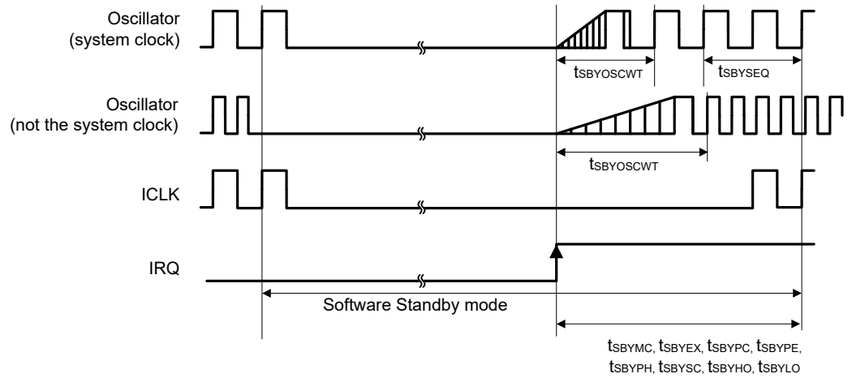
注11.在Subosc速度模式下，副时钟振荡器或LOCO在软件待机模式下继续振荡。
注12.当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：16μs（典型值）、48μs（最大值）。

注13.恢复时间可以用tSBYOSCWT+tSBYSEQ等式计算。并且它们可以通过以下值和等式确定。对于n，从内部时钟分频设置中选择最大值。

唤醒时间典型值			MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

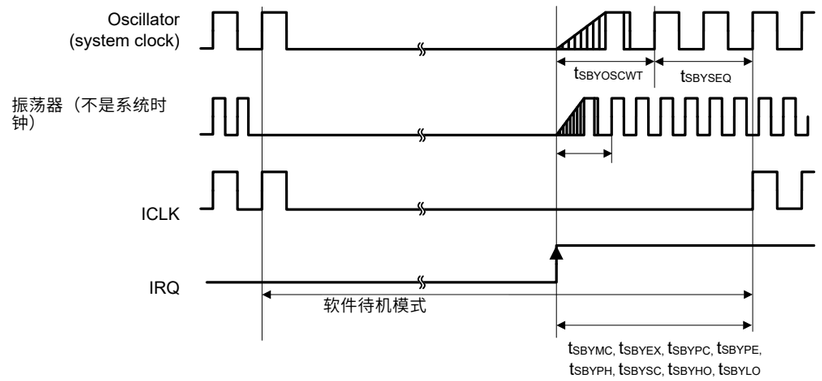


When stabilization of the system clock oscillator is slower

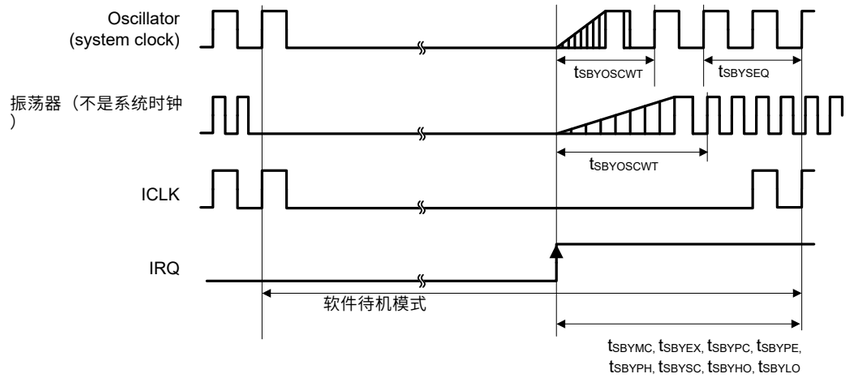


When stabilization of an oscillator other than the system clock is slower

Figure 53.15 Software Standby mode cancellation timing



当系统时钟振荡器的稳定速度较慢时



当系统时钟以外的振荡器稳定较慢时

Figure 53.15 软件待机模式取消时序

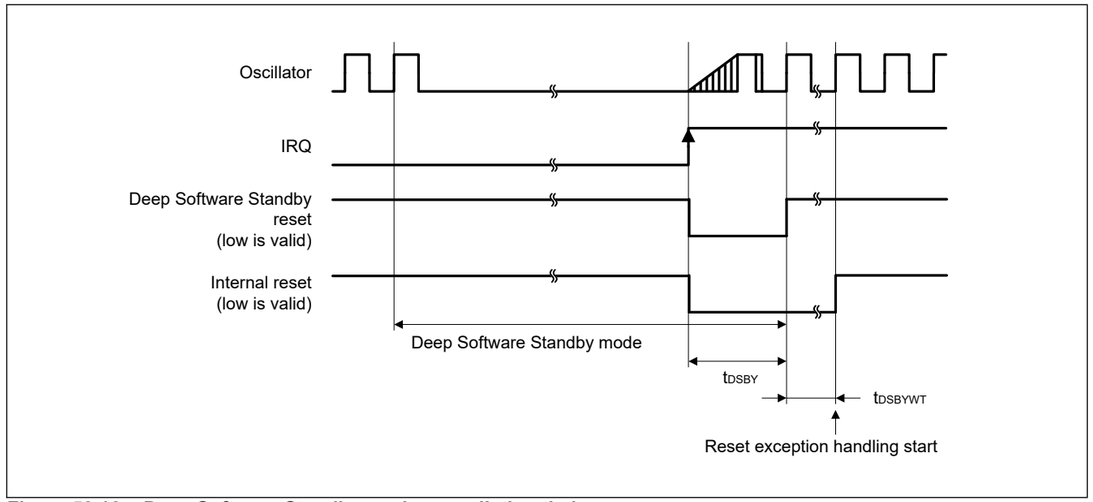
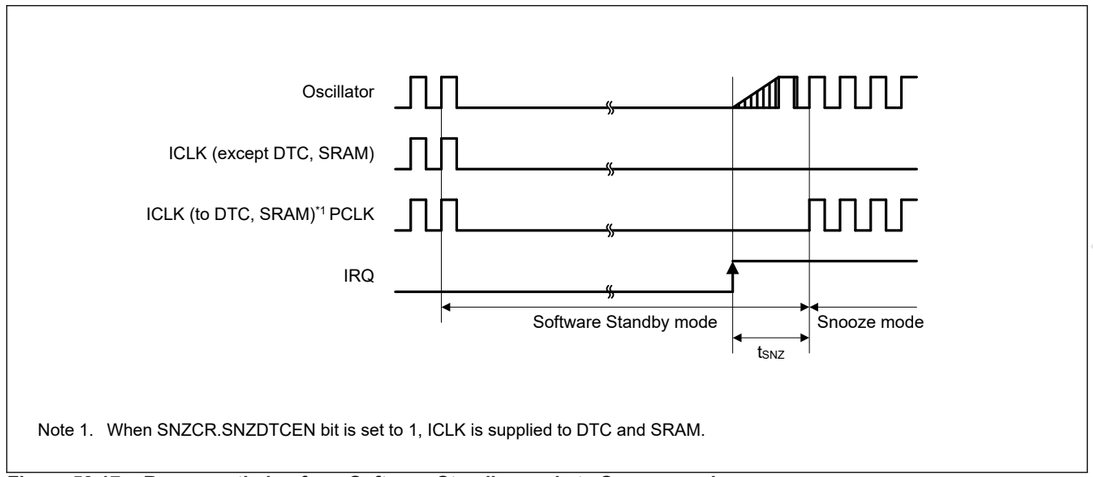


Figure 53.16 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 53.17 Recovery timing from Software Standby mode to Snooze mode

53.3.5 NMI and IRQ Noise Filter

Table 53.21 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

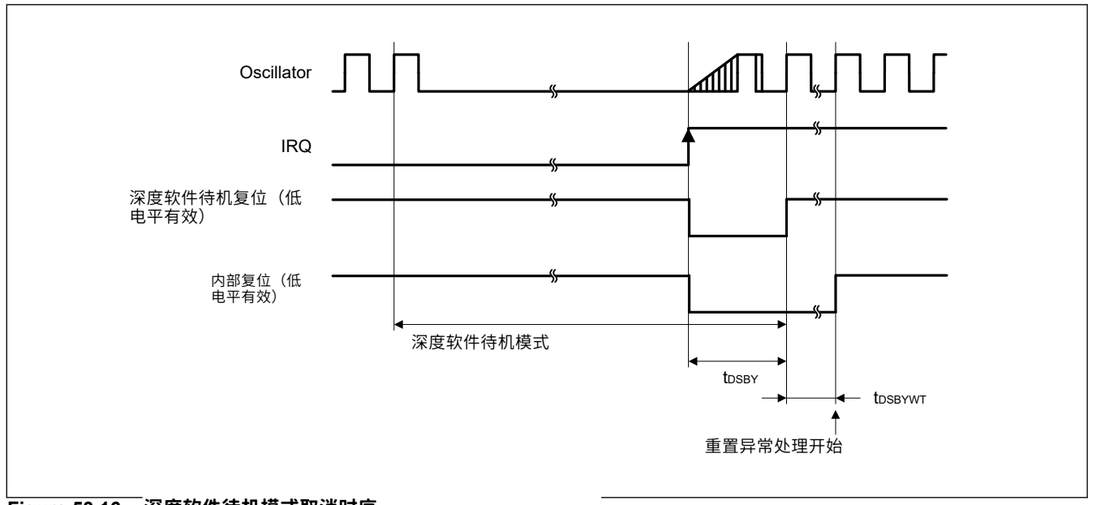
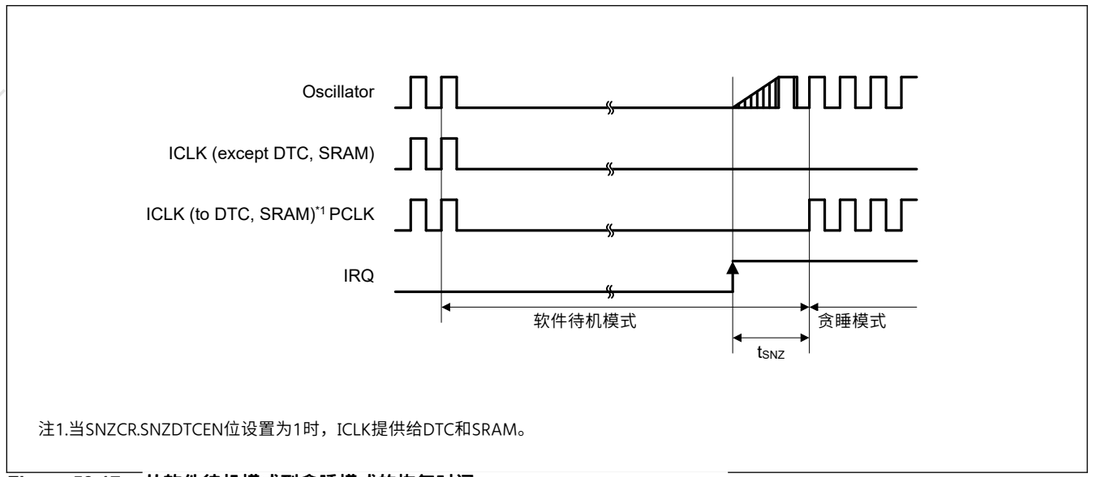


Figure 53.16 深度软件待机模式取消时序



注1.当SNZCR.SNZDTCEN位设置为1时，ICLK提供给DTC和SRAM。

Figure 53.17 从软件待机模式到贪睡模式的恢复时间

53.3.5 NMI和IRQ噪声滤波器

Table 53.21 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	—	—	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	—	—	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

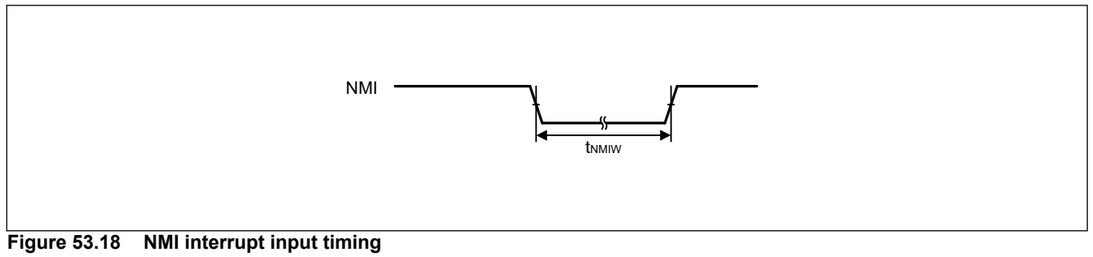


Figure 53.18 NMI interrupt input timing

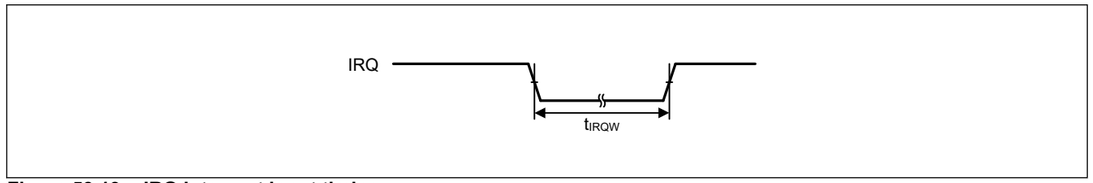


Figure 53.19 IRQ interrupt input timing

53.3.6 Bus Timing

Table 53.22 Bus timing

Condition:
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.
EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	—	12.5	ns	Figure 53.22 to Figure 53.25
Byte control delay	t_{BCD}	—	12.5	ns	
CS delay	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD delay	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR/WRn delay	t_{WRD}	—	12.5	ns	
Write data delay	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT setup time	t_{WTS}	12.5	—	ns	Figure 53.26
WAIT hold time	t_{WTH}	0	—	ns	

Note: 软件待机模式下最少200ns。
Note: 如果时钟源切换，则增加切换源的4个时钟周期。
注1.tPcyc表示PCLKB周期。
注2.tNMICK表示NMI数字滤波器采样时钟的周期。注3.tIRQCK表示IRQi数字滤波器采样时钟的周期。

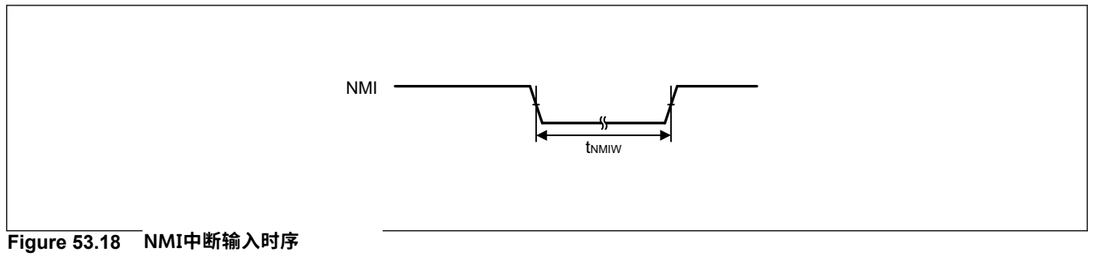


Figure 53.18 NMI中断输入时序

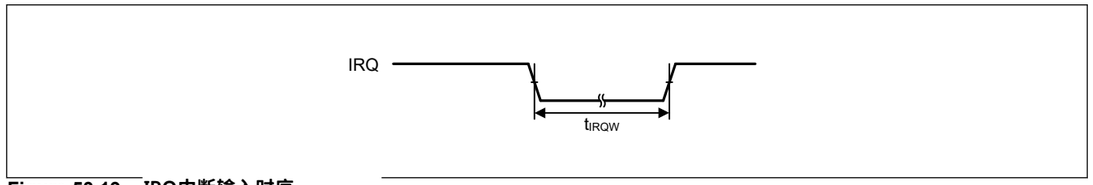


Figure 53.19 IRQ中断输入时序

53.3.6 巴士时间

Table 53.22 公交车计时

Condition:
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF。
EBCLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。其他：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter	Symbol	Min	Max	Unit	测试条件
地址延迟	t_{AD}	—	12.5	ns	图53.22至 Figure 53.25
字节控制延迟	t_{BCD}	—	12.5	ns	
CS delay	t_{CSD}	—	12.5	ns	
ALE延迟时间	t_{ALED}	—	12.5	ns	
RD delay	t_{RSD}	—	12.5	ns	
读取数据建立时间	t_{RDS}	12.5	—	ns	
读取数据保持时间	t_{RDH}	0	—	ns	
WR/WRn delay	t_{WRD}	—	12.5	ns	
写数据延迟	t_{WDD}	—	12.5	ns	
写数据保持时间	t_{WDH}	0	—	ns	
等待设置时间	t_{WTS}	12.5	—	ns	Figure 53.26
WAIT保持时间	t_{WTH}	0	—	ns	

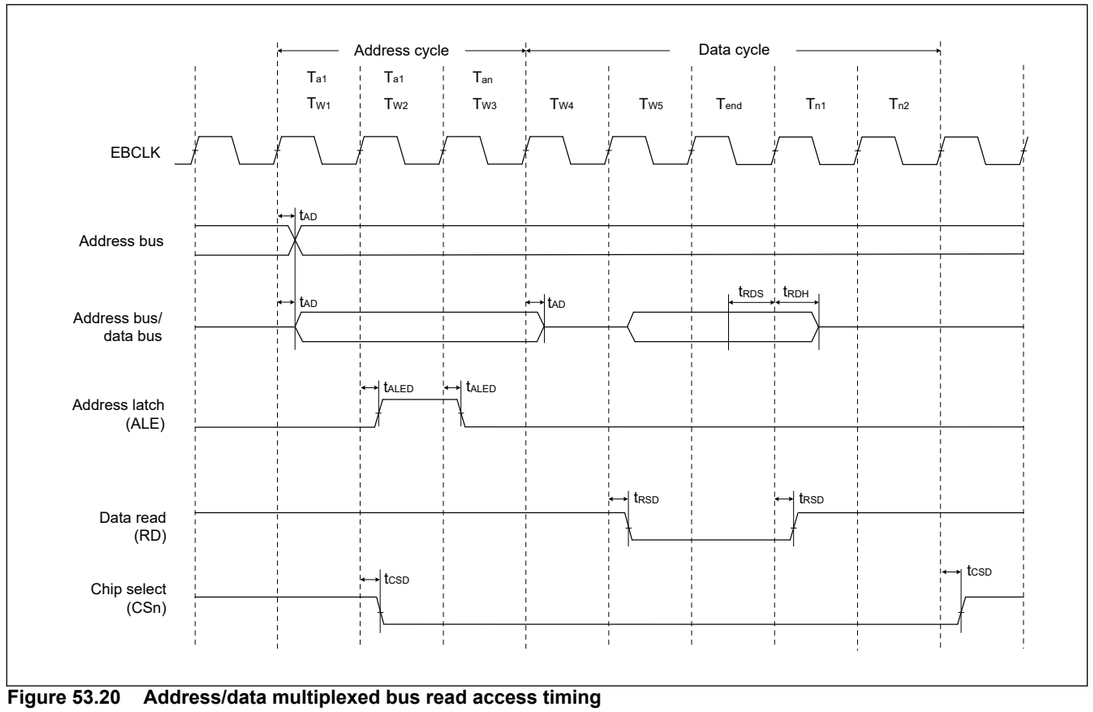


Figure 53.20 Address/data multiplexed bus read access timing

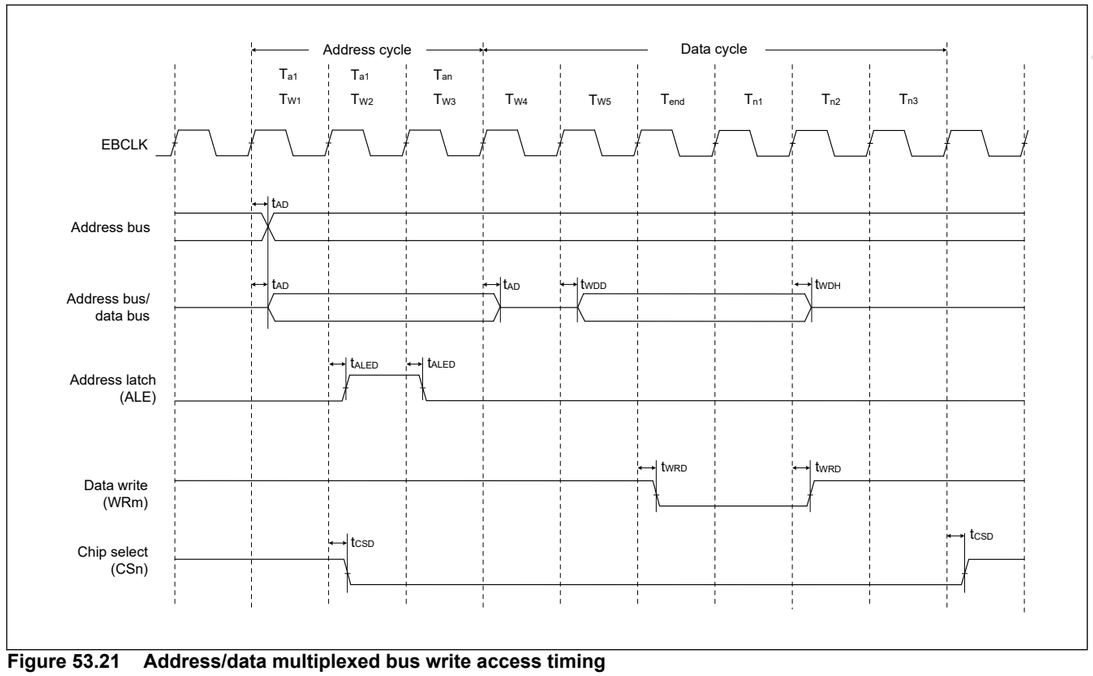


Figure 53.21 Address/data multiplexed bus write access timing

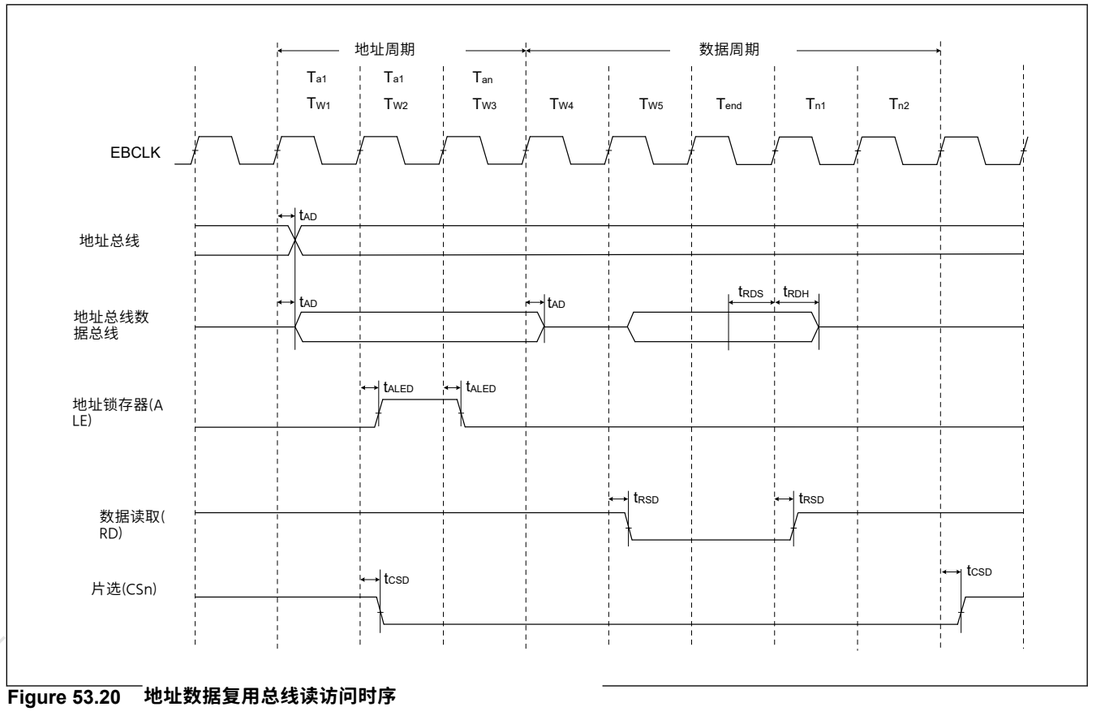


Figure 53.20 地址数据复用总线读访问时序

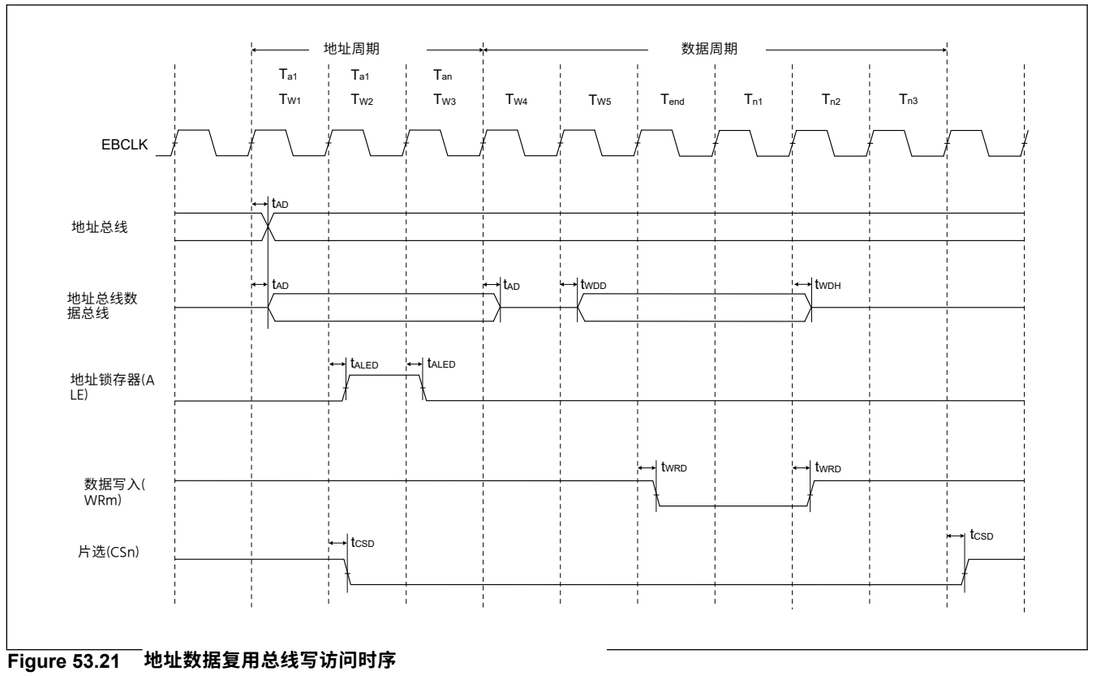


Figure 53.21 地址数据复用总线写访问时序

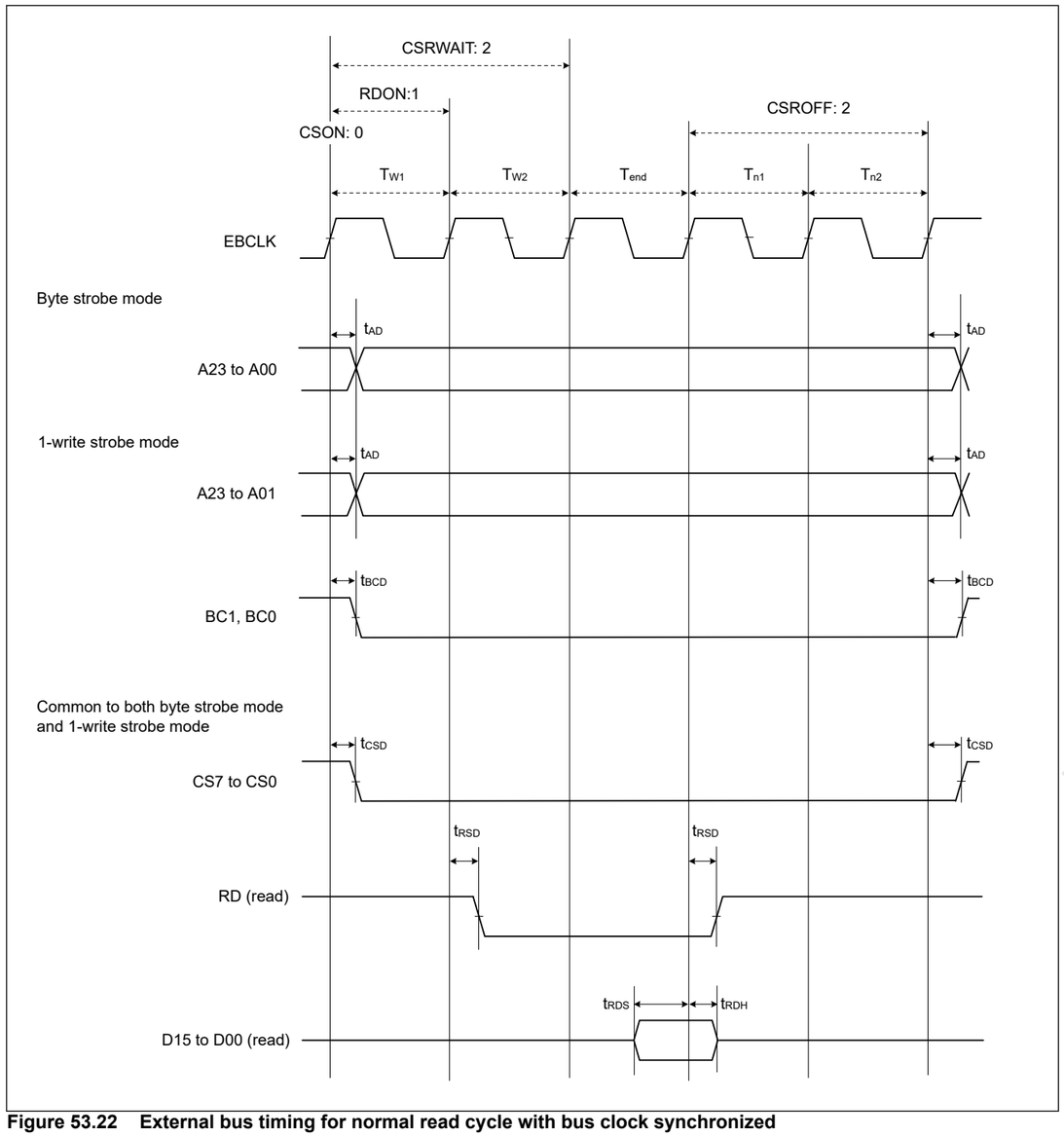


Figure 53.22 External bus timing for normal read cycle with bus clock synchronized

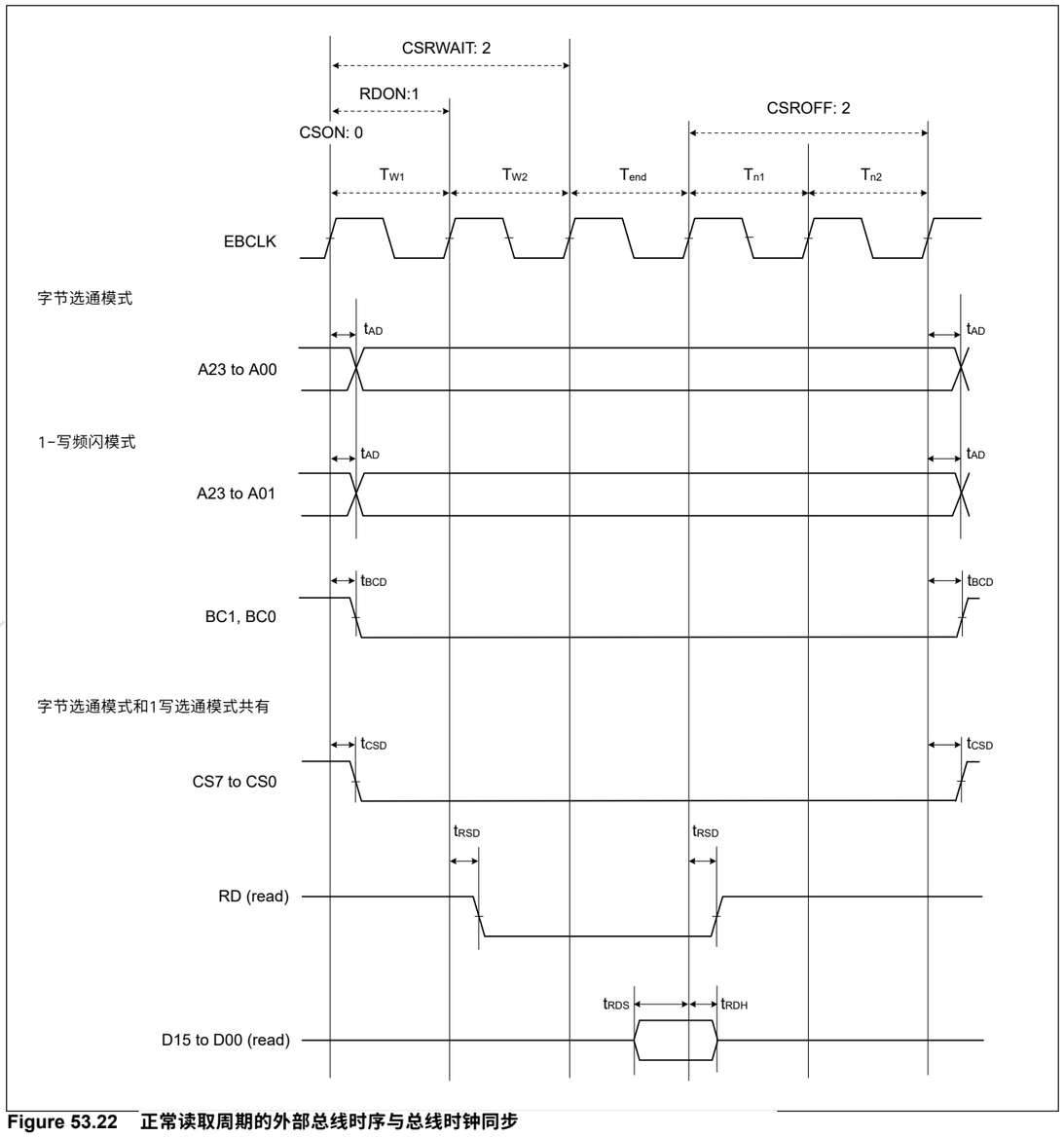


Figure 53.22 正常读取周期的外部总线时序与总线时钟同步

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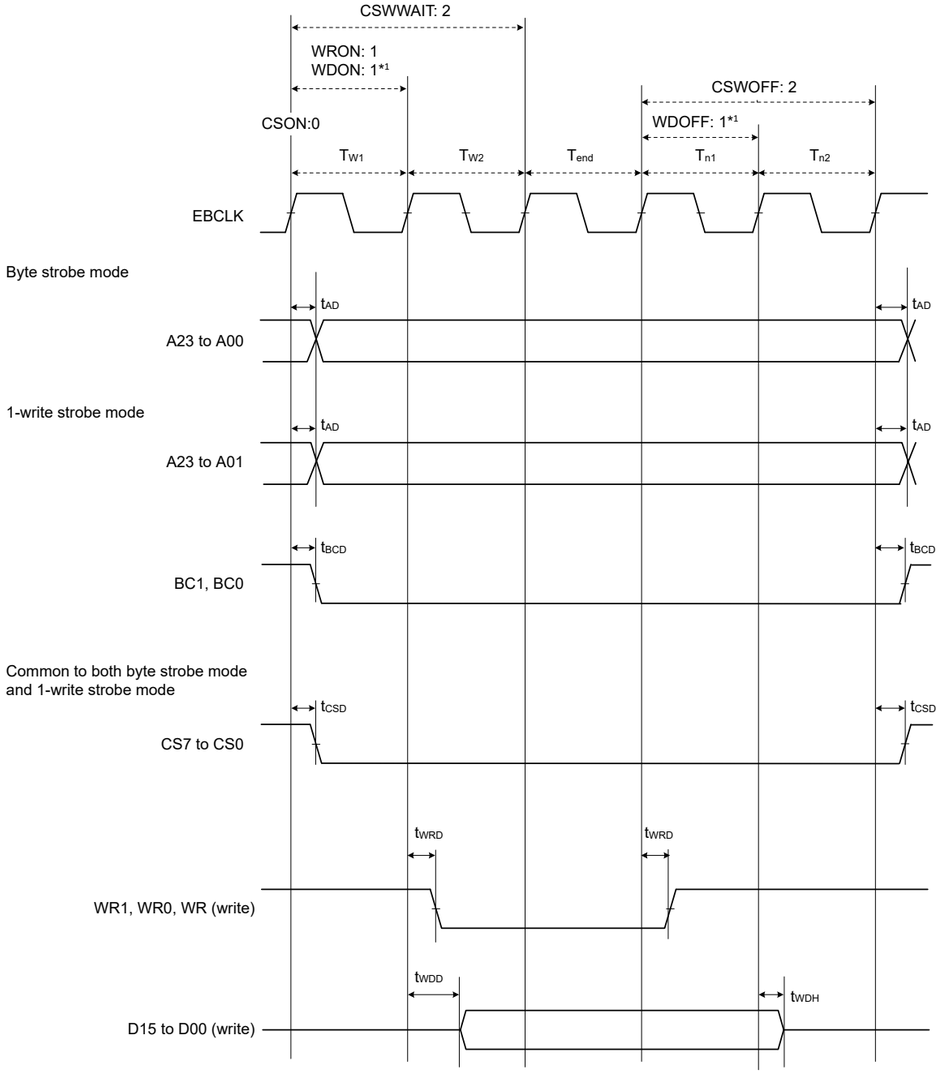
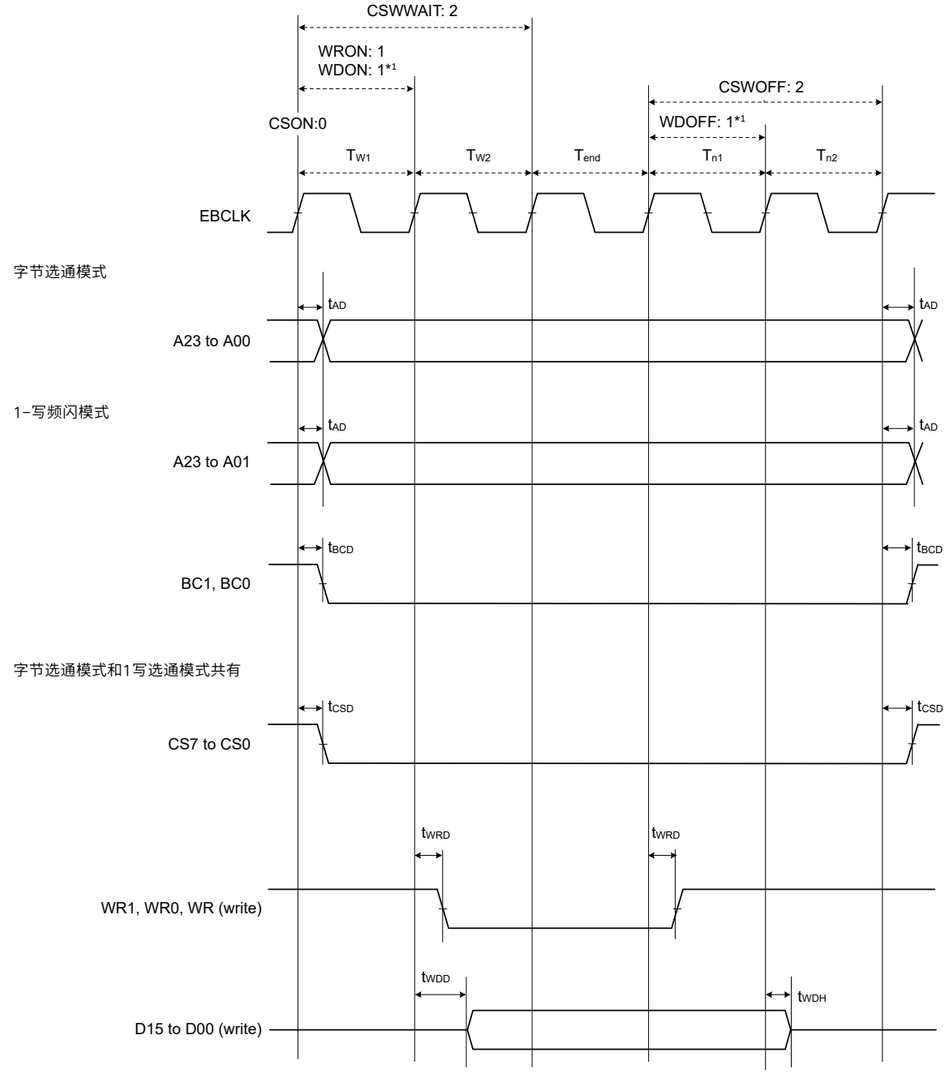


Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 53.23 External bus timing for normal write cycle with bus clock synchronized



注1.始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 53.23 与总线时钟同步的正常写周期的外部总线时序

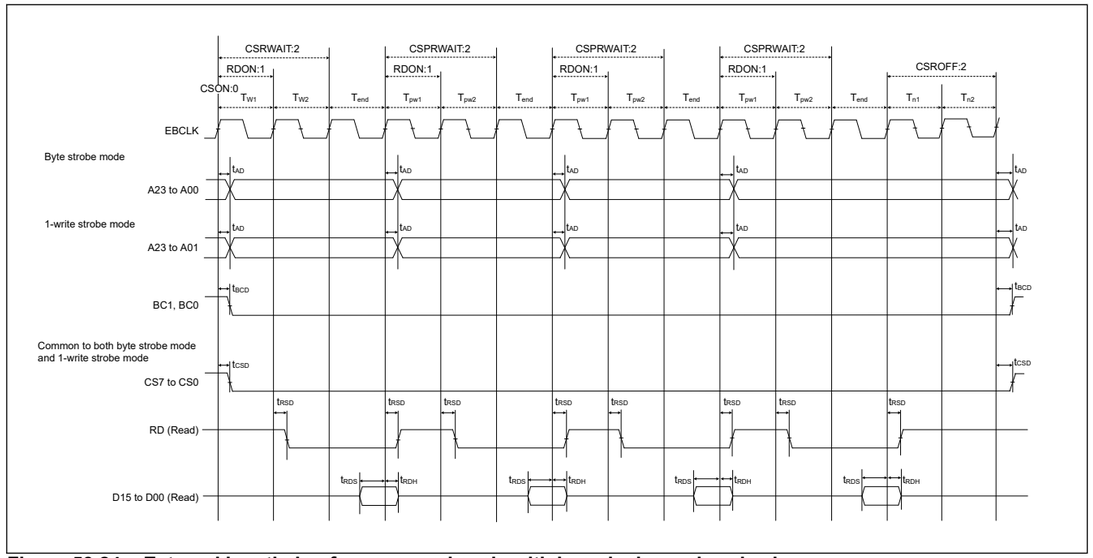
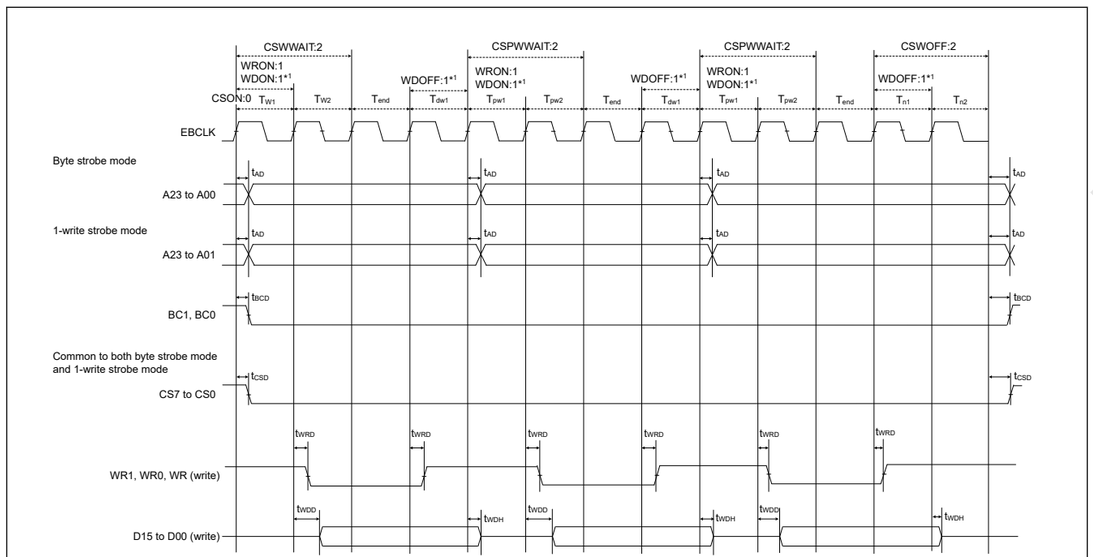


Figure 53.24 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 53.25 External bus timing for page write cycle with bus clock synchronized

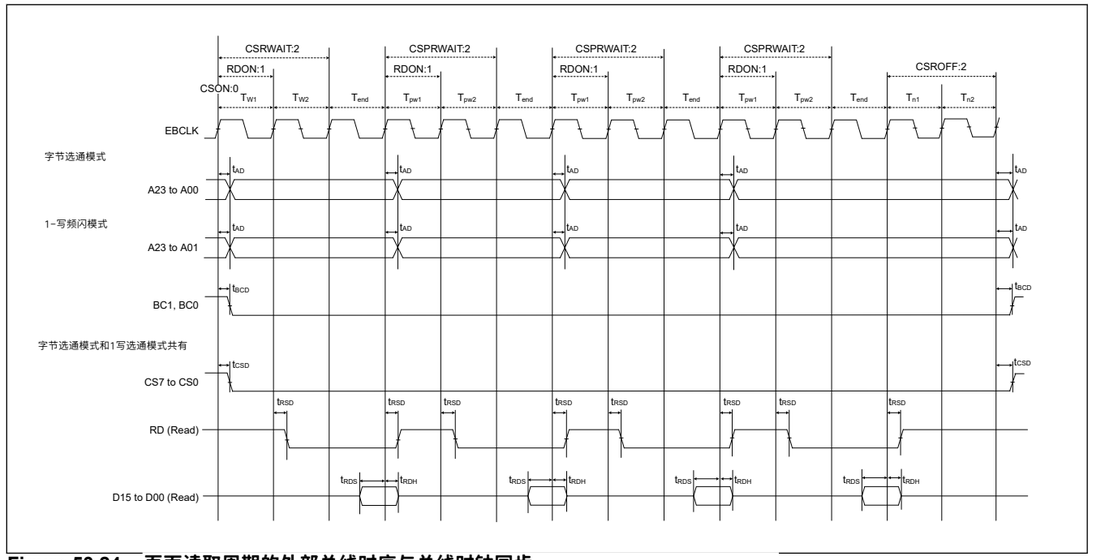
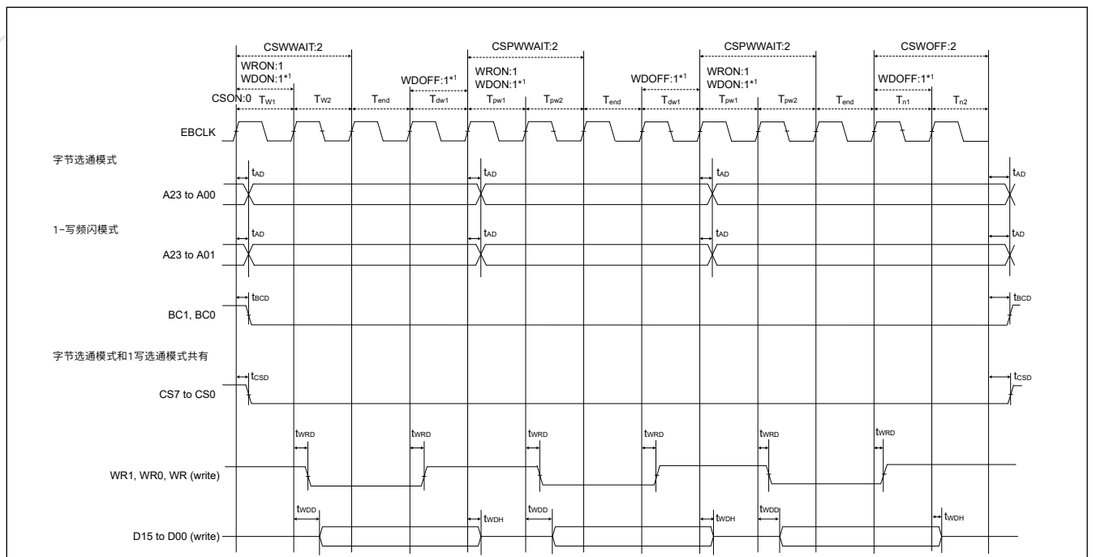


Figure 53.24 页面读取周期的外部总线时序与总线时钟同步



注1.始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 53.25 页面写入周期的外部总线时序与总线时钟同步

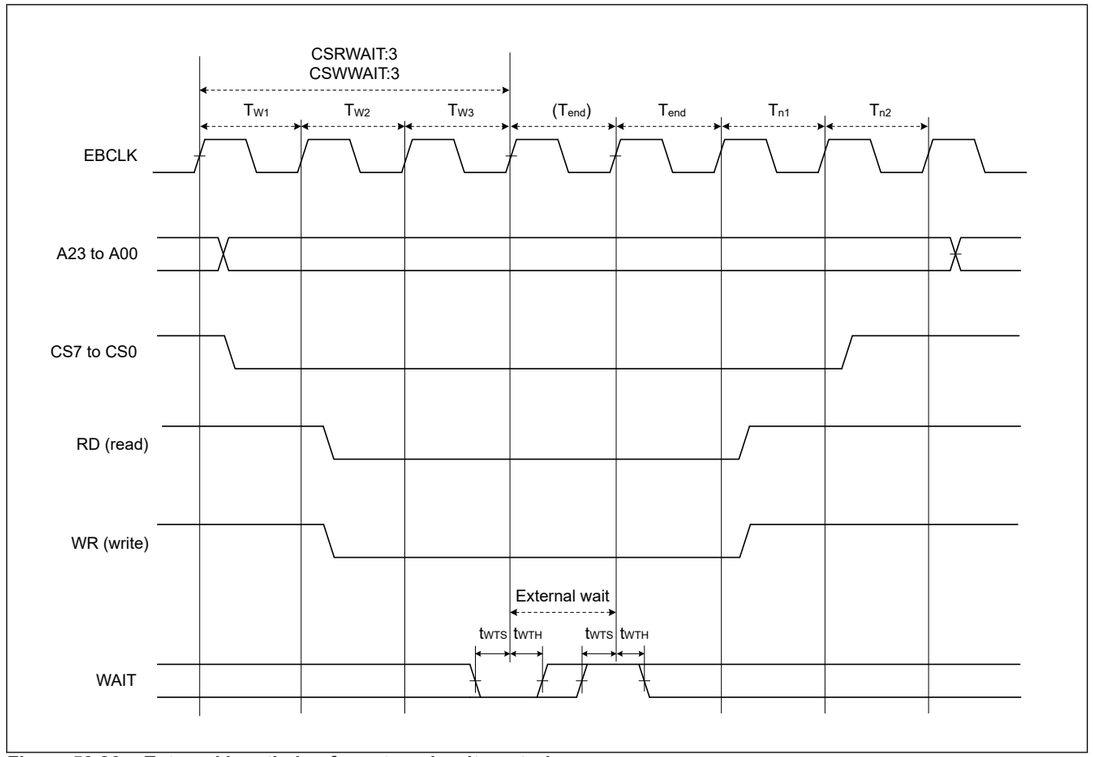


Figure 53.26 External bus timing for external wait control

53.3.7 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 53.23 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing (1 of 2)

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 53.27
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 53.28
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 53.29
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer	t_{GTISK}*1	—	4	ns	Figure 53.30
		High drive buffer		—	4		
	GTIOCxY output skew (x = 4 to 9, Y = A or B)	Middle drive buffer		—	4		
		High drive buffer		—	4		
	GTIOCxY output skew (x = 0 to 9, Y = A or B)	Middle drive buffer		—	6		
		High drive buffer		—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 53.31

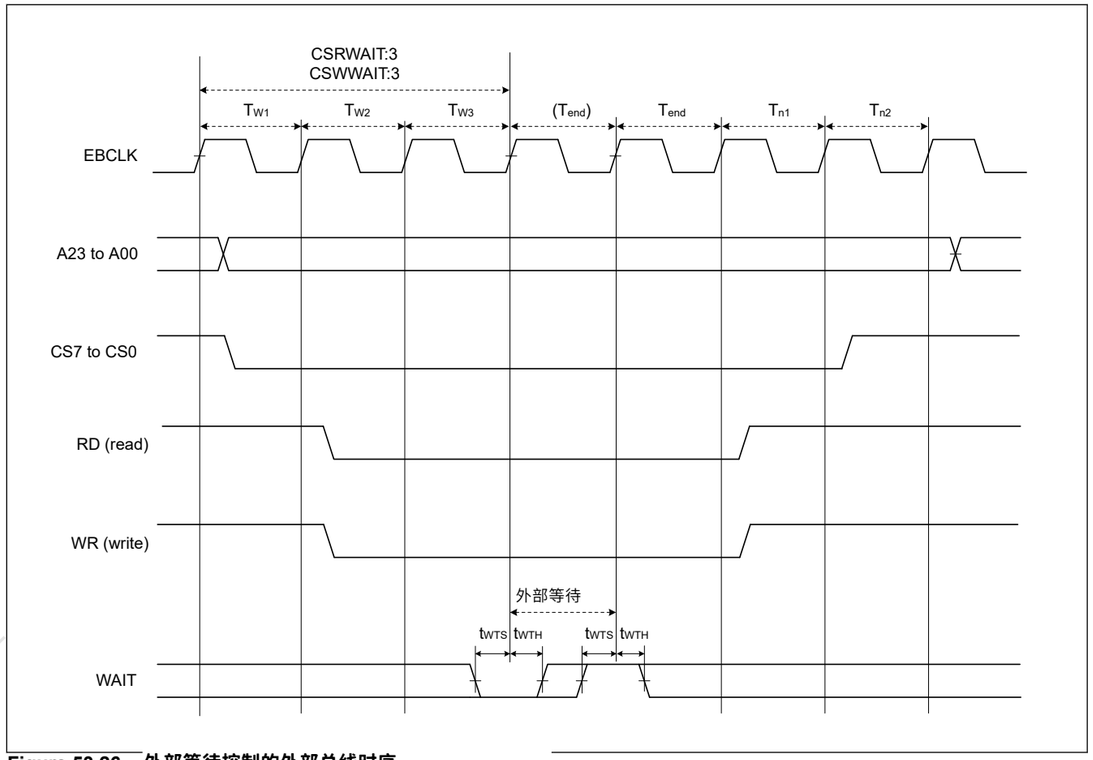


Figure 53.26 外部等待控制的外部总线时序

53.3.7 IO端口、POEG、GPT、AGT和ADC12触发时序

Table 53.23 IO端口、POEG、GPT、AGT和ADC12触发时序（1of2）

GPT32 Conditions:
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
AGT Conditions:
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度		t_{PRW}	1.5	—	t_{Pcyc}	Figure 53.27
POEG	POEG输入触发脉冲宽度		t_{POEW}	3	—	t_{Pcyc}	Figure 53.28
GPT	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 53.29
		双刃		2.5	—		
	GTIOCxY输出偏差（x=0到3，Y=A或B）	中间驱动缓冲器	t_{GTISK}*1	—	4	ns	Figure 53.30
		高驱动缓冲器		—	4		
	GTIOCxY输出偏差（x=4到9，Y=A或B）	中间驱动缓冲器		—	4		
		高驱动缓冲器		—	4		
	GTIOCxY输出偏移（x=0到9，Y=A或B）	中间驱动缓冲器		—	6		
		高驱动缓冲器		—	6		
	OPS输出偏差 GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 53.31

Table 53.23 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing (2 of 2)

GPT32 Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
AGT	AGTIO, AGTEE input cycle	t_{ACYC}*2	100	—	ns	Figure 53.32
	AGTIO, AGTEE input high width, low width	t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	t_{ACYC2}	62.5	—	ns	
ADC12	ADC12 trigger input pulse width	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 53.33

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

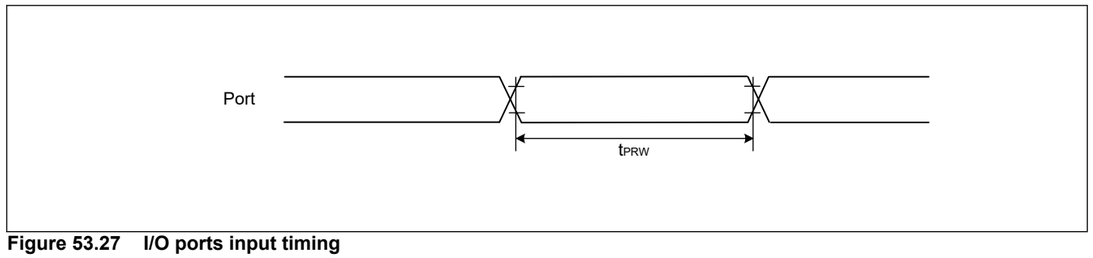


Figure 53.27 I/O ports input timing

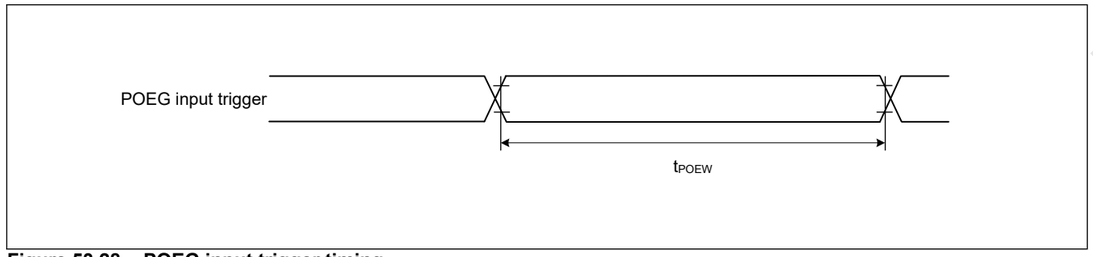


Figure 53.28 POEG input trigger timing

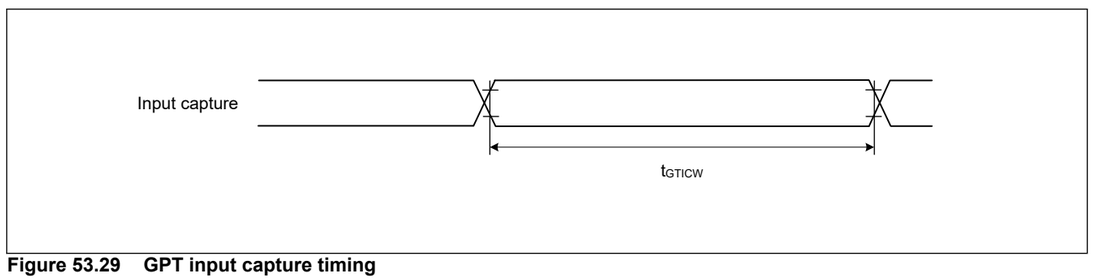


Figure 53.29 GPT input capture timing

Table 53.23 IO端口、POEG、GPT、AGT和ADC12触发时序（2个中的2个）

GPT32 Conditions:
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
AGT Conditions:
在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
AGT	AGTIO、AGTEE输入周期	t_{ACYC}*2	100	—	ns	Figure 53.32
	AGTIO、AGTEE输入高宽、低宽	t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO、AGTO、AGTOA、AGTOB输出周期	t_{ACYC2}	62.5	—	ns	
ADC12	ADC12触发输入脉冲宽度	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 53.33

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
注1.当使用相同的驱动器IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。
注2.输入周期的限制：
不切换源时钟时：tPcyc×2<tACYC应满足。
切换源时钟时：tPcyc×6<tACYC应满足。

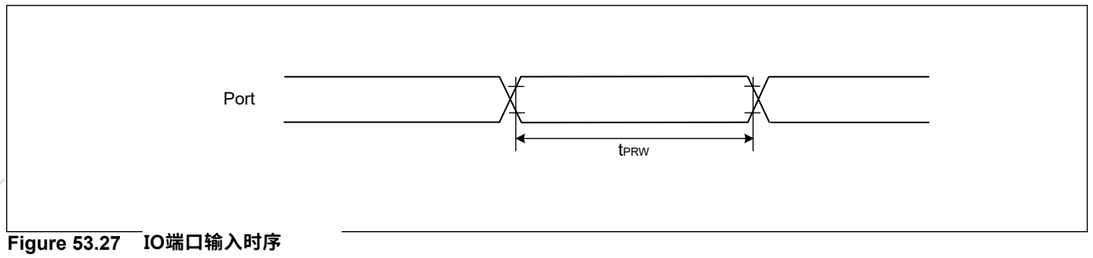


Figure 53.27 IO端口输入时序

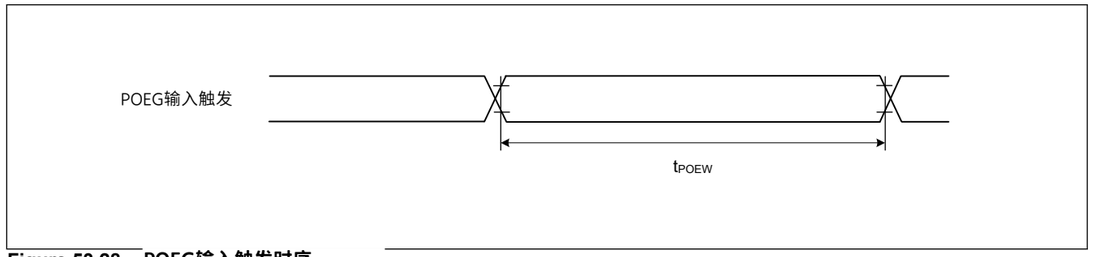


Figure 53.28 POEG输入触发时序

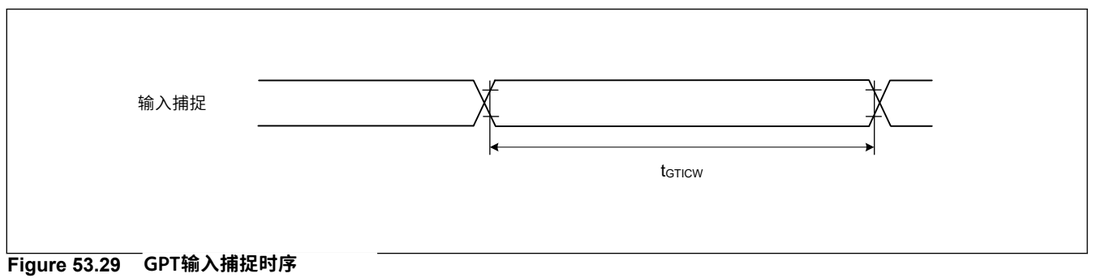


Figure 53.29 GPT输入捕捉时序

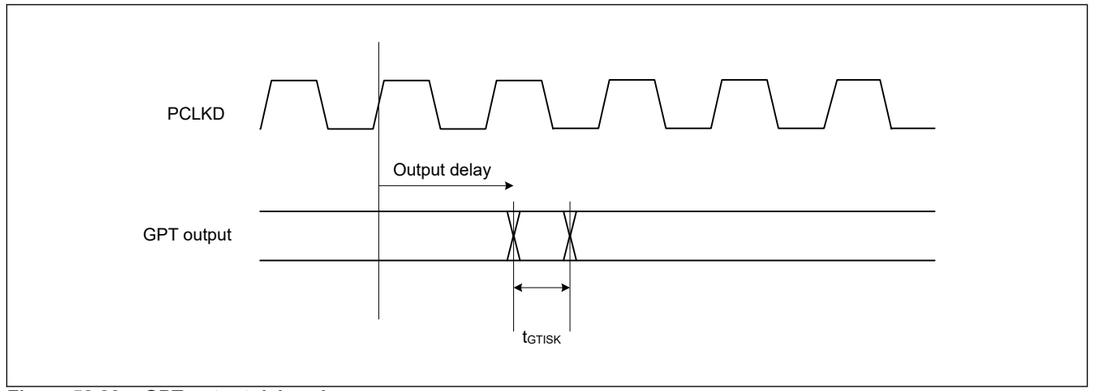


Figure 53.30 GPT output delay skew

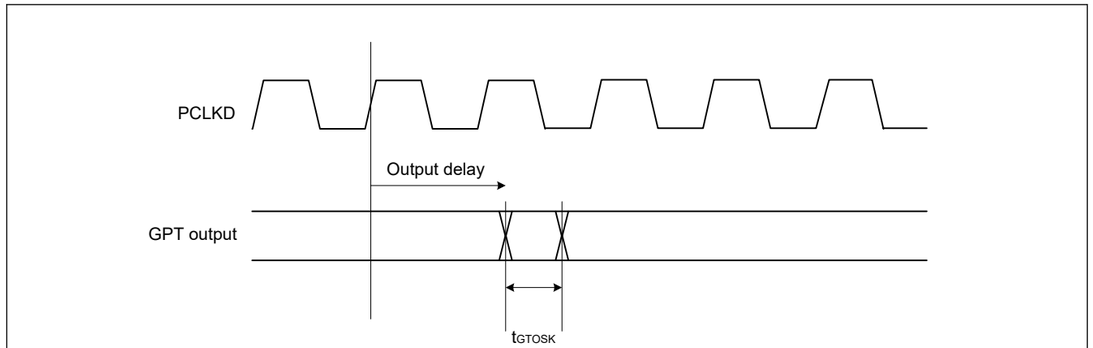


Figure 53.31 GPT output delay skew for OPS

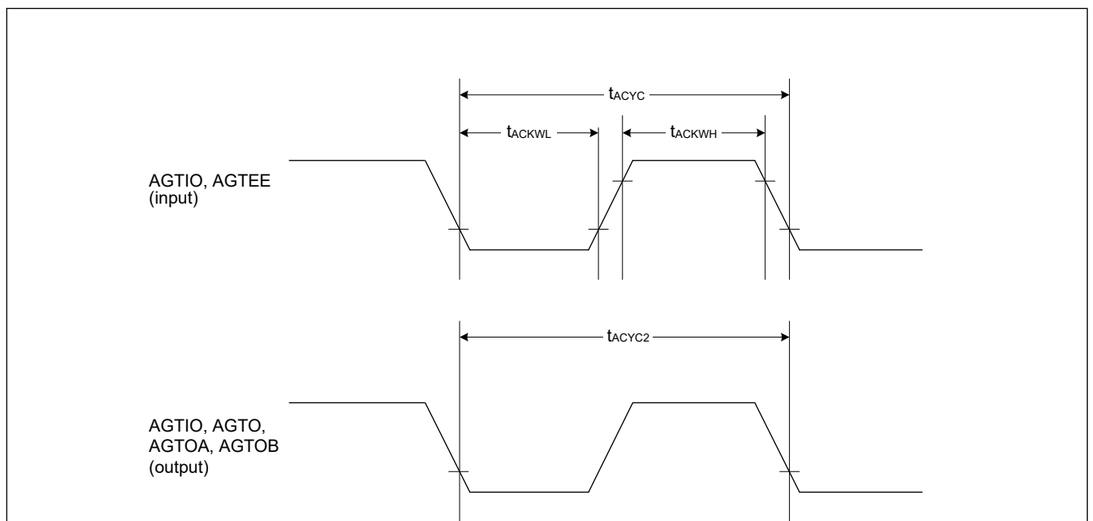


Figure 53.32 AGT input/output timing

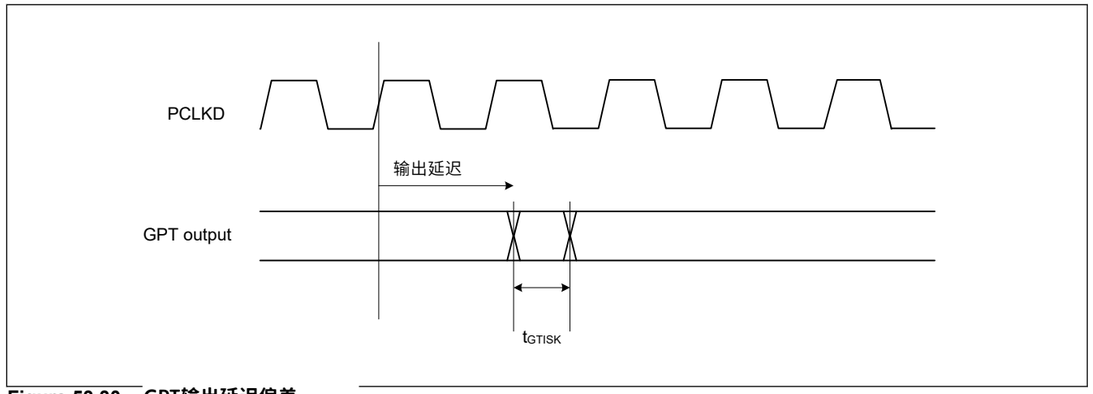


Figure 53.30 GPT输出延迟偏差

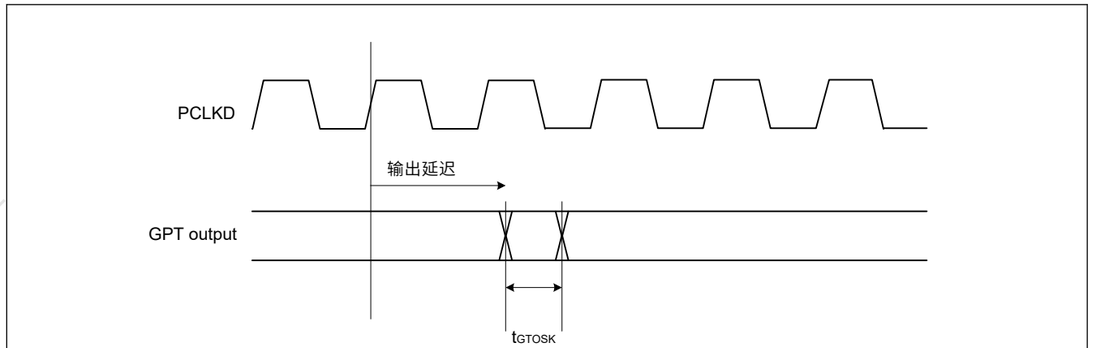


Figure 53.31 OPS的GPT输出延迟偏差

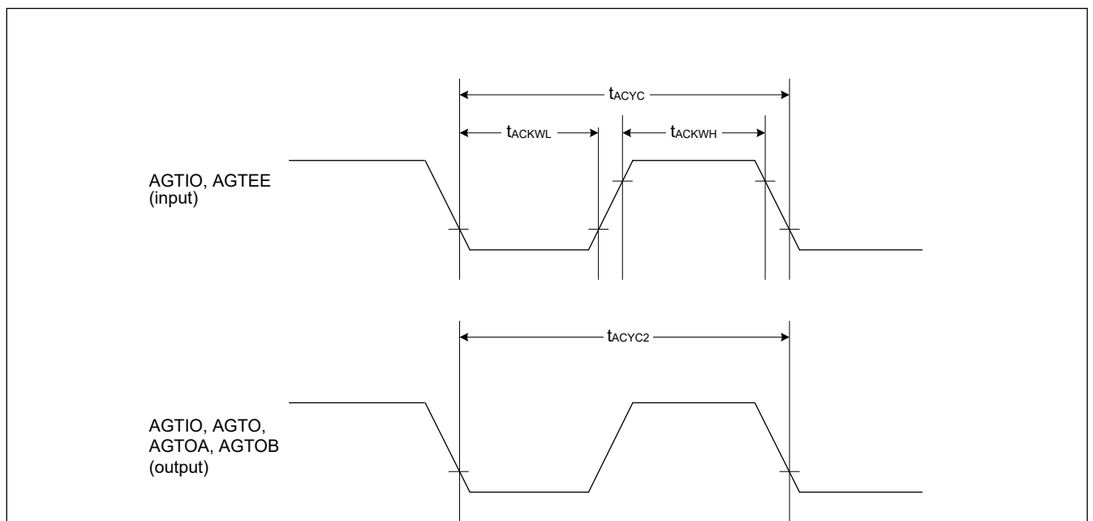


Figure 53.32 AGT input/output timing

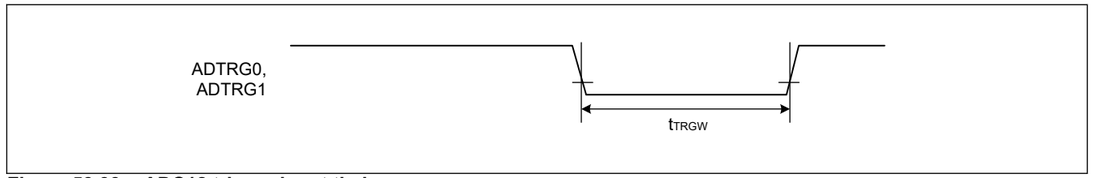


Figure 53.33 ADC12 trigger input timing

53.3.8 CAC Timing

Table 53.24 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$*1	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}	—	—	ns	—
		$t_{PBcyc} > t_{cac}$*1		5 × t_{cac} + 6.5 × t_{PBcyc}	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

53.3.9 SCI Timing

Table 53.25 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 53.34
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6 (other than SCI1, SCI2) 8 (SCI1, SCI2)	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay	Clock synchronous master mode (internal clock)	t_{TXD}	—	5	ns	Figure 53.35
		Clock synchronous slave mode (external clock)	t_{TXD}	—	25	ns	
	Receive data setup time	Clock synchronous master mode (internal clock)	t_{RXS}	15	—	ns	
		Clock synchronous slave mode (external clock)	t_{RXS}	5	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.

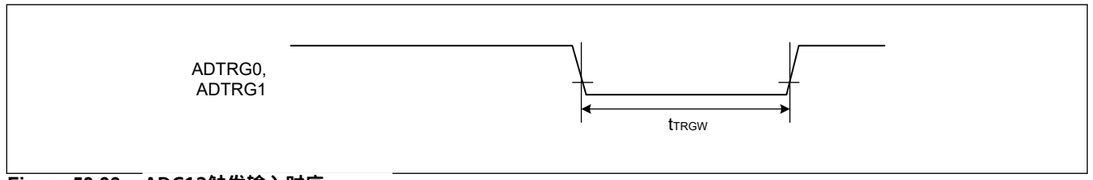


Figure 53.33 ADC12触发输入时序

53.3.8 CAC时序

Table 53.24 CAC计时

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	$t_{PBcyc} \le t_{cac}$*1	t_{CACREF}	4.5 × t_{cac} + 3 × t_{PBcyc}	—	—	ns	—
		$t_{PBcyc} > t_{cac}$*1		5 × t_{cac} + 6.5 × t_{PBcyc}	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
注1.tcac：CAC计数时钟源周期。

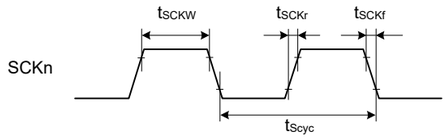
53.3.9 SCI时序

Table 53.25 SCI时序（1）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

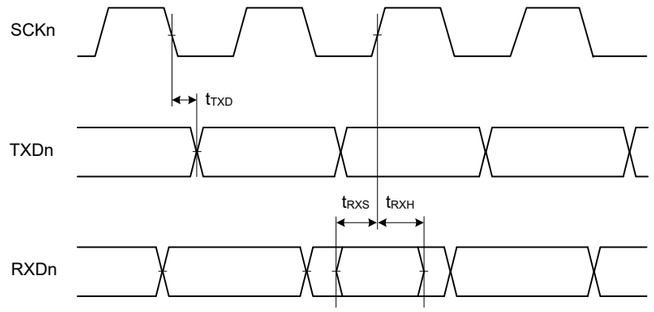
Parameter			符号	最小值	最大	单位	测试条件
SCI输入时钟周期		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 53.34
		时钟同步		6	—		
	输入时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间		t_{SCKr}	—	5	ns	
	输入时钟下降时间		t_{SCKf}	—	5	ns	
	输出时钟周期	Asynchronous	t_{Scyc}	6 (other than SCI1, SCI2) 8 (SCI1, SCI2)	—	t_{Pcyc}	
		时钟同步		4	—		
	输出时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		t_{SCKr}	—	5	ns	
	输出时钟下降时间		t_{SCKf}	—	5	ns	
	传输数据延迟	时钟同步主模式（内部时钟）	t_{TXD}	—	5	ns	Figure 53.35
		时钟同步从机模式（外部时钟）	t_{TXD}	—	25	ns	
	接收数据建立时间时钟同步主模式（内部时钟）		t_{RXS}	15	—	ns	
		时钟同步从机模式（外部时钟）	t_{RXS}	5	—	ns	
	接收数据保持时间	时钟同步	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.



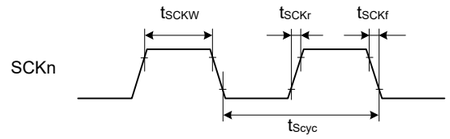
Note: n = 0 to 9

Figure 53.34 SCK clock input/output timing



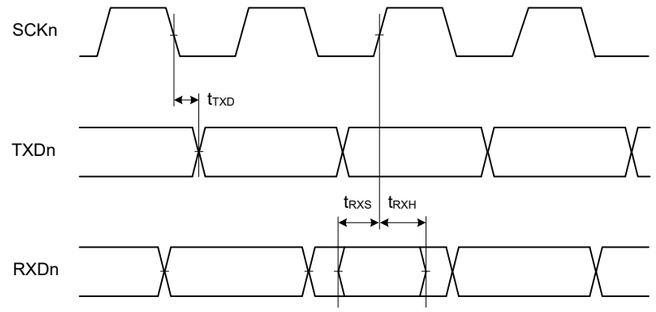
Note: n = 0 to 9

Figure 53.35 SCI input/output timing in clock synchronous mode



Note: n = 0 to 9

Figure 53.34 SCK时钟输入输出时序



Note: n = 0 to 9

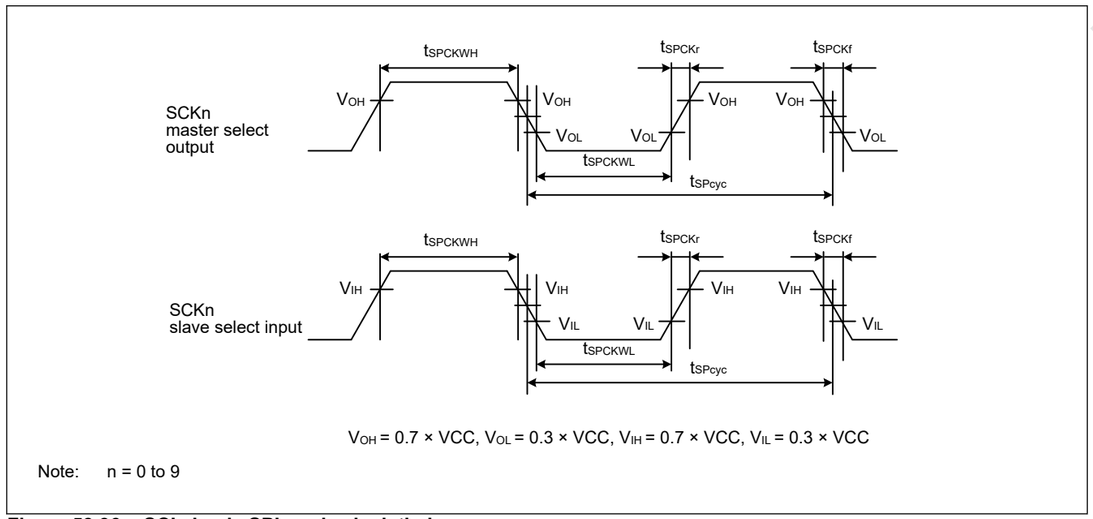
Figure 53.35 时钟同步模式下的SCI输入输出时序

Table 53.26 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 53.36
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Data input setup time	master	t_{SU}	15	—	ns	Figure 53.37 to Figure 53.40
		slave		5	—	ns	
	Data input hold time		t_{H}	5	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	Data output hold time		t_{OH}	-5	—	ns	
	Data rise and fall time		t_{Dr}, t_{Df}	—	5	ns	
	SS input rise and fall time		t_{SSLr}, t_{SSLf}	—	5	ns	
	Slave access time		t_{SA}	—	3 × t_{Pcyc} + 25	ns	Figure 53.40
	Slave output release time		t_{REL}	—	3 × t_{Pcyc} + 25	ns	

Note: t_{Pcyc}: PCLKA cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = 0 to 9

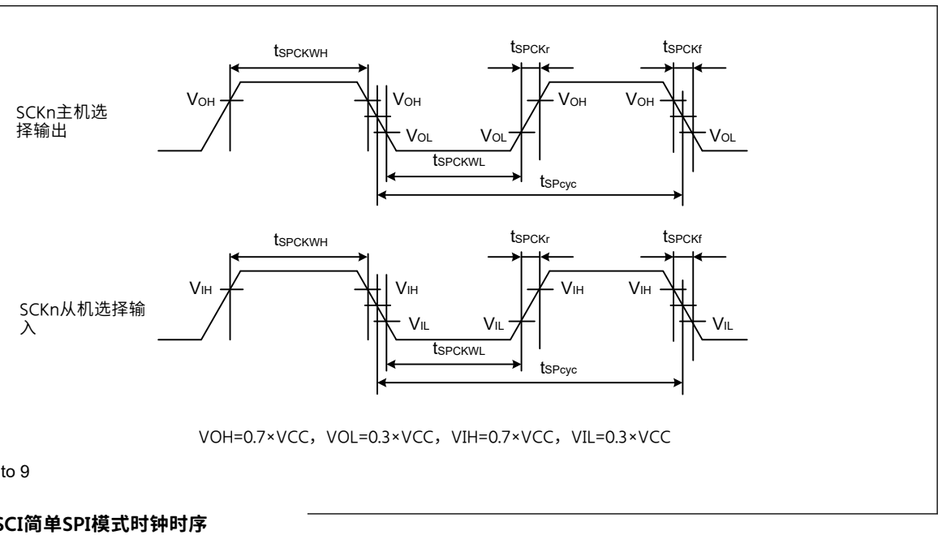
Figure 53.36 SCI simple SPI mode clock timing

Table 53.26 SCI时序（2）

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter			Symbol	Min	Max	Unit	测试条件
简单的SPI	SCK时钟周期输出（主机）		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 53.36
	SCK时钟周期输入（从机）			6	65536		
	SCK时钟高脉冲宽度		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	数据输入建立时间	master	t_{SU}	15	—	ns	图53.37至图53.40
		slave		5	—	ns	
	数据输入保持时间		t_{H}	5	—	ns	
	SS输入建立时间		t_{LEAD}	1	—	t_{SPcyc}	
	SS输入保持时间		t_{LAG}	1	—	t_{SPcyc}	
	数据输出延迟	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	数据输出保持时间		t_{OH}	-5	—	ns	
	数据上升和下降时间		t_{Dr}, t_{Df}	—	5	ns	
	SS输入上升和下降时间		t_{SSLr}, t_{SSLf}	—	5	ns	
	从站访问时间		t_{SA}	—	3 × t_{Pcyc} + 25	ns	Figure 53.40
	从机输出释放时间		t_{REL}	—	3 × t_{Pcyc} + 25	ns	

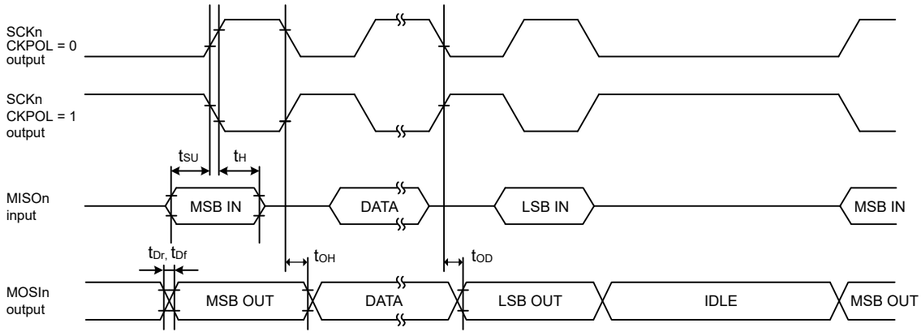
Note: t_{Pcyc}: PCLKA cycle.



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

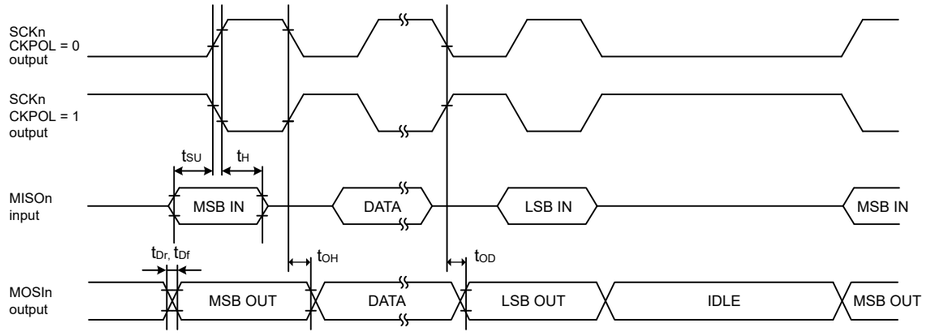
Note: n = 0 to 9

Figure 53.36 SCI简单SPI模式时钟时序



Note: n = 0 to 9

Figure 53.37 SCI simple SPI mode timing for master when CKPH = 1



Note: n = 0 to 9

Figure 53.37 CKPH=1时主机的SCI简单SPI模式时序

Note: n = 0 to 9

Figure 53.38 SCI simple SPI mode timing for master when CKPH = 0

Note: n = 0 to 9

Figure 53.38 CKPH=0时主机的SCI简单SPI模式时序

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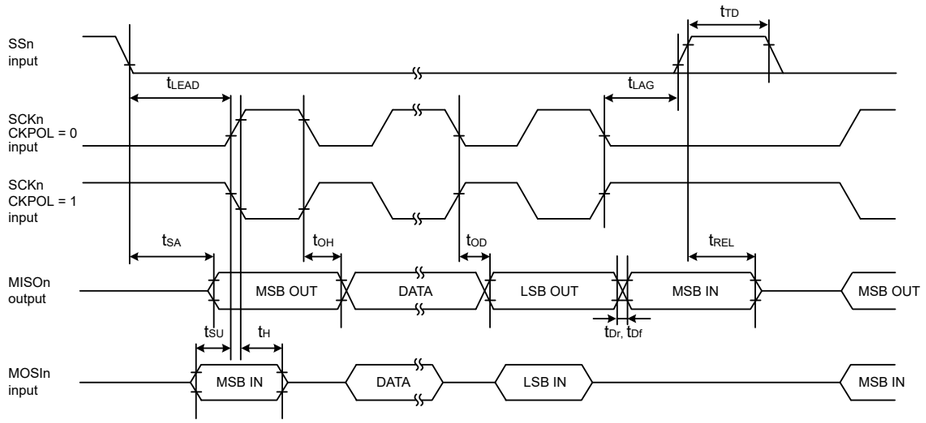
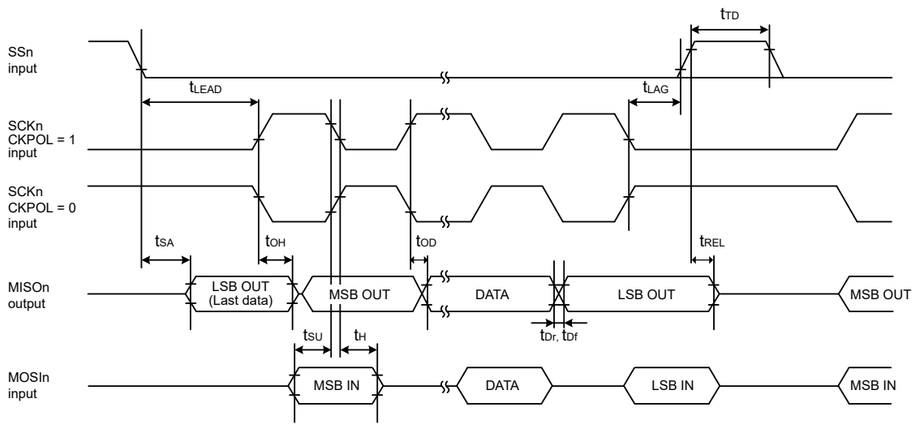


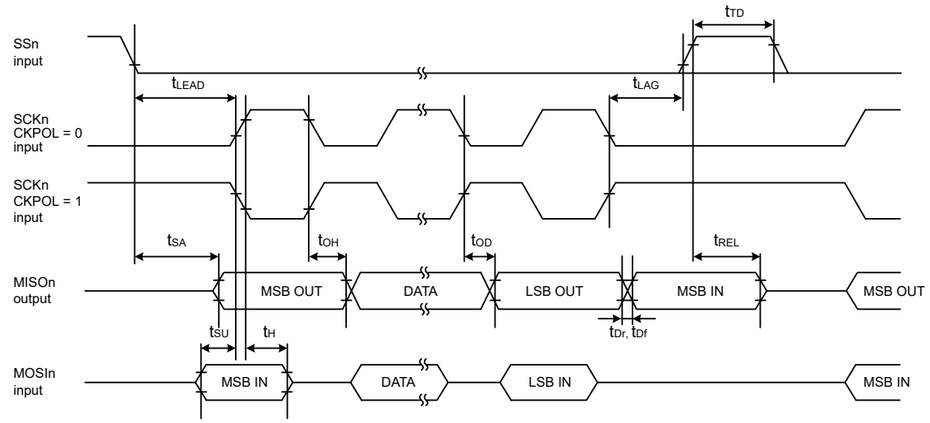
Note: n = 0 to 9

Figure 53.39 SCI simple SPI mode timing for slave when CKPH = 1



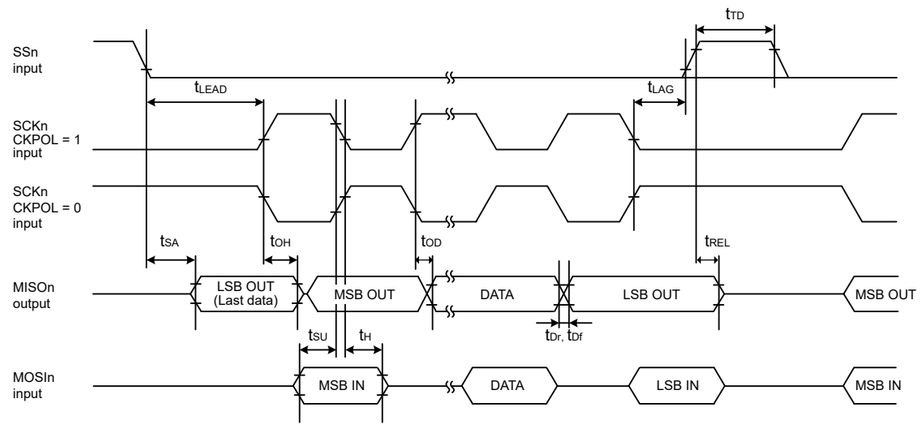
Note: n = 0 to 9

Figure 53.40 SCI simple SPI mode timing for slave when CKPH = 0



Note: n = 0 to 9

Figure 53.39 CKPH=1时从机的SCI简单SPI模式时序



Note: n = 0 to 9

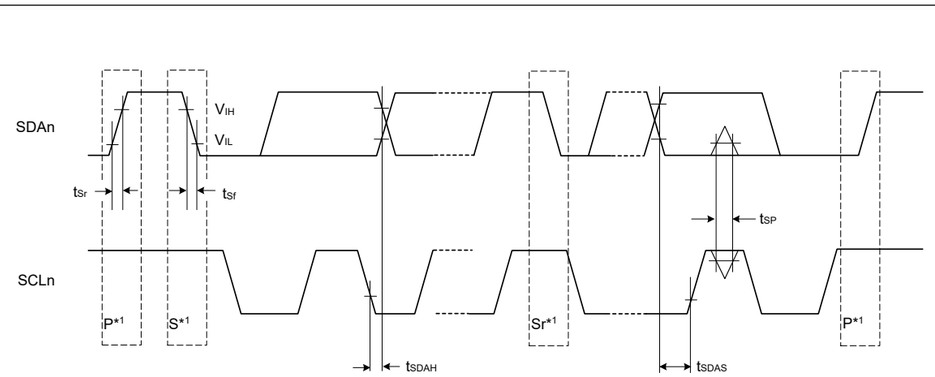
Figure 53.40 CKPH=0时从机的SCI简单SPI模式时序

Table 53.27 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 53.41
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 53.41
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

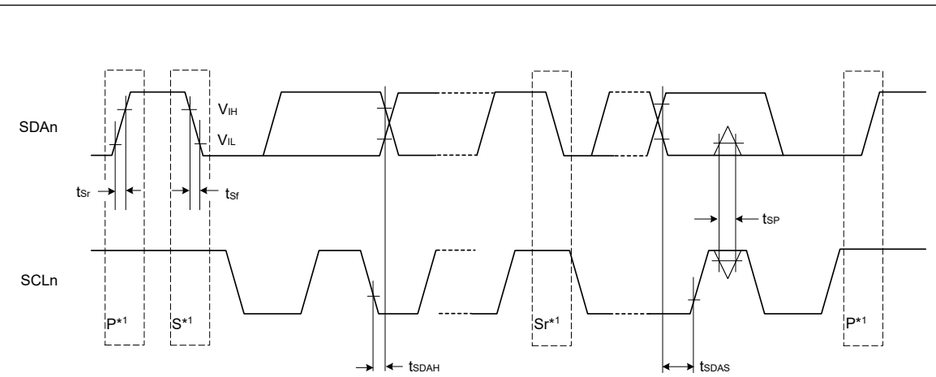
Figure 53.41 SCI simple IIC mode timing

Table 53.27 SCI时序（3）

条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	—	1000	ns	Figure 53.41
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	250	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	—	300	ns	Figure 53.41
	SDA输入下降时间	t_{Sf}	—	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	100	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
注1.Cb表示公交线路的总容量。



Test conditions:
VIH=VCC×0.7，VIL=VCC×0.3
VOL=0.6V，IOL=6mA

Note: n = 0 to 9
注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 53.41 SCI简单IIC模式时序

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53.3.10 SPI Timing

Table 53.28 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 53.42
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	µs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 53.43 to Figure 53.48
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	—		
		Slave	t_H	20	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc}$ - 10*1	$N \times t_{SPcyc}$ + 100*1	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc}$ - 10*2	$N \times t_{SPcyc}$ + 100*2	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	25	ns	Figure 53.47 and Figure 53.48
	Slave output release time		t_{REL}	—	25		

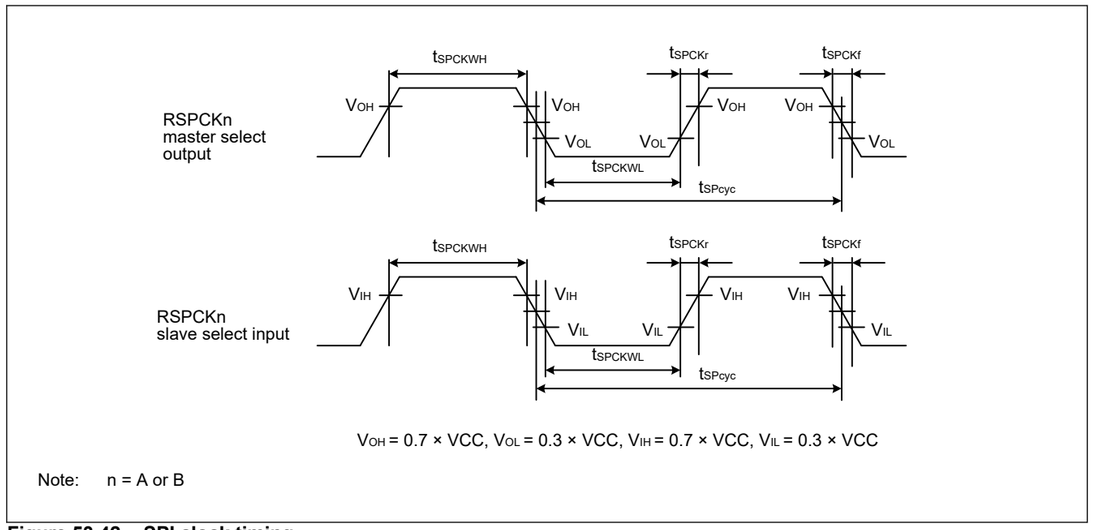
53.3.10 SPI时序

Table 53.28 SPI时序

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter			Symbol	Min	Max	Unit	测试条件
SPI	RSPCK时钟周期	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 53.42
		Slave		4	4096		
	RSPCK时钟高脉冲宽度	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK时钟低脉冲宽度	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK时钟上升和下降时间	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	µs	
	数据输入建立时间	Master	t_{SU}	4	—	ns	图53.43至图53.48
		Slave		5	—		
	数据输入保持时间	主控（PCLKA分频比设置为12）	t_{HF}	0	—	ns	
		主控（PCLKA分频比设置为12以外的值）	t_H	t_{Pcyc}	—		
		Slave	t_H	20	—		
	SSL设置时间	Master	t_{LEAD}	$N \times t_{SPcyc}$ - 10*1	$N \times t_{SPcyc}$ + 100*1	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	SSL保持时间	Master	t_{LAG}	$N \times t_{SPcyc}$ - 10*2	$N \times t_{SPcyc}$ + 100*2	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	数据输出延迟	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	数据输出保持时间	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	连续传输延迟	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$			
	MOSI和MISO上升和下降时间	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL上升和下降时间	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	从站访问时间		t_{SA}	—	25	ns	图53.47和 Figure 53.48
	从机输出释放时间		t_{REL}	—	25		

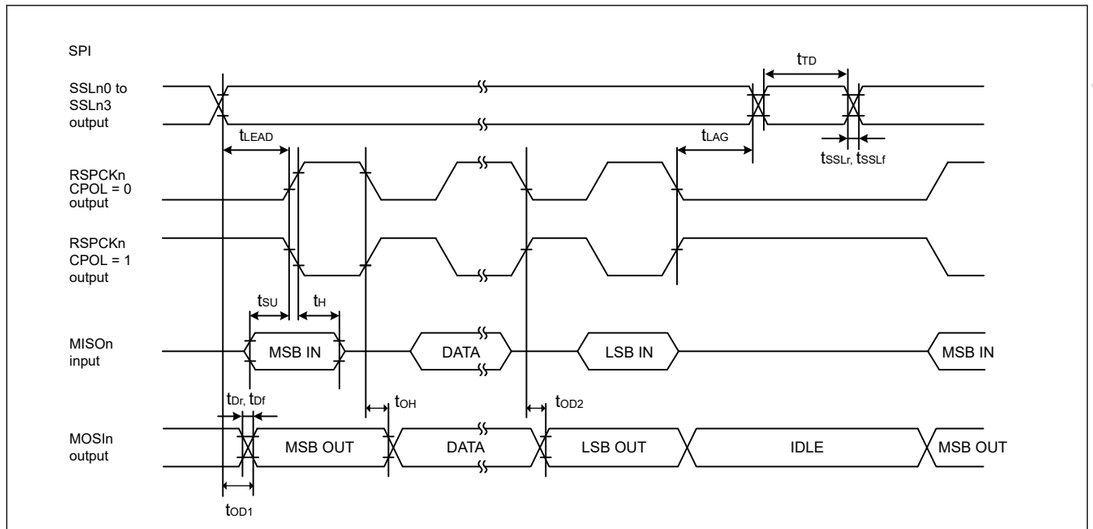
Note: t_{Pcyc}: PCLKA cycle.
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A or B

Figure 53.42 SPI clock timing

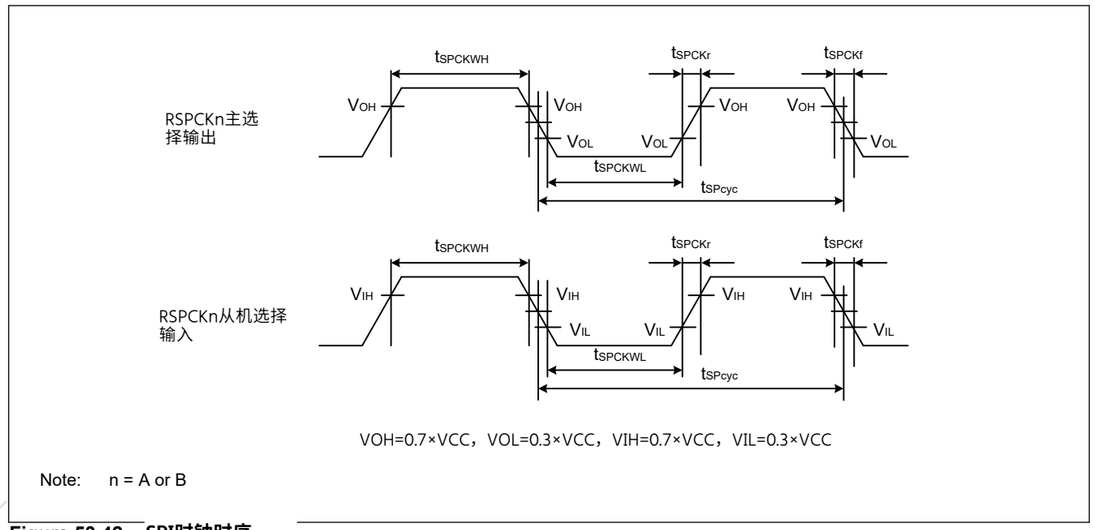


Note: n = A or B

Figure 53.43 SPI timing for master when CPHA = 0

Note: t_{Pcyc}: PCLKA cycle.
Note: 必须使用名称后附有字母的引脚，例如_A、_B，以表明组成员身份。对于SPI接口，测量每组的电气特性的交流部分。

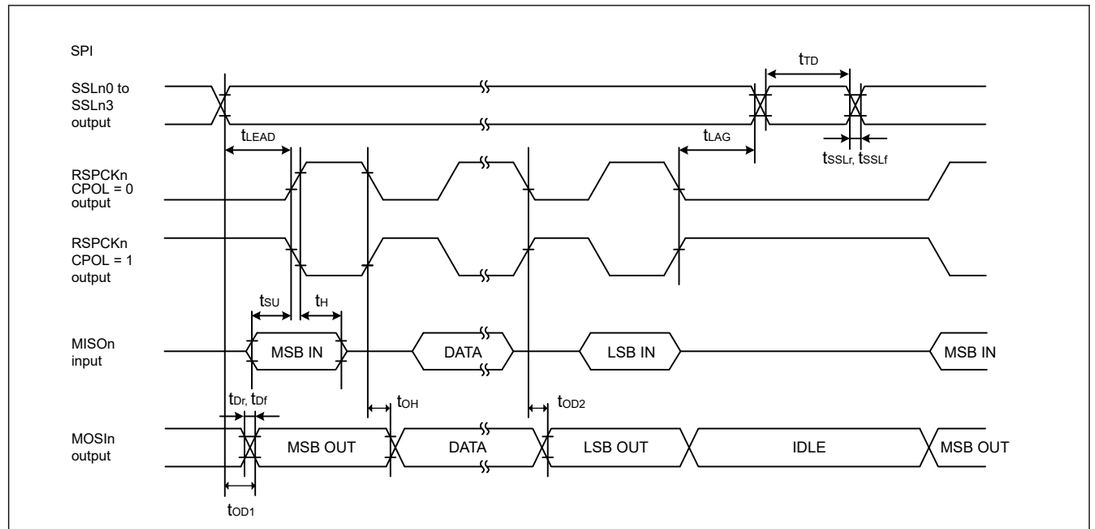
注1.N由SPCKD寄存器设置为1到8的整数。注2.N由SSLND寄存器设置为1到8的整数。



VOH=0.7×VCC，VOL=0.3×VCC，VIH=0.7×VCC，VIL=0.3×VCC

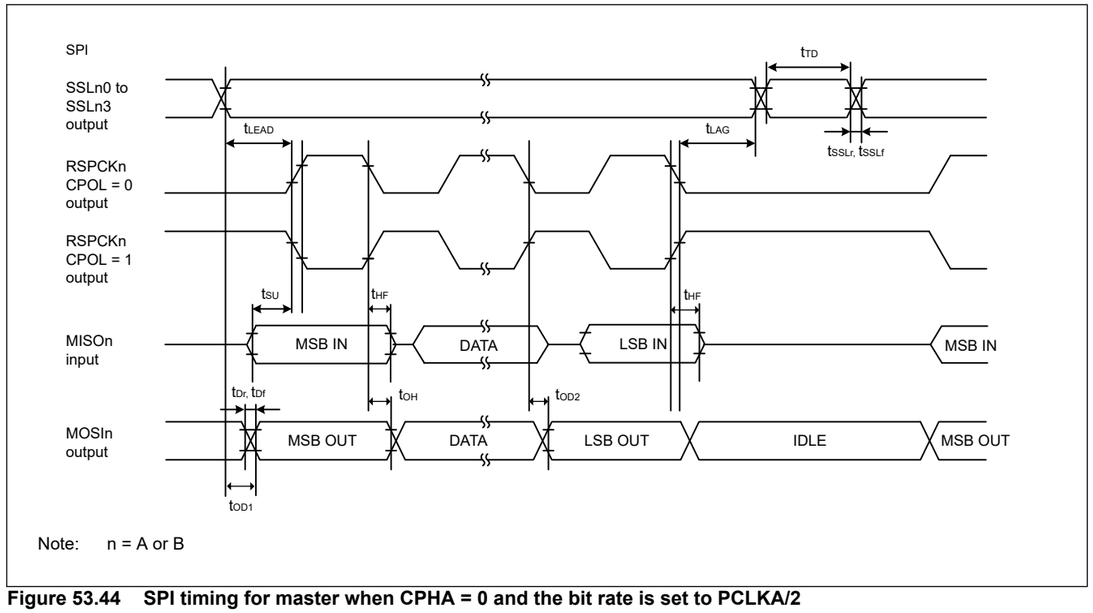
Note: n = A or B

Figure 53.42 SPI时钟时序



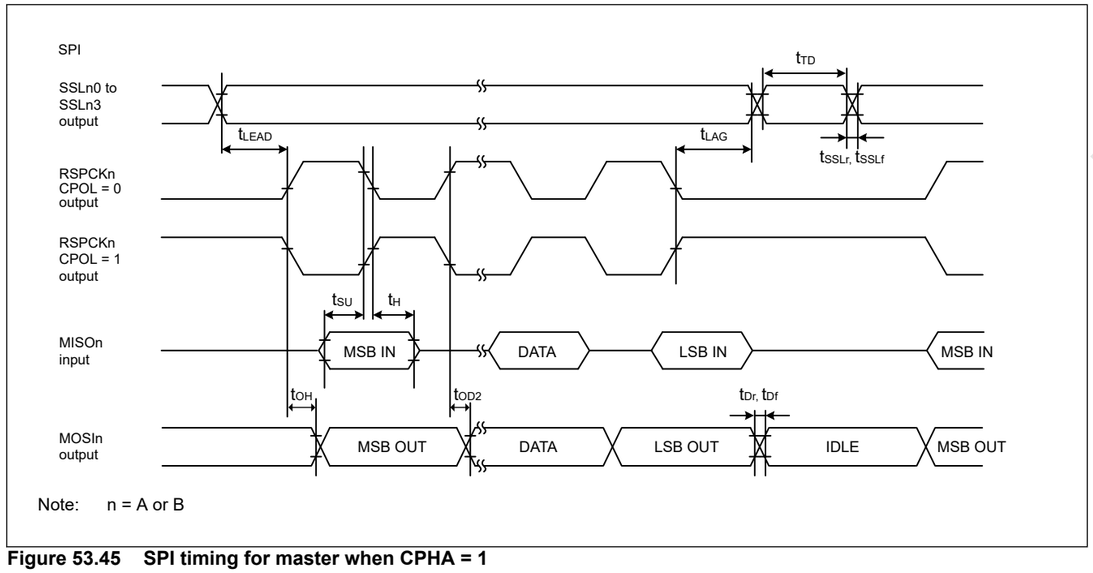
Note: n = A or B

Figure 53.43 CPHA=0时主机的SPI时序



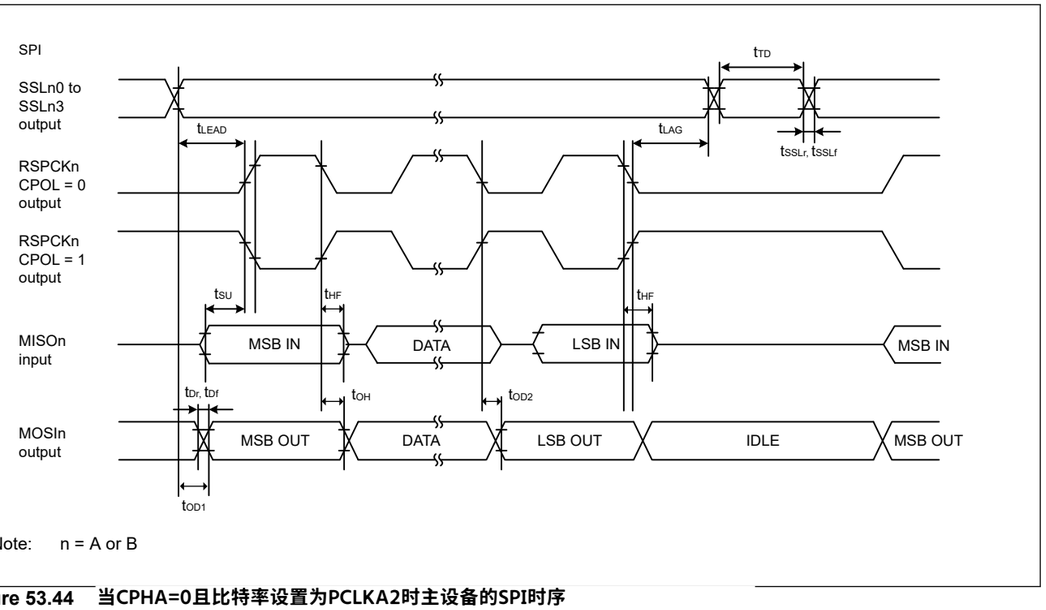
Note: n = A or B

Figure 53.44 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



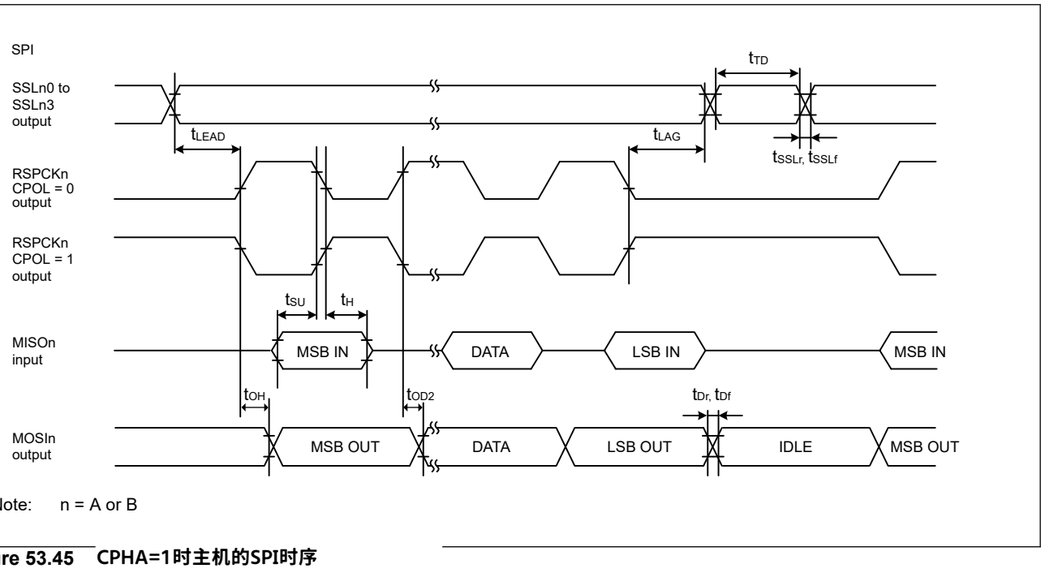
Note: n = A or B

Figure 53.45 SPI timing for master when CPHA = 1



Note: n = A or B

Figure 53.44 当CPHA=0且比特率设置为PCLKA2时主设备的SPI时序



Note: n = A or B

Figure 53.45 CPHA=1时主机的SPI时序

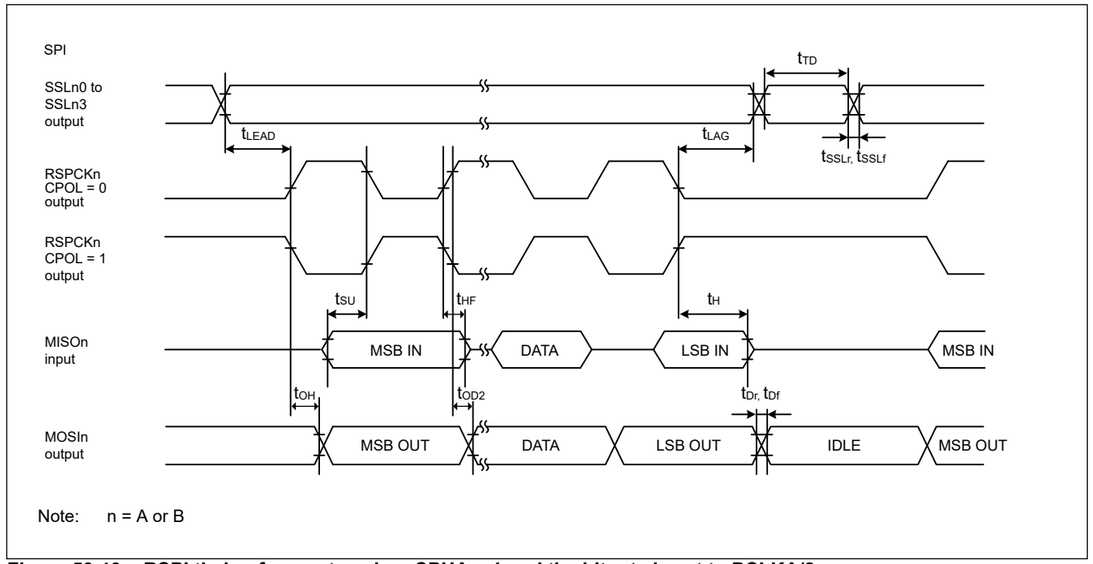


Figure 53.46 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

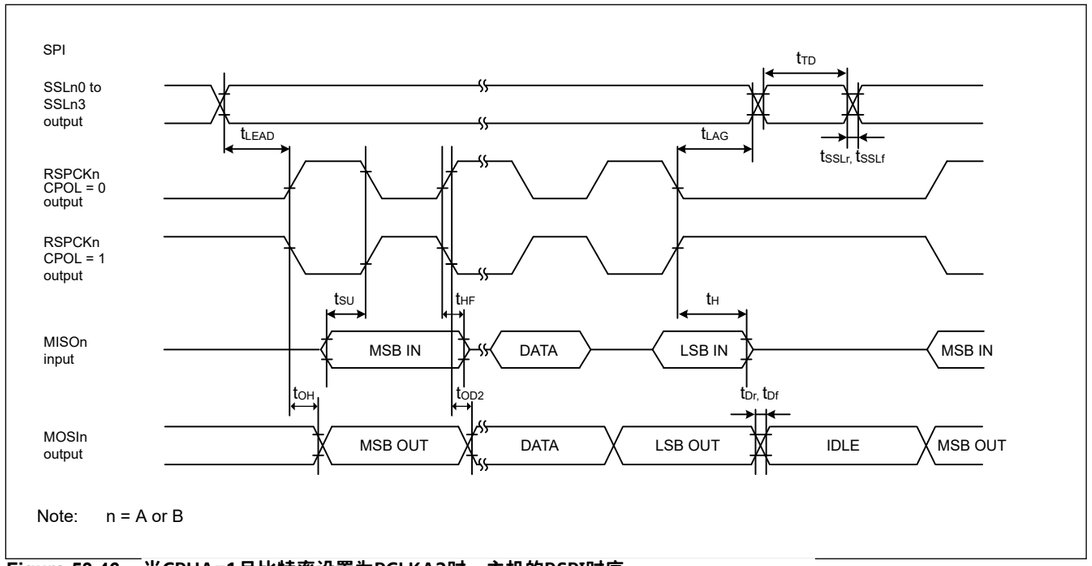


Figure 53.46 当CPHA=1且比特率设置为PCLKA2时，主机的RSPI时序

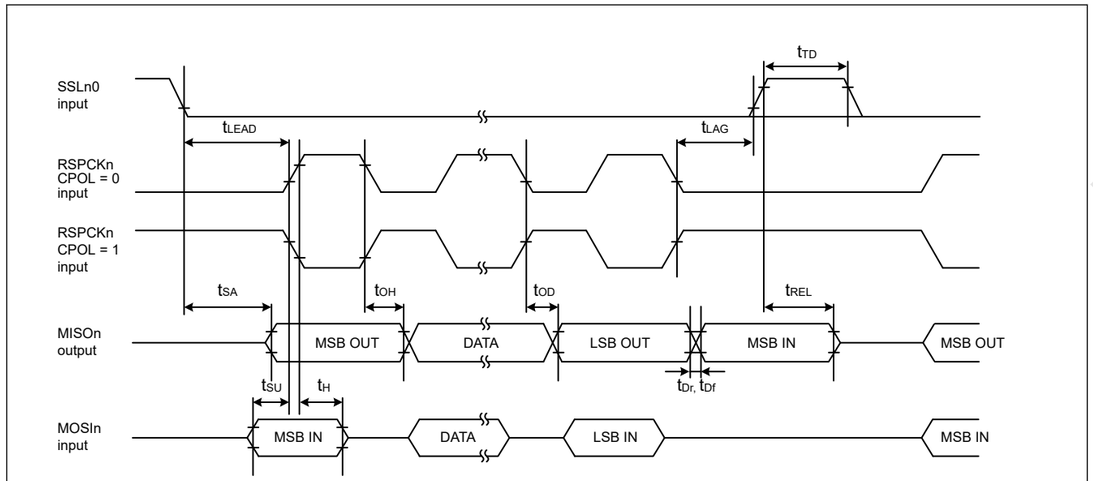


Figure 53.47 SPI timing for slave when CPHA = 0

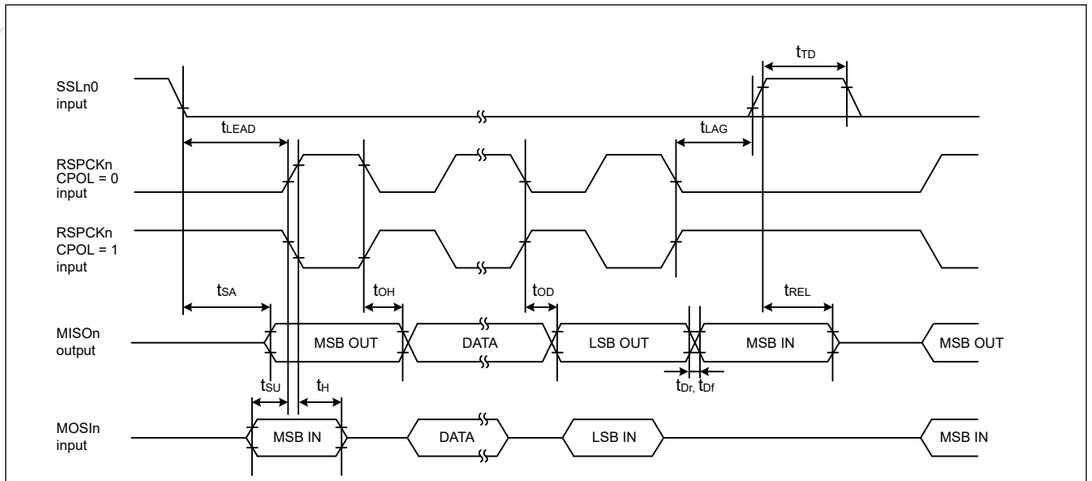


Figure 53.47 CPHA=0时从机的SPI时序

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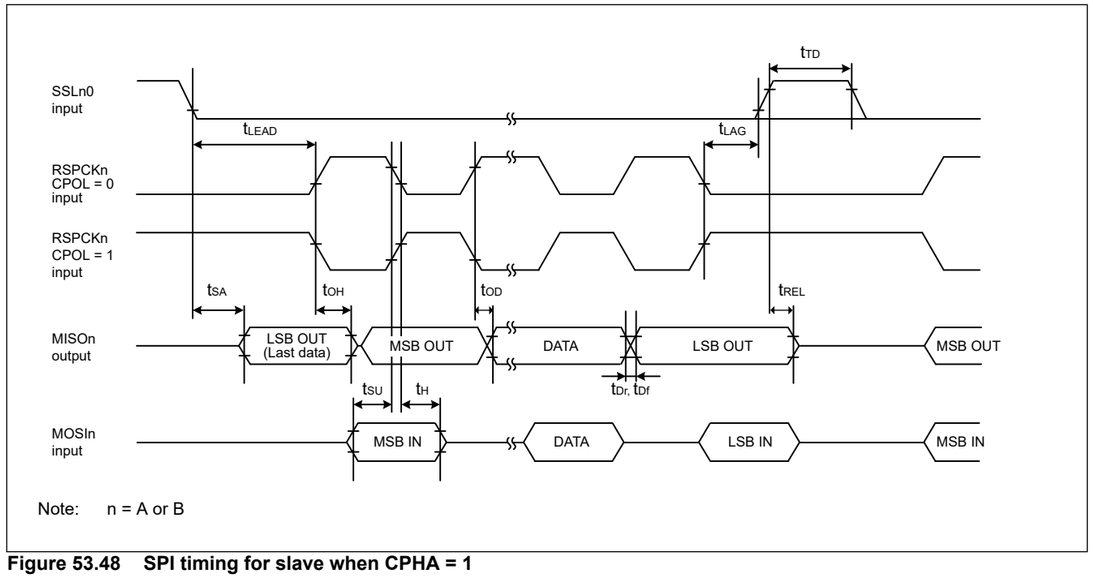

Figure 53.48 SPI timing for slave when CPHA = 1

53.3.11 QSPI Timing

Table 53.29 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 53.49
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	—	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	—	ns	
	Data input setup time	t_{Su}	10	—	ns	Figure 53.50
	Data input hold time	t_{IH}	0	—	ns	
	QSSL setup time	t_{LEAD}	(N + 0.5) × t_{Qscyc} - 5*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	QSSL hold time	t_{LAG}	(N + 0.5) × t_{Qscyc} - 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	Data output delay	t_{OD}	—	4	ns	
	Data output hold time	t_{OH}	–3.3	—	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.

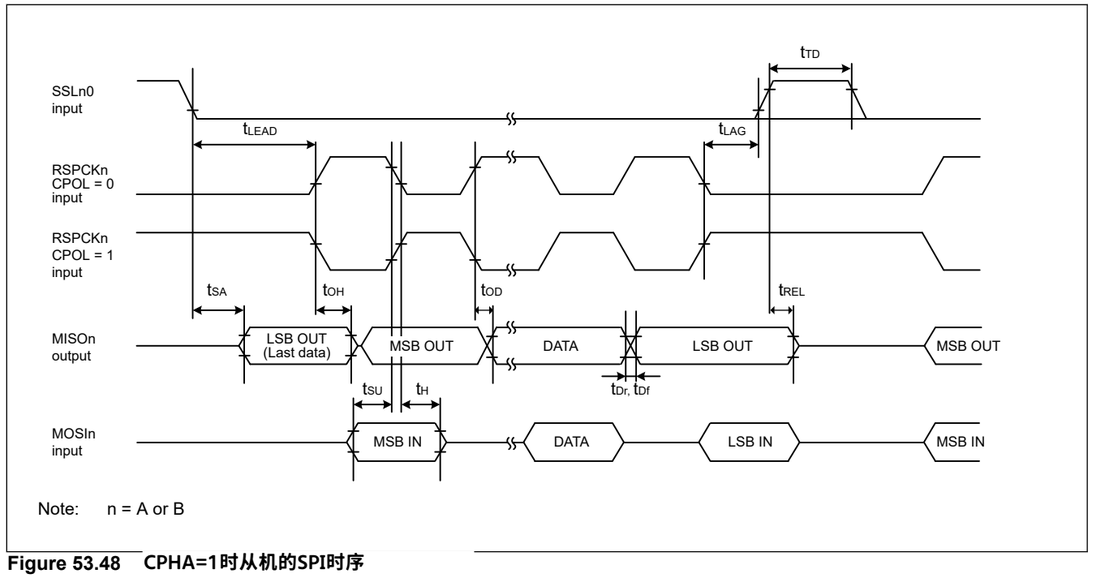

Figure 53.48 CPHA=1时从机的SPI时序

53.3.11 QSPI Timing

Table 53.29 QSPI timing

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
QSPI	QSPCK时钟周期	t_{QScyc}	2	48	t_{Pcyc}	Figure 53.49
	QSPCK时钟高脉冲宽度	t_{QSWH}	t_{QScyc} × 0.4	—	ns	
	QSPCK时钟低脉冲宽度	t_{QSWL}	t_{QScyc} × 0.4	—	ns	
	数据输入建立时间	t_{Su}	10	—	ns	Figure 53.50
	数据输入保持时间	t_{IH}	0	—	ns	
	QSSL设置时间	t_{LEAD}	(N + 0.5) × t_{Qscyc} - 5*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	QSSL保持时间	t_{LAG}	(N + 0.5) × t_{Qscyc} - 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	数据输出延迟	t_{OD}	—	4	ns	
	数据输出保持时间	t_{OH}	–3.3	—	ns	
	连续传输延迟	t_{TD}	1	16	t_{QScyc}	

Note: t_{Pcyc}: PCLKA cycle.
注1.在SFMSLD中N设置为0或1。注2.在SFMSHD中N设置为0或1。

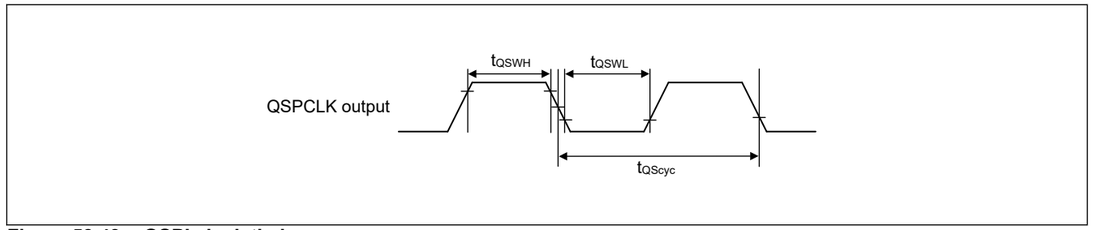

Figure 53.49 QSPI clock timing

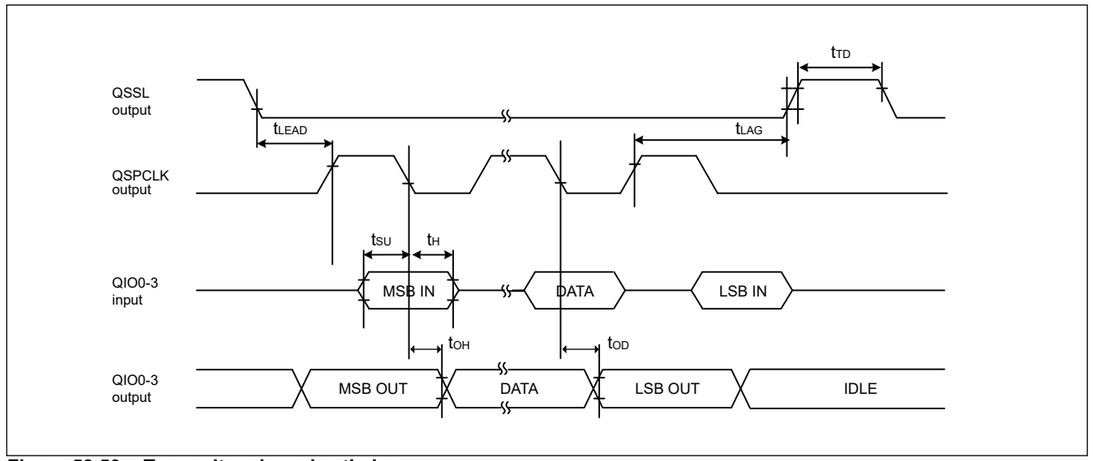

Figure 53.50 Transmit and receive timing

53.3.12 OSPI Timing

Table 53.30 OSPI timing (1 of 2)

(1) Conditions: High speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_SCLK, OM_DQS, OM_SIO0-7.
(2) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_CS0, OM_CS1.

Parameter		Symbol	Min	Max	Unit	Test conditions
OM_SCLK clock frequency	SPI	f_{OCcyc}	—	50	MHz	Figure 53.51
	SOPI/DOPI	f_{OCcyc}	—	100	MHz	
OM_SCLK high pulse width		t_{OCwh}	0.475	0.525	t_{OCcyc}	
OM_SCLK low pulse width		t_{OCwl}	0.475	0.525	t_{OCcyc}	
OM_SCLK rise time		t_{OCr}	—	1.8	ns	
OM_SCLK fall time		t_{OCf}	—	1.8	ns	
OM_CS setup time	SPI/SOPI	t_{OCLEAD}	1.5 × t_{OCcyc} – 10.4 (Minimum register settings)	2.5 × t_{OCcyc} + 6.9 (Maximum register settings)	ns	Figure 53.52, Figure 53.53
	DOPI	t_{OCLEAD}	1.25 × t_{OCcyc} – 7.9 (Minimum register settings)	2.25 × t_{OCcyc} + 4.4 (Maximum register settings)	ns	Figure 53.54

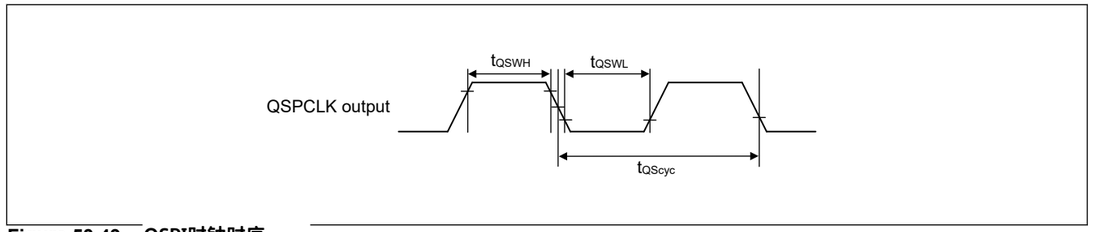

Figure 53.49 QSPI时钟时序

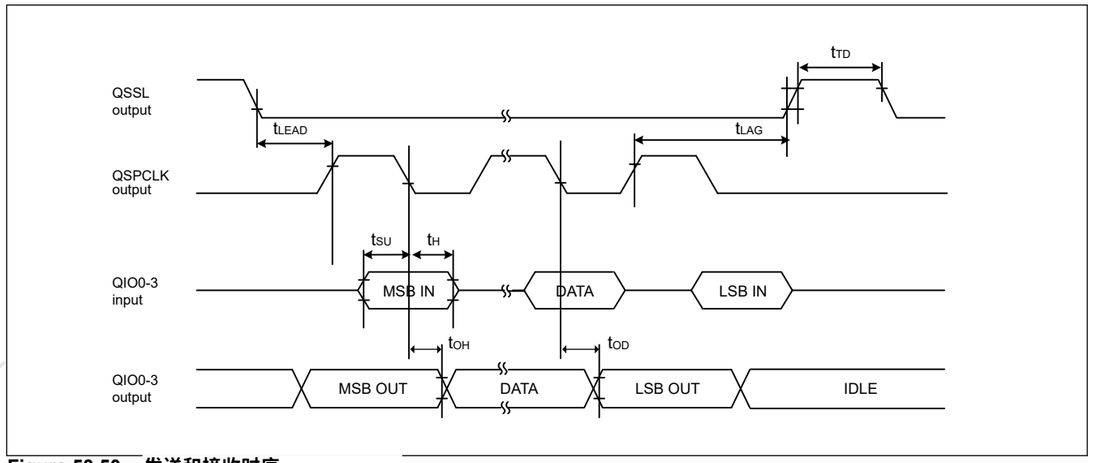

Figure 53.50 发送和接收时序

53.3.12 OSPI Timing

Table 53.30 OSPI时序(1of2)

(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高速高驱动输出：OM_SCLK、OM_DQS、OM_SIO0-7。(2)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：OM_CS0、OM_CS1。

Parameter		Symbol	Min	Max	Unit	测试条件
OM_SCLK 时钟频率	SPI	f_{OCcyc}	—	50	MHz	Figure 53.51
	SOPI/DOPI	f_{OCcyc}	—	100	MHz	
OM_SCLK高脉冲宽度		t_{OCwh}	0.475	0.525	t_{OCcyc}	
OM_SCLK低脉冲宽度		t_{OCwl}	0.475	0.525	t_{OCcyc}	
OM_SCLK上升时间		t_{OCr}	—	1.8	ns	
OM_SCLK下降时间		t_{OCf}	—	1.8	ns	
OM_CS建立时间	SPI/SOPI	t_{OCLEAD}	1.5 × t_{OCcyc} – 10.4 (Minimum register settings)	2.5 × t_{OCcyc} + 6.9 (Maximum register settings)	ns	Figure 53.52, Figure 53.53
	DOPI	t_{OCLEAD}	1.25 × t_{OCcyc} – 7.9 (Minimum register settings)	2.25 × t_{OCcyc} + 4.4 (Maximum register settings)	ns	Figure 53.54

Table 53.30 OSPI timing (2 of 2)

(1) Conditions: High speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_SCLK, OM_DQS, OM_SIO0-7.
(2) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_CS0, OM_CS1.

Parameter		Symbol	Min	Max	Unit	Test conditions
OM_CS hold time	SPI/SOPI	t_{OCLAG}	1 × t_{OCcyc} – 6.9 (Minimum register settings)	4.5 × t_{OCcyc} + 10.4 (Maximum register settings)	ns	Figure 53.52, Figure 53.53
	DOPI read	t_{OCLAG}	3.25 × t_{OCcyc} – 4.4 (Minimum register settings)	4.25 × t_{OCcyc} + 7.9 (Maximum register settings)	ns	Figure 53.54
	DOPI write	t_{OCLAG}	0.75 × t_{OCcyc} – 4.4 (Minimum register settings)	4.25 × t_{OCcyc} + 7.9 (Maximum register settings)	ns	
Continuous transfer delay time		t_{OCTD}	1 × t_{OCcyc} – 1 (Minimum register settings)	8.5 × t_{OCcyc} + 1 (Maximum register settings)	ns	Figure 53.52, Figure 53.53, Figure 53.54
Data input setup time	SPI SCLK base point	t_{SU}	10.5	—	ns	Figure 53.52
Data input hold time		t_H	0.5	—	ns	
Data input setup time	SOPI/DOPI DQS base point*1	t_{SU}	-1.3	—	ns	Figure 53.53, Figure 53.54
Data input hold time		t_H	3.25	—	ns	
Skew of Clock to Data Strobe		t_{CKDS}	—	20	ns	
Data output delay time	SPI/SOPI	t_{OD}	—	2.65	ns	Figure 53.52, Figure 53.53
Data output hold time		t_{OH}	-2.65	—	ns	
Data output buffer off time	SOPI	t_{BOFF}	2.1	—	ns	Figure 53.53
Data output delay time	DOPI*1	t_{OD}	—	3.65	ns	Figure 53.54, Figure 53.55
Data output hold time		t_{OH}	1.1	—	ns	
Data output buffer off time	DOPI	t_{BOFF}	1.1	—	ns	Figure 53.54
DQS refresh input setup time		t_{DQSS}	20	—	ns	Figure 53.56
DQS refresh input hold time		t_{DQSH}	0.5 × tOCcyc	—	ns	

Note: t_{OCcyc} indicates the OM_SCLK cycle.
Note 1. OM_SCLK frequency: 100 MHz

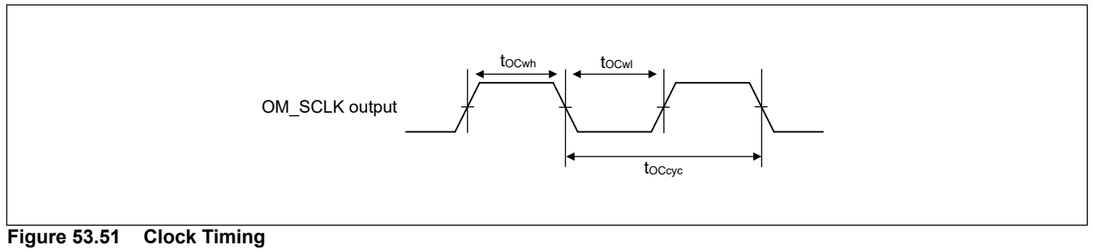

Figure 53.51 Clock Timing

Table 53.30 OSPI时序（2之2）

(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高速高驱动输出：OM_SCLK、OM_DQS、OM_SIO0-7。(2)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：OM_CS0、OM_CS1。

Parameter		Symbol	Min	Max	Unit	测试条件
OM_CS保持时间	SPI/SOPI	t_{OCLAG}	1 × t_{OCcyc} – 6.9 (Minimum register settings)	4.5 × t_{OCcyc} + 10.4 (Maximum register settings)	ns	Figure 53.52, Figure 53.53
	DOPI read	t_{OCLAG}	3.25 × t_{OCcyc} – 4.4 (Minimum register settings)	4.25 × t_{OCcyc} + 7.9 (Maximum register settings)	ns	Figure 53.54
	DOPI write	t_{OCLAG}	0.75 × t_{OCcyc} – 4.4 (Minimum register settings)	4.25 × t_{OCcyc} + 7.9 (Maximum register settings)	ns	
连续传输延迟时间		t_{OCTD}	1 × t_{OCcyc} – 1 (Minimum register settings)	8.5 × t_{OCcyc} + 1 (Maximum register settings)	ns	Figure 53.52, Figure 53.53, Figure 53.54
数据输入建立时间	SPISCLK基点	t_{SU}	10.5	—	ns	Figure 53.52
数据输入保持时间		t_H	0.5	—	ns	
数据输入建立时间	SOPIDOPIDQS基点*1	t_{SU}	-1.3	—	ns	Figure 53.53, Figure 53.54
数据输入保持时间		t_H	3.25	—	ns	
时钟与数据的偏差 Strobe		t_{CKDS}	—	20	ns	
数据输出延迟时间	SPI/SOPI	t_{OD}	—	2.65	ns	Figure 53.52, Figure 53.53
数据输出保持时间		t_{OH}	-2.65	—	ns	
数据输出缓冲区关闭时间	SOPI	t_{BOFF}	2.1	—	ns	Figure 53.53
数据输出延迟时间	DOPI*1	t_{OD}	—	3.65	ns	Figure 53.54, Figure 53.55
数据输出保持时间		t_{OH}	1.1	—	ns	
数据输出缓冲区关闭时间	DOPI	t_{BOFF}	1.1	—	ns	Figure 53.54
DQS刷新输入建立时间		t_{DQSS}	20	—	ns	Figure 53.56
DQS刷新输入保持时间		t_{DQSH}	0.5 × tOCcyc	—	ns	

Note: tOCcyc表示OM_SCLK周期。
Note 1. OM_SCLK frequency: 100 MHz

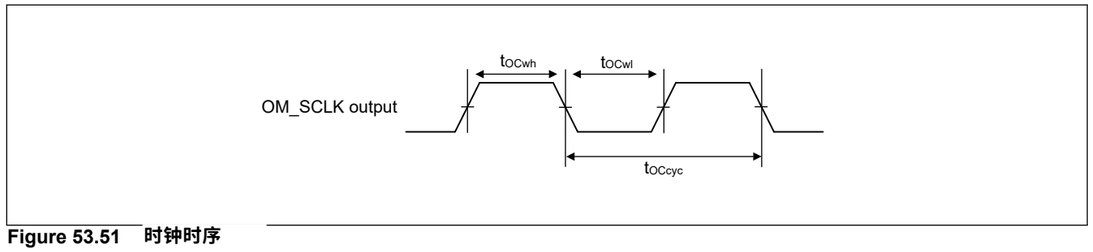

Figure 53.51 时钟时序

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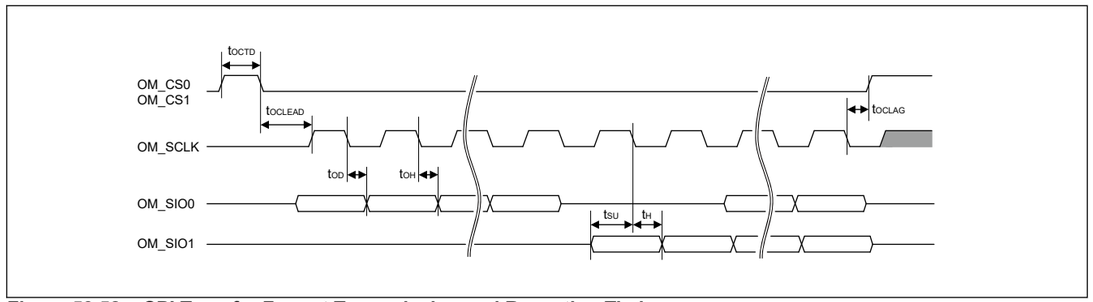

Figure 53.52 SPI Transfer Format Transmission and Reception Timing

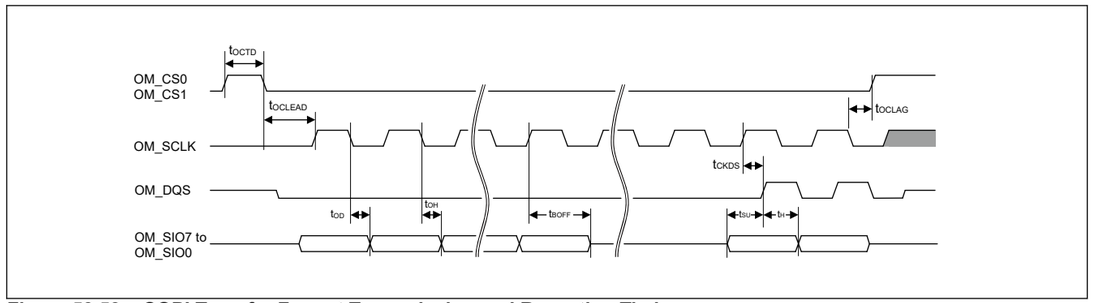

Figure 53.53 SOPI Transfer Format Transmission and Reception Timing

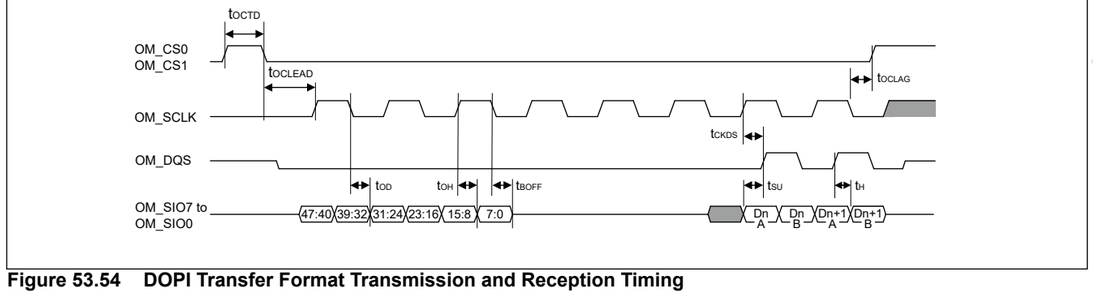

Figure 53.54 DOPI Transfer Format Transmission and Reception Timing

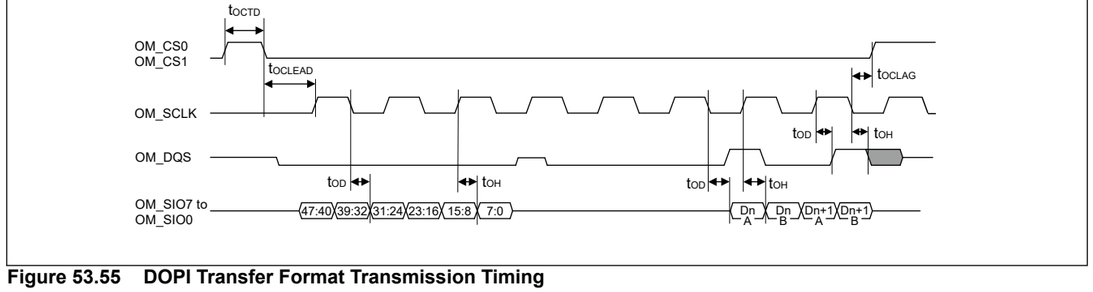

Figure 53.55 DOPI Transfer Format Transmission Timing

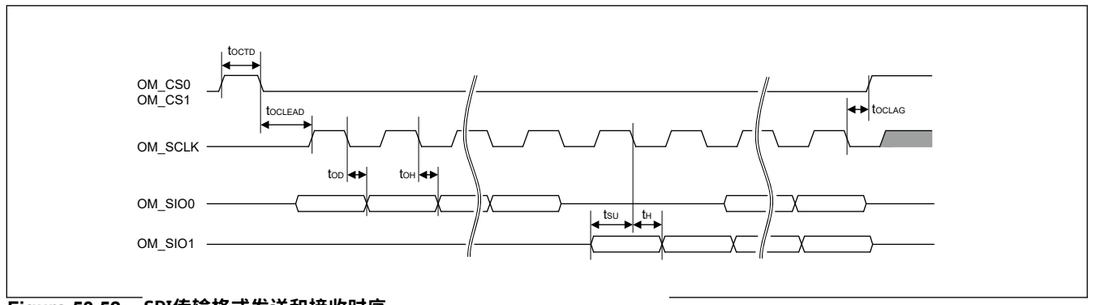

Figure 53.52 SPI传输格式发送和接收时序

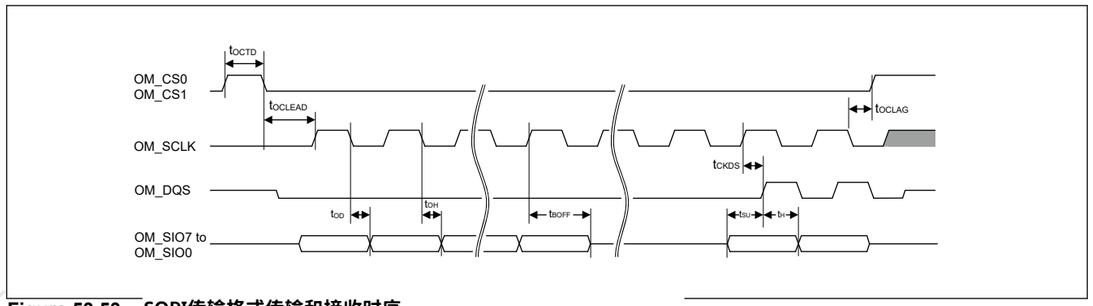

Figure 53.53 SOPI传输格式传输和接收时序

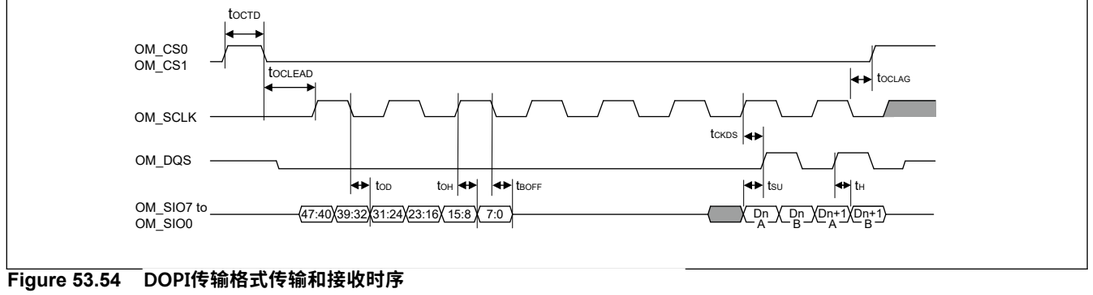

Figure 53.54 DOPI传输格式传输和接收时序

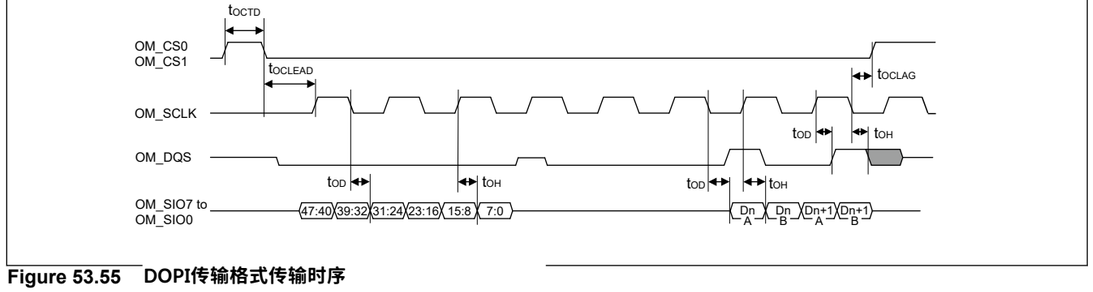

Figure 53.55 DOPI传输格式传输时序

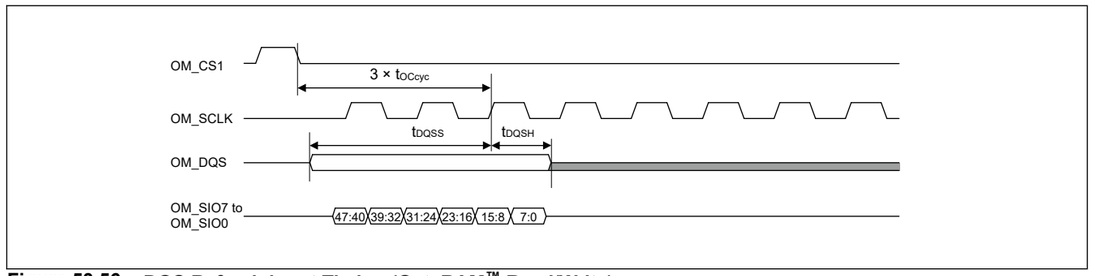

Figure 53.56 DQS Refresh input Timing (OctaRAM™ Read/Write)

53.3.13 IIC Timing

Table 53.31 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SDA2, SCL2.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 53.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

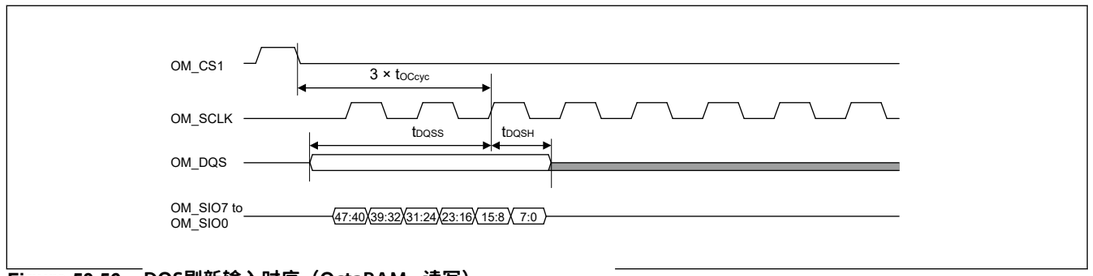

Figure 53.56 DQS刷新输入时序（OctaRAM 读写）

53.3.13 IIC Timing

Table 53.31 IIC时序(1)(1of2)

(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_B、SCL1_B、SDA2、SCL2。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL1_A、SDA1_A。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min	Max	Unit	测试条件
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 53.57
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	1000	ns	
	SCL、SDA下降时间	t_{Sf}	—	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	—	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	—	ns	
	STOP条件输入建立时间	t_{STOS}	1000	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

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Table 53.31 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SDA2, SCL2.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL1_A, SDA1_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 53.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*1	300	ns	
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*1	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—		
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SCL0_A, SDA0_A, SCL1_A, and SDA1_A.

Table 53.31 IIC时序(1)(2of2)

(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_B、SCL1_B、SDA2、SCL2。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL1_A、SDA1_A。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min	Max	Unit	测试条件
IIC (Fast mode)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 53.57
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL、SDA上升时间	t_{Sr}	20 × (external pullup voltage/5.5V)*1	300	ns	
	SCL、SDA下降时间	t_{Sf}	20 × (external pullup voltage/5.5V)*1	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	—	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	重复启动条件输入建立时间	t_{STAS}	300	—	ns	
	STOP条件输入建立时间	t_{STOS}	300	—		
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。
Note: 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。
Note: 必须使用名称后附有字母的引脚，例如"_A"、"_B"，以表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

注1.仅支持SCL0_A、SDA0_A、SCL1_A和SDA1_A。

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Table 53.32 IIC timing (2)

Setting of the SCL0/1_A, SDA0/1_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	—	ns	Figure 53.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/ 5.5V)	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × tIICcyc	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	—	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 1. Cb indicates the total capacity of the bus line.

Table 53.32 IIC timing (2)

PmnPFS寄存器中的端口驱动能力位不需要设置SCL01_A、SDA01_A引脚。

Parameter		Symbol	Min	Max	Unit	测试条件
IIC (Fast-mode+) ICFER.FMPE = 1	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 240	—	ns	Figure 53.57
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL、SDA上升时间	t_{Sr}	—	120	ns	
	SCL、SDA下降时间	t_{Sf}	20 × (external pullup voltage/ 5.5V)	120	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × tIICcyc	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 120	—	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	—	ns	
	禁用唤醒功能时的启动条件输入保持时间	t_{STAH}	t_{IICcyc} + 120	—	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	—	ns	
	重启条件输入建立时间	t_{STAS}	120	—	ns	
	停止条件输入建立时间	t_{STOS}	120	—	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	数据输入保持时间	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	550	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。
Note: 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。
注1.Cb表示总线的总容量。

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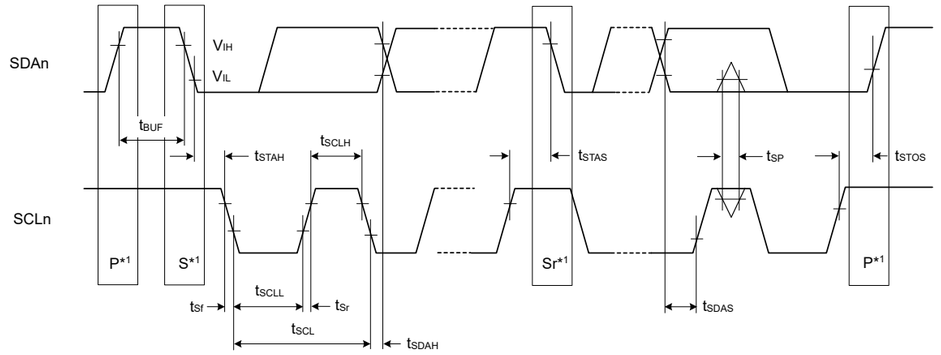


Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

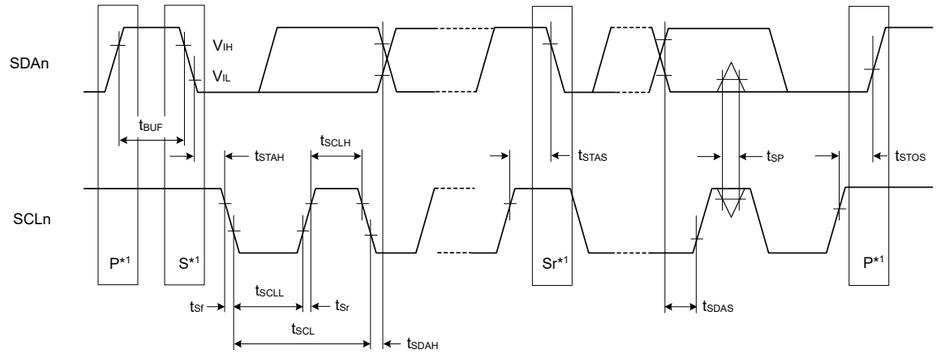
Figure 53.57 I²C bus interface input/output timing

53.3.14 SSIE Timing

Table 53.33 SSIE timing

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" , "_B" or "_C" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK0	Cycle	Master	t_O	80	—	ns	Figure 53.58
		Slave	t_I	80	—	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	—	t_O	
		Slave		0.35	—	t_I	
	Rising time/ falling time	Master	t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave		—	0.15	t_O / t_I	
SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0, SSIDATA0	Input set up time	Master	t_{SR}	12	—	ns	Figure 53.60, Figure 53.61
		Slave		12	—	ns	
	Input hold time	Master	t_{HR}	8	—	ns	
		Slave		15	—	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 53.60, Figure 53.61
	Output delay time from SSILRCK0/ SSIFS0 change	Slave	t_{DTRW}	—	20	ns	Figure 53.62*1
GTIOC2A, AUDIO_CLK	Cycle		t_{EXcyc}	20	—	ns	Figure 53.59
	High level/ low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	



注1.S、P和Sr表示以下条件：
S：开始条件P：
停止条件
Sr：重启条件

Figure 53.57 I2C总线接口输入输出时序

53.3.14 SSIE Timing

Table 53.33 SSIE timing

(1)通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。(2)使用名称后附有字母的引脚，例如"_A"、"_B"或"_C"来表示组成员身份。对于SSIE接口，测量每组的电气特性的交流部分。

Parameter			Symbol	目标规格		Unit	Comments
				Min.	Max.		
SSIBCK0	Cycle	Master	t_O	80	—	ns	Figure 53.58
		Slave	t_I	80	—	ns	
	高电平低电平	Master	t_{HC}/t_{LC}	0.35	—	t_O	
		Slave		0.35	—	t_I	
	上升时间下降时间	Master	t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave		—	0.15	t_O / t_I	
SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0, SSIDATA0	输入建立时间	Master	t_{SR}	12	—	ns	Figure 53.60, Figure 53.61
		Slave		12	—	ns	
	输入保持时间	Master	t_{HR}	8	—	ns	
		Slave		15	—	ns	
	输出延迟时间	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 53.60, Figure 53.61
	SSILRCK0的输出延迟时间 SSIFS0 change	Slave	t_{DTRW}	—	20	ns	Figure 53.62*1
GTIOC2A, AUDIO_CLK	Cycle		t_{EXcyc}	20	—	ns	Figure 53.59
	高电平低电平		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA0 pin.

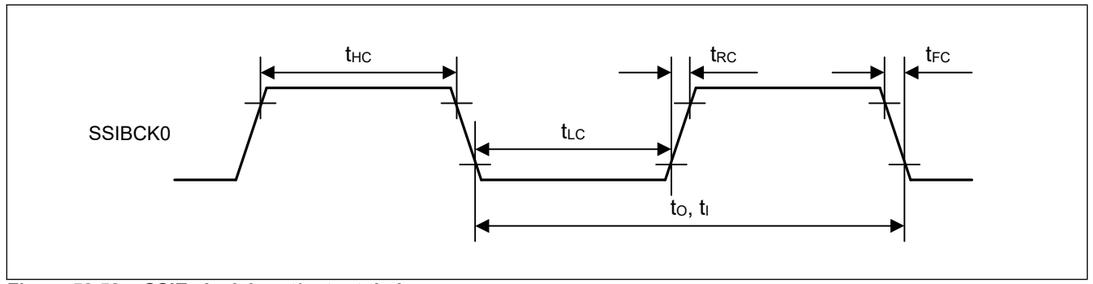


Figure 53.58 SSIE clock input/output timing

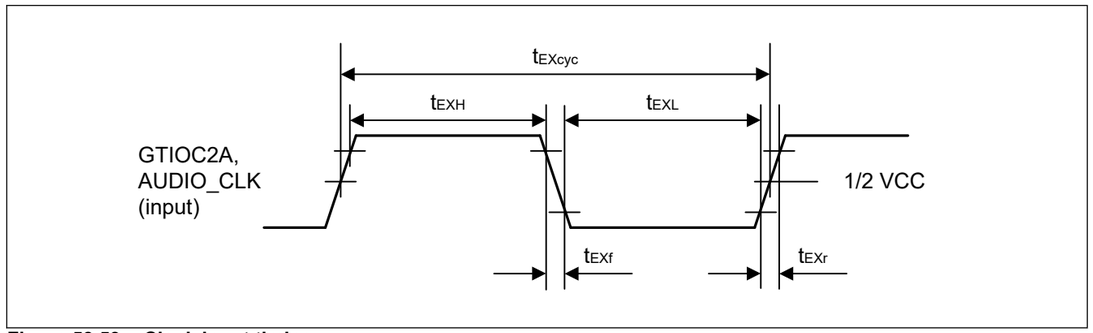


Figure 53.59 Clock input timing

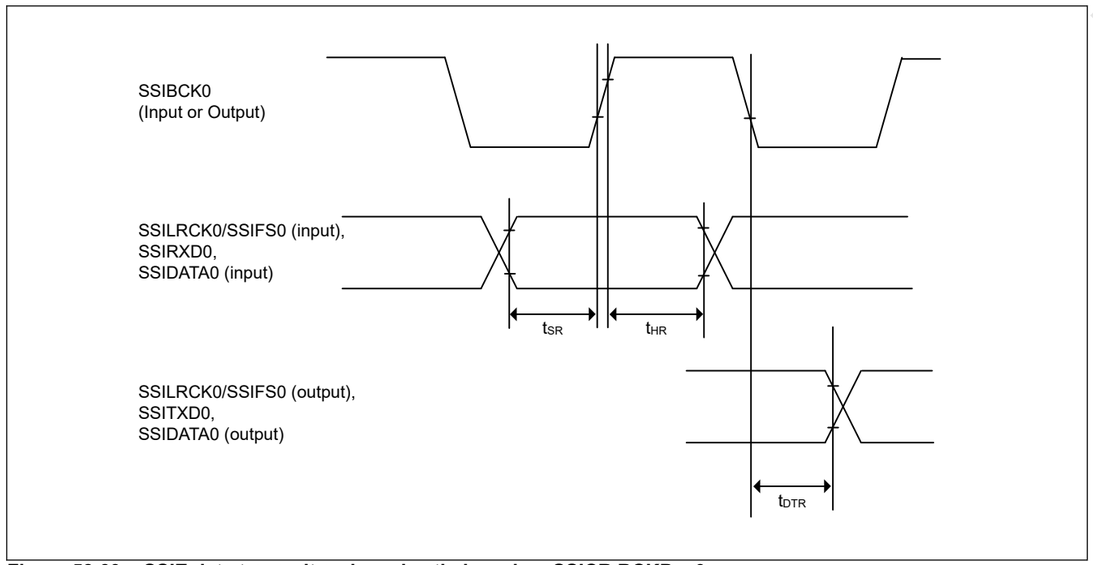


Figure 53.60 SSIE data transmit and receive timing when SSICR.BCKP = 0

注1.对于从模式传输，SSIE有一个路径，通过该路径，从SSILRCK0SSIFS0引脚输入的信号用于生成发送数据，发送数据逻辑输出到SSITXD0或SSIDATA0引脚。

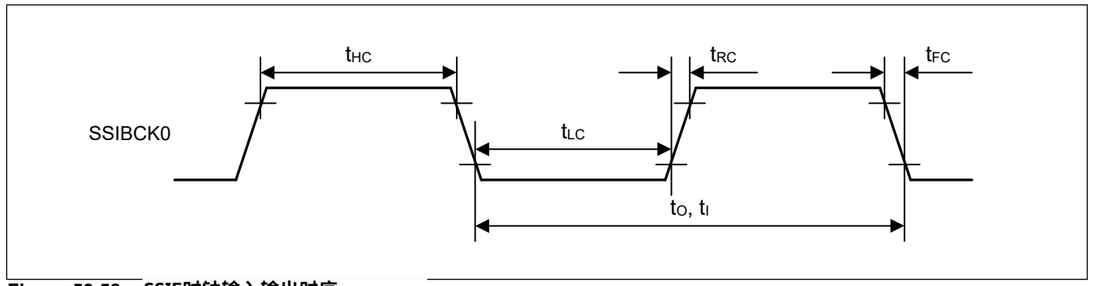


Figure 53.58 SSIE时钟输入输出时序

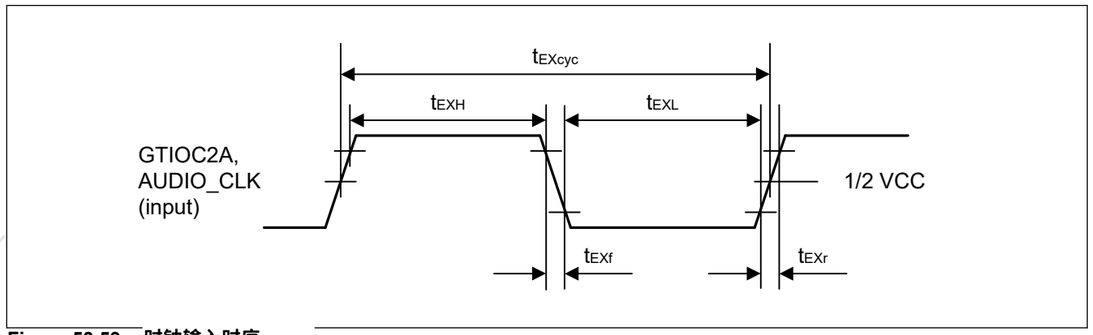


Figure 53.59 时钟输入时序

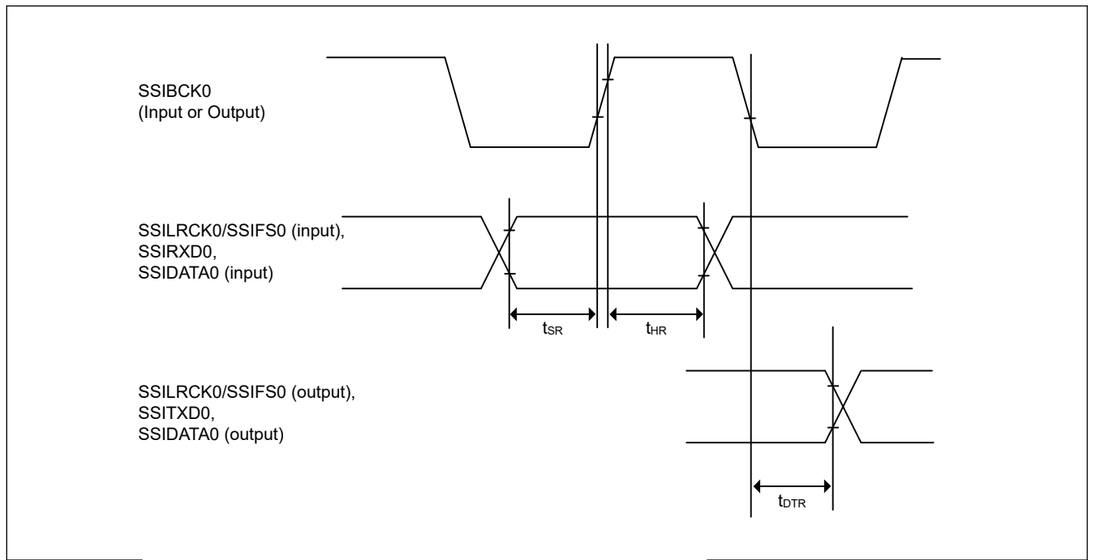


Figure 53.60 SSICR.BCKP=0时的SSIE数据发送和接收时序

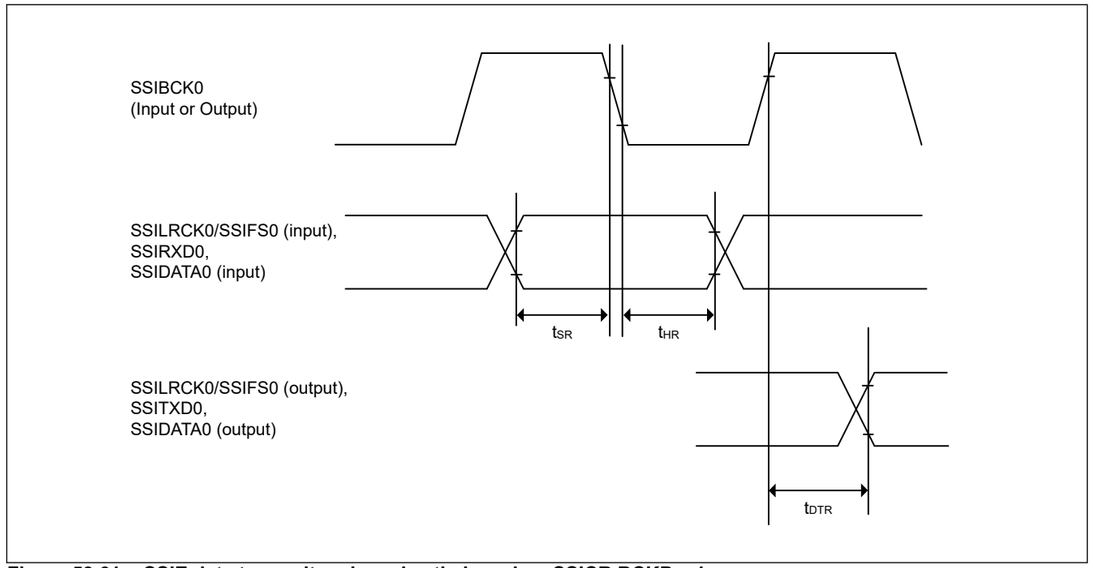


Figure 53.61 SSIE data transmit and receive timing when SSICR.BCKP = 1

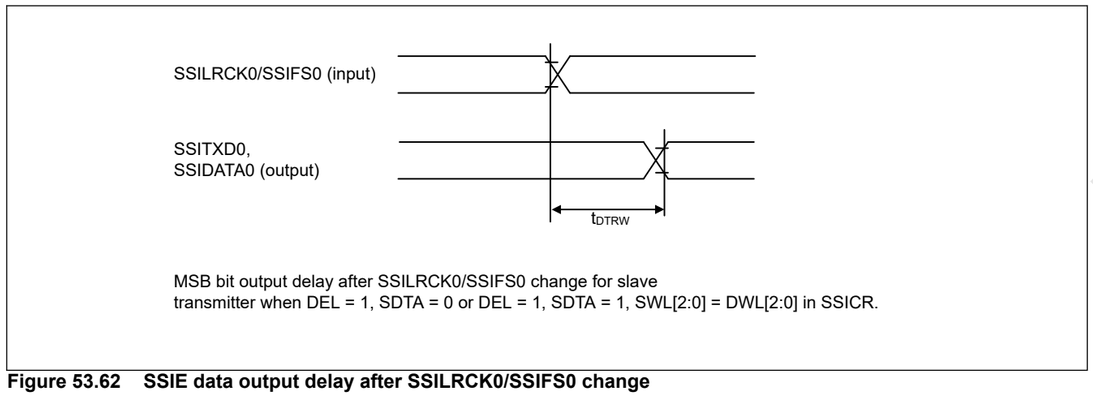


Figure 53.62 SSIE data output delay after SSILRCK0/SSIFS0 change

53.3.15 SD/MMC Host Interface Timing

Table 53.34 SD/MMC Host Interface signal timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Parameter	Symbol	Min	Max	Unit	Test conditions
SDCLK clock cycle	T_{SDCYC}	20	—	ns	Figure 53.63
SDCLK clock high pulse width	T_{SDWH}	6.5	—	ns	
SDCLK clock low pulse width	T_{SDWL}	6.5	—	ns	
SDCLK clock rise time	T_{SDLH}	—	3	ns	
SDCLK clock fall time	T_{SDHL}	—	3	ns	
SDCMD/SDDAT output data delay	T_{SDODLY}	–7	4	ns	
SDCMD/SDDAT input data setup	T_{SDIS}	4.5	—	ns	
SDCMD/SDDAT input data hold	T_{SDIH}	1.5	—	ns	

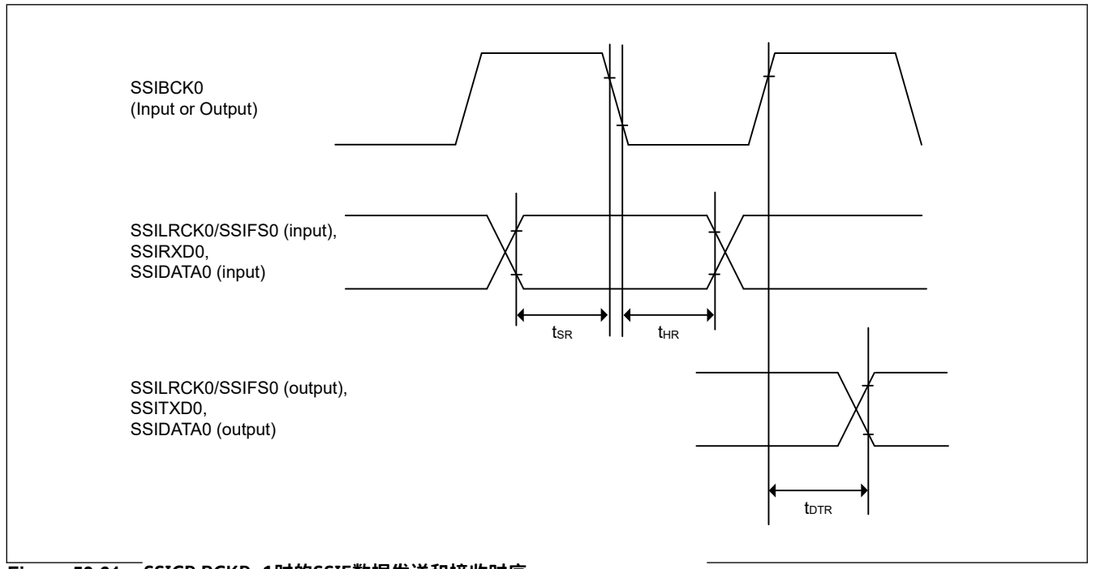


Figure 53.61 SSICR.BCKP=1时的SSIE数据发送和接收时序

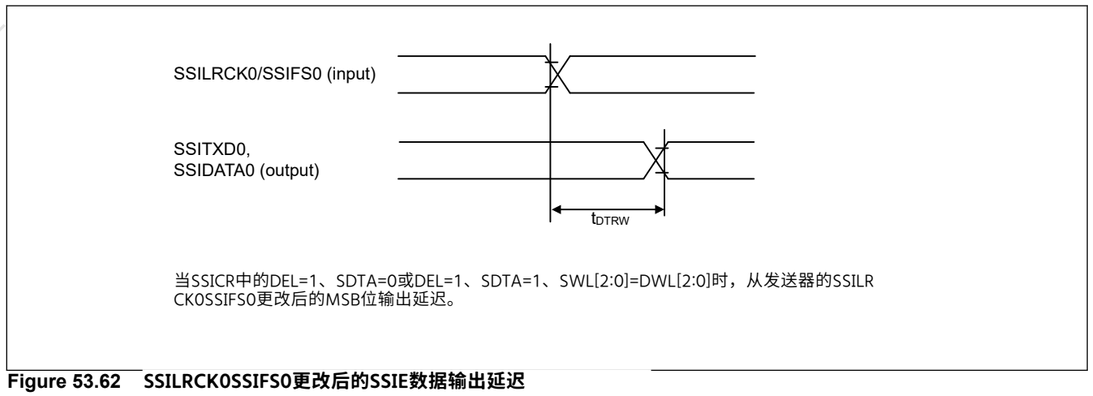


Figure 53.62 SSILRCK0SSIFS0更改后的SSIE数据输出延迟

53.3.15 SDMMC主机接口时序

Table 53.34 SDMMC主机接口信号时序

条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
时钟占空比为50%。

Parameter		Symbol	Min	Max	Unit	测试条件
SDCLK	时钟周期	T_{SDCYC}	20	—	ns	Figure 53.63
SDCLK	时钟高脉冲宽度	T_{SDWH}	6.5	—	ns	
SDCLK	时钟低脉冲宽度	T_{SDWL}	6.5	—	ns	
SDCLK	时钟上升时间	T_{SDLH}	—	3	ns	
SDCLK	时钟下降时间	T_{SDHL}	—	3	ns	
SDCMDSDDAT输出数据延迟		T_{SDODLY}	–7	4	ns	
SDCMDSDDAT输入数据设置		T_{SDIS}	4.5	—	ns	
SDCMDSDDAT输入数据保持		T_{SDIH}	1.5	—	ns	

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Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

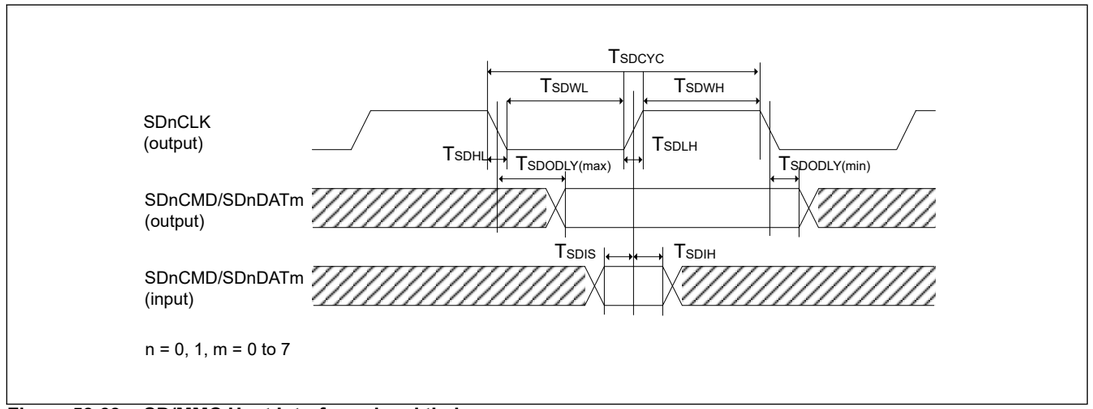


Figure 53.63 SD/MMC Host Interface signal timing

53.3.16 ETHERC Timing

Table 53.35 ETHERC timing (1 of 2)

Conditions: ETHERC (RMII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
ETHERC (RMII)	REF50CK0 cycle time	T_{ck}	20	—	ns	Figure 53.64 to Figure 53.67
	REF50CK0 frequency, typical 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK0 duty	—	35	65	%	
	REF50CK0 rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1 output delay	T_{co}	2.5	12.0	ns	
	RMII_xxxx*2 setup time	T_{su}	3	—	ns	
	RMII_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET0_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 53.68

Note: 必须使用名称后附有字母的引脚，例如“_A”、“_B”，以表示组成员身份。对于SDMMC主机接口，对每组电气特性的交流部分进行测量。

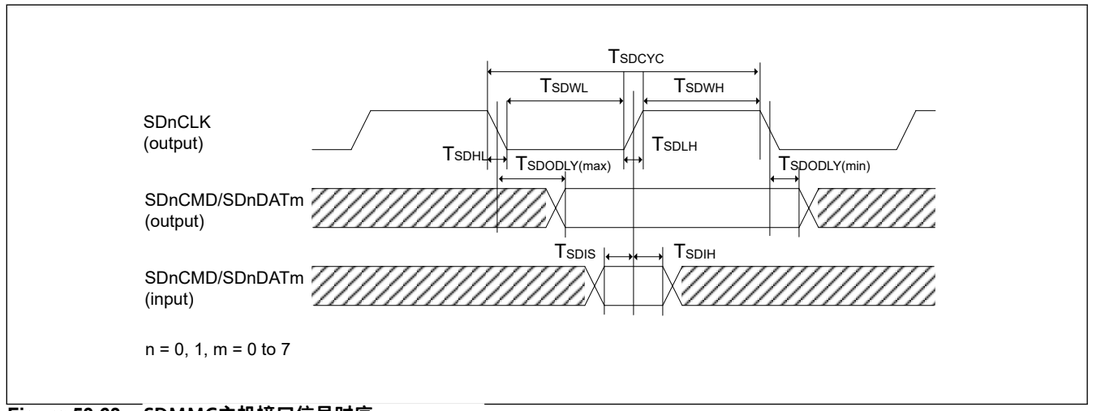


Figure 53.63 SDMMC主机接口信号时序

53.3.16 ETHERC Timing

Table 53.35 ETHERC计时（1of2）

条件：ETHERC(RMII)：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：ET0_MDC, ET0_MDIO.
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
ETHERC(MII)：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

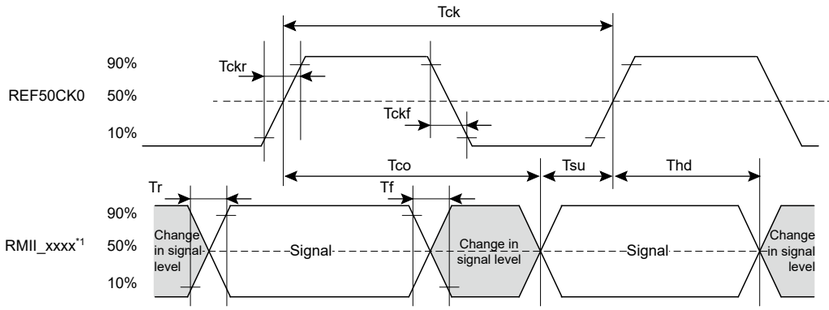
Parameter		Symbol	Min	Max	Unit	测试条件
ETHERC (RMII)	REF50CK0循环时间	T_{ck}	20	—	ns	图53.64至Figure 53.67
	REF50CK0频率，典型值50MHz	—	—	50 + 100 ppm	MHz	
	REF50CK0 duty	—	35	65	%	
	REF50CK0 rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1输出延迟	T_{co}	2.5	12.0	ns	
	RMII_xxxx*2建立时间	T_{su}	3	—	ns	
	RMII_xxxx*2保持时间	T_{hd}	1	—	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET0_WOL输出延迟	t_{WOLd}	1	23.5	ns	Figure 53.68

Table 53.35 ETHERC timing (2 of 2)

Conditions: ETHERC (RMII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins:
ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET0_TX_EN output delay	t_{TENd}	1	20	ns	Figure 53.69
	ET0_ETXD0 to ET_ETXD3 output delay	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	—	ns	
	ET0_CRS hold time	t_{CRSh}	10	—	ns	
	ET0_COL setup time	t_{COLs}	10	—	ns	Figure 53.70
	ET0_COL hold time	t_{COLh}	10	—	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET0_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 53.71
	ET0_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET0_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET0_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET0_RX_ER setup time	t_{RERs}	10	—	ns	Figure 53.72
	ET0_RX_ER hold time	t_{RESh}	10	—	ns	
	ET0_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 53.73

Note: The following pins must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group. REF50CK0_A, REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B.
Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.



Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

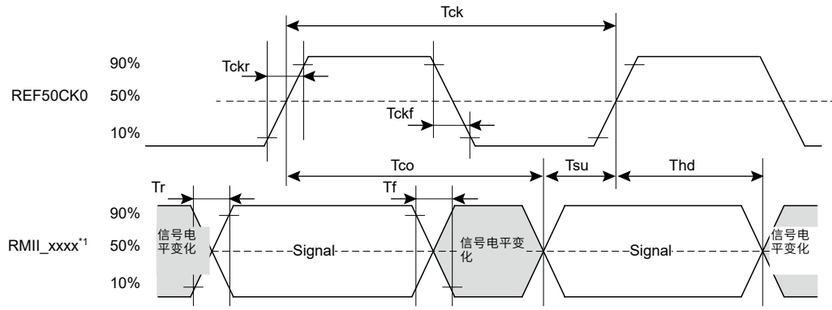
Figure 53.64 REF50CK0 and RMII signal timing

Table 53.35 ETHERC时间(2of2)

条件：ETHERC(RMII)：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：
ET0_MDC, ET0_MDIO.
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
ETHERC(MII)：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
ETHERC (MII)	ET0_TX_CLK周期时间	t_{Tcyc}	40	—	ns	—
	ET0_TX_EN输出延迟	t_{TENd}	1	20	ns	Figure 53.69
	ET0_ETXD0到ET_ETXD3输出延迟	t_{MTDd}	1	20	ns	
	ET0_CRS建立时间	t_{CRSs}	10	—	ns	
	ET0_CRS保持时间	t_{CRSh}	10	—	ns	
	ET0_COL建立时间	t_{COLs}	10	—	ns	Figure 53.70
	ET0_COL保持时间	t_{COLh}	10	—	ns	
	ET0_RX_CLK周期时间	t_{TRcyc}	40	—	ns	—
	ET0_RX_DV建立时间	t_{RDVs}	10	—	ns	Figure 53.71
	ET0_RX_DV保持时间	t_{RDVh}	10	—	ns	
	ET0_ERXD0到ET_ERXD3建立时间	t_{MRDs}	10	—	ns	
	ET0_ERXD0到ET_ERXD3保持时间	t_{MRDh}	10	—	ns	
	ET0_RX_ER建立时间	t_{RERs}	10	—	ns	Figure 53.72
	ET0_RX_ER保持时间	t_{RESh}	10	—	ns	
	ET0_WOL输出延迟	t_{WOLd}	1	23.5	ns	Figure 53.73

Note: 以下引脚必须使用名称后附加字母的引脚，例如"_A"、"_B"，以表示组成员身份。对于ETHERC(RMII)主机接口，测量每组的电气特性的交流部分。REF50CK0_A
REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B.
Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.



Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Figure 53.64 REF50CK0和RMII信号时序

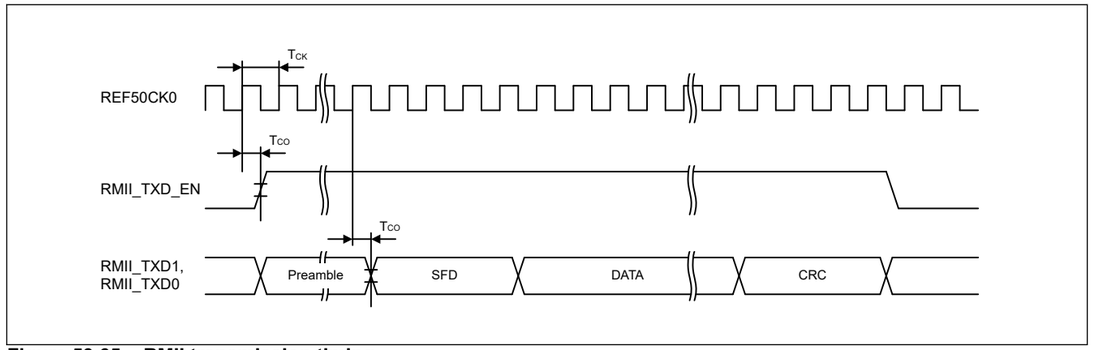


Figure 53.65 RMII transmission timing

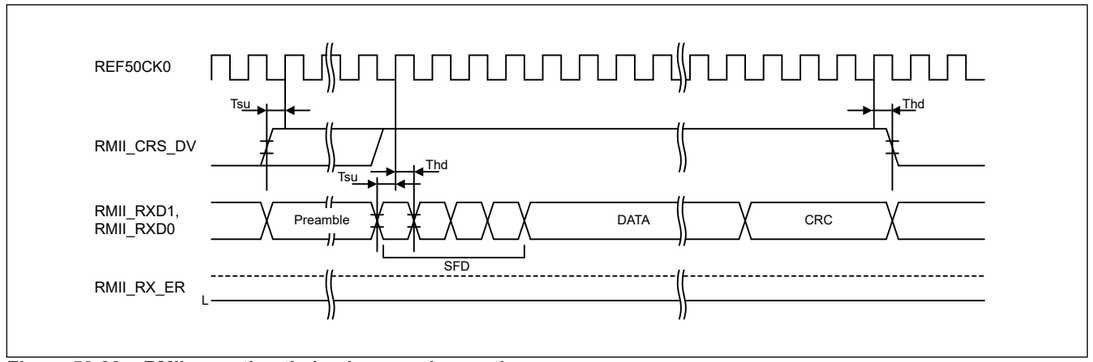


Figure 53.66 RMII reception timing in normal operation

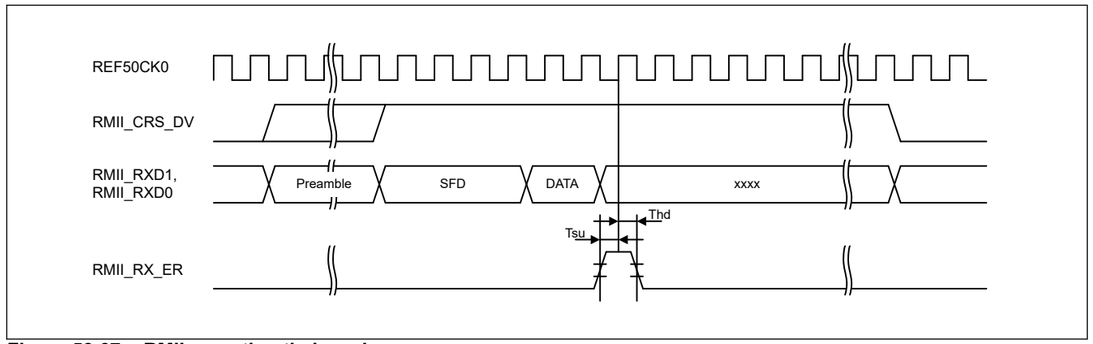


Figure 53.67 RMII reception timing when an error occurs

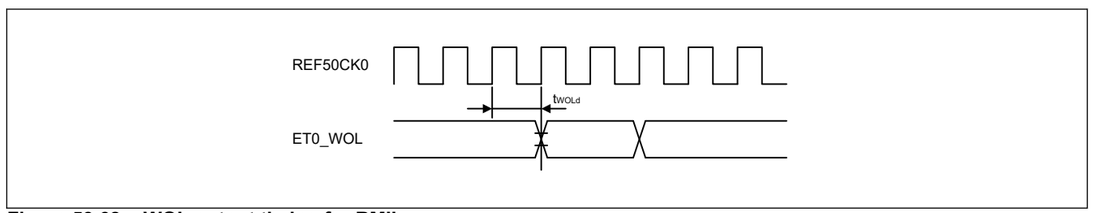


Figure 53.68 WOL output timing for RMII

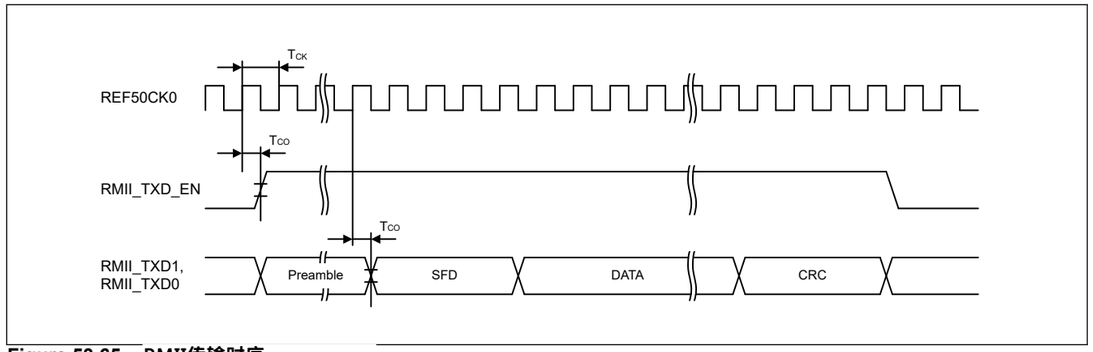


Figure 53.65 RMII传输时序

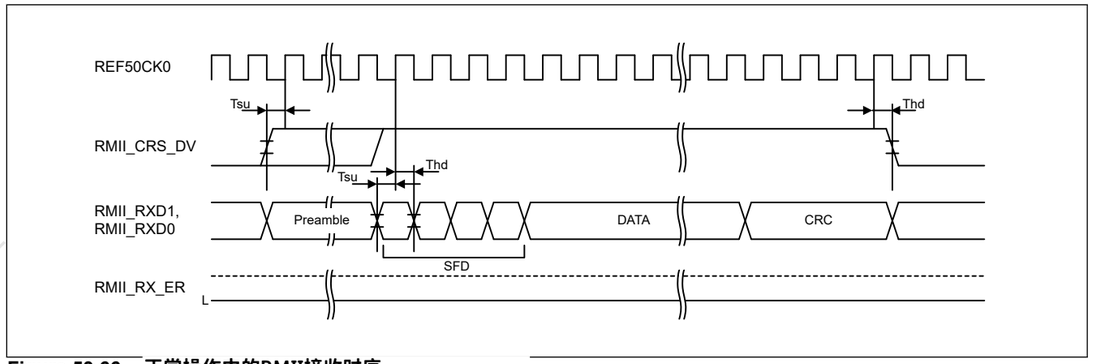


Figure 53.66 正常操作中的RMII接收时序

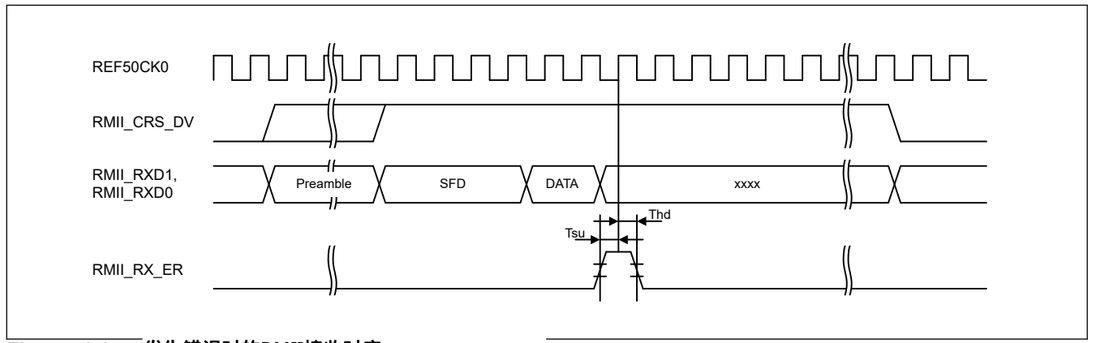


Figure 53.67 发生错误时的RMII接收时序

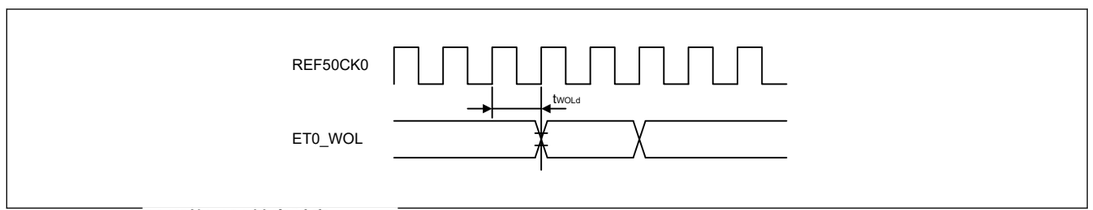


Figure 53.68 RMII的WOL输出时序

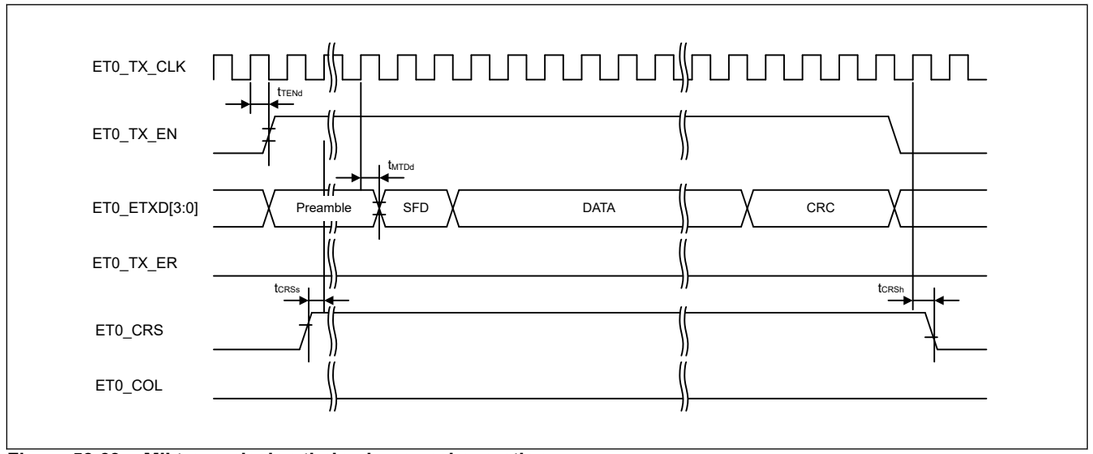


Figure 53.69 MII transmission timing in normal operation

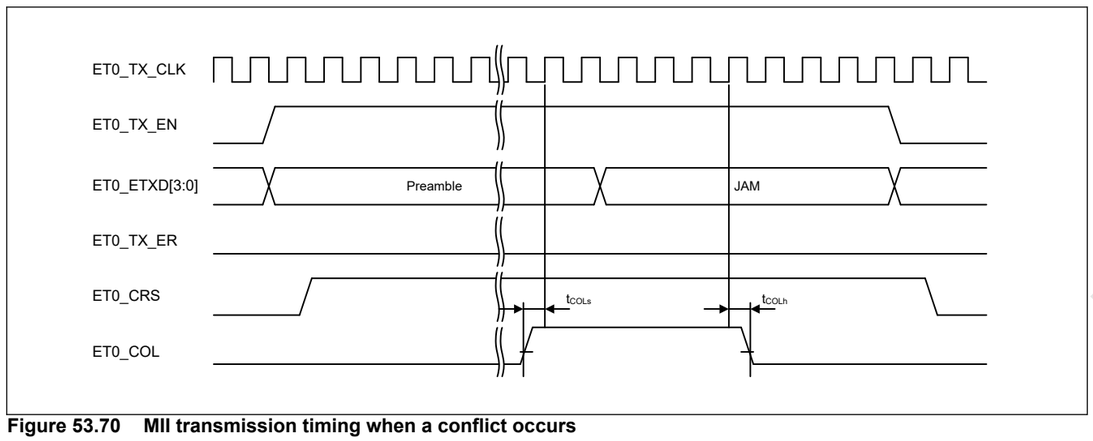


Figure 53.70 MII transmission timing when a conflict occurs

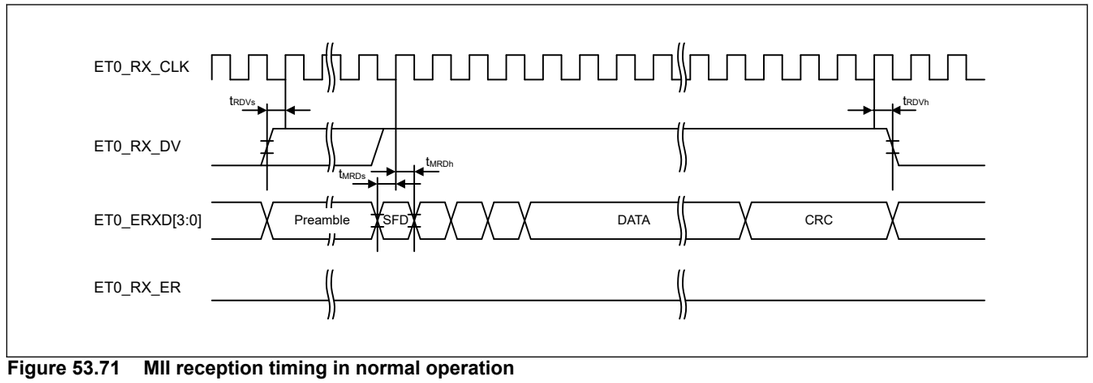


Figure 53.71 MII reception timing in normal operation

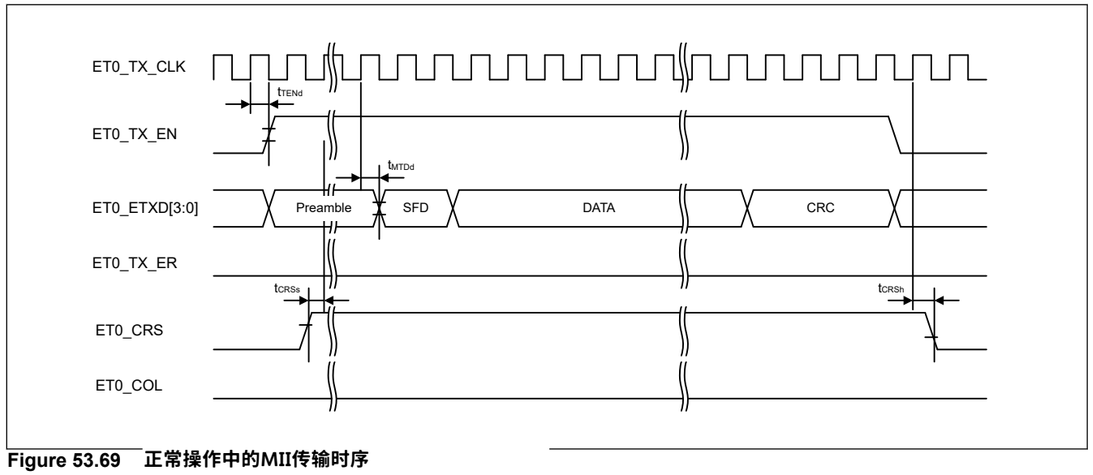


Figure 53.69 正常操作中的MII传输时序

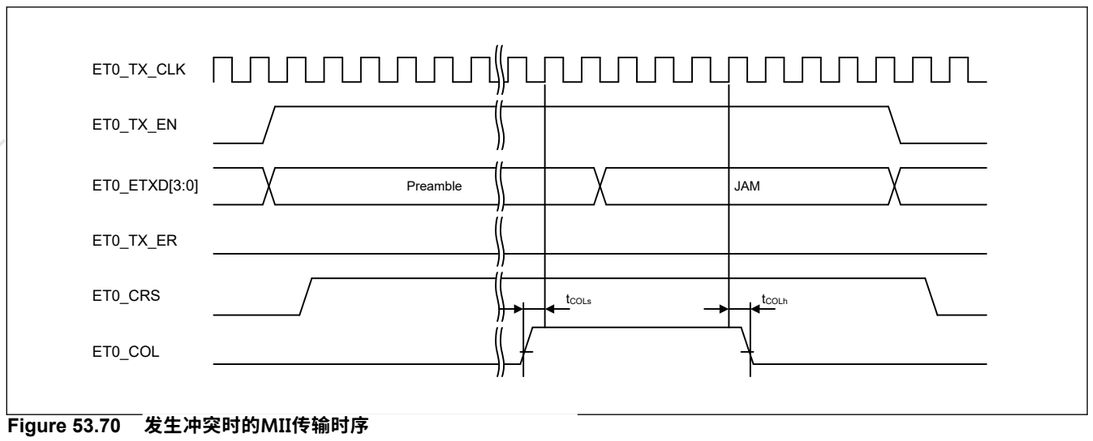


Figure 53.70 发生冲突时的MII传输时序

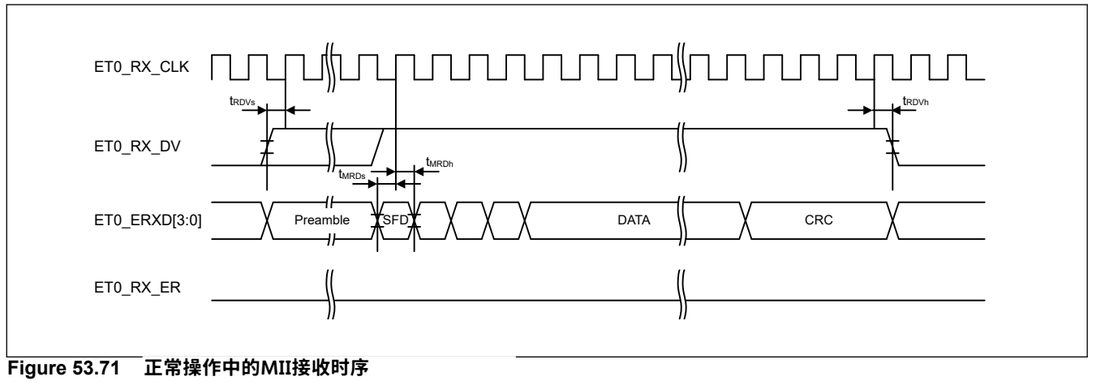


Figure 53.71 正常操作中的MII接收时序

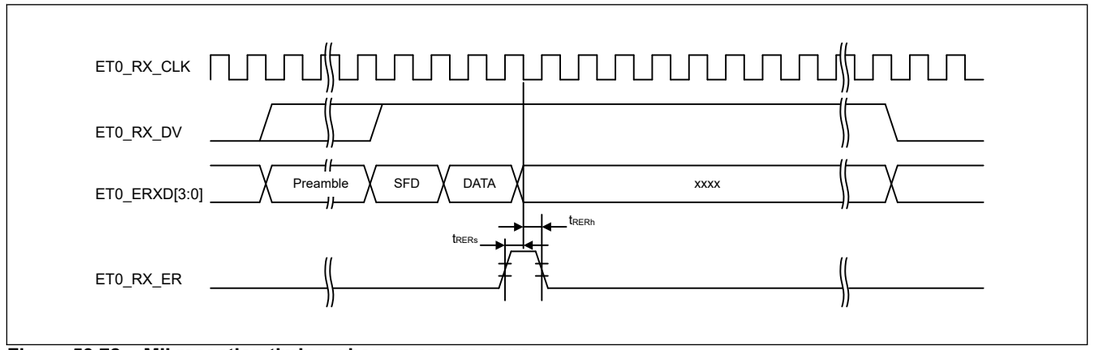


Figure 53.72 MII reception timing when an error occurs

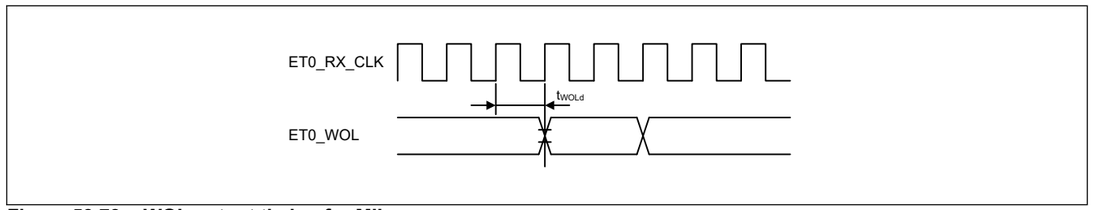


Figure 53.73 WOL output timing for MII

53.4 USB Characteristics

53.4.1 USBFS Timing

Table 53.36 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.74
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

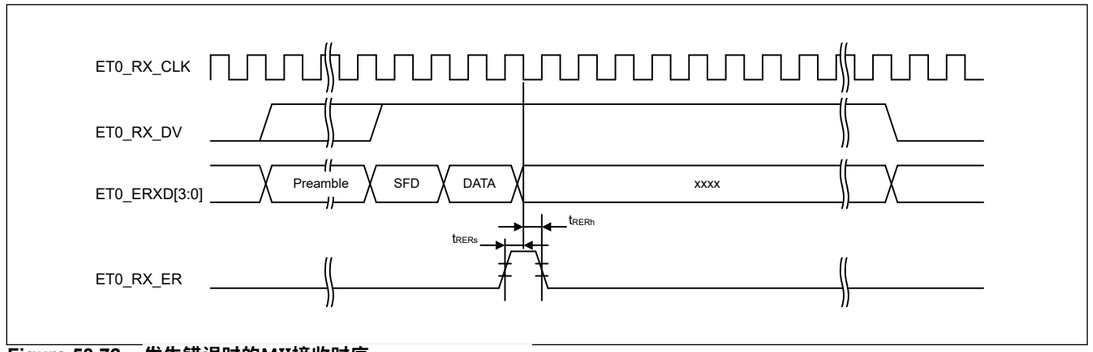


Figure 53.72 发生错误时的MII接收时序

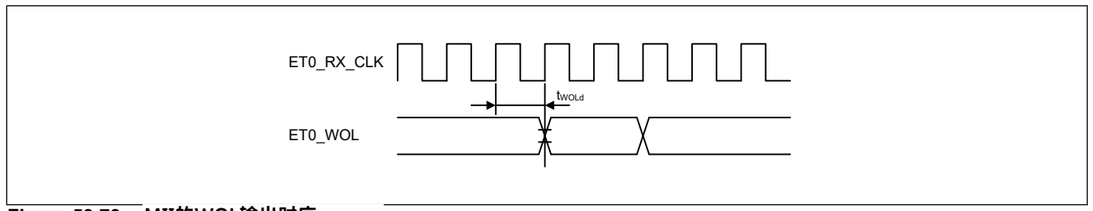


Figure 53.73 MII的WOL输出时序

53.4 USB特性

53.4.1 USBFS Timing

Table 53.36 仅主机的USBFS低速特性（USB_DP和USB_DM引脚特性）

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	—	—	V	—
	输入低电压	V_{IL}	—	—	0.8	V	—
	差分输入灵敏度	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	—	2.5	V	—
输出特性	输出高压	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	输出低电压	V_{OL}	0.0	—	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.74
	上升时间	t_{LR}	75	—	300	ns	
	秋季时间	t_{LF}	75	—	300	ns	
	上升下降时间比	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
上拉和下拉特性	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	—	24.80	kΩ	—

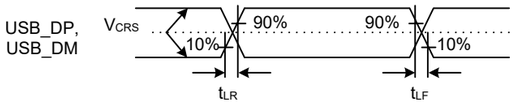


Figure 53.74 USB_DP and USB_DM output timing in low-speed mode

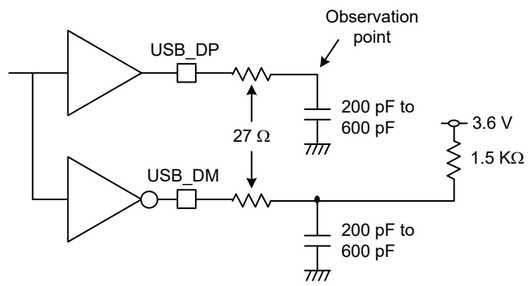


Figure 53.75 Test circuit in low-speed mode

Table 53.37 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.76
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

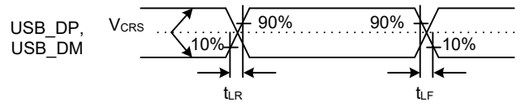


Figure 53.74 低速模式下的USB_DP和USB_DM输出时序

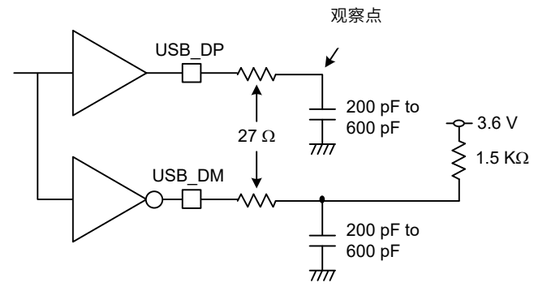


Figure 53.75 低速模式下的测试电路

Table 53.37 USBFS全速特性（USB_DP和USB_DM引脚特性）

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	—	—	V	—
	输入低电压	V_{IL}	—	—	0.8	V	—
	差分输入灵敏度	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	—	2.5	V	—
输出特性	输出高压	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	输出低电压	V_{OL}	0.0	—	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.76
	上升时间	t_{LR}	4	—	20	ns	
	秋季时间	t_{LF}	4	—	20	ns	
	上升下降时间比	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	输出电阻	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
上拉和下拉特性	设备控制器模式下的DM上拉电阻	R_{pu}	0.900	—	1.575	kΩ	空闲状态期间
			1.425	—	3.090	kΩ	在发送和接收期间
	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	—	24.80	kΩ	—

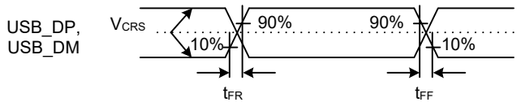


Figure 53.76 USB_DP and USB_DM output timing in full-speed mode

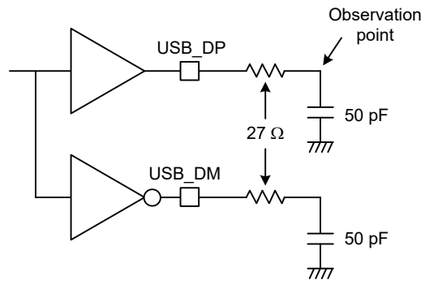


Figure 53.77 Test circuit in full-speed mode

Table 53.38 USBFS characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	—	175	μA	—
	D- sink current	I_{DM_SINK}	25	—	175	μA	—
	DCD source current	I_{DP_SRC}	7	—	13	μA	—
	Data detection voltage	V_{DAT_REF}	0.25	—	0.4	V	—
	D+ source voltage	V_{DP_SRC}	0.5	—	0.7	V	Outout current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	—	0.7	V	Outout current = 250 μA

53.4.2 USBHS Timing

Table 53.39 USBHS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—

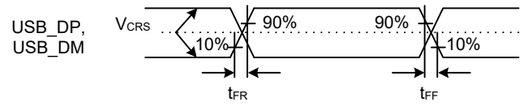


Figure 53.76 全速模式下的USB_DP和USB_DM输出时序

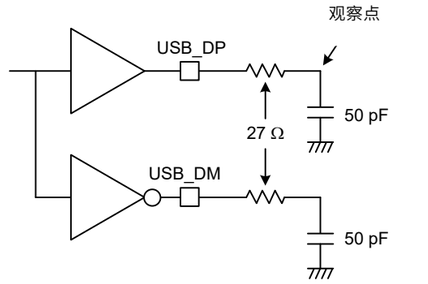


Figure 53.77 全速模式下的测试电路

Table 53.38 USBFS特性（USB_DP和USB_DM引脚特性）

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
电池充电 Specification	D+灌电流	I_{DP_SINK}	25	—	175	μA	—
	D- sink current	I_{DM_SINK}	25	—	175	μA	—
	DCD源电流	I_{DP_SRC}	7	—	13	μA	—
	数据检测电压	V_{DAT_REF}	0.25	—	0.4	V	—
	D+源电压	V_{DP_SRC}	0.5	—	0.7	V	Outout current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	—	0.7	V	Outout current = 250 μA

53.4.2 USBHS Timing

Table 53.39 仅适用于主机的USBHS低速特性（USB_DP和USB_DM引脚特性）（1of2）

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	—	—	V	—
	输入低电压	V_{IL}	—	—	0.8	V	—
	差分输入灵敏度	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	—	2.5	V	—

Table 53.39 USBHS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (2 of 2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.78
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

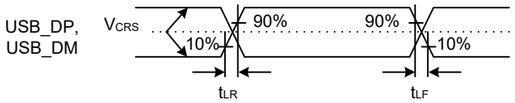


Figure 53.78 USB_DP and USB_DM output timing in low-speed mode

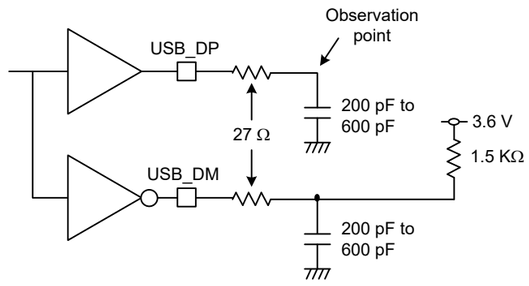


Figure 53.79 Test circuit in low-speed mode

Table 53.40 USBHS full-speed characteristics (USB_DP and USB_DM pin characteristics) (1 of 2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—

Table 53.39 仅主机的USBHS低速特性（USB_DP和USB_DM引脚特性）（2of2）

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出特性	输出高压	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	输出低电压	V_{OL}	0.0	—	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.78
	上升时间	t_{LR}	75	—	300	ns	
	秋季时间	t_{LF}	75	—	300	ns	
	上升下降时间比	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
上拉和下拉特性	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	—	24.80	kΩ	—

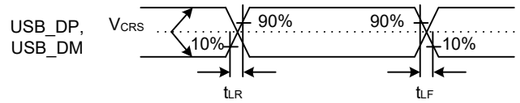


Figure 53.78 低速模式下的USB_DP和USB_DM输出时序

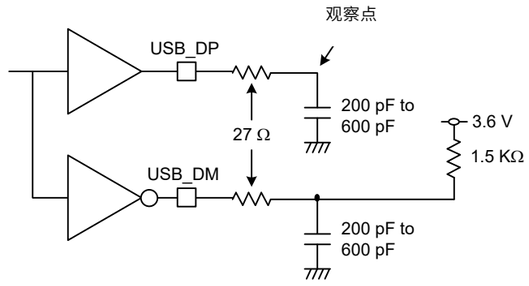


Figure 53.79 低速模式下的测试电路

Table 53.40 USBHS全速特性（USB_DP和USB_DM引脚特性）（1of2）

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	—	—	V	—
	输入低电压	V_{IL}	—	—	0.8	V	—
	差分输入灵敏度	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	—	2.5	V	—

Table 53.40 USBHS full-speed characteristics (USB_DP and USB_DM pin characteristics) (2 of 2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.80
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	40.5	—	49.5	Ω	Rs Not used (PHYSET.REPSEL[1:0] = 01b and PHYSET. HSEB = 0)
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

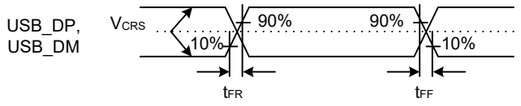


Figure 53.80 USB_DP and USB_DM output timing in full-speed mode

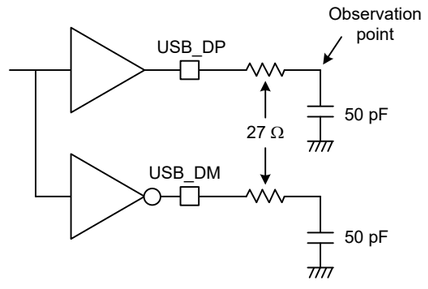


Figure 53.81 Test circuit in full-speed mode

Table 53.41 USB High Speed Characteristics (USB_DP and USB_DM Pin Characteristics) (1 of 2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Squelch detect sensitivity	VHSSQ	100	—	150	mV	Figure 53.82
	Disconnect detect sensitivity	VHSDSC	525	—	625	mV	Figure 53.83
	Common mode voltage	VHSCM	-50	—	500	mV	—

Table 53.40 USBHS全速特性（USB_DP和USB_DM引脚特性）(2of2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输出特性	输出高压	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
	输出低电压	V_{OL}	0.0	—	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 53.80
	上升时间	t_{LR}	4	—	20	ns	
	秋季时间	t_{LF}	4	—	20	ns	
	上升下降时间比	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	输出电阻	Z_{DRV}	40.5	—	49.5	Ω	Rs未使用（PHYSET.REPSEL[1:0]=01b和PHYSET.HSEB=0）
上拉和下拉特性	设备控制器模式下的DM上拉电阻	R_{pu}	0.900	—	1.575	kΩ	空闲状态期间
			1.425	—	3.090	kΩ	在发送和接收期间
	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	—	24.80	kΩ	—

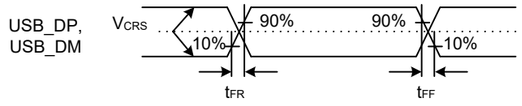


Figure 53.80 全速模式下的USB_DP和USB_DM输出时序

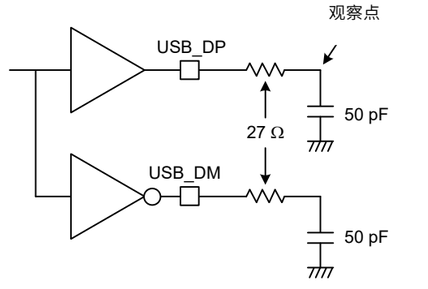


Figure 53.81 全速模式下的测试电路

Table 53.41 USB高速特性（USB_DP和USB_DM引脚特性）（1of2）

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	静噪检测灵敏度	VHSSQ	100	—	150	mV	Figure 53.82
	断开检测灵敏度	VHSDSC	525	—	625	mV	Figure 53.83
	共模电压	VHSCM	-50	—	500	mV	—

Table 53.41 USB High Speed Characteristics (USB_DP and USB_DM Pin Characteristics) (2 of 2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Output characteristics	Idle state	VHSOI	-10	—	10	mV	—
	Output high level voltage	VHSOH	360	—	440	mV	—
	Output low level voltage	VHSOL	-10	—	10	mV	—
	Chirp J output voltage (difference)	VCHIRPJ	700	—	1100	mV	—
	Chirp K output voltage (difference)	VCHIRPK	-900	—	-500	mV	—
AC characteristics	Rise time	tHSR	500	—	—	ps	—
	Fall time	tHSF	500	—	—	ps	Figure 53.84
	Output resistance	ZHSDRV	40.5	—	49.5	Ω	—

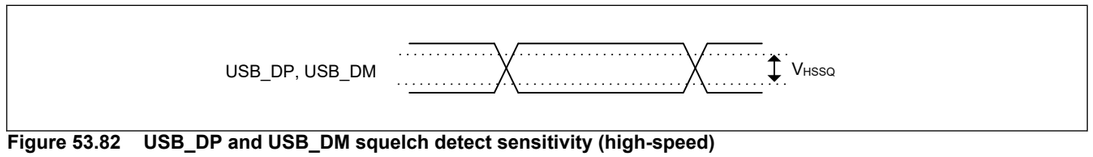


Figure 53.82 USB_DP and USB_DM squelch detect sensitivity (high-speed)

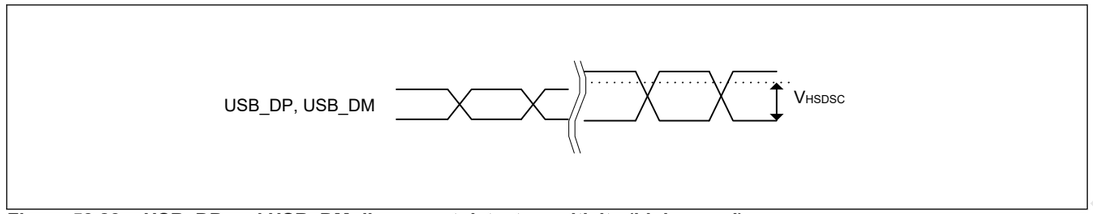


Figure 53.83 USB_DP and USB_DM disconnect detect sensitivity (high-speed)

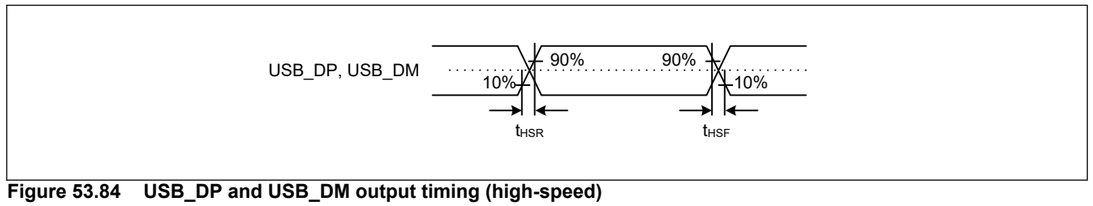


Figure 53.84 USB_DP and USB_DM output timing (high-speed)

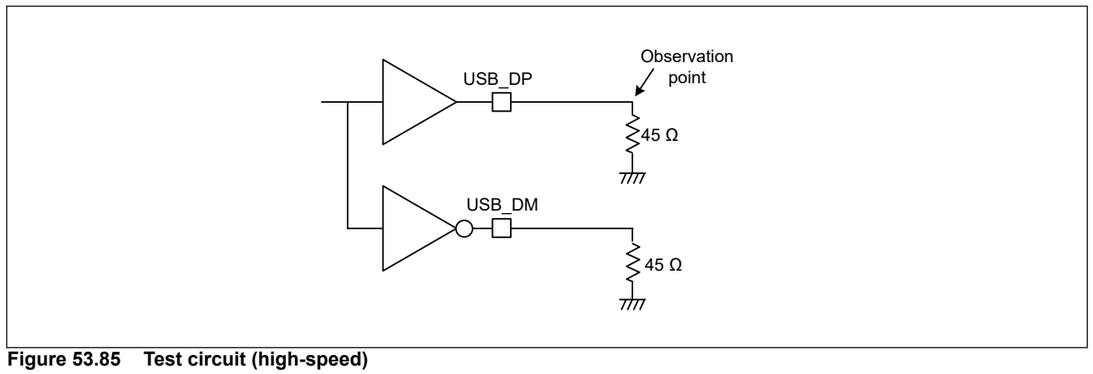


Figure 53.85 Test circuit (high-speed)

Table 53.41 USB高速特性（USB_DP和USB_DM引脚特性）（2之2）

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Typ	Max	Unit	测试条件
输出特性	空闲状态	VHSOI	-10	—	10	mV	—
	输出高电平电压	VHSOH	360	—	440	mV	—
	输出低电平电压	VHSOL	-10	—	10	mV	—
	啁啾J输出电压（差值）	VCHIRPJ	700	—	1100	mV	—
	啁啾K输出电压（差）	VCHIRPK	-900	—	-500	mV	—
交流特性	上升时间	tHSR	500	—	—	ps	—
	秋季时间	tHSF	500	—	—	ps	Figure 53.84
	输出电阻	ZHSDRV	40.5	—	49.5	Ω	—

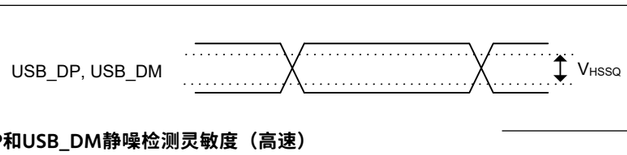


Figure 53.82 USB_DP和USB_DM静噪检测灵敏度（高速）

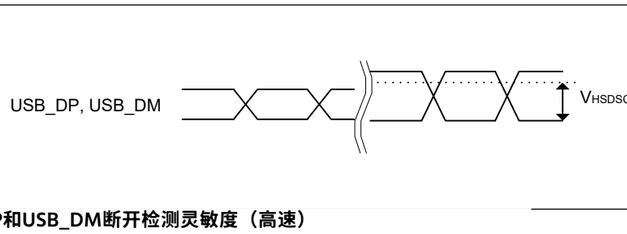


Figure 53.83 USB_DP和USB_DM断开检测灵敏度（高速）

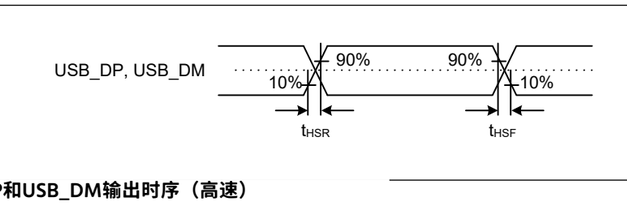


Figure 53.84 USB_DP和USB_DM输出时序（高速）

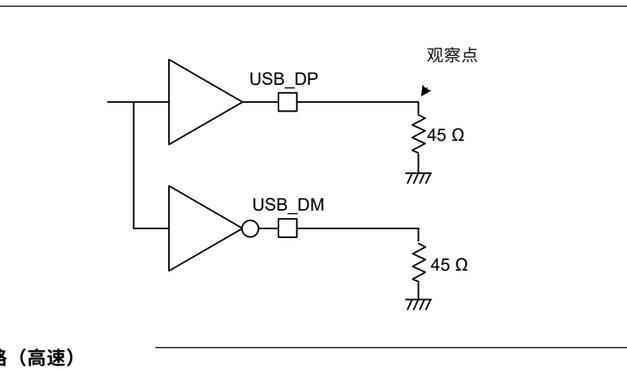


Figure 53.85 测试电路（高速）

Table 53.42 USBHS high-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	—	175	μA	—
	D- sink current	I_{DM_SINK}	25	—	175	μA	—
	DCD source current	I_{DP_SRC}	7	—	13	μA	—
	Data detection voltage	V_{DAT_REF}	0.25	—	0.4	V	—
	D+ source voltage	V_{DP_SRC}	0.5	—	0.7	V	Outout current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	—	0.7	V	Outout current = 250 μA

53.5 ADC12 Characteristics

Table 53.43 A/D conversion characteristics for unit 0

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
High-precision high-speed channels (AN000 to AN005)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	μs	Sampling in 13 states
		Max. = 400 Ω	0.40 (0.14)*2	—	—	μs	Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision normal-speed channels (AN006 to AN010, AN012, AN013)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	μs	Sampling in 33 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of pins AN000 to AN010, AN012, AN013 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note: When both unit0 and unit1 are used, do not select the following analog input combinations at the same time except the interleave function. If selected, values might not fall within the indicated ranges.
- AN100 and AN000 or AN001 or AN002
- AN101 and AN000 or AN001 or AN002 or AN003
- AN102 and AN000 or AN001 or AN002 or AN003 or AN004

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Table 53.42 USBHS高速特性（USB_DP和USB_DM引脚特性）

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
电池充电 Specification	D+灌电流	I_{DP_SINK}	25	—	175	μA	—
	D- sink current	I_{DM_SINK}	25	—	175	μA	—
	DCD源电流	I_{DP_SRC}	7	—	13	μA	—
	数据检测电压	V_{DAT_REF}	0.25	—	0.4	V	—
	D+源电压	V_{DP_SRC}	0.5	—	0.7	V	Outout current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	—	0.7	V	Outout current = 250 μA

53.5 ADC12 Characteristics

Table 53.43 单元0的AD转换特性

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	最大	单位	测试条件
Frequency			1	—	50	MHz	—
模拟输入电容			—	—	30	pF	—
量化误差			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
高精度高速通道（AN000至AN005）	转换时间*1 (operation at PCLKC = 50 MHz)	允许的信号源阻抗 Max.=1kΩ	0.52 (0.26)*2	—	—	μs	在13个州进行抽样
		Max. = 400 Ω	0.40 (0.14)*2	—	—	μs	在7种状态下采样VCC=AVCC0=3.0至3.6 V3.0V≤VREFH0≤AVCC0
	偏移误差		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	绝对精度		—	±2.0	±4.5	LSB	—
	DNL微分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
高精度常速通道（AN006至AN010、AN012、AN013）	转换时间*1 (Operation at PCLKC = 50 MHz)	允许的信号源阻抗 Max.=1kΩ	0.92 (0.66)*2	—	—	μs	在33个州进行抽样
	偏移误差		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	绝对精度		—	±2.0	±4.5	LSB	—
	DNL微分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果在AD转换期间发生访问，则值可能不在指定范围内。使用12位AD转换器时，不允许使用引脚AN000至AN010、AN012、AN013作为数字输出。

这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note: 当同时使用unit0和unit1时，除了交错功能外，不要同时选择以下模拟输入组合。如果选中，值可能不在指定范围内。●

AN100和AN000或AN001或AN002
- AN101和AN000或AN001或AN002或AN003
- AN102和AN000或AN001或AN002或AN003或AN004

注1.转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

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Note 2. Values in parentheses indicate the sampling time.

Table 53.44 A/D conversion characteristics for unit 1

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
High-precision high-speed channels (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	µs	Sampling in 13 states
		Max. = 400 Ω	0.40 (0.14)*2	—	—	µs	Sampling in 7 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision normal-speed channels (AN116 to AN128)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of pins AN100 to AN102 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note: When both unit0 and unit1 are used, do not select the following analog input combinations at the same time except the interleave function. If selected, values might not fall within the indicated ranges.
- AN100 and AN000 or AN001 or AN002
- AN101 and AN000 or AN001 or AN002 or AN003
- AN102 and AN000 or AN001 or AN002 or AN003 or AN004

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 53.45 A/D conversion characteristics for interleaving (1 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter	Min	Typ	Max	Unit	Test conditions
Frequency	1	—	50	MHz	—
Analog input capacitance	—	—	30	pF	—
Quantization error	—	±0.5	—	LSB	—
Resolution	—	—	12	Bits	—

注2：括号内的数值表示采样时间。

Table 53.44 单元1的AD转换特性

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	最大	单位	测试条件
Frequency			1	—	50	MHz	—
模拟输入电容			—	—	30	pF	—
量化误差			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
高精度高速通道（AN100至AN102）	转换时间*1 (Operation at PCLKC = 50 MHz)	允许的信号源阻抗 Max.=1kΩ	0.52 (0.26)*2	—	—	µs	在13个州进行抽样
		Max. = 400 Ω	0.40 (0.14)*2	—	—	µs	在7种状态下采样VCC=AVCC0=3.0至3.6 V3.0V≤VREFH≤AVCC0
	偏移误差		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	绝对精度		—	±2.0	±4.5	LSB	—
	DNL微分非线性误差		—	±0.5	±1.5	LSB	—
	INL积分非线性误差		—	±1.0	±2.5	LSB	—
正常精度正常速度通道（AN116至AN128）	转换时间*1 (Operation at PCLKC = 50 MHz)	允许的信号源阻抗 Max.=1kΩ	0.92 (0.66)*2	—	—	µs	在33个州进行抽样
	偏移误差		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	绝对精度		—	±2.0	±7.5	LSB	—
	DNL微分非线性误差		—	±0.5	±4.5	LSB	—
	INL积分非线性误差		—	±1.0	±5.5	LSB	—

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果在AD转换期间发生访问，则值可能不在指定范围内。使用12位AD转换器时，不允许将引脚AN100到AN102用作数字输出。

这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note: 当同时使用unit0和unit1时，除了交错功能外，不要同时选择以下模拟输入组合。如果选中，值可能不在指定范围内。●

AN100和AN000或AN001或AN002
- AN101和AN000或AN001或AN002或AN003
- AN102和AN000或AN001或AN002或AN003或AN004

注1.转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

注2：括号内的数值表示采样时间。

Table 53.45 交错的AD转换特性(1of2)

Conditions: PCLKC = 1 to 50 MHz

Parameter	Min	Typ	最大	单位	测试条件
Frequency	1	—	50	MHz	—
模拟输入电容	—	—	30	pF	—
量化误差	—	±0.5	—	LSB	—
Resolution	—	—	12	Bits	—

Table 53.45 A/D conversion characteristics for interleaving (2 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision high-speed channels (AN000 & AN100, AN001 & AN101, AN002 & AN102))	Conversion time*1 (operation at PCLKC = 50 MHz)	Max. = 400 Ω	0.20	—	—	µs	Sampling in 7states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±3.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±3.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of pins AN000 to AN010, AN012, AN013, AN100 to AN102 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Table 53.46 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	—
Sampling time	4.15	—	—	µs	—

Table 53.45 交错的AD转换特性(2of2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	最大	单位	测试条件
High-precision high-speed channels (AN000 & AN100, AN001 & AN101, AN002 & AN102))	转换时间*1 (operation at PCLKC = 50 MHz)	Max. = 400 Ω	0.20	—	—	µs	在7个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	偏移误差		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	绝对精度		—	±2.0	±4.5	LSB	—
	DNL微分非线性误差		—	±0.5	±3.5	LSB	—
	INL积分非线性误差		—	±1.0	±3.5	LSB	—

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果在AD转换期间发生访问，则值可能不在指定范围内。使用12位AD转换器时，不允许使用引脚AN000至AN010、AN012、AN013、AN100至AN102作为数字输出。这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

注1.转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

Table 53.46 AD内部参考电压特性

Parameter	Min	Typ	Max	Unit	测试条件
AD内部参考电压	1.13	1.18	1.23	V	—
采样时间	4.15	—	—	µs	—

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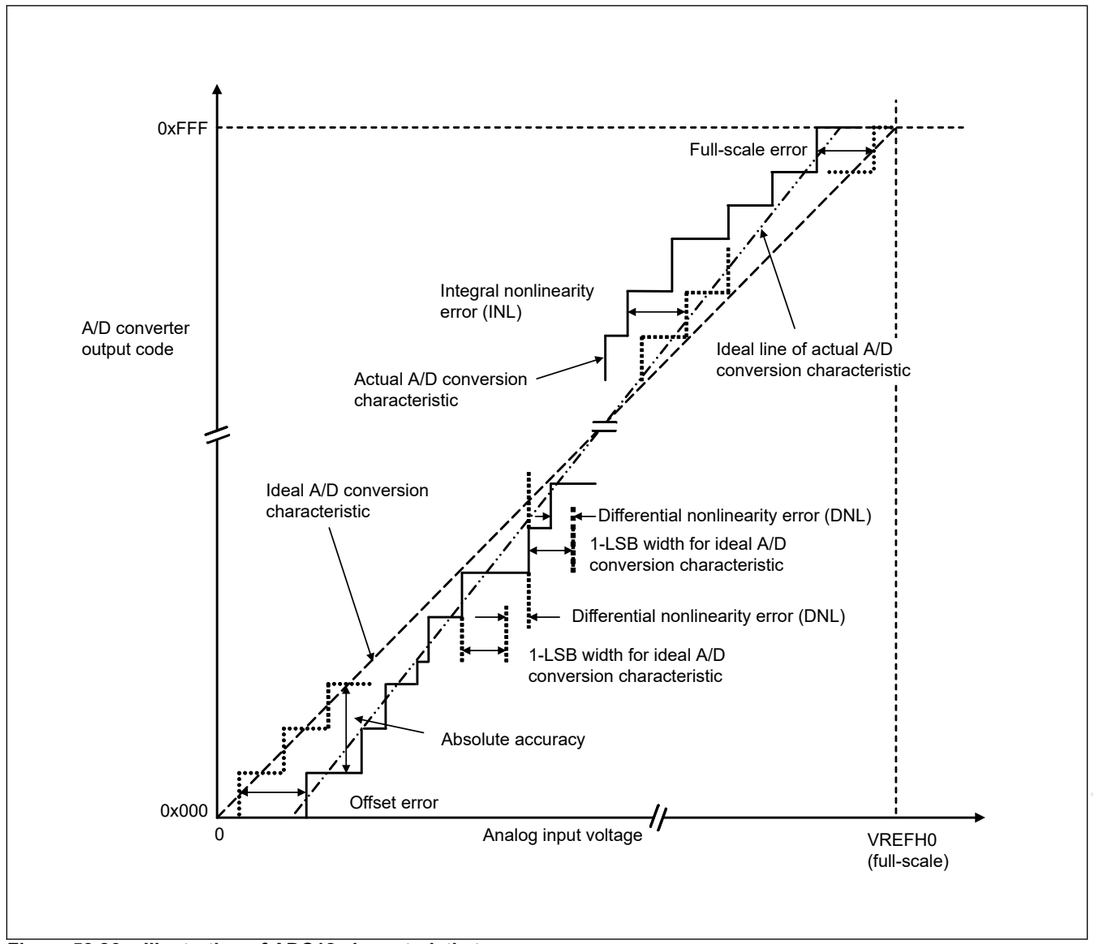

Figure 53.86 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

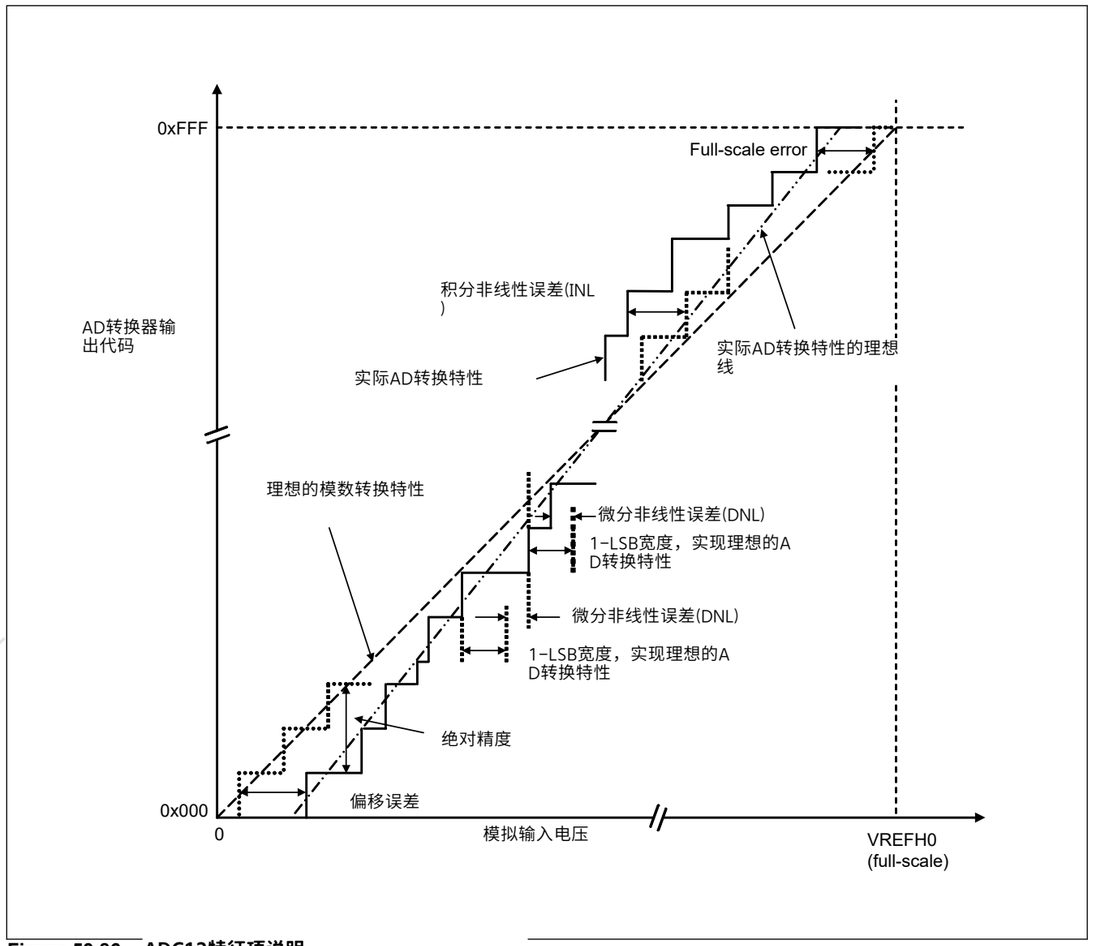

Figure 53.86 ADC12特征项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压可以满足基于理论模数转换特性输出等码的预期.例如，如果使用12位分辨率且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在0x003到0x00D的范围内，尽管从理论上的AD转换特性可以预期输出代码为0x008。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

53.6 DAC12 Characteristics

Table 53.47 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VREFH	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VREFH – 0.2	V	—

53.7 TSN Characteristics

Table 53.48 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

53.8 OSC Stop Detect Characteristics

Table 53.49 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 53.87

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

53.6 DAC12 Characteristics

Table 53.47 DA转换特性

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	—	—	12	Bits	—
无输出放大器					
绝对精度	—	—	±24	LSB	阻性负载2MΩ
INL	—	±2.0	±8.0	LSB	阻性负载2MΩ
DNL	—	±1.0	±2.0	LSB	—
输出阻抗	—	8.5	—	kΩ	—
转换时间	—	—	3	µs	电阻负载2MΩ，电容负载20pF
输出电压范围	0	—	VREFH	V	—
带输出放大器					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
转换时间	—	—	4.0	µs	—
阻性负载	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
输出电压范围	0.2	—	VREFH – 0.2	V	—

53.7 TSN Characteristics

Table 53.48 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	—	—	± 1.0	—	°C	—
温度斜率	—	—	4.0	—	mV/°C	—
输出电压（25°C时）	—	—	1.24	—	V	—
温度传感器启动时间	t_{START}	—	—	30	µs	—
采样时间	—	4.15	—	—	µs	—

53.8 OSC停止检测特性

Table 53.49 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	—	—	1	ms	Figure 53.87

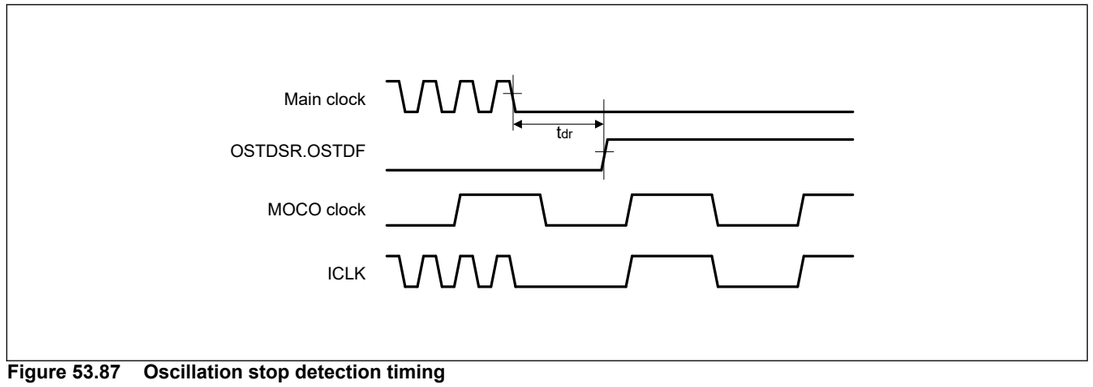

Figure 53.87 Oscillation stop detection timing

53.9 POR and LVD Characteristics

Table 53.50 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 53.88
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 53.89
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 53.90
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 53.91
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 53.88
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 53.89
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 53.90
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 53.91
Minimum VCC down time*1			t_{VOFF}	200	—	—	µs	Figure 53.88, Figure 53.89
Response delay			t_{det}	—	—	200	µs	Figure 53.89 to Figure 53.91
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	µs	Figure 53.90, Figure 53.91
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

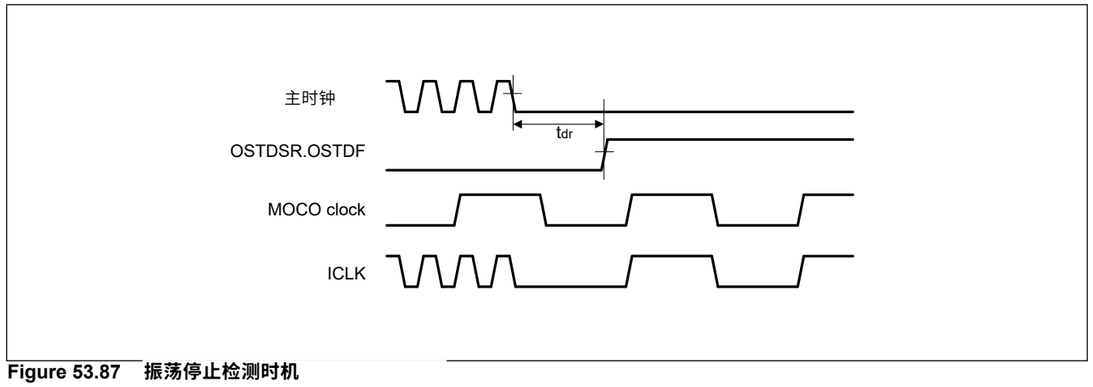

Figure 53.87 振荡停止检测时机

53.9 POR和LVD特性

Table 53.50 上电复位电路及电压检测电路特性（一）

Parameter			Symbol	Min	Typ	Max	单元	测试条件
电压检测电平	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 53.88
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	电压检测电路（LVD0）		V_{det0_1}	2.84	2.94	3.04		Figure 53.89
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	电压检测电路（LVD1）		V_{det1_1}	2.89	2.99	3.09		Figure 53.90
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	电压检测电路（LVD2）		V_{det2_1}	2.89	2.99	3.09		Figure 53.91
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
内部复位时间	上电复位时间		t_{POR}	—	4.5	—	ms	Figure 53.88
	LVD0复位时间		t_{LVD0}	—	0.51	—		Figure 53.89
	LVD1复位时间		t_{LVD1}	—	0.38	—		Figure 53.90
	LVD2复位时间		t_{LVD2}	—	0.38	—		Figure 53.91
最小VCC停机时间*1			t_{VOFF}	200	—	—	µs	Figure 53.88, Figure 53.89
响应延迟			t_{det}	—	—	200	µs	图53.89至 Figure 53.91
LVD操作稳定时间（启用LVD后）			$t_{d(E-A)}$	—	—	10	µs	Figure 53.90, Figure 53.91
迟滞宽度（LVD1和LVD2）			V_{LVH}	—	70	—	mV	

注1.最小VCC停机时间是指VCC低于电压检测电平VPOR、Vdet0、Vdet1和Vdet2用于POR和LVD。

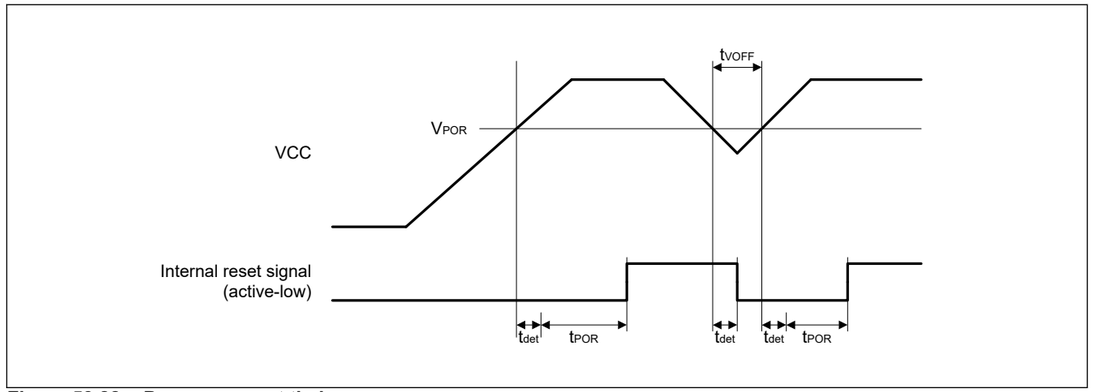

Figure 53.88 Power-on reset timing

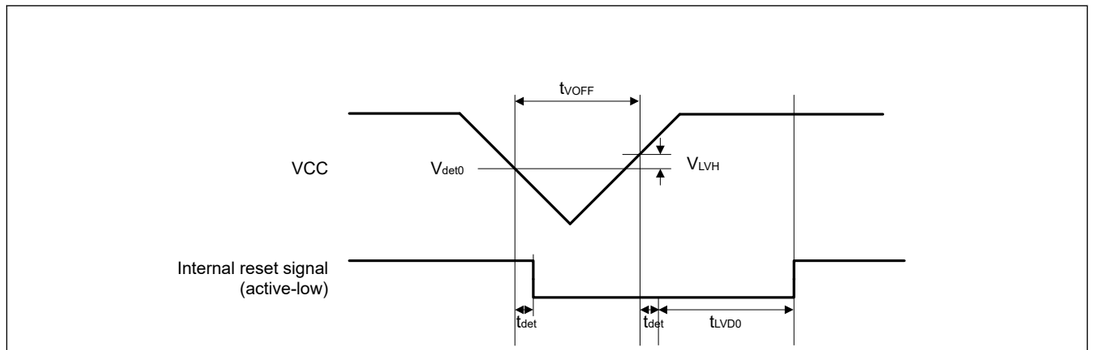

Figure 53.89 Voltage detection circuit timing (V_{det0})

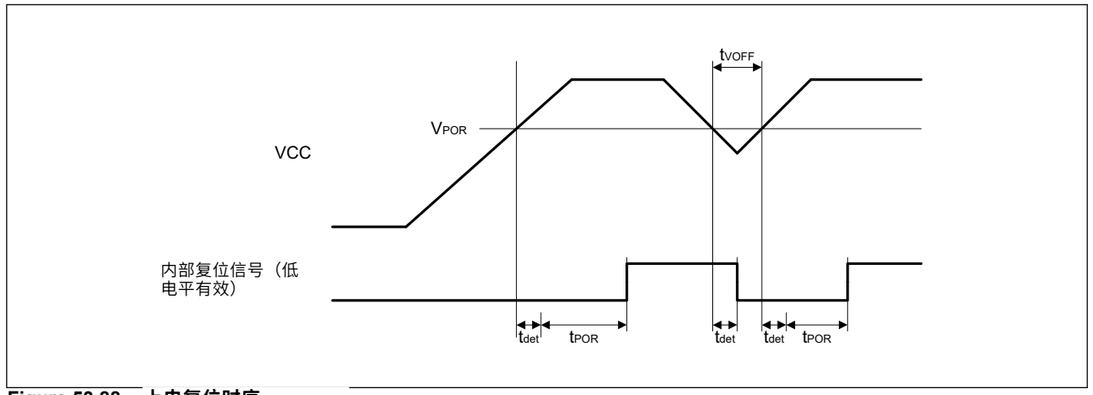

Figure 53.88 上电复位时序

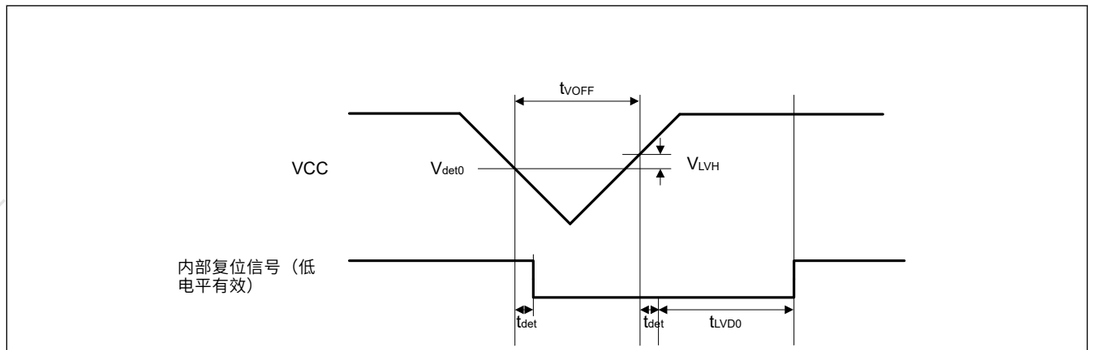

Figure 53.89 电压检测电路时序（Vdet0）

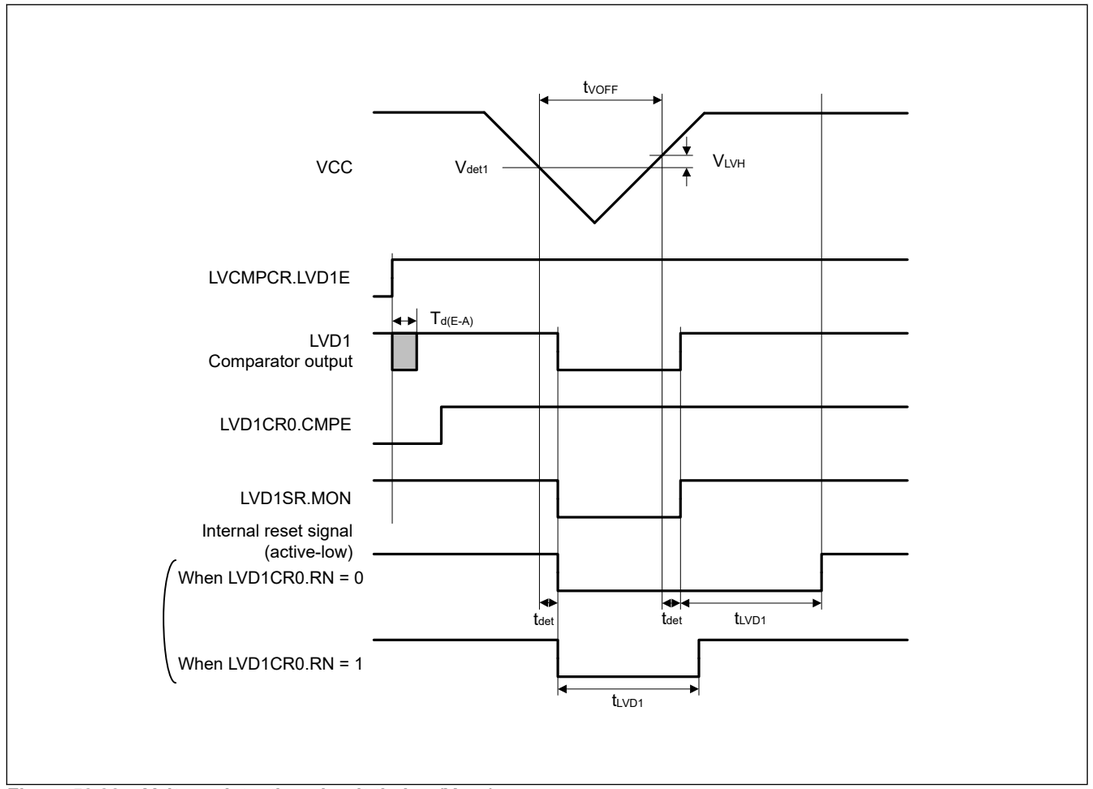

Figure 53.90 Voltage detection circuit timing (V_{det1})

Figure 53.90 Voltage detection circuit timing (V_{det1})

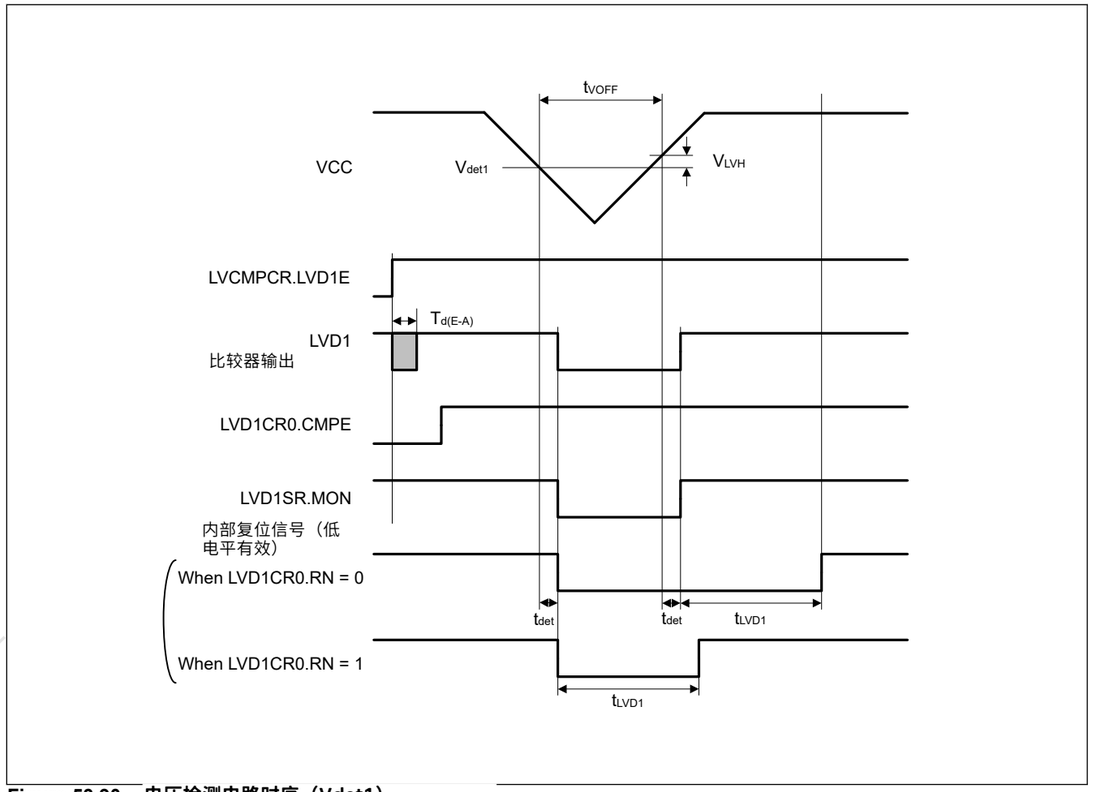

Figure 53.90 电压检测电路时序（Vdet1）

Figure 53.90 电压检测电路时序（Vdet1）

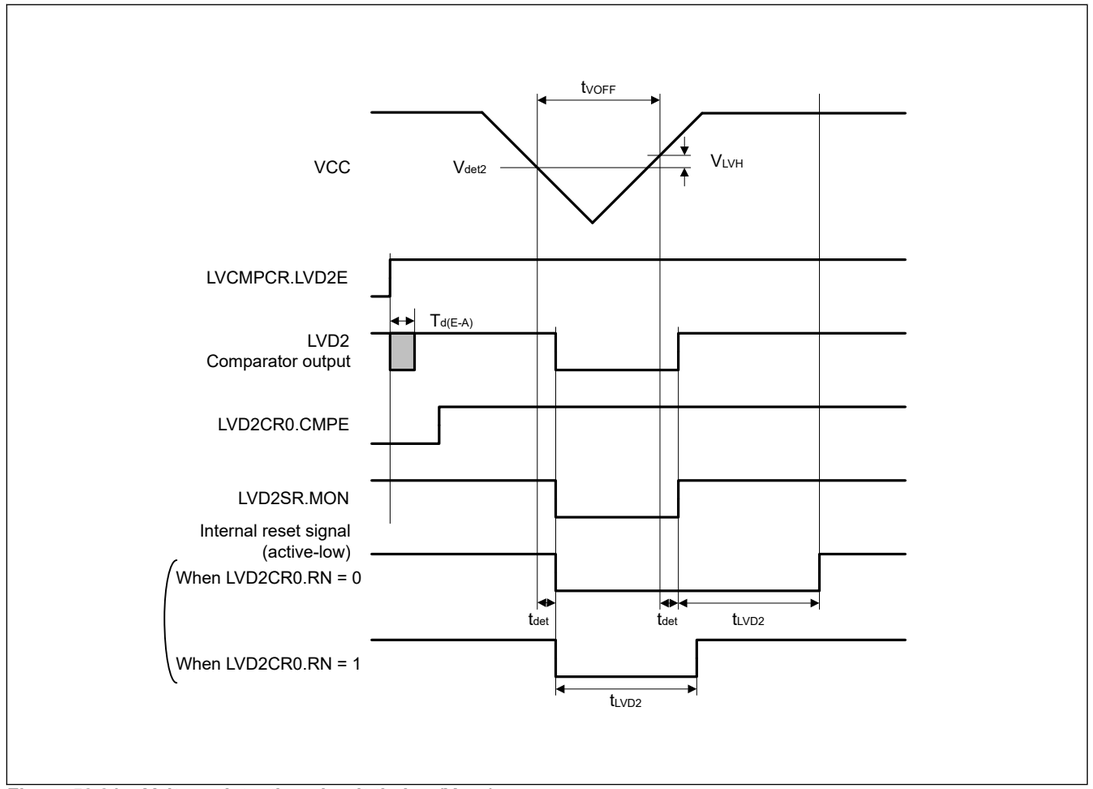

Figure 53.91 Voltage detection circuit timing (V_{det2})

53.10 VBATT Characteristics

Table 53.51 Battery backup function characteristics

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.65 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 53.92
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	—	—	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	µs	
VBATT low voltage detection level	$V_{battldet}$	1.8	1.9	2.0	V	Figure 53.93
Minimum VBATT down time	$t_{BATTOFF}$	200	—	—	µs	
Response delay	$t_{BATTdet}$	—	—	200	µs	
VBATT monitor operation stabilization time (after VBATTMNSELR.VBATTMNSEL is changed to 1)	$t_{d(E-A)}$	—	—	20	µs	
VBATT current increase (when VBATTMNSELR.VBATTMNSEL is 1 compared to the case that VBATTMNSELR.VBATTMNSEL is 0)	$I_{VBATTSEL}$	—	140	350	nA	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

Note 1. Low CL crystal cannot be used below VBATT = 1.8V.

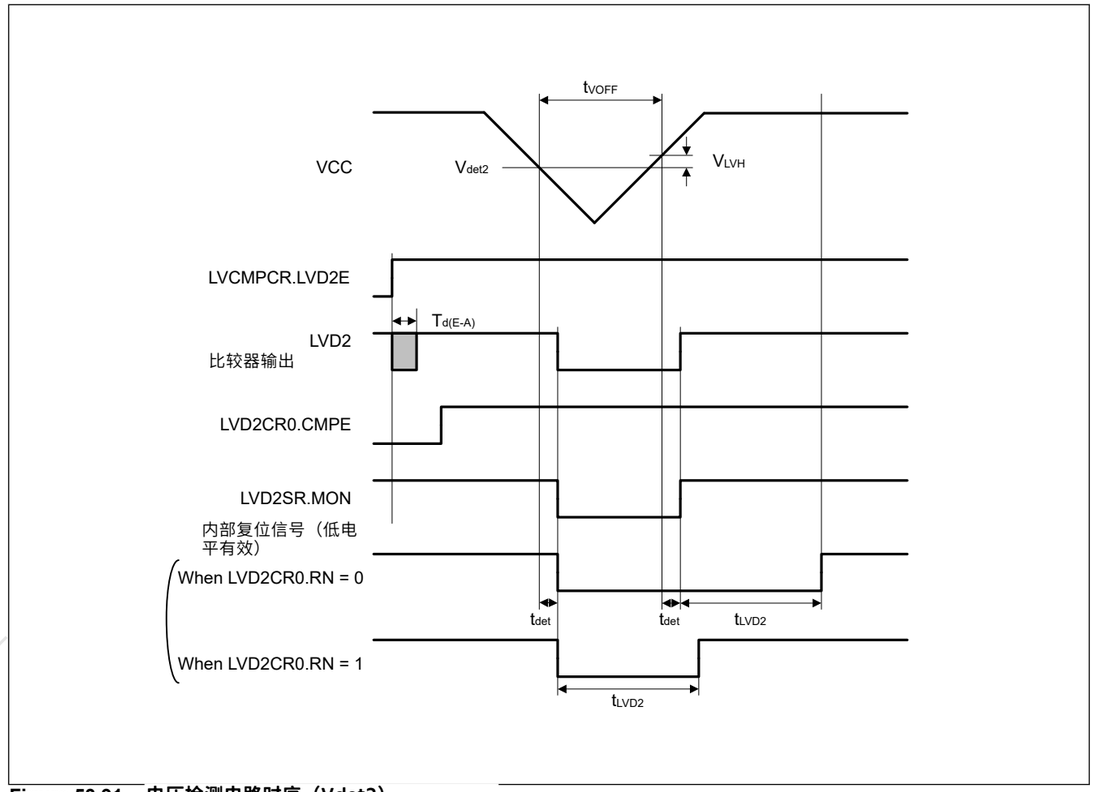

Figure 53.91 电压检测电路时序（Vdet2）

53.10 VBATT Characteristics

Table 53.51 电池备份功能特点

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.65 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
切换到备用电池的电压电平	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 53.92
VCC压降引起的电源切换下限VBATT电压	V_{BATTSW}	2.70	—	—	V	
启动电源切换的VCC-off周期	$t_{VOFFBATT}$	200	—	—	µs	
VBATT低电压检测电平	$V_{battldet}$	1.8	1.9	2.0	V	Figure 53.93
最短VBATT停机时间	$t_{BATTOFF}$	200	—	—	µs	
响应延迟	$t_{BATTdet}$	—	—	200	µs	
VBATT监视器运行稳定时间（VBATTMNSELR.VBATTMNSEL变为1后）	$t_{d(E-A)}$	—	—	20	µs	
VBATT电流增加（当与VBATTMNSELR.VBATTMNSEL为0的情况相比，VBATTMNSELR.VBATTMNSEL为1）	$I_{VBATTSEL}$	—	140	350	nA	

Note: 开始电源切换的VCC-off周期表示VCC低于切换到备用电池的电压电平最小值(VDETBATT)的周期。

注1.低于VBATT=1.8V时不能使用低CL晶振。

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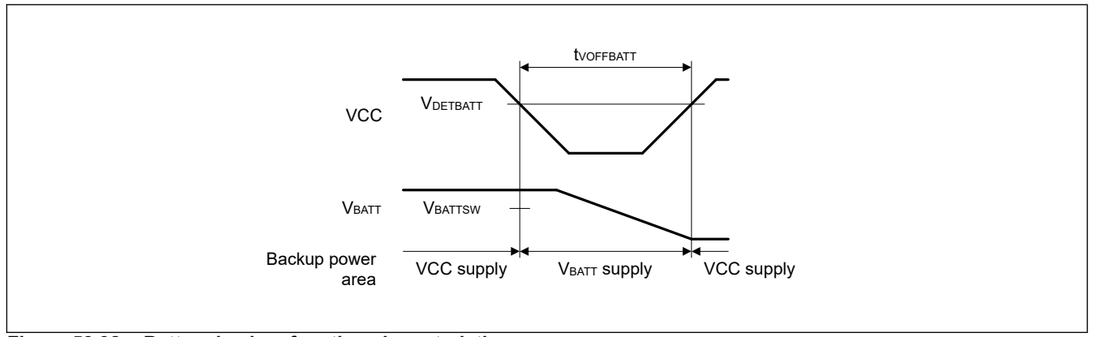

Figure 53.92 Battery backup function characteristics

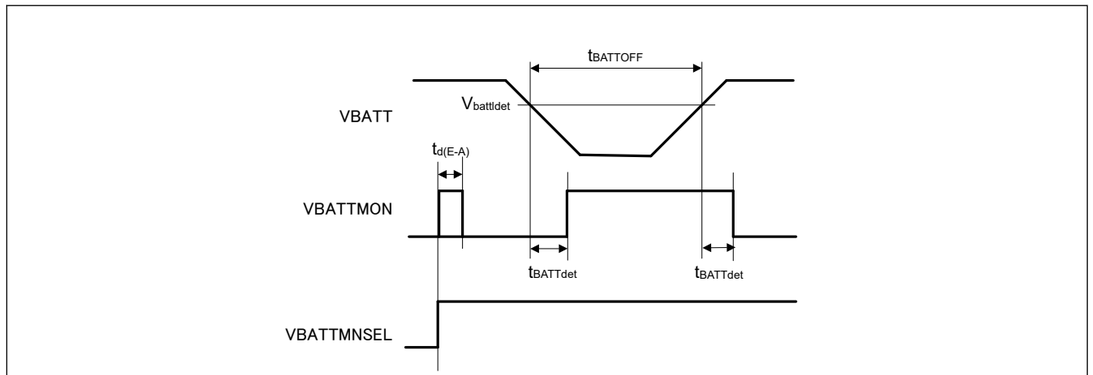

Figure 53.93 Battery backup function characteristics

53.11 CTSU Characteristics

Table 53.52 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	—
TS pin capacitive load	C_{base}	—	—	50	pF	—
Permissible output high current	ΣI_{oH}	—	—	-40	mA	When the mutual capacitance method is applied

53.12 Flash Memory Characteristics

53.12.1 Code Flash Memory Characteristics

Table 53.53 Code flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	

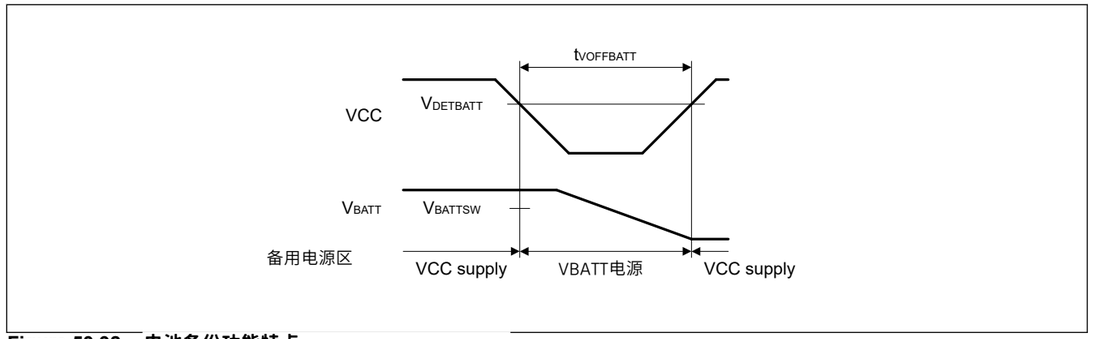

Figure 53.92 电池备份功能特点

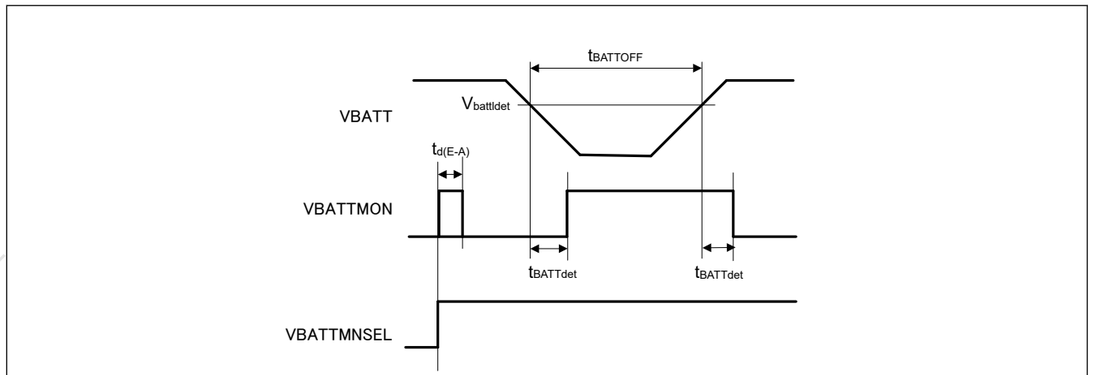

Figure 53.93 电池备份功能特点

53.11 CTSU Characteristics

Table 53.52 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C_{tscap}	9	10	11	nF	—
TS引脚容性负载	C_{base}	—	—	50	pF	—
允许输出大电流	ΣI_{oH}	—	—	-40	mA	应用互电容法时

53.12 闪存特性

53.12.1 代码闪存特性

Table 53.53 代码闪存特性(1of2)

条件：编程或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	Typ*6	Max	Min	Typ*6	Max		
编程时间NPEC≤100次	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	

Table 53.53 Code flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	
Suspend delay during programming		t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time		t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5		t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode		t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode		t_{REET}	—	—	144	—	—	80	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2		t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

Table 53.53 代码闪存特性(2of2)

条件：编程或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	Typ*6	Max	Min	Typ*6	Max		
编程时间NPEC>10 0次	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
擦除时间 NPEC≤100次	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
擦除时间 NPEC>100次	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	
编程期间暂停延迟		t_{SPD}	—	—	264	—	—	120	µs	
编程恢复时间		t_{PRT}	—	—	110	—	—	50	µs	
挂起优先模式下擦除期间的第一个挂起延迟		t_{SESD1}	—	—	216	—	—	120	µs	
挂起优先模式下擦除期间的第二挂起延迟		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
擦除优先模式下擦除期间的挂起延迟		t_{SEED}	—	—	1.7	—	—	1.7	ms	
挂起优先模式擦除期间的第一次擦除恢复时间*5		t_{REST1}	—	—	1.7	—	—	1.7	ms	
挂起优先模式下擦除期间的第二次擦除恢复时间		t_{REST2}	—	—	144	—	—	80	µs	
在擦除优先模式下擦除期间擦除恢复时间		t_{REET}	—	—	144	—	—	80	µs	
强制停止命令		t_{FD}	—	—	32	—	—	20	µs	
数据保持时间*2		t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

注2.这表示在指定范围内执行重新编程时特性的最小值。
注3：此结果来自可靠性测试。
注4.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=10 000）时，可以对每个块执行n次擦除。例如，当对8KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。

注5.恢复时间包括重新应用暂停时切断的擦除脉冲（最多1个完整脉冲）的时间。
注6.VCC=3.3V和室温下的参考值。

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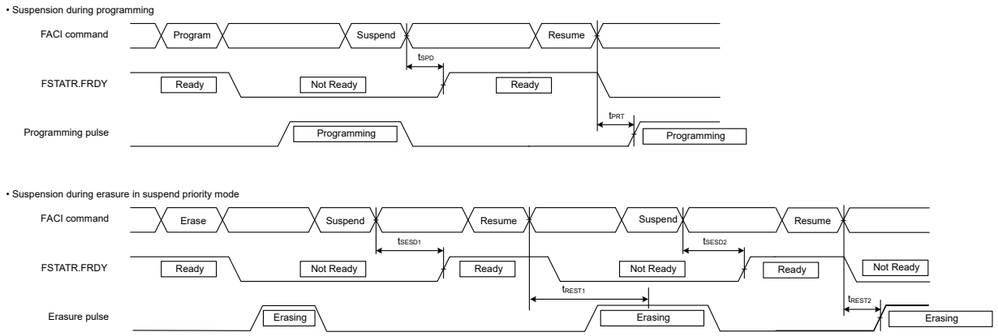


Figure 53.94 Suspension and forced stop timing for flash memory programming and erasure

53.12.2 Data Flash Memory Characteristics

Table 53.54 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

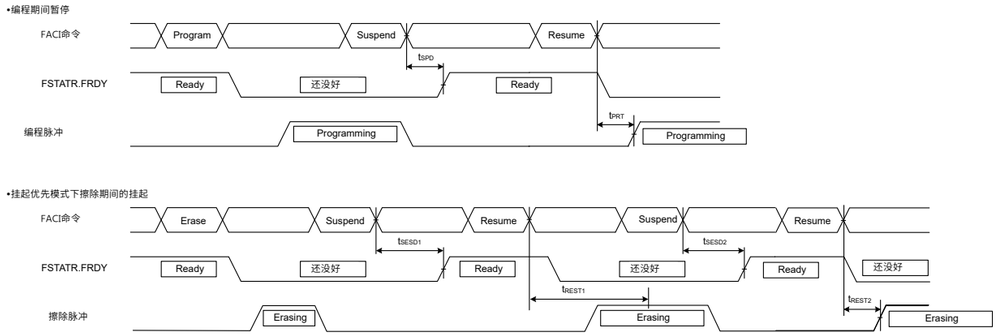


Figure 53.94 闪存编程和擦除的暂停和强制停止时序

53.12.2 数据闪存特性

Table 53.54 数据闪存特性(1of2)

条件：编程或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	典型*6最大值最小值			Typ*6	Max		
编程时间	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
擦除时间	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
空白检查时间	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	
编程期间暂停延迟	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
编程恢复时间		t_{DPRT}	—	—	110	—	—	50	µs	
挂起优先模式下擦除期间的第一个挂起延迟	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		

Table 53.54 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	μs	
Second erasing resume time during erasure in suspend priority modeFirst erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	μs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	μs	
Forced stop command		t_{FD}	—	—	32	—	—	20	μs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

53.12.3 Option Setting Memory Characteristics

Table 53.55 Option setting memory characteristics

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

Table 53.54 数据闪存特性(2of2)

条件：编程或擦除：FCLK=4至50MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
			Min	典型*6最大值最小值			Typ*6	Max		
挂起优先模式下擦除期间的第二挂起延迟	64-byte	t_{DSESD2}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
在擦除优先模式下擦除期间暂停延迟	64-byte	t_{DSEED}	—	—	300	—	—	300	μs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
挂起优先模式擦除期间的第一次擦除恢复时间*5		t_{DREST1}	—	—	300	—	—	300	μs	
挂起优先模式下擦除期间的第二次擦除恢复时间 挂起优先模式下擦除期间的第二次擦除恢复时间		t_{DREST2}	—	—	126	—	—	70	μs	
在擦除优先模式下擦除期间擦除恢复时间		t_{DREET}	—	—	126	—	—	70	μs	
强制停止命令		t_{FD}	—	—	32	—	—	20	μs	
数据保持时间*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

注1.重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=125 000）时，可以对每个块执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。禁止覆盖。
注2.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
注3.这表示在指定范围内执行重新编程时特性的最小值。
注4：此结果来自可靠性测试。
注5.恢复时间包括重新应用暂停时切断的擦除脉冲（最多1个完整脉冲）的时间。
注6.VCC=3.3V和室温下的参考值。

53.12.3 选项设置内存特性

Table 53.55 选项设置内存特性

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	测试条件
		Min	Typ*4	Max	Min	Typ*4	Max		
编程时间NOPC≤100次	t_{OP}	—	83	309	—	45	162	ms	
编程时间NOPC>100次	t_{OP}	—	100	371	—	55	195	ms	
重编程周期	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	
数据保持时间*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

注1.这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
注2.这表示在指定范围内执行重新编程时特性的最小值。
注3：此结果来自可靠性测试。
注4.VCC=3.3V和室温下的参考值。

53.13 Boundary Scan

Table 53.56 Boundary scan characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 53.95
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 53.96
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay	t_{TDOD}	—	—	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 53.97

Note 1. Boundary scan does not function until the power-on reset becomes negative.

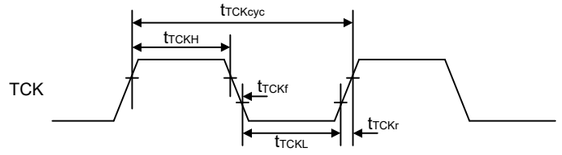


Figure 53.95 Boundary scan TCK timing

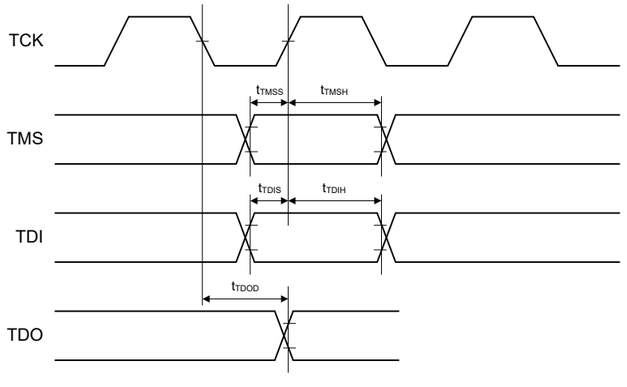


Figure 53.96 Boundary scan input/output timing

53.13 边界扫描

Table 53.56 边界扫描特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	100	—	—	ns	Figure 53.95
TCK时钟高脉冲宽度	t_{TCKH}	45	—	—	ns	
TCK时钟低脉冲宽度	t_{TCKL}	45	—	—	ns	
TCK时钟上升时间	t_{TCKr}	—	—	5	ns	
TCK时钟下降时间	t_{TCKf}	—	—	5	ns	
TMS设置时间	t_{TMSS}	20	—	—	ns	Figure 53.96
TMS保持时间	t_{TMSH}	20	—	—	ns	
TDI建立时间	t_{TDIS}	20	—	—	ns	
TDI保持时间	t_{TDIH}	20	—	—	ns	
TDO数据延迟	t_{TDOD}	—	—	40	ns	
边界扫描电路启动时间*1	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 53.97

注1.在上电复位变为负值之前，边界扫描不起作用。

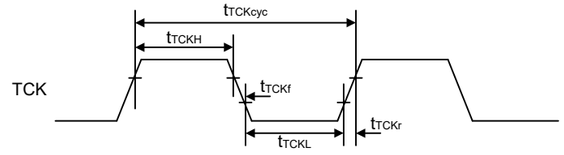


Figure 53.95 边界扫描TCK时序

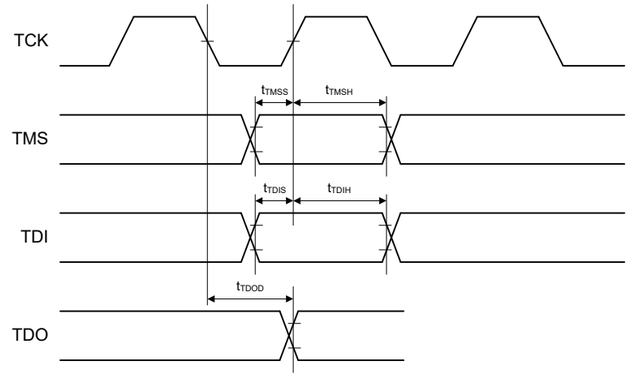


Figure 53.96 边界扫描输入输出时序

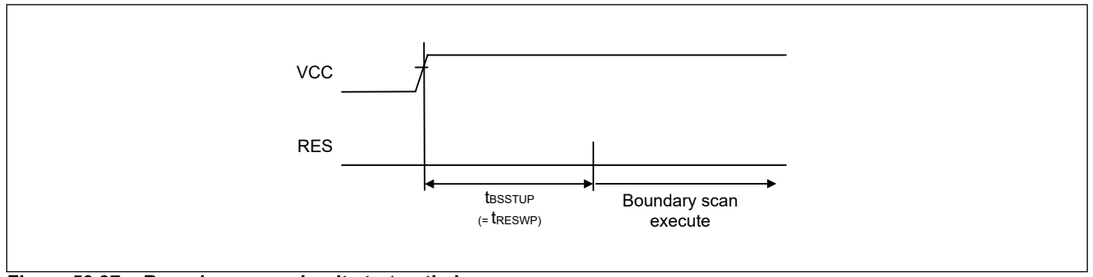


Figure 53.97 Boundary scan circuit startup timing

53.14 Joint European Test Action Group (JTAG)

Table 53.57 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	—	—	ns	Figure 53.98
TCK clock high pulse width	t_{TCKH}	15	—	—	ns	
TCK clock low pulse width	t_{TCKL}	15	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TMS setup time	t_{TMSS}	8	—	—	ns	Figure 53.99
TMS hold time	t_{TMSH}	8	—	—	ns	
TDI setup time	t_{TDIS}	8	—	—	ns	
TDI hold time	t_{TDIH}	8	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	20	ns	

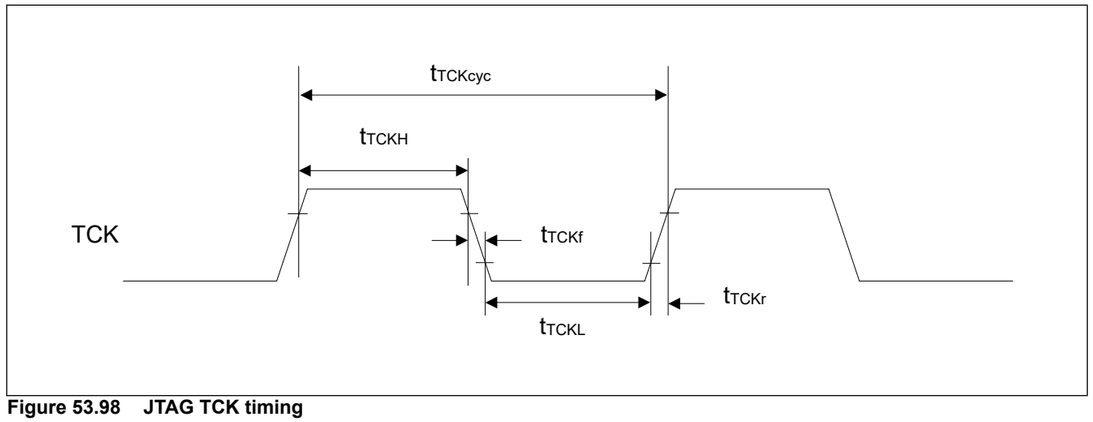


Figure 53.98 JTAG TCK timing

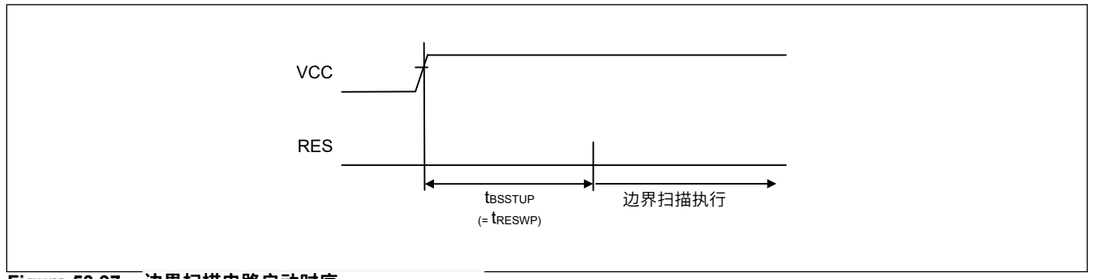


Figure 53.97 边界扫描电路启动时序

53.14 欧洲联合测试行动小组(JTAG)

Table 53.57 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	40	—	—	ns	Figure 53.98
TCK时钟高脉冲宽度	t_{TCKH}	15	—	—	ns	
TCK时钟低脉冲宽度	t_{TCKL}	15	—	—	ns	
TCK时钟上升时间	t_{TCKr}	—	—	5	ns	
TCK时钟下降时间	t_{TCKf}	—	—	5	ns	
TMS设置时间	t_{TMSS}	8	—	—	ns	Figure 53.99
TMS保持时间	t_{TMSH}	8	—	—	ns	
TDI建立时间	t_{TDIS}	8	—	—	ns	
TDI保持时间	t_{TDIH}	8	—	—	ns	
TDO数据延迟时间	t_{TDOD}	—	—	20	ns	

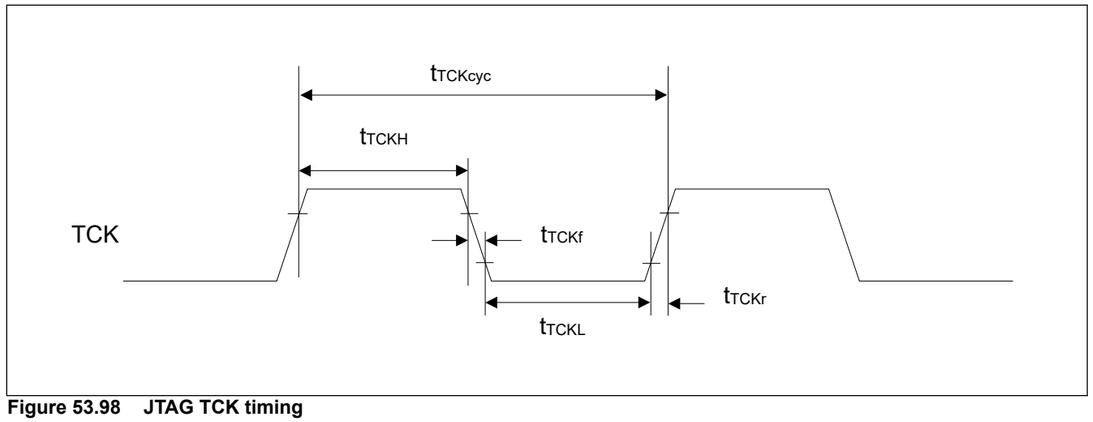


Figure 53.98 JTAG TCK timing

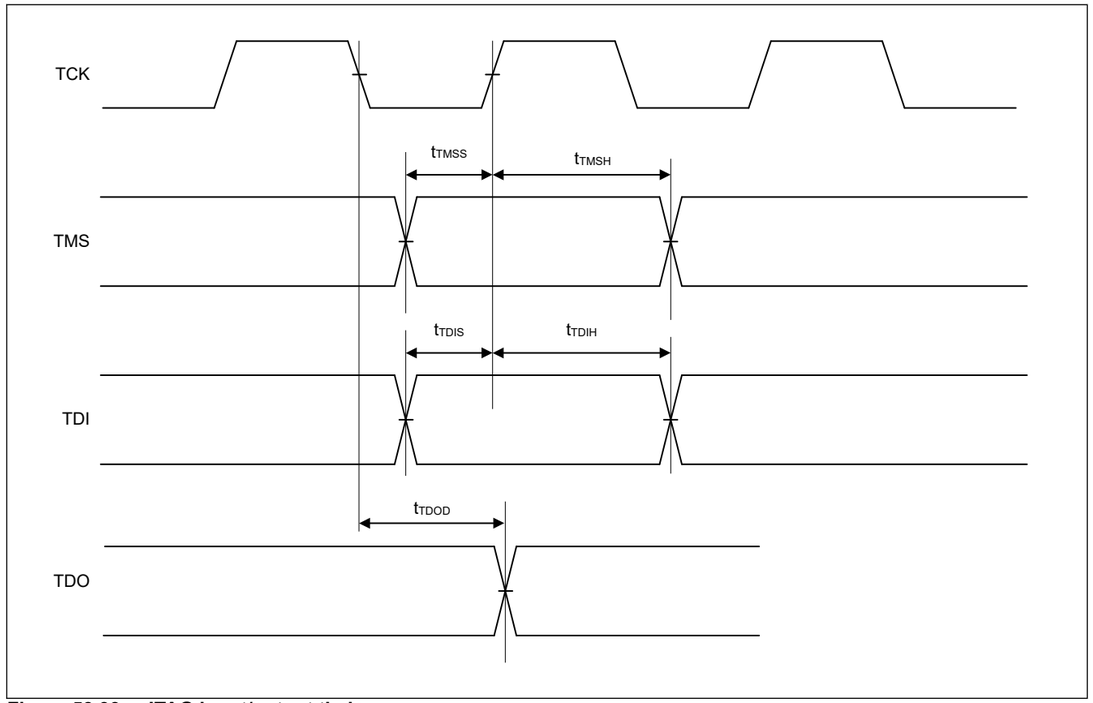


Figure 53.99 JTAG input/output timing

53.15 Serial Wire Debug (SWD)

Table 53.58 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 53.100
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 53.101
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

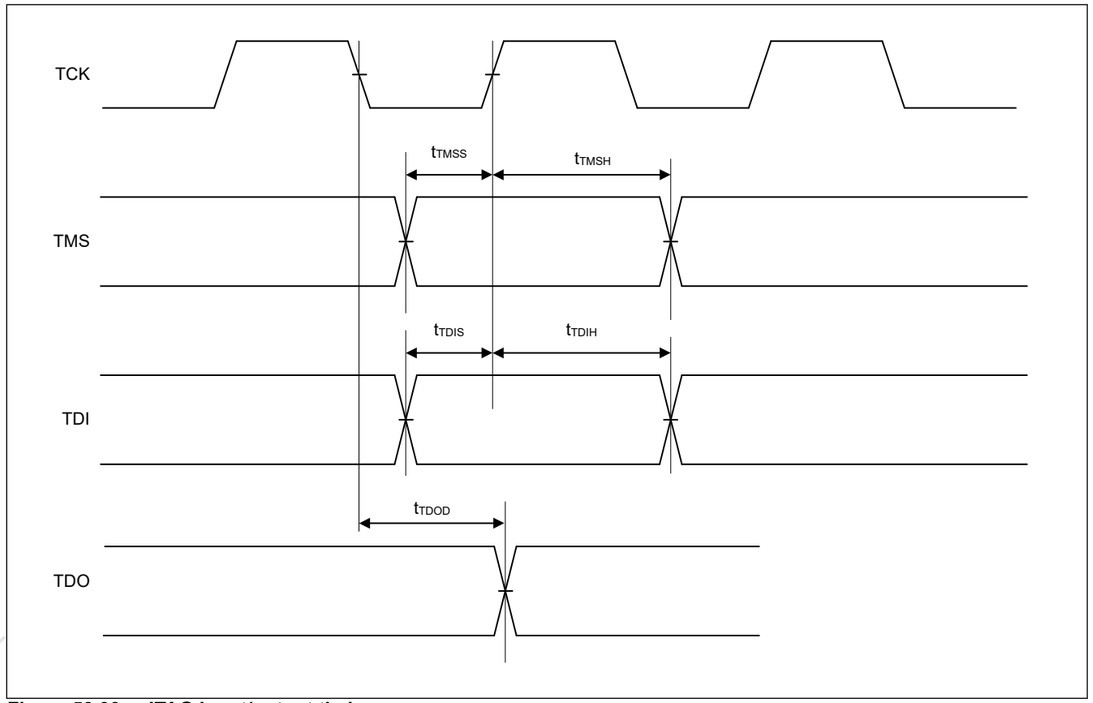


Figure 53.99 JTAG input/output timing

53.15 串行线调试(SWD)

Table 53.58 SWD

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	40	—	—	ns	Figure 53.100
SWCLK时钟高脉冲宽度	t_{SWCKH}	15	—	—	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	15	—	—	ns	
SWCLK时钟上升时间	t_{SWCKr}	—	—	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	—	—	5	ns	
SWDIO设置时间	t_{SWDS}	8	—	—	ns	Figure 53.101
SWDIO保持时间	t_{SWDH}	8	—	—	ns	
SWDIO数据延迟时间	t_{SWDD}	2	—	28	ns	

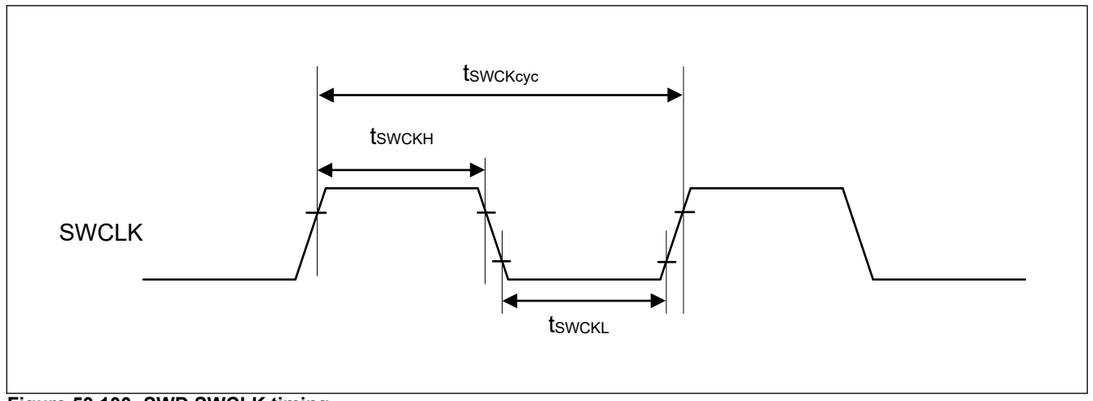


Figure 53.100 SWD SWCLK timing

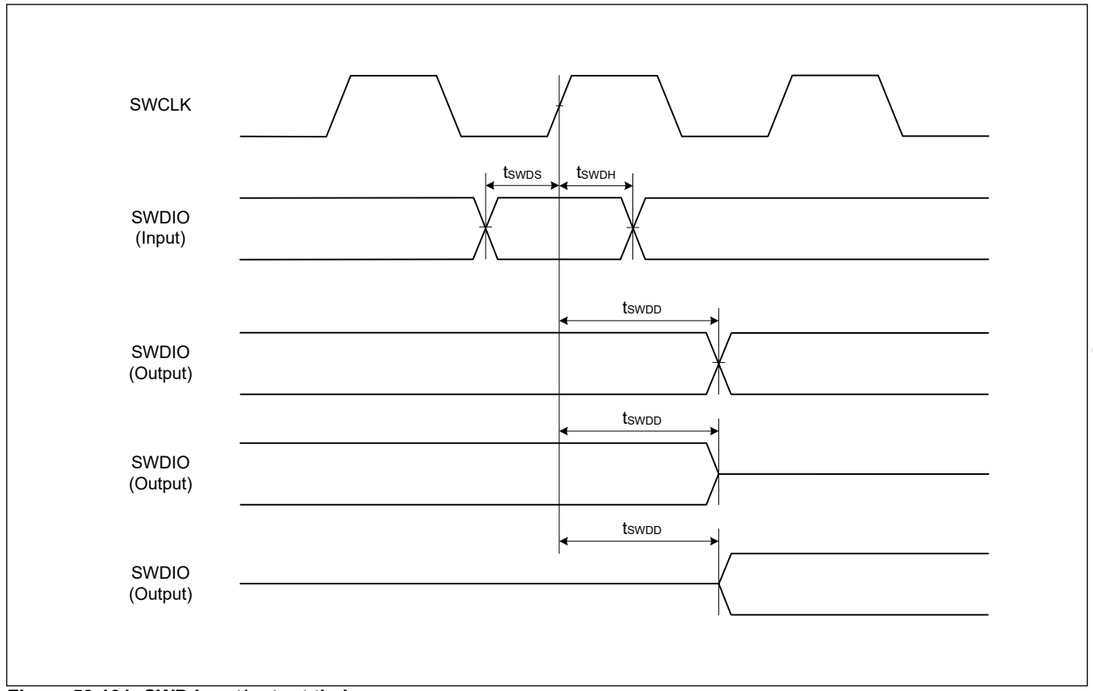


Figure 53.101 SWD input/output timing

53.16 Embedded Trace Macro Interface (ETM)

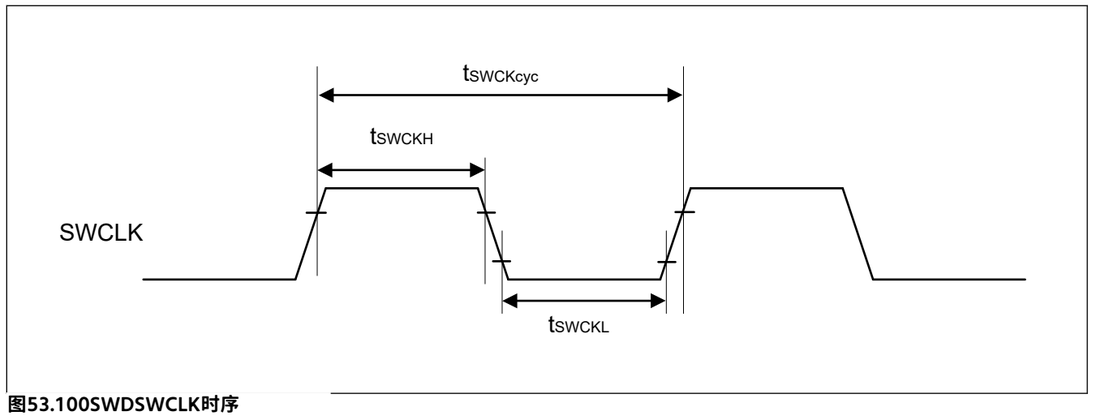


图53.100SWDSWCLK时序

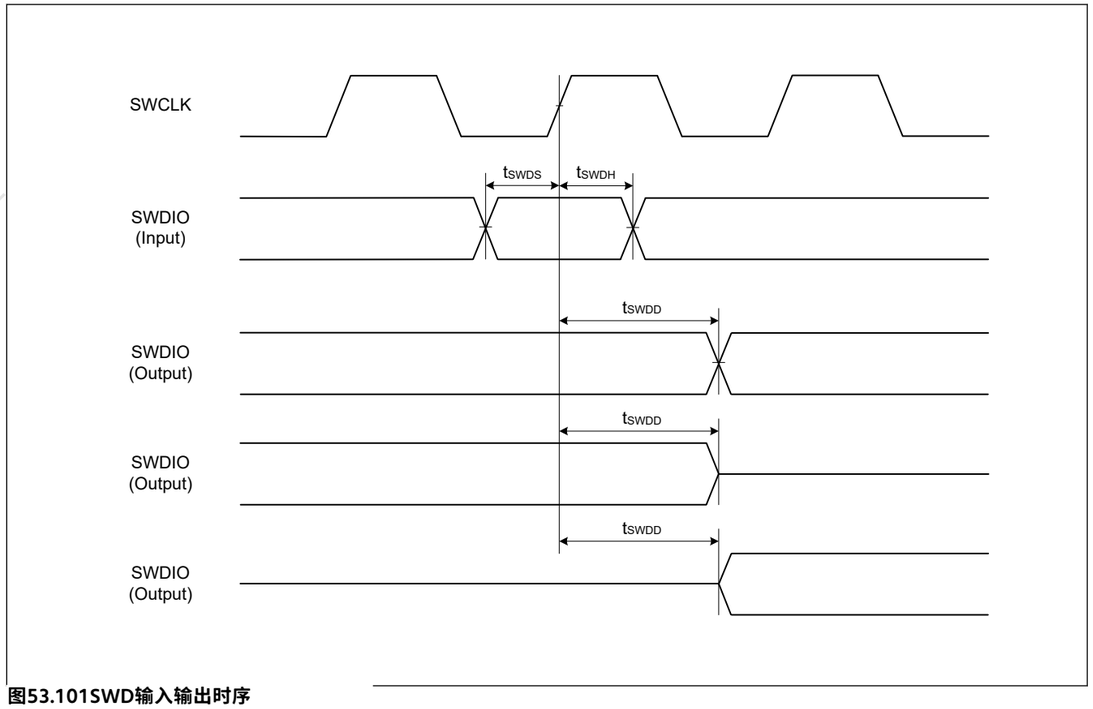


图53.101SWD输入输出时序

53.16 嵌入式跟踪宏接口(ETM)

Table 53.59 ETM

Conditions: High speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	20	—	—	ns	Figure 53.102
TCLK clock high pulse width	t_{TCLKH}	9	—	—	ns	
TCLK clock low pulse width	t_{TCLKL}	9	—	—	ns	
TCLK clock rise time	t_{TCLKr}	—	—	1	ns	
TCLK clock fall time	t_{TCLKf}	—	—	1	ns	
TDATA[3:0] output setup time	t_{TRDS}	2.5	—	—	ns	Figure 53.103
TDATA[3:0] output hold time	t_{TRDH}	1.5	—	—	ns	

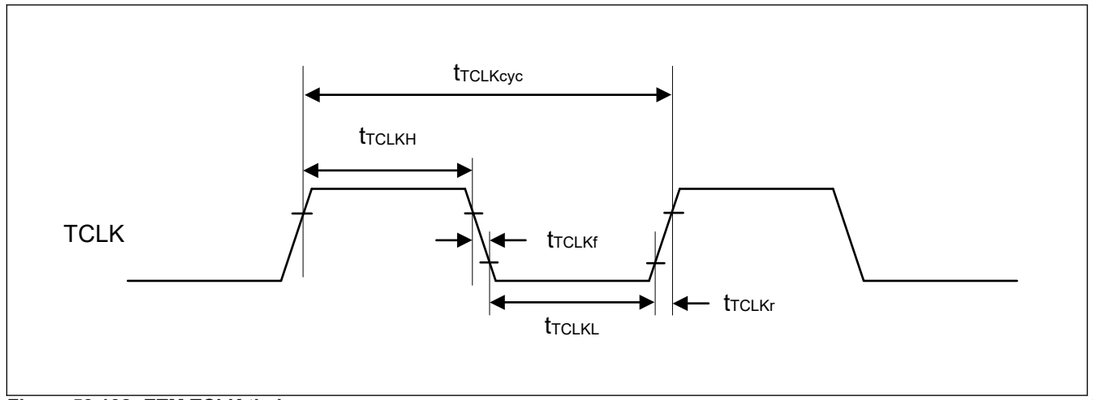


Figure 53.102 ETM TCLK timing

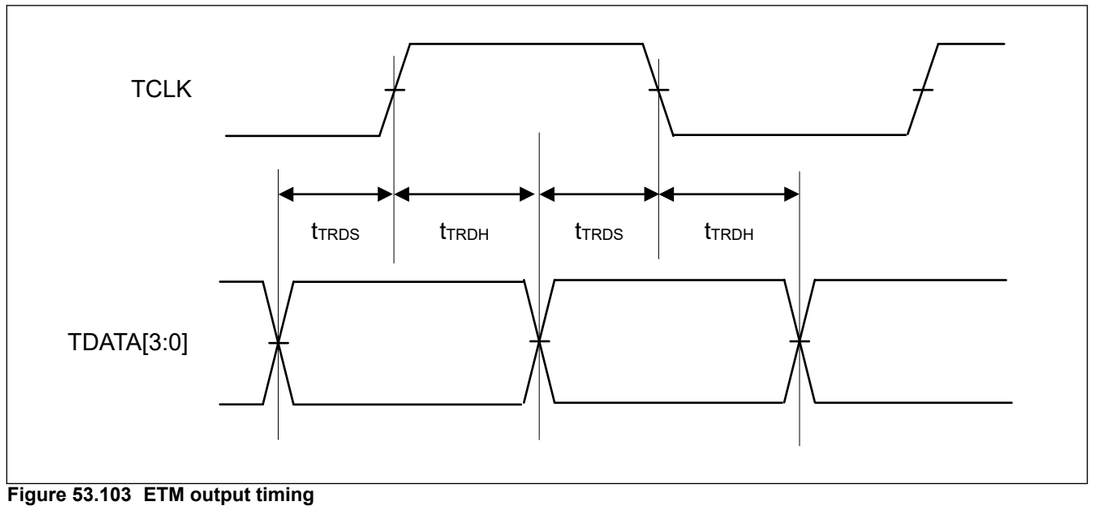


Figure 53.103 ETM output timing

Table 53.59 ETM

条件：在PmnPFS寄存器的端口驱动能力位中选择高速高驱动输出。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCLK时钟周期时间	$t_{TCLKcyc}$	20	—	—	ns	Figure 53.102
TCLK时钟高脉冲宽度	t_{TCLKH}	9	—	—	ns	
TCLK时钟低脉冲宽度	t_{TCLKL}	9	—	—	ns	
TCLK时钟上升时间	t_{TCLKr}	—	—	1	ns	
TCLK时钟下降时间	t_{TCLKf}	—	—	1	ns	
TDATA[3:0]输出建立时间	t_{TRDS}	2.5	—	—	ns	Figure 53.103
TDATA[3:0]输出保持时间	t_{TRDH}	1.5	—	—	ns	

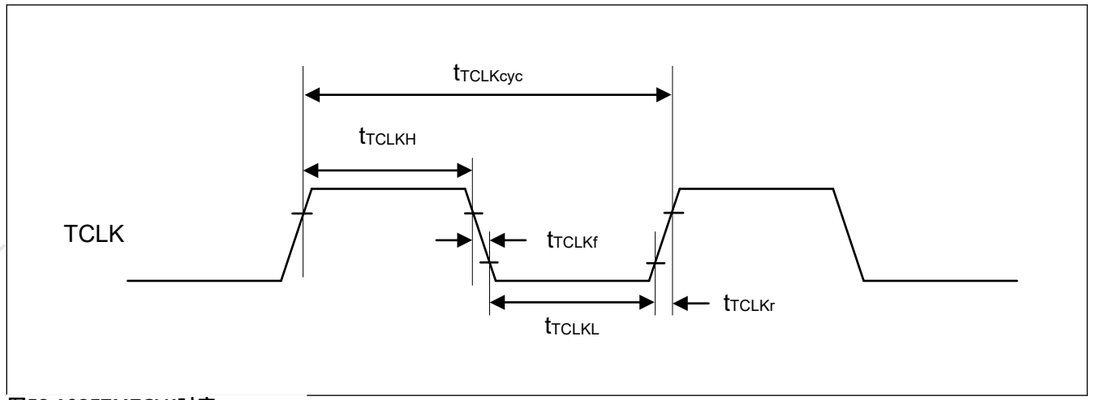


图53.102ETMTCLK时序

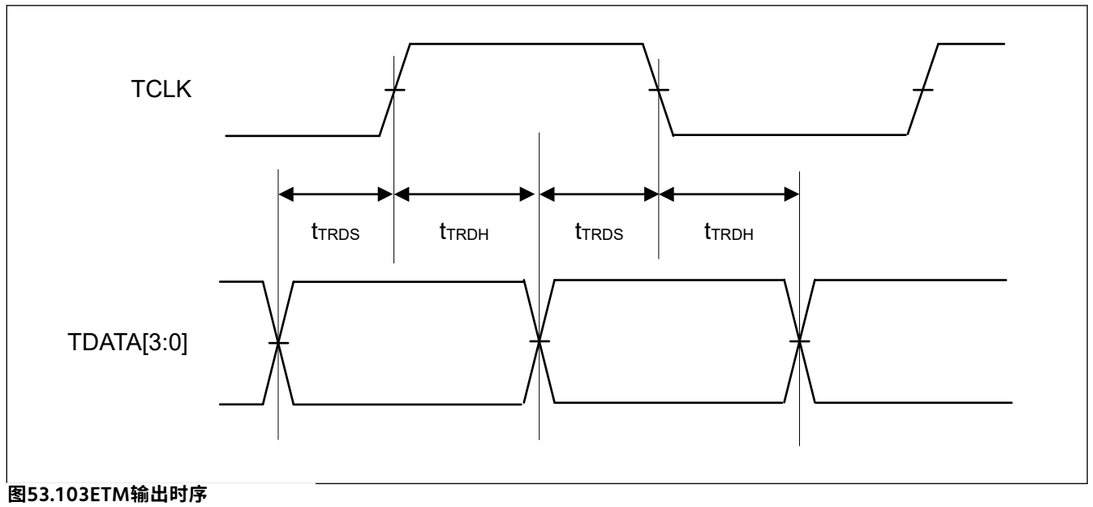


图53.103ETM输出时序

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
						IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O		Keep	Hi-Z	Keep
JTAG	TCK/TMS/TDI	Pull-up	Keep-O		Keep	Hi-Z	Keep
	TDO	output	Keep-O		Keep	TDO output	Keep
IRQ	IRQx	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
	AGTIOn (n=1,3)	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
USBFS	USB_OVRCURx	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
	USB_OVRCURx-DS/ USB_VBUS	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O*4		Keep*3	Hi-Z	Keep
USBHS	USBHS_OVRCURx/ USBHS_VBUS	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
	USBHS_DP/ USBHS_DM	Hi-Z	Keep-O*4		Keep*5	Hi-Z	Keep
RTC	RTCICx	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
	RTCOUT	Hi-Z	[RTCOUT selected] RTCOUT output		Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output		Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained		Keep	Hi-Z	Keep
External bus (CS area)	EBCLK	Hi-Z	[EBCLK output] H		Keep	Hi-Z	Keep
	Dx	Hi-Z	[Dx output] Hi-Z		Keep	Hi-Z	Keep
	Ax	Hi-Z	[Ax output] Hi-Z	[Ax output] Keep-O	Keep	Hi-Z	Keep
	BCx/CSx/RD/WRx	Hi-Z	[BCx/CSx/RD/WRx output] Hi-Z	[BCx/CSx/RD/WRx output] H	Keep	Hi-Z	Keep
	ALE	Hi-Z	[ALE output] Hi-Z	[ALE output] L	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O		Keep	Hi-Z	Keep

Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. Input is enabled while the pin is used as an input pin.
Note 5. For host operation, set the USBHS.SYSCFG.DRPD bit to 1 to enable the USBHS_DP and USBHS_DM pull-down resistors. For device operation, set the USBHS.SYSCFG.DPRPU bit to 1 to enable the DP pull-up resistor.

Appendix 1. 每种处理模式下的端口状态

Function	引脚功能	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
						IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O		Keep	Hi-Z	Keep
JTAG	TCK/TMS/TDI	Pull-up	Keep-O		Keep	Hi-Z	Keep
	TDO	output	Keep-O		Keep	TDO输出	Keep
IRQ	IRQx	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
	AGTIOn (n=1,3)	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
USBFS	USB_OVRCURx	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
	USB_OVRCURx-DS/ USB_VBUS	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O*4		Keep*3	Hi-Z	Keep
USBHS	USBHS_OVRCURx/ USBHS_VBUS	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
	USBHS_DP/ USBHS_DM	Hi-Z	Keep-O*4		Keep*5	Hi-Z	Keep
RTC	RTCICx	Hi-Z	Keep-O*2		Keep*3	Hi-Z	Keep
	RTCOUT	Hi-Z	[RTCOUT selected] RTCOUT output		Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output		Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[DAn输出(DAOE=1)]DA输出保留		Keep	Hi-Z	Keep
外部总线（CS区）	EBCLK	Hi-Z	[EBCLK output] H		Keep	Hi-Z	Keep
	Dx	Hi-Z	[Dx output] Hi-Z		Keep	Hi-Z	Keep
	Ax	Hi-Z	[Ax output] Hi-Z	[Ax output] Keep-O	Keep	Hi-Z	Keep
	BCx/CSx/RD/WRx	Hi-Z	[BCx/CSx/RD/WRx output] Hi-Z	[BCx/CSx/RD/WRx output] H	Keep	Hi-Z	Keep
	ALE	Hi-Z	[ALE output] Hi-Z	[ALE output] L	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O		Keep	Hi-Z	Keep

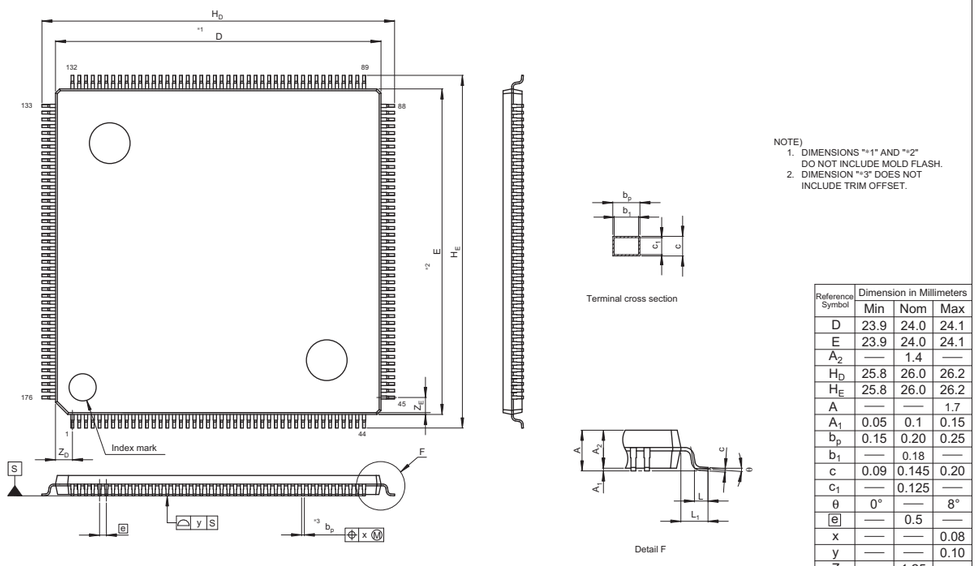
Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O：输出引脚保留其先前的值。输入引脚变为高阻抗。
保持：在软件待机模式期间保持引脚状态。

注1.保持IO端口状态直到DPSBYCR.IOKEEP位被清除为0。
注2.如果引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
注3.如果引脚被指定为深度软件待机取消源，则启用输入。
注4.当引脚用作输入引脚时，输入被启用。
注5.对于主机操作，将USBHS.SYSCFG.DRPD位设置为1以启用USBHS_DP和USBHS_DM下拉电阻。对于设备操作，将USBHS.SYSCFG.DPRPU位设置为1以启用DP上拉电阻。

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

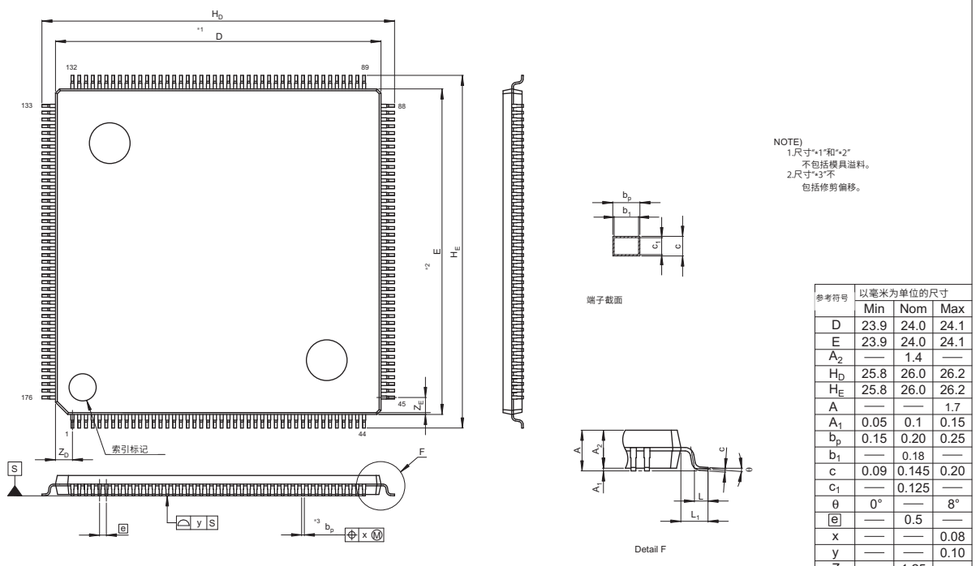
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.1 LQFP 176-pin

Appendix 2. 包装尺寸

最新版本的封装尺寸或安装信息显示在瑞萨电子的“封装”中
电子公司网站。

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g



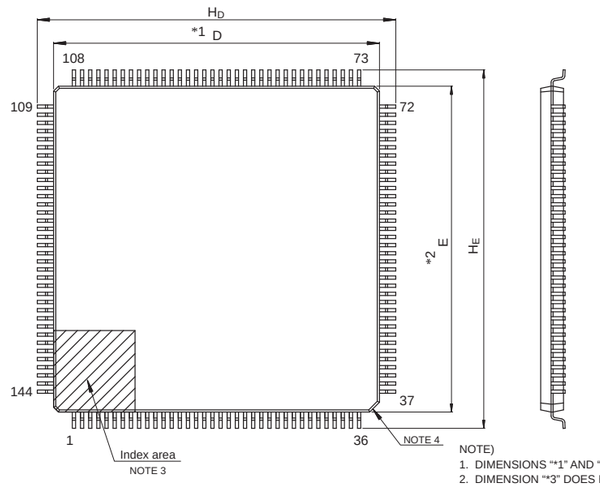
NOTE)
1.尺寸"*1"和"*2"
不包括模具溢料。
2.尺寸"*3"不
包括修剪偏移。

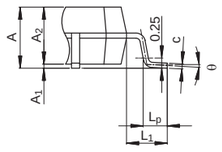
参考符号	以毫米为单位的尺寸		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.1 LQFP 176-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm





Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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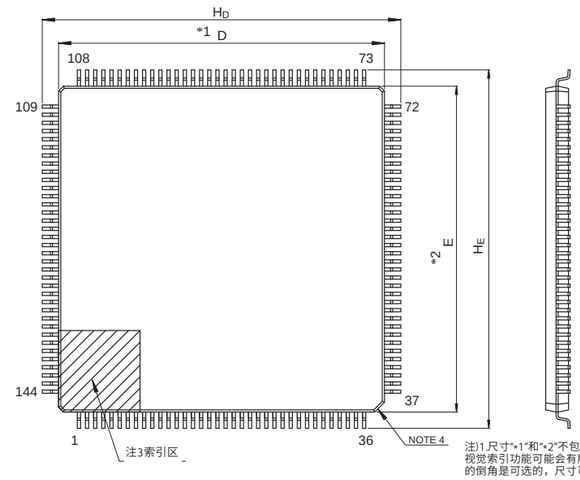
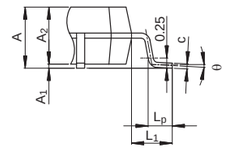
Figure 2.2 LQFP 144-pin

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。



Detail F

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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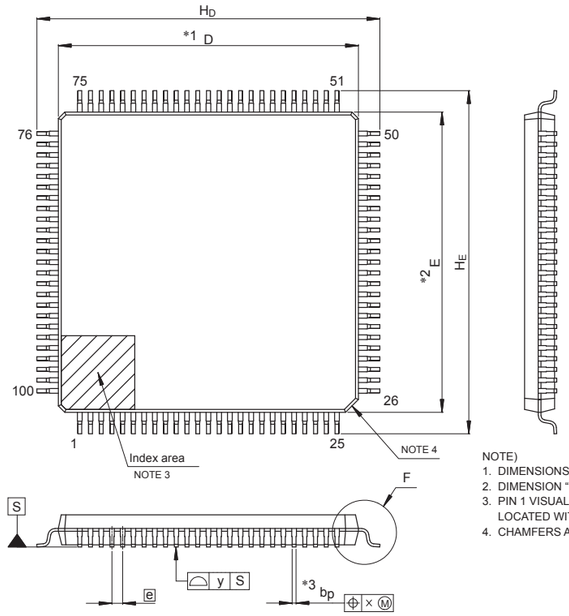
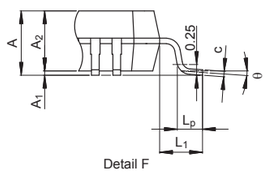
Figure 2.2 LQFP 144-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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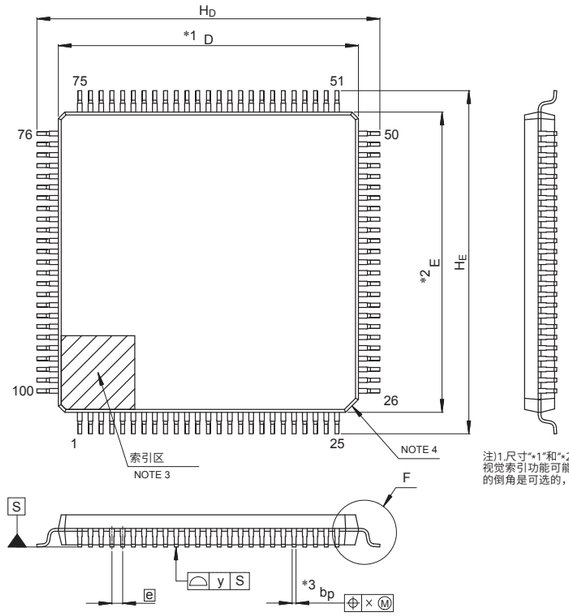
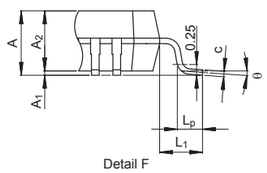
Figure 2.3 LQFP 100-pin

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm





注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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Figure 2.3 LQFP 100-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 3)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x400_1B000
FCACHE	Flash Cache	0x400_1C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4008_0000
PORT1	Port 1 Control Registers	0x4008_0020
PORT2	Port 2 Control Registers	0x4008_0040
PORT3	Port 3 Control Registers	0x4008_0060
PORT4	Port 4 Control Registers	0x4008_0080
PORT5	Port 5 Control Registers	0x4008_00A0
PORT6	Port 6 Control Registers	0x4008_00C0
PORT7	Port 7 Control Registers	0x4008_00E0
PORT8	Port 8 Control Registers	0x4008_0100
PORT9	Port9 Control Registers	0x4008_0120
PORTA	Port A Control Registers	0x4008_0140
PORTB	Port B Control Registers	0x4008_0160
PFS	Pmn Pin Function Control Register	0x4008_0800
ELC	Event Link Controller	0x4008_2000
RTC	Realtime Clock	0x4008_3000

Appendix 3. I/O Registers

本附录按功能描述了IO寄存器地址和访问周期。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of3)

Name	Description	基址
RMPU	瑞萨内存保护单元	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	总线控制	0x4000_3000
DMAC0	直接内存访问控制器0	0x4000_5000
DMAC1	直接内存访问控制器1	0x4000_5040
DMAC2	直接内存访问控制器2	0x4000_5080
DMAC3	直接内存访问控制器3	0x4000_50C0
DMAC4	直接内存访问控制器4	0x4000_5100
DMAC5	直接内存访问控制器5	0x4000_5140
DMAC6	直接内存访问控制器6	0x4000_5180
DMAC7	直接内存访问控制器7	0x4000_51C0
DMA	DMAC模块激活	0x4000_5200
DTC	数据传输控制器	0x4000_5400
ICU	中断控制器	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU系统安全控制单元	0x4000_8000
DBG	调试功能	0x400_1B000
FCACHE	闪存缓存	0x400_1C100
SYSC	系统控制	0x4001_E000
PORT0	端口0控制寄存器	0x4008_0000
PORT1	端口1控制寄存器	0x4008_0020
PORT2	端口2控制寄存器	0x4008_0040
PORT3	端口3控制寄存器	0x4008_0060
PORT4	端口4控制寄存器	0x4008_0080
PORT5	端口5控制寄存器	0x4008_00A0
PORT6	端口6控制寄存器	0x4008_00C0
PORT7	端口7控制寄存器	0x4008_00E0
PORT8	端口8控制寄存器	0x4008_0100
PORT9	端口9控制寄存器	0x4008_0120
PORTA	端口A控制寄存器	0x4008_0140
PORTB	端口B控制寄存器	0x4008_0160
PFS	Pmn引脚功能控制寄存器	0x4008_0800
ELC	事件链接控制器	0x4008_2000
RTC	实时时钟	0x4008_3000

Table 3.1 Peripheral base address (2 of 3)

Name	Description	Base address
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000
USBFS	USB 2.0 FS Module	0x4009_0000
SDHI0	SD Host Interface 0	0x4009_2000
SSIE0	Serial Sound Interface Enhanced (SSIE)	0x4009_D000
IIC0	Inter-Integrated Circuit 0	0x4009_F000
IIC0WU	Inter-Integrated Circuit 0 Wake-up Unit	0x4009_F014
IIC1	Inter-Integrated Circuit 1	0x4009_F100
IIC2	Inter-Integrated Circuit 2	0x4009_F200
OSPI	Octa Serial Peripheral Interface	0x400A_6000
CAN0	CAN0 Module	0x400A_8000
CEC	Consumer Electronics Control	0x400A_C000
CANFD	CANFD Module Control	0x400B_0000
CTSU	Capacitive Touch Sensing Unit	0x400D_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
AGT2	Low Power Asynchronous General purpose Timer 2	0x400E_8200
AGT3	Low Power Asynchronous General purpose Timer 3	0x400E_8300
AGT4	Low Power Asynchronous General purpose Timer 4	0x400E_8400
AGT5	Low Power Asynchronous General purpose Timer 5	0x400E_8500
TSN	Temperature Sensor	0x400F_3000
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
USBHS	USB 2.0 High-Speed Module	0x4011_1000
EDMAC0	DMA Controller for the Ethernet Controller Channel 0	0x4011_4000
ETHERC0	Ethernet Controller Channel 0	0x4011_4100
SCI0	Serial Communication Interface 0	0x4011_8000
SCI1	Serial Communication Interface 1	0x4011_8100
SCI2	Serial Communication Interface 2	0x4011_8200
SCI3	Serial Communication Interface 3	0x4011_8300
SCI4	Serial Communication Interface 4	0x4011_8400
SCI5	Serial Communication Interface 5	0x4011_8500
SCI6	Serial Communication Interface 6	0x4011_8600
SCI7	Serial Communication Interface 7	0x4011_8700
SCI8	Serial Communication Interface 8	0x4011_8800
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000

Table 3.1 外设基地址（2个，共3个）

Name	Description	基址
IWDT	独立看门狗定时器	0x4008_3200
WDT	看门狗定时器	0x4008_3400
CAC	时钟频率精度测量电路	0x4008_3600
MSTP	模块停止控制A、B、C、D	0x4008_4000
POEG	GPT端口输出使能模块	0x4008_A000
USBFS	USB2.0FS模块	0x4009_0000
SDHI0	SD主机接口0	0x4009_2000
SSIE0	串行声音接口增强(SSIE)	0x4009_D000
IIC0	Inter-Integrated Circuit 0	0x4009_F000
IIC0WU	内部集成电路0唤醒单元	0x4009_F014
IIC1	Inter-Integrated Circuit 1	0x4009_F100
IIC2	Inter-Integrated Circuit 2	0x4009_F200
OSPI	Octa串行外设接口	0x400A_6000
CAN0	CAN0 Module	0x400A_8000
CEC	消费电子控制	0x400A_C000
CANFD	CANFD模块控制	0x400B_0000
CTSU	电容式触控感应单元	0x400D_0000
PSCU	外围安全控制单元	0x400E_0000
AGT0	低功耗异步通用定时器0	0x400E_8000
AGT1	低功耗异步通用定时器1	0x400E_8100
AGT2	低功耗异步通用定时器2	0x400E_8200
AGT3	低功耗异步通用定时器3	0x400E_8300
AGT4	低功耗异步通用定时器4	0x400E_8400
AGT5	低功耗异步通用定时器5	0x400E_8500
TSN	温度感应器	0x400F_3000
CRC	CRC Calculator	0x4010_8000
DOC	数据运算电路	0x4010_9000
USBHS	USB2.0高速模块	0x4011_1000
EDMAC0	以太网控制器通道0的DMA控制器	0x4011_4000
ETHERC0	以太网控制器通道0	0x4011_4100
SCI0	串行通讯接口0	0x4011_8000
SCI1	串行通讯接口1	0x4011_8100
SCI2	串行通讯接口2	0x4011_8200
SCI3	串行通讯接口3	0x4011_8300
SCI4	串行通讯接口4	0x4011_8400
SCI5	串行通讯接口5	0x4011_8500
SCI6	串行通讯接口6	0x4011_8600
SCI7	串行通讯接口7	0x4011_8700
SCI8	串行通讯接口8	0x4011_8800
SCI9	串行通讯接口9	0x4011_8900
SPI0	串行外设接口0	0x4011_A000

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Table 3.1 Peripheral base address (3 of 3)

Name	Description	Base address
SPI1	Serial Peripheral Interface 1	0x4011_A100
SCE9	Secure Cryptographic Engine	0x4016_1000
GPT320	General PWM 32-Bit Timer 0	0x4016_9000
GPT321	General PWM 32-Bit Timer 1	0x4016_9100
GPT322	General PWM 32-Bit Timer 2	0x4016_9200
GPT323	General PWM 32-Bit Timer 3	0x4016_9300
GPT164	General PWM 16-Bit Timer 4	0x4016_9400
GPT165	General PWM 16-Bit Timer 5	0x4016_9500
GPT166	General PWM 16-Bit Timer 6	0x4016_9600
GPT167	General PWM 16-Bit Timer 7	0x4016_9700
GPT168	General PWM 16-Bit Timer 8	0x4016_9800
GPT169	General PWM 16-Bit Timer 9	0x4016_9900
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
ADC121	12bit A/D Converter 1	0x4017_0200
DAC12	12-bit D/A converter	0x4017_1000
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000
QSPI	Quad-SPI	0x6400_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.1 外设基地址(3of3)

Name	Description	基址
SPI1	串行外设接口1	0x4011_A100
SCE9	安全加密引擎	0x4016_1000
GPT320	通用PWM32位定时器0	0x4016_9000
GPT321	通用PWM32位定时器1	0x4016_9100
GPT322	通用PWM32位定时器2	0x4016_9200
GPT323	通用PWM32位定时器3	0x4016_9300
GPT164	通用PWM16位定时器4	0x4016_9400
GPT165	通用PWM16位定时器5	0x4016_9500
GPT166	通用PWM16位定时器6	0x4016_9600
GPT167	通用PWM16位定时器7	0x4016_9700
GPT168	通用PWM16位定时器8	0x4016_9800
GPT169	通用PWM16位定时器9	0x4016_9900
GPT_OPS	输出相位切换控制器	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
ADC121	12bit A/D Converter 1	0x4017_0200
DAC12	12-bit D/A converter	0x4017_1000
FLAD	数据闪存	0x407F_C000
FACI	Flash应用命令接口	0x407F_E000
QSPI	Quad-SPI	0x6400_0000

Note: 名称=外设名称
描述=外围功能
基地址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

●寄存器按相关模块分组。

●访问周期数是指基于指定参考时钟的周期数。

●在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作。

●IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。

●当ICLK的频率等于PCLK的频率时，分频的时钟同步周期数始终是恒定的。

●当ICLK频率大于PCLK频率时，分频时钟同步周期数至少增加1个PCLK周期。

●写访问周期数是指非缓冲写访问所获得的周期数。

Note: 这适用于当来自CPU的访问与从外部存储器获取指令或来自其他总线主控器（例如DTC或DMAC）的总线访问不冲突时的周期数。

Table 3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	Port n Control Registers, Pmn Pin Function Control Register
ELC, RTC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	Module Stop Control
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable Module for GPT
USBFS	0x4009_0000	0x4009_3FFF	6	5	3 to 6	3 to 5	PCLKB	USB 2.0 FS Module
USBFS	0x4009_4000	0x4009_4FFF	4	3	1 to 4	1 to 3	PCLKB	USB 2.0 FS Module
SDHI0, SSIE0, IICn, IIC0WU	0x4009_2000	0x4009_FFFF	5	4	2 to 5	2 to 4	PCLKB	SD Host Interface 0, Serial Sound Interface Enhanced, Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit
OSPI	0x400A_6000	0x400A_6FFF	15	17	12 to 15	15 to 17	PCLKB	Octa Serial Peripheral Interface
CANn	0x400A_8000	0x400A_9FFF	5	4	2 to 5	2 to 4	PCLKB	CANn Module
CEC	0x400A_C000	0x400A_CFFF	4	3	1 to 3	1 to 3	PCLKB	Consumer Electronics Control
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
CTSU	0x400D_0000	0x400D_FFFF	4	3	1 to 4	1 to 3	PCLKB	Capacitive Touch Sensing Unit
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
USBHS	0x4011_1000	0x4011_1FFF	(BWAIT+5)*2	(BWAIT+4)*2	(BWAIT+4)*2	(BWAIT+2) to (BWAIT +4)*2	PCLKA	USB 2.0 High-Speed Module

Table 3.2 访问周期(1of3)

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	瑞萨内存保护单元、TrustZone过滤器、SRAM控制，总线控制、直接内存访问控制器n、DMAC模块激活、DTC控制寄存器、中断控制器
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU系统安全控制单元，调试功能，闪存
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	系统控制
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	系统控制
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	端口n控制寄存器，Pmn引脚功能控制Register
ELC, RTC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	事件链接控制器，实时时钟，独立看门狗定时器，看门狗定时器，时钟频率Accuracy测量电路
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	模块停止控制
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	端口输出使能GPT模块
USBFS	0x4009_0000	0x4009_3FFF	6	5	3 to 6	3 to 5	PCLKB	USB2.0FS模块
USBFS	0x4009_4000	0x4009_4FFF	4	3	1 to 4	1 to 3	PCLKB	USB2.0FS模块
SDHI0, SSIE0, IICn, IIC0WU	0x4009_2000	0x4009_FFFF	5	4	2 to 5	2 to 4	PCLKB	SD主机接口0，串行声音接口增强型，国米集成电路n内部集成电路0唤醒单元
OSPI	0x400A_6000	0x400A_6FFF	15	17	12 to 15	15 to 17	PCLKB	Octa串行外设Interface
CANn	0x400A_8000	0x400A_9FFF	5	4	2 to 5	2 to 4	PCLKB	CANn模块
CEC	0x400A_C000	0x400A_CFFF	4	3	1 to 3	1 to 3	PCLKB	消费类电子产品Control
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
CTSU	0x400D_0000	0x400D_FFFF	4	3	1 to 4	1 to 3	PCLKB	Capacitive Touch传感单元
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	外围安全控制单元
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	低电量Asynchronous一般用途Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	温度感应器
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC计算器，数据运算电路
USBHS	0x4011_1000	0x4011_1FFF	(BWAIT+5)*2	(BWAIT+4)*2	(BWAIT+4)*2	(BWAIT+2) to (BWAIT +4)*2	PCLKA	USB 2.0 High-Speed Module

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Table 3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
EDMAC0	0x4011_4000	0x4011_40FF	6	5	3 to 6	3 to 5	PCLKA	DMA Controller for the Ethernet Controller Channel 0
ETHERC0	0x4011_4100	0x4011_4FFF	15	14	12 to 15	12 to 14	PCLKA	Ethernet Controller Channel 0
SCIn	0x4011_8000	0x4011_8FFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*4	4*4	2 to 5*4	2 to 4*4	PCLKA	Serial Peripheral Interface n
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module
SCE9	0x4016_1000	0x4016_1FFF	6	4	3 to 6	2 to 4	PCLKA	Secure Cryptographic Engine
GPT32n, GPT16n, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter
QSPI	0x6400_0000	0x6400_000F	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0010	0x6400_0013	25 to *5	6 to *5	25 to *5	5 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	4	3	1 to 4	1 to 3	PCLKA	Quad-SPI

Table 3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.
Note 2. BWAIT is the number of waits (not cycles) described in the USBHS.BUSWAIT register.
Note 3. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 4. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.
Note 5. The access cycles depend on the QSPI bus cycles.

Table 3.2 访问周期（2个，共3个）

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
EDMAC0	0x4011_4000	0x4011_40FF	6	5	3 to 6	3 to 5	PCLKA	DMA控制器 以太网控制器 Channel 0
ETHERC0	0x4011_4100	0x4011_4FFF	15	14	12 to 15	12 to 14	PCLKA	以太网控制器 Channel 0
SCIn	0x4011_8000	0x4011_8FFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	串行通信 Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*4	4*4	2 to 5*4	2 to 4*4	PCLKA	串行外设 Interface n
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module
SCE9	0x4016_1000	0x4016_1FFF	6	4	3 to 6	2 to 4	PCLKA	安全密码学 Engine
GPT32n, GPT16n, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	通用PWM32位定时器n，通用 PWM16位定时器n，输出相位 开关控制器
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter
QSPI	0x6400_0000	0x6400_000F	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0010	0x6400_0013	25 to *5	6 to *5	25 to *5	5 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	4	3	1 to 4	1 to 3	PCLKA	Quad-SPI

Table 3.2 访问周期（3个，共3个）

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = FCLK		ICLK > FCLK*1			
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	数据闪存、闪存 应用命令 Interface

注1.若PCLK或FCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2。5是1到3。

注2.BWAIT是USBHS.BUSWAIT寄存器中描述的等待数（不是周期数）。
注3.访问16位寄存器（FTDRHL、FRDRHL、FCR、FDR、LSR和CDR）时，访问比中所示的值多2个周期
表3.2。访问8位寄存器（包括FTDRH、FTDRL、FRRDH和FRDRL）时，访问周期如下图所示：
Table 3.2.
注4.访问32位寄存器(SPDR)时，访问比表3.2中的值多2个周期。访问8位或16位寄存器（SPDR_HA）时，访问周期如表3.2所示。

注5.访问周期取决于QSPI总线周期。

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